MOSEL - VITELIC

Memory Data Book

1993-1994

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VITELIC

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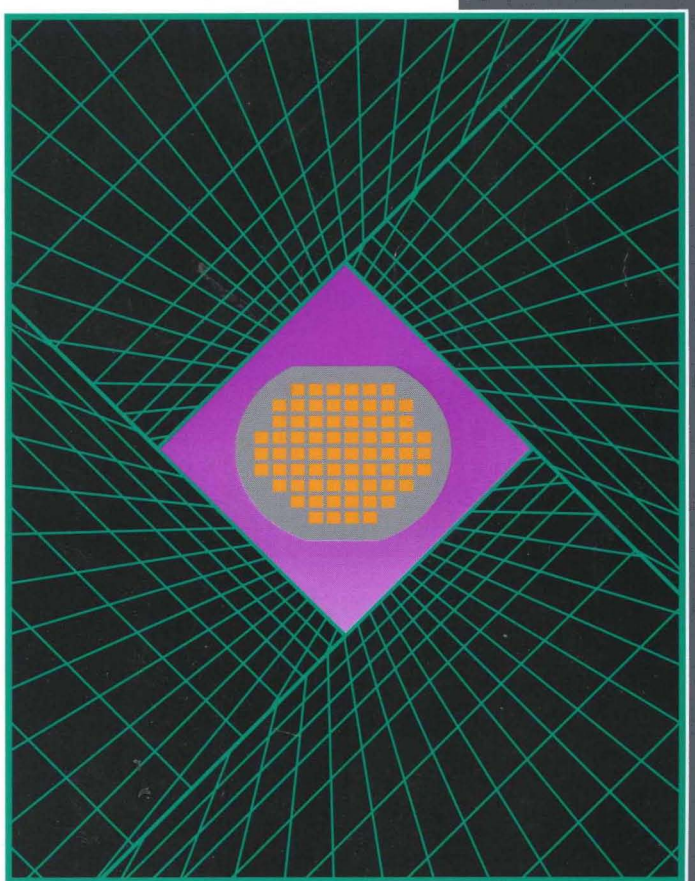

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MOSEL-VITELIC INC.

1993/94 DATA BOOK

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The Mosel-Vitelic memory data book is organized by product families, beginning with general information on the company and products. The products begin with dynamic RAMs, then video RAMs, DRAM modules, high speed static RAMs, standard static RAMS, FIFOs, and specialty products. Within each section, data sheets are arranged in order of densities except FIFOs and specialty products. Application Notes and Package Dimensions then follow and finally the Mosel-Vitelic Sales Network.

LIFE SUPPORT POLICY

Mosel-Vitelic products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of Mosel-Vitelic Corporation.

1. Life support devices or systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

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MOSEL-VITELIC Corporation designs, develops, manufactures, and markets high performance and application specific memory products. The company was merged from MOS Electronics Corporation and Vitelic Corporation in 1991. Headquarters of the company is located in Science Based Industrial Park, Taiwan with subsidiaries in USA, Japan, and Hong Kong.

MOSEL-VITELIC currently offers a wide range of products including high speed and standard SRAMs, DRAMs, Video RAMs, SIMMs, and application specific memories.

One of MOSEL-VITELIC's major strengths is its design engineering capability—a combination of many man-years of experience in memory circuit development and advanced computer-based tools for efficient design methodology. Current CAD tools allow product to be designed in a few weeks compared to man-years required previously. Talented designers, working with variations on a basic schematic, can now bring a variety of complex feature-intensive products through the design stage far more rapidly than before. New effective design verification tools translate to a high probability of working silicon on the first wafer run.

MOSEL-VITELIC's memory products employ proprietary high speed, low power designs with the state-of-the-art CMOS technology. The technology uses CMOS for low power consumption, multi-layer poly-silicon and two layers of metal interconnect for high packing density, and gate lengths of the sub-micron level for high speed performance. In addition, MOSEL-VITELIC uses the most advanced state-of-the art CMOS manufacturing facilities to ensure a high level of performance and reliability. Advanced circuit design techniques and process technology are used to provide high degrees of ESD protection and latch-up immunity.

MOSEL-VITELIC is able to exploit its advanced design capability and its high performance process capability through its partnerships with major semiconductor corporations who are equipped with highly automated and ultra-clean manufacturing facilities. In most cases these are manufacturing, licensing and joint development relationships. MOSEL-VITELIC gains enhanced production capability and access to domestic markets in Europe and the Far East through these alliances.

In addition, MOSEL-VITELIC is building its own 0.4–0.6 micron fab in the Science Based Industrial Park, Taiwan. This wafer fabrication facility will be used primarily for the introduction of new products. The company intends to maintain and increase its manufacturing alliances to complement this in-house production capability.

MOSEL-VITELIC is committed to serving the needs of the high performance, application specific memory market with extremely reliable, thoroughly tested, high quality products. Quality starts at the design stage by building in extra performance margins and is enhanced through each stage of the manufacturing process to timely customer deliveries. MOSEL-VITELIC works closely with its customers to build in the application specific memory features and functions required to produce leading edge computer systems.

MOSEL-VITELIC PRODUCT SELECTION GUIDE

DRAMS

Part Number	Description	Speeds (ns)	Package(s)	I_{CC} Max. (mA)	I_{CCSB} Max. (mA)	Availability
V53C256A	256K x 1 DRAM	70,80,100	J,P	60	1.2	Now
V53C464A/466A	64K x4 DRAM	70,80,100	J,P	65	0.2	Now
V53C864	64K x 8 DRAM	70,80,100	K,P	65	1	Now
V53C100F	1 Meg x 1 DRAM	60,70,80	K,P	90/80/70	2	Now
V53C100H	1 Meg x 1 DRAM	45,50,55,60	K,P	110/100/90/85	0.15	Now
V53C100N	1 Meg x 1 DRAM – 3.3V	60,70,80	K,P	45/40/35	0.04	Now
V53C104F	256K x 4 DRAM	60,70,80	K,P	90/80/70	2	Now
V53C104H	256K x 4 DRAM	45,50,55,60	K,P	110/100/90/85	0 15	Now
V53C104N	256K x 4 DRAM – 3.3V	60,70,80	K,P	45/40/35	0.04	Now
V53C664	64K x 16 DRAM	80,100	K	115/90	1	Now
V53C8256H	256K x 8 DRAM	45,50,60	K,P	160/150/ 145/135	0.8	Now
V53C8256N	256K x 8 DRAM – 3.3V	60,70,80	K,P	65/60/55	1	Now
V53C8512	512K x 8 DRAM	50,60,70	K	120/110/105	1	Q4 '93
V53C9512	512K x 9 DRAM	50,60,70	K	120/110/105	1	Q4 '93
V53C400	4 Meg x 1 DRAM	60,70,80,100	K	100/90/80/70	1	Now
V53C404	1 Meg x 4 DRAM	60,70,80,100	K	100/90/80/70	1	Now

MEMORY MODULES

Part Number	Description	Speeds (ns)	Package(s)	I_{CC} Max. (mA)	I_{CCSB} Max. (mA)	Availability
V104J8	256K x 8 SIMM (2 chips)	60,70,80	S	130	2	Now
V100J8	1 Meg x 8 SIMM (8 chips)	60,70,80	S	480	8	Now
V404J8	1 Meg x 8 SIMM (2 chips)	70,80	S	140	2	Now
V400J8	4 Meg x 8 SIMM (8 chips)	70,80	S	560	8	Now
V1 04J9	256K x 9 SIMM (3 chips)	70,80	S	160	4	Now
V100J9	1 Meg x 9SIMM (9 chips)	60.70,80	S	540	9	Now
V404J9	1 Meg x 9 SIMM (3 chips)	70,80	S	240	3	Now
V400J9	4 Meg x 9 SIMM (9 chips)	70,80	S	660	13	Now
V104J36	256K x 36 SIMM (12 chips)	70,80	S	760	12.8	Now
V104J236	512K x 36 SIMM (24 chips)	70,80	S	1320	24	Now
V404J36	1 Meg x 36 SIMM (12 chips)	70,80	S	900	12	Now

VIDEO RAMS

Part Number	Description	Speeds (ns)	Package(s)	I_{CC} Max. (mA)	I_{CCSB} Max. (mA)	Availability
V53C261	64K x 4 Video RAM	100,120	K,P,Z	60/50	6	Now
V52C4256/8	256K x 4 Video RAM	60,70,80,100	K,Z	95/85/75/65	7	Now
V52C8126/8	128K x 8 Video RAM	70,80,100	K,Z	90/80/70	7	Now
V52C8254	256K x 8 Video RAM	60,70,80	K	95/85/75	8	Q4 '93
V52C8255/6	256K x 8 Video RAM	60,70,80	K	95/85/75	8	Q4 '93
V52C8258	256K x 8 Video RAM	60,70,80	K	135/105	10	Q4 '93

HIGH SPEED STATIC RAMS

Part Number	Description	Speeds (ns)	Package(s)	I_{CC} Max. (mA)	I_{CCSB} Max. (mA)	Availability
MS6264A	8K x 8 SRAM	20,25,35	N,R	150	0.1/3	Now
MS62256A	32K x 8 SRAM	20,25,35,45	N,R	180	10	Now
MS62256H	32K x 8 SRAM	15,20,25,35	N,R	200	40	Q3 '93
MS621002	256K x 4 SRAM	20,25,35	K	130	1	Now
MS621008	128K x 8 SRAM	20,25,35	E,K	150	2	Now

STANDARD STATIC RAMS

Part Number	Description	Speeds (ns)	Package(s)	I_{CC} Max. (mA)	I_{CCSB} Max. (mA)	Availability
MS6516	2K x 8 SRAM	100	P,S	70	0.01	Now
MS6264	8K x 8 SRAM	70,100	F,P	85	0.1	Now
MS6264N	8K x 8 SRAM – 3.3V	100	F,P	50	0.1	Now
MS6265	8K x8 SRAM – Low Power	100	F,N,P	40	0.01	Now
MS62256	32K x 8 SRAM	100	N,F,P	70	0.1	Now
		70	N,F,P	80	0.1	Now
MS62256C	32K x 8 SRAM Low Low Power	70,100	F,N,P	80	0.02	Now
MS62256N	32K x 8 SRAM – 3.3V	70,100	S,R	60	0.1	Now
MS628128	128K x 8 SRAM	80,100,120	F,P	80	3	Q4 '93

FIFOS

Part Number	Description	Speeds (ns)	Package(s)	I_{CC} Max. (mA)	I_{CCSB} Max. (mA)	Availability
MS7200	256 x 9 FIFO	25,35	F,J,N,P	125	0.5	Now
MS7201A	512 x 9 FIFO					
MS7202A	1 K x 9 FIFO	50,80	F,J,N,P	80	0.5	
MS7203	2K x 9 FIFO	50,80	F,J,N,P	125	2	Now
		20,25,35	J,N,P	125	2	Now
MS7204	4K x 9 FIFO	50,80	F,J,N,P	125	2	Now
		20,25,35	J,P	125	2	Now
MS76215	512 x 18 Synchronous FIFO	20,25,30	G,J	200	—	Now
MS76225	1K x 18 Synchronous FIFO					
MS76500A	64 x 16 Bi-Directional FIFO	25,30	J	75		Now
MS76502A	256 x 16 Bi-Directional FIFO	25,30	J	75		Now
MS76542	256 x 36 x 2 Bi-Directional FIFO	25,30,35	G,Q	180	1	Now

FUJITSU	MOSEL-VITELIC
MB81258	V53C258
MB81C1000A	V53C100F
MB81C4256A	V53C104F
MB814100	V53C400F
MB814400	V53C404F
MB81461	V53C261
GOLDSTAR	**MOSEL-VITELIC**
GM71256	V53C256
GM71C1000	V53C100F
GM71C4256A	V53C104F
HITACHI	**MOSEL-VITELIC**
HM51256	V53C256
HM51258	V53C258
HM511001	V53C100F
HM514256	V53C104F
HM514100	V53C400F
HM514400	V53C404F
HM53461	V53C261
HM53235	V52C4256
HM53251	V52C4258
HM538121	V52C8126
HM538123	V52C8128
HYUNDAI	**MOSEL-VITELIC**
HY53C256	V53C256
HY51C1000	V53C100F
HY51C4256	V53C104F
MICRON	**MOSEL-VITELIC**
MT1259	V53C256
MT4C1024	V53C100F
MT4C256	V53C104F
MT4C1004	V53C400F
MT4C4001	V53C404F
MT4C4064	V53C261
MITSUBISHI	**MOSEL-VITELIC**
M5M4257AP	V53C256
M5M41000B	V53C100F
M5M44256	V53C104F
M5M44100	V53C400F
M5M4400	V53C404F
M5M4C264	V53C261
MOTOROLA	**MOSEL-VITELIC**
MCM6257B	V53C256
MCM511000A	V53C100F
MCM514256A	V53C104F
MCM514100	V53C400F
MCM514400	V53C404F
NEC	**MOSEL-VITELIC**
µPD41256	V53C256
µPD421000	V53C100F
µPD424256	V53C104F
µPD424100	V53C400F
µPD424400	V53C404F
µPD41264	V53C261
OKI	**MOSEL-VITELIC**
MSM41256A	V53C256
MSM511000	V53C100F
MSM514256	V53C104F
MSM514100	V53C400F
MSM514400	V53C404F
SAMSUNG	**MOSEL-VITELIC**
KM41C256A	V53C256
KM41C1000	V53C100F
KM44C256A	V53C104F
KM41C4000	V53C400F
KM44C1000	V53C404F
SHARP	**MOSEL-VITELIC**
LH21256	V53C256
LH64256	V53C104F
SIEMENS	**MOSEL-VITELIC**
HYB414257	V53C256
HYB511000	V53C100F
HYB514256	V53C104F
HYB514100	V53C400F
HYB514400	V53C404F
TI	**MOSEL-VITELIC**
TMS1259	V53C256
TMS4C1024	V53C100F
TMS44C256	V53C104F
TMS44100	V53C400F
TMS44400	V53C404F
TMS4461	V53C261
TOSHIBA	**MOSEL-VITELIC**
TC511259	V53C256
TC511000	V53C100F
TC514256	V53C104F
TC514100	V53C400F
TC514400	V53C404F

Function 256K x 4 VRAM	Mosel-Vitelic V52C4256	Hitachi HM53235
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)		
BW New Mask		
BW Old Mask		
Flash Write New Mask		X
Load Mask Register		
Load Color Register		
Read Trans/Serial Out	X	X
Split Read Trans		
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans		
Mask Write Trans/Serial In		

Function 128K x 8 VRAM	Mosel-Vitelic V52C8128	Hitachi HM538123
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)	X	
BW New Mask	X	
BW Old Mask		
Flash Write New Mask	X	X
Load Mask Register		
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans	X	
Mask Write Trans/Serial In	X	

Function 256K x 4 VRAM	Mosel-Vitelic V52C4258	Hitachi HM53251
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)	X	
BW New Mask	X	
BW Old Mask		
Flash Write New Mask	X	
Load Mask Register		
Load Color Register	X	
Read Trans/Serial Out	X	X
Split Read Trans	X	
Write Trans/Serial In		X
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans	X	
Mask Write Trans/Serial In	X	

Function 256K x 4 VRAM	Mosel-Vitelic V52C4256	Micron MT42C4255
R/W New Mask	X	X
R/W Old Mask		X
Block Write (BW)		
BW New Mask		
BW Old Mask		
Flash Write New Mask		
Load Mask Register		X
Load Color Register		
Read Trans/Serial Out	X	X
Split Read Trans		X
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		X
Split Write Trans		
Mask Write Trans/Serial In		

Function 128K x 8 VRAM	Mosel-Vitelic V52C8126	Hitachi HM538121
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)		
BW New Mask		
BW Old Mask		
Flash Write New Mask		
Load Mask Register		
Load Color Register		
Read Trans/Serial Out	X	X
Split Read Trans		
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans		
Mask Write Trans/Serial In		

Function 256K x 4 VRAM	Mosel-Vitelic V52C4258	Micron MT42C4256
R/W New Mask	X	X
R/W Old Mask		X
Block Write (BW)	X	X
BW New Mask	X	X
BW Old Mask		X
Flash Write New Mask	X	
Load Mask Register		X
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	X
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		X
Split Write Trans	X	
Mask Write Trans/Serial In	X	

Function 128K x 8 VRAM	Mosel-Vitelic V52C8126	Micron MT42C8127
R/W New Mask	X	X
R/W Old Mask		X
Block Write (BW)		
BW New Mask		
BW Old Mask		
Flash Write New Mask		
Load Mask Register		X
Load Color Register		
Read Trans/Serial Out	X	X
Split Read Trans		X
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		X
Split Write Trans		
Mask Write Trans/Serial In		

Function 128K x 8 VRAM	Mosel-Vitelic V52C8128	Mitsubishi M5M482128
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)	X	X
BW New Mask	X	X
BW Old Mask		
Flash Write New Mask	X	X
Load Mask Register		
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	X
Write Trans/Serial In	X	
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans	X	X
Mask Write Trans/Serial In	X	X

Function 128K x 8 VRAM	Mosel-Vitelic V52C8128	Micron MT42C8128
R/W New Mask	X	X
R/W Old Mask		X
Block Write (BW)	X	X
BW New Mask	X	X
BW Old Mask		X
Flash Write New Mask	X	
Load Mask Register		X
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	X
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		X
Split Write Trans	X	
Mask Write Trans/Serial In	X	

Function 256K x 4 VRAM	Mosel-Vitelic V52C4256	NEC μPD524273
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)		
BW New Mask		
BW Old Mask		
Flash Write New Mask		
Load Mask Register		
Load Color Register		
Read Trans/Serial Out	X	X
Split Read Trans		
Write Trans/Serial In	X	
Pseudo Write Trans	X	
Alternate Write Trans		
Split Write Trans		
Mask Write Trans/Serial In		

Function 256K x 4 VRAM	Mosel-Vitelic V52C4258	Mitsubishi M5M44256
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)	X	X
BW New Mask	X	X
BW Old Mask		
Flash Write New Mask	X	X
Load Mask Register		
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	X
Write Trans/Serial In	X	
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans	X	X
Mask Write Trans/Serial In	X	X

Function 256K x 4 VRAM	Mosel-Vitelic V52C4258	NEC μPD524256
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)	X	
BW New Mask	X	
BW Old Mask		
Flash Write New Mask	X	X
Load Mask Register		
Load Color Register	X	
Read Trans/Serial Out	X	
Split Read Trans	X	
Write Trans/Serial In	X	X
Pseudo Write Trans	X	
Alternate Write Trans		
Split Write Trans	X	
Mask Write Trans/Serial In	X	

Function 128K x 8 VRAM	Mosel-Vitelic V52C8128	NEC μPD42275
R/W New Mask	X	X
R/W Old Mask		X
Block Write (BW)	X	X
BW New Mask	X	X
BW Old Mask		X
Flash Write New Mask	X	X
Load Mask Register		X
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	X
Write Trans/Serial In	X	
Pseudo Write Trans	X	
Alternate Write Trans		
Split Write Trans	X	
Mask Write Trans/Serial In	X	

Function 128K x 8 VRAM	Mosel-Vitelic V52C8128	TI TMS48C121
R/W New Mask	X	X
R/W Old Mask		X
Block Write (BW)	X	X
BW New Mask	X	X
BW Old Mask		X
Flash Write New Mask	X	
Load Mask Register		X
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	X
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		X
Split Write Trans	X	
Mask Write Trans/Serial In	X	

Function 256K x 4 VRAM	Mosel-Vitelic V52C4256	TI TMS44C250
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)		
BW New Mask		
BW Old Mask		
Flash Write New Mask		
Load Mask Register		
Load Color Register		
Read Trans/Serial Out	X	X
Split Read Trans		
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans		
Mask Write Trans/Serial In		

Function 256K x 4 VRAM	Mosel-Vitelic V52C4256	Toshiba TC524256
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)		
BW New Mask		
BW Old Mask		
Flash Write New Mask		
Load Mask Register		
Load Color Register		
Read Trans/Serial Out	X	X
Split Read Trans		
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans		
Mask Write Trans/Serial In		

Function 256K x 4 VRAM	Mosel-Vitelic V52C4258	TI TMS44C521
R/W New Mask	X	X
R/W Old Mask		X
Block Write (BW)	X	X
BW New Mask	X	X
BW Old Mask		X
Flash Write New Mask	X	
Load Mask Register		X
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	X
Write Trans/Serial In	X	X
Pseudo Write Trans	X	X
Alternate Write Trans		X
Split Write Trans	X	
Mask Write Trans/Serial In	X	

Function 256K x 4 VRAM	Mosel-Vitelic V52C4258	Toshiba TC5524258
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)	X	X
BW New Mask	X	X
BW Old Mask		
Flash Write New Mask	X	X
Load Mask Register		
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	X
Write Trans/Serial In	X	
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans	X	X
Mask Write Trans/Serial In	X	X

Function 128K x 8 VRAM	Mosel-Vitelic V52C8126	Toshiba TC58126A
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)		
BW New Mask		
BW Old Mask		
Flash Write New Mask		
Load Mask Register		
Load Color Register		
Read Trans/Serial Out	X	X
Split Read Trans		
Write Trans/Serial In	X	
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans		
Mask Write Trans/Serial In		X

Function 128K x 8 VRAM	Mosel-Vitelic V52C8128	Toshiba TC58128A/B
R/W New Mask	X	X
R/W Old Mask		
Block Write (BW)	X	X
BW New Mask	X	X
BW Old Mask		
Flash Write New Mask	X	X
Load Mask Register		
Load Color Register	X	X
Read Trans/Serial Out	X	X
Split Read Trans	X	X
Write Trans/Serial In		
Pseudo Write Trans	X	X
Alternate Write Trans		
Split Write Trans	X	X
Mask Write Trans/Serial In	X	X

CYPRESS	MOSEL-VITELIC
CY7C106-20PC	MS621002-20EC
CY7C106-20SC	MS621002-20KC
CY7C106-25PC	MS621002-25EC
CY7C106-25SC	MS621002-25KC
CY7C106-35PC	MS621002-35EC
CY7C106-35SC	MS621002-35KC
CY7C108-20PC	MS621008-20EC
CY7C108-20SC	MS621008-20KC
CY7C108-25PC	MS621008-25EC
CY7C108-25SC	MS621008-25KC
CY7C108-35PC	MS621008-35EC
CY7C108-35SC	MS621008-35KC
CY7C166-20PC	MS6267A-25NC
CY7C166-20PC	MS6267A-35NC
CY7C166-20PC	MS6267A-45NC
CY7C185-25/35/45/55PC	MS6264A-25/35/45NC
CY7C185-25/35/45/55VC	MS6264A-25/35/45RC
CY7C185-30SC	MS6264A-25SC
CY7C185-35PC	MS6264A-35PC
CY7C185A-25PC	MS6264A-25PC
CY7C185A-30PC	MS6264A-25PC
CY7C185A-35SC	MS6264A-35SC
CY7C186-25/35/45/55PC	MS6264AL-25/35/45PC
CY7C186-25/35/45/55VC	MS6264AL-25/35/45RC
CY7C194-25PC	MS62252A-25NC
CY7C194-25SC	MS62252A-25RC
CY7C194-35PC	MS62252A-35NC
CY7C194-35SC	MS62252A-35RC
CY7C194-45PC	MS62252A-45NC
CY7C194-45SC	MS62252A-45RC
CY7C196-20PC	MS62253A-20NC
CY7C196-20VC	MS62253A-20RC
CY7C196-25PC	MS62253A-25NC
CY7C196-25VC	MS62253A-25RC
CY7C197-25PC	MS62251A-25NC
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CY7C197-35SC	MS62251A-35RC
CY7C197-45PC	MS62251A-45NC
CY7C197-45SC	MS62251A-45RC
CY7C198-25PC	MS62256A-25PC
CY7C199-25VC	MS62256A-25RC
CY7C198-25SC	MS62256A-25SC
CY7C198-30PC	MS62256A-25PC
CY7C199-30VC	MS62256A-25RC
CY7C198-30SC	MS62256A-25SC
CY7C198-35PC	MS62256A-35PC
CY7C199-35VC	MS62256A-35RC
CY7C198-35SC	MS62256A-35SC
CY7C198-45PC	MS62256A-45PC
CY7C199-45VC	MS62256A-45RC
CY7C198-45SC	MS62256A-45SC
CY7C199-55VC	MS62256A-45NC
CY7C198-55PC	MS62256A-55PC
CY7C199-55VC	MS62256A-45RC
CY7C198-55SC	MS62256A-45SC
CY7C199-25PC	MS62256A-25NC
CY7C199-35PC	MS62256A-30NC
CY7C199-35PC	MS62256A-35NC
CY7C199-45PC	MS62256A-45NC

FUJITSU	MOSEL-VITELIC
MB81C78A	MS6264A-35NC
MB81C78A-25P	MS6264A-25PC
MB81C78A-35P	MS6264A-35PC
MB81C78A-35PF	MS6264A-35FC
MB81C78A-35PJ	MS6264A-35RC
MB81C78A-45P-SK	MS6264A-45NC
MB81C78A-45PF	MS6264A-45FC
MB81C81A35P	MS62251A-25NC
MB81C81A35P	MS62251A-35NC
MB81C81A35PJ	MS62251A-25RC
MB81C81A35PJ	MS62251A-35RC
MB81C81A45P	MS62251A-45NC
MB81C81A45PJ	MS62251A-45RC
MB81C84-35P	MS62252A-25NC
MB81C84A-35P	MS62252A-35NC
MB81C84A-45P	MS62252A-45NC
MB81C84A35PJ	MS62252A-25RC
MB81C84A35PJ	MS62252A-35RC
MB81C84A45PJ	MS62252A-45RC
MB8287-35BH	MS62256A-35NC
MB8287-35PJ	MS62256A-35RC
MB8287-45PJ	MS62256A-45RC
MB8287-45PSH	MS62256A-45NC
MB82B00525P	MS621002-20EC
MB82B00525P	MS621002-25EC
MB82B00525PJ	MS621002-20KC
MB82B00525PJ	MS621002-25KC
MB82B00535P	MS621002-35EC
MB82B00535PJ	MS621002-35KC
MB8416-10DIP	MS6516L-10PC
MB84256A-10LLFP	MS62257-10FC
MB84256A-10LLP	MS62257-10PC
MB84256A-10LP	MS62256L-10PC
MB84256A-10LPF	MS62256L-10FC
MB84256A-12LLFP	MS62256CLL-10FC
MB84256A-12LLP	MS62256CLL-10PC
MB84256A-12LP	MS62256L-10PC
MB84256A-12LPF	MS62256L-10FC
MB84256A-15LLFP	MS62257-10FC
MB84256A-15LLP	MS62257-10PC
MB84256A-70LP	MS62256L-70PC
MB84256A-70LPF	MS62256L-70FC
MB84256A-85LLFP	MS62257-70FC
MB84256A-85LLP	MS62257-70FC
MB84256A-85LP	MS62256L-85PC
MB84256A-85LPF	MS62256L-85FC
MB8464A-80/10/15LLP	MS6265-10PC
MB8464A-80/10/15LLP-SK	MS6265-10NC
MB8464A-80/10/15LLPF	MS6265-10FC
MB8464A-80/10/15LP	MS6264L-10PC
MB8464A-80/10/15LP-SK	MS6265-10NC

MB8464A-80/10/15LPF	MS6264L-10FC
MB8464A-80/10/15P	MS6264L-70PC
MB8464A-80/10/15P-SK	MS6265-10NC
MB8464A-80/10/15PF	MS6264L-70/100FC
GOLDSTAR	**MOSEL-VITELIC**
GM76C256L-10	MS62256L-10PC
GM76C256L-12	MS62256L-10PC
GM76C256L-15	MS62256L-10PC
GM76C256L-85	MS62256L-85PC
GM76C256LFW-10	MS62256L-10FC
GM76C256LFW-12	MS62256L-10FC
GM76C256LFW-15	MS62256L-10FC
GM76C256LFW-85	MS62256L-85FC
GM76C28-10/12	MS6516L-10PC
HITACHI	**MOSEL-VITELIC**
HM6116FLP-2/3/4	MS6516L-10SC
HM6116FP-2/3/4	MS6516L-10SC
HM6116LP-2/3/4	MS6516L-10PC
HM6116P-2/3/4	MS6516L-10PC
HM6207HJP-25	MS62251A-25RC
HM6207HJP-35	MS62251A-35RC
HM6207HJP-45	MS62251A-45RC
HM6207HP-25	MS62251A-25NC
HM6207HP-35	MS62251A-35NC
HM6207HP-45	MS62251A-45NC
HM6208H9-25	MS62252A-25NC
HM6208HJP-25	MS62252A-25RC
HM6208HJP-35	MS62252A-35RC
HM6208HJP-45	MS62252A-45RC
HM6208HP-35	MS62252A-35NC
HM6208HP-45	MS62252A-45NC
HM62256CLP-10SL	MS62257-10PC
HM62256CLP-12SL	MS62257-10PC
HM62256CLP-15SL	MS62257-10PC
HM62256LFP-10SLT	MS62257-10FC
HM62256LFP-10T	MS62256L-10FC
HM62256LFP-12SLT	MS62257-10FC
HM62256LFP-12T	MS62256L-10FC
HM62256LFP-15SLT	MS62257-10FC
HM62256LFP-15T	MS62256L-10FC
HM62256LFP-8T	MS62256L-85FC
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HM62256LP-15	MS62256L-10PC
HM62256LP-8	MS62256L-85PC
HM624256JP-35	MS621002-25KC
HM624256JP-35	MS621002-35KC
HM624256JP-45	MS621002-20KC
HM624256P-35	MS621002-25EC
HM624256P-35	MS621002-35EC
HM624256P-45	MS621002-20EC
HM6264AFP-10/12/15	MS6264L-10FC
HM6264ALFP-10/12/15	MS6264L-10FC
HM6264ALFP-10/12/15/L	MS6265-10FC

HM6264ALP-10/12/15	MS6264L-10PC
HM6264ALP-10/12/15L	MS6265-10PC
HM6264ALSP-10/12/15	MS6265-10NC
HM6264AP-10/12/15	MS6264L-10PC
HM6264ASP-10/12/15	MS6265-10NC
HM6264FP-10/12/15	MS6264L-10FC
HM6264LFP-10/12/15	MS6264L-10FC
HM6264LFP-10/12/15L	MS6265-10FC
HM6264LP-10/12/15	MS6264L-10PC
HM6264LP-10/12/15L	MS6265-10PC
HM6264P-10/12/15	MS6264L-10PC
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HM62832HJP-30	MS62256A-25RC
HM62832HJP-30	MS62256A-25SC
HM62832HJP-35	MS62256A-35RC
HM62832HJP-35	MS62256A-35SC
HM62832HJP-45	MS62256A-45RC
HM62832HJP-45	MS62256A-45SC
HM62832HP-25	MS62256A-25NC
HM62832HP-25	MS62256A-25NC
HM62832HP-30	MS62256A-25NC
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HM62832HP-45	MS62256A-45NC
HM62832HP-45	MS62256A-45PC
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HM62832JP-45	MS62256A-45RC
HM62832P-35	MS62256A-35NC
HM62832P-45	MS62256A-45NC
HM6709JP-20	MS62253A-20NC
HM6709JP-20	MS62253A-20RC
HM6709JP-25	MS62253A-25NC
HM6709JP-25	MS62253A-25RC
HM6789HAP-20	MS6267A-20NC
HM6789HAP-20	MS6267A-25NC
HM6789HAP-20	MS6267A-35NC
HM6789HAP-20	MS6267A-45NC
HYUNDAI	**MOSEL-VITELIC**
HY6116ALX-10/12/15P	MS6516L-10PC
HY6116AX-10/12/15P	MS6516L-10PC
HY6264L-85/100/120/150J	MS6264L-10FC
HY6264L-85/100/120/150P	MS6264L-10PC
HY62C256LJ-10	MS62256L-10FC
HY62C256LJ-12	MS62256L-10FC
HY62C256LJ-15	MS62256L-10FC
HY62C256LP-10	MS62256L-10PC
HY62C256LP-12	MS62256L-10PC
HY62C256LP-15	MS62256L-10PC
HY63C256P-35	MS62256A-35PC
HY63C256P-45	MS62256A-45PC

IDT	MOSEL-VITELIC
IDT61298S/L20P	MS62253A-20NC
IDT61298S/L20Y	MS62253A-20RC
IDT61298S/L25P	MS62253A-25NC
IDT61298S/L25Y	MS62253A-25RC
IDT6198S/L-20P	MS6267A-20NC
IDT6198S/L-25P	MS6267A-25NC
IDT6198S/L-35P	MS6267A-35NC
IDT6198S/L-35P	MS6267A-45NC
IDT71024	MS621008-20EC
IDT71024	MS621008-20KC
IDT71024	MS621008-25EC
IDT71024	MS621008-25KC
IDT71024	MS621008-35EC
IDT71024	MS621008-35KC
IDT71028	MS621002-25KC
IDT71028	MS621002-20EC
IDT71028	MS621002-20KC
IDT71028	MS621002-25EC
IDT71028	MS621002-35EC
IDT71028	MS621002-35KC
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IDT7125630Y	MS62256A-25RC
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IDT7125635TP	MS62256A-35NC
IDT7125635Y	MS62256A-35RC
IDT7125645P	MS62256A-45PC
IDT7125645TP	MS62256A-45NC
IDT7125645Y	MS62256A-45RC
IDT71256525PE	MS62256A-25SC
IDT71256525TP	MS62256A-25NC
IDT71256525Y	MS62256A-25RC
IDT71256S25P	MS62256A-25PC
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IDT71256S25Y	MS62256A-25SC
IDT71256S30P	MS62256A-25PC
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IDT71256S30Y	MS62256A-25SC
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IDT71256S35TP	MS62256A-35NC
IDT71256S35Y	MS62256A-35SC
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IDT71256S45PE	MS62256A-45RC
IDT71256S45TP	MS62256A-45NC
IDT71256S45Y	MS62256A-45SC
IDT71256S55P	MS62256A-55PC
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IDT7164S-25/30/35	MS6264A-25/30/35SC
IDT7164S-25/30/35P	MS6264A-25/30/35PC
IDT7164S-25/30/35PE	MS6264A-25/30/35FC
IDT7164S25P	MS6264A-25PC
IDT7164S25TP	MS6264A-25NC
IDT7164S30P	MS6264A-25PC
IDT7164S30Y	MS6264A-25RC
IDT7164S30Y	MS6264A-25SC
IDT7164S35P	MS6264A-35PC
IDT7164S35Y	MS6264A-35RC
IDT7164S35Y	MS6264A-35SC
IDT7164STP35	MS6264A-35NC

INTEL	MOSEL-VITELIC
P5164-PDIP20/25	MS6264A-25PC
P5164SL-PDIP100	MS6264L-10PC
PG51256SL-10 SOIC PACK	MS62256L-10FC
PG51256SL-10 P DIP	MS62256L-10PC
PG51256SL-70 SOIC PACK	MS62256L-70FC
PG51256SL-70 P DIP	MS62256L-70PC
PG5164SL-SOIC100	MS6264L-10FC?

MICROTECH	MOSEL-VITELIC
MT5C2568-25	MS62256A-25NC
MT5C2568-25DJ	MS62256A-25RC
MT5C2568-30	MS62256A-25NC
MT5C2568-30DJ	MS62256A-25RC
MT5C2568-35	MS62256A-35NC
MT5C2568-35DJ	MS62256A-35RC
MT5C2568-35W	MS62256A-35PC
MT5C2568-45	MS62256A-45NC
MT5C2568-45DJ	MS62256A-45RC
MT5C2568-45W	MS62256A-45PC

MICRON	MOSEL-VITELIC
MT5C1005DJ-20	MS621002-20EC
MT5C1005DJ-25	MS621002-25EC
MT5C1005DJ-35	MS621002-35EC
MT5C1005W-20	MS621002-20KC
MT5C1005W-25	MS621002-25KC
MT5C1005W-35	MS621002-35KC
MT5C1008DJ-20	MS621008-20EC
MT5C1008DJ-25	MS621008-25EC
MT5C1008DJ-35	MS621008-35EC
MT5C1008W-20	MS621008-20KC
MT5C1008W-25	MS621008-25KC
MT5C1008W-35	MS621008-35KC

MT5C2564-25	MS62252A-25NC
MT5C2564-35	MS62252A-35NC
MT5C2564-45	MS62252A-45NC
MT5C2564DJ-25	MS62252A-25RC
MT5C2564DJ-35	MS62252A-35RC
MT5C2564DJ-45	MS62252A-45RC
MT5C2565-20	MS62253A-20NC
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MT5C2565DJ-20	MS62253A-20RC
MT5C2565DJ-25	MS62253A-25RC
MT5C2568-25	MS62256A-25NC
MT5C2568-35	MS62256A-30NC
MT5C2568-35	MS62256A-35NC
MT5C2568-45	MS62256A-45NC
MT5C2568DJ-25	MS62256A-25RC
MT5C2568DJ-35	MS62256A-25RC
MT5C2568DJ-35	MS62256A-25SC
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MT5C2568W-25	MS62256A-25PC
MT5C2568W-35	MS62256A-35PC
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MT5C5257-45	MS62251A-45NC
MT5C5257DJ-25	MS62251A-25RC
MT5C5257DJ-35	MS62251A-35RC
MT5C5257DJ-45	MS62251A-45RC
MT5C6405-25	MS6267A-25NC
MT5C6405-35	MS6267A-35NC
MT5C6405-35	MS6267A-45NC
MT5C6408-25	MS6264A-25NC
MT5C6408-25/30/35DJL	MS6264A-25/30/35RC
MT5C6408-25/30/35L	MS6264A-25/30/35NC
MT5C6408-35	MS6264A-35NC
MT5C6408DJ-30	MS6264A-25RC
MT5C6408DJ-35	MS6264A-35RC
MT5C6408G-30	MS6264A-25SC
MT5C6408G-35	MS6264A-35SC
MT5C6408W-25	MS6264A-25PC
MT5C6408W-30	MS6264A-25PC
MT5C6408W-35	MS6264A-35PC

MITSUBISHI	MOSEL-VITELIC
M5M	MS621002-20EC
M5M178P-35/45/55	MS6264A-35/45NC
M5M5165FP-70/10/12/15	MS6264L-70/10FC
M5M5165FP-70/10/12/15	MS6264L-70/10FC
M5M5165P-70/10/12/15	MS6264L-70/10PC
M5M5165P-70/10/12/15L	MS6264L-70/10PC
M5M5256AFP-10L	MS62256L-10FC
M5M5256AFP-70L	MS62256L-70FC
M5M5256AFP-85L	MS62256L-85FC
M5M5256FP-10L	MS62256L-10FC
M5M5256FP-10LL	MS62257-10FC
M5M5256FP-12L	MS62256L-10FC
M5M5256FP-12LL	MS62257-10FC
M5M5256FP-15L	MS62256L-10FC
M5M5256FP-15LL	MS62257-10FC
M5M5256P-10L	MS62256L-10PC
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M5M5257J-45	MS62251A-45RC
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M5M5258J-25	MS62252A-25RC
M5M5258J-35	MS62252A-35RC
M5M5258J-45	MS62252A-45RC
M5M5258P-25	MS62252A-25NC
M5M5258P-35	MS62252A-35NC
M5M5258P-45	MS62252A-45NC

MOTOROLA	MOSEL-VITELIC
MCM60L256AF-10	MS62256L-10FC
MCM60L256AF-12	MS62256L-10FC
MCM60L256AF-70	MS62256L-70FC
MCM60L256AF-85	MS62256L-85FC
MCM60L256AP-10	MS62256L-10PC
MCM60L256AP-12	MS62256L-10PC
MCM60L256AP-70	MS62256L-70PC
MCM6164CP-45/55	MS6264A-45NC
MCM6206J25	MS62256A-25RC
MCM6206J25	MS62256A-25SC
MCM6206J30	MS62256A-25RC
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MCM6206NJ-30	MS62256A-25RC
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MCM6206NJ-45	MS62256A-45RC
MCM6206NP-30	MS62256A-25NC
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MCM6206P30	MS62256A-25PC
MCM6206P35	MS62256A-35NC
MCM6206P35	MS62256A-35PC

MCM6206P45	MS62256A-45NC
MCM6206P45	MS62256A-45PC
MCM6206P55	MS62256A-45NC
MCM6206P55	MS62256A-55PC
MCM6207J25	MS62251A-25RC
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MCM6207P25	MS62251A-25NC
MCM6207P35	MS62251A-35NC
MCM6207P45	MS62251A-45NC
MCM6208J20	MS621008-20KC
MCM6208J25	MS621008-25KC
MCM6208J35	MS621008-35KC
MCM6208P20	MS621008-20EC
MCM6208P25	MS621008-25EC
MCM6208P35	MS621008-35EC
MCM6209J-20	MS62253A-20RC
MCM6209J-25	MS62253A-25RC
MCM6209P-20	MS62253A-20NC
MCM6209P-25	MS62253A-25NC
MCM6228J25	MS621002-20KC
MCM6228J25	MS621002-25KC
MCM6228J35	MS621002-35KC
MCM6228P25	MS621002-20EC
MCM6228P25	MS621002-25EC
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MCM6264CNJ35	MS6264A-35RC
MCM6264CNJ35	MS6264A-35SC
MCM6264CP25	MS6264A-25NC
MCM6264CP25	MS6264A-25PC
MCM6264CP30	MS6264A-25PC
MCM6264CP35	MS6264A-35NC
MCM6264CP35	MS6264A-35PC
MCM6290P15	MS6267A-25NC
MCM6290P15	MS6267A-35NC
MCM6290P15	MS6267A-45NC
MSM60L256AP-85	MS62256L-85PC

NEC	**MOSEL-VITELIC**
UPD43256AC-10L	MS62256L-10PC
UPD43256AC-10L	MS62257-10PC
UPD43256AC-12L	MS62256L-10PC
UPD43256AC-15L	MS62256L-10PC
UPD43256AC-85L	MS62256L-85PC
UPD43256AC-85LL	MS62257-70PC
UPD43256AGU-10LL	MS62257-10FC
UPD43256AGU-85LL	MS62257-75FC
UPD43256BC-70L	MS62256L-70PC
UPD43256BC-85L	MS62256L-85PC
UPD43256BGU-70L	MS62256L-70FC
UPD43256BGU-85L	MS62256L-85FC
UPD43258CR-25	MS62256A-25NC
UPD43258CR-35	MS62256A-35NC
UPD43258CR-45	MS62256A-45NC
UPD43258LA-25	MS62256A-25RC
UPD43258LA-35	MS62256A-35RC
UPD43258LA-45	MS62256A-45RC
uPD4363C-45	MS6267A-25NC
uPD4363C-45	MS6267A-35NC
uPD4363C-45	MS6267A-45NC
UPDAGU-10L	MS62256L-10FC
UPDAGU-12L	MS62256L-10FC
UPDAGU-15L	MS62256L-10FC
UPDAGU-85L	MS62256L-85FC
µPD446-OBSOLETE	MS6516L-10PC

OKI	**MOSEL-VITELIC**
MSM51257AL-10GS	MS62256L-10FC
MSM51257AL-10RS	MS62256L-10PC
MSM51257AL-12GS	MS62256L-10FC
MSM51257AL-12RS	MS62256L-10PC
MSM51257AL-85GS	MS62256L-85FC
MSM51257AL-85RS	MS62256L-85PC
MSM51257ALL-10GS	MS62257-10FC
MSM51257ALL-10RS	MS62257-10PC
MSM51257ALL-85GS	MS62257-70FC
MSM51257ALL-85RS	MS62257-70PC
MSM5165AL-10GS	MS6264L-10FC
MSM5165AL-10RS	MS6264L-10PC

PSI	**MOSEL-VITELIC**
P4C125625J	MS62256A-25RC
P4C125625J	MS62256A-25SC
P4C125625P	MS62256A-25NC
P4C125625P	MS62256A-25PC
P4C125630J	MS62256A-25RC
P4C125630J	MS62256A-25SC
P4C125630P	MS62256A-25NC
P4C125630P	MS62256A-25PC
P4C125635J	MS62256A-35RC
P4C125635J	MS62256A-35SC
P4C125635P	MS62256A-35NC
P4C125635P	MS62256A-35PC
P4C125645J	MS62256A-45RC
P4C125645J	MS62256A-45SC
P4C125645P	MS62256A-45NC
P4C125645P	MS62256A-45PC
P4C125655J	MS62256A-45RC
P4C125655J	MS62256A-45SC
P4C125655P	MS62256A-45NC
P4C125655P	MS62256A-55PC
P4C1257-25J	MS62251A-25RC
P4C1257-25P	MS62251A-25NC
P4C1257-35J	MS62251A-35RC
P4C1257-35P	MS62251A-35NC
P4C1257-45J	MS62251A-35RC
P4C1257-45P	MS62251A-35NC
P4C125825J	MS62252A-25RC
P4C125825P	MS62252A-25NC
P4C125835J	MS62252A-35RC
P4C125835P	MS62252A-35NC

P4C125845J	MS62252A-35RC
P4C125845P	MS62252A-35NC
P4C198L-25P	MS6267A-25NC
P4C198L-35P	MS6267A-35NC
P4C198L-45P	MS6267A-45NC

S-MOS	MOSEL-VITELIC
SRM20256LC-10	MS62256L-10PC
SRM20256LC-12	MS62256L-10PC
SRM20256LC-85	MS62256L-85PC
SRM20256LM-10	MS62256L-10FC
SRM20256LM-12	MS62256L-10FC
SRM20256LM-85	MS62256L-85FC
SRM20256N-45	MS62256A-45NC
SRM20256N-55	MS62256A-45NC
SRM22256C-55	MS62256A-55PC
SRM22256C-70	MS62256L-70PC
SRM22256M-55	MS62256L-70FC
SRM22256M-70	MS62256L-70FC
SRM2264LC10/12	MS6264L-10PC
SRM2264LM10/12	MS6264L-10FC

SAMSUNG	MOSEL-VITELIC
KM62256ALP-10	MS62256L-10PC
KM62256ALP-12	MS62256L-10PC
KM62256ALP-8	MS62256L-10PC
KM62256ALSG-10	MS62256L-10FC
KM62256ALSG-12	MS62256L-10FC
KM62256ALSG-8	MS62256L-10FC
KM6264A-70/10/12/P	MS6264L-70/10PC
KM6264AL-70/10/12P	MS6264L-70/10PC
KM68257P-35	MS62256A-35PC
KM68257P-45	MS62256A-45PC

SGS THOMPSON	MOSEL-VITELIC
MK4832LN-120	MS62256L-10PC
MK4832LN-70	MS62256L-70PC
MK48H64LN-70/12	MS6264L-70/10PC
MK48H64LS-70/12	MS6264L-70/10FC
MK48H64N-70/12	MS6264L-70/10PC
MK48H64S-70/12	MS6264L-70/10FC

SHARP	MOSEL-VITELIC
LH5116-10	MS6516L-10PC
LH5116H-10	MS6516L-10PI
LH5117-10	MS6516L-10PC
LH5117H-10	MS6516L-10PI
LH5118-10	MS6516L-10PC
LH5118H-10	MS6516L-10PI
LH51256P-10	MS62256L-10PC
LH51256P-12L	MS62256L-10PC
LH5160-10L	MS6264L-10PC
LH5160-10L	MS6264L-10PI
LH5160D-10L	MS6265-10NC
LH5160N-10L	MS6264L-10FC
LH5164D-10L	MS6264L-10PC
LH5164N-10L	MS6264L-10FC
LH521002-20	MS621002-20KC
LH521002D-20	MS621002-20EC
LH521002D-25	MS621002-25EC
LH521002D-35	MS621002-35EC
LH521002K-25	MS621002-25KC
LH521002K-35	MS621002-35KC
LH521008D-20	MS621008-20EC
LH521008D-25	MS621008-25EC
LH521008D-35	MS621008-35EC
LH521008K-20	MS621008-20KC
LH521008K-25	MS621008-25KC
LH521008K-35	MS621008-35KC
LH52251AD-25	MS62251A-25NC
LH52251AD-35	MS62251A-35NC
LH52251AD-45	MS62251A-35NC
LH52251AK-25	MS62251A-25RC
LH52251AK-35	MS62251A-35RC
LH52251AK-45	MS62251A-35RC
LH52252AD-25	MS62252A-25NC
LH52252AD-35	MS62252A-35NC
LH52252AD-45	MS62252A-45NC
LH52252AK-25	MS62252A-25RC
LH52252AK-35	MS62252A-35RC
LH52252AK-45	MS62252A-45RC
LH52253A-20RC	MS62253A-20RC
LH52253A-25NC	MS62253A-25NC
LH52253A-25RC	MS62253A-25RC
LH52256L-12	MS62256L-10PC
LH52256L-70	MS62256L-70PC
LH52256L-90	MS62256L-85PC
LH52256N-120L	MS62256L-10FC
LH52256N-70L	MS62256L-70FC
LH52256N-90	MS62256L-85FC
LH52258D-25	MS62256A-25NC
LH52258D-25	MS62256A-25PC
LH52258D-25	MS62256A-25NC
LH52258D-35	MS62256A-25NC
LH52258D-35	MS62256A-35NC
LH52258D-35	MS62256A-35NC
LH52258D-45	MS62256A-45NC
LH52258D-45	MS62256A-45NC
LH52258P-35	MS62256A-22225PC
LH52258P-35	MS62256A-35PC
LH52258P-45	MS62256A-45PC
LH5267A-25NC	MS6267A-25NC
LH5267A-35NC	MS6267A-35NC
LH5267A-45NC	MS6267A-45NC
LJ52253A-20NC	MS62253A-20NC

SONY	MOSEL-VITELIC
CSXK58257M-10LL	MS62257-10PC
CSXK58257M-12LL	MS62257-10PC
CSXK58257M-85LL	MS62257-70FC
CXK51256-35P	MS62251A-25NC

CXK51256-35P	MS62251A-35NC
CXK51256-45P	MS62251A-45NC
CXK54256-35P	MS62252A-25NC
CXK54256-35P	MS62252A-35NC
CXK54259-45P	MS62252A-45NC
CXK5465P-25	MS6267A-25NC
CXK5465P-35	MS6267A-35NC
CXK5465P-35	MS6267A-45NC
CXK581020-35J	MS621008-20KC
CXK581020-35J	MS621008-25KC
CXK581020-35J	MS621008-35KC
CXK581020-35SP	MS621008-20EC
CXK581020-35SP	MS621008-25EC
CXK581020-35SP	MS621008-35EC
CXK5816M-10/12/15	MS6516L-10SC
CXK5816M-10L/12L/15L	MS6516L-10SC
CXK5816PN-10/12/15	MS6516L-10PC
CXK5816PN-10L/12L/15L	MS6516L-10PC
CXK58257P-10L	MS62256L-10PC
CXK58257P-12L	MS62256L-10PC
CXK58257P-70L	MS62256L-70PC
CXK58257P-85L	MS62256L-85PC
CXK58257SP-10L	MS62256L-10FC
CXK58257SP-12L	MS62256L-10FC
CXK58257SP-70L	MS62256L-70FC
CXK58257SP-85L	MS62256L-85FC
CXK58258-45P	MS62256A-45PC
CXK58258-45SP	MS62256A-45NC
CXK58258-55P	MS62256A-55PC
CXK58258-55SP	MS62256A-45NC
CXK58258B-25J	MS62256A-25RC
CXK58258B-25J	MS62256A-25SC
CXK58258B-25P	MS62256A-25NC
CXK58258B-25P	MS62256A-25PC
CXK58258B-35J	MS62256A-35RC
CXK58258B-35J	MS62256A-35SC
CXK58258B-35P	MS62256A-35NC
CXK58258B-35P	MS62256A-35PC
CXK58258P-35	MS62256A-35PC
CXK58258P-45	MS62256A-45PC
CXK58258P-55	MS62256A-45PC
CXK58258SP-25	MS62256A-25NC
CXK58258SP-30	MS62256A-25NC
CXK58258SP-35	MS62256A-35NC
CXK58258SP-45	MS62256A-45NC
CXK58258SP-55	MS62256A-45NC
CXK5863AJ-25	MS6264A-25RC
CXK5863AJ30	MS6264A-25RC
CXK5863AJ30	MS6264A-25SC
CXK5863AJ35	MS6264A-35RC
CXK5863AJ35	MS6264A-35SC
CXK5863AP-25	MS6264A-25NC
CXK5863AP25	MS6264A-25NC
CXK5863AP25	MS6264A-25PC
CXK5863AP30	MS6264A-25PC
CXK5863AP35	MS6264A-35NC
CXK5863AP35	MS6264A-35PC
CXK5863J-25/30/35	MS6264A-25/35RC
CXK5863M-25/30/35	MS6264A-25/35FC
CXK5863P-25/30/35	MS6264A-25/35NC
CXK5864BM-70/10/12L	MS6264L-70/10FC
CXK5864BM-70/10/12LL	MS6265-10FC
CXK5864BP-70/10/12	MS6264L-70/10PC
CXK5864BP-70/10/12LL	MS6265-10PC
CXK5864BSP-70/10/12L	MS6265-10NC
CXK5864BSP-70/10/12LL	MS6265-10NC

TOSHIBA	MOSEL-VITELIC
TC5517P-10/12/15	MS6516L-10PC
TC55257BFL-10	MS62256L-10FC
TC55257BFL-10L	MS62257-10PC
TC55257BFL-85	MS62256L-85FC
TC55257BFL-85L	MS62257-70PC
TC55257BPL-10	MS62256L-10PC
TC55257BPL-85	MS62256L-85PC
TC55328J-25	MS62256A-25RC
TC55328J-25	MS62256A-25SC
TC55328J-25	MS62256A-25RC
TC55328J-35	MS62256A-35RC
TC55328J-35	MS62256A-35SC
TC55328P-25	MS62256A-25NC
TC55328P-25	MS62256A-25PC
TC55328P-25	MS62256A-25NC
TC55328P-35	MS62256A-35NC
TC55328P-35	MS62256A-35PC
TC55328P-45	MS62256A-45NC
TC55328P-45	MS62256A-45PC
TC55417P-25H	MS6267A-25NC
TC55417P-35H	MS6267A-35NC
TC55417P-35H	MS6267A-45NC
TC55464J-25	MS62252A-25RC
TC55464J-35	MS62252A-35RC
TC55464P-25	MS62252A-25NC
TC55464P-35	MS62252A-35NC
TC55465J-20	MS62253A-20RC
TC55465J-25	MS62253A-25RC
TC55465P-20	MS62253A-20NC
TC55465P-25	MS62253A-25NC
TC5563APL-10/12/15	MS6265-10NC
TC5563APL-10/12/15L	MS6265-10NC
TC5565AFL-10/12/15	MS6264L-10FC
TC5565AFL-10/12/15L	MS6264L-10FC
TC5565APL-10/12/15	MS6264L-10PC
TC5565APL-10/12/15L	MS6264L-10PC
TC5588J35	MS6264A-25RC
TC5588J35	MS6264A-25SC
TC5588J35	MS6264A-35NC
TC5588J35	MS6264A-35RC
TC5588J35	MS6264A-35SC
TC5588P-25	MS6264A-25NC
TC5588P-25	MS6264A-25NC
TC5588P-30	MS6264A-25PC
TC5588P35	MS6264A-35PC

UMC	MOSEL-VITELIC
UM6116-2/2L	MS6516L-10PC
UM6116-2T/2LT	MS6516L-10PI
UM6116M-2/2L	MS6516L-10SC
UM6116M-2T/2LT	MS6516L-10SI
UM62256-10	MS62256L-10PC
UM62256-12L	MS62256L-10PC
UM62256M-10	MS62256L-10FC
UM62256M-12L	MS62256L-10FC
UM6264-70/10/12	MS6264L-70/10PC
UM6264-70/10/12L	MS6264L-70/10PC
UM6264A-10/12	MS6264L-10PC
UM6264A-10/12L	MS6264L-10PC
UM6264A-10/12LL	MS6265-10PC
UM6264AK-10/12	MS6265-10NC
UM6264AK-10/12L	MS6265-10NC
UM6264AK-10/12LL	MS6265-10NC
UM6264AM-10/12	MS6264L-10FC
UM6264AM-10/12L	MS6264L-10FC
UM6264K-70/10/12	MS6265-10NC
UM6264K-70/10/12L	MS6265-10NC
UM6264M-70/10/12	MS6264L-70/10FC
UM6264M-70/10/12L	MS6264L-70/10FC

WINDBOND	MOSEL-VITELIC
W2416-10/10L	MS6516L-10PC
W2416S-10/10L	MS6516L-10SC
W2464-10/12	MS6264L-10PC
W2464-10/12L	MS6264L-10PC
W2464K-10/12	MS6265-10NC
W2464K-10/12L	MS6265-10NC
W2464S-10/12	MS6264L-10FC
W2464S-10/12L	MS6264L-10FC

AMD	MOSEL-VITELIC
AM7200-25PC	7200-25PC
AM7200-35PC	7200-35PC
AM7200-50PC	7200-50PC
AM7200-65PC	7200-50PC
AM7200-80PC	7200-80PC
AM7200-25JC	7200-25JC
AM7200-35JC	7200-35JC
AM7200-50JC	7200-50JC
AM7200-65JC	7200-50JC
AM7200-80JC	7200-80JC
AM7200-25RC	7200-25NC
AM7200-35RC	7200-35NC
AM7200-50RC	7200-50NC
AM7200-65RC	7200-50NC
AM7200-80RC	7200-80NC
AM7201-25PC	7201A-25PC
AM7201-35PC	7201A-35PC
AM7201-50PC	7201A-50PC
AM7201-65PC	7201A-50PC
AM7201-80PC	7201A-80PC
AM7201-25JC	7201A-25JC
AM7201-35JC	7201A-35JC
AM7201-50JC	7201A-50JC
AM7201-65JC	7201A-50JC
AM7201-80JC	7201A-80JC
AM7201-25RC	7201A-25NC
AM7201-35RC	7201A-35NC
AM7201-50RC	7201A-50NC
AM7201-65RC	7201A-50NC
AM7201-80RC	7201A-80NC
AM7202-25PC	7202A-25PC
AM7202-35PC	7202A-35PC
AM7202-50PC	7202A-50PC
AM7202-65PC	7202A-50PC
AM7202-80PC	7202A-80PC
AM7202-25JC	7202A-25JC
AM7202-35JC	7202A-35JC
AM7202-50JC	7202A-50JC
AM7202-65JC	7202A-50JC
AM7202-80JC	7202A-80JC
AM7202-25RC	7202A-25NC
AM7202-35RC	7202A-35NC
AM7202-50RC	7202A-50NC
AM7202-65RC	7202A-50NC
AM7202-80RC	7202A-80NC
AM7203-35PC	7203-35PC
AM7203-50PC	7203-50PC
AM7203-65PC	7203-50PC
AM7203-80PC	7203-80PC
AM7203-35JC	7203-35JC
AM7203-50JC	7203-50JC
AM7203-65JC	7203-50JC
AM7203-80JC	7203-80JC
AM7204-35PC	7204-35PC
AM7204-50PC	7204-50PC
AM7204-65PC	7204-50PC
AM7204-80PC	7204-80PC
AM7204-120PC	7204-80PC
AM7204-35JC	7204-35JC
AM7204-50JC	7204-50JC
AM7204-65JC	7204-50JC
AM7204-80JC	7204-80JC
AM7204-120JC	7204-80JC

CYPRESS	MOSEL-VITELIC
CY7C420-30PC	7201A-25PC
CY7C420-40PC	7201A-35PC
CY7C420-65PC	7201A-50PC
CY7C421-30PC	7201A-25NC
CY7C421-40PC	7201A-35NC
CY7C421-65PC	7201A-50NC
CY7C421-30JC	7201A-25JC
CY7C421-40JC	7201A-35JC
CY7C421-65JC	7201A-50JC
CY7C424-30PC	7202A-25PC
CY7C424-40PC	7202A-35PC
CY7C424-65PC	7202A-50PC
CY7C425-30PC	7202A-25NC
CY7C425-40PC	7202A-35NC
CY7C425-65PC	7202A-50NC
CY7C425-30JC	7202A-25JC
CY7C425-40JC	7202A-35JC
CY7C425-65JC	7202A-50JC
CY7C428-40PC	7203-35PC
CY7C428-65PC	7203-50PC
CY7C429-40PC	7203-35NC
CY7C429-65PC	7203-50NC
CY7C429-40JC	7203-35JC
CY7C429-65JC	7203-50JC

DALLAS	MOSEL-VITELIC
DS2009-35	7201A-35PC
DS2009-50	7201A-50PC
DS2009-65	7201A-50PC
DS2009-80	7201A-80PC
DS2009R-35	7201A-35JC
DS2009R-50	7201A-50JC
DS2009R-65	7201A-50JC
DS2009R-80	7201A-80JC
DS2010-35	7202A-35PC
DS2010-50	7202A-50PC
DS2010-65	7202A-50PC
DS2010-80	7202A-80PC
DS2010R-35	7202A-35JC
DS2010R-50	7202A-50JC
DS2010R-65	7202A-50JC
DS2010R-80	7202A-80JC
DS2011-35	7203A-35PC
DS2011-50	7203A-50PC
DS2011-65	7203A-50PC
DS2011-80	7203A-80PC
DS2011R-35	7203A-35JC

DS2011R-50	7203A-50JC
DS2011R-65	7203A-50JC
DS2011R-80	7203A-80JC
IDT	**MOSEL-VITELIC**
IDT7200L25TP	7200L-25NC
IDT7200L35TP	7200L-35NC
IDT7200L50TP	7200L-50NC
IDT7200L65TP	7200L-50NC
IDT7200L80TP	7200L-80NC
IDT7200L120TP	7200L-80NC
IDT7200L25J	7200L-25JC
IDT7200L35J	7200L-35JC
IDT7200L50J	7200L-50JC
IDT7200L65J	7200L-50JC
IDT7200L80J	7200L-80JC
IDT7200L120J	7200L-80JC
IDT7200L25SO	7200L-25FC
IDT7200L35SO	7200L-35FC
IDT7200L50SO	7200L-50FC
IDT7200L65SO	7200L-50FC
IDT7200L80SO	7200L-80FC
IDT7200L120SO	7200L-80FC
IDT7200S25TP	7200-25NC
IDT7200S35TP	7200-35NC
IDT7200S50TP	7200-50NC
IDT7200S65TP	7200-50NC
IDT7200S80TP	7200-80NC
IDT7200S120TP	7200-80NC
IDT7200S25J	7200-25JC
IDT7200S35J	7200-35JC
IDT7200S50J	7200-50JC
IDT7200S65J	7200-50JC
IDT7200S80J	7200-80JC
IDT7200S120J	7200-80JC
IDT7200S25SO	7200-25FC
IDT7200S35SO	7200-35FC
IDT7200S50SO	7200-50FC
IDT7200S65SO	7200-50FC
IDT7200S80SO	7200-80FC
IDT7200S120SO	7200-80FC
IDT7201L50P	7201AL-50PC
IDT7201L65P	7201AL-50PC
IDT7201L80P	7201AL-80PC
IDT7201L120P	7201AL-80PC
IDT7201L50J	7201AL-50JC
IDT7201L65J	7201AL-50JC
IDT7201L80J	7201AL-80JC
IDT7201L120J	7201AL-80JC
IDT7201LA25P	7201AL-25PC
IDT7201LA35P	7201AL-35PC
IDT7201LA50P	7201AL-50PC
IDT7201LA65P	7201AL-50PC
IDT7201LA80P	7201AL-80JC
IDT7201LA120P	7201AL-80JC
IDT7201LA25TP	7201AL-25NC
IDT7201LA35TP	7201AL-35NC
IDT7201LA50TP	7201AL-50NC
IDT7201LA65TP	7201AL-50NC
IDT7201LA80TP	7201AL-80NC
IDT7201LA120TP	7201AL-80NC
IDT7201LA25J	7201AL-25JC
IDT7201LA35J	7201AL-35JC
IDT7201LA50J	7201AL-50JC
IDT7201LA65J	7201AL-50JC
IDT7201LA80J	7201AL-80JC
IDT7201LA120J	7201AL-80JC
IDT7201LA25SO	7201AL-25FC
IDT7201LA35SO	7201AL-35FC
IDT7201LA50SO	7201AL-50FC
IDT7201LA65SO	7201AL-50FC
IDT7201LA80SO	7201AL-80FC
IDT7201LA120SO	7201AL-80FC
IDT7201S50P	7201A-50PC
IDT7201S65P	7201A-50PC
IDT7201S80P	7201A-80PC
IDT7201S120P	7201A-80PC
IDT7201S50J	7201A-50JC
IDT7201S65J	7201A-50JC
IDT7201S80J	7201A-80JC
IDT7201S120J	7201A-80JC
IDT7201SA25P	7201A-25PC
IDT7201SA35P	7201A-35PC
IDT7201SA50P	7201A-50PC
IDT7201SA65P	7201A-50PC
IDT7201SA80P	7201A-80PC
IDT7201SA120P	7201A-80PC
IDT7201SA25TP	7201A-25NC
IDT7201SA35TP	7201A-35NC
IDT7201SA50TP	7201A-50NC
IDT7201SA65TP	7201A-50NC
IDT7201SA80TP	7201A-80NC
IDT7201SA120TP	7201A-80NC
IDT7201SA25J	7201A-25JC
IDT7201SA35J	7201A-35JC
IDT7201SA50J	7201A-50JC
IDT7201SA65J	7201A-50JC
IDT7201SA80J	7201A-80JC
IDT7201SA120J	7201A-80JC
IDT7201SA25SO	7201A-25FC
IDT7201SA35SO	7201A-35FC
IDT7201SA50SO	7201A-50FC
IDT7201SA65SO	7201A-50FC
IDT7201SA80SO	7201A-80FC
IDT7201SA120SO	7201A-80FC
IDT7202L50P	7202AL-50PC
IDT7202L65P	7202AL-50PC
IDT7202L80P	7202AL-80PC
IDT7202L120P	7202AL-80PC
IDT7202L50J	7202AL-50JC
IDT7202L65J	7202AL-50JC
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IDT7202L120J	7202AL-80JC
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IDT7202LA50SO	7202AL-50FC
IDT7202LA65SO	7202AL-50FC
IDT7202LA80SO	7202AL-80FC
IDT7202LA120SO	7202AL-80FC
IDT7202S50P	7202A-50PC
IDT7202S65P	7202A-50PC
IDT7202S80P	7202A-80PC
IDT7202S120P	7202A-80PC
IDT7202S50J	7202A-50JC
IDT7202S65J	7202A-50JC
IDT7202S80J	7202A-80JC
IDT7201S120J	7202A-80JC
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IDT7202SA50TP	7202A-50NC
IDT7202SA65TP	7202A-50NC
IDT7202SA80TP	7202A-80NC
IDT7202SA120TP	7202A-80NC
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IDT7202SA35J	7202A-35JC
IDT7202SA50J	7202A-50JC
IDT7202SA65J	7202A-50JC
IDT7202SA80J	7202A-80JC
IDT7202SA120J	7202A-80JC
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IDT7202SA120SO	7202A-80FC
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IDT7203L80P	7203L-80PC
IDT7203L120P	7203L-80PC
IDT7203L35J	7203L-35JC
IDT7203L50J	7203L-50JC
IDT7203L65J	7203L-50JC
IDT7203L80J	7203L-80JC
IDT7203L120J	7203L-80JC
IDT7203S35P	7203-35PC
IDT7203S50P	7203-50PC
IDT7203S65P	7203-50PC
IDT7203S80P	7203-80PC
IDT7203S120P	7203-80PC
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IDT7203S50J	7203-50JC
IDT7203S65J	7203-50JC
IDT7203S80J	7203-80JC
IDT7203S120J	7203-80JC
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IDT7204L65P	7204L-50PC
IDT7204L80P	7204L-80PC
IDT7204L120P	7204L-80PC
IDT7204L35J	7204L-35JC
IDT7204L50J	7204L-50JC
IDT7204L65J	7204L-50JC
IDT7204L80J	7204L-80JC
IDT7204L120J	7204L-80JC
IDT7204S35P	7204-35PC
IDT7204S50P	7204-50PC
IDT7204S65P	7204-50PC
IDT7204S80P	7204-80PC
IDT7204S120P	7204-80PC
IDT7204S35J	7204-35JC
IDT7204S50J	7204-50JC
IDT7204S65J	7204-50JC
IDT7204S80J	7204-80JC
IDT7204S120J	7204-80JC

MOSTEK	**MOSEL-VITELIC**
MK4501-10N	7201A-80PC
MK4501-12N	7201A-80PC
MK4501-65N	7201A-50PC
MK4501-80N	7201A-80PC

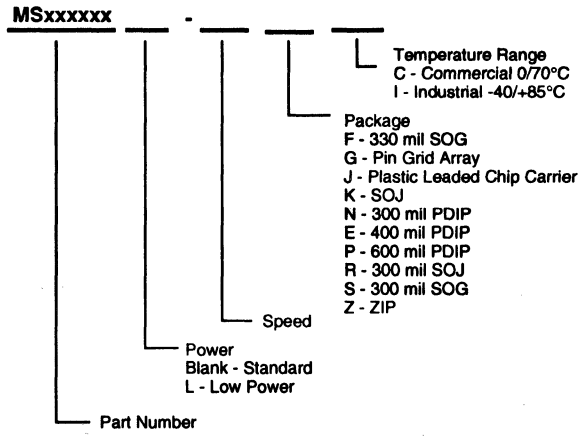
SAMSUNG	**MOSEL-VITELIC**
KM75C101AP-25	7201A-25PC
KM75C101AP-35	7201A-35PC
KM75C101AP-80	7201A-80PC
KM75C101AJ-25	7201A-25JC
KM75C101AJ-35	7201A-35JC
KM75C101AJ-80	7201A-80JC
KM75C101AN-25	7201A-25NC
KM75C101AN-35	7201A-35NC
KM75C101AN-80	7201A-80NC
KM75C102AP-25	7202A-25PC
KM75C102AP-35	7202A-35PC
KM75C102AP-80	7202A-80PC

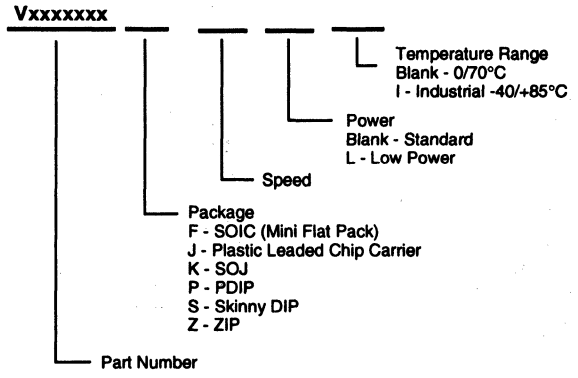
KM75C102AJ-25	7202A-25JC
KM75C102AJ-35	7202A-35JC
KM75C102AJ-80	7202A-80JC
KM75C102AN-25	7202A-25NC
KM75C102AN-35	7202A-35NC
KM75C102AN-80	7202A-80NC
KM75C03AP-35	7203A-35PC
KM75C03AP-80	7203A-80PC
KM75C03AJ-35	7203A-35JC
KM75C03AJ-80	7203A-80JC
KM75C03AN-35	7203A-35NC
KM75C03AN-80	7203A-80NC

SHARP	MOSEL-VITELIC
LH5495D-25	7200-25NC
LH5495D-35	7200-35NC
LH5495D-45	7200-35NC
LH5496-35	7201A-35PC
LH5496-50	7201A-50PC
LH5496D-35	7201A-35NC
LH5496D-50	7201A-50NC
LH5497-35	7202A-35PC
LH5497-50	7202A-50PC
LH5497D-35	7202A-35NC
LH5497D-50	7202A-50NC
LH5498-35	7203-35PC
LH5498-50	7203-50PC
LH5498D-35	7203-35NC
LH5498D-50	7203-50NC

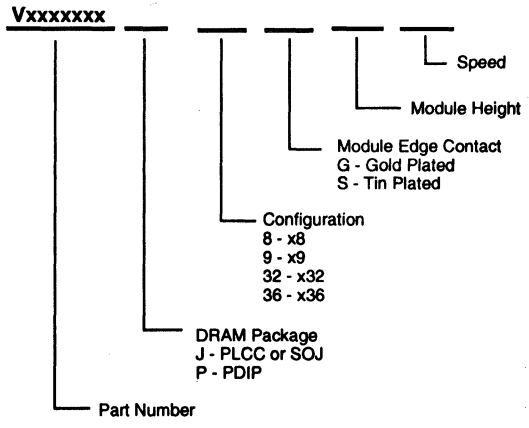
TI	MOSEL-VITELIC
SN74ACT7201A-35N	7201AL-35PC
SN74ACT7201A-50N	7201AL-50PC
SN74ACT7202-35N	7202AL-35PC
SN74ACT7202-50N	7202AL-50PC

RAMs





Modules



MOSEL-VITELIC QUALITY AND RELIABILITY ASSURANCE PROGRAM

Introduction

Mosel/Vitelic Corporation is committed to provide all products fabricated and tested to standards which assure that product quality and reliability shall exceed the requirements of our customers.

To meet this commitment, Mosel/Vitelic builds quality into all products by using the following procedures:

1. Products are developed using only proven design rules which are based upon demonstrated quality and reliability factors.
2. Products are fabricated using mature, stable processes which are already in high volume production in our wafer vendors' factories. Vitelic and our wafer vendors jointly monitor trends in key process and yield parameters to identify any potential shifts in the underlying processes.
3. Initial production lots of new products are evaluated thoroughly for quality and reliability and for manufacturability. If design or process changes are required during the life of a product, the modified product is treated as a new design and re-qualified completely.
4. New products are thoroughly characterized over a wide range of temperature and operating voltage conditions. Statistical distributions of key operating parameters are measured and parametric test programs are set to screen out any units of product with a measured parameter outside the normal distribution, even though these units may very well meet the standard product performance specification.
5. Data gathered at various quality inspection points in the product flow are charted and distributed to management, engineering and operating personnel to insure that conformance to quality standards is kept uppermost in all employees' minds and that problems are identified and resolved.
6. Quality and reliability of each product family are monitored on a continuous on-going basis for the life of the products. Characterization data and parameter distributions are re-measured periodically to insure that the product has not changed.
7. Improvements in product quality and reliability goals are part of the Mosel/Vitelic Corporate Objectives and Key Results Program, and progress in achieving improvements to meet these corporate goals is reviewed thoroughly at each operating unit of the company.

Examples of the application of these procedures are included in the following sections.

Initial Qualification Procedure for New Products

Initial qualification data is gathered for new products on samples from at least three separate production lots which have been manufactured after any initial fluctuations in design or process have been removed. The standard qualification tests for reliability include:

High-Temperature Operating Life
High-Temperature Storage Life
Low-Temperature Operating Life
Temperature/Humidity/Bias Life
Alpha Particle-Soft Errors
Temperature Cycle
Thermal Shock
Solderability
Lead Fatigue
Resistance to Solvents
Resistance to Electrostatic Discharge
Resistance to Electrostatic Latch-Up

These standard tests are designed to subject the finished product to controlled stresses which are outside the normal range of operating environment of the product. In most cases, an acceleration factor can be derived which relates the expected failure rate under normal operating conditions to the observed failure rate under accelerated operation. In accelerated tests such as High-Temperature Operating Life, the acceleration factors are based on well-established physical theory, such as temperature-activated process rate theory and electrical field-enhanced dielectric breakdown theory. In other tests, such as Temperature/Humidity/Bias Life and Pressure Pot Storage Life, the acceleration factors are very empirical and the tests serve only as comparative guidelines within the integrated circuit industry.

In either case, Mosel/Vitelic uses generally accepted test methods (Mil. Std 883, where applicable) and acceleration factors for measuring and reporting product quality and reliability results.

Up-to-date quality and reliability data on our products is available. Please contact your local Mosel/Vitelic sales office for information.

MOSEL-VITELIC

V53C256A FAMILY
HIGH PERFORMANCE, LOW POWER
256K X 1 BIT FAST PAGE MODE
CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C256A	60/60L	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns	45 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	15 ns	20 ns	25 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns	60 ns
Min. Read-Write Cycle Time, (t_{RC})	115 ns	130 ns	145 ns	175 ns

LOW POWER V53C256AL	60L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	1.2 mA	1.2 mA	1.2 mA	1.2 mA

2

Features

- Low power dissipation for V53C256A-10
  - Operating Current—60 mA max.
  - TTL Standby Current—3.5 mA max.
- Low CMOS Standby Current
  - V53C256A—3.0 mA max.
  - V53C256AL—1.2 mA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Common I/O capability
- Fast Page Mode operation for a sustained data rate greater than 21 MHz.
- 256 Refresh cycles/4 ms
- Standard packages are 16 pin Plastic DIP and 18 pin PLCC

Description

The V53C256A is a high speed 262,144 x 1 bit CMOS dynamic random access memory. Fabricated with VICMOS III technology, the V53C256A offers a combination of size and features unattainable with NMOS technology: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, for the V53C256AL, reduced CMOS standby mode supply current (I_{DD6}).

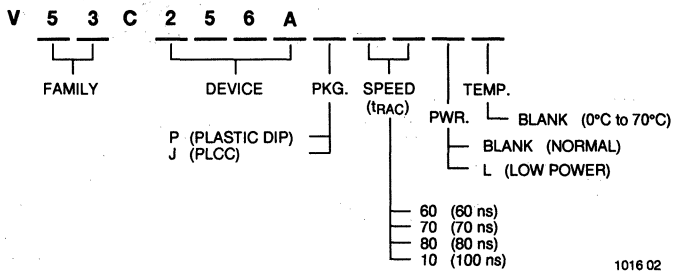
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random or sequential access of up to 512 bits within a row with cycle times as short as 50 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical timing requirements for fast usable speed. These features make the V53C256 ideally suited for cache based mainframe and mini computers, graphics, digital signal processing and high performance microprocessor systems.

The V53C256AL-10 offers a maximum data retention power of 10 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. This mode is entered by holding RAS at a voltage greater than V_{DD}–0.2 when it is inactive.

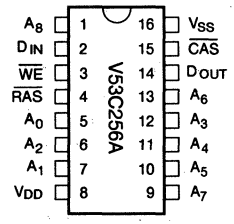
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power		Temperature Mark
	P	J	60	70	80	100	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	•	Blank

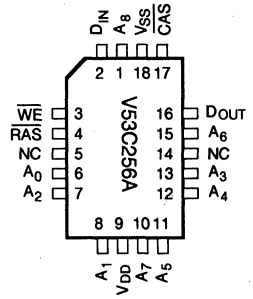
Package	Pkg.	Pin Count
Plastic DIP	P	16
PLCC	J	18



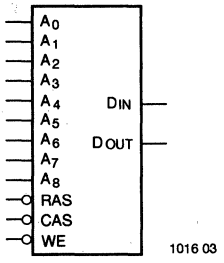
16 Lead Plastic DIP PIN CONFIGURATION Top View



18 Lead PLCC Package PIN CONFIGURATION Top View



LOGIC SYMBOL



Absolute Maximum Ratings*

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} .....–1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS} .....–1.0 V to +7.0 V
Data Out Current .....50 mA
Power Dissipation .....1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

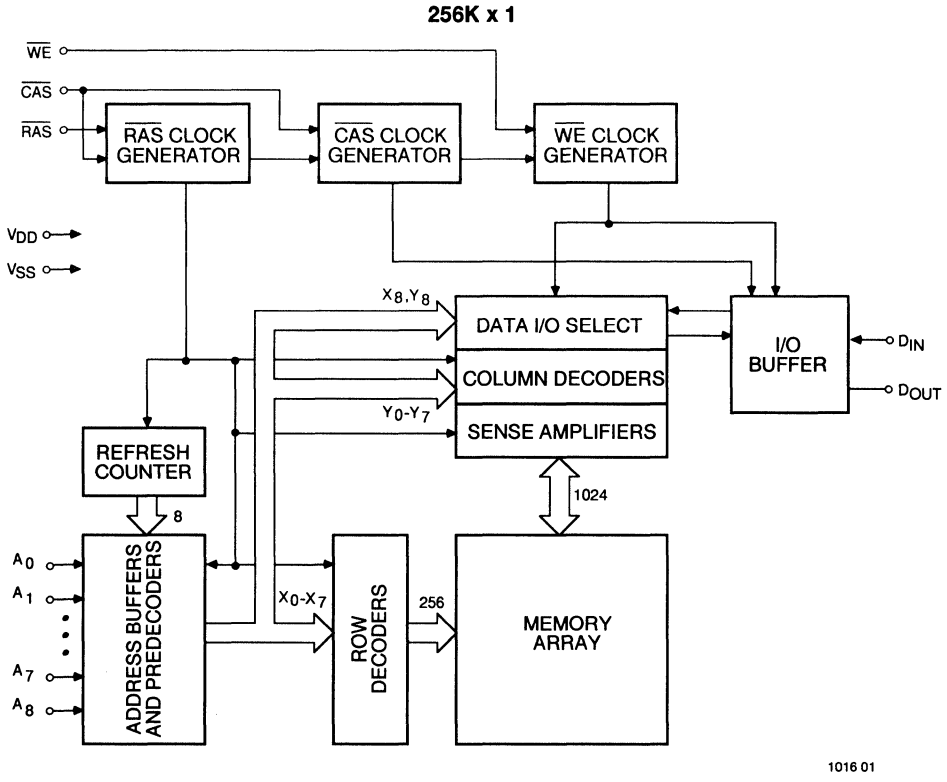
Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address, D_{IN}	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	4	5	pF
C_{OUT}	D_{OUT}	4	6	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C256A		V53C256AL		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10	10	−10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10	10	−10	10	µA	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60		80		80	mA	$t_{RC} = t_{RC}$ (min.)	1,2
		70		70		70			
		80		65		65			
		100		60		60			
I_{DD2}	V_{DD} Supply Current, TTL Standby			3.5		2.0	mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60		80		80	mA	$t_{RC} = t_{RC}$ (min.)	2
		70		70		70			
		80		60		60			
		100		50		50			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60		50		50	mA	Minimum Cycle	1,2
		70		45		45			
		80		40		40			
		100		35		35			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			4		2.5	mA	$\overline{RAS}$=V_{IH},$\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby			3		1.2	mA	$\overline{RAS} \ge V_{DD}$ −0.2 V, $\overline{CAS} = V_{IH}$, other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage (all inputs)		−1	0.8	−1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)		2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4		V	I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	115		130		145		175		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	45		50		55		65		ns	
4	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
5	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		15		15		15		ns	
6	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		40		45		ns	
7	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	20	35	20	40	20	55	ns	4
8	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
9	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10		15		15		20		ns	
10	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	25	55	25	60	25	75	ns	5
11	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	6,7,8
12	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40		45 15	ns	8,9,
13	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		15		15		20		25	ns	8,15
14	$t_{CL1CH1(R)}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	15	75K	15	75K	20	75K	25	75K	ns	
15	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15		15		20		25		ns	
16	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
17	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		5		5		5		ns	10
18	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		5		ns	10
19	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		15		15		15		ns	
20	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	15	0	15	0	20	0	25	ns	11

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CH2QV}	t_{OH}	Data Hold Time from $\overline{CAS}$	0		0		0		0		ns	11
22	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		15		20		ns	
23	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
24	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		70		ns	
25	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	20		20		25		30		ns	
26	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		25		25		30		ns	
27	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		70		ns	
28	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12,13
29	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		15		15		20		ns	
30	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		0		ns	14
31	t_{WH1DX}	t_{DH}	Data In Hold Time	15		15		15		20		ns	14
32	t_{RL1DX}	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	50		55		60		70		ns	
33	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	140		155		175		210		ns	
34	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	85		95		110		135		ns	
35	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay In Read-Modify-Write Cycle	60		70		80		100		ns	12
36	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	15		15		20		25		ns	12
37	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	30		35		40		45		ns	12
38	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50		55	ns	15
39	$t_{CL2CL2(R)}$	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		60		ns	

AC Characteristics (Cont'd.)

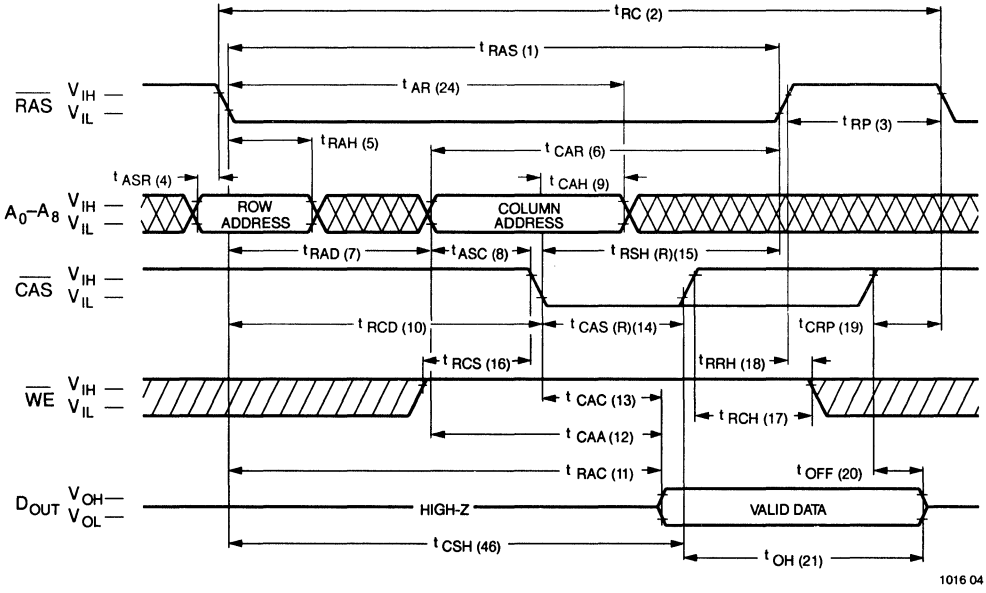
#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
40	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	70		75		85		95		ns	
41	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		30		ns	
42	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		30		ns	
43	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
44	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		10		ns	
45	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	15		20		25		30		ns	
46	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
47	t_T	t_T	Transition Time (Rise and Fall)	3	25	3	25	3	25	3	25	ns	16
		t_{RI}	Refresh Interval (256 Cycles)	4			4		4		4	ms	17

2

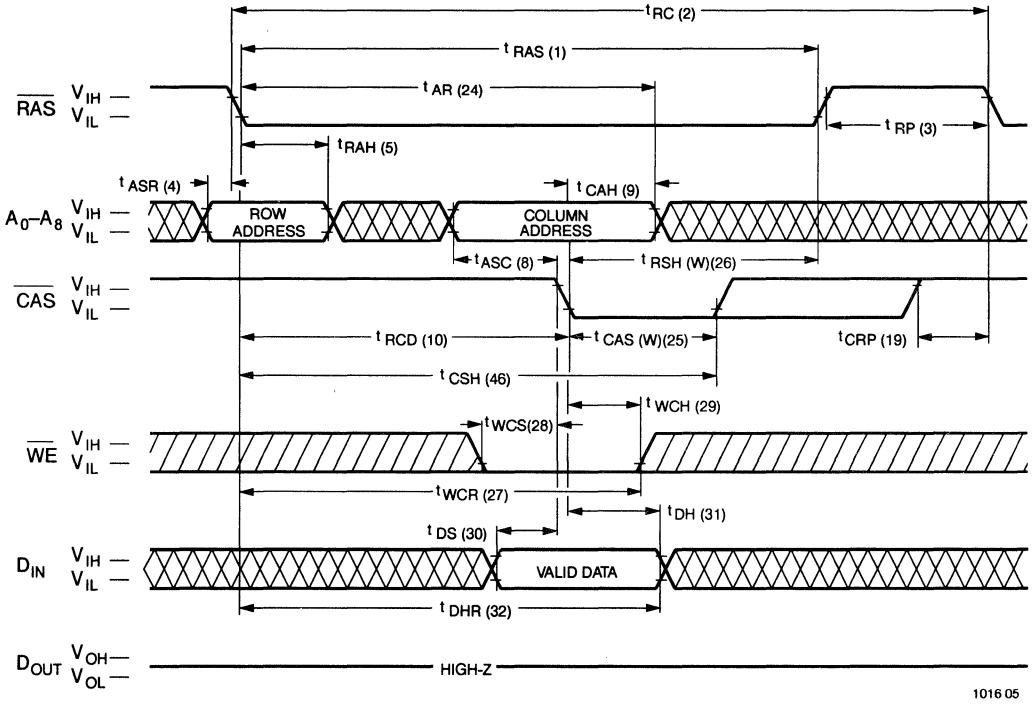
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} (min.) may undershoot to −1.0 V for periods not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
5. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limits ensure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
6. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
8. Measured with a load equivalent to two TTL inputs and 100 pF in parallel.
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
10. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
11. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the later occurance of $\overline{CAS}$ or $\overline{WE}$.
15. Access time is determined by the longer of t_{CAA}, t_{CAC}, or t_{CAP}.
16. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC measurements assume t_T = 5 ns.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

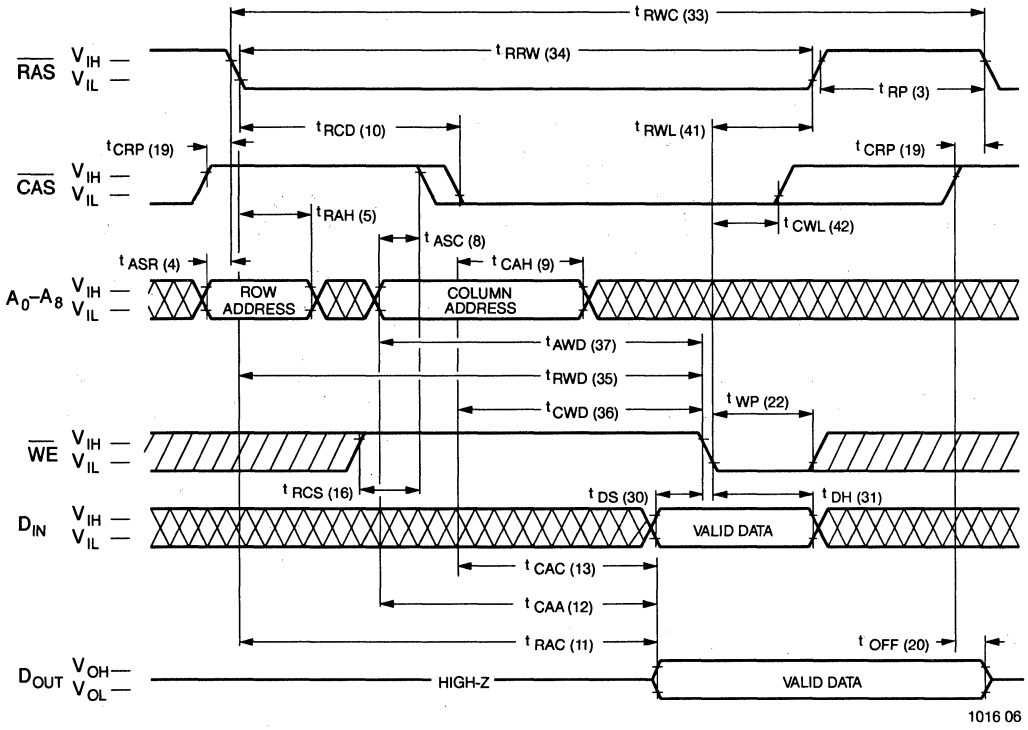
Waveforms of Read Cycle



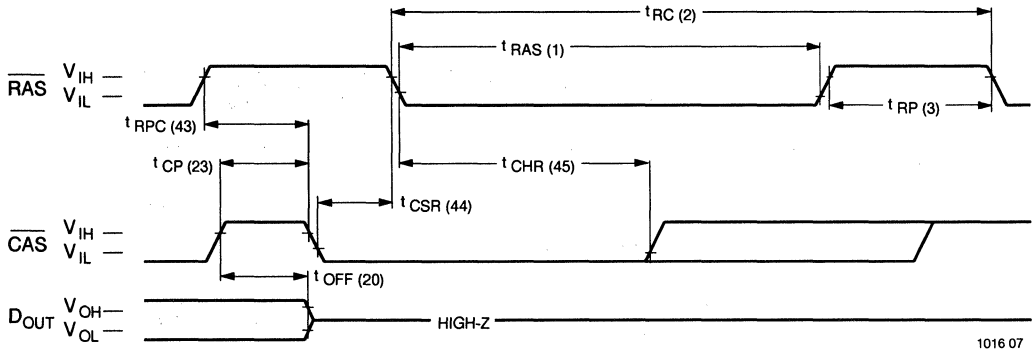
Waveforms of Early Write Cycle



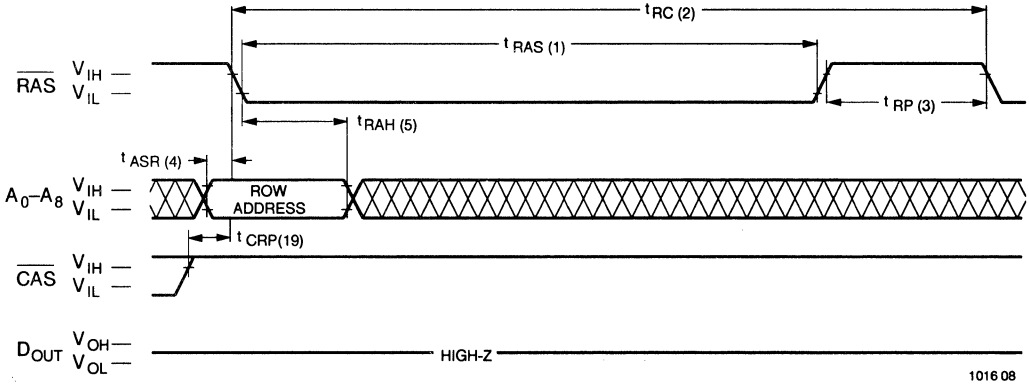
Waveforms of Read-Modify-Write Cycle



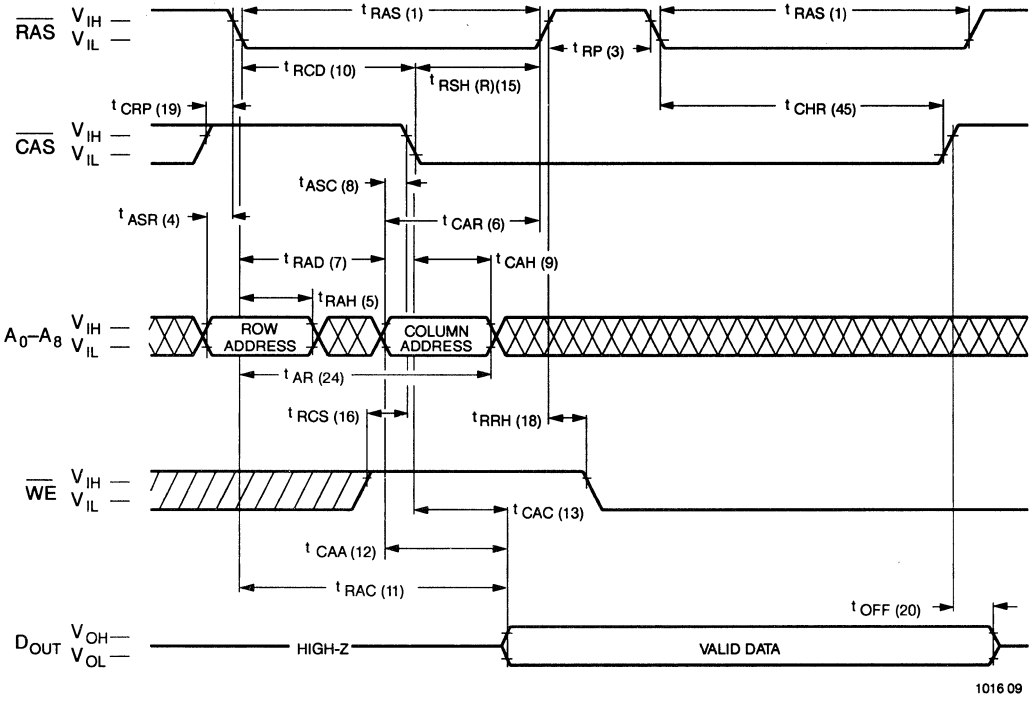
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



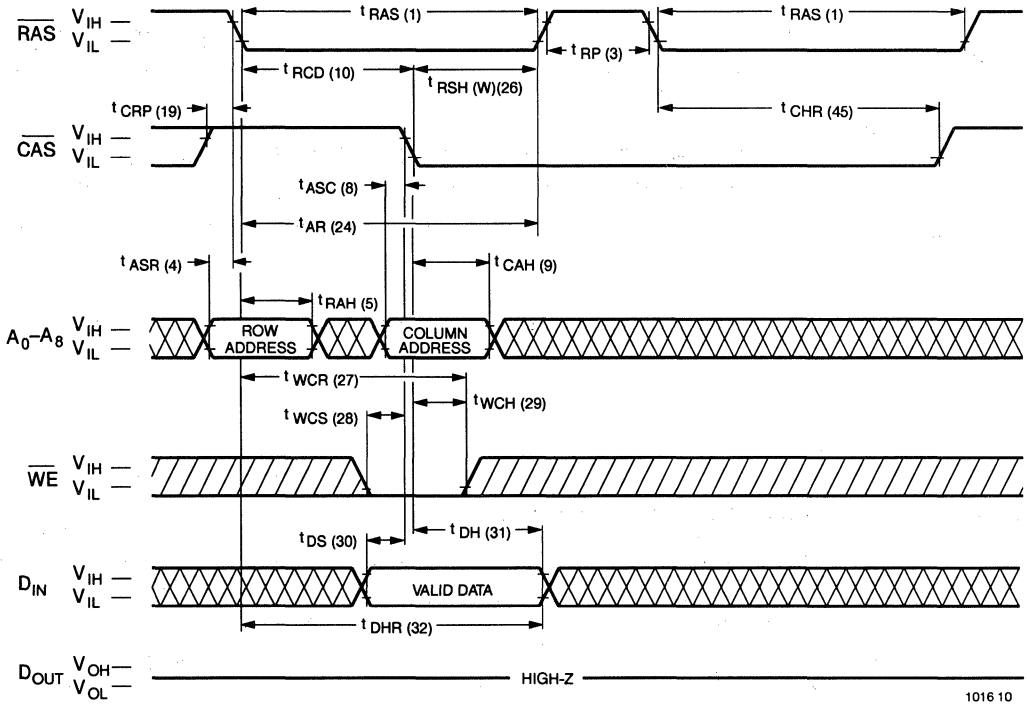
Waveforms of $\overline{RAS}$-Only Refresh Cycle



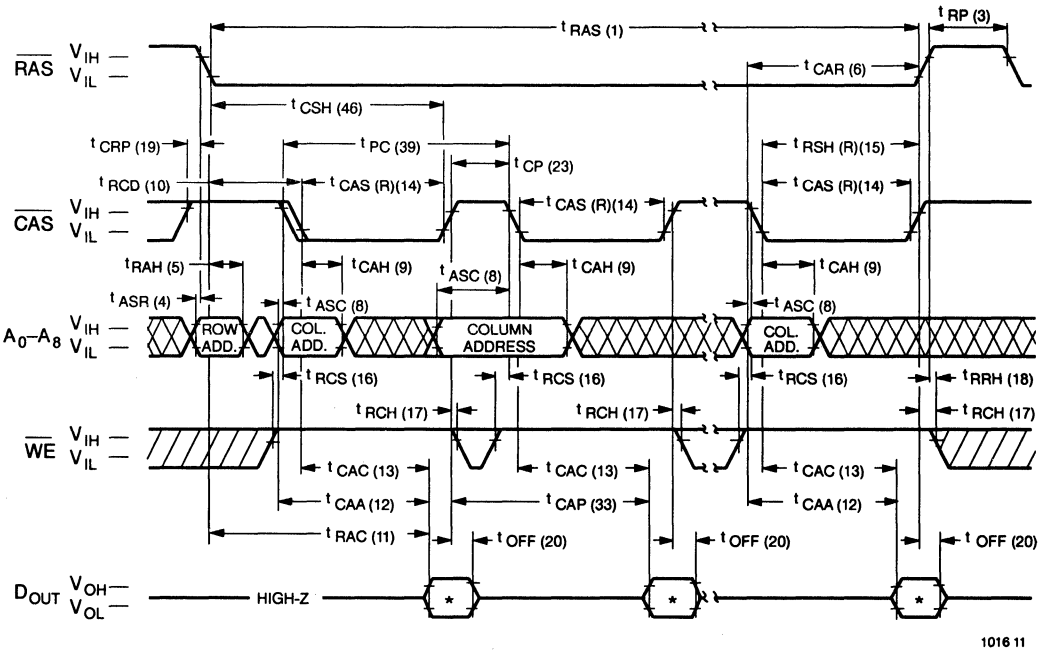
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)

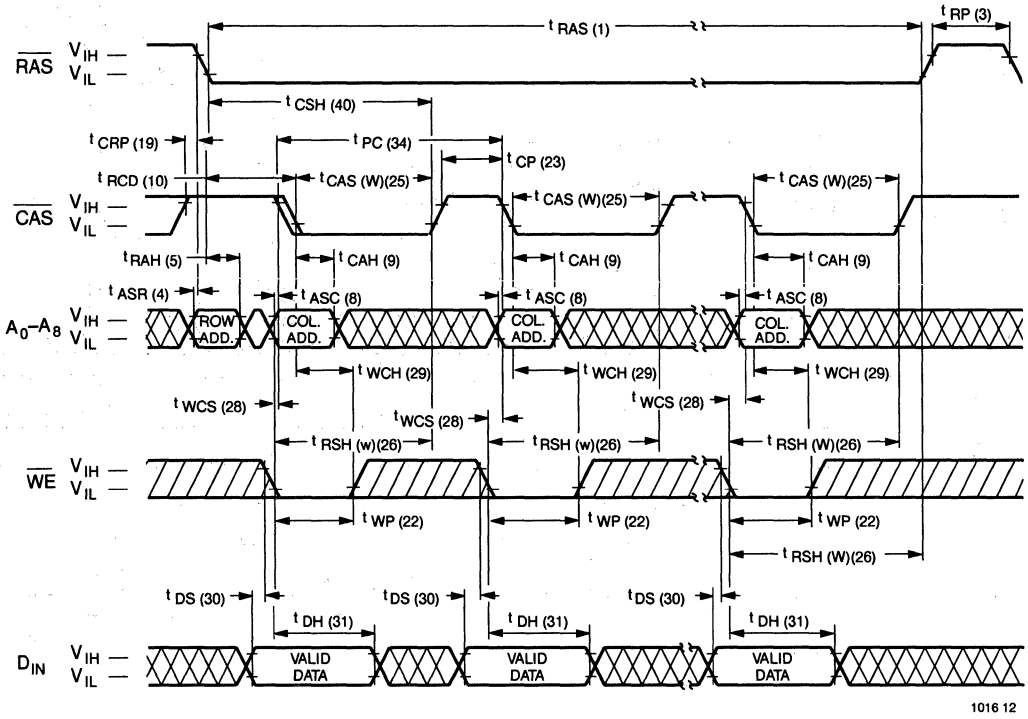


Waveforms of Fast Page Mode Read Cycle

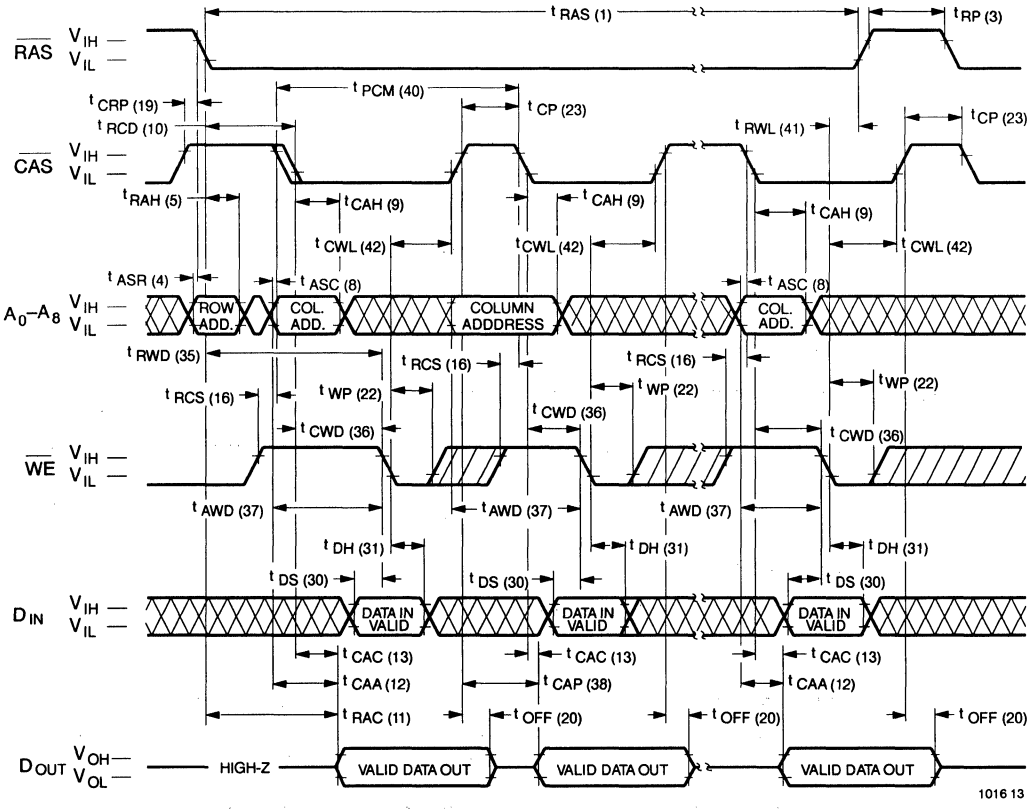


* Valid Data

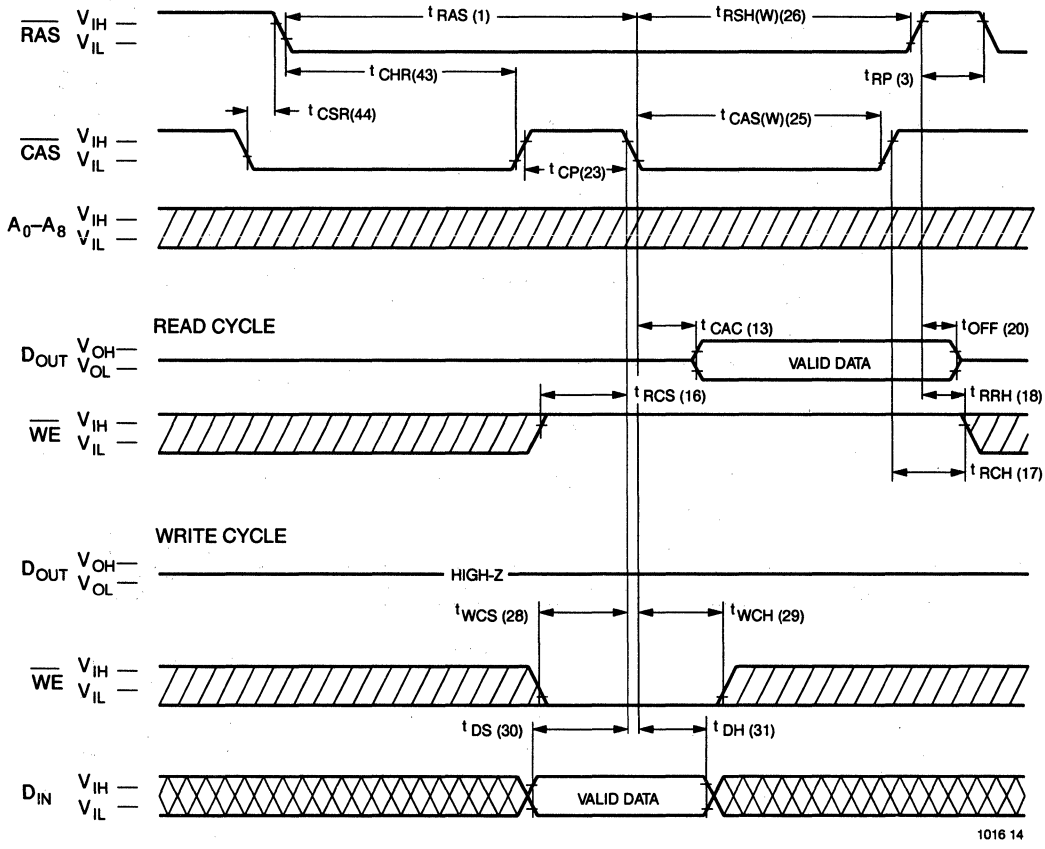
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Modify-Write Cycle



Waveforms of Refresh Counter Test Cycle



Functional Description

The V53C256A is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C256A reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the presice time that the $\overline{CAS}$ edge occurs, the delay from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} (min.) and t_{CAC} (min.) are both satisfied.

Write Cycle

A write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled write cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the output (D_{OUT}) pin will be in the High-Z state at the beginning of the Write function. Ending the write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

Refresh Cycle

To retain data, 256 refresh cycles are required in each 4 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_7) with $\overline{RAS}$ at least once every 4 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C256A will use the output of an internal 8-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, D_{OUT} will remain in the High-Z state during the cycle.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to write consecutive data patterns (256 write cycles) and then verify the written data by applying 256 consecutive read cycles. In this mode, the V53C256A ignores external row/column addresses and takes the output from the internal counter instead.

Data Retention Mode

The V53C256A offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C256A power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 256

Fast Page Mode Operation

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high.

Thus, access begins at the occurance of a valid column address rather than at the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as on output enable.

During Fast Page Mode operation, Read, Write, Read-Modify-Write, or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is determined by the by the $\overline{CAS}$ rising edge. If the column address is valid after the rising edge of $\overline{CAS}$, the access is timed from the occurrance of the valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 19 MHz for applications that require high data rates like bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Data Output Operation

The V53C256A Data Output pin (D_{OUT}) has a three-state capability and is controlled by $\overline{CAS}$. When $\overline{CAS}$ is high($\geq V_{IH}$), the output is in the High-Z state. Table 1 summarizes the D_{OUT} states possible for various memory cycles.

Power-On

After application of the V_{DD} an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval). During Power-On, the V_{DD} current requirement of the V53C256A is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C256A Data Output
Operation for Various Cycle Types

Cycle Type	D_{OUT} State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	Active, not valid
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

V53C464A FAMILY
HIGH PERFORMANCE, LOW POWER
64K X 4 BIT FAST PAGE MODE
CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C464A	60/60L	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns	45 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns	65 ns
Min. Read-Write Cycle Time, (t_{RC})	115 ns	130 ns	145 ns	175 ns

LOW POWER V53C464AL	60L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	1.2 mA	1.2 mA	1.2 mA	1.2 mA

2

Features

- Low power dissipation for V53C464A-10
  - Operating Current—65 mA max.
  - TTL Standby Current—3.5 mA max.
- Low CMOS Standby Current
  - V53C464A—3 mA max.
  - V53C464AL—1.2 mA max.
- Read-Modify-Write, $\overline{RAS}$-only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Fast Page Mode operation for a sustained data rate greater than 21 MHz
- 256 Refresh cycles/4 ms
- Standard packages are 18 pin Plastic DIP and 18 pin PLCC

Description

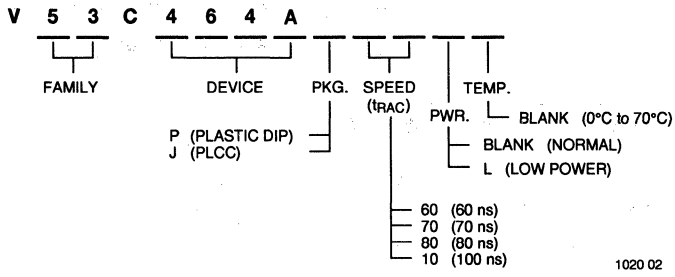
The V53C464A is a high speed 65,536 x 4 bit CMOS dynamic random access memory. Fabricated with VICMOS III technology, the V53C464A offers a combination of size and features unattainable with NMOS technology: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request extended refresh for very low data retention power (V53C464AL).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 256 (x4) bits within a row with cycle times as short as 45 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C464A ideally suited for graphics, digital signal processing and high performance computing systems.

The V53C464AL-10 offers a maximum data retention power of 10 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. For selected V53C464AL devices with Refresh Interval longer than 4 ms, consult the factory.

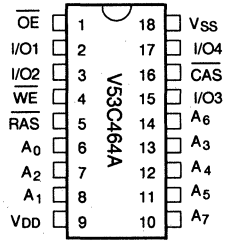
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power		Temperature Mark
	P	J	60	70	80	100	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	•	Blank

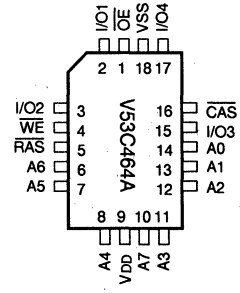


Description	Pkg.	Pin Count
Plastic DIP	P	18
PLCC	J	18

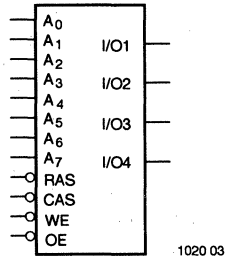
18 Lead Plastic DIP PIN CONFIGURATION Top View



18 Lead PLCC Package PIN CONFIGURATION Top View



LOGIC SYMBOL



Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... −1.0V to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... −1.0V to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

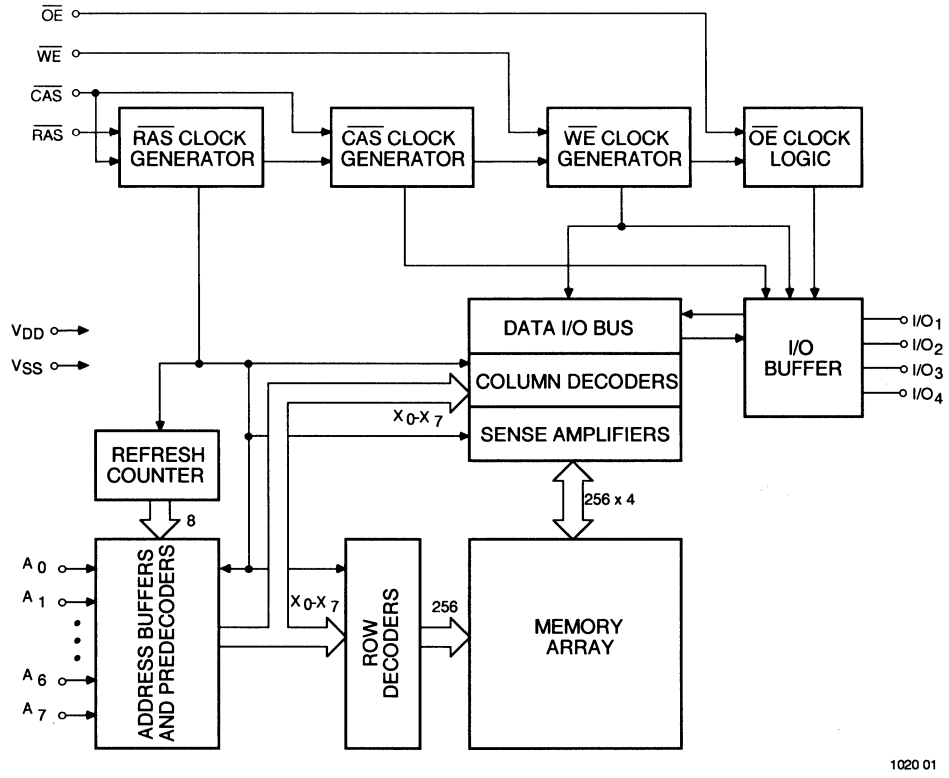
T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	I/O	4	6	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram

64K x 4



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C464A		V53C464AL		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10	10	–10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10	10	–10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60		80		80	mA	$t_{RC} = t_{RC}$ (min.)	1,2
		70		75		75			
		80		70		70			
		100		65		65			
I_{DD2}	V_{DD} Supply Current, TTL Standby			3.5		2.0	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60		80		80	mA	$t_{RC} = t_{RC}$ (min.)	2
		70		75		75			
		80		65		65			
		100		55		55			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60		50		50	mA	Minimum Cycle	1,2
		70		45		45			
		80		40		40			
		100		35		35			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			4		2.5	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby			3		1.2	mA	$\overline{RAS} \ge V_{DD}$ –0.2 V, $\overline{CAS}$ at V_{IH}, other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage		–1	0.8	–1	0.8	V		3
V_{IH}	Input High Voltage		2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4		V	I_{OH} = –5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted
AC Test conditions, input pulse levels 0 to 3 V

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	115		130		145		175		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	45		50		55		65		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		20		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	40	25	45	25	50	25	65	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		15		15		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	10		15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		25		30		35		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		15		15		15		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		5		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		5		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	15		15		20		25		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		15		15		20		25	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20		20		25	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40		45	ns	6,7,10

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	17
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	10	0	15	0	20	0	25	ns	17
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		70		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	20	35	20	40	20	55	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		25		30		35		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		30		35		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		15		15		20		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		15		20		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		70		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		30		35		ns	
32	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data In Hold Time	10		15		15		20		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	10		20		20		25		ns	
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	15		20		25		30		ns	
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	170		185		210		250		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	105		125		145		175		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	40		50		60		70		ns	12

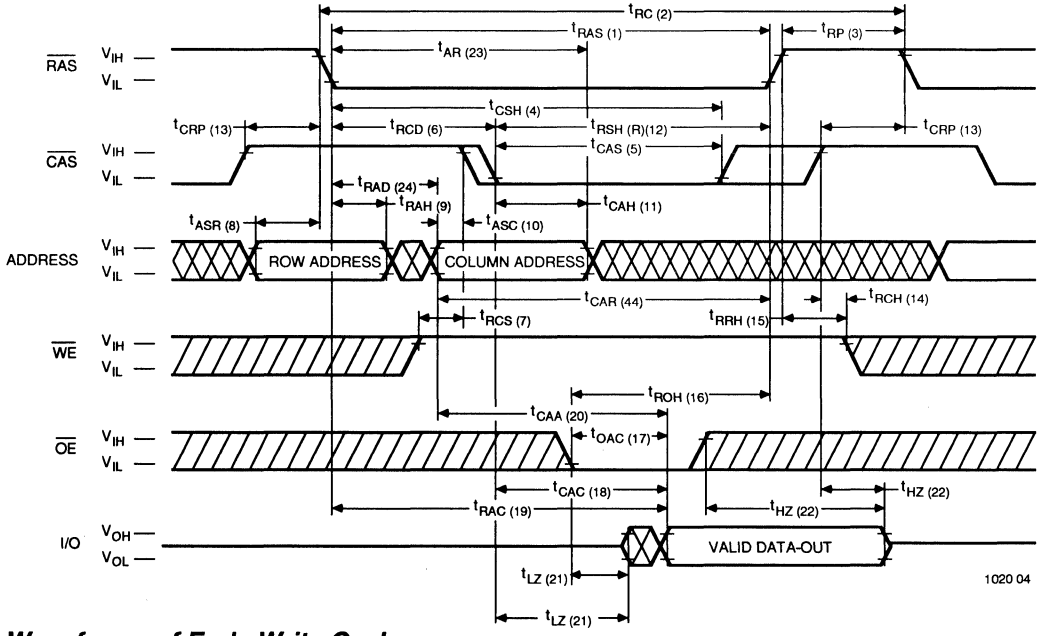
AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	80		95		110		135		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	65		80		95		110		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	50		60		70		80		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		65		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		40		45		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50		55	ns	6, 7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	50		55		60		70		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	15		20		25		30		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	85		105		120		140		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (256 Cycles)		4		4		4		4	ms	16

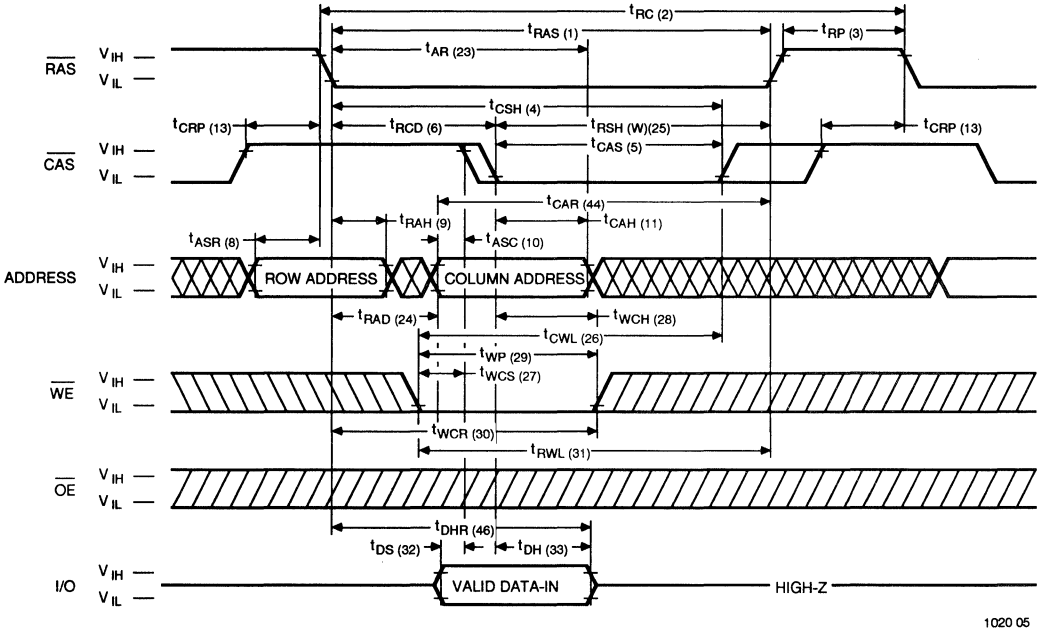
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
17. Assumes a three-state test load of 5 pF and a 380 Ohm Thevenin equivalent.

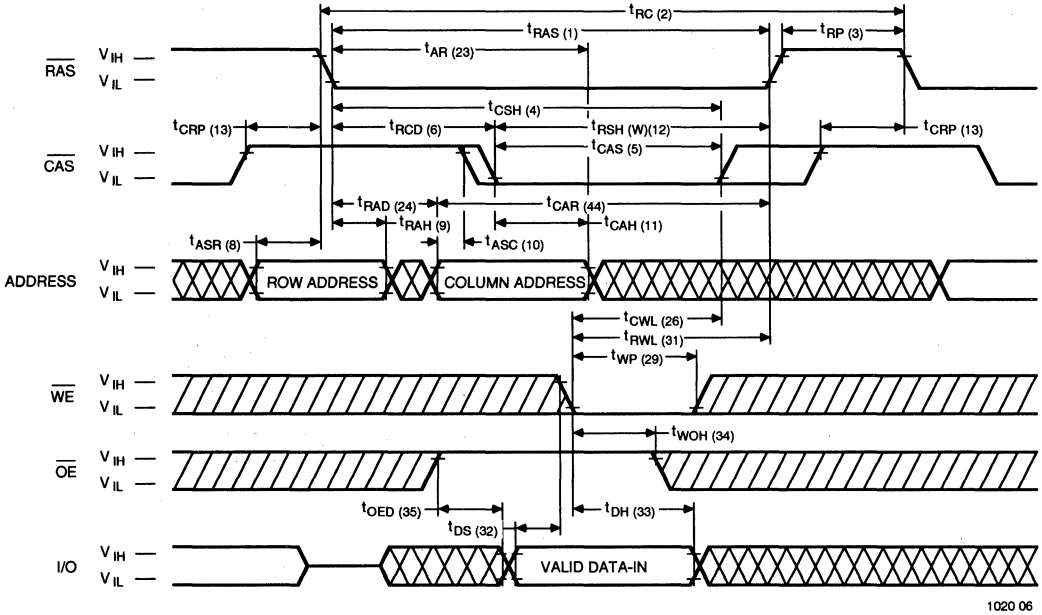
Waveforms of Read Cycle



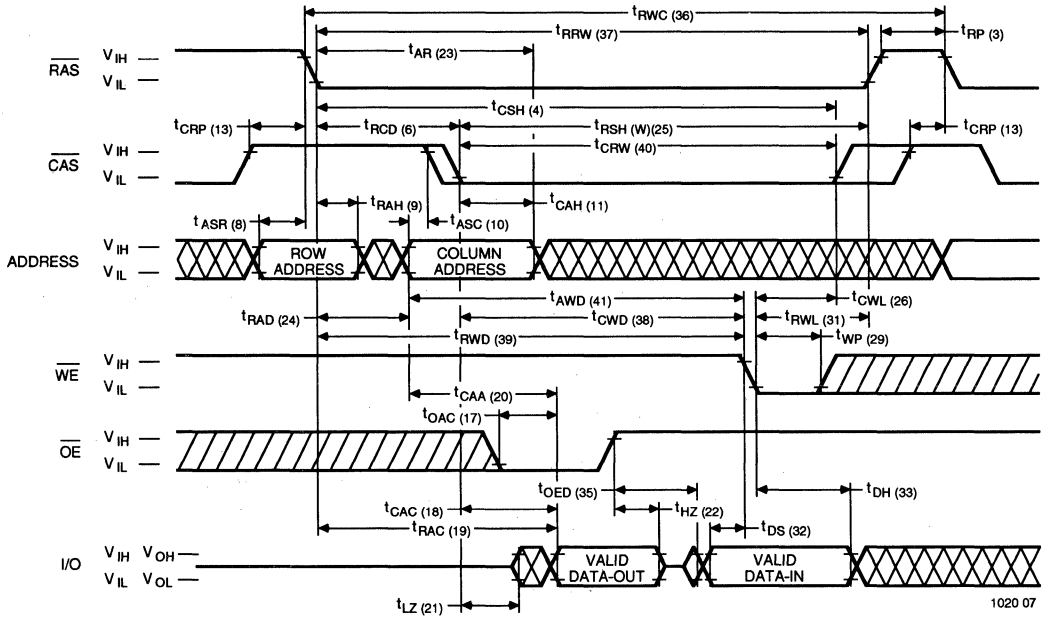
Waveforms of Early Write Cycle



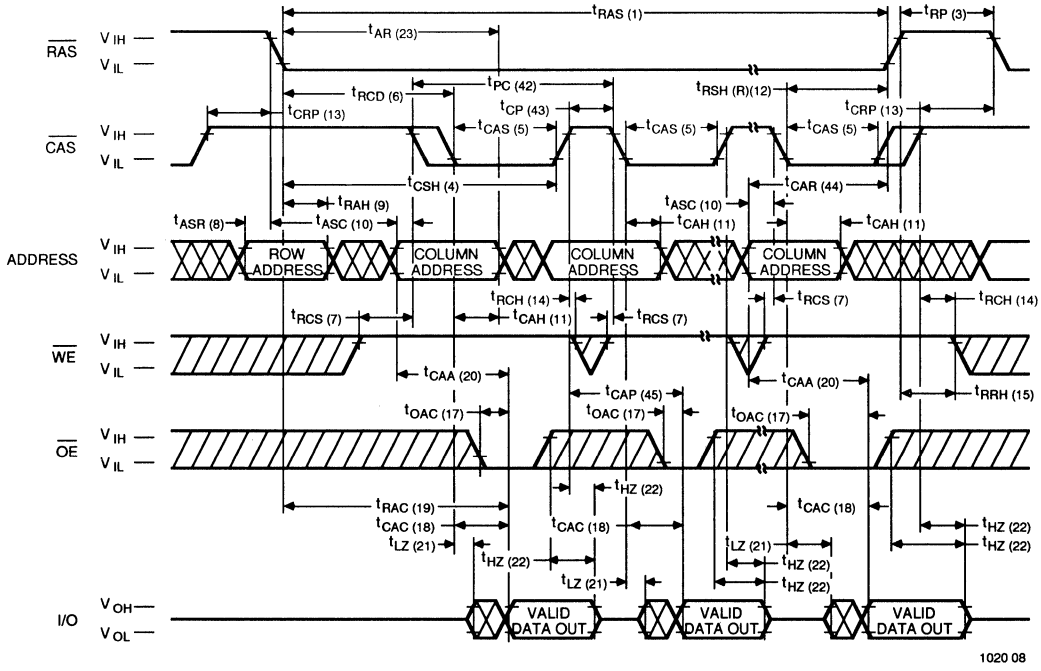
Waveforms of $\overline{OE}$ Controlled Write Cycle



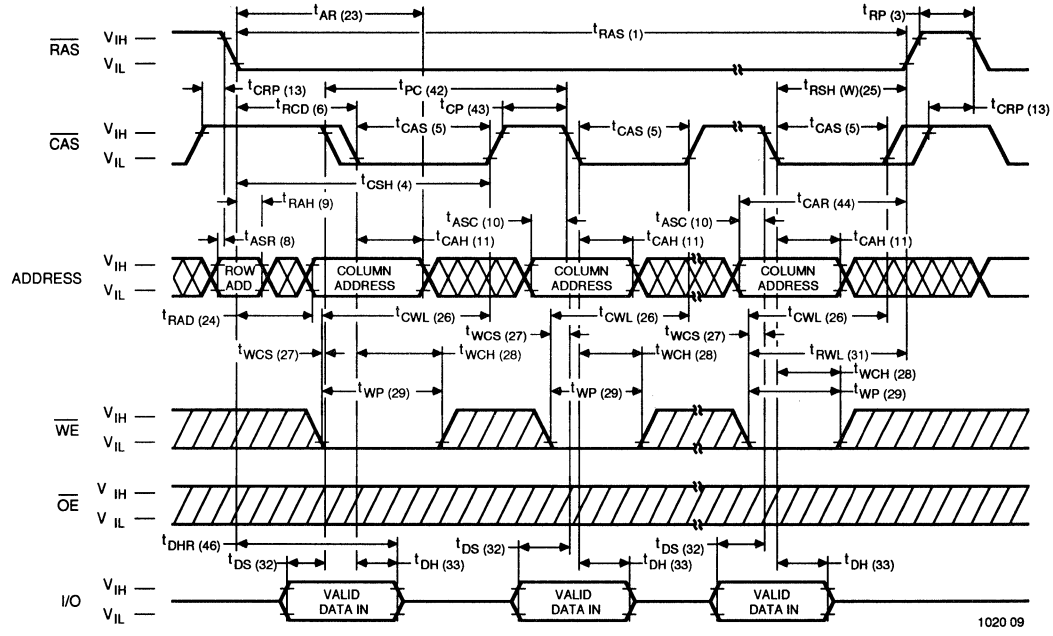
Waveforms of Read-Modify-Write Cycle



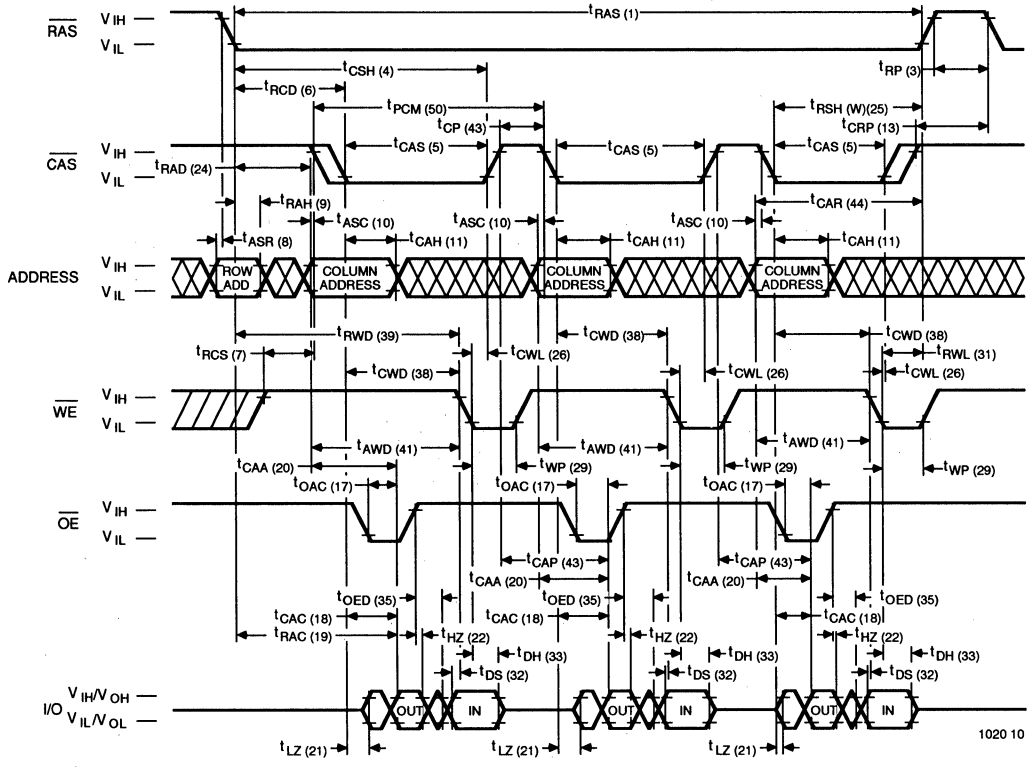
Waveforms of Fast Page Mode Read Cycle



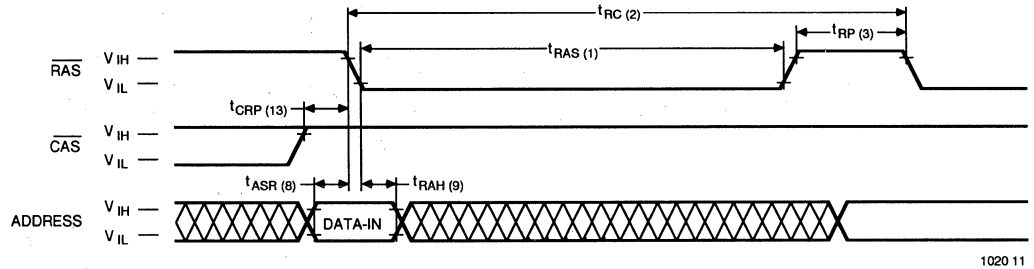
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Write Cycle

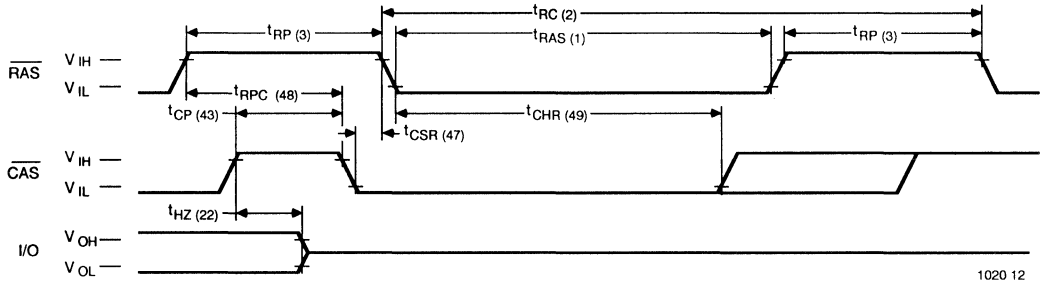


Waveforms of $\overline{RAS}$-Only Refresh Cycle



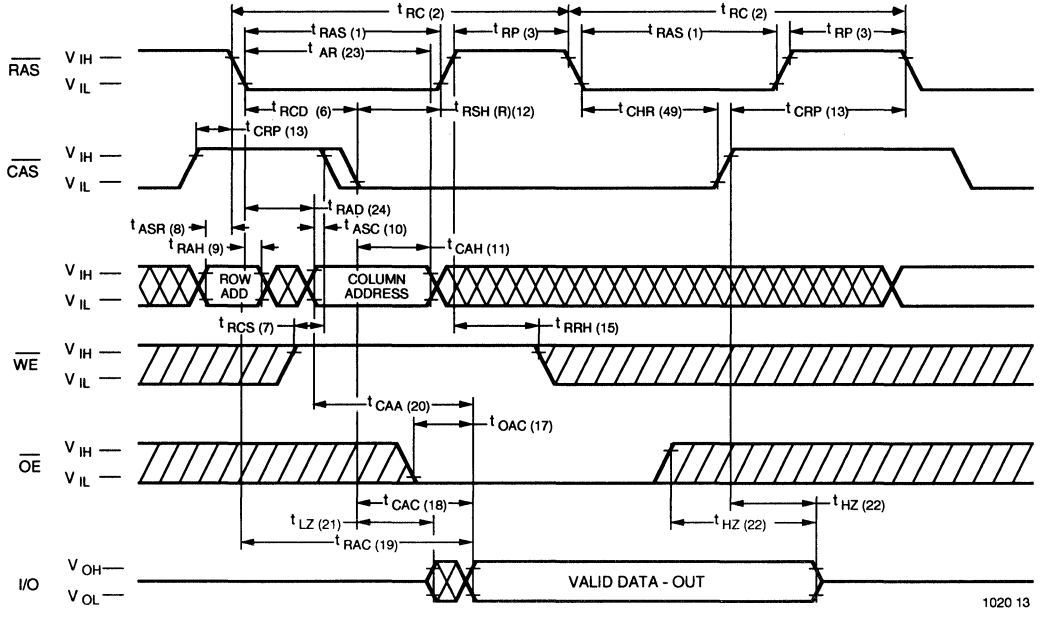
NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

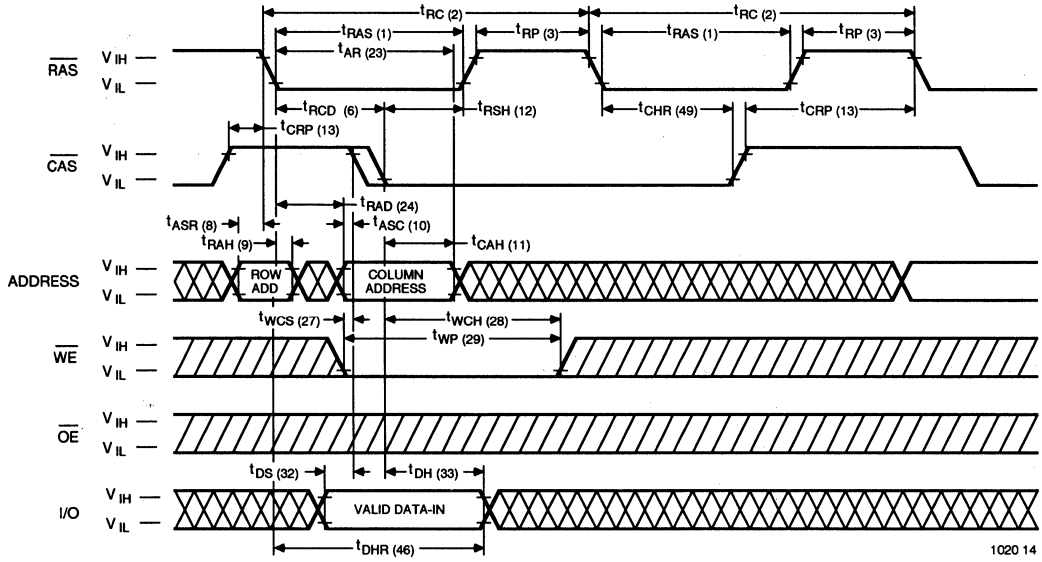


NOTE: $\overline{WE}$, $\overline{OE}$, A_0, A_7 = Don't care

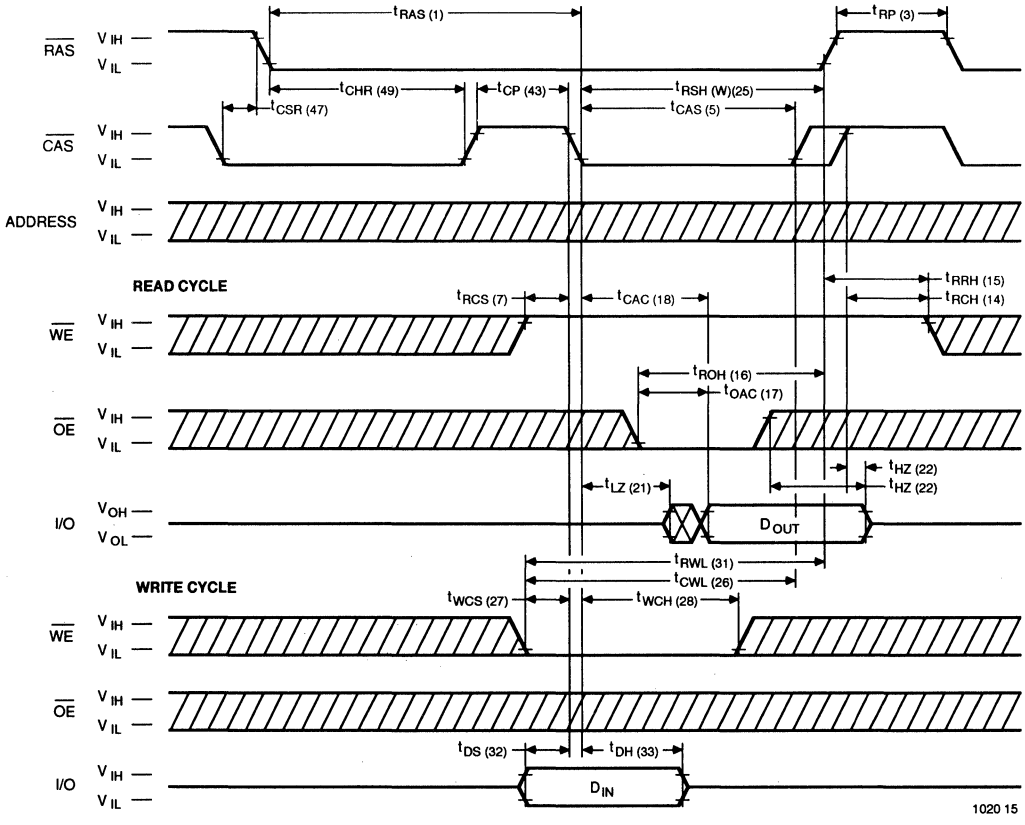
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C464A is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C464A reads and writes data by multiplexing a 16-bit address into an 8-bit row and an 8-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This insures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$-controlled or $\overline{CAS}$-controlled, depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$-controlled Write Cycle, $\overline{OE}$ must be in the high state, and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 256 Refresh Cycles are required in each 4 ms period. There are two ways to refresh the memory:

1. By selecting each of the 256 row addresses determined by A_0 through A_7 at least once every 4 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ is low during the falling edge of $\overline{RAS}$, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C464A will use the output of an internal 8-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output will remain in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C464A offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C464A power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 256

Fast Page Mode Operation

Fast Page Mode operation permits all 256 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing succesive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edgeand is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 19 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255 \times t_{PC}}$$

Data Output Operation

The V53C464A Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required, followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C464A is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle, and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C464A Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High–Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High–Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

HIGH PERFORMANCE, LOW POWER 1M X 1 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C100F	60/60L	70/70L	80/80L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	20 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read-Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns

LOW POWER V53C100FL	60L	70L	80L
Max. CMOS Standby Current, (I_{DD6})	200 µA	200 µA	200 µA

Features

- 1M x 1-bit organization
- Low power dissipation for V53C100F-80
  - Operating Current – 70 mA max.
  - TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C100F – 1.0 mA max.
  - V53C100FL – 0.2 mA max.
- Read-Modify-Write, RAS-Only Refresh, CAS-before-RAS Refresh capability
- Common I/O capability
- Refresh Interval
  - V53C100F – 512 cycles/8ms
  - V53C100FL – 512 cycles/64ms
- Fast Page Mode operation for a sustained data rate greater than 25 MHz
- Standard packages are 18 pin Plastic DIP and 26/20 pin SOJ
- Low Battery Back-up Current
  - V53C100FL – 300 µA max.
  - 200 µA max. available on request

Description

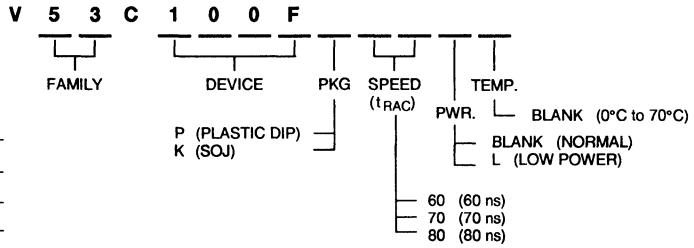
The V53C100F is a high speed 1,048,576 x 1 bit CMOS dynamic random access memory. The V53C100F offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random or sequential access of up to 1024 bits within a row with cycle times as short as 40 ns. Because of static circuitry, the CAS clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical timing requirements for fast usable speed. These features make the V53C100F ideally suited for cache based mainframe and mini computers, graphics, digital signal processing and high performance microprocessor systems.

The V53C100FL offers a maximum data retention power of 1.65 mW when operating in CMOS standby mode and performing CAS-before-RAS refresh cycles.

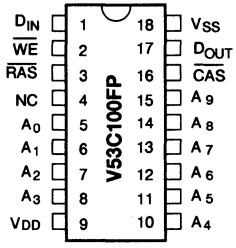
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	60	70	80	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank

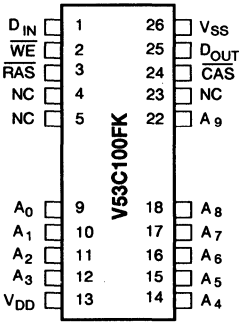


Description	Pkg.	Pin Count
Plastic DIP	P	18
SOJ	K	26/20

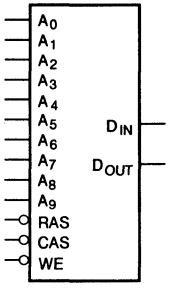
18 Lead Plastic DIP PIN CONFIGURATION
Top View



26/20 Lead SOJ Package PIN CONFIGURATION
Top View



LOGIC SYMBOL



Pin Names

A_0–A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{DD}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... −1.0 V to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

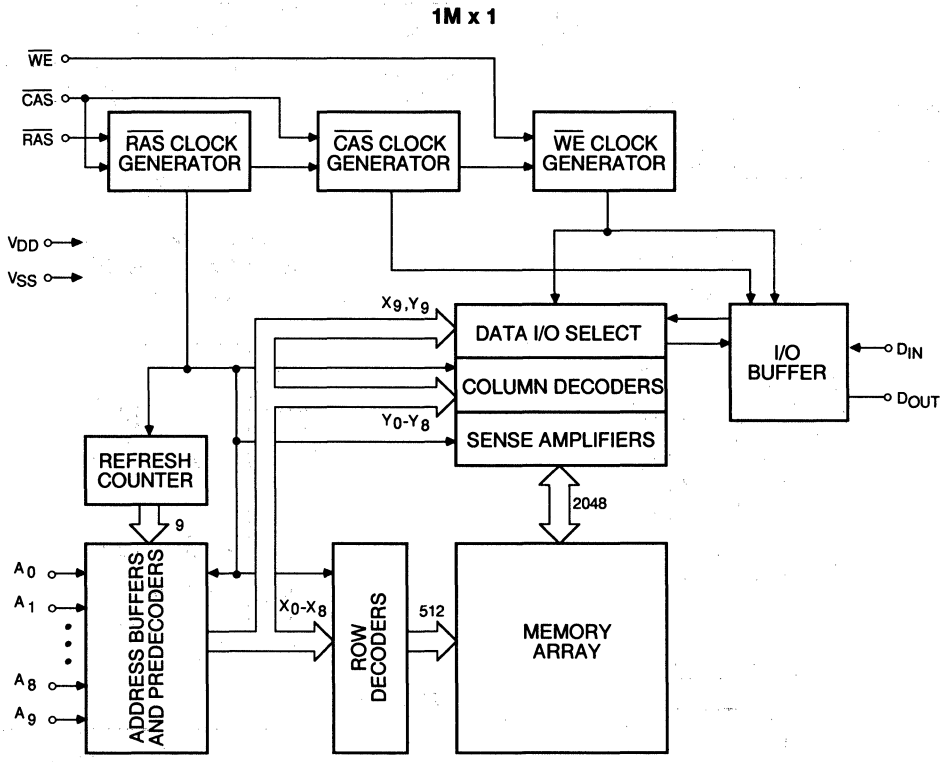
Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	7	pF
C_{OUT}	I/O	—	7	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C100F		V53C100FL		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10	10	−10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10	10	−10	10	µA	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60		90		90	mA	$t_{RC} = t_{RC}$ (min.)	1,2
		70		80		80			
		80		70		70			
I_{DD2}	V_{DD} Supply Current, TTL Standby			2.0		2.0	mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60		90		90	mA	$t_{RC} = t_{RC}$ (min.)	2
		70		80		80			
		80		70		70			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60		80		80	mA	Minimum Cycle	1,2
		70		70		70			
		80		60		60			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			3.0		2.0	mA	$\overline{RAS}$=V_{IH},$\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby			1.0		0.2	mA	$\overline{RAS} \ge V_{DD}$ −0.2 V, $\overline{CAS} \ge V_{DD}$ −0.2 V, other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage (all inputs)		−1	0.8	−1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)		2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4		V	I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	ns	
2	t_{RL2RL}	t_{RC}	Read or Write Cycle Time	120		130		150		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		ns	
4	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
5	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		10		ns	
6	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		40		ns	
7	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	4
8	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
9	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		ns	
10	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	ns	5
11	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	6,7,8
12	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40	ns	8,9, 15
13	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		15		20		20	ns	8,15
14	$t_{CL1CH1(R)}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	15	75K	20	75K	20	75K	ns	
15	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15		20		20		ns	
16	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
17	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	10
18	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	10
19	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
20	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	ns	11

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CH2QV}	t_{OH}	Data Hold Time from $\overline{CAS}$	0		0		0		ns	11
22	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		15		ns	
23	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
24	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
25	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	15		20		20		ns	
26	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	15		20		20		ns	
27	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
28	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
29	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		15		15		ns	
30	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		ns	14
31	t_{WH1DX}	t_{DH}	Data In Hold Time	15		15		15		ns	14
32	t_{RL1DX}	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
33	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	140		155		175		ns	
34	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	80		95		105		ns	
35	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time Read-Modify-Write Cycle	60		70		80		ns	12
36	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	15		20		20		ns	12
37	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	30		35		40		ns	12
38	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		35		40		45	ns	15
39	$t_{CL2CL2(R)}$	t_{PC}	Fast Page Mode Read or Write Cycle Time	40		45		50		ns	

AC Characteristics (Cont'd.)

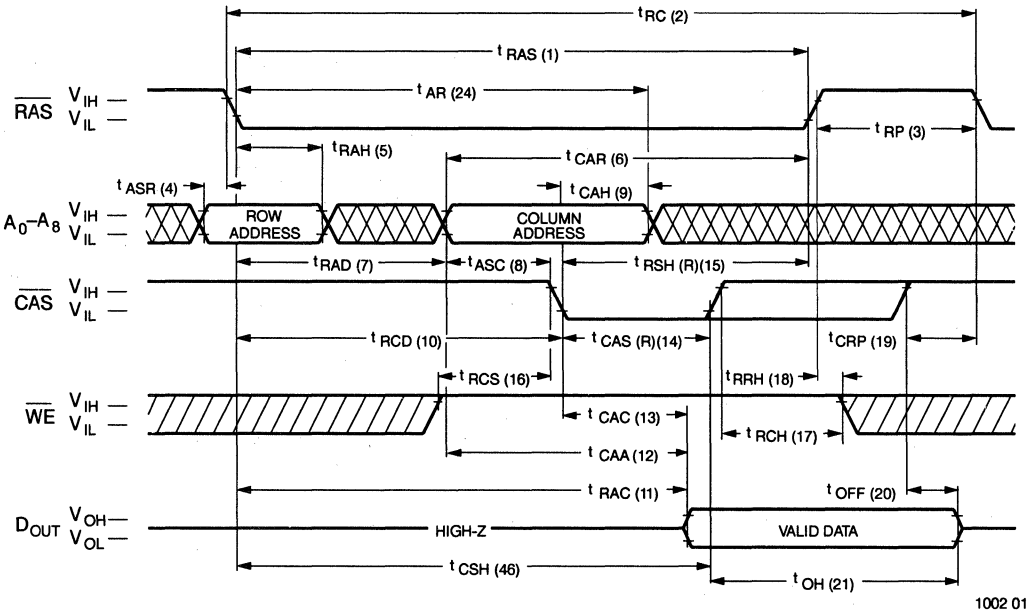
#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
40	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	60		70		75		ns	
41	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		ns	
42	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		ns	
43	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
44	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
45	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	30		30		30		ns	
46	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
47	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	16
		t_{REF}	Refresh Interval (512 Cycles)		8		8		8	ms	17
		t_{REF}	Refresh Interval V53C100FL only (512 Cycles, t_{RC} = 125 µs)		64		64		64	ms	18

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in First Page Mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} (min.) may undershoot to −1.0 V for periods not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
5. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limits ensure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
6. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
10. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
11. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
12. t_{WCS}, t_{WHC}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the later occurance of $\overline{CAS}$ or $\overline{WE}$.
15. Access time is determined by the longer of t_{CAA}, t_{CAC}, or t_{CAP}.
16. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC measurements assume t_T = 5 ns.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
    t_{RC} = 125 µs (125 µs x 512 = 64 ms)
    $t_{RAS} = t_{RAS}$ (min.) to 1 µs
    Input voltages: $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V
    $V_{IL} < 0.2$ V
    $\overline{WE}$ $V_{IN} > V_{DD} - 0.2$ V
    All other inputs at stable V_{IH} or V_{IL}

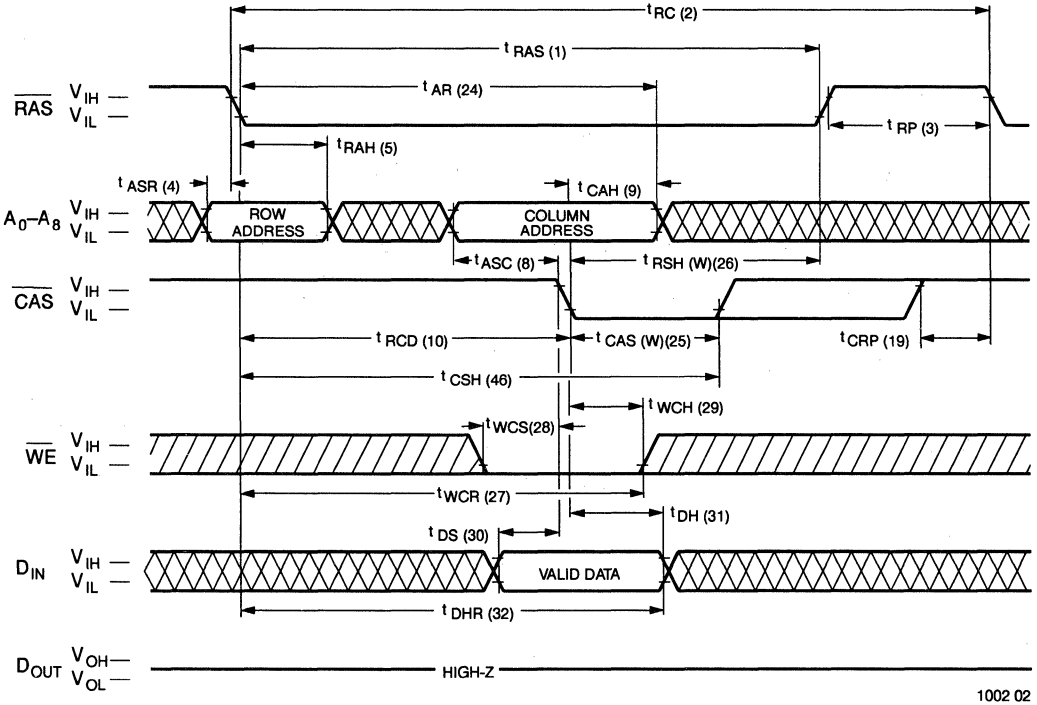
2

Waveforms of Read Cycle



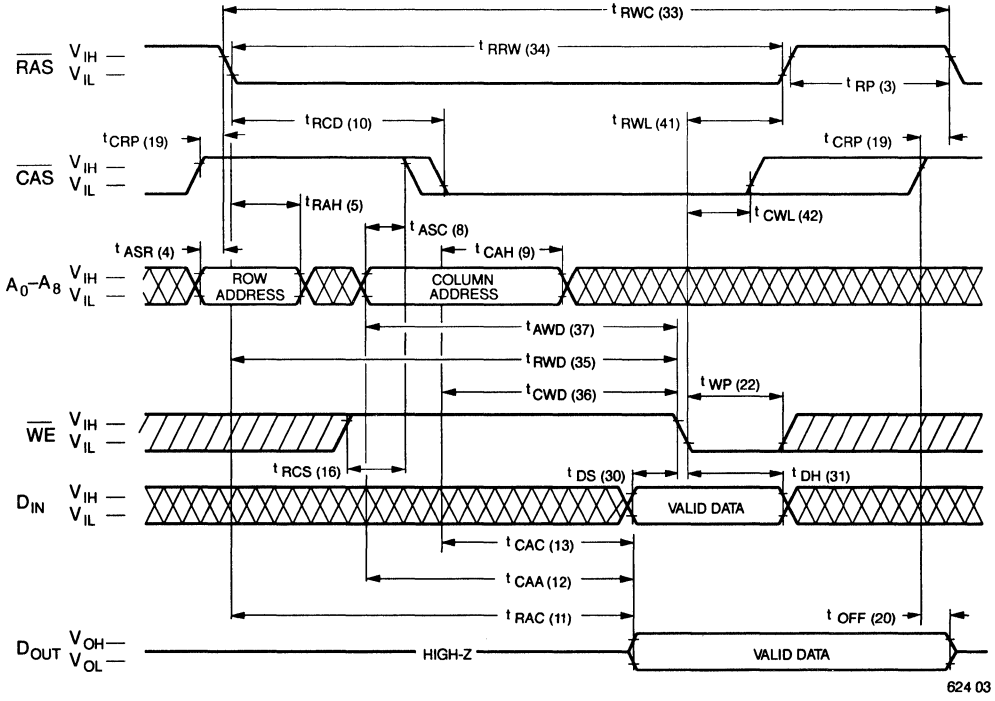
1002 01

Waveforms of Early Write Cycle

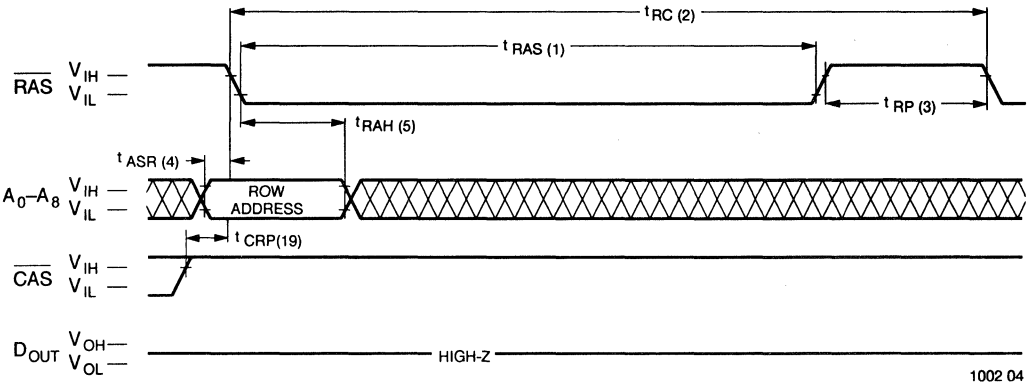


1002 02

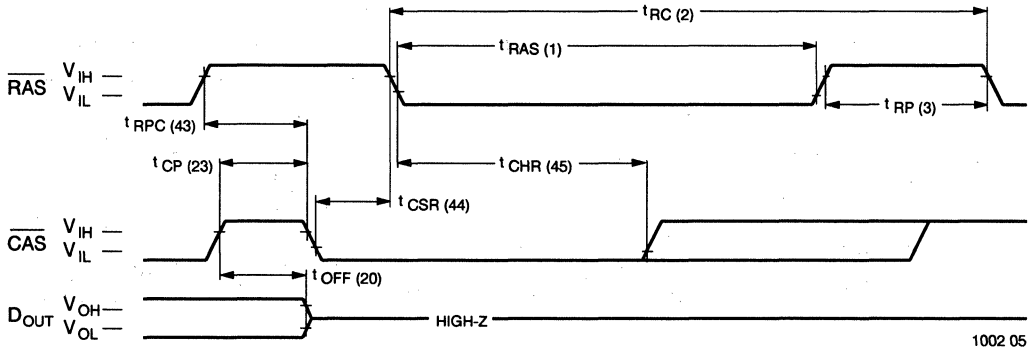
Waveforms of Read-Modify-Write Cycle



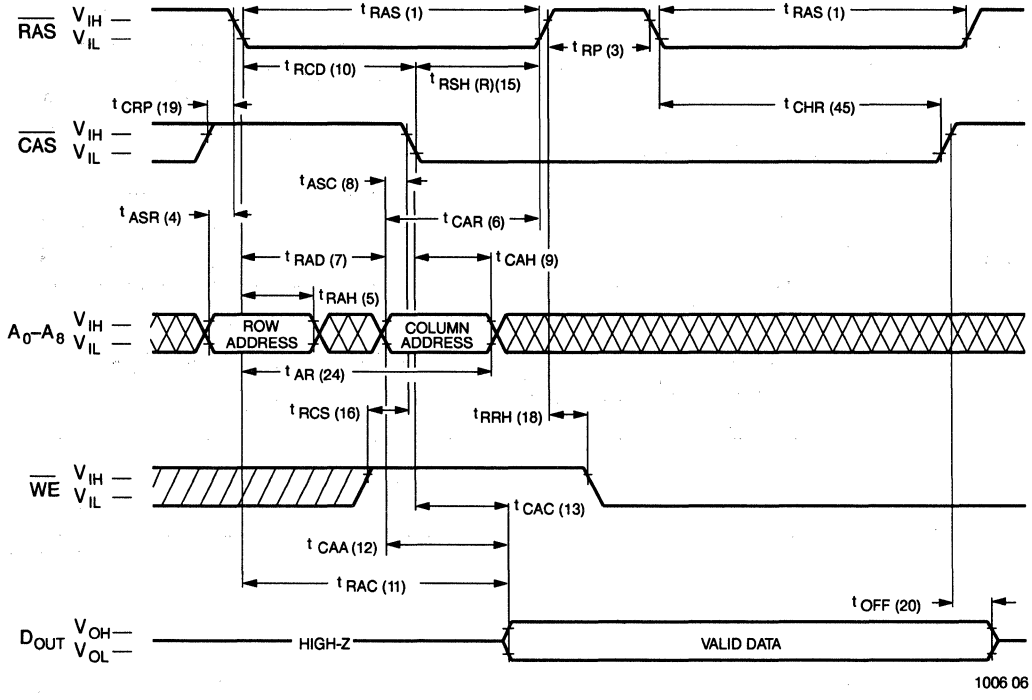
Waveforms of $\overline{RAS}$-Only Refresh Cycle



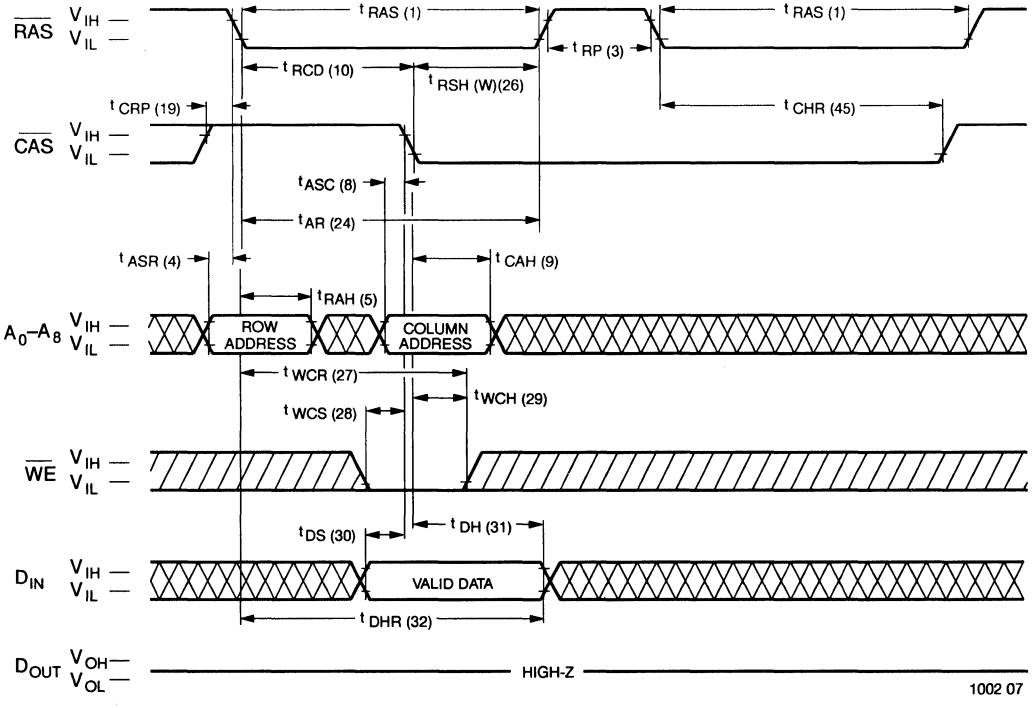
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



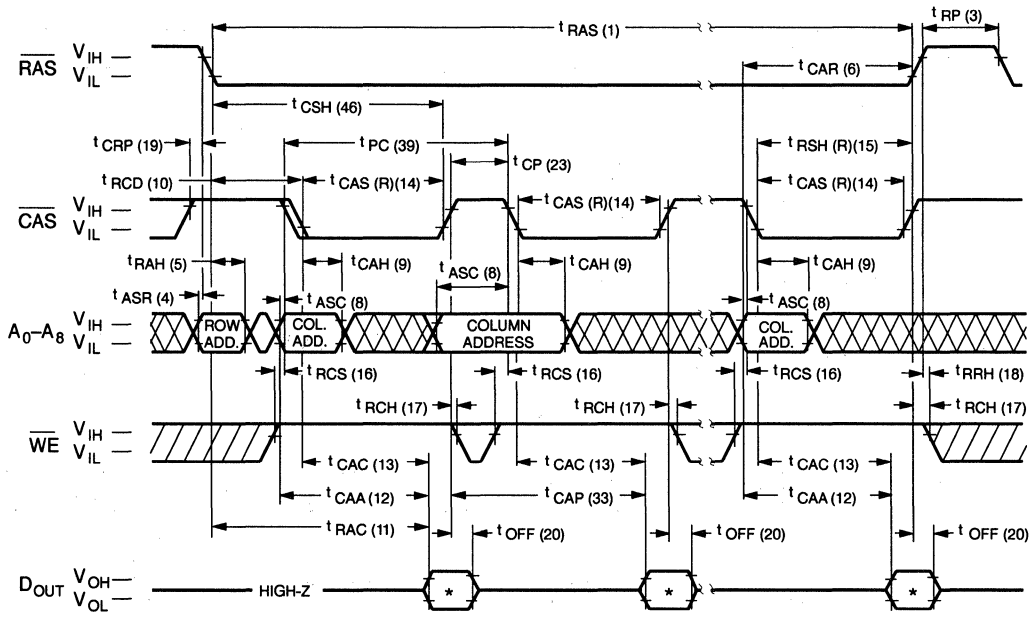
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



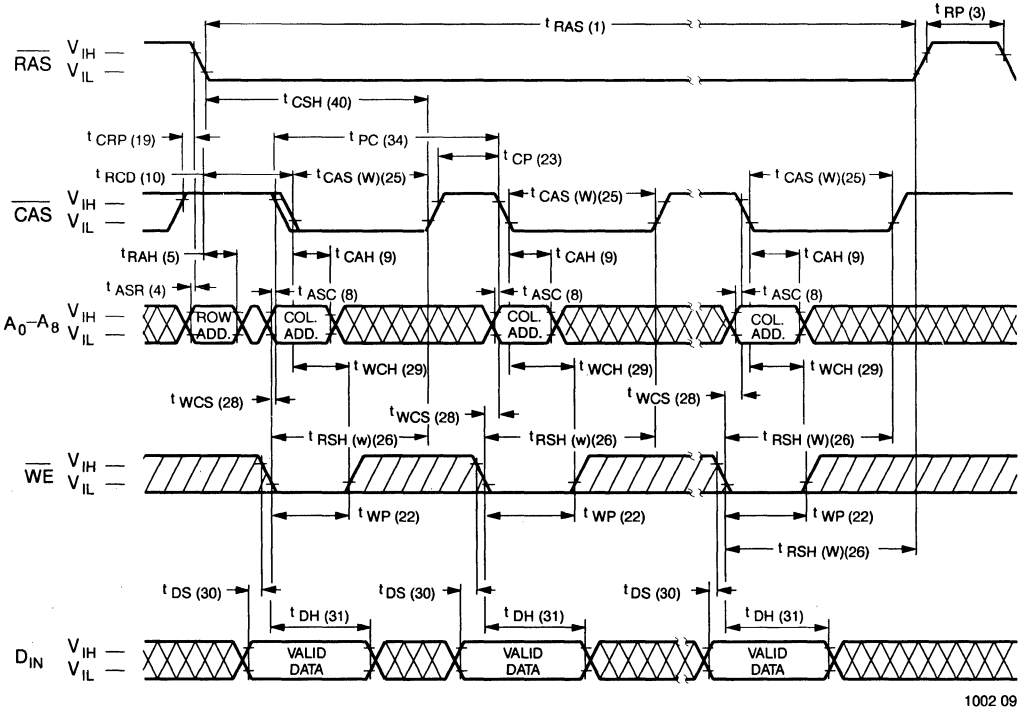
Waveforms of Fast Page Mode Read Cycle



1002 08

* Valid Data

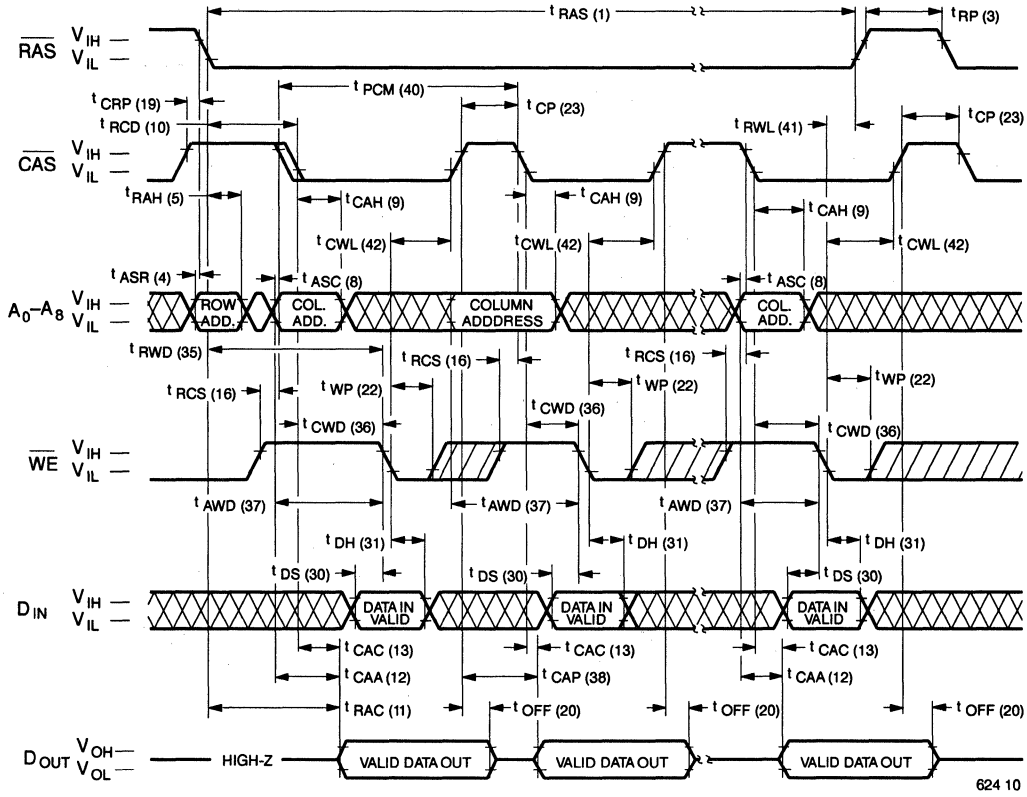
Waveforms of Fast Page Mode Write Cycle



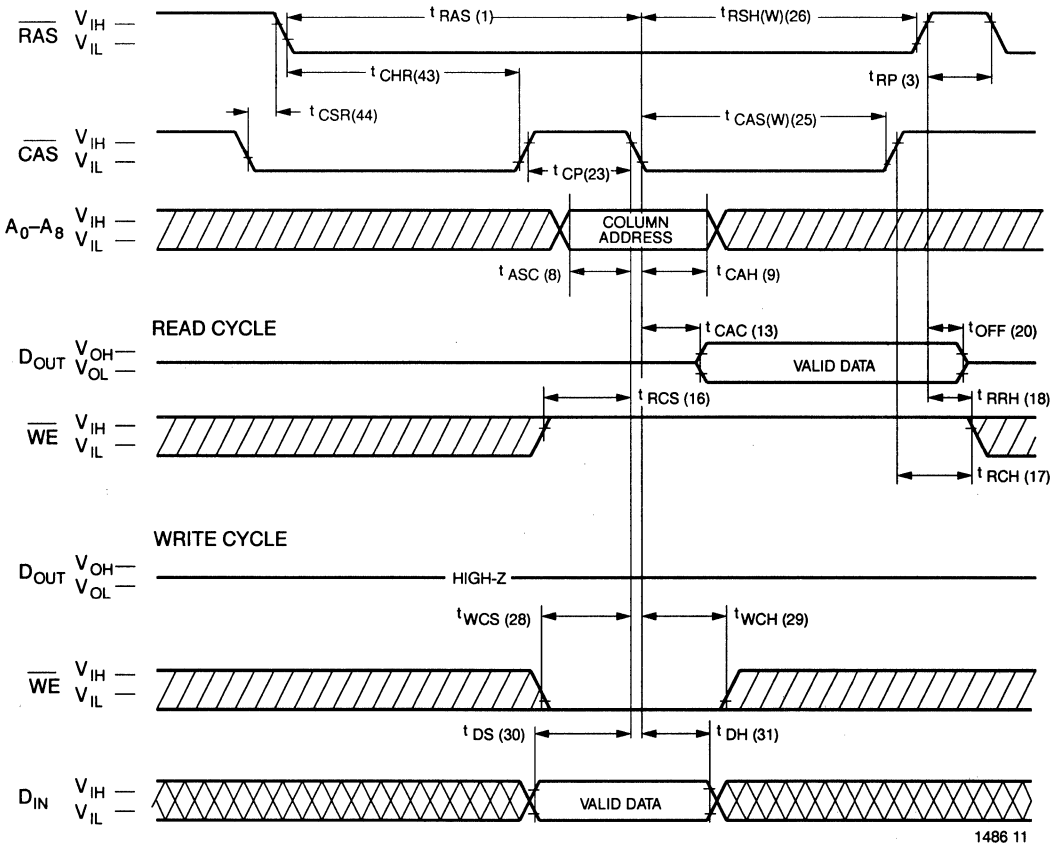
1002 09

2

Waveforms of Fast Page Mode Read-Modify-Write Cycle



Waveforms of Refresh Counter Test Cycle



Functional Description

The V53C100F is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C100F reads and writes data by multiplexing a 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} (min.) and t_{CAC} (min.) are both satisfied.

Write Cycle

A Write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the output (D_{OUT}) pin will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to Refresh the memory:

1. By selecting all 512 address combinations of A0 through A8 each 8 ms, a refresh of all rows is completed. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C100F will use the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, D_{OUT} will remain in the High-Z state during the cycle.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to write consecutive data patterns (512 Write cycles) and then verify the written data by applying 512 consecutive Read cycles. In this mode, the V53C100F ignores external row/column addresses and takes the output from the internal counter instead.

Data Retention Mode

The V53C100F offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C100F power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining RAS low while performing successive CAS cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while CAS is high.

Thus, access begins at the occurance of a valid column address rather than at the falling edge of CAS, eliminating t_{ASC} and t_T from the critical timing path. CAS latches the address into the column address buffer and acts as on output enable.

During Fast Page Mode operation, Read, Write, Read-Modify-Write, or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of CAS, the access time is determined by the by the CAS rising edge. If the column address is valid after the rising edge of CAS, the access is timed from the occurrance of the valid address and is specified by t_{CAA}. In both cases, the falling edge of CAS latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 25 MHz for applications that require high data rates like bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{1{,}024}{t_{RC} + 1{,}023 \times t_{PC}}$$

Data Output Operation

The V53C100F Data Output pin (D_{OUT}) has a three-state capability and is controlled by CAS. When CAS is high($\geq V_{IH}$), the output is in the High-Z state. Table 1 summarizes the D_{OUT} states possible for various memory cycles.

Power On

After application of the V_{DD} an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a RAS clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval). During power on, the V_{DD} current requirement of the V53C100F is dependent on the input levels of RAS and CAS. If RAS is Low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that RAS and CAS track with V_{DD} or be held at a valid V_{IH} during power on to avoid current surges.

Table 1. V53C100F Data Output
Operation for Various Cycle Types

Cycle Type	D_{OUT} State
Read Cycles	Data from Addressed Memory Cell
CAS-Controlled Write Cycle (Early Write)	High-Z
WE-Controlled Write Cycle (Late Write)	Active, not valid
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
RAS-only Refresh	High-Z
CAS-before-RAS Refresh Cycle	Data remains as in previous cycle
CAS-only Cycles	High-Z

2

ULTRA-HIGH PERFORMANCE LOW POWER 1M X 1 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C100H	45/45L	50/50L	55/55L	60/60L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	45 ns	50 ns	55 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	22 ns	24 ns	28 ns	30 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	12 ns	12 ns	15 ns	15 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	25 ns	28 ns	38 ns	40 ns
Min. Read-Write Cycle Time, (t_{RC})	90 ns	100 ns	110 ns	120 ns

LOW POWER V53C100HL	45L	50L	55L	60 L
Max. CMOS Standby Current, (I_{DD6})	150 µA	150µA	150 µA	150 µA

Features

- 1M x 1-bit organization
- $\overline{RAS}$ Access time: 45, 50, 55, 60 ns
- Low power dissipation
  - V53C100H-60
    - — Operating Current – 85 mA max.
    - — TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C100H – 1.0 mA max.
  - V53C100HL – 0.15 mA max.
- Low Battery Back-up Current
  - V53C100HL – 200µA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Fast Page Mode operation for a sustained data rate greater than 40 MHz
- Refresh Interval
  - V53C100H – 512 cycles/8 ms
  - V53C100HL – 512 cycles/ 64ms
- Available in 18 pin Plastic DIP and 26/20 pin SOJ packages

Description

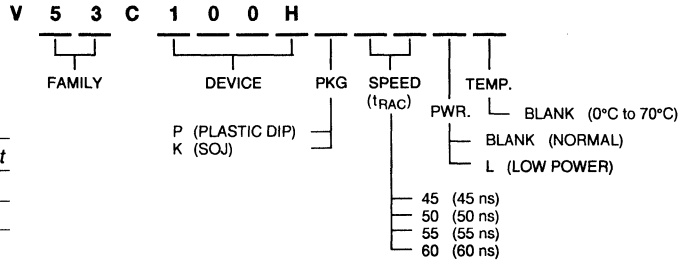
The V53C100H is a high speed 1,048,576 x 1 bit CMOS dynamic random access memory. Fabricated with Mosel-Vitelic's VICMOS III technology, the V53C100H offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C100HL).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random or sequential access of up to 1024 bits within a row with cycle times as short as 25 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical timing requirements for fast usable speed. These features make the V53C100H ideally suited for cache based mainframe and mini computers, graphics, digital signal processing and high performance microprocessor systems.

The V53C100HL offers a maximum data retention power of 1.1 mW when operating in CMOS standby mode and performing CAS-before-RAS refresh cycles. This mode is entered by holding $\overline{RAS}$ at a voltage greater than V_{DD}–0.2 when it is inactive.

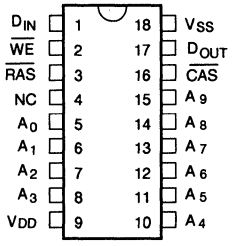
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power		Temperature Mark
	P	K	45	50	55	60	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	•	Blank

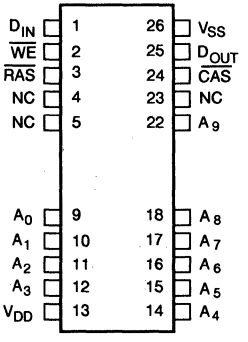


Description	Pkg.	Pin Count
Plastic DIP	P	18
SOJ	K	26/20

18 Lead Plastic DIP PIN CONFIGURATION
Top View



26/20 Lead SOJ Package PIN CONFIGURATION
Top View



Pin Names

A_0–A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{DD}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage Relative to V_{SS} .....–1.0 V to +7.0 V
Data Out Current .....50 mA
Power Dissipation .....1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

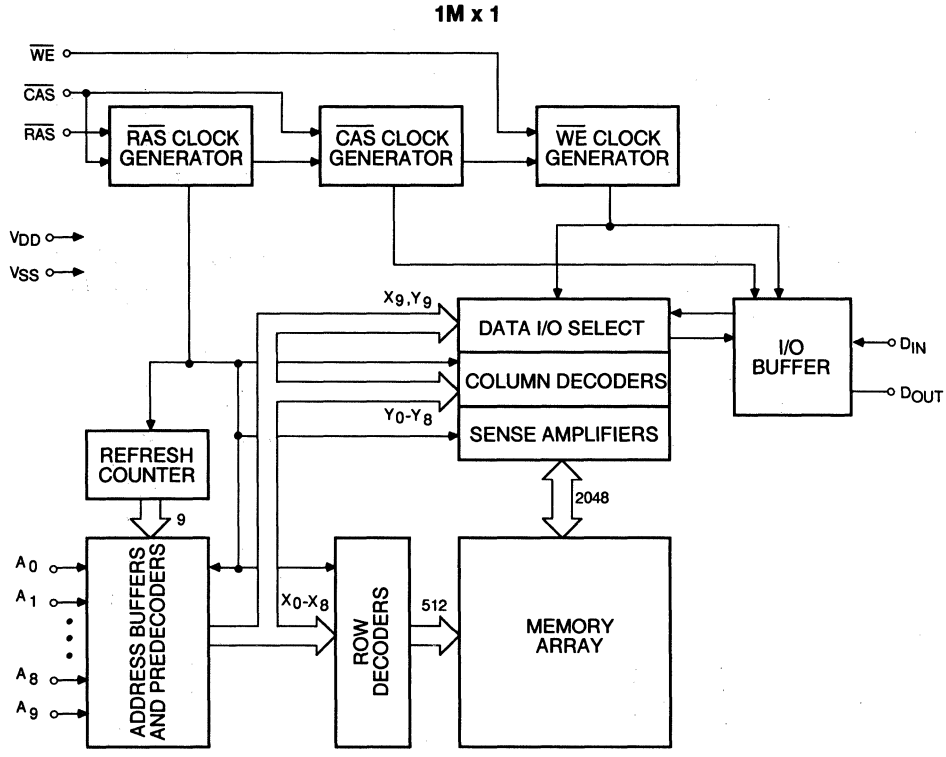
Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	4	5	pF
C_{OUT}	I/O	5	7	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C100H			V53C100HL			Unit	Test Conditions	Notes
			Min.	Typ.	Max.	Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10		10	−10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10		10	−10		10	µA	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	45			110			110	mA	$t_{RC} = t_{RC}$ (min.)	1,2
		50			100			100			
		55			90			90			
		60			85			85			
I_{DD2}	V_{DD} Supply Current, TTL Standby				2.0			2.0	mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	45			110			110	mA	$t_{RC} = t_{RC}$ (min.)	2
		50			100			100			
		55			90			90			
		60			85			85			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	45			100			100	mA	Minimum Cycle	1,2
		50			90			90			
		55			85			85			
		60			80			80			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled				2.0			2.0	mA	$\overline{RAS}$=V_{IH},$\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby				1.0			0.15	mA	$\overline{RAS} \ge V_{DD}$−0.2 V, $\overline{CAS} \ge V_{DD}$−0.2 V, All other inputs≥V_{SS}	
I_{DD7}	Battery Backup Data Retention Current (V53C100HL Only)				N.A.			0.2	mA	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle t_{RC} = 125 µs CMOS clock levels	18
V_{IL}	Input Low Voltage		−1		0.8	−1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{DD} +1	2.4		V_{DD} +1	V		3
V_{OL}	Output Low Voltage				0.4			0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4			2.4			V	I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	45/L		50/L		55/L		60/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	45	75K	50	75K	55	75K	60	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	90		100		110		120		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	35		40		45		50		ns	
4	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
5	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8		9		10		10		ns	
6	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	22		24		28		30		ns	
7	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	23	14	26	15	27	15	30	ns	4
8	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
9	t_{CL1AX}	t_{CAH}	Column Address Hold Time	6		7		10		10		ns	
10	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	31	19	36	20	40	20	45	ns	5
11	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		45		50		55		60	ns	6,7,8
12	t_{AVQV}	t_{CAA}	Access Time from Column Address		22		24		28		30	ns	8,9
13	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		12		12		15		15	ns	8,15
14	$t_{CL1CH1(R)}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	12		12		15		15		ns	
15	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	14		14		15		15		ns	
16	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
17	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	10
18	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	10
19	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	4		4		5		5		ns	
20	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	8	0	8	0	10	0	10	ns	11

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	45/L		50/L		55/L		60/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CH2QV}	t_{OH}	Data Hold Time from $\overline{CAS}$	0		0		0		0		ns	11
22	t_{WL1WH1}	t_{WP}	Write Pulse Width	6		7		10		10		ns	
23	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	7		8		10		10		ns	
24	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	30		35		45		50		ns	
25	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	12		12		15		15		ns	
26	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	14		14		15		15		ns	
27	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	30		35		45		50		ns	
28	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12,13
29	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	6		7		10		10		ns	
30	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		0		ns	14
31	t_{WH1DX}	t_{DH}	Data In Hold Time	6		7		10		10		ns	14
32	t_{RL1DX}	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	30		35		45		50		ns	
33	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	110		120		130		140		ns	
34	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	65		70		75		80		ns	
35	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time Read-Modify-Write Cycle	45		50		55		60		ns	12
36	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	14		14		15		15		ns	12
37	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	22		24		28		30		ns	12
38	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		24		26		32		34	ns	15
39	$t_{CL2CL2(R)}$	t_{PC}	Fast Page Mode Read or Write Cycle Time	25		28		38		40		ns	

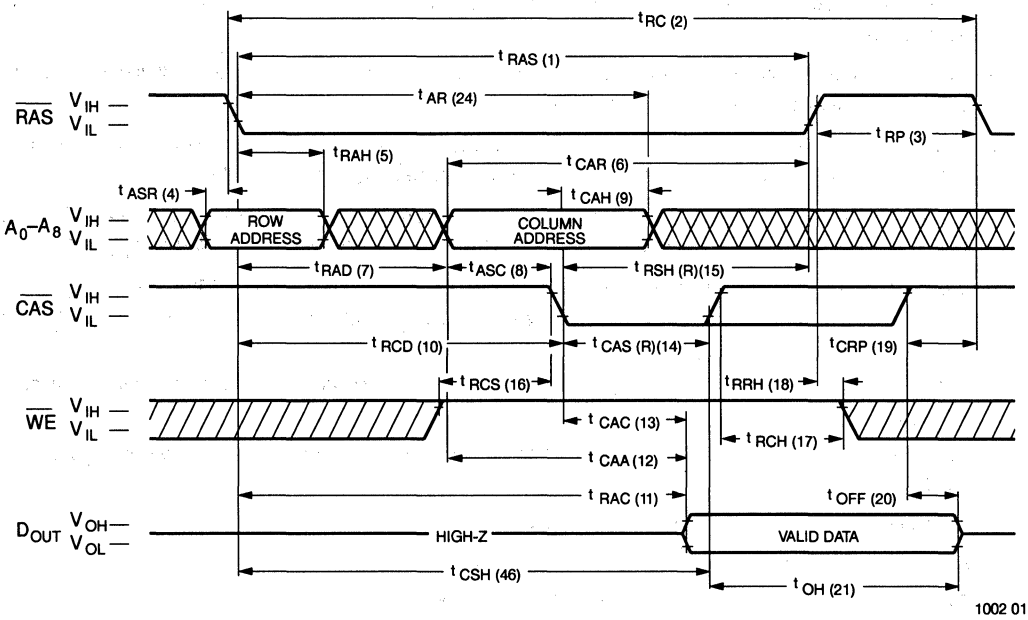
AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	45/L		50/L		55/L		60/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
40	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	52		54		58		60		ns	
41	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	14		14		15		15		ns	
42	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	14		14		15		15		ns	
43	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
44	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		10		ns	
45	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	12		12		15		15		ns	
46	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	45		50		55		60		ns	
47	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	16
		t_{REF}	Refresh Interval (512 Cycles)		8		8		8		8	ms	17
		t_{REF}	Refresh Interval V53C100HL Only (512 cycles, t_R =125 µs)		64		64		64		64	ms	17, 18

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in First Page Mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} (min.) may undershoot to −1.0 V for periods not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
5. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limits ensure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
6. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
10. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
11. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
12. t_{WCS}, t_{WHC}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the later occurance of $\overline{CAS}$ or $\overline{WE}$.
15. Access time is determined by the longer of t_{CAA}, t_{CAC}, or t_{CAP}.
16. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC measurements assume t_T = 5 ns.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
    t_{RC} = 125 µs (125 µs x 512 = 64ms)
    $t_{RAS} = t_{RAS}$ (min) to 1 us
    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V
    $V_{IL} < 0.2$ V
    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V
    All other inputs at stable V_{IH} or V_{IL}

Waveforms of Read Cycle



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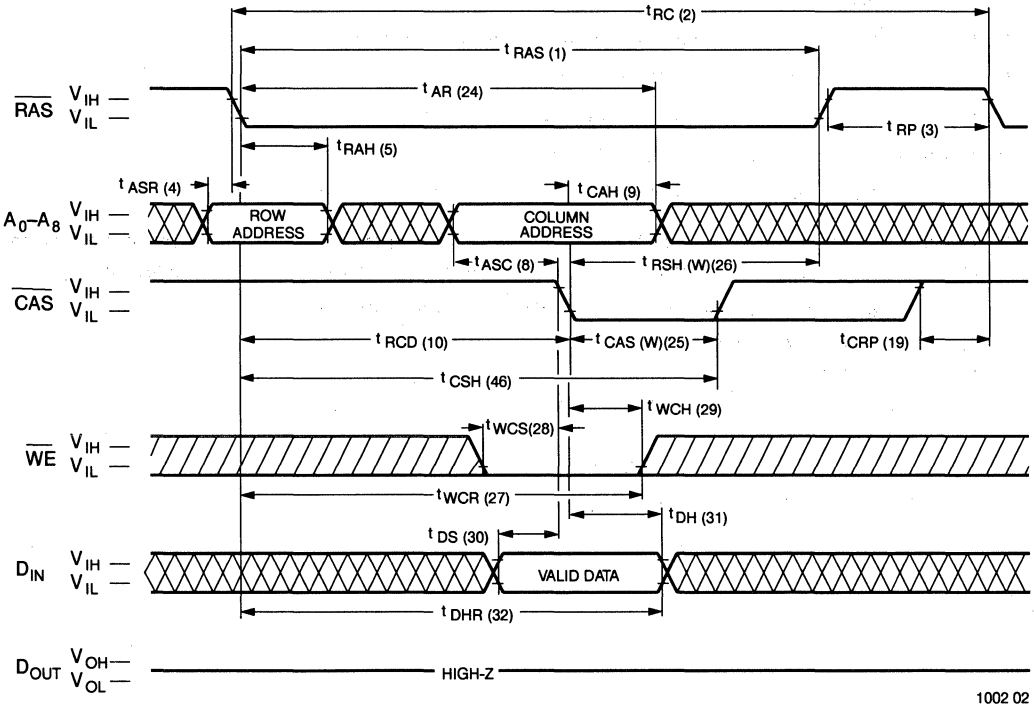
Waveforms of Early Write Cycle



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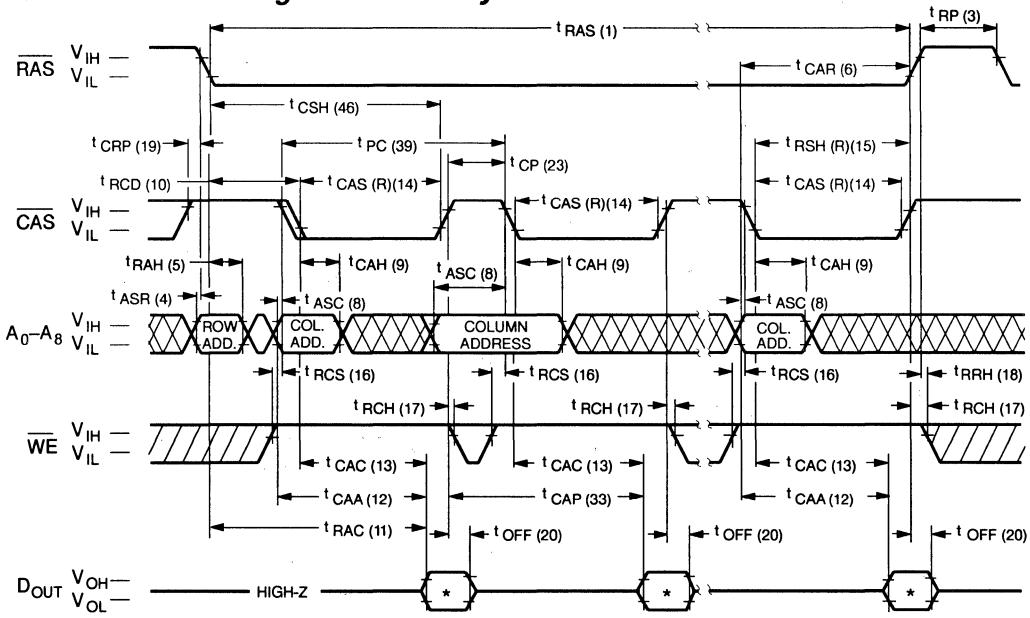
Waveforms of Fast Page Mode Read Cycle



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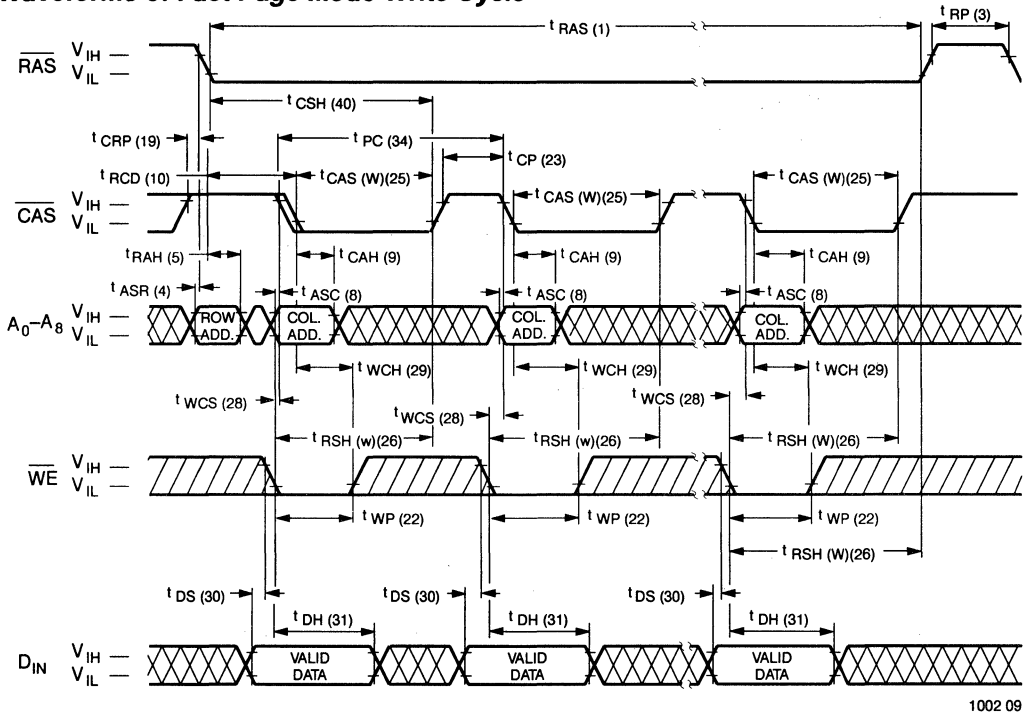
* Valid Data

Waveforms of Fast Page Mode Write Cycle



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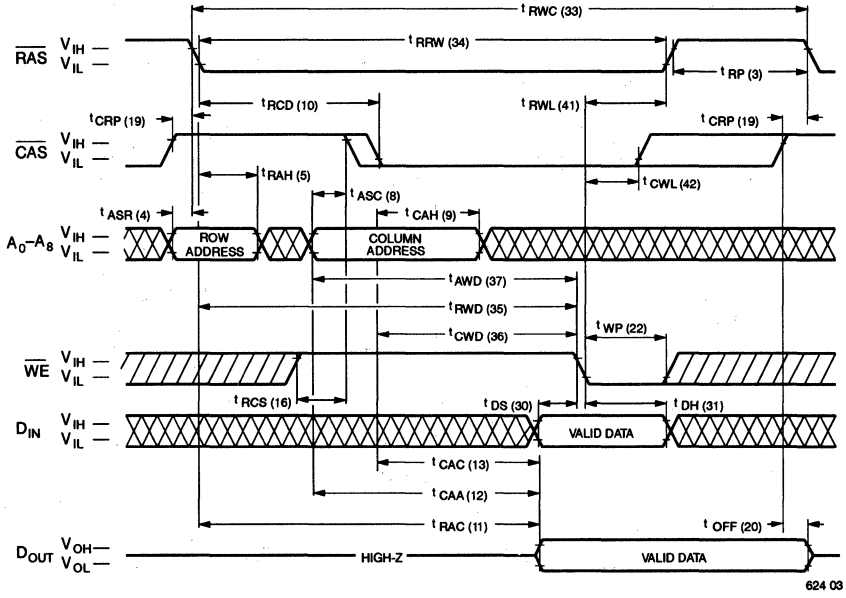
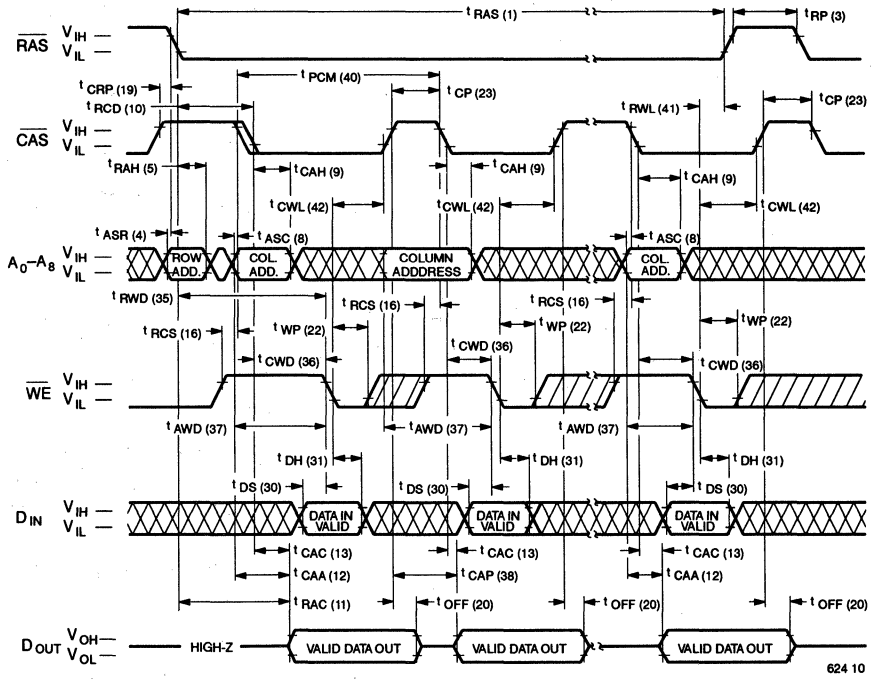
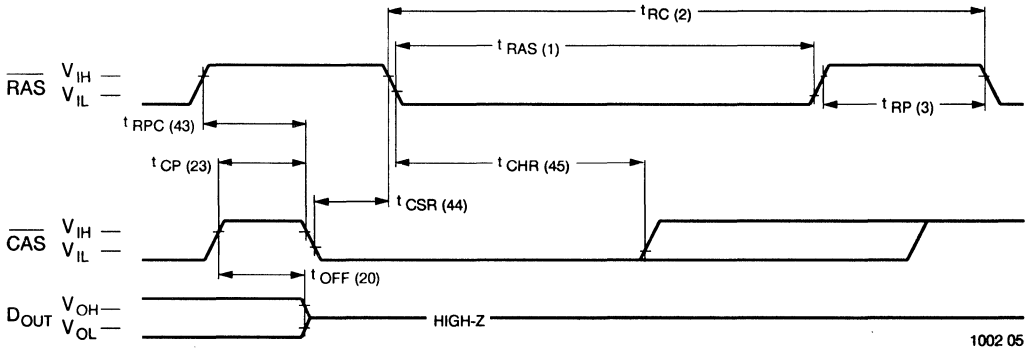
Waveforms of Read-Modify-Write Cycle



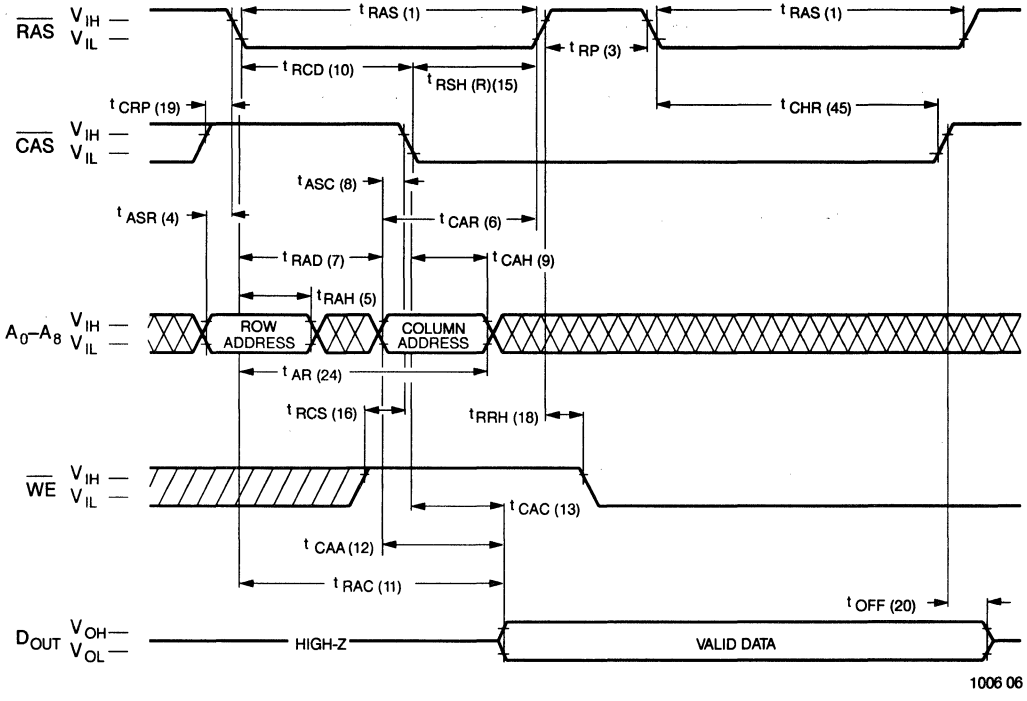
Waveforms of Fast Page Mode Read-Modify-Write Cycle



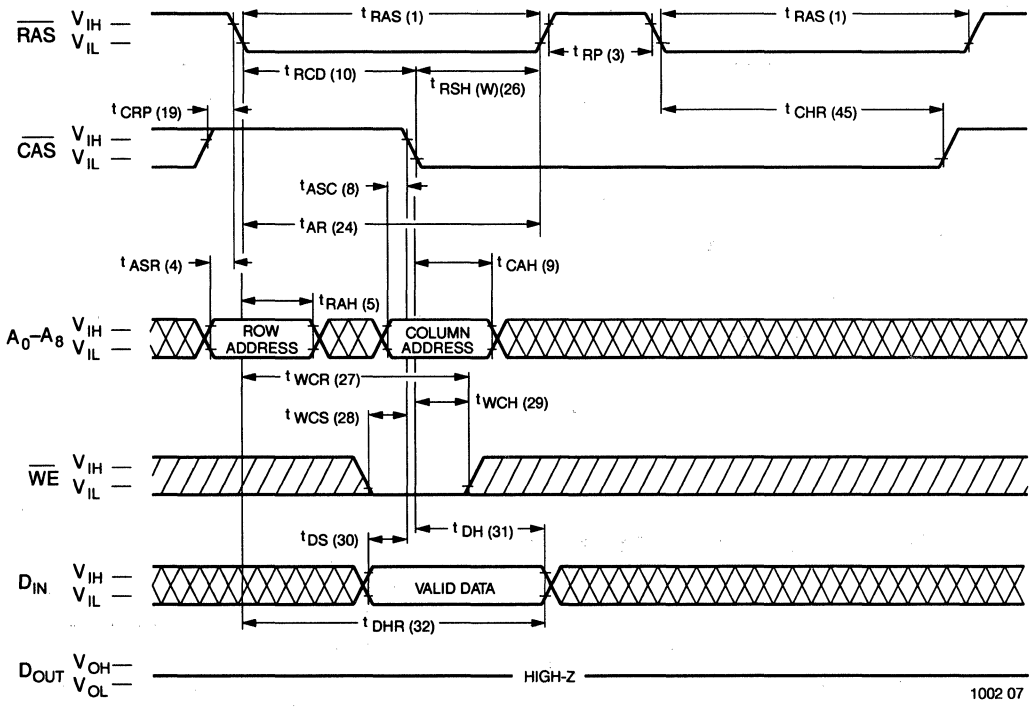
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle)



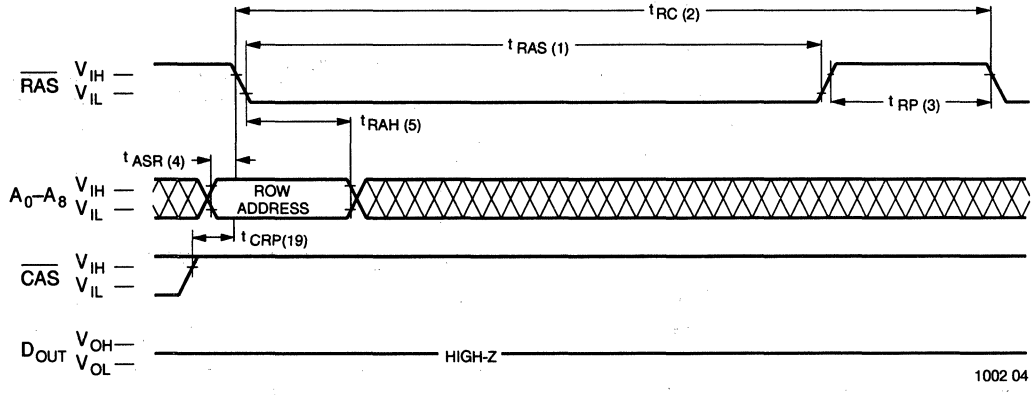
Waveforms of Hidden Refresh Cycle (Read)



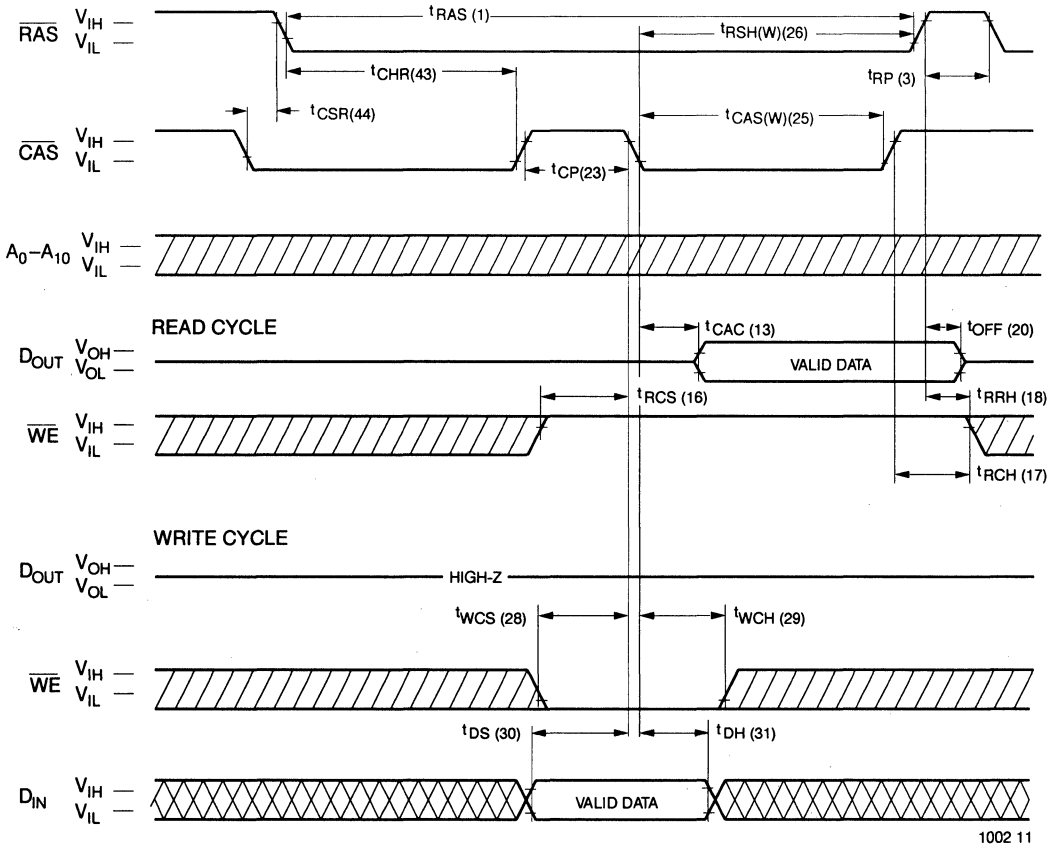
Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{RAS}$-Only Refresh Cycle



Waveforms of $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C100H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C100H reads and writes data by multiplexing a 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the presice time that the $\overline{CAS}$ edge occurs, the delay from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} (min.) and t_{CAC} (min.) are both satisfied.

Write Cycle

A Write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the output (D_{OUT}) pin will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to Refresh the memory:

1. By selecting all 512 address combinations of A0 through A8 each 8 ms, a refresh of all rows is completed. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C100H will use the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, D_{OUT} will remain in the High-Z state during the cycle.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to write consecutive data patterns (512 Write cycles) and then verify the written data by applying 512 consecutive Read cycles. In this mode, the V53C100H ignores external row/column addresses and takes the output from the internal counter instead.

Data Retention Mode

The V53C100H offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C100H power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high.

Thus, access begins at the occurance of a valid column address rather than at the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as on output enable.

During Fast Page Mode operation, Read, Write, Read-Modify-Write, or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is determined by the by the $\overline{CAS}$ rising edge. If the column address is valid after the rising edge of $\overline{CAS}$, the access is timed from the occurrance of the valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 40 MHz for applications that require high data rates like bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{1{,}024}{t_{RC} + 1{,}023 \times t_{PC}}$$

Data Output Operation

The V53C100H Data Output pin (D_{OUT}) has a three-state capability and is controlled by $\overline{CAS}$. When $\overline{CAS}$ is high($\geq V_{IH}$), the output is in the High-Z state. Table 1 summarizes the D_{OUT} states possible for various memory cycles.

Power On

After application of the V_{DD} an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During power on, the V_{DD} current requirement of the V53C100H is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on to avoid current surges.

Table 1. V53C100H Data Output
Operation for Various Cycle Types

Cycle Type	D_{OUT} State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	Active, not valid
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

2

HIGH PERFORMANCE, 3.3 VOLT 1M X 1 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C100N	60/60L	70/70L	80/80L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	45 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	20 ns	25 ns	25 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns
Min. Read-Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns

LOW POWER V53C100NL	60L	70L	80L
Max. CMOS Standby Current, (I_{DD6})	40 µA	40 µA	40 µA

Features

- 1M x 1-bit organization
- Low power dissipation for V53C100N-80
  - Operating Current – 35 mA max.
  - TTL Standby Current – 1.0 mA max.
- Low CMOS Standby Current
  - V53C100N – 400µA max.
  - V53C100NL – 40µA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Common I/O capability
- Refresh Interval
  - V53C100N – 512 cycles/8ms
  - V53C100NL – 512 cycles/64ms
- Fast Page Mode operation for a sustained data rate greater than 25 MHz
- Standard packages are 18 pin Plastic DIP and 26/20 pin SOJ
- Low Battery Back-up Current
  - V53C100NL – 150 µA max.

Description

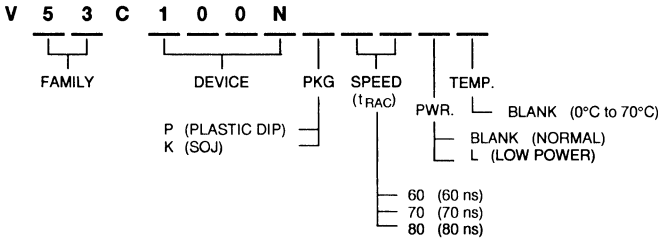
The V53C100N is a high speed 1,048,576 x 1 bit CMOS dynamic random access memory. Fabricated with MOSEL-Vitelic's VICMOS IV technology, the V53C100N offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random or sequential access of up to 1024 bits within a row with cycle times as short as 45 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical timing requirements for fast usable speed. These features make the V53C100N ideally suited for cache based mainframe and mini computers, graphics, digital signal processing and high performance microprocessor systems.

The V53C100NL offers a maximum data retention power of 0.8 mW when operating in CMOS standby mode and performing $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

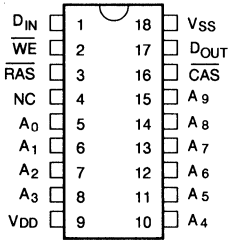
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	60	70	80	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank

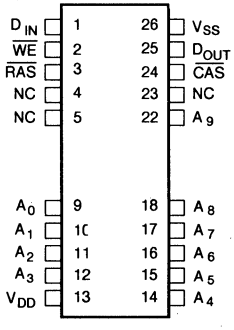


Description	Pkg.	Pin Count
Plastic DIP	P	18
SOJ	K	26/20

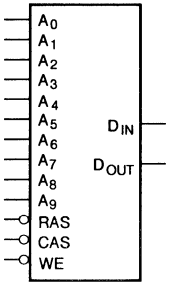
18 Lead Plastic DIP PIN CONFIGURATION
Top View



26/20 Lead SOJ Package PIN CONFIGURATION
Top View



LOGIC SYMBOL



Pin Names

A_0–A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{DD}	+3.3V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 V to +6.0 V
Voltage on V_{DD} relative to V_{SS} ..... –1.0 V to +6.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

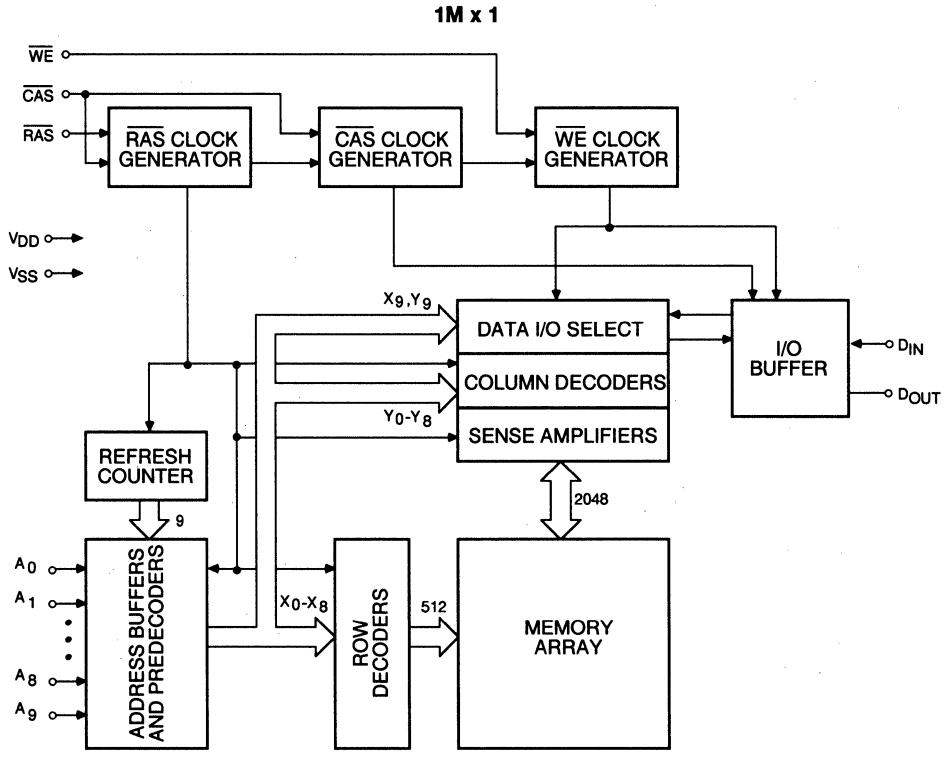
Capacitance*

T_A = 25°C, V_{DD} = 3.3 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	7	pF
C_{OUT}	I/O	—	7	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C100N		V53C100NL		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10	10	−10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10	10	−10	10	µA	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60		45		45	mA	$t_{RC} = t_{RC}$ (min.)	1,2
		70		40		40			
		80		35		35			
I_{DD2}	V_{DD} Supply Current, TTL Standby			1.0		1.0	mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60		45		45	mA	$t_{RC} = t_{RC}$ (min.)	2
		70		40		40			
		80		35		35			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60		50		50	mA	Minimum Cycle	1,2
		70		40		40			
		80		35		35			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			2.0		1.0	mA	$\overline{RAS}$=V_{IH},$\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby			400		40	µA	$\overline{RAS} \ge V_{DD}$ −0.2 V, $\overline{CAS} \ge V_{DD}$ −0.2 V, other inputs ≥ V_{SS}	
I_{DD7}	Battery Back-up Data Retention Current (V53C100NL only)			N.A.		0.15	mA	$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle t_{RC}=125µs, t_{RAS}<1µs CMOS Clock Levels	1, 18
V_{IL}	Input Low Voltage (all inputs)		−1	0.6	−1	0.6	V		3
V_{IH}	Input High Voltage (all inputs)		2.2	V_{DD} +1	2.2	V_{DD} +1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4		V	I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 3.3 V ±10%, V_{SS} = 0 V, unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	ns	
2	t_{RL2RL}	t_{RC}	Read or Write Cycle Time	120		130		150		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		ns	
4	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
5	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		15		ns	
6	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		ns	
7	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	25	20	30	20	35	ns	4
8	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
9	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		ns	
10	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	40	25	45	25	55	ns	5
11	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	6,7,8
12	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		45	ns	8,9, 15
13	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		25		25	ns	8,15
14	$t_{CL1CH1(R)}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	20	75K	25	75K	25	75K	ns	
15	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		25		25		ns	
16	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
17	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	10
18	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	10
19	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
20	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	ns	11

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CH2QV}	t_{OH}	Data Hold Time from $\overline{CAS}$	0		0		0		ns	11
22	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		15		ns	
23	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
24	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
25	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	20		25		25		ns	
26	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		25		25		ns	
27	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
28	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
29	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		15		ns	
30	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		ns	14
31	t_{WH1DX}	t_{DH}	Data In Hold Time	15		15		15		ns	14
32	t_{RL1DX}	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
33	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	145		160		180		ns	
34	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	85		100		110		ns	
35	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time Read-Modify-Write Cycle	60		70		80		ns	12
36	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	20		25		25		ns	12
37	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	35		40		45		ns	12
38	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50	ns	15
39	$t_{CL2CL2(R)}$	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		ns	

AC Characteristics (Cont'd.)

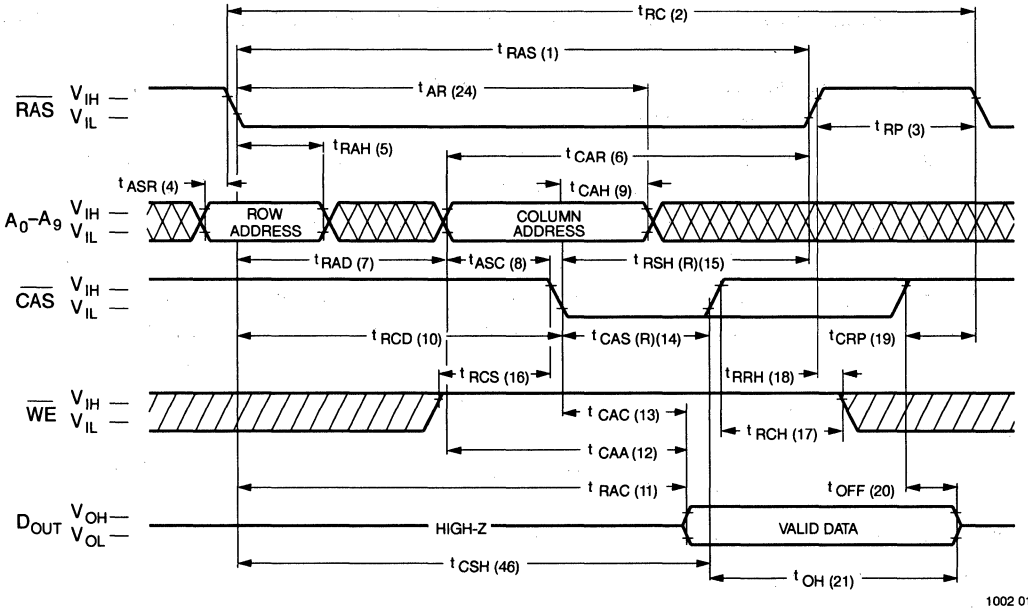
#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
40	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	70		80		85		ns	
41	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		25		ns	
42	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		25		ns	
43	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
44	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
45	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	30		30		30		ns	
46	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
47	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	16
		t_{REF}	Refresh Interval (512 Cycles)		8		8		8	ms	17
		t_{REF}	Refresh Interval V53C100NL only (512 Cycles, t_{RC} = 125 µs)		64		64		64	ms	18

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} (min.) may undershoot to −1.0 V for periods not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
5. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limits ensure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
6. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
10. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
11. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
12. t_{WCS}, t_{WHC}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the later occurance of $\overline{CAS}$ or $\overline{WE}$.
15. Access time is determined by the longest of t_{CAA}, t_{CAC}, or t_{CAP}.
16. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC measurements assume t_T = 5 ns.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
    t_{RC} = 125 µs (125 µs x 512 = 64 ms)
    $t_{RAS} = t_{RAS}$ (min.) to 1 µs

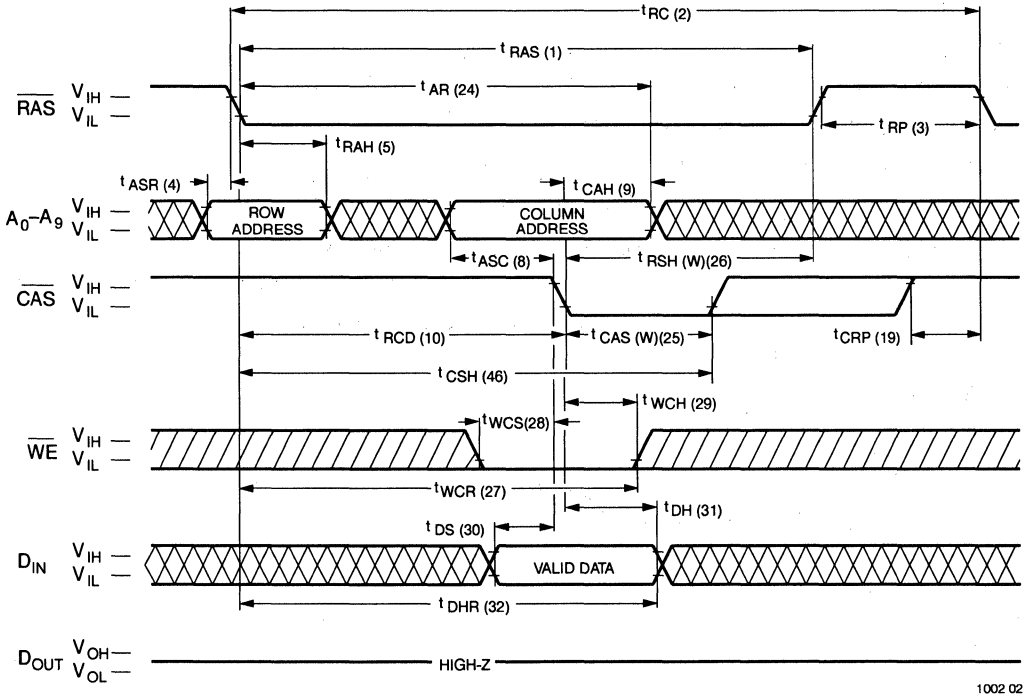
Input voltages:	$\overline{RAS}$ and $\overline{CAS}$	$V_{IH} > V_{DD} - 0.2$ V
		$V_{IL} < 0.2$ V
	$\overline{WE}$	$V_{IN} > V_{DD} - 0.2$ V
	All other inputs at stable	V_{IH} or V_{IL}

Waveforms of Read Cycle



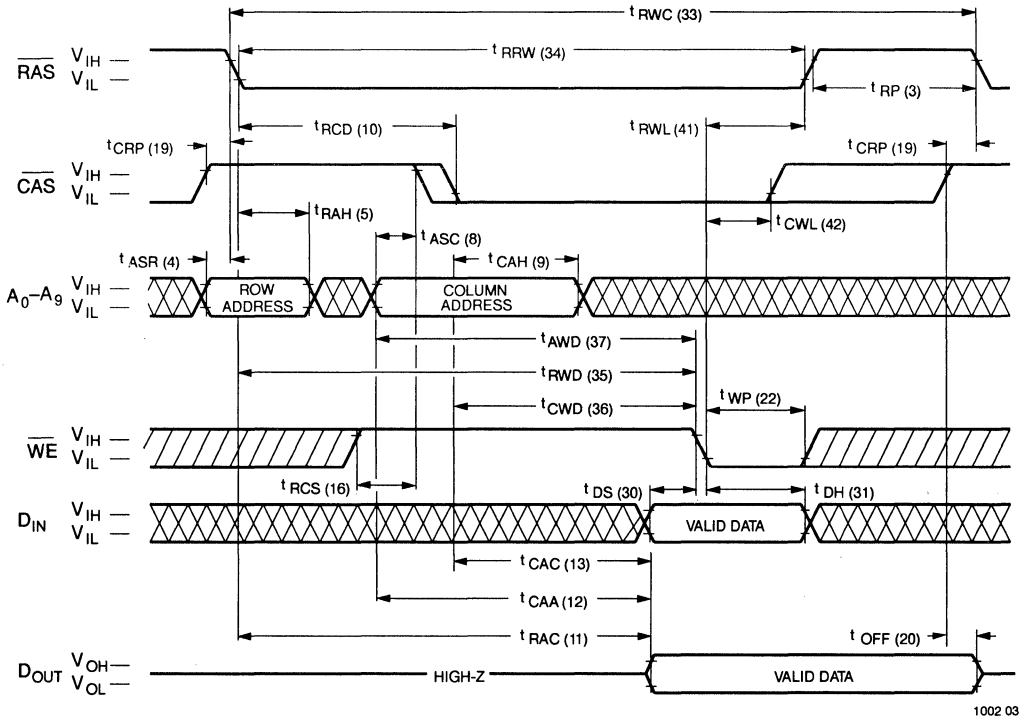
1002 01

Waveforms of Early Write Cycle

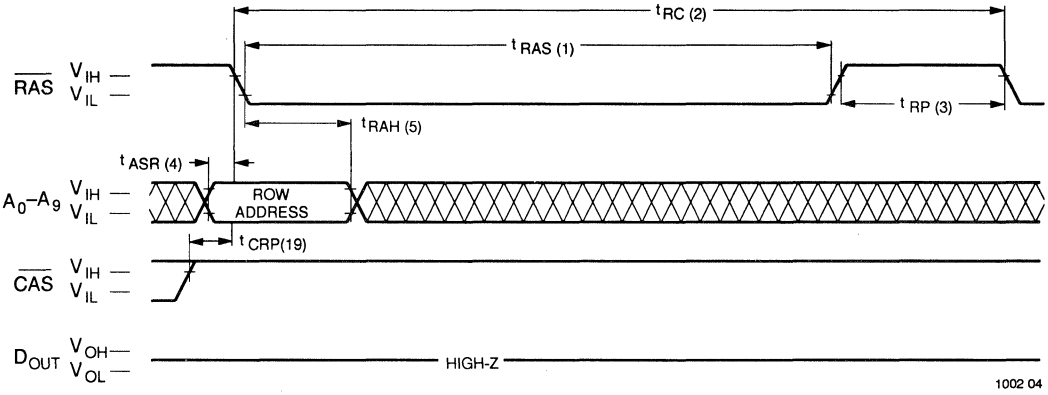


1002 02

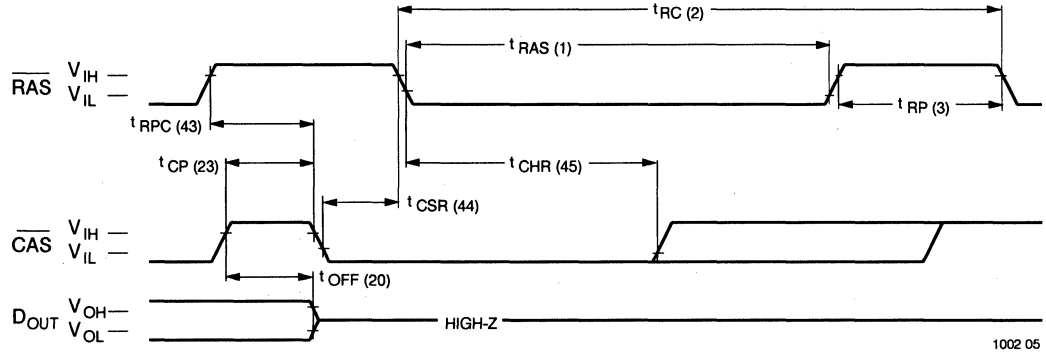
Waveforms of Read-Modify-Write Cycle



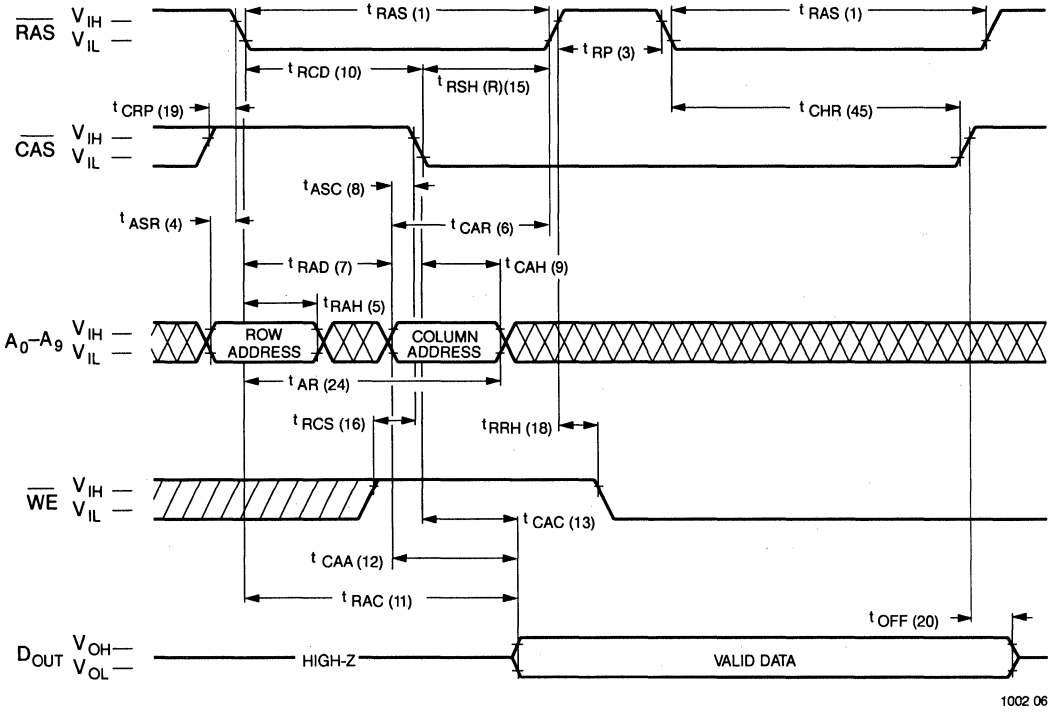
Waveforms of $\overline{RAS}$-Only Refresh Cycle



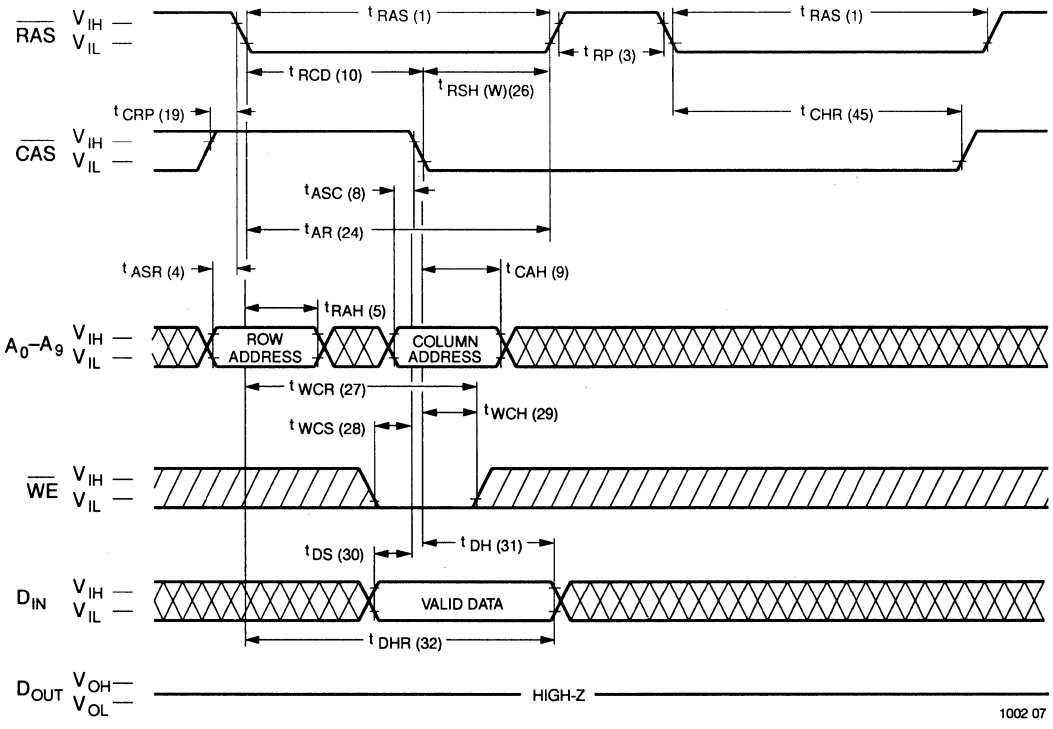
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



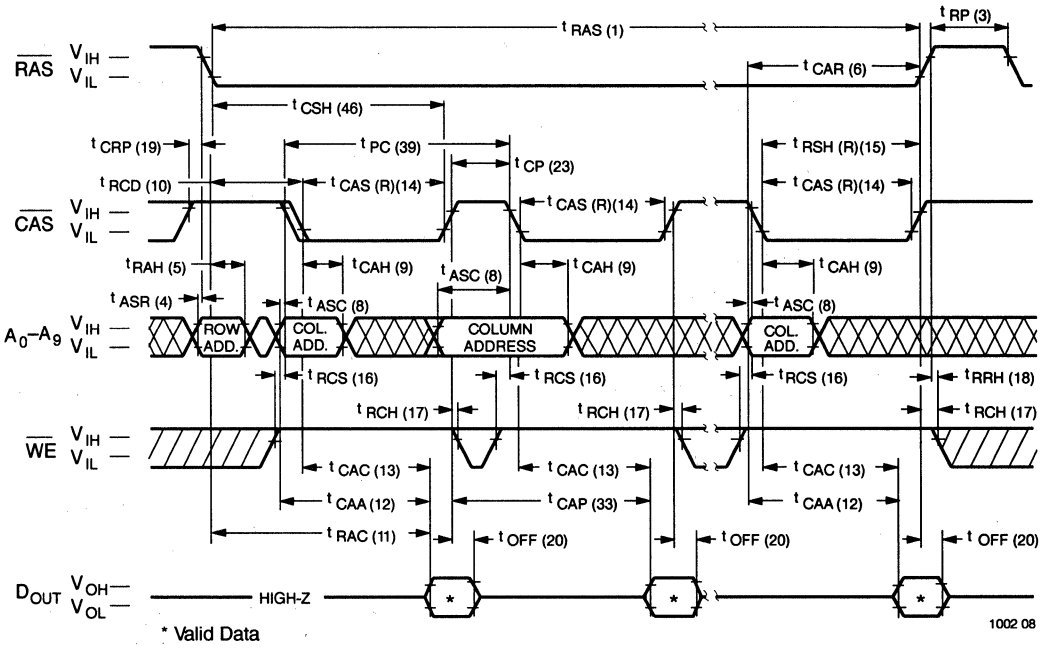
Waveforms of Hidden Refresh Cycle (Read)



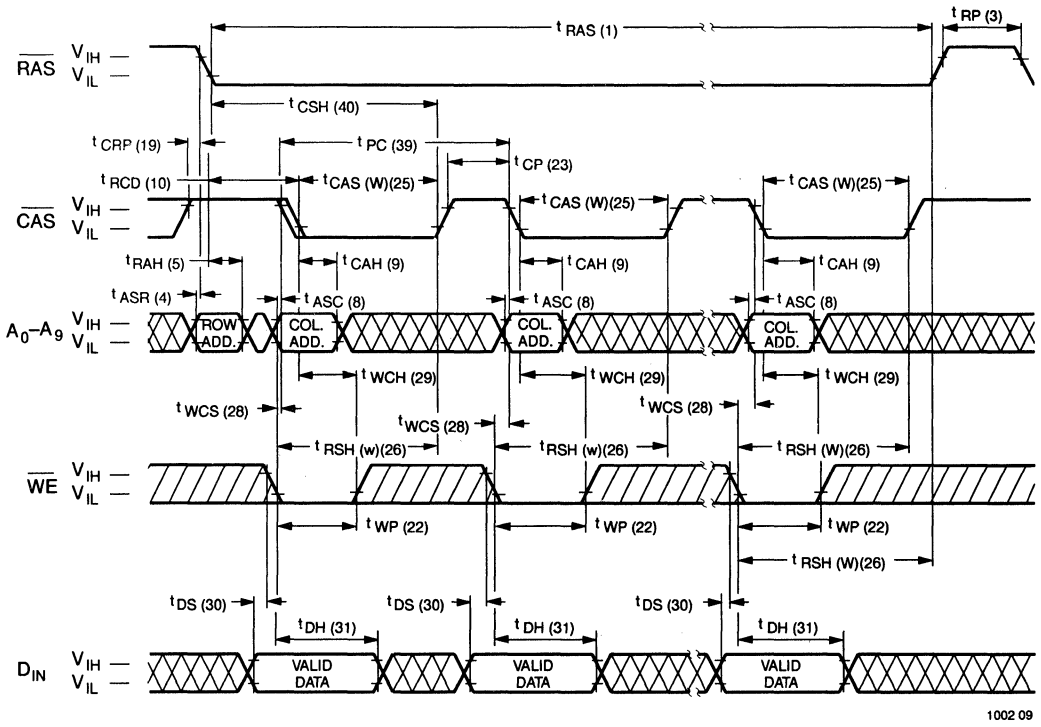
Waveforms of Hidden Refresh Cycle (Write)



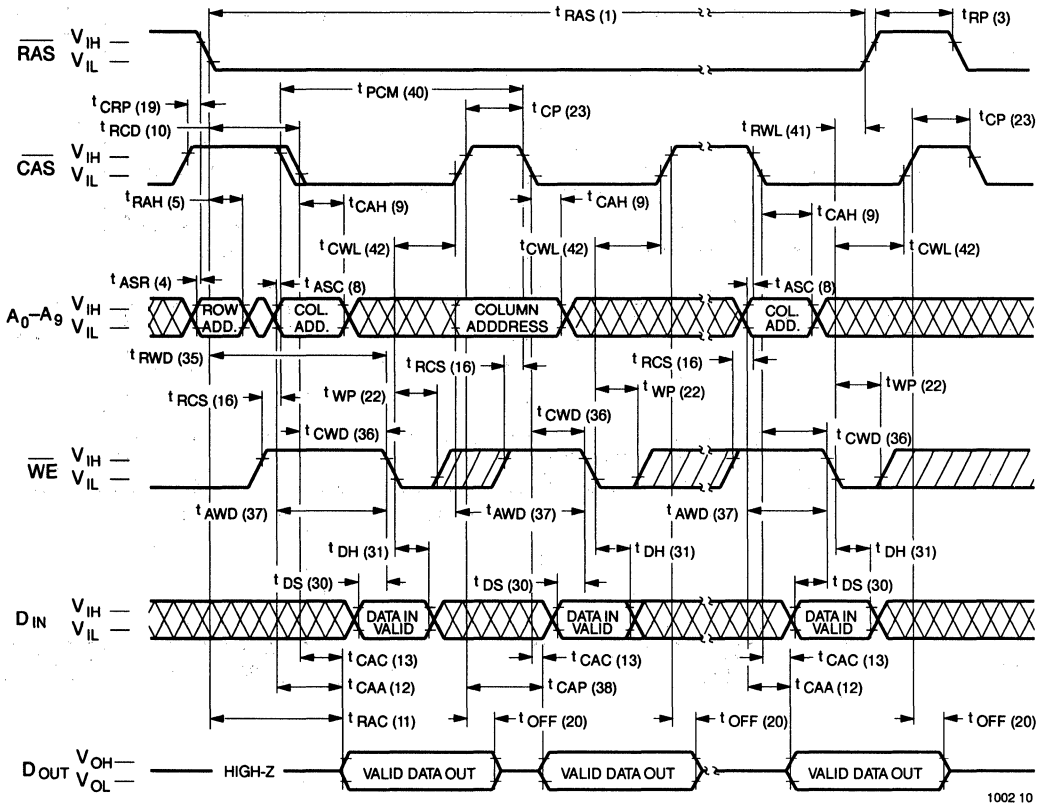
Waveforms of Fast Page Mode Read Cycle



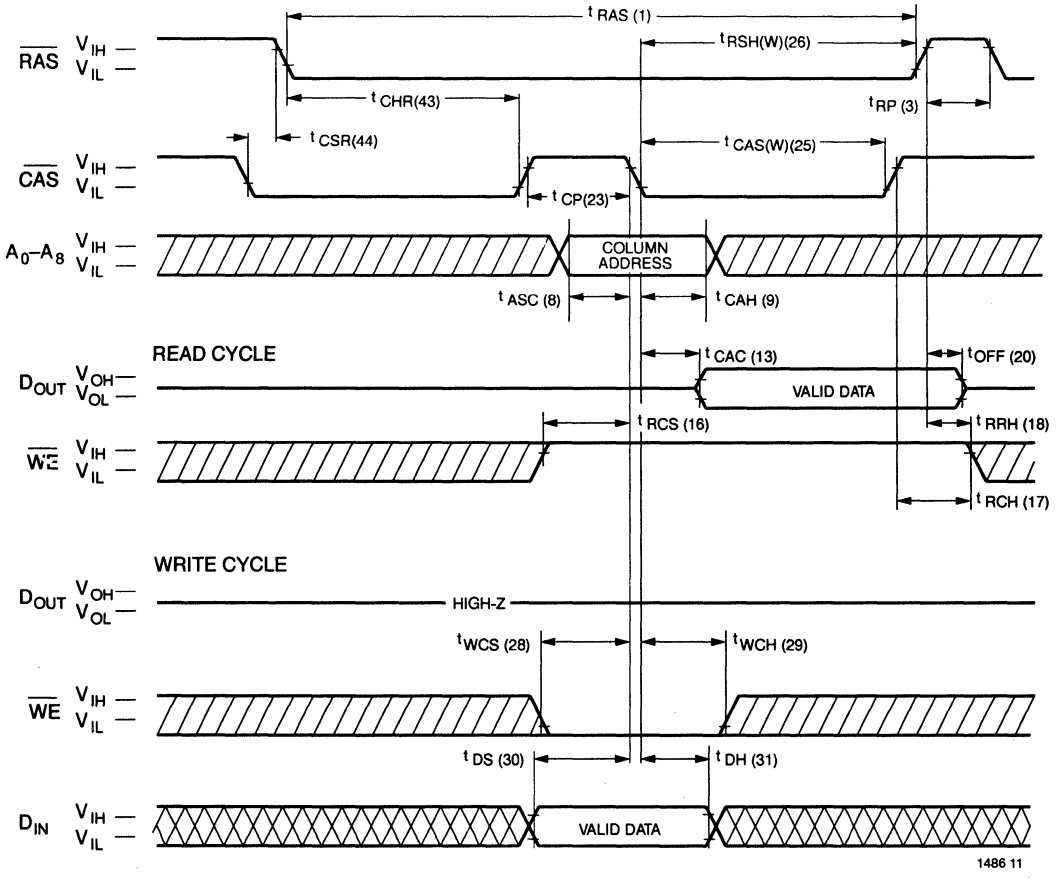
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Modify-Write Cycle



Waveforms of Refresh Counter Test Cycle



Functional Description

The V53C100N is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C100N reads and writes data by multiplexing a 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} (min.) and t_{CAC} (min.) are both satisfied.

Write Cycle

A Write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the output (D_{OUT}) pin will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to Refresh the memory:

1. By selecting all 512 address combinations of A0 through A8 each 8 ms, a refresh of all rows is completed. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C100N will use the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, D_{OUT} will remain in the High-Z state during the cycle.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to write consecutive data patterns (512 Write cycles) and then verify the written data by applying 512 consecutive Read cycles. In this mode, the V53C100N ignores external row/column addresses and takes the output from the internal counter instead.

Data Retention Mode

The V53C100N offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C100N power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high.

Thus, access begins at the occurance of a valid column address rather than at the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as on output enable.

During Fast Page Mode operation, Read, Write, Read-Modify-Write, or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is determined by the by the $\overline{CAS}$ rising edge. If the column address is valid after the rising edge of $\overline{CAS}$, the access is timed from the occurrance of the valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 25 MHz for applications that require high data rates like bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{1{,}024}{t_{RC} + 1{,}023 \times t_{PC}}$$

Data Output Operation

The V53C100N Data Output pin (D_{OUT}) has a three-state capability and is controlled by $\overline{CAS}$. When $\overline{CAS}$ is high($\geq V_{IH}$), the output is in the High-Z state. Table 1 summarizes the D_{OUT} states possible for various memory cycles.

Power On

After application of the V_{DD} an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval). During power on, the V_{DD} current requirement of the V53C100N is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on to avoid current surges.

Table 1. V53C100N Data Output
Operation for Various Cycle Types

Cycle Type	D_{OUT} State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	Active, not valid
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

2

V53C104A
HIGH PERFORMANCE, LOW POWER 256K X 4 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C104A	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	45 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns
Min. Read/Write Cycle Time, (t_{RC})	130 ns	150 ns	180 ns

LOW POWER V53C104AL	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	1.0 mA	1.0 mA	1.0 mA

Features

- 256K x 4 organization
- RAS access time: 70, 80, 100 ns
- Low power dissipation for V53C104A-10
  - Operating Current—65 mA max.
  - TTL Standby Current—2.0 mA max.
- Low CMOS Standby Current
  - V53C104A—1.5 mA max.
  - V53C104AL—1.0 mA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Common I/O
- 512 Refresh cycles/8 ms
- On-chip substrate bias generator
- Fast Page Mode for a sustained data rate greater than 22 MHz
- Standard packages are 20 pin Plastic DIP and 26/20 pin SOJ

Description

The V53C104A is a high speed 262144 x 4 bit CMOS dynamic random access memory. Fabricated with VICMOS III technology, the V53C104A offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C104AL).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x4) bits within a row with cycle times as short as 45 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C104A ideally suited for graphics, digital signal processing and high performance computing systems.

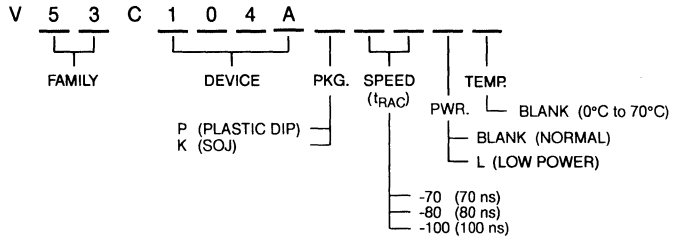
The V53C104AL offers a maximum data retention power of 5.5 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. For selected V53C104AL devices with Refresh Interval longer than 8 ms, consult factory.

Device Usage Chart

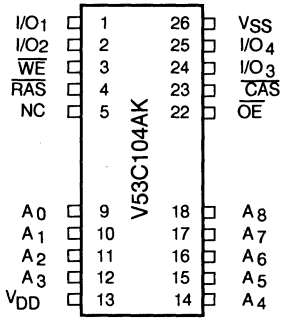
Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	70	80	100	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank

V53C104A Rev. 01 June 1990

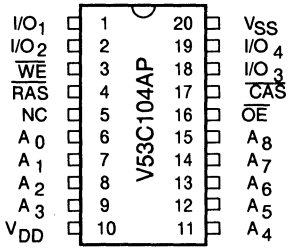
Description	Pkg.	Pin Count
Plastic DIP	P	20
SOJ	K	26/20



26/20 Lead SOJ Package PIN CONFIGURATION Top View



20 Lead Plastic DIP PIN CONFIGURATION Top View



Pin Names

A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_4	Data Input, Output
V_{DD}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... –1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... –1.0 V to +7.0 V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

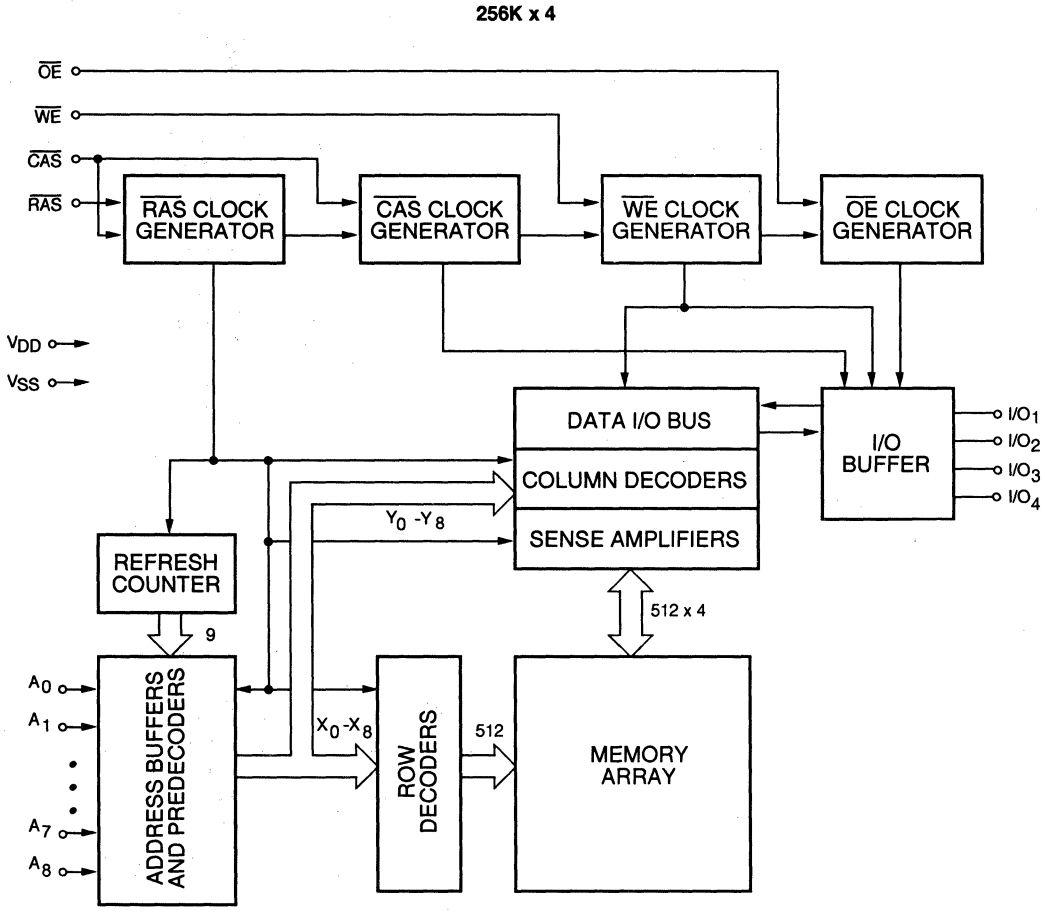
Capacitance*

T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C104A		V53C104AL		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10	10	−10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10	10	−10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	70		85		85	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		80		75		75			
		100		65		65			
I_{DD2}	V_{DD} Supply Current, TTL Standby			2.0		2.0	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	70		85		85	mA	$t_{RC} = t_{RC}$ (min.)	2
		80		75		75			
		100		65		65			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	70		65		65	mA	Minimum Cycle	1, 2
		80		55		55			
		100		50		50			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			3.0		2.0	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	
I_{DD6}	V_{DD} Supply Current,			1.5		1.0	mA	$\overline{RAS}$ ≥ V_{DD} −0.2 V, $\overline{CAS}$ at V_{IH} all other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage		−1.0	0.8	−1.0	0.8	V		3
V_{IH}	Input High Voltage		2.4	V_{DD}+1	2.4	V_{DD}+1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4			I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		70		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	25	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		20		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		10		10		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		20		20		25	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20		25	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		45	ns	6,7, 10

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	20	0	20	0	20	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		75		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		25		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		20		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		20		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		75		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		20		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	20		20		25		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	20		20		25		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	185		205		245		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	125		135		165		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	50		50		60		ns	12

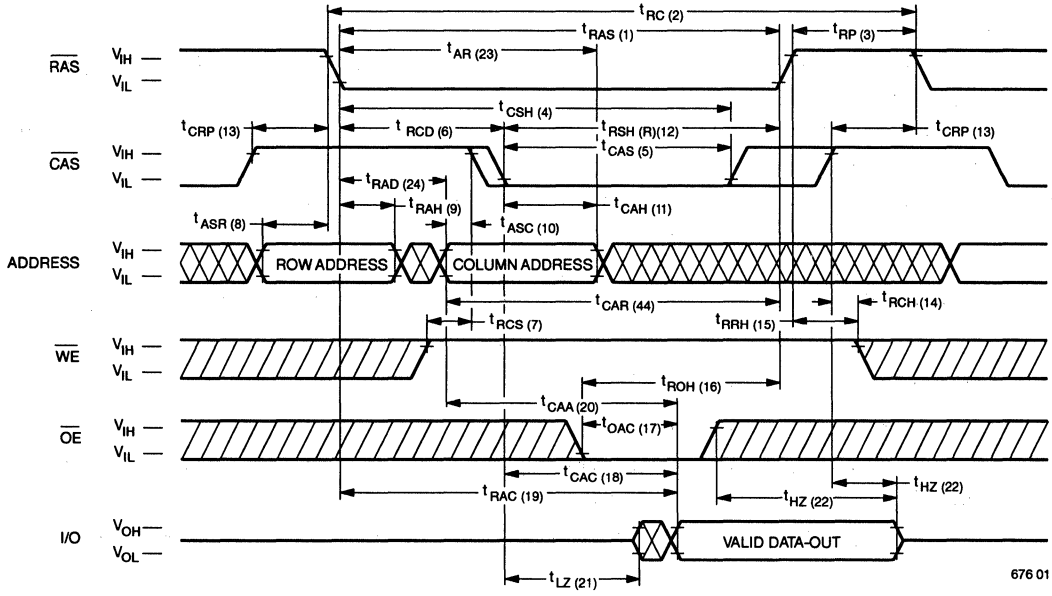
AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	100		110		135		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	75		75		90		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	65		70		80		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55		60		75		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		30		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95		100		115		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (512 Cycles)		8		8		8	ms	17

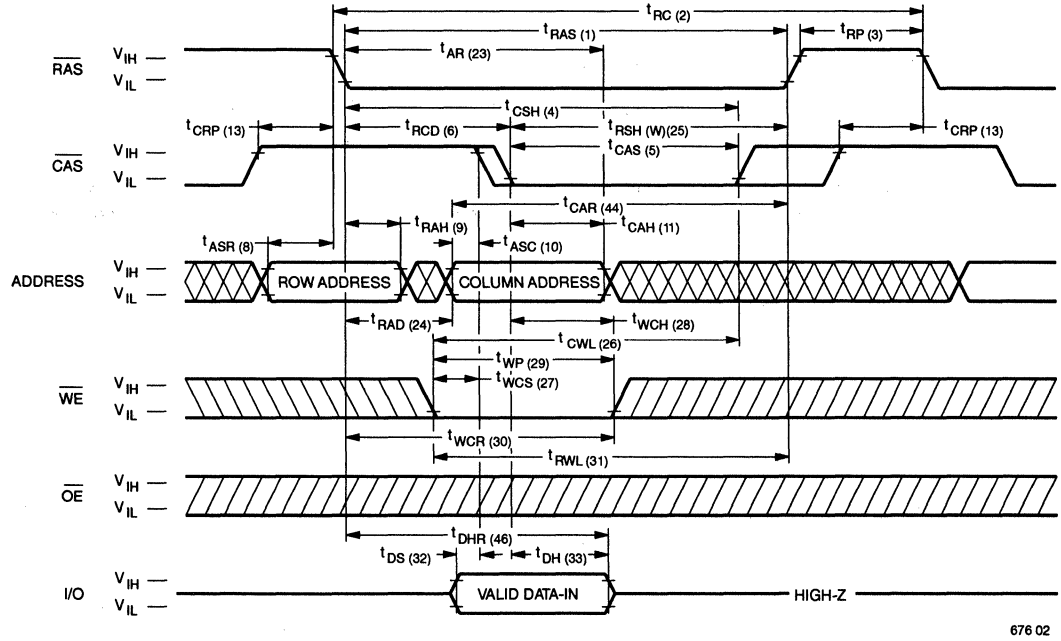
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

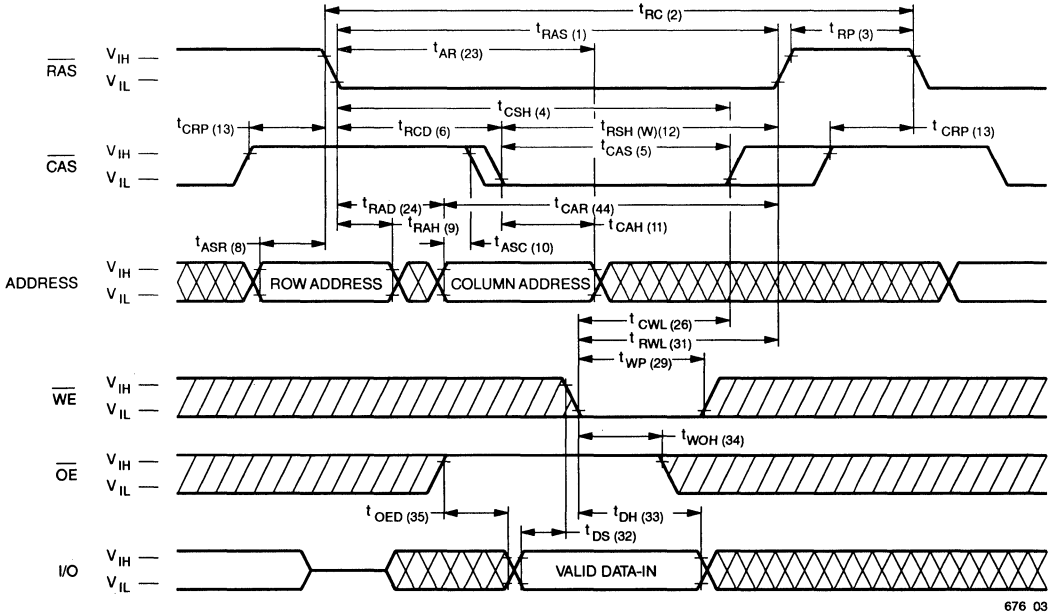
Waveforms of Read Cycle



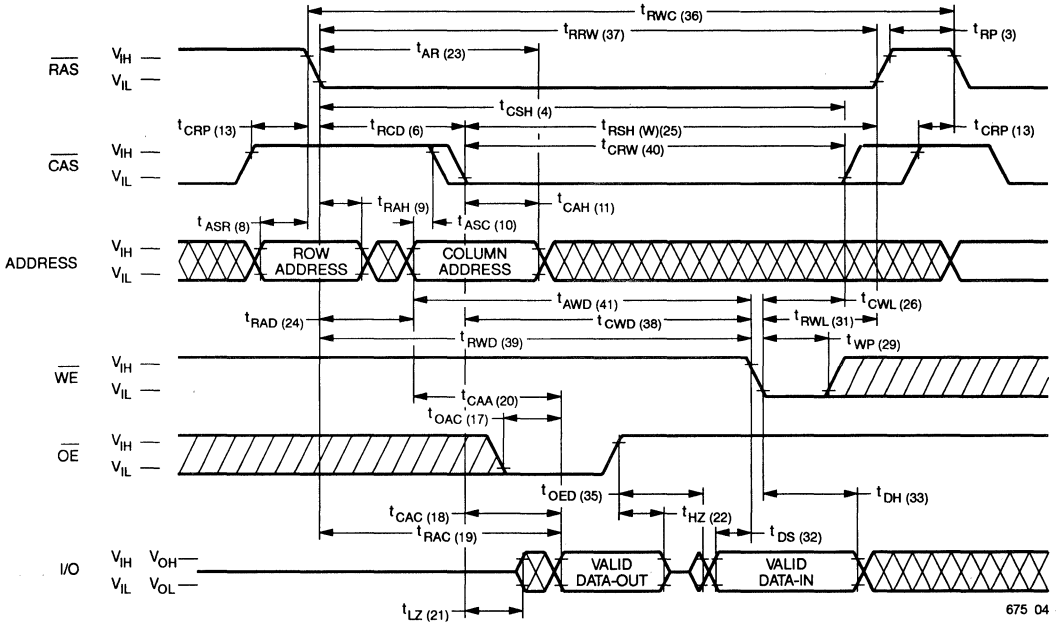
Waveforms of Early Write Cycle



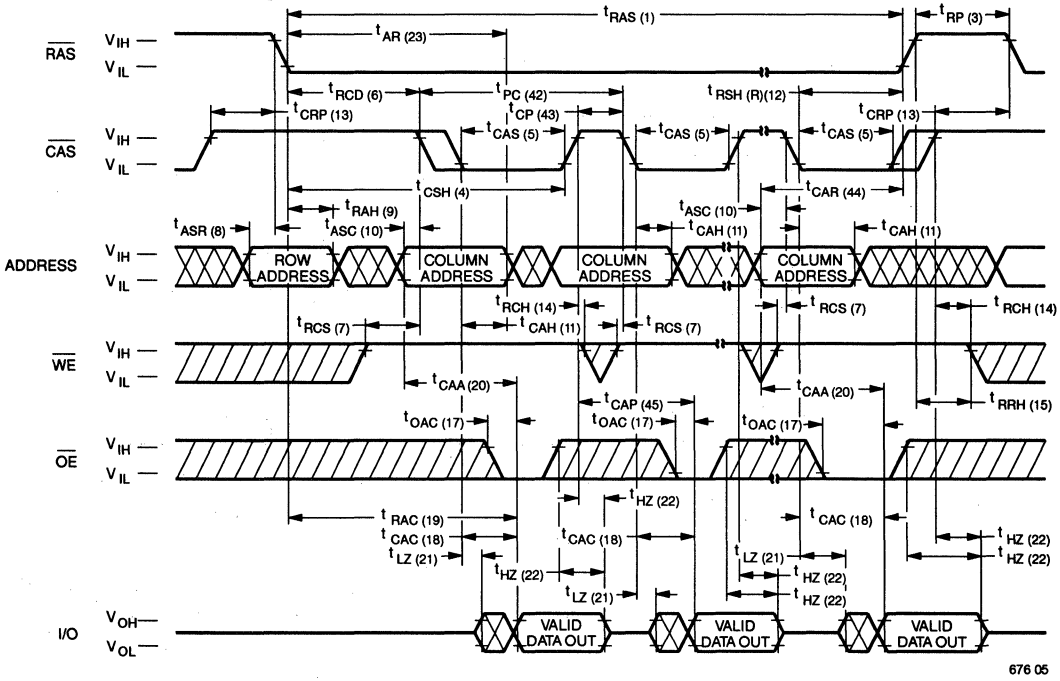
Waveforms of $\overline{OE}$-Controlled Write Cycle



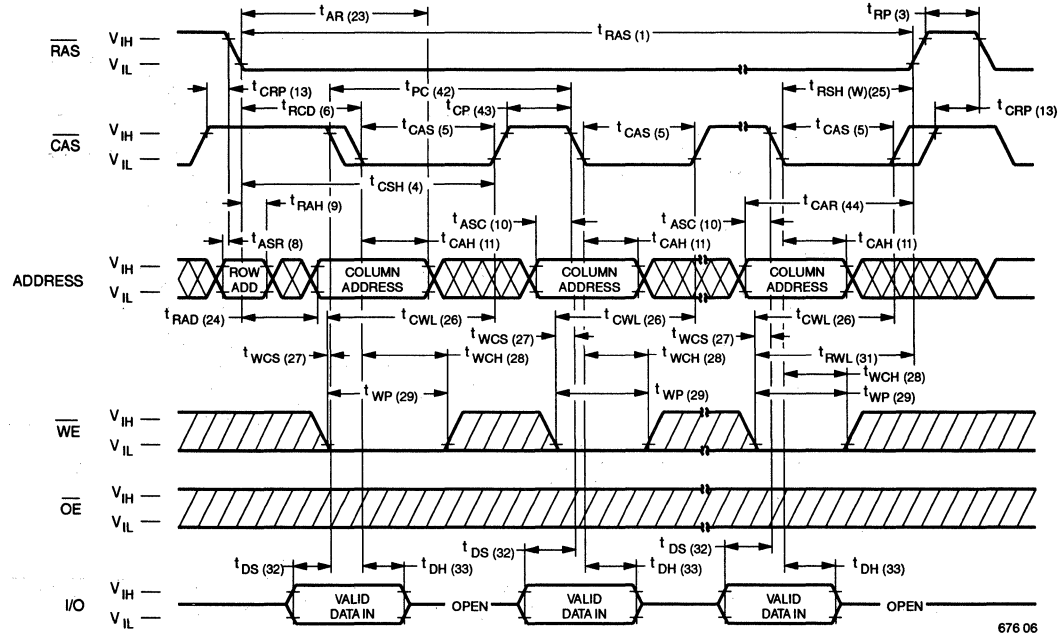
Waveforms of Read-Modify-Write Cycle



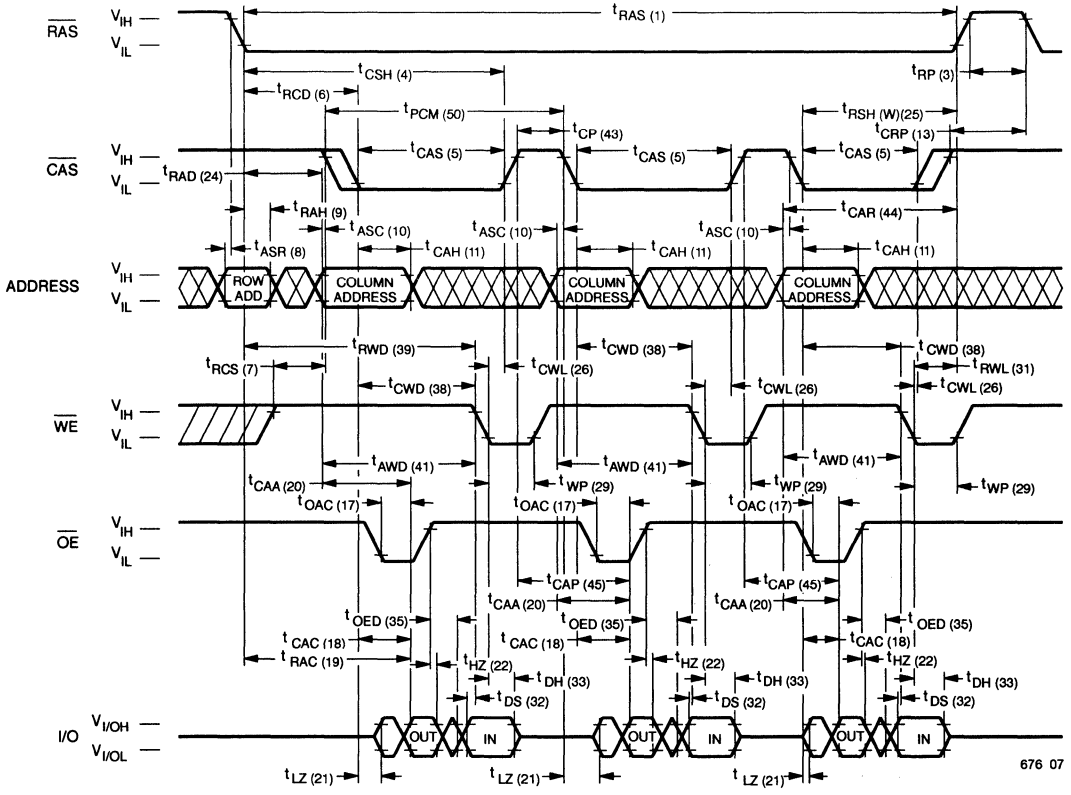
Waveforms of Fast Page Mode Read Cycle



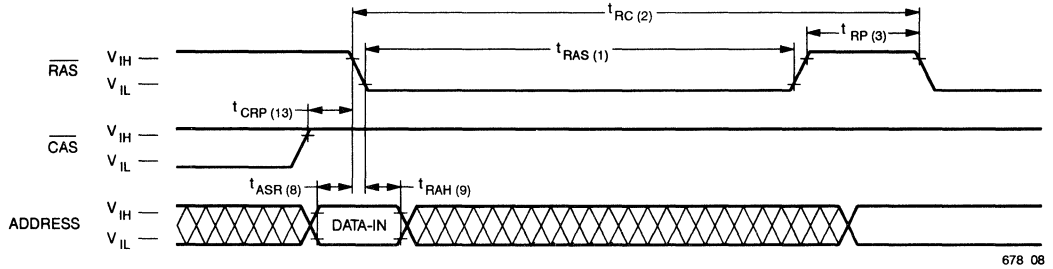
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Write Cycle

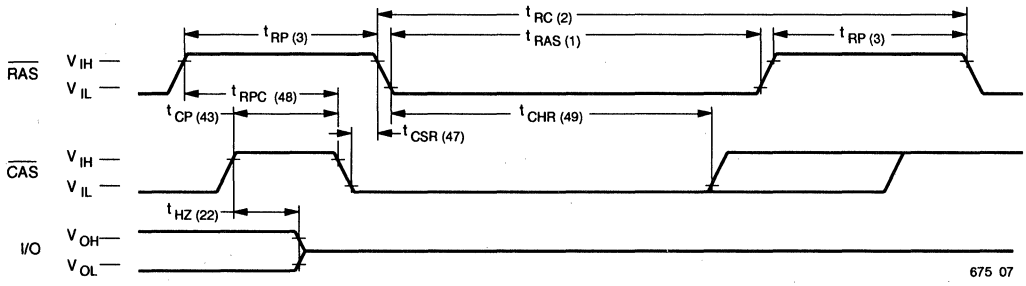


Waveforms of RAS-Only Refresh Cycle



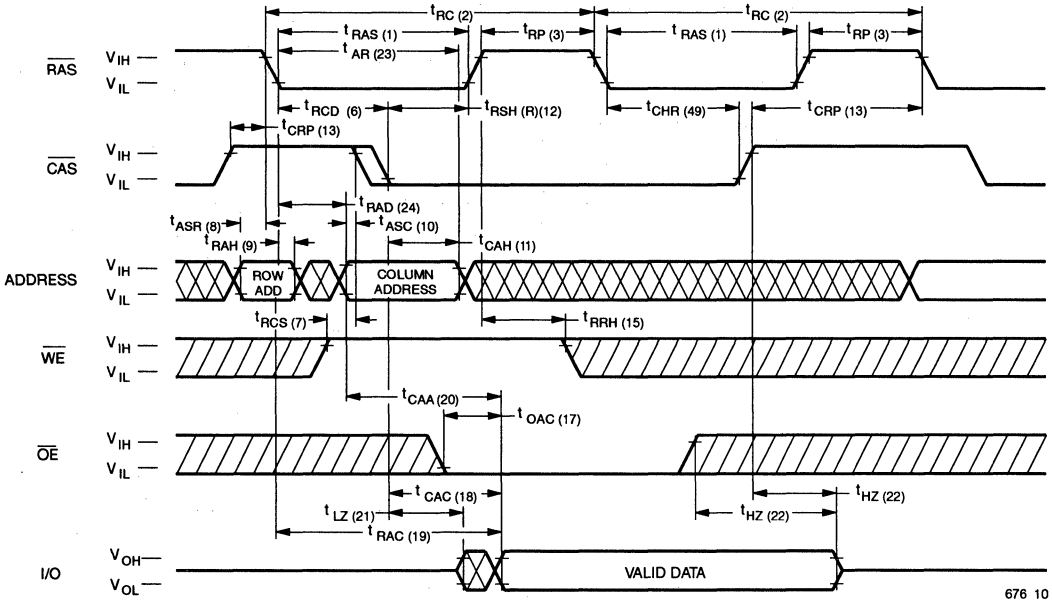
NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

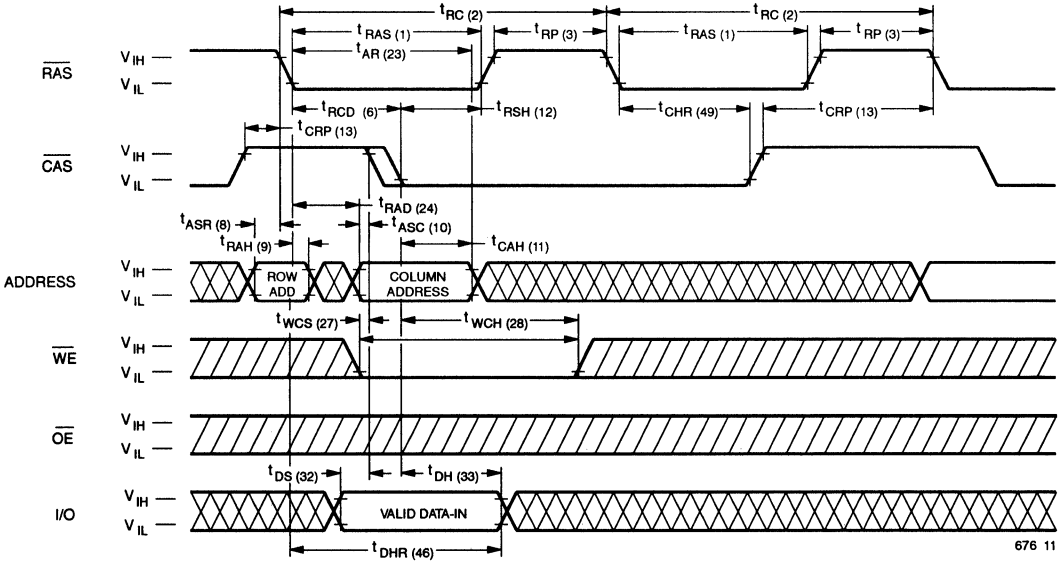


NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_7 = Don't care

Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



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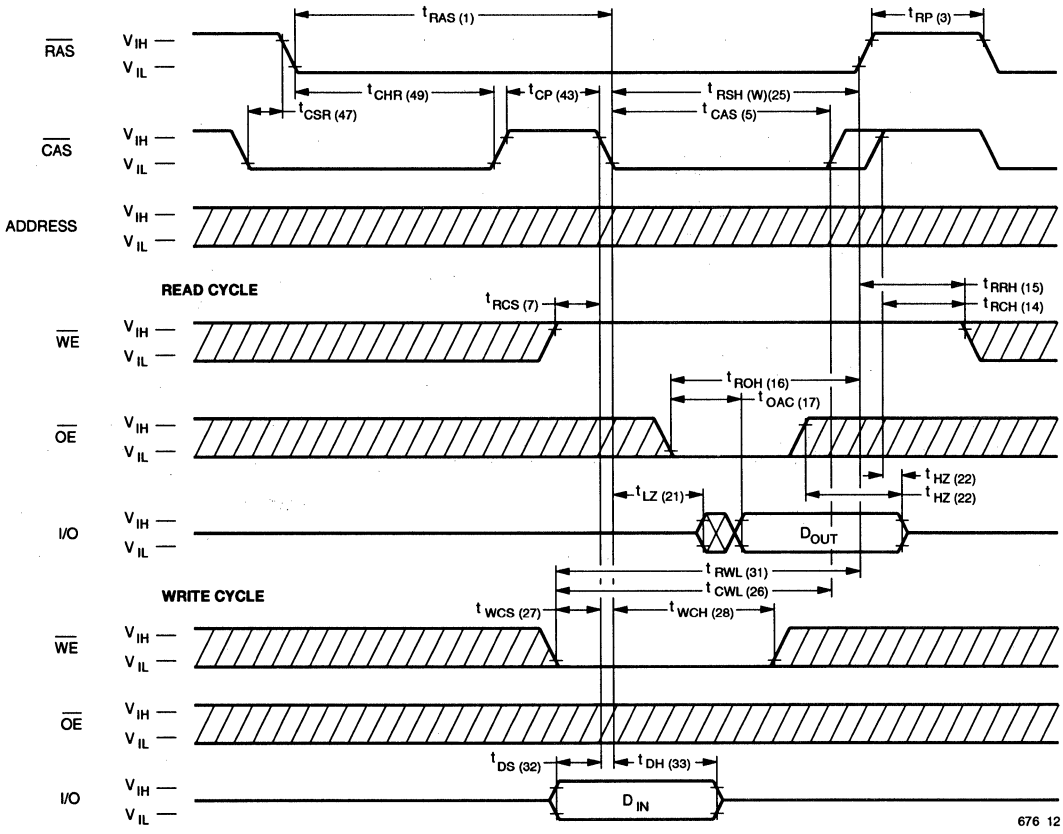
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C104A is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C104A reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C104A uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C104A offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C104A power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 22MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Data Output Operation

The V53C104A Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During power on, the V_{DD} current requirement of the V53C104A is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C104A Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

V53C104F
HIGH PERFORMANCE, LOW POWER
256K X 4 BIT FAST PAGE MODE
CMOS DYNAMIC RAM

PRELIMINARY

HIGH PERFORMANCE V53C104F	60/60L	70/70L	80/80L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns

LOW POWER V53C104FL	60L	70L	80L
Max. CMOS Standby Current, (I_{DD6})	200µA	200µA	200µA

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Features

- 256K x 4 Organization
- RAS access time: 60,70,80 ns
- Low power dissipation for V53C104F-80
  - Operating Current – 70 mA max.
  - TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C104F – 1.0 mA max.
  - V53C104FL – 0.2 mA max.
- Read-Modify-Write, RAS-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability.
- Common I/O capability
- Refresh Interval
  - V53C104F – 512 cycles/8ms
  - V53C104FL – 512 cycles/64ms
- Fast Page Mode for a sustained data rate greater than 25 MHz
- Standard packages are 20 pin Plastic DIP and 26/20 pin SOJ
- Low Battery Back-up Current
  - V53C104FL – 300 µA max.
  - 200 µA max. available on request

Description

The V53C104F is a high speed 262,144 x 4 bit CMOS dynamic random access memory. The V53C104F offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C104FL).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x4) bits within a row with cycle times as short as 40 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C104F ideally suited for graphics, digital signal processing and high performance computing systems.

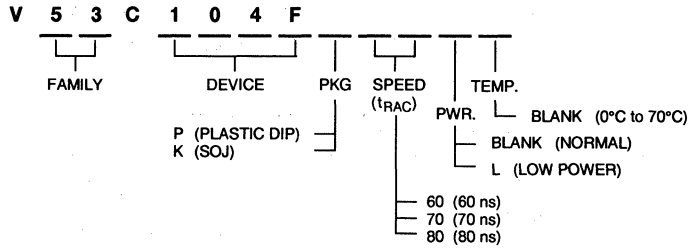
The V53C104FL offers a maximum data retention power of 1.65 mW when operating in CMOS standby mode and performing CAS-before-RAS refresh cycles.

Device Usage Chart

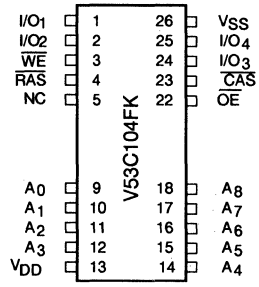
Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	60	70	80	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank

V53C104F Rev. 01 January 1993

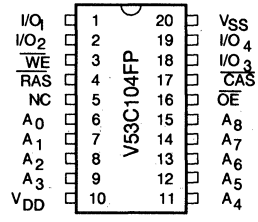
Description	Pkg.	Pin Count
Plastic DIP	P	20
SOJ	K	26/20



26/20 Lead SOJ Package PIN CONFIGURATION Top View



20 Lead Plastic DIP PIN CONFIGURATION Top View



Pin Names

A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_4	Data Input, Output
V_{DD}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

*Absolute Maximum Ratings**

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... –1.0 V to +7.0 V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

*Capacitance**

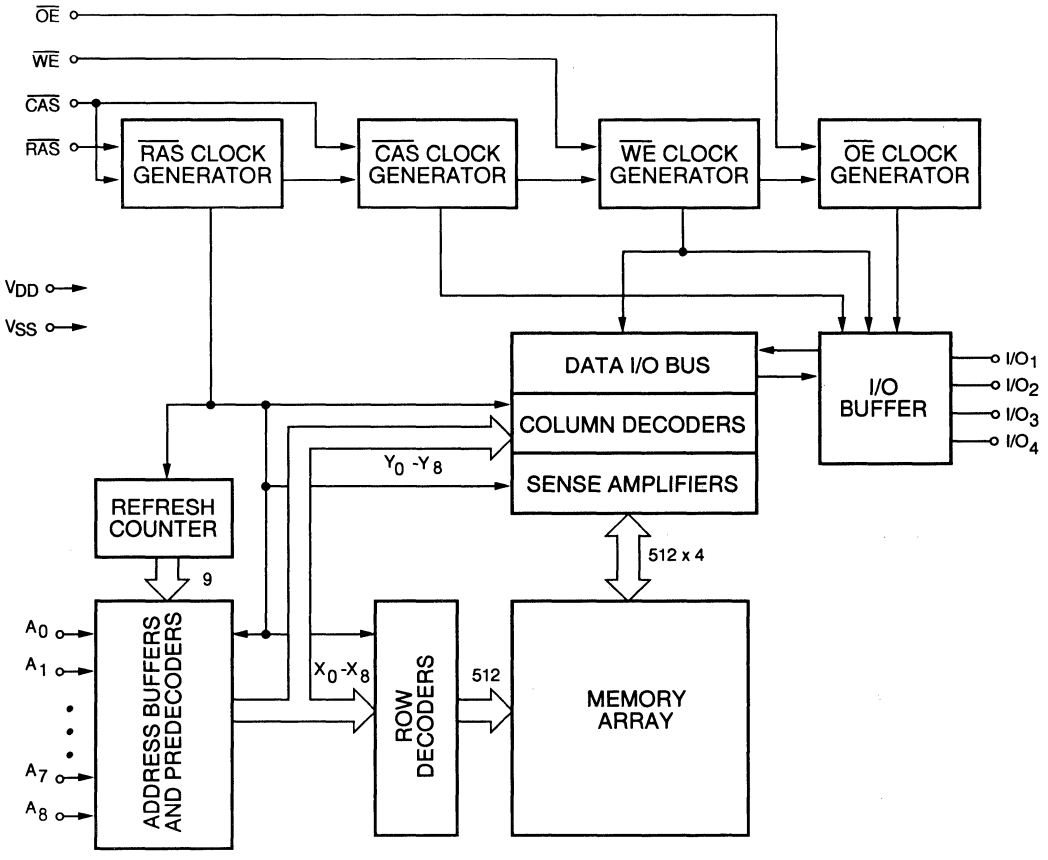
T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram

256K x 4



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C104F		V53C104FL		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10	10	−10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10	10	−10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60		90		90	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		70		80		80			
		80		70		70			
I_{DD2}	V_{DD} Supply Current, TTL Standby			2.0		2.0	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60		90		90	mA	$t_{RC} = t_{RC}$ (min.)	2
		70		80		80			
		80		70		70			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60		80		80	mA	Minimum Cycle	1, 2
		70		70		70			
		80		60		60			
I_{DD5}	Standby, Output Enabled			3.0		2.0	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current CMOS Standby			1.0		0.2	mA	$\overline{RAS}$ ≥ V_{DD} −0.2 V, $\overline{CAS}$ ≥ V_{DD} -0.2 V other input ≥ V_{SS}	
V_{IL}	Input Low Voltage		−1.0	0.8	−1.0	0.8	V		3
V_{IL}	Input High Voltage		2.4	V_{DD}+1	2.4	V_{DD}+1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL}= 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4			I_{OH} = -5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	120		130		150		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	15		20		20		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		10		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15		20		20		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		10		10		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		15		20		20	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		15		20		20	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40	ns	6,7, 10

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	20	0	20	0	20	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH\ (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	15		20		20		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		15		15		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		15		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		15		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	15		20		20		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	15		20		20		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	170		185		205		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	105		125		135		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	40		50		50		ns	12

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	85		100		110		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	65		75		75		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	60		65		70		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	40		45		50		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		45		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		35		40		45	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		30		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	85		95		100		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{REF}	Refresh Interval (512 Cycles)		8		8		8	ms	17
		t_{REF}	Refresh Interval V53C104FL Only (512 Refresh cycles, t_{RC}=125 µs)		64		64		64	ms	17,18

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$ before $\overline{RAS}$ refresh cycles.

    t_{RC} = 125 µs (125 µs x 512 = 64 ms)

    $t_{RAS} = t_{RAS}$ (min) to 1 µs

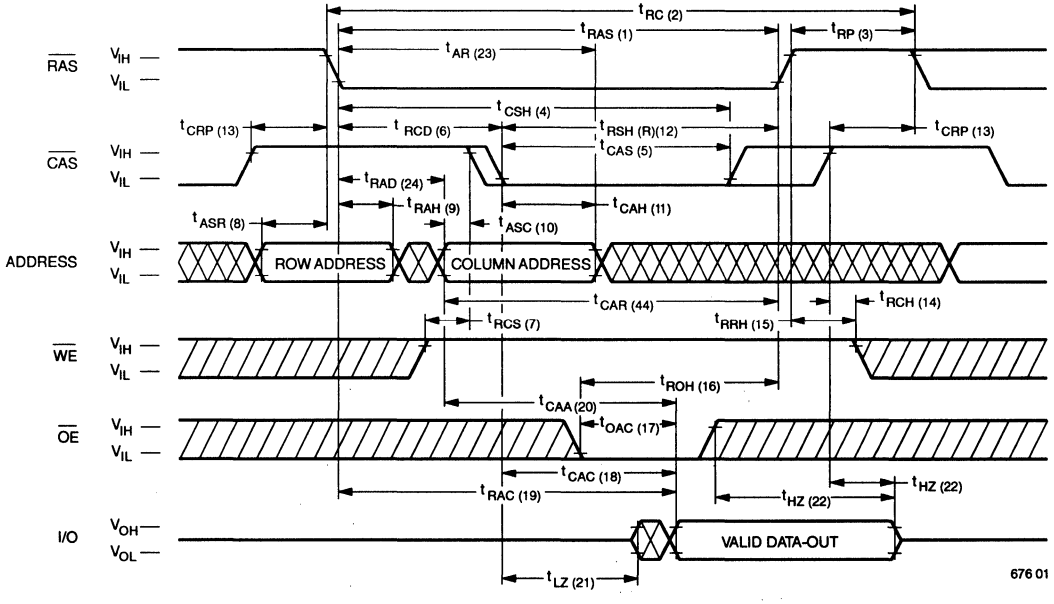
    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V

    $V_{IL} < 0.2$ V

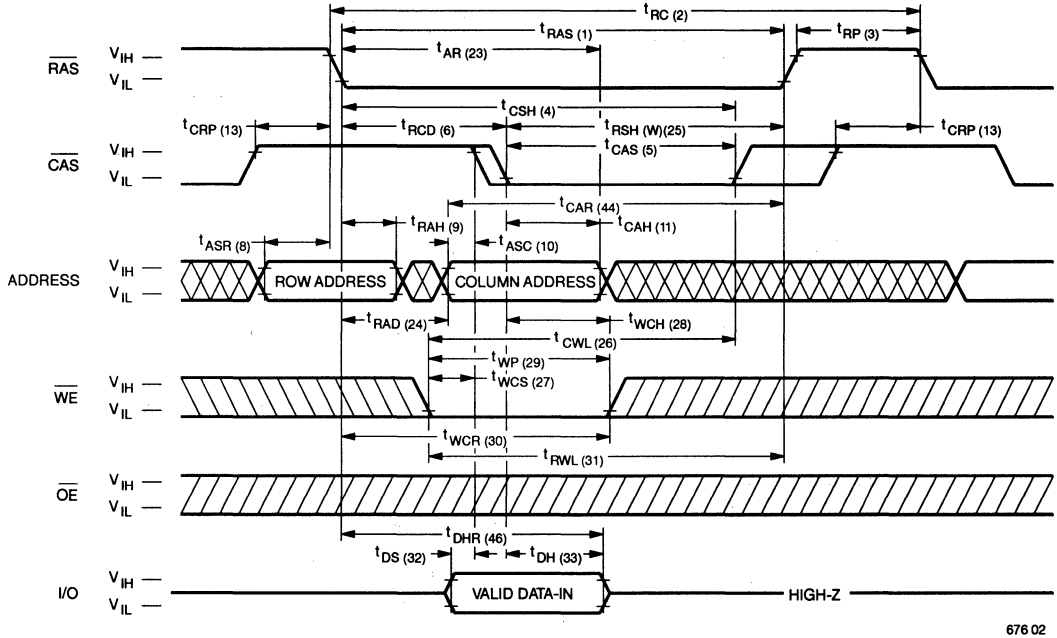
    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V

    All other inputs at stable V_{IH} or V_{IL}

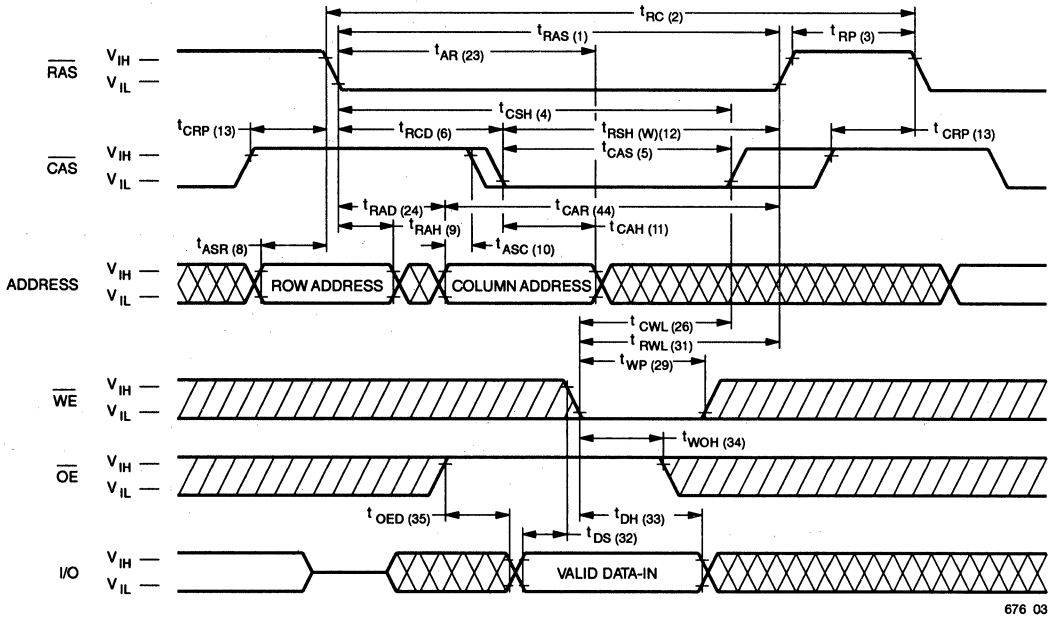
Waveforms of Read Cycle



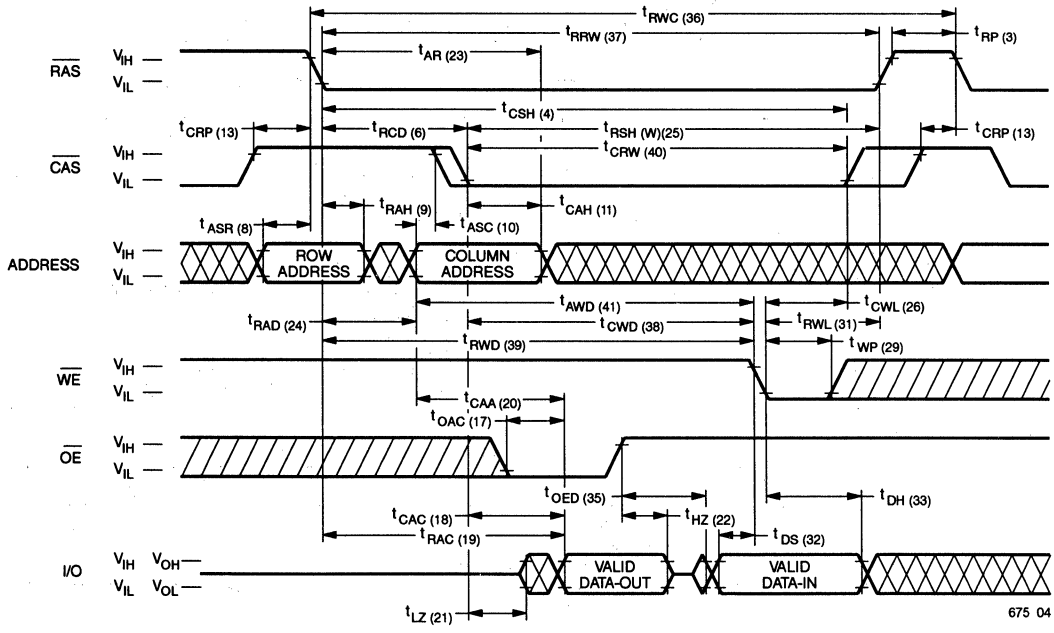
Waveforms of Early Write Cycle



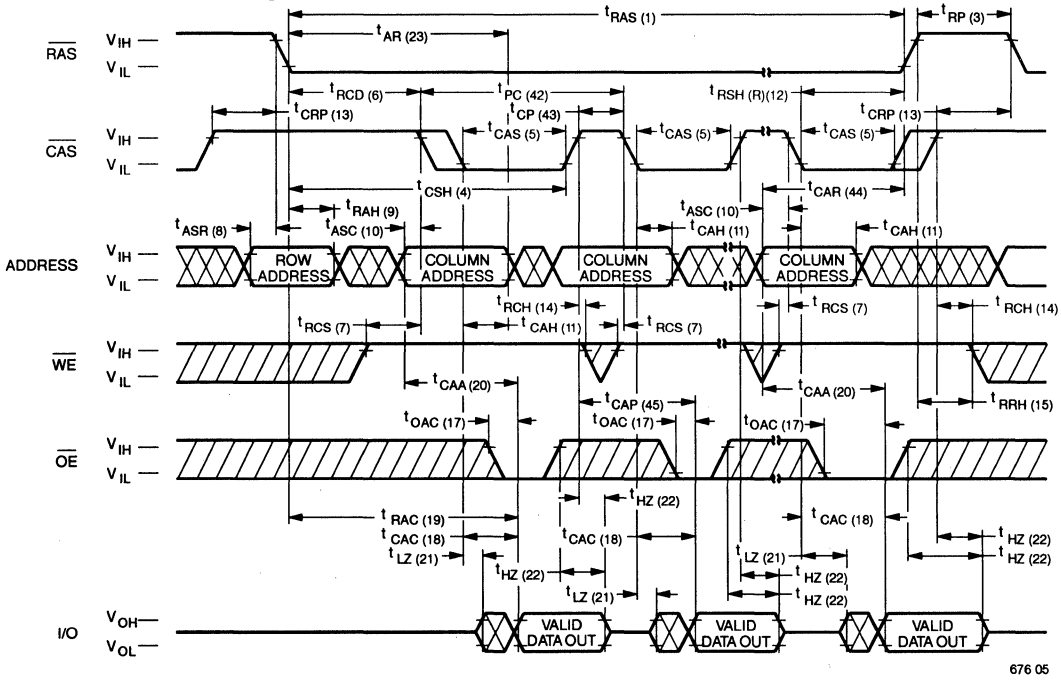
Waveforms of $\overline{OE}$-Controlled Write Cycle



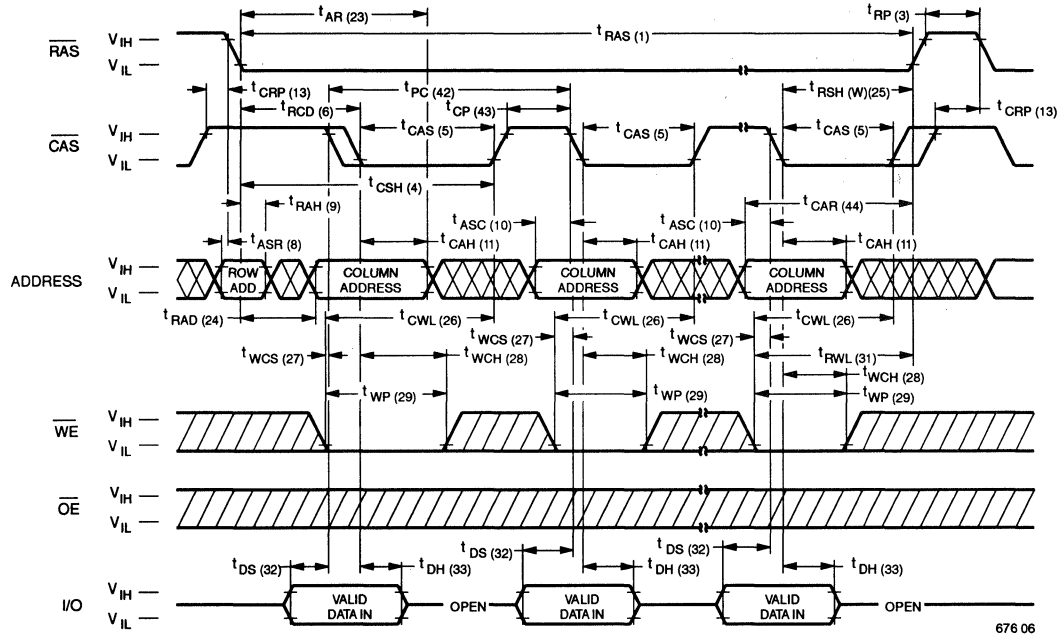
Waveforms of Read-Modify-Write Cycle



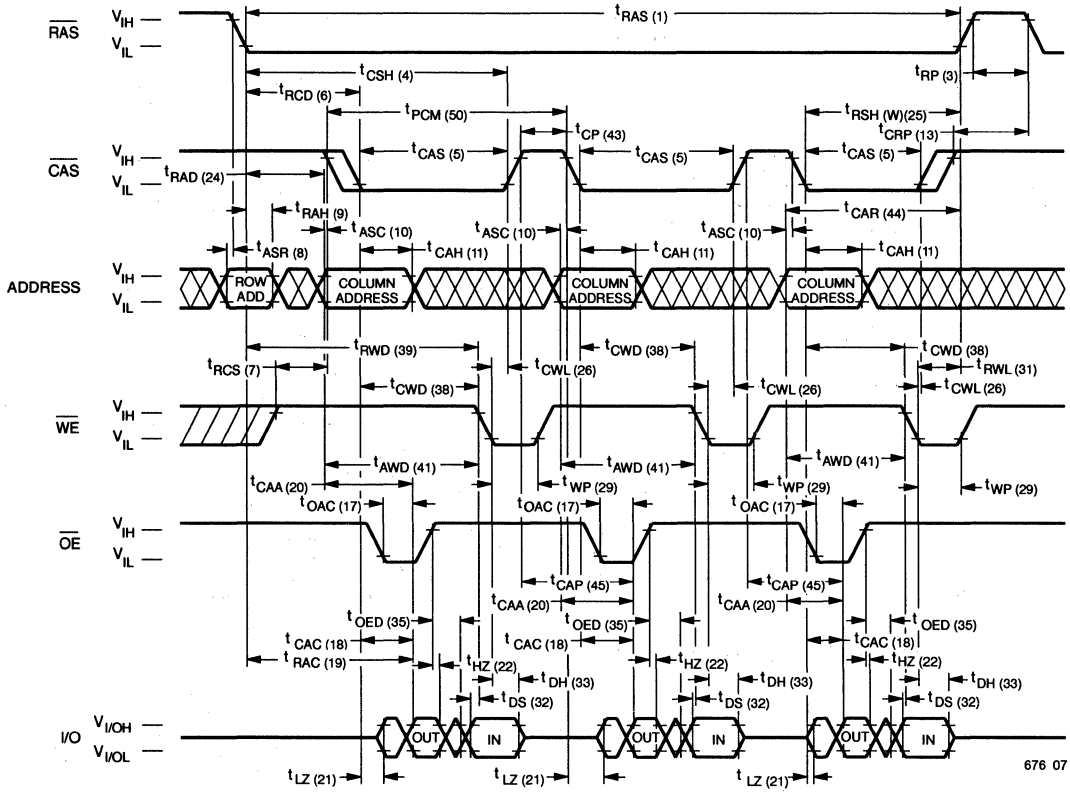
Waveforms of Fast Page Mode Read Cycle



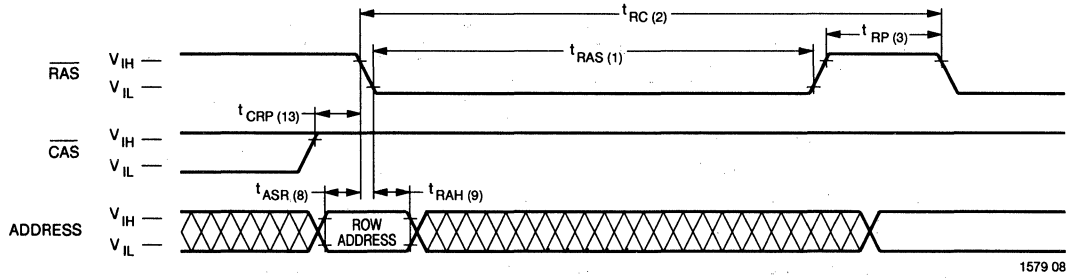
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Write Cycle

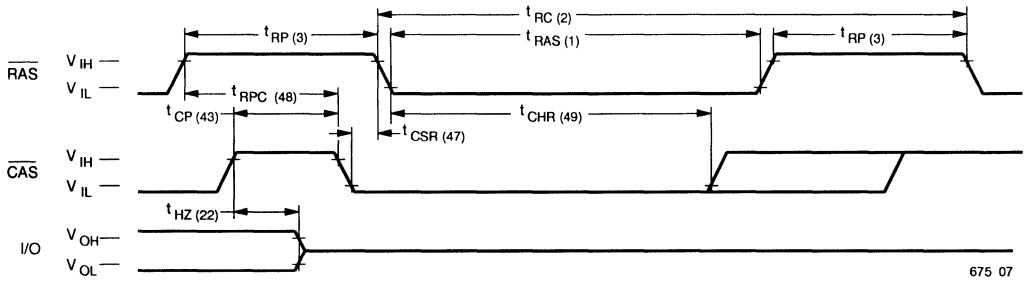


Waveforms of RAS-Only Refresh Cycle



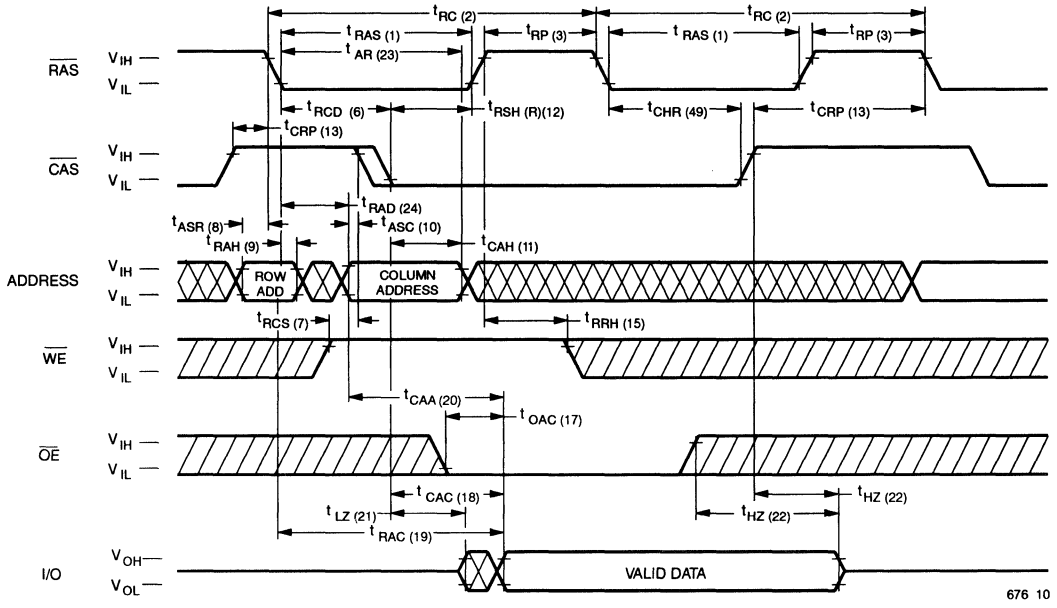
NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

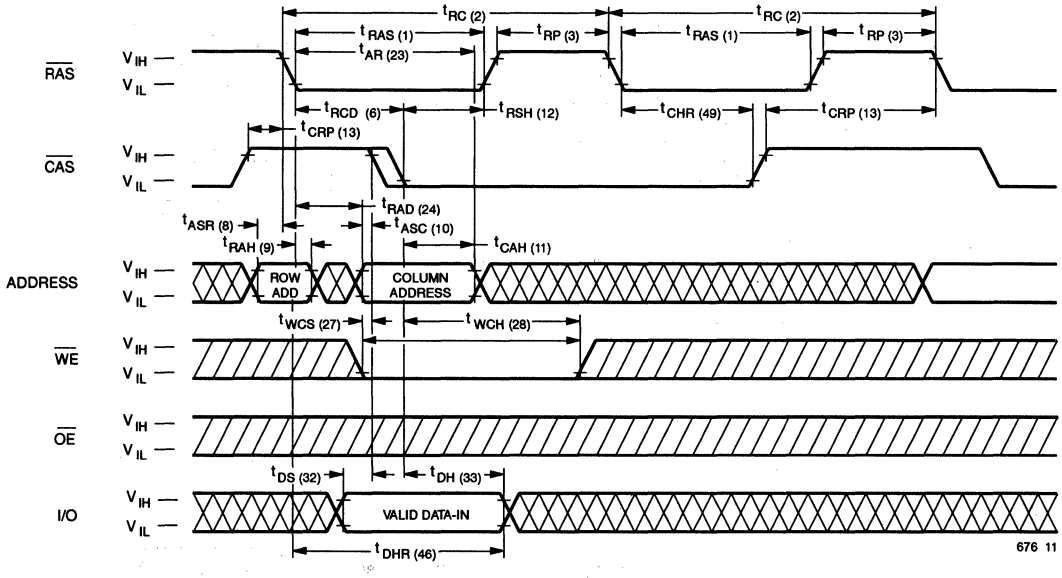


NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_7 = Don't care

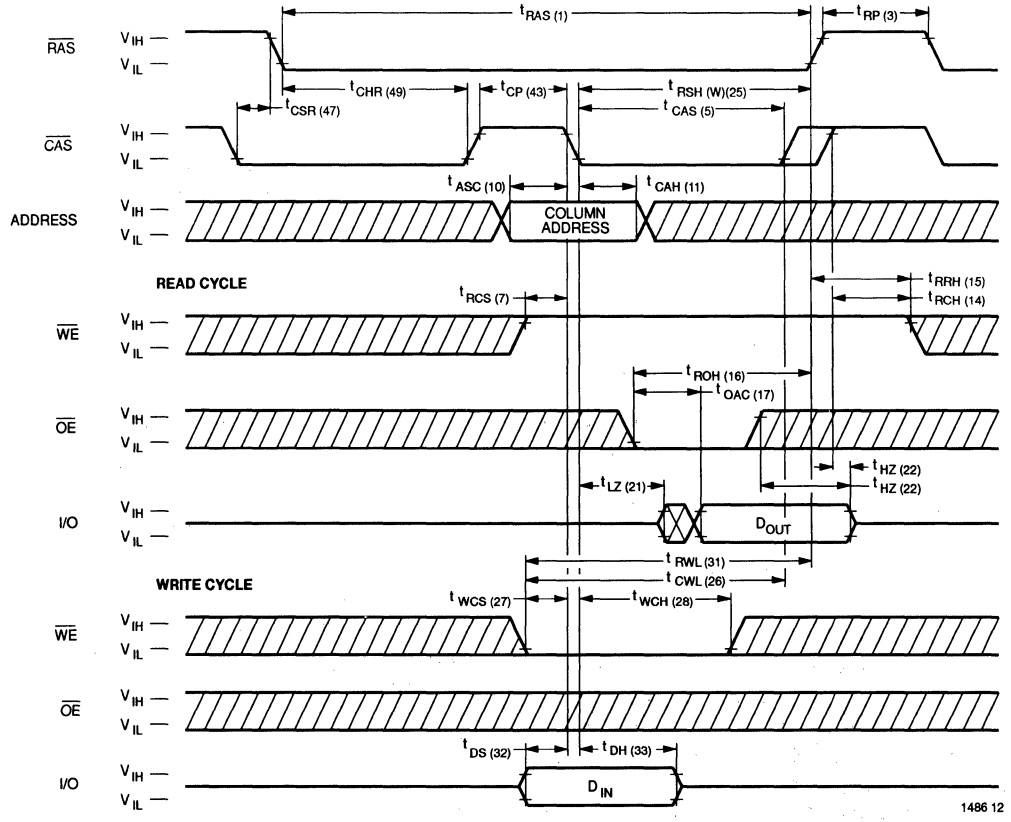
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C104F is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C104F reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C104F uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C104F offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C104F power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 25 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Data Output Operation

The V53C104F Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C104F is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C104F Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

ULTRA-HIGH PERFORMANCE, LOW POWER 256K X 4 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE	45/45L	50/50L	55/55L	60/60L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	45 ns	50 ns	55 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	22 ns	24 ns	28 ns	30 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	25 ns	28 ns	38 ns	40 ns
Min. Read/Write Cycle Time, (t_{RC})	90 ns	100 ns	110 ns	120 ns

LOW POWER V53C104HL	45L	50L	55L	60L
Max. CMOS Standby Current, (I_{DD6})	150 µA	150 µA	150 µA	150 µA

Features

- 256K x 4-bit organization
- $\overline{RAS}$ access time: 45,50,55,60 ns
- Low power dissipation
  - V53C104H-60
    - — Operating Current – 85 mA max
    - — TTL Standby Current – 2.0 mA max
- Low CMOS Standby Current
  - V53C104H – 1.0 mA max
  - V53C104HL – .15 mA max
- Low Battery Back-up Current
  - V53C104HL – 200µA max
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V53C104H – 512 cycles/8 ms
  - V53C104HL – 512 cycles/64 ms
- Fast Page Mode for a sustained data rate greater than 40 MHz
- Available in 20 pin Plastic DIP and 26/20 pin SOJ packages

Description

The V53C104H is a high speed 262,144 x 4 bit CMOS dynamic random access memory. Fabricated with Mosel-Vitelic's VICMOS III technology, the V53C104H offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C104HL).

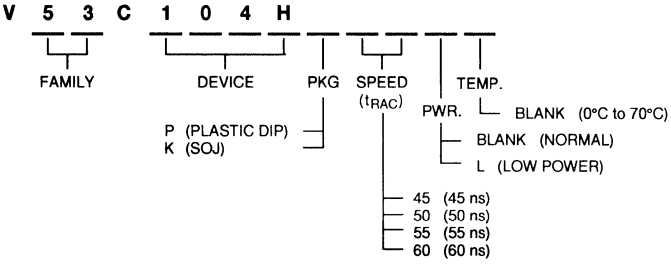
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x4) bits within a row with cycle times as short as 25 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C104H ideally suited for graphics, digital signal processing and high performance computing systems.

The V53C104HL offers a maximum data retention power of 1.1 mW when operating in CMOS standby mode and performing $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. This mode is entered by holding $\overline{RAS}$ at a voltage greater than V_{DD} – 0.2 when it is inactive.

Device Usage Chart

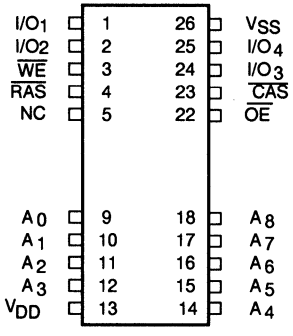
Operating Temperature Range	Package Outline		Access Time (ns)				Power		Temperature Mark
	P	K	45	50	55	60	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	•	Blank

V53C104H Rev. 03 February 1993

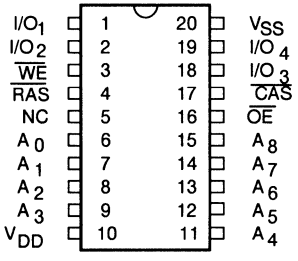


Description	Pkg.	Pin Count
Plastic DIP	P	20
SOJ	K	26/20

26/20 Lead SOJ Package PIN CONFIGURATION Top View



20 Lead Plastic DIP PIN CONFIGURATION Top View



Pin Names

A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_4	Data Input, Output
V_{DD}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 V to +7.0 V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

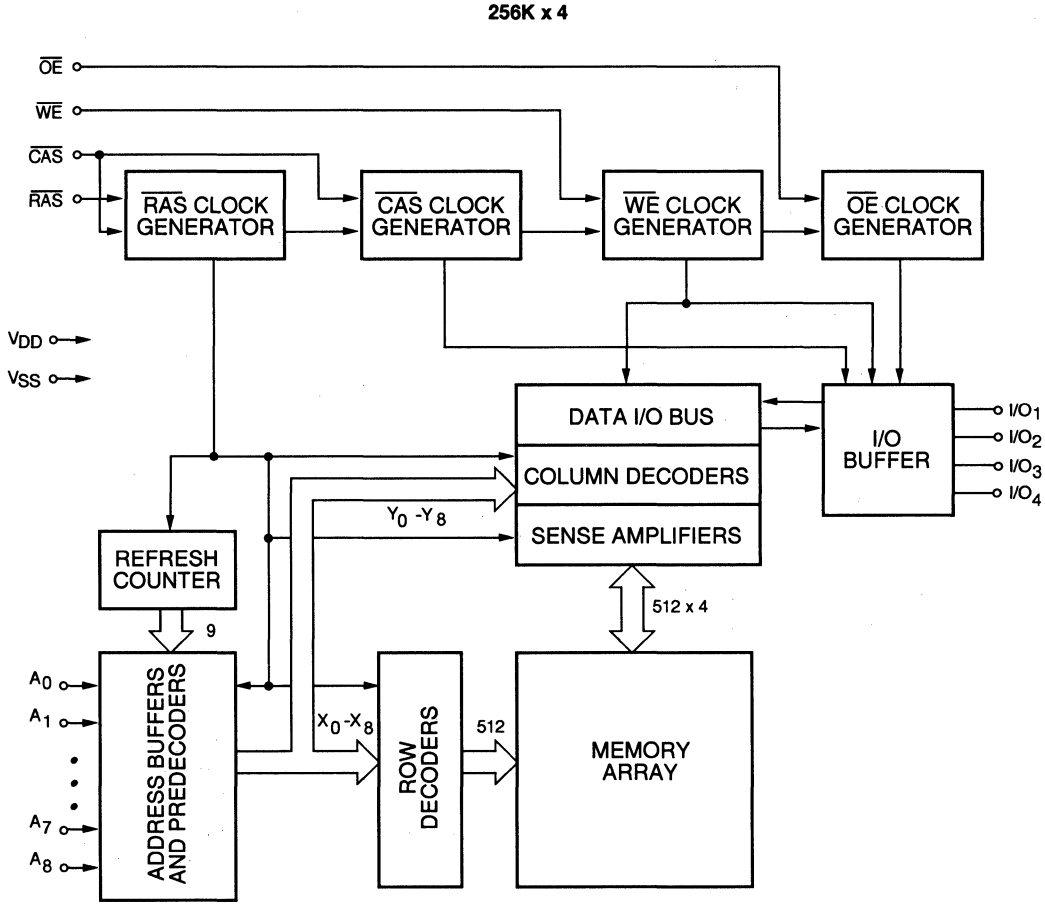
Capacitance*

T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C104H			V53C104HL			Unit	Test Conditions	Notes
			Min.	Typ.	Max.	Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10		10	-10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10		10	-10		10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	45			110			110	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		50			100			100			
		55			90			90			
		60			85			85			
I_{DD2}	V_{DD} Supply Current, TTL Standby				2			2	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	45			110			110	mA	$t_{RC} = t_{RC}$ (min.)	2
		50			100			100			
		55			90			90			
		60			85			85			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	45			100			100	mA	Minimum Cycle	1, 2
		50			90			90			
		55			85			85			
		60			80			80			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled				2.0			2.0	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby				1.0			0.15	mA	$\overline{RAS} \ge V_{DD} - 0.2$ V, $\overline{CAS} \ge V_{DD} - 0.2$ V, All other inputs ≥ V_{SS}	
I_{DD7}	Battery Back-up Data Retention Current (V53C104HL Only)				N.A.			0.2	mA	$\overline{CAS}$-before-$\overline{RAS}$ Refresh cycle t_{RC} = 125 µs CMOS clock levels	18
V_{IL}	Input Low Voltage		−1		0.8	-1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{DD}+1	2.4		V_{DD}+1	V		3
V_{OL}	Output Low Voltage				0.4			0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4			2.4			V	I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	45/L		50/L		55/L		60/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	45	75K	50	75K	55	75K	60	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	90		100		110		120		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	35		40		45		50		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	45		50		55		60		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	12		12		15		15		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	31	19	36	20	40	20	45	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8		9		10		10		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	6		7		10		10		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	14		14		15		15		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	4		4		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	9		9		10		10		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		12		12		15		15	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		12		12		15		15	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		45		50		55		60	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		22		24		28		30	ns	6,7, 10

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	45/L		50/L		55/L		60/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	8	0	8	0	10	0	20	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	30		35		45		50		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	23	14	26	15	27	15	30	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	14		14		15		15		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	14		14		15		15		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	6		7		10		10		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	6		7		10		10		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	30		35		45		50		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	14		14		15		15		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	6		7		10		10		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	9		9		10		10		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	8		8		10		10		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	135		145		160		170		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	85		90		100		105		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	31		33		38		40		ns	12

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	45/L		50/L		55/L		60/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	65		70		80		85		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	50		54		62		65		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	41		43		55		58		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	25		28		38		40		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	7		8		10		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	22		24		28		30		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		24		26		32		34	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	30		35		45		50		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	12		12		15		15		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	65		70		82		85		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
		t_{REF}	Refresh Interval (512 Cycles)		8		8		8		8	ms	17
		t_{REF}	Refresh Interval V53C104HL Only (512 Cycles, t_{RC}= 125 µs)		64		64		64		64	ms	17,18

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

    t_{RC} = 125 µs (125 µs x 512 = 64 ms)

    $t_{RAS} = t_{RAS}$ (min.) to 1 µs

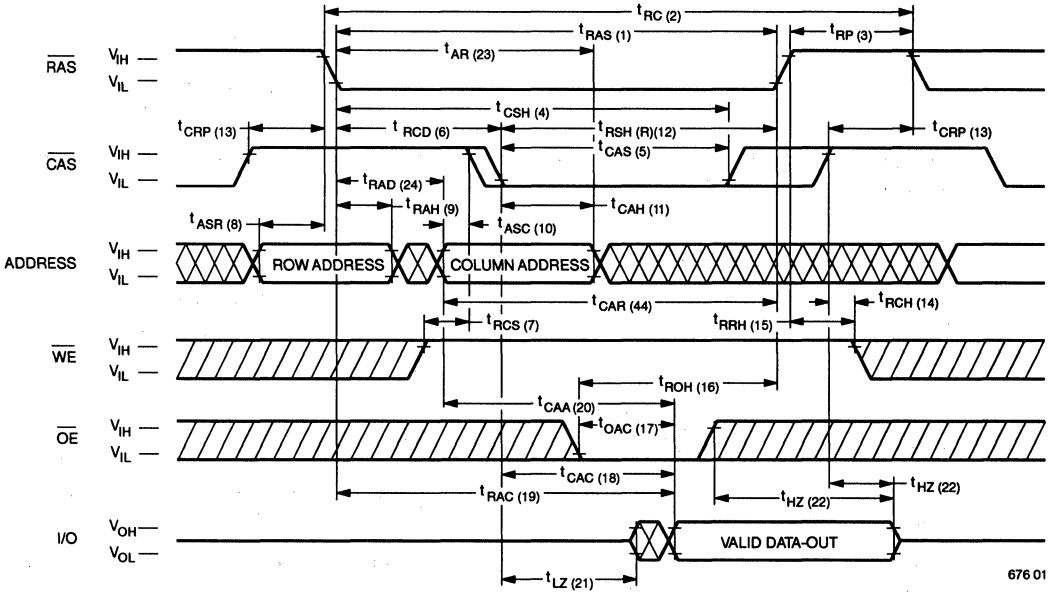
    Input voltages: $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V

    $V_{IL} < 0.2$ V

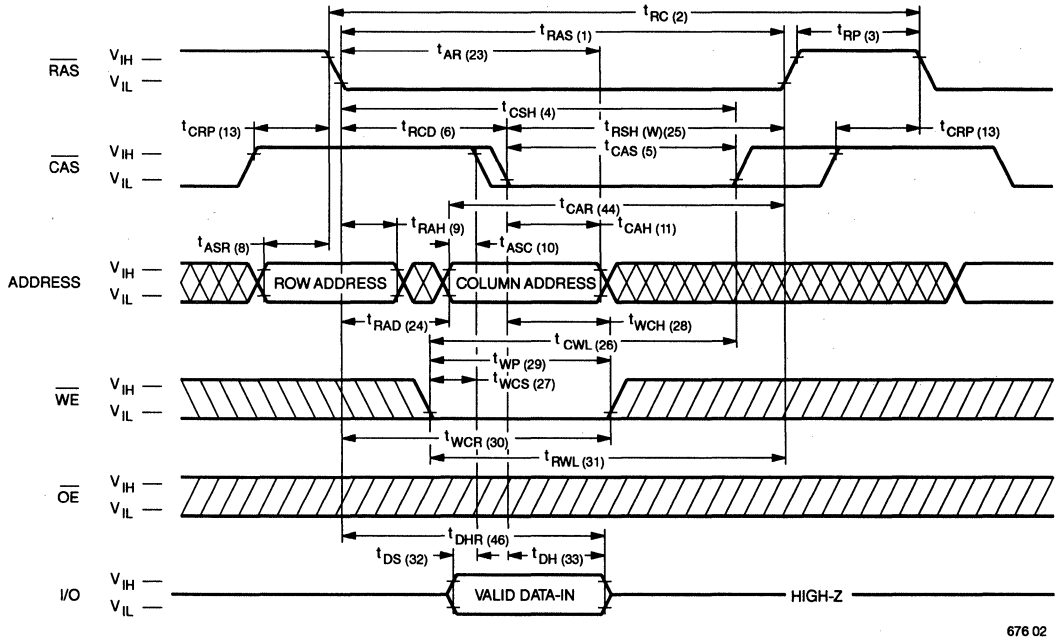
    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V

    All other inputs at stable V_{IH} or V_{IL}

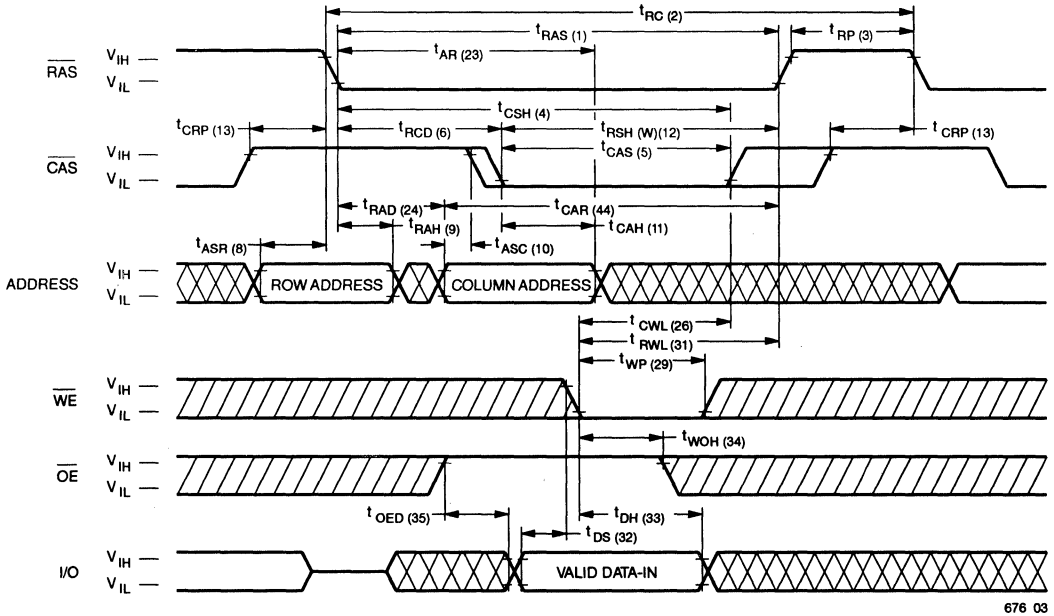
Waveforms of Read Cycle



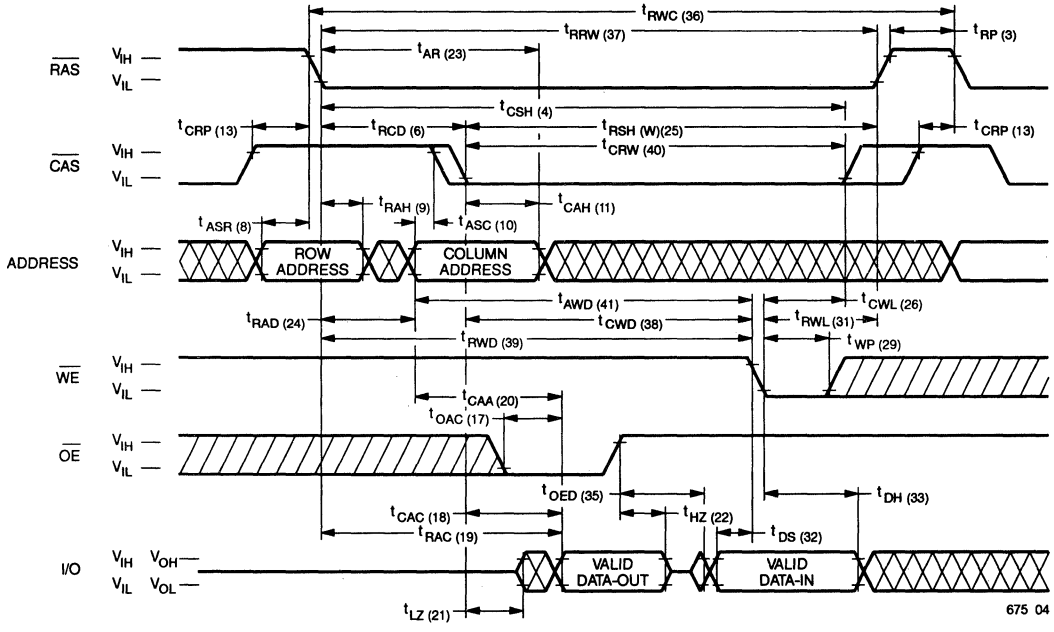
Waveforms of Early Write Cycle



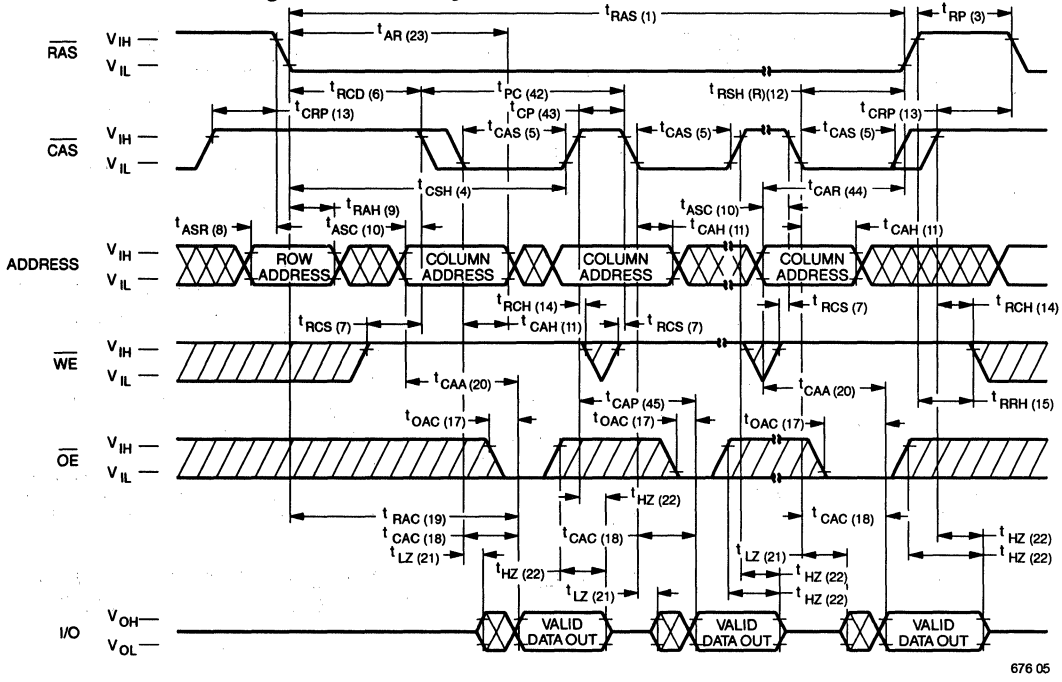
Waveforms of $\overline{OE}$-Controlled Write Cycle



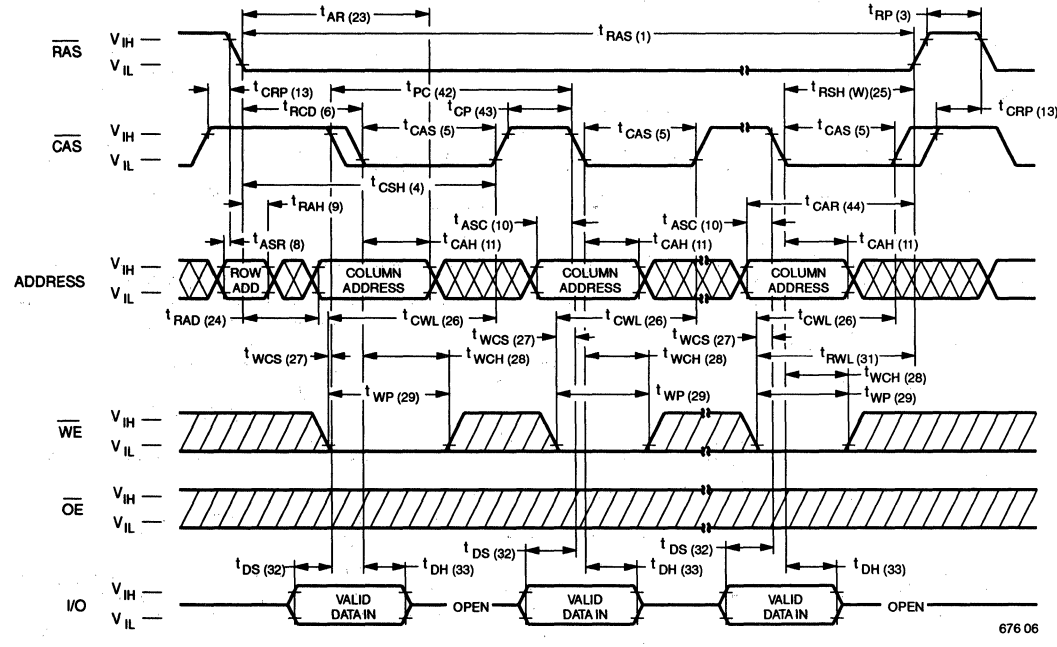
Waveforms of Read-Modify-Write Cycle



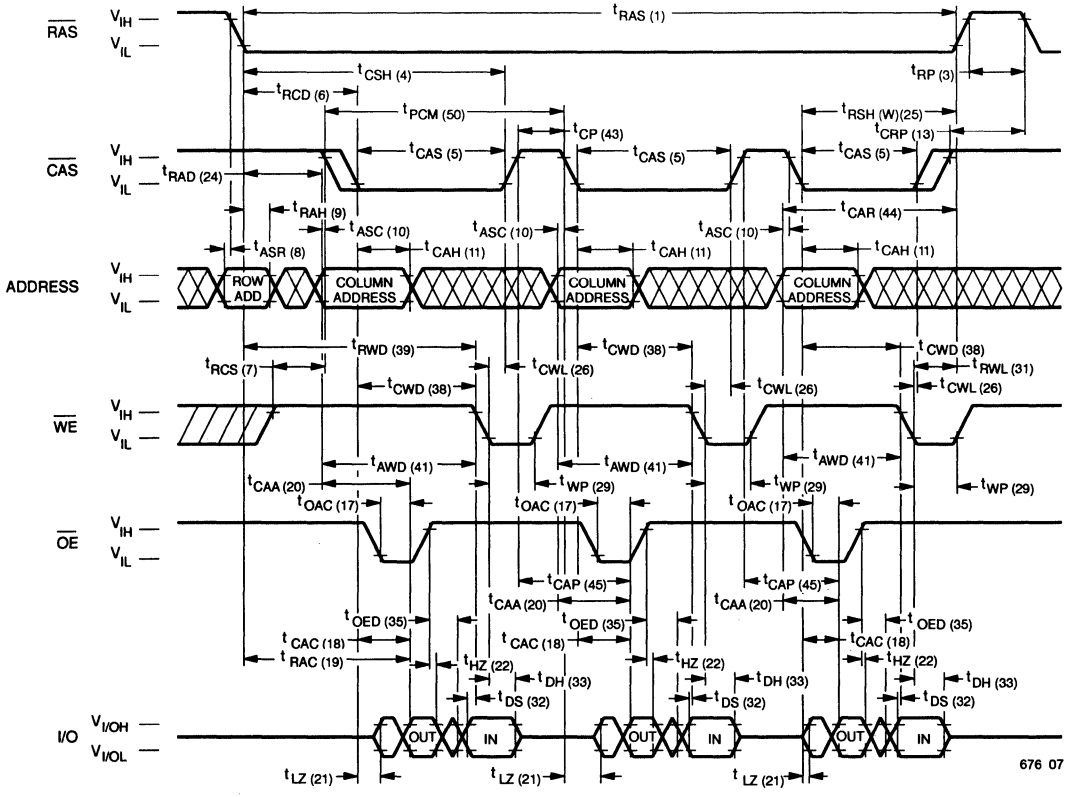
Waveforms of Fast Page Mode Read Cycle



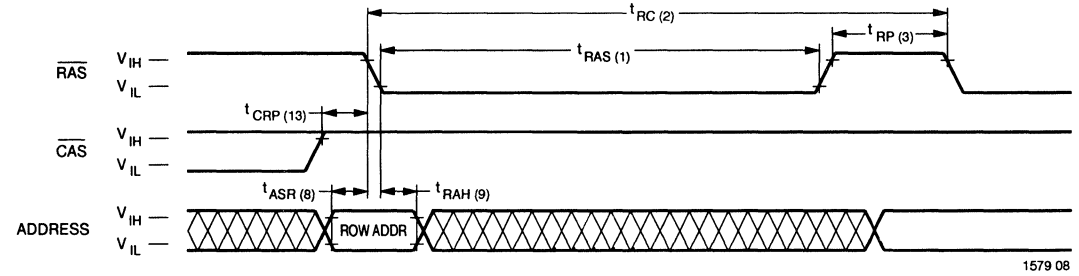
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Write Cycle

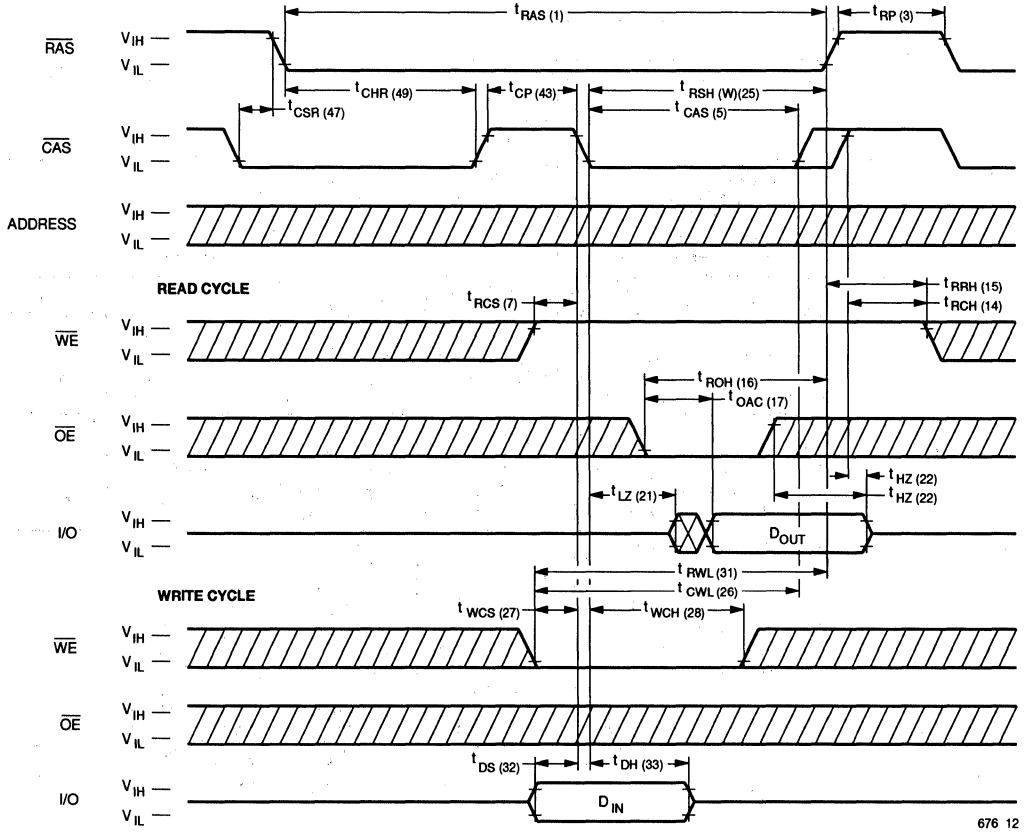


Waveforms of RAS-Only Refresh Cycle

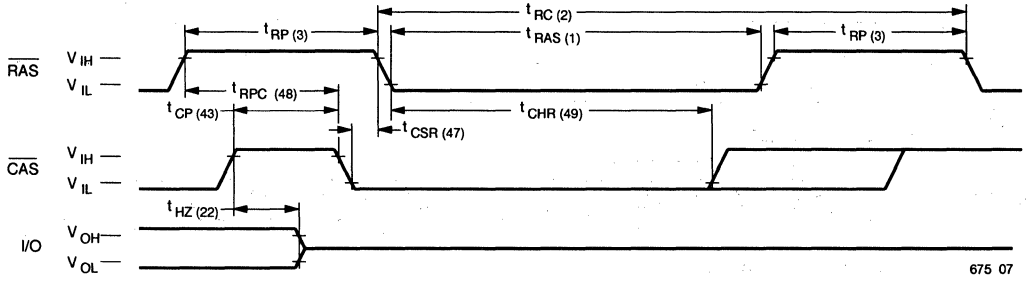


NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

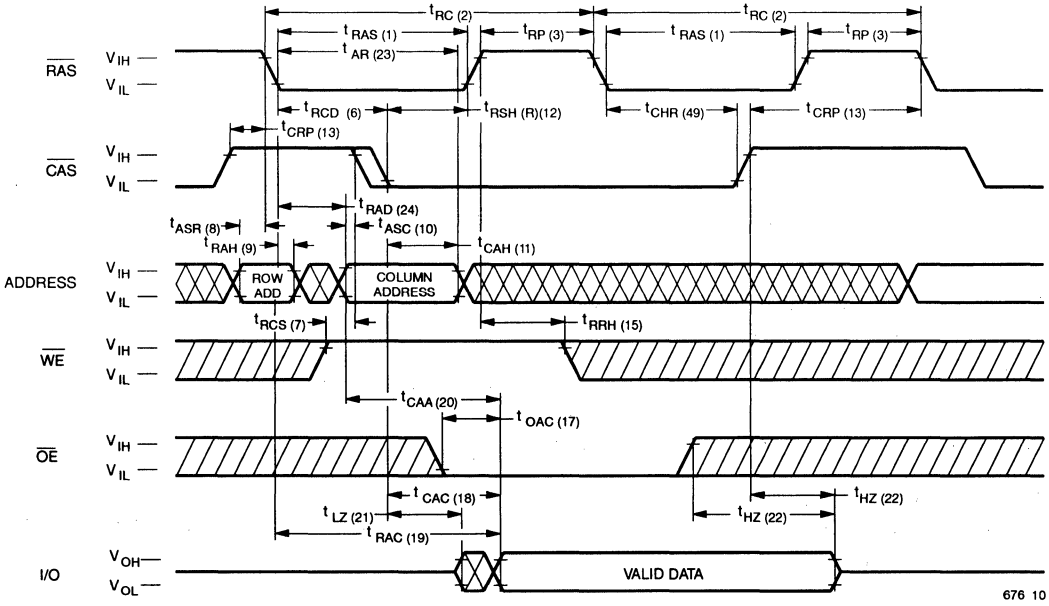


Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

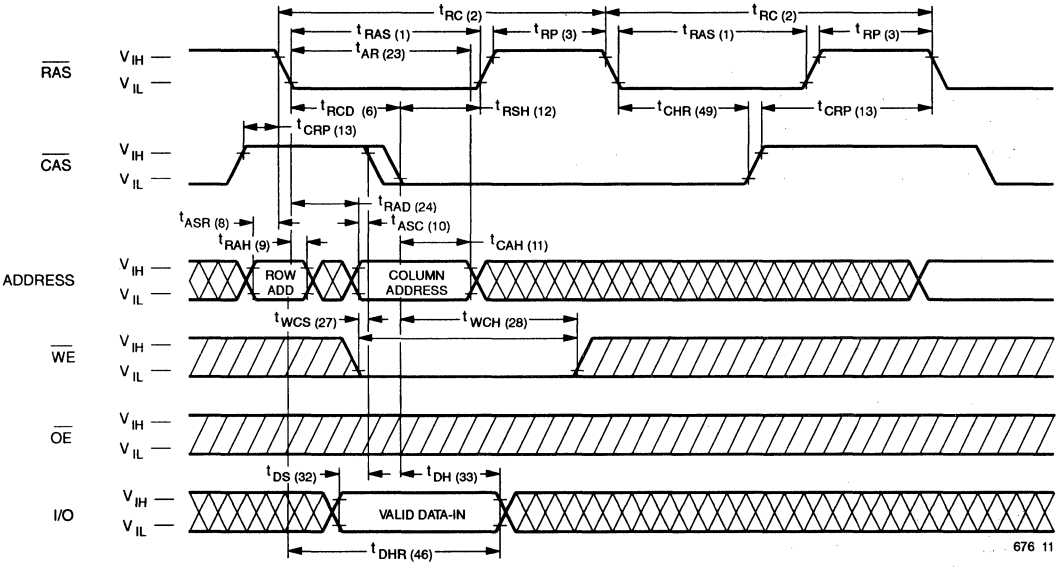


NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_7 = Don't care

Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Functional Description

The V53C104H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C104H reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C104H uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C104H offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C104H power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 40 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Data Output Operation

The V53C104H Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C104H is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C104H Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

V53C104N
HIGH PERFORMANCE, 3.3 VOLT 256K X 4 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C104N	60/60L	70/70L	80/80L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	45 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns

LOW POWER V53C104NL	60L	70L	80L
Max. CMOS Standby Current, (I_{DD6})	40 µA	40 µA	40 µA

Features

- 256K x 4 Organization
- $\overline{RAS}$ access time: 60,70,80 ns
- Low power dissipation for V53C104N-80
  - Operating Current – 35 mA max.
  - TTL Standby Current – 1.0 mA max.
- Low CMOS Standby Current
  - V53C104N – 400 µA max.
  - V53C104NL – 40 µA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability.
- Common I/O capability
- Refresh Interval
  - V53C104N – 512 cycles/8ms
  - V53C104NL – 512 cycles/64ms
- On-chip substrate bias generator
- Fast Page Mode for a sustained data rate greater than 25 MHz
- Standard packages are 20 pin Plastic DIP and 26/20 pin SOJ
- Low Battery Back-up Current
  - V53C104NL – 150 µA max.

Description

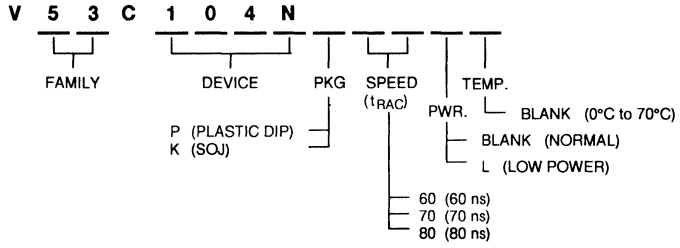
The V53C104N is a high speed 262,144 x 4 bit CMOS dynamic random access memory. Fabricated with Mosel-Vitelic's VICMOS IV technology, the V53C104N offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C104NL).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x4) bits within a row with cycle times as short as 45 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C104N ideally suited for graphics, digital signal processing and high performance computing systems.

The V53C104NL offers a maximum data retention power of 1.65 mW when operating in CMOS standby mode and performing $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

Device Usage Chart

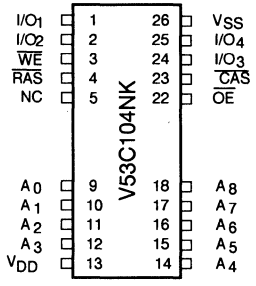
Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	60	70	80	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank



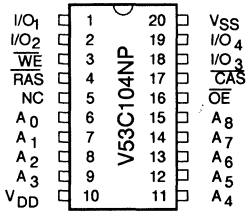
Description	Pkg.	Pin Count
Plastic DIP	P	20
SOJ	K	26/20

2

26/20 Lead SOJ Package PIN CONFIGURATION Top View



20 Lead Plastic DIP PIN CONFIGURATION Top View



Pin Names

A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_4	Data Input, Output
V_{DD}	+3.3V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 V to +6.0 V
Voltage on V_{DD} relative to V_{SS} ..... –0.5 V to +6.0 V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

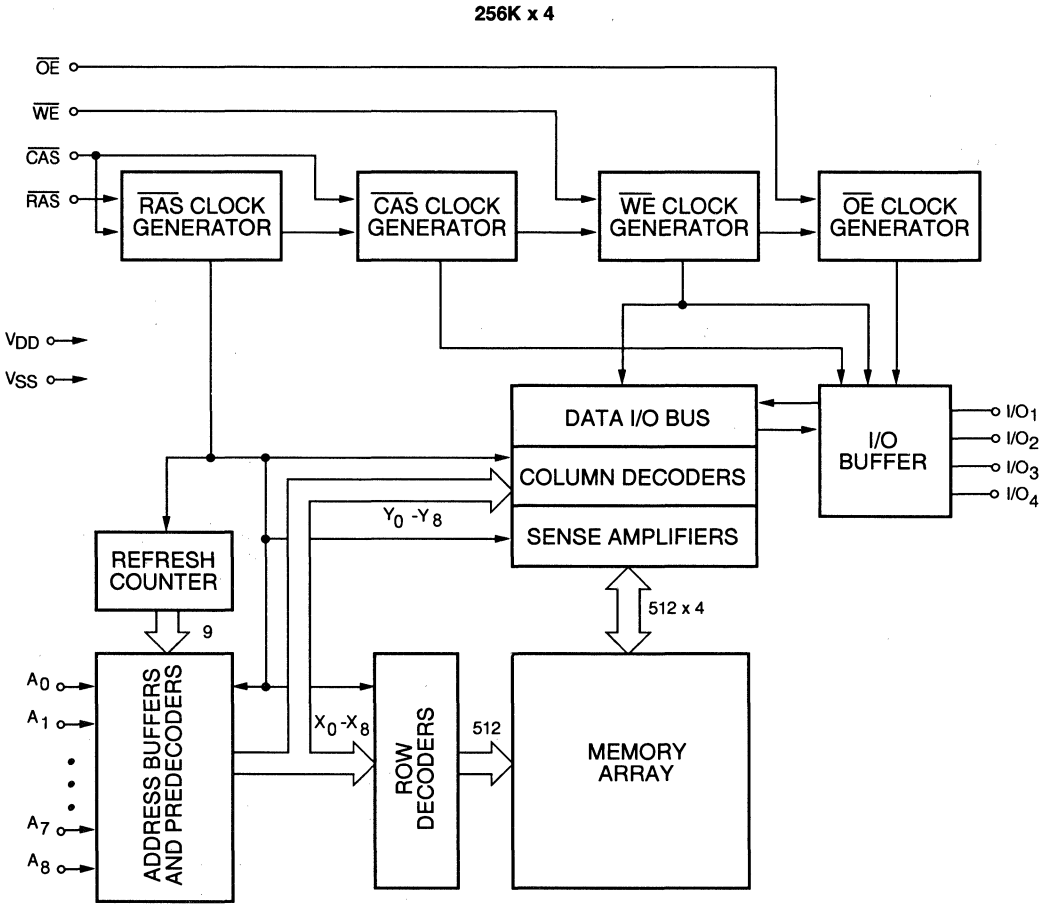
Capacitance*

T_A = 25°C, V_{DD} = 3.3 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 3.3 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C104N		V53C104NL		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10	10	–10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10	10	–10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60		45		45	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		70		40		40			
		80		35		35			
I_{DD2}	V_{DD} Supply Current, TTL Standby			1.0		1.0	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60		45		45	mA	$t_{RC} = t_{RC}$ (min.)	2
		70		40		40			
		80		35		35			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60		50		50	mA	Minimum Cycle	1, 2
		70		40		40			
		80		35		35			
I_{DD5}	Standby, Output Enabled			2.0		1.0	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current CMOS Standby			400		40	µA	$\overline{RAS}$ ≥ V_{DD} –0.2 V, $\overline{CAS}$ ≥ V_{DD} -0.2 V other input ≥ V_{SS}	
I_{DD7}*	Battery Back-up Data Retention Current (V53C104NL only)			N.A.		0.15	µA	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle t_{RC} = 125 µs CMOS Clock Levels	1, 18
V_{IL}	Input Low Voltage		–0.5	0.6	–0.5	0.6	V		3
V_{IL}	Input High Voltage		2.4	V_{DD}+0.5	2.4	V_{DD}+0.5	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 3 mA	
V_{OH}	Output High Voltage		2.4		2.4			I_{OH} = -3 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 3.3V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	120		130		150		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		25		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	40	25	45	25	55	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		25		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		10		10		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		20		25		25	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		25		25	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		45	ns	6,7, 10

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	20	0	20	0	20	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	25	20	30	20	35	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		25		25		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		25		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		15		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		15		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		25		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		15		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	15		15		15		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	15		20		20		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	180		195		215		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	115		135		145		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	45		55		55		ns	12

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	85		100		110		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	75		85		85		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	65		70		75		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		30		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95		105		110		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{REF}	Refresh Interval (512 Cycles)		8		8		8	ms	17
		t_{REF}	Refresh Interval V53C104NL Only (512 Refresh cycles, t_{RC}=125 µs)		64		64		64	ms	17,18

Notes

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to −1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$ before $\overline{RAS}$ refresh cycles.

    t_{RC} = 125 µs (125 µs x 512 = 64 ms)

    $t_{RAS} = t_{RAS}$ (min) to 1 µs

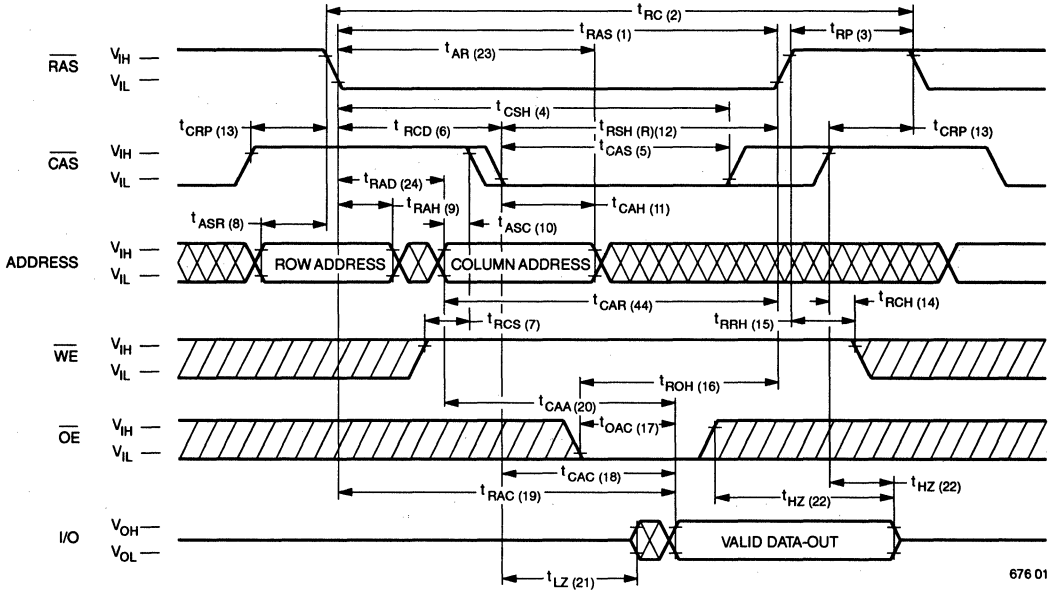
    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V

    $V_{IL} < 0.2$ V

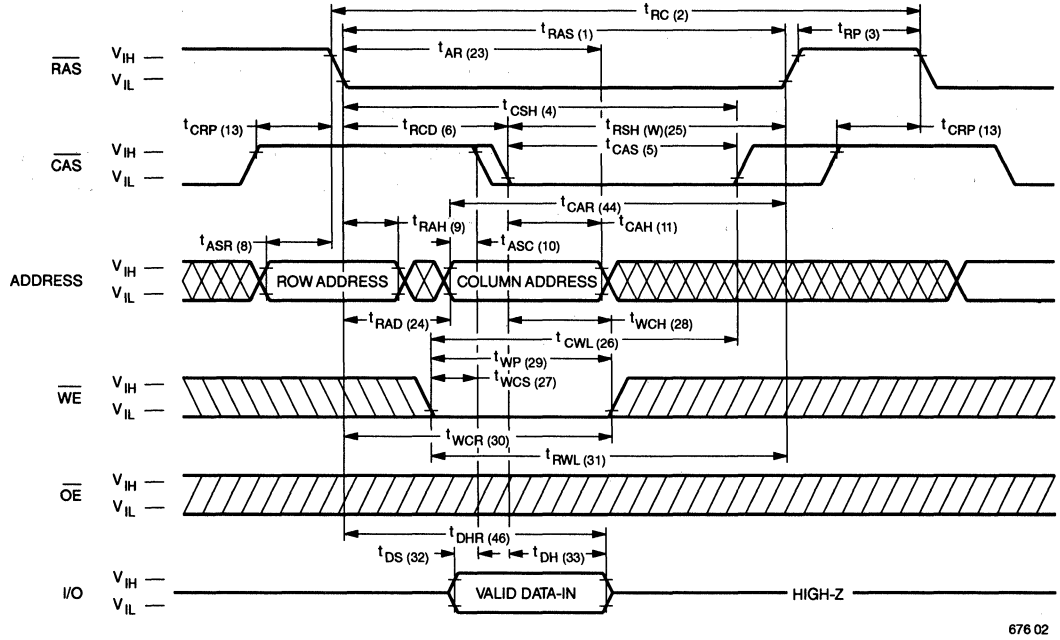
    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V

    All other inputs at stable V_{IH} or V_{IL}

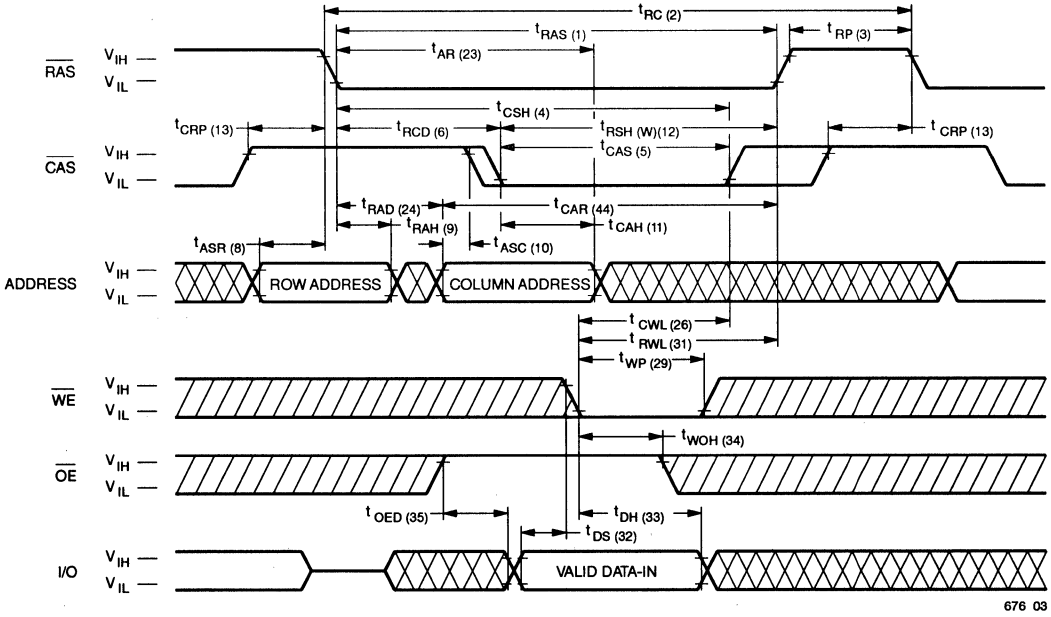
Waveforms of Read Cycle



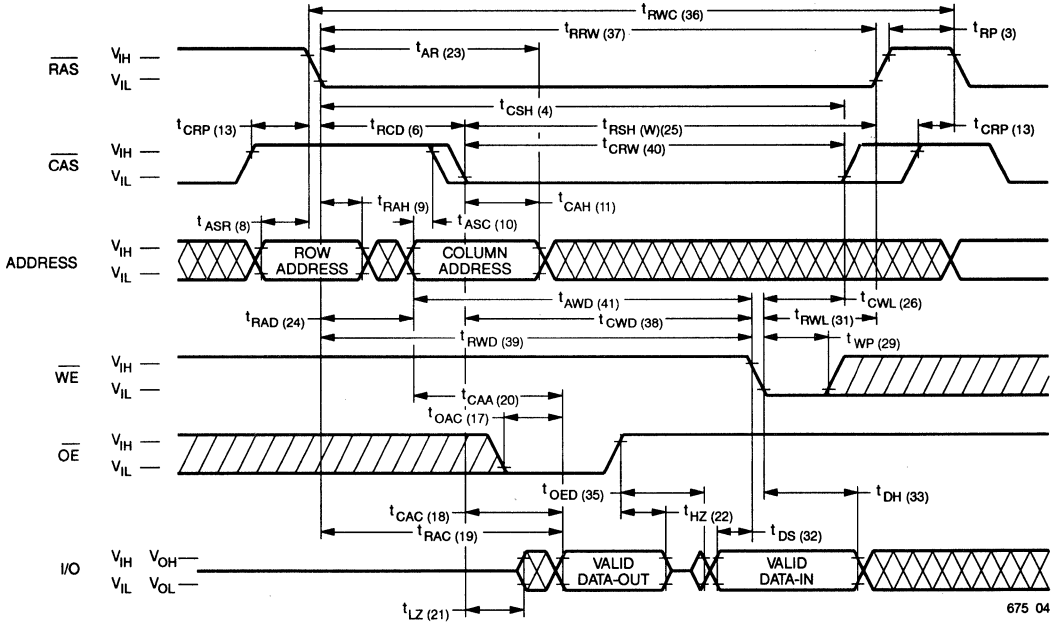
Waveforms of Early Write Cycle



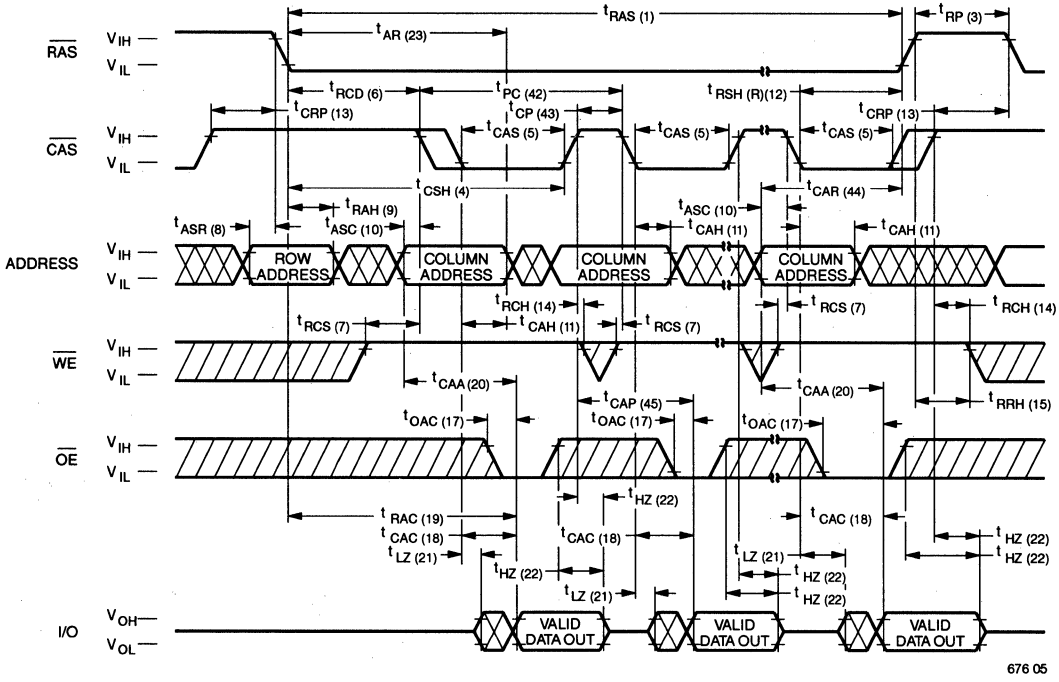
Waveforms of $\overline{OE}$-Controlled Write Cycle



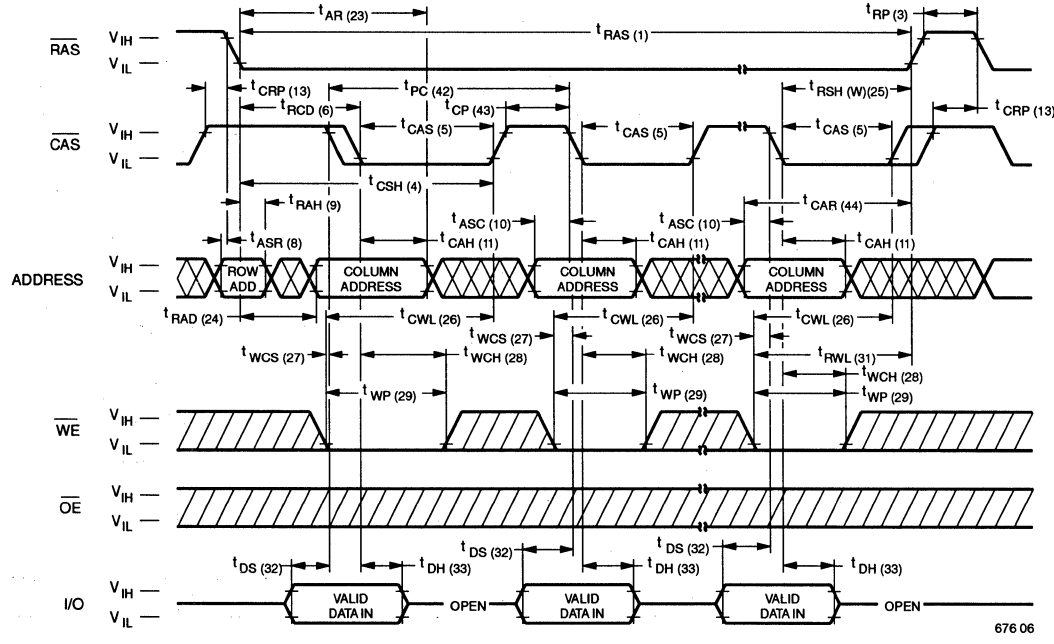
Waveforms of Read-Modify-Write Cycle



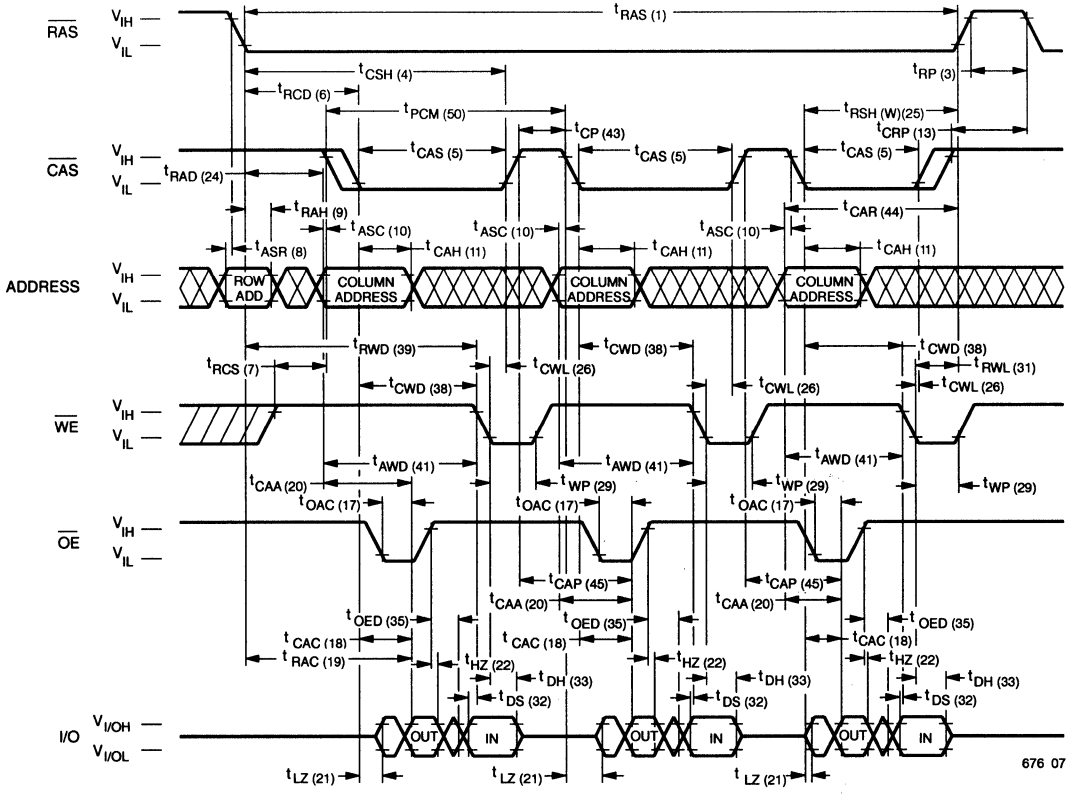
Waveforms of Fast Page Mode Read Cycle



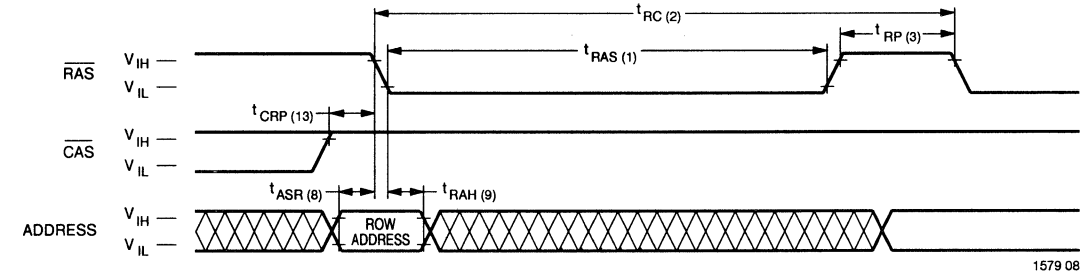
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Write Cycle

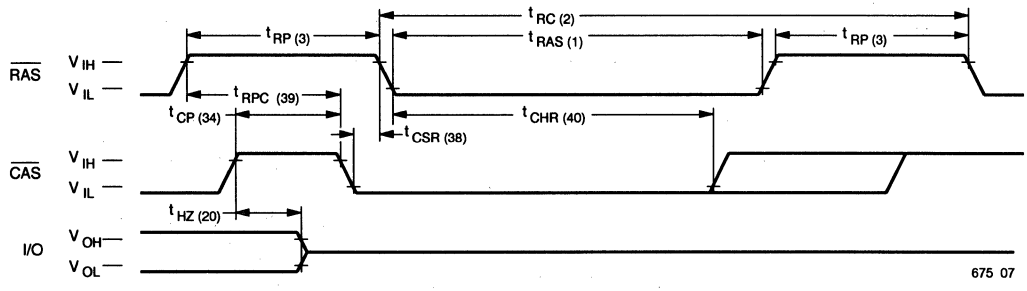


Waveforms of $\overline{RAS}$-Only Refresh Cycle



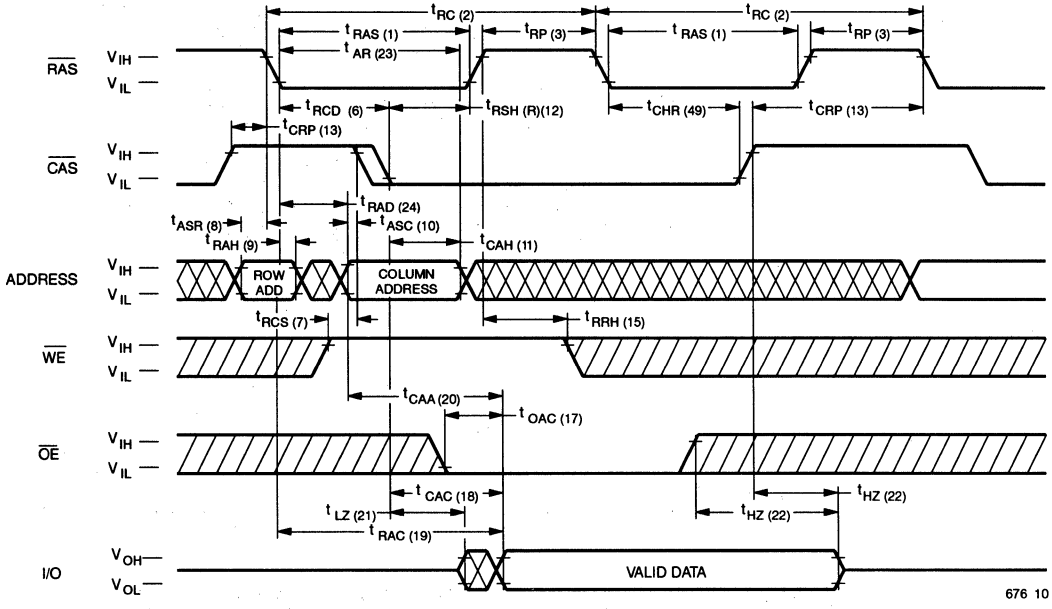
NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

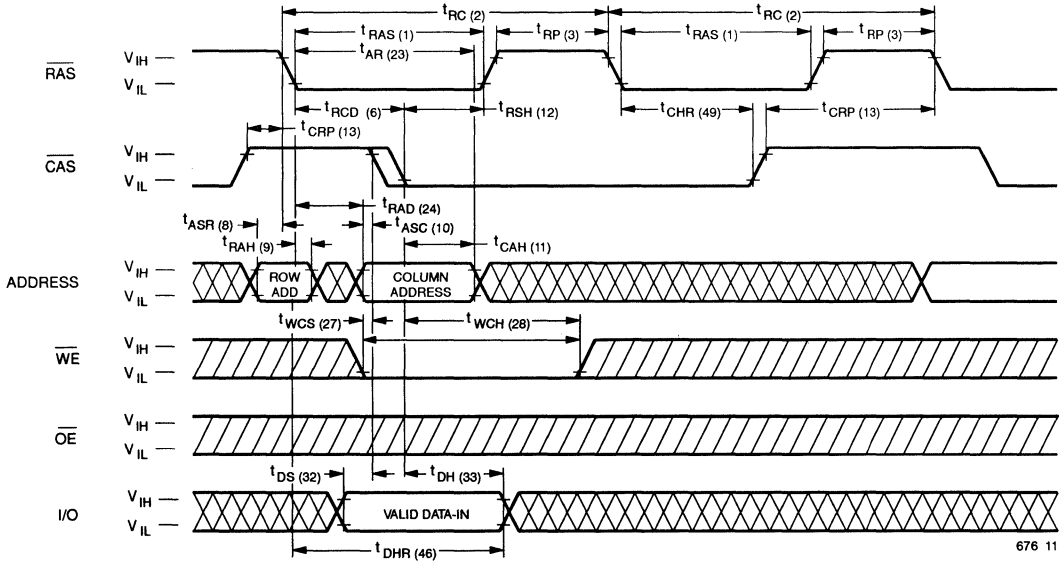


NOTE: $\overline{WE}$, A_0–A_8 = Don't care

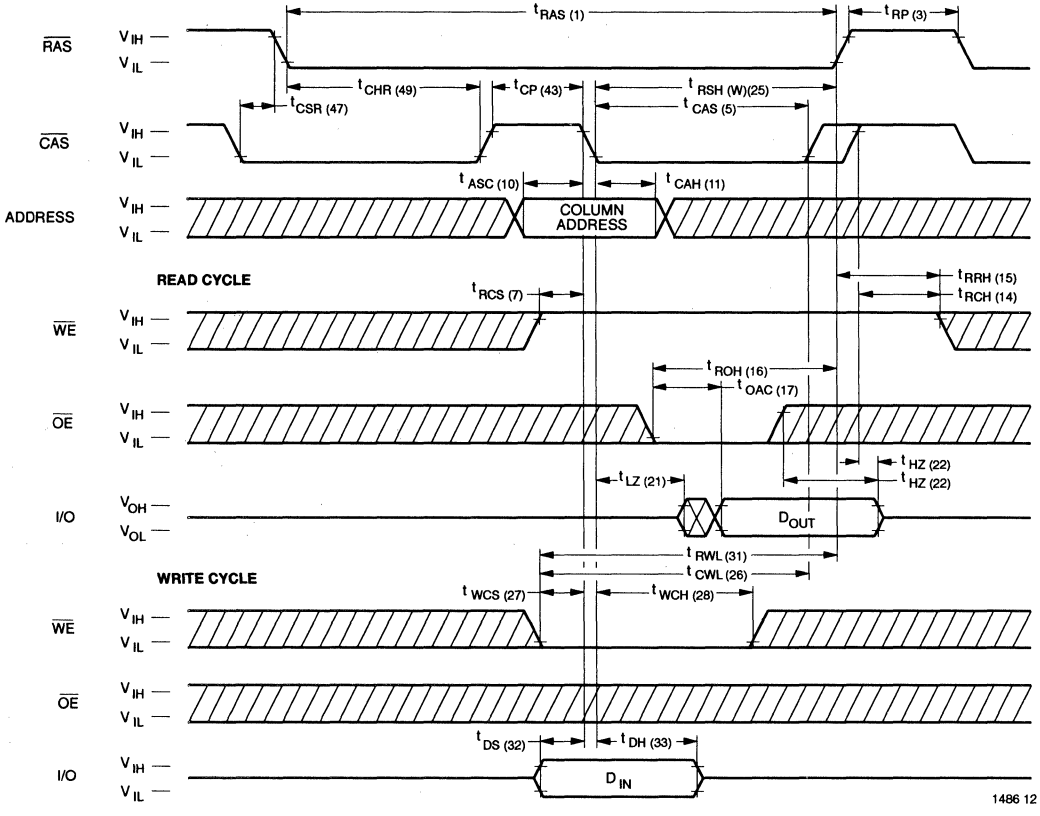
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C104N is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C104N reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C104N uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C104N offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C104N power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 25 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Data Output Operation

The V53C104N Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C104N is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C104N Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

V53C664	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	45 ns	55 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	55 ns	65 ns
Min. Read/Write Cycle Time, (t_{RC})	135 ns	170 ns

LOW POWER V53C664L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	200µA	200 µA

Features

- 64K by 16-bit organization
- $\overline{RAS}$ Access time: 80, 100 ns
- Low power dissipation
  - V53C664K10
    - — Operating Current – 90 mA max.
    - — TTL Standby Current – 2 mA max.
- Low CMOS Standby Current
  - V53C664 – 1.0 mA max.
  - V53C664L – 0.2 mA max.
- Low Battery Back-up Current
  - V53C664L – 300 µA max.
  - 200 µA with 64ms refresh interval available on request
- Fast Page, Byte-Write, Read-Modify-Write, $\overline{CAS}$ before $\overline{RAS}$ refresh, and $\overline{RAS}$-only refresh capability
- Refresh Interval
  - V53C664 – 256 cycles/4ms
  - V53C664L – 256 cycles/32ms
- Available in 40 Pin Plastic SOJ package

Description

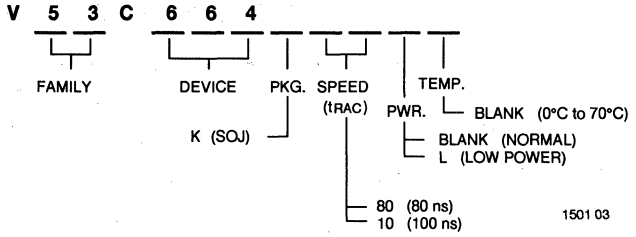
The V53C664 is a new generation, 65,536 word x 16 bit CMOS dynamic RAM fabricated with VICMOS III technology. The 16-bit wide organization makes the V53C664 ideal for high bandwidth applications such as imaging and graphics. In addition, the version with very low standby current, V53C664L, is extremely suitable for portable applications such as laptop and notebook personal computers.

The V53C664 supports Fast Page Mode operation for high data bandwidth. Fast Page Mode allows 256 random accesses within a single row with access cycle times as short as 55 ns per 16-bit word. The addition of Byte Write control, of upper and lower byte, makes the V53C664 ideal for use in 16-, 32-bit wide data bus systems.

Mulitplexed address inputs and common input/output permit the V53C664 to be packaged in a standard 40 pin plastic SOJ to provide high system bit densities.

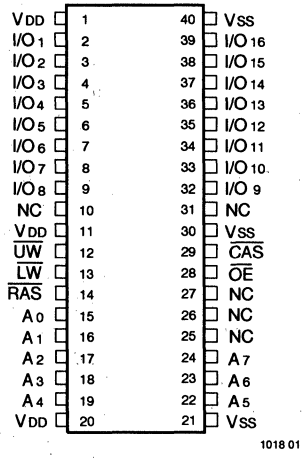
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)		Power		Temperature Mark
	K	80	100	Low	Std.	
0°C to 70°C	•	•	•	•	•	Blank



Description	*Pkg.*	*Pin Count*
Plastic SOJ	K	40

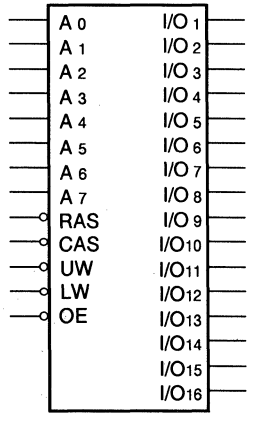
40-Pin Plastic SOJ
PIN CONFIGURATION
Top View



Pin Names

Symbol	Name
A0 – A7	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{UW}$	Read/Upper Byte Write Input
$\overline{LW}$	Read/Lower Byte Write Input
$\overline{OE}$	Output Enable
I/O1 – I/O16	Data Input/Output
V_{DD}	Power (+ 5V)
V_{SS}	Ground
NC	No Connection

Logic Symbol



Absolute Maximum Ratings*

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage Relative to V_{SS} .....–1.0 to +7.0 V
Data Out Current .....50 mA
Power Dissipation .....1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

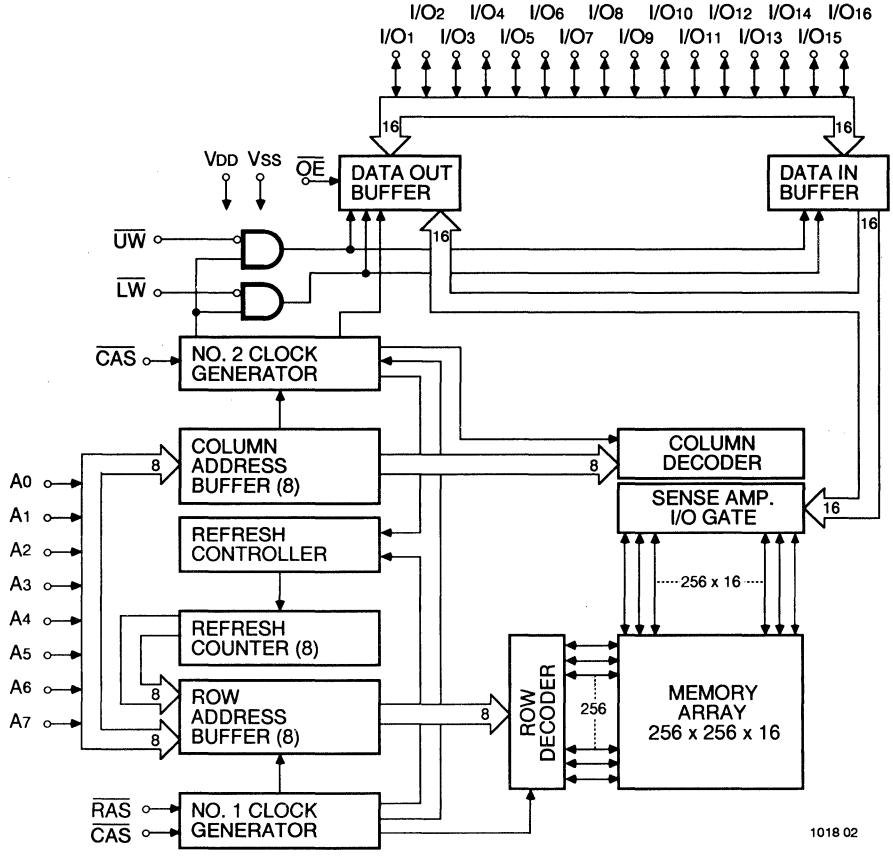
V_{DD} = 5V ± 10%, V_{SS} = 0V

Symbol	Parameter	Min.	Max.	Unit
C_{IN1}	Input Capacitance (A0 – A7)	3	4	pF
C_{IN2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$)	4	5	pF
C_{OUT}	Output Capacitance (I/O1 – I/O16)	5	7	pF

*NOTE: Capacitance is sampled and not 100% tested

2

Block Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C664			V53C664L			Unit	Test Conditions	Notes
			Min.	Typ.	Max.	Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10		10	−10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10		10	−10		10	µA	$V_{SS} \le D_{OUT} \le V_{DD}$ $\overline{RAS},\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	80			115			115	mA	$t_{RC} = t_{RC}$ (min.)	1,2
		100			90			90			
I_{DD2}	V_{DD} Supply Current, TTL Standby				2.0			2.0	mA	$\overline{RAS},\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	80			115			115	mA	$t_{RC} = t_{RC}$ (min.)	2
		100			90			90			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	80			100			100	mA	Minimum Cycle	1,2
		100			90			90			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled				5.0			5.0	mA	$\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IL}$ other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby				1.0			0.2	mA	$\overline{RAS} \ge V_{DD}-0.2$ V, $\overline{CAS} \ge V_{DD} - 0.2$V, other inputs ≥ V_{SS}	
I_{DD7}*	Battery Backup Data Retention Current (only "L" Version)				N.A.			0.3*	mA	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycles t_{RC} = 125 µs CMOS clock levels	18
V_{IL}	Input Low Voltage		−1		0.8	−1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{DD} +1	2.4		V_{DD} +1	V		3
V_{OL}	Output Low Voltage				0.4			0.4	V	I_{OL} = -2.5 mA	
V_{OH}	Output High Voltage		2.4			2.4			V	I_{OH} = 2.1 mA	

*I_{DD7} = 0.2 mA max. with t_{RC} = 250µs (64ms refresh interval) available on request.

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5V ± 10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3 V

#	JEDEC Symbol	Symbol	Parameter	80		100		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	135	—	170	—	ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	45	—	60	—	ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	80	—	100	—	ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	30	10K	35	10K	ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	65	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
12	$t_{CL1RH1(R)}$	t_{RSHr}	$\overline{RAS}$ Hold Time (Read Cycle)	30	—	35	—	ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time referenced to $\overline{CAS}$	0	—	0	—	ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0	—	0	—	ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10	—	10	—	ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$	—	25	—	30	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$	—	30	—	35	ns	6, 7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$	—	80	—	100	ns	6, 8, 9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address	—	45	—	55	ns	6, 7, 10
21	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	25	0	25	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55	—	65	—	ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	45	ns	11
25	$t_{CL1RH1(W)}$	t_{RSHw}	RAS or CAS Hold Time in Write Cycle	30	—	35	—	ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20	—	20	—	ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Set-Up Time	0	—	0	—	ns	12, 13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	15	—	15	—	ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55	—	65	—	ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20	—	20	—	ns	

AC Characteristics (continued)

#	JEDEC Symbol	Symbol	Parameter	80		100		Unit	Notes
				Min.	Max.	Min.	Max.		
32	t_{DVWL2}	t_{DS}	Data-In Set-Up Time	0	—	0	—	ns	14
33	t_{WL1DX}	t_{DH}	Data-In Hold Time	15	—	15	—	ns	14
34	t_{WL1GL2}	t_{WOH}	$\overline{OE}$ Hold Time	10		10		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	10	—	20	—	ns	
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	175	—	220	—	ns	
37	t_{RL2RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	120	—	150	—	ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	50	—	65	—	ns	12
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time in Read-Modify-Write Cycle	100	—	130	—	ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	80	—	95	—	ns	
41	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	65	—	85	—	ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	55	—	65	—	ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	45	—	55	—	ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge	—	50	—	60	ns	7
46	t_{RL1DX}	t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55	—	65	—	ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	5	—	5	—	ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	10	—	10	—	ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	100	—	120	—	ns	
51	t_{WH2CL2}	t_{MCS}	Byte-Masked Write Setup Time	0		0		ns	
52	t_{RH2WL2}	t_{MRH}	Byte-Masked Write Hold Time Referenced to $\overline{RAS}$	0		0		ns	
53	t_{CH2WL2}	t_{MCH}	Byte-Masked Write Hold Time Referenced to $\overline{RAS}$	0		0		ns	
		t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	15
		t_{REF}	Refresh Interval (256 Cycles)	—	4	—	4	ms	17
		t_{REF}	Refresh Interval (256 Refresh Cycles, t_{RC} = 125 µs, V53C664L Only)	—	32	—	32	ms	17, 18

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in First Page Mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} (min.) may undershoot to −1.0 V for periods not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limits ensure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to one TTL loads and 50 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC}, or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{WHC}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the later occurance of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

    t_{RC} = 125 µs (125 µs x 256 = 32ms)

    $t_{RAS} = t_{RAS}$ (min) to 1µs

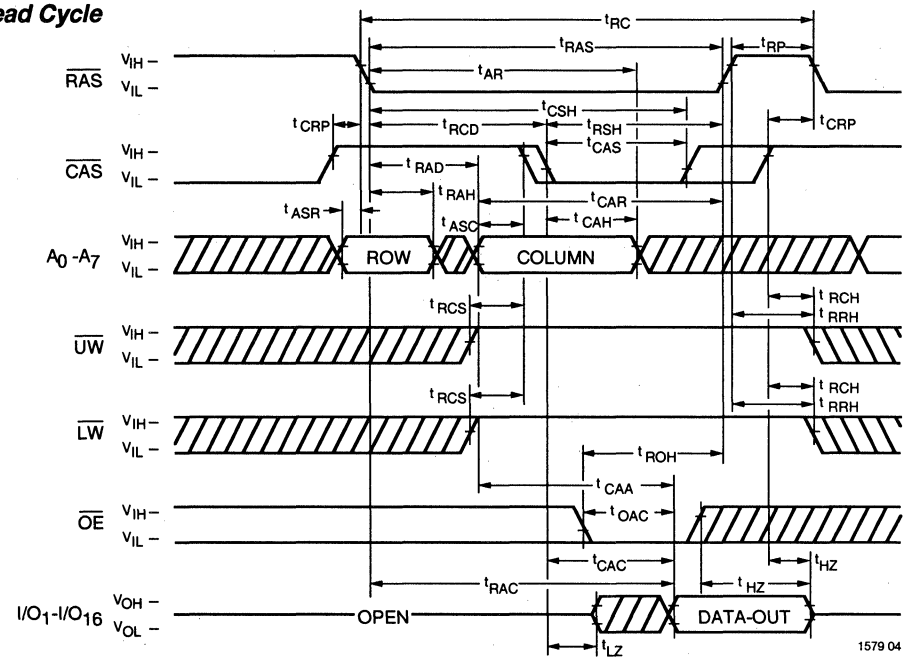
    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V

    $V_{IL} < 0.2$ V

    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V

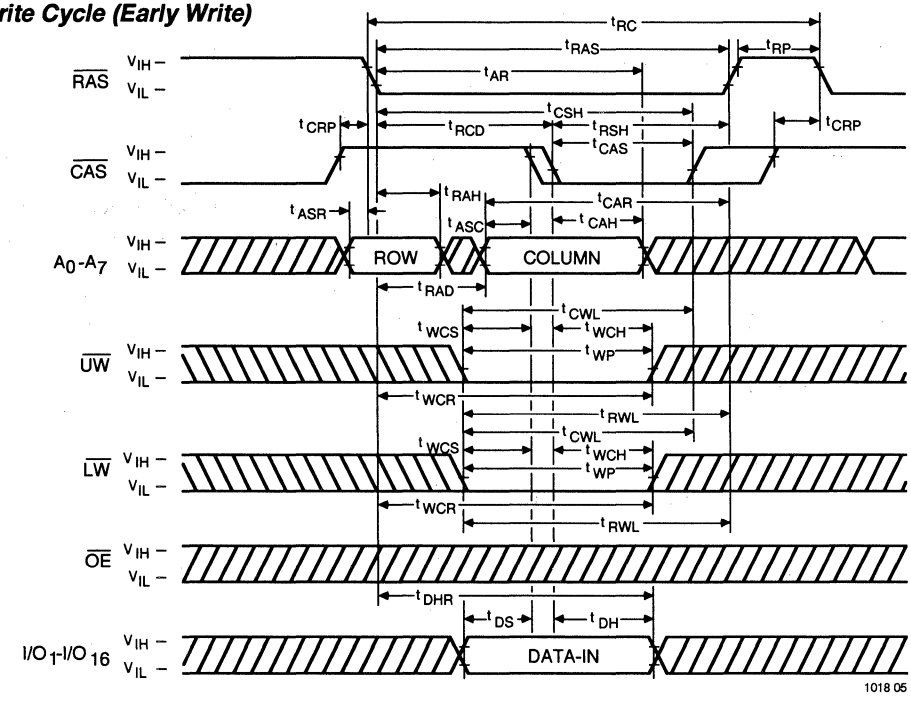
    All other inputs at stable V_{IH} or V_{IL}

Read Cycle



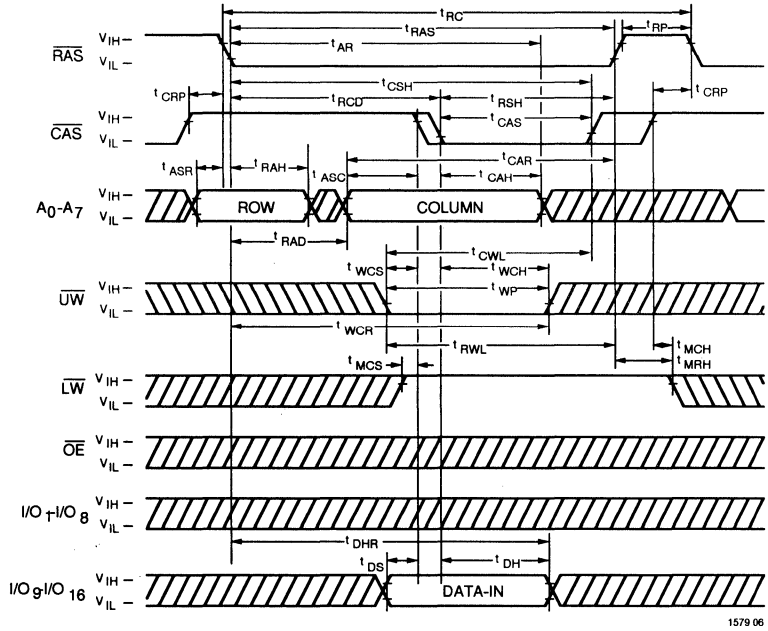
NOTE: D_{IN} = OPEN

Write Cycle (Early Write)



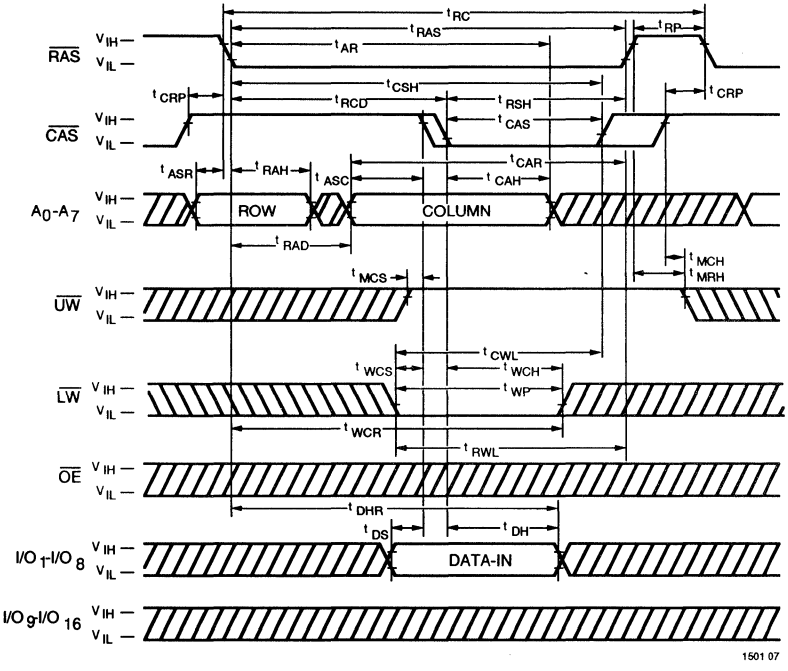
NOTE: D_{OUT} = OPEN

Upper Byte Write Cycle (Early Write)



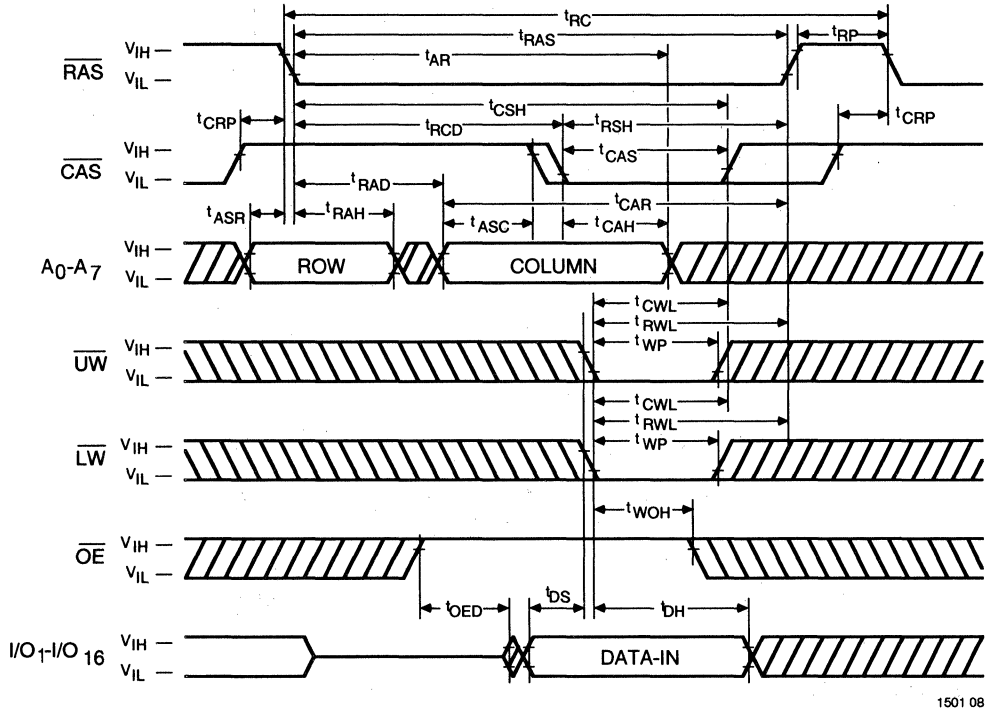
NOTE: D_{OUT} = OPEN

Lower Byte Write Cycle (Early Write)



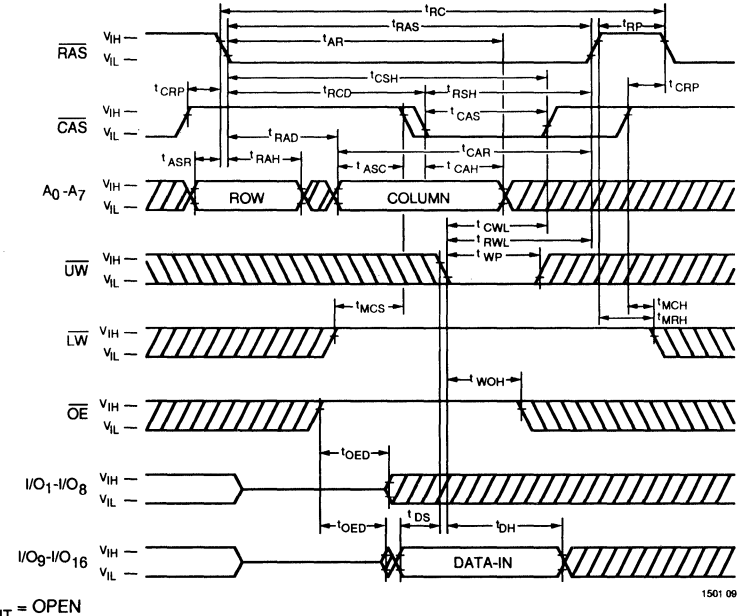
NOTE: D_{OUT} = OPEN

Write Cycle ($\overline{OE}$-Controlled Write)



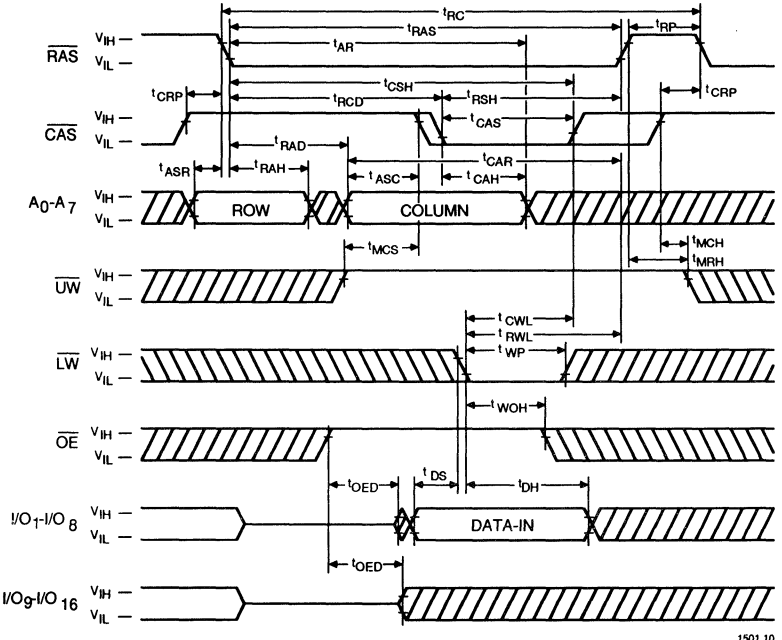
NOTE: D_{OUT} = OPEN

Upper Byte Write Cycle ($\overline{OE}$-Controlled Write)



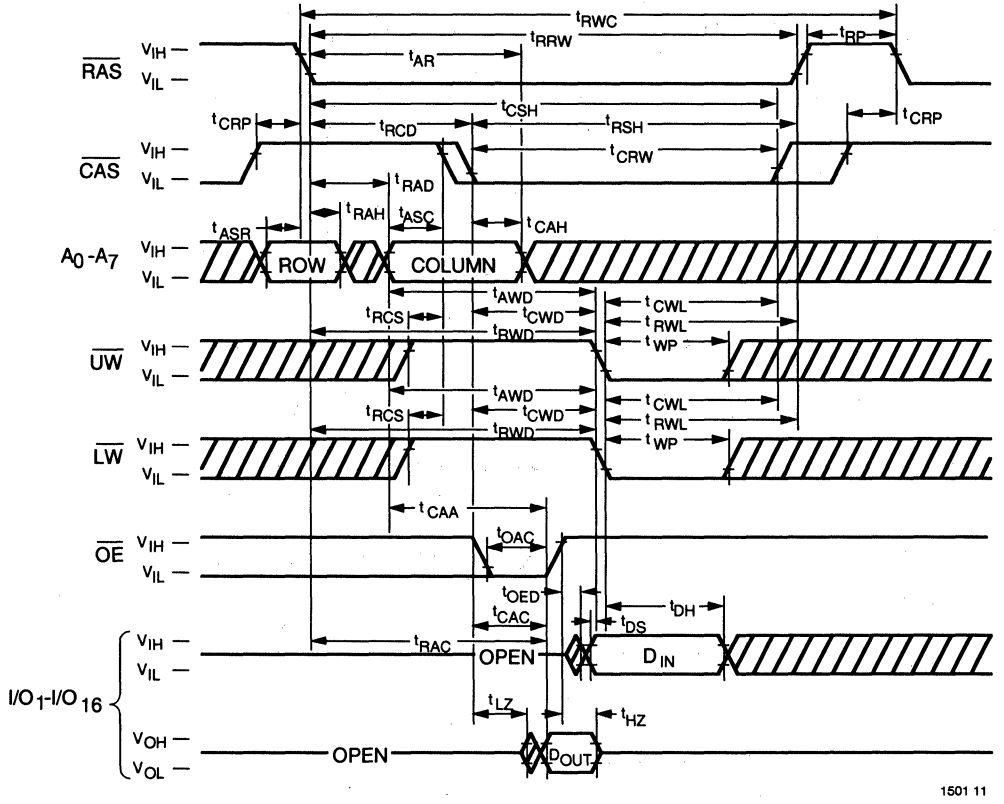
NOTE: D_{OUT} = OPEN

Lower Byte Write Cycle ($\overline{OE}$-Controlled Write)

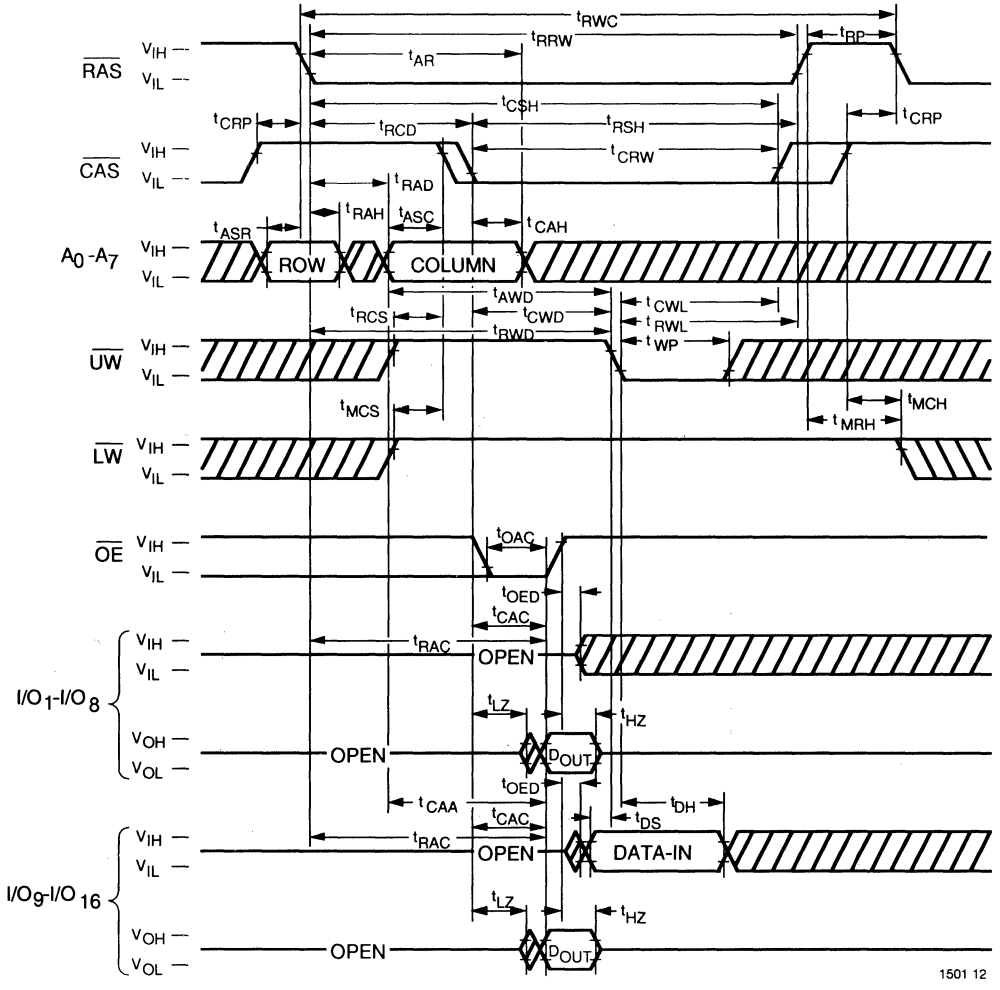


NOTE: D_{OUT} = OPEN

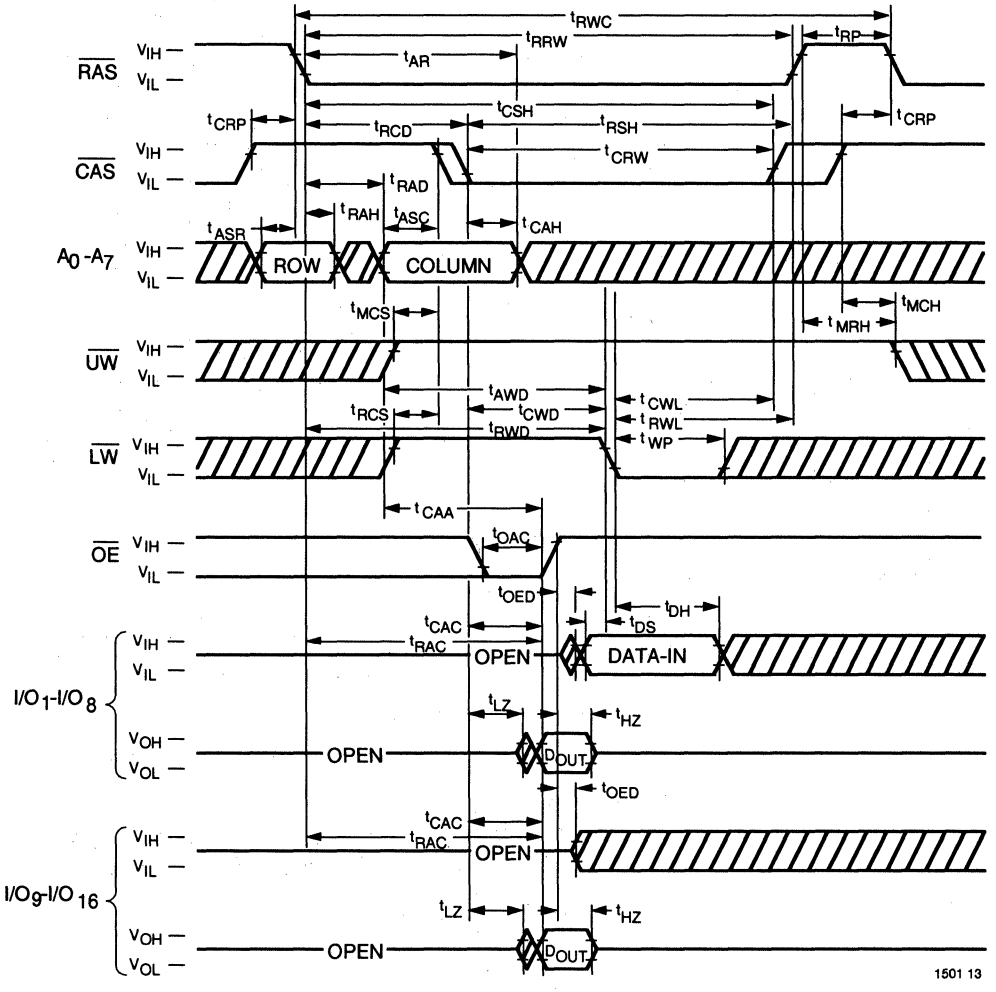
Read-Modify-Write Cycle



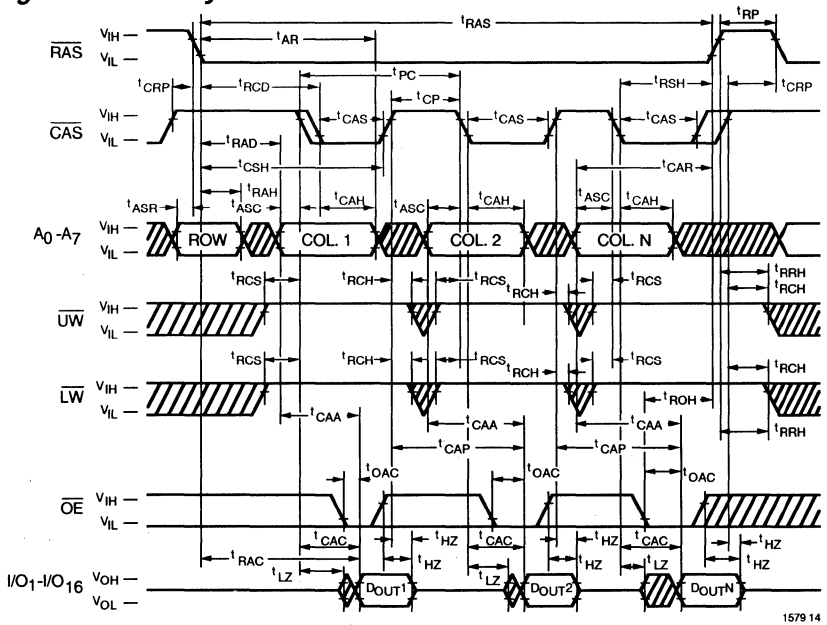
Read-Modify-Upper-Byte-Write Cycle



Read-Modify-Lower-Byte-Write Cycle

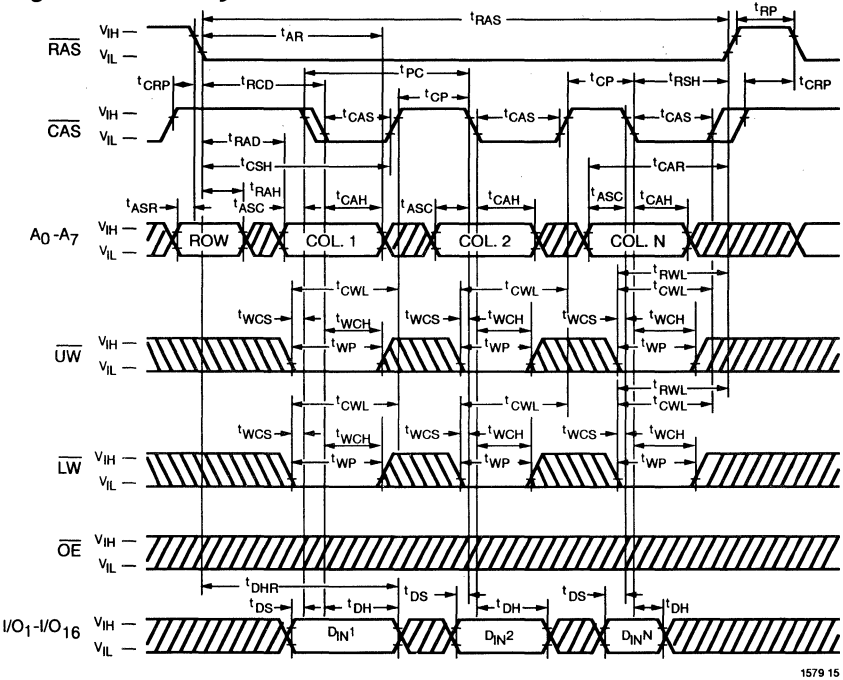


Fast Page Mode Read Cycle



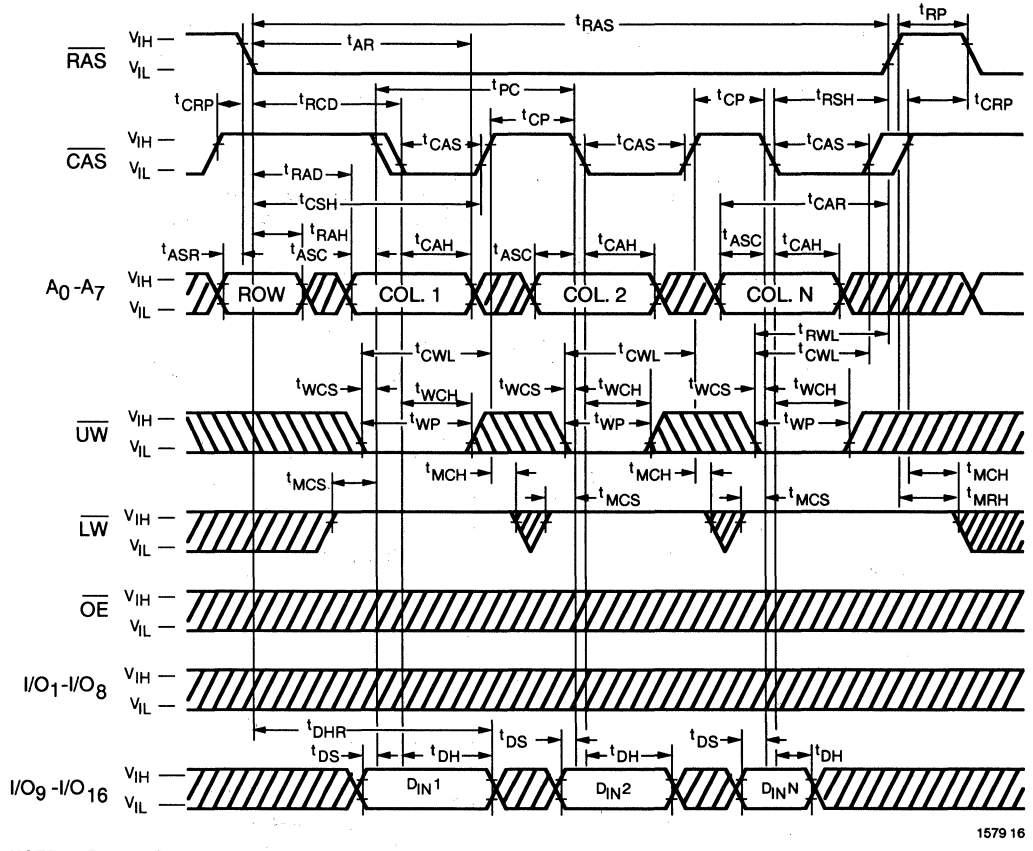
NOTE: D_{IN} = OPEN

Fast Page Mode Write Cycle



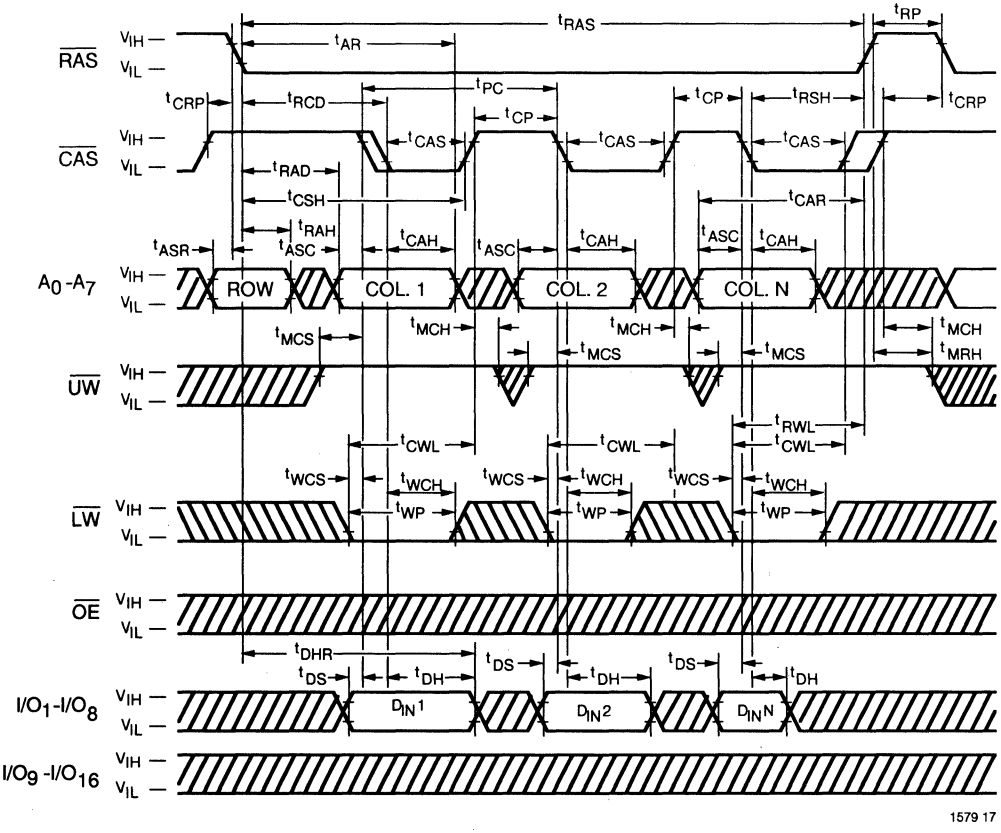
NOTE: D_{OUT} = OPEN

Fast Page Mode Upper Byte Write Cycle



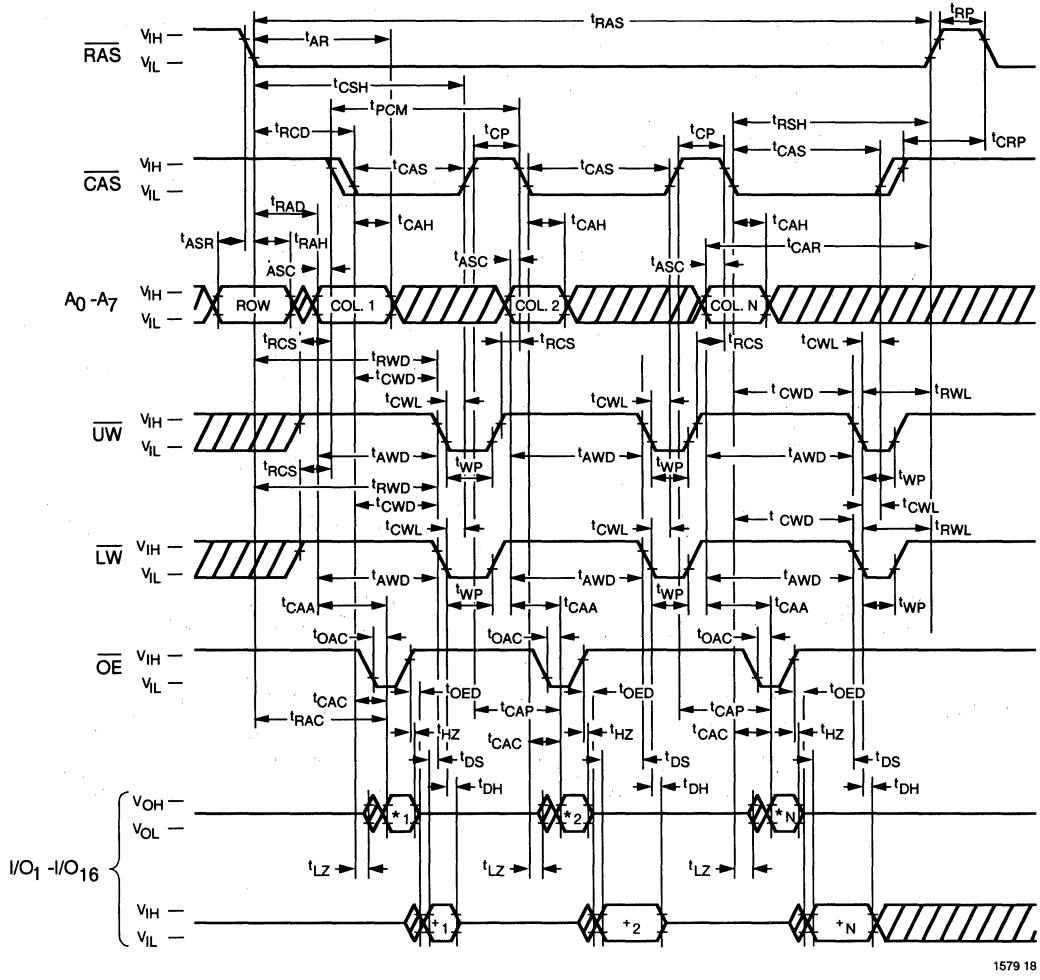
NOTE: D_{OUT} = OPEN

Fast Page Mode Lower Byte Write Cycle



NOTE: D_{OUT} = OPEN

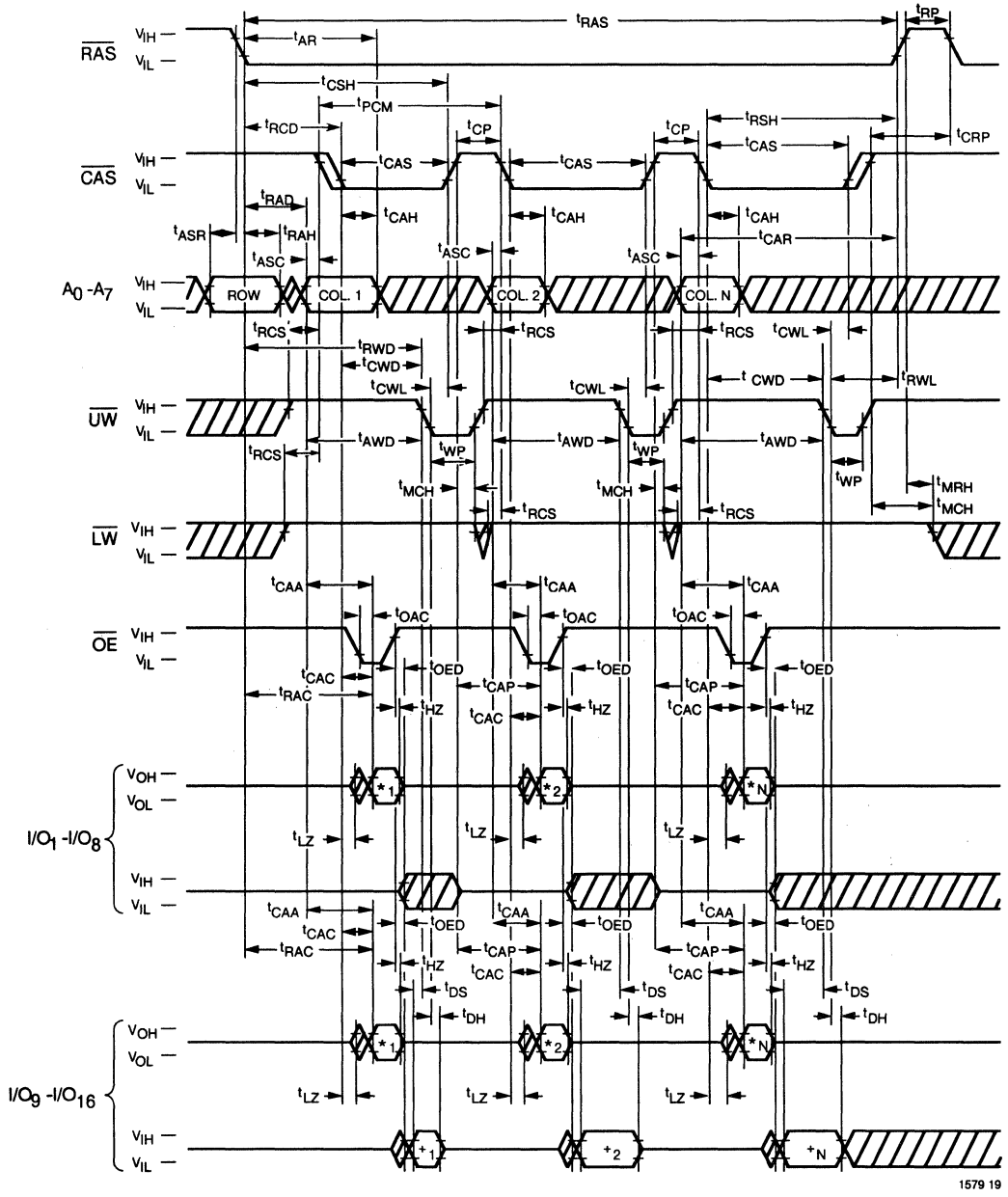
Fast Page Read-Modify-Write Cycle



1579 18

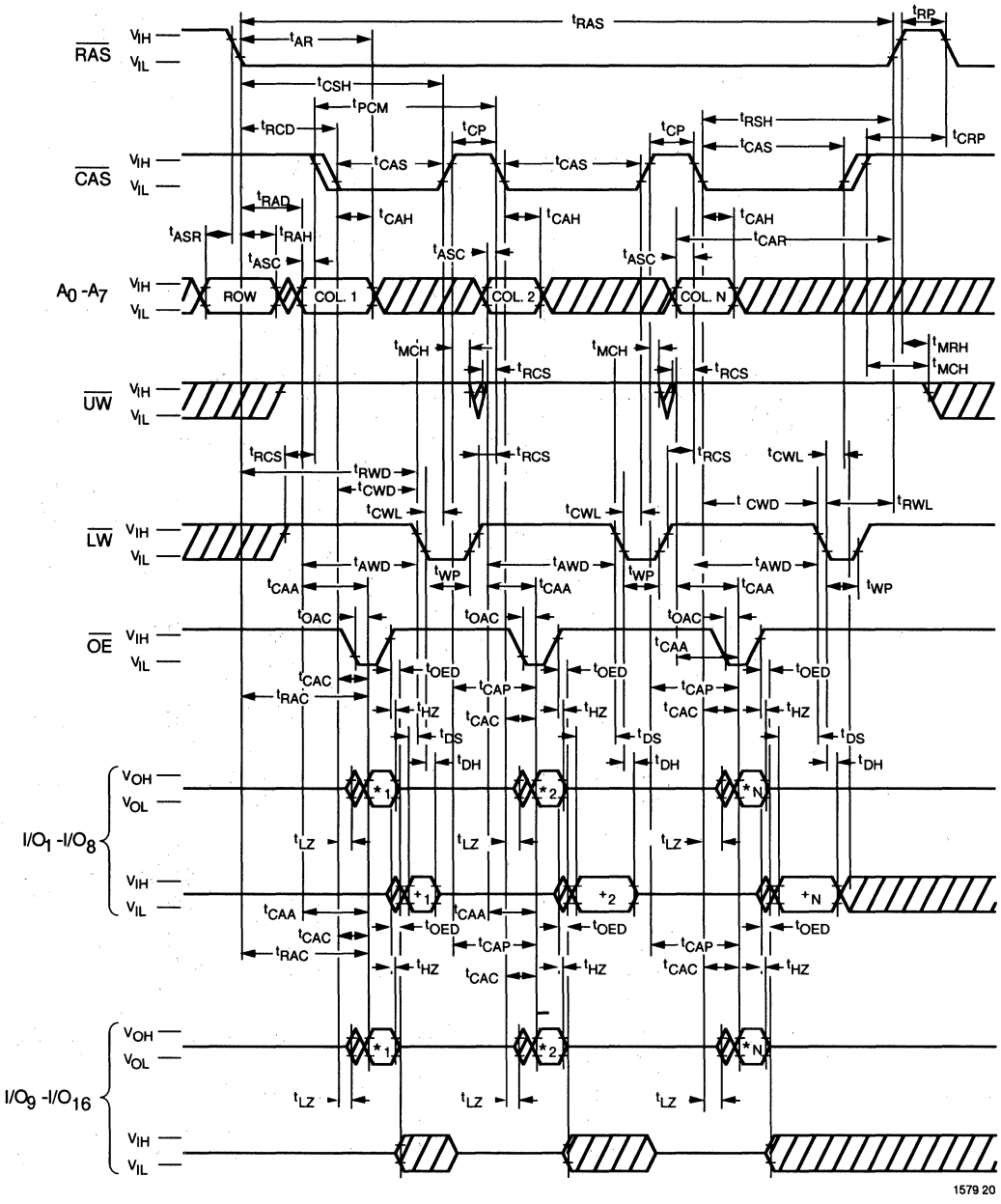
NOTE: * = D_{OUT}, + = D_{IN}

Fast Page Mode Read-Modify-Upper-Byte-Write Cycle



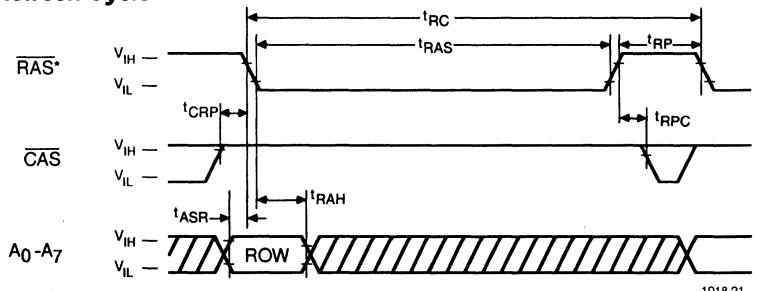
NOTE: * = D_{OUT}, + = D_{IN}

Fast Page Mode Read-Modify-Lower-Byte-Write Cycle



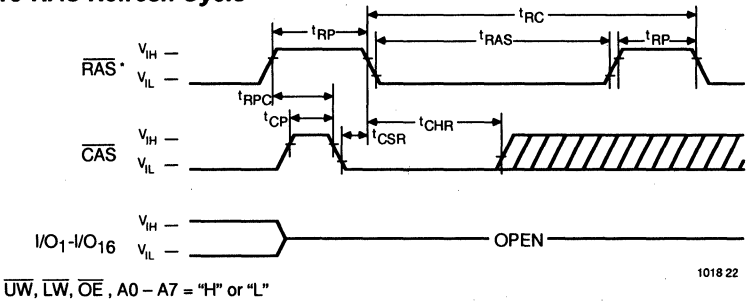
NOTE: * = D_{OUT}, + = D_{IN}

RAS-Only Refresh Cycle



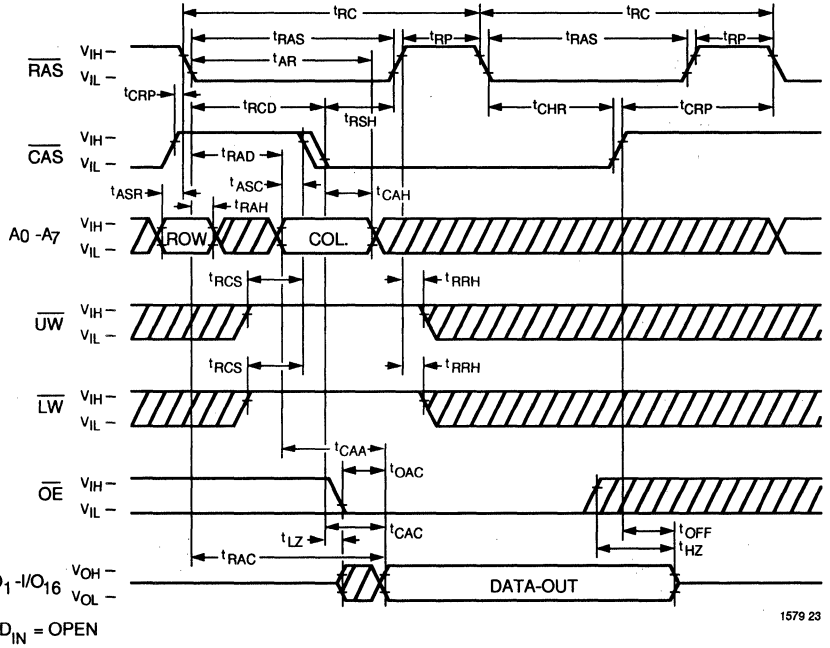
NOTE: $\overline{UW}$, $\overline{LW}$, $\overline{OE}$ = "H" or "L"

CAS-Before-RAS Refresh Cycle



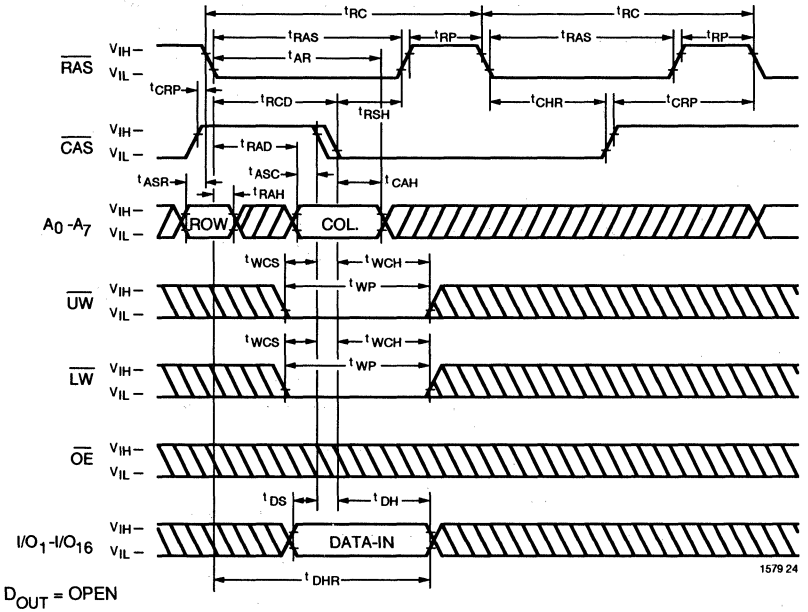
NOTE: D_{IN}, $\overline{UW}$, $\overline{LW}$, $\overline{OE}$, A0 – A7 = "H" or "L"

Hidden Refresh Cycle (Read)



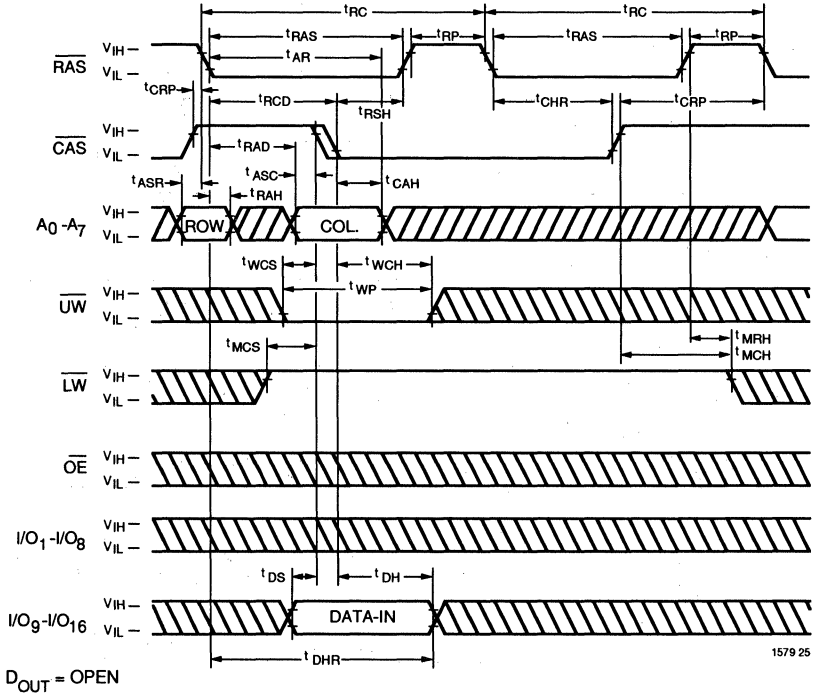
NOTE: D_{IN} = OPEN

Hidden Refresh Cycle (Write)



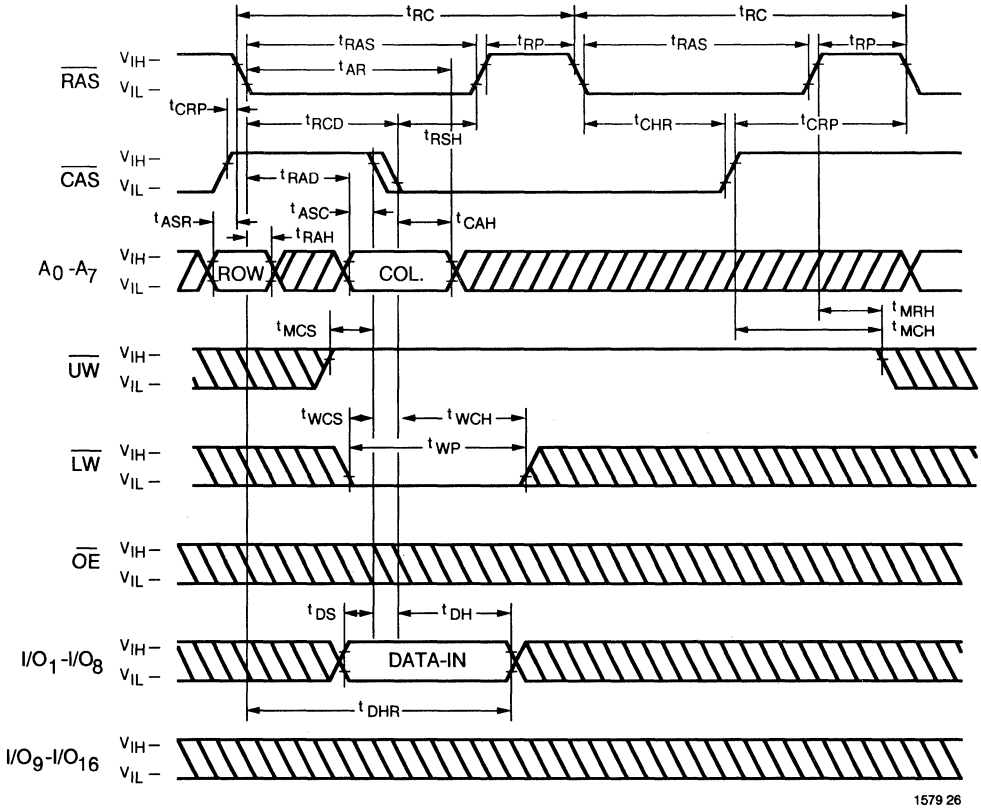
NOTE: D_{OUT} = OPEN

Hidden Refresh Cycle (Upper Byte Write)



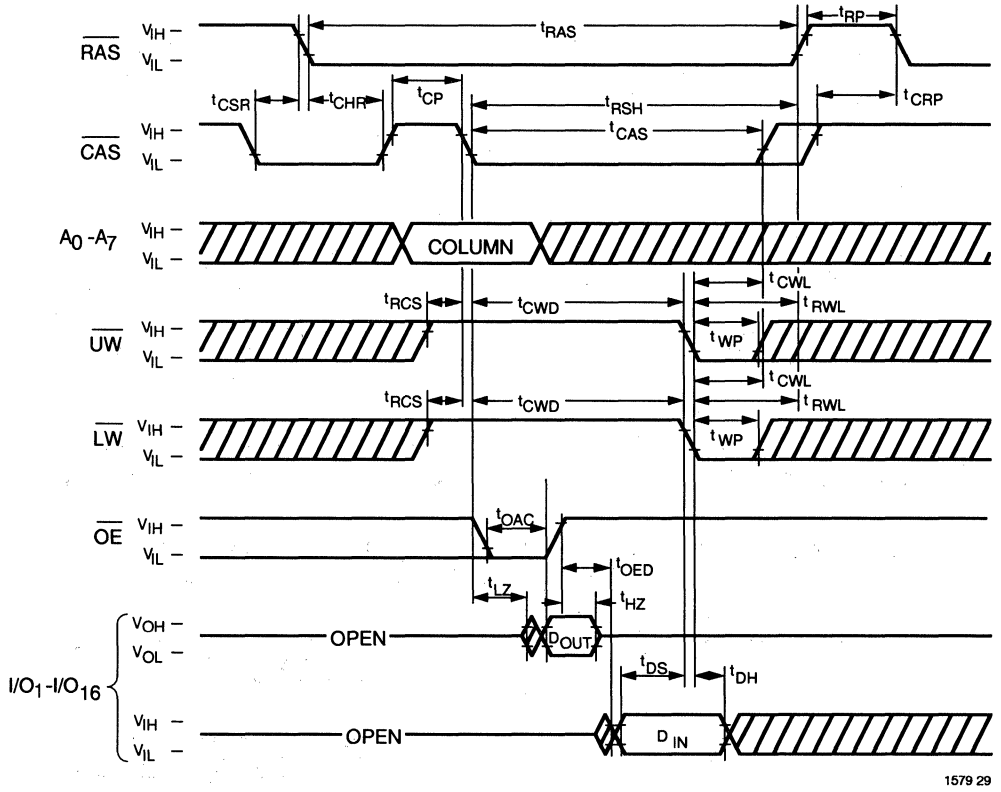
NOTE: D_{OUT} = OPEN

Hidden Refresh Cycle (Lower Byte Write)



NOTE: D_{OUT} = OPEN

$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



V53C8256H
ULTRA-HIGH PERFORMANCE, LOW POWER 256K X 8 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE	45/45L	50/50L	55/55L	60/60L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	45 ns	50 ns	55 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	22 ns	24 ns	28 ns	30 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	25 ns	28 ns	38 ns	40 ns
Min. Read/Write Cycle Time, (t_{RC})	100 ns	110 ns	115 ns	120 ns

LOW POWER V53C8256HL	45L	50L	55L	60L
Max. CMOS Standby Current, (I_{DD6})	150 µA	150 µA	150 µA	150 µA

Features

- 256K x 8-bit organization
- $\overline{RAS}$ access time: 45, 50, 55, 60 ns
- Low power dissipation
  - V53C8256H-60
    - — Operating Current – 135 mA max
    - — TTL Standby Current – 2.0 mA max
- Low CMOS Standby Current
  - V53C8256H – 1.0 mA max
  - V53C8256HL – .15 mA max
- Low Battery Back-up Current
  - V53C8256HL – 200µA max
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V53C8256H – 512 cycles/8 ms
  - V53C8256HL – 512 cycles/64 ms
- Fast Page Mode for a sustained data rate greater than 33 MHz
- Available in 24 pin 300 mil Plastic DIP and 26/24 pin 300 mil SOJ packages

Description

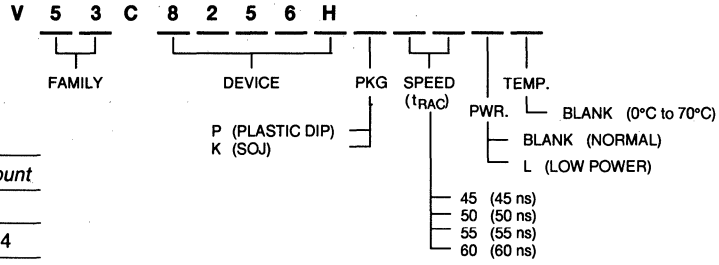
The V53C8256H is a high speed 262,144 x 8 bit CMOS dynamic random access memory. Fabricated with Mosel-Vitelic's VICMOS III technology, the V53C8256H offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C8256HL).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x8) bits within a row with cycle times as short as 30 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C8256H ideally suited for graphics, digital signal processing and high performance computing systems.

The V53C8256HL offers a maximum data retention power of 1.1 mW when operating in CMOS standby mode and performing $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles. This mode is entered by holding $\overline{RAS}$ at a voltage greater than V_{DD} – 0.2 when it is inactive.

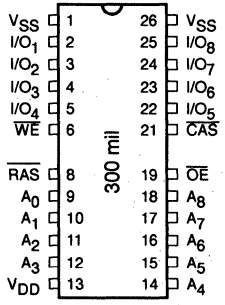
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power		Temperature Mark
	P	K	45	50	55	60	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	•	Blank

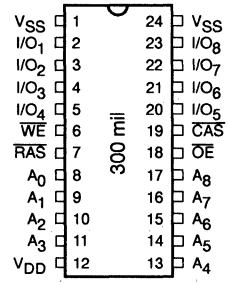


Description	*Pkg.*	*Pin Count*
Plastic DIP	P	24
SOJ	K	26/24

26/24 Lead SOJ PIN CONFIGURATION Top View



24 Lead Plastic DIP PIN CONFIGURATION Top View



Pin Names

A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_8	Data Input, Output
V_{DD}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

*Absolute Maximum Ratings**

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage Relative to V_{SS} .....–1.0 V to +7.0 V
Data Output Current .....50 mA
Power Dissipation .....1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

*Capacitance**

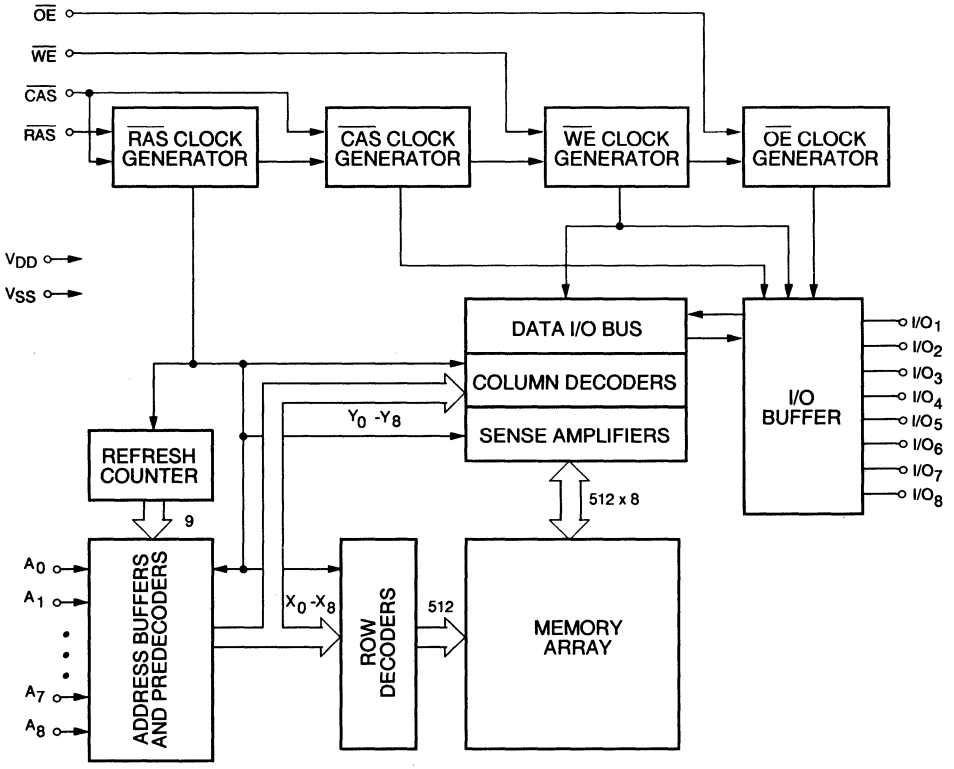
T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram

256K x 8



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C8256H			V53C8256HL			Unit	Test Conditions	Notes
			Min.	Typ.	Max.	Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10		10	-10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10		10	-10		10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	45			160			160	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		50			150			150			
		55			145			145			
		60			135			135			
I_{DD2}	V_{DD} Supply Current, TTL Standby				2			2	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	45			160			160	mA	$t_{RC} = t_{RC}$ (min.)	2
		50			150			150			
		55			145			145			
		60			135			135			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	45			95			95	mA	Minimum Cycle	1, 2
		50			90			90			
		55			85			85			
		60			80			80			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled				2.0			2.0	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby				1.0			0.15	mA	$\overline{RAS} \ge V_{DD} - 0.2$ V, $\overline{CAS} \ge V_{DD} - 0.2$ V, All other inputs ≥ V_{SS}	
I_{DD7}	Battery Back-up Data Retention Current (V53C8256HL Only)				N.A.			0.3	mA	$\overline{CAS}$-before-$\overline{RAS}$ Refresh cycle t_{RC} = 125 µs CMOS clock levels	18
V_{IL}	Input Low Voltage		–1		0.8	-1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{DD}+1	2.4		V_{DD}+1	V		3
V_{OL}	Output Low Voltage				0.4			0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4			2.4			V	I_{OH} = –5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	45/L		50/L		55/L		60/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	45	75K	50	75K	55	75K	60	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	100		110		115		120		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	35		40		45		50		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	45		50		55		60		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	12		12		15		15		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	31	19	36	20	40	20	45	ns	
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	4
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8		9		10		10		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	6		7		10		10		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	14		14		15		15		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	4		4		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	9		9		10		10		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		12		12		15		15	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		12		12		15		15	ns	6, 7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		45		50		55		60	ns	6, 8, 9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		22		24		28		30	ns	6, 7, 10
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	8	0	8	0	10	0	10	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	35		40		45		50		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	23	14	26	15	27	15	30	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH\ (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	14		14		15		15		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	14		14		15		15		ns	

AC Characteristics (Cont'd)

#	JEDEC Symbol	Symbol	Parameter	45/L		50/L		55/L		60/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12, 13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	6		7		10		10		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	6		7		10		10		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	35		40		45		50		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	14		14		15		15		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	6		7		10		10		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	9		9		10		10		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	8		8		10		10		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	135		145		160		170		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	85		90		100		105		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	31		33		38		40		ns	12
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	65		70		80		85		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	50		54		62		65		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	41		43		55		58		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	25		28		38		40		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	7		8		10		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	22		24		28		30		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		24		26		32		34	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	35		40		45		50		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	12		12		15		15		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	65		70		82		85		ns	

AC Characteristics (Cont'd)

#	JEDEC Symbol	Symbol	Parameter	45/L		50/L		55/L		60/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
		t_{REF}	Refresh Interval (512 Cycles)		8		8		8		8	ms	17
		t_{REF}	Refresh Interval V53C8256HL Only (512 Cycles, t_{RC}= 125 µs)		64		64		64		64	ms	17, 18

2

Notes:

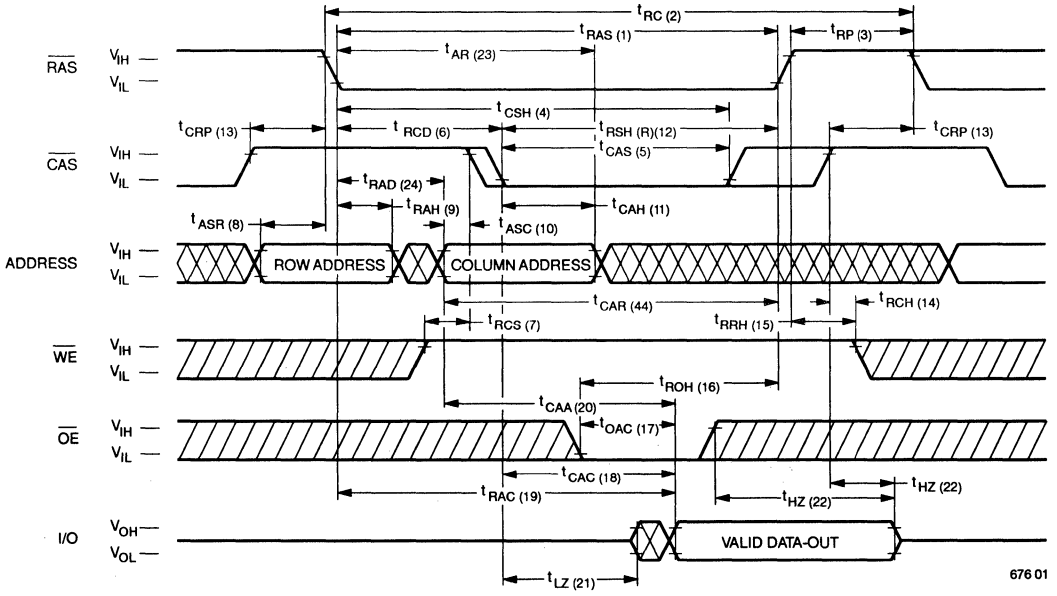
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

    t_{RC} = 125 µs (125 µs x 512 = 64 ms)

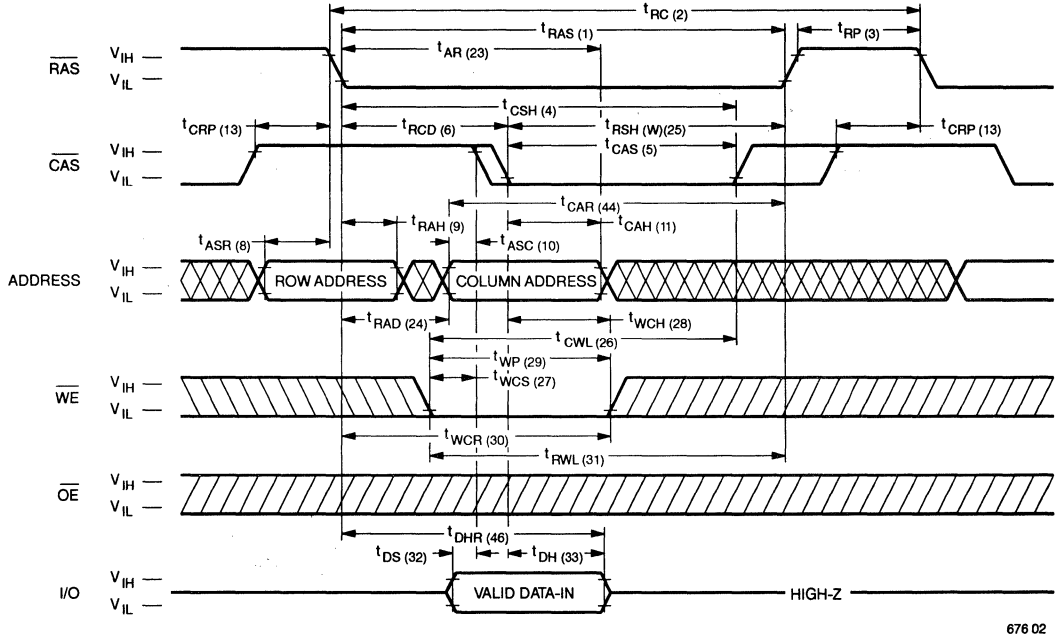
    $t_{RAS} = t_{RAS}$ (min.) to 1 µs

    Input voltages: $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V
    $V_{IL} < 0.2$ V
    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V
    All other inputs at stable V_{IH} or V_{IL}

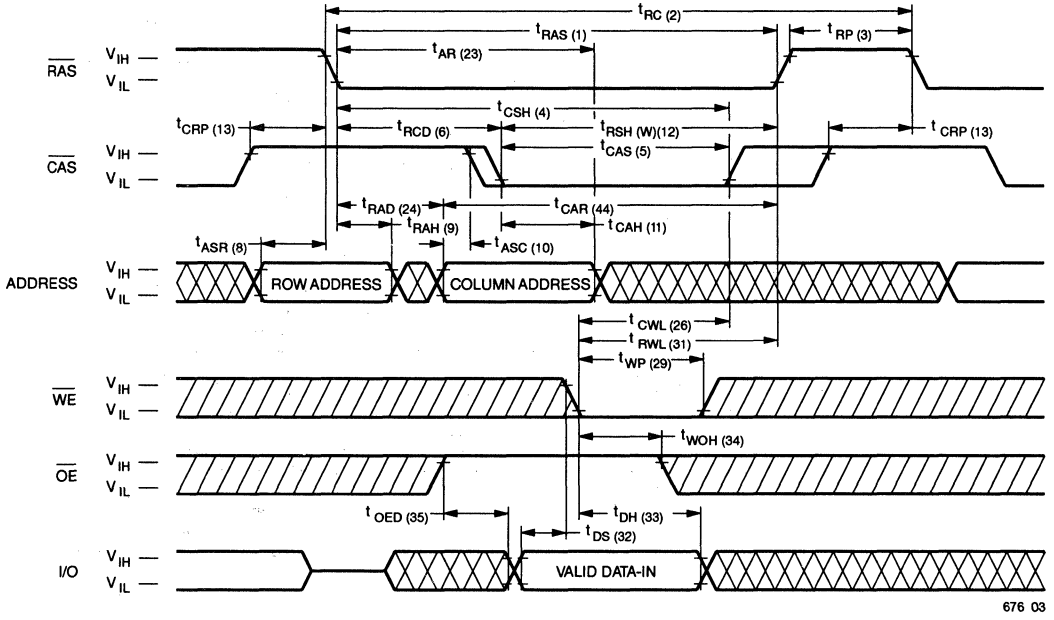
Waveforms of Read Cycle



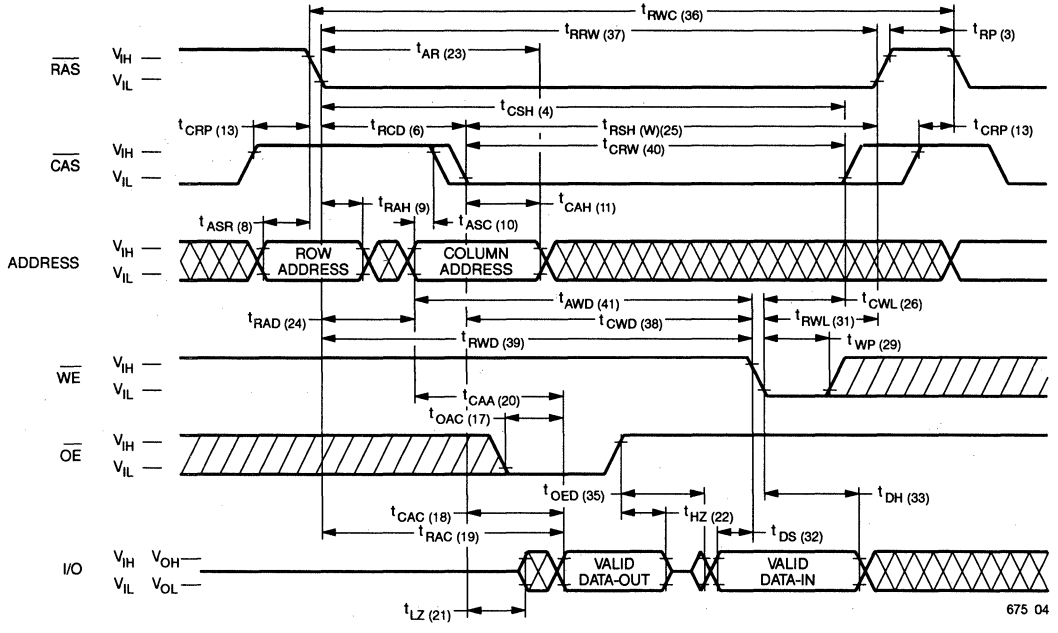
Waveforms of Early Write Cycle



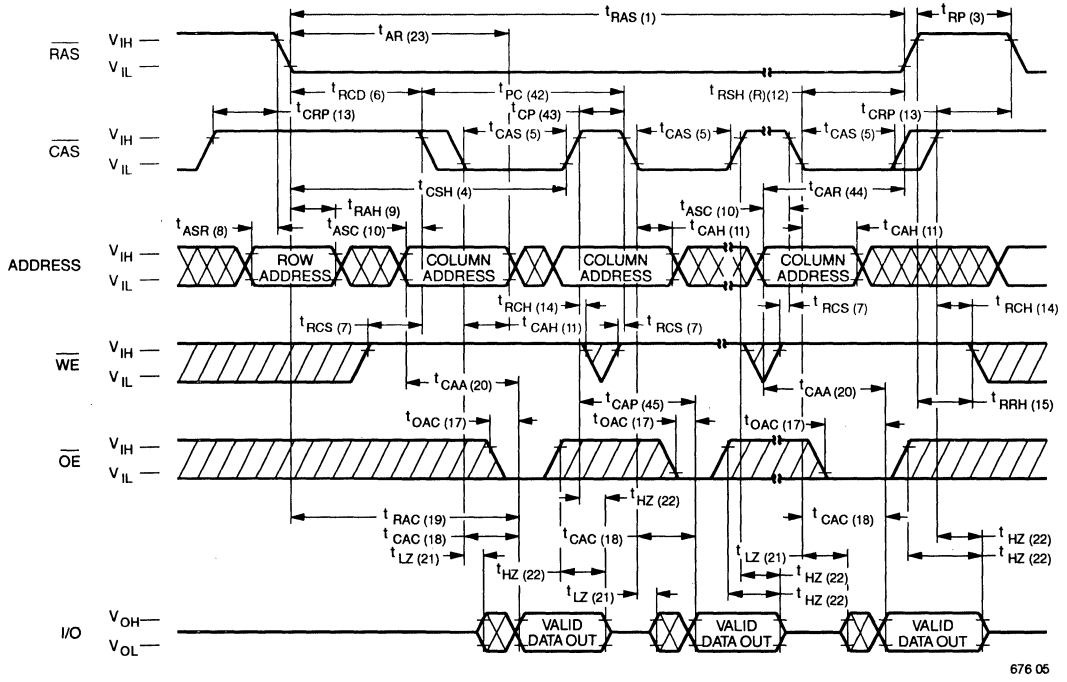
Waveforms of $\overline{OE}$-Controlled Write Cycle



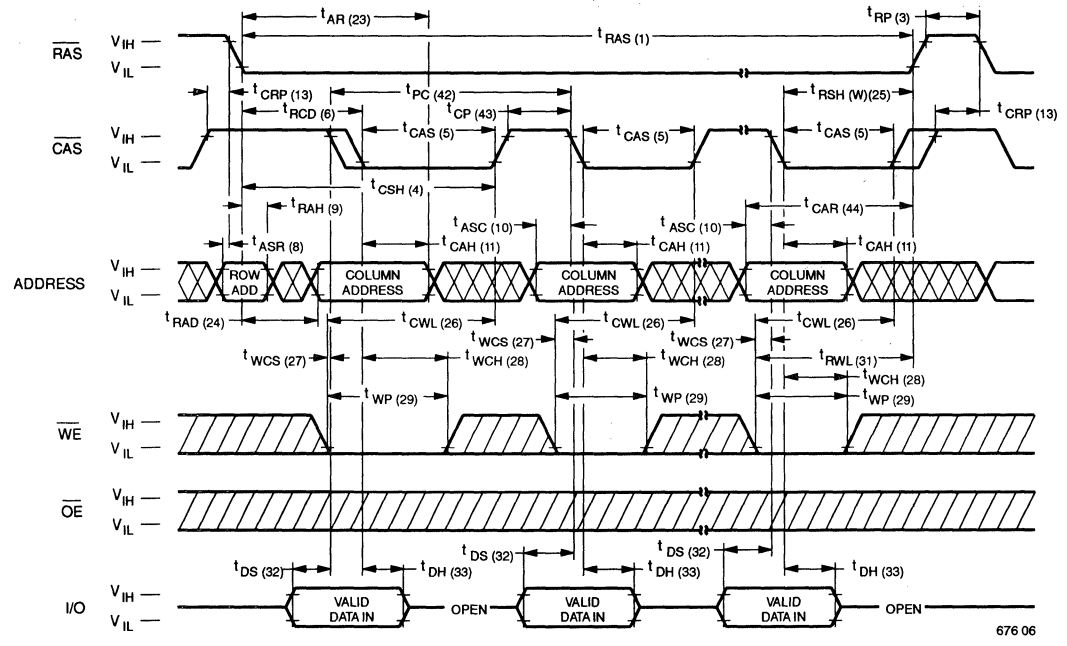
Waveforms of Read-Modify-Write Cycle



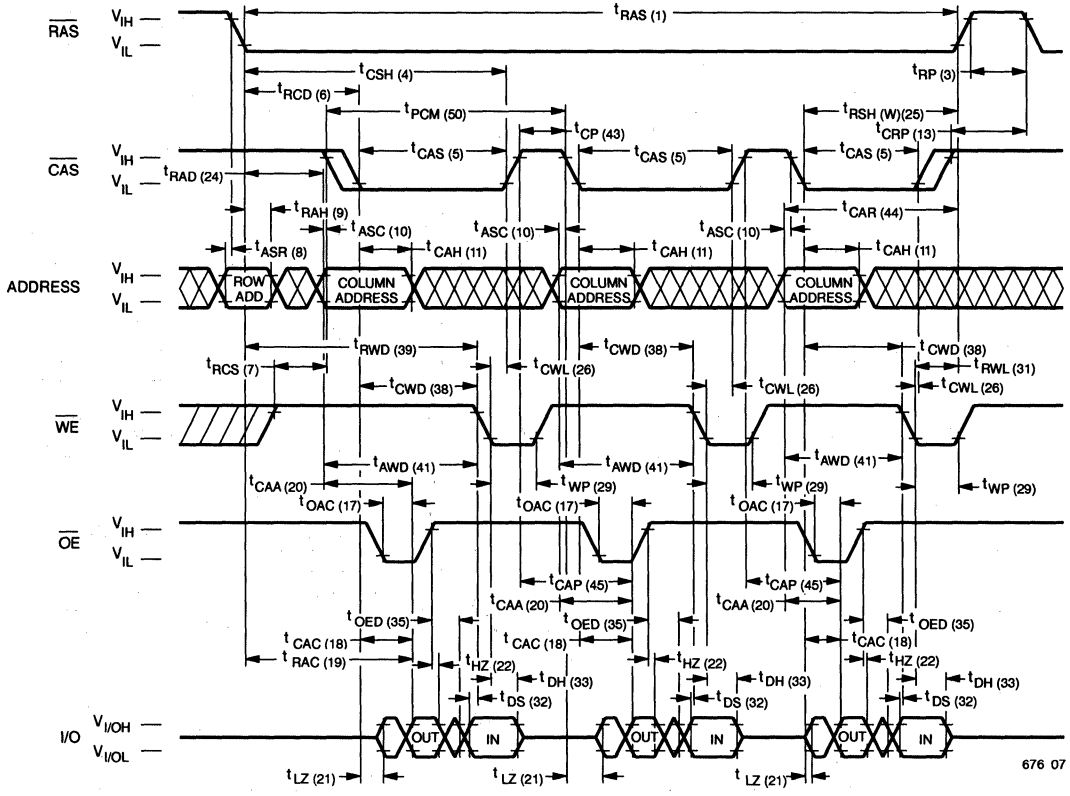
Waveforms of Fast Page Mode Read Cycle



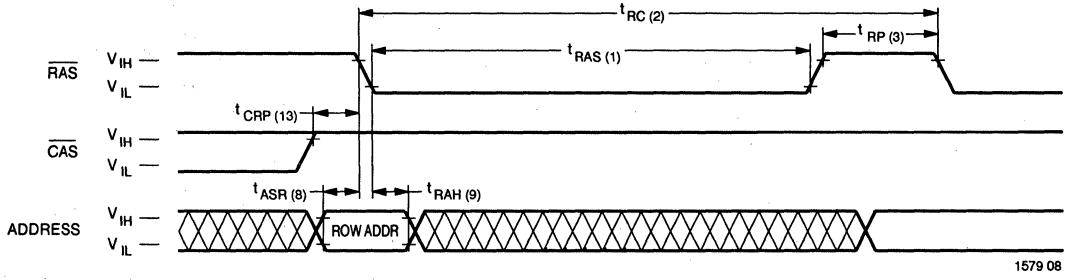
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Write Cycle

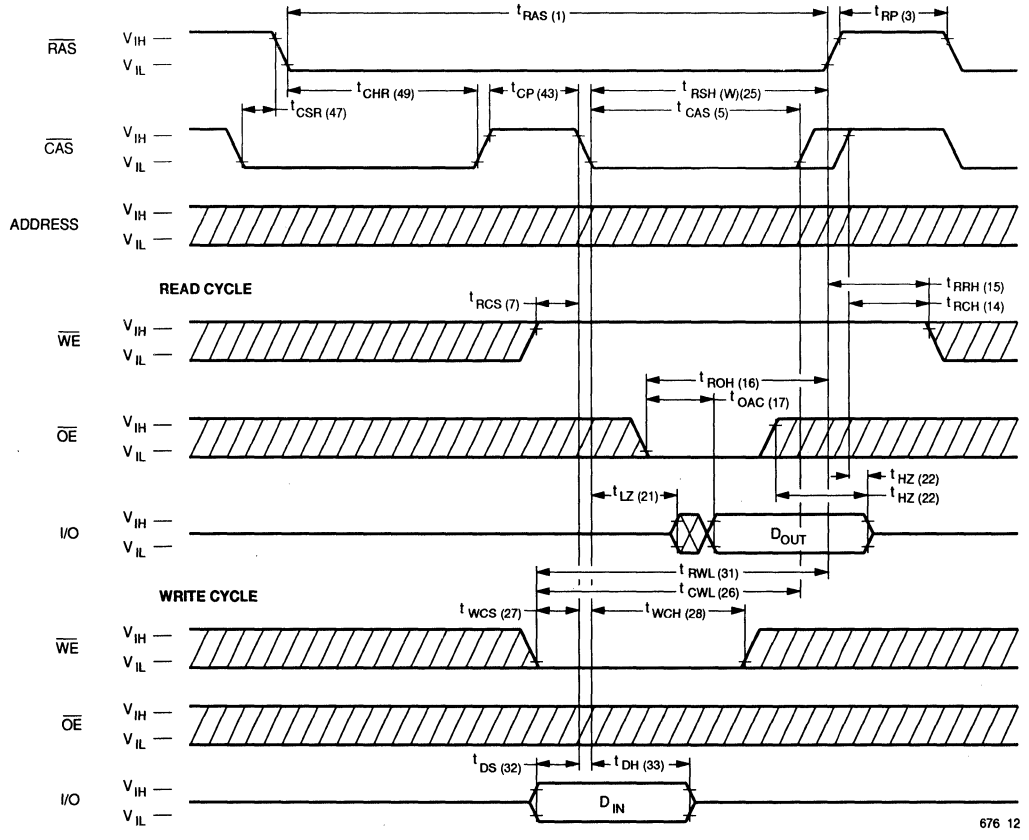


Waveforms of RAS-Only Refresh Cycle

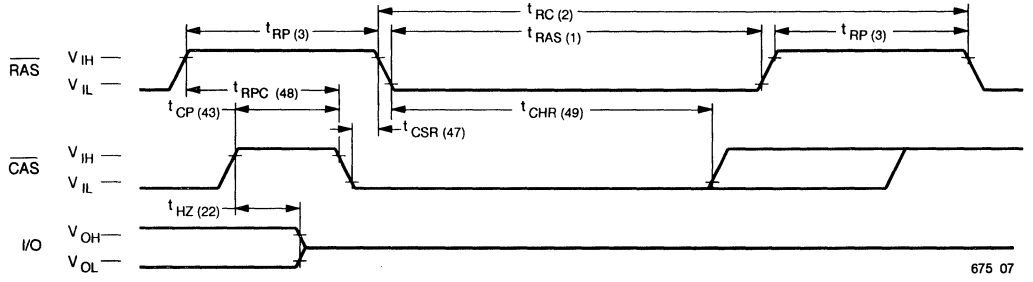


NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

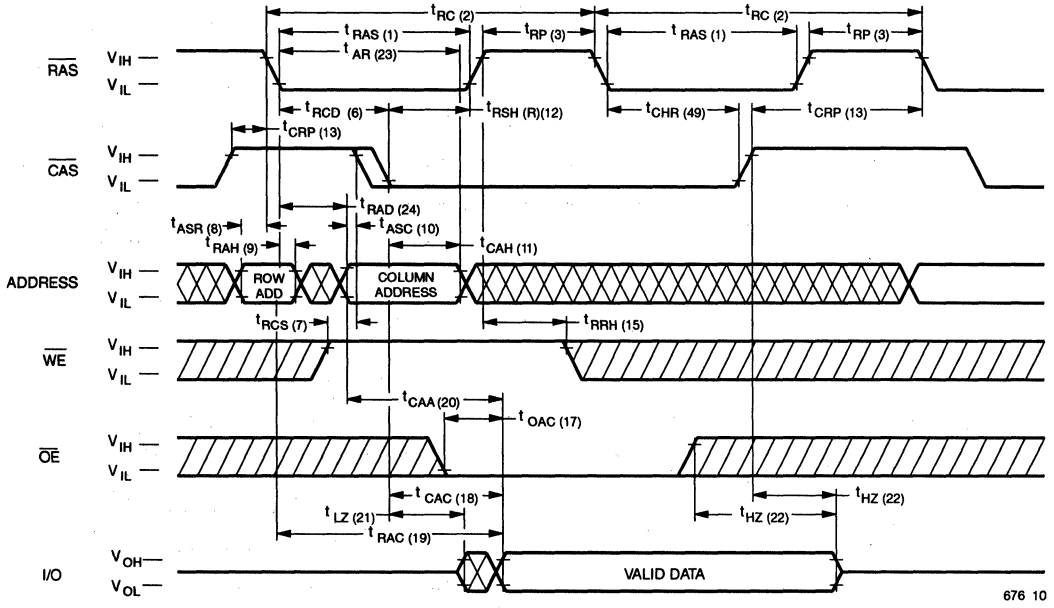


Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

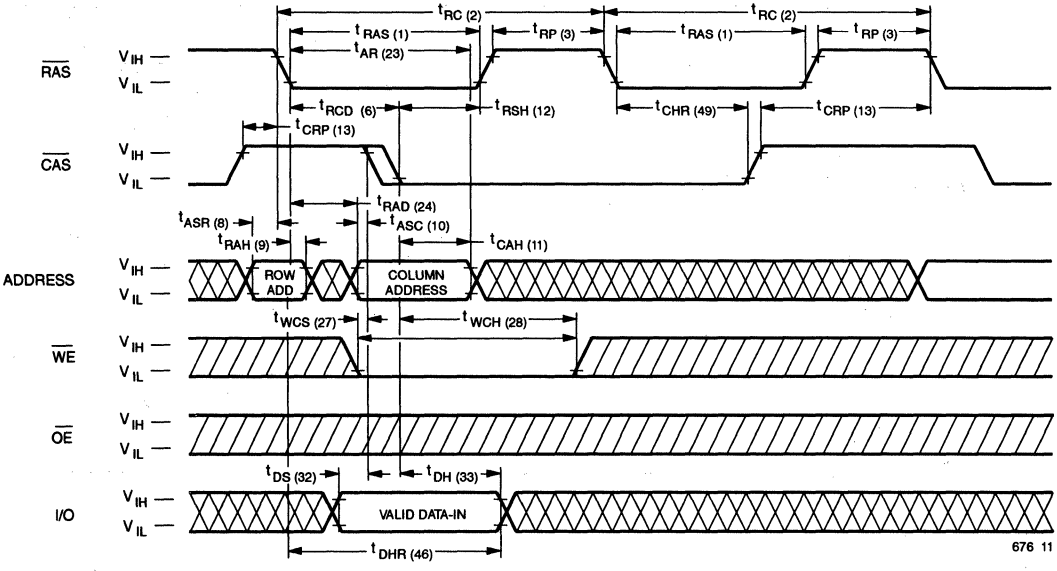


NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_7 = Don't care

Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Functional Description

The V53C8256H is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C8256H reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C8256H uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C8256H offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C8256H power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 33 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

Data Output Operation

The V53C8256H Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C8256H is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C8256H Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

V53C8256N
HIGH PERFORMANCE, 3.3 VOLT 256K X 8 BIT FAST PAGE MODE CMOS DYNAMIC RAM

ADVANCED INFORMATION

HIGH PERFORMANCE V53C8256N	60/60L	70/70L	80/80L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	45 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns
Min. Read-Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns

LOW POWER V53C8256N	60L	70L	80L
Max. CMOS Standby Current, (I_{DD6})	80 µA	80 µA	80 µA

Features

- 3.3 Volt Operation
- 256K x 8-bit organization
- RAS access time: 60,70,80 ns
- Low power dissipation for V53C8256N-80
  - Operating Current – 55 mA max.
  - TTL Standby Current – 1.0 mA max.
- Low CMOS Standby Current
  - V53C8256N – 500 µA max.
  - V53C8256NL – 80 µA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Common I/O capability
- Refresh Interval
  - V53C8256N – 512 cycles/8ms
  - V53C8256NL – 512 cycles/64ms
- On-chip substrate bias generator
- Fast Page Mode operation for a sustained data rate greater than 25 MHz
- Standard packages are 24 pin Plastic DIP and 26/24 300 mil SOJ package
- Low Battery Back-up Current
  - V53C8256NL – 200 µA max.

Description

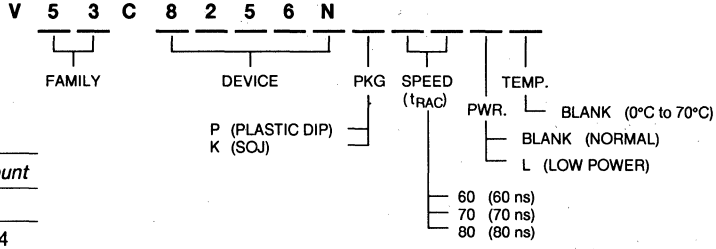
The V53C8256N is a high speed 262,144 x 8 bit CMOS dynamic random access memory. The V53C8256N offers a combination of features: 3.3 V Operation, Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C8256NL).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random or sequential access of up to 512 (x8) bits within a row with cycle times as short as 45 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical timing requirements for fast usable speed. These features make the V53C8256N ideally suited for cache based mainframe and mini computers, graphics, digital signal processing and high performance microprocessor systems.

The V538256NL offers a maximum data retention power of 0.8 mW when operating in CMOS standby mode and performing $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

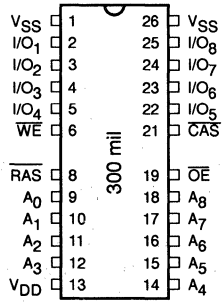
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power		Temperature Mark
	P	K	60	70	80	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	Blank

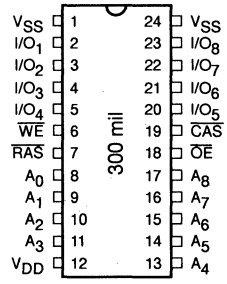


Description	*Pkg.*	*Pin Count*
Plastic DIP	P	24
SOJ	K	26/24

26/24 Lead SOJ PIN CONFIGURATION Top View



24 Lead Plastic DIP PIN CONFIGURATION Top View



Pin Names

A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_8	Data Input, Output
V_{DD}	+3.3V Supply
V_{SS}	0V Supply
NC	No Connect

*Absolute Maximum Ratings**

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage Relative to V_{SS} .....–0.5 V to +6.0 V
Data Output Current .....50 mA
Power Dissipation .....1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

*Capacitance**

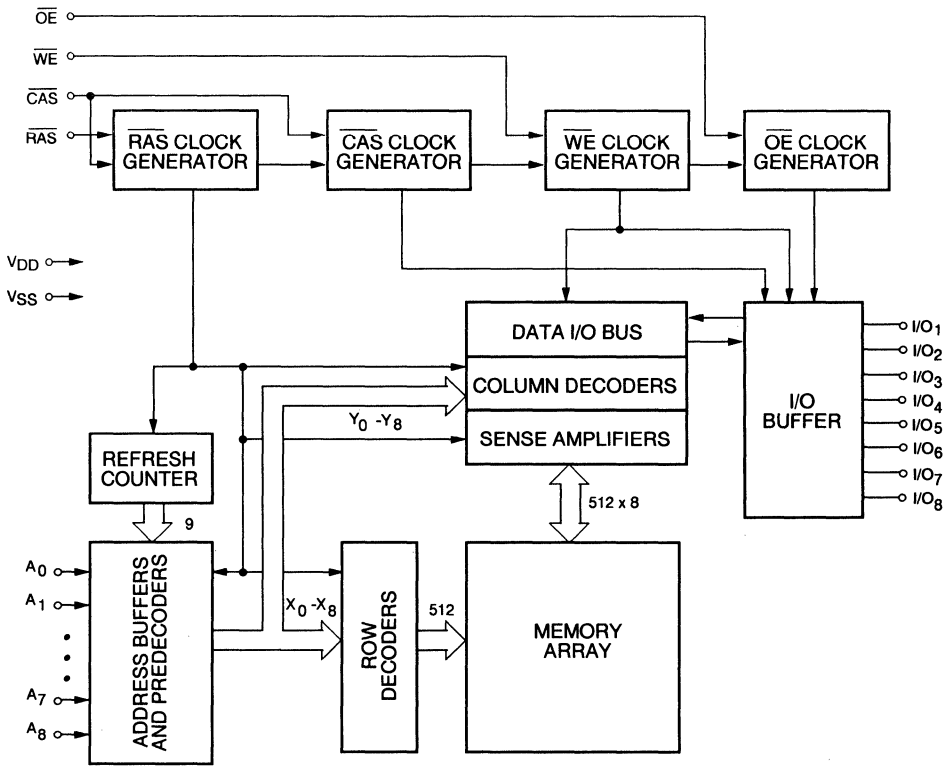
T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram

256K x 8



2

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 3.3V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C8256N			V53C8256NL			Unit	Test Conditions	Notes
			Min.	Typ.	Max.	Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10		10	-10		10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10		10	-10		10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60			65			65	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		70			60			60			
		80			55			55			
I_{DD2}	V_{DD} Supply Current, TTL Standby				1.0			1.0	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60			65			65	mA	$t_{RC} = t_{RC}$ (min.)	2
		70			60			60			
		80			55			55			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60			60			60	mA	Minimum Cycle	1, 2
		70			50			50			
		80			45			45			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled				2.0			1.0	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby				0.6			0.08	mA	$\overline{RAS} \ge V_{DD} - 0.2$ V, $\overline{CAS} \ge V_{DD} - 0.2$ V, All other inputs ≥ V_{SS}	
I_{DD7}	Battery Back-up Data Retention Current (V53C8256NL Only)				N.A.			0.3	mA	$\overline{CAS}$-before-$\overline{RAS}$ Refresh cycle t_{RC} = 125 µs CMOS clock levels	18
V_{IL}	Input Low Voltage		-0.5		0.6	-0.5		0.6	V		3
V_{IH}	Input High Voltage		2.2		V_{DD} + 0.5	2.2		V_{DD} + 0.5	V		3
V_{OL}	Output Low Voltage				0.4			0.4	V	I_{OL} = 3 mA	
V_{OH}	Output High Voltage		2.4			2.4			V	I_{OH} = -3 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 3.3V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	120		130		150		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		25		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	40	25	45	25	55	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		15		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		25		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	5		5		5		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	5		5		5		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		10		10		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		20		25		25	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		25		25	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		45	ns	6,7, 10

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	20	0	20	0	20	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	25	20	30	20	35	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH\ (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		25		25		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		15		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		15		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		25		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		15		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	15		15		15		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	15		20		20		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	180		195		215		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	115		135		145		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	45		55		55		ns	12

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	85		100		110		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	75		85		85		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	65		70		75		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		30		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95		105		110		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{REF}	Refresh Interval (512 Cycles)		8		8		8	ms	17
		t_{REF}	Refresh Interval V53C104NL Only (512 Refresh cycles, t_{RC}=125 µs)		64		64		64	ms	17,18

Notes:

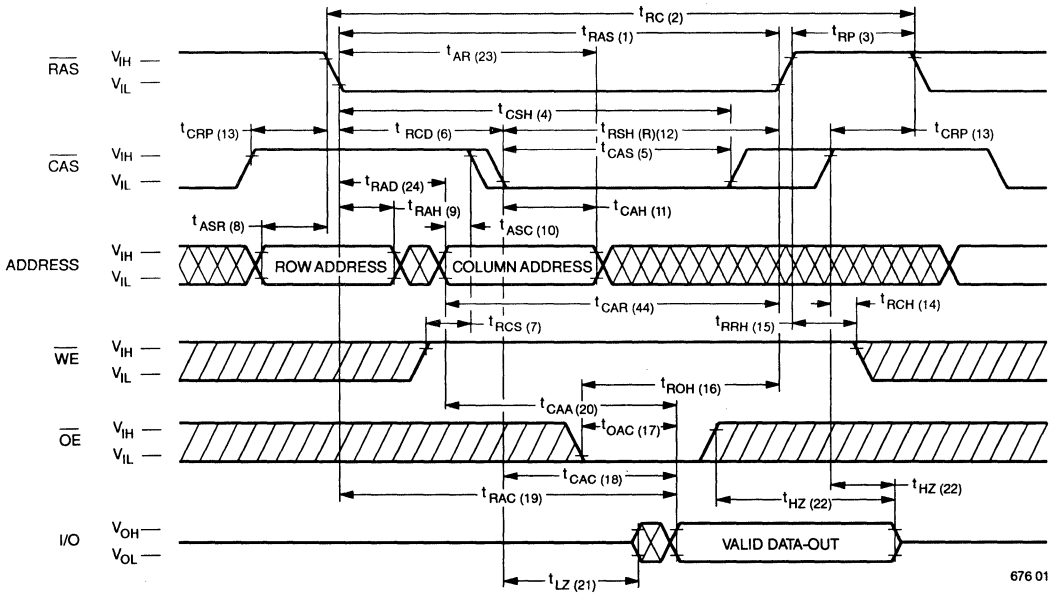
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 50 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

    t_{RC} = 125 µs (125 µs x 512 = 64 ms)

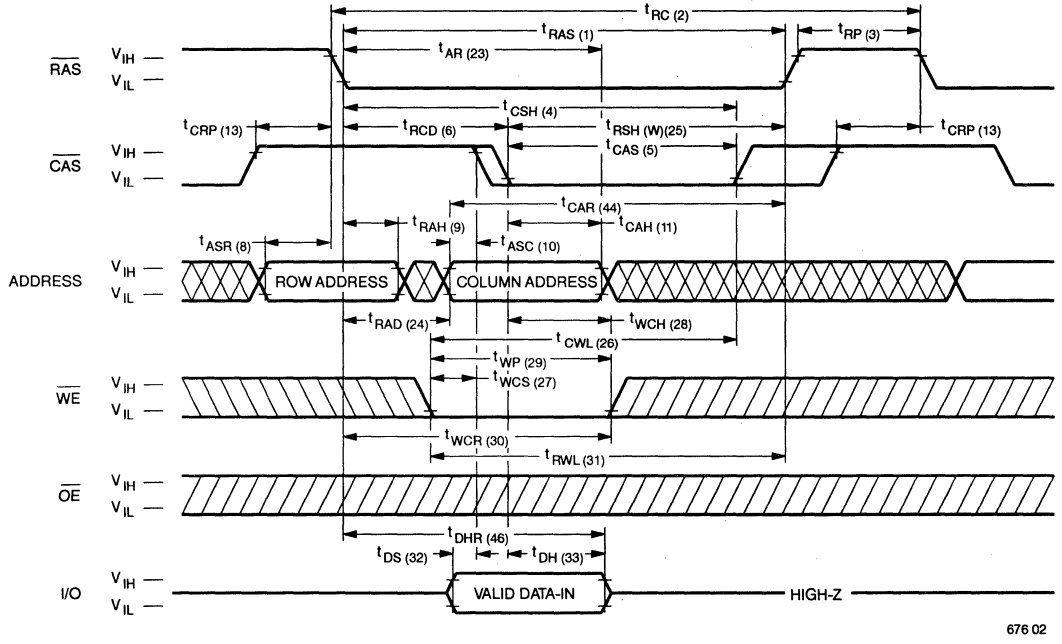
    $t_{RAS} = t_{RAS}$ (min.) to 1 µs

    Input voltages: $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V
    $V_{IL} < 0.2$ V
    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V
    All other inputs at stable V_{IH} or V_{IL}

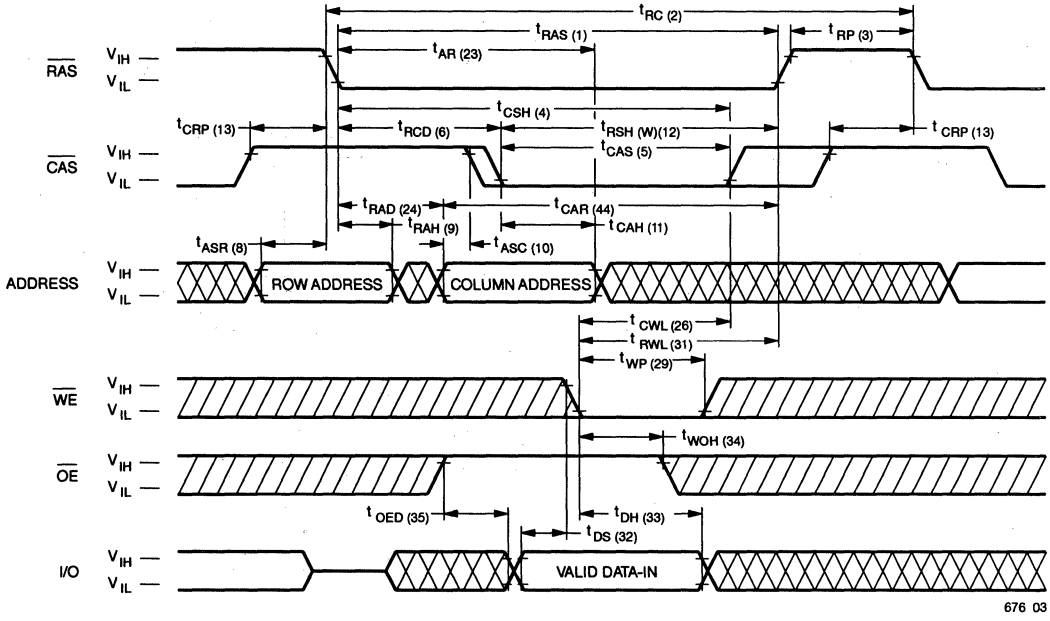
Waveforms of Read Cycle



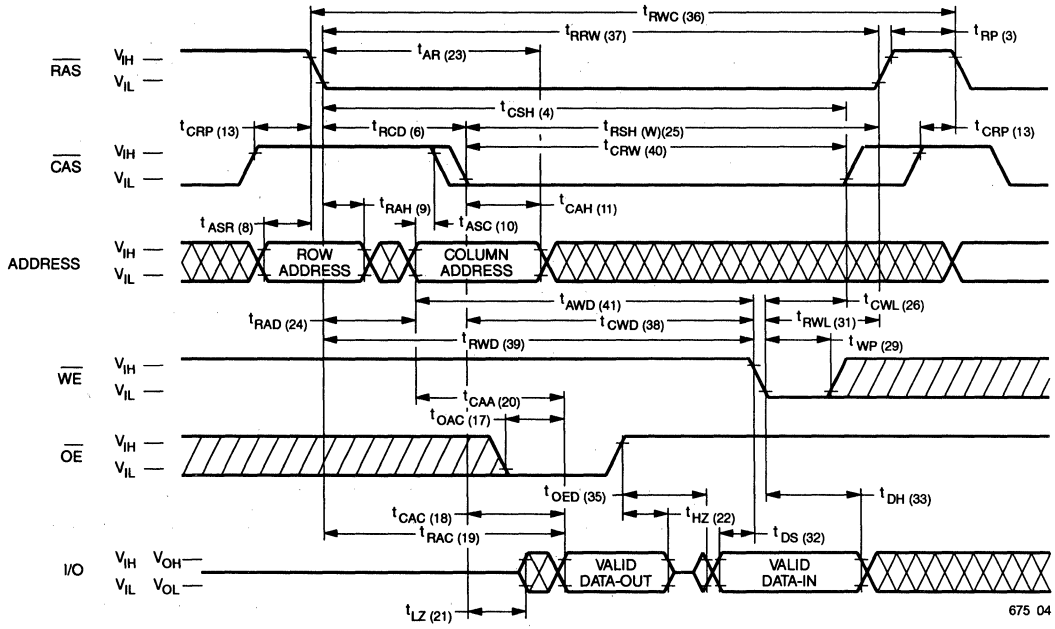
Waveforms of Early Write Cycle



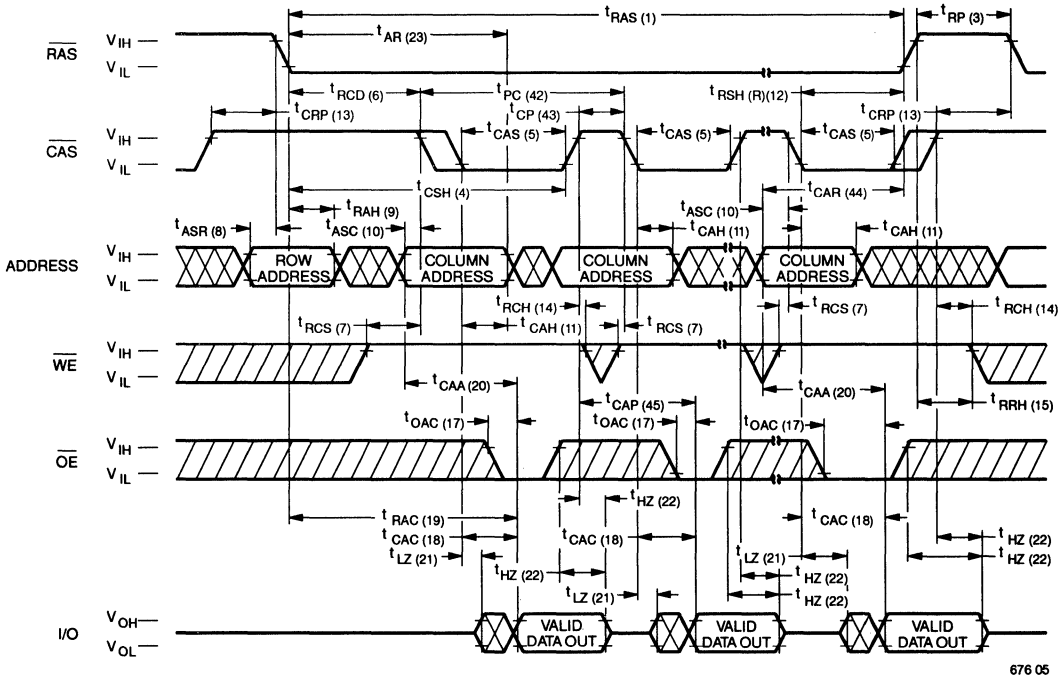
Waveforms of $\overline{OE}$-Controlled Write Cycle



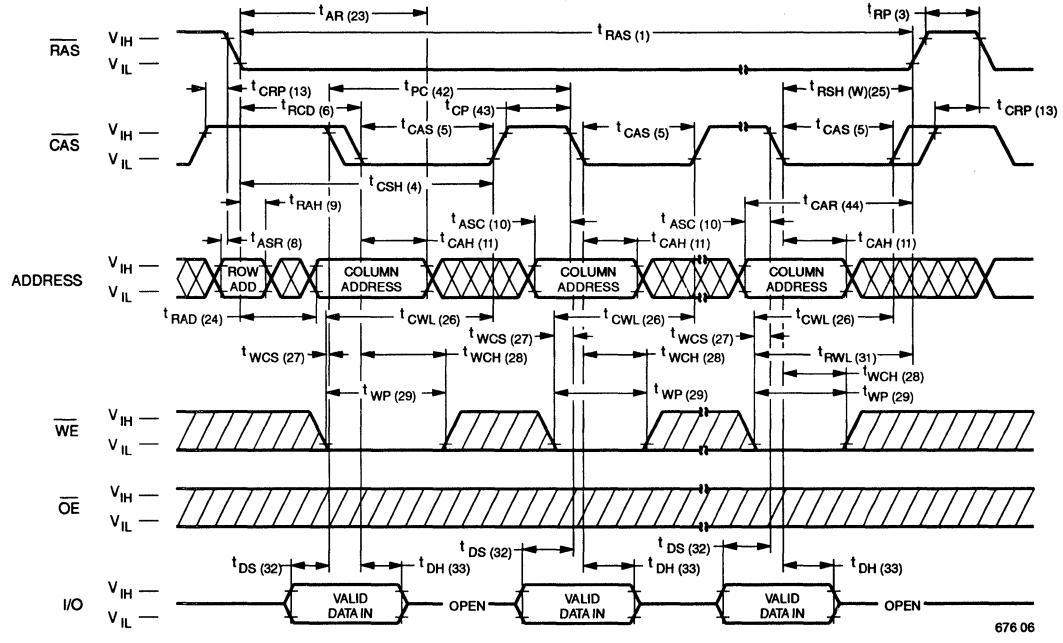
Waveforms of Read-Modify-Write Cycle



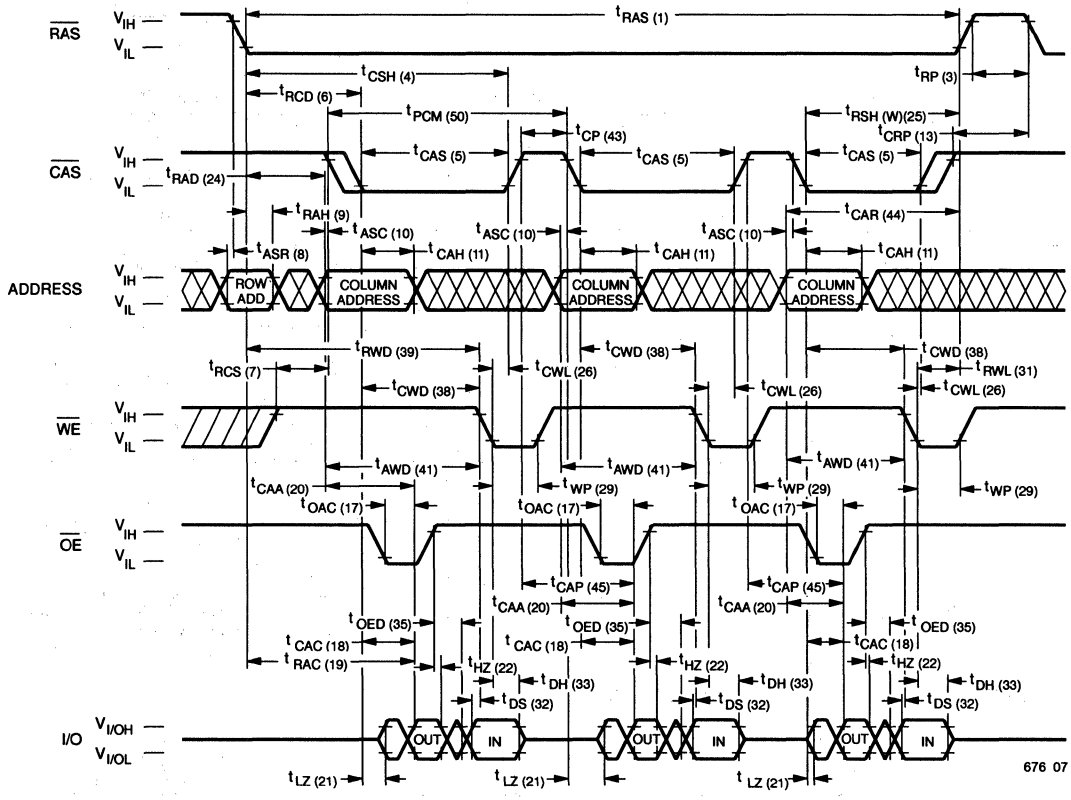
Waveforms of Fast Page Mode Read Cycle



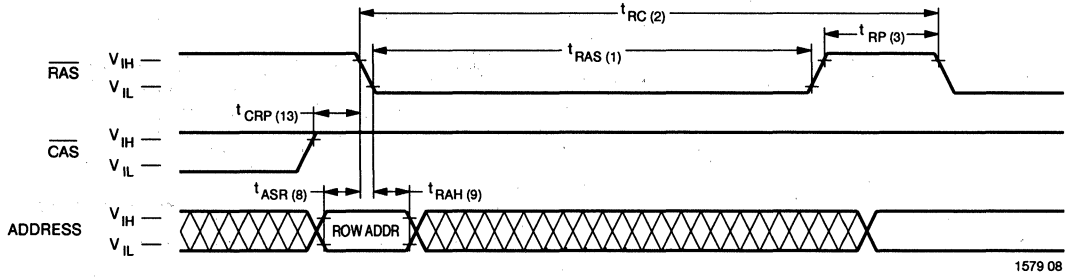
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Write Cycle

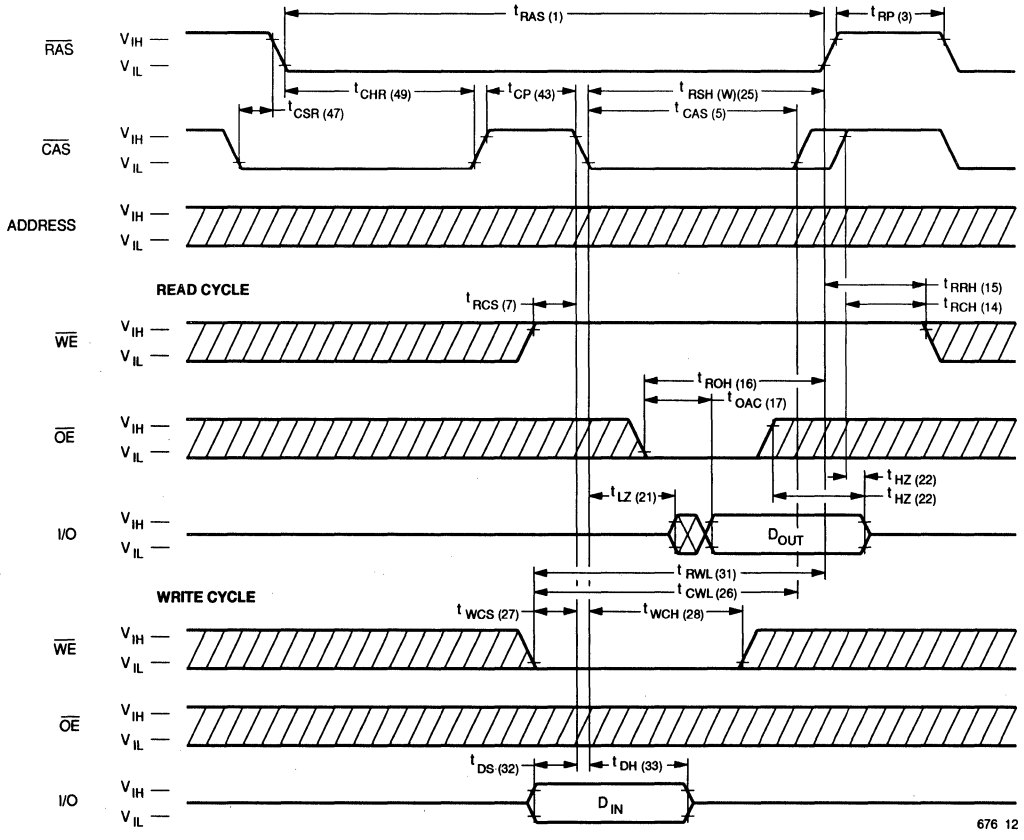


Waveforms of RAS-Only Refresh Cycle

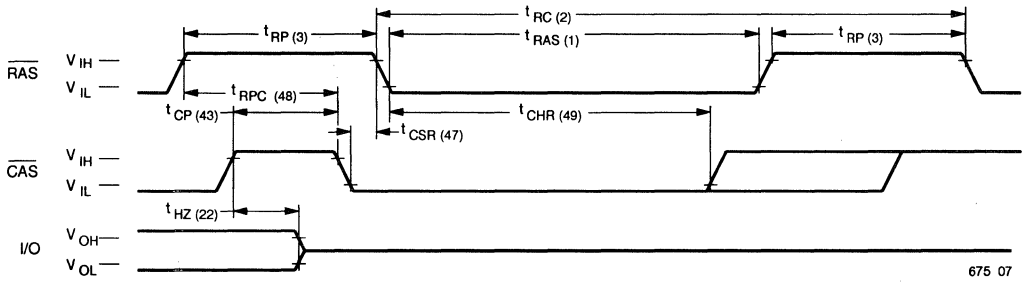


NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

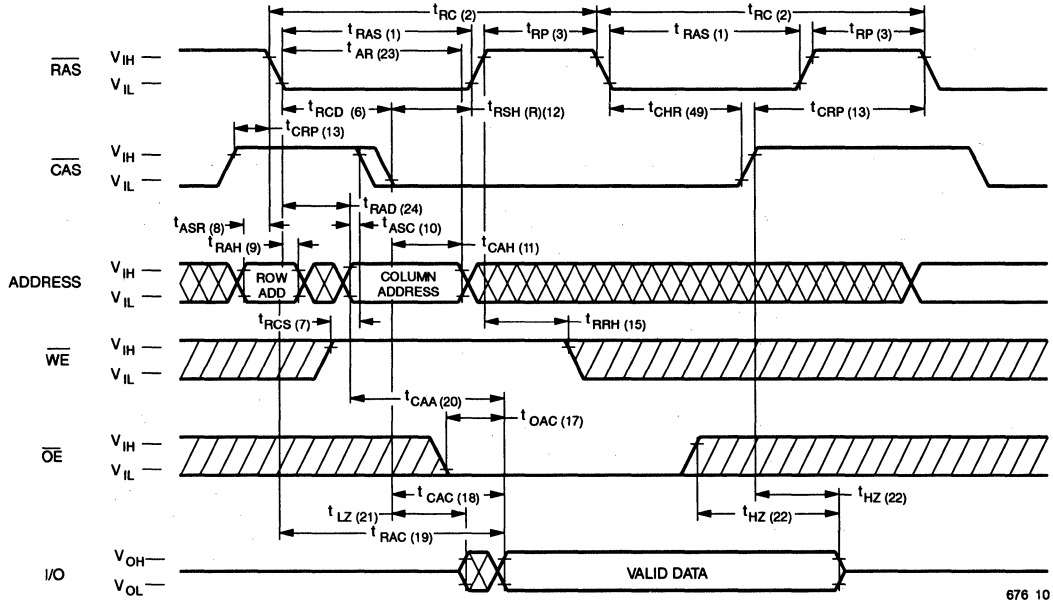


Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

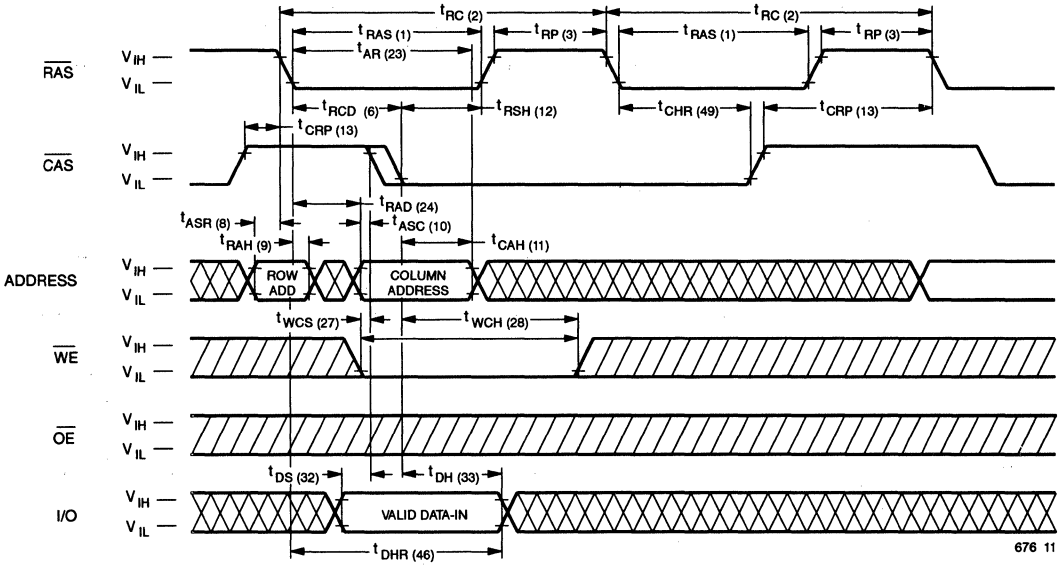


NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_7 = Don't care

Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Functional Description

The V53C8256N is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C8256N reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses (A_0 through A_8) with $\overline{RAS}$ at least once every 8 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C8256N uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C8256N offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C8256N power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 512

Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 25 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

Data Output Operation

The V53C8256N Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C8256N is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C8256N Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

V53C8257H
ULTRA-HIGH SPEED, 256K X 8 BIT BURST AND FAST PAGE MODE CMOS DYNAMIC RAM

ADVANCED INFORMATION

HIGH PERFORMANCE	45/45L	50/50L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	45 ns	50 ns
Max. Column Address Access Time, (t_{CAA})	24 ns	26 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	30 ns	32 ns
Min. Read/Write Cycle Time, (t_{RC})	100 ns	110 ns
Min. Burst Mode Cycle Time, (t_{BC})	15 ns	20 ns

Features

- 256K x 8-bit organization
- Burst Mode for a sustained data rate greater than 65 MHz
- Fast Page Mode for a sustained data rate greater than 33 MHz
- $\overline{RAS}$ access time: 45, 50 ns
- Low power dissipation
  - V53C8257H-45
    - — Operating Current – 135 mA max
    - — TTL Standby Current – 2.0 mA max
- Low CMOS Standby Current
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V53C8257H – 512 cycles/8 ms
- Available in 24 pin 300 mil Plastic DIP and 26/24 pin 300 mil SOJ packages

Description

The V53C8257H is a high speed 262,144 x 8 bit CMOS dynamic random access memory. The V53C8257H offers a combination of features: Burst Mode and Fast Page Mode for high data bandwidth.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Burst Mode operation provides 256 (x8) sequential address bursts with cycle times as short as 15 ns. Burst Mode operation requires no external address information. Fast Page Mode operation allows random access of up to 512 (x8) bits within a row with cycle times as short as 30 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C8257H ideally suited for graphics, digital signal processing and high performance computing systems.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Power		Temperature Mark
	P	K	45	50	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	Blank

HIGH PERFORMANCE, LOW POWER 4M X 1 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C400F	60/60L	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns	65 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns	180 ns

LOW POWER V53C400FL	60L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	0.4 mA	0.4 mA	0.4 mA	0.4 mA

Features

- 4M x 1-bit organization
- RAS access time: 60,70,80,100 ns
- Low power dissipation
  - V53C400F-10
    - — Operating Current – 75 mA max.
    - — TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C400F – 1.0 mA max.
  - V53C400FL – 0.4 mA max.
- Battery Back-up Mode (V53C400FL Only)
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V53C400F – 1024 cycles/16ms
  - V53C400FL – 1024 cycles/64ms
- On-chip substrate bias generator
- Fast Page Mode for a sustained data rate greater than 20 MHz
- Available in 26/20 pin SOJ package (300 mil)

Description

The V53C400F is a high speed 4,194,304x1 bit CMOS dynamic random access memory. The V53C400F offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C400FL).

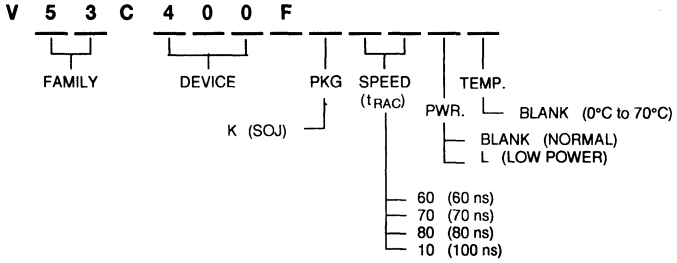
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 1024 bits within a row with cycle times as short as 50 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C400F ideally suited for graphics, digital signal processing and high performance computing systems.

The V53C400FL offers a maximum data retention power of 3.3 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

Device Usage Chart

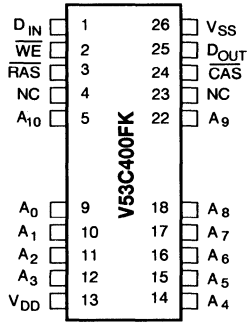
Operating Temperature Range	Package Outline	Access Time (ns)				Power		Temperature Mark
	K	60	70	80	100	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank

V53C400F Rev. 01 January 1993

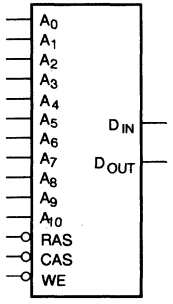


Description	Pkg.	Pin Count
SOJ	K	26/20

26/20 Lead SOJ Package PIN CONFIGURATION Top View



LOGIC SYMBOL



Pin Names

A_0–A_{10}	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{DD}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 V to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

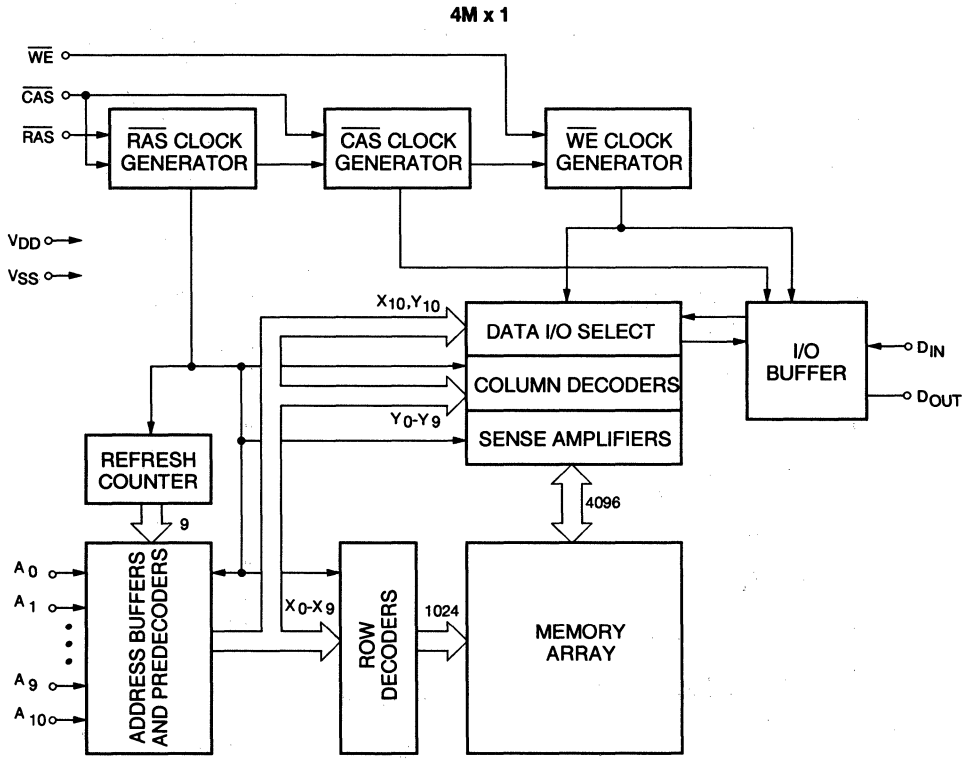
Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	—	7	pF
C_{OUT}	D_{IN}/D_{OUT}	—	7	pF

*Note: Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C400F		V53C400FL		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10	10	−10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10	10	−10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60		100		100	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		70		90		90			
		80		80		80			
		100		70		70			
I_{DD2}	V_{DD} Supply Current, TTL Standby			2.0		2.0	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60		100		100	mA	$t_{RC} = t_{RC}$ (min.)	2
		70		90		90			
		80		80		80			
		100		70		70			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60		100		100	mA	Minimum Cycle	1, 2
		70		90		90			
		80		80		80			
		100		70		70			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			5		4	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	
I_{DD6}	V_{DD} Supply Current, CMOS Standby			1		0.4	mA	$\overline{RAS} \ge V_{DD}$ − 0.2 V $\overline{CAS} \ge V_{DD}$ − 0.2V other inputs ≥ V_{SS}	
I_{DD7}	Battery Back-up Data Retention Current (Only V53C400L)			N.A.		0.6	mA	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle t_{RC} = 62.5 µs CMOS clock levels	18
V_{IL}	Input Low Voltage		−1.0	0.8	−1.0	0.8	V		3
V_{IH}	Input High Voltage		2.4	V_{DD}+1	2.4	V_{DD}+1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4			I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL}	t_{RC}	Read or Write Cycle Time	120		130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		70		ns	
4	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
5	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		10		15		ns	
6	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		40		50		ns	
7	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	4
8	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
9	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		20		ns	
10	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	25	75	ns	5
11	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	6,7,8
12	t_{AVQV}	t_{CAA}	Access Time from ColumnAddress		30		35		40		50	ns	8,9,10
13	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		15		20		20		25	ns	8,10
14	$t_{CL1CH1(R)}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	15		20		20		25		ns	
15	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15		20		20		25		ns	
16	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
17	t_{CH2WX}	t_{RCH}	Read Command Hold Time (Referenced to $\overline{CAS}$)	0		0		0		0		ns	11
18	t_{RH2WX}	t_{RRH}	Read Command Hold Time (Referenced to $\overline{RAS}$)	0		0		0		0		ns	11
19	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		10		ns	
20	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	0	25	ns	12
21	t_{CH2QV}	t_{OH}	Data Hold Time from $\overline{CAS}$	0		0		0		0		ns	11
22	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		15		20		ns	

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
23	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
24	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		75		ns	
25	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	15		20		20		25		ns	
26	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	15		20		20		25		ns	
27	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		75		ns	
28	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	13,14
29	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		15		15		20		ns	
30	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		0		ns	15
31	t_{WH1DX}	t_{DH}	Data In Hold Time	15		15		15		20		ns	15
32	t_{RL1DX}	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	50		55		60		75		ns	
33	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	140		155		175		210		ns	
34	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	80		95		105		130		ns	
35	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time Read-Modify-Write Cycle	60		70		80		100		ns	13
36	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	15		20		20		25		ns	13
37	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	30		35		40		50		ns	13
38	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		35		40		45		55	ns	17
39	$t_{CL2CL2(R)}$	t_{PC}	Fast Page Mode Read or Write Cycle Time	40		45		55		65		ns	
40	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	70		75		80		95		ns	
41	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		25		ns	
42	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		25		ns	
43	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5		5		5		5		ns	

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
44	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	5		5		5		5		ns	
45	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	15		15		15		15		ns	
46	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
47	t_{WH2RL2}	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle)	10		10		10		10		ns	
48	t_{RL1WL2}	t_{WRH}	$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	10		10		10		10		ns	
49	t_{WL1RL2}	t_{WSR}	$\overline{RAS}$ to $\overline{WE}$ set-up Time (Test Mode)	10		10		10		10		ns	20, 21
50	t_{RL1WH1}	t_{WHR}	$\overline{RAS}$ to $\overline{WE}$ hold Time (Test Mode)	10		10		10		10		ns	20, 21
51	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	16
52		t_{REF}	Refresh Interval (1024 Cycles)		16		16		16		16	ms	19
53		t_{REF}	Refresh Interval V53C400FL Only (1024 Cycles, t_{RC} = 62.5 µs)		64		64		64		64	ms	18,19

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
5. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
6. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
8. Measured with a load equivalent to two TTL inputs and 100 pF.
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
10. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
11. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
12. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage level.
13. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
14. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
15. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
16. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
17. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
18. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
19. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

    t_{RC} = 62.5 µs (62.5 µs x 1024 = 64 ms)

    t_{RAS} = t_{RAS} (min) to 1 µs

    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V

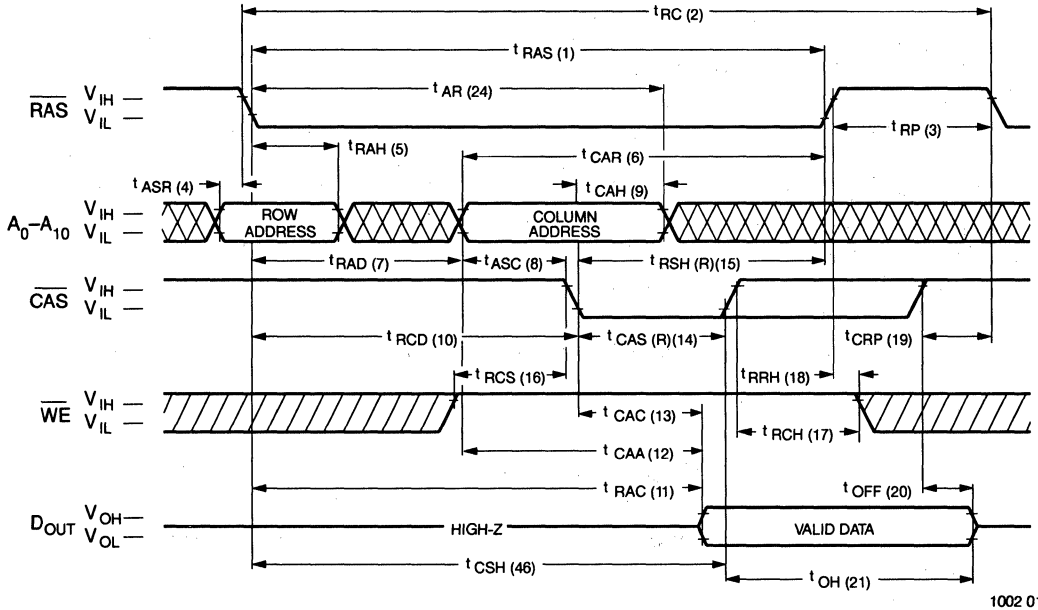
    $V_{IL} < 0.2$ V

    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V

    All other inputs at stable V_{IH} or V_{IL}
20. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$-before-$\overline{RAS}$ cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is 8-bits parallel testing function.

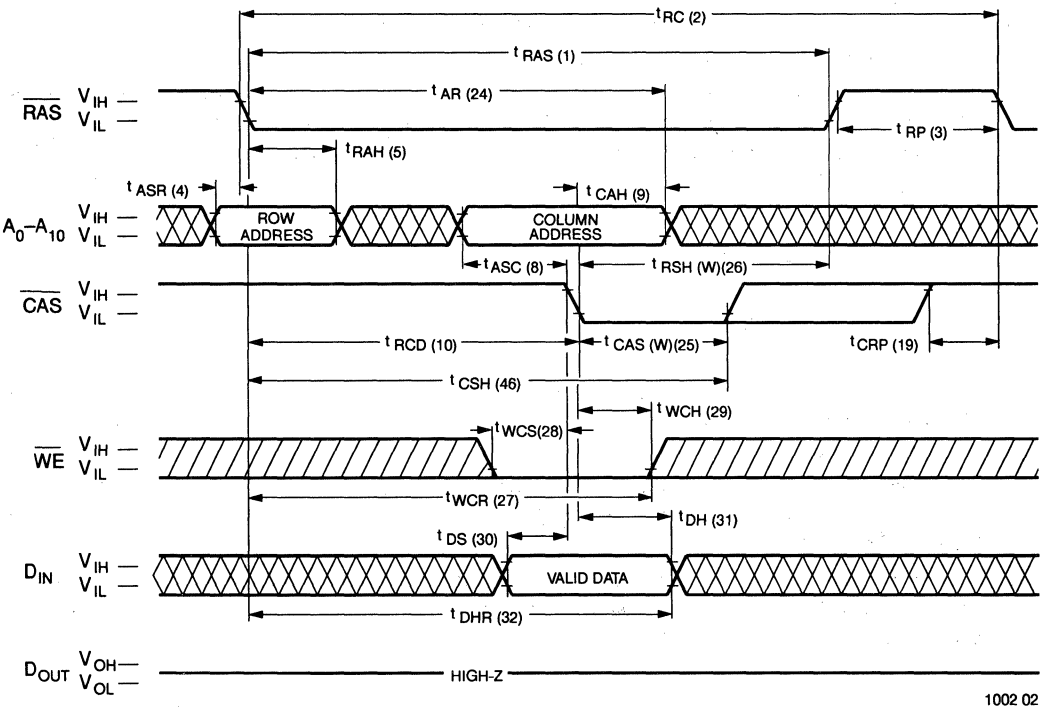
    RA_{10}, CA_{10}, CA_0 are not used. In the read cycle, if two internal bits on one I/O pin are equal, the I/O pin will indicate a high level. If internal bits on one I/O are not equal, then the I/O pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
21. In a test mode read cycle, the value of access time parameters is delayed by 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value (5 ns) to the specified value in this data sheet.

Waveforms of Read Cycle



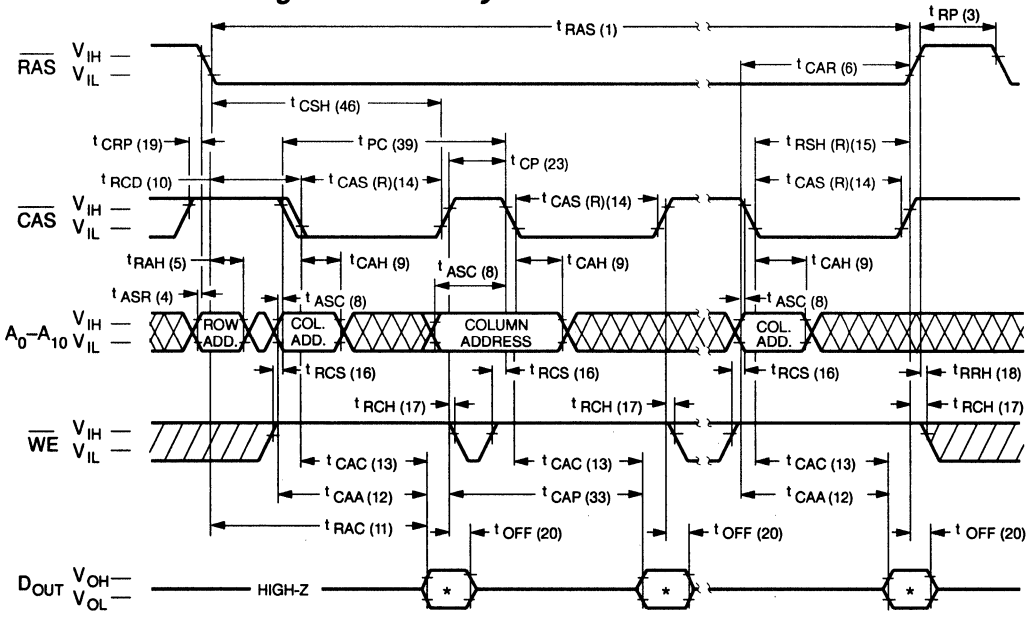
1002 01

Waveforms of Early Write Cycle



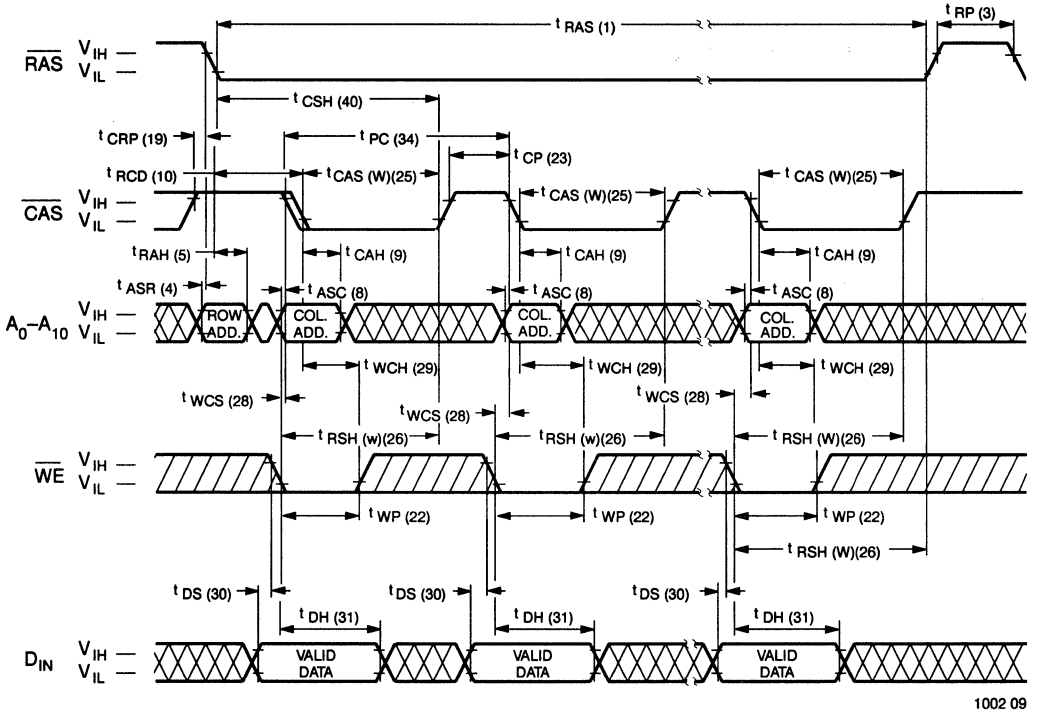
1002 02

Waveforms of Fast Page Mode Read Cycle

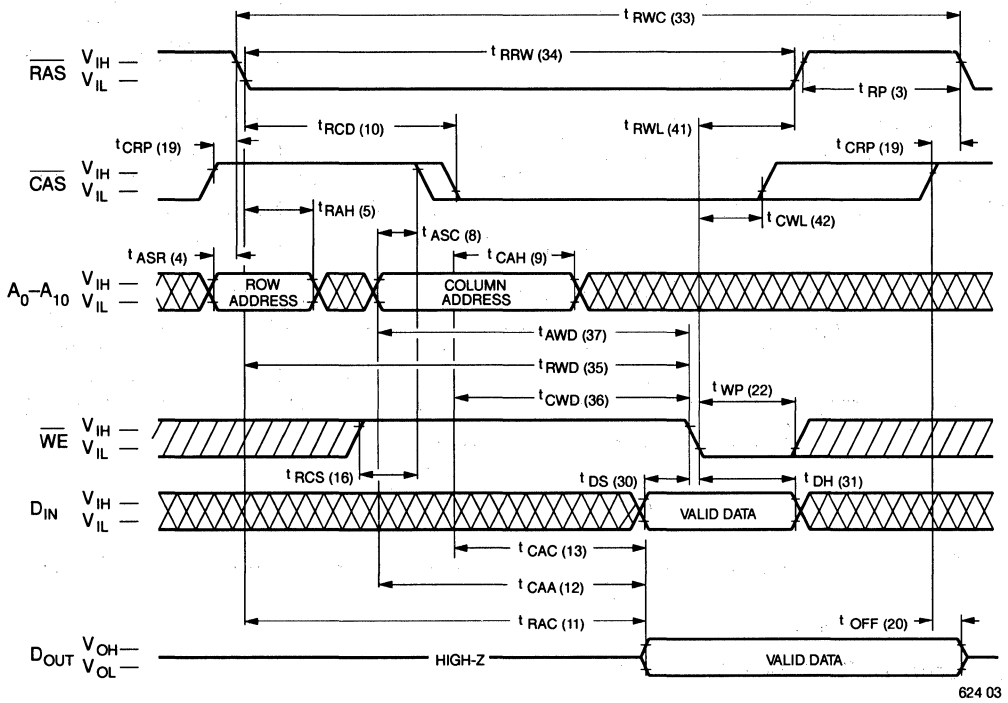


* Valid Data

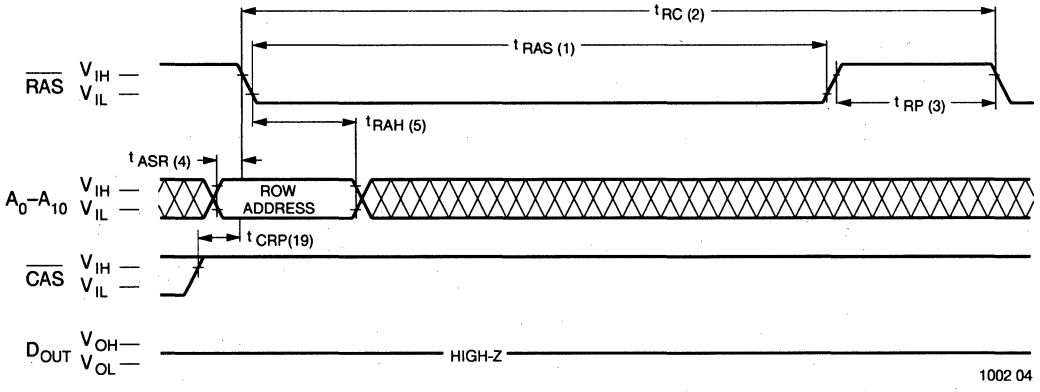
Waveforms of Fast Page Mode Write Cycle



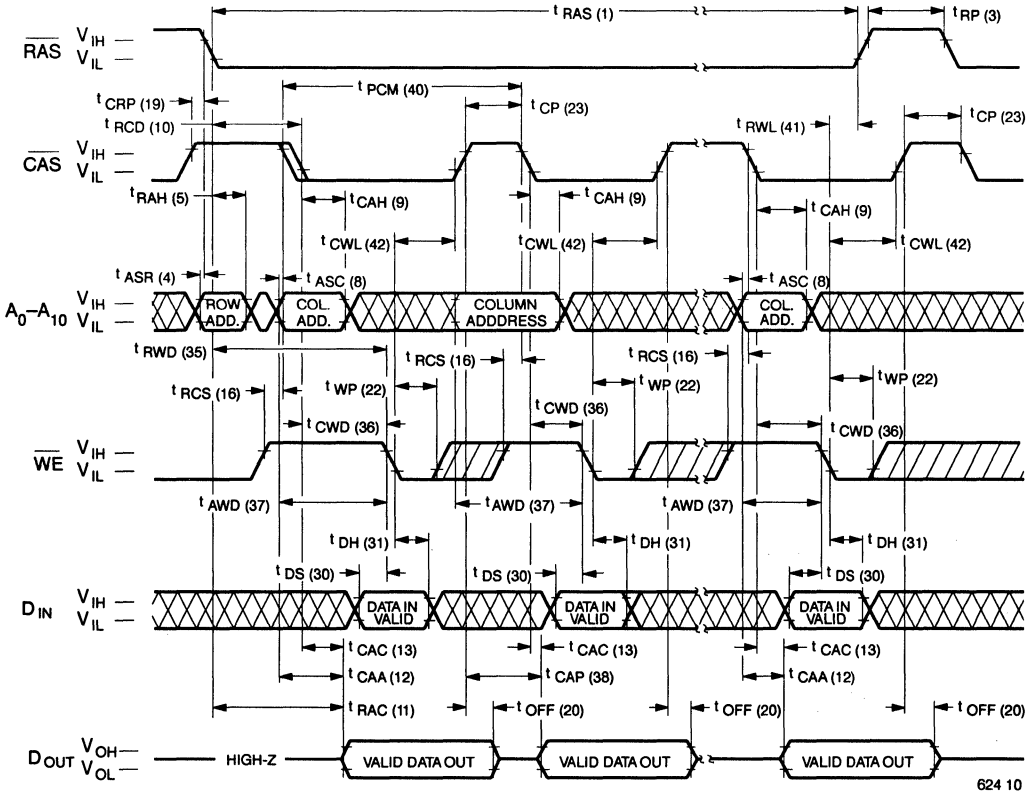
Waveforms of Read-Modify-Write Cycle



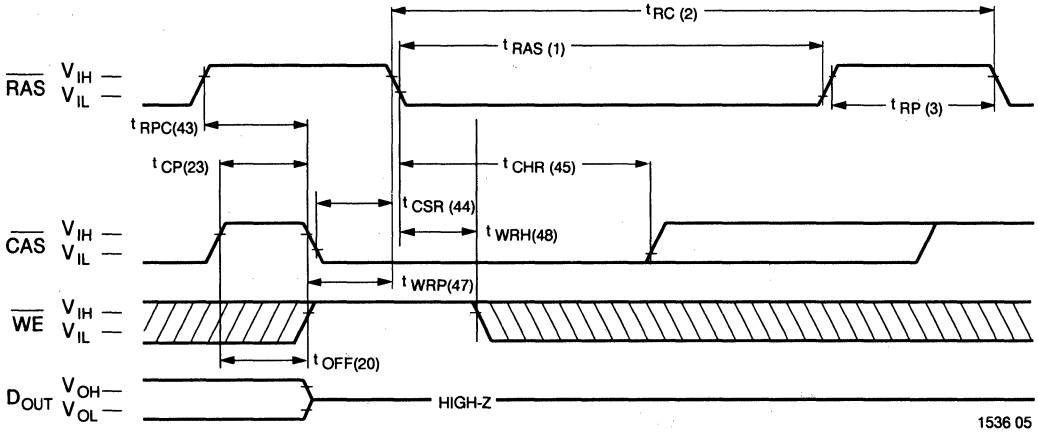
Waveforms of $\overline{RAS}$-Only Refresh Cycle



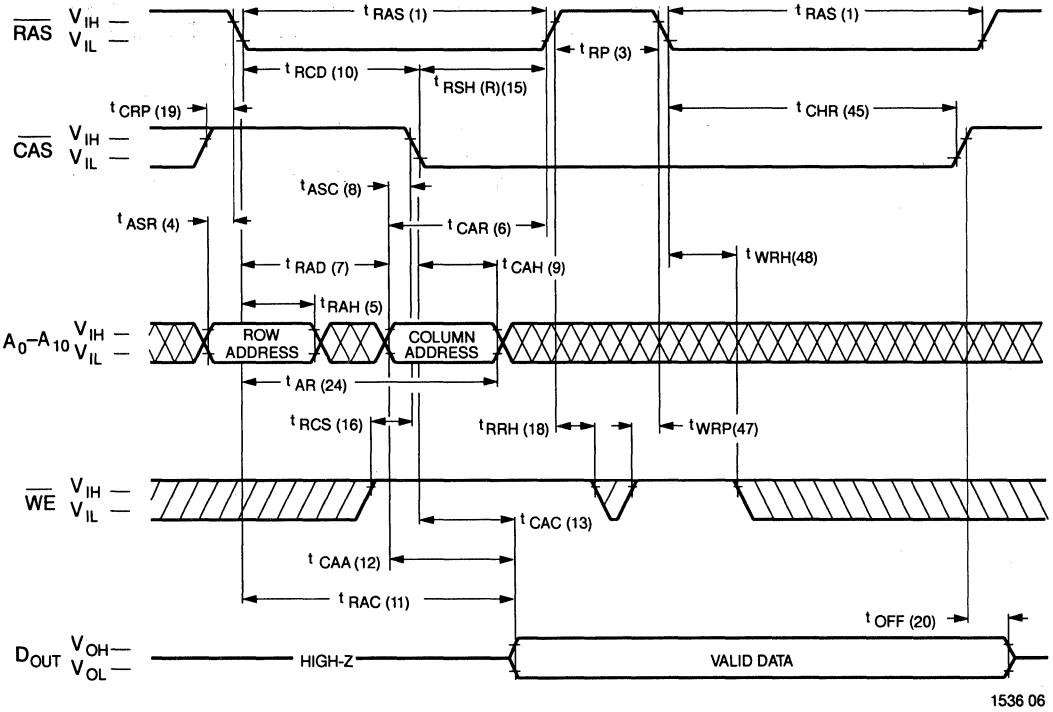
Waveforms of Fast Page Mode Read-Modify-Write Cycle



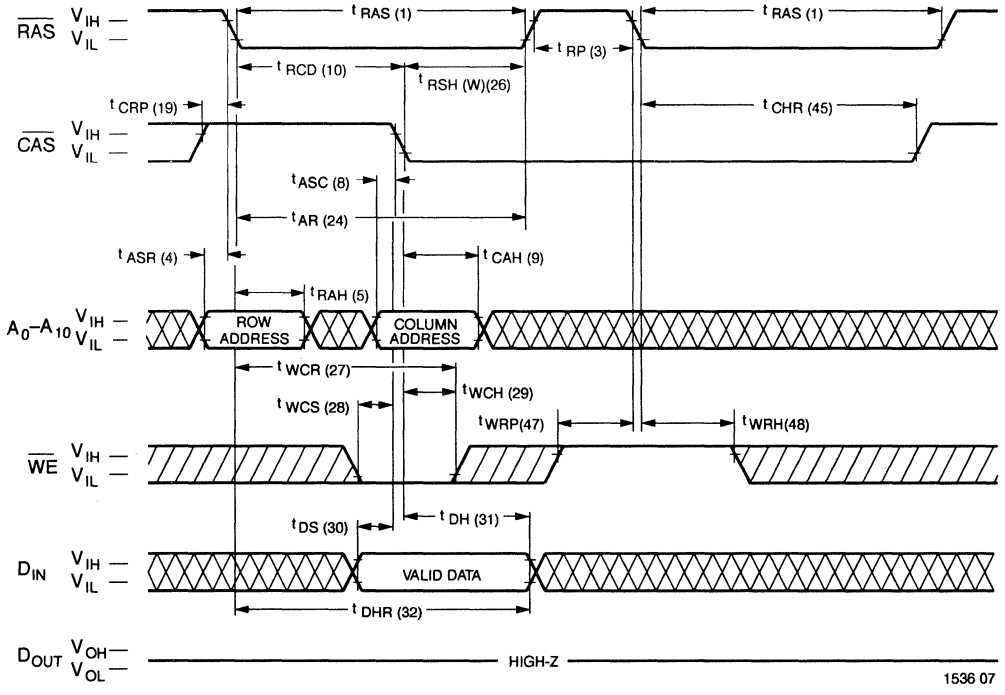
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



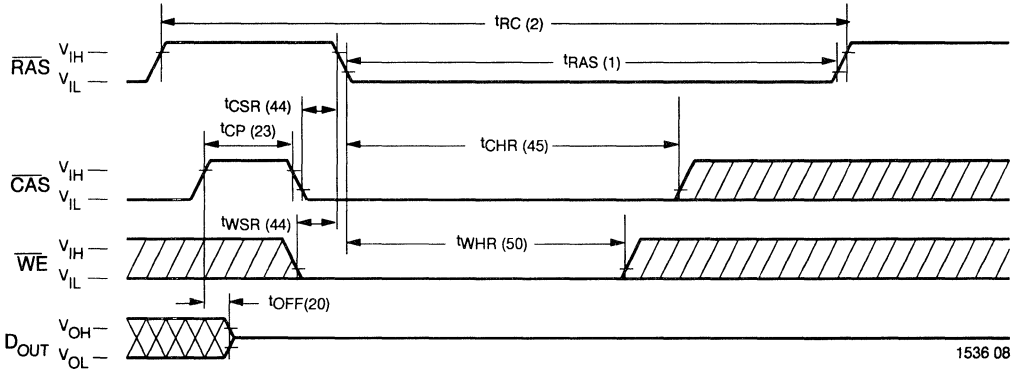
Waveforms of Hidden Refresh Cycle (Read)



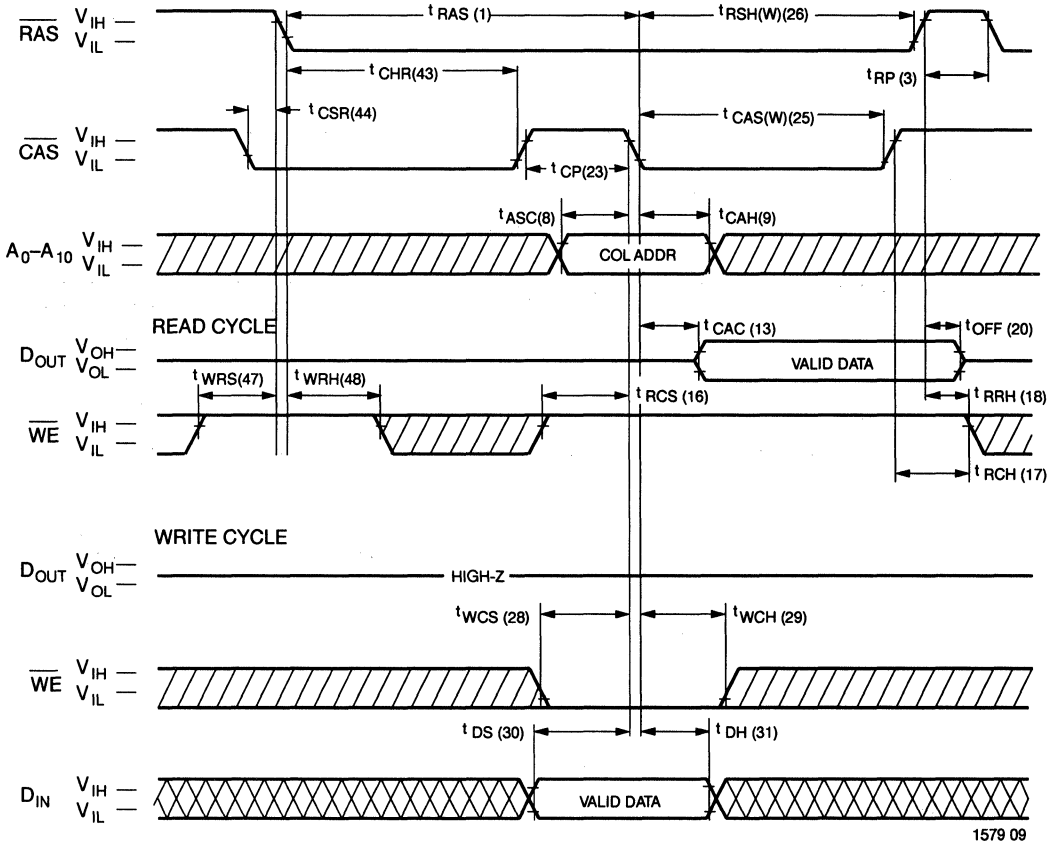
Waveforms of Hidden Refresh Cycle (Write)



Test Mode Initiation Cycle



Waveforms of $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C400F is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C400F reads and writes data by multiplexing a 22-bit address into an 11-bit row and an 11-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} (min.) and t_{CAC} (min.) are both satisfied.

Write Cycle

A Write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the output (D_{OUT}) pin will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

Refresh Cycle

To retain data, 1024 Refresh Cycles are required in each 16 ms period. There are two ways to Refresh the memory:

1. By selecting all 1024 address combinations of A0 through A9 each 16 ms, a refresh of all rows is completed. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C400 will use the output of an internal 10-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, D_{OUT} will remain in the High-Z state during the cycle.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to write consecutive data patterns (1024 Write cycles) and then verify the written data by applying 1024 consecutive Read cycles. In this mode, the V53C400F ignores external row/column addresses and takes the output from the internal counter instead.

Data Retention Mode

The V53C400F offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C400F power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 1024

Fast Page Mode Operation

Fast Page Mode operation permits all 2048 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high.

Thus, access begins at the occurance of a valid column address rather than at the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as on output enable.

During Fast Page Mode operation, Read, Write, Read-Modify-Write, or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is determined by the by the $\overline{CAS}$ rising edge. If the column address is valid after the rising edge of $\overline{CAS}$, the access is timed from the occurrance of the valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 20 MHz for applications that require high data rates like bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{2{,}048}{t_{RC} + 2{,}047 \times t_{PC}}$$

Data Output Operation

The V53C400F Data Output pin (D_{OUT}) has a three-state capability and is controlled by $\overline{CAS}$. When $\overline{CAS}$ is high($\geq V_{IH}$), the output is in the High-Z state. Table 1 summarizes the D_{OUT} states possible for various memory cycles.

Power On

After application of the V_{DD} an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval). During power on, the V_{DD} current requirement of the V53C400F is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on to avoid current surges.

Table 1. V53C400F Data Output
Operation for Various Cycle Types

Cycle Type	D_{OUT} State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	Active, not valid
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

HIGH PERFORMANCE, LOW POWER 1M X 4 BIT FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE V53C404F	60/60L	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns	65 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns	180 ns

LOW POWER V53C404FL	60L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	0.4 mA	0.4 mA	0.4 mA	0.4 mA

2

Features

- 1M x 4-bit organization
- RAS access time: 60,70,80,100 ns
- Low power dissipation
  - V53C404F-10
    - — Operating Current – 65 mA max.
    - — TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C404F – 1.0 mA max.
  - V53C404FL – 0.4 mA max.
- Battery Back-up Mode (V53C404FL Only)
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V53C404F – 1024 cycles/16ms
  - V53C404FL – 1024 cycles/64ms
- On-chip substrate bias generator
- Fast Page Mode for a sustained data rate greater than 20 MHz
- Available in 26/20 pin SOJ package (300 mil)

Description

The V53C404F is a high speed 1,048,576x4 bit CMOS dynamic random access memory. The V53C404F offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C404FL).

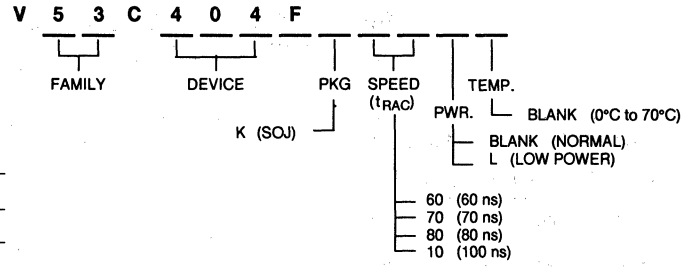
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 1024 (x4) bits within a row with cycle times as short as 50 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C404F ideally suited for main memories, graphics, digital signal processing and high performance computing systems.

The V53C404FL offers a maximum data retention power of 5.5 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

Device Usage Chart

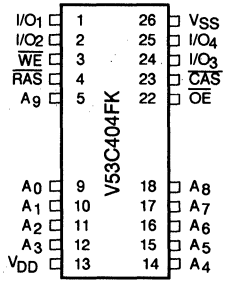
Operating Temperature Range	Package Outline	Access Time (ns)				Power		Temperature Mark
	K	60	70	80	100	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank

V53C404F Rev. 0.01 February1993



Description	Pkg.	Pin Count
SOJ	K	26/20

26/20 Lead SOJ Package PIN CONFIGURATION Top View



Pin Names

A_0–A_9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_4	Data Input, Output
V_{DD}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 V to +7.0 V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

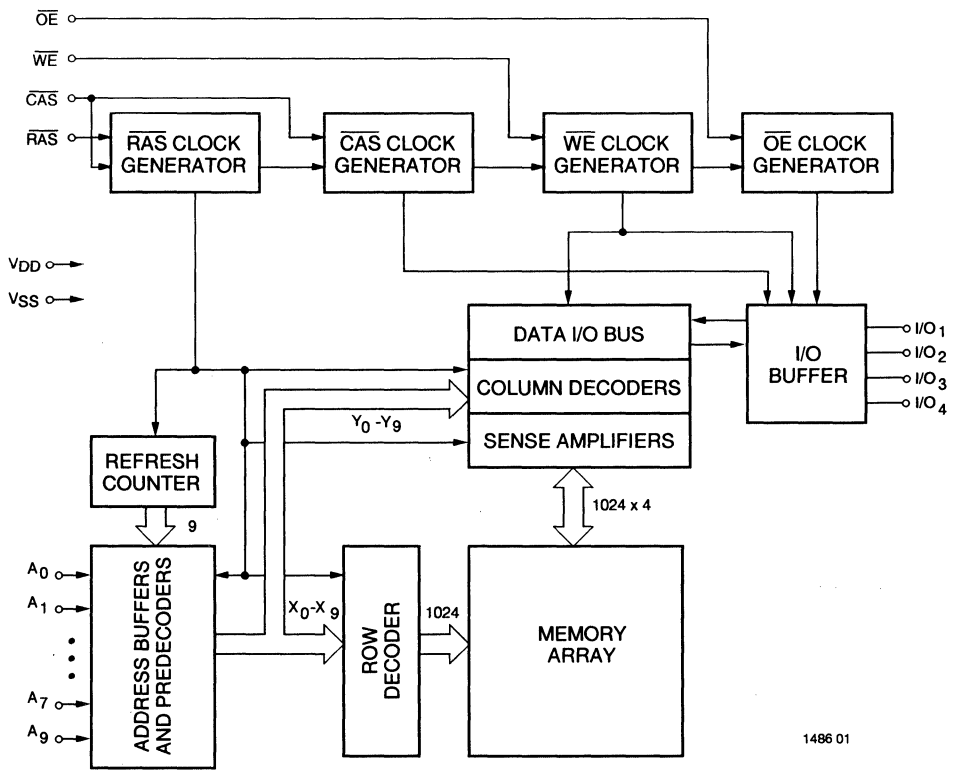
T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram

1M x 4



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C404F		V53C404FL		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		−10	10	−10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		−10	10	−10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	60		110		110	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		70		100		100			
		80		90		90			
		100		65		65			
I_{DD2}	V_{DD} Supply Current, TTL Standby			2.0		2.0	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	60		95		95	mA	$t_{RC} = t_{RC}$ (min.)	2
		70		85		85			
		80		75		75			
		100		65		65			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	60		95		95	mA	Minimum Cycle	1, 2
		70		85		85			
		80		75		75			
		100		65		65			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			5		4	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	
I_{DD6}	V_{DD} Supply Current, CMOS Standby			1		0.4	mA	$\overline{RAS} \ge V_{DD}$ − 0.2 V $\overline{CAS} \ge V_{DD}$ − 0.2V other inputs ≥ V_{SS}	
I_{DD7}	Battery Back-up Data Retention Current (Only V53C404FL)			N.A.		0.6	mA	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle t_{RC} = 62.5 µs CMOS clock levels	18
V_{IL}	Input Low Voltage		−1.0	0.8	−1.0	0.8	V		3
V_{IH}	Input High Voltage		2.4	V_{DD}+1	2.4	V_{DD}+1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4			I_{OH} = −5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted
AC Test Conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL}	t_{RC}	Read or Write Cycle Time	120		130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		70		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	15		20		20		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20		20		20	60	25	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15		20		20		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time (Referenced to $\overline{CAS}$)	0		0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time (Referenced to $\overline{RAS}$)	0		0		0		0		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		10		20		25		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		15		20		20		25	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		15		20		20		25	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40		50	ns	6,7,10
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0	20	0	20	0	25	0	25	ns	16

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		75		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	30	15	40	20	50	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	15		20		20		25		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		25		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		15		15		20		ns	
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		15		20		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		75		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		25		ns	
32	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data In Hold Time	15		15		15		20		ns	14
34	$t_{WLG1GL2}$	t_{WOH}	Write to $\overline{OE}$ Hold Time	15		20		20		25		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	15		20		20		25		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	170		185		205		245		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	105		125		135		165		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	40		50		50		60		ns	12
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	85		100		110		135		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	65		75		75		90		ns	
41	t_{AVWL2}	t_{AWD}	Column Address to $\overline{WE}$ Delay	60		65		70		80		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		65		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		40		50		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		35		40		45		55	ns	7

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
46	t_{RL1DX2}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	50		55		60		75		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	5		5		5		5		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5		5		5		5		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	15		15		15		15		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	95		100		110		130		ns	
51	t_{WH2RL2}	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle)	10		10		10		10		ns	
52	t_{RL1WL2}	t_{WRH}	$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	10		10		10		10		ns	
53	t_{WL1RL2}	t_{WSR}	$\overline{RAS}$ to $\overline{WE}$ set-up Time (Test Mode)	10		10		10		10		ns	19,20
54	t_{RL1WH1}	t_{WHR}	$\overline{RAS}$ to $\overline{WE}$ hold Time (Test Mode)	10		10		10		10		ns	
55	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
56		t_{REF}	Refresh Interval (1024 Cycles)		16		16		16		16	ms	17
57		t_{REF}	Refresh Interval V53C404FL Only (1024 Cycles, t_{RC} = 62.5 µs)		64		64		64		64	ms	17,18

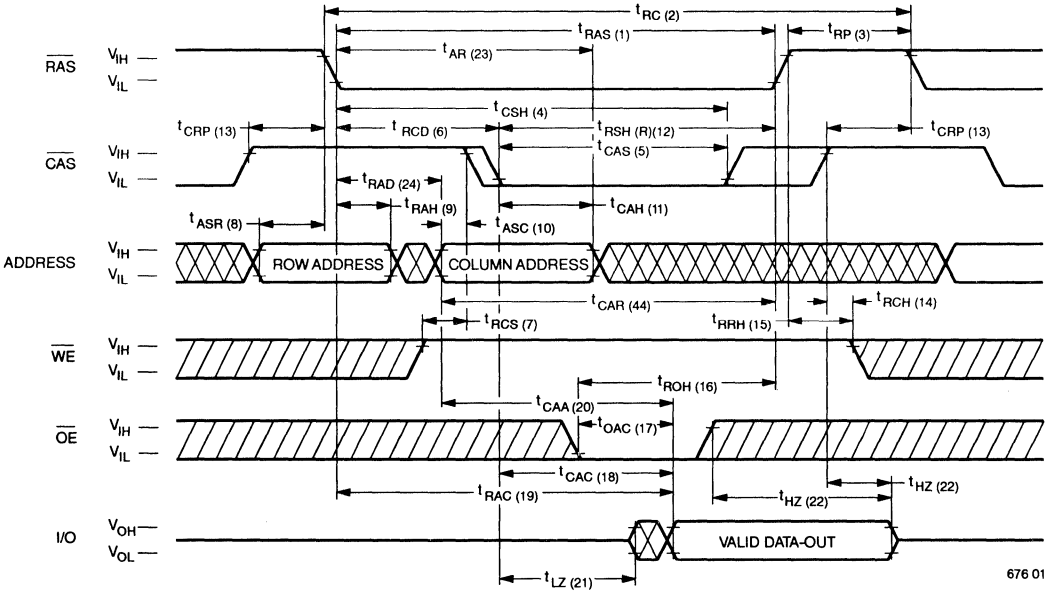
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
    t_{RC} = 62.5 µs (62.5 µs x 1024 = 64 ms)
    $t_{RAS} = t_{RAS}$ (min) to 1 µs
    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V
    $V_{IL} < 0.2$ V
    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V
    All other inputs at stable V_{IH} or V_{IL}
19. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$-before-$\overline{RAS}$ cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is 8-bits parallel testing function.

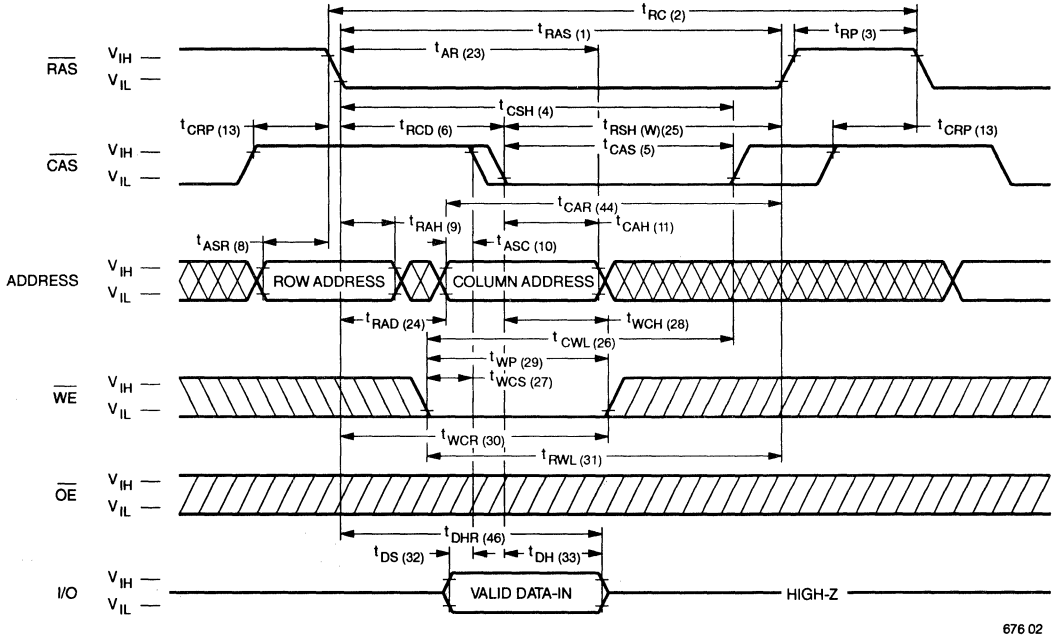
    CA0 is not used. In the read cycle, if two internal bits on one I/O pin are equal, the I/O pin will indicate a high level. If internal bits on one I/O are not equal, then the I/O pin will indicate a low level.

    The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
20. In a test mode read cycle, the value of access time parameters is delayed by 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value (5 ns) to the specified value in this data sheet.

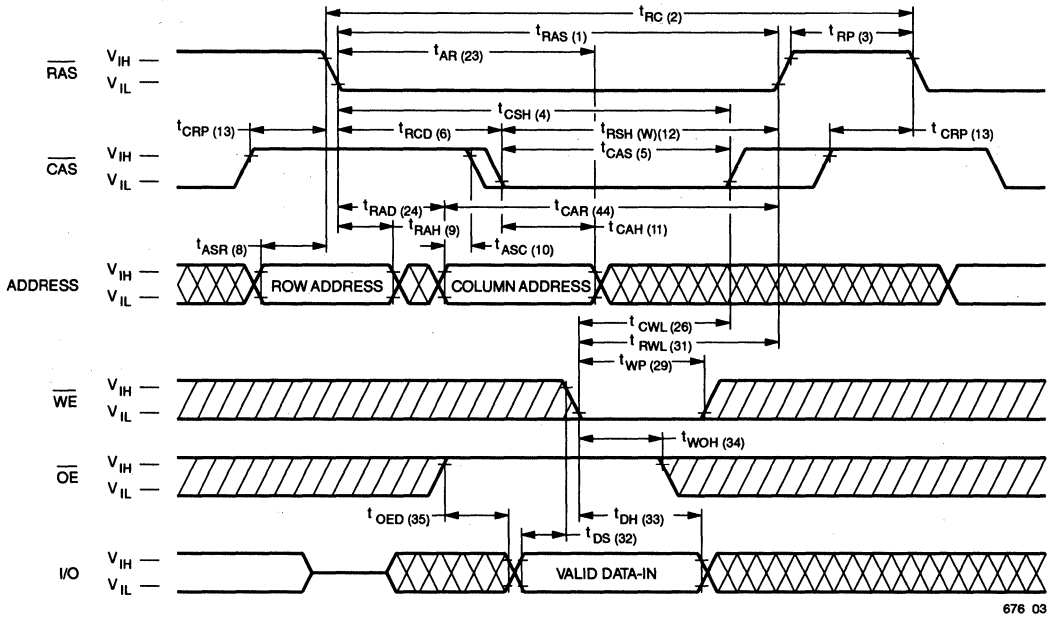
Waveforms of Read Cycle



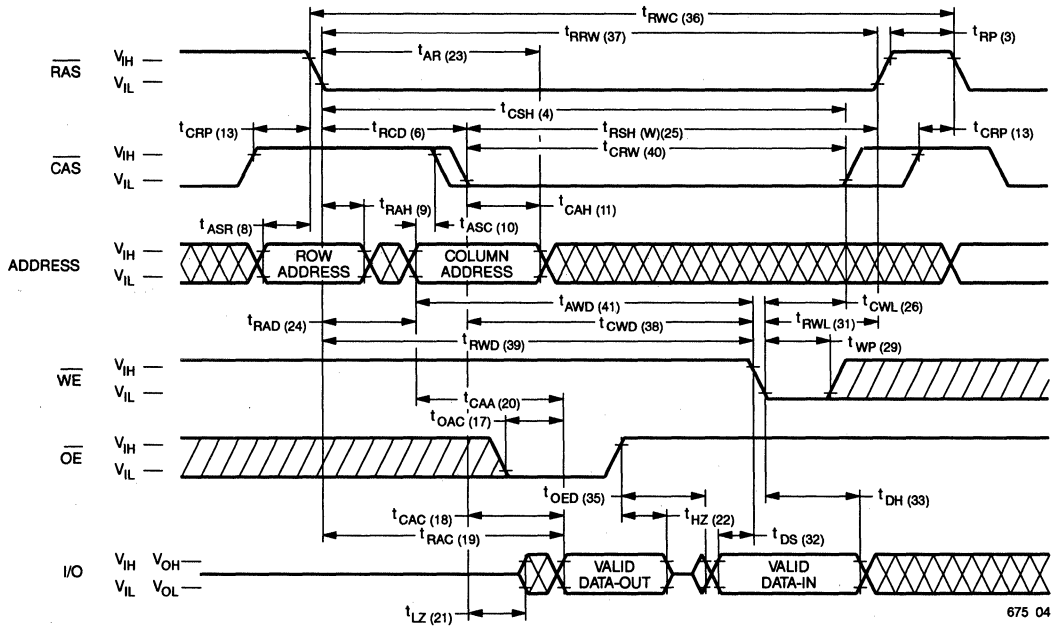
Waveforms of Early Write Cycle



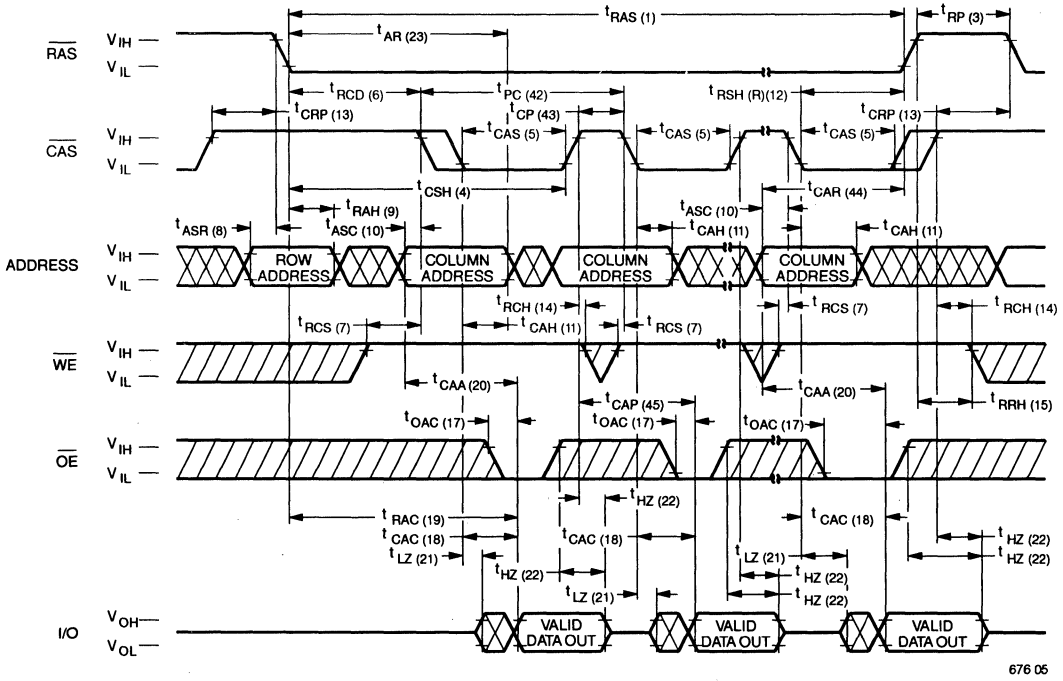
Waveforms of $\overline{OE}$-Controlled Write Cycle



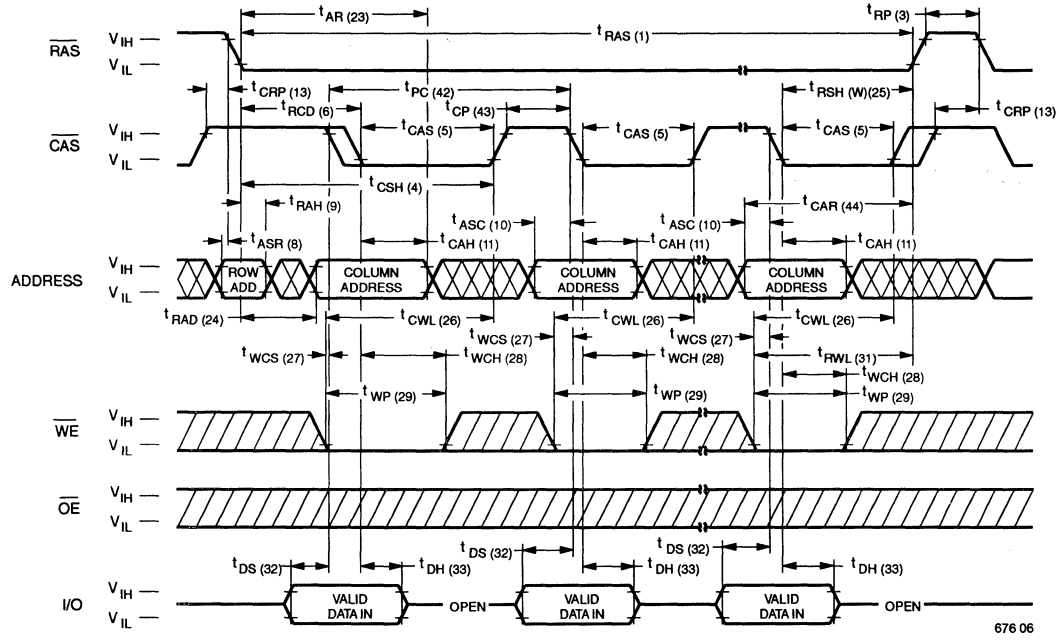
Waveforms of Read-Modify-Write Cycle



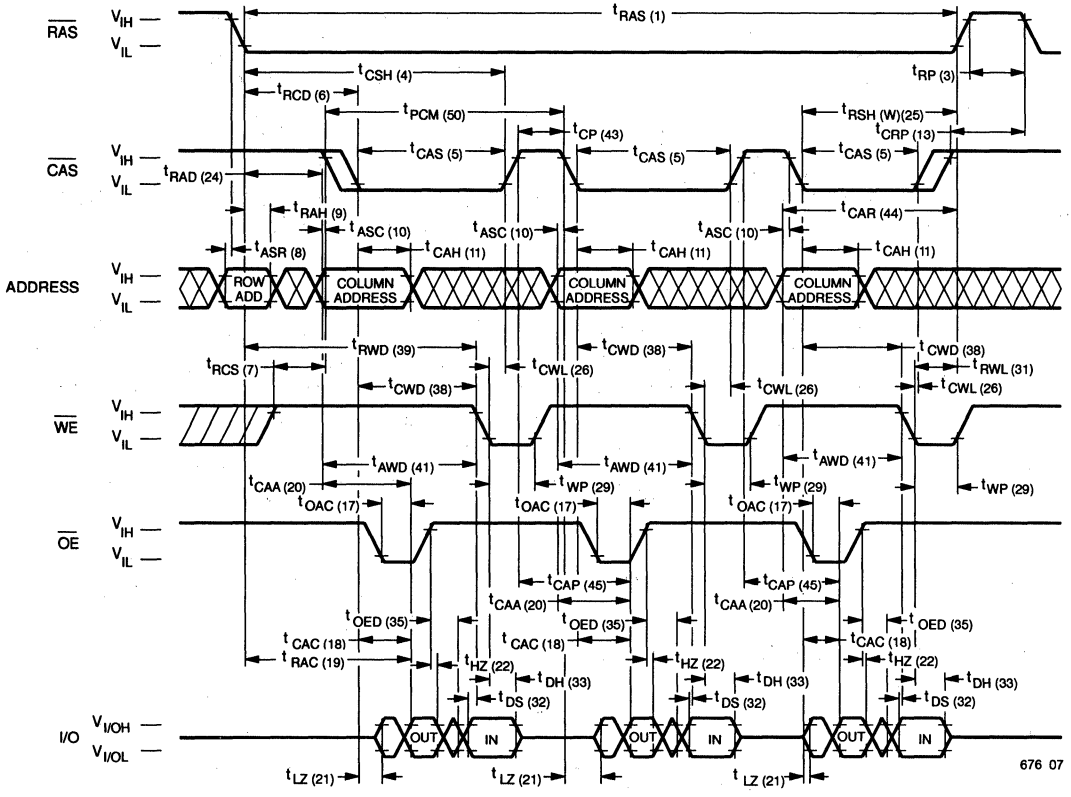
Waveforms of Fast Page Mode Read Cycle



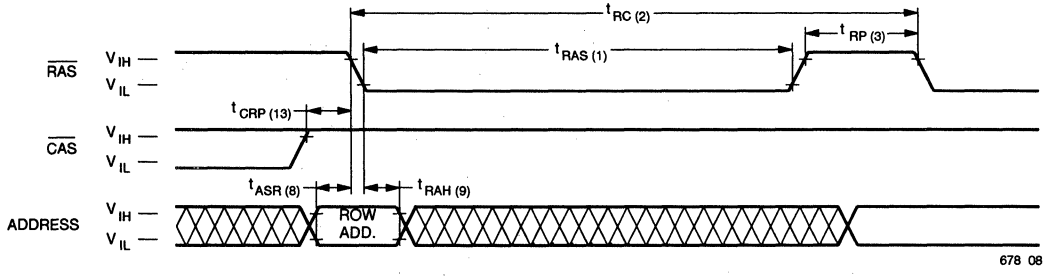
Waveforms of Fast Page Mode Write Cycle



Waveforms of Fast Page Mode Read-Write Cycle

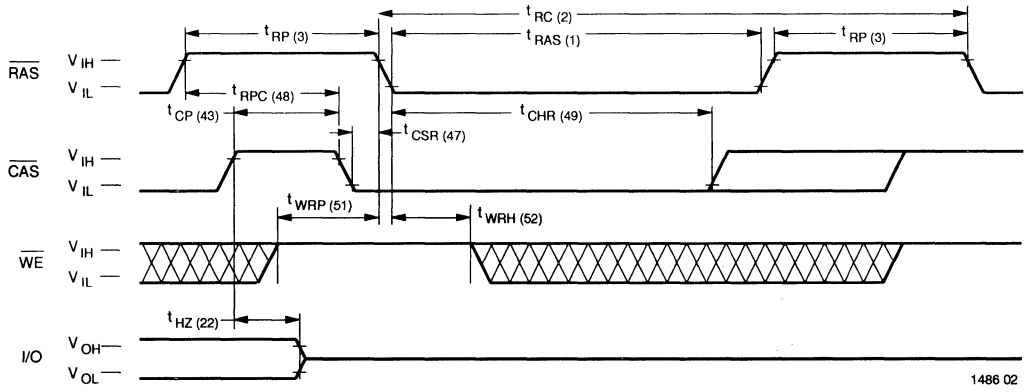


Waveforms of $\overline{RAS}$-Only Refresh Cycle



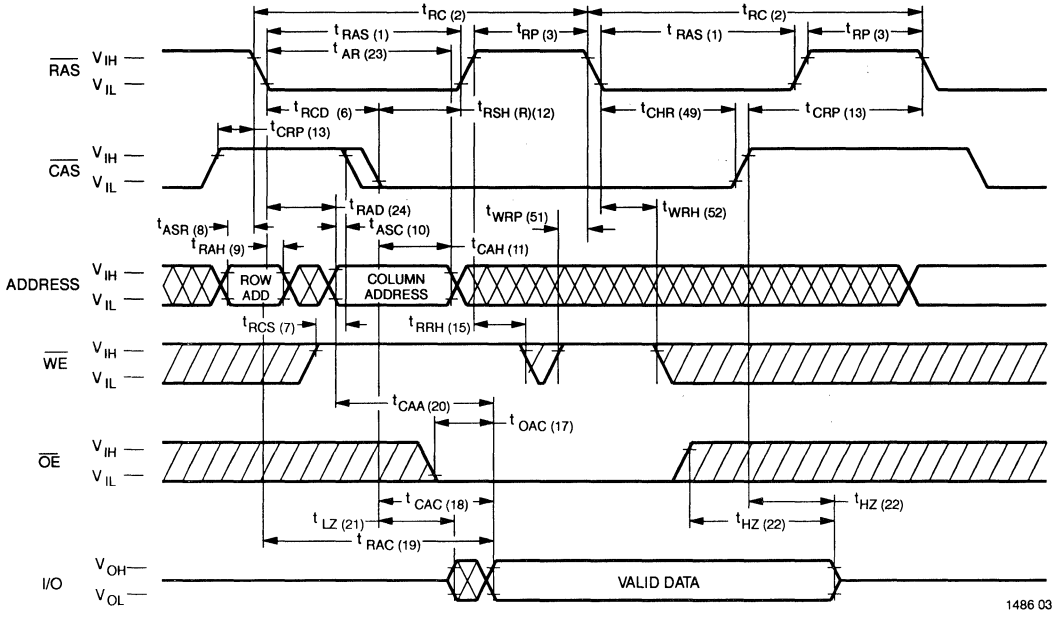
NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

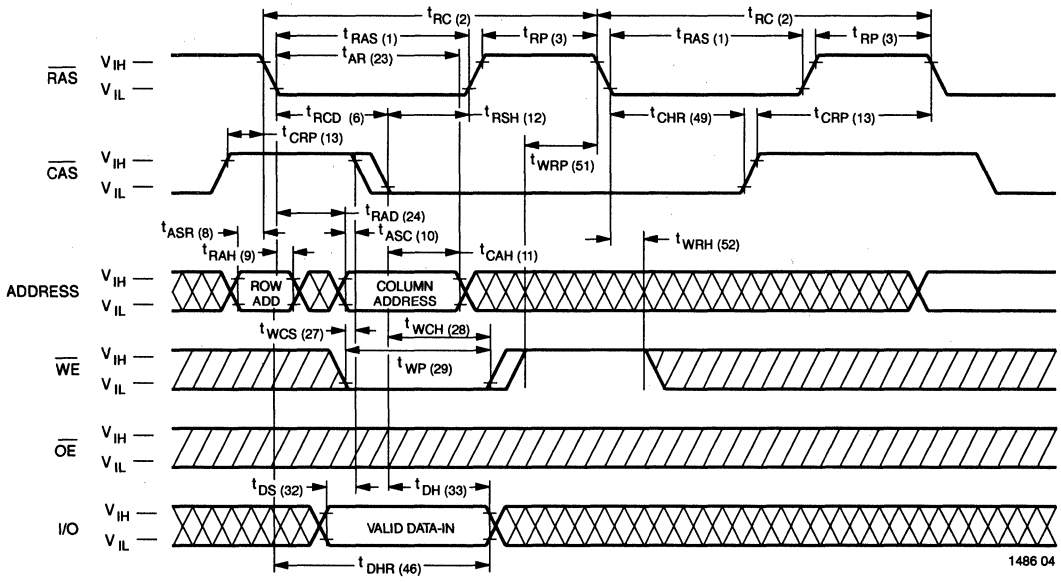


NOTE: $\overline{WE}$, $\overline{OE}$, A_0–A_7 = Don't care

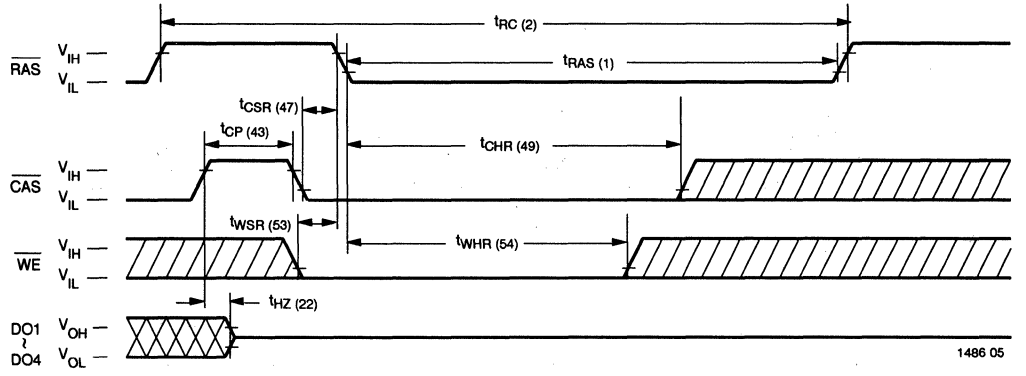
Waveforms of Hidden Refresh Cycle (Read)



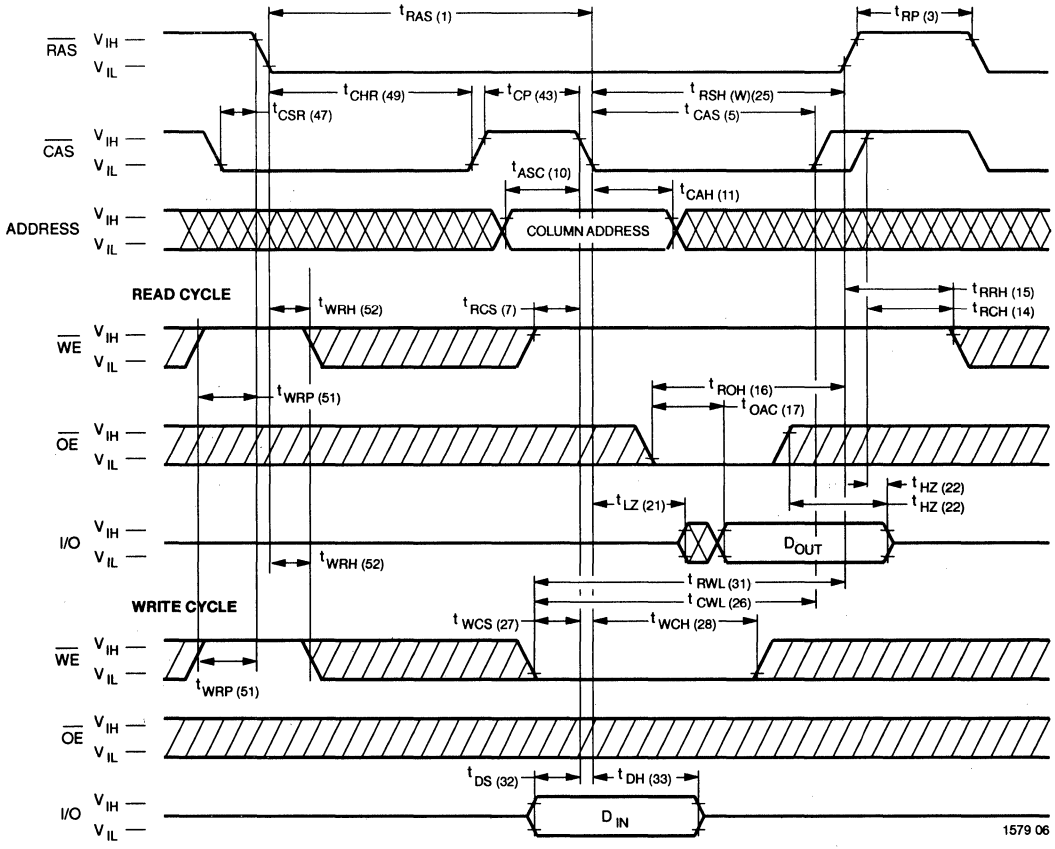
Waveforms of Hidden Refresh Cycle (Write)



Test Mode Initiation Cycle



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C404F is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C404F reads and writes data by multiplexing an 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 1024 Refresh Cycles are required in each 16 ms period. There are two ways to refresh the memory:

1. By clocking each of the 1024 row addresses (A_0 through A_9) with $\overline{RAS}$ at least once every 16 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C404F uses the output of an internal 10-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C404F offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C404 power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 1024

Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 18 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

Data Output Operation

The V53C404F Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C404F is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C404F Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

HIGH PERFORMANCE V53C405	60/60L	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns	65 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns	180 ns

LOW POWER V53C405L	60L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	0.4 mA	0.4 mA	0.4 mA	0.4 mA

Features

- 1M x 4-bit 4 $\overline{CAS}$ organization
- RAS access time: 60,70,80,100 ns
- Low power dissipation
  - V53C405-10
    - — Operating Current – 65 mA max.
    - — TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C405 – 1.0 mA max.
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V53C405 – 1024 cycles/16ms
  - V53C405L – 1024 cycles/64ms
- Fast Page Mode for a sustained data rate greater than 20 MHz
- Available in 26/24 pin SOJ package (300 mil)

Description

The V53C405 is a high speed 1,048,576x4 bit CMOS dynamic random access memory. The V53C405 offers 4 $\overline{CAS}$ inputs, in addition to: Fast Page Mode for high data bandwidth, low CMOS standby current and, on request, extended refresh for very low data retention power (V53C405L).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 1024 (x4) bits within a row with cycle times as short as 45 ns. These features make the V53C405 ideally suited for parity bits for the SIMM module and parity memory for the main memories, graphics, digital signal processing and high performance computing systems.

The V53C405L offers a maximum data retention power of 5.5 mW when operating in CMOS standby mode and performing $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)				Power		Temperature Mark
	K	60	70	80	100	Low	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank

V53C405 Rev. 00 March 1993

V53C8512/V53C9512
HIGH PERFORMANCE, LOW POWER
512K x 8 AND 512K x 9 BIT
FAST PAGE MODE
CMOS DYNAMIC RAM

PRELIMINARY

HIGH PERFORMANCE V53C8512/V53C9512	50/50L	60/60L	70/70L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	50 ns	60 ns	70 ns
Max. Column Address Access Time, (t_{CAA})	25 ns	30 ns	35 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	35 ns	40 ns	45 ns
Min. Read/Write Cycle Time, (t_{RC})	110 ns	120 ns	130 ns

LOW POWER V53C8512L/V53C9512L	50L	60L	70L
Max. CMOS Standby Current, (I_{DD6})	0.15 mA	0.15 mA	0.15 mA

Features

- 512K x 8 and 512K x 9 Organization
- RAS access time: 50, 60, 70 ns
- Low power dissipation for V53C8512/9512
  - Operating Current – 105 mA max.
  - TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C8512/9512 – 5 mA max.
  - V53C8512L/9512L – 0.15 mA max.
- Read-Modify-Write, RAS-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Common I/O capability
- Refresh Interval
  - V53C8512/9512 – 1024 cycles/16 ms
  - V53C8512L/9512L – 1024 cycles/16 ms
- On-chip substrate bias generator
- Fast Page Mode for a sustained data rate greater than 28 MHz
- Standard package is 28 pin 400 mil SOJ

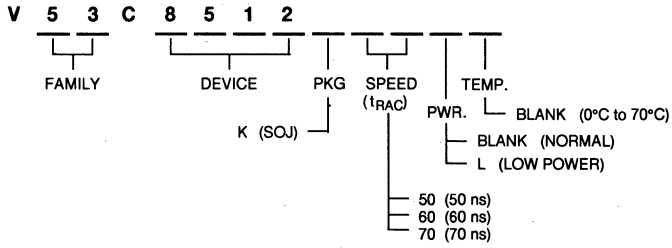
Description

The V53C8512 is a 524,288 x 8 and the V53C9512 is a 524,288 x 9 bit high speed CMOS dynamic random access memory. The V53C8512 and V53C9512 offer a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C8512L and V53C9512L).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x8) bits within a row with cycle times as short as 35 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C8512 and V53C9512 ideally suited for graphics, digital signal processing and high performance computing systems.

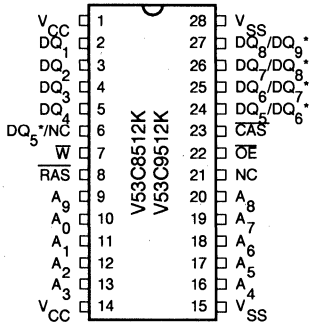
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)			Power		Temperature Mark
	K	50	60	70	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	Blank



Description	Pkg.	Pin Count
SOJ	K	28

28 Lead SOJ Package PIN CONFIGURATION Top View



*for the V53C9512

Pin Names

A_0–A_9	Address Inputs
DQ_1–DQ_9	Data In/Out
V_{SS}	Ground
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
V_{CC}	Power (+5V)
NC	No Connection

Absolute Maximum Ratings*

Parameter	Rating	Units
Ambient Temperature Under Bias	–10 to +80	°C
Storage Temperature (plastic)	–55 to +125	°C
Voltage Relative to V_{SS}	–1.0 to +7.0	V
Voltage on V_{DD} relative to V_{SS}	–1.0 to +7.0	V
Data Output Current	50	mA
Power Dissipation	700	mW

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

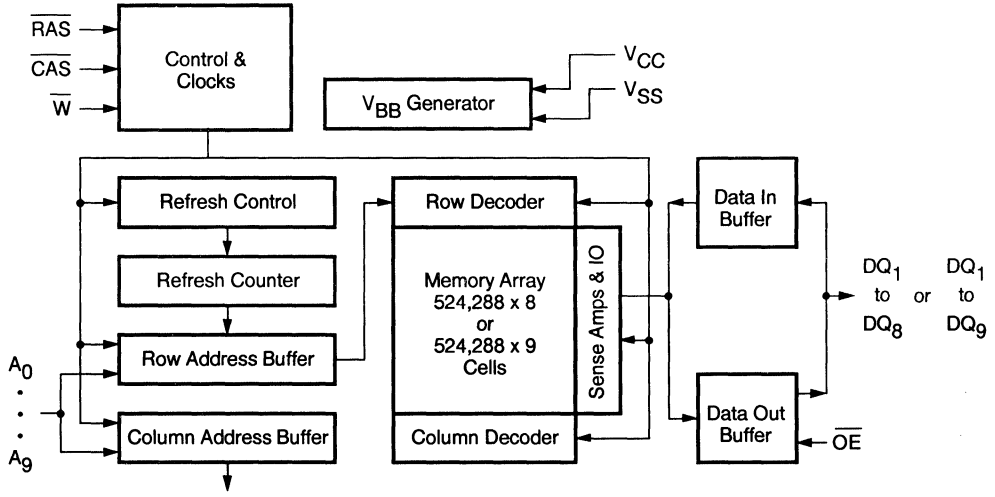
Capacitance*

T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	—	6	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$	—	7	pF
C_{OUT}	Data Input/Output	—	7	pF

*Note: Capacitance is sampled and not 100% tested.

Block Diagram



DC and Operating Characteristics (1, 2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C8512/9512		V53C8512L/9512L		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10	10	–10	10	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10	10	–10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	50		120		120	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		60		110		110			
		70		105		105			
I_{DD2}	V_{DD} Supply Current, TTL Standby			2.0		2.0	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh	50		120		120	mA	$t_{RC} = t_{RC}$ (min.)	2
		60		110		110			
		70		105		105			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation	50		95		95	mA	Minimum Cycle	1, 2
		60		90		90			
		70		85		85			
I_{DD5}	Standby, Output Enabled			5.0		5.0	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current CMOS Standby			1.0		0.15	mA	$\overline{RAS}$ ≥ V_{DD} –0.2 V, $\overline{CAS}$ ≥ V_{DD} -0.2 V other input ≥ V_{SS}	
V_{IL}	Input Low Voltage		–1.0	0.8	–1.0	0.8	V		3
V_{IL}	Input High Voltage		2.4	V_{DD}+1	2.4	V_{DD}+1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL}= 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4			I_{OH} = -5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	50/L		60/L		70/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	50	10K	60	10K	70	10K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	110		120		130		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	40		45		50		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	50		60		70		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	12	10K	15	10K	20	10K	ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	18	38	19	45	20	50	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	8		9		10		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	8		9		10		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	12		15		20		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	10		15		20		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		12		15		20	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		12		15		20	ns	6,7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		50		60		70	ns	6,8,9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		25		30		35	ns	6,7,10
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	10	0	10	0	10	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	45		50		55		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	13	25	14	30	15	35	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH\ (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	12		15		20		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	12		15		20		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	8		9		10		ns	

AC Characteristics (Cont'd)

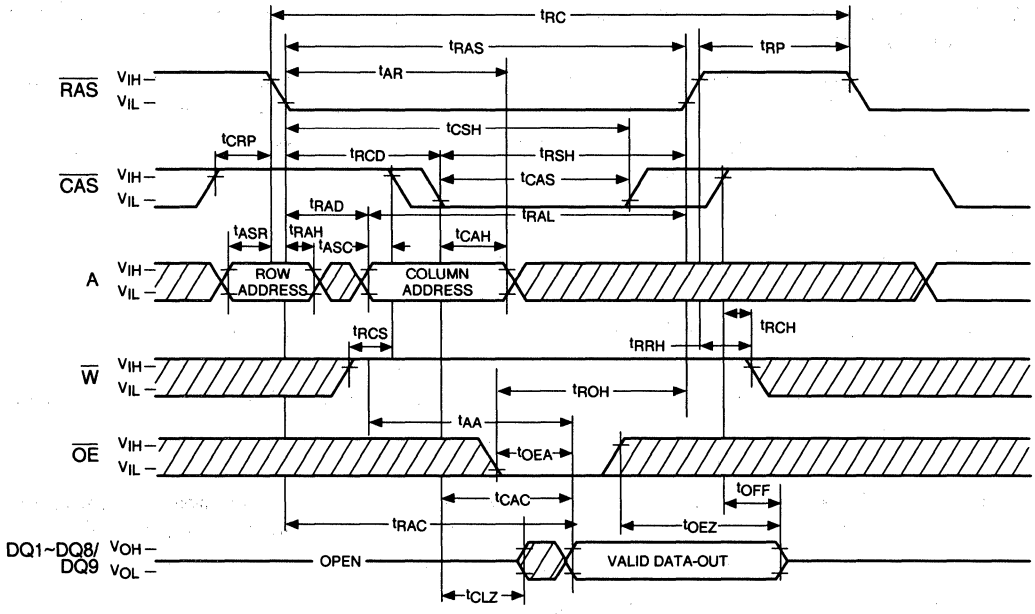
#	JEDEC Symbol	Symbol	Parameter	50/L		60/L		70/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	8		9		10		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	45		50		55		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	12		15		20		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	8		9		10		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	10		15		20		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	10		10		15		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	160		170		180		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	110		115		120		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	35		40		50		ns	12
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	80		90		100		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	55		65		75		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	50		55		60		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	35		40		45		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	25		30		35		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		30		35		40	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	45		50		55		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	20		20		20		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	80		90		100		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{REF}	Refresh Interval (1024 Cycles)		16		16		16	ms	17

Notes

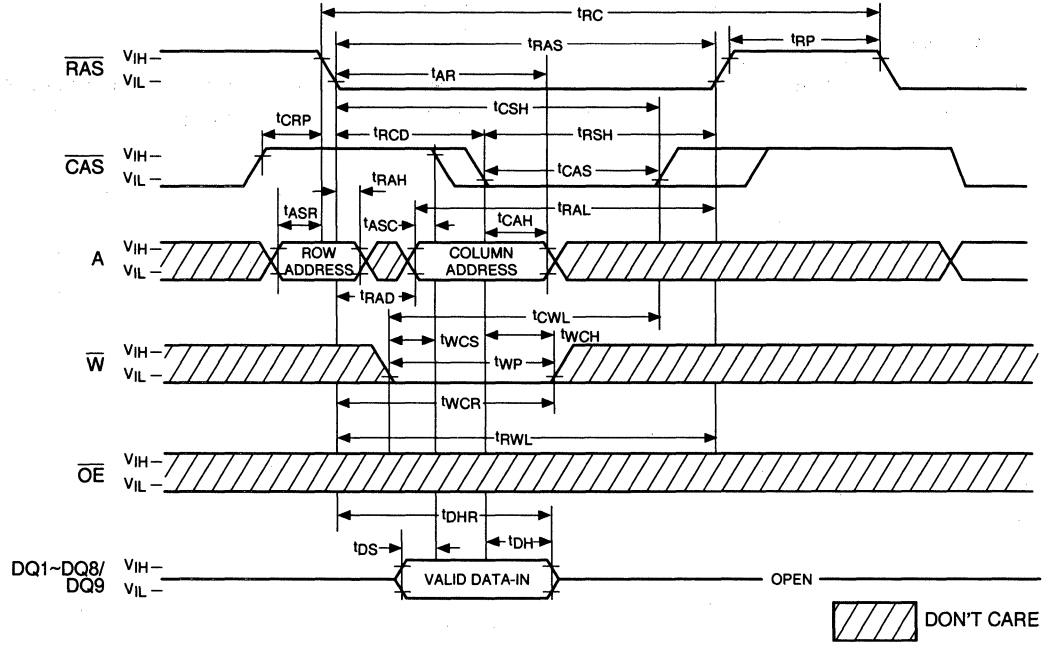
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to −1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

TIMING DIAGRAMS

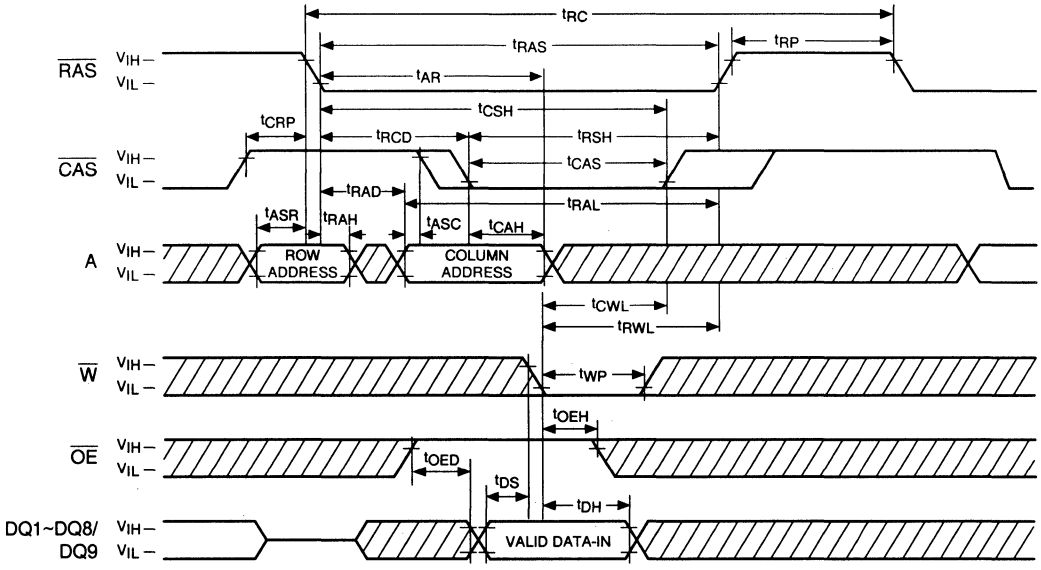
Read Cycle



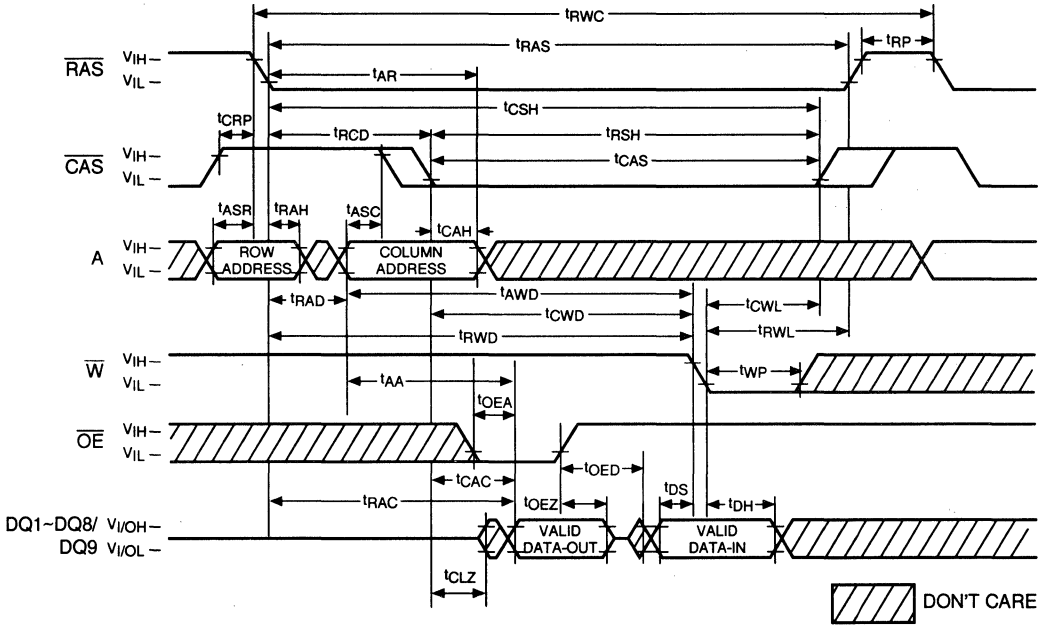
Early Write Cycle



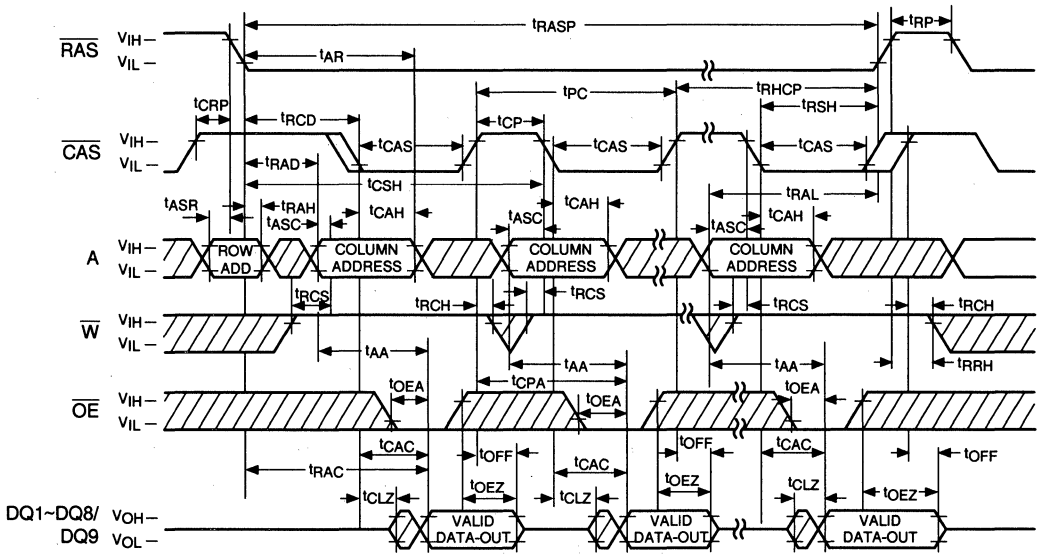
$\overline{OE}$-Controlled Write Cycle



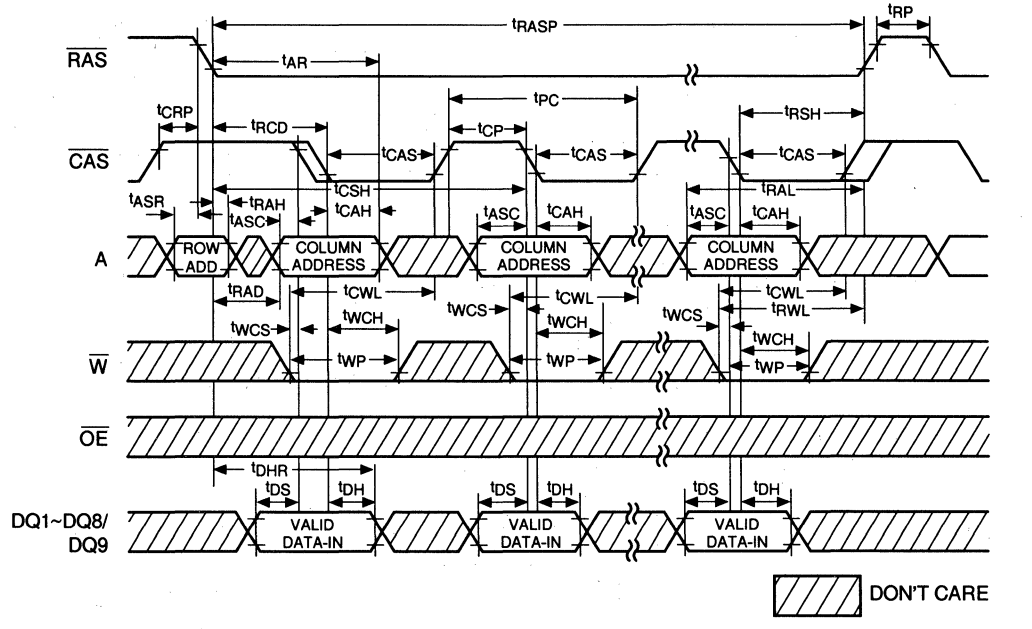
Read-Modify-Write Cycle



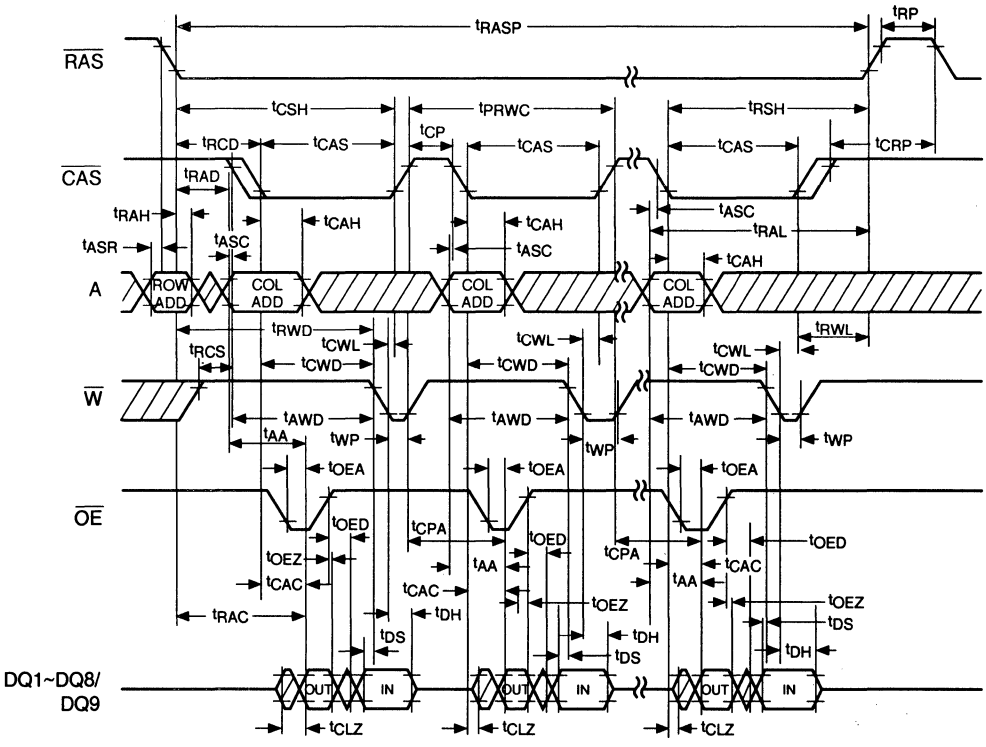
Fast Page Mode Read Cycle



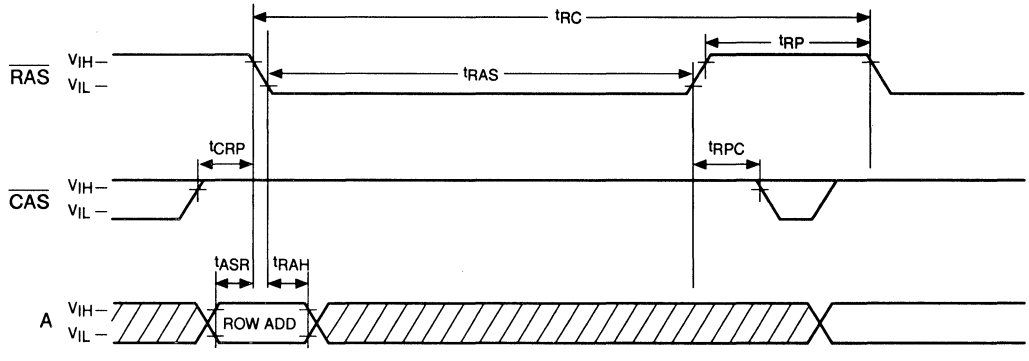
Fast Page Mode Write Cycle (Early Write)



Fast Page Mode Read-Modify-Write Cycle



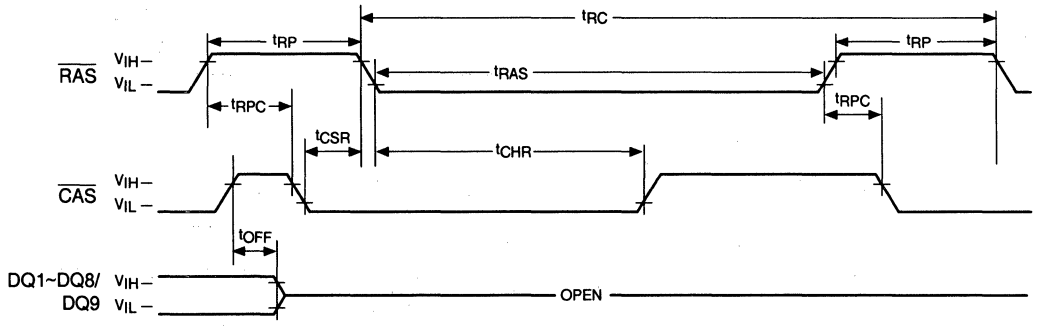
RAS-Only Refresh Cycle



Note: $\overline{W}$, $\overline{OE}$ = Don't Care

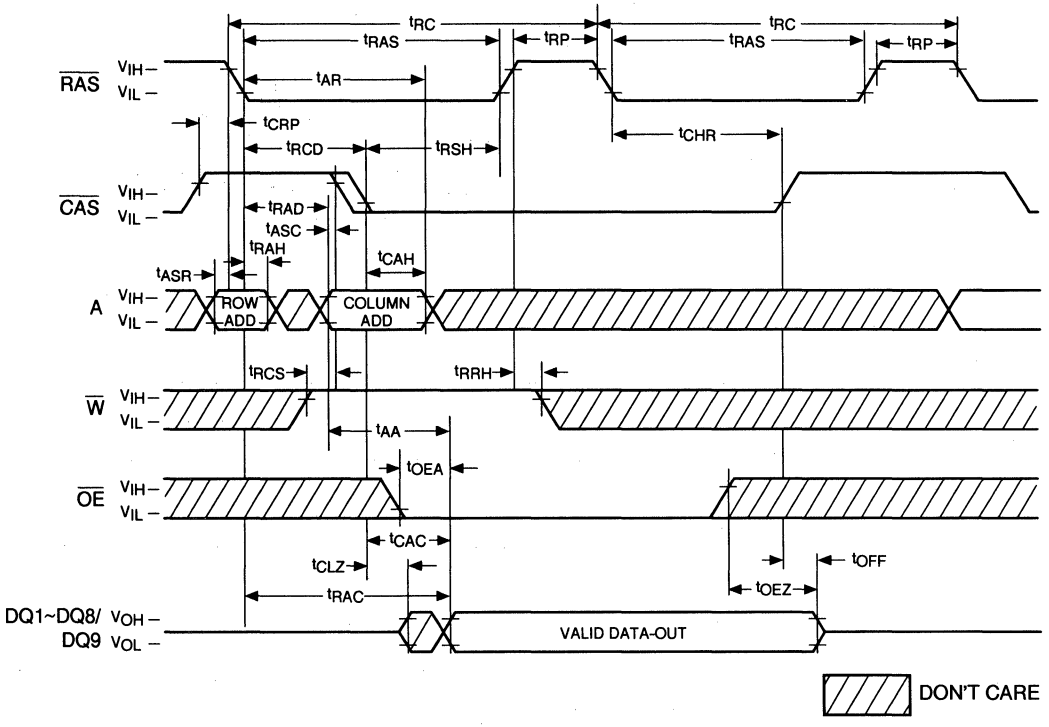
DON'T CARE

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

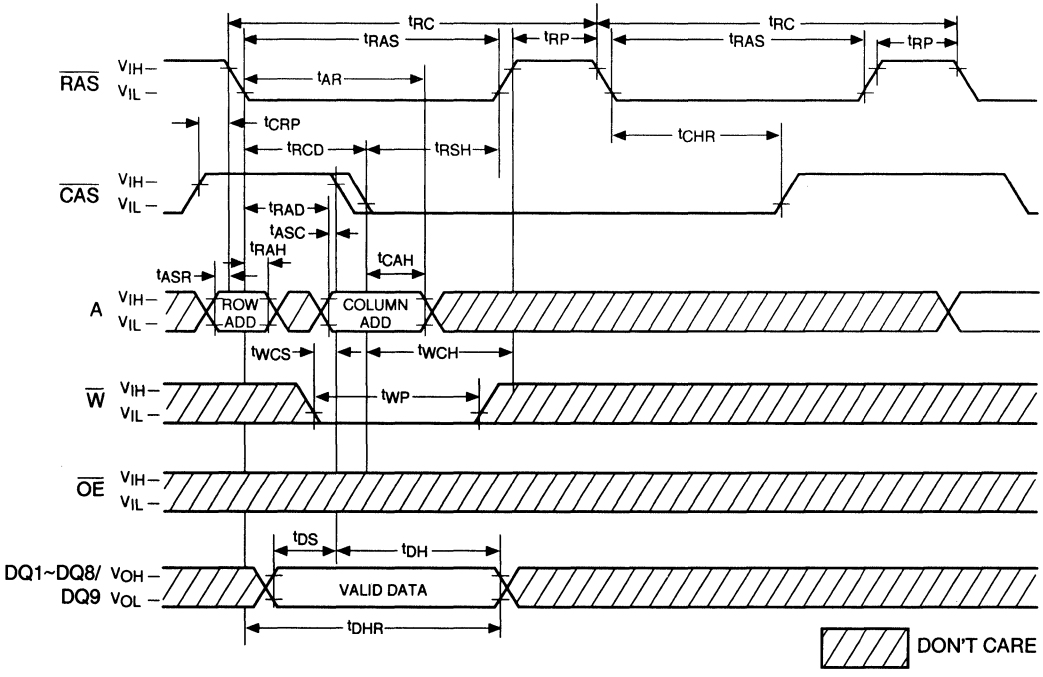


Note: $\overline{W}$ = V_{IH}, $\overline{OE}$, A = Don't Care

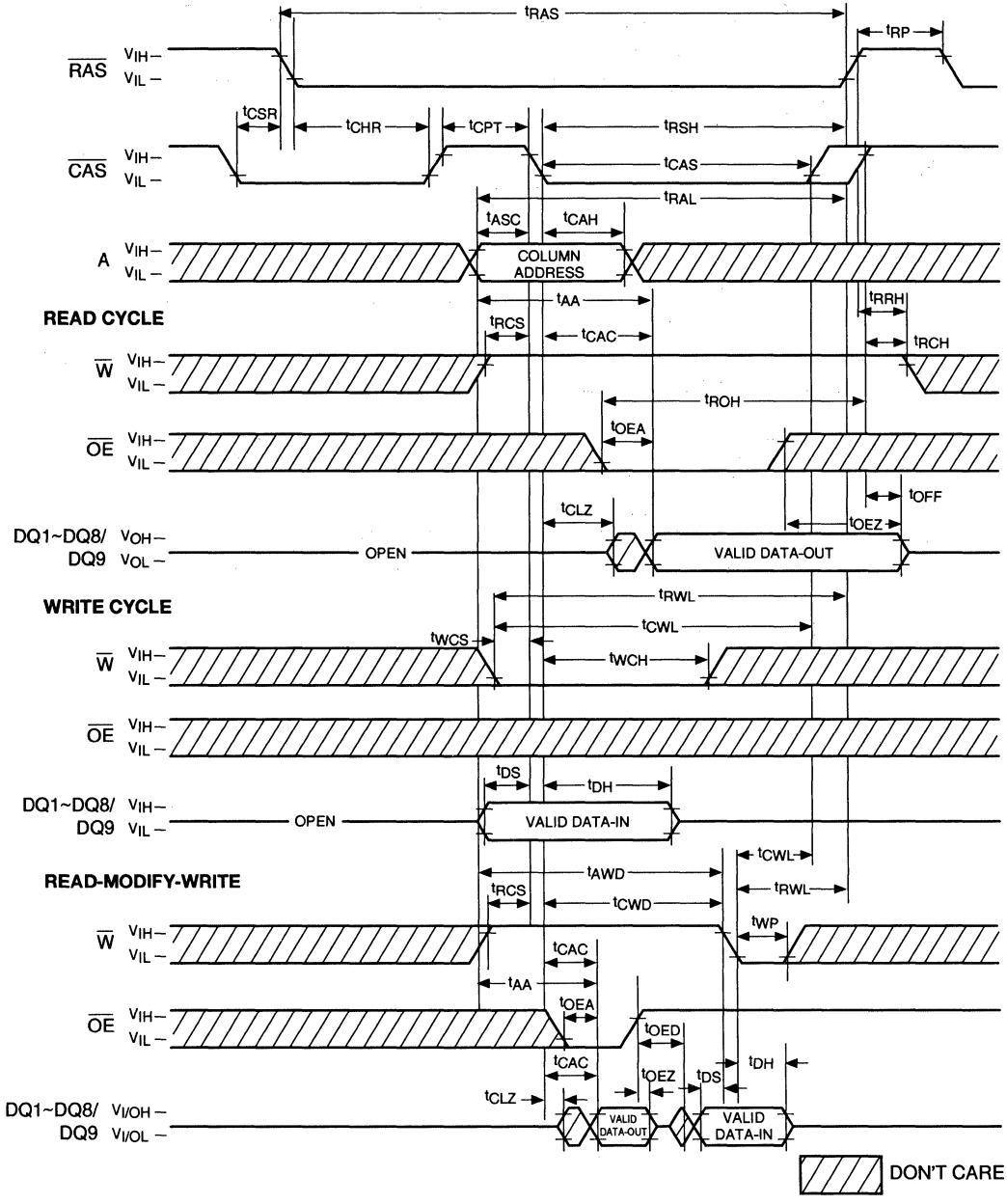
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V53C8512/9512 and V53C8512L/9512L are CMOS dynamic RAMs optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C8512/9512 reads and writes data by multiplexing a 19-bit address into a 10-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 1024 Refresh Cycles are required in each 16 ms period. There are two ways to refresh the memory:

1. By clocking each of the 1024 row addresses (A_0 through A_9) with $\overline{RAS}$ at least once every 16 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C8512/9512 uses the output of an internal 10-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V53C8512/9512 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V53C8512/9512 power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX}-t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 1024

Fast Page Mode Operation

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 28 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{RC} + 511 \times t_{PC}}$$

Data Output Operation

The V53C8512/9512 Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V53C8512/9512 is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V53C8512/9512 Data Output *Operation for Various Cycle Types*

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	$\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

V53C8512N/V53C9512N
3.3 VOLT, LOW POWER
512K x 8 AND 512K x 9 BIT
FAST PAGE MODE
CMOS DYNAMIC RAM

PRELIMINARY

HIGH PERFORMANCE V53C8512N/V53C9512N	60/60L	70/70L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns

LOW POWER V53C8512NL/V53C9512NL	60L	70L
Max. CMOS Standby Current, (I_{DD6})	1 mA	1 mA

2

Features

- 3.3 Volt ± 10% Operation
- Slef Refresh
- 512K x 8 and 512K x 9 Organization
- RAS access time: 60, 70 ns
- Low power dissipation for V53C8512N/9512N
  - Operating Current – 50 mA max.
  - TTL Standby Current – 1 mA max.
- Low CMOS Standby Current
  - V53C8512N/9512N – 2.5 mA max.
  - V53C8512NL/9512NL – 0.5 mA max.
- Read-Modify-Write, RAS-Only Refresh, CAS-Before-RAS Refresh capability
- Common I/O capability
- Refresh Interval
  - V53C8512N/9512N – 1024 cycles/16 ms
  - V53C8512NL/9512NL – 1024 cycles/16 ms
- On-chip substrate bias generator
- Fast Page Mode for a sustained data rate greater than 25 MHz
- Standard package is 28 pin 400 mil SOJ
- Low Battery Back-up Current
  - V53C8512NL/9512NL – 0.5 mA max.

Description

The V53C8512N is a 524,288 x 8 and the V53C9512N is a 524,288 x 9 bit high speed CMOS dynamic random access memory. The V53C8512N and V53C9512N offer a combination of features: 3.3 Volt operation, Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, self refresh and extended refresh for very low data retention power (V53C8512NL and V53C9512NL).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x4) bits within a row with cycle times as short as 40 ns. Because of static circuitry, the CAS clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C8512N and V53C9512N ideally suited for graphics, digital signal processing and high performance computing systems.

The V53C8512NL and V53C9512NL offer a maximum data retention power of 3.3 mW when operating in CMOS standby mode and performing CAS-before-RAS refresh cycles.

Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)		Power		Temperature Mark
	K	60	70	Low	Std.	
0°C to 70°C	•	•	•	•	•	Blank

HIGH PERFORMANCE	70	80	100
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	60 ns
Min. Read/Write Cycle Time, (t_{RC})	130 ns	150 ns	180 ns

Features

- 256K x 16 and 18-bit organization
- $\overline{RAS}$ access time: 70, 80, 100 ns
- Dual $\overline{CAS}$ Input
- Low power dissipation
  - V53C16256-70, V53C18256-70
    - — Operating Current – 110 mA max
    - — TTL Standby Current – 1.0 mA max
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Refresh Interval
  - V53C16256/18256 – 512 cycles/8 ms
- Fast Page Mode
- Available in 40-pin 400 mil SOJ and 40-pin ZIP
- Single +5V Power Supply
- TTL Interface

Description

The V53C16256 is a 262,144 x 16 bit and the V53C18256 is a 262,144 x 18 bit high-performance CMOS dynamic random access memory. The V53C16256 and V53C18256 offer Fast Page mode with dual $\overline{CAS}$ inputs. An address, $\overline{CAS}$ and $\overline{RAS}$ input capacitances are reduced to one quarter when the x4 DRAM is used to construct the same memory density. The V53C16256 and V53C18256 have asymmetric address and accepts 512 cycle 8ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 512 x 16/18 bits, within a page, with cycle times as short as 45ns.

TheV53C16256 is best suited for graphics, and DSP applications and V53C18256 is best suited for the portable and laptop computer main memory applications.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power	Temperature Mark
	P	Z	70	80	100	Std.	
0°C to 70 °C	•	•	•	•	•	•	Blank

V53C16257/18257
256K X 16 AND 256K X 18 BIT
CMOS DYNAMIC RAMS

HIGH PERFORMANCE	70	80	100
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	60 ns
Min. Read/Write Cycle Time, (t_{RC})	130 ns	150 ns	180 ns

Features

- 256K x 16 and 18-bit organization
- $\overline{RAS}$ access time: 70, 80, 100 ns
- Dual Write Enable Inputs
- Low power dissipation
  - V53C16257-70, V53C18257-70
    - — Operating Current – 110 mA max
    - — TTL Standby Current – 1.0 mA max
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Refresh Interval
  - V53C16257/18257 – 1024 cycles/16 ms
- Fast Page Mode
- Available in 40-pin 400 mil SOJ and 40-pin ZIP
- Single +5V Power Supply
- TTL Interface

Description

The V53C16257 is a 262,144 x 16 bit and the V53C18257 is a 262,144 x 18 bit high-performance CMOS dynamic random access memory. The V53C16257 and V53C18257 offer Fast Page mode with dual write enable inputs. An address, $\overline{CAS}$ and $\overline{RAS}$ input capacitances are reduced to one quarter when the x4 DRAM is used to construct the same memory density. The V53C16257 and V53C18257 have an asymmetric address and accepts 1024 cycle 16ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 512 x 16/18 bits, within a page, with cycle times as short as 45ns.

TheV53C16257 is best suited for graphics, and DSP applications and V53C18257 is best suited for the portable and laptop computer main memory applications.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)			Power	Temperature Mark
	P	Z	70	80	100	Std.	
0°C to 70 °C	•	•	•	•	•	•	Blank

HIGH PERFORMANCE V53C261	10	12
Max. RAS Access Time, (t_{RAC})	100 ns	120 ns
Max Column Address Time, (t_{CAA})	45 ns	55 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	60 ns	70 ns
Min. Read/Write Cycle Time, (t_{RC})	175 ns	205 ns
Min. Serial Port Cycle Time, (t_{SCC})	35 ns	40 ns

Features

- Low power dissipation for V53C261-12
  - RAM Port operating alone - 50 mA
  - SAM Port operating alone - 35 mA
  - RAM/SAM operating together - 85 mA
- Low CMOS standby current - 6 mA
- Fast Page Mode access, $\overline{RAS}$-only refresh, and $\overline{CAS}$-before-$\overline{RAS}$ Refresh capability
- Bi-directional data transfer between RAM and SAM with Turbomode™ real-time operation.
- Bit-masked Write function on RAM port for additional flexibility.
- 256 Refresh cycles/4 ms.
- Standard packages are 24 pin 400 mil Plastic DIP and 24 pin ZIP.

Description

The V53C261 is a high speed 65,536 x 4 bit multiport CMOS dynamic memory. The two ports, random access and serial access, are configured to offer optimum flexibility in graphics and other systems that require an interface between a processor and a high speed serial data channel such as a CRT or graphics display device.

The organization of the random access port of the V53C261 is exactly like that of the V53C464, a 64K x 4 CMOS DRAM. Additional functions such as transfer between RAM and SAM utilize otherwise unused states of the $\overline{CAS}$, DT/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$ and $\overline{SE}$ signals sampled at the falling edge of $\overline{RAS}$ at the beginning of a cycle.

The Serial Access Memory (SAM) is organized as 256 x 4 bits that can be read or written at high speed. The contents of the SAM can be loaded into RAM, and the contents of a selected RAM row (256 x 4) can be loaded into SAM. Except when transferring data between one another, the SAM and RAM operate in an asynchronous manner. The transfer from RAM to SAM or SAM to RAM also refreshes the transferred row in the RAM.

In a RAM to SAM load cycle, 8 bits are needed to specify which of the 256 rows is to be transferred. The state of the address lines at the falling edge of $\overline{CAS}$ is used to specify the starting point in the SAM where data is to be written or read. The static mechanization of the SAM (allowed by CMOS) does not require refreshing. The first access to SAM, either read or write, will be to the location specified at $\overline{CAS}$ time in the previous cycle, and subsequent accesses will continue in an increasing address direction, modulo 256.

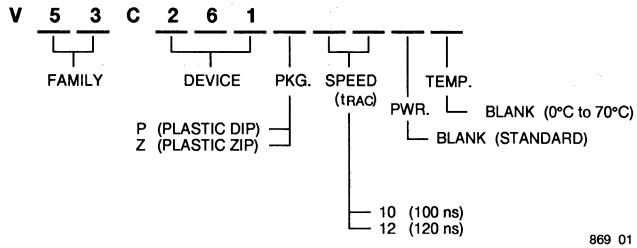
The V53C261 is processed utilizing VICMOS technology. This advanced CMOS processing allows memory devices to be fabricated with lower operating current and higher performance than comparable NMOS designs. All I/O signals are TTL compatible. Input and I/O capacitances are significantly lowered to enhance system performance.

Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)		Power	Temperature Mark
	P	Z	100	120	Std.	
0°C to 70 °C	•	•	•	•	•	Blank

V53C261 Rev. 02 June 1990

Description	Pkg.	Pin Count
Plastic DIP	P	24
Plastic ZIP	Z	24



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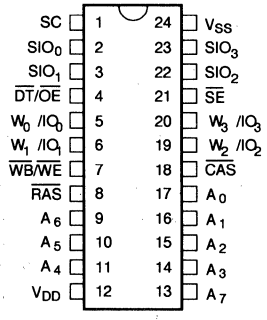
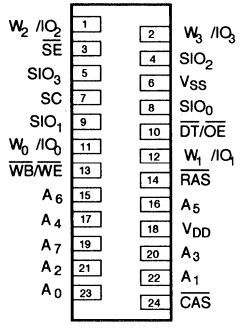
24 Lead Plastic DIP PIN CONFIGURATION
Top View



24 Lead Plastic ZIP PIN CONFIGURATION
Top View



869 02

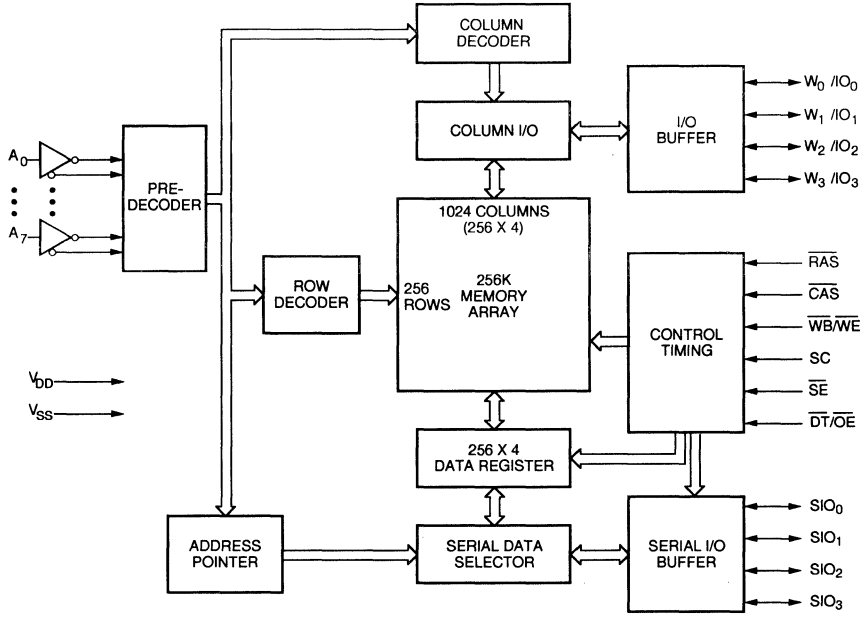
Capacitance*

T_A = 25°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance		5	pF
C_{IN2}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WB/WE}$ $\overline{SE}$, SC, $\overline{DT/OE}$ Capacitance		8	pF
C_{OUT}	I/O Capacitance		7	pF

* Note: Capacitance is sampled and not 100% tested

Block Diagram



869 03

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... −1.0 V to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... −1.0 V to +7.0 V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

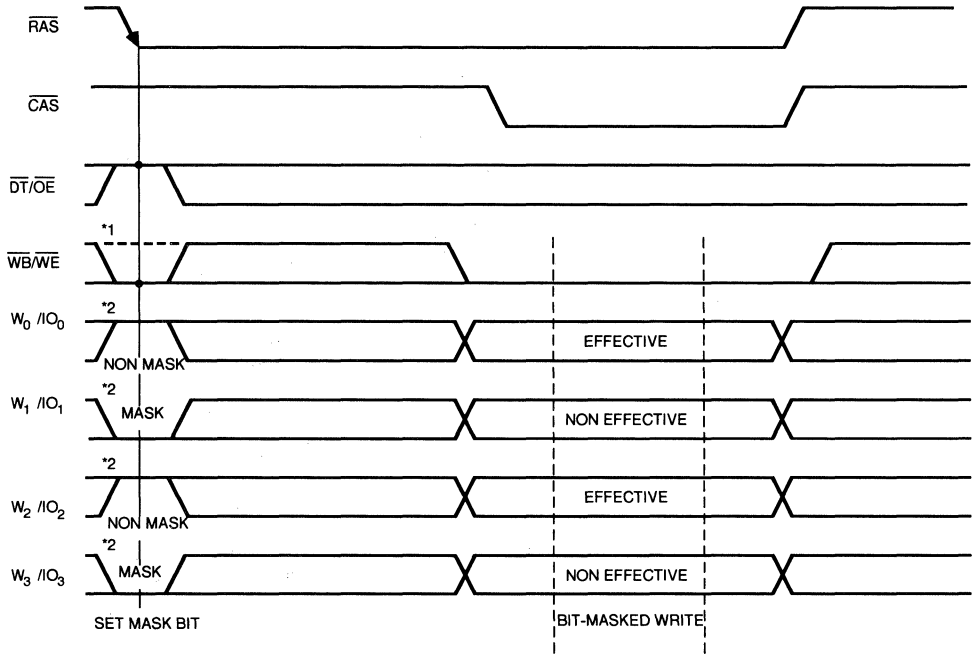
*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

AC Test Conditions

Input Voltage Levels ..... 0 to 3.0 V
Input Rise and Fall Times ..... 5 ns between 0.8 and 2.4 V
Input Timing Reference Levels ..... 0.8 and 2.4 V
Output Timing Reference Levels ..... 0.8 and 2.4 V
Output Load (RAM Port) ..... 2 TTL and 100 pF
Output Load (SAM Port) ..... 2 TTL and 50 pF

3

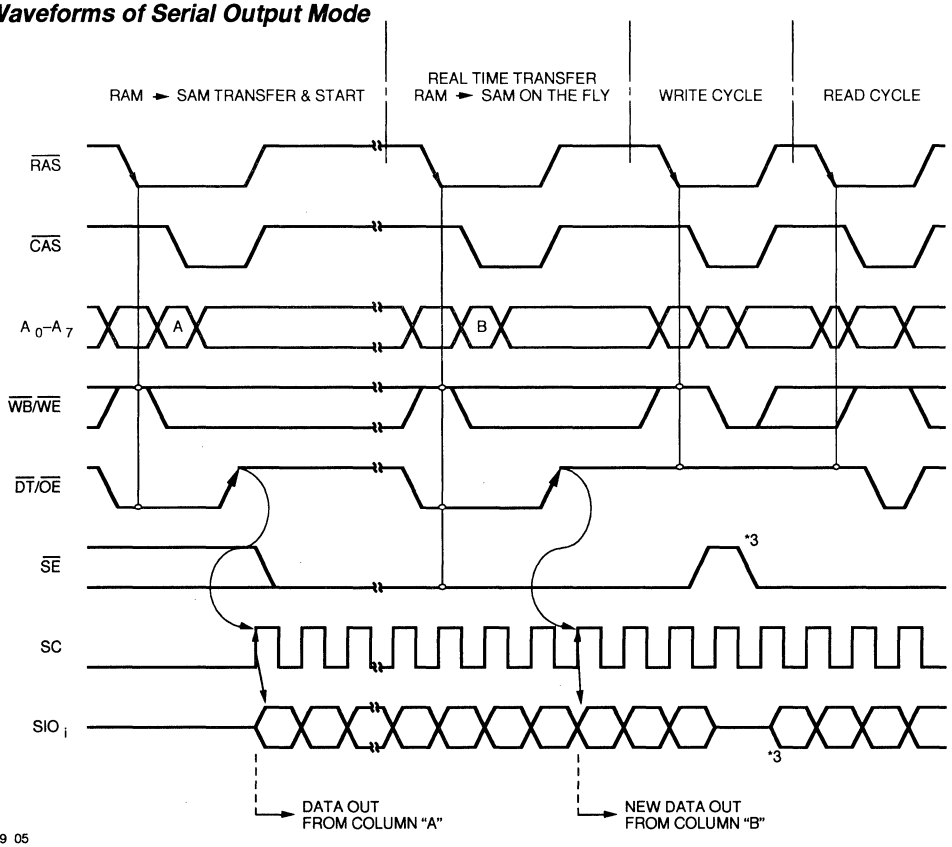
Waveforms of Bit Masked Write



*1 If WB/WE = "H" all 4 bits of data are written into RAM
*2 W0–3/IO0–3 = "H" Non masked
W0–3/IO0–3 = "L" Masked

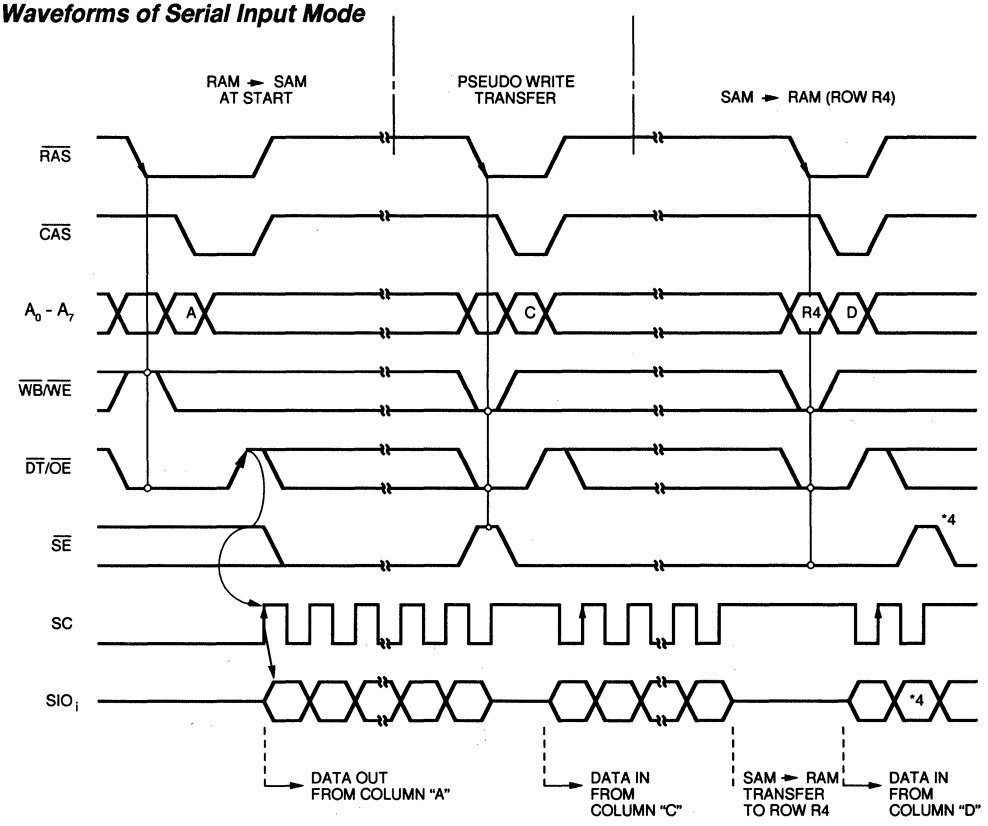
869 04

Waveforms of Serial Output Mode



*3 If $\overline{SE}$ goes to "H" level, SIO_i enters the high impedance state, but the serial data selector continues to function.

Waveforms of Serial Input Mode



*4 If $\overline{SE}$ goes to "H" level, SIO_i input data is ignored, but the serial data selector continues to function

869 06

DC Characteristics (1, 5)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C261 min	V53C261 max	V53C261 Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)		–10	10	µA	$V_{SS} < V_{IN} < V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10	10	µA	$V_{SS} < V_{OUT} < V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ and $\overline{SE}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current	100		60	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC} (min), SC=V_{IL}	2,3
		120		50			
I_{DD2}	V_{DD} Supply Current TTL Standby			8	mA	RAM/SAM ports TTL Standby $\overline{RAS}$, $\overline{CAS}$ at V_{IH}, I/O > V_{SS} SC=V_{IL}	
I_{DD3}	V_{DD} Supply Current $\overline{RAS}$-Only Refresh	100		60	mA	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH} SAM port TTL Standby t_{RC} (min), SC=V_{IL}	2,3
		120		50			
I_{DD4}	V_{DD} SupplyCurrent Fast Page Mode Operation	100		50	mA	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling SAM port TTL Standby t_{PC} (min), SC=V_{IL}	2,3
		120		40			
I_{DD5}	V_{DD} Supply Current $\overline{CAS}$-before-$\overline{RAS}$ Refresh	100		60	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC} (min), SC=V_{IL}	2,3
		120		50			
I_{DD6}	V_{DD} SupplyCurrent RAM/SAM Transfer Mode	100		65	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port TTL Standby t_{RC} (min), SC=V_{IL}	2,3
		120		55			
I_{DD7}	V_{DD} SupplyCurrent Both Ports Active	100		100	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active t_{RC} (min), t_{SCC} (min)	2,3
		120		85			
I_{DD8}	V_{DD} Supply Current SAM Only Operation	100		40	mA	$\overline{RAS}/\overline{CAS}$ at V_{IH}, I/O > V_{SS} SAM port Active t_{SCC} (min)	2
		120		35			
I_{DD9}	V_{DD} Supply Current $\overline{RAS}$-Only Refresh and SAM Active	100		100	mA	$\overline{RAS}$ Cycling, $\overline{CAS}$ at V_{IH}, SAM port Active t_{RC} (min), t_{SCC} (min)	2,3
		120		85			
I_{DD10}	V_{DD} Supply Current, Fast Page Mode Operation and SAM Active	100		90	mA	$\overline{RAS}$=V_{IL}, $\overline{CAS}$ Cycling SAM port Active t_{PC} (min), t_{SCC} (min)	2,3
		120		75			

3

DC Characteristics (Cont'd.)

Symbol	Parameter	Access Time	V53C261 min	V53C261 max	Unit	Test Conditions	Notes
I_{DD11}	V_{DD} Supply Current $\overline{CAS}$-before-$\overline{RAS}$ Refresh and SAM Active	100		100	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active t_{RC} (min), t_{SCC} (min)	2,3
		120		85			
I_{DD12}	V_{DD} Supply Current RAM/SAM Transfer Mode and SAM Active	100		105	mA	$\overline{RAS}/\overline{CAS}$ Cycling, SAM port Active t_{RC} (min), t_{SCC} (min)	2,3
		120		90			
I_{DD13}	V_{DD} Supply Current Both Ports CMOS Standby			6	mA	$\overline{RAS}$, $\overline{CAS}$, $\overline{SE}$, $\overline{WB}/\overline{WE}$, $\overline{DT}/\overline{OE}$ >V_{DD} –0.5 V SC < 0.6 V	
V_{IL}	Input Low Voltage		–1	0.8	V		
V_{IH}	Input High Voltage		2.4	V_{DD} +1	V		
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		V	I_{OH} = –2 mA	

AC Characteristics (1,4,5,6)

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise specified.

Read, Write, Read-Modify-Write and Refresh Cycles

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
	t_T	Transition Time (Rise and Fall)	3	25	3	25	ns	
	t_{RI}	Refresh Interval (256 Cycles)		4		4	ms	
1	t_{RC}	Read or Write Cycle Time	175		205		ns	
2	t_{RAS}	$\overline{RAS}$ Pulse Width	100	37K	120	37K	ns	
3	t_{RP}	$\overline{RAS}$ Precharge Time	65		75		ns	
4	t_{CSH}	$\overline{CAS}$ Hold Time	100		120		ns	
5	t_{CAS}	$\overline{CAS}$ Pulse Width	30		35		ns	
6	t_{ASR}	Row Address Setup Time	0		0		ns	
7	t_{RAH}	Row Address Hold Time	15		15		ns	
8	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
9	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	70	25	85	ns	7
10	t_{ASC}	Column Address Setup Time	0		0		ns	
11	t_{CAH}	Column Address Hold Time	20		20		ns	
12	t_{RSH}	$\overline{RAS}$ Hold Time	30		35		ns	
13	t_{DHS}	$\overline{DT}$ High Setup Time	0		0		ns	
14	t_{DHH}	$\overline{DT}$ High Hold Time	20		20		ns	
15	t_{AR}	Column Address Hold Time from $\overline{RAS}$	70		80		ns	

AC Characteristics (Cont'd.)

Read Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max	Min	Max
16	t_{RAC}	$\overline{RAS}$ Access Time		100		120	ns	8,9
17	t_{CAC}	$\overline{CAS}$ Access Time		30		35	ns	9,10 11
18	t_{CAA}	Column Address Access Time		45		55	ns	9
19	t_{RCS}	Read Command Setup Time	0		0		ns	
20	t_{RRH}	Read Command Hold Time, $\overline{RAS}$-Referenced	5		10		ns	12
21	t_{RCH}	Read Command Hold Time, $\overline{CAS}$-Referenced	0		0		ns	12
22	t_{OAC}	$\overline{OE}$ Access Time		25		30	ns	9
23	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to Output High-Z		25		30	ns	13
24	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Output Low-Z	0		0		ns	
25	t_{OH}	Output Hold Time From $\overline{OE}$ or $\overline{CAS}$	0		0		ns	

AC Characteristics (Cont'd.)

Write Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
26	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	30		35		ns	
27	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	30		35		ns	
28	t_{WP}	Write Command Pulse Width	20		25		ns	
29	t_{WCS}	Write Command Setup Time	0		0		ns	14
30	t_{WCH}	Write Command Hold Time	20		25		ns	
31	t_{DS}	Data In Setup Time	0		0		ns	
32	t_{DH}	Data In Hold Time	20		25		ns	
33	t_{WBS}	Write Mask Setup Time	0		0		ns	
34	t_{WBH}	Write Mask Hold Time	20		20		ns	
35	t_{WS}	Write Mask Select Setup Time	0		0		ns	
36	t_{WH}	Write Mask Select Hold Time	20		20		ns	
37	t_{OEH}	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	10		15		ns	
38	t_{WCR}	Write Hold Time from $\overline{RAS}$	80		95		ns	
39	t_{DHR}	Data Hold Time from $\overline{RAS}$	80		95		ns	

AC Characteristics (Cont'd.)

Read-Modify-Write Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
40	t_{RWC}	Read-Modify-Write Cycle Time	245		285		ns	
41	t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	170	37K	200	37K	ns	
42	t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	100		115		ns	
43	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	135		160		ns	14
44	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	65		75		ns	14
45	t_{AWD}	Column Address to $\overline{WE}$ Delay	80		95		ns	
46	t_{OED}	$\overline{OE}$ to Data In Delay Time	25		30		ns	

Fast Page Mode Operation

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
47	t_{PC}	Page Mode Cycle Time	60		70		ns	
48	t_{CP}	$\overline{CAS}$ Precharge Time	20		25		ns	
49	t_{CAP}	Access Time from Column Precharge		55		65	ns	15

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
50	t_{CSR}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Setup Time	10		10		ns	
51	t_{CHR}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Hold Time	25		25		ns	
52	t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0		ns	

AC Characteristics (Cont'd.)

Read/Write, Pseudo Write Transfer and Serial Read/Write Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
53	t_{SCC}	Serial Clock Cycle Time	35		40		ns	
54	t_{SCL}	SC Precharge Time	10		10		ns	
55	t_{SOO}	$\overline{SE}$ to Serial Out Setup Time	0		5		ns	
56	t_{SOH}	Serial Out Hold after SC High	0		5		ns	
57	t_{SCA}	Serial Output Access Time from SC		30		35	ns	16
58	t_{SOA}	Serial Output Access Time from $\overline{SE}$		25		30	ns	16
59	t_{SOZ}	Serial Output Disable Time from $\overline{SE}$ High		20		25	ns	13
60	t_{SCH}	SC Pulse Width	15		15		ns	
61	t_{SOE}	$\overline{SE}$ Pulse Width	10		10		ns	
62	t_{SOP}	$\overline{SE}$ Precharge Time	10		10		ns	
63	t_{DLS}	Transfer Command to $\overline{RAS}$ Setup Time	0		0		ns	
64	t_{RDH}	Transfer Command to $\overline{RAS}$ Hold Time	75		90		ns	
65	t_{CDH}	Transfer Command to $\overline{CAS}$ Hold Time	25		30		ns	
66	t_{SDD}	SC to Transfer Command Lead Time	15		20		ns	
67	t_{SDH}	SC Hold Time after $\overline{DT}$ High	10		10		ns	
68	t_{SZS}	Serial Data Input to $\overline{DT}$ High Delay Time		0		0	ns	
69	t_{DTP}	$\overline{DT}$ Precharge Time	25		30		ns	
70	t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	75		85		ns	
71	t_{SWS}	Serial Write Enable Setup Time	10		10		ns	
72	t_{SWH}	Serial Write Enable Hold Time	15		20		ns	
73	t_{SWIS}	Serial Write Disable Setup Time	10		10		ns	
74	t_{SWIH}	Serial Write Disable Hold Time	15		20		ns	
75	t_{SRS}	SC to $\overline{RAS}$ Setup Time	20		20		ns	

AC Characteristics (Cont'd.)

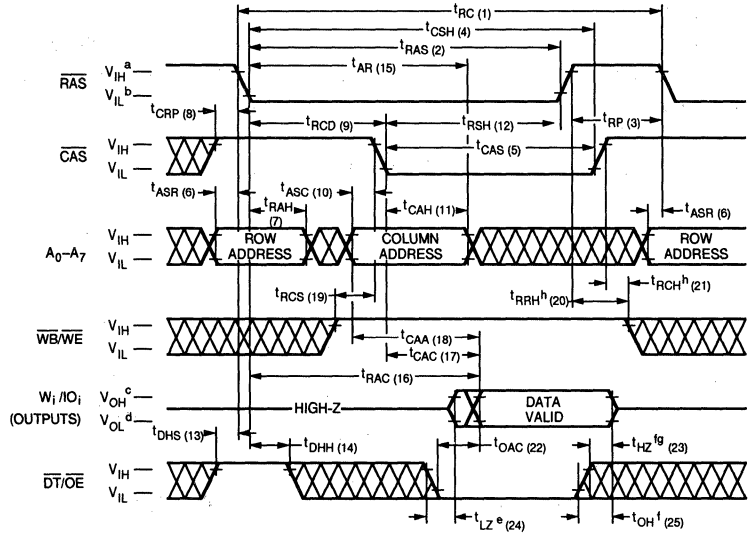
Read/Write, Pseudo Write Transfer and Serial Read/Write Cycle

#	Symbol	Parameter	10		12		Unit	Notes
			Min	Max	Min	Max		
76	t_{ES}	Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Setup Time	0		0		ns	
77	t_{EH}	Pseudo Transfer Command ($\overline{SE}$) to $\overline{RAS}$ Hold Time	20		20		ns	
78	t_{SIS}	Serial Data In Setup Time	0		0		ns	
79	t_{SIH}	Serial Data In Hold Time	10		10		ns	
80	t_{SDS}	SC to $\overline{DT}$ High Setup Time	0		0		ns	
81	t_{SCR}	SC to $\overline{RAS}$ Precharge Setup Time	0		0		ns	

Notes:

1. All voltages are referenced to V_{SS}.
2. I_{DD} is dependent on output loading when the device output is enabled. I_{DD} (max.) is measured with all outputs open.
3. I_{DD} is dependent on the number of address transitions while $\overline{CAS}$ is at V_{IH}. Specified I_{DD} (max.) is measured with a maximum of two transitions per address input per random cycle and one transition per address cycle in Fast Page Mode.
4. V_{IH} (min.) and V_{IL} (max.) are the reference levels for measuring input signal timing. Transition times are measured between V_{IH} (min.) and V_{IL} (max.).
5. An initial pause of 200 µs and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks or upon Power Up. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
6. AC characteristics assume t_T = 5 ns. All AC measurements are made with a load equivalent to two TTL inputs and either 50 or 100 pF in parallel. V_{IL} (min.) > V_{SS} and V_{IH} (max.) < V_{DD}.
7. t_{RCD} (max.) is for reference only. t_{RCD} (min.) = t_{RAH} (min.) + 2t_T + t_{ASC} (min.)
8. Assumes that $t_{RCD} < t_{RCD}$ (max.). If $t_{RCD} > t_{RCD}$ (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
9. Measured with a load equivalent to 2 TTL loads and 100 pF in parallel.
10. Assumes $t_{RCD} > t_{RCD}$ (max.).
11. If $t_{ASC} < (t_{CAA}$ (max.) - t_{CAC} (max.) - tT), access time is defined by t_{CAA} rather than t_{CAC}.
12. Either t_{RCH} or t_{RRH} must be satisfied.
13. An output disable time defines the time when the output reaches the open-circuit condition and is not referenced to output voltage levels.
14. t_{WCS}, t_{RWD} and t_{CWD} are specified for reference only. If $t_{WCS} > t_{WCS}$ (min.), the cycle is a $\overline{CAS}$-controlled write cycle (Early Write), and the $\overline{IO}$ pins will be at High-Z during the entire cycle. If $t_{CWD} > t_{CWD}$(min.), and $t_{RWD} > t_{RWD}$(min.), the cycle is a Read-Modify-Write cycle, and the $\overline{IO}$ pins will reflect the data read from the addressed location. If any of the above conditions is not satisfied, the condition of the Data Out pins will be indeterminate.
15. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
16. Measured with a load equivalent to 2 TTL loads and 50 pF in parallel.

Waveforms of Read Cycle



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NOTES:

a., b. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals.

c., d. V_{OH} (min) and V_{OL} (max) are reference levels for measuring timing of D_{OUT}.

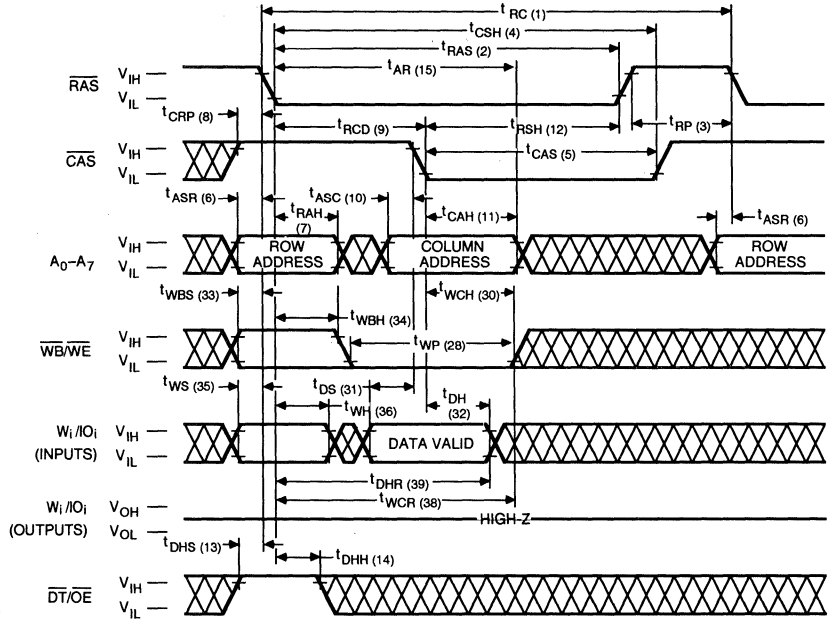
e. t_{LZ} is referenced to the later of $\overline{CAS}$ and $\overline{OE}$ low transition.

f. t_{HZ} and t_{OH} are referenced to the earlier of $\overline{CAS}$ and $\overline{OE}$ high transition.

g. Transition is measured +500 mV from steady state voltage with specified three state load (5 pF and a 380 Ohm Thevenin equivalent).

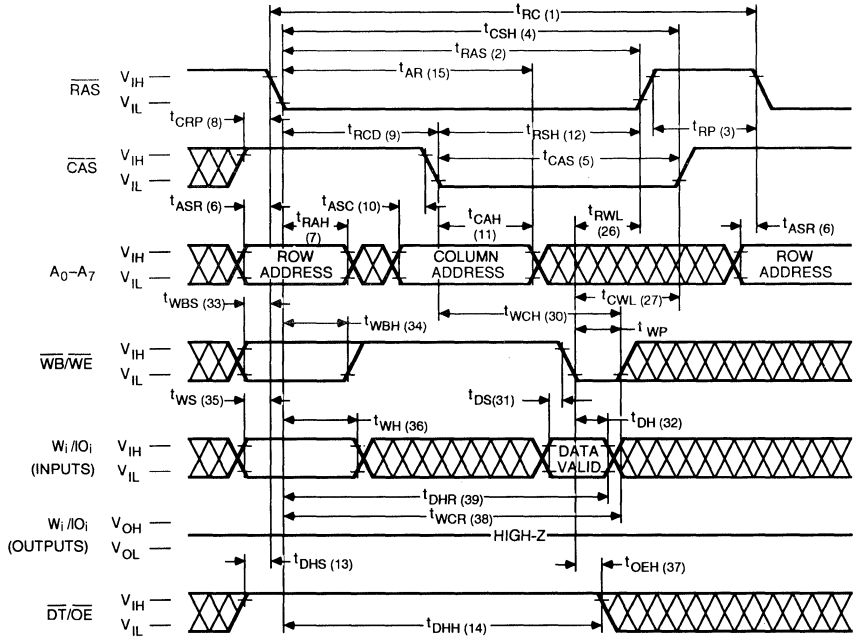
h. Either t_{RCH} or t_{RRH} must be satisfied.

Waveforms of Write Cycle (Early Write)



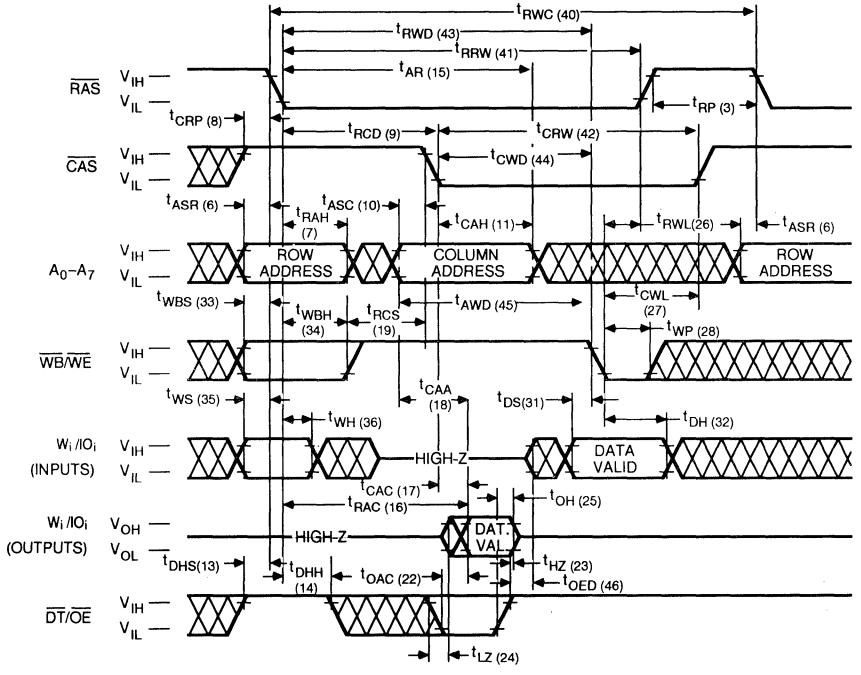
869 08

Waveforms of Write Cycle (Delayed Write)



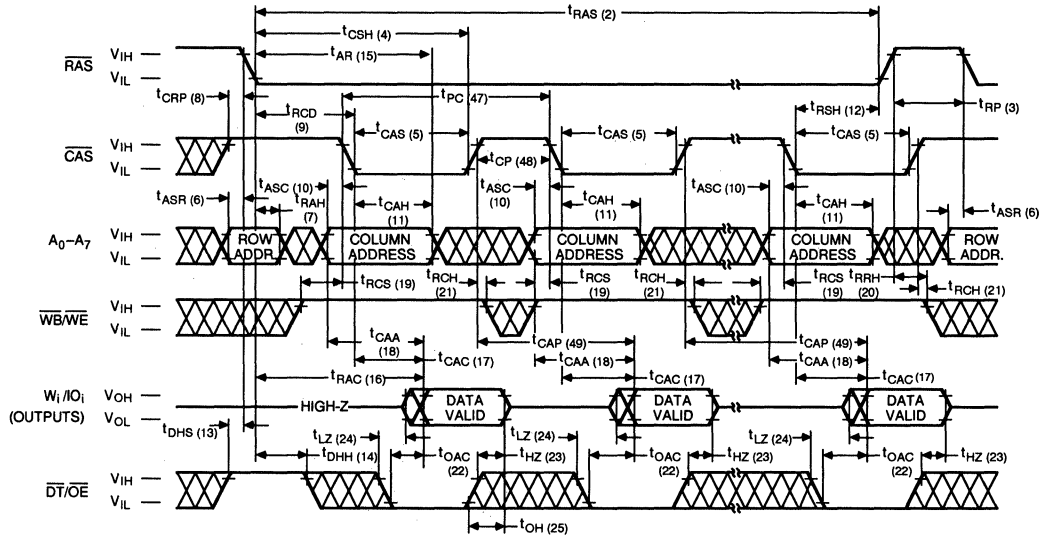
869 09

Waveforms of Read-Modify-Write Cycle



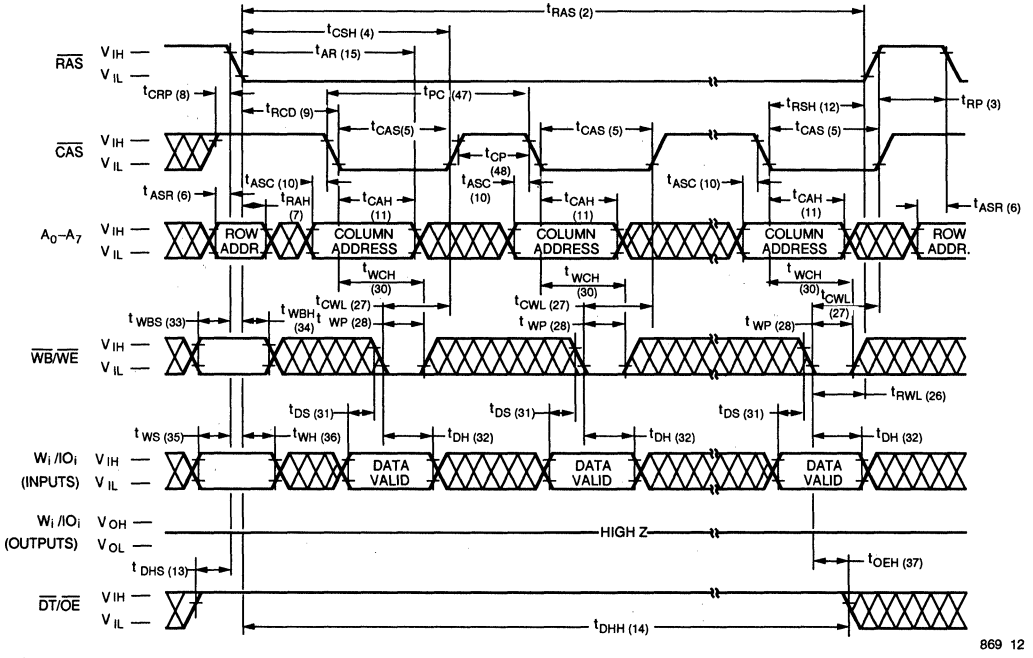
869 10

Waveforms of Fast Page Read Cycle



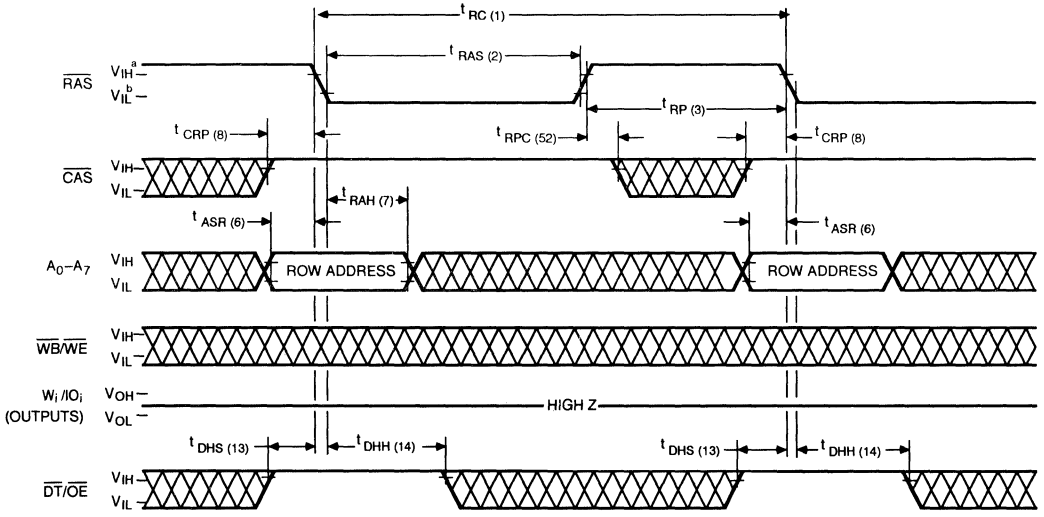
869 11

Waveforms of Fast Page Mode Write Cycle



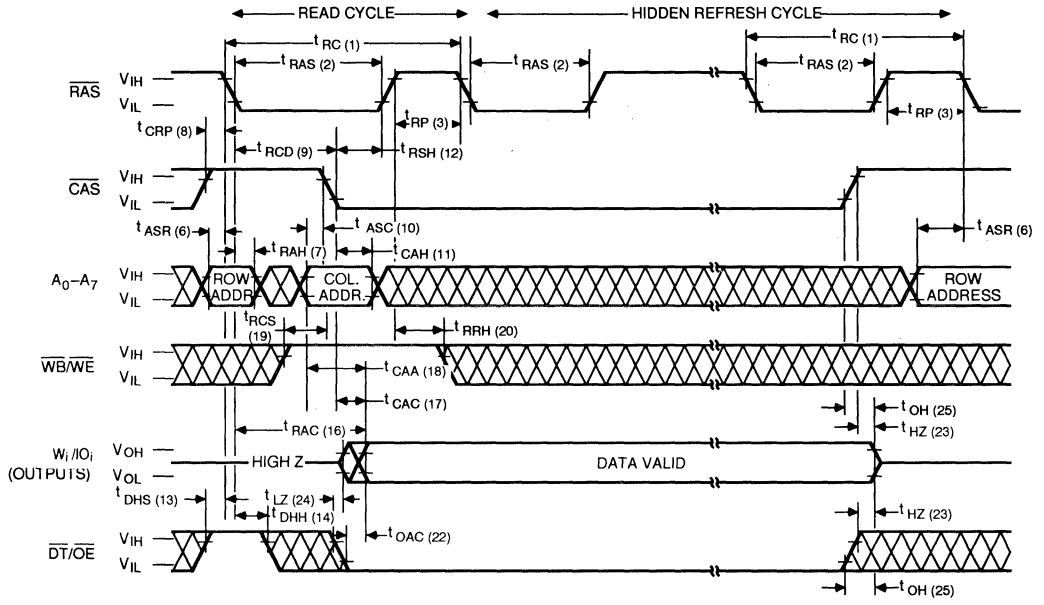
869 12

Waveforms of $\overline{RAS}$-Only Refresh Cycle



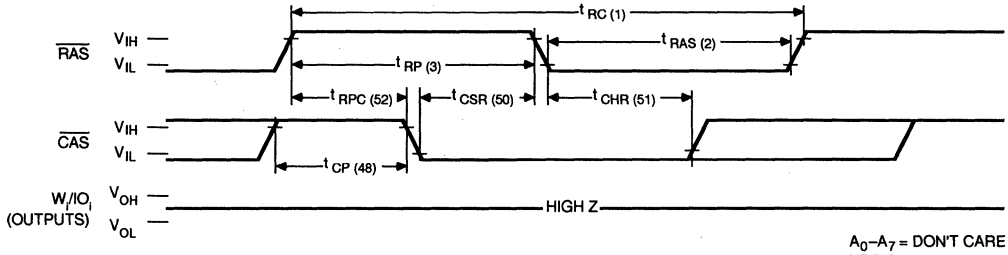
869 13

Waveforms of Hidden Refresh Cycle



869 14

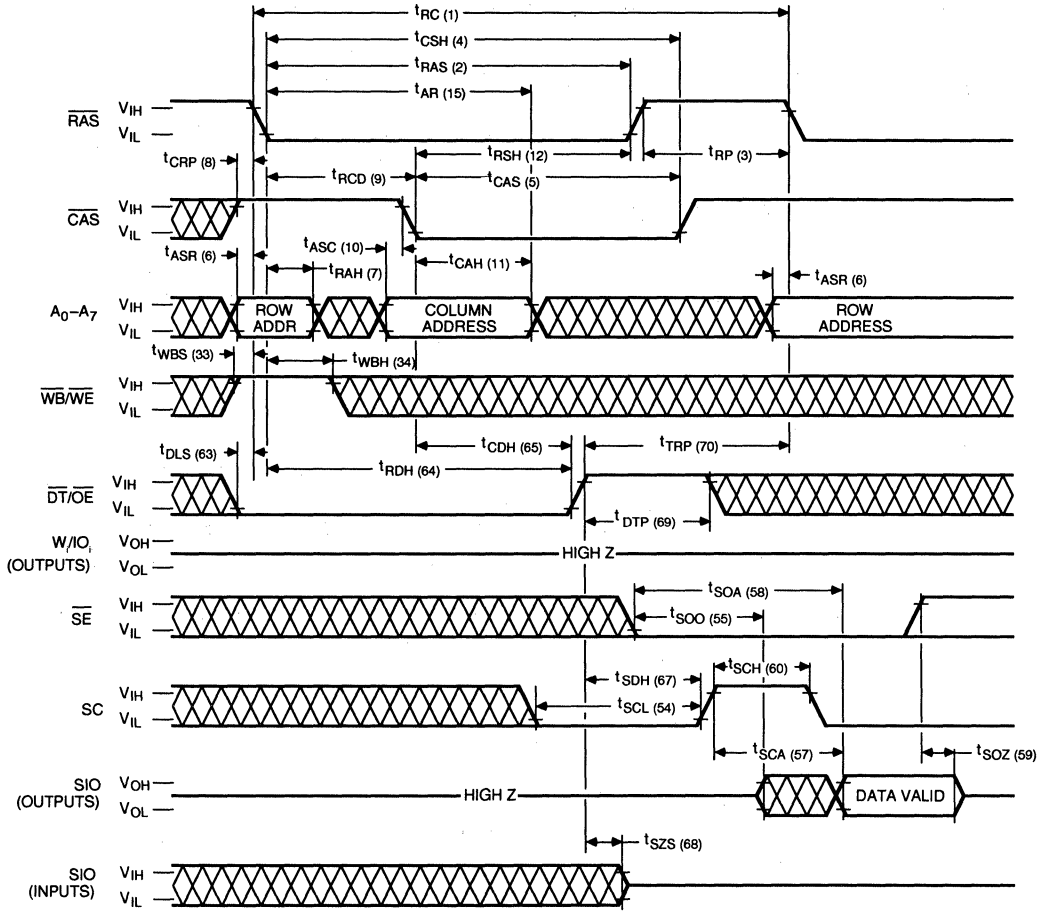
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



A_0–A_7 = DON'T CARE
$\overline{DT/OE}$ = DON'T CARE
$\overline{WB/WE}$ = DON'T CARE

869 14a

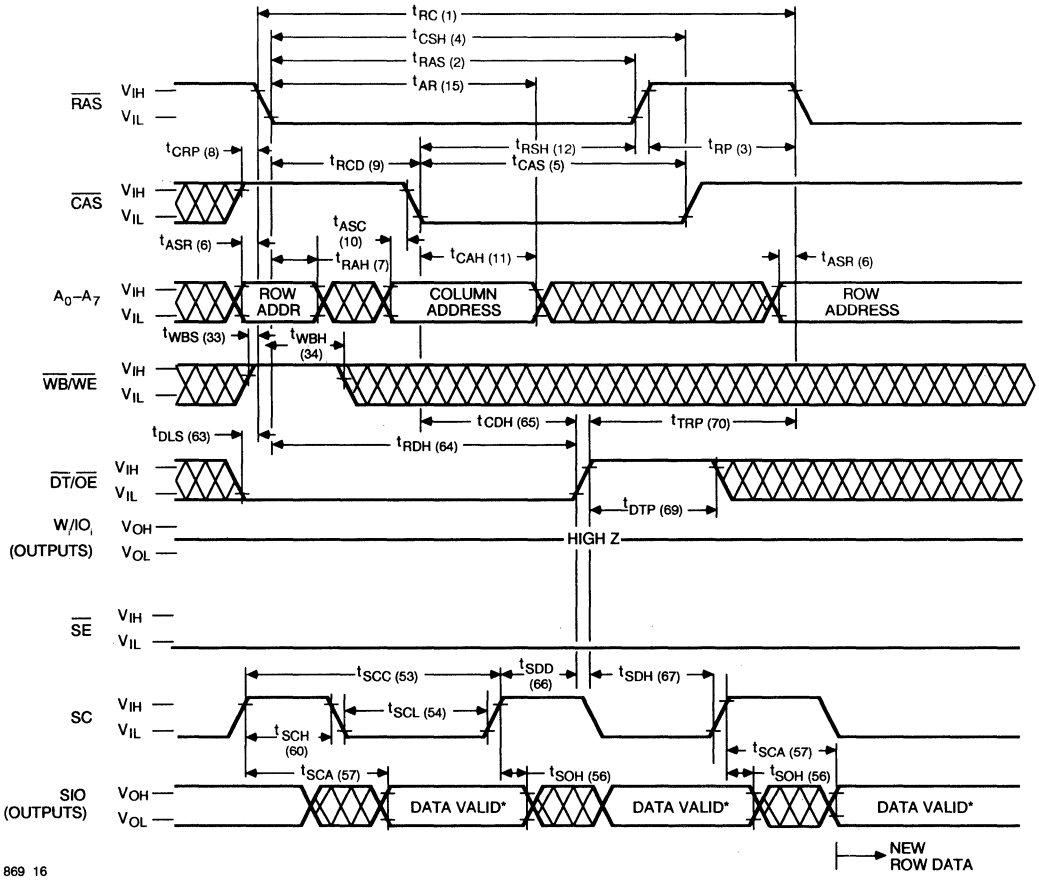
Waveforms of Read Transfer Cycle (RAM-SAM) Serial Read Setup*



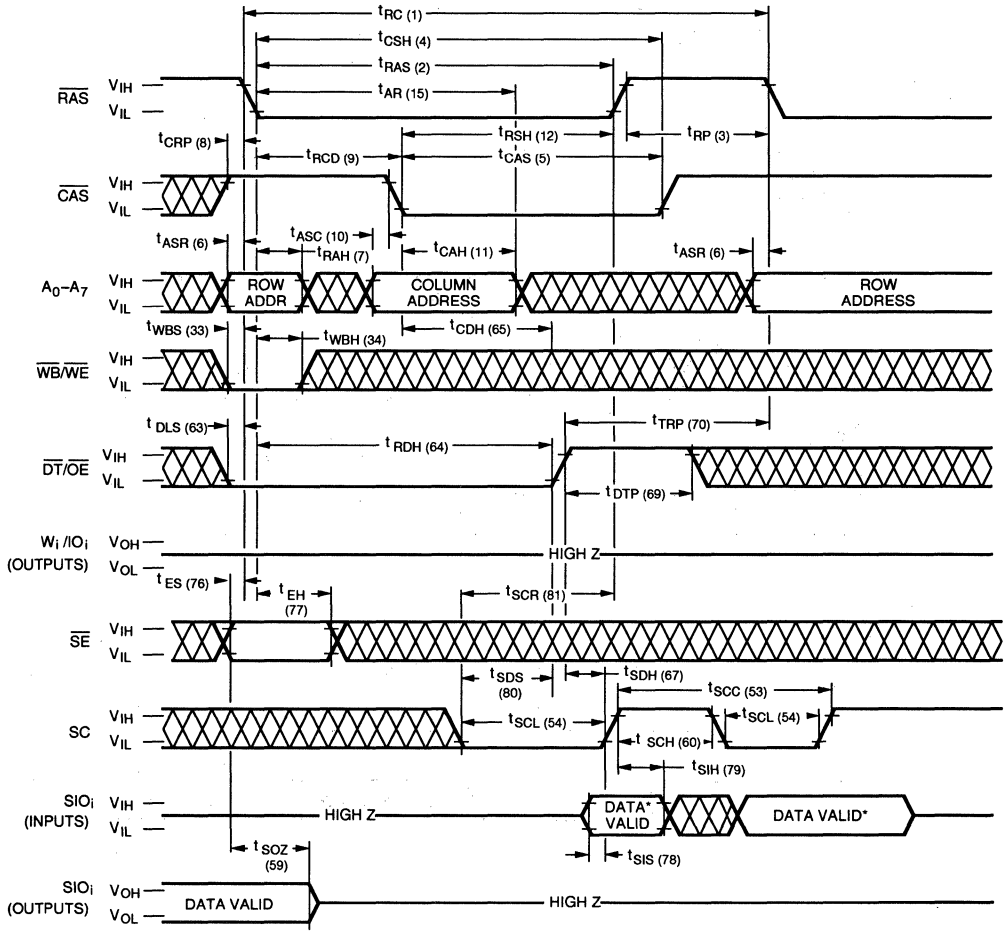
NOTE: * IN THE CASE THAT THE PREVIOUS TRANSFER IS WRITE TRANSFER.

869 15

Waveforms of Read Transfer Cycle (RAM-SAM) (Turbomode™)



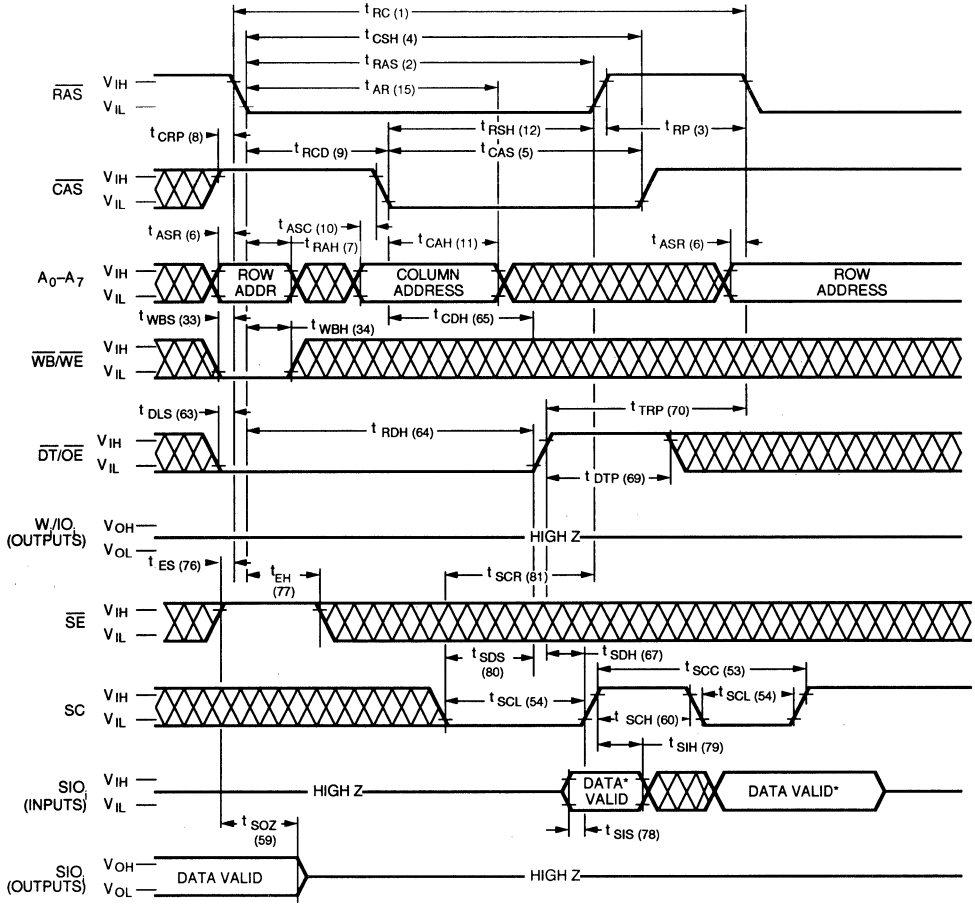
Waveforms of Write Transfer Cycle (SAM-RAM)



NOTE* IF $\overline{SE}$ IS "H" LEVEL, THE SERIAL INPUT DATA ARE NOT WRITTEN INTO THE DATA REGISTER, BUT THE SERIAL DATA SELECTOR CONTINUES TO FUNCTION.

869 17a

Waveforms of Pseudo Write Transfer Cycle Serial Write Setup



NOTE* IF $\overline{SE}$ IS "H" LEVEL, THE SERIAL INPUT DATA ARE NOT WRITTEN INTO THE DATA REGISTER, BUT THE SERIAL DATA SELECTOR CONTINUES TO FUNCTION.

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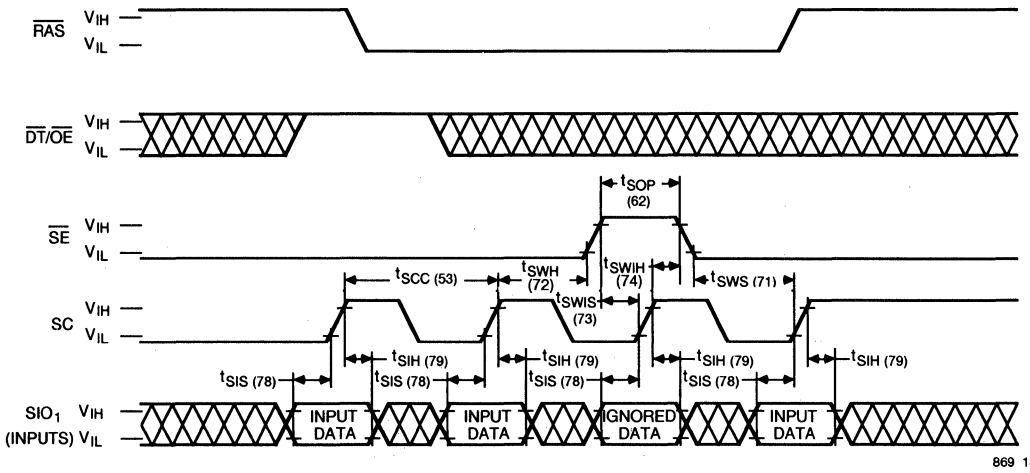
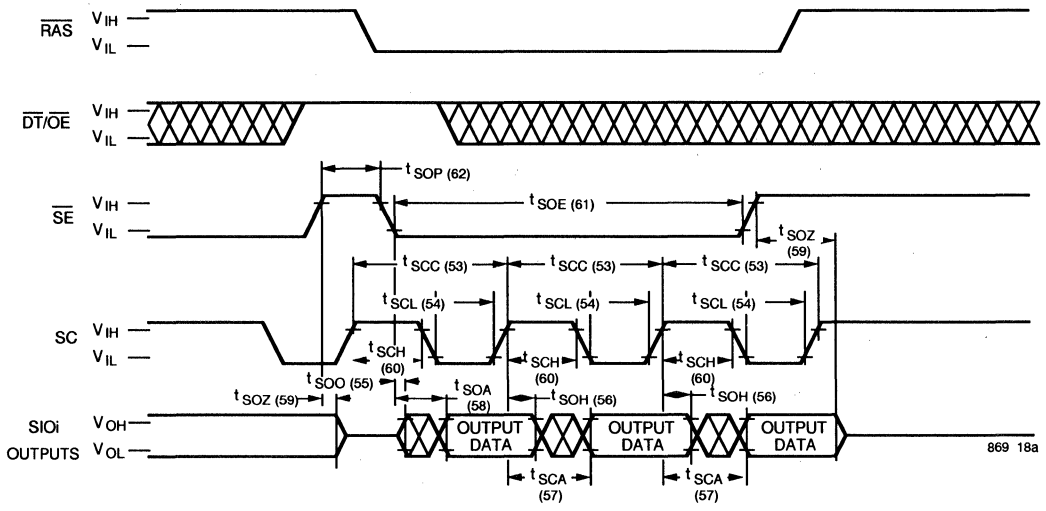
Waveforms of Serial Write Cycle



869 18

Waveforms of Serial Read Cycle



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Functional Description

RAM Operation

The V53C261 is a CMOS dynamic memory with 2 ports. One port, the RAM port, operates in the same way as the V53C464—64K x 4 DRAM. The other port, the Serial Access Port (SAM), allows data to be either read from or written to the memory at very high data rates.

The V53C261 reads and writes data via the RAM port by multiplexing a 16-bit address into an 8-bit row and an 8-bit column address. The Row Address Strobe ($\overline{RAS}$) latches the row address on chip. The column address, however, flows through the internal column address buffer and is latched by the Column Address Strobe ($\overline{CAS}$) signal. Because column access time becomes primarily dependent upon a valid column address rather than the falling edge of $\overline{CAS}$, signal timing restrictions on $\overline{CAS}$ can be greatly loosened with no effect on access time.

Memory Cycle

A memory cycle is initiated by the falling edge of $\overline{RAS}$. A memory cycle may not be ended or aborted prior to fulfilling the t_{RAS} (min) timing specification once it has been started. This precaution is necessary for proper device operation and integrity. A new memory cycle may not be started until the minimum precharge time t_{RP}/t_{CP} has been satisfied.

Read Cycle

A read cycle is a memory cycle in which data are retrieved from the memory array and presented on the W_i/IO_i pins. Read cycles can take the form of single operations to a specific row and column address or page mode accesses to any of 256 column addresses within a single row.

Write Cycle

A write cycle is a memory cycle in which data supplied externally to W_i/IO_i are written into the location in memory specified by the address. Using the masked write function, any combination of W_i/IO_i lines may be written and the remainder ignored. Write cycles can take the form of single operations to a specific row and column address or page mode accesses to any of 256 column addresses within a single row.

Refresh Cycle

To retain the data in a V53C261 DRAM a refresh operation activating each of the 256 row addresses must be performed at least once every 4 ms. Any operation such as read, write, RMW, $\overline{RAS}$-only cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle or transfer cycle refreshes the addressed row.

Fast Page Mode Operation

Fast Page Mode permits all 256 columns of 4-bits within a selected row of the V53C261 to be randomly accessed at a high data rate. After a normal cycle initiation, maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to resupply it. The column buffer acts as a transparent latch while $\overline{CAS}$ is high and, when $\overline{CAS}$ goes low, holds the addresses applied. Because of the transparent latches, the column address "flows through" and the read access begins upon stable addresses rather than the falling $\overline{CAS}$ edge. This eliminates t_{ASC} and t_T from the critical timing path and helps to speed up access while making operation simpler.

During a Fast Page Mode operation, read, write, read-modify-write, or read-write-read cycles are possible to random addresses within a selected row. Multiple operations to the same address are permitted as well as more than 256 accesses to any combination of addresses within the selected row. The only limiting factor to the number of such Page Mode accesses is consideration of refresh timing. Following the entry cycle into Page Mode, access time is t_{CAA} or t_{CAP}-dependent. If the column address is valid before or coincident with the rising edge of $\overline{CAS}$, then t_{CAP} is the access controlling parameter. If the column address is valid after the rising edge of $\overline{CAS}$, access time is determined by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output buffers.

With Fast Page Mode, very high sustained data rates can be achieved. The following equation can be used to calculate the data rate possible:

$$\text{Data Rate} = \frac{256}{t_{RC} + 255\, t_{PC}}$$

Mode Selection

RAM Operation to to be Performed	SAM Mode to be Entered	Control Signals (Sampled at the falling edge of $\overline{RAS}$)					$A_0 - A_7$ Sample Time	
		$\overline{CAS}$	$\overline{DT}/\overline{OE}$	$\overline{WB}/\overline{WE}$	$\overline{SE}$	W_i/IO_i	$\overline{RAS}$	$\overline{CAS}$
Read	Mode not affected	H	H	X	X	X	Row	Column Add.
Write	Mode not affected			H	X	X	Row	Column Add.
Bit Masked Write	Mode not affected			L	X	H*	Row	Column Add.
	Mode not affected			L	X	L*	Row	Column Add.
RAM → SAM Transfer	Output Mode		L	H	X	X	Row	SAM Start**
SAM → RAM Transfer	Input Mode			L	L	X	Row	SAM Start**
Pseudo Transfer	Input Mode			L	H	X	X	SAM Start**
$\overline{CAS}$-before-$\overline{RAS}$ or Hidden Refresh	Mode not affected	L	X	X	X	X	X	X

X = DON'T CARE

* The state of the W_i/IO_i lines is sampled at the falling edge of $\overline{RAS}$ to set the Write Bit Mask Register. If W_i/IO_i is high at the falling edge of $\overline{RAS}$, no masking action is taken and the corresponding data bit will be subject to change by a write operation. If W_i/IO_i is low at the falling edge of $\overline{RAS}$, the corresponding bit is masked and will not be altered by a write operation.

** The 8 address signals, $A_0 - A_7$, are used to select the RAM row address that will be affected by a transfer to or from the SAM and the starting address for a SAM read or write operation. The falling edge of $\overline{RAS}$ strobes the row address, and the falling edge of $\overline{CAS}$ strobes the SAM starting address.

Combined RAM-SAM Operation

Transfer

The transfer operation of the V53C261 allows a row (256 bits) of data to be transferred between RAM and SAM in either direction. The signals and states that control the transfer operation are specified in the Mode Selection Table.

To start a serial write operation, it is necessary to cause the SIO_0–SIO_3 pins of the SAM port to be in a high-Z state. The pseudo write transfer cycle accomplishes this purpose and must be performed any time the SAM mode is to be changed from read to write. No data transfer takes place, but addresses are set up as in any other transfer cycle. A read transfer cycle (RAM to SAM) changes the mode from write to read.

SAM Operation

General

The Serial Access Memory (SAM) of the V53C261 is organized as 256 words x 4 bits per word. It is possible to load the SAM from two sources: the RAM and the external serial I/O lines, SIO_i. SAM has two operational modes, read and write (viewed externally). Mode changes were described in the previous section.

When the SAM is in the read mode, data are first transferred from the RAM to SAM and then can be accessed serially via the SIO_i lines beginning with any SAM address. The progression of data output is from lower to higher numbered bits and addresses are modulo 256.

When the SAM is in the write mode, data are captured into the SAM using the SIO_i lines and can be written into a selected row in the RAM by a write transfer operation.

Read/Write

The SC pin is used as a 'shift clock' for the SAM port. Serial access is triggered by the rising edge of SC. When the SAM is in the write mode, the rising edge of SC causes data to be strobed into the selected cell of the SAM. In the read cycle, output data become valid after t_{SCA} from the rising edge of SC and remain valid until the next cycle. The SAM address is automatically incremented by SC.

The $\overline{SE}$ pin is used as an output/input enable pin for the SAM. It does not, however, gate the SC signal. The SAM address counter for read or write operations will continue to increment regardless of the state of $\overline{SE}$.

Turbomode Read Transfer

The V53C261 offers Turbomode real-time read transfer between RAM and SAM. By using the Turbomode feature, a continuous data stream can be generated even if the row address must be changed. No loss of timing is caused by Turbomode transfer. The data transfer from the RAM to SAM is triggered by the rising edge of $\overline{DT/OE}$ after the $\overline{RAS}$/$\overline{CAS}$ cycle has set up the data to be transferred and the start address. New row data is available for SAM output after $\overline{DT/OE}$ returns to a high state in compliance with specification parameters t_{SDD} and t_{SDH}. SC should be applied continuously and $\overline{DT/OE}$ timed from SC to achieve non-stop transfer.

Write Transfer

When the SAM has been placed into a write mode, and the required data have been captured via SIO_i, the write transfer operation will cause the content of the SAM to be written into the selected RAM row. After the write transfer cycle has been completed, more data can be written to the SAM via SIO_i.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified refresh interval. During Power-On, the V_{DD} current requirement of the V53C261 is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during Power-On, the device will go into an active cycle, and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

3

MULTIPORT VIDEO RAM WITH 256K X 4 DRAM AND 512 X 4 SAM

HIGH PERFORMANCE V52C4256	60	70	80	10
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	25 ns	25 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns	55 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	140 ns	150 ns	180 ns
Max. Serial Access Time, (t_{SCA})	25 ns	25 ns	25 ns	25 ns
Min. Serial Port Cycle Time, (t_{SCC})	30 ns	30 ns	30 ns	30 ns

Features

- Organization
  - RAM Port: 262,144 words x 4 bits
  - SAM Port: 512 words x 4 bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write, Write-Per-Bit
  - 512 Refresh Cycles/8 ms
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
  - Fully Static Register
- RAM-SAM Bidirectional Transfer
  - Read/Write/Pseudo Write Transfer
  - Real Time Read Transfer
- Low Power Dissipation
  - RAM Port Operating Alone – 85 mA
  - SAM Port Operating Alone – 50 mA
- Low CMOS Standby Current – 7 mA
- Package
  - 28 pin 400 mil SOJ
  - 28 pin 400 mil ZIP

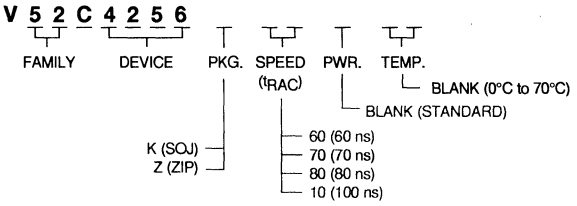
Description

The V52C4256 VRAM is equipped with a 262,144-words by 4-bits dynamic random access memory (RAM) port and a 512-words by 4-bits static serial access memory (SAM) port. The V52C4256 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

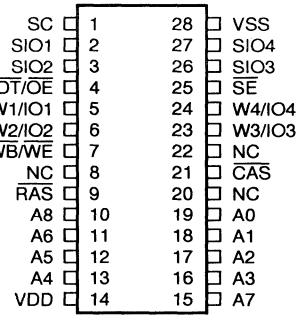
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power	Temperature Mark
	K	Z	60	70	80	100	Std	
0°C–70°C	•	•	•	•	•	•	•	Blank

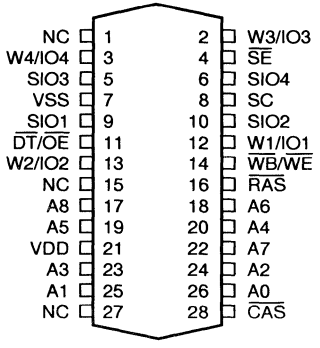
Description	Pkg.	Pin Count
SOJ	K	28
ZIP	Z	28



28 Lead Pin Configuration



K – SOJ



Z – ZIP

Pin Names

Name	Description
A0-A8	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
DT/OE	Data Transfer/Output Enable
WB/WE	Write per Bit/Write Enable
W1/IO1-W4/IO4	Write Mask/Data In, Out
SC	Serial Clock
SE	Serial Enable
SIO1-SIO4	Serial Input/Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 to +7.0 V
Short Circuit Out Current ..... 50 mA
Power Dissipation ..... 1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

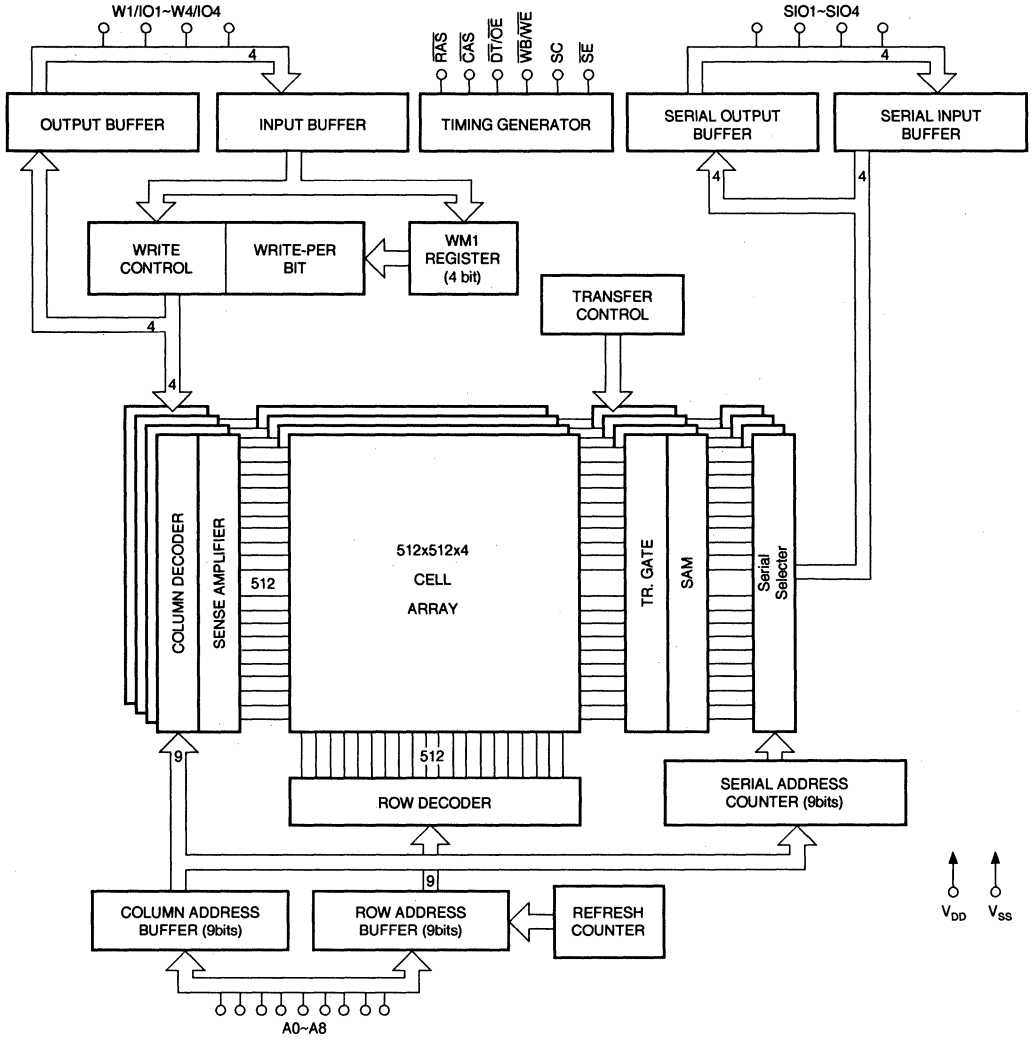
Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF

*Note: Capacitance is sampled and not 100% tested.

Functional Diagram



DC and Operating Characteristics

(V_{DD} = 5V ± 10%, T_A = 0–70°C)

Symbol	Parameter (RAM Port)	SAM Port	-60		-70		-80		-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
I_{DD1}	Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75		65	mA	1,2
I_{DD1A}		Active		130		120		110		100	mA	1,2
I_{DD2}	Standby Current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	Standby		7		7		7		7	mA	
I_{DD2A}		Active		55		50		45		40	mA	1,2
I_{DD3}	$\overline{RAS}$-Only Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH},	Standby		95		85		75		65	mA	1,2
I_{DD3A}	t_{RC} = t_{RC} Min.	Active		130		120		110		100	mA	1,2
I_{DD4}	Page Mode Current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling,	Standby		75		70		65		60	mA	1,2
I_{DD4A}	t_{PC} = t_{PC} Min.	Active		130		120		110		100	mA	1,2
I_{DD5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = t_{RC} Min.	Standby		95		85		75		65	mA	1,2
I_{DD5A}		Active		130		120		110		100	mA	1,2
I_{DD6}	Data Transfer Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75		65	mA	1,2
I_{DD6A}		Active		130		120		110		100	mA	1,2
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V		-10	10	-10	10	-10	10	-10	10	µA	
$I_{O(L)}$	Output Leakage Current 0V ≤ V_{OUT} ≤ 5.5V, Output Disable		-10	10	-10	10	-10	10	-10	10	µA	
V_{OH}	Output "H" Level Voltage I_{OUT} = -2 mA		2.4		2.4		2.4		2.4		V	
V_{OL}	Output "L" Level Voltage I_{OUT} = 2 mA			0.4		0.4		0.4		0.4	V	
V_{IH}	Input High Voltage		2.4	V_{DD}+1	2.4	V_{DD}+1	2.4	V_{DD}+1	2.4	V_{DD}+1	V	
V_{IL}	Input Low Voltage		-1.0	0.8	-1.0	0.8	-1.0	0.8	-1.0	0.8	V	

3

AC Electrical Characteristics *Notes: 3, 4, 5*

Symbol	Parameter	-60		-70		-80		-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	120		140		150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	175		195		195		235		ns	
t_{PC}	Fast Page Mode Cycle Time	40		45		50		55		ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85		90		90		100		ns	
t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	6,12
t_{AA}	Access Time from Column Address		30		35		40		50	ns	6,12
t_{CAC}	Access Time from $\overline{CAS}$		15		20		25		25	ns	6,13
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		35		40		45		50	ns	6,13
t_{OFF}	Output Buffer Turn-Off Delay	0	15	0	20	0	20	0	20	ns	8
t_T	Transition Time (Rise and Fall)	3	35	3	35	3	35	3	35	ns	5
t_{RP}	$\overline{RAS}$ Precharge Time	50		60		60		70		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode only)	60	100K	70	100K	80	100K	100	100K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15		20		25		25		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	20	10K	25	10K	25	10K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	55	20	75	ns	12
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		55		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		10		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10		10		10		ns	
t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		10		10		ns	
t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
t_{CAH}	Column Address Hold Time	10		15		15		15		ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50		55		55		70		ns	
t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		0		ns	9
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		0		0		ns	9
t_{WCH}	Write Command Hold Time	10		15		15		15		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50		55		55		70		ns	
t_{WP}	Write Command Pulse Width	10		15		15		15		ns	

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	-60		-70		-80		-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		25		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		25		ns	
t_{DS}	Data Setup Time	0		0		0		0		ns	10
t_{DH}	Data Hold Time	15		15		15		15		ns	10
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50		55		55		70		ns	
t_{WCS}	Write Command Setup Time	0		0		0		0		ns	11
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90		100		100		130		ns	11
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60		65		65		80		ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40		45		45		55		ns	11
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0		0		0		ns	
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0		0		0		ns	
t_{OEA}	Access Time from $\overline{OE}$		15		20		20		25	ns	6
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	0	10	0	10	0	10	0	20	ns	8
t_{OED}	$\overline{OE}$ to Data Delay Time	10		10		10		20		ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	10		10		10		20		ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10		15		15		15		ns	
t_{CSR}	$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		10		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0		0		0		ns	
t_{REF}	Refresh Period		8		8		8		8	ms	
t_{WSR}	$\overline{WB}$ Setup Time	0		0		0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	15		15		15		15		ns	
t_{MS}	Write-Per-Bit Mask Data Setup Time	0		0		0		0		ns	
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15		15		15		ns	
t_{THS}	$\overline{DT}$ High Setup Time	0		0		0		0		ns	
t_{THH}	$\overline{DT}$ High Hold Time	15		15		15		15		ns	
t_{TLS}	$\overline{DT}$ Low Setup Time	0		0		0		0		ns	
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10K	15	10K	15	10K	15	10K	ns	
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	55	10K	60	10K	65	10K	80	10K	ns	
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	20		25		30		30		ns	
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	15		20		25		25		ns	

AC Electrical Characteristics (Cont'd)

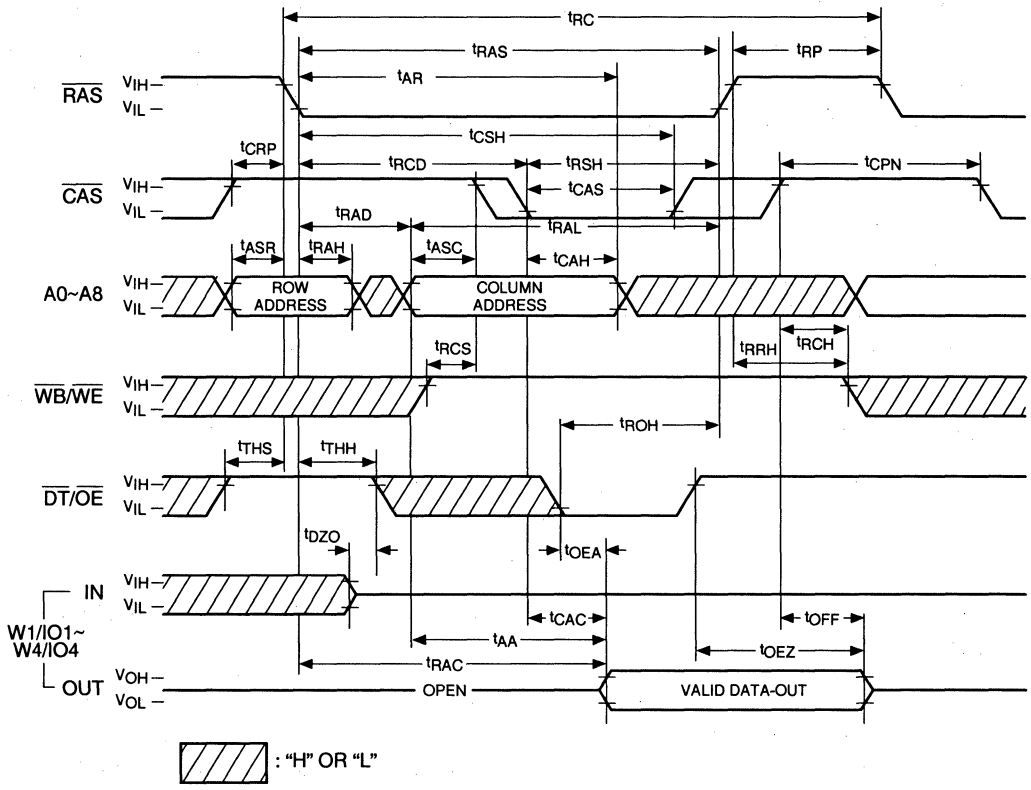
Symbol	Parameter	-60		-70		-80		-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{ESR}	$\overline{SE}$ Setup Time referenced to $\overline{RAS}$	0		0		0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15		15		15		ns	
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	50		60		60		70		ns	
t_{TP}	$\overline{DT}$ Precharge Time	20		20		20		30		ns	
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	65		70		80		100		ns	
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	40		45		45		50		ns	
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	20		20		25		25		ns	
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5		5		5		ns	
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15		15		15		ns	
t_{SRS}	Last SC to $\overline{RAS}$ Setup Time (Serial Input)	20		25		25		30		ns	
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	20		20		20		25		ns	
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	40		40		40		50		ns	
t_{SDZ}	Serial Output Buffer Turn-Off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	40	10	40	10	40	10	50	ns	8
t_{SCC}	SC Cycle Time	30		30		30		30		ns	
t_{SC}	SC Pulse Width (SC High Time)	10		10		10		10		ns	
t_{SCP}	SC Precharge Time (SC Low Time)	10		10		10		10		ns	
t_{SCA}	Access Time from SC		25		25		25		25	ns	7
t_{SOH}	Serial Output Hold Time from SC	5		5		5		5		ns	
t_{SDS}	Serial Input Setup Time	0		0		0		0		ns	
t_{SDH}	Serial Input Hold Time	15		15		15		15		ns	
t_{SEA}	Access Time from $\overline{SE}$		25		25		25		25	ns	7
t_{SE}	$\overline{SE}$ Pulse Width	25		25		25		25		ns	
t_{SEP}	$\overline{SE}$ Precharge Time	25		25		25		25		ns	
t_{SEZ}	Serial Output Buffer Turn-Off Delay from $\overline{SE}$	0	20	0	20	0	20	0	20	ns	8
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0		0		0		ns	
t_{SZS}	Serial Input to First SC Delay Time	0		0		0		0		ns	
t_{SWS}	Serial Write Enable Setup Time	5		5		5		5		ns	
t_{SWH}	Serial Write Enable Hold Time	15		15		15		15		ns	
t_{SWIS}	Serial Write Disable Setup Time	5		5		5		5		ns	
t_{SWIH}	Serial Write Disable Hold Time	15		15		15		15		ns	

Notes

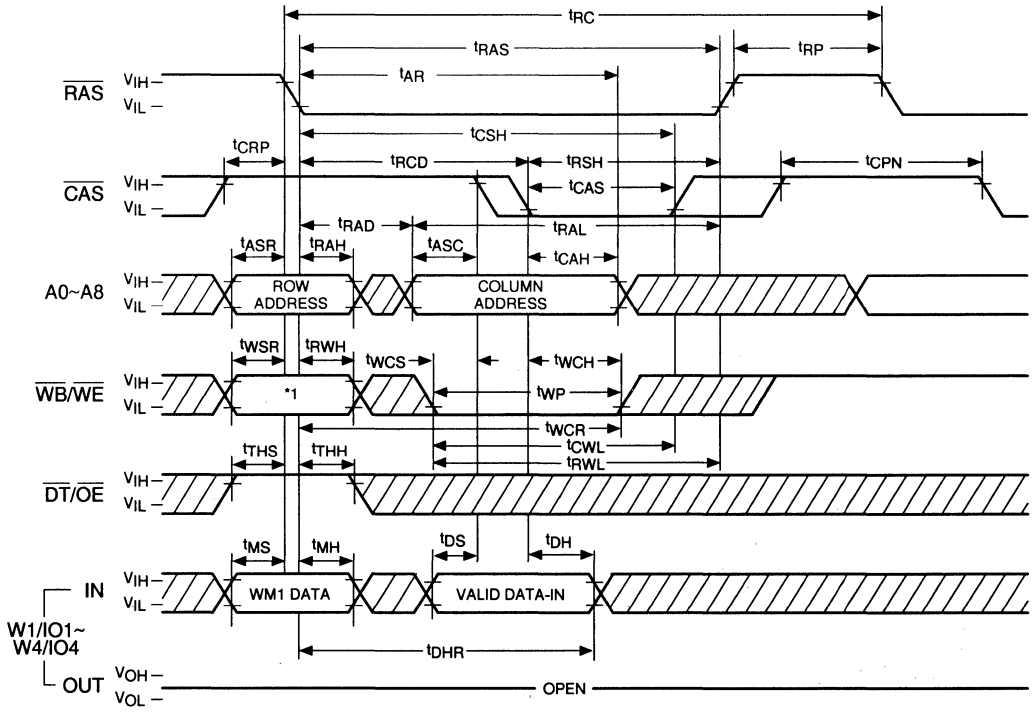
1. These parameters depend on cycle rate.
2. These parameters depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC measurements assume t_T = 5 ns.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. RAM port outputs are measured with a load equivalent to 1 TTL load and 100 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
7. SAM port outputs are measured with a load equivalent to 1 TTL load and 30 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
8. t_{OFF} (max.), t_{OEZ} (max.), t_{SDZ} (max.) and t_{SEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
12. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

Read Cycle



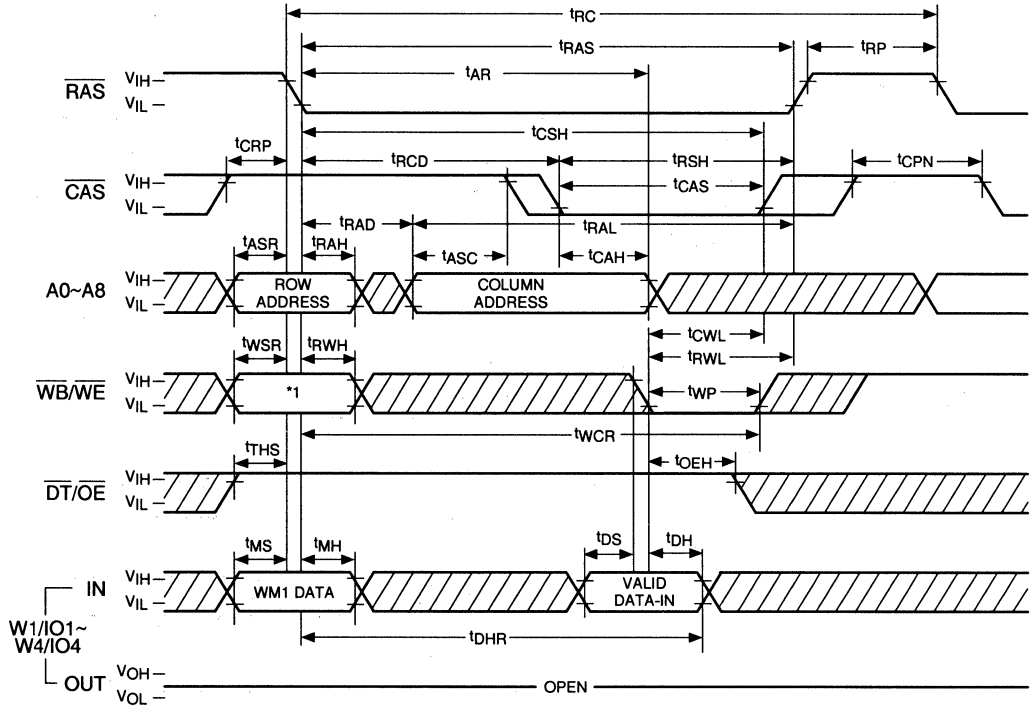
Write Cycle (Early Write)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

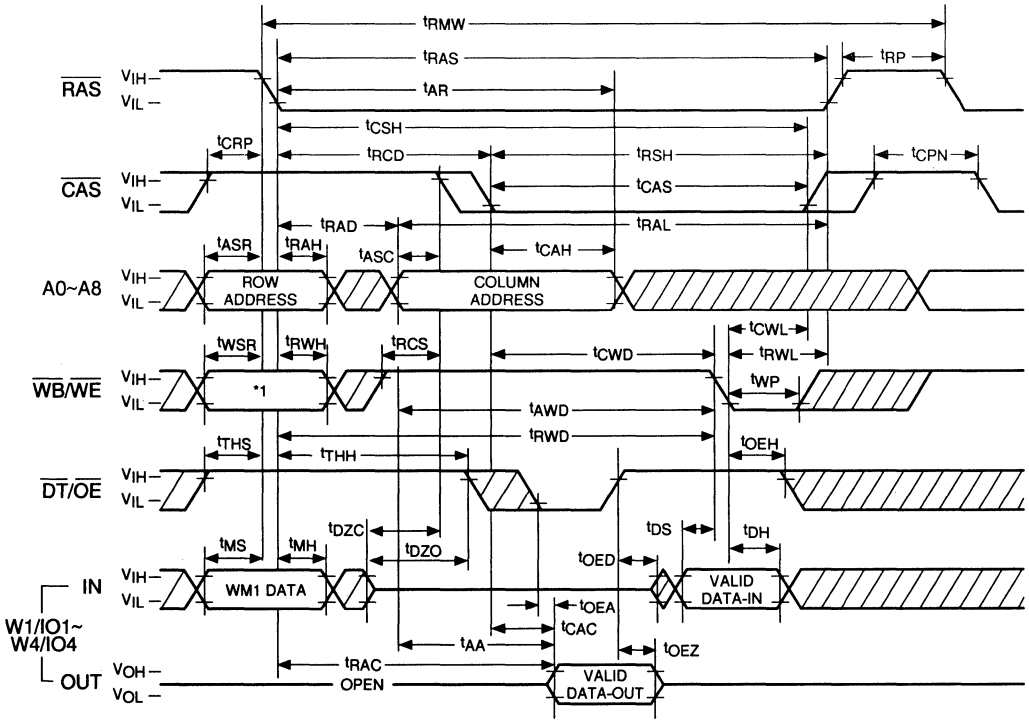
Write Cycle ($\overline{OE}$ Controlled Write)



*1 $\overline{WB/WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

Read-Modify-Write Cycle

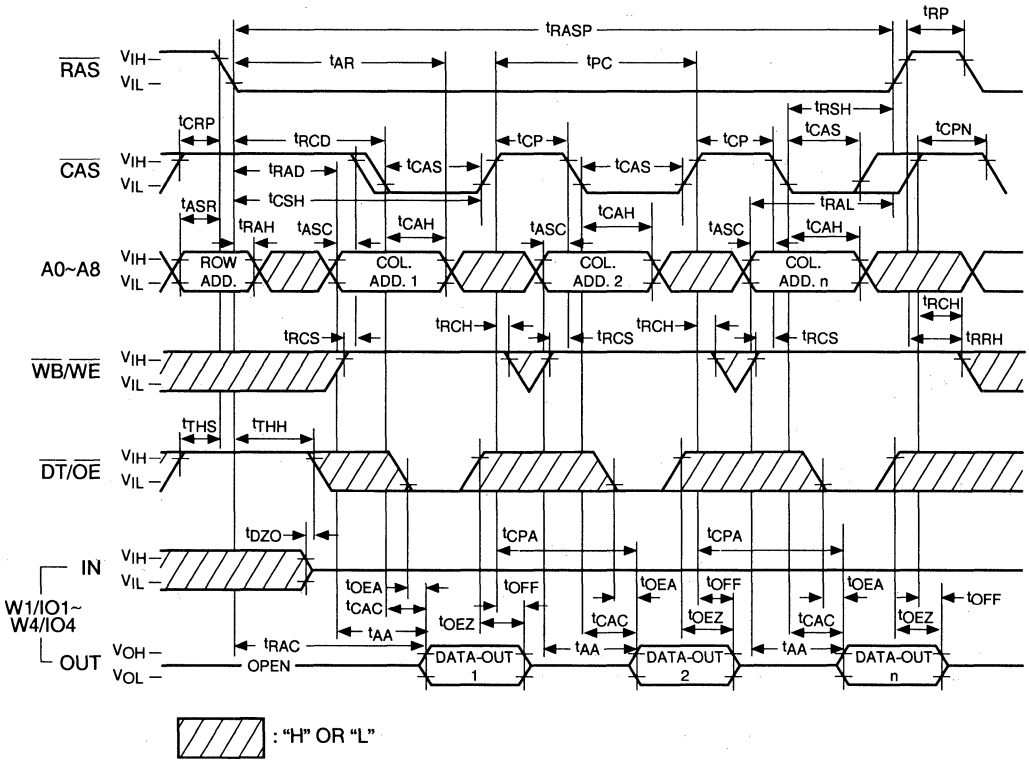


*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

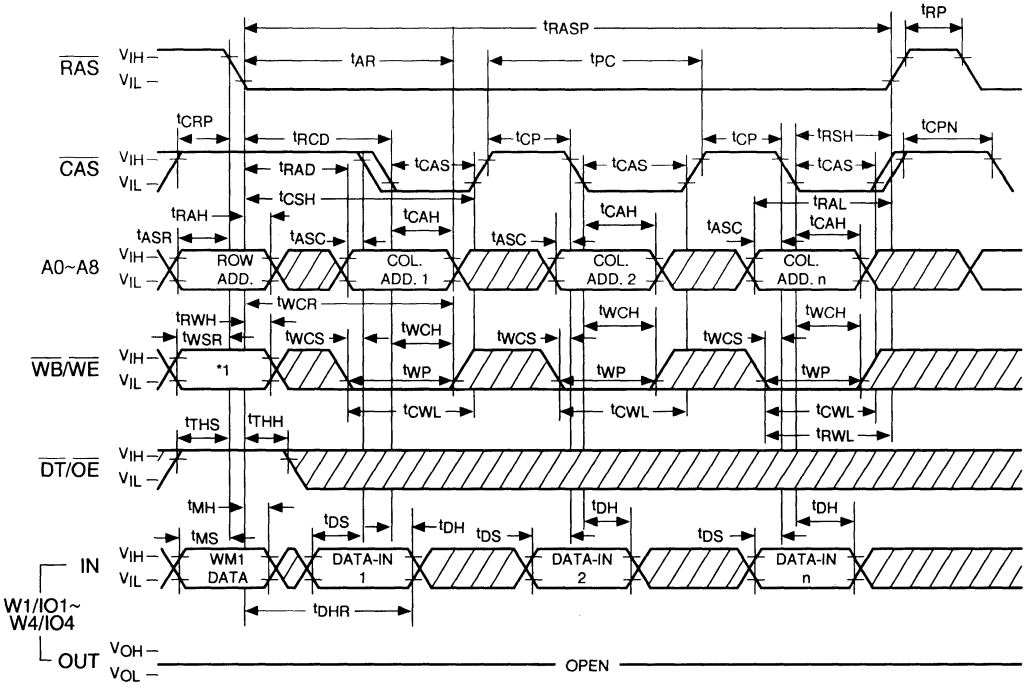
WM1 data: 0: Write Disable
1: Write Enable

: "H" OR "L"

Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)

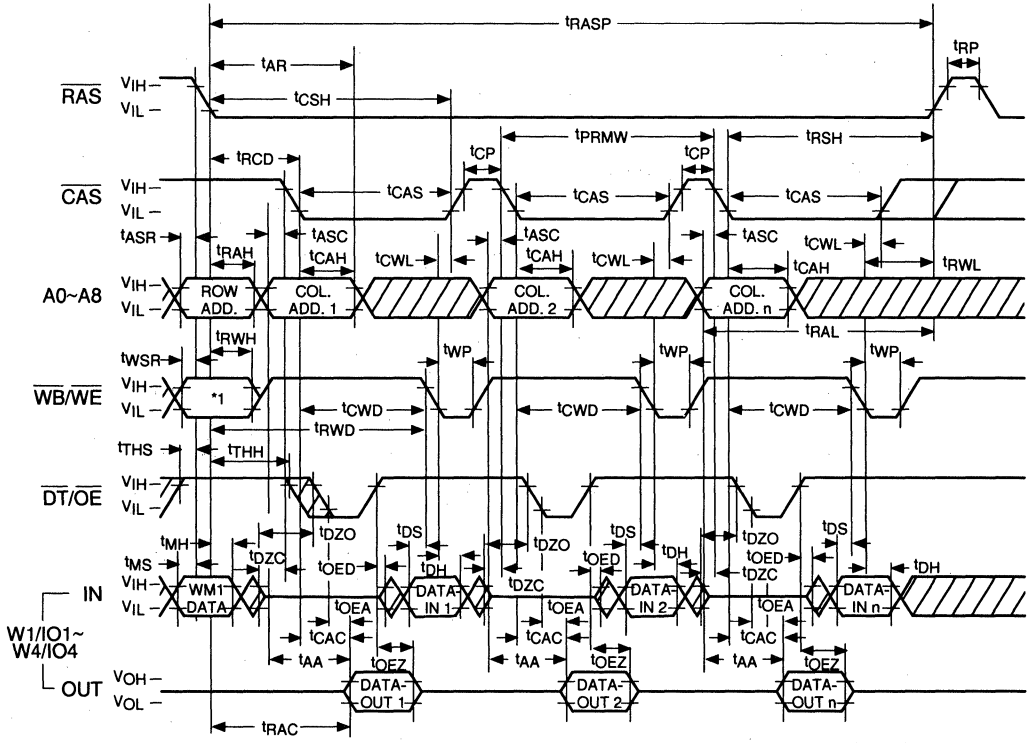


: "H" OR "L"

*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

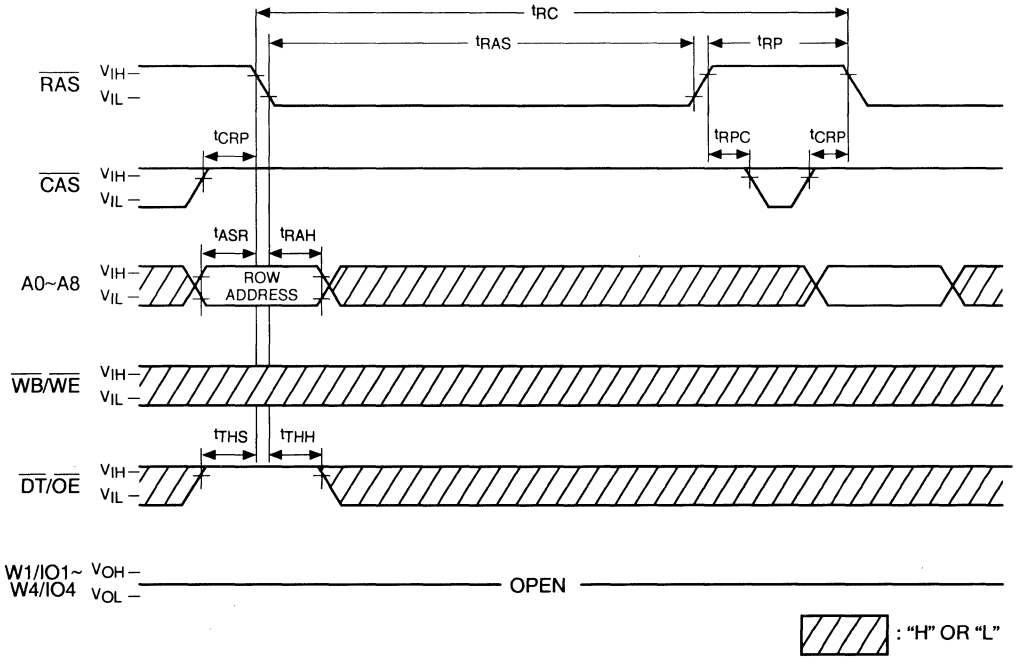
Fast Page Mode Read-Modify-Write Cycle



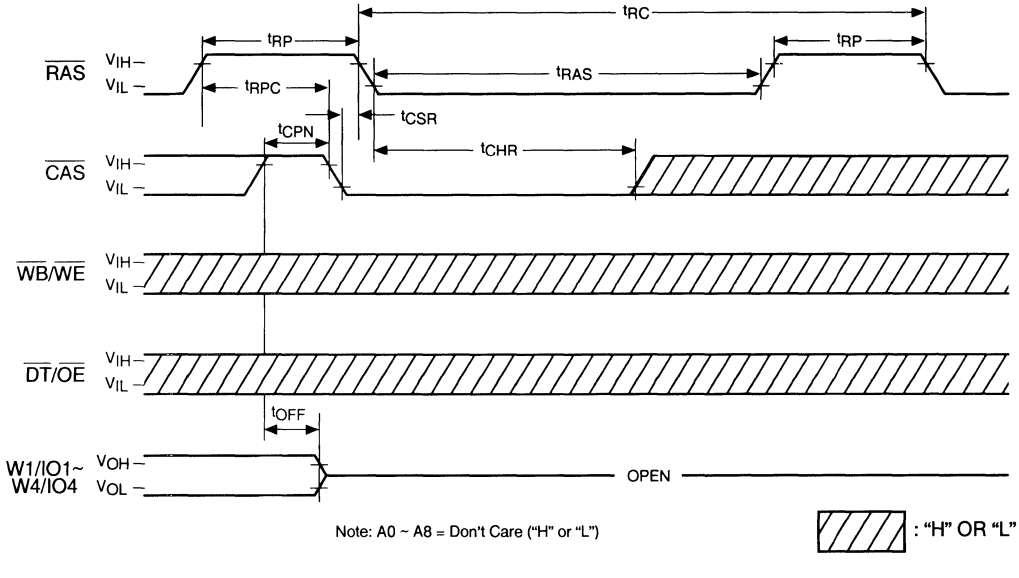
*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

$\overline{RAS}$ Only Refresh Cycle

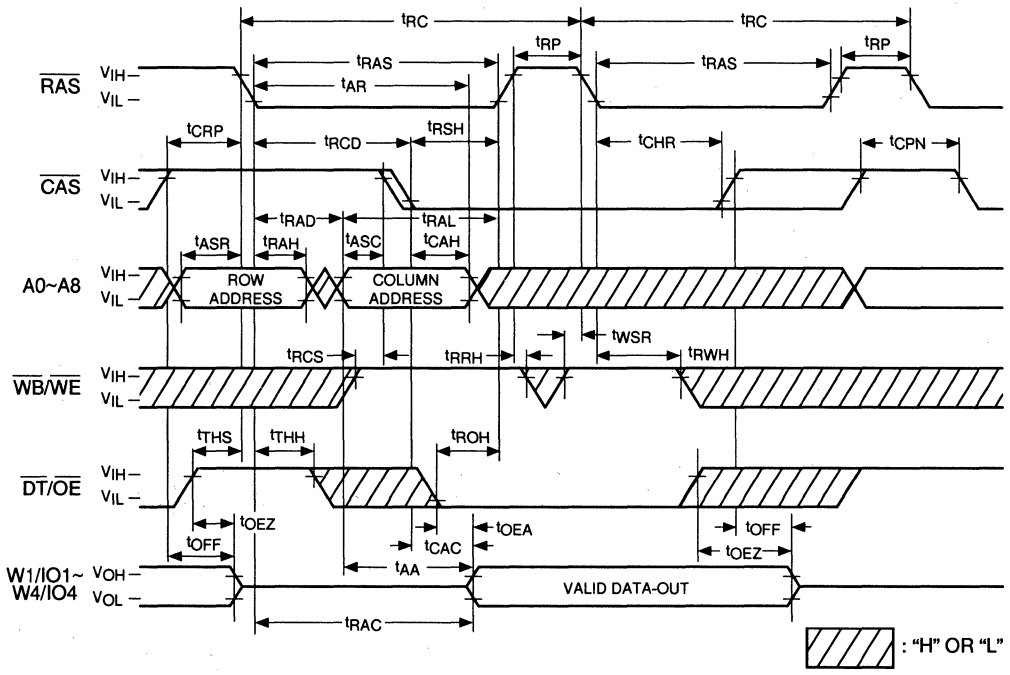


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

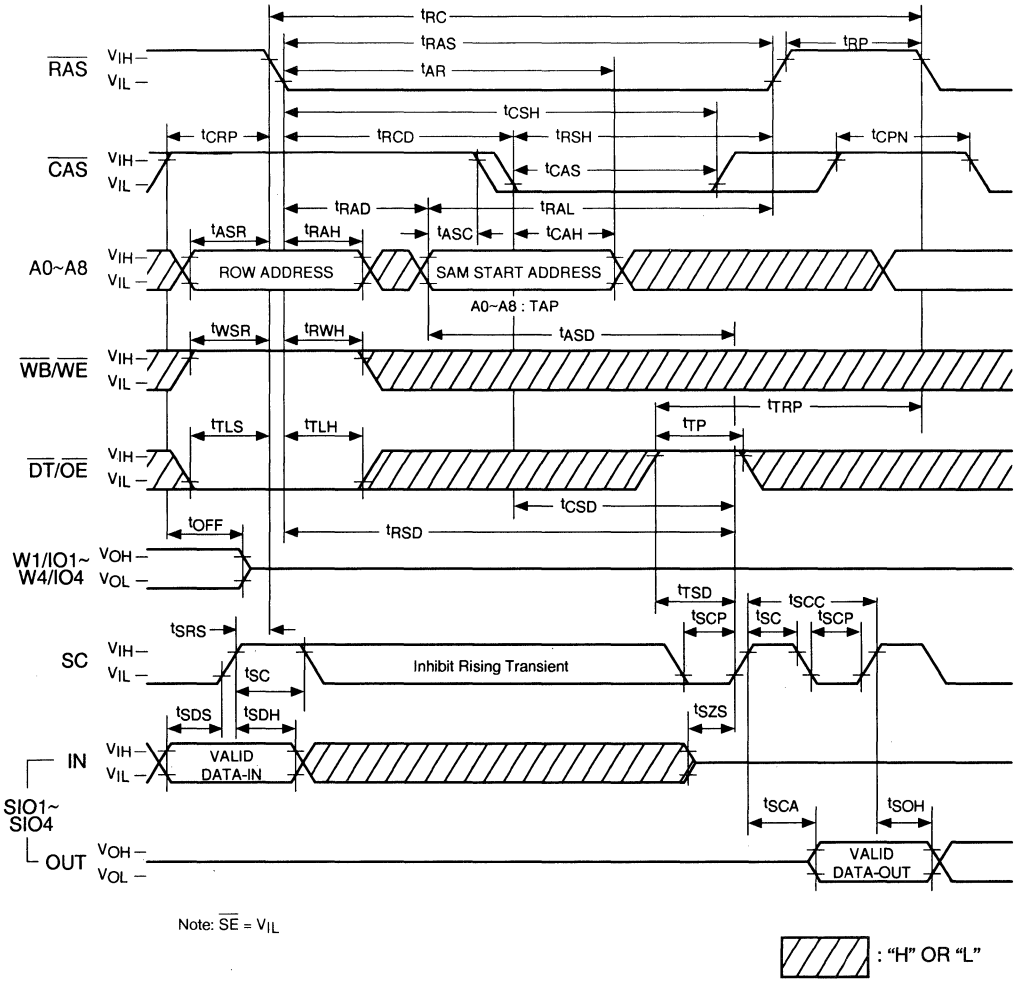


Note: A0 ~ A8 = Don't Care ("H" or "L")

Hidden Refresh Cycle



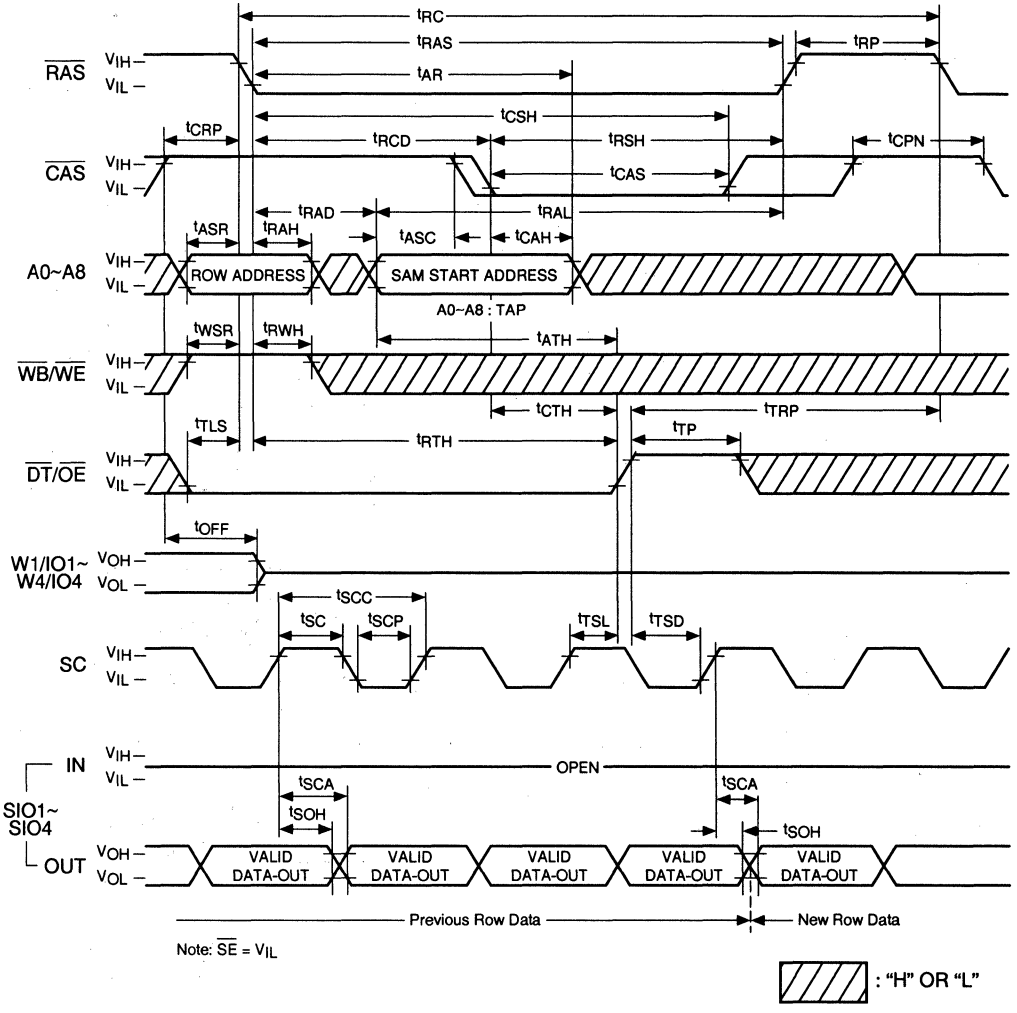
Read Transfer Cycle (Previous Transfer is Write Transfer Cycle)



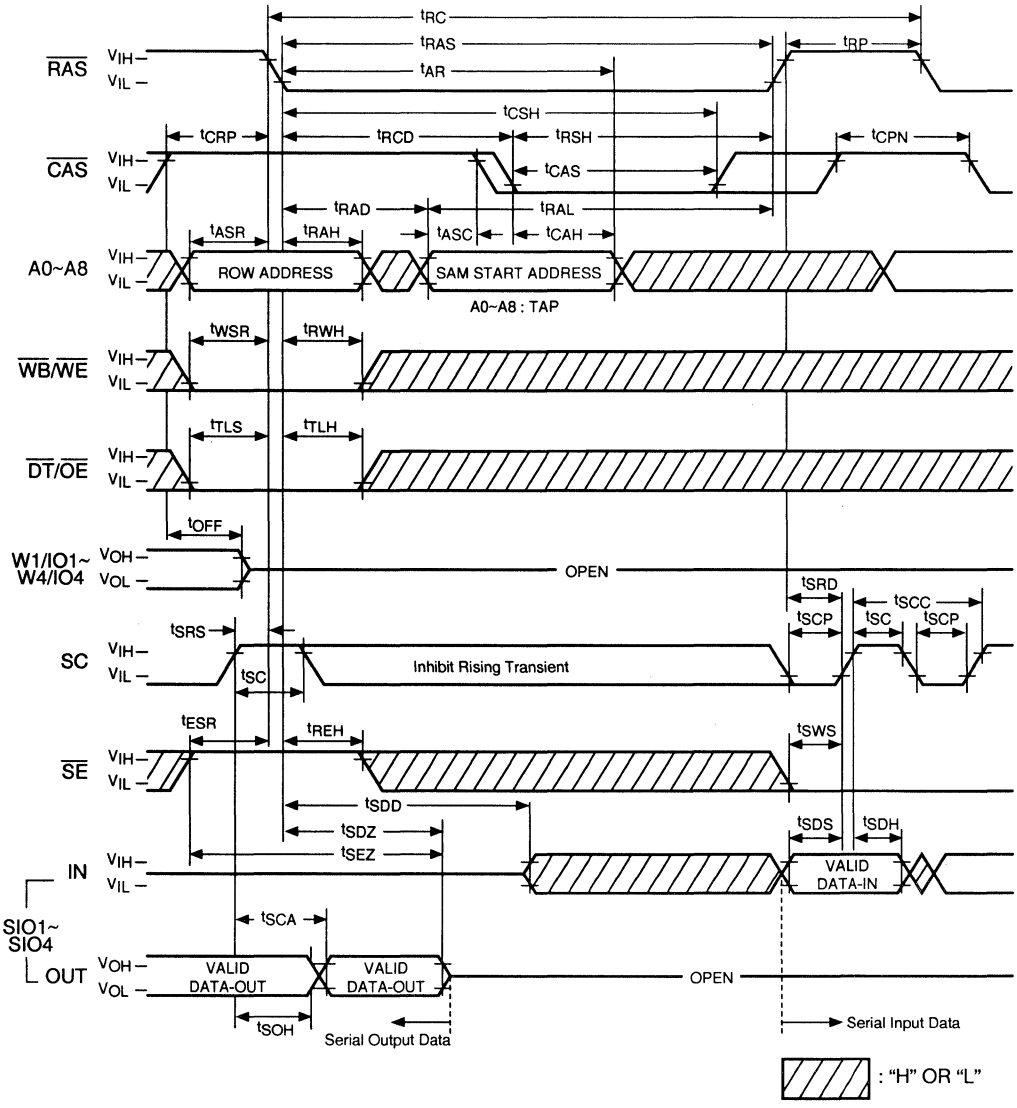
Note: $\overline{SE}$ = V_{IL}

: "H" OR "L"

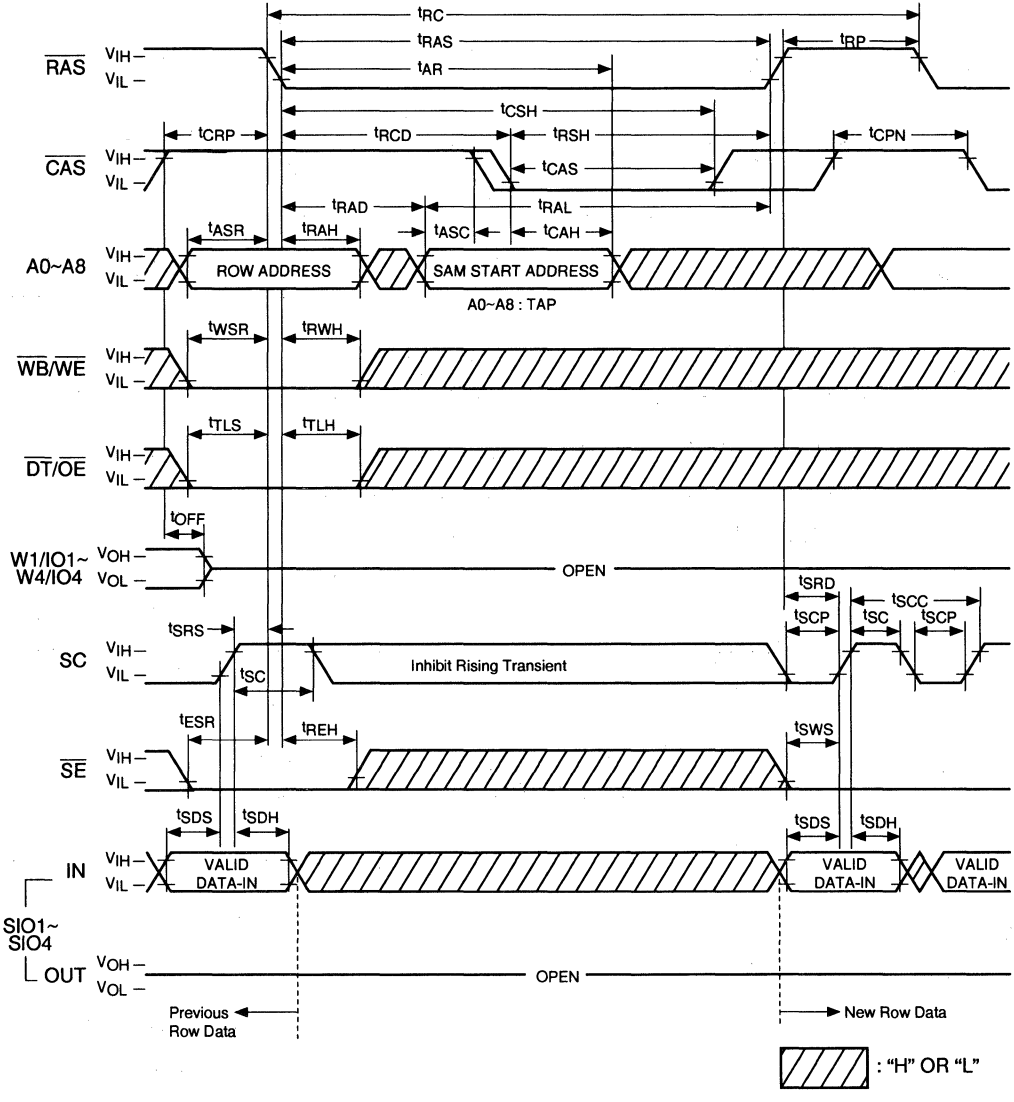
Real Time Read Transfer Cycle



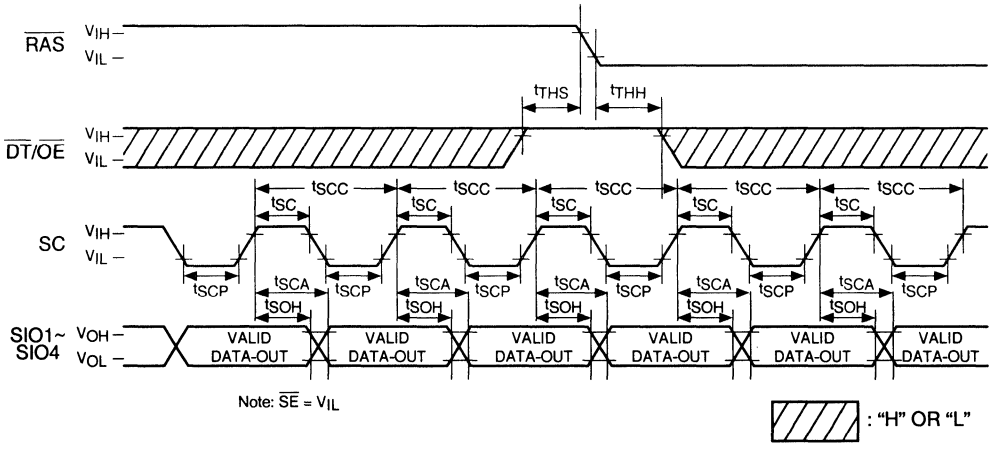
Pseudo Write Transfer Cycle



Write Transfer Cycle

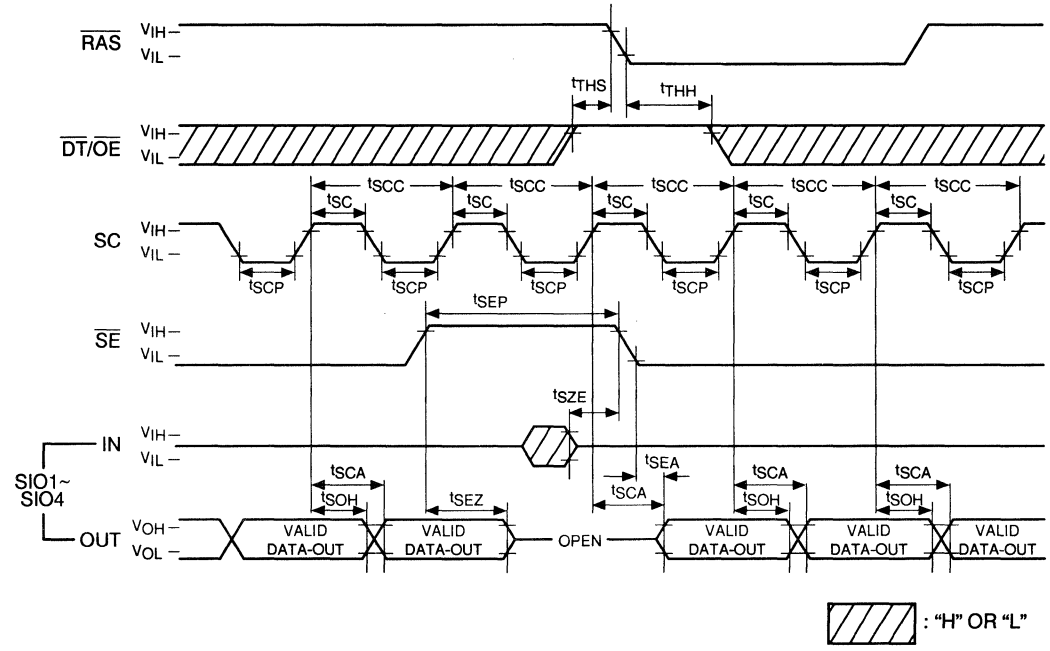


Serial Read Cycle ($\overline{SE}$ = V_{IL})

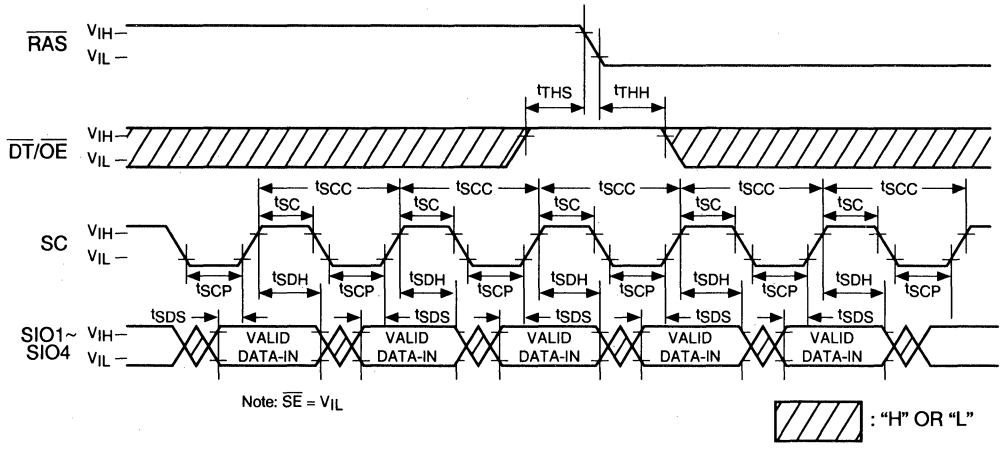


3

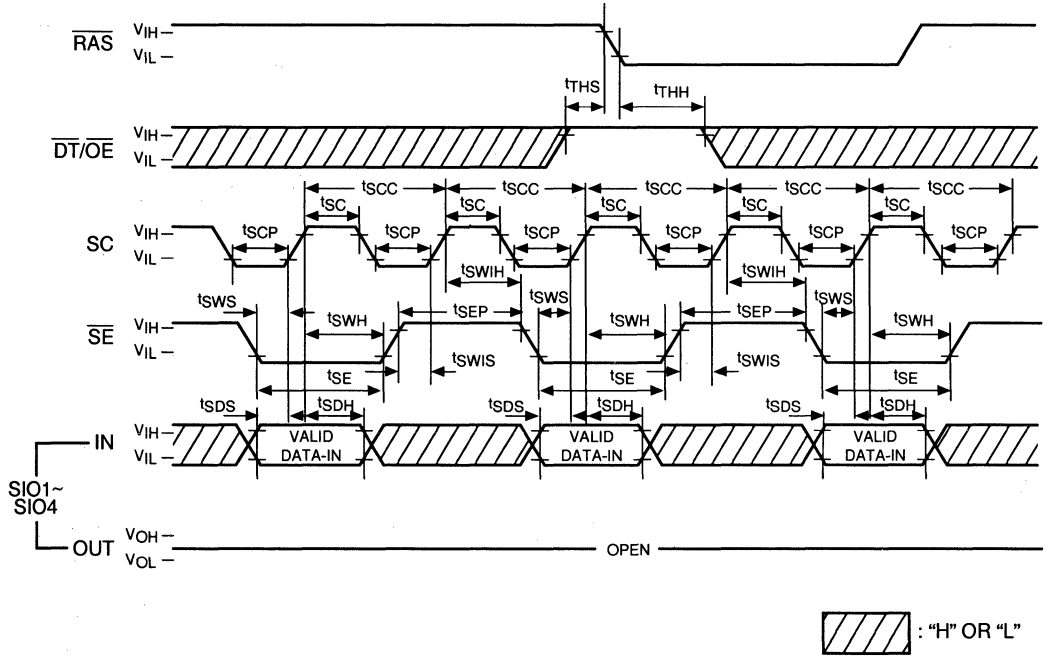
Serial Read Cycle ($\overline{SE}$ Controlled Outputs)



Serial Write Cycle ($\overline{SE}$ = V_{IL})



Serial Write Cycle ($\overline{SE}$ Controlled Inputs)



Pin Functions

Address Inputs: A0–A8

The 18 address bits required to decode 4 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the V52C4256 are multiplexed onto 9 address input pins (A_0–A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

Row Address Strobe: $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$ and $\overline{SE}$ to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

Column Address Strobe: $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

Data Transfer/Output Enable: $\overline{DT/OE}$

The $\overline{DT/OE}$ input is a multifunction pin. When $\overline{DT/OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT/OE}$ is used as an output enable control. When the $\overline{DT/OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

Write Per Bit/Write Enable: $\overline{WB/WE}$

The $\overline{WB/WE}$ input is also a multifunction pin. When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB/WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).

When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write transfer).

Write Mask Data/Data Input and Output: W_1/IO_1–W_4/IO_4

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB/WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT/OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT/OE}$, whichever occurs first.

Serial Clock: SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the normal transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0). The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read/pseudo write/write transfer operations and should not be clocked while the SAM port is in the standby mode, to prevent the SAM pointer from being incremented.

Serial Enable: $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

Serial Input/Output: SIO1–SIO4

Serial input and output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During the subsequent write transfer cycle, the SAM remains in the input mode.

Operation Mode

The RAM port and data transfer operating of the V52C4256 are determined by the state of $\overline{CAS}$, $\overline{DT}$/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$ and $\overline{SE}$ at the falling edge of $\overline{RAS}$. Table 1 and Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operations, respectively.

Table 1. Operation Truth Table

$\overline{RAS}$ Falling Edge ↓				
$\overline{CAS}$	$\overline{DT}$/$\overline{OE}$	$\overline{WB}$/$\overline{WE}$	$\overline{SE}$	Function
0	•	•	•	$\overline{CAS}$-before-$\overline{RAS}$ Refresh
1	0	0	0	Write Transfer
1	0	0	1	Pseudo Write Transfer
1	0	1	•	Read Transfer
1	1	0	•	Read/Write per Bit
1	1	1	•	Read/Write

Table 2. Functional Truth Table

Function	$\overline{RAS}$↓				Address		W/IO		Write Mask
	$\overline{CAS}$	$\overline{DT}$/$\overline{OE}$	$\overline{WB}$/$\overline{WE}$	$\overline{SE}$	$\overline{RAS}$↓	$\overline{CAS}$↓	$\overline{RAS}$↓	$\overline{CAS}$↓ $\overline{WE}$↓	WM1
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	0	•	•	•	•	–	•	–	–
Write Transfer	1	0	0	0	Row	TAP	•	•	–
Pseudo Write Transfer	1	0	0	1	Row	TAP	•	•	–
Read Transfer	1	0	1	•	Row	TAP	•	•	–
Write per Bit	1	1	0	•	Row	Column	WM1	DIN	Load use
Read/Write	1	1	1	•	Row	Column	•	DIN	–

Note: • = "0" or "1", TAP = SAM Start Address, – = not used.

RAM Port Operation

Fast Page Mode Cycle

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycles during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 µs. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT/OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT/OE}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-Only Refresh

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with the "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

The V52C4256 also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

Hidden Refresh

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (refer to Figure 1).

Write-Per-Bit Function

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB/WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched into the write-mask register (WM1). When a "0" is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written. When an "1" is sensed on any of the W_i/IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

At the falling edge of $\overline{RAS}$				
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	Wi/IOi (i = 1–4)	Function
H	H	H	•	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

Table 3. Truth Table for Write-Per-Bit Function

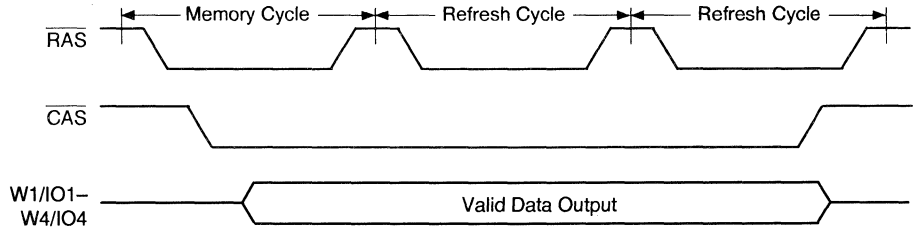


Figure 1. Hidden Refresh Cycle

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

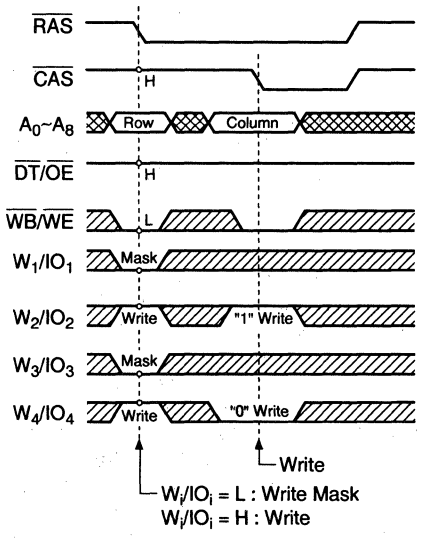


Figure 2. Write-per-bit timing cycle

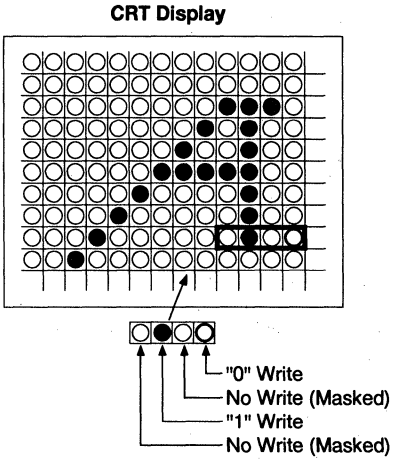


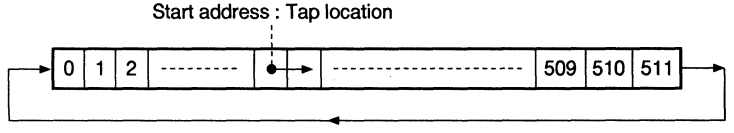
Figure 3. Corresponding bit-map

SAM Port Operation

The V52C4256 is provided with a 512 words by 4 bits serial access memory (SAM).

High speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read/write/pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM → SAM) has been performed. The data is shifted out of the SAM port starting at any of the 512 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit, and then wraps around to the least significant bit, as illustrated below.



Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode, in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

SAM Port Operation	$\overline{DT/OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	Function	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode	H	⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode	H	⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

Table 4. Truth Table for SAM Port Operation

Refresh

The SAM data registers are static flip-flop, therefore a refresh is not required.

Data Transfer Operation

The V52C4256 features the internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 4. During a normal transfer, 512 wors by 4 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer).

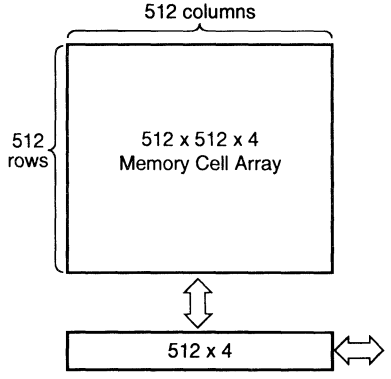


Figure 4. Data Transfer

As shown in Table 5, the V52C4256 supports three types of transfer operations: read transfer, write transfer, and pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT/OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB/WE}$ and $\overline{SE}$ which are latched at the falling edge of $\overline{RAS}$. During data transfer operations, the SAM port is switched from input to output mode (Read Transfer) or output to input mode (Write Transfer/ Pseudo Write Transfer). During a data transfer cycle, the row address A_0–A_8 selects one of the 512 rows of the memory array to or from which data will be transferred, and the column address A_0–A_8 selects one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle.

At the falling edge of $\overline{RAS}$							
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	$\overline{SE}$	Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
H	L	H	•	Read Transfer	RAM → SAM	512 x 4	Input → Output
H	L	L	L	Write Transfer	SAM → RAM	512 x 4	Output → Input
H	L	L	H	Pseudo Write Transfer	—	—	Output → Input

Note: • = "H" or "L"

Table 5. Transfer Modes

Read Transfer Cycle

A read transfer cycle consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low" and $\overline{WB/WE}$ "high" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT/OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT/OE}$ and this data becomes valid on the SIO lines after the specified access time (t_{SCA}) from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 5 shows the operation block diagram for the read transfer operation.

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay (t_{TSD}) from the rising edge of $\overline{DT/OE}$, as shown in Figure 6.

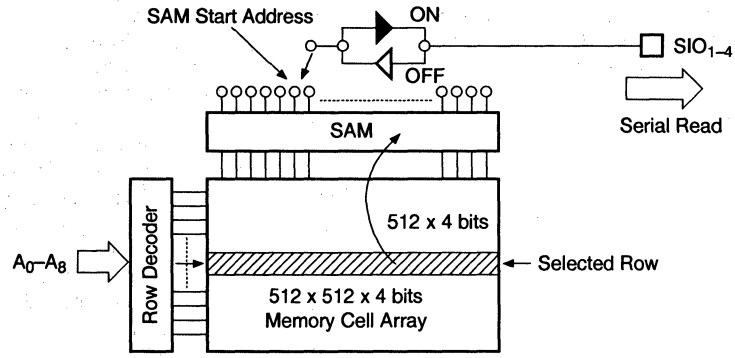


Figure 5. Block Diagram for Read Transfer Operation

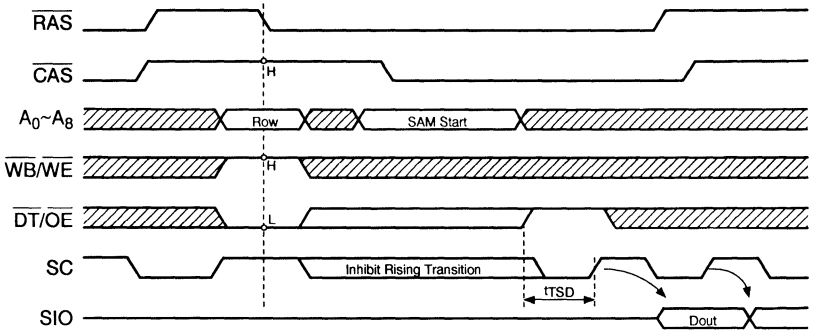


Figure 6. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the DT/OE signal goes "high" and the serial access time (t_{SCA}) for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of DT/OE must be synchronized with RAS, CAS and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 7.

The timing restrictions t_{TSL}/t_{TSD} are 5ns min/15ns min.

Write Transfer Cycle

A write transfer cycle consists of loading the contents of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding CAS "high", DT/OE "low", WB/WE "low", and SE "low" at the falling edge of RAS. Figures 8 and 9 show the timing diagram and block diagram for write transfer operations, respectively.

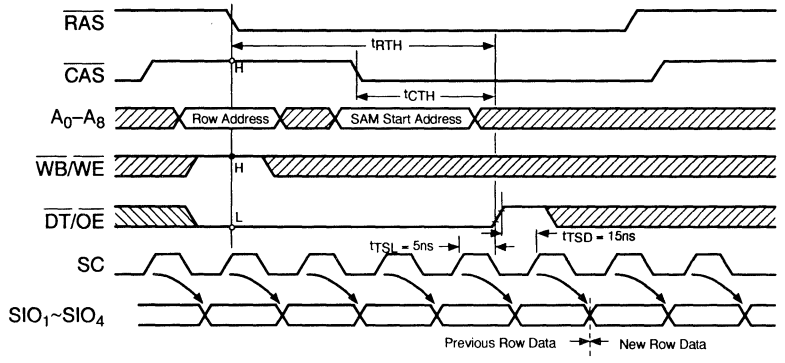


Figure 7. Real Time Read Transfer

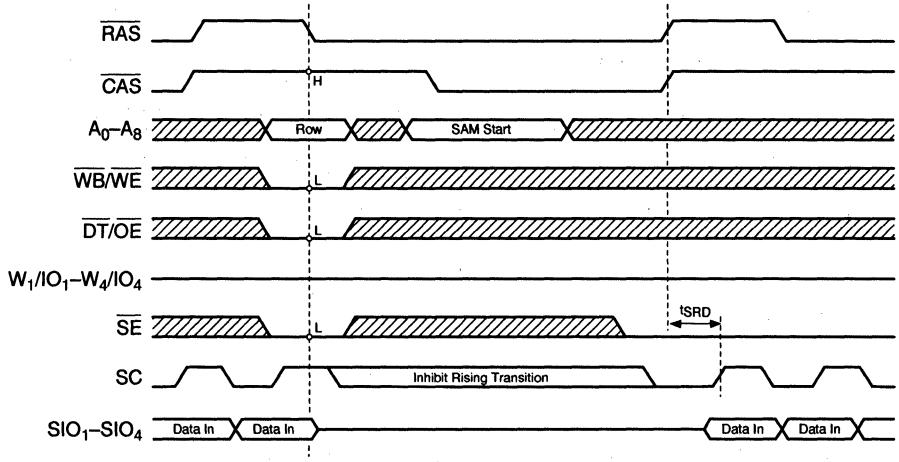


Figure 8. Write Transfer Timing

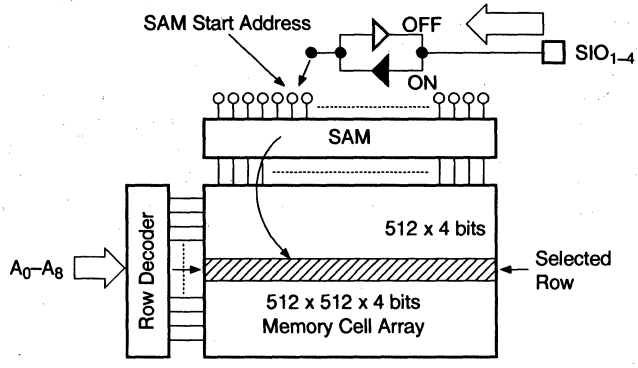


Figure 9. Block Diagram for Write Transfer Operation

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determies the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay (t_{SRD}) from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

Pseudo Write Transfer Cycle

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (a data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low", $\overline{WB/WE}$ "low" and $\overline{SE}$ "high" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

Register Operation Sequence - Example

Figure 10 illustrates an example of register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly intialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location, which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 511), and wraps around to the least significant address location. The SAM address is incremented as long as SC is clocked.

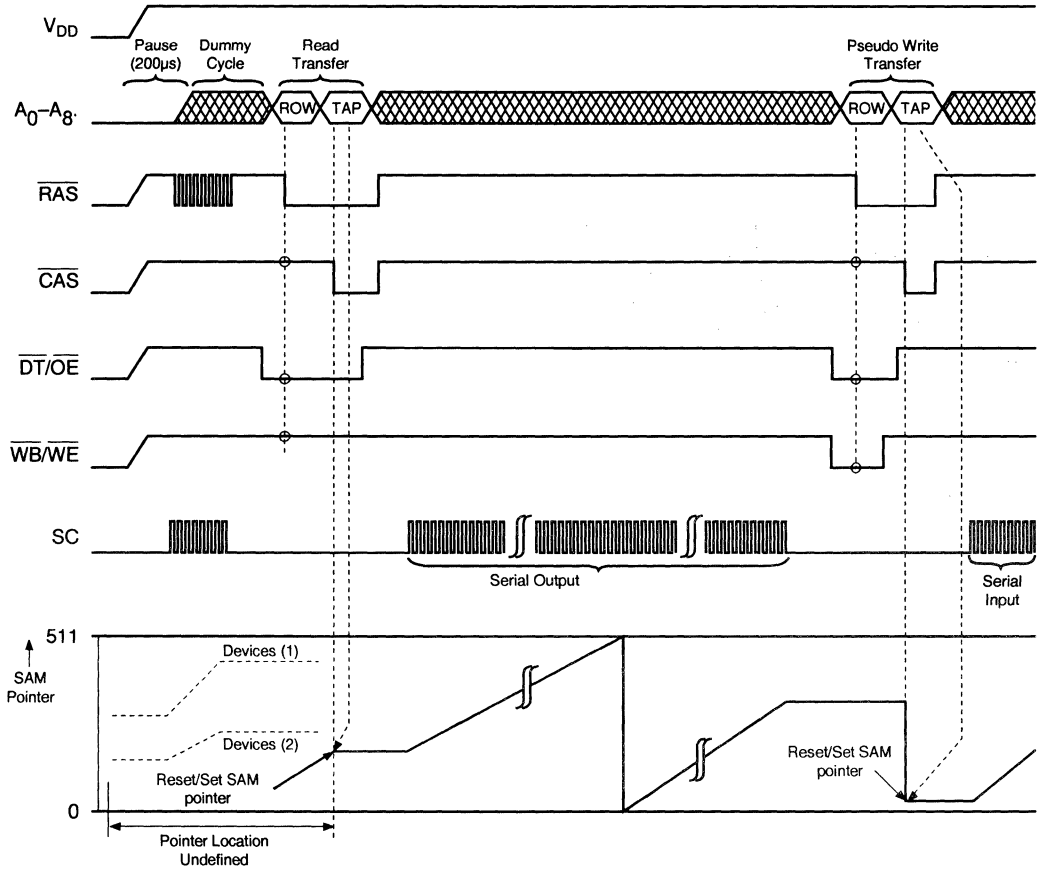
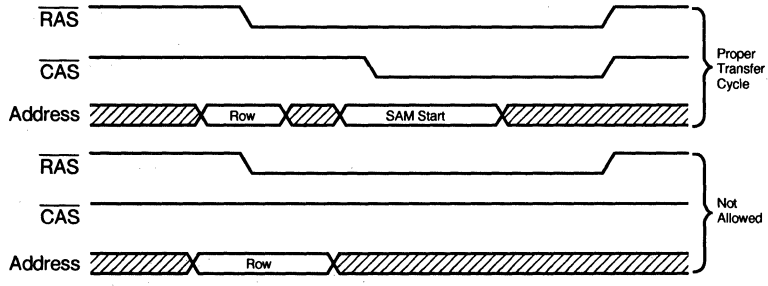


Figure 10. Example of SAM Register Operation Sequence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

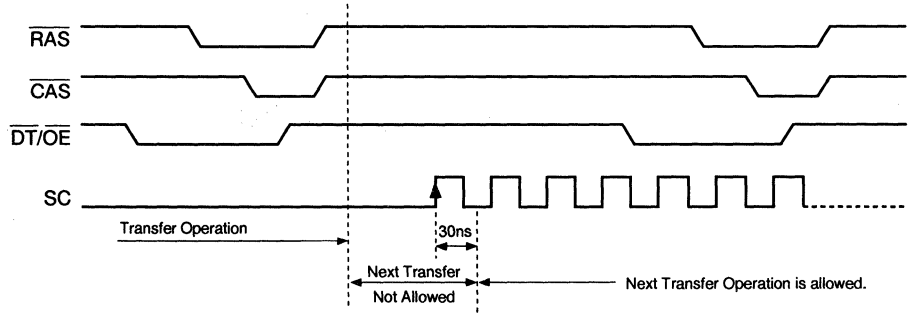
Transfer Operation Without $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column addresses are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore, a transfer cycle with $\overline{CAS}$ held "high" is not allowed (refer to the illustration below).



Read Transfer Cycle After Read Transfer Cycle

Another read transfer may be performed following the read transfer provided that a minimum delay of 30 ns from the rising edge of the first clock SC is satisfied (refer to the illustration shown below).



Power-Up

Power must be applied to the $\overline{RAS}$ and $\overline{DT/OE}$ input signals to pull them "high" before or at the same time as the V_{DD} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT/OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT/OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

Initial State After Power-Up

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$ and $\overline{WB/WE}$ held "high", the internal state of the V52C4256 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μs pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
WM1 Register	Write Enable
TAP pointer	Invalid

3

HIGH PERFORMANCE V52C4258	60	70	80	10
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	25 ns	25 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns	55 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	140 ns	150 ns	180 ns
Max. Serial Access Time, (t_{SCA})	25 ns	25 ns	25 ns	25 ns
Min. Serial Port Cycle Time, (t_{SCC})	30 ns	30 ns	30 ns	30 ns

Features

- Organization
  - RAM Port: 262,144 words x 4 bits
  - SAM Port: 512 words x 4 bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write, Write-Per-Bit
  - Block Write/Flash Write
  - Color Register Load/Read
  - 512 Refresh Cycles/8 ms
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
  - Fully Static Register
- RAM-SAM Bidirectional Transfer
  - Read/Write/Pseudo Write Transfer
  - Real Time Read Transfer
  - Split Read/Write Transfer
- Low Power Dissipation
  - RAM Port Operating Alone – 85 mA
  - SAM Port Operating Alone – 50 mA
- Low CMOS Standby Current – 7 mA
- Package
  - 28 pin 400 mil SOJ
  - 28 pin 400 mil ZIP

Description

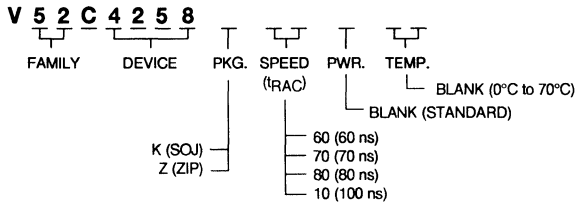
The V52C4258 VRAM is equipped with a 262,144-words by 4-bits dynamic random access memory (RAM) port and a 512-words by 4-bits static serial access memory (SAM) port. The V52C4258 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

In addition to the conventional multiport video RAM operating modes, the V52C4258 features the block write and flash write functions on the RAM port and a split register data transfer capability on the SAM port.

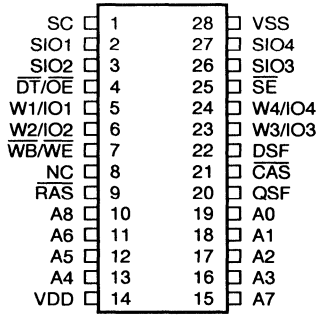
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power	Temperature Mark
	K	Z	60	70	80	100	Std	
0°C–70°C	•	•	•	•	•	•	•	Blank

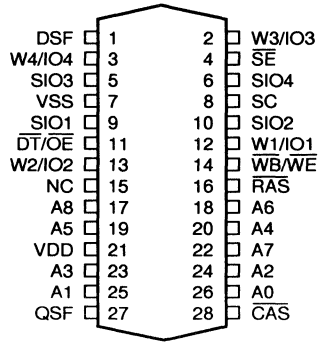
Description	Pkg.	Pin Count
SOJ	K	28
ZIP	Z	28



28 Lead Pin Configuration



K – SOJ



Z – ZIP

Pin Names

Name	Description
A0-A8	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
DT/OE	Data Transfer/Output Enable
WB/WE	Write per Bit/Write Enable
DSF	Special Function Control
W1/IO1-W4/IO4	Write Mask/Data In, Out
SC	Serial Clock
SE	Serial Enable
SIO1-SIO4	Serial Input/Output
QSF	Special Flag Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 to +7.0 V
Short Circuit Out Current ..... 50 mA
Power Dissipation ..... 1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

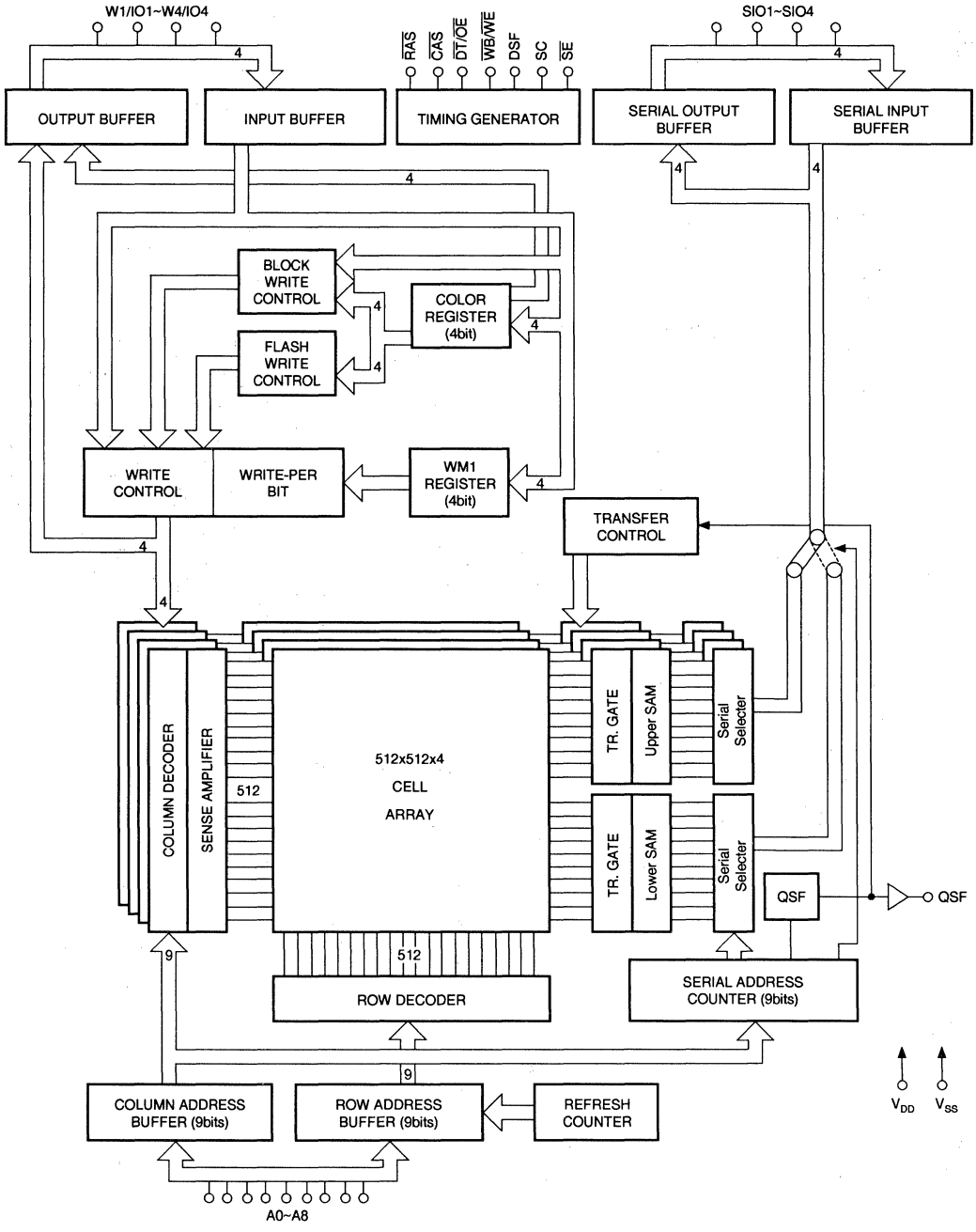
Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF
C_{OUT}	Output Capacitance (QSF)		9	pF

*Note: Capacitance is sampled and not 100% tested.

Functional Diagram



DC and Operating Characteristics

(V_{DD} = 5V ± 10%, T_A = 0–70°C)

Symbol	Parameter (RAM Port)	SAM Port	-60		-70		-80		-10		Unit	Note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
I_{DD1}	Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75		65	mA	1,2
I_{DD1A}		Active		130		120		110		100	mA	1,2
I_{DD2}	Standby Current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	Standby		7		7		7		7	mA	
I_{DD2A}		Active		55		50		45		40	mA	1,2
I_{DD3}	$\overline{RAS}$-Only Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH},	Standby		95		85		75		65	mA	1,2
I_{DD3A}	t_{RC} = t_{RC} Min.	Active		130		120		110		100	mA	1,2
I_{DD4}	Page Mode Current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling,	Standby		75		70		65		60	mA	1,2
I_{DD4A}	t_{PC} = t_{PC} Min.	Active		130		120		110		100	mA	1,2
I_{DD5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = t_{RC} Min.	Standby		95		85		75		65	mA	1,2
I_{DD5A}		Active		130		120		110		100	mA	1,2
I_{DD6}	Data Transfer Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75		65	mA	1,2
I_{DD6A}		Active		130		120		110		100	mA	1,2
I_{DD7}	Flash Write Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75		65	mA	1,2
I_{DD7A}		Active		130		120		110		100	mA	1,2
I_{DD8}	Block Write Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		95		85		75		65	mA	1,2
I_{DD8A}		Active		130		120		110		100	mA	1,2
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V		-10	10	-10	10	-10	10	-10	10	µA	
$I_{O(L)}$	Output Leakage Current 0V ≤ V_{OUT} ≤ 5.5V, Output Disable		-10	10	-10	10	-10	10	-10	10	µA	
V_{OH}	Output "H" Level Voltage I_{OUT} = -2 mA		2.4		2.4		2.4		2.4		V	
V_{OL}	Output "L" Level Voltage I_{OUT} = 2 mA			0.4		0.4		0.4		0.4	V	
V_{IH}	Input High Voltage		2.4	V_{DD}+1	2.4	V_{DD}+1	2.4	V_{DD}+1	2.4	V_{DD}+1	V	
V_{IL}	Input Low Voltage		-1.0	0.8	-1.0	0.8	-1.0	0.8	-1.0	0.8	V	

3

AC Electrical Characteristics *Notes: 3, 4, 5*

Symbol	Parameter	-60		-70		-80		-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	120		140		150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	175		195		195		235		ns	
t_{PC}	Fast Page Mode Cycle Time	40		45		50		55		ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	85		90		90		100		ns	
t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	6,12
t_{AA}	Access Time from Column Address		30		35		40		50	ns	6,12
t_{CAC}	Access Time from $\overline{CAS}$		15		20		25		25	ns	6,13
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		35		40		45		50	ns	6,13
t_{OFF}	Output Buffer Turn-Off Delay	0	15	0	20	0	20	0	20	ns	8
t_T	Transition Time (Rise and Fall)	3	35	3	35	3	35	3	35	ns	5
t_{RP}	$\overline{RAS}$ Precharge Time	50		60		60		70		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	70	10K	80	10K	100	10K	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode only)	60	100K	70	100K	80	100K	100	100K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	15		20		25		25		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	20	10K	25	10K	25	10K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	50	20	55	20	75	ns	12
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30		35		40		55		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		10		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10		10		10		ns	
t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		10		10		ns	
t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
t_{CAH}	Column Address Hold Time	10		15		15		15		ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	50		55		55		70		ns	
t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		0		ns	9
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		0		0		ns	9
t_{WCH}	Write Command Hold Time	10		15		15		15		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	50		55		55		70		ns	

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	-60		-70		-80		-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{WP}	Write Command Pulse Width	10		15		15		15		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		25		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		25		ns	
t_{DS}	Data Setup Time	0		0		0		0		ns	10
t_{DH}	Data Hold Time	15		15		15		15		ns	10
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	50		55		55		70		ns	
t_{WCS}	Write Command Setup Time	0		0		0		0		ns	11
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	90		100		100		130		ns	11
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	60		65		65		80		ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	40		45		45		55		ns	11
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0		0		0		ns	
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0		0		0		ns	
t_{OEA}	Access Time from $\overline{OE}$		15		20		20		25	ns	6
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	0	10	0	10	0	10	0	20	ns	8
t_{OED}	$\overline{OE}$ to Data Delay Time	10		10		10		20		ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	10		10		10		20		ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	10		15		15		15		ns	
t_{CSR}	$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		10		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0		0		0		ns	
t_{REF}	Refresh Period		8		8		8		8	ms	
t_{WSR}	$\overline{WB}$ Setup Time	0		0		0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	15		15		15		15		ns	
t_{FSR}	DSF Setup Time referenced to $\overline{RAS}$	0		0		0		0		ns	
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$ (1)	15		15		15		15		ns	
t_{FHR}	DSF Hold Time referenced to $\overline{RAS}$ (2)	50		55		55		70		ns	
t_{FSC}	DSF Setup Time referenced to $\overline{CAS}$	0		0		0		0		ns	
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	15		15		15		15		ns	
t_{MS}	Write-Per-Bit Mask Data Setup Time	0		0		0		0		ns	
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15		15		15		ns	
t_{THS}	$\overline{DT}$ High Setup Time	0		0		0		0		ns	
t_{THH}	$\overline{DT}$ High Hold Time	15		15		15		15		ns	
t_{TLS}	$\overline{DT}$ Low Setup Time	0		0		0		0		ns	

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	-60		-70		-80		-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10K	15	10K	15	10K	15	10K	ns	
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	55	10K	60	10K	65	10K	80	10K	ns	
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	20		25		30		30		ns	
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	15		20		25		25		ns	
t_{ESR}	$\overline{SE}$ Setup Time referenced to $\overline{RAS}$	0		0		0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15		15		15		ns	
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	50		60		60		70		ns	
t_{TP}	$\overline{DT}$ Precharge Time	20		20		20		30		ns	
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	65		70		80		100		ns	
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	40		45		45		50		ns	
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	20		20		25		25		ns	
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5		5		5		ns	
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15		15		15		ns	
t_{SRS}	Last SC to $\overline{RAS}$ Setup Time (Serial Input)	20		25		25		30		ns	
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	20		20		20		25		ns	
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	40		40		40		50		ns	
t_{SDZ}	Serial Output Buffer Turn-Off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	40	10	40	10	40	10	50	ns	8
t_{SCC}	SC Cycle Time	30		30		30		30		ns	
t_{SC}	SC Pulse Width (SC High Time)	10		10		10		10		ns	
t_{SCP}	SC Precharge Time (SC Low Time)	10		10		10		10		ns	
t_{SCA}	Access Time from SC		25		25		25		25	ns	7
t_{SOH}	Serial Output Hold Time from SC	5		5		5		5		ns	
t_{SDS}	Serial Input Setup Time	0		0		0		0		ns	
t_{SDH}	Serial Input Hold Time	15		15		15		15		ns	
t_{SEA}	Access Time from $\overline{SE}$		25		25		25		25	ns	7
t_{SE}	$\overline{SE}$ Pulse Width	25		25		25		25		ns	
t_{SEP}	$\overline{SE}$ Precharge Time	25		25		25		25		ns	
t_{SEZ}	Serial Output Buffer Turn-Off Delay from $\overline{SE}$	0	20	0	20	0	20	0	20	ns	8
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0		0		0		ns	

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	-60		-70		-80		-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{SZS}	Serial Input to First SC Delay Time	0		0		0		0		ns	
t_{SWS}	Serial Write Enable Setup Time	5		5		5		5		ns	
t_{SWH}	Serial Write Enable Hold Time	15		15		15		15		ns	
t_{SWIS}	Serial Write Disable Setup Time	5		5		5		5		ns	
t_{SWIH}	Serial Write Disable Hold Time	15		15		15		15		ns	
t_{STS}	Split Transfer Setup Time	25		25		30		30		ns	
t_{STH}	Split Transfer Hold Time	25		25		30		30		ns	
t_{SQD}	SC–QSF Delay Time		25		25		25		25	ns	
t_{TQD}	$\overline{DT}$–QSF Delay Time		25		25		25		25	ns	
t_{CQD}	$\overline{CAS}$–QSF Delay Time		35		35		35		35	ns	
t_{RQD}	$\overline{RAS}$–QSF Delay Time		75		75		75		85	ns	

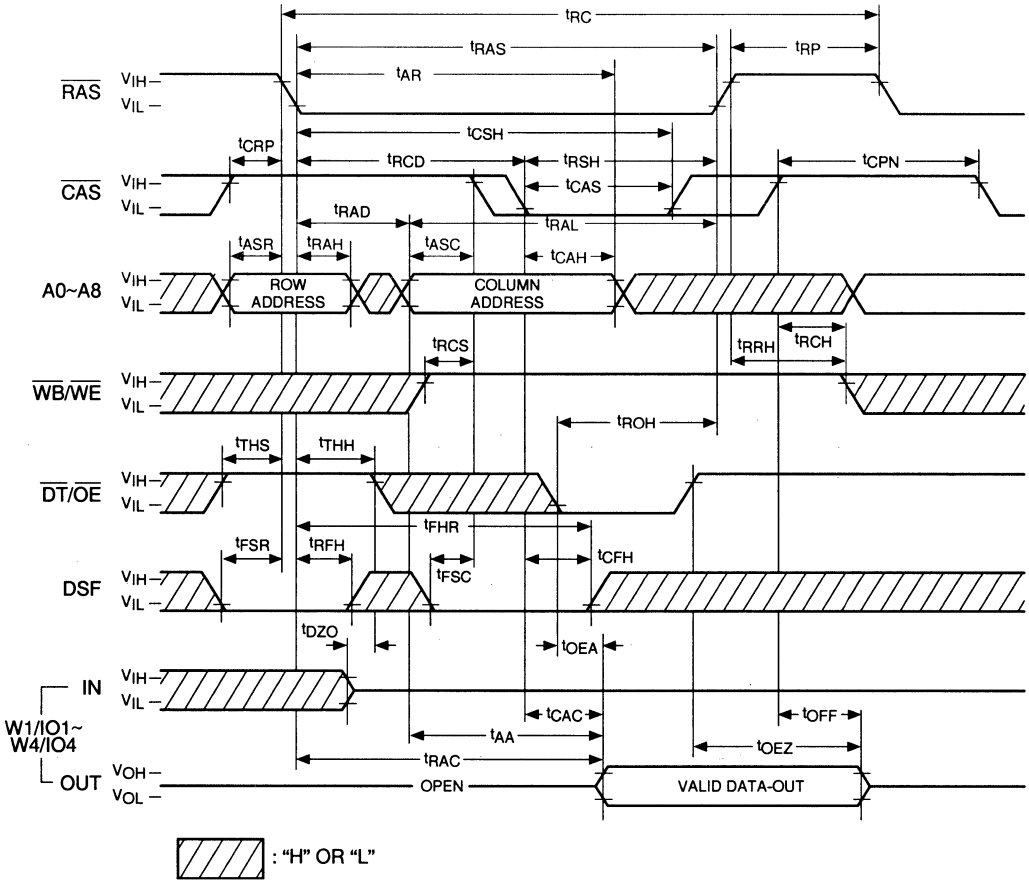
3

Notes

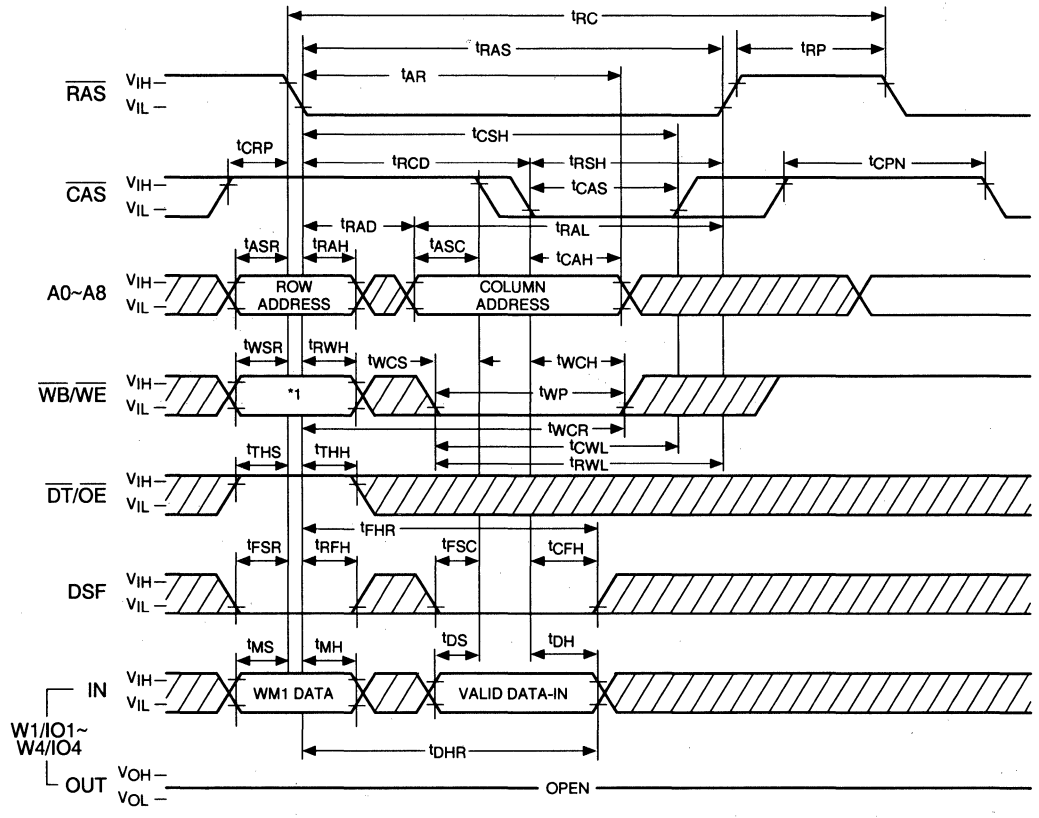
1. These parameters depend on cycle rate.
2. These parameters depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC measurements assume t_T = 5 ns.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. RAM port outputs are measured with a load equivalent to 1 TTL load and 100 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
7. SAM port outputs are measured with a load equivalent to 1 TTL load and 30 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
8. t_{OFF} (max.), t_{OEZ} (max.), t_{SDZ} (max.) and t_{SEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
12. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

Read Cycle



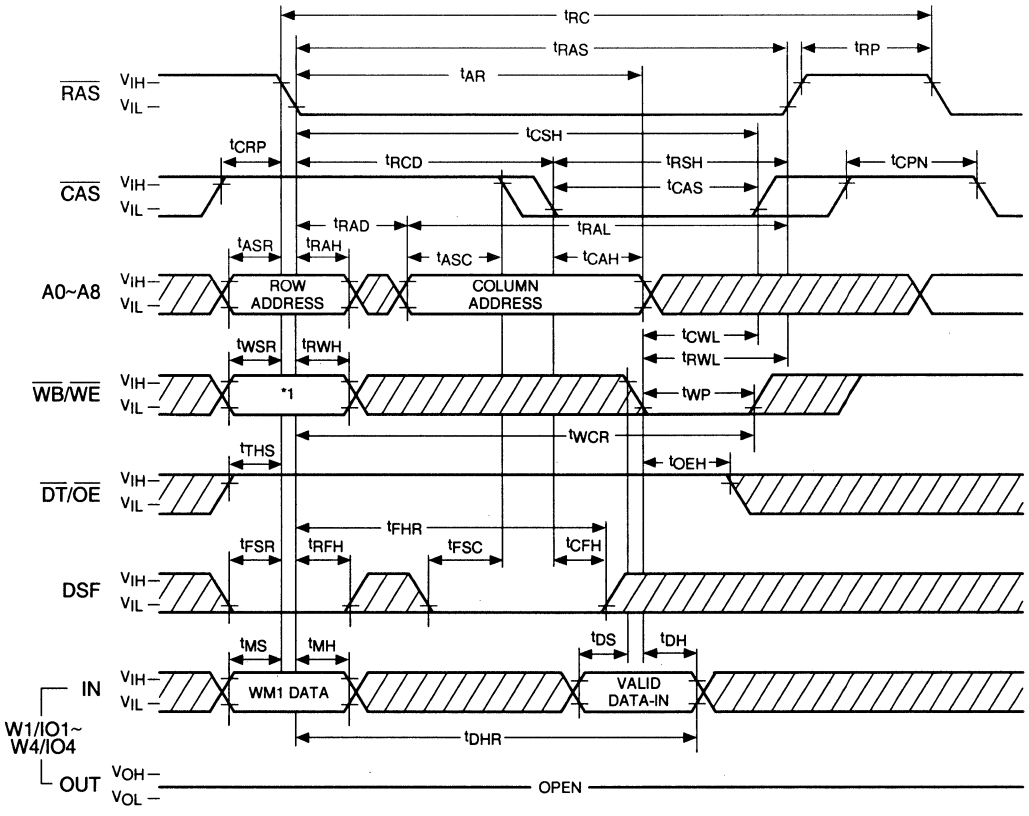
Write Cycle (Early Write)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

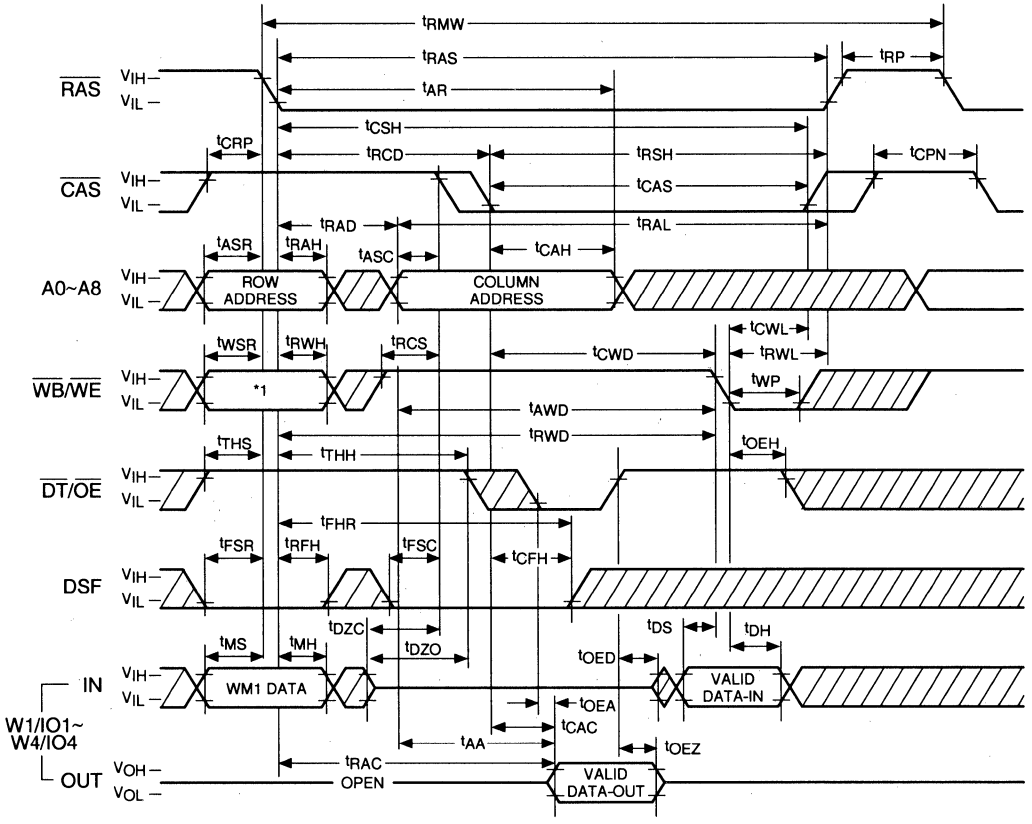
Write Cycle ($\overline{OE}$ Controlled Write)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

Read-Modify-Write Cycle

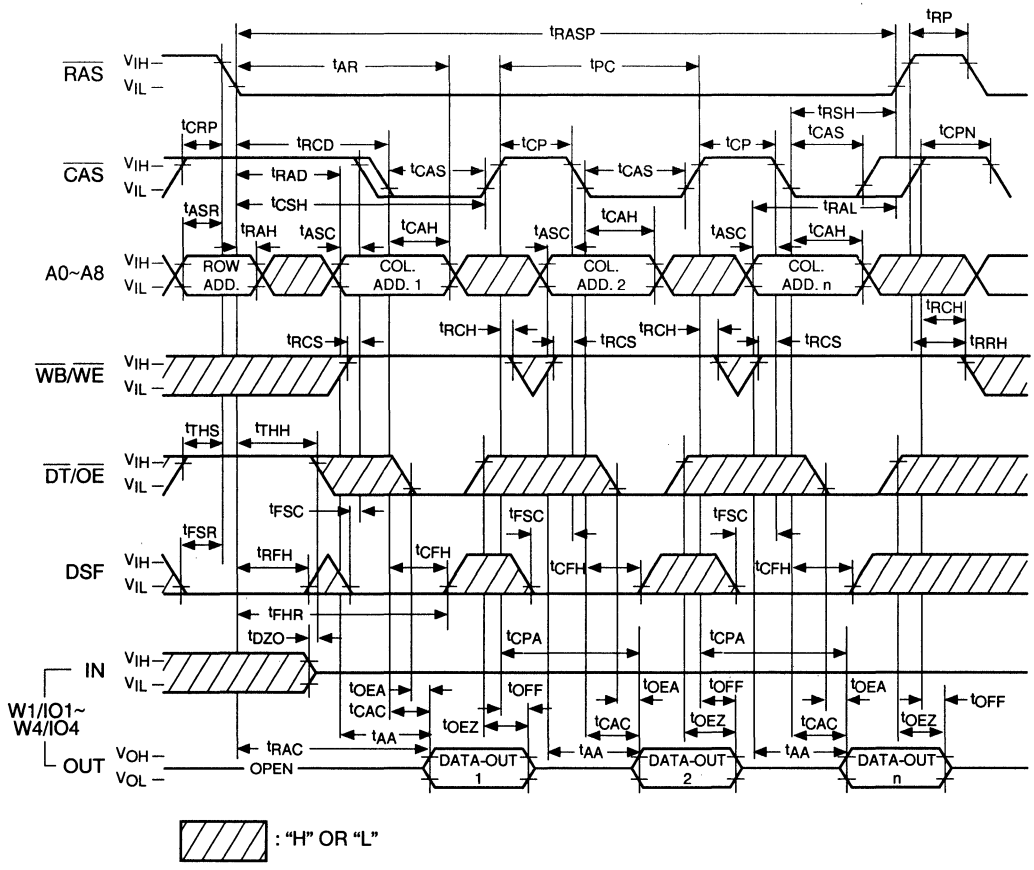


*1 WB/WE	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

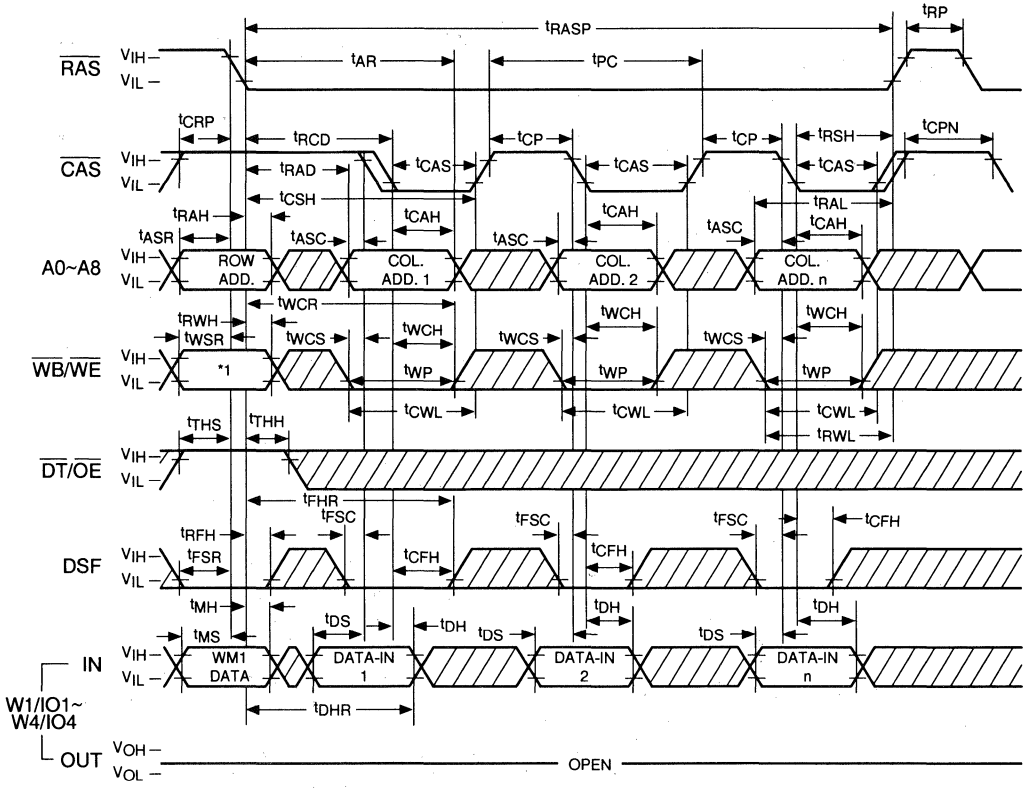
WM1 data: 0: Write Disable
1: Write Enable

: "H" OR "L"

Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)

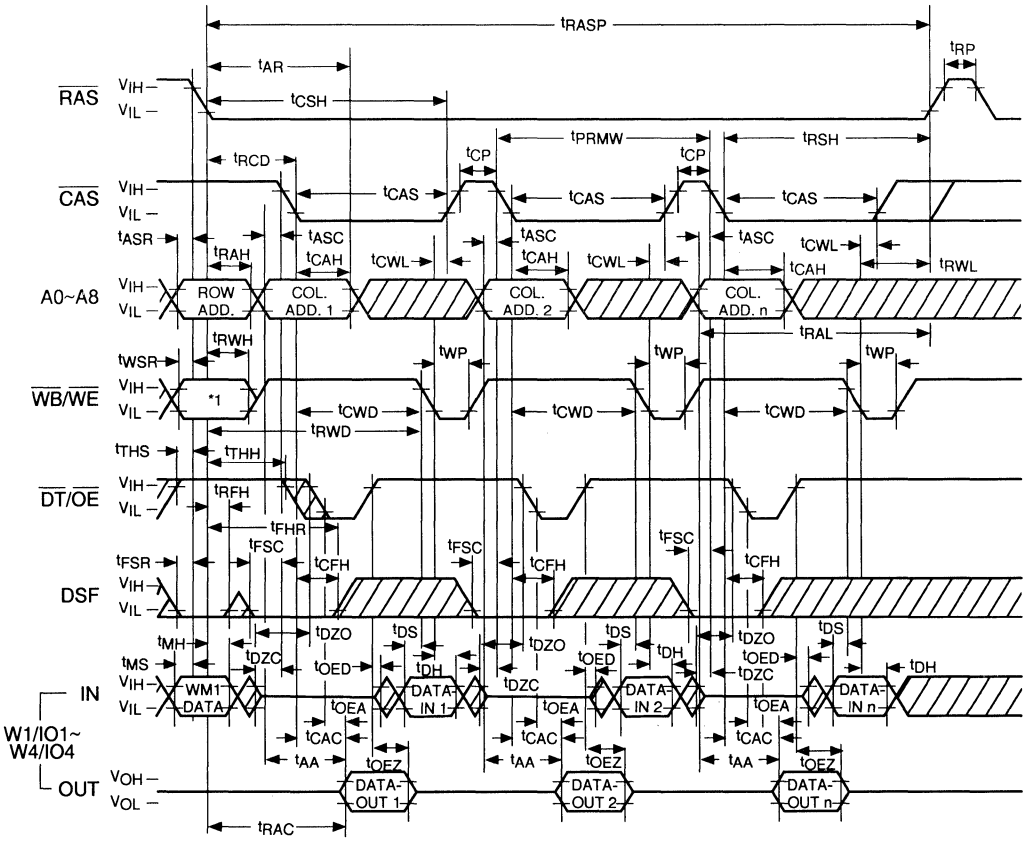


*1 $\overline{WB}/\overline{WE}$	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

: "H" OR "L"

Fast Page Mode Read-Modify-Write Cycle

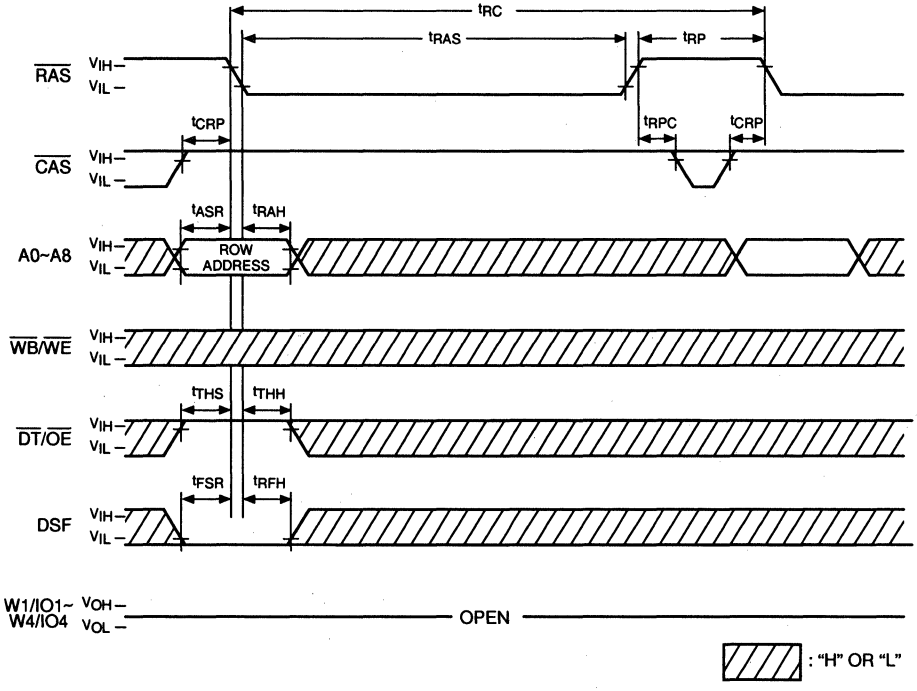


: "H" OR "L"

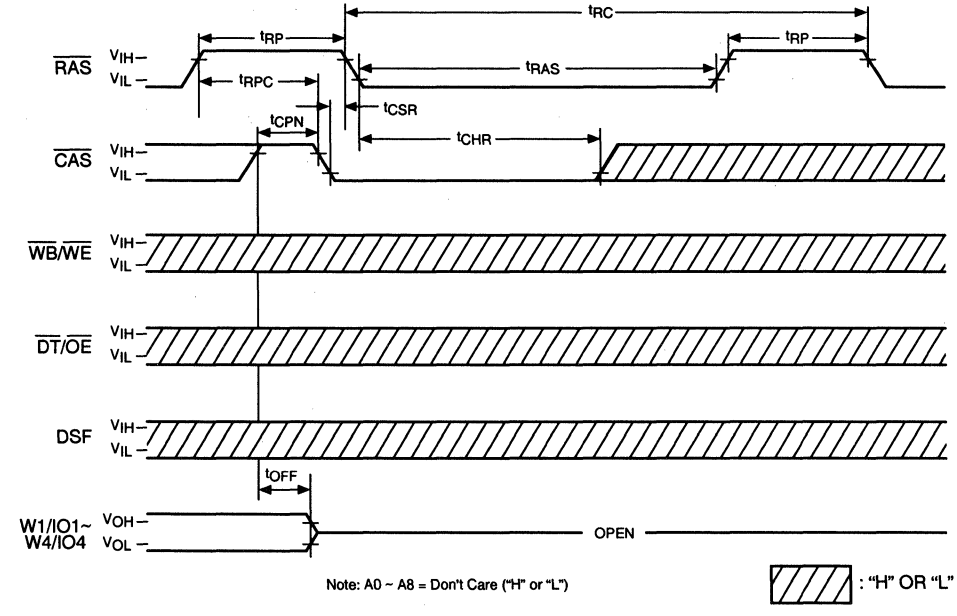
*1 WB/WE	W1/IO1~W4/IO4	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

$\overline{RAS}$ Only Refresh Cycle

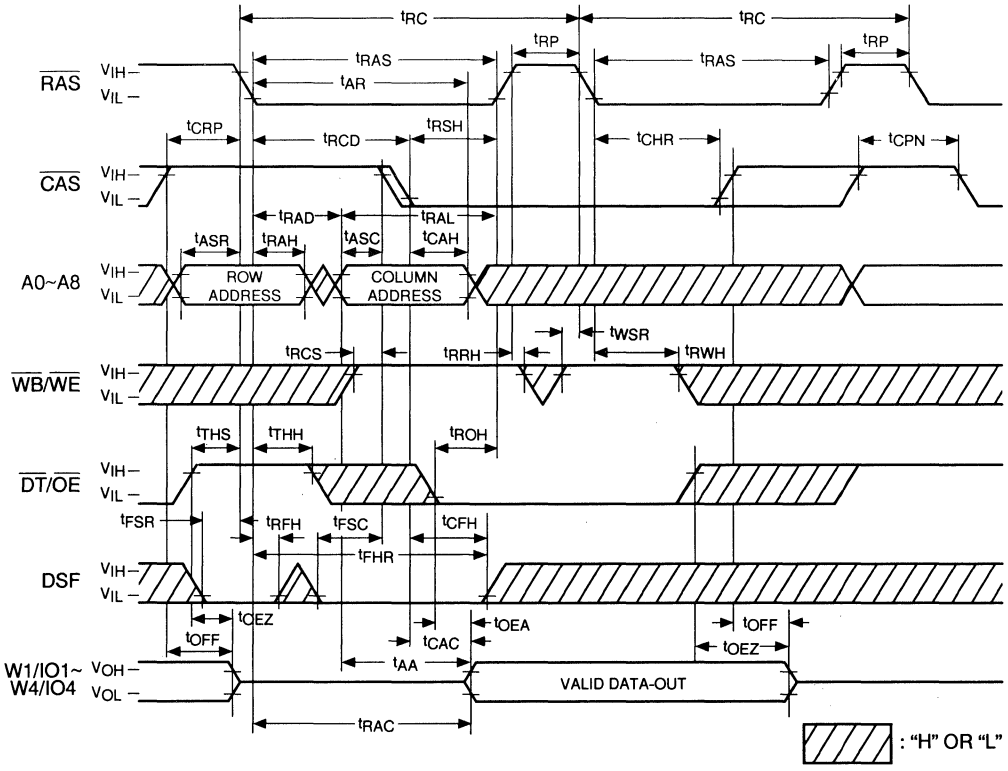


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

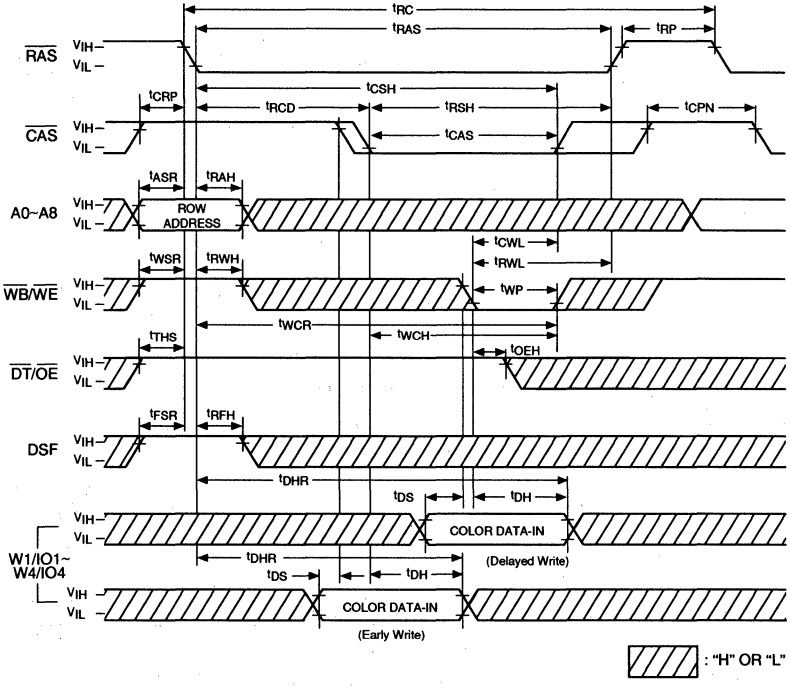


Note: A0 ~ A8 = Don't Care ("H" or "L")

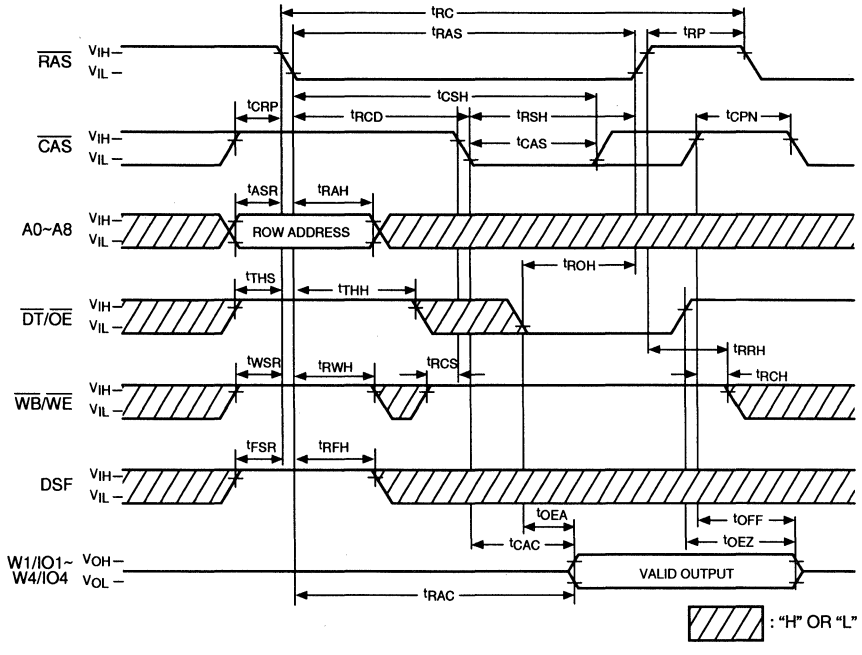
Hidden Refresh Cycle



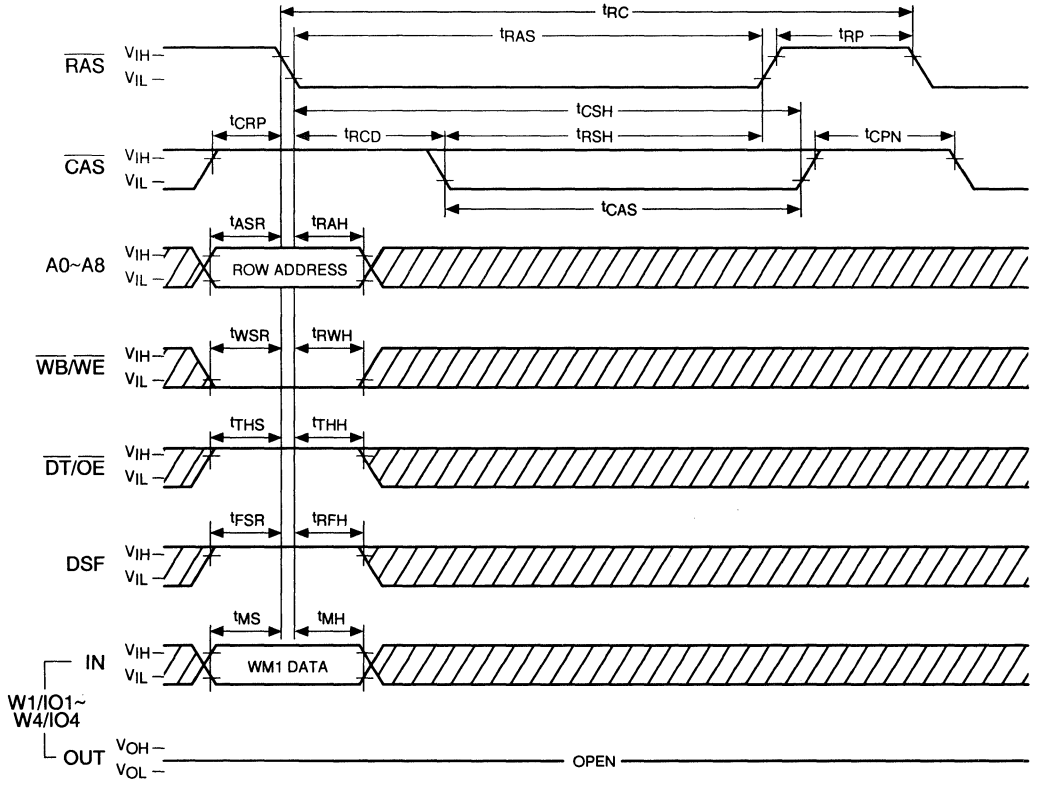
Load Color Register Cycle



Read Color Register Cycle

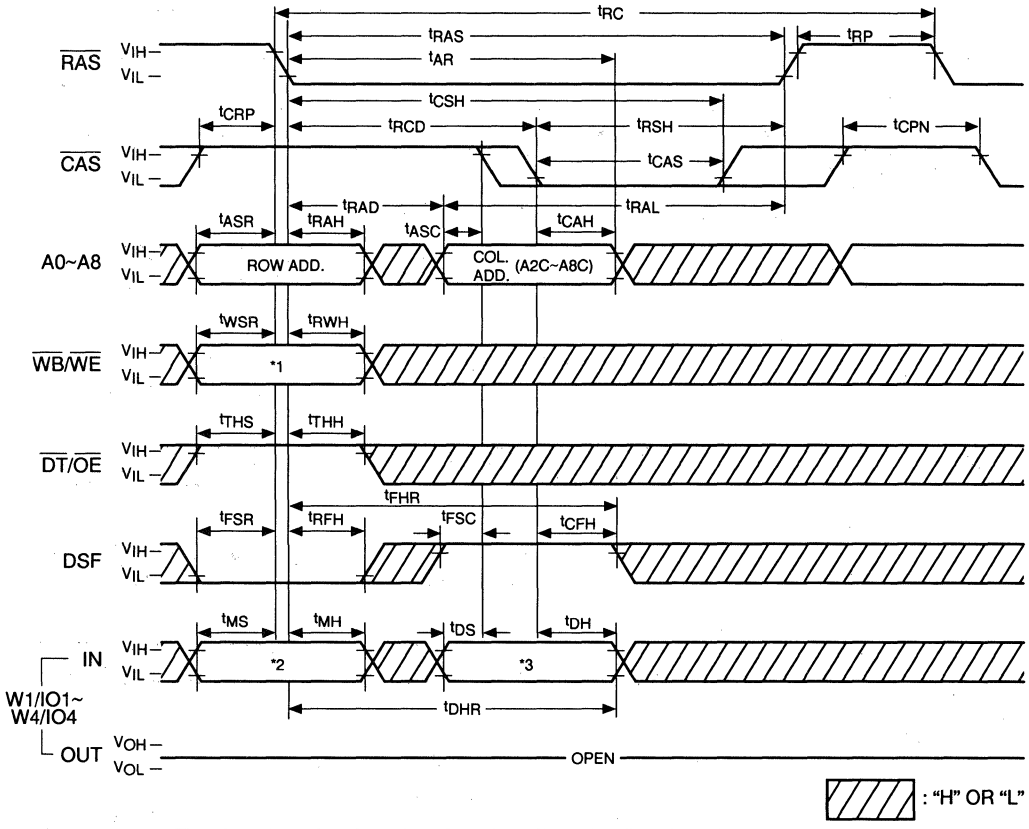


Flash Write Cycle



WM1 DATA	Cycle
0	Flash Write Disable
1	Flash Write Enable

Block Write Cycle



*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W4/IO4	Cycle
0	WM1 data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

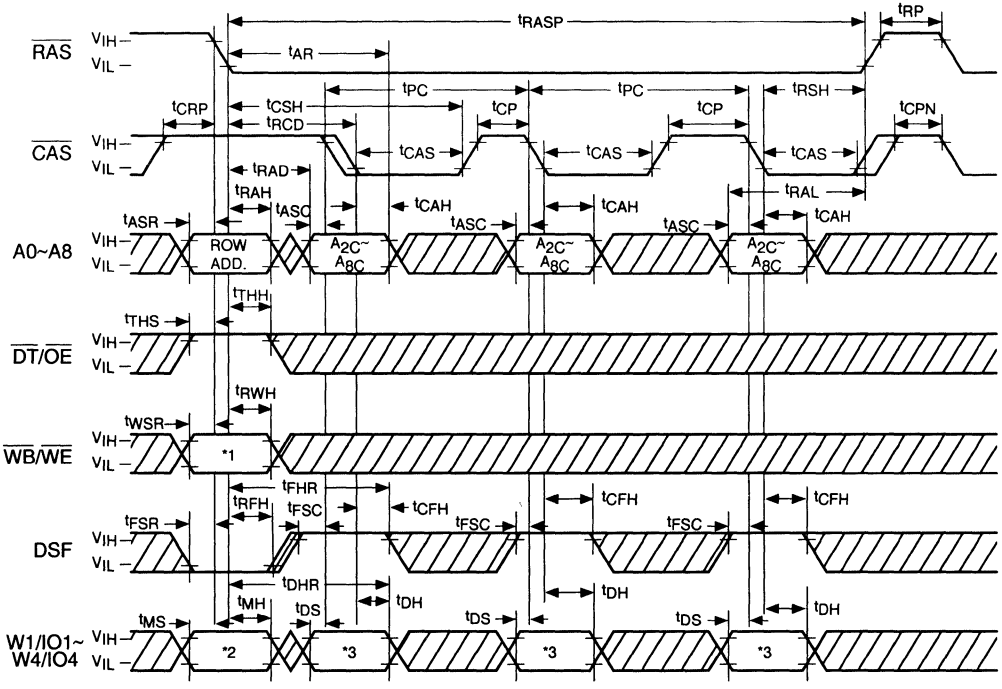
WM1 data: 0: Write Disable
1: Write Enable

*3) Column Select

W1/IO1 — Column 0 (A_{1C} = 0, A_{0C} = 0)
W2/IO2 — Column 1 (A_{1C} = 0, A_{0C} = 1)
W3/IO3 — Column 2 (A_{1C} = 1, A_{0C} = 0)
W4/IO4 — Column 3 (A_{1C} = 1, A_{0C} = 1)

Wn/IOn
= 0 : Disable
= 1 : Enable

Page Mode Block Write Cycle



*1 WB/WE	*2 W1/IO1~W4/IO4	Cycle
0	WM1 data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

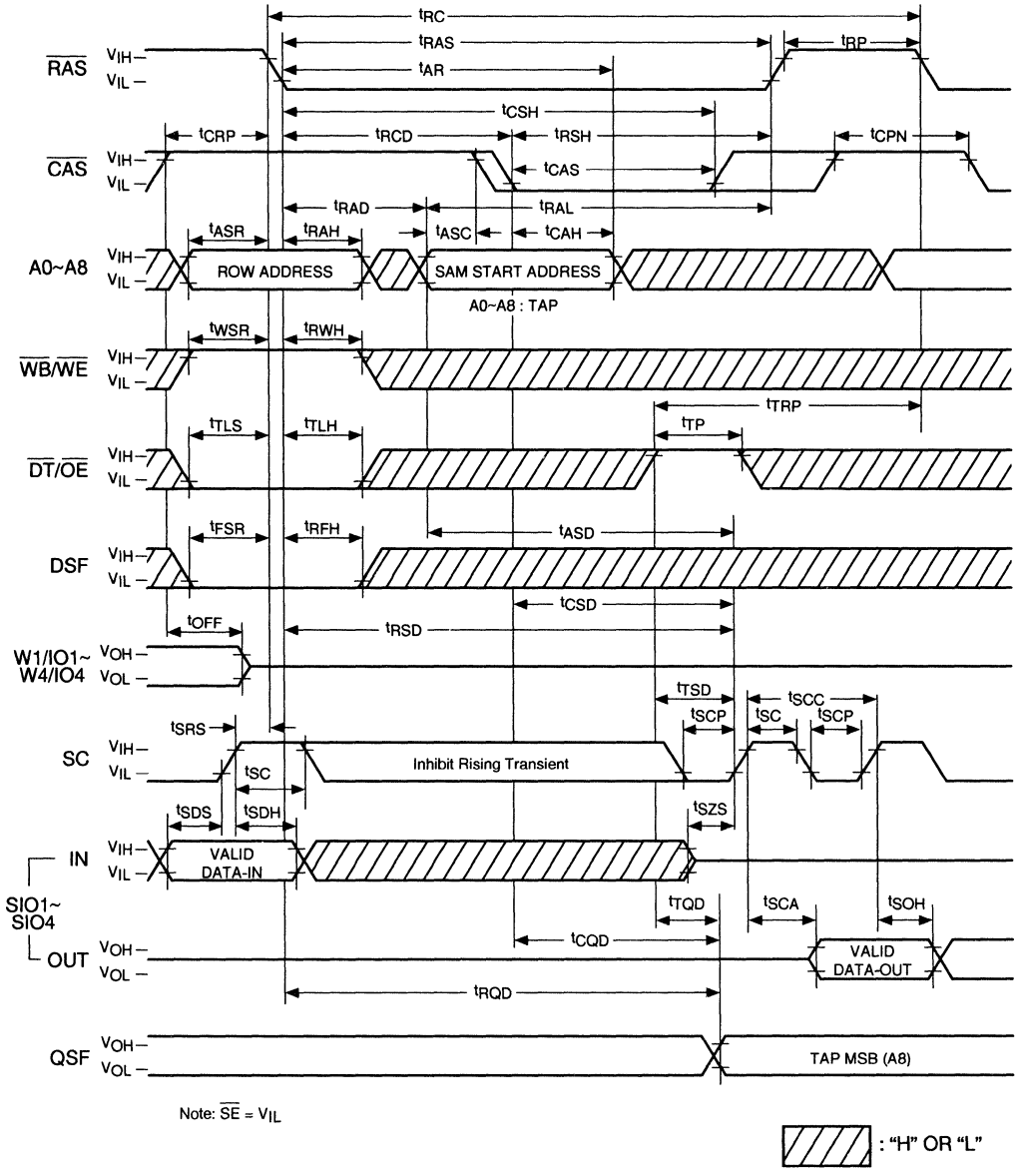
WM1 data: 0: Write Disable
1: Write Enable

*3) Column Select

W1/IO1 — Column 0 (A_{1C} = 0, A_{0C} = 0)
W2/IO2 — Column 1 (A_{1C} = 0, A_{0C} = 1)
W3/IO3 — Column 2 (A_{1C} = 1, A_{0C} = 0)
W4/IO4 — Column 3 (A_{1C} = 1, A_{0C} = 1)

Wn/IOn
= 0 : Disable
= 1 : Enable

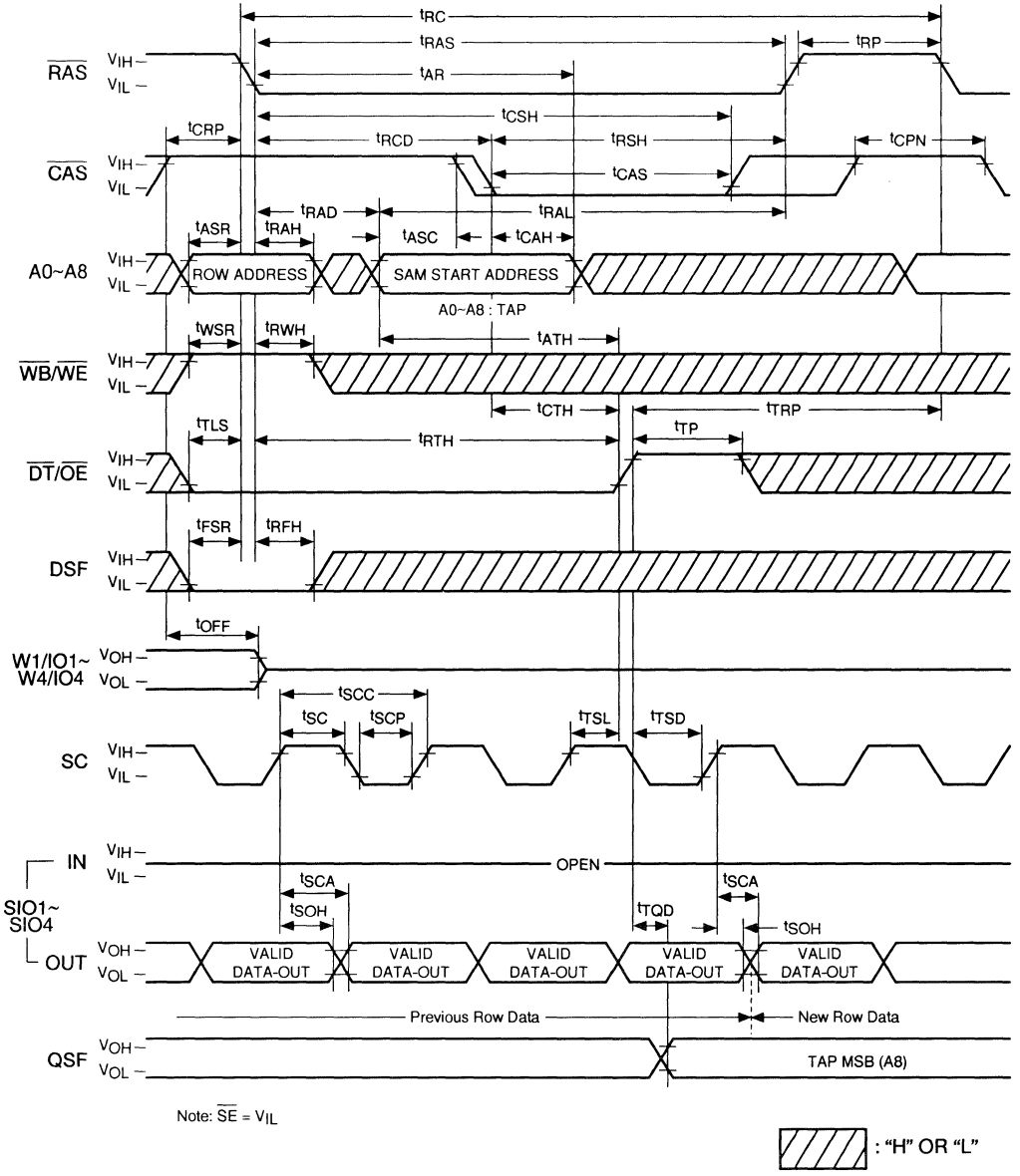
Read Transfer Cycle (Previous Transfer is Write Transfer Cycle)



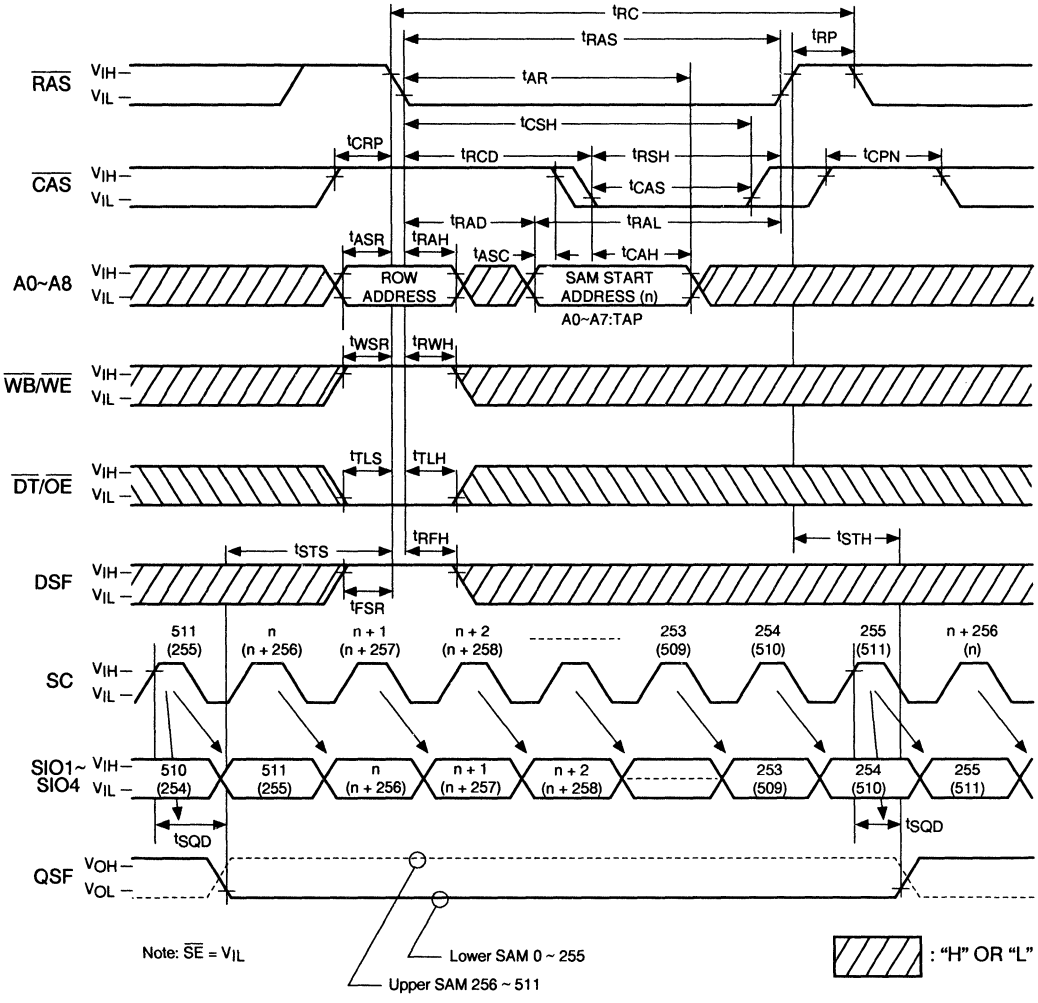
Note: $\overline{SE}$ = V_{IL}

: "H" OR "L"

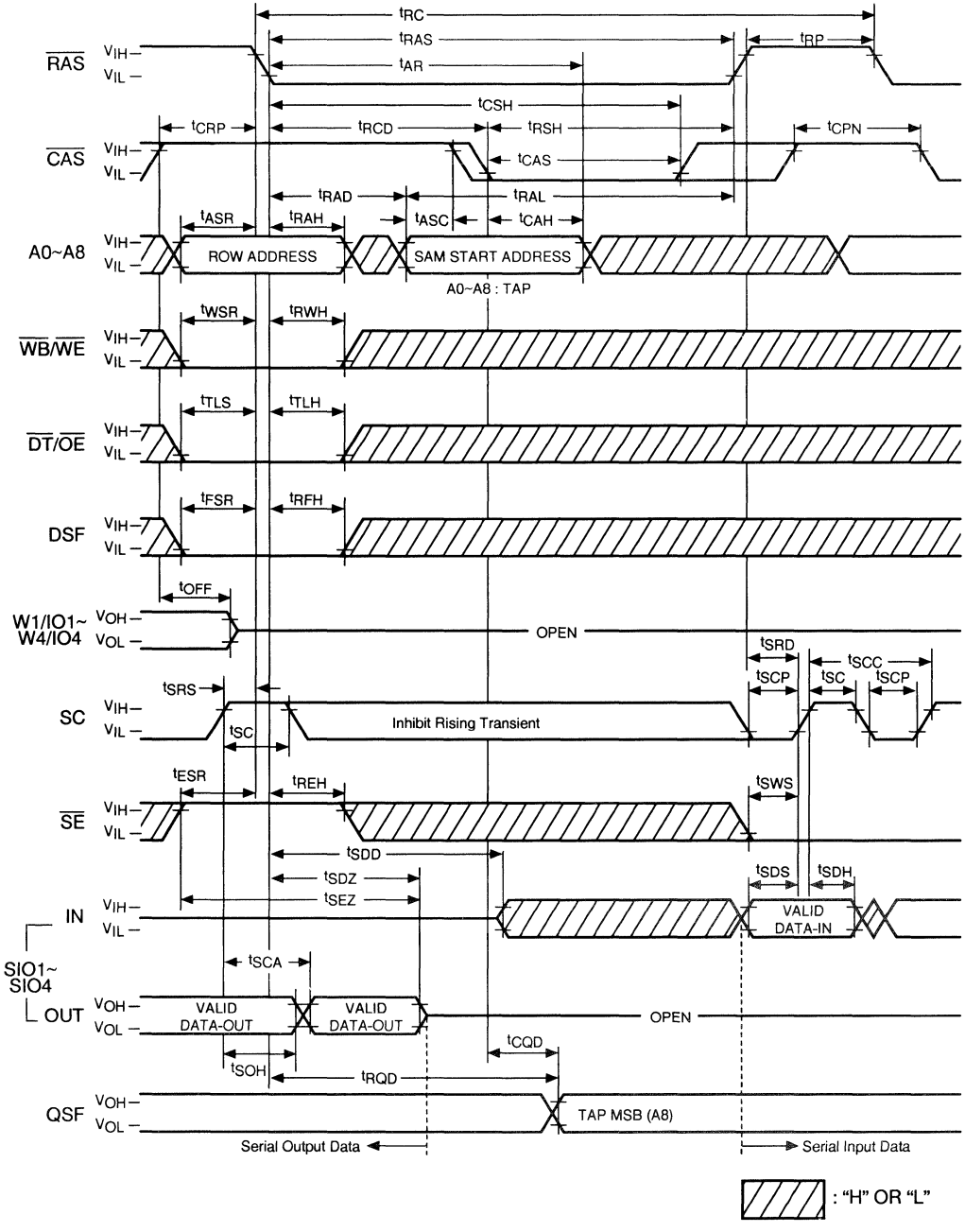
Real Time Read Transfer Cycle



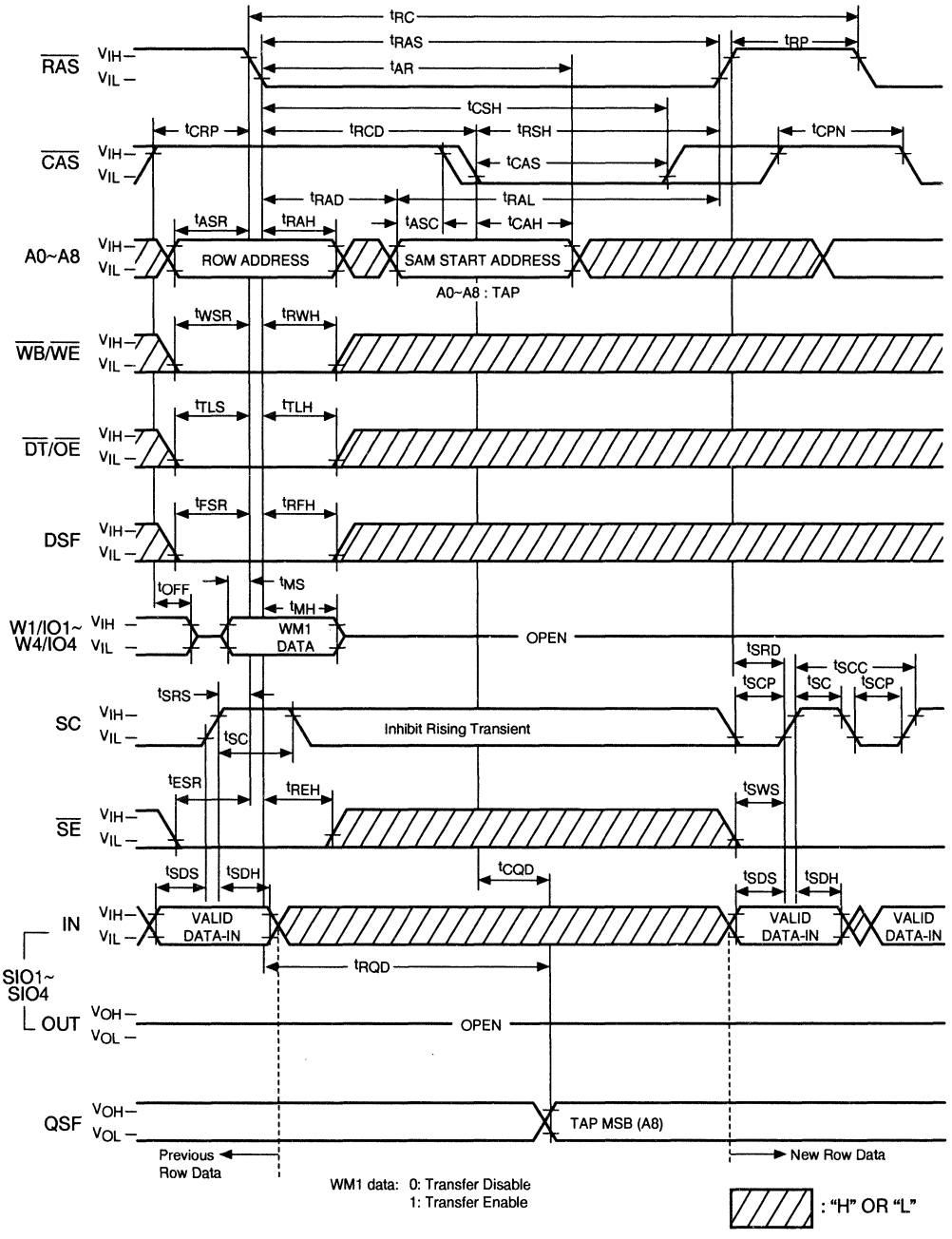
Split Read Transfer Cycle



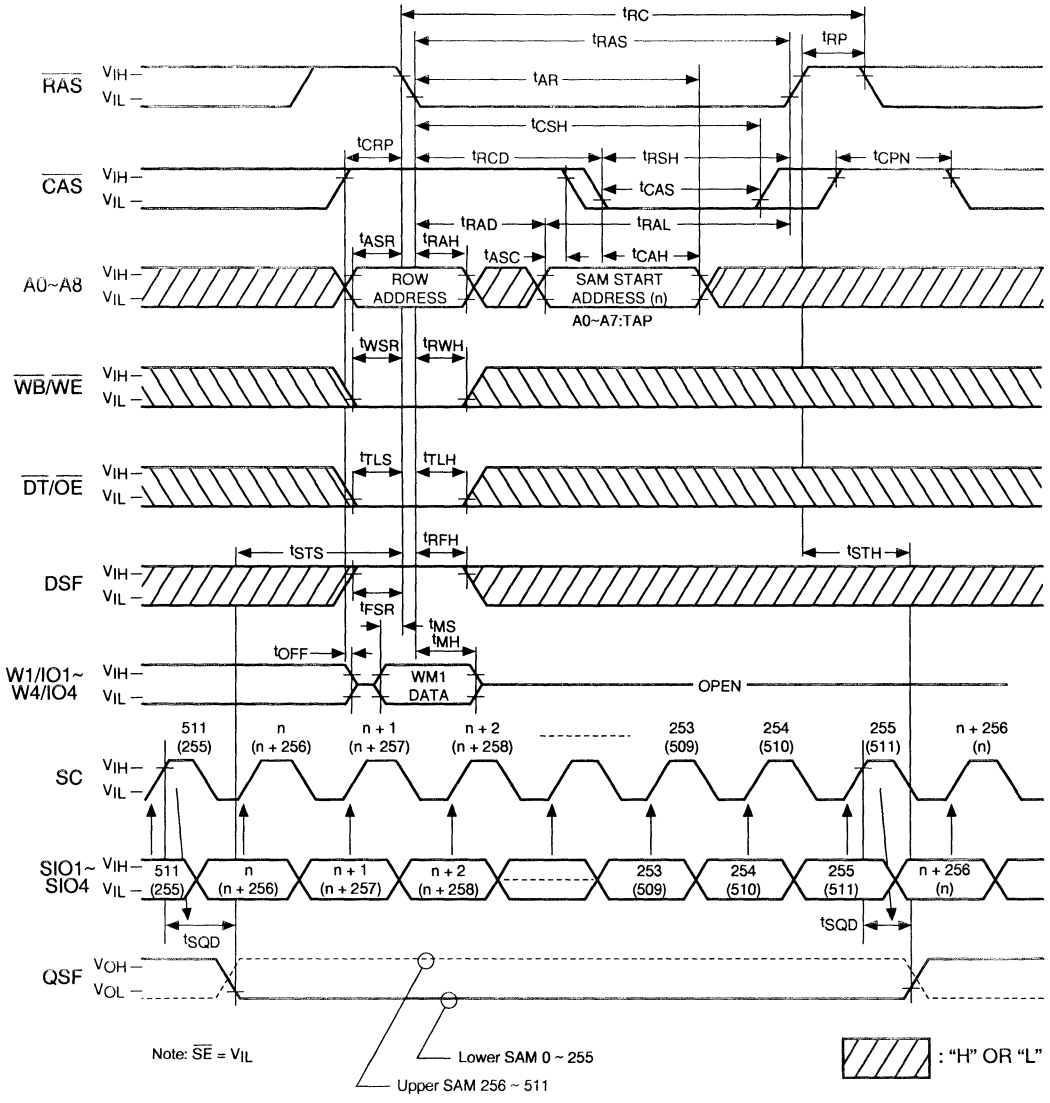
Pseudo Write Transfer Cycle



Write Transfer Cycle

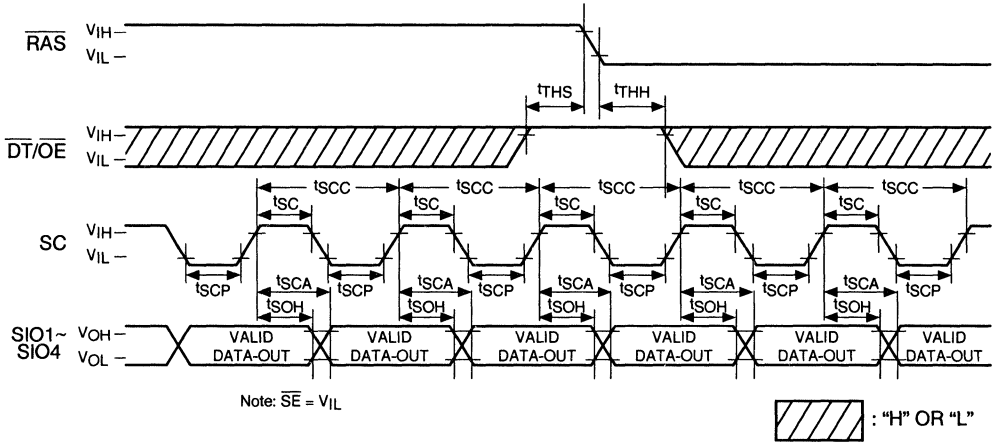


Split Write Transfer Cycle

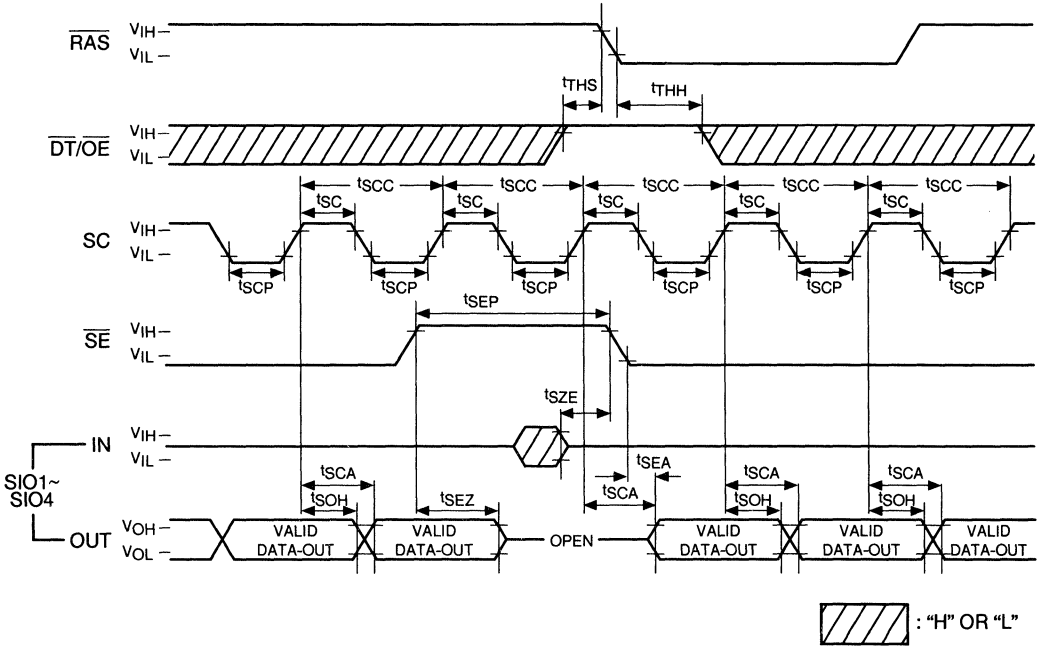


WM1 DATA: 0: Transfer Disable
1: Transfer Enable

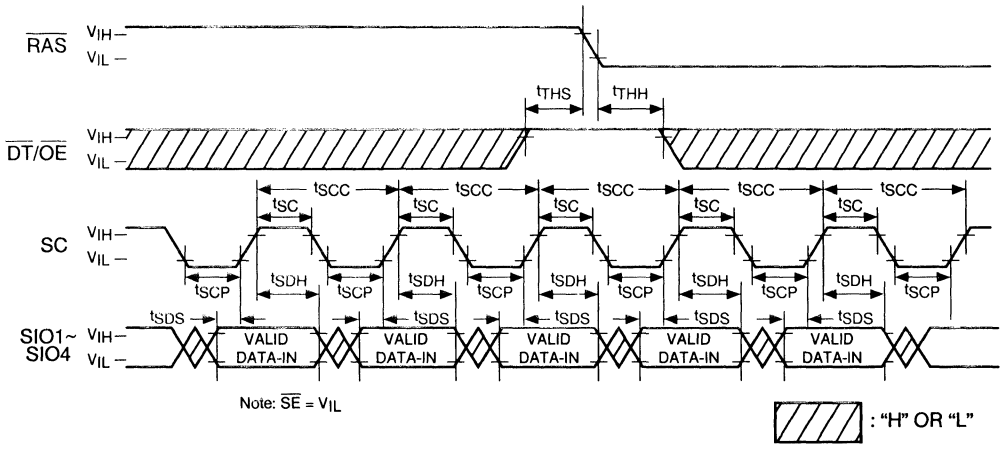
Serial Read Cycle ($\overline{SE}$ = V_{IL})



Serial Read Cycle ($\overline{SE}$ Controlled Outputs)



Serial Write Cycle ($\overline{SE}$ = V_{IL})



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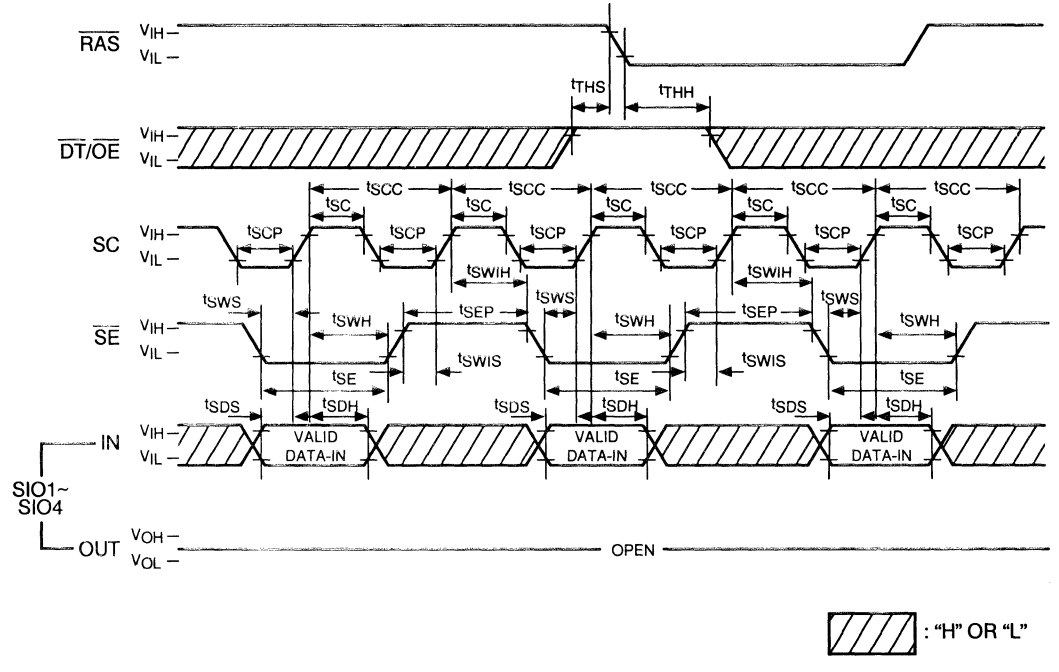
Serial Write Cycle ($\overline{SE}$ Controlled Inputs)



Pin Functions

Address Inputs: A0–A8

The 18 address bits required to decode 4 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the V52C4258 are multiplexed onto 9 address input pins (A_0–A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following nine column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

Row Address Strobe: $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, $\overline{SE}$ and DSF to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

Column Address Strobe: $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits and the state of the special function input DSF. DSF is used in conjunction with the $\overline{RAS}$ control to select either read/write operations or the special block write feature on the RAM port when the DSF input is held "low" at the falling edge of $\overline{RAS}$. Refer to the operation truth table shown in Table 1. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

Data Transfer/Output Enable: $\overline{DT/OE}$

The $\overline{DT/OE}$ input is a multifunction pin. When $\overline{DT/OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT/OE}$ is used as an output enable control. When the $\overline{DT/OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

Write Per Bit/Write Enable: $\overline{WB/WE}$

The $\overline{WB/WE}$ input is also a multifunction pin. When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB/WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).

When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (masked write transfer).

Write Mask Data/Data Input and Output: W_1/IO_1–W_4/IO_4

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB/WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT/OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT/OE}$, whichever occurs first.

Serial Clock: SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 9-bits serial pointer (8-bits in split register mode) which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the normal transfer cycle. When the pointer reaches the most significant address location (decimal 511), the next SC clock will place it at the least significant address location (decimal 0). The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read/pseudo write/write transfer operations and should not be clocked while the SAM port is in the standby mode, to prevent the SAM pointer from being incremented.

Serial Enable: $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

Special Function Control: DSF

The DSF input is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and allows for the selection of various random port and data transfer operating modes. In addition to the conventional multiport DRAM, the special features, consisting of flash write, block write, load/read color register and split read/write transfer can be invoked.

Special Function Output: QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0–255) is being accessed, and QSF "high" indicates that the upper split SAM (Bit 256–511) is being accessed. QSF is monitored so that after it toggles and after allowing for a delay of t_{STS}, split read/write transfer operation can be performed on the non-active split SAM.

Serial Input/Output: SIO1–SIO4

Serial input and output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During the subsequent write transfer cycle, the SAM remains in the input mode.

3

Operation Mode

The RAM port and data transfer operating of the V52C4258 are determined by the state of $\overline{CAS}$, $\overline{DT}$/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$, $\overline{SE}$ and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$.

Table 1 and Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operations, respectively.

Table 1. Operation Truth Table

$\overline{CAS}$ Falling Edge ↓			DSF	0	0	1	1
$\overline{RAS}$ Falling Edge ↓			DSF	0	1	0	1
$\overline{CAS}$	$\overline{DT}$/$\overline{OE}$	$\overline{WB}$/$\overline{WE}$	$\overline{SE}$				
0	•	•	•	$\overline{CAS}$-before-$\overline{RAS}$ Refresh			
1	0	0	0	Masked Write Transfer	Split Write Transfer	Masked Write Transfer	Split Write Transfer with
1	0	0	1	Pseudo Write Transfer	With Mask	Pseudo Write Transfer	Mask
1	0	1	•	Read Transfer	Split Read Transfer	Read Transfer	Split Read Transfer
1	1	0	•	Read/Write per Bit	Masked Flash Write	Masked Block Write	Masked Flash Write
1	1	1	•	Read/Write	Load/Read Color	Block Write	Load/Read Color

Table 2. Functional Truth Table

Function	RAS↓					CAS↓	Address		W/IO			Write Mask	Register	
	CAS	DT/OE	WB/WE	DSF	SE	DSF	RAS↓	CAS↓	RAS↓	CAS↓	CAS↓ WE↓		WM1	Color
CAS-before-RAS Refresh	0	•	•	•	•	–	•	–	•	–	–	–	–	–
Masked Write Transfer	1	0	0	0	0	•	Row	TAP	WM1	•	•	WM1	Load use	–
Pseudo Write Transfer	1	0	0	0	1	•	Row	TAP	•	•	•	–	–	–
Split Write Transfer	1	0	0	1	•	•	Row	TAP	WM1	–	•	WM1	Load use	–
Read Transfer	1	0	1	0	•	•	Row	TAP	•	•	•	–	–	–
Split Read Transfer	1	0	1	1	•	•	Row	TAP	•	•	•	–	–	–
Write per Bit	1	1	0	0	•	0	Row	Column	WM1	–	DIN	WM1	Load use	–
Masked Block Write	1	1	0	0	•	1	Row	Column A2C-8C	WM1	Column Select	–	WM1	Load use	use
Masked Flash Write	1	1	0	1	•	•	Row	•	WM1	–	•	WM1	Load use	use
Read/Write	1	1	1	0	•	0	Row	Column	•	–	DIN	–	–	–
Block Write	1	1	1	0	•	1	Row	Column A2C-8C	•	Column Select	–	–	–	use
Load/Read Color	1	1	1	1	•	•	Row	•	•	–	Color	–	–	Load/Read

Note: • = "0" or "1", TAP = SAM Start Address, – = not used.

If the special function control input (DSF) is in the "low" state at the falling edges of RAS and CAS, only the conventional multiport DRAM operating features can be invoked: CAS-before-RAS refresh, write transfer, pseudo-write transfer, read transfer, write-per-bit and read/write modes. If the DSF input is "high" at the falling edge of RAS, special features such as split write transfer, split read transfer, flash write and load/read color register can be invoked. If the DSF input is "low" at the falling edge of RAS and "high" at the falling edge of CAS, the block write special feature can be invoked.

RAM Port Operation

Fast Page Mode Cycle

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycles during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 µs. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT/OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT/OE}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-Only Refresh

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with the "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

The V52C4258 also offer an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

Hidden Refresh

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (refer to Figure 1.)

Write-Per-Bit Function

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB/WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched into the write-mask register (WM1). When a "0" is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written. When an "1" is sensed on any of the W_i/IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

At the falling edge of $\overline{RAS}$				
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	Wi/IOi (i = 1–4)	Function
H	H	H	•	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

Table 3. Truth Table for Write-Per-Bit Function

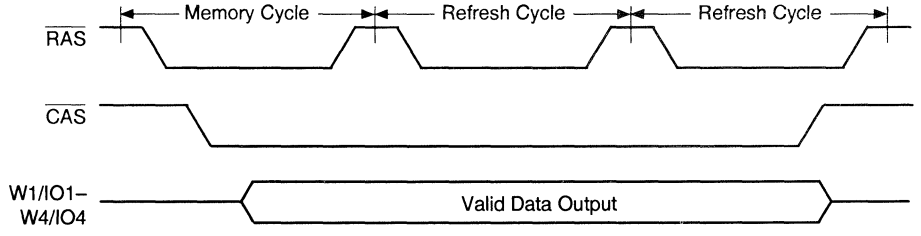


Figure 1. Hidden Refresh Cycle

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

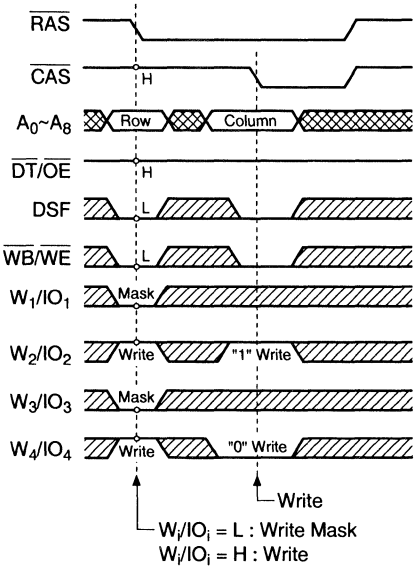


Figure 2. Write-per-bit timing cycle

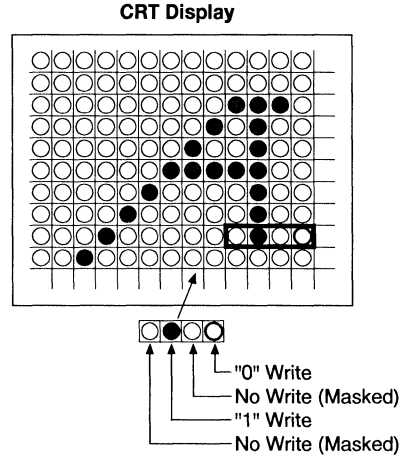


Figure 3. Corresponding bit-map

Load Color Register/Read Color Register

The V52C4258 is provided with an on-chip 4-bits register (color register) for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{WB/WE}$, $\overline{DT/OE}$ and DSF "high" at the falling edge of $\overline{RAS}$. The data presented on the W_i/IO_i lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WB/WE}$, whichever occurs late. The data stored in the color register can be read out by performing a read color register cycle. This cycle is activated by holding $\overline{CAS}$, $\overline{WB/WE}$, $\overline{DT/OE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by holding $\overline{WB/WE}$ "high" at the falling edge of $\overline{CAS}$ and throughout the remainder of the cycle. The data in the color register becomes valid on the W_i/IO_i lines after the specified access times from $\overline{RAS}$ and $\overline{DT/OE}$ are satisfied. During the load/read color register cycle, valid A_0–A_8 row addresses are not required, but the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

Flash Write

Flash write is a special RAM port write operation, which in a single $\overline{RAS}$ cycle allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB/WE}$ "low" and DSF "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ in order to enable the flash write operation for selected I/O blocks (refer to Figures 4 and 5).

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycles and by specifying a different row address location during each flash write cycle (refer to Figure 6). Assuming a cycle time of 180ns, a plane clear operation can be completed in less than 92.2μs.

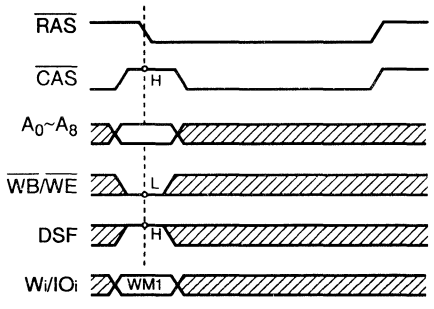


Figure 4. Flash Write Timing

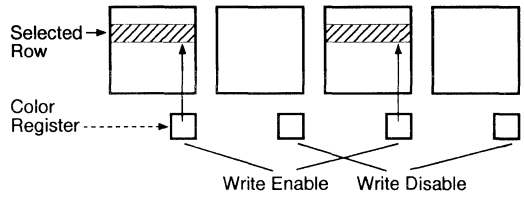


Figure 5. Flash Write

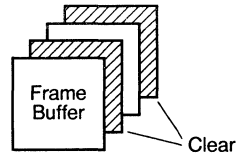


Figure 6. Plane clear application example

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Block Write

Block write is also a special RAM port write operation which, in a single $\overline{RAS}$ cycle, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding $\overline{CAS}$ and $\overline{DT/OE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$ and by holding DSF "high" at the falling edge of $\overline{CAS}$. The state of the $\overline{WB/WE}$ input at the falling edge of $\overline{RAS}$ determines whether or not the I/O data mask is enabled ($\overline{WB/WE}$ must be "low" to enable the I/O data mask or "high" to disable it). At the falling edge of $\overline{RAS}$, a valid row address and I/O mask data are also specified. At the falling edge of $\overline{CAS}$, the starting column address location and column mask data must be provided. During a block write cycle, the 2 least significant column address locations (A0C and A1C) are internally controlled and only the seven most significant column addresses (A2C–A8C) are latched at the falling edge of $\overline{CAS}$. (Refer to Figure 7.)

An example of the block write function is shown in Figure 8 with a data mask on W1/IO1, W4/IO4 and column 2. Block write is most effective for window clear and fill operations in frame buffer applications, as shown on Figure 9.

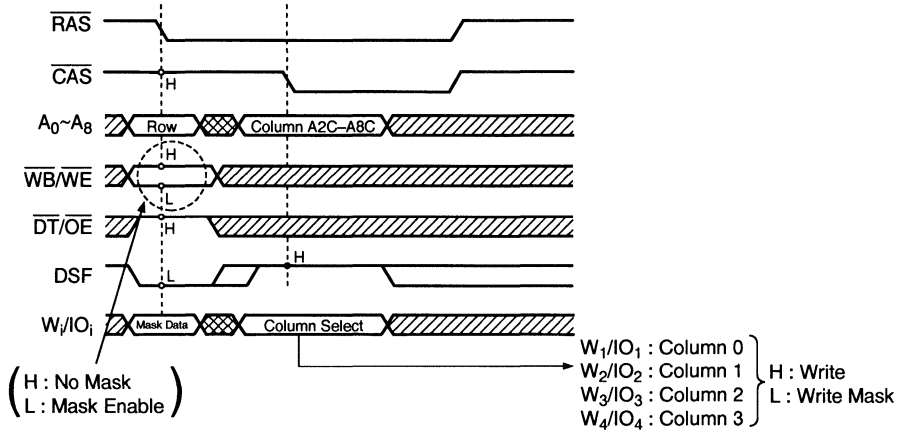


Figure 7. Block Write Timing

	Mask Data	Column Select	Color Register Data
W_1/IO_1	0	1	0
W_2/IO_2	1	1	0
W_3/IO_3	1	0	1
W_4/IO_4	0	1	1

	Column 0	Column 1	Column 2	Column 3	
W_1/IO_1					← Mask
W_2/IO_2	0	0		0	
W_3/IO_3	1	1		1	
W_4/IO_4					← Mask
			↑ Mask		

Figure 8. Example for Block Write

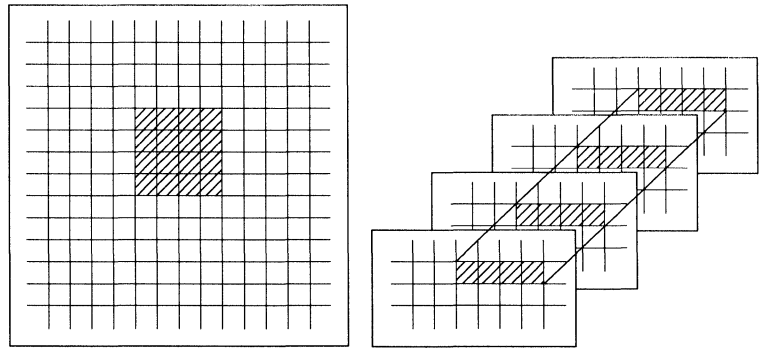


Figure 9. Example of Block Write Application

Fast Page Mode Block Write Cycle

Fast page mode block write can be used to perform high speed clear and fill operaitons. The cycle is initiated by holding the DSF signal "low" at the falling edge of $\overline{RAS}$ and a fast page mode block write is performed during each subsequent $\overline{CAS}$ cycle with DSF held "high" at the falling edge of $\overline{CAS}$.

If the DSF signal is "low" at the falling edge of $\overline{CAS}$, a normal fast page mode read/write operation will occur. Therefore, a combination of block write and read/write operations can be performed

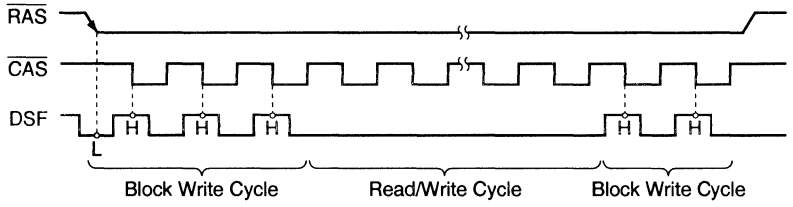


Figure 10. Fast Page Mode Block Write Cycle

during a fast page mode block write cycle (refer to Figure 10).

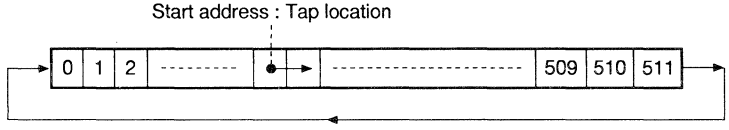
SAM Port Operation

The V52C4258 is provided with a 512 words by 4 bits serial access memory (SAM) which can be operated in the single register mode or in the split register mode.

Single Register Mode

When operating in the single register mode, high speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read/write/ pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM → SAM) has been performed. The data is shifted out of the SAM port starting at any of the 512 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most



significant bit, and then wraps around to the least significant bit, as illustrated below.

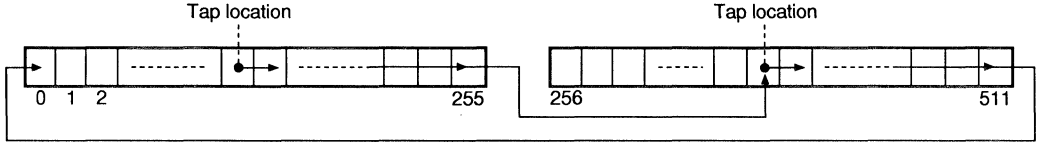
Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode, in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

SAM Port Operation	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	Function	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode	H	⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode	H	⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

Table 4. Truth Table for SAM Port Operation

Split Register Mode

In split register mode, data can be shifted into or out of one half of the SAM while a split read or split write transfer is being performed on the other half of the SAM. A normal (non-split) read/write/pseudo write transfer operation must precede any split read/write transfer operation. The non-split read, write and pseudo write transfers will set the SAM port into output mode or input mode. The split read and write transfers will not change the SAM port mode set by the preceding normal transfer operation. RAM port operation may be performed independently except during split transfers. In the split register mode, serial data can be shifted in or out of one of the split SAM registers starting from any of the 256 tap locations, excluding the last address of each split SAM. Data is shifted in or out sequentially starting from the selected tap location to the most significant bit (255 or 511) of the first split SAM. Then the SAM pointer moves to the tap location selected for the second split SAM, to shift data in or out sequentially starting from this tap location to the most significant bit (511 or 255), and finally wraps around to the least significant bit, as



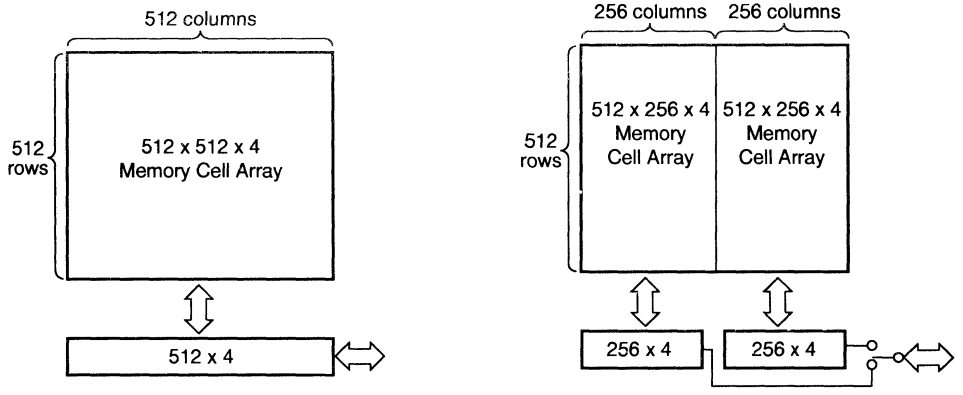
illustrated below.

Refresh

The SAM data registers are static flip-flop, therefore a refresh is not required.

Data Transfer Operation

The V52C4258 features two types of internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 11. During a normal transfer, 512 words by 4 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer). During a split transfer, 256 words by 4 bits of data can be loaded from the lower/upper half of the RAM into the lower/upper half of the SAM (Split Read Transfer) or from the lower/upper half of the SAM into the lower/upper half of the RAM (Split Write Transfer). The normal transfer and split transfer modes are



a. Normal (Non-split) Transfer

b. Split Transfer

Figure 11. Transfer Operation

controlled by the DSF special function input signal.

As shown in Table 5, the V52C4258 supports five types of transfer operations: read transfer, split read transfer, write transfer, split write transfer, and pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$, $\overline{SE}$ and DSF which are latched at the falling edge of $\overline{RAS}$. During normal data transfer operations, the SAM port is switched from input to output mode (Read Transfer) or output to input mode (Write Transfer/Pseudo Write Transfer), whereas it remains unchanged during split transfer operations (Split Read or Split Write Transfer). During a data transfer cycle, the row address A_0–A_8 selects one of the 512 rows of the memory array to or from which data will be transferred, and the column address A_0–A_8 selects one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle. During split data transfer cycles, the most significant column address (A8C) is controlled internally to determine which half of the serial

At the falling edge of $\overline{RAS}$								
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	$\overline{SE}$	DSF	Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
H	L	H	•	L	Read Transfer	RAM → SAM	512 x 4	Input → Output
H	L	L	L	L	Write Transfer	SAM → RAM	512 x 4	Output → Input
H	L	L	H	L	Pseudo Write Transfer	—	—	Output → Input
H	L	H	•	H	Split Read Transfer	RAM → SAM	256 x 4	Not changed
H	L	L	•	H	Split Write Transfer	SAM → RAM	256 x 4	Not changed

Note: • = "H" or "L"

Table 5. Transfer Modes

register will be accessed.

Read Transfer Cycle

A read transfer cycle consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low", $\overline{WB/WE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT/OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT/OE}$ and this data becomes valid on the SIO lines after the specified access time (t_{SCA}) from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 12 shows the operation block diagram for the read transfer operation.

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay (t_{TSD}) from the

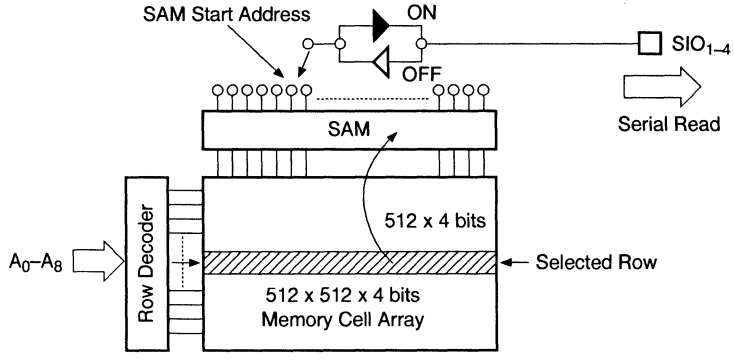


Figure 12. Block Diagram for Read Transfer Operation

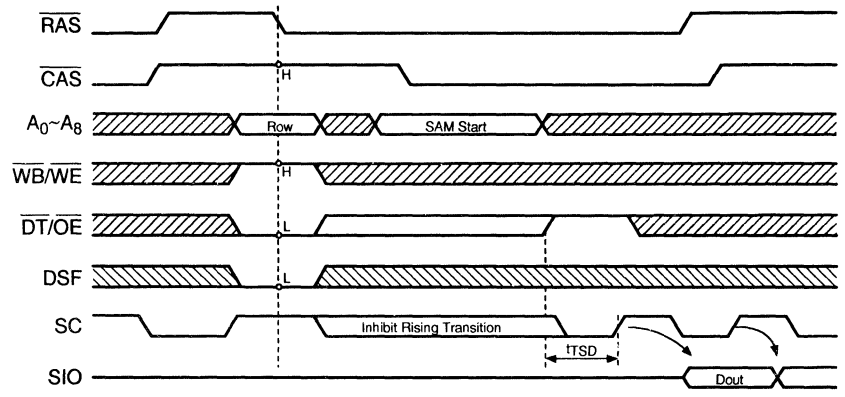


Figure 13. Read Transfer Timing

rising edge of $\overline{DT}/\overline{OE}$, as shown in Figure 13.

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time (t_{SCA}) for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 14.

The timing restrictions t_{TSL}/t_{TSD} are 5ns min/15ns min. The split read transfer mode eliminates these timing restrictions.

Write Transfer Cycle

A write transfer cycle consists of loading the contents of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "low" and DSF "low" at the falling edge of $\overline{RAS}$. This write transfer is selectively controlled per RAM I/O block by setting the mask data on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ (same as in the write-per-bit operation). Figures 15 and 16 show the timing diagram and block diagram

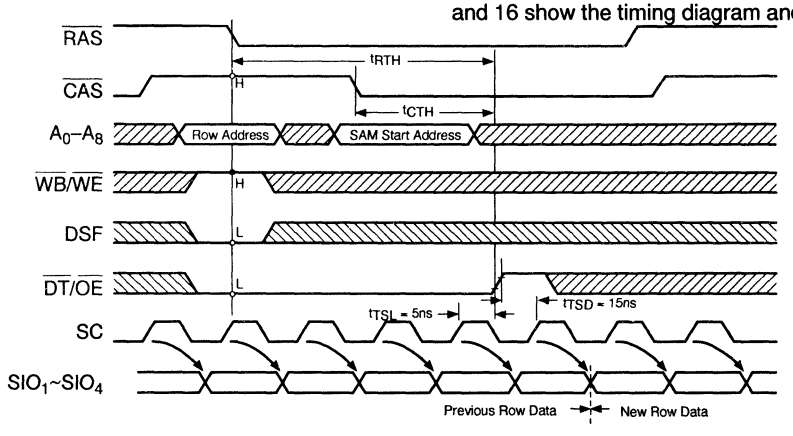


Figure 14. Real Time Read Transfer

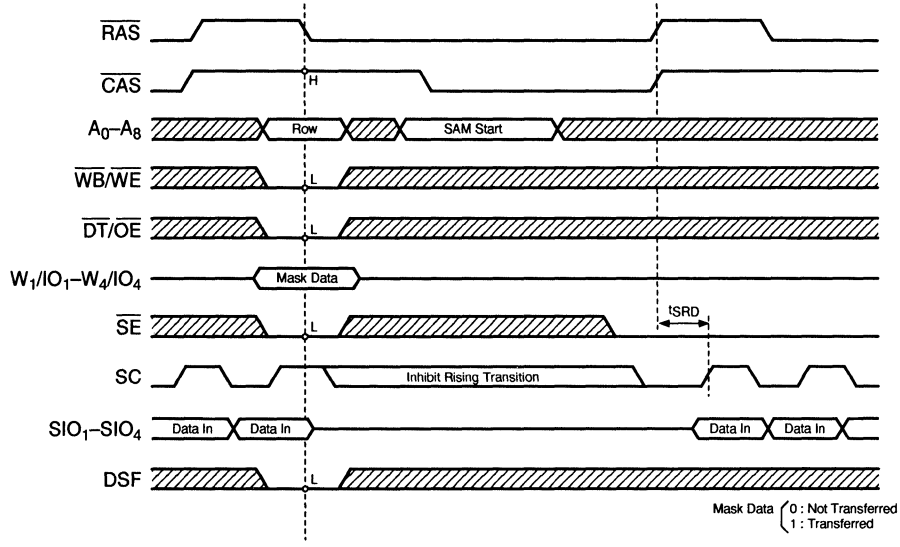


Figure 15. Write Transfer Timing

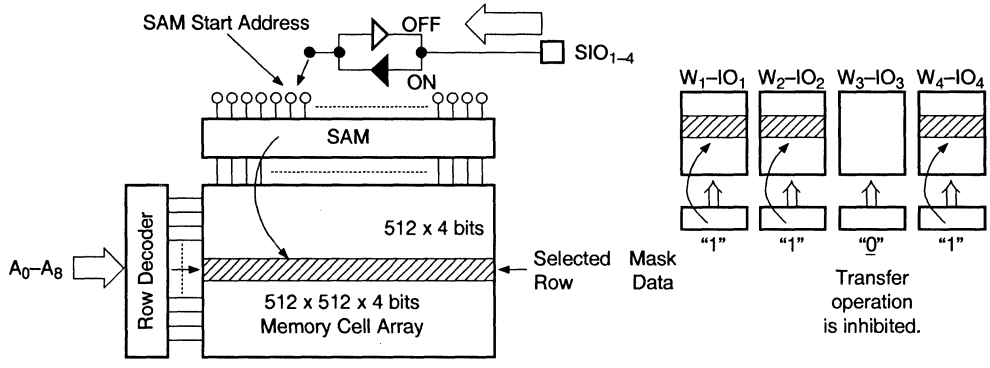


Figure 16. Block Diagram for Write Transfer Operation

for write transfer operations, respectively.

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay (t_{SRD}) from the rising edge of $\overline{RAS}$, at which time a new row of data

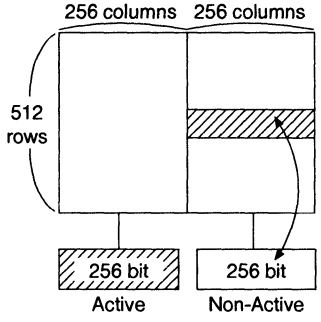
can be written in the serial register.

Pseudo Write Transfer Cycle

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (a data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low", $\overline{WB/WE}$ "low", $\overline{SE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

Split Data Transfer and QSF

The V52C4258 features a bidirectional split data transfer capability between the RAM and the SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or split write transfer operations can be performed to or from one half of the serial register while serial data can be shifted into or out of the other half of the serial register, as shown in Figure 17. The most significant column address location (A8C) is controlled internally to determine which half of the serial register will be accessed. QSF is an output which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM, as shown in



Active SAM	QSF Level
lower SAM	"Low"
upper SAM	"High"

Figure 17. Split Register Mode

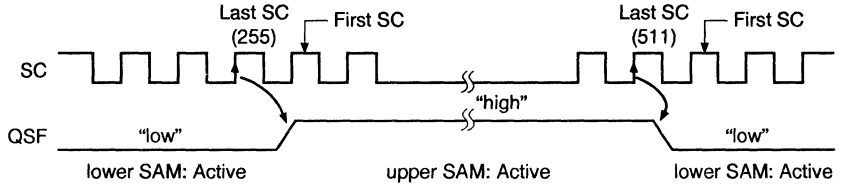


Figure 18. QSF Output State During Split Register Mode

Figure 18.

Split Read Transfer Cycle

A split read transfer consists of loading 256 words by 4 bits of data from a selected row of the split RAM array into the corresponding non-active split SAM register.

Serial data can be shifted out of the other half of the split SAM register simultaneously. The block diagram and timing diagram for split read transfer mode are shown in Figures 19 and 20, respectively. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of on-the-fly read transfers. A split read transfer can be performed after a delay of t_{STS} from the change of state of the QSF output is satisfied.

A normal (non-split) read transfer operation must precede split read transfer cycles as shown in the

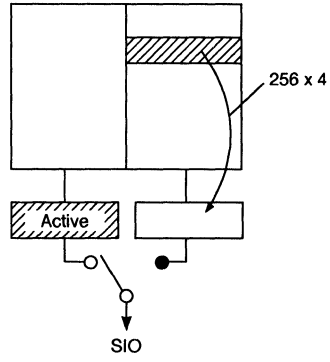


Figure 19. Block Diagram for Split Read Transfer

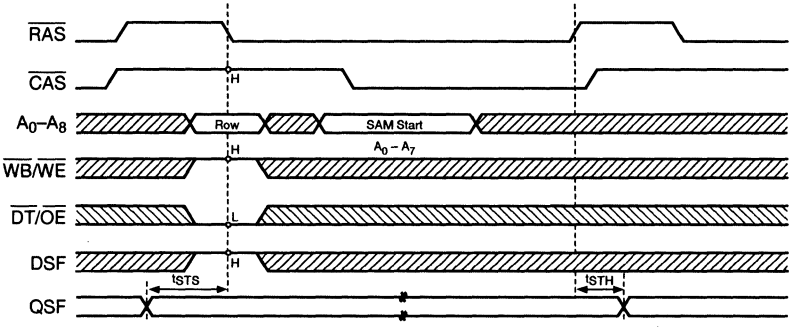


Figure 20. Timing Diagram for Split Read Transfer

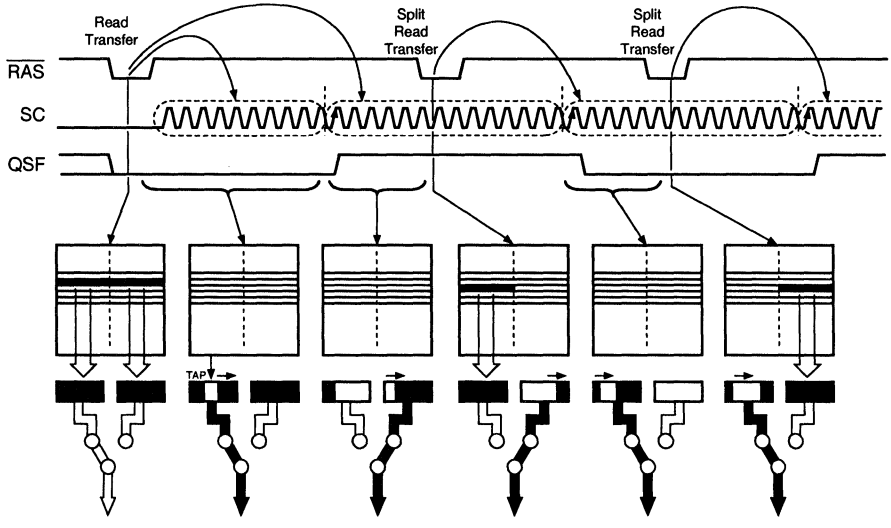


Figure 21. Example of Consecutive Read Transfer Operations

Split Write Transfer Cycle

A split write transfer cycle consists of loading 256 words by 4 bits of data from the non-active split SAM register into a selected row of the corresponding split RAM array.

Serial data can be shifted into the other half of the split SAM register simultaneously. The block diagram and timing diagram for split write transfer mode are shown in Figures 22 and 23, respectively. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. A split write transfer can be performed after a delay of t_{STS} from the change of state of the QSF output is satisfied.

A pseudo write transfer operation must precede split transfer cycles as shown in Figure 24. The purpose of the pseudo write transfer operation is to switch the SAM port from output mode to input mode and to set the initial tap location prior to split write transfer operations.

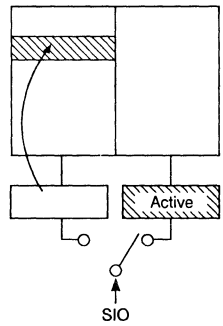


Figure 22. Block Diagram for Split Write Transfer

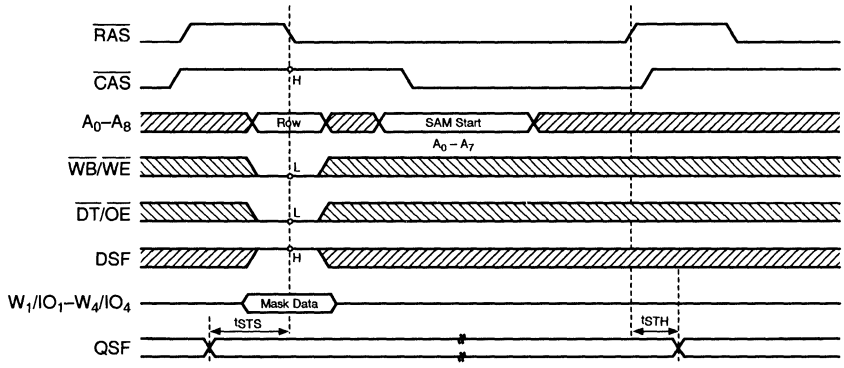


Figure 23. Timing Diagram for Split Write Transfer

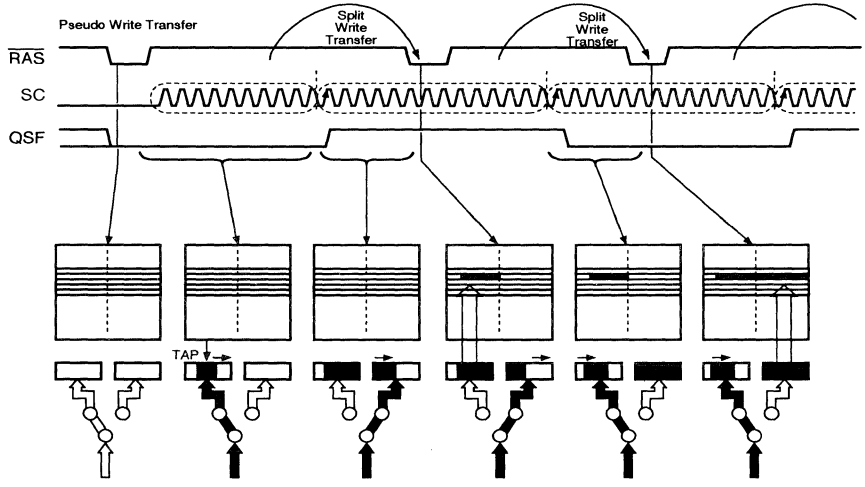


Figure 24. Example of Consecutive Write Transfer Operations

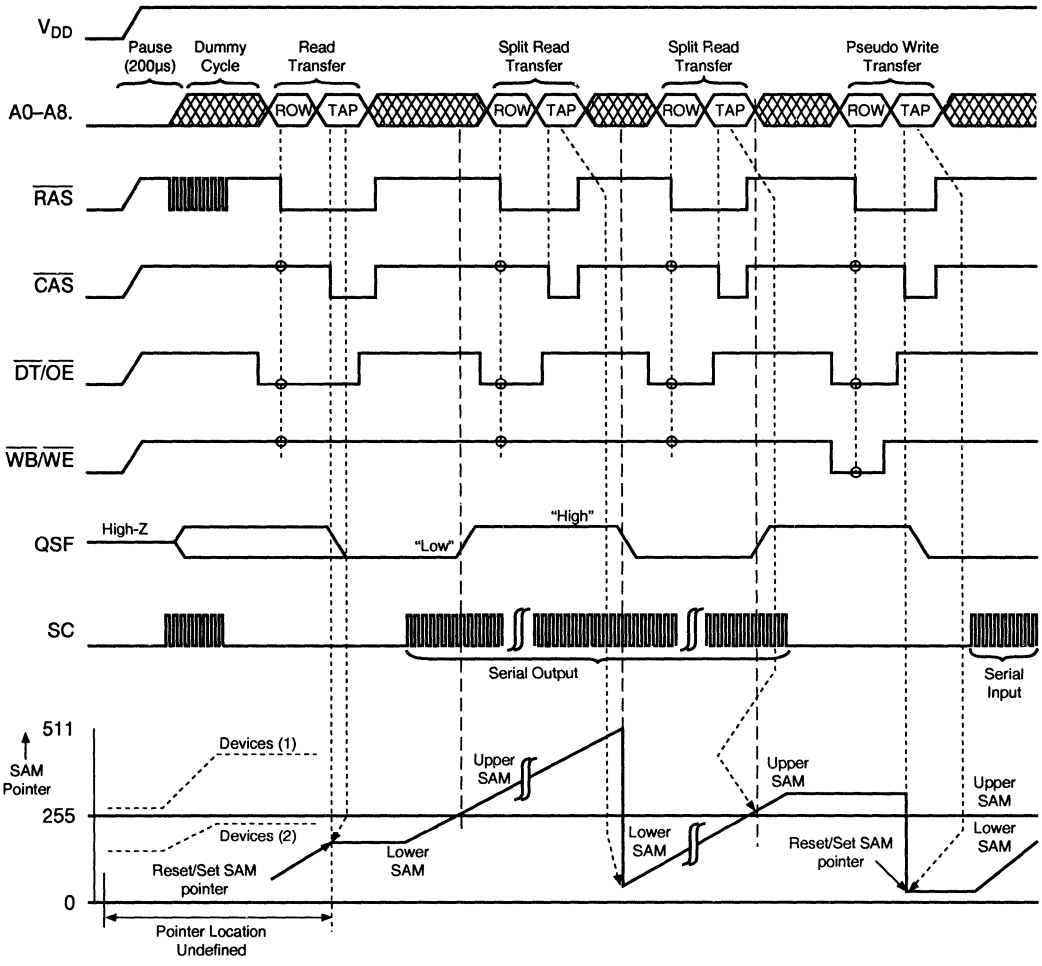


Figure 25. Example of Split SAM Register Operation Sequence

Split-Register Operation Sequence - Example

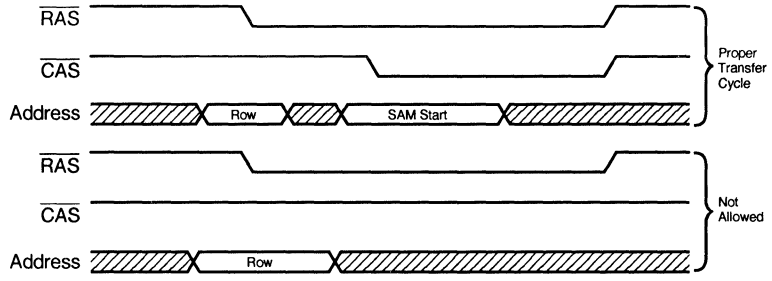
Split read/write transfers must be preceded by a normal (non-split) transfer, such as a read, write or pseudo write transfer. Figure 25 illustrates an example of split register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location, which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 511), and wraps around to the tap location set by the split read transfer performed for the lower SAM while the upper SAM is being accessed. The SAM address is incremented as long as SC is clocked. The following split read transfer sets a new tap location in the upper split SAM register (address 256 in this example), and the pointer is incremented from this location by cycling the SC clock.

example in Figure 21.

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for either write transfers or split write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

Transfer Operation Without $\overline{CAS}$

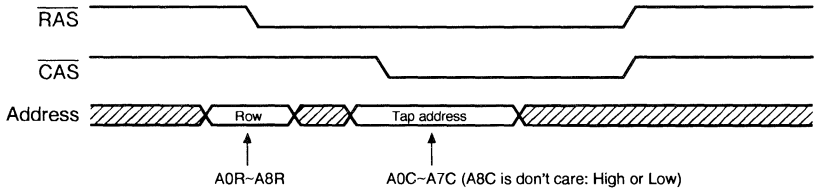
During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column addresses are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore, a transfer cycle with $\overline{CAS}$ held "high" is not allowed (refer to



the illustration below).

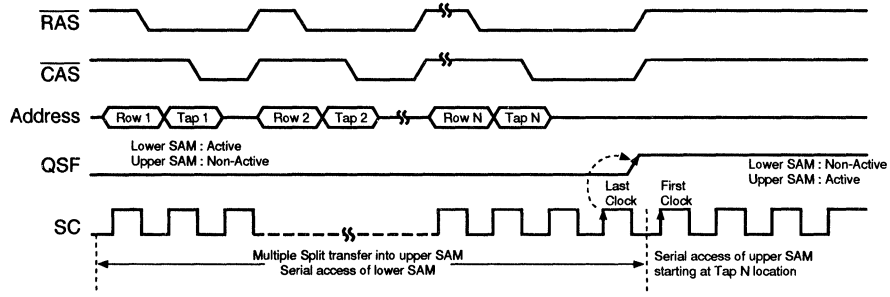
Tap Location Selection in Split Transfer Operation

a. In a split transfer operation, column addresses A0C through A7C must be latched at the falling edge of $\overline{CAS}$ in order to set the tap location in one of the split SAM registers. During a split transfer, column address A8C is controlled internally and therefore it is ignored internally at the falling edge of $\overline{CAS}$. During a split transfer, it is not allowed to set the last address location (A0C–A7C = FF), in



either the lower SAM or the upper SAM, as the tap location.

b. In the case of multiple split transfers performed into the same split SAM register, the tap location specified during the last split transfer, before QSF toggles, will prevail. In the example shown below, multiple split transfers are performed into the upper SAM (non-active) while the lower SAM (active) is being accessed at the time when QSF toggles, the first SC serial clock will start shifting serial data starting from the Tap N address location.



Split Read/Write Transfer Operation Allowable Period

Figure 26 illustrates the relationship between the serial clock SC and the special function output QSF during split read/write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF. As indicated in Figure 26, a split read/write transfer is not allowed during the period of $t_{STH} + t_{STS}$.

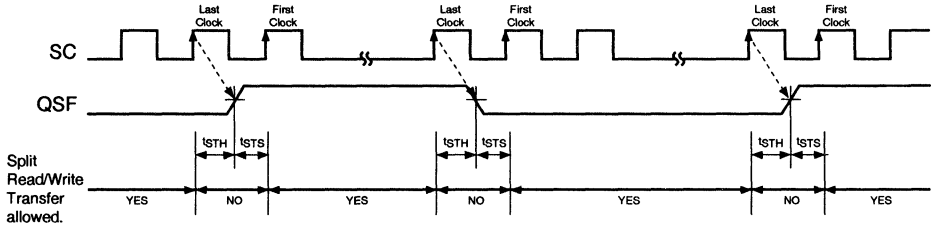
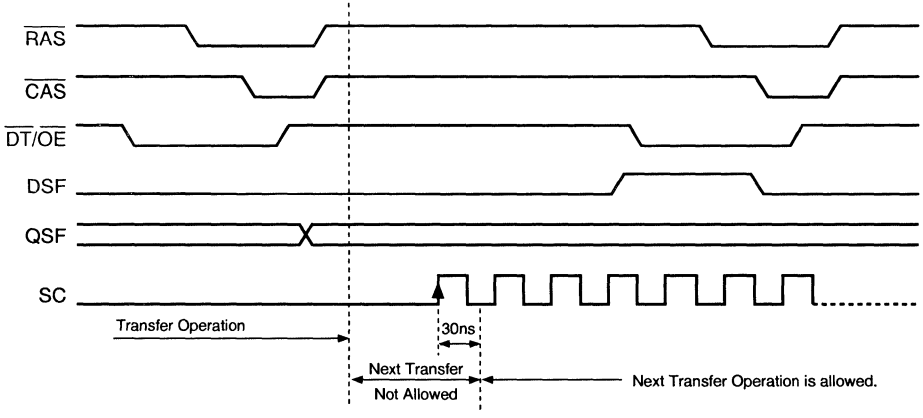


Figure 26. Split Transfer Operation Allowable Periods

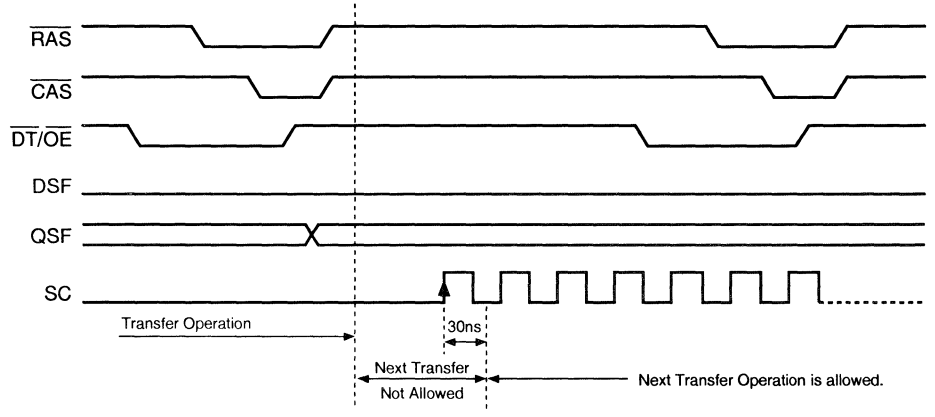
Split Transfer Cycle After Normal Transfer Cycle

A split transfer may be performed following a normal transfer (Read/Write/Pseudo-Write transfer) provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (refer to the illustration shown below).



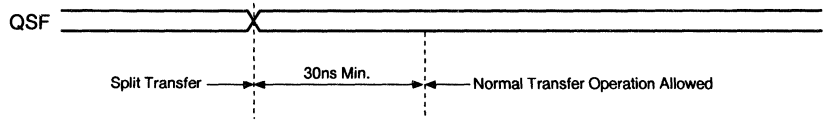
Normal Read Transfer Cycle After Normal Read Transfer Cycle

Another read transfer may be performed following the read transfer provided that a minimum delay of 30 ns from the rising edge of the first clock SC is satisfied (refer to the illustration shown below).



Normal Transfer After Split Transfer

A normal transfer (read/write/psuedo write) may be performed following split transfer operation provided that a 30ns minimum delay is satisfied after the QSF signal toggles.



Power-Up

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{DD} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

Initial State After Power-Up

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the V52C4258 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μs pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
WM1 Register	Write Enable
TAP pointer	Invalid

MULTIPORT VIDEO RAM WITH 128K X 8 DRAM AND 256 X 8 SAM

HIGH PERFORMANCE V52C8126	70	80	10
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	20 ns	25 ns	25 ns
Max. Column Address Access Time, (t_{AA})	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns
Min. Read/Write Cycle Time, (t_{RC})	140 ns	150 ns	180 ns
Max. Serial Access Time, (t_{SCA})	25 ns	25 ns	25 ns
Min. Serial Port Cycle Time, (t_{SCC})	30 ns	30 ns	30 ns

Features

- Organization
  - RAM Port: 131,072 words x 8 bits
  - SAM Port: 256 words x 8 bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write, Write-Per-Bit
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
  - 512 Refresh Cycles/8 ms
- SAM Port
  - High Speed Serial Read/Write Capability
  - 256 Tap Locations
  - Fully Static Register
- RAM-SAM Bidirectional Transfer
  - Read/Write/Pseudo Write Transfer
  - Real Time Read Transfer
- Low Power Dissipation
  - RAM Port Operating Alone – 90 mA
  - SAM Port Operating Alone – 50 mA
- Low Standby Current – 7 mA
- Package
  - 40 pin 400 mil SOJ
  - 40 pin 475 mil ZIP

Description

The V52C8126 VRAM is equipped with a 131,072-words by 8-bits dynamic random access memory (RAM) port and a 256-words by 8-bits static serial access memory (SAM) port. The V52C8126 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

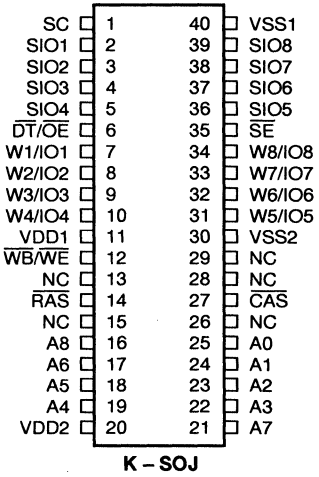
The V52C8126 is fabricated in CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

Device Usage Chart

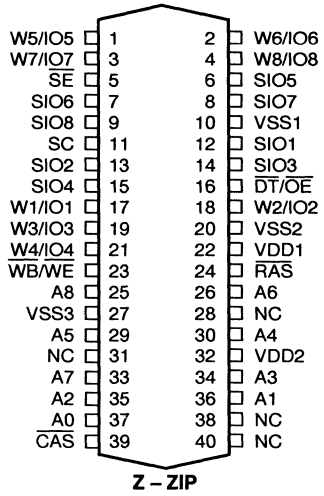
Operating Temperature Range	Package Outline		Access Time (ns)			Power	Temperature Mark
	K	Z	70	80	100	Std	
0°C–70°C	•	•	•	•	•	•	Blank

Description	Pkg.	Pin Count
SOJ	K	40
ZIP	Z	40

40 Lead Pin Configuration



K – SOJ



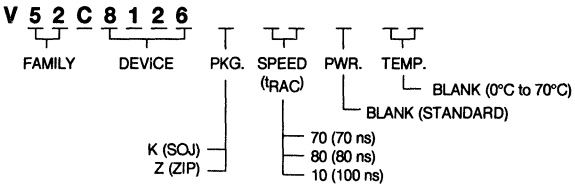
Z – ZIP

Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF

*Note: Capacitance is sampled and not 100% tested.



Pin Names

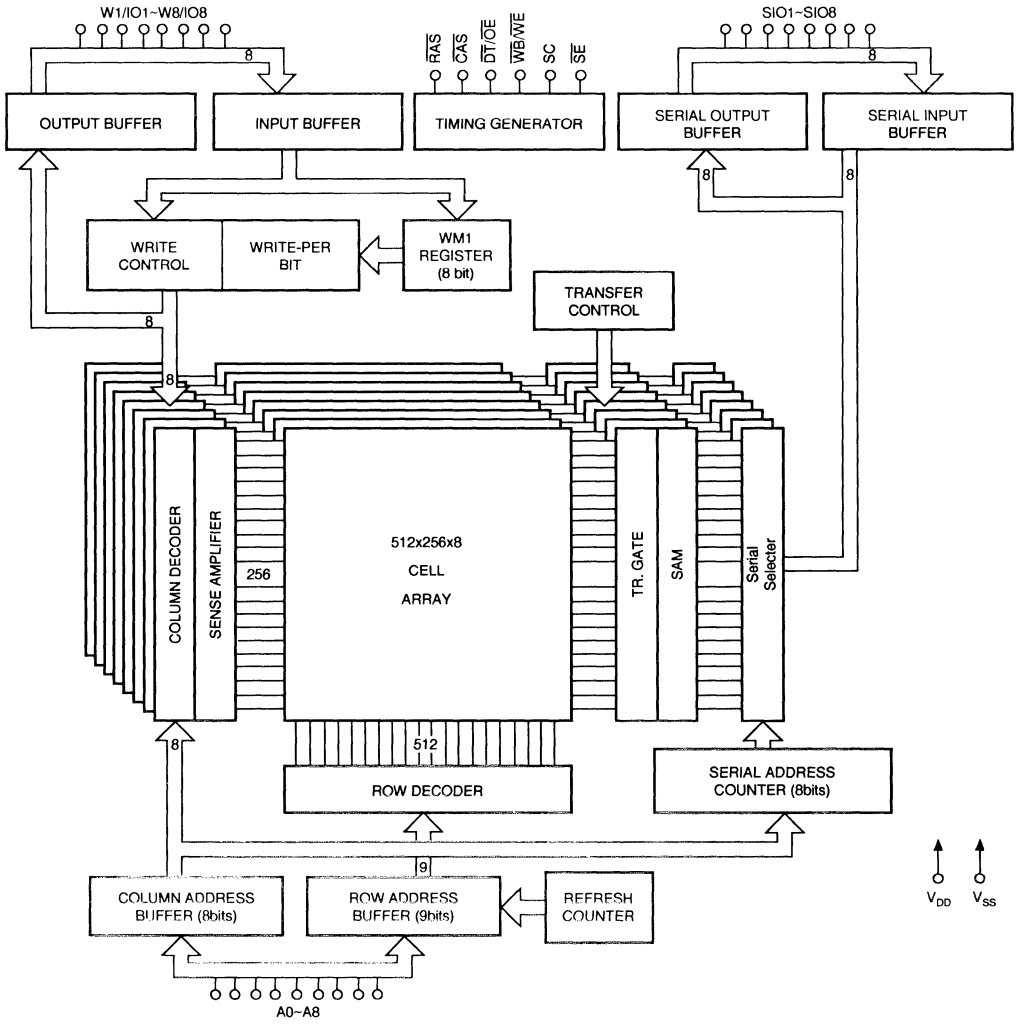
Name	Description
A0-A8	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
DT/OE	Data Transfer/Output Enable
WB/WE	Write per Bit/Write Enable
W1/IO1-W8/IO8	Write Mask/Data In, Out
SC	Serial Clock
SE	Serial Enable
SIO1-SIO8	Serial Input/Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 to +7.0 V
Short Circuit Out Current ..... 50 mA
Power Dissipation ..... 1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Functional Diagram



DC and Operating Characteristics

(V_{DD} = 5V ± 10%, T_A = 0–70°C)

Symbol	Parameter (RAM Port)	SAM Port	V52C8126-70		V52C8126-80		V52C8126-10		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{DD1}	Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD1A}		Active		125		115		105	mA	1,2
I_{DD2}	Standby Current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	Standby		7		7		7	mA	
I_{DD2A}		Active		50		45		40	mA	1,2
I_{DD3}	$\overline{RAS}$-Only Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD3A}		Active		125		115		105	mA	1,2
I_{DD4}	Page Mode Current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} Min.	Standby		75		70		65	mA	1,2
I_{DD4A}		Active		125		115		105	mA	1,2
I_{DD5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD5A}		Active		125		115		105	mA	1,2
I_{DD6}	Data Transfer Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD6A}		Active		125		115		105	mA	1,2
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V		-10	10	-10	10	-10	10	µA	
$I_{O(L)}$	Output Leakage Current 0V ≤ V_{OUT} ≤ 5.5V, Output Disable		-10	10	-10	10	-10	10	µA	
V_{OH}	Output "H" Level Voltage I_{OUT} = -2mA		2.4		2.4		2.4		V	
V_{OL}	Output "L" Level Voltage I_{OUT} = 2mA			0.4		0.4		0.4	V	
V_{IH}	Input High Voltage		2.4	V_{DD}+1	2.4	V_{DD}+1	2.4	V_{DD}+1	V	
V_{IL}	Input Low Voltage		-1.0	0.8	-1.0	0.8	-1.0	0.8	V	

AC Electrical Characteristics *Notes: 3, 4, 5*

Symbol	Parameter	V52C8126-70		V52C8126-80		V52C8126-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	140		150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	195		195		235		ns	
t_{PC}	Fast Page Mode Cycle Time	45		50		55		ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		90		100		ns	
t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	6, 12
t_{AA}	Access Time from Column Address		35		40		50	ns	6, 12
t_{CAC}	Access Time from $\overline{CAS}$		20		25		25	ns	6, 13
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		40		45		50	ns	6, 13
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20	0	20	ns	8
t_T	Transition Time (Rise and Fall)	3	35	3	35	3	35	ns	5
t_{RP}	$\overline{RAS}$ Precharge Time	60		60		70		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode only)	70	100K	80	100K	100	100K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20		25		25		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	25	10K	25	10K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	55	20	75	ns	12
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40		55		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10		10		ns	
t_{ASR}	Row Address Setup Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		10		ns	
t_{ASC}	Column Address Setup Time	0		0		0		ns	
t_{CAH}	Column Address Hold Time	15		15		15		ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		55		70		ns	
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	9
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		0		ns	9
t_{WCH}	Write Command Hold Time	15		15		15		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		55		70		ns	
t_{WP}	Write Command Pulse Width	15		15		15		ns	

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	V52C8126-70		V52C8126-80		V52C8126-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		ns	
t_{DS}	Data Setup Time	0		0		0		ns	10
t_{DH}	Data Hold Time	15		15		15		ns	10
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		55		70		ns	
t_{WCS}	Write Command Setup Time	0		0		0		ns	11
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		100		130		ns	11
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		65		80		ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		45		55		ns	11
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0		0		ns	
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0		0		ns	
t_{OEA}	Access Time from $\overline{OE}$		20		20		25	ns	6
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	0	10	0	10	0	20	ns	8
t_{OED}	$\overline{OE}$ to Data Delay Time	10		10		20		ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	10		10		20		ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15		15		ns	
t_{CSR}	$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0		0		ns	
t_{REF}	Refresh Period		8		8		8	ms	
t_{WSR}	$\overline{WB}$ Setup Time	0		0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	15		15		15		ns	
t_{MS}	Write-Per-Bit Mask Data Setup Time	0		0		0		ns	
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15		15		ns	
t_{THS}	$\overline{DT}$ High Setup Time	0		0		0		ns	
t_{THH}	$\overline{DT}$ High Hold Time	15		15		15		ns	
t_{TLS}	$\overline{DT}$ Low Setup Time	0		0		0		ns	
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10K	15	10K	15	10K	ns	
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	60	10K	65	10K	80	10K	ns	
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	25		30		30		ns	
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	20		25		25		ns	

AC Electrical Characteristics (Cont'd)

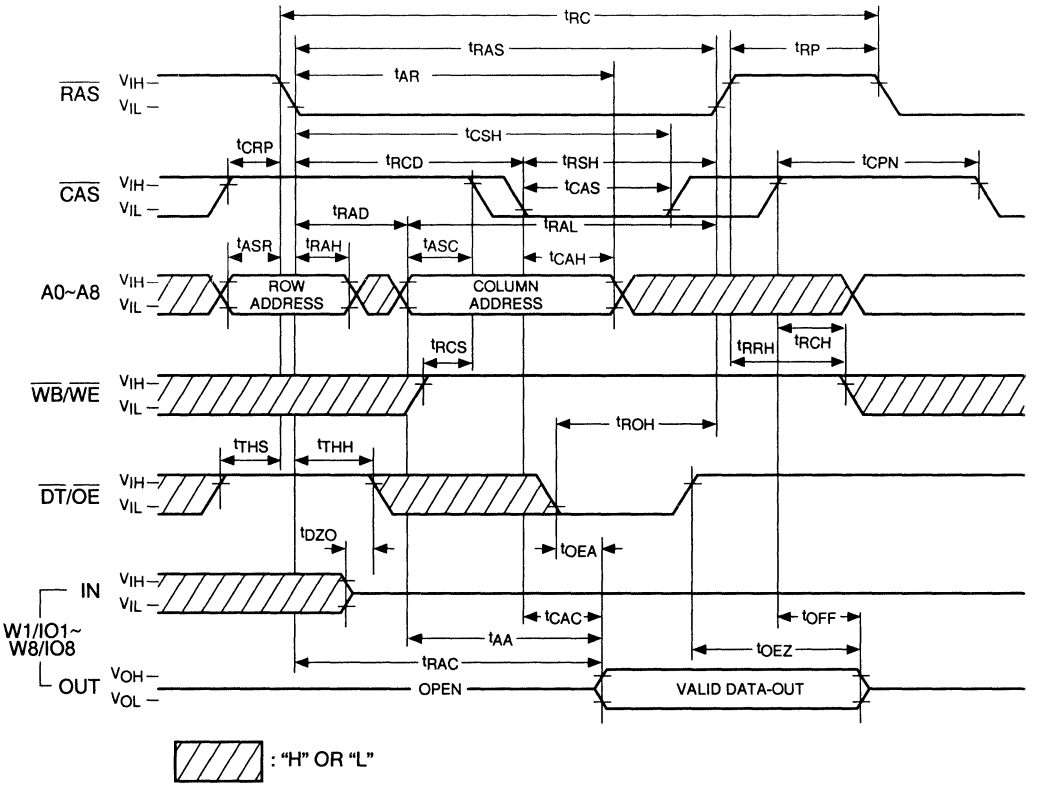
Symbol	Parameter	V52C8126-70		V52C8126-80		V52C8126-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{ESR}	$\overline{SE}$ Setup Time referenced to $\overline{RAS}$	0		0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15		15		ns	
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		60		70		ns	
t_{TP}	$\overline{DT}$ Precharge Time	20		20		30		ns	
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	70		80		100		ns	
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		45		50		ns	
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	20		25		25		ns	
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5		5		ns	
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15		15		ns	
t_{SRS}	Last SC to $\overline{RAS}$ Setup Time (Serial Input)	25		25		30		ns	
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	20		20		25		ns	
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	40		40		50		ns	
t_{SDZ}	Serial Output Buffer Turn-Off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	40	10	40	10	50	ns	8
t_{SCC}	SC Cycle Time	30		30		30		ns	
t_{SC}	SC Pulse Width (SC High Time)	10		10		10		ns	
t_{SCP}	SC Precharge Time (SC Low Time)	10		10		10		ns	
t_{SCA}	Access Time from SC		25		25		25	ns	7
t_{SOH}	Serial Output Hold Time from SC	5		5		5		ns	
t_{SDS}	Serial Input Setup Time	0		0		0		ns	
t_{SDH}	Serial Input Hold Time	15		15		15		ns	
t_{SEA}	Access Time from $\overline{SE}$		25		25		25	ns	7
t_{SE}	$\overline{SE}$ Pulse Width	25		25		25		ns	
t_{SEP}	$\overline{SE}$ Precharge Time	25		25		25		ns	
t_{SEZ}	Serial Output Buffer Turn-Off Delay from $\overline{SE}$	0	20	0	20	0	20	ns	8
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0		0		ns	
t_{SZS}	Serial Input to First SC Delay Time	0		0		0		ns	
t_{SWS}	Serial Write Enable Setup Time	5		5		5		ns	
t_{SWH}	Serial Write Enable Hold Time	15		15		15		ns	
t_{SWIS}	Serial Write Disable Setup Time	5		5		5		ns	
t_{SWIH}	Serial Write Disable Hold Time	15		15		15		ns	

Notes

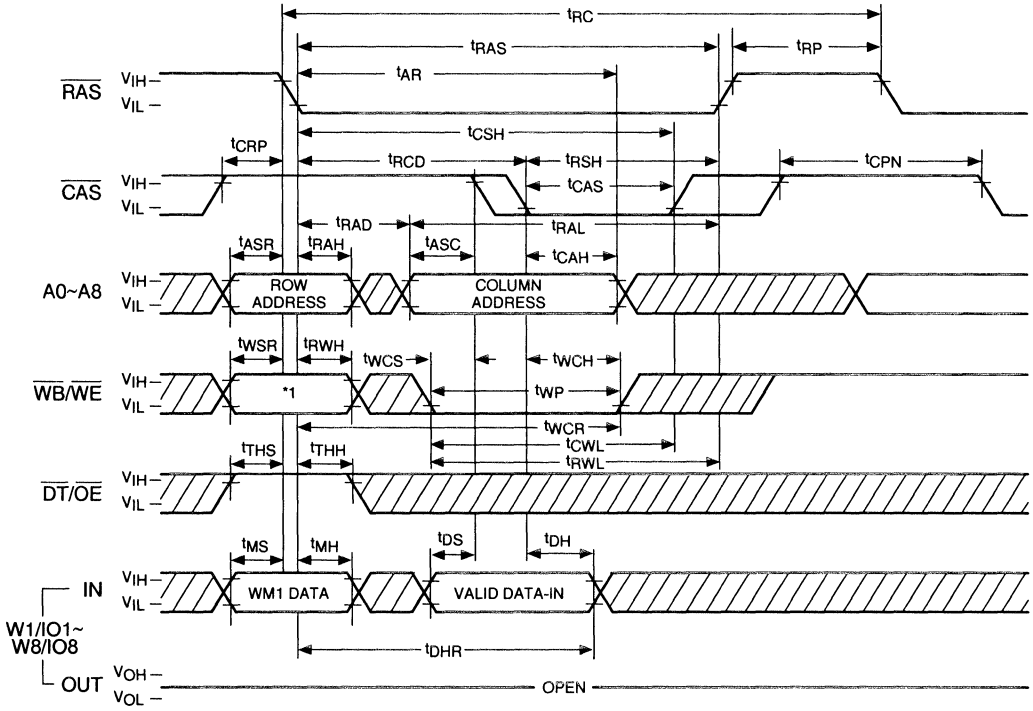
1. These parameters depend on cycle rate.
2. These parameters depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC measurements assume t_T = 5 ns.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. RAM port outputs are measured with a load equivalent to 1 TTL load and 100 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
7. SAM port outputs are measured with a load equivalent to 1 TTL load and 30 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
8. t_{OFF} (max.), t_{OEZ} (max.), t_{SDZ} (max.) and t_{SEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
12. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

Read Cycle



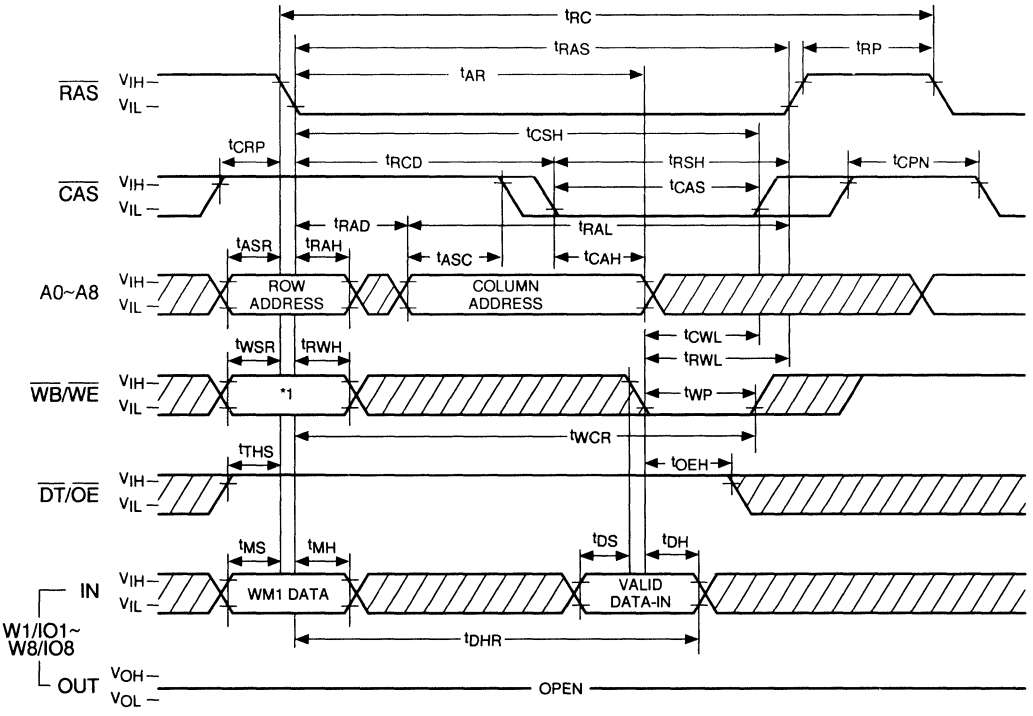
Write Cycle (Early Write)



*1 WB/WE	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

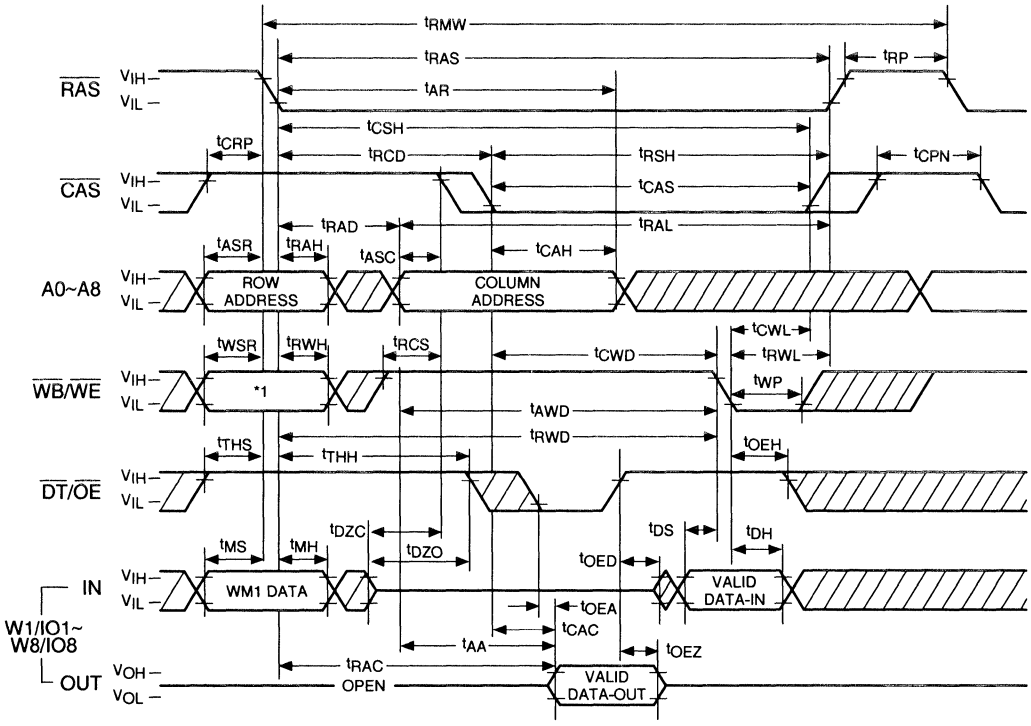
Write Cycle ($\overline{OE}$ Controlled Write)



*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

Read-Modify-Write Cycle

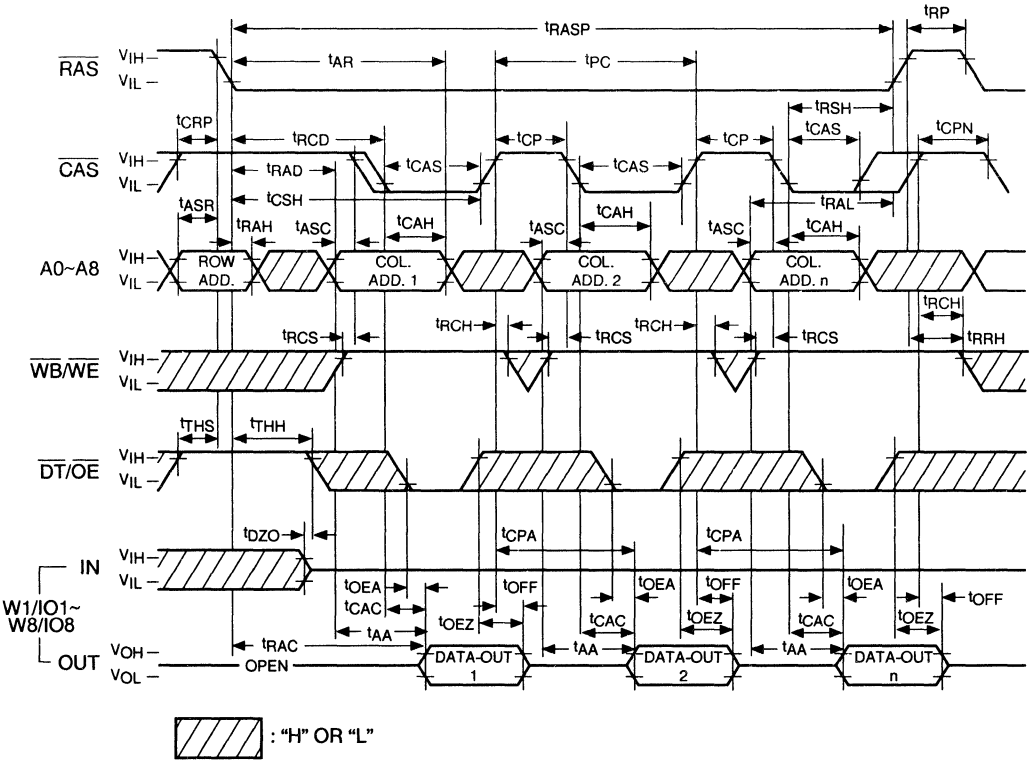


*1 WB/WE	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

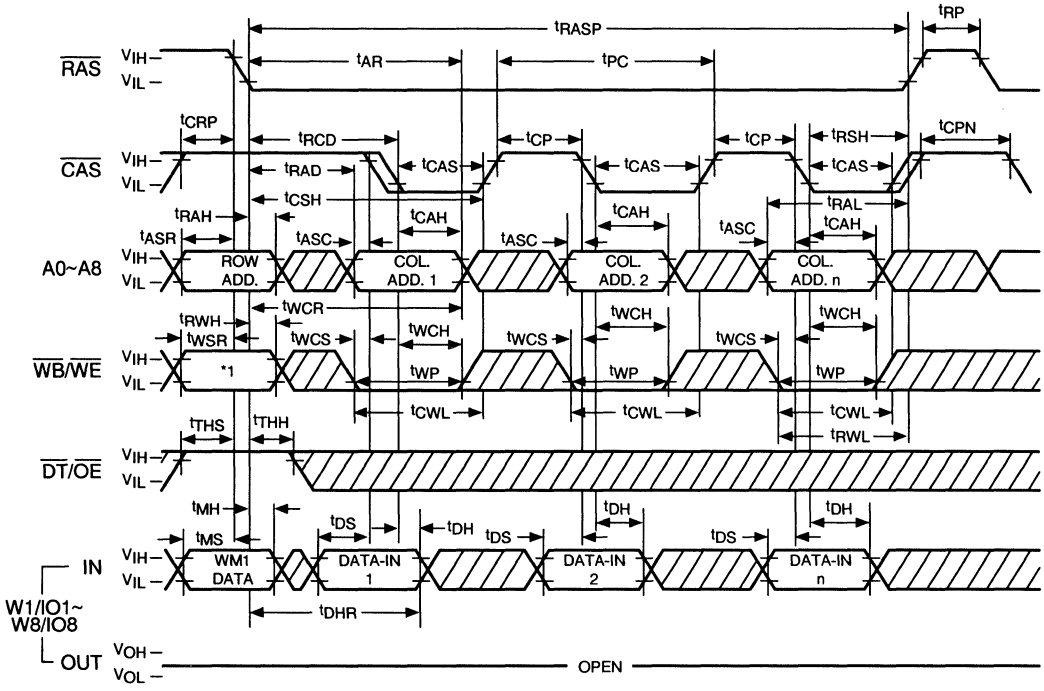
WM1 data: 0: Write Disable
1: Write Enable

: "H" OR "L"

Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)

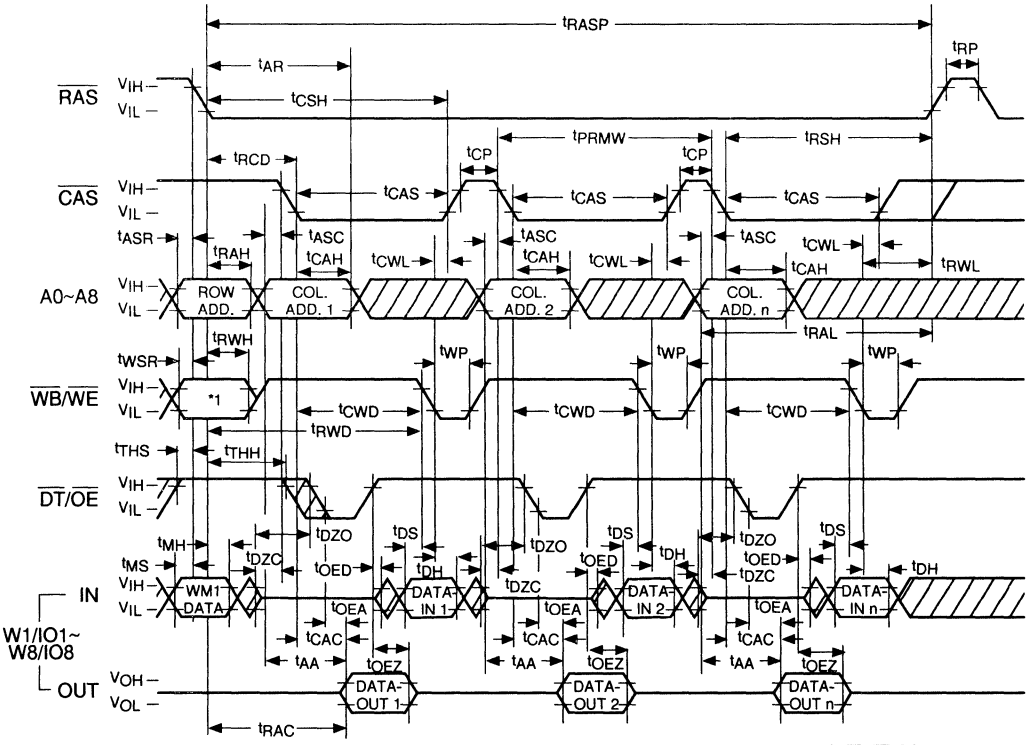


: "H" OR "L"

*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

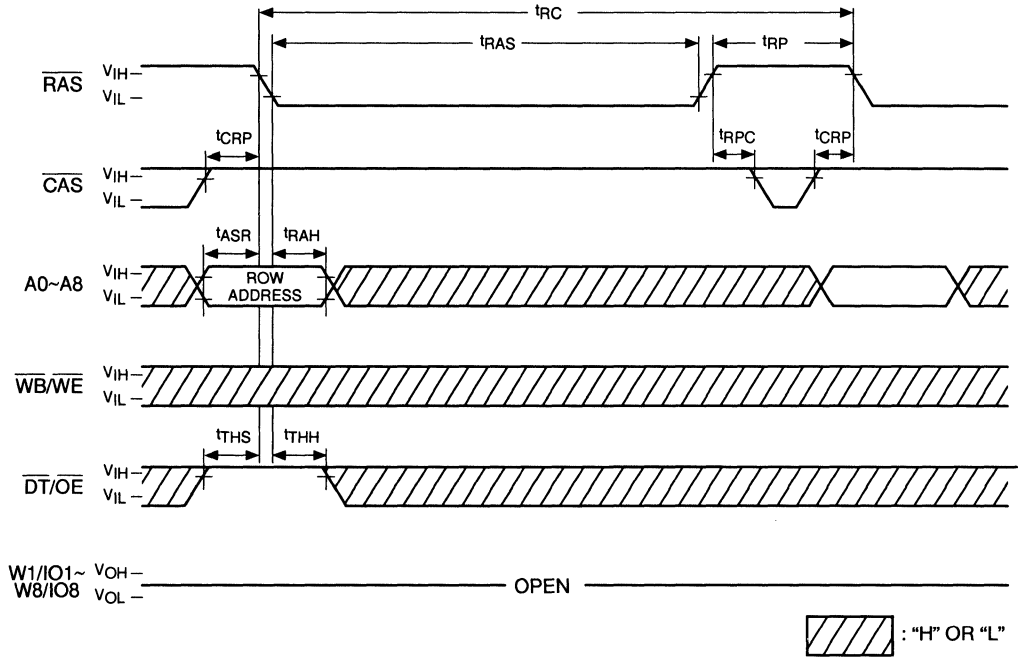
Fast Page Mode Read-Modify-Write Cycle



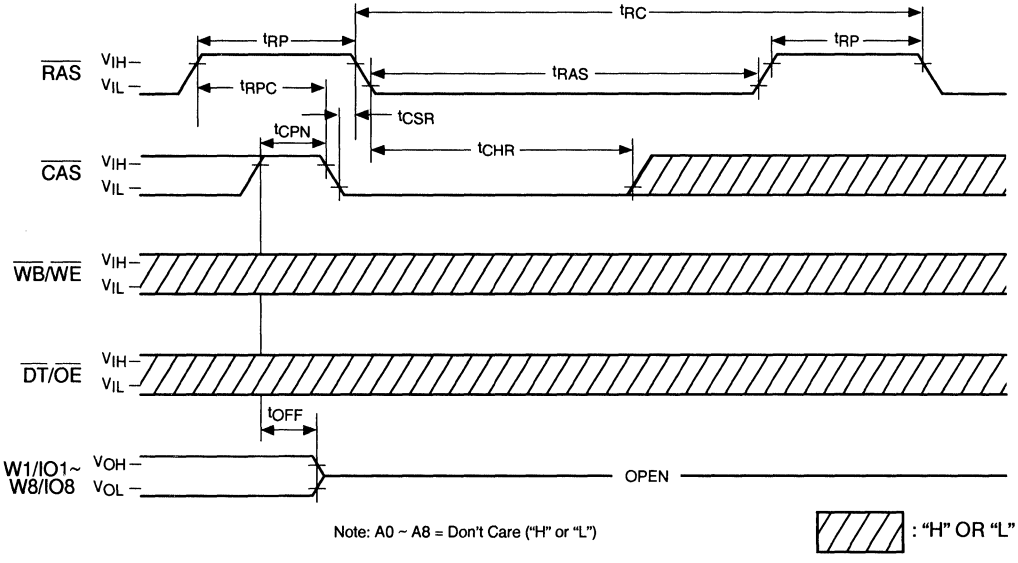
*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

$\overline{RAS}$ Only Refresh Cycle

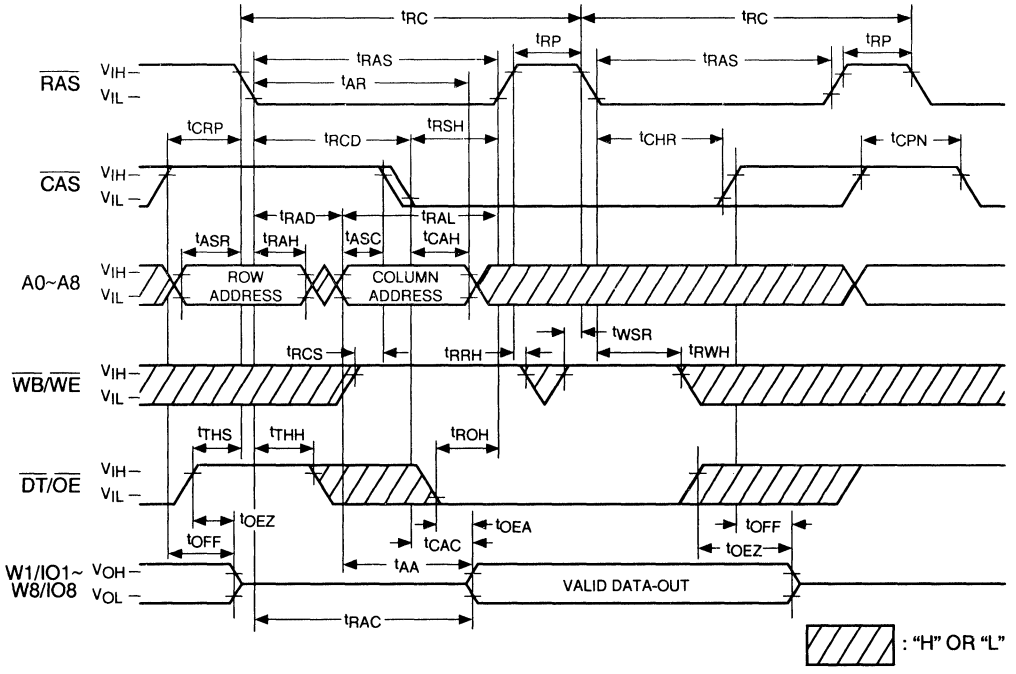


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

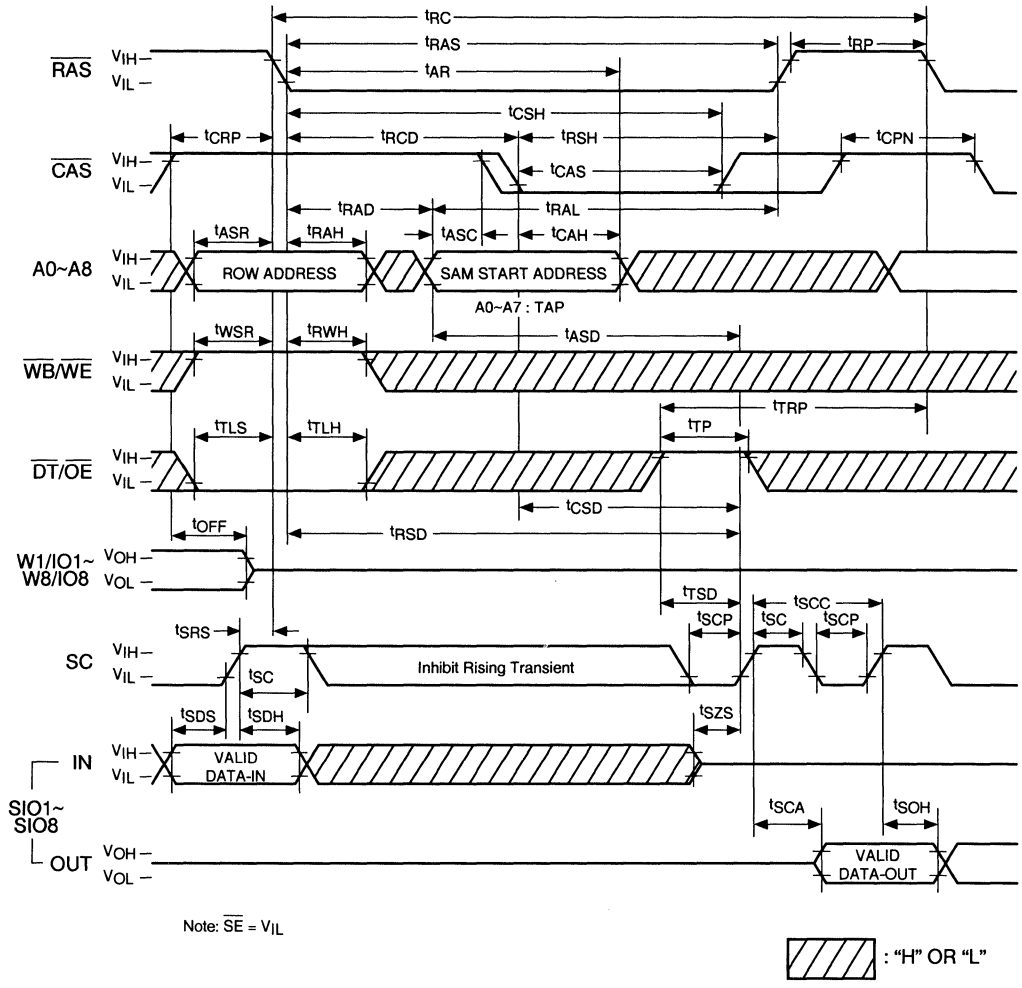


Note: A0 ~ A8 = Don't Care ("H" or "L")

Hidden Refresh Cycle



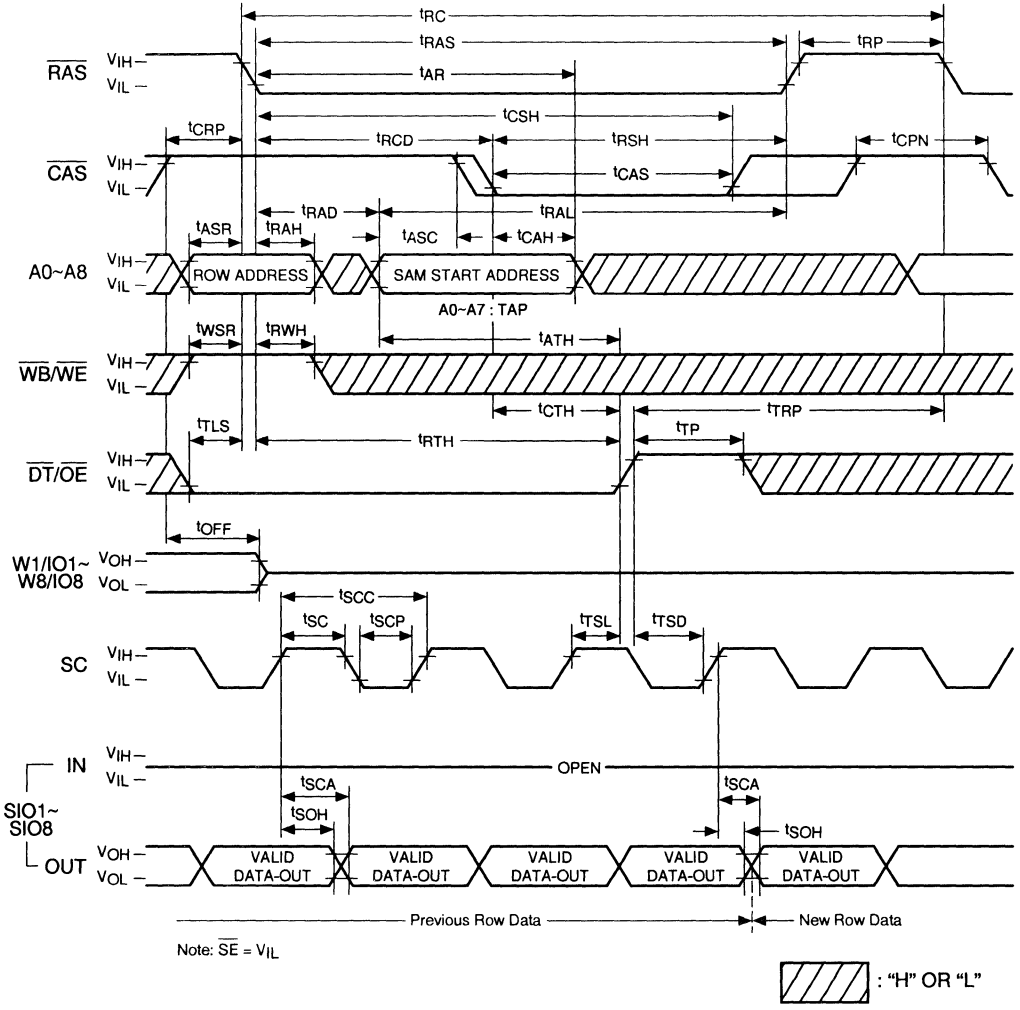
Read Transfer Cycle (Previous Transfer is Write Transfer Cycle)



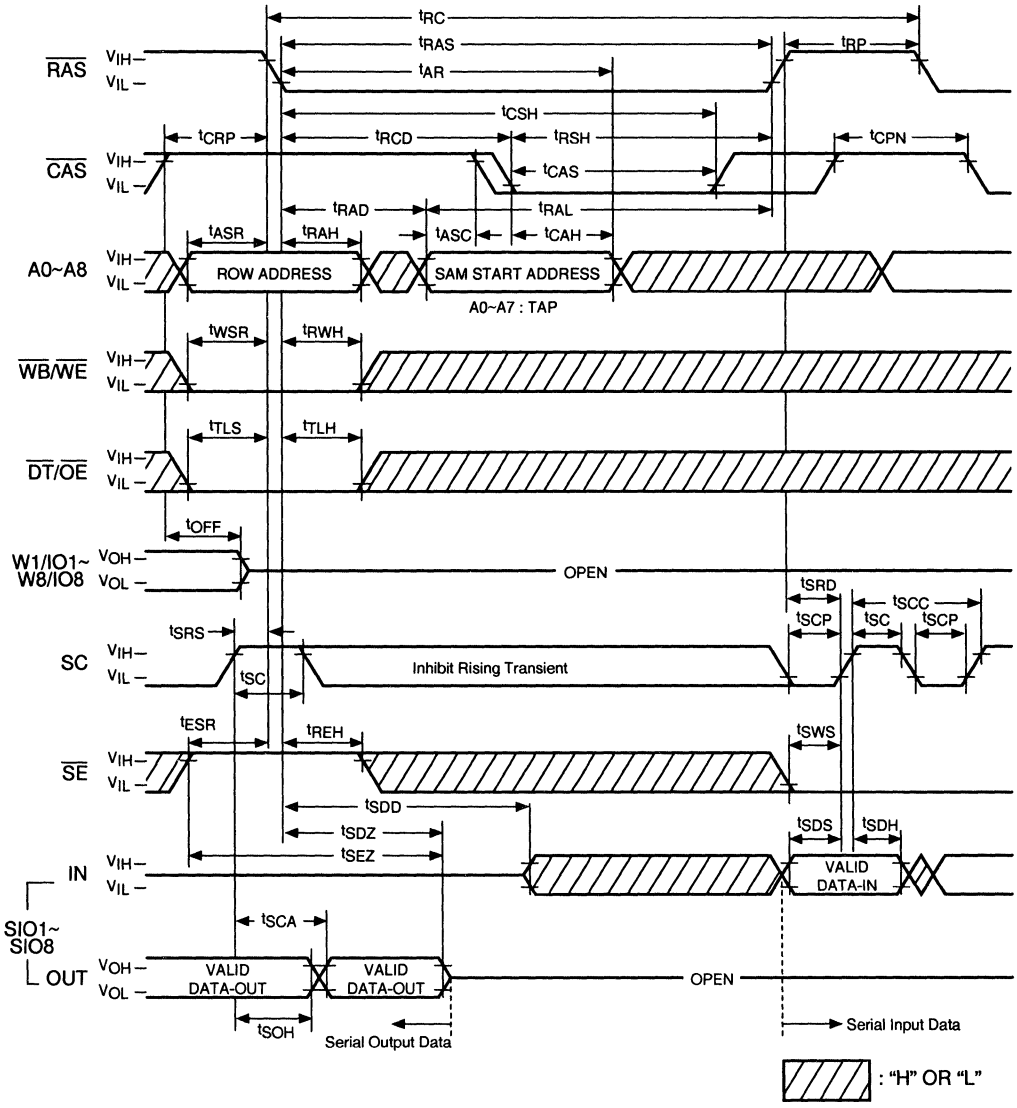
Note: $\overline{SE}$ = V_{IL}

: "H" OR "L"

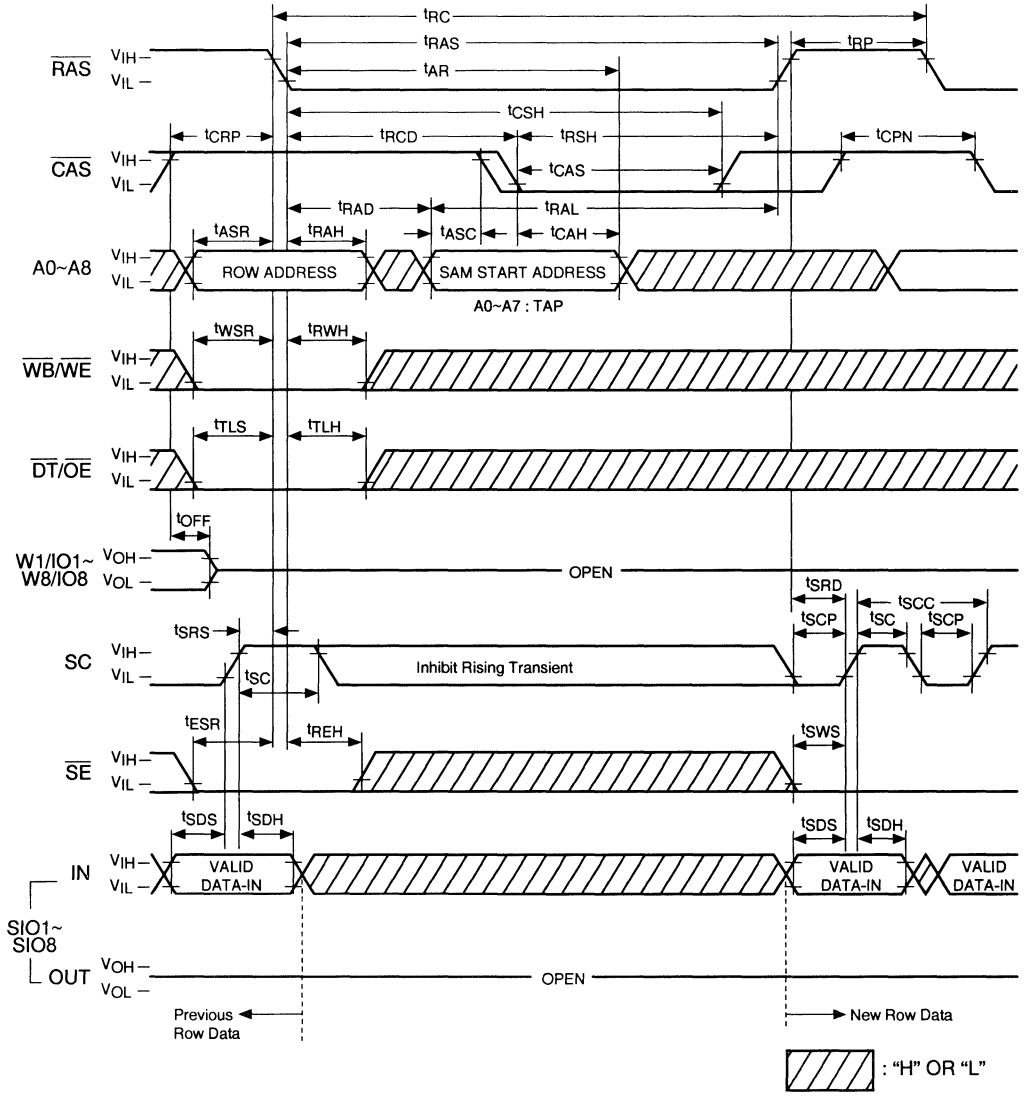
Real Time Read Transfer Cycle



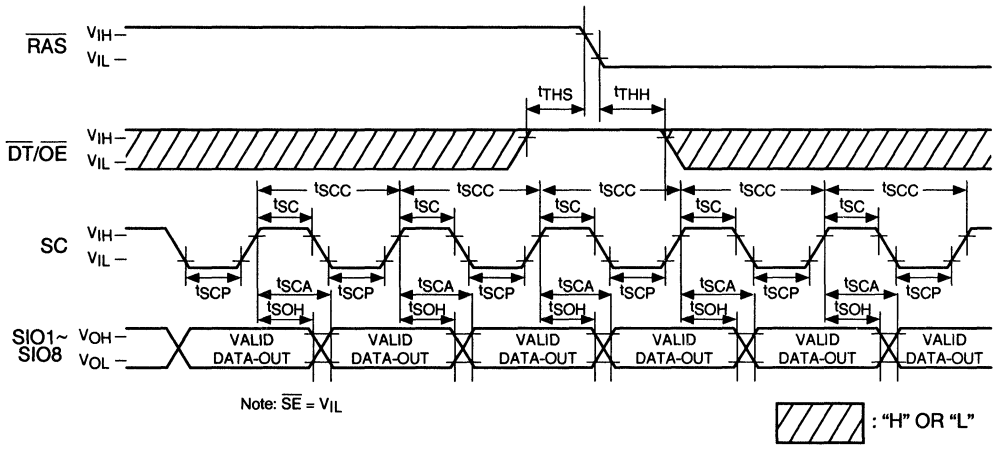
Pseudo Write Transfer Cycle



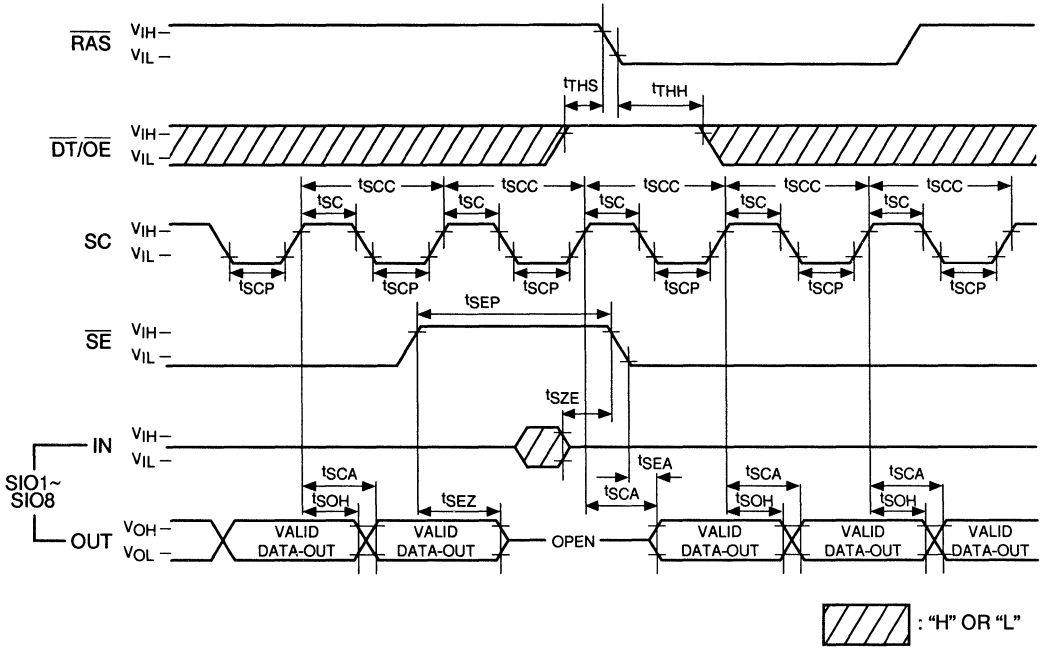
Write Transfer Cycle



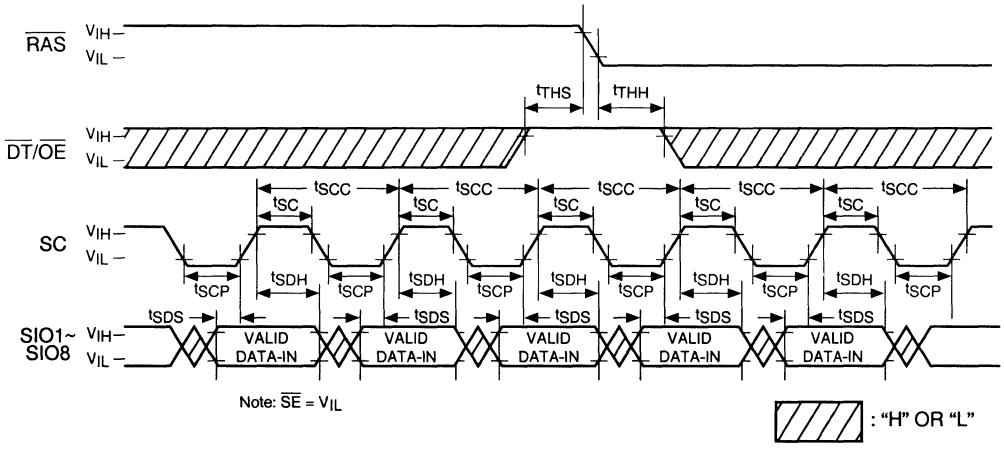
Serial Read Cycle ($\overline{SE}$ = V_{IL})



Serial Read Cycle ($\overline{SE}$ Controlled Outputs)

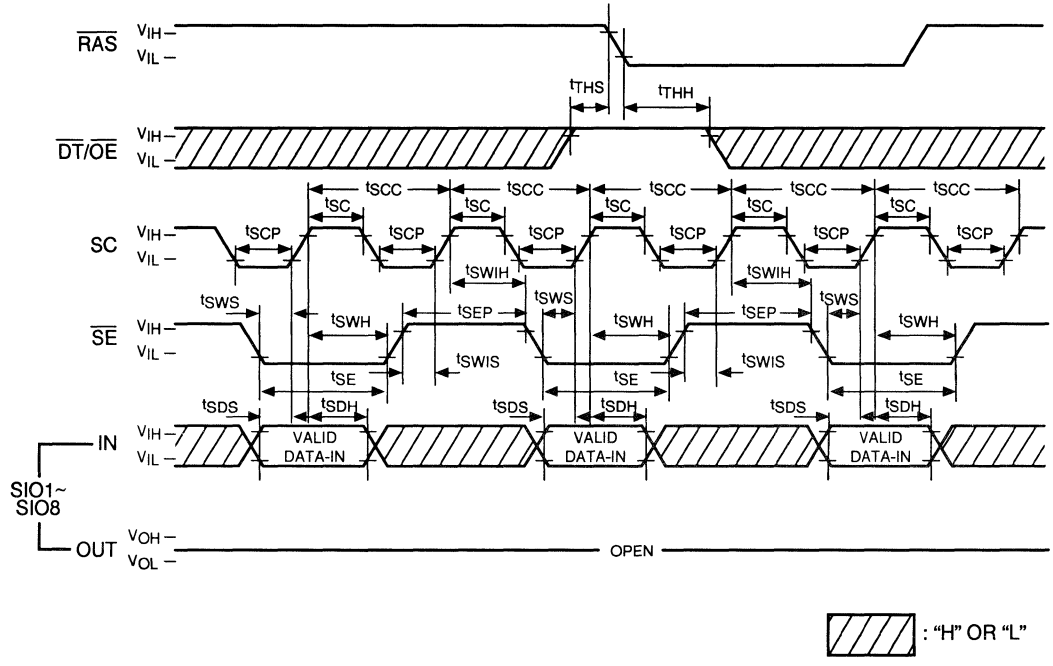


Serial Write Cycle ($\overline{SE}$ = V_{IL})



3

Serial Write Cycle ($\overline{SE}$ Controlled Inputs)



Pin Functions

Address Inputs: A0–A8

The 17 address bits required to decode 8 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the V52C8126 are multiplexed onto 9 address input pins (A_0–A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following eight column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

Row Address Strobe: $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$ and $\overline{SE}$ to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

Column Address Strobe: $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

Data Transfer/Output Enable: $\overline{DT/OE}$

The $\overline{DT/OE}$ input is a multifunction pin. When $\overline{DT/OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT/OE}$ is used as an output enable control. When the $\overline{DT/OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

Write Per Bit/Write Enable: $\overline{WB/WE}$

The $\overline{WB/WE}$ input is also a multifunction pin. When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB/WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).

When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (write transfer).

Write Mask Data/Data Input and Output: W_1/IO_1–W_8/IO_8

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB/WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT/OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT/OE}$, whichever occurs first.

Serial Clock: SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 8-bits serial pointer which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the normal transfer cycle. When the pointer reaches the most significant address location (decimal 255), the next SC clock will place it at the least significant address location (decimal 0). The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read/pseudo write/write transfer operations and should not be clocked while the SAM port is in the standby mode, to prevent the SAM pointer from being incremented.

Serial Enable: $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

Serial Input/Output: SIO1–SIO8

Serial input and output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During the subsequent write transfer cycle, the SAM remains in the input mode.

Operation Mode

The RAM port and data transfer operating of the V52C8126 are determined by the state of $\overline{CAS}$, $\overline{DT}$/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$, and $\overline{SE}$ at the falling edge of $\overline{RAS}$. The Table 1 and Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operations, respectively.

Table 1. Operation Truth Table

$\overline{RAS}$ Falling Edge ↓				
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	$\overline{SE}$	Function
0	•	•	•	$\overline{CAS}$-before-$\overline{RAS}$ Refresh
1	0	0	0	Write Transfer
1	0	0	1	Pseudo Write Transfer
1	0	1	•	Read Transfer
1	1	0	•	Read/Write per Bit
1	1	1	•	Read/Write

Table 2. Functional Truth Table

Function	$\overline{RAS}$↓				Address		*W/IO*		Write Mask
	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	$\overline{SE}$	$\overline{RAS}$↓	$\overline{CAS}$↓	$\overline{RAS}$↓	$\overline{CAS}$↓ $\overline{WE}$↓	WM1
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	0	•	•	•	•	–	•	–	–
Write Transfer	1	0	0	0	Row	TAP	•	•	–
Pseudo Write Transfer	1	0	0	1	Row	TAP	•	•	–
Read Transfer	1	0	1	•	Row	TAP	•	•	–
Write per Bit	1	1	0	•	Row	Column	WM1	DIN	Load use
Read/Write	1	1	1	•	Row	Column	•	DIN	–

Note : • = "0" or "1", TAP = SAM Start Address, – = not used.

RAM Port Operation

Fast Page Mode Cycle

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple CAS cycles during a single active RAS cycle. During a fast page cycle, the RAS signal may be maintained active for a period up to 100 µs. For the initial fast page mode access, the output data is valid after the specified access times from RAS, CAS, column address and DT/OE. For all subsequent fast page mode read operations, the output data is valid after the specified access times from CAS, column address and DT/OE. When the write-per-bit function is enabled, the mask data latched at the falling edge of RAS is maintained throughout the fast page mode write or read-modify-write cycle.

RAS-Only Refresh

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with the "RAS-Only" cycle.

CAS-before-RAS Refresh

The V52C8126 also offers an internal-refresh function. When CAS is held "low" for a specified period (t_{CSR}) before RAS goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next CAS-before-RAS cycle. For successive CAS-before-RAS refresh cycles, CAS can remain "low" while cycling RAS.

Hidden Refresh

A hidden refresh is a CAS-before-RAS refresh performed by holding CAS "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling RAS after the specified RAS-precharge period (refer to Figure 1.)

Write-Per-Bit Function

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When WB/WE is held "low" at the falling edge of RAS, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched into the write-mask register (WM1). When a "0" is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written. When an "1" is sensed on any of the W_i/IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

At the falling edge of RAS				
CAS	DT/OE	WB/WE	Wi/IOi (i = 1–8)	Function
H	H	H	•	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

Table 3. Truth Table for Write-Per-Bit Function

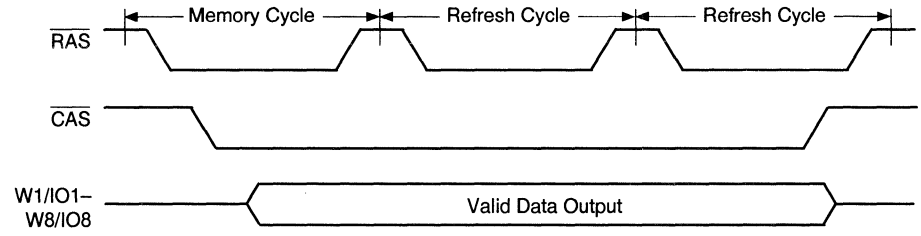


Figure 1. Hidden Refresh Cycle

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

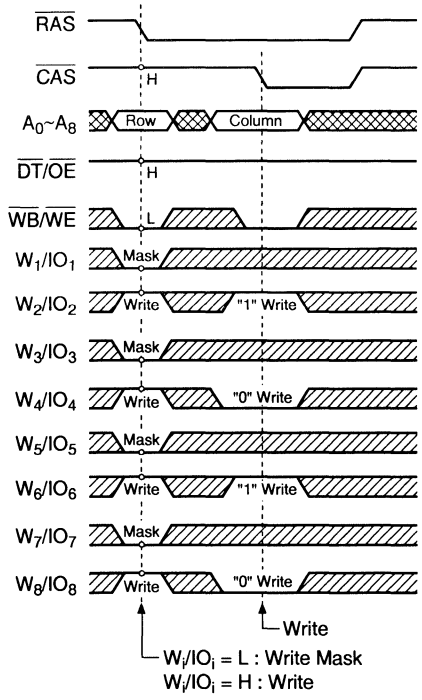


Figure 2. Write-per-bit timing cycle

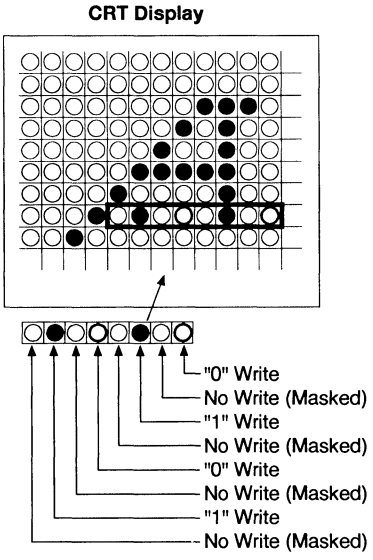


Figure 3. Corresponding bit-map

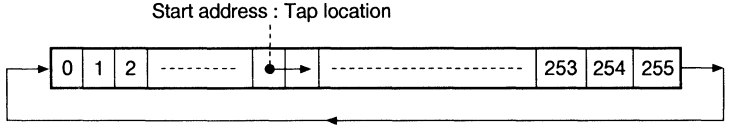
3

SAM Port Operation

The V52C8126 is provided with a 256 words by 8 bits serial access memory (SAM).

High speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read/write/pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM → SAM) has been performed. The data is shifted out of the SAM port starting at any of the 256 bits locations. The TAP location corresponds to the column address selected at the falling edge of $\overline{CAS}$ during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit, and then wraps around to the least significant bit, as illustrated below.



Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode, in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

SAM Port Operation	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	Function	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode	H	⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode	H	⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

Table 4. Truth Table for SAM Port Operation

Refresh

The SAM data registers are static flip-flop, therefore a refresh is not required.

Data Transfer Operation

The V52C8126 features the internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 4. During a normal transfer, 256 words by 8 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer).

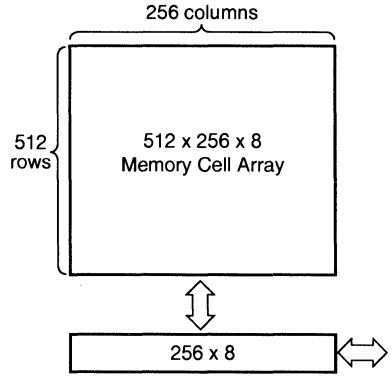


Figure 4. Data Transfer

As shown in Table 5, the V52C8126 supports three types of transfer operations: Read transfer, write transfer and pseudo write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT}/\overline{OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB}/\overline{WE}$ and $\overline{SE}$ latched at the falling edge of $\overline{RAS}$. During data transfer operations, the SAM port is switched from input to output mode (Read Transfer) or output to input mode (Write Transfer/Pseudo Write Transfer). During a data transfer cycle, the row address A_0–A_8 selects one of the 512 rows of the memory array to or from which data will be transferred, and the column address A_0–A_7 selects one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle.

At the falling edge of $\overline{RAS}$							
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	$\overline{SE}$	Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
H	L	H	•	Read Transfer	RAM → SAM	256 x 8	Input → Output
H	L	L	L	Write Transfer	SAM → RAM	256 x 8	Output → Input
H	L	L	H	Pseudo Write Transfer	—	—	Output → Input

Note: • = "H" or "L"

Table 5. Transfer Modes

Read Transfer Cycle

A read transfer cycle consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low" and $\overline{WB/WE}$ "high" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT/OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT/OE}$ and this data becomes valid on the SIO lines after the specified access time (t_{SCA}) from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 5 shows the operation block diagram for the read transfer operation.

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay (t_{TSD}) from the rising edge of $\overline{DT/OE}$, as shown in Figure 6.

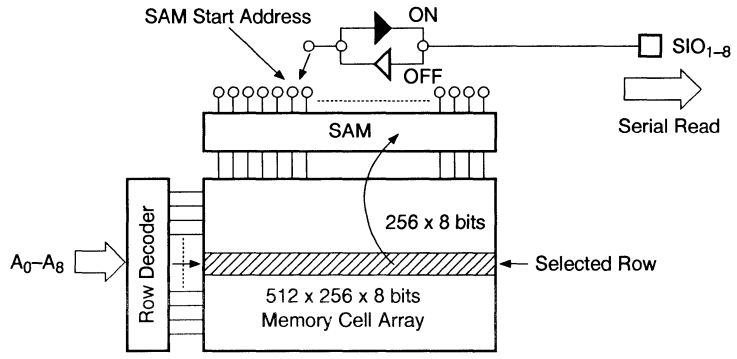


Figure 5. Block Diagram for Read Transfer Operation

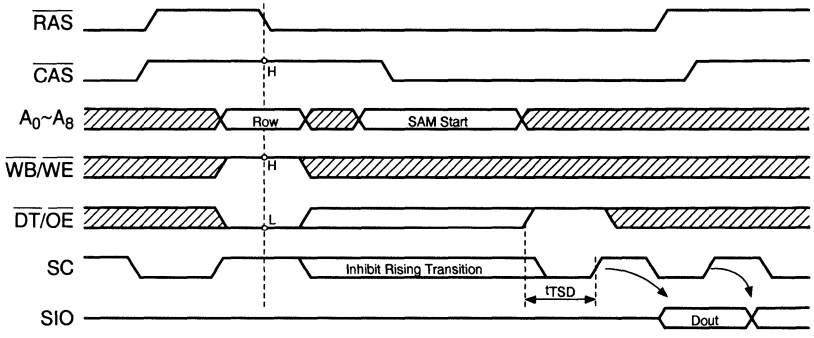


Figure 6. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT/OE}$ signal goes "high" and the serial access time (t_{SCA}) for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT/OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 7.

The timing restrictions t_{TSL}/t_{TSD} are 5ns min/15ns min.

Write Transfer Cycle

A write transfer cycle consists of loading the contents of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low", $\overline{WB/WE}$ "low" and $\overline{SE}$ "low" at the falling edge of $\overline{RAS}$. Figures 8 and 9 show the timing diagram and block diagram for write transfer operations, respectively.

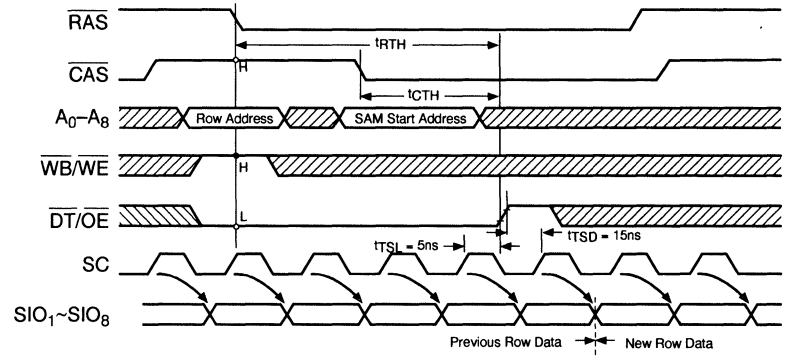


Figure 7. Real Time Read Transfer

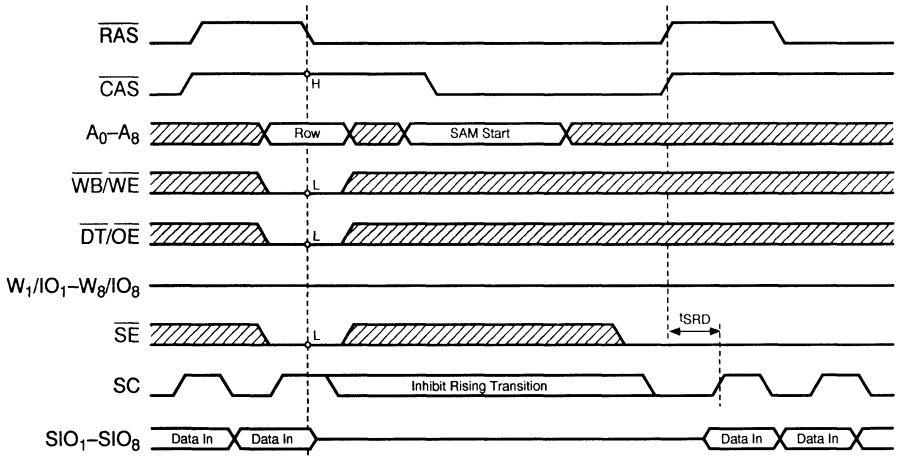


Figure 8. Write Transfer Timing

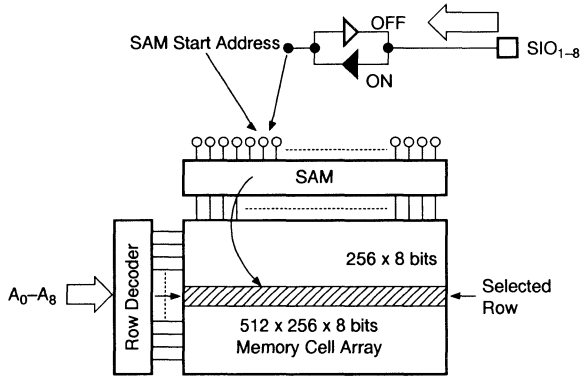


Figure 9. Block Diagram for Write Transfer Operation

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determies the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay (t_{SRD}) from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

Pseudo Write Transfer Cycle

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (a data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low", $\overline{WB/WE}$ "low" and $\overline{SE}$ "high" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

Register Operation Sequence - Example

Figure 10 illustrates an example of register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly intialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location, which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 255), and wraps around to the least significant address location. The SAM address is incremented as long as SC is clocked.

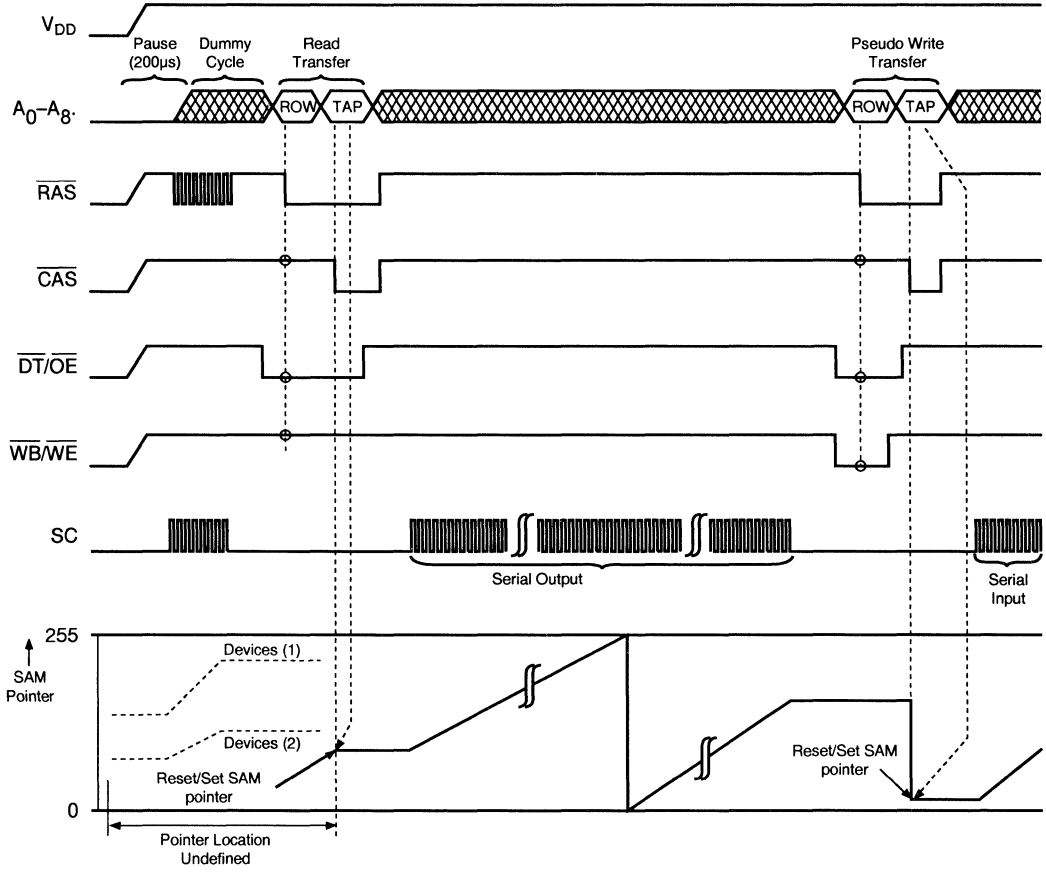
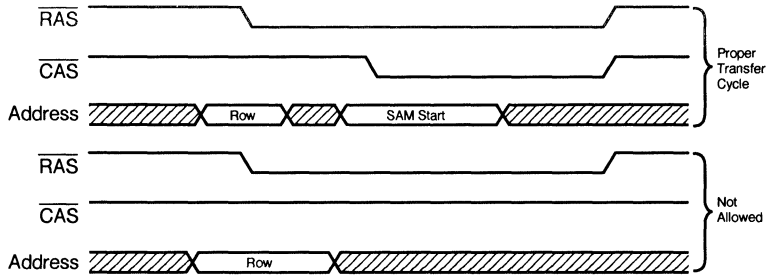


Figure 10. Example of SAM Register Operation Sequence

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for write transfers. The column address latched at the falling edge of $\overline{CAS}$ during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

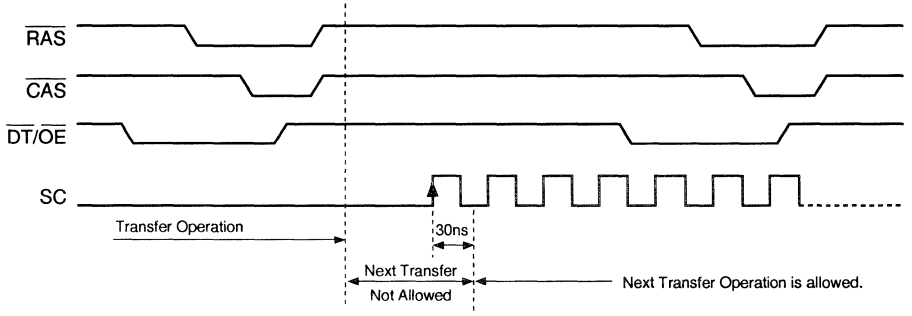
Transfer Operation Without $\overline{CAS}$

During all transfer cycles, the $\overline{CAS}$ input clock must be cycled, so that the column addresses are latched at the falling edge of $\overline{CAS}$, to set the SAM tap location. If $\overline{CAS}$ was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore, a transfer cycle with $\overline{CAS}$ held "high" is not allowed (refer to the illustration below).



Read Transfer Cycle After Read Transfer Cycle

Another read transfer may be performed following the read transfer provided that a minimum delay of 30 ns from the rising edge of the first clock SC is satisfied (refer to the illustration shown below).



Power-Up

Power must be applied to the $\overline{RAS}$ and $\overline{DT/OE}$ input signals to pull them "high" before or at the same time as the V_{DD} supply is turned on. After power-up, a pause of 200 µseconds minimum is required with $\overline{RAS}$ and $\overline{DT/OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT/OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

Initial State After Power-Up

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$ and $\overline{WB/WE}$ held "high", the internal state of the V52C8126 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 µs pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
TAP pointer	Invalid
WM1 Register	Write Enable

MULTIPORT VIDEO RAM WITH 128K X 8 DRAM AND 256 X 8 SAM

HIGH PERFORMANCE V52C8128	70	80	10
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	20 ns	25 ns	25 ns
Max. Column Address Access Time, (t_{AA})	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns
Min. Read/Write Cycle Time, (t_{RC})	140 ns	150 ns	180 ns
Max. Serial Access Time, (t_{SCA})	25 ns	25 ns	25 ns
Min. Serial Port Cycle Time, (t_{SCC})	30 ns	30 ns	30 ns

Features

- Organization
  - RAM Port: 131,072 words x 8 bits
  - SAM Port: 256 words x 8 bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write, Write-Per-Bit
  - Block Write/Flash Write
  - Color Register Load/Read
  - 512 Refresh Cycles/8 ms
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
- SAM Port
  - High Speed Serial Read/Write Capability
  - 256 Tap Locations
  - Fully Static Register
- RAM-SAM Bidirectional Transfer
  - Read/Write/Pseudo Write Transfer
  - Real Time Read Transfer
  - Split Read/Write Transfer
- Low Power Dissipation
  - RAM Port Operating Alone – 90 mA
  - SAM Port Operating Alone – 50 mA
- Low CMOS Standby Current – 7 mA
- Package
  - 40 pin 400 mil SOJ
  - 40 pin 475 mil ZIP

Description

The V52C8128 VRAM is equipped with a 131,072-words by 8-bits dynamic random access memory (RAM) port and a 256-words by 8-bits static serial access memory (SAM) port. The V52C8128 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

In addition to the conventional multiport video RAM operating modes, the V52C8128 features the block write and flash write functions on the RAM port and a split register data transfer capability on the SAM port.

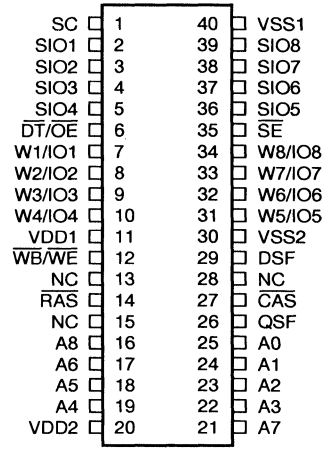
The V52C8128 is fabricated in CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

Device Usage Chart

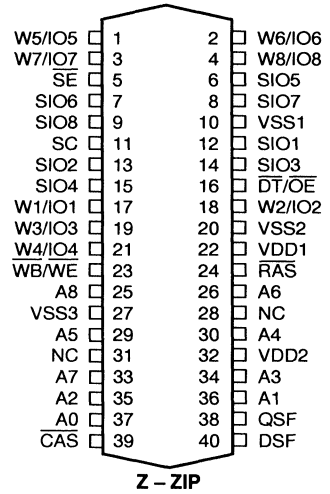
Operating Temperature Range	Package Outline		Access Time (ns)			Power	Temperature Mark
	K	Z	70	80	100	Std	
0°C–70°C	•	•	•	•	•	•	Blank

Description	Pkg.	Pin Count
SOJ	K	40
ZIP	Z	40

40 Lead Pin Configuration



K – SOJ



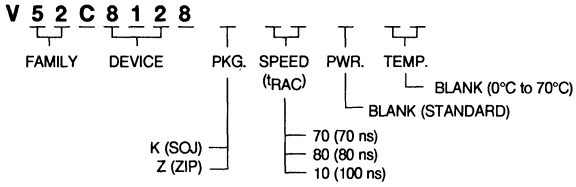
Z – ZIP

Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF
C_{OUT}	Output Capacitance (QSF)		9	pF

*Note: Capacitance is sampled and not 100% tested.



Pin Names

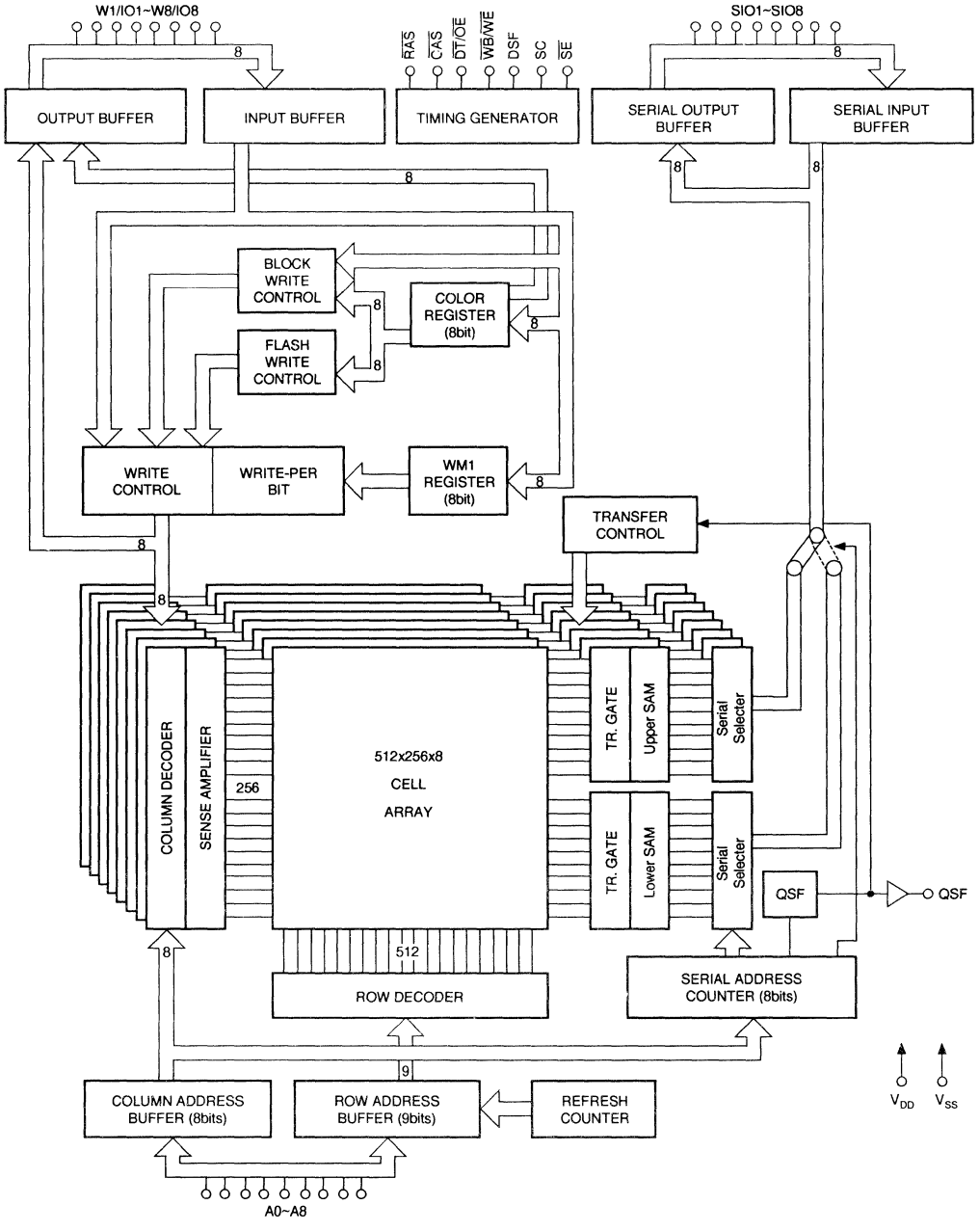
Name	Description
A0-A8	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
DT/OE	Data Transfer/Output Enable
WB/WE	Write per Bit/Write Enable
DSF	Special Function Control
W1/IO1-W8/IO8	Write Mask/Data In, Out
SC	Serial Clock
SE	Serial Enable
SIO1-SIO8	Serial Input/Output
QSF	Special Flag Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 to +7.0 V
Short Circuit Out Current ..... 50 mA
Power Dissipation ..... 1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Functional Diagram



DC and Operating Characteristics

(V_{DD} = 5V ± 10%, T_A = 0–70°C)

Symbol	Parameter (RAM Port)	SAM Port	V52C8128-70		V52C8128-80		V52C8128-10		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
I_{DD1}	Operating Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD1A}		Active		125		115		105	mA	1,2
I_{DD2}	Standby Current $\overline{RAS}$, $\overline{CAS}$ = V_{IH}	Standby		7		7		7	mA	
I_{DD2A}		Active		50		45		40	mA	1,2
I_{DD3}	$\overline{RAS}$-Only Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD3A}		Active		125		115		105	mA	1,2
I_{DD4}	Page Mode Current $\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} Min.	Standby		75		70		65	mA	1,2
I_{DD4A}		Active		125		115		105	mA	1,2
I_{DD5}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current $\overline{RAS}$ Cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD5A}		Active		125		115		105	mA	1,2
I_{DD6}	Data Transfer Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD6A}		Active		125		115		105	mA	1,2
I_{DD7}	Flash Write Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD7A}		Active		125		115		105	mA	1,2
I_{DD8}	Block Write Current $\overline{RAS}$, $\overline{CAS}$ Cycling, t_{RC} = t_{RC} Min.	Standby		90		80		70	mA	1,2
I_{DD8A}		Active		125		115		105	mA	1,2
$I_{I(L)}$	Input Leakage Current 0V ≤ V_{IN} ≤ 5.5V, all other pins not under test = 0V		-10	10	-10	10	-10	10	µA	
$I_{O(L)}$	Output Leakage Current 0V ≤ V_{OUT} ≤ 5.5V, Output Disable		-10	10	-10	10	-10	10	µA	
V_{OH}	Output "H" Level Voltage I_{OUT} = -2mA		2.4		2.4		2.4		V	
V_{OL}	Output "L" Level Voltage I_{OUT} = 2mA			0.4		0.4		0.4	V	
V_{IH}	Input High Voltage		2.4	V_{DD} + 1	2.4	V_{DD} + 1	2.4	V_{DD} + 1	V	
V_{IL}	Input Low Voltage		-1.0	0.8	-1.0	0.8	-1.0	0.8	V	

AC Electrical Characteristics *Notes: 3, 4, 5*

Symbol	Parameter	V52C8128-70		V52C8128-80		V52C8128-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	140		150		180		ns	
t_{RMW}	Read-Modify-Write Cycle Time	195		195		235		ns	
t_{PC}	Fast Page Mode Cycle Time	45		50		55		ns	
t_{PRMW}	Fast Page Mode Read-Modify-Write Cycle Time	90		90		100		ns	
t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	6, 12
t_{AA}	Access Time from Column Address		35		40		50	ns	6, 12
t_{CAC}	Access Time from $\overline{CAS}$		20		25		25	ns	6, 13
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		40		45		50	ns	6, 13
t_{OFF}	Output Buffer Turn-Off Delay	0	20	0	20	0	20	ns	8
t_T	Transition Time (Rise and Fall)	3	35	3	35	3	35	ns	5
t_{RP}	$\overline{RAS}$ Precharge Time	60		60		70		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	100	10K	ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode only)	70	100K	80	100K	100	100K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20		25		25		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	25	10K	25	10K	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	55	20	75	ns	12
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	12
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40		55		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page Mode)	10		10		10		ns	
t_{ASR}	Row Address Setup Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		10		ns	
t_{ASC}	Column Address Setup Time	0		0		0		ns	
t_{CAH}	Column Address Hold Time	15		15		15		ns	
t_{AR}	Column Address Hold Time referenced to $\overline{RAS}$	55		55		70		ns	
t_{RCS}	Read Command Setup Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	9
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		0		ns	9
t_{WCH}	Write Command Hold Time	15		15		15		ns	
t_{WCR}	Write Command Hold Time referenced to $\overline{RAS}$	55		55		70		ns	

3

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	V52C8128-70		V52C8128-80		V52C8128-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WP}	Write Command Pulse Width	15		15		15		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		ns	
t_{DS}	Data Setup Time	0		0		0		ns	10
t_{DH}	Data Hold Time	15		15		15		ns	10
t_{DHR}	Data Hold Time referenced to $\overline{RAS}$	55		55		70		ns	
t_{WCS}	Write Command Setup Time	0		0		0		ns	11
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	100		100		130		ns	11
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	65		65		80		ns	11
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	45		45		55		ns	11
t_{DZC}	Data to $\overline{CAS}$ Delay Time	0		0		0		ns	
t_{DZO}	Data to $\overline{OE}$ Delay Time	0		0		0		ns	
t_{OEA}	Access Time from $\overline{OE}$		20		20		25	ns	6
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	0	10	0	10	0	20	ns	8
t_{OED}	$\overline{OE}$ to Data Delay Time	10		10		20		ns	
t_{OEH}	$\overline{OE}$ Command Hold Time	10		10		20		ns	
t_{ROH}	$\overline{RAS}$ Hold Time referenced to $\overline{OE}$	15		15		15		ns	
t_{CSR}	$\overline{CAS}$ Setup Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$-before-$\overline{RAS}$ Cycle	10		10		10		ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	0		0		0		ns	
t_{REF}	Refresh Period		8		8		8	ms	
t_{WSR}	$\overline{WB}$ Setup Time	0		0		0		ns	
t_{RWH}	$\overline{WB}$ Hold Time	15		15		15		ns	
t_{FSR}	DSF Setup Time referenced to $\overline{RAS}$	0		0		0		ns	
t_{RFH}	DSF Hold Time referenced to $\overline{RAS}$ (1)	15		15		15		ns	
t_{FHR}	DSF Hold Time referenced to $\overline{RAS}$ (2)	55		55		70		ns	
t_{FSC}	DSF Setup Time referenced to $\overline{CAS}$	0		0		0		ns	
t_{CFH}	DSF Hold Time referenced to $\overline{CAS}$	15		15		15		ns	
t_{MS}	Write-Per-Bit Mask Data Setup Time	0		0		0		ns	
t_{MH}	Write-Per-Bit Mask Data Hold Time	15		15		15		ns	
t_{THS}	$\overline{DT}$ High Setup Time	0		0		0		ns	
t_{THH}	$\overline{DT}$ High Hold Time	15		15		15		ns	
t_{TLS}	$\overline{DT}$ Low Setup Time	0		0		0		ns	

AC Electrical Characteristics (Cont'd)

Symbol	Parameter	V52C8128-70		V52C8128-80		V52C8128-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{TLH}	$\overline{DT}$ Low Hold Time	15	10K	15	10K	15	10K	ns	
t_{RTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{RAS}$ (Real Time Read Transfer)	60	10K	65	10K	80	10K	ns	
t_{ATH}	$\overline{DT}$ Low Hold Time referenced to Column Address (Real Time Read Transfer)	25		30		30		ns	
t_{CTH}	$\overline{DT}$ Low Hold Time referenced to $\overline{CAS}$ (Real Time Read Transfer)	20		25		25		ns	
t_{ESR}	$\overline{SE}$ Setup Time referenced to $\overline{RAS}$	0		0		0		ns	
t_{REH}	$\overline{SE}$ Hold Time referenced to $\overline{RAS}$	15		15		15		ns	
t_{TRP}	$\overline{DT}$ to $\overline{RAS}$ Precharge Time	60		60		70		ns	
t_{TP}	$\overline{DT}$ Precharge Time	20		20		30		ns	
t_{RSD}	$\overline{RAS}$ to First SC Delay Time (Read Transfer)	70		80		100		ns	
t_{ASD}	Column Address to First SC Delay Time (Read Transfer)	45		45		50		ns	
t_{CSD}	$\overline{CAS}$ to First SC Delay Time (Read Transfer)	20		25		25		ns	
t_{TSL}	Last SC to $\overline{DT}$ Lead Time (Real Time Read Transfer)	5		5		5		ns	
t_{TSD}	$\overline{DT}$ to First SC Delay Time (Read Transfer)	15		15		15		ns	
t_{SRS}	Last SC to $\overline{RAS}$ Setup Time (Serial Input)	25		25		30		ns	
t_{SRD}	$\overline{RAS}$ to First SC Delay Time (Serial Input)	20		20		25		ns	
t_{SDD}	$\overline{RAS}$ to Serial Input Delay Time	40		40		50		ns	
t_{SDZ}	Serial Output Buffer Turn-Off Delay from $\overline{RAS}$ (Pseudo Write Transfer)	10	40	10	40	10	50	ns	8
t_{SCC}	SC Cycle Time	30		30		30		ns	
t_{SC}	SC Pulse Width (SC High Time)	10		10		10		ns	
t_{SCP}	SC Precharge Time (SC Low Time)	10		10		10		ns	
t_{SCA}	Access Time from SC		25		25		25	ns	7
t_{SOH}	Serial Output Hold Time from SC	5		5		5		ns	
t_{SDS}	Serial Input Setup Time	0		0		0		ns	
t_{SDH}	Serial Input Hold Time	15		15		15		ns	
t_{SEA}	Access Time from $\overline{SE}$		25		25		25	ns	7
t_{SE}	$\overline{SE}$ Pulse Width	25		25		25		ns	
t_{SEP}	$\overline{SE}$ Precharge Time	25		25		25		ns	
t_{SEZ}	Serial Output Buffer Turn-Off Delay from $\overline{SE}$	0	20	0	20	0	20	ns	8
t_{SZE}	Serial Input to $\overline{SE}$ Delay Time	0		0		0		ns	

AC Electrical Characteristics (Cont'd)

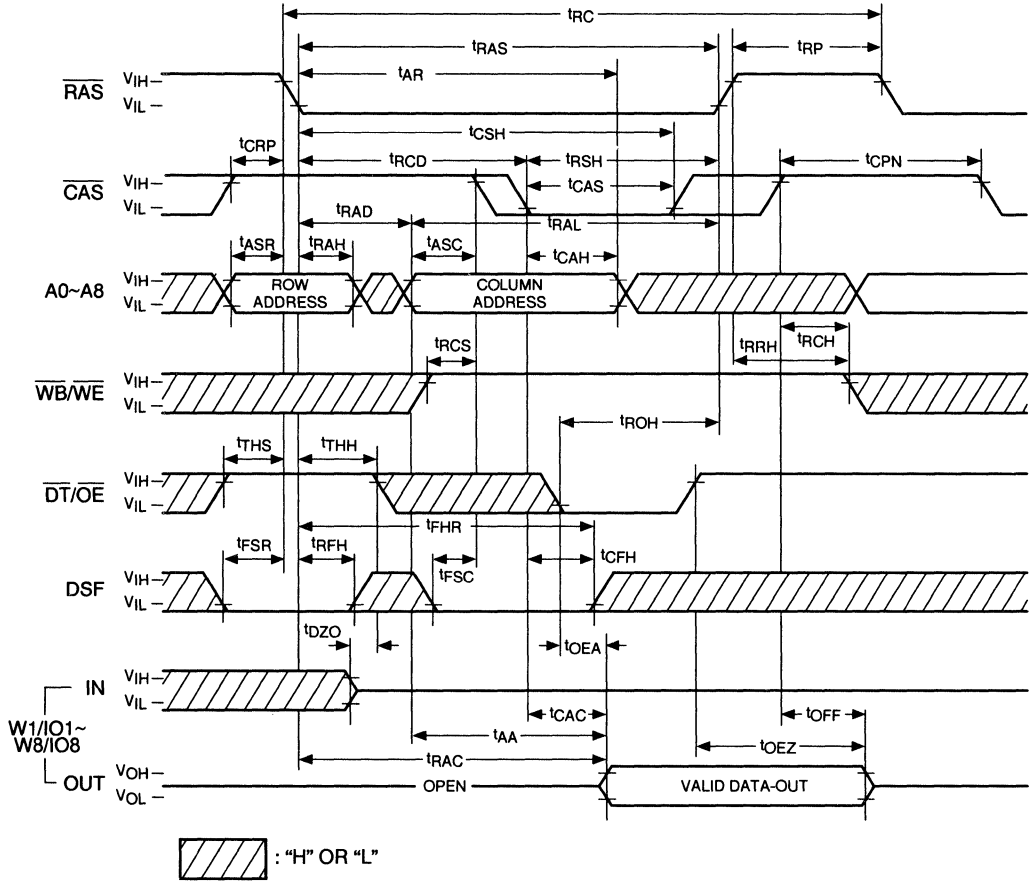
Symbol	Parameter	V52C8128-70		V52C8128-80		V52C8128-10		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{SZS}	Serial Input to First SC Delay Time	0		0		0		ns	
t_{SWS}	Serial Write Enable Setup Time	5		5		5		ns	
t_{SWH}	Serial Write Enable Hold Time	15		15		15		ns	
t_{SWIS}	Serial Write Disable Setup Time	5		5		5		ns	
t_{SWIH}	Serial Write Disable Hold Time	15		15		15		ns	
t_{STS}	Split Transfer Setup Time	25		30		30		ns	
t_{STH}	Split Transfer Hold Time	25		30		30		ns	
t_{SQD}	SC–QSF Delay Time		25		25		25	ns	
t_{TQD}	$\overline{DT}$–QSF Delay Time		25		25		25	ns	
t_{CQD}	$\overline{CAS}$–QSF Delay Time		35		35		35	ns	
t_{RQD}	$\overline{RAS}$–QSF Delay Time		75		75		85	ns	

Notes

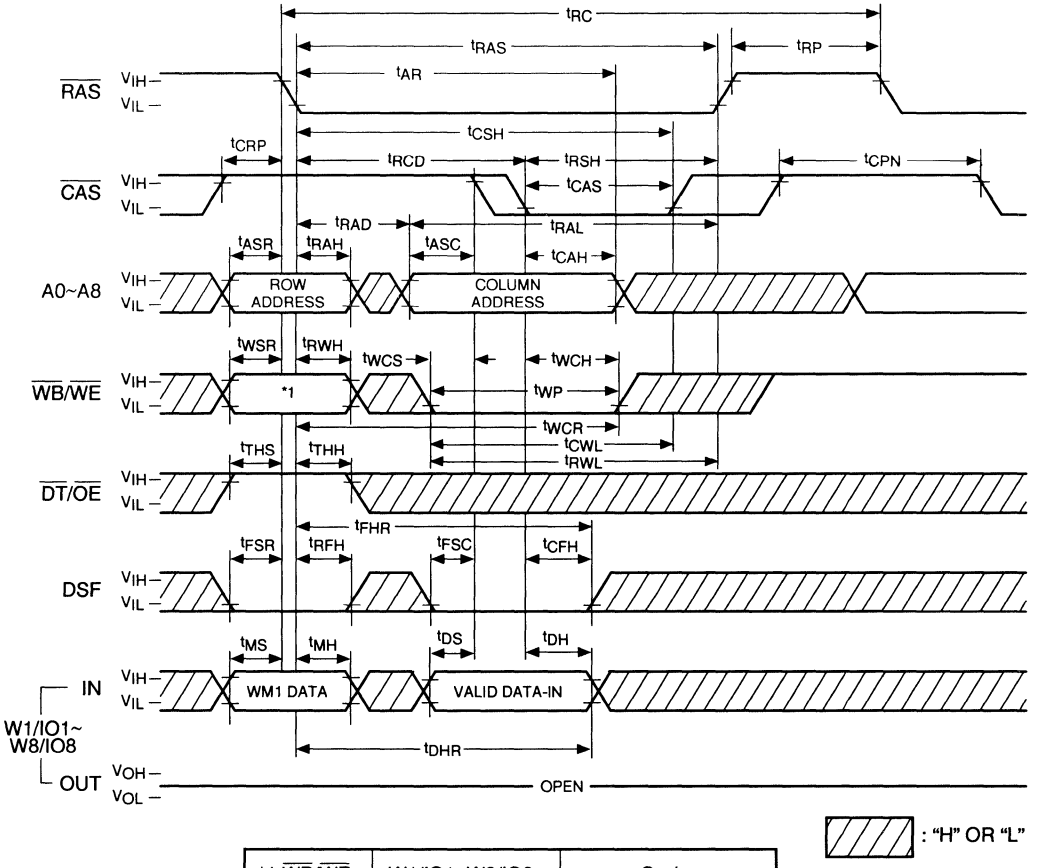
1. These parameters depend on cycle rate.
2. These parameters depend on output loading. Specified values are obtained with the output open.
3. An initial pause of 200µs is required after power-up, followed by any 8 $\overline{RAS}$ cycles ($\overline{DT}/\overline{OE}$ "high") and any 8 SC cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles instead of 8 $\overline{RAS}$ cycles are required.
4. AC measurements assume t_T = 5 ns.
5. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
6. RAM port outputs are measured with a load equivalent to 1 TTL load and 100 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
7. SAM port outputs are measured with a load equivalent to 1 TTL load and 30 pF. D_{OUT} reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
8. t_{OFF} (max.), t_{OEZ} (max.), t_{SDZ} (max.) and t_{SEZ} (max.) define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referenced to $\overline{CAS}$ leading edge of early write cycles and to $\overline{WB}/\overline{WE}$ leading edge in $\overline{OE}$-controlled write cycles and read-modify-write cycles.
11. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min.), $t_{CWD} \geq t_{CWD}$ (min.) and $t_{AWD} \geq t_{AWD}$ (min.), the cycle is a read-modify-write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
12. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled by t_{CAC}.
13. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.

TIMING WAVEFORMS

Read Cycle



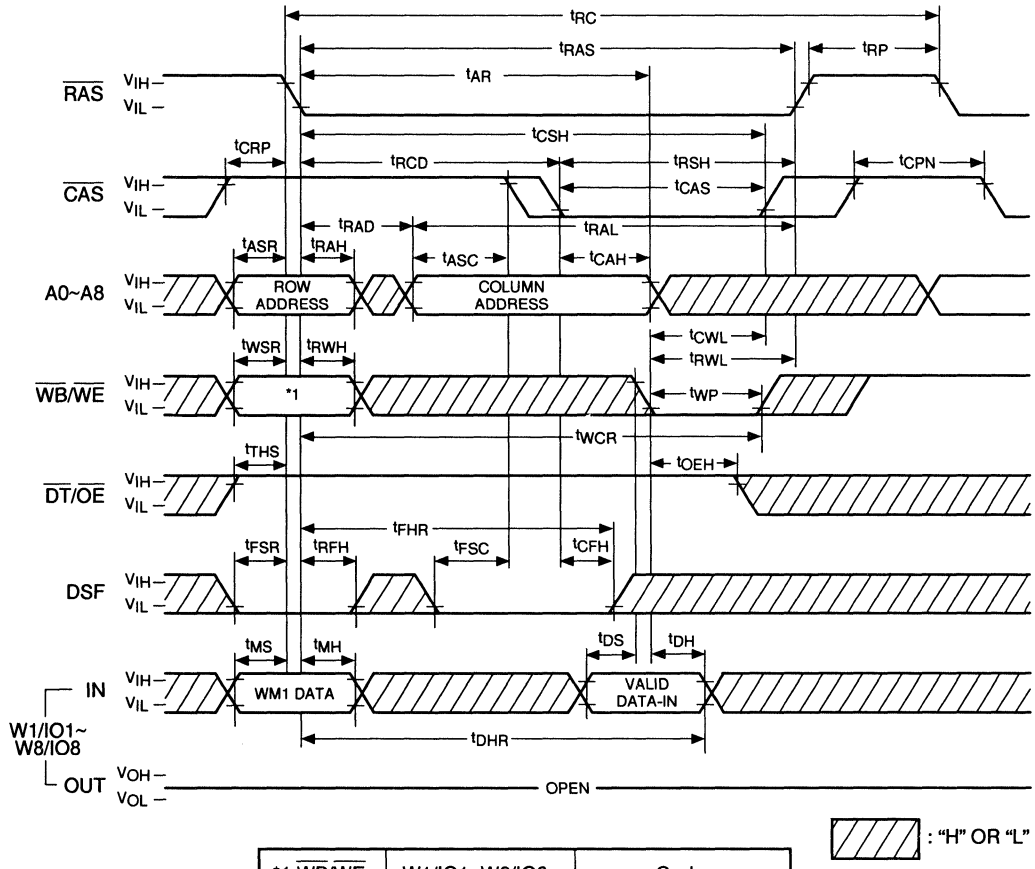
Write Cycle (Early Write)



*1 WB/WE	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

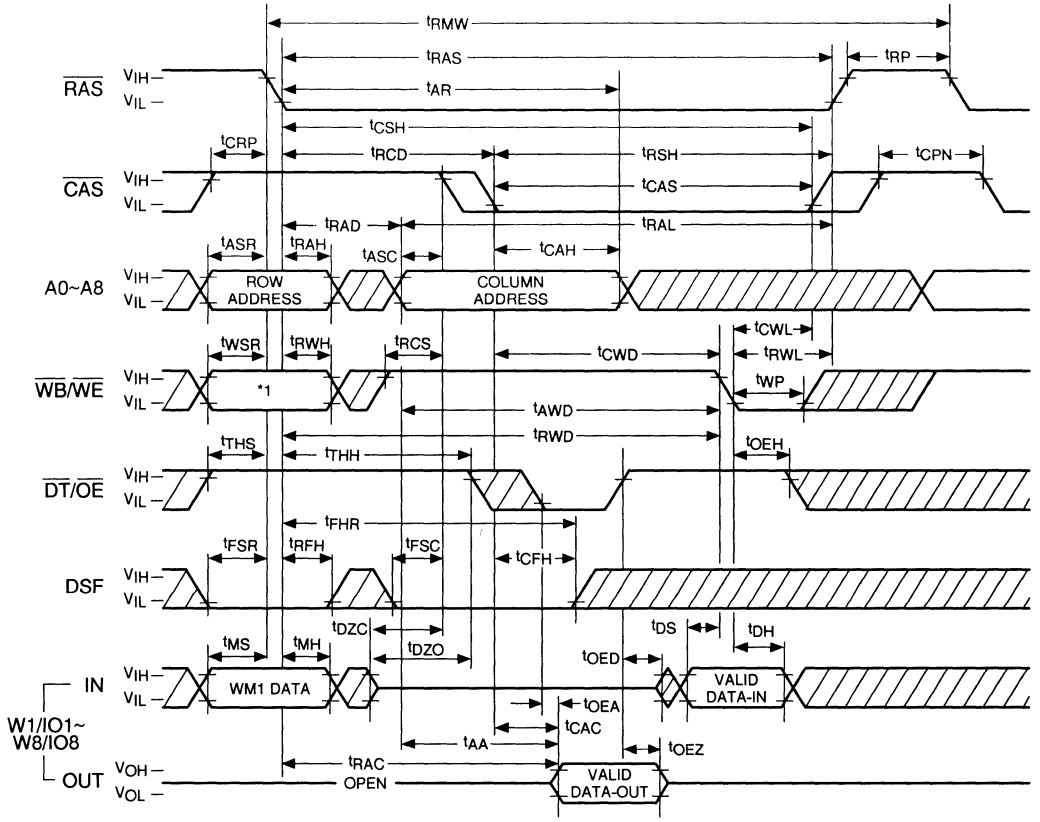
Write Cycle ($\overline{OE}$ Controlled Write)



*1 $\overline{WB/WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

Read-Modify-Write Cycle

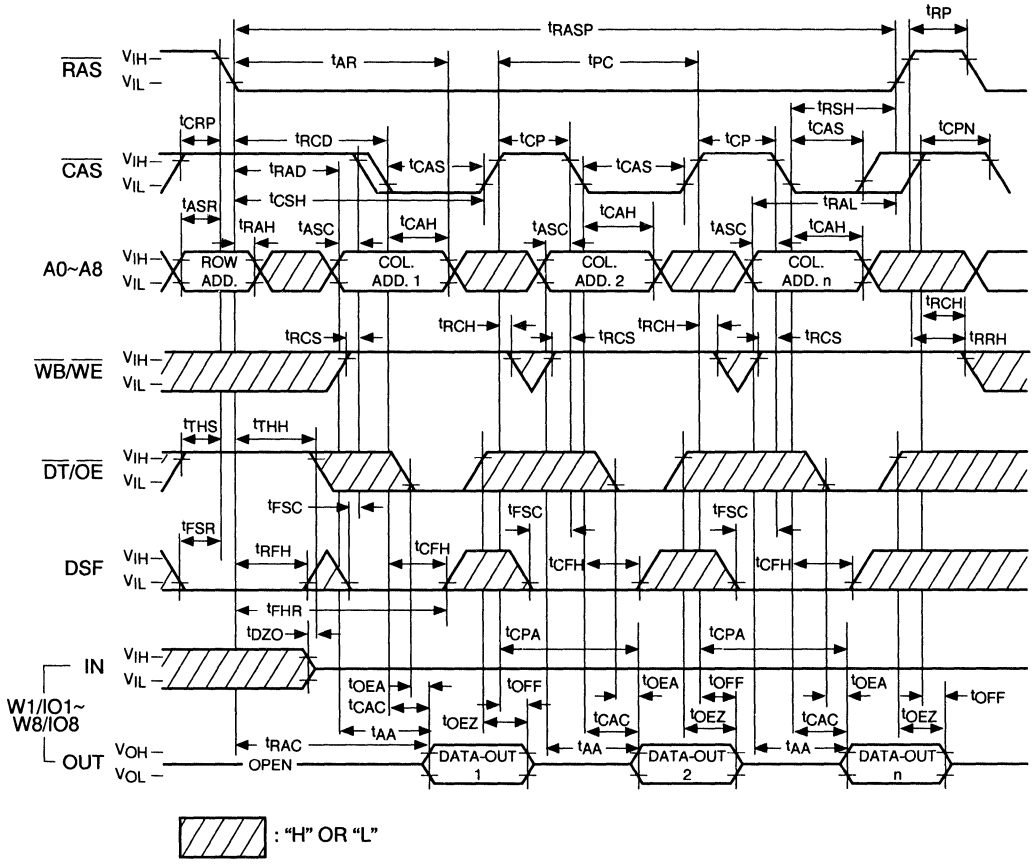


*1 WB/WE	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

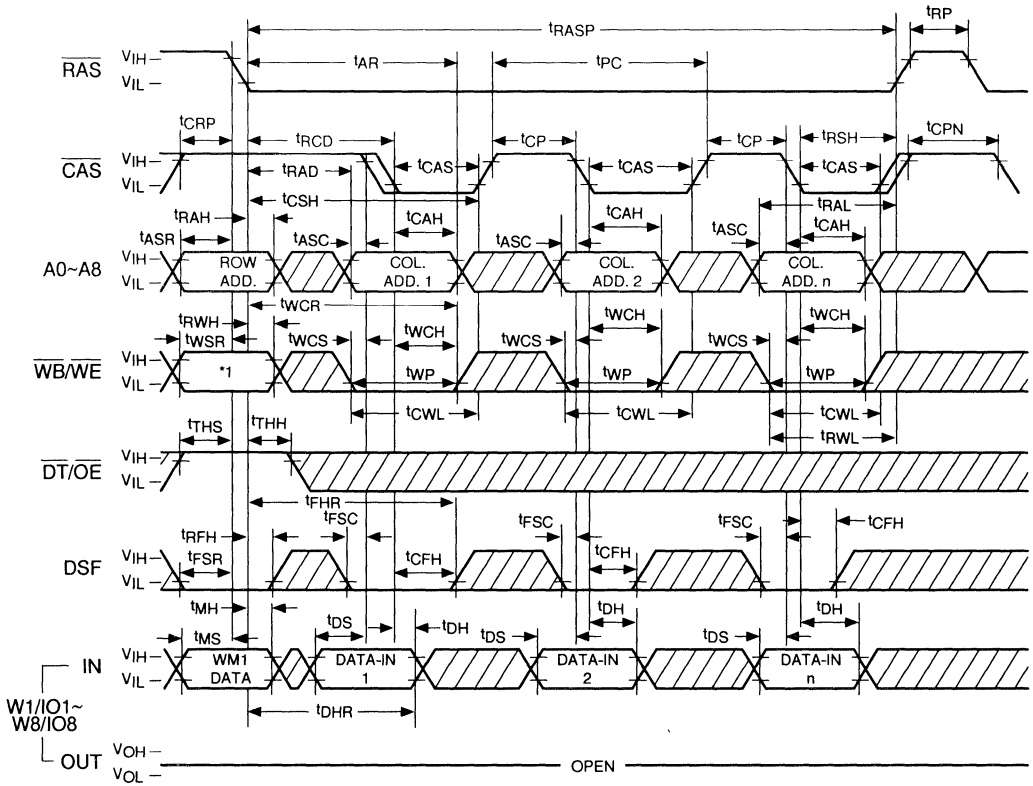
WM1 data: 0: Write Disable
1: Write Enable

: "H" OR "L"

Fast Page Mode Read Cycle



Fast Page Mode Write Cycle (Early Write)

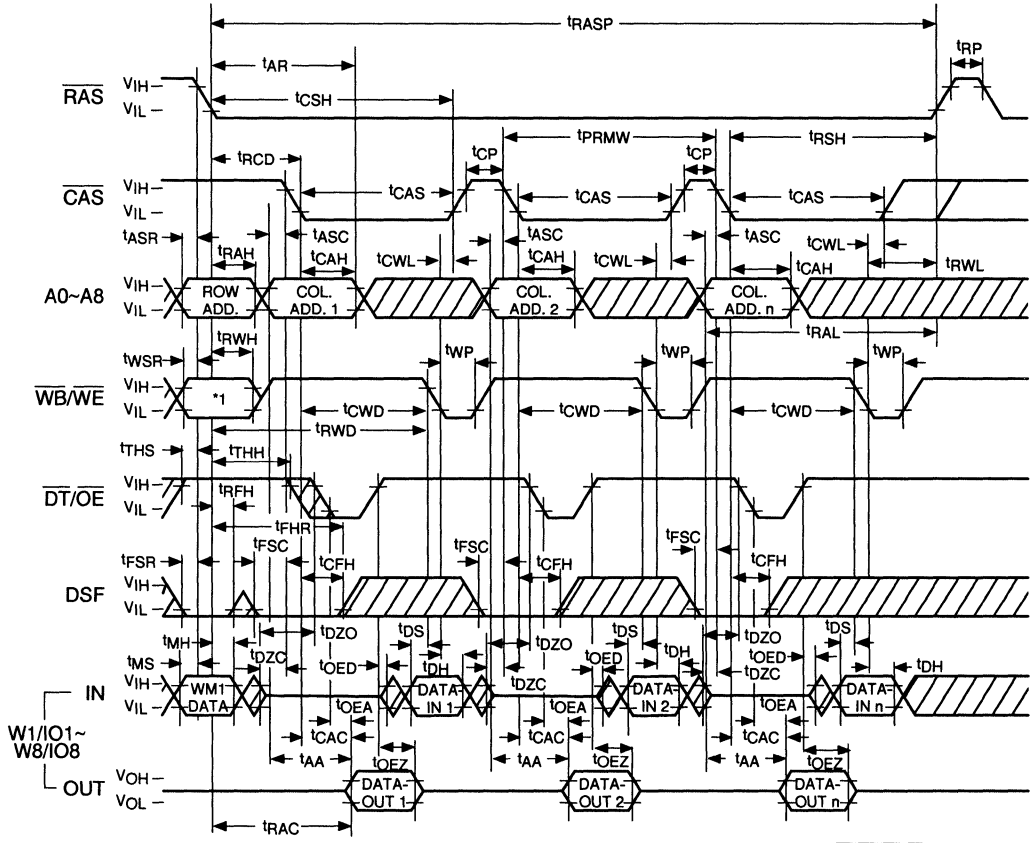


*1 $\overline{WB}/\overline{WE}$	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

: "H" OR "L"

Fast Page Mode Read-Modify-Write Cycle

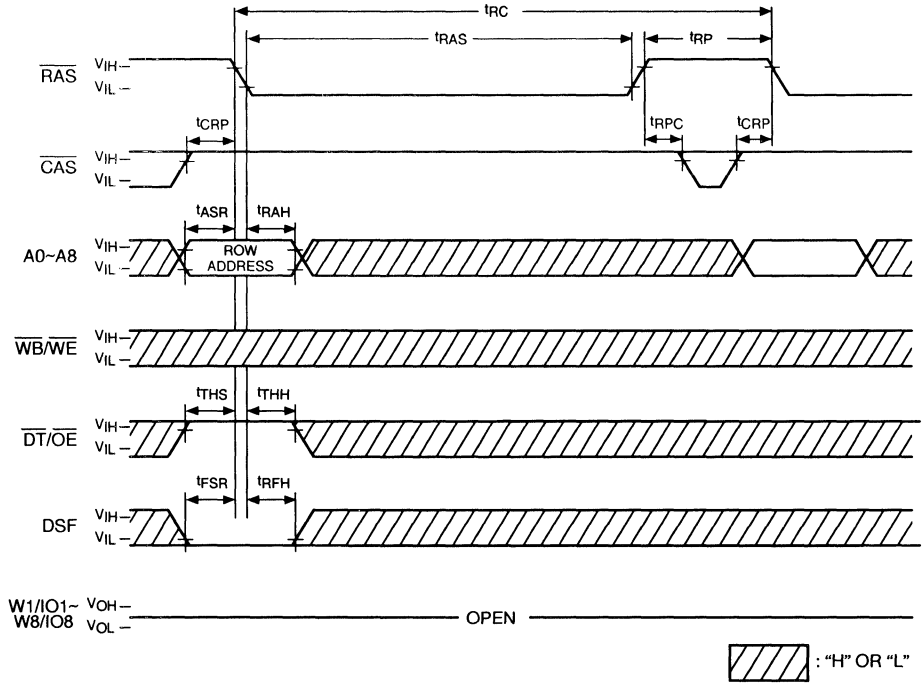


: "H" OR "L"

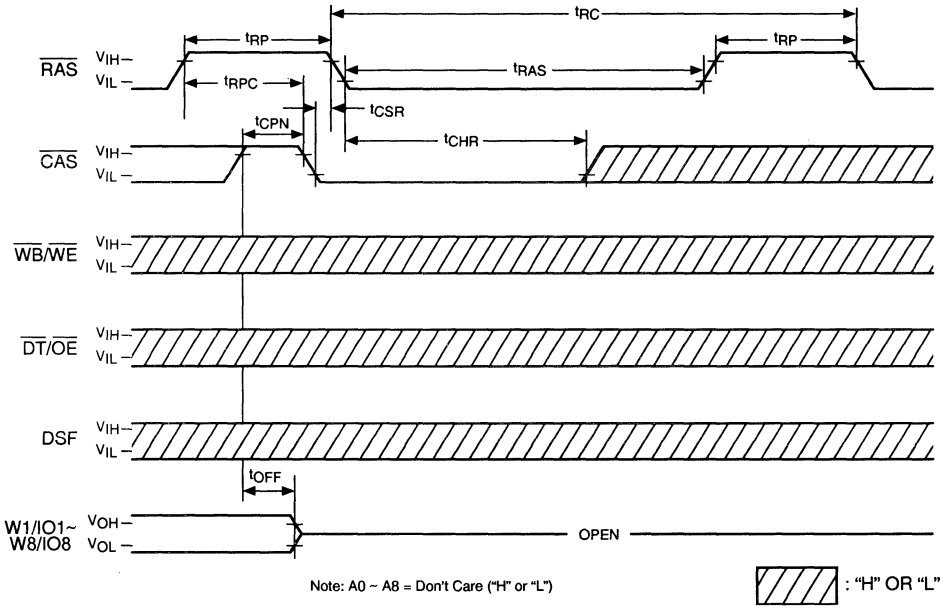
*1 WB/WE	W1/IO1~W8/IO8	Cycle
0	WM1 data	Write per bit
1	Don't Care	Normal Write

WM1 data: 0: Write Disable
1: Write Enable

$\overline{RAS}$ Only Refresh Cycle

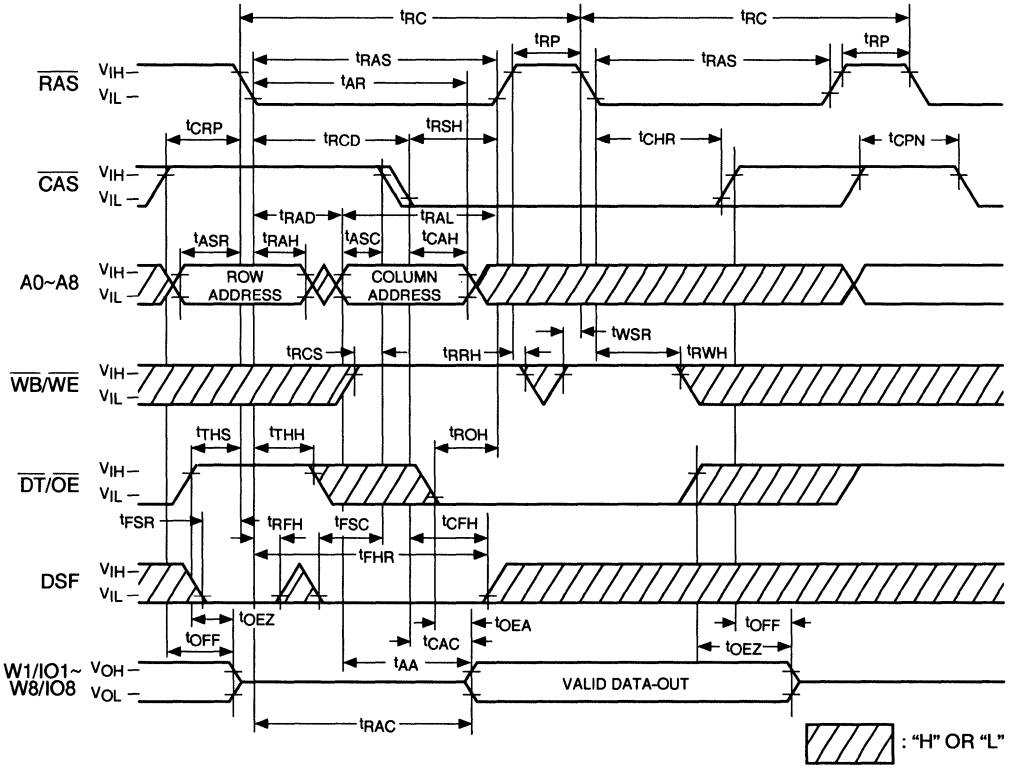


$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle

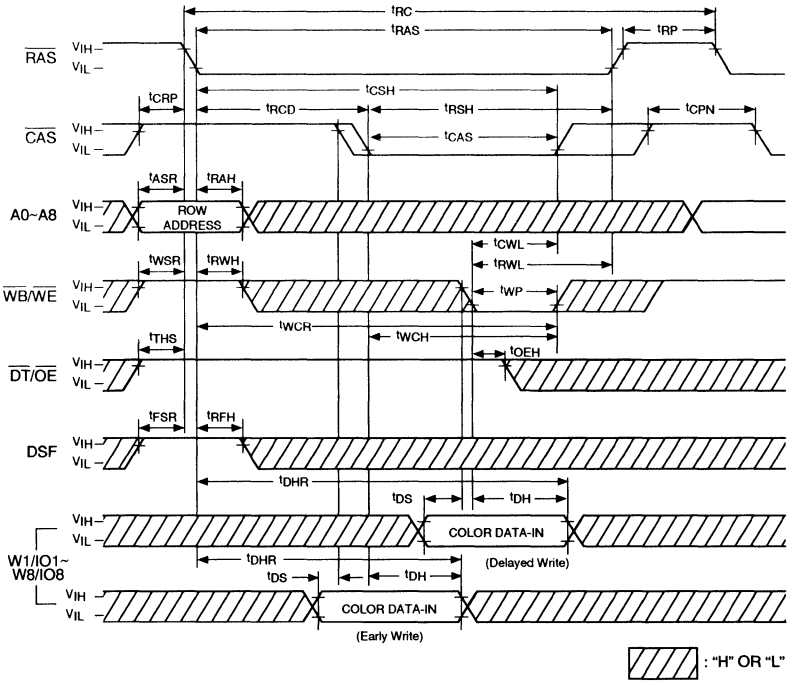


Note: A0 ~ A8 = Don't Care ("H" or "L")

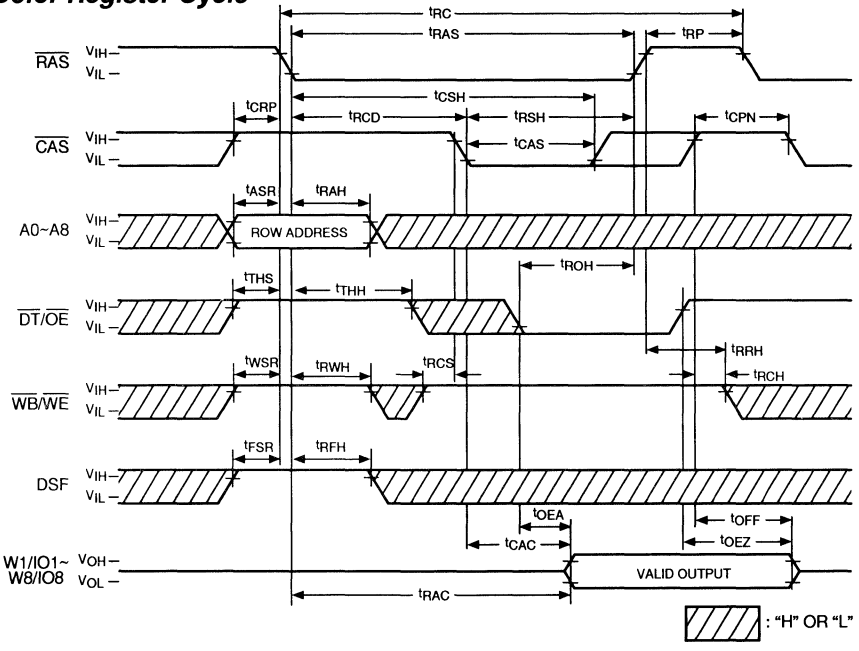
Hidden Refresh Cycle



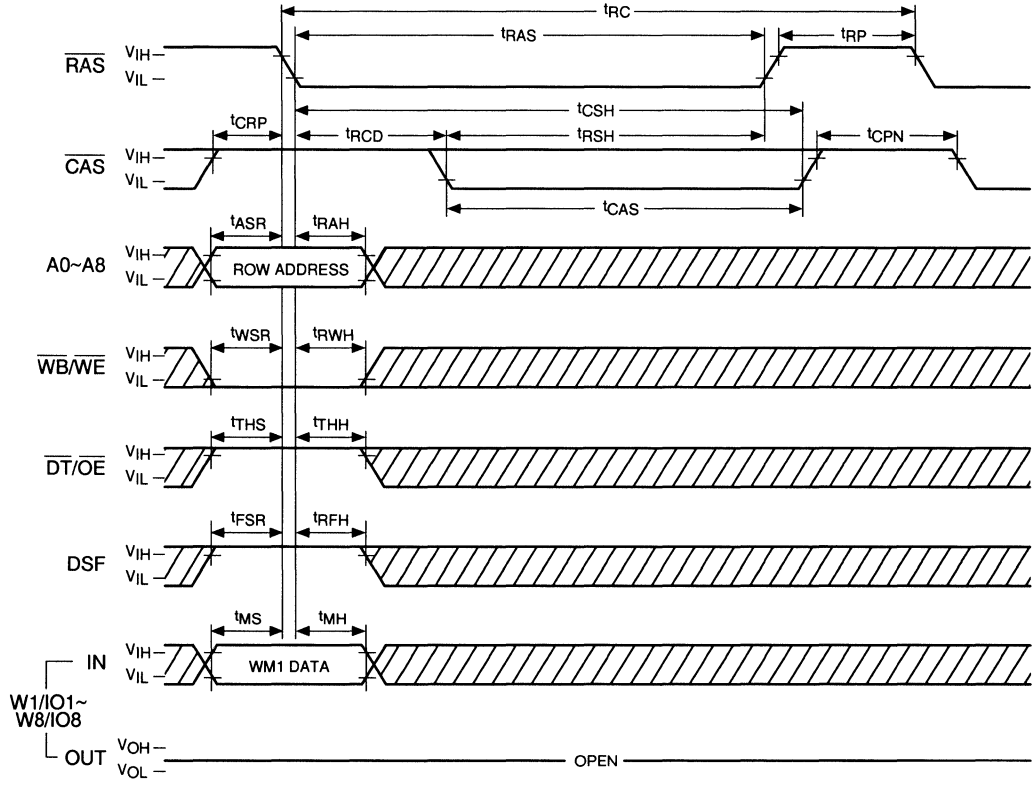
Load Color Register Cycle



Read Color Register Cycle

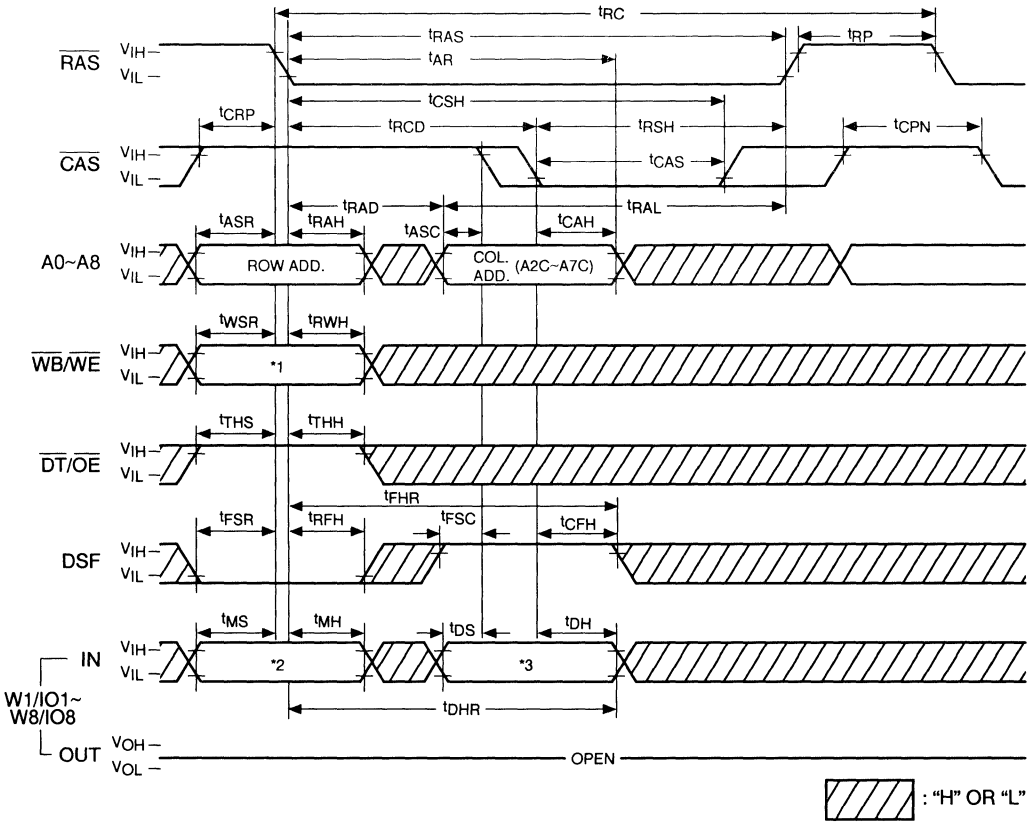


Flash Write Cycle



WM1 DATA	Cycle
0	Flash Write Disable
1	Flash Write Enable

Block Write Cycle



*1 $\overline{WB}/\overline{WE}$	*2 W1/IO1~W8/IO8	Cycle
0	WM1 data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

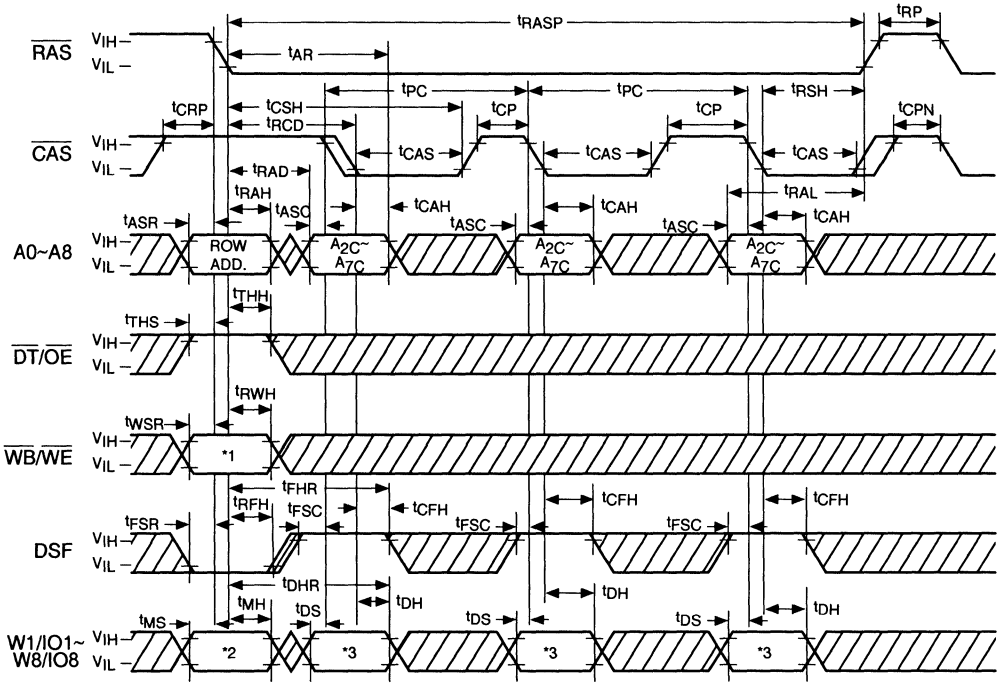
WM1 data: 0: Write Disable
1: Write Enable

*3) Column Select

W1/IO1 — Column 0 (A_{1C} = 0, A_{0C} = 0)
W2/IO2 — Column 1 (A_{1C} = 0, A_{0C} = 1)
W3/IO3 — Column 2 (A_{1C} = 1, A_{0C} = 0)
W4/IO4 — Column 3 (A_{1C} = 1, A_{0C} = 1)

Wn/IOn
= 0 : Disable
= 1 : Enable

Page Mode Block Write Cycle



*1 WB/WE	*2 W1/IO1~W8/IO8	Cycle
0	WM1 data	Masked Block Write
1	Don't Care	Block Write (Non Mask)

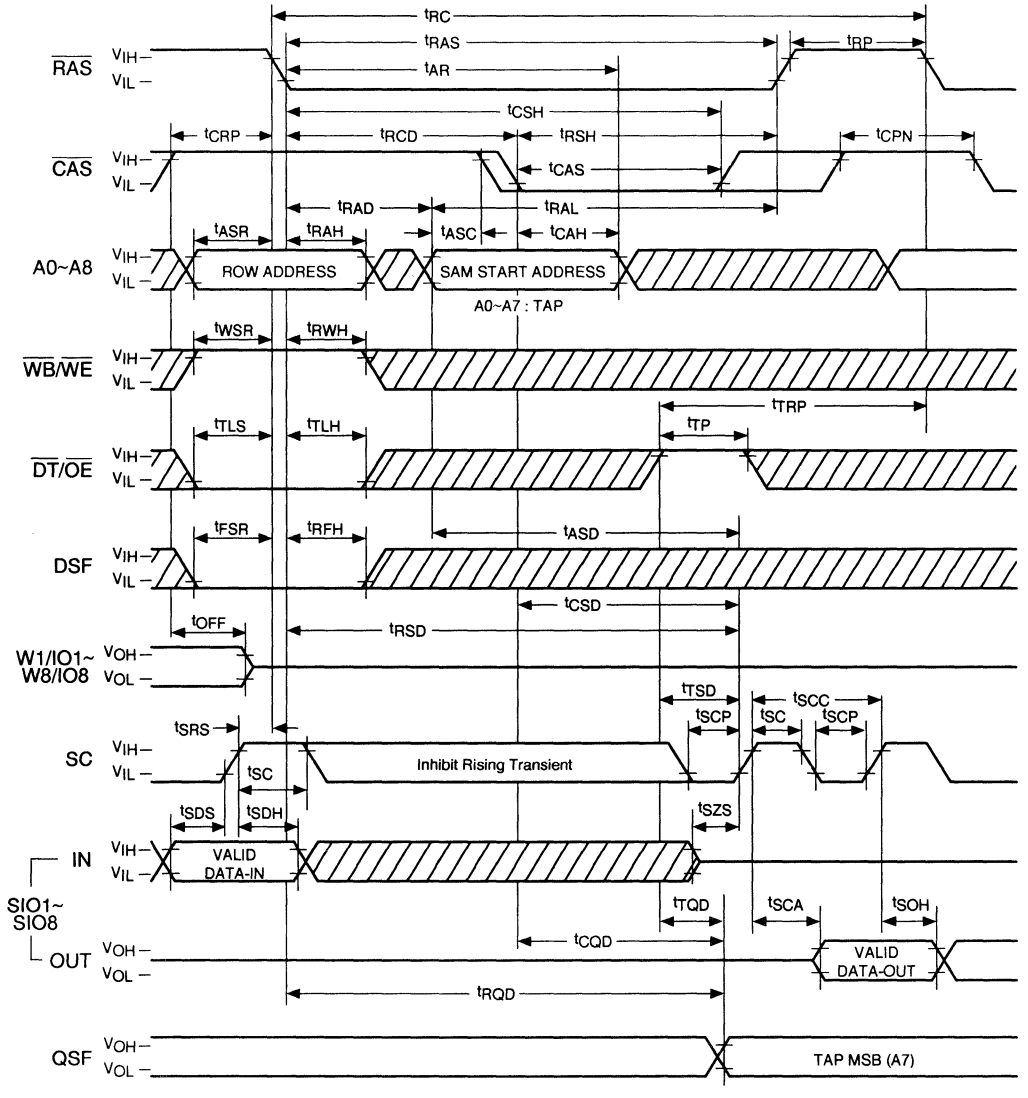
WM1 data: 0: Write Disable
1: Write Enable

*3) Column Select

W1/IO1 — Column 0 (A_{1C} = 0, A_{0C} = 0)
W2/IO2 — Column 1 (A_{1C} = 0, A_{0C} = 1)
W3/IO3 — Column 2 (A_{1C} = 1, A_{0C} = 0)
W4/IO4 — Column 3 (A_{1C} = 1, A_{0C} = 1)

Wn/IOn
= 0 : Disable
= 1 : Enable

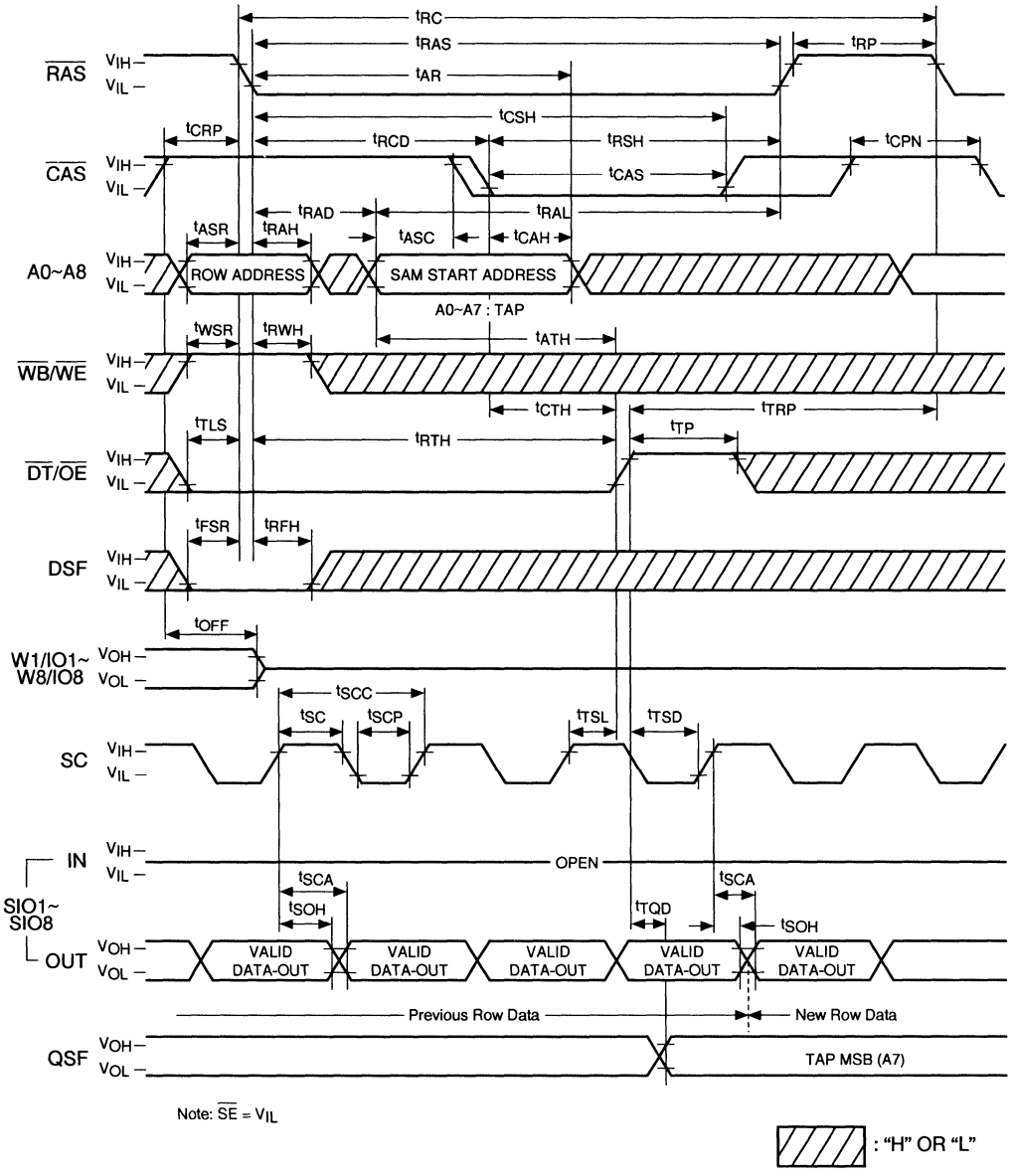
Read Transfer Cycle (Previous Transfer is Write Transfer Cycle)



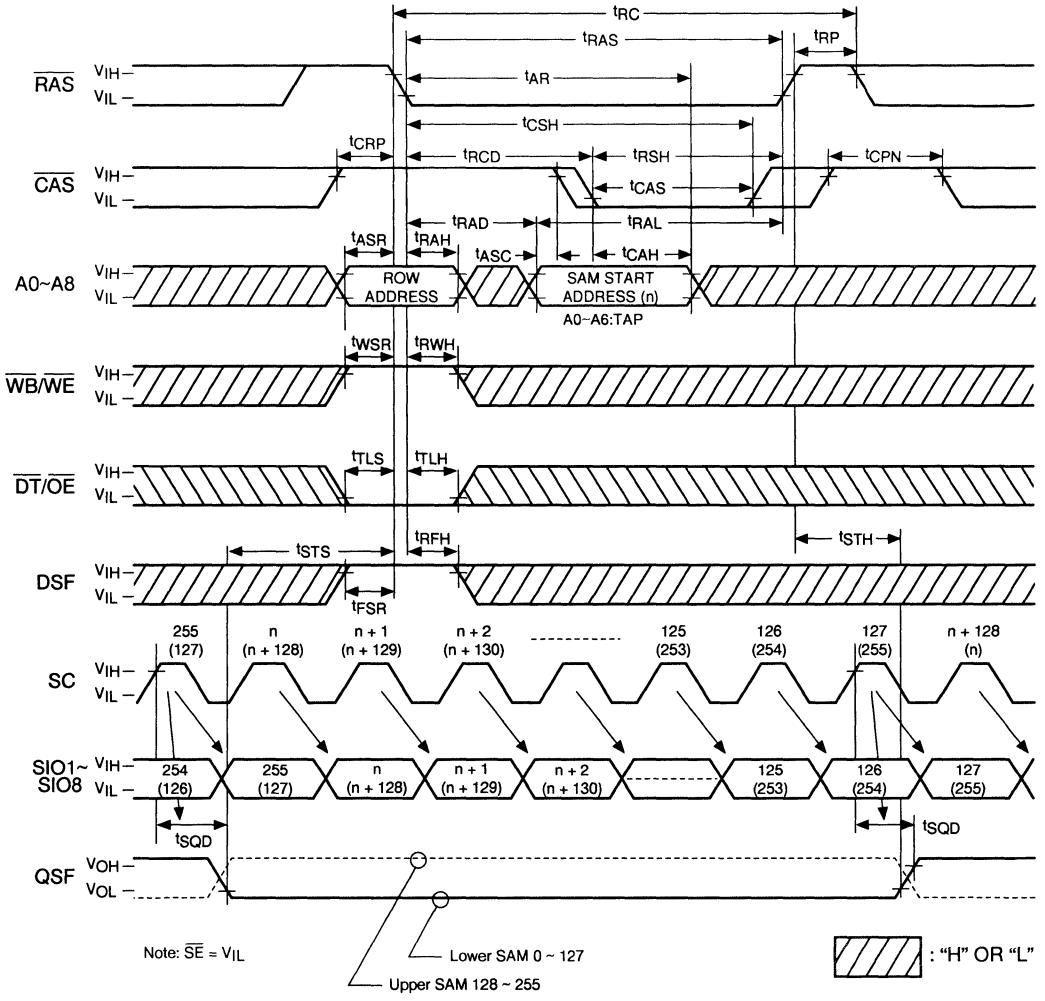
Note: $\overline{SE}$ = V_{IL}

: "H" OR "L"

Real Time Read Transfer Cycle

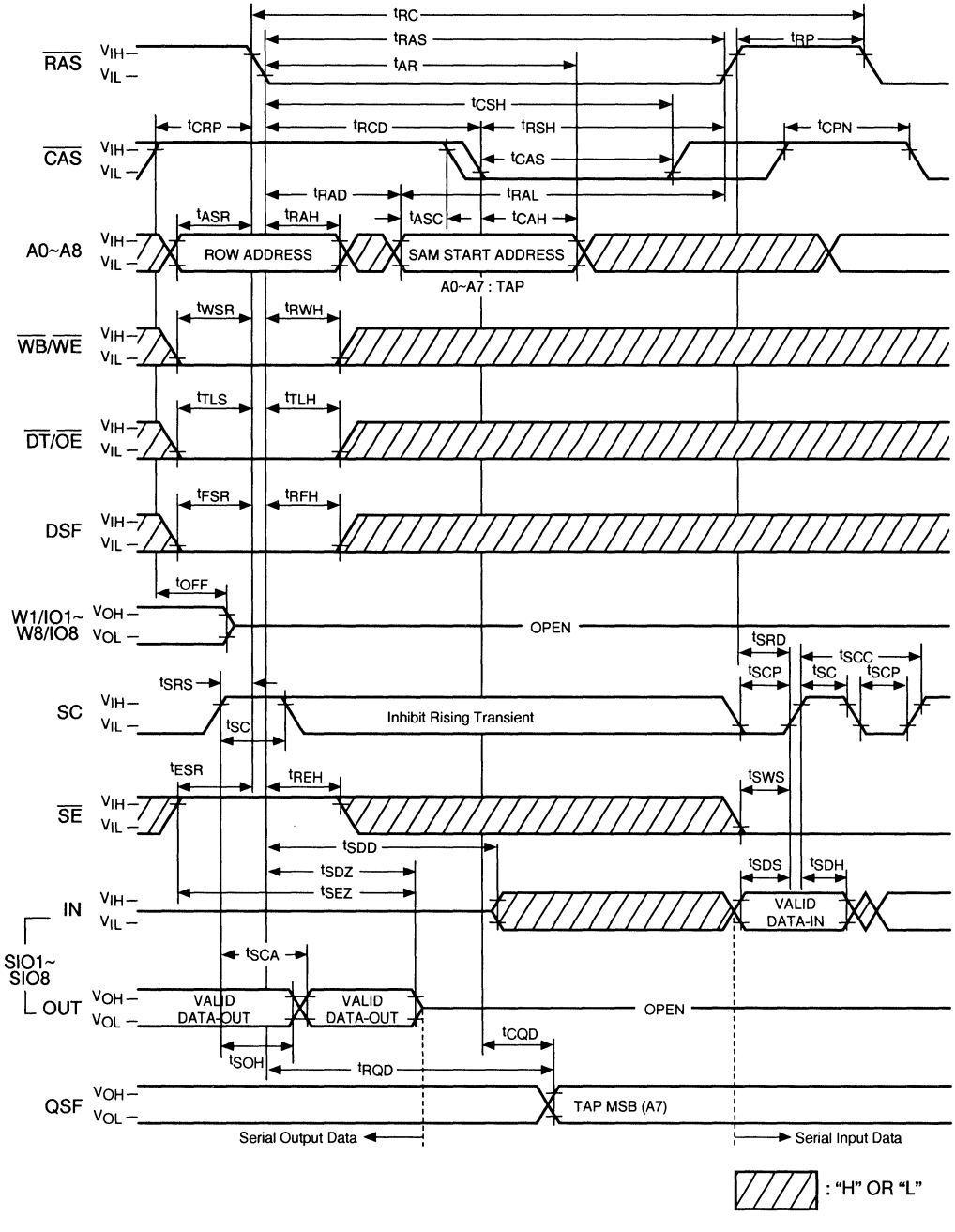


Split Read Transfer Cycle

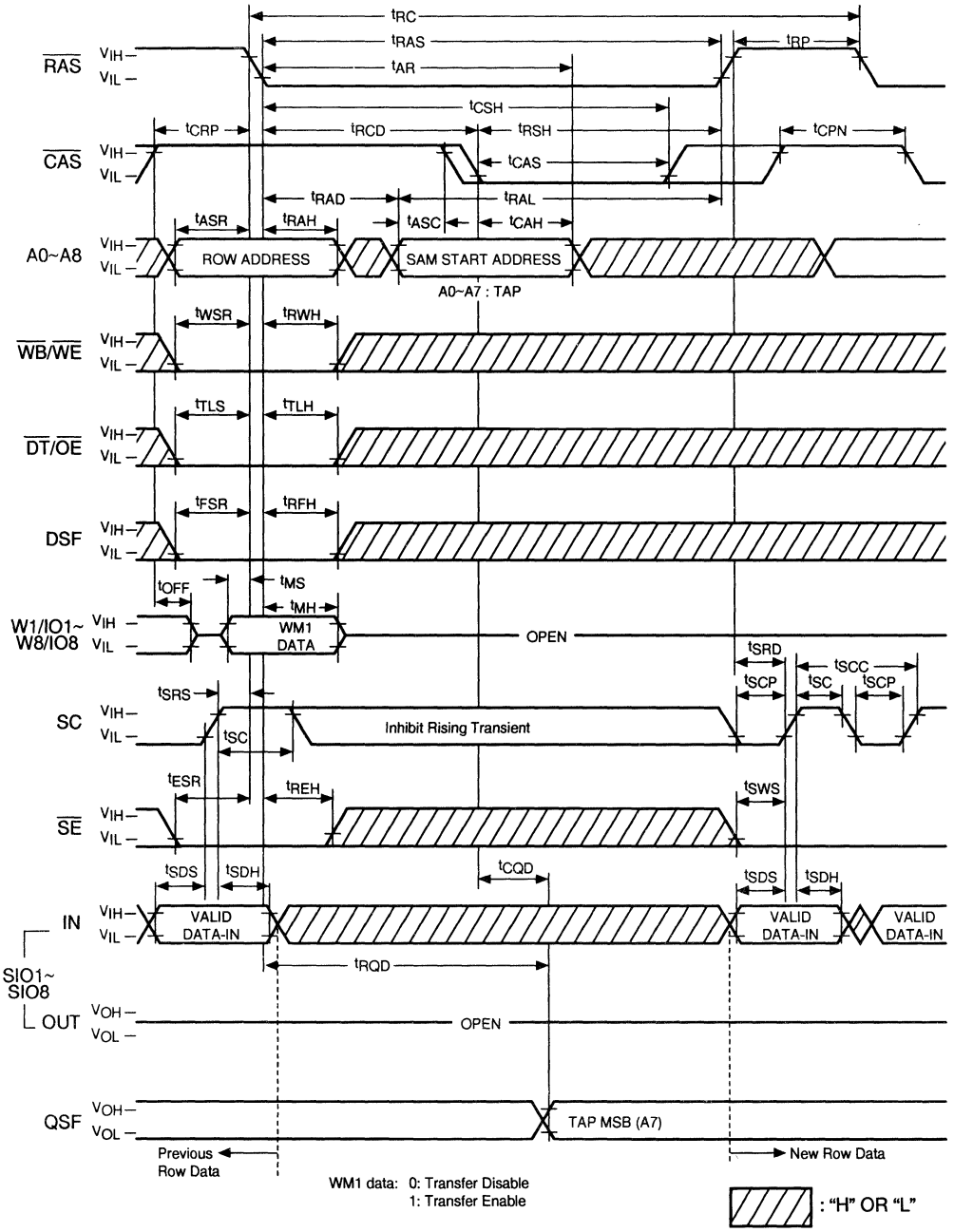


3

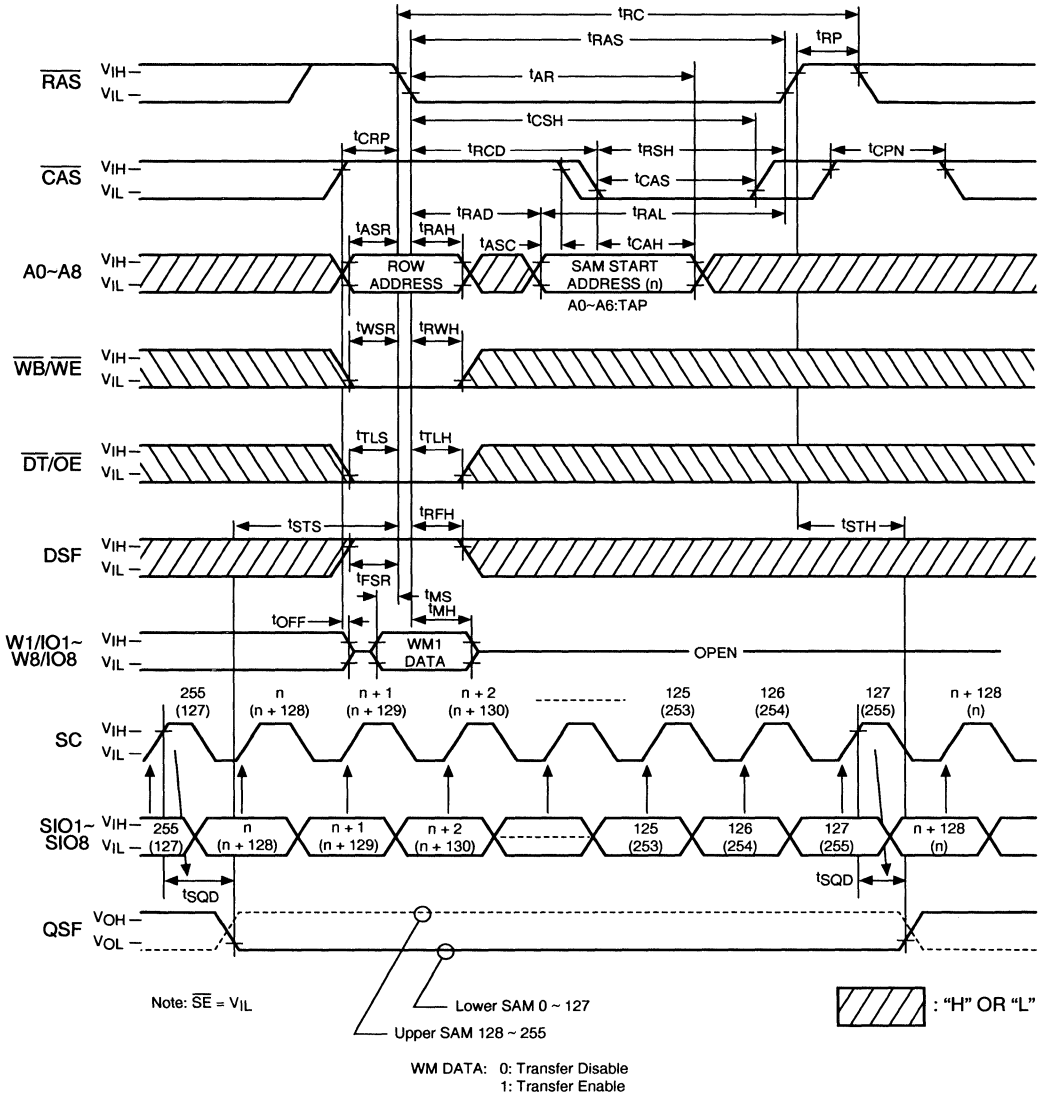
Pseudo Write Transfer Cycle



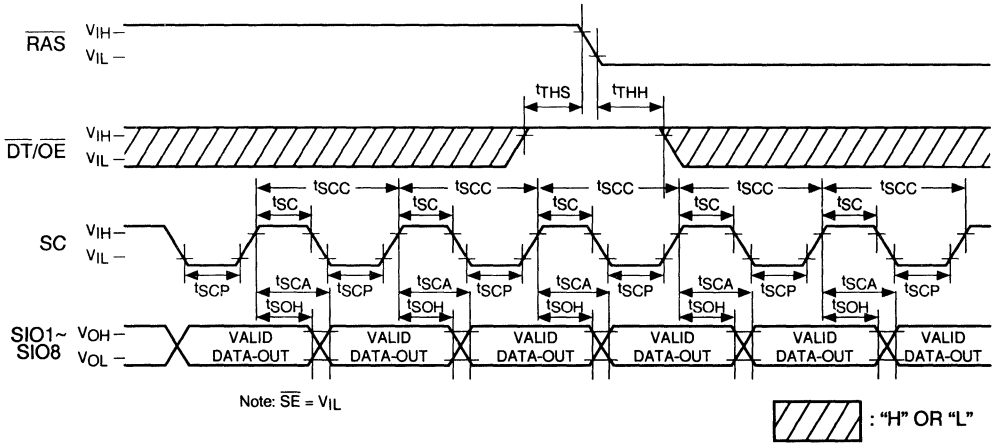
Write Transfer Cycle



Split Write Transfer Cycle

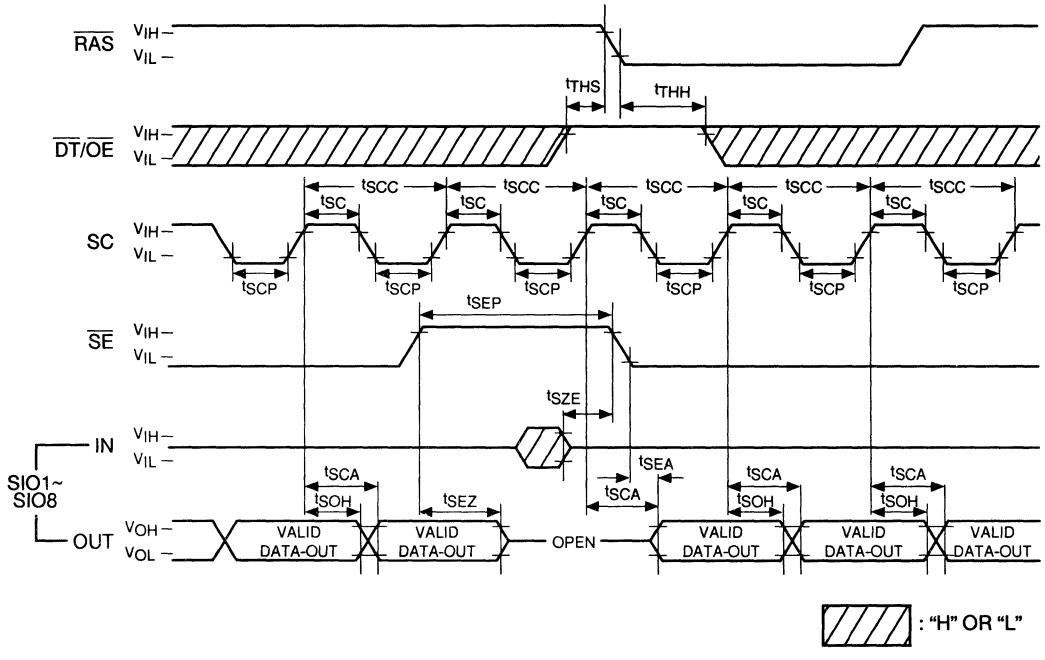


Serial Read Cycle ($\overline{SE}$ = V_{IL})

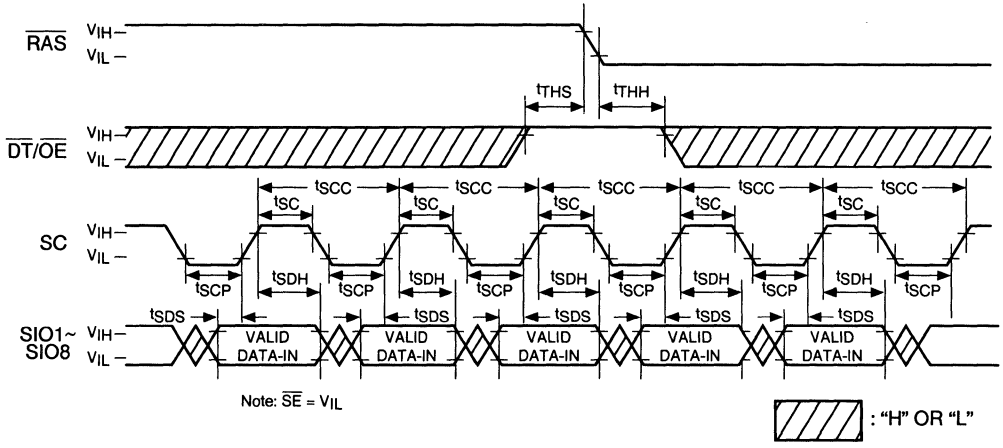


3

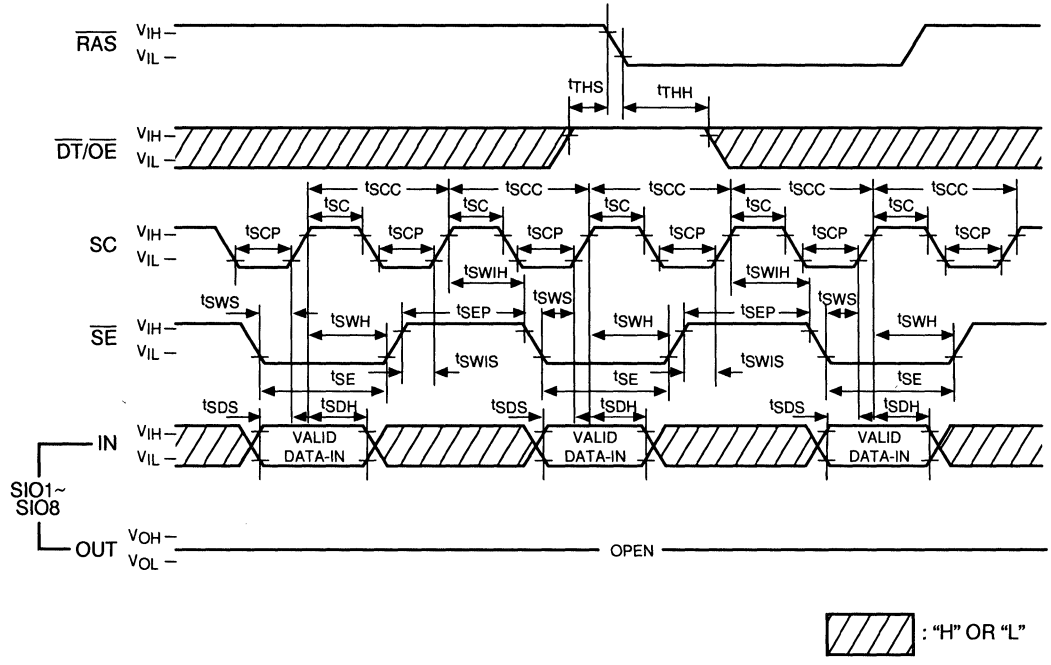
Serial Read Cycle ($\overline{SE}$ Controlled Outputs)



Serial Write Cycle ($\overline{SE}$ = V_{IL})



Serial Write Cycle ($\overline{SE}$ Controlled Inputs)



Pin Functions

Address Inputs: A0–A8

The 17 address bits required to decode 8 bits of the 1,048,576 cell locations within the dynamic RAM memory array of the V52C8128 are multiplexed onto 9 address input pins (A_0–A_8). Nine row address bits are latched on the falling edge of the row address strobe ($\overline{RAS}$) and the following eight column address bits are latched on the falling edge of the column address strobe ($\overline{CAS}$).

Row Address Strobe: $\overline{RAS}$

A random access cycle or a data transfer cycle begins at the falling edge of $\overline{RAS}$. $\overline{RAS}$ is the control input that latches the row address bits and the states of $\overline{CAS}$, $\overline{DT/OE}$, $\overline{WB/WE}$, $\overline{SE}$ and DSF to invoke the various random access and data transfer operating modes shown in Table 2. $\overline{RAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. The RAM port is placed in standby mode when the $\overline{RAS}$ control is held "high".

Column Address Strobe: $\overline{CAS}$

$\overline{CAS}$ is the control input that latches the column address bits and the state of the special function input DSF. DSF is used in conjunction with the $\overline{RAS}$ control to select either read/write operation or the special Block Write feature on the RAM port when DSF is held "low" at the falling edge of $\overline{RAS}$. Refer to the operation truth table shown in Table 1. $\overline{CAS}$ has minimum and maximum pulse widths and a minimum precharge requirement which must be maintained for proper device operation and data integrity. $\overline{CAS}$ also acts as an output enable for the output buffers on the RAM port.

Data Transfer/Output Enable: $\overline{DT/OE}$

The $\overline{DT/OE}$ input is a multifunction pin. When $\overline{DT/OE}$ is "high" at the falling edge of $\overline{RAS}$, RAM port operations are performed and $\overline{DT/OE}$ is used as an output enable control. When the $\overline{DT/OE}$ is "low" at the falling edge of $\overline{RAS}$, a data transfer operation is started between the RAM port and the SAM port.

Write Per Bit/Write Enable: $\overline{WB/WE}$

The $\overline{WB/WE}$ input is also a multifunction pin. When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, during RAM port operations, it is used to write data into the memory array in the same manner as a standard DRAM. When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, during RAM port operations, the write-per-bit function is enabled. The $\overline{WB/WE}$ input also determines the direction of data transfer between the RAM array and the serial register (SAM).

When $\overline{WB/WE}$ is "high" at the falling edge of $\overline{RAS}$, the data is transferred from RAM to SAM (read transfer). When $\overline{WB/WE}$ is "low" at the falling edge of $\overline{RAS}$, the data is transferred from SAM to RAM (masked write transfer).

Write Mask Data/Data Input and Output: W_1/IO_1–W_8/IO_8

When the write-per-bit function is enabled, the mask data on the W_i/IO_i pins is latched into the write mask register (WM1) at the falling edge of $\overline{RAS}$. Data is written into the DRAM on data lines where the write-mask data is a logic "1". Writing is inhibited on data lines where the write-mask data is a logic "0". The write-mask data is valid for only one cycle. Data is written into the RAM port during a write or read-modify-write cycle. The input data is latched at the falling edge of either $\overline{CAS}$ or $\overline{WB/WE}$, whichever occurs late. During an early-write cycle, the outputs are in the high-impedance state. Data is read out of the RAM port during a read or read-modify-write cycle. The output data becomes valid on the W_i/IO_i pins after the specified access times from $\overline{RAS}$, $\overline{CAS}$, $\overline{DT/OE}$ and column address are satisfied and will remain valid as long as $\overline{CAS}$ and $\overline{DT/OE}$ are kept "low". The outputs will return to the high-impedance state at the rising edge of either $\overline{CAS}$ or $\overline{DT/OE}$, whichever occurs first.

Serial Clock: SC

All operations of the SAM port are synchronized with the serial clock SC. Data is shifted in or out of the SAM registers at the rising edge of SC. In a serial read, the output data becomes valid on the SIO pins after the maximum specified serial access time t_{SCA} from the rising edge of SC. The serial clock SC also increments the 8-bits serial pointer (7-bits in split register mode) which is used to select the SAM address. The pointer address is incremented in a wrap-around mode to select sequential locations after the starting location which is determined by the column address in the normal transfer cycle. When the pointer reaches the most significant address location (decimal 255), the next SC clock will place it at the least significant address location (decimal 0). The serial clock SC must be held at a constant V_{IH} or V_{IL} level during read/pseudo write/write transfer

operations and should not be clocked while the SAM port is in the standby mode, to prevent the SAM pointer from being incremented.

Serial Enable: $\overline{SE}$

The $\overline{SE}$ input is used to enable serial access operation. In a serial read cycle, $\overline{SE}$ is used as an output control. In a serial write cycle, $\overline{SE}$ is used as a write enable control. When $\overline{SE}$ is "high", serial access is disabled, however, the serial address pointer location is still incremented when SC is clocked even when $\overline{SE}$ is "high".

Special Function Control Input: DSF

The DSF input is latched at the falling edge of $\overline{RAS}$ and $\overline{CAS}$ and allows for the selection of various random port and data transfer operating modes. In addition to the conventional multiport DRAM, the special features, consisting of flash write, block write, load/read color register and split read/write transfer can be invoked.

Special Function Output: QSF

QSF is an output signal which, during split register mode, indicates which half of the split SAM is being accessed. QSF "low" indicates that the lower split SAM (Bit 0–127) is being accessed, and QSF "high" indicates that the upper split SAM (Bit 128–255) is being accessed. QSF is monitored so that after it toggles and after allowing for a delay of t_{STS}, split read/write transfer operation can be performed on the non-active split SAM.

Serial Input/Output: SIO1–SIO8

Serial input and output share common I/O pins. Serial input or output mode is determined by the most recent read, write or pseudo write transfer cycle. When a read transfer cycle is performed, the SAM port is in the output mode. When a write or pseudo write transfer cycle is performed, the SAM port is switched from output mode to input mode. During the subsequent write transfer cycle, the SAM remains in the input mode.

Operation Mode

The RAM port and data transfer operating of the V52C8128 are determined by the state of $\overline{CAS}$, $\overline{DT}$/$\overline{OE}$, $\overline{WB}$/$\overline{WE}$, $\overline{SE}$ and DSF at the falling edge of $\overline{RAS}$ and by the state of DSF at the falling edge of $\overline{CAS}$. The Table 1 and Table 2 show the operation truth table and the functional truth table for a listing of all available RAM port and transfer operations, respectively.

Table 1. Operation Truth Table

$\overline{CAS}$ Falling Edge ↓			DSF	0	0	1	1
$\overline{RAS}$ Falling Edge ↓			DSF	0	1	0	1
$\overline{CAS}$	$\overline{DT}$/$\overline{OE}$	$\overline{WB}$/$\overline{WE}$	$\overline{SE}$				
0	•	•	•	$\overline{CAS}$-before-$\overline{RAS}$ Refresh			
1	0	0	0	Masked Write Transfer	Split Write Transfer	Masked Write Transfer	Split Write Transfer with
1	0	0	1	Pseudo Write Transfer	With Mask	Pseudo Write Transfer	Mask
1	0	1	•	Read Transfer	Split Read Transfer	Read Transfer	Split Read Transfer
1	1	0	•	Read/Write per Bit	Masked Flash Write	Masked Block Write	Masked Flash Write
1	1	1	•	Read/Write	Load/Read Color	Block Write	Load/Read Color

Table 2. Functional Truth Table

Function	$\overline{RAS}\downarrow$					$\overline{CAS}\downarrow$	Address		W/IO			Write Mask	Register	
	$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	DSF	$\overline{SE}$	DSF	$\overline{RAS}\downarrow$	$\overline{CAS}\downarrow$	$\overline{RAS}\downarrow$	$\overline{CAS}\downarrow$	$\overline{CAS}\downarrow$ $\overline{WE}\downarrow$		WM1	Color
$\overline{CAS}$-before-$\overline{RAS}$ Refresh	0	•	•	•	•	–	•	–	•	–	–	–	–	–
Masked Write Transfer	1	0	0	0	0	•	Row	TAP	WM1	•	•	WM1	Load use	–
Pseudo Write Transfer	1	0	0	0	1	•	Row	TAP	•	•	•	–	–	–
Split Write Transfer	1	0	0	1	•	•	Row	TAP	WM1	–	•	WM1	Load use	–
Read Transfer	1	0	1	0	•	•	Row	TAP	•	•	•	–	–	–
Split Read Transfer	1	0	1	1	•	•	Row	TAP	•	•	•	–	–	–
Write per Bit	1	1	0	0	•	0	Row	Column	WM1	–	DIN	WM1	Load use	–
Masked Block Write	1	1	0	0	•	1	Row	Column A2C-7C	WM1	Column Select	–	WM1	Load use	use
Masked Flash Write	1	1	0	1	•	•	Row	•	WM1	–	•	WM1	Load use	use
Read/Write	1	1	1	0	•	0	Row	Column	•	–	DIN	–	–	–
Block Write	1	1	1	0	•	1	Row	Column A2C-7C	•	Column Select	–	–	–	use
Load/Read Color	1	1	1	1	•	•	Row	•	•	–	Color	–	–	Load/Read

Note : • = "0" or "1", TAP = SAM Start Address, – = not used.

If the special function control input (DSF) is in the "low" state at the falling edges of $\overline{RAS}$ and $\overline{CAS}$, only the conventional multiport DRAM operating features can be invoked: $\overline{CAS}$-before-$\overline{RAS}$ refresh, write transfer, pseudo-write transfer, read transfer, write per bit and read/write modes. If the DSF input is "high" at the falling edge of $\overline{RAS}$, special features such as split write transfer, split read transfer, flash write and load/read color register can be invoked. If the DSF input is "low" at the falling edge of $\overline{RAS}$ and "high" at the falling edge of $\overline{CAS}$, the block write special feature can be invoked.

RAM Port Operation

Fast Page Mode Cycle

Fast page mode allows data to be transferred into or out of multiple column locations of the same row by performing multiple $\overline{CAS}$ cycles during a single active $\overline{RAS}$ cycle. During a fast page cycle, the $\overline{RAS}$ signal may be maintained active for a period up to 100 µs. For the initial fast page mode access, the output data is valid after the specified access times from $\overline{RAS}$, $\overline{CAS}$, column address and $\overline{DT/OE}$. For all subsequent fast page mode read operations, the output data is valid after the specified access times from $\overline{CAS}$, column address and $\overline{DT/OE}$. When the write-per-bit function is enabled, the mask data latched at the falling edge of $\overline{RAS}$ is maintained throughout the fast page mode write or read-modify-write cycle.

$\overline{RAS}$-Only Refresh

The data in the DRAM requires periodic refreshing to prevent data loss. Refreshing is accomplished by performing a memory cycle at each of the 512 rows in the DRAM array within the specified 8ms refresh period. Although any normal memory cycle will perform the refresh operation, this function is most easily accomplished with the "$\overline{RAS}$-Only" cycle.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh

The V52C8128 also offers an internal-refresh function. When $\overline{CAS}$ is held "low" for a specified period (t_{CSR}) before $\overline{RAS}$ goes "low", an internal refresh address counter and on-chip refresh control clock generators are enabled and an internal refresh operation takes place. When the refresh operation is completed, the internal refresh address counter is automatically incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ cycle. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain "low" while cycling $\overline{RAS}$.

Hidden Refresh

A hidden refresh is a $\overline{CAS}$-before-$\overline{RAS}$ refresh performed by holding $\overline{CAS}$ "low" from a previous read cycle. This allows for the output data from the previous memory cycle to remain valid while performing a refresh. The internal refresh address counter provides the address and the refresh is accomplished by cycling $\overline{RAS}$ after the specified $\overline{RAS}$-precharge period (refer to Figure 1.)

Write-Per-Bit Function

The write-per-bit function selectively controls the internal write-enable circuits of the RAM port. When $\overline{WB/WE}$ is held "low" at the falling edge of $\overline{RAS}$, during a random access operation, the write-mask is enabled. At the same time, the mask data on the W_i/IO_i pins is latched into the write-mask register (WM1). When a "0" is sensed on any of the W_i/IO_i pins, their corresponding write circuits are disabled and new data will not be written. When an "1" is sensed on any of the W_i/IO_i pins, their corresponding write circuits will remain enabled so that new data is written. The truth table of the write-per-bit function is shown in Table 3.

At the falling edge of $\overline{RAS}$				Function
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	Wi/IOi (i = 1–8)	
H	H	H	•	Write Enable
H	H	L	1	Write Enable
			0	Write Mask

Table 3. Truth Table for Write-Per-Bit Function

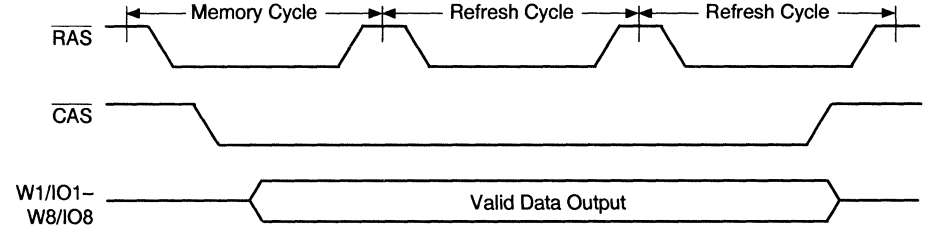


Figure 1. Hidden Refresh Cycle

An example of the write-per-bit function illustrating its application to displays is shown in Figures 2 and 3.

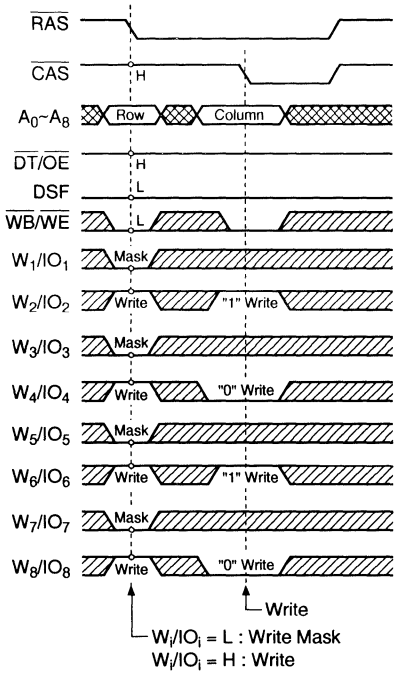


Figure 2. Write-per-bit timing cycle

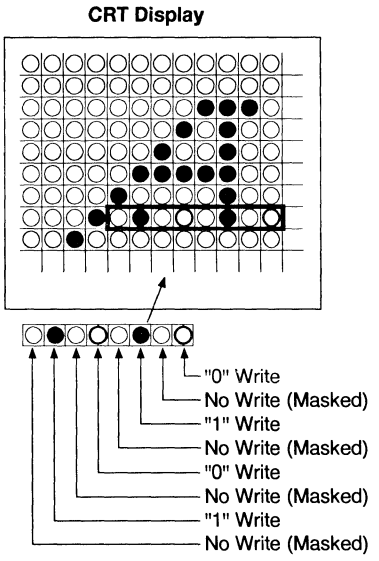


Figure 3. Corresponding bit-map

3

Load Color Register/Read Color Register

The V52C8128 is provided with an on-chip 8-bits register (color register) for use during the flash write or block write operation. Each bit of the color register corresponds to one of the DRAM I/O blocks. The load color register cycle is initiated by holding $\overline{CAS}$, $\overline{WB/WE}$, $\overline{DT/OE}$ and DSF "high" at the falling edge of $\overline{RAS}$. The data presented on the W_i/IO_i lines is subsequently latched into the color register at the falling edge of either $\overline{CAS}$ or $\overline{WB/WE}$, whichever occurs late. The data stored in the color register can be read out by performing a read color register cycle. This cycle is activated by holding $\overline{CAS}$, $\overline{WB/WE}$, $\overline{DT/OE}$ and DSF "high" at the falling edge of $\overline{RAS}$ and by holding $\overline{WB/WE}$ "high" at the falling edge of $\overline{CAS}$ and throughout the remainder of the cycle. The data in the color register becomes valid on the W_i/IO_i lines after the specified access times from $\overline{RAS}$ and $\overline{DT/OE}$ are satisfied. During the load/read color register cycle, valid A_0–A_8 row addresses are not required, but the memory cells on the row address latched at the falling edge of $\overline{RAS}$ are refreshed.

Flash Write

Flash write is a special RAM port write operation, which in a single $\overline{RAS}$ cycle allows for the data in the color register to be written into all the memory locations of a selected row. Each bit of the color register corresponds to one of the DRAM I/O blocks and the flash write operation can be selectively controlled on an I/O basis in the same manner as the write-per-bit operation.

A flash write cycle is performed by holding $\overline{CAS}$ "high", $\overline{WB/WE}$ "low" and DSF "high" at the falling edge of $\overline{RAS}$. The mask data must also be provided on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ in order to enable the flash write operation for selected I/O blocks (refer to Figures 4 and 5).

Flash write is most effective for fast plane clear operations in frame buffer applications. Selected planes can be cleared by performing 512 flash write cycles and by specifying a different row address location during each flash write cycle (refer to Figure 6). Assuming a cycle time of 180ns, a plane clear operation can be completed in less than 92.2μs.

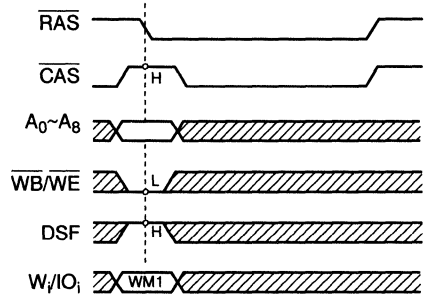


Figure 4. Flash Write Timing

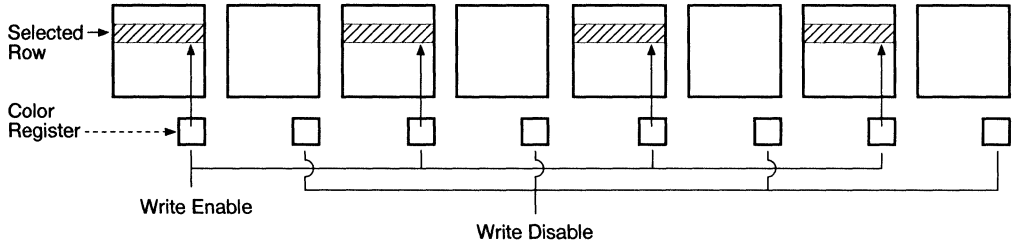


Figure 5. Flash Write

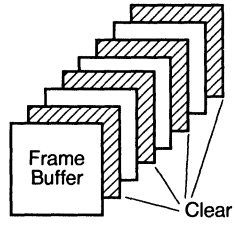


Figure 6. Plane clear application example

Block Write

Block write is also a special RAM port write operation which, in a single RAS cycle, allows for the data in the color register to be written into 4 consecutive column address locations starting from a selected column address in a selected row. The block write operation can be selectively controlled on an I/O basis and a column mask capability is also available.

A block write cycle is performed by holding CAS and DT/OE "high" and DSF "low" at the falling edge of RAS and by holding DSF "high" at the falling edge of CAS. The state of the WB/WE input at the falling edge of RAS determines whether or not the I/O data mask is enabled (WB/WE must be "low" to enable the I/O data mask or "high" to disable it). At the falling edge of RAS, a valid row address and I/O mask data are also specified. At the falling edge of CAS, the starting column address location and column mask data must be provided. During a block write cycle, the 2 least significant column address locations (A0C and A1C) are internally controlled and only the six most significant column addresses (A2C–A7C) are latched at the falling edge of CAS. (Refer to Figure 7).

An example of the block write function is shown in Figure 8 with a data mask on W1/IO1, W4/IO4, W6/IO6, W7/IO7 and column 2. Block write is most effective for window clear and fill operations in frame buffer applications, as shown on Figure 9.

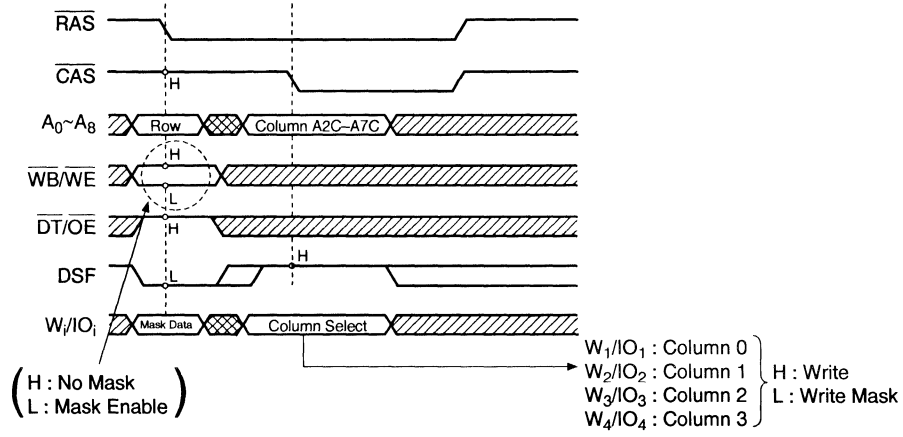


Figure 7. Block Write Timing

3

	Mask Data	Column Select	Color Register Data
W_1/IO_1	0	1	0
W_2/IO_2	1	1	0
W_3/IO_3	1	0	1
W_4/IO_4	0	1	1
W_5/IO_5	1	—	1
W_6/IO_6	0	—	1
W_7/IO_7	0	—	0
W_8/IO_8	1	—	0

	Column 0	Column 1	Column 2	Column 3	
W_1/IO_1					← Mask
W_2/IO_2	0	0		0	
W_3/IO_3	1	1		1	
W_4/IO_4					← Mask
W_5/IO_5	1	1		1	
W_6/IO_6					← Mask
W_7/IO_7					← Mask
W_8/IO_8	0	0		0	
			↑ Mask		

Figure 8. Example for Block Write Operation

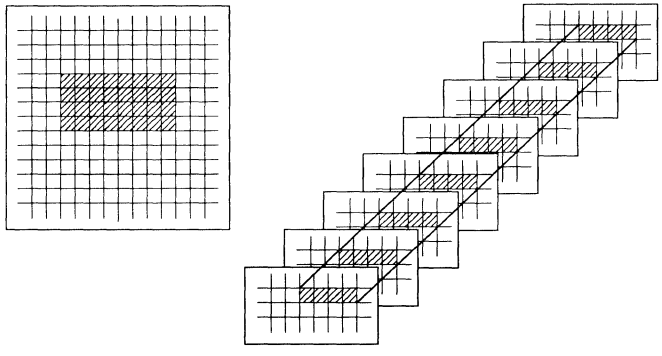


Figure 9. Example of Block Write Application

Fast Page Mode Block Write Cycle

Fast page mode block write can be used to perform high speed clear and fill operaitons. The cycle is initiated by holding the DSF signal "low" at the falling edge of RAS and a fast page mode block write is performed during each subsequent CAS cycle with DSF held "high" at the falling edge of CAS.

If the DSF signal is "low" at the falling edge of CAS, a normal fast page mode read/write operation will occur. Therefore, a combination of block write and read/write operations can be performed during a fast page mode block write cycle (refer to Figure 10).

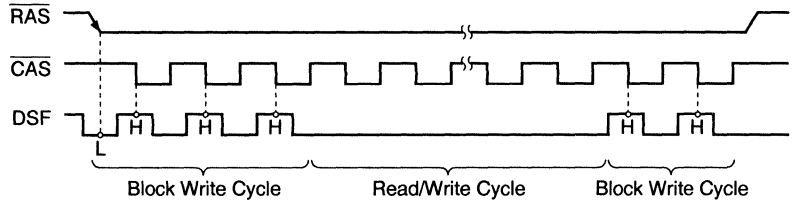


Figure 10. Fast Page Mode Block Write Cycle

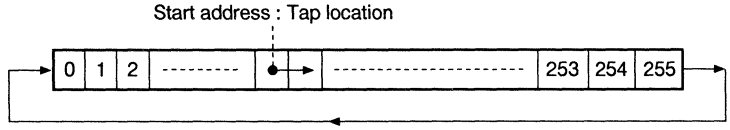
SAM Port Operation

The V52C8128 is provided with a 256 words by 8 bits serial access memory (SAM) which can be operated in the single register mode or in the split register mode.

Single Register Mode

When operating in the single register mode, high speed serial read or write operations can be performed through the SAM port independent of the RAM port operations, except during read/write/ pseudo-write transfer cycles. The preceding transfer operation determines the direction of data flow through the SAM port. If the preceding transfer operation is a read transfer, the SAM port is in the output mode. If the preceding transfer operation is a write or pseudo write transfer, the SAM port is in the input mode. The pseudo write transfer operation only switches the SAM port from output mode to input mode; data is not transferred from SAM to RAM.

Serial data can be read out of the SAM port after a read transfer (RAM → SAM) has been performed. The data is shifted out of the SAM port starting at any of the 256 bits locations. The TAP location corresponds to the column address selected at the falling edge of CAS during the read transfer cycle. The SAM registers are configured as circular data registers. The data is shifted out sequentially starting from the selected tap location to the most significant bit, and then wraps around to the least significant bit, as illustrated below.



Subsequent real-time read transfer may be performed on-the-fly as many times as desired, within the refresh constraints of the DRAM array. Simultaneous serial read operation can be performed with some timing restrictions. A pseudo write transfer cycle is performed to change the SAM port from output mode to input mode, in order to write data into the serial registers through the SAM port. A write transfer cycle must be used subsequently to load the SAM data into the RAM row selected by the row address at the falling edge of $\overline{RAS}$. The starting location in the SAM registers for the next serial write is selected by the column address at the falling edge of $\overline{CAS}$. The truth table for single register mode SAM operation is shown in Table 4.

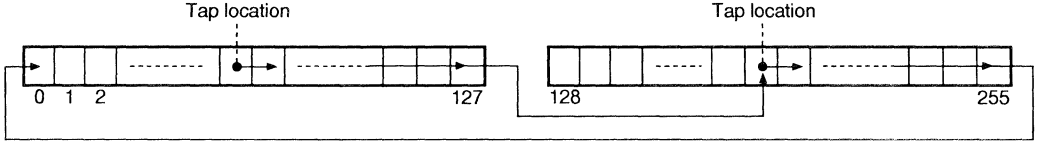
SAM Port Operation	$\overline{DT}/\overline{OE}$ at the falling edge of $\overline{RAS}$	SC	$\overline{SE}$	Function	Preceded by a
Serial Output Mode	H	⎍	L	Enable Serial Read	Read Transfer
			H	Disable Serial Read	
Serial Input Mode	H	⎍	L	Enable Serial Write	Write Transfer
			H	Disable Serial Write	
Serial Input Mode	H	⎍	L	Enable Serial Write	Pseudo Write Transfer
			H	Disable Serial Write	

Table 4. Truth Table for SAM Port Operation

3

Split Register Mode

In split register mode, data can be shifted into or out of one half of the SAM while a split read or split write transfer is being performed on the other half of the SAM. A normal (non-split) read/write/pseudo write transfer operation must precede any split read/write transfer operation. The non-split read, write and pseudo write transfers will set the SAM port into output mode or input mode. The split read and write transfers will not change the SAM port mode set by the preceding normal transfer operation. RAM port operation may be performed independently except during split transfers. In the split register mode, serial data can be shifted in or out of one of the split SAM registers starting from any of the 128 tap locations, excluding the last address of each split SAM. Data is shifted in or out sequentially starting from the selected tap location to the most significant bit (127 or 255) of the first split SAM. Then the SAM pointer moves to the tap location selected for the second split SAM, to shift data in or out sequentially starting from this tap location to the most significant bit (255 or 127), and finally wraps around to the least significant bit, as illustrated below.

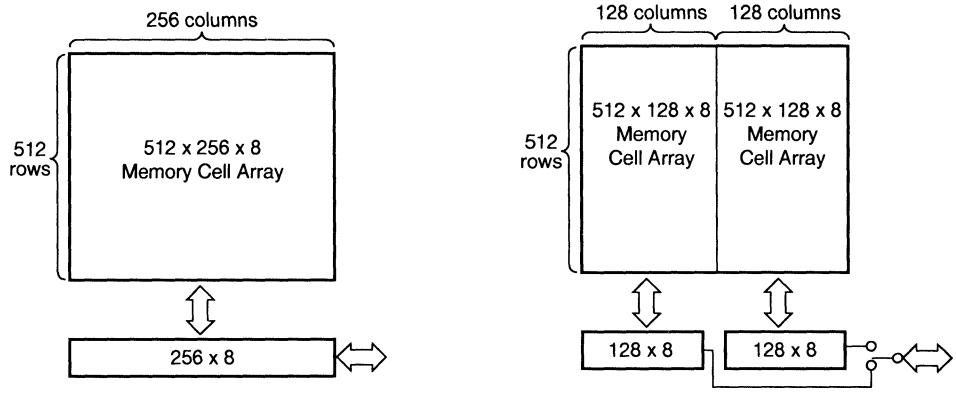


Refresh

The SAM data registers are static flip-flop, therefore a refresh is not required.

Data Transfer Operation

The V52C8128 features two types of internal bidirectional data transfer capability between RAM and the SAM, as shown in Figure 11. During a normal transfer, 256 words by 8 bits of data can be loaded from RAM to SAM (Read Transfer) or from SAM to RAM (Write Transfer). During a split transfer, 128 words by 8 bits of data can be loaded from the lower/upper half of the RAM into the lower/upper half of the SAM (Split Read Transfer) or from the lower/upper half of the SAM into the lower/upper half of the RAM (Split Write Transfer). The normal transfer and split transfer modes are controlled by the DSF special function input signal.



a. Normal (Non-split) Transfer **b. Split Transfer**

Figure 11. Transfer Operation

As shown in Table 5, the V52C8128 supports five types of transfer operations: Read transfer, Split Read transfer, Write transfer, Split Write transfer and Pseudo Write transfer. Data transfer operations between RAM and SAM are invoked by holding the $\overline{DT/OE}$ signal "low" at the falling edge of $\overline{RAS}$. The type of data transfer operation is determined by the state of $\overline{CAS}$, $\overline{WB/WE}$, $\overline{SE}$ and DSF which are latched at the falling edge of $\overline{RAS}$. During normal data transfer operations, the SAM port is switched from input to output mode (Read Transfer) or output to input mode (Write Transfer/Pseudo Write Transfer), whereas it remains unchanged during split transfer operations (Split Read or Write Transfer). During a data transfer cycle, the row address A_0–A_8 selects one of the 512 rows of the memory array to or from which data will be transferred, and the column address A_0–A_7 selects one of the tap locations in the serial register. The selected tap location is the start position in the SAM port from which the first serial data will be read out during the subsequent serial read cycle or the start position in the SAM port into which the first serial data will be written during the subsequent serial write cycle. During split data transfer cycles, the most significant column address (A7C) is controlled internally to determine which half of the serial register will be accessed.

At the falling edge of $\overline{RAS}$								
$\overline{CAS}$	$\overline{DT/OE}$	$\overline{WB/WE}$	$\overline{SE}$	DSF	Transfer Mode	Transfer Direction	Transfer Bit	SAM Port Mode
H	L	H	•	L	Read Transfer	RAM → SAM	256 x 8	Input → Output
H	L	L	L	L	Write Transfer	SAM → RAM	256 x 8	Output → Input
H	L	L	H	L	Pseudo Write Transfer	—	—	Output → Input
H	L	H	•	H	Split Read Transfer	RAM → SAM	128 x 8	Not changed
H	L	L	•	H	Split Write Transfer	SAM → RAM	128 x 8	Not changed

Note: • = "H" or "L"

Table 5. Transfer Modes

Read Transfer Cycle

A read transfer cycle consists of loading a selected row of data from the RAM array into the SAM register. A read transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low", $\overline{WB/WE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row to be transferred into the SAM. The transfer cycle is completed at the rising edge of $\overline{DT/OE}$. When the transfer is completed, the SAM port is set into the output mode. In a read/real time read transfer cycle, the transfer of a new row of data is completed at the rising edge of $\overline{DT/OE}$ and this data becomes valid on the SIO lines after the specified access time (t_{SCA}) from the rising edge of the subsequent serial clock (SC) cycle. The start address of the serial pointer of the SAM is determined by the column address selected at the falling edge of $\overline{CAS}$.

Figure 12 shows the operation block diagram for the read transfer operation.

In a read transfer cycle (which is preceded by a write transfer cycle), the SC clock must be held at a constant V_{IL} or V_{IH}, after the SC high time has been satisfied. A rising edge of the SC clock must not occur until after the specified delay (t_{TSD}) from the rising edge of $\overline{DT/OE}$, as shown in Figure 13.

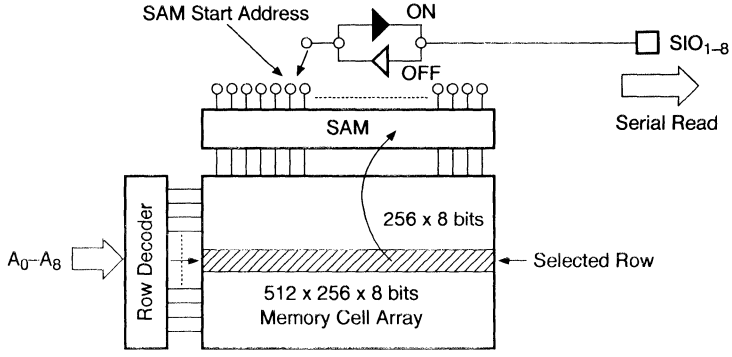


Figure 12. Block Diagram for Read Transfer Operation

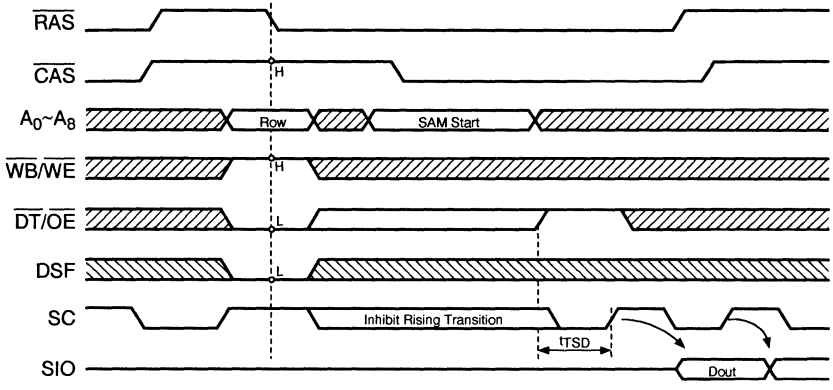


Figure 13. Read Transfer Timing

In a real time read transfer cycle (which is preceded by another read transfer cycle), the previous row data appears on the SIO lines until the $\overline{DT}/\overline{OE}$ signal goes "high" and the serial access time (t_{SCA}) for the following serial clock is satisfied. This feature allows for the first bit of the new row of data to appear on the serial output as soon as the last bit of the previous row has been strobed without any timing loss. To make this continuous data flow possible, the rising edge of $\overline{DT}/\overline{OE}$ must be synchronized with $\overline{RAS}$, $\overline{CAS}$ and the subsequent rising edge of SC (t_{RTH}, t_{CTH}, and t_{TSL}/t_{TSD} must be satisfied), as shown in Figure 14.

The timing restrictions t_{TSL}/t_{TSD} are 5ns min/15ns min. The split read transfer mode eliminates these timing restrictions.

Write Transfer Cycle

A write transfer cycle consists of loading the contents of the SAM register into a selected row of the RAM array. If the SAM data to be transferred must first be loaded through the SAM port, a pseudo write transfer operation must precede the write transfer cycles. However, if the SAM port data to be transferred into the RAM was previously loaded into the SAM via a read transfer, the SAM to RAM transfer can be executed simply by performing a write transfer directly. A write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT}/\overline{OE}$ "low", $\overline{WB}/\overline{WE}$ "low", $\overline{SE}$ "low" and DSF "low" at the falling edge of $\overline{RAS}$. This write transfer is selectively controlled per RAM I/O block by setting the mask data on the W_i/IO_i lines at the falling edge of $\overline{RAS}$ (same as in the write-per-bit operation). Figures 15 and 16 show the timing diagram and block diagram for write transfer operations, respectively.

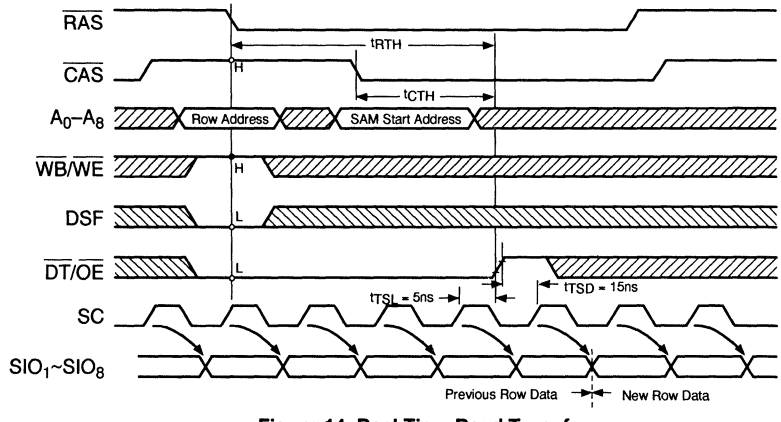


Figure 14. Real Time Read Transfer

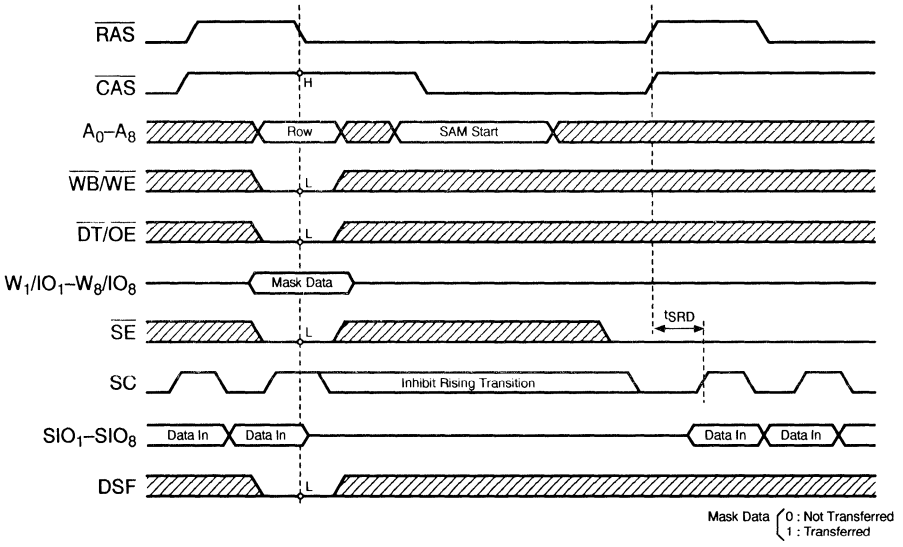


Figure 15. Write Transfer Timing

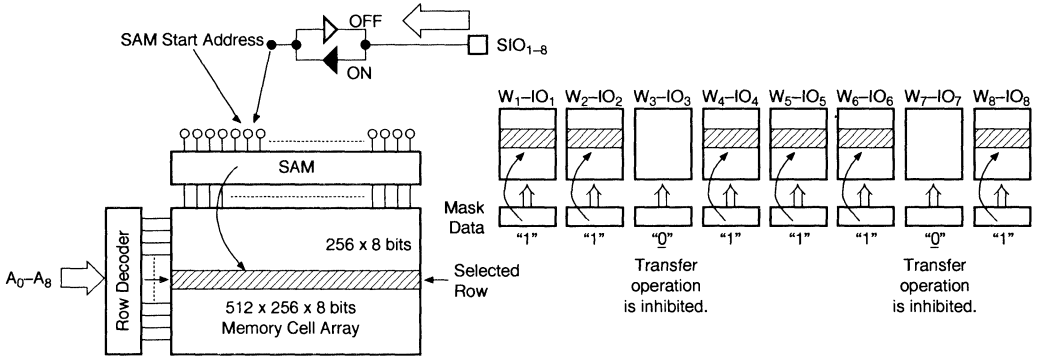


Figure 16. Block Diagram for Write Transfer Operation

The row address selected at the falling edge of $\overline{RAS}$ determines the RAM row address into which the data will be transferred. The column address selected at the falling edge of $\overline{CAS}$ determines the start address of the serial pointer of the SAM. After the write transfer is completed, the SIO lines are set in the input mode so that serial data synchronized with the SC clock can be loaded.

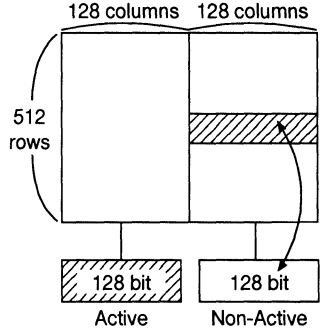
When consecutive write transfer operations are performed, new data must not be written into the serial register until the $\overline{RAS}$ cycle of the preceding write transfer is completed. Consequently, the SC clock must be held at a constant V_{IL} or V_{IH} during the $\overline{RAS}$ cycle. A rising edge of the SC clock is only allowed after the specified delay (t_{SRD}) from the rising edge of $\overline{RAS}$, at which time a new row of data can be written in the serial register.

Pseudo Write Transfer Cycle

A pseudo write transfer cycle must be performed before loading data into the serial register after a read transfer operation has been executed. The only purpose of a pseudo write transfer is to change the SAM port mode from output mode to input mode (a data transfer from SAM to RAM does not occur). After the serial register is loaded with new data, a write transfer cycle must be performed to transfer the data from SAM to RAM. A pseudo write transfer is invoked by holding $\overline{CAS}$ "high", $\overline{DT/OE}$ "low", $\overline{WB/WE}$ "low", $\overline{SE}$ "high" and DSF "low" at the falling edge of $\overline{RAS}$. The timing conditions are the same as the one for the write transfer cycle except for the state of $\overline{SE}$ at the falling edge of $\overline{RAS}$.

Split Data Transfer and QSF

The V52C8128 features a bidirectional split data transfer capability between the RAM and the SAM. During split data transfer operation, the serial register is split into two halves which can be controlled independently. Split read or split write transfer operations can be performed to or from one half of the serial register while serial data can be shifted into or out of the other half of the serial register, as shown in Figure 17. The most significant column address location (A7C) is controlled internally to determine which half of the serial register will be accessed. QSF is an output which indicates which half of the serial register is in an active state. QSF changes state when the last SC clock is applied to active split SAM, as shown in Figure 18.



Active SAM	QSF Level
lower SAM	"Low"
upper SAM	"High"

Figure 17. Split Register Mode

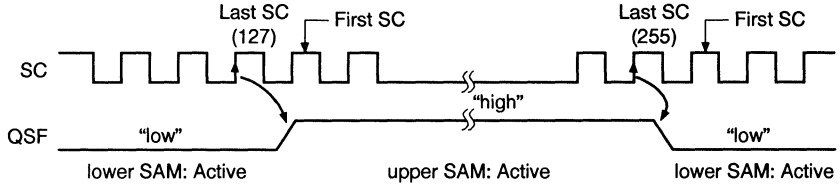


Figure 18. QSF Output State During Split Register Mode

Split Read Transfer Cycle

A split read transfer consists of loading 128 words by 8 bits of data from a selected row of the split RAM array into the corresponding non-active split SAM register.

Serial data can be shifted out of the other half of the split SAM register simultaneously. The block diagram and timing diagram for split read transfer mode are shown in Figures 19 and 20, respectively. During split read transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus eliminating timing restrictions as in the case of on-the-fly read transfers. A split read transfer can be performed after a delay of t_{STS} from the change of state of the QSF output is satisfied.

A normal (non-split) read transfer operation must precede split read transfer cycles as shown in the example in Figure 21.

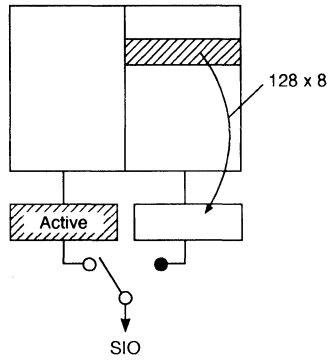


Figure 19. Block Diagram for Split Read Transfer

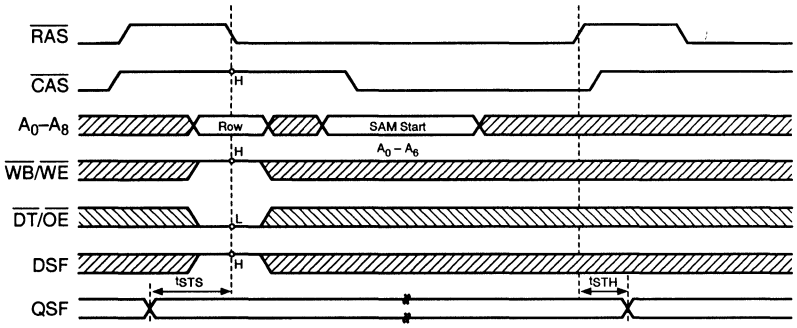


Figure 20. Timing Diagram for Split Read Transfer

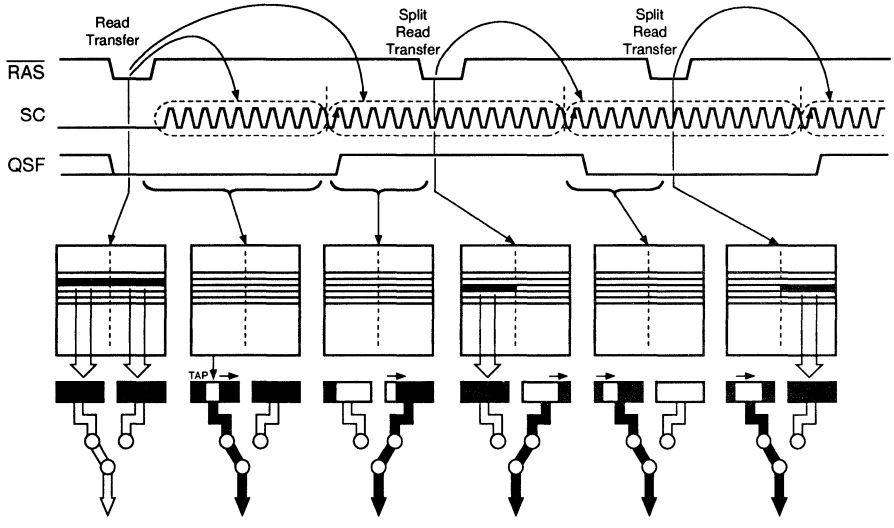


Figure 21. Example of Consecutive Read Transfer Operations

Split Write Transfer Cycle

A split write transfer cycle consists of loading 128 words by 8 bits of data from the non-active split SAM register into a selected row of the corresponding split RAM array.

Serial data can be shifted into the other half of the split SAM register simultaneously. The block diagram and timing diagram for split write transfer mode are shown in Figures 22 and 23, respectively. During split write transfer operation, the RAM port input clocks do not have to be synchronized with the serial clock SC, thus allowing for real time transfer. A split write transfer can be performed after a delay of t_{STS} from the change of state of the QSF output is satisfied.

A pseudo write transfer operation must precede split transfer cycles as shown in Figure 24. The purpose of the pseudo write transfer operation is to switch the SAM port from output mode to input mode and to set the initial tap location prior to split write transfer operations.

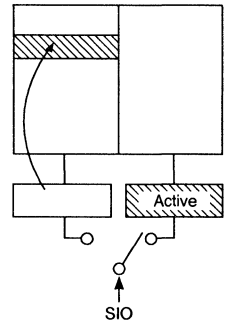


Figure 22. Block Diagram for Split Write Transfer

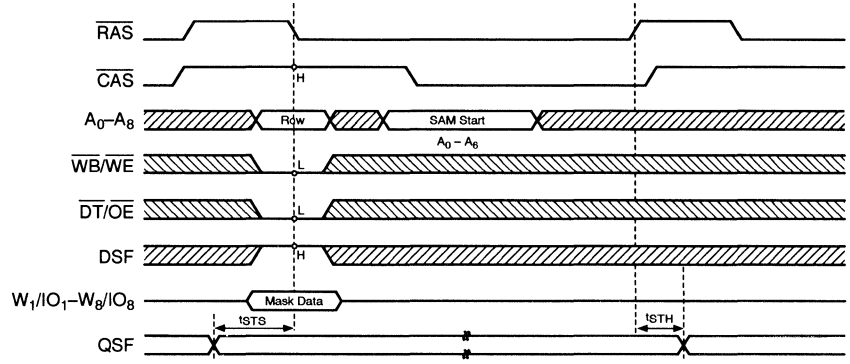


Figure 23. Timing Diagram for Split Write Transfer

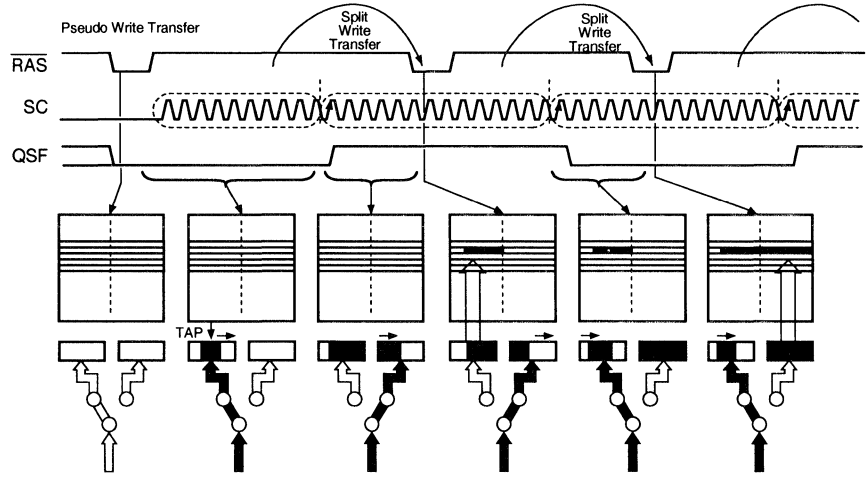


Figure 24. Example of Consecutive Write Transfer Operations

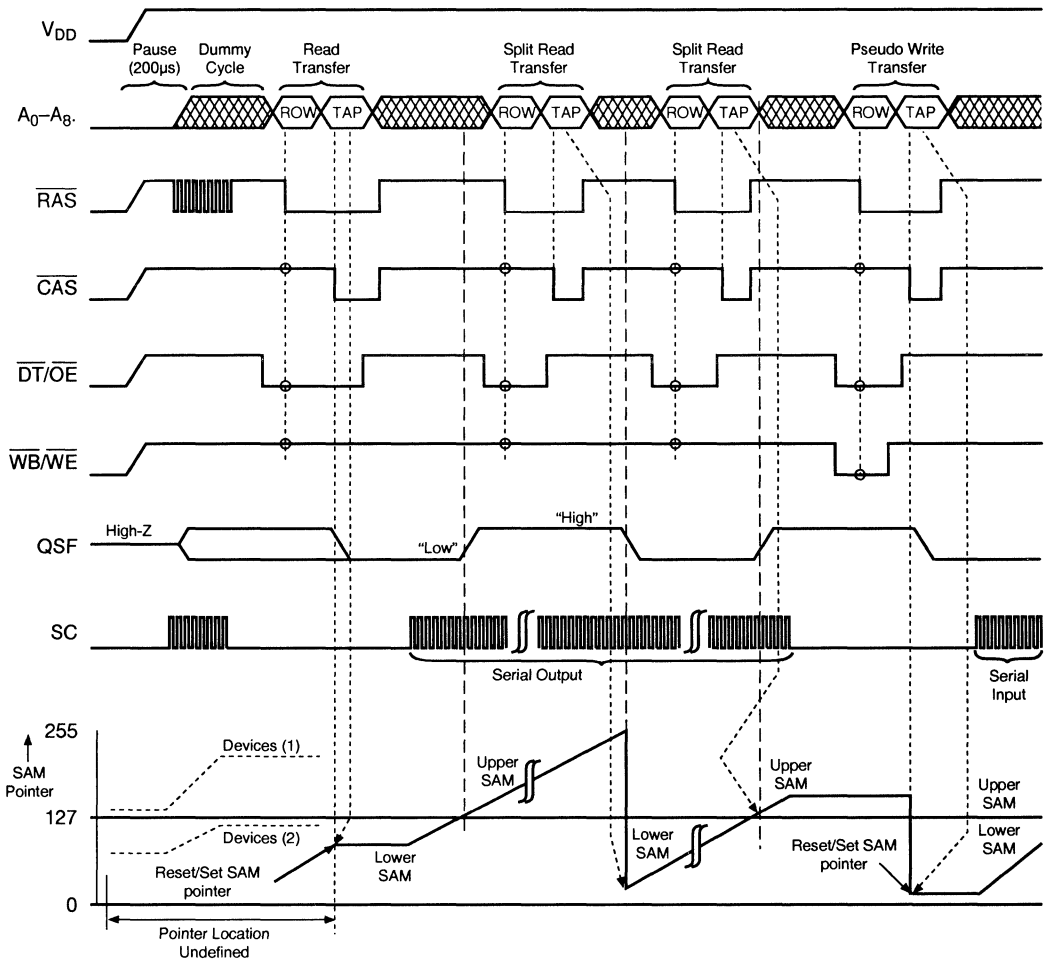


Figure 25. Example of Split SAM Register Operation Sequence

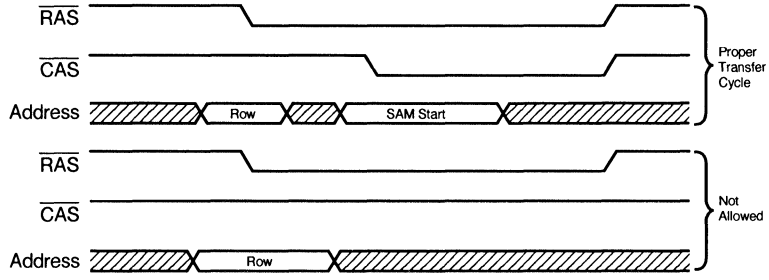
Split-Register Operation Sequence - Example

Split read/write transfers must be preceded by a normal (non-split) transfer, such as a read, write or pseudo write transfer. Figure 25 illustrates an example of split register operation sequence after device power-up and initialization. After power-up, a minimum of 8 $\overline{RAS}$ and 8 SC clock cycles must be performed to properly initialize the device. A read transfer is then performed and the column address latched at the falling edge of $\overline{CAS}$ sets the SAM tap pointer location, which up to that point was in an undefined location. Subsequently, the pointer address is incremented by cycling the serial clock SC from the starting location to the last location in the register (address 255), and wraps around to the tap location set by the split read transfer performed for the lower SAM while the upper SAM is being accessed. The SAM address is incremented as long as SC is clocked. The following split read transfer sets a new tap location in the upper split SAM register (address 128 in this example), and the pointer is incremented from this location by cycling the SC clock.

The next operation is a pseudo write transfer which switches the SAM port from output mode to input mode in preparation for either write transfers or split write transfers. The column address latched at the falling edge of CAS during the pseudo write transfer sets the serial register tap location. Serial data will be written into the SAM starting from this location.

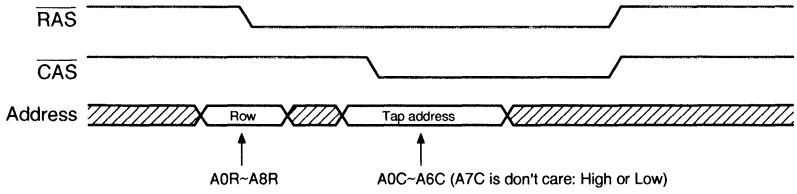
Transfer Operation Without CAS

During all transfer cycles, the CAS input clock must be cycled, so that the column addresses are latched at the falling edge of CAS, to set the SAM tap location. If CAS was maintained at a constant "high" level during a transfer cycle, the SAM pointer location would be undefined. Therefore, a transfer cycle with CAS held "high" is not allowed (refer to the illustration below).

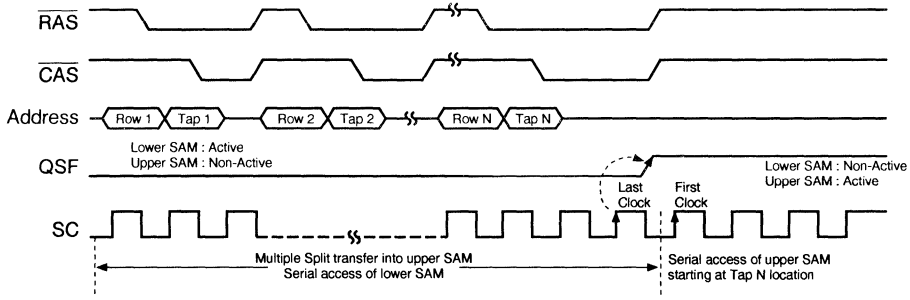


Tap Location Selection in Split Transfer Operation

a. In a split transfer operation, column addresses A0C through A6C must be latched at the falling edge of CAS in order to set the tap location in one of the split SAM registers. During a split transfer, column address A7C is controlled internally and therefore it is ignored internally at the falling edge of CAS. During a split transfer, it is not allowed to set the last address location (A0C–A6C = 7F), in either the lower SAM or the upper SAM, as the tap location.



b. In the case of multiple split transfers performed into the same split SAM register, the tap location specified during the last split transfer, before QSF toggles, will prevail. In the example shown below, multiple split transfers are performed into the upper SAM (non-active) while the lower SAM (active) is being accessed at the time when QSF toggles, the first SC serial clock will start shifting serial data starting from the Tap N address location.



3

Split Read/Write Transfer Operation Allowable Period

Figure 26 illustrates the relationship between the serial clock SC and the special function output QSF during split read/write transfers and highlights the time periods where split transfers are allowed, relative to SC and QSF. As indicated in Figure 26, a split read/write transfer is not allowed during the period of $t_{STH} + t_{STS}$.

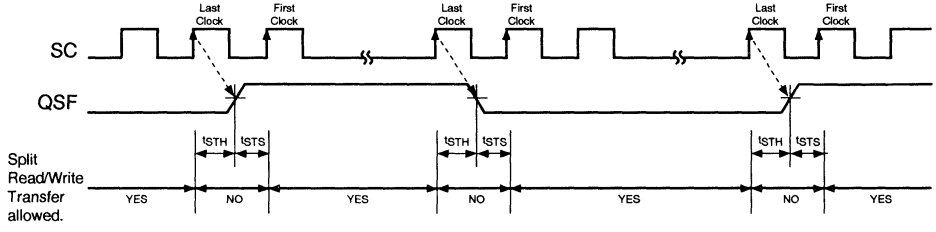
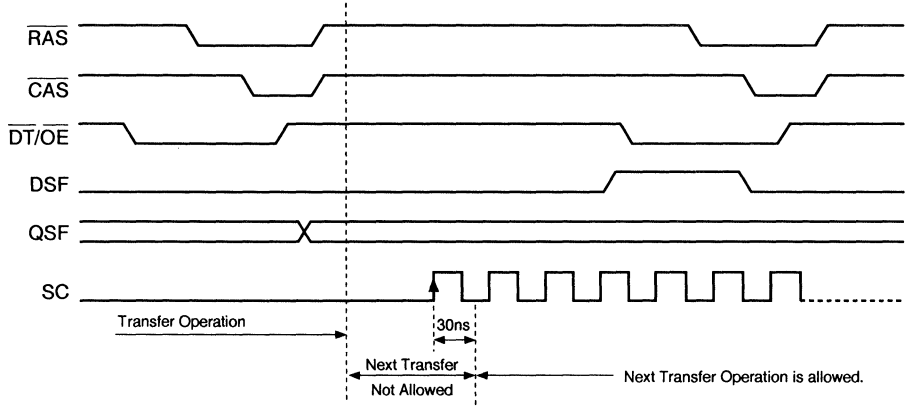


Figure 26. Split Transfer Operation Allowable Periods

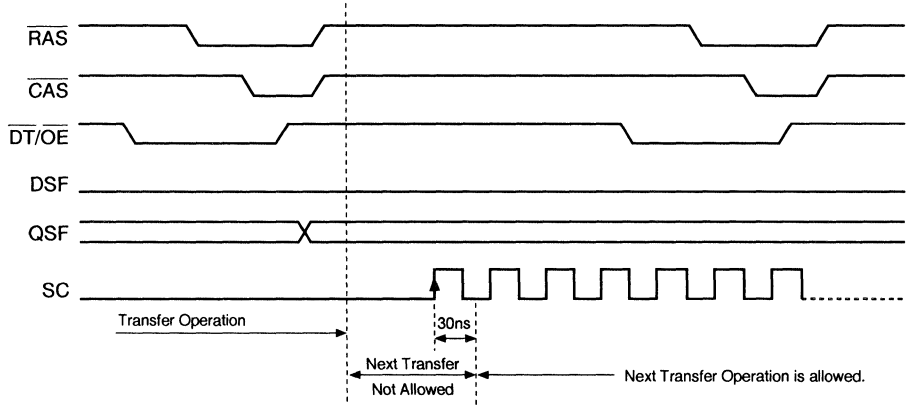
Split Transfer Cycle After Normal Transfer Cycle

A split transfer may be performed following a normal transfer (Read/Write/Pseudo-Write transfer) provided that a minimum delay of 30ns from the rising edge of the first clock SC is satisfied (refer to the illustration shown below).



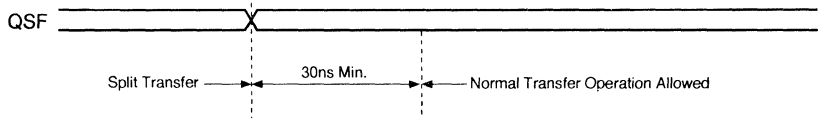
Normal Read Transfer Cycle After Normal Read Transfer Cycle

Another read transfer may be performed following the read transfer provided that a minimum delay of 30 ns from the rising edge of the first clock SC is satisfied (refer to the illustration shown below).



Normal Transfer After Split Transfer

A normal transfer (read/write/psuedo write) may be performed following split transfer operation provided that a 30ns minimum delay is satisfied after the QSF signal toggles.



Power-Up

Power must be applied to the $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ input signals to pull them "high" before or at the same time as the V_{DD} supply is turned on. After power-up, a pause of 200 μseconds minimum is required with $\overline{RAS}$ and $\overline{DT}/\overline{OE}$ held "high". After the pause, a minimum of 8 $\overline{RAS}$ and 8 SC dummy cycles must be performed to stabilize the internal circuitry, before valid read, write or transfer operations can begin. During the initialization period, the $\overline{DT}/\overline{OE}$ signal must be held "high". If the internal refresh counter is used, a minimum 8 $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of 8 $\overline{RAS}$ cycles.

Initial State After Power-Up

When power is achieved with $\overline{RAS}$, $\overline{CAS}$, $\overline{DT}/\overline{OE}$ and $\overline{WB}/\overline{WE}$ held "high", the internal state of the V52C8128 is automatically set as follows.

However, the initial state can not be guaranteed for various power-up conditions and input signal levels. Therefore, it is recommended that the initial state be set after the initialization of the device is performed (200 μs pause followed by a minimum of 8 $\overline{RAS}$ cycles and 8 SC cycles) and before valid operations begin.

	State after power-up
SAM port	Input Mode
QSF	High-Impedance
Color Register	all "0"
WM1 Register	Write Enable
TAP pointer	Invalid

MULTIPORT VIDEO RAM WITH 256K X 8 DRAM AND 512 X 8 SAM

HIGH PERFORMANCE V52C8254	60	70	80
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	25 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns	40 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	140 ns	150 ns
Max. Serial Access Time, (t_{SCA})	17 ns	17 ns	20 ns
Min. Serial Port Cycle Time, (t_{SCC})	22 ns	22 ns	25 ns

Features

- Organization
  - RAM Port: 262,144 words x 8 bits
  - SAM Port: 512 words x 8 bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write
  - Nibble (4 bit) Write
  - Non-Persistent Write-Per-Bit
  - Block Write/Flash Write
  - 512 Refresh Cycles/8 ms
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
- RAM-SAM Bidirectional Transfer
  - Read/Write Transfer
  - Split Read/Write Transfer
- Low CMOS Standby Current – 10 mA
- Package
  - 40 pin 400 mil SOJ

Description

The V52C8254 VRAM is organized as 262,144-words by 8-bits dynamic random access memory (RAM) port and a 512-words by 8-bits static serial access memory (SAM) port. The V52C8254 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

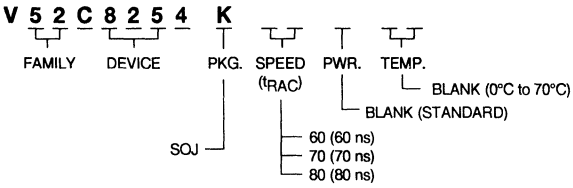
In addition to the conventional multiport video RAM operating modes, the V52C8254 features the nibble write mode, split read/write transfer and block/flash write mode.

The V52C8254 is fabricated in CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

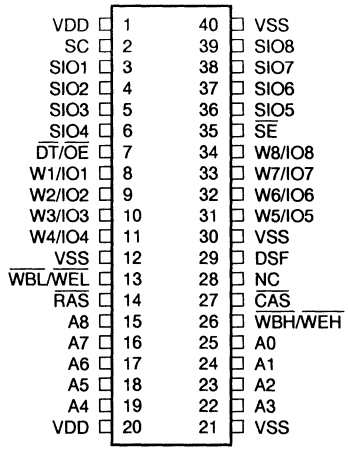
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)			Power	Temperature
	K	60	70	80	Std	Mark
0°C–70°C	•	•	•	•	•	Blank

Description	Pkg.	Pin Count
SOJ	K	40



40 Lead Pin Configuration



K – SOJ

Pin Names

Name	Description
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{WBL/WEL}$	Write per Bit/Write Enable (lower 4 bits)
$\overline{WBH/WEH}$	Write per Bit/Write Enable (higher 4 bits)
DSF	Special Function Control
W1/IO1-W8/IO8	Write Mask/Data In, Out
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1-SIO8	Serial Input/Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF
C_{OUT}	Output Capacitance (QSF)		9	pF

*Note: Capacitance is sampled and not 100% tested.

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 to +7.0 V
Short Circuit Out Current ..... 50 mA
Power Dissipation ..... 1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

MULTIPORT VIDEO RAM WITH 256K X 8 DRAM AND 512 X 8 SAM

HIGH PERFORMANCE V52C8255	60	70	80
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	25 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns	40 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	140 ns	150 ns
Max. Serial Access Time, (t_{SCA})	17 ns	17 ns	20 ns
Min. Serial Port Cycle Time, (t_{SCC})	22 ns	22 ns	25 ns

Features

- Organization
  - RAM Port: 262,144 words x 8 bits
  - SAM Port: 512 words x 8 bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write
  - Non-Persistent Write-Per-Bit
  - Block Write/Flash Write
  - 512 Refresh Cycles/8 ms
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
- RAM-SAM Bidirectional Transfer
  - Read/Write Transfer
  - Split Read/Write Transfer
- Low CMOS Standby Current – 10 mA
- Package
  - 40 pin 400 mil SOJ

Description

The V52C8255 VRAM is organized as 262,144-words by 8-bits dynamic random access memory (RAM) port and a 512-words by 8-bits static serial access memory (SAM) port. The V52C8255 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

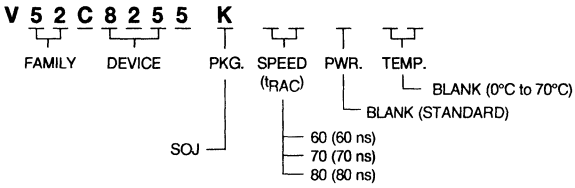
In addition to the conventional multiport video RAM operating modes, the V52C8255 features the block write and flash write functions on the RAM port and a split read/write data transfer capability on the SAM port.

The V52C8255 is fabricated in CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

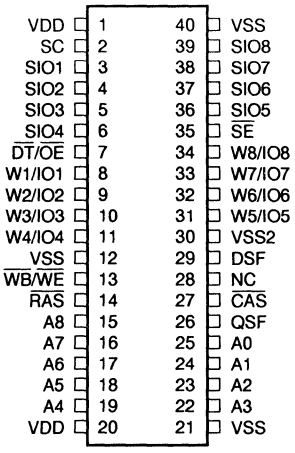
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)			Power	Temperature
	K	60	70	80	Std	Mark
0°C–70°C	•	•	•	•	•	Blank

Description	Pkg.	Pin Count
SOJ	K	40



40 Lead Pin Configuration



K – SOJ

Pin Names

Name	Description
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{WB/WE}$	Write per Bit/Write Enable
DSF	Special Function Control
W1/IO1-W8/IO8	Write Mask/Data In, Out
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1-SIO8	Serial Input/Output
QSF	Special Flag Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF
C_{OUT}	Output Capacitance (QSF)		9	pF

*Note: Capacitance is sampled and not 100% tested.

Absolute Maximum Ratings*

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage Relative to V_{SS} .....–1.0 to +7.0 V
Short Circuit Out Current .....50 mA
Power Dissipation .....1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

MULTIPORT VIDEO RAM WITH 256K X 8 DRAM AND 512 X 8 SAM

HIGH PERFORMANCE V52C8256	60	70	80
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	25 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns	40 ns
Min. Hyper Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	140 ns	150 ns
Max. Serial Access Time, (t_{SCA})	17 ns	17 ns	20 ns
Min. Serial Port Cycle Time, (t_{SCC})	22 ns	22 ns	25 ns

Features

- Organization
  - RAM Port: 262,144 words x 8 bits
  - SAM Port: 512 words x 8 bits
- RAM Port
  - Hyper Page Mode (with extended Data Out)
  - Persistent Mask Write
  - Block Write/Flash Write
  - 512 Refresh Cycles/8 ms
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
  - Programmable Split SAM
- RAM-SAM Bidirectional Transfer
  - Read/Write Transfer
  - Split Read/Write Transfer
- Low CMOS Standby Current – 10 mA
- Package
  - 40 pin 400 mil SOJ

Description

The V52C8256 VRAM is organized as 262,144-words by 8-bits dynamic random access memory (RAM) port and a 512-words by 8-bits static serial access memory (SAM) port. The V52C8256 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

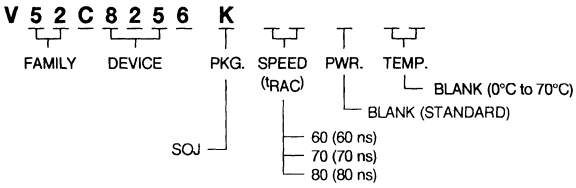
In addition to the conventional multiport video RAM operating modes, the V52C8256 features the persistent mask write, programmable SAM, block/flash write and split read/write transfer.

The V52C8256 is fabricated in CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

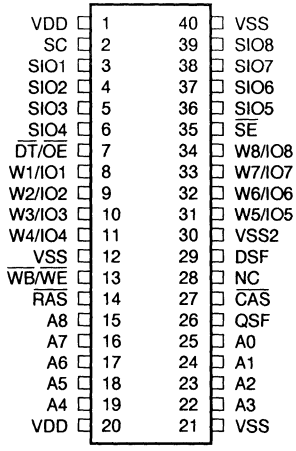
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)			Power	Temperature Mark
	K	60	70	80	Std	
0°C–70°C	•	•	•	•	•	Blank

Description	Pkg.	Pin Count
SOJ	K	40



40 Lead Pin Configuration



K – SOJ

Pin Names

Name	Description
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{WB/WE}$	Write per Bit/Write Enable
DSF	Special Function Control
W1/IO1-W8/IO8	Write Mask/Data In, Out
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1-SIO8	Serial Input/Output
QSF	Special Flag Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

3

Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF
C_{OUT}	Output Capacitance (QSF)		9	pF

*Note: Capacitance is sampled and not 100% tested.

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 to +7.0 V
Short Circuit Out Current ..... 50 mA
Power Dissipation ..... 1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

MULTIPORT VIDEO RAM WITH 256K X 8 DRAM AND 512 X 8 SAM

HIGH PERFORMANCE V52C8258	60	70	80
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. $\overline{CAS}$ Access Time, (t_{CAC})	15 ns	20 ns	25 ns
Max. Column Address Access Time, (t_{AA})	30 ns	35 ns	40 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	140 ns	150 ns
Max. Serial Access Time, (t_{SCA})	17 ns	17 ns	20 ns
Min. Serial Port Cycle Time, (t_{SCC})	22 ns	22 ns	25 ns

Features

- Organization
  - RAM Port: 262,144 words x 8 bits
  - SAM Port: 512 words x 8 bits
- RAM Port
  - Fast Page Mode, Read-Modify-Write
  - Persistent Mask Write
  - Block Write/Flash Write
  - 512 Refresh Cycles/8 ms
  - $\overline{CAS}$-before-$\overline{RAS}$ Refresh, Hidden Refresh, $\overline{RAS}$-only Refresh
- SAM Port
  - High Speed Serial Read/Write Capability
  - 512 Tap Locations
  - Programmable Split SAM
- RAM-SAM Bidirectional Transfer
  - Read/Write Transfer
  - Split Read/Write Transfer
- Low CMOS Standby Current – 10 mA
- Package
  - 40 pin 400 mil SOJ

Description

The V52C8258 VRAM is equipped with a 262,144-words by 8-bits dynamic random access memory (RAM) port and a 512-words by 8-bits static serial access memory (SAM) port. The V52C8258 supports three types of operations: random access to and from the RAM port, high speed serial access to and from the SAM port, and bidirectional transfer of data between any selected row in the RAM port and the SAM port. The RAM port and the SAM port can be accessed independently except when data is being transferred between them internally.

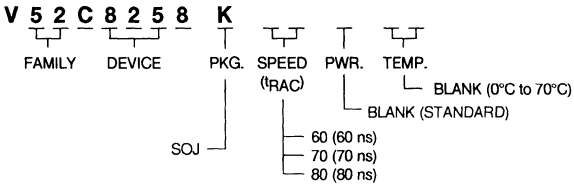
In addition to the conventional multiport video RAM operating modes, the V52C8258 features the persistent mask write, programmable split SAM and split read/write transfer.

The V52C8258 is fabricated in CMOS silicon gate process as well as advanced circuit designs to provide low power dissipation and wide operating margins.

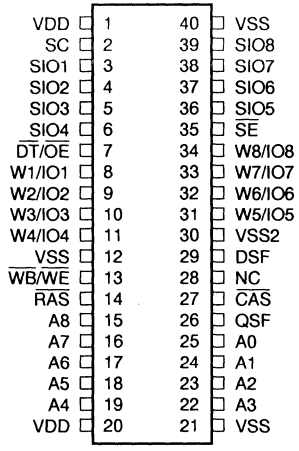
Device Usage Chart

Operating Temperature Range	Package Outline	Access Time (ns)			Power	Temperature
	K	60	70	80	Std	Mark
0°C–70°C	•	•	•	•	•	Blank

Description	Pkg.	Pin Count
SOJ	K	40



40 Lead Pin Configuration



K – SOJ

Pin Names

Name	Description
A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{DT/OE}$	Data Transfer/Output Enable
$\overline{WB/WE}$	Write per Bit/Write Enable
DSF	Special Function Control
W1/IO1-W8/IO8	Write Mask/Data In, Out
SC	Serial Clock
$\overline{SE}$	Serial Enable
SIO1-SIO8	Serial Input/Output
QSF	Special Flag Output
VDD/VSS	Power (5V)/Ground
NC	No Connection

Capacitance*

T_A = 25°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, f = 1MHz

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance		7	pF
$C_{IN/OUT}$	Input/Output Capacitance		9	pF
C_{OUT}	Output Capacitance (QSF)		9	pF

*Note: Capacitance is sampled and not 100% tested.

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to V_{SS} ..... −1.0 to +7.0 V
Short Circuit Out Current ..... 50 mA
Power Dissipation ..... 1 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

V100J9 and V100J8
1M X 9, 1M X 8 BIT FAST PAGE MODE
CMOS DYNAMIC RAM MEMORY MODULE

HIGH PERFORMANCE V100J8/9	60/60L	70/70L	80/80L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	40 ns	45 ns	50 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns	150 ns

LOW POWER V100J8/9L	60L	70L	80L
Max. CMOS Standby Current, (I_{DD6})	1.6/1.8 mA	1.6/1.8 mA	1.6/1.8 mA

Features

- 1M x 8 (or x 9)-bit organization
- Utilizes eight or nine 1M x 1 CMOS RAMs
- RAS access time: 60, 70, 80 ns
- Low power dissipation
  - V100J8/9-80
    - — Operating Current – 560/630 mA max.
    - — TTL Standby Current – 18 mA max.
- Low CMOS Standby Current
  - V100J8/9 – 8/9 mA max.
  - V100J8/9L – 1.6/1.8 mA max.
- Battery Back-up Mode (V100J8/9L Only)
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V100J8/9 – 512 cycles/8 ms
  - V100J8/9L – 512 cycles/64 ms
- Fast Page Mode for a sustained data rate greater than 25 MHz
- Available in standard 30-lead single-in-line module

Description

The V100J8/9 are high speed 1,048,576 x 8/9 bit CMOS dynamic random access memory modules. The V100J8/9 offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V100J8/9L).

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 1024 bits within a row with cycle times as short as 40 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V100J8/9L ideally suited for high performance computing systems.

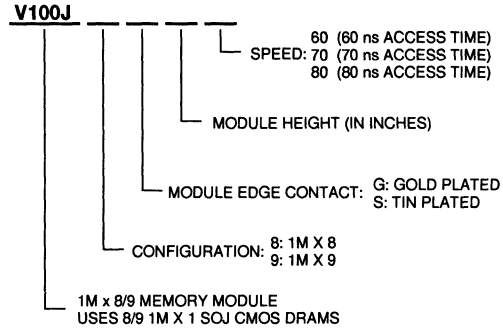
The V100J8/9L offer a maximum data retention power of 13.2/14.85 mW when operating in CMOS standby mode and performing $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

4

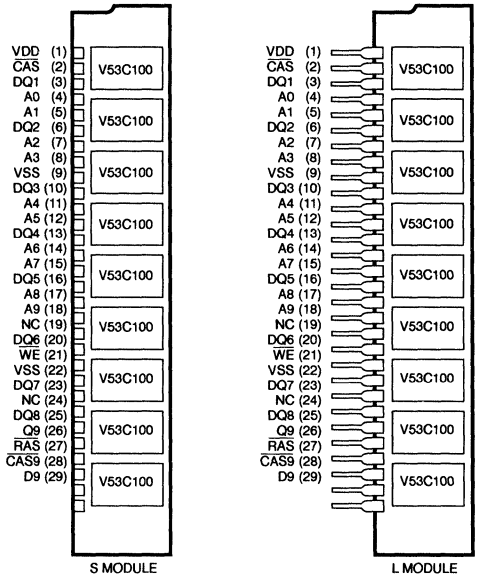
Device Usage Chart

Operating Temperature Range	Bit Organization		Module Type		Access Time (ns)			Power	
	x 8	x 9	S	L	60	70	80	Std	Low
0°C–70°C	•	•	•	•	•	•	•	•	•

Part Number Information



Pin Configuration x 9 Organization



NOTE: *x 8 Organization*
Pins 26, 28, 29 are not connected

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage on any pin Relative to V_{SS} ... −1.0 to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 9.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Pin Names (x 9 Organization)

Name	Description
A0–A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobes
$\overline{WE}$	Write Enable
DQ1–DQ8	Data In/Data Out
D9	Data In
Q9	Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

x 8 Organization
$\overline{CAS9}$, D9, Q9 are not connected

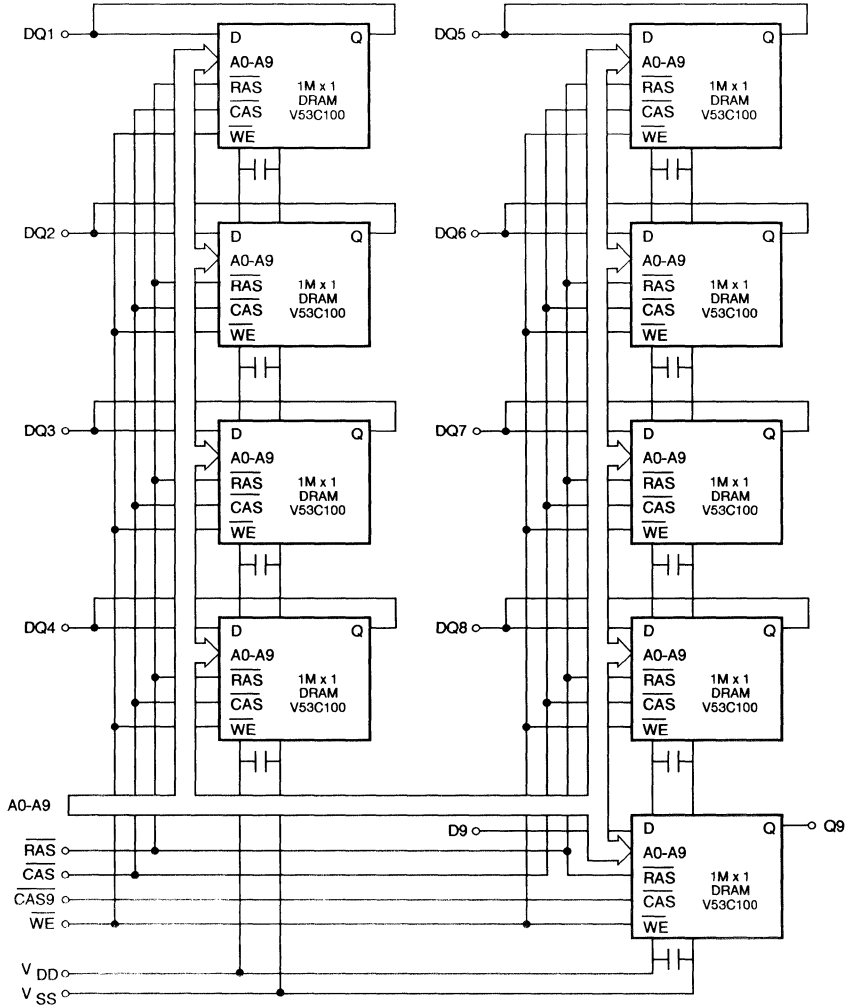
Capacitance* (x9 Organization)

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		70	pF
C_{IN}	Input Capacitance, $\overline{RAS}$, $\overline{WE}$		75	pF
$C_{IN(DQ)}$	Data Input/Output Capacitance, DQ1-DQ8		20	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS}$		75	pF
$C_{IN(CAS9)}$	Input Capacitance, $\overline{CAS9}$		10	pF
$C_{IN(D9)}$	Input Capacitance, D9		10	pF
$C_{O(Q9)}$	Output Capacitance, Q9		15	pF

*Note: Capacitance is sampled and not 100% tested.

Functional Diagram *x 9 Organization*



NOTE: ***x 8 Organization***
CAS9, D9, Q9 are not connected

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DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Power	Access Time	V100J8 Min.	V100J8 Max.	V100J9 Min.	V100J9 Max.	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)			–80	80	–90	90	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)			–10	10	–10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		60		720		810	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
			70		640		720			
			80		560		630			
I_{DD2}	V_{DD} Supply Current, TTL Standby				16		18	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh		60		720		810	mA	$t_{RC} = t_{RC}$ (min.)	2
			70		640		720			
			80		560		630			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		60		640		720	mA	Minimum Cycle	1, 2
			70		560		630			
			80		480		540			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			24		27	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	
		LOW			16		18			
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD			8		9	mA	$\overline{RAS} \ge V_{DD} - 0.2$ V $\overline{CAS} \ge V_{DD} - 0.2$V other inputs ≥ V_{SS}	
		LOW			1.6		1.8			
I_{DD7}	Battery Back-up Data Retention Current (Only V100J8/9L)	LOW			2.4		2.7	mA	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle t_{RC} = 125 µs CMOS clock levels	18
V_{IL}	Input Low Voltage			–1.0	0.8	–1.0	0.8	V		3
V_{IH}	Input High Voltage			2.4	V_{DD}+1	2.4	V_{DD}+1	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage			2.4		2.4			I_{OH} = –5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	ns	
2	t_{RL2RL}	t_{RC}	Read or Write Cycle Time	120		130		150		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		ns	
4	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
5	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		10		ns	
6	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		40		ns	
7	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	ns	4
8	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
9	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		ns	
10	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	45	20	50	20	60	ns	5
11	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80	ns	6,7,8
12	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40	ns	8,9,15
13	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		15		20		20	ns	8,15
14	$t_{CL1CH1(R)}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	15	75K	20	75K	20	75K	ns	
15	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15		20		20		ns	
16	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
17	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	10
18	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	10
19	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		ns	
20	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	20	0	20	0	20	ns	11

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AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CH2QV}	t_{OH}	Data Hold Time from $\overline{CAS}$	0		0		0		ns	11
22	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		15		ns	
23	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
24	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
25	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	15		20		20		ns	
26	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	15		20		20		ns	
27	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
28	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12, 13
29	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		15		15		ns	
30	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		ns	14
31	t_{WH1DX}	t_{DH}	Data In Hold Time	15		15		15		ns	14
32	t_{RL1DX}	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	50		55		60		ns	
33	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		35		40		45	ns	15
34	$t_{CL2CL2(R)}$	t_{PC}	Fast Page Mode Read or Write Cycle Time	40		45		50		ns	
35	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		ns	
36	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		ns	
37	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/L		70/L		80/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	30		30		30		ns	
40	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		ns	
41	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	16
42		t_{REF}	Refresh Interval (512 Cycles)		8		8		8	ms	17
43		t_{REF}	Refresh Interval V100J8/9L Only (512 Cycles, t_{RC} = 125 µs)		64		64		64	ms	18

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Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in First Page Mode.
3. Specified V_{IL} (min.) is steady state operation. During transitions, V_{IL} (min.) may undershoot to –1.0 V for periods not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
5. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) and t_{RAD} (max.) limits ensure that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
6. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
8. Measured with a load equivalent to two TTL loads and 100 pF.
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
10. Either t_{RRH} or t_{RCH} must be satisfied for a Read Cycle to occur.
11. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
12. t_{WCS}, t_{WHC}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the later occurance of $\overline{CAS}$ or $\overline{WE}$.
15. Access time is determined by the longer of t_{CAA}, t_{CAC}, or t_{CAP}.
16. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC measurements assume t_T = 5 ns.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

    t_{RC} = 125 µs (125 µs x 512 = 64 ms)

    $t_{RAS} = t_{RAS}$ (min.) to 1 µs

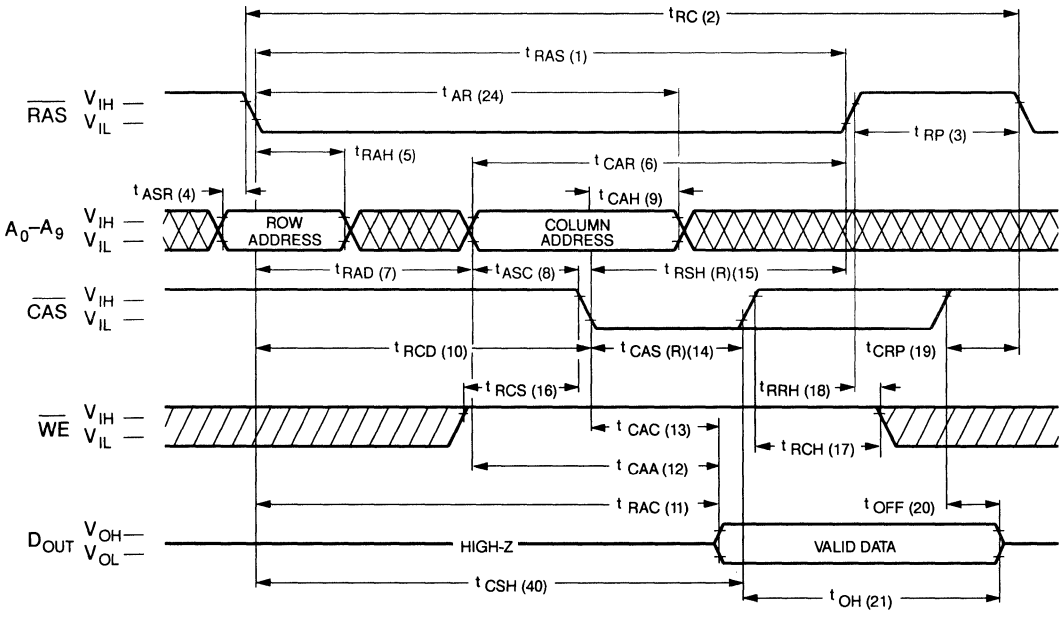
    Input voltages: $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V

    $V_{IL} < 0.2$ V

    $\overline{WE}$ $V_{IN} > V_{DD} - 0.2$ V

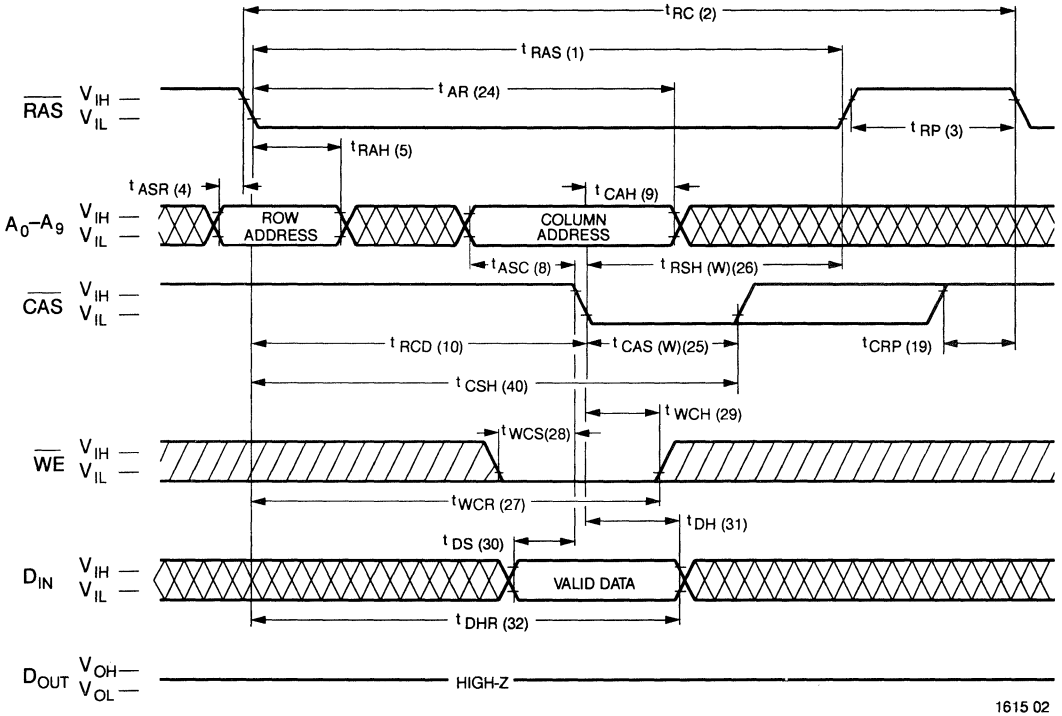
    All other inputs at stable V_{IH} or V_{IL}

Waveforms of Read Cycle



1615 01

Waveforms of Early Write Cycle



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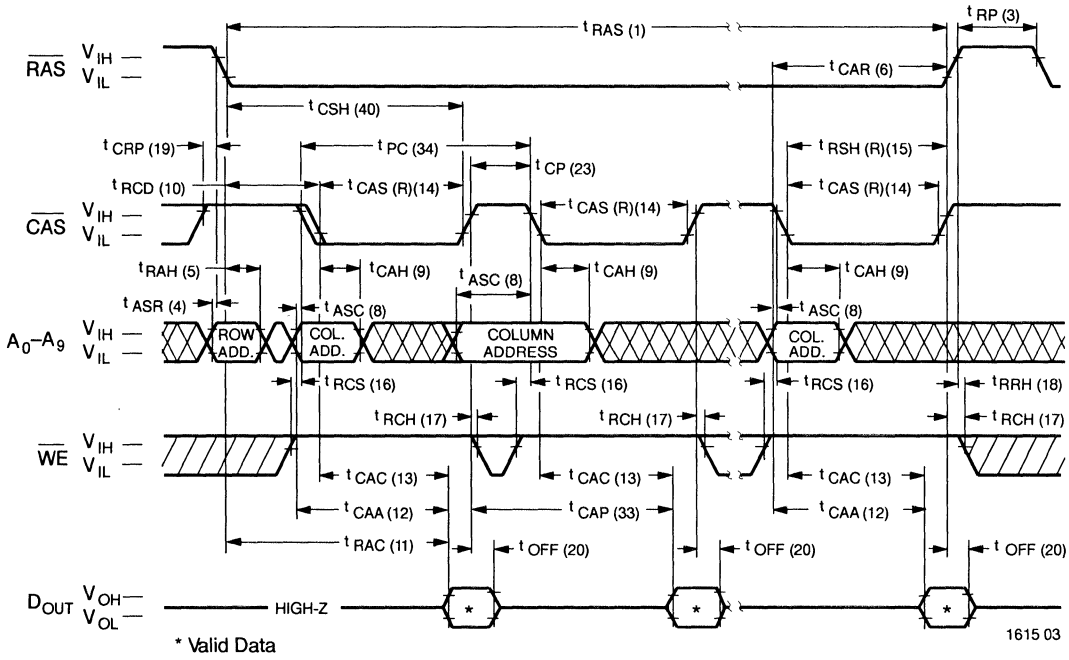
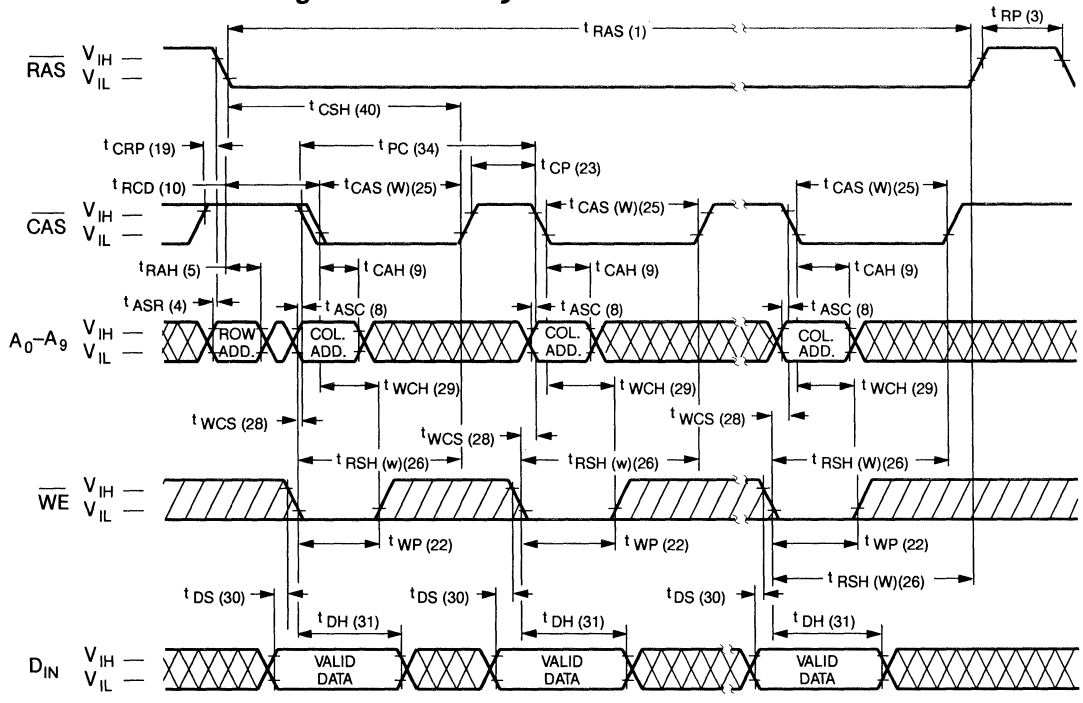
Waveforms of Fast Page Mode Read Cycle

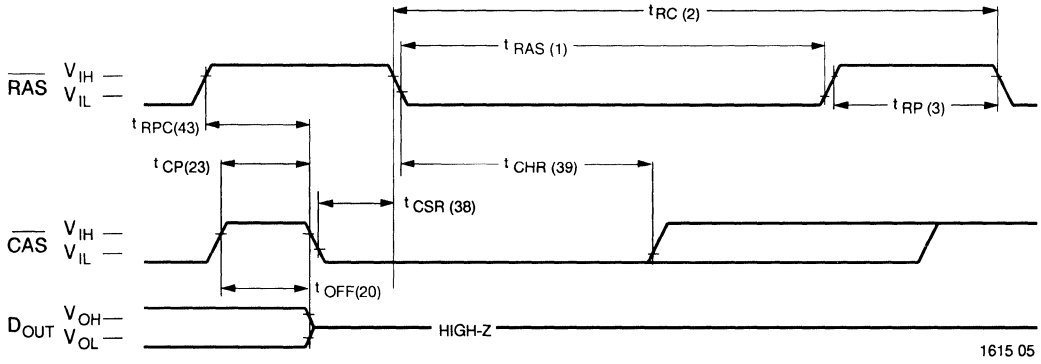


* Valid Data

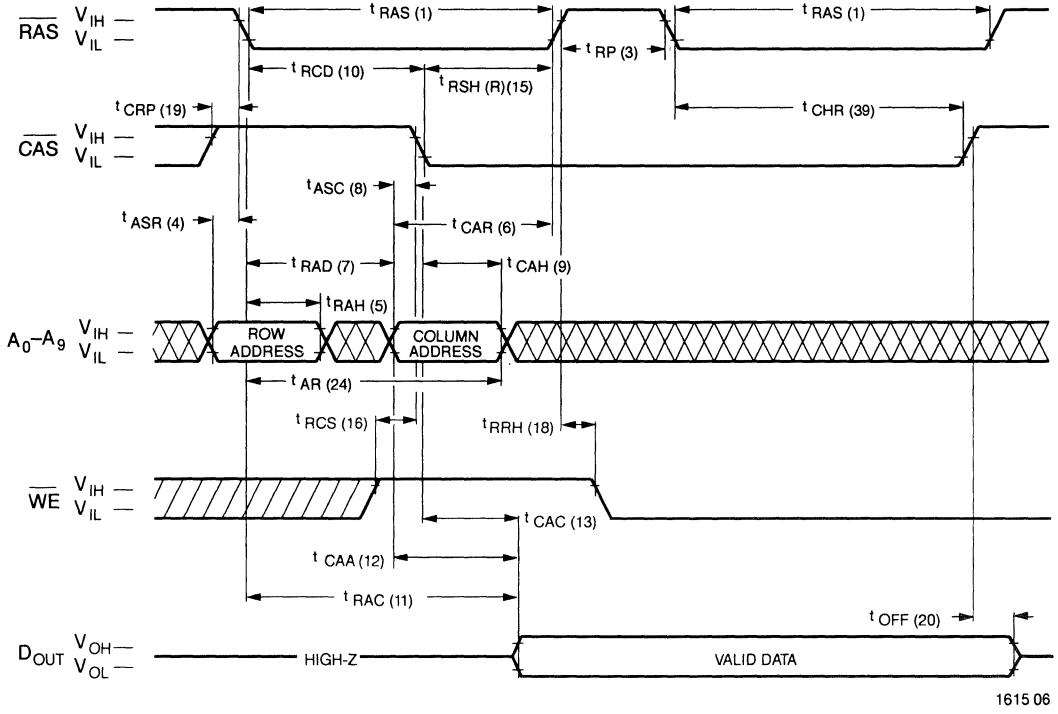
Waveforms of Fast Page Mode Write Cycle



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



Waveforms of Hidden Refresh Cycle (Read)



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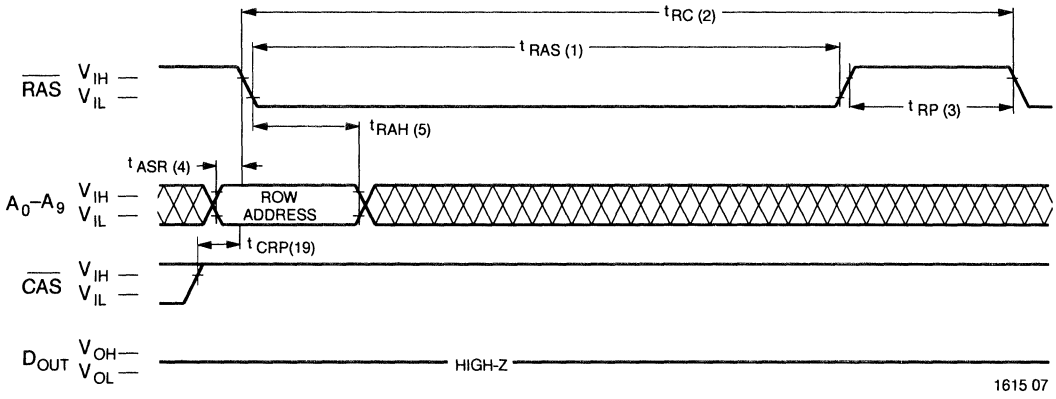
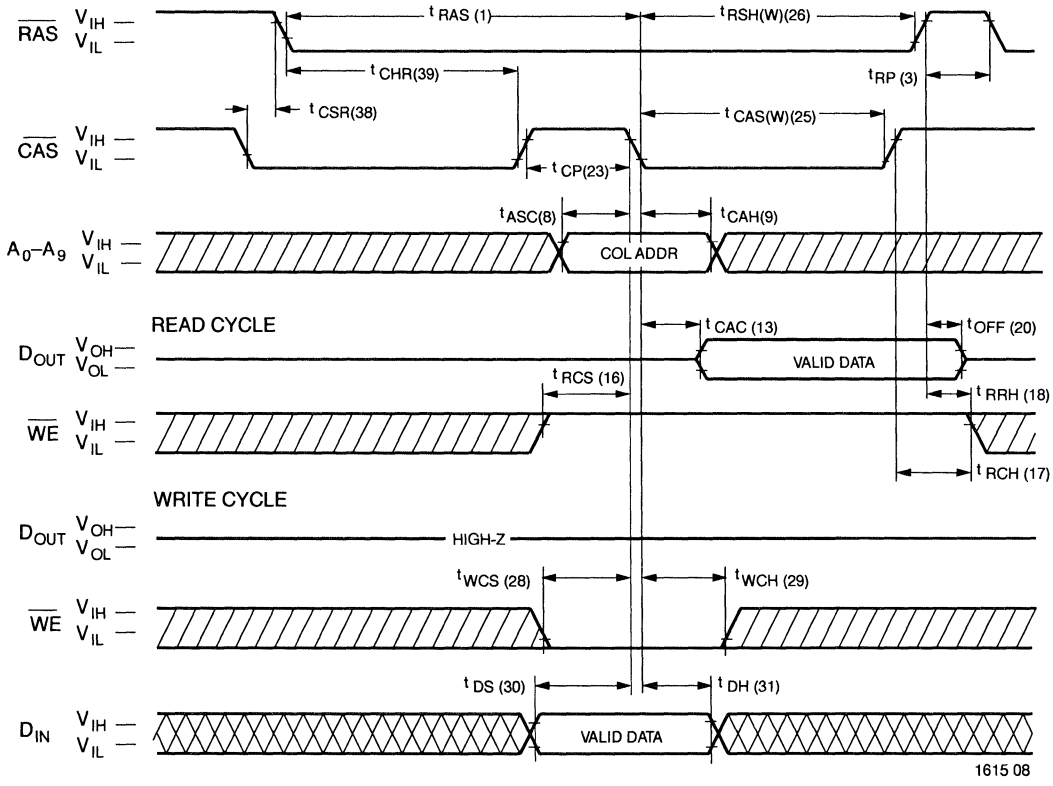
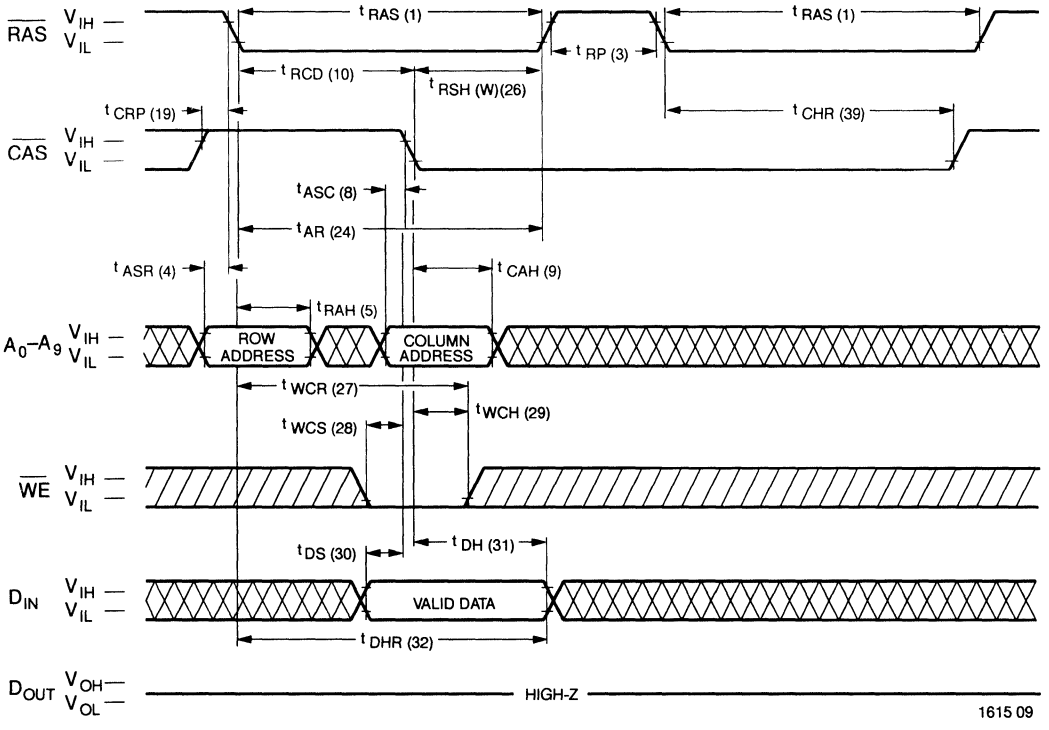
Waveforms of $\overline{RAS}$-Only Refresh Cycle



Waveforms of $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle



Waveforms of Hidden Refresh Cycle (Write)



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MOSEL-VITELIC V104J8/9 (256K x 8, 256K x 9) CMOS MEMORY MODULE

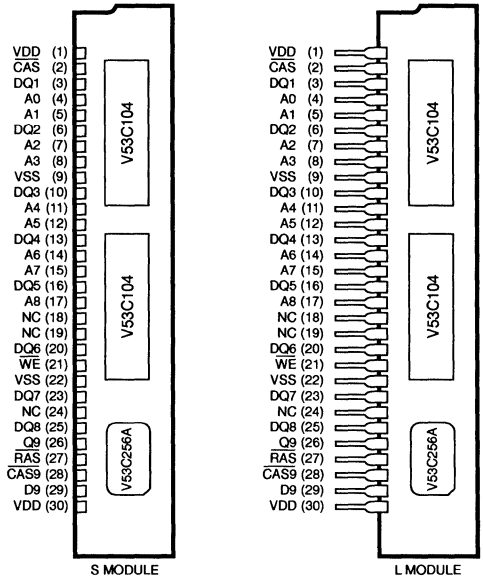
Features

- 262,144 x 8 (or x 9) bit organization
- Utilizes 256K x 4 and 256K x 1 CMOS DRAMs
- Fast Page mode operation
- Fast access times 70 ns, 80 ns and 100 ns
- Low power dissipation
- Common $\overline{CAS}$ control for eight common Data-in and Data-out lines
- Separate $\overline{CAS}$ control for one separate pair of Data-in and Data-out (x 9 organization)
- Single 5 V ±10% supply
- All I/O are fully TTL compatible
- Standard 30-lead single-in-line module

Description

The V104J8/9 Memory Module is organized as 262,144 x 8 (or 9) bits in a 30-lead single-in-line module. The 256K x 8 memory module uses two Vitelic 256K x 4 DRAMs. The 256K x 9 memory module uses two Vitelic 256K x 4 DRAMs and one Vitelic 256K x 1 DRAM. Decoupling capacitors, mounted beneath each package, are surface mounted on the epoxy substrate board. The onboard capacitors eliminate the need for bypassing on the mother board and offer superior performance due to reduced lead inductance.

V104J Pin Configuration x 9 Organization

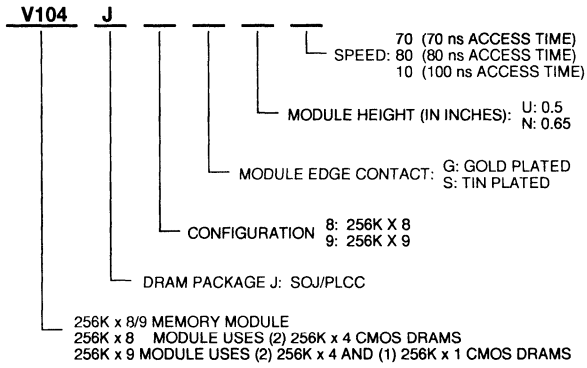


NOTE: *x 8 Organization*
Pins 26, 28, 29 are not connected

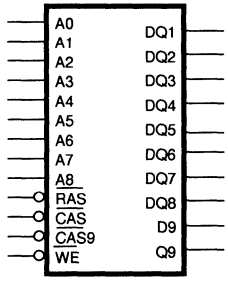
Device Usage Chart

Operating Temperature Range	Bit Organization		Module Type		Access Time (ns)			Power	
	x 8	x 9	S	L	70	80	100	Std	Low
0°C–70°C	•	•	•	•	•	•	•	•	•

Part Number Information



Logic Symbol x 9 Organization



___ x 8 Organization

CAS9, D9, Q9 are not connected

Pin Names (x 9 Organization)

Name	Description
A0–A8	Address Inputs
RAS	Row Address Strobe
CAS, CAS9	Column Address Strobes
WE	Write Enable
DQ1–DQ8	Data In/Data Out
D9	Data In
Q9	Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

___ x 8 Organization

CAS9, D9, Q9 are not connected

Absolute Maximum Ratings*

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} .....–1.0 to +7.0 V
Voltage on V_{DD} relative to V_{SS} .....–1.0 to +7.0 V
Data Out Current .....50 mA
Power Dissipation .....3.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

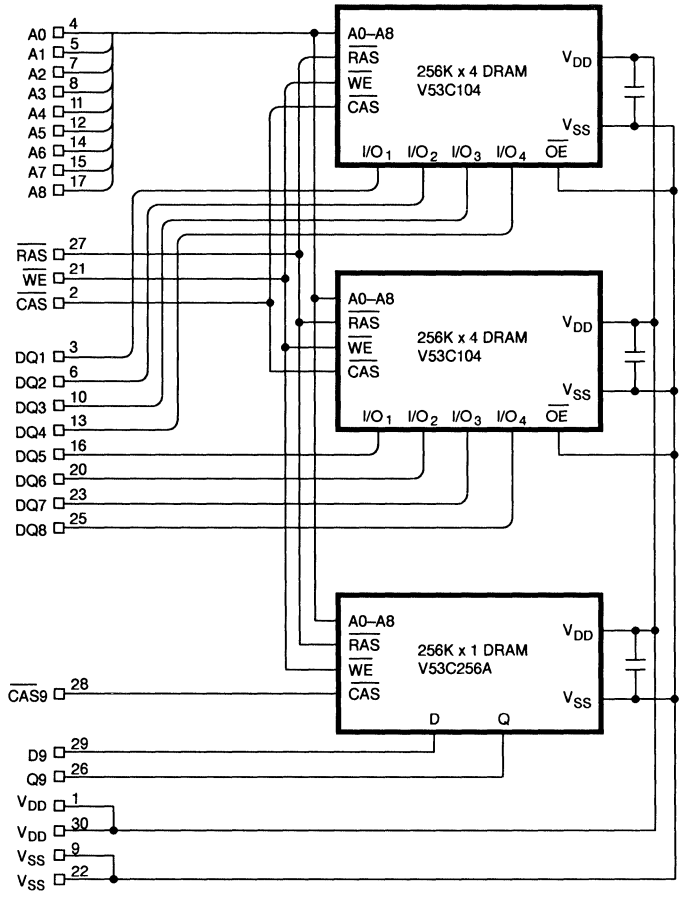
T_A = 0°C TO 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		12	pF
C_{IN}	Input Capacitance, RAS, WE		15	pF
$C_{IN(DQ)}$	Input Capacitance, Data Inputs		14	pF
$C_{IN(CAS)}$	Input Capacitance, CAS		10	pF
$C_{IN(CAS9)}$	Input Capacitance, CAS9		5	pF
$C_{IN(D9)}$	Input Capacitance, D9		4	pF
$C_{O(Q9)}$	Output Capacitance, Q9		6	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.2		µF

*Note: Capacitance is sampled and not 100% tested

Functional Diagram

x 9 Organization



NOTE: *x 8 Organization*
Pins 26, 28, 29 are not connected

DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Power	Access Time (ns)	V104J8		V104J9		Unit	Test Conditions	Notes
				Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)			–20	20	–30	30	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)			–10	10	–10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		70		170		240	mA	$t_{RC} = t_{RC}$ (min.)	1,2
			80		150		210			
			100		130		180			
I_{DD2}	V_{DD} Supply Current, TTL Standby	STD			4		7.5	mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			4		6			
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh		70		170		240	mA	$t_{RC} = t_{RC}$ (min.)	2
			80		150		210			
			100		130		180			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		70		130		175	mA	Minimum Cycle	1,2
			80		110		150			
			100		100		135			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			6		10	mA	$\overline{RAS}$=V_{IH},$\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
		LOW			4		6.5			
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD			2		5	mA	$\overline{RAS} \ge V_{DD}$ –0.2 V, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			2		3.2			
V_{IL}	Input Low Voltage (all inputs)			–1	0.8	–1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)			2.4	VDD +1	2.4	VDD +1	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage			2.4		2.4		V	I_{OH} = –5 mA	

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AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		100/100L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		70		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	25	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		20		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20		25	ns	6,7
17	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	6,8,9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		50	ns	6,7,10
19	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
20	t_{CH2QZ}	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	20	0	20	0	20	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		75		ns	
22	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	11

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		100/100L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		25		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		20		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		20		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		75		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		ns	
30	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		20		ns	14
32	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	75		75		90		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		ns	
34	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55		60		75		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
39	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
40	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		30		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (512 Cycles)		8		8		8	ms	17

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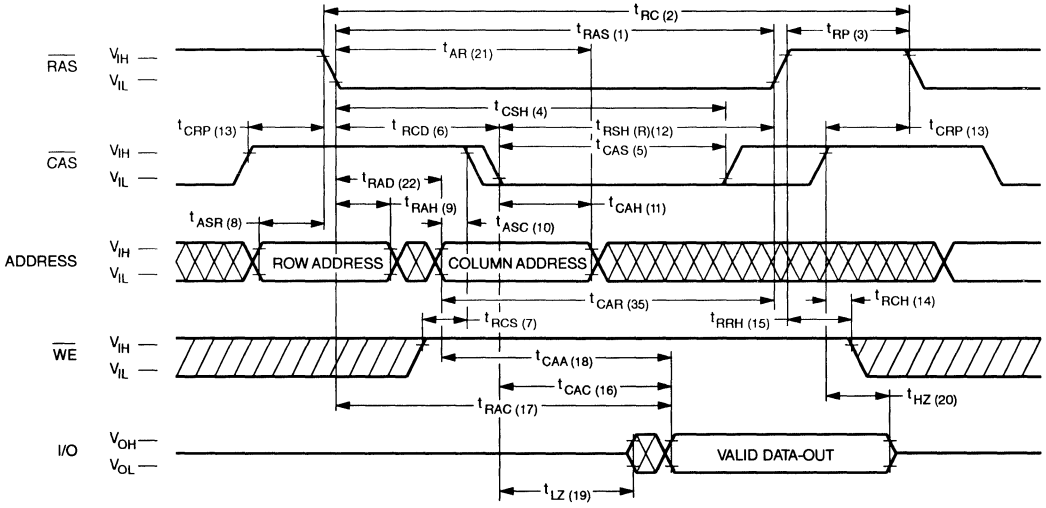
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

Waveforms of Read Cycle



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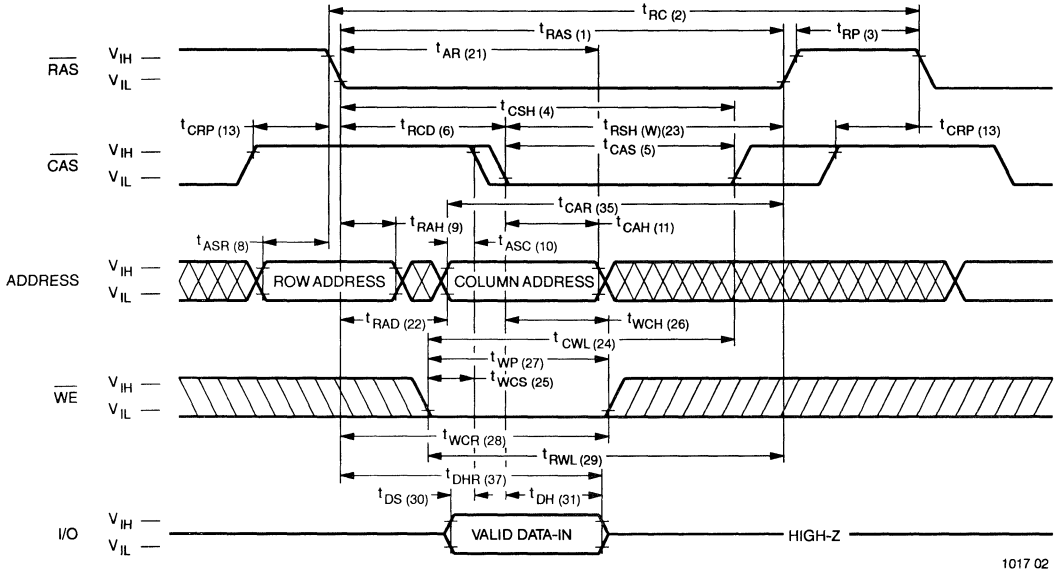
Waveforms of Early Write Cycle



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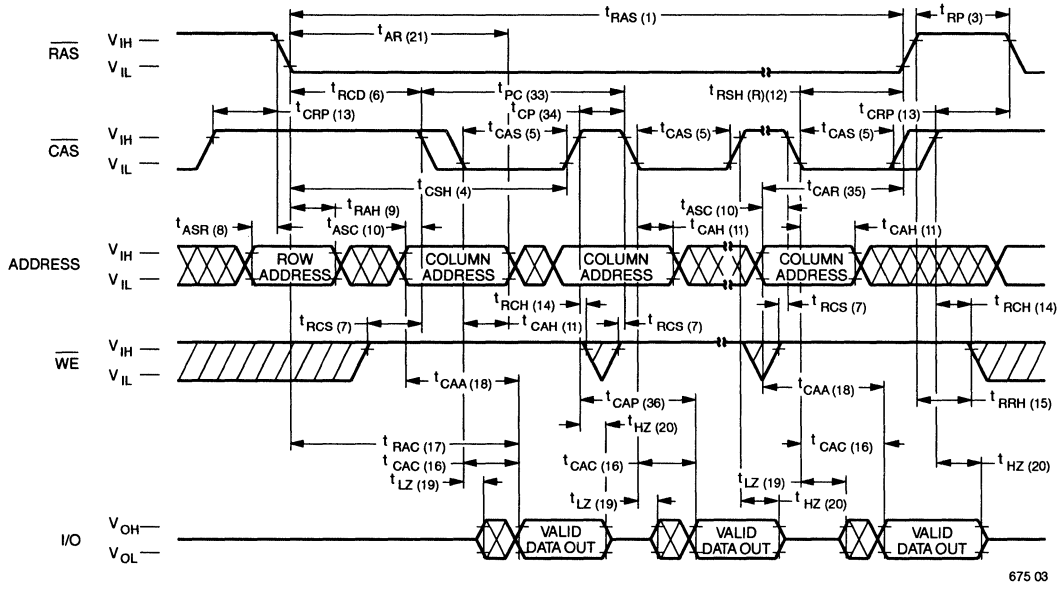
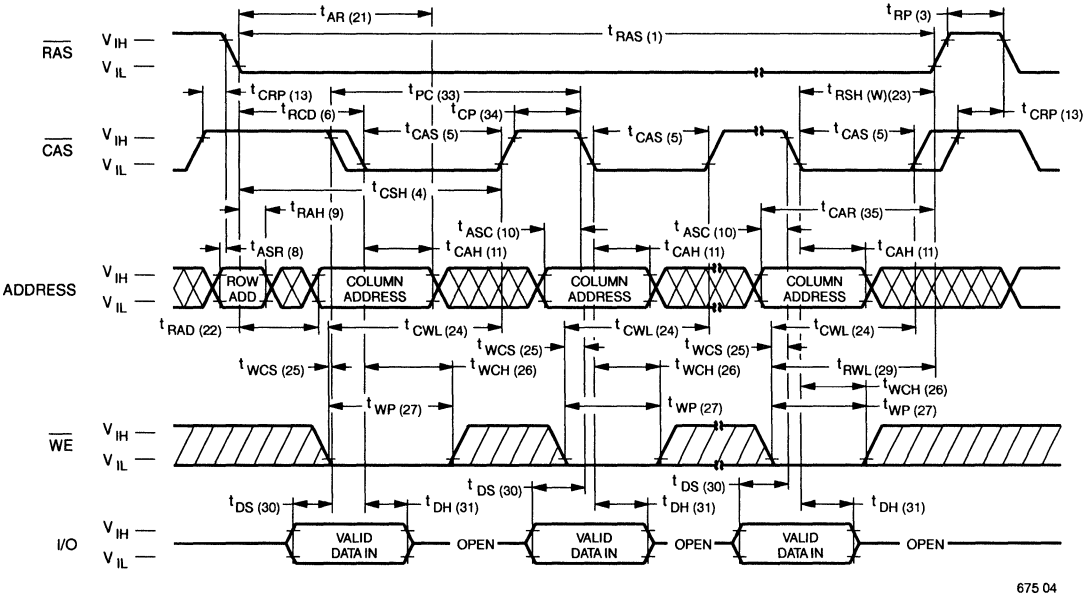
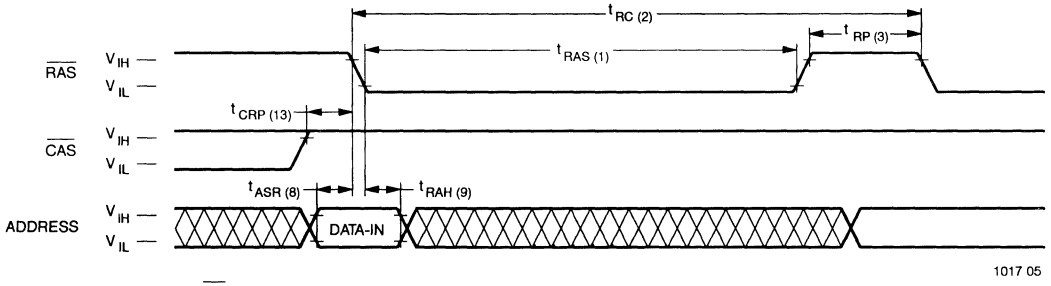
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle

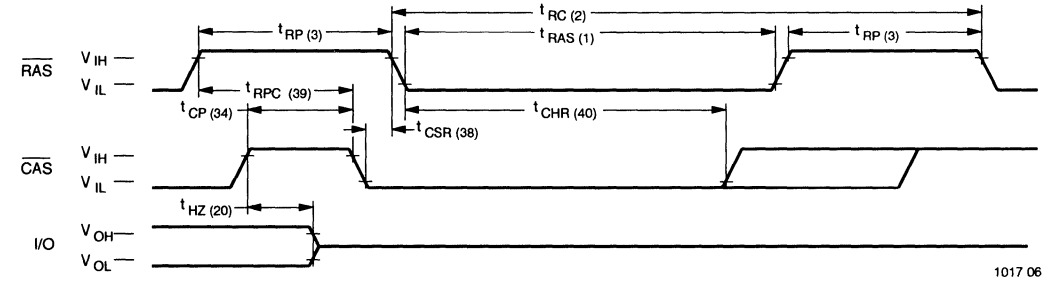


Waveforms of $\overline{RAS}$-Only Refresh Cycle



NOTE: $\overline{WE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



NOTE: $\overline{WE}$, A_0–A_8 = Don't care

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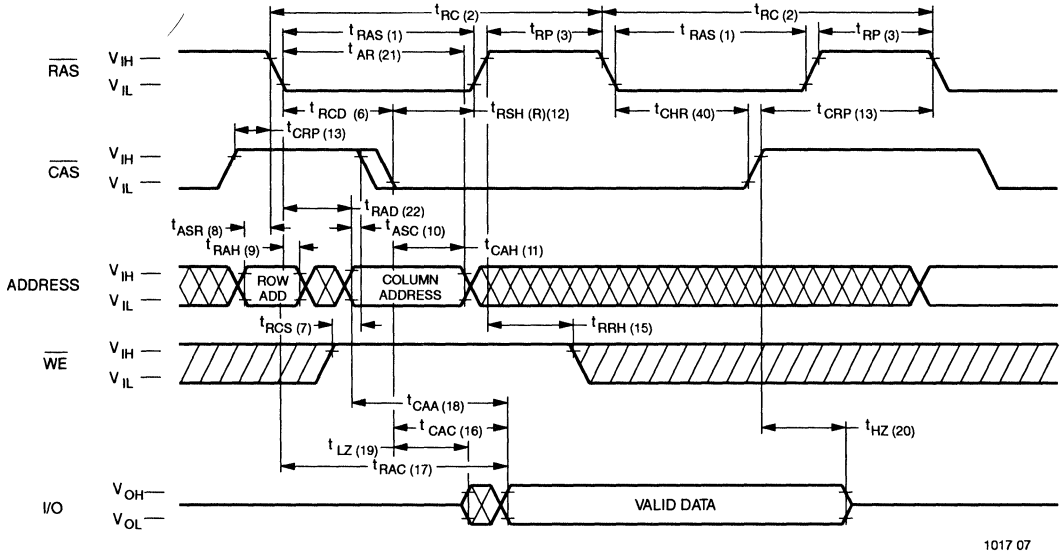
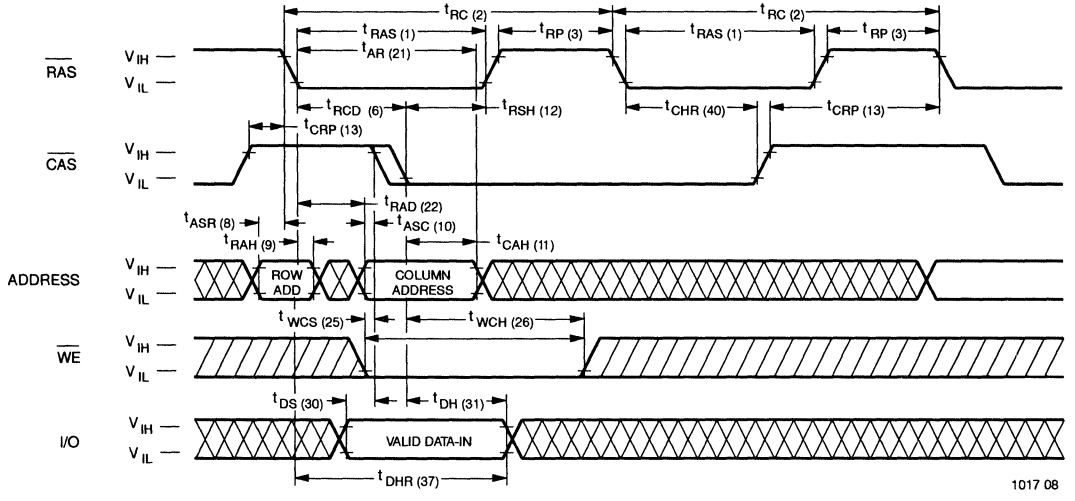
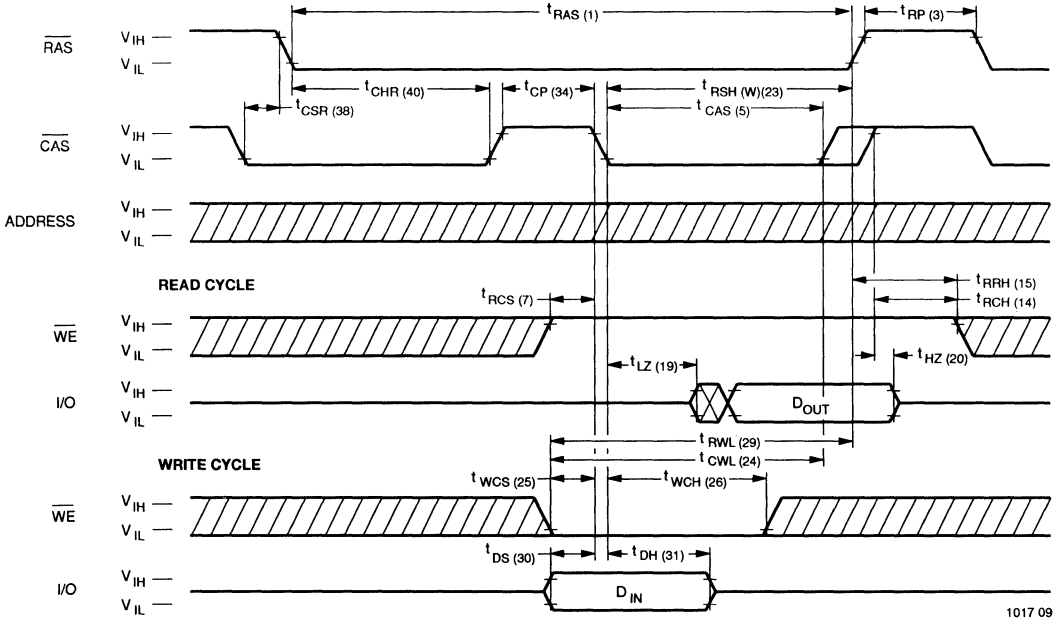
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Refresh Counter Test Cycle



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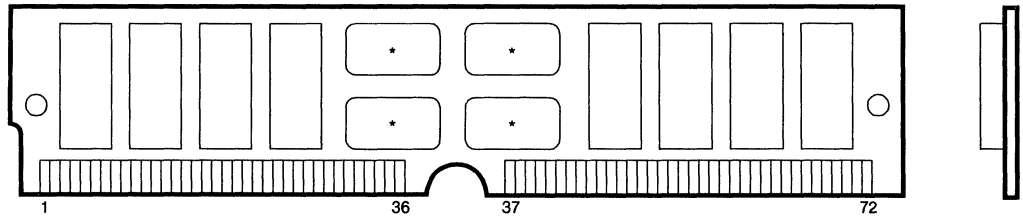
Features

- 262,144 x 32 bit or 262,144 x 36 bit organizations
- Utilizes 256K x 4 and 256K x 1 CMOS DRAMs
- Fast access times 70 ns, 80 ns, 100 ns
- Fast Page mode operation
- Low power dissipation
- CAS before RAS refresh, RAS only refresh, and Hidden refresh capability
- Single 5 V ±10% supply
- All I/O are fully TTL compatible
- Standard 72-lead single-in-line module

Description

The V104J32 Memory Module is organized as 262,144 x 32 bits in a 72-lead single-in-line module. The 256K x 32 memory module uses 8 Mosel-Vitelic 256K x 4 DRAMs. The V104J36 is organized as 262,144 x 36 bits in the 72 lead single-in-line module and uses 8 Mosel-Vitelic 256K x 4 DRAMs and 4 Mosel-Vitelic 256K x 1 DRAMS. The x36 modules are ideal for use in systems where high memory density and parity bits are needed.

V104J32/36
Pin Configuration



*V104J36 Only

1	VSS	16	A4	31	A8	45	NC	59	VDD
2	DQ0	17	A5	32	NC	46	NC	60	DQ32
3	DQ18	18	A6	33	NC	47	$\overline{W}$	61	DQ14
4	DQ1	19	NC	34	$\overline{RAS2}$	48	NC	62	DQ33
5	DQ19	20	DQ4	35	NC [DQ26]	49	DQ9	63	DQ15
6	DQ2	21	DQ22	36	NC [DQ8]	50	DQ27	64	DQ34
7	DQ20	22	DQ5	37	NC [DQ17]	51	DQ10	65	DQ16
8	DQ3	23	DQ23	38	NC [DQ35]	52	DQ28	66	NC
9	DQ21	24	DQ6	39	VSS	53	DQ11	67	*1
10	VDD	25	DQ24	40	$\overline{CAS0}$	54	DQ29	68	*2
11	NC	26	DQ7	41	$\overline{CAS2}$	55	DQ12	69	*3
12	A0	27	DQ25	42	$\overline{CAS3}$	56	DQ30	70	*4
13	A1	28	A7	43	$\overline{CAS1}$	57	DQ13	71	NC
14	A2	29	NC	44	$\overline{RAS0}$	58	DQ31	72	VSS
15	A3	30	VDD						

V104J32/V104J36

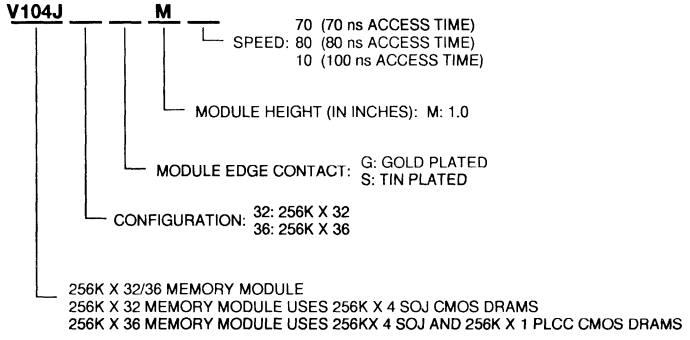
	-70	-80	-10
*1	VSS	VSS	VSS
*2	NC	NC	NC
*3	VSS	NC	VSS
*4	NC	VSS	VSS

* Presence detection. Pin connection change is available on request.

Device Usage Chart

Operating Temperature Range	Organization		Module Type	Access Time (ns)			Power	
	256K x 32	256K x 36	S	70	80	100	Std	Low
0°C–70°C	•	•	•	•	•	•	•	•

Part Number Information



V104J32/36 Pin Names

Name	Description
A0–A8	Address Inputs
$\overline{RAS}$, $\overline{RAS2}$	Row Address Strobes
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobes
$\overline{W}$	Read/Write Input
DQ0–DQ35	Data In/Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... –1.0 to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... –1.0 to +7.0 V
Data Out Current ..... 50 mA
V104J32/36 Power Dissipation ..... 12.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

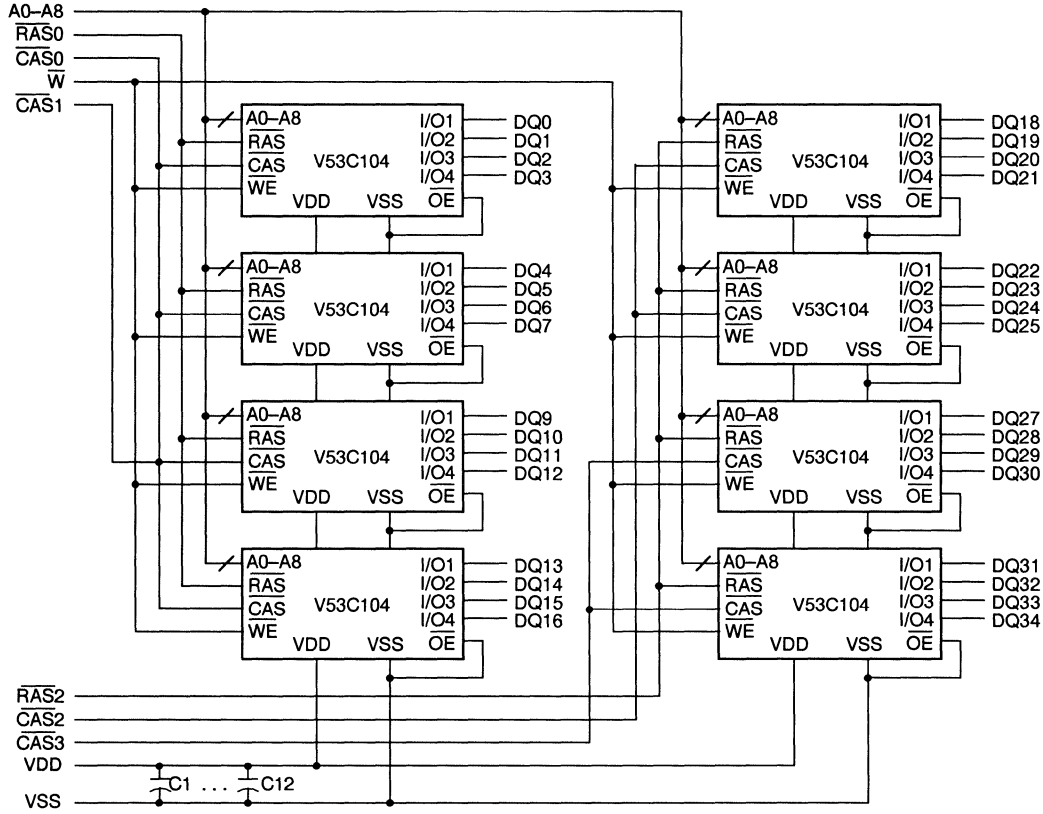
V104J32/36 Capacitance*

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

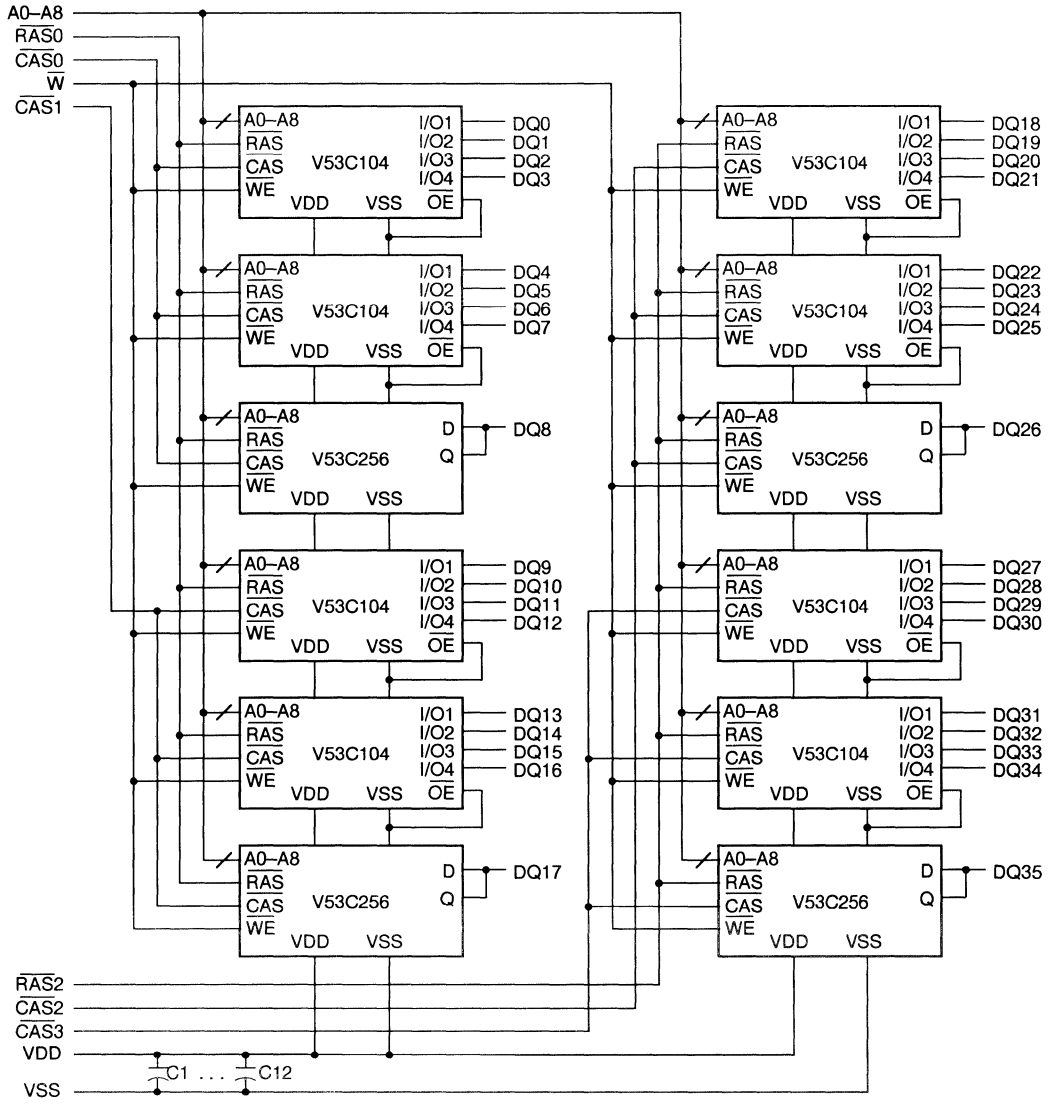
Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		88	pF
C_{IN}	Input Capacitance, $\overline{W}$		104	pF
$C_{IN(DQ)}$	Input Capacitance, Data Inputs		17	pF
$C_{IN(RAS)}$	Input Capacitance, $\overline{RAS0}$, $\overline{RAS2}$		57	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS0}$–$\overline{CAS3}$		36	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.2		µF

*Note: Capacitance is sampled and not 100% tested

V104J32 Functional Diagram



V104J36 Functional Diagram



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DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Power	Access Time (ns)	V104J32		V104J36		Unit	Test Conditions	Notes
				Min.	Max.	Min	Max			
I_{LI}	Input Leakage Current (any input pin)			–80	80	–120	120	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)				10		10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		70		860		960	mA	$t_{RC} = t_{RC}$ (min.)	1,2
			80		760		840			
			100		630		720			
I_{DD2}	V_{DD} Supply Current, TTL Standby	STD			27		30	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			22		24			
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh		70		860		960	mA	$t_{RC} = t_{RC}$ (min.)	2
			80		760		840			
			100		650		720			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		70		630		700	mA	Minimum Cycle	1,2
			80		540		600			
			100		490		570			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			36		40	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
		LOW			23		26			
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD			18		20	mA	$\overline{RAS} \ge V_{DD}$–0.2 V, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			11.5		12.8			
V_{IL}	Input Low Voltage (all inputs)			–1	0.8	–1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)			2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage			2.4		2.4		V	I_{OH} = –5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		70		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	25	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		20		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20		25	ns	6,7
17	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	6,8,9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		45	ns	6,7,10
19	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
20	t_{CH2QZ}	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	20	0	20	0	20	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		75		ns	
22	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	11

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AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		25		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		20		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		20		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		75		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		ns	
30	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		20		ns	14
32	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	75		75		90		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		ns	
34	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55		60		75		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
39	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
40	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		30		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (512 Cycles)		8		8		8	ms	17

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit and are not referenced to the output voltage levels.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

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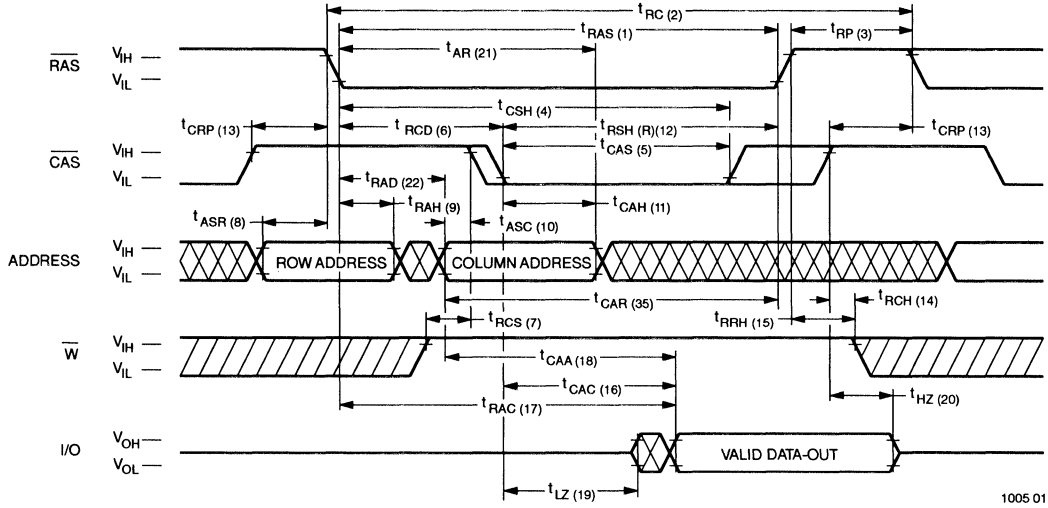
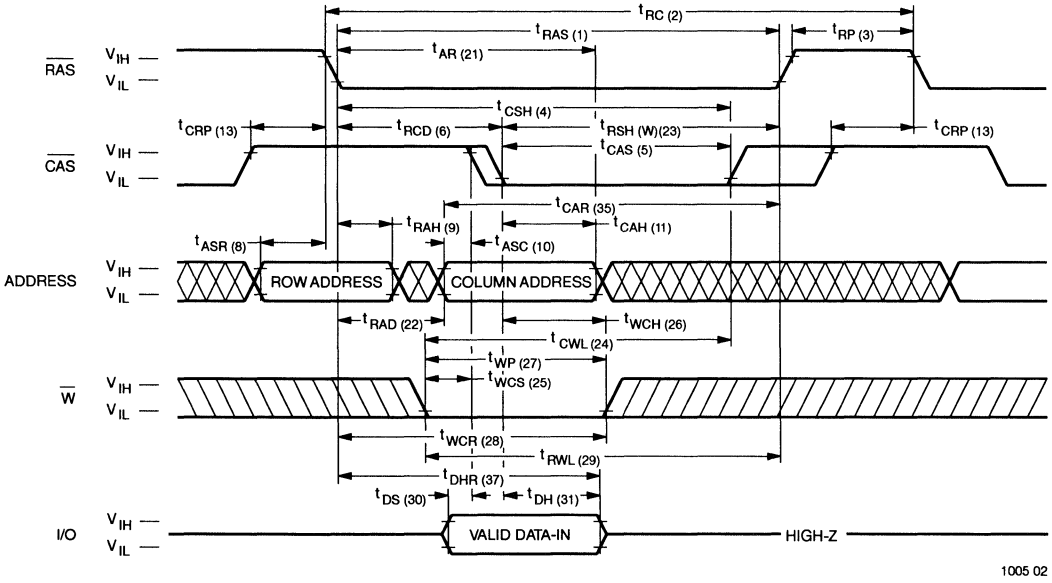
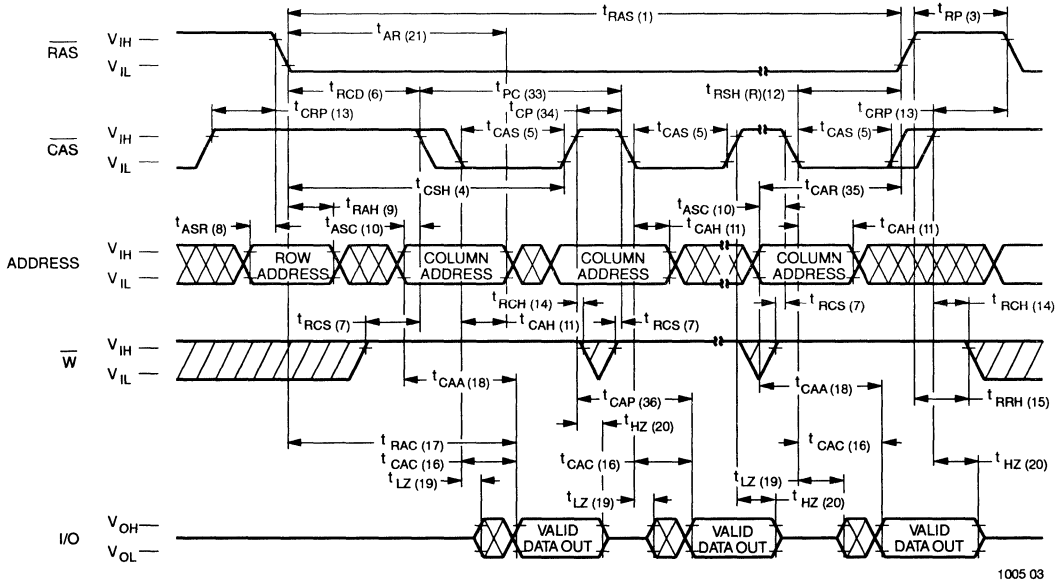
Waveforms of Read Cycle



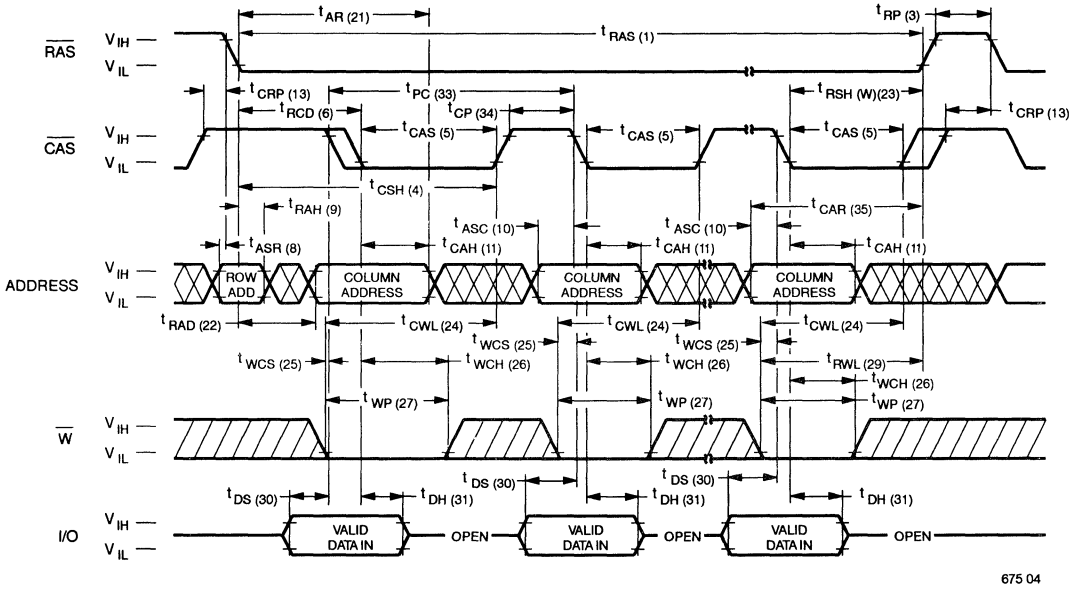
Waveforms of Early Write Cycle



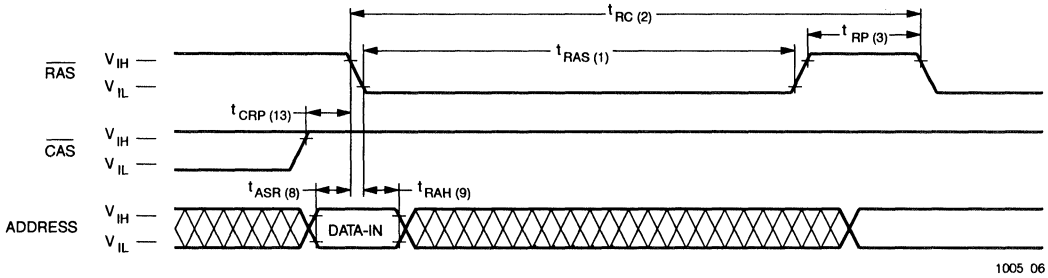
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle

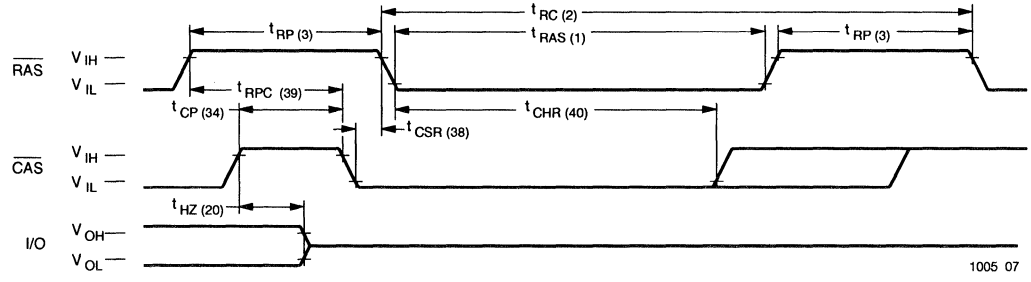


Waveforms of $\overline{RAS}$-Only Refresh Cycle



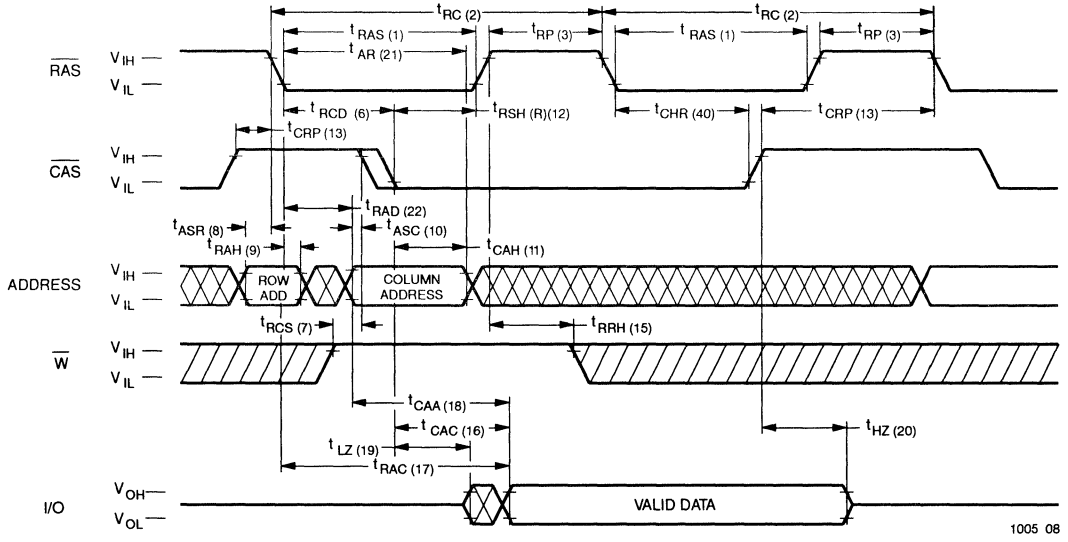
NOTE: $\overline{W}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

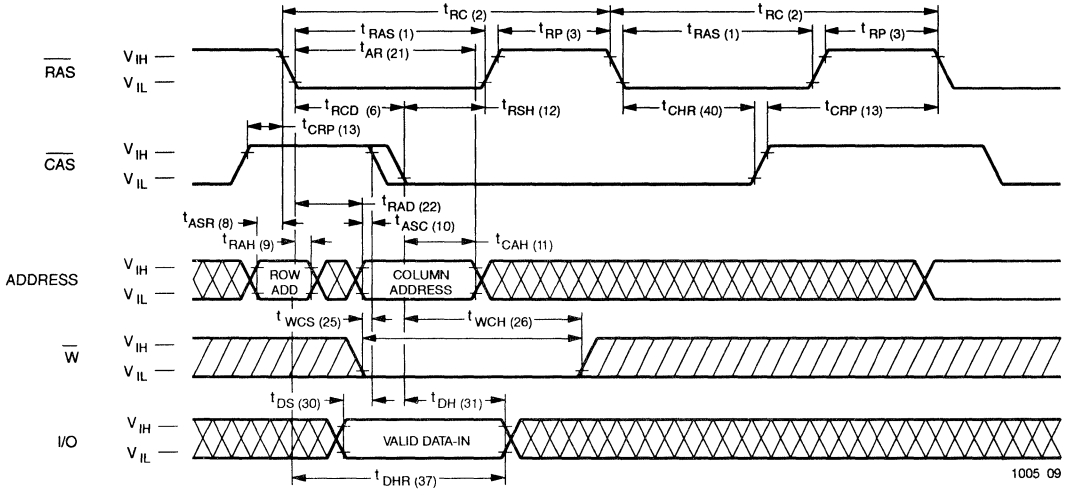


NOTE: $\overline{W}$, A_0 – A_8 = Don't care

Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



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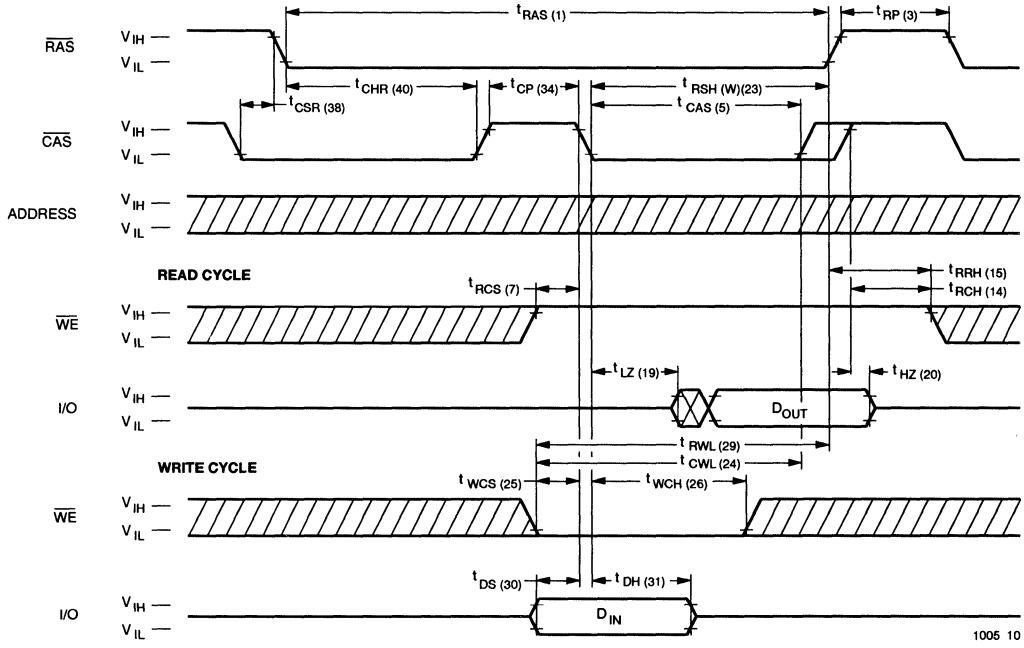
Waveforms of CAS-before-RAS Refresh Counter Test Cycle



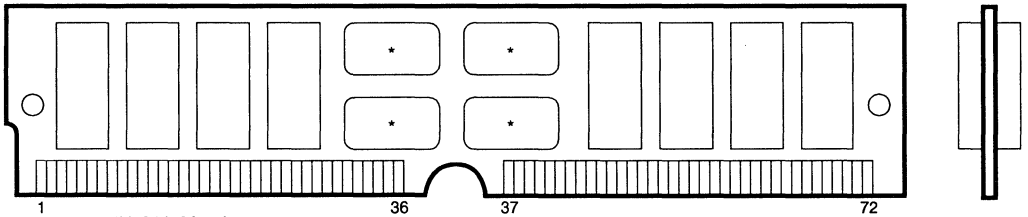
Features

- 524,288 x 32 bit or 524, 288 x 36 bit organizations
- Utilizes 256K x 4 and 256K x 1 CMOS DRAMs
- Fast access times 70 ns, 80 ns, 100 ns
- Fast Page mode operation
- Low power dissipation
- CAS before RAS refresh, RAS only refresh, and Hidden refresh capability
- Single 5 V ±10% supply
- All I/O are fully TTL compatible
- Standard 72-lead single-in-line module

Description

The V104J232 Memory Module is organized as 524,288 x 32 bits in a 72-lead single-in-line module. The 512K x 32 memory module uses 16 Mosel-Vitelic 256K x 4 DRAMs. The V104J236 is organized as 524, 288 x 36 bits in the 72 lead single-in-line module and uses 16 Mosel-Vitelic 256K x 4 DRAMs and 8 Mosel-Vitelic 256K x 1 DRAMS. The x36 modules are ideal for use in systems where high memory density with parity bits are needed.

V104J232/236 Pin Configuration



*V104J236 only

1	VSS	16	A4	31	A8	45	$\overline{RAS1}$	59	VDD
2	DQ0	17	A5	32	NC	46	NC	60	DQ32
3	DQ18	18	A6	33	$\overline{RAS3}$	47	$\overline{W}$	61	DQ14
4	DQ1	19	NC	34	$\overline{RAS2}$	48	NC	62	DQ33
5	DQ19	20	DQ4	35	NC [DQ26]	49	DQ9	63	DQ15
6	DQ2	21	DQ22	36	NC [DQ8]	50	DQ27	64	DQ34
7	DQ20	22	DQ5	37	NC [DQ17]	51	DQ10	65	DQ16
8	DQ3	23	DQ23	38	NC [DQ35]	52	DQ28	66	NC
9	DQ21	24	DQ6	39	VSS	53	DQ11	67	*1
10	VDD	25	DQ24	40	$\overline{CAS0}$	54	DQ29	68	*2
11	NC	26	DQ7	41	$\overline{CAS2}$	55	DQ12	69	*3
12	A0	27	DQ25	42	$\overline{CAS3}$	56	DQ30	70	*4
13	A1	28	A7	43	$\overline{CAS1}$	57	DQ13	71	NC
14	A2	29	NC	44	$\overline{RAS0}$	58	DQ31	72	VSS
15	A3	30	VDD						

* Signal in [ ] is V104J236 only, otherwise pins are no connect (NC).

V104J232/V104J236

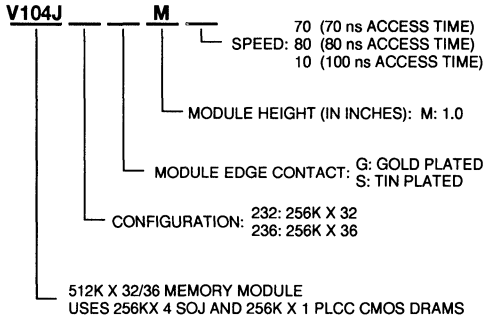
	-70	-80	-10
*1	NC	NC	NC
*2	VSS	VSS	VSS
*3	VSS	NC	VSS
*4	NC	VSS	VSS

* Presence detection. Pin connection change is available on request.

Device Usage Chart

Operating Temperature Range	Organization		Module Type	Access Time (ns)			Power	
	512K x 32	512K x 36	S	70	80	100	Std	Low
0°C–70°C	•	•	•	•	•	•	•	•

Part Number Information



V104J232/236 Pin Names

Name	Description
A0–A8	Address Inputs
$\overline{RAS0}$–$\overline{RAS3}$	Row Address Strobes
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobes
$\overline{W}$	Read/Write Input
DQ0–DQ35	Data In/Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} .....–1.0 to +7.0 V
Voltage on V_{DD} relative to V_{SS} .....–1.0 to +7.0 V
Data Out Current .....50 mA
V104J232/236 Power Dissipation.....24.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

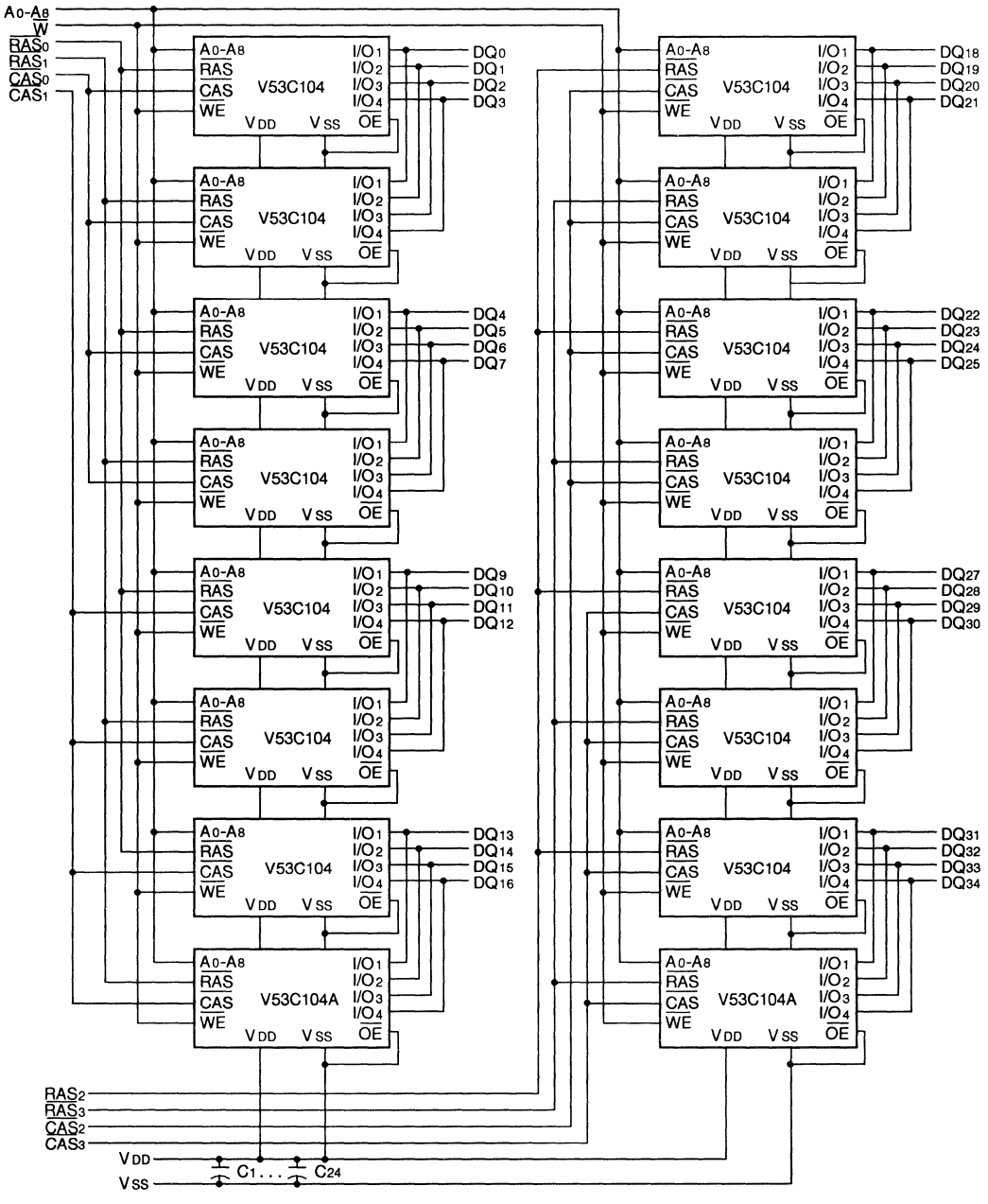
V104232/J236 Capacitance*

T_A = 0°C TO 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

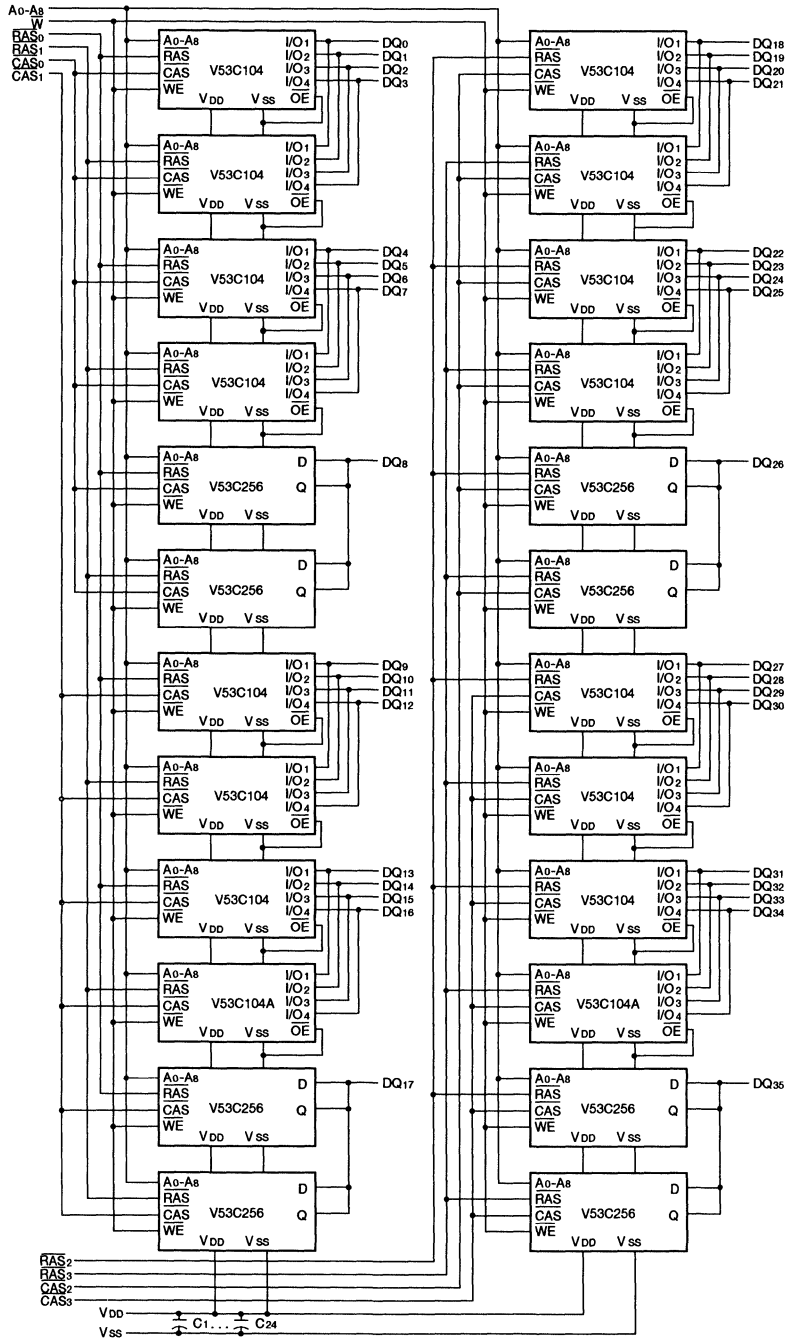
Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		176	pF
C_{IN}	Input Capacitance, $\overline{W}$		208	pF
$C_{IN(DQ)}$	Input Capacitance, Data Inputs		17	pF
$C_{IN(RAS)}$	Input Capacitance, $\overline{RAS0}$–$\overline{RAS3}$		57	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS0}$–$\overline{CAS3}$		36	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.2		µF

*Note: Capacitance is sampled and not 100% tested

V104J232 Functional Diagram



V104J236 Functional Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Power	Access Time (ns)	V104J232		V104J236		Unit	Test Conditions	Notes
				Min.	Max.	Min	Max			
I_{LI}	Input Leakage Current (any input pin)			–160	160	–240	240	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)			–20	20	–20	20	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		70		1730		1920	mA	$t_{RC} = t_{RC}$ (min.)	1,2
			80		1510		1680			
			100		1300		1440			
I_{DD2}	V_{DD} Supply Current, TTL Standby	STD			54		60	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			43		48			
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh		70		1730		1920	mA	$t_{RC} = t_{RC}$ (min.)	2
			80		1510		1680			
			100		1300		1440			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		70		1260		1400	mA	Minimum Cycle	1,2
			80		1080		1200			
			100		972		1080			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			72		80	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
		LOW			47		52			
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD			36		40	mA	$\overline{RAS}$ ≥ V_{DD}–0.2 V, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			23		25.6			
V_{IL}	Input Low Voltage (all inputs)			–1	0.8	–1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)			2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage			2.4		2.4		V	I_{OH} = –5 mA	

4

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		70		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	25	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		20		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20		25	ns	6,7
17	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	6,8,9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		45	ns	6,7,10
19	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
20	t_{CH2QZ}	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	20	0	20	0	20	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		75		ns	
22	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	11

AC Characteristics (Cont'd.)

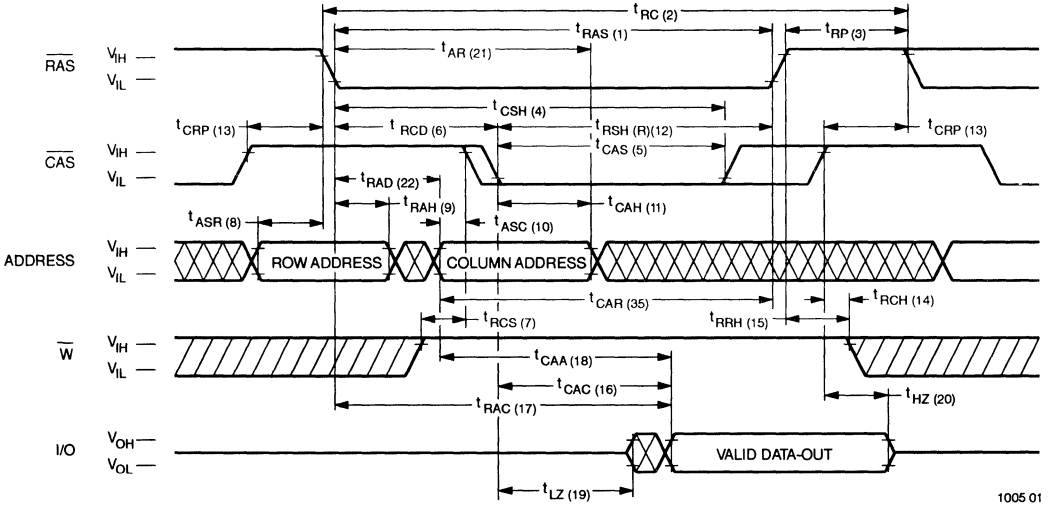
#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		25		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		20		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		20		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		75		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		ns	
30	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		20		ns	14
32	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	75		75		90		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		ns	
34	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55		60		75		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
39	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
40	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		30		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (512 Cycles)		8		8		8	ms	17

4

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 50 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit and are not referenced to the output voltage levels.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

Waveforms of Read Cycle



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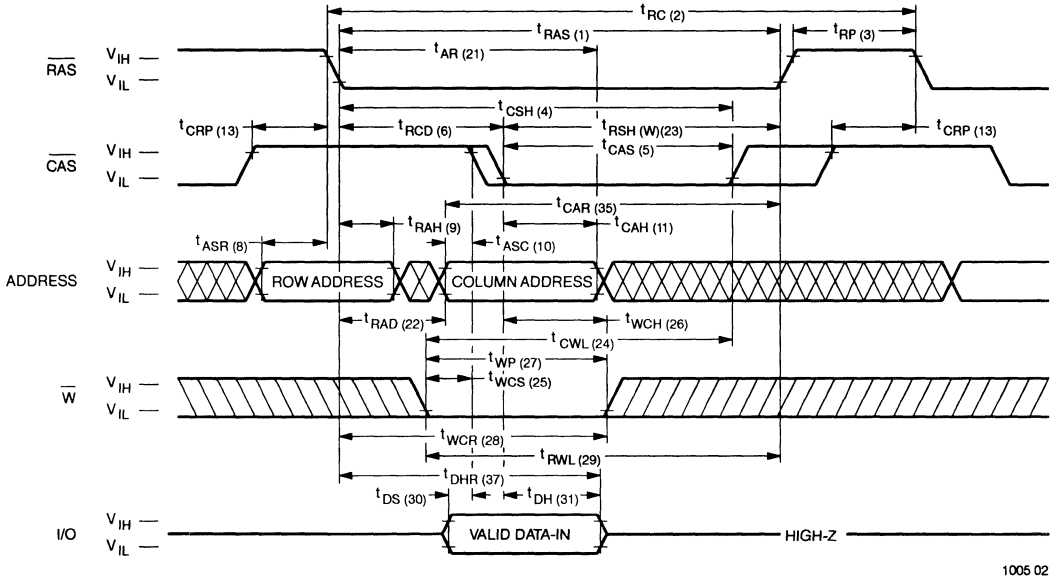
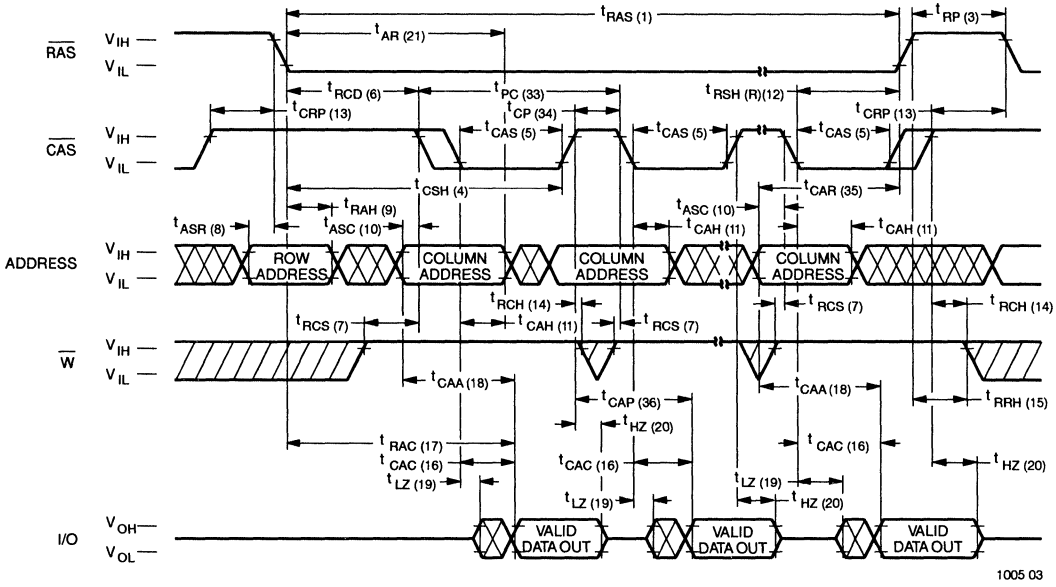
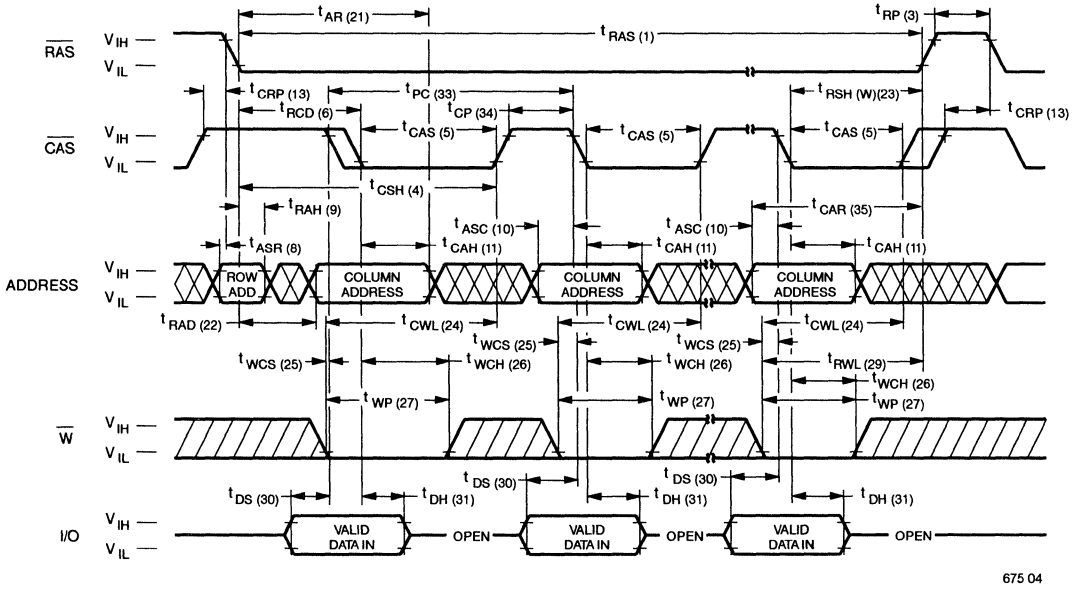
Waveforms of Early Write Cycle



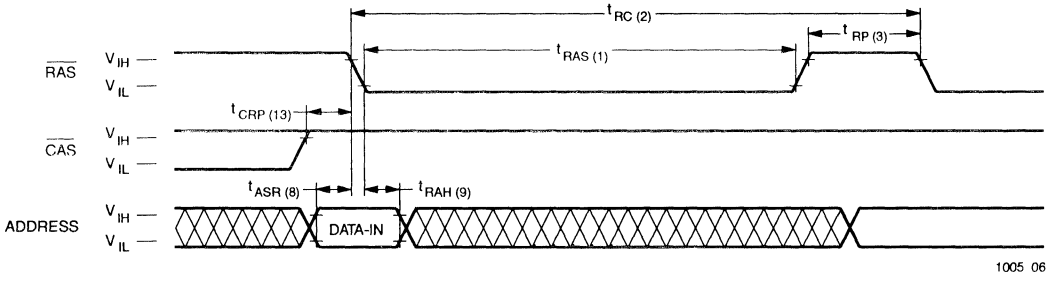
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle

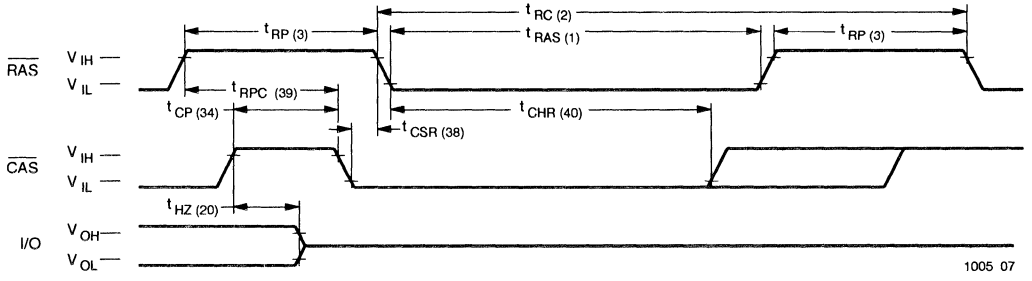


Waveforms of $\overline{RAS}$-Only Refresh Cycle



NOTE: $\overline{W}$ = Don't care

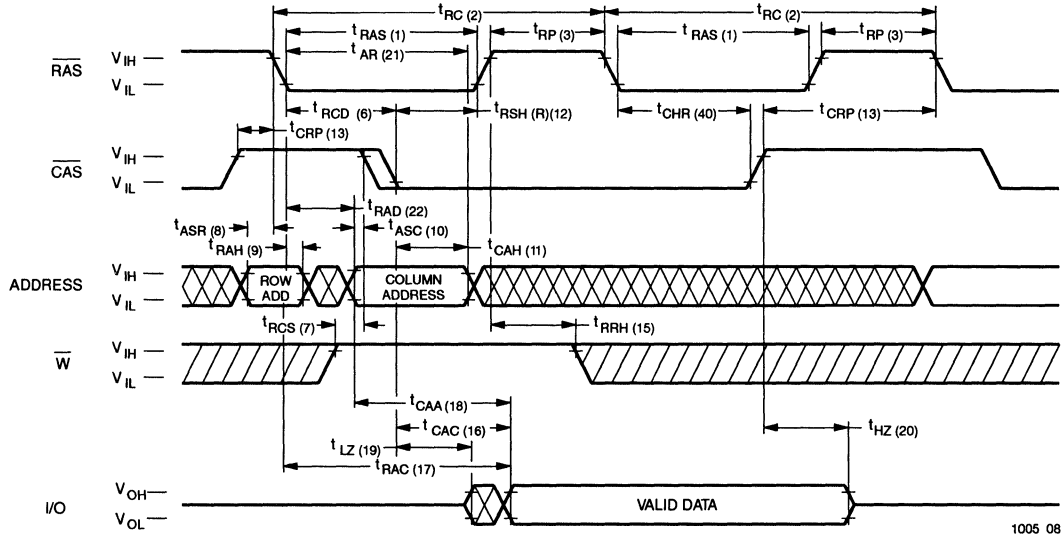
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



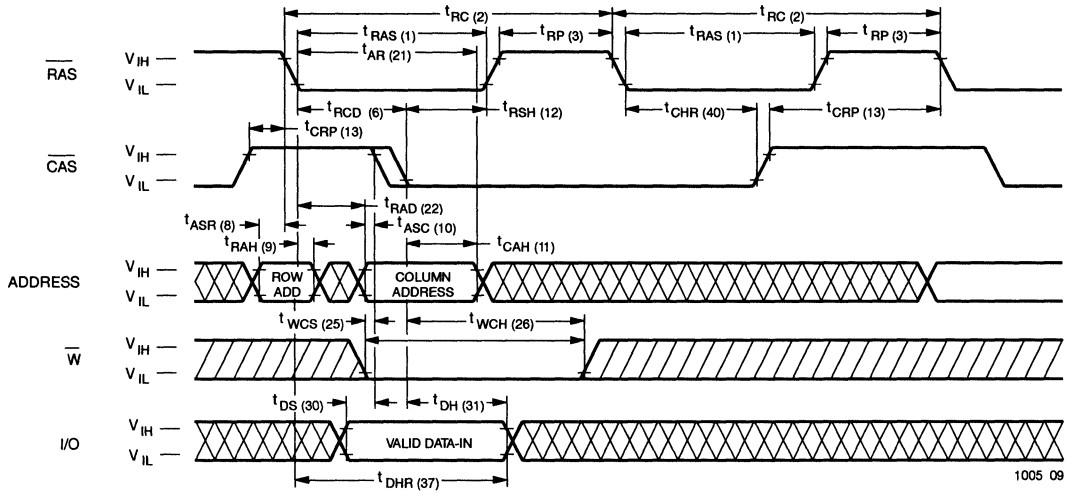
NOTE: $\overline{W}$, A_0–A_8 = Don't care

4

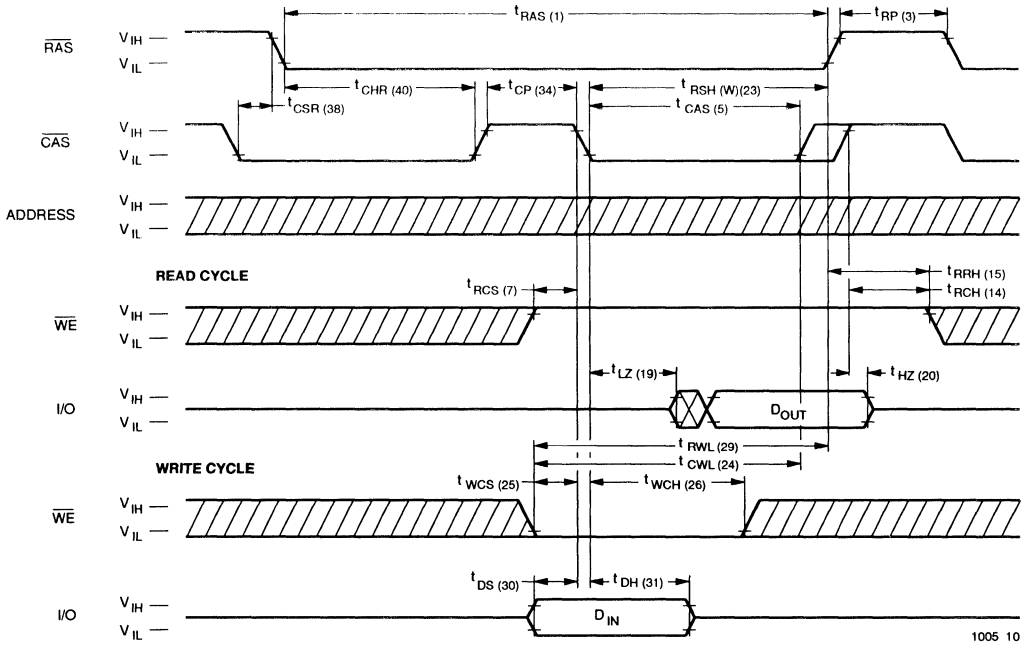
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



4

4M X 8, 4M X 9 BIT FAST PAGE MODE CMOS DYNAMIC RAM MEMORY MODULE HIGH PERFORMANCE, LOW POWER

HIGH PERFORMANCE V400J8/9	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	50 ns	55 ns	65 ns
Min. Read/Write Cycle Time, (t_{RC})	130 ns	150 ns	180 ns

LOW POWER V400J8/9L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	3.2/3.6 mA	3.2/3.6 mA	3.2/3.6 mA

Features

- 4M x 8 and 4M x 9-bit organization
- Utilizes eight or nine 4M x 1 CMOS RAMs
- RAS access time: 70, 80, 100 ns
- Low power dissipation
  - V400J8/9-80
    - — Operating Current – 640/720 mA max.
    - — TTL Standby Current – 18 mA max.
- Low CMOS Standby Current
  - V400J8/9 – 8/9 mA max.
  - V400J8/9L – 3.2/3.6 mA max.
- Battery Back-up Mode (V400J8/9L Only)
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V400J8/9 – 1024 cycles/16ms
  - V400J8/9L – 1024 cycles/64ms
- Substrate bias generator on each chip
- Fast Page Mode for a sustained data rate greater than 20 MHz
- Available in standard 30-lead single-in-line module

Description

The V400J8/9 are high speed 4,194,304 x 8/9 bit CMOS dynamic random access memory modules. The V400J8/9 offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V400J8/9L).

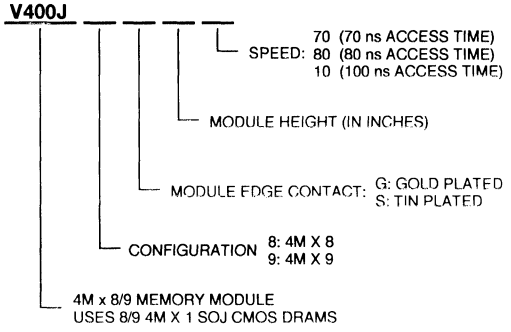
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 1024 bits within a row with cycle times as short as 50 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V400J8/9L ideally suited for high performance computing systems.

The V400J8/9L offer a maximum data retention power of 26.5/30 mW when operating in CMOS standby mode and performing $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

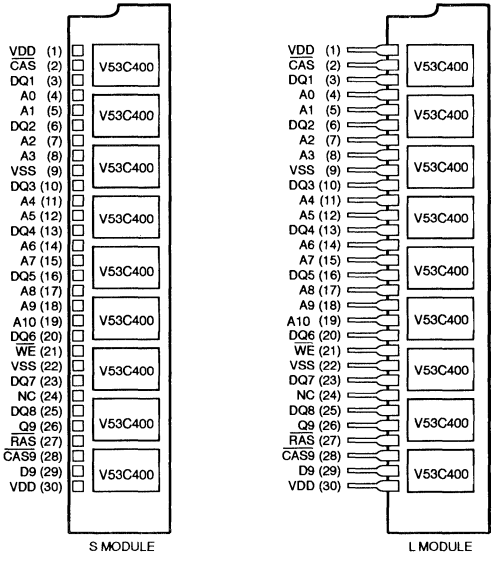
Device Usage Chart

Operating Temperature Range	Bit Organization		Module Type		Access Time (ns)			Power	
	x 8	x 9	S	L	70	80	100	Std	Low
0°C–70°C	•	•	•	•	•	•	•	•	•

Part Number Information



Pin Configuration x 9 Organization



NOTE: *x 8 Organization*
Pins 26, 28, 29 are not connected

Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 9.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Pin Names (x 9 Organization)

Name	Description
A0–A10	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobes
$\overline{WE}$	Write Enable
DQ1–DQ8	Data In/Data Out
D9	Data In
Q9	Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

x 8 Organization
$\overline{CAS9}$, D9, Q9 are not connected

Capacitance* (x9 Organization)

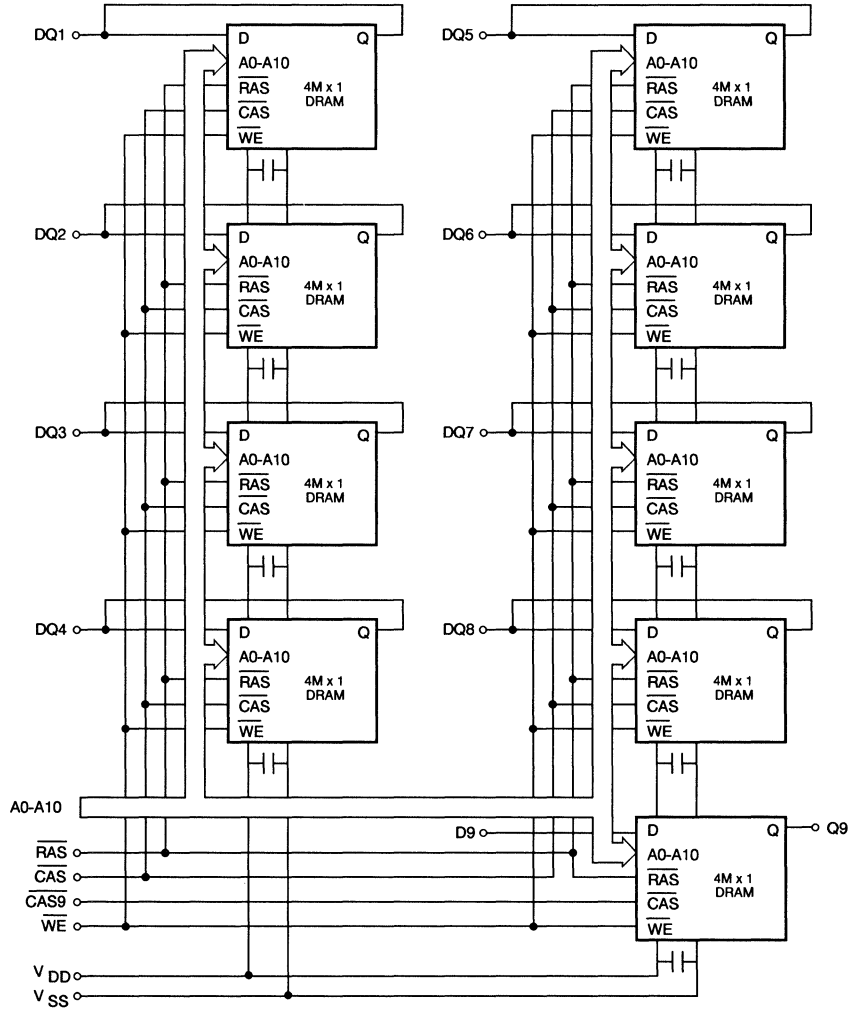
T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		70	pF
C_{IN}	Input Capacitance, $\overline{RAS}$, $\overline{WE}$		75	pF
$C_{IN(DQ)}$	Data Input/Output Capacitance, DQ1-DQ8		20	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS}$		75	pF
$C_{IN(CAS9)}$	Input Capacitance, $\overline{CAS9}$		7	pF
$C_{IN(D9)}$	Input Capacitance, D9		7	pF
$C_{O(Q9)}$	Output Capacitance, Q9		7	pF

*Note: Capacitance is sampled and not 100% tested.

4

Functional Diagram x 9 Organization



NOTE: ***x 8 Organization***
$\overline{CAS9}$, D9, Q9 are not connected

DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Power	Access Time	V400J8 Min.	V400J8 Max.	V400J9 Min.	V400J9 Max.	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)			−80	80	−90	90	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)			−10	10	−10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		70		720		810	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
			80		640		720			
			100		560		630			
I_{DD2}	V_{DD} Supply Current, TTL Standby				16		18	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh		70		720		810	mA	$t_{RC} = t_{RC}$ (min.)	2
			80		640		720			
			100		560		630			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		70		640		720	mA	Minimum Cycle	1, 2
			80		560		630			
			100		480		540			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			40		45	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	
		LOW			32		36			
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD		8		9		mA	$\overline{RAS} \ge V_{DD} - 0.2$ V $\overline{CAS} \ge V_{DD} - 0.2$V other inputs ≥ V_{SS}	
		LOW		3.2		3.6				
I_{DD7}	Battery Back-up Data Retention Current (Only V400J8/9L)	LOW		4.8		5.4		mA	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle t_{RC} = 62.5 µs CMOS clock levels	18
V_{IL}	Input Low Voltage			−1.0	0.8	−1.0	0.8	V		3
V_{IH}	Input High Voltage			2.4	V_{DD}+1	2.4	V_{DD}+1	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage			2.4		2.4			I_{OH} = −5 mA	

4

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted

#	JEDEC Symbol	Symbol	Parameter	70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL}	t_{RC}	Read or Write Cycle Time	130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		70		ns	
4	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
5	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		15		ns	
6	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		50		ns	
7	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	50	ns	4
8	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
9	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		20		ns	
10	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	25	75	ns	5
11	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	6,7,8
12	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		50	ns	8,9,10
13	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20		25	ns	8,10
14	$t_{CL1CH1(R)}$	$t_{CAS(R)}$	$\overline{CAS}$ Pulse Width in Read Cycle	20	10K	20	10K	25	10K	ns	
15	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		20		25		ns	
16	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
17	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	11
18	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	11
19	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		10		ns	
20	t_{CH2QX}	t_{OFF}	Output Buffer Turn Off Delay	0	15	0	20	0	25	ns	12

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t_{CH2QV}	t_{OH}	Data Hold Time from $\overline{CAS}$	0		0		0		ns	11
22	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		15		20		ns	
23	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
24	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		75		ns	
25	$t_{CL1CH1(W)}$	$t_{CAS(W)}$	$\overline{CAS}$ Pulse Width in Write Cycle	20		20		25		ns	
26	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		25		ns	
27	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		75		ns	
28	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	13,14
29	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		15		20		ns	
30	t_{DVWL2}	t_{DS}	Data In Setup Time	0		0		0		ns	15
31	t_{WH1DX}	t_{DH}	Data In Hold Time	15		15		20		ns	15
32	t_{RL1DX}	t_{DHR}	Data In Hold Time Referenced to $\overline{RAS}$	55		60		75		ns	
33	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		55	ns	17
34	$t_{CL2CL2(R)}$	t_{PC}	Fast Page Mode Read or Write Cycle Time	50		55		65		ns	
35	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		ns	
36	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		ns	
37	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5		5		5		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	5		5		5		ns	

4

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	70/L		80/L		10/L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
39	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Cycle	15		15		15		ns	
40	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns	
41	t_{WH2RL2}	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle)	10		10		10		ns	
42	t_{RL1WL2}	t_{WRH}	$\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle)	10		10		10		ns	
43	t_{WL1RL2}	t_{WSR}	$\overline{RAS}$ to $\overline{WE}$ set-up Time (Test Mode)	10		10		10		ns	20, 21
44	t_{RL1WH1}	t_{WHR}	$\overline{RAS}$ to $\overline{WE}$ hold Time (Test Mode)	10		10		10		ns	20, 21
45	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	16
46		t_{REF}	Refresh Interval (1024 Cycles)		16		16		16	ms	19
47		t_{REF}	Refresh Interval V400J8/9L Only (1024 Cycles, t_{RC} = 62.5 µs)		64		64		64	ms	18,19

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
5. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
6. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
7. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
8. Measured with a load equivalent to two TTL inputs and 100 pF.
9. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
10. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
11. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
12. t_{OFF} and t_{ON} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage level.
13. t_{WCS} is not a restrictive operating parameter.
14. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
15. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
16. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
17. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
18. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
19. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

    t_{RC} = 62.5 µs (62.5 µs x 1024 = 64 ms)

    $t_{RAS} = t_{RAS}$ (min) to 1 µs

    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V

    $V_{IL} < 0.2$ V

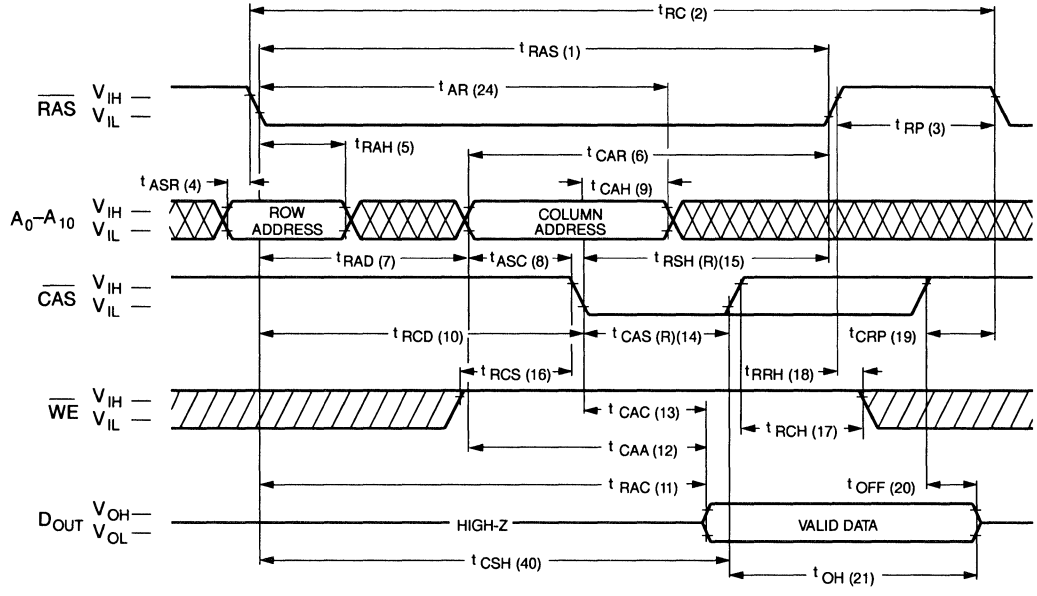
    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V

    All other inputs at stable V_{IH} or V_{IL}
20. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$-before-$\overline{RAS}$ cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is 8-bits parallel testing function.

    RA_{10}, CA_{10}, CA_0 are not used. In the read cycle, if two internal bits on one I/O pin are equal, the I/O pin will indicate a high level. If internal bits on one I/O are not equal, then the I/O pin will indicate a low level. The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
21. In a test mode read cycle, the value of access time parameters is delayed by 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value (5 ns) to the specified value in this data sheet.

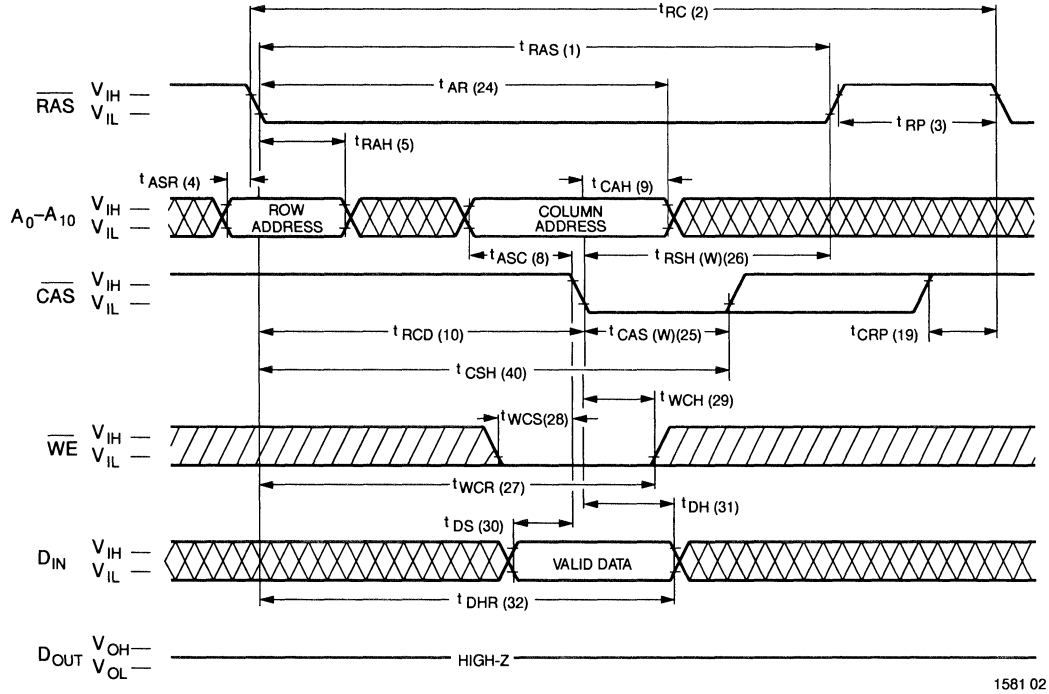
4

Waveforms of Read Cycle



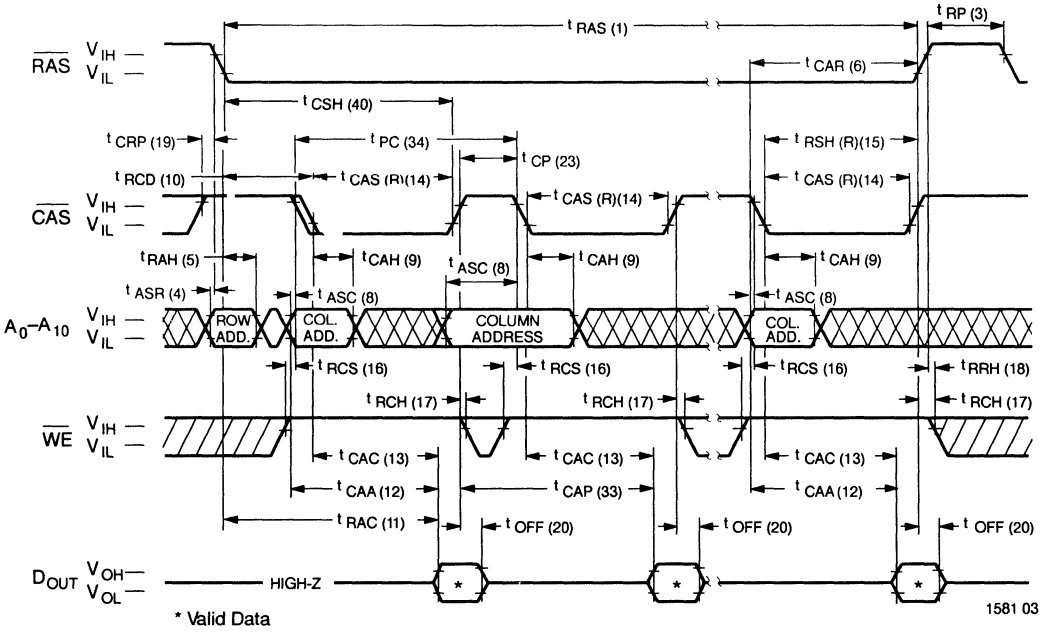
1581 01

Waveforms of Early Write Cycle

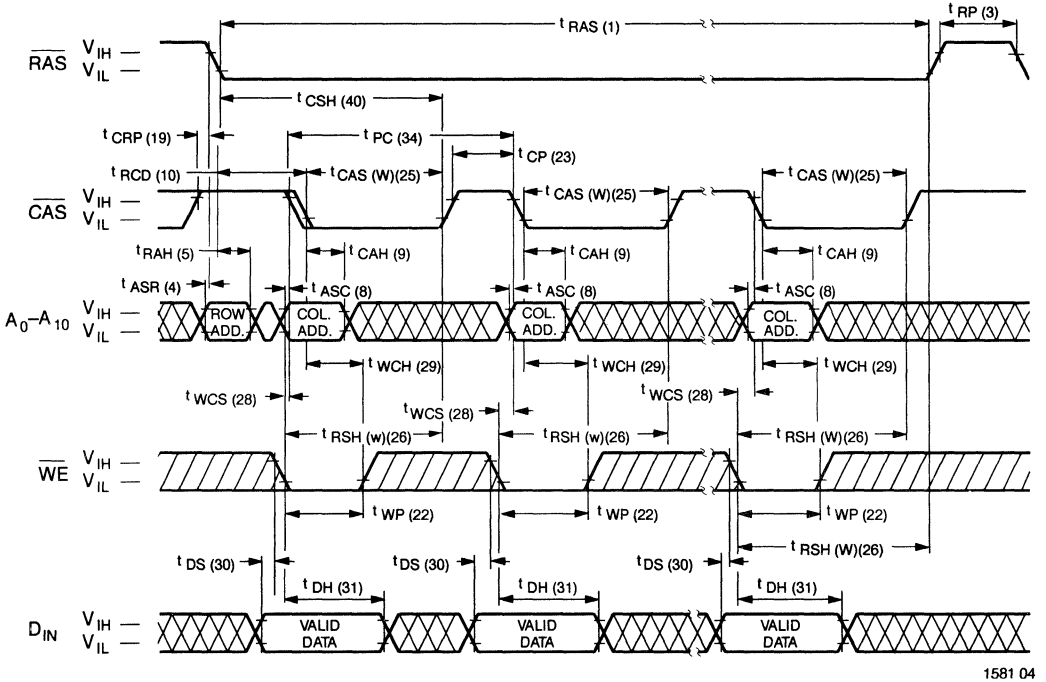


1581 02

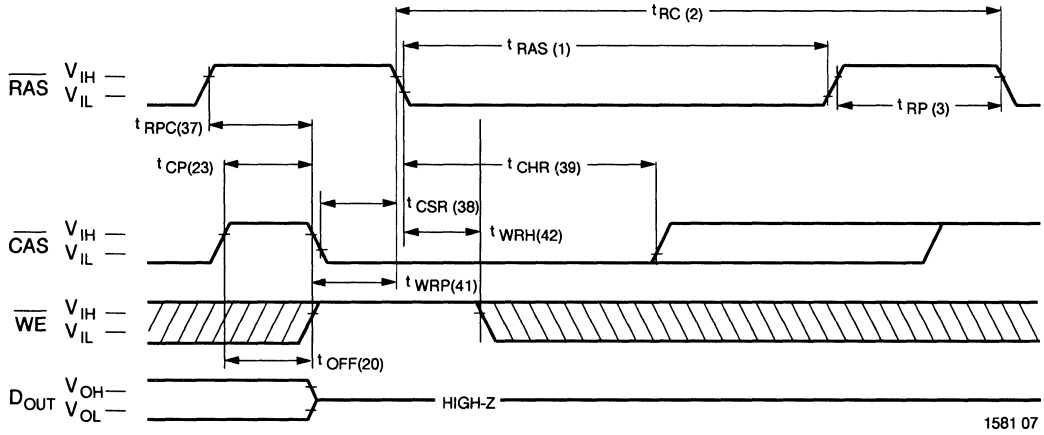
Waveforms of Fast Page Mode Read Cycle



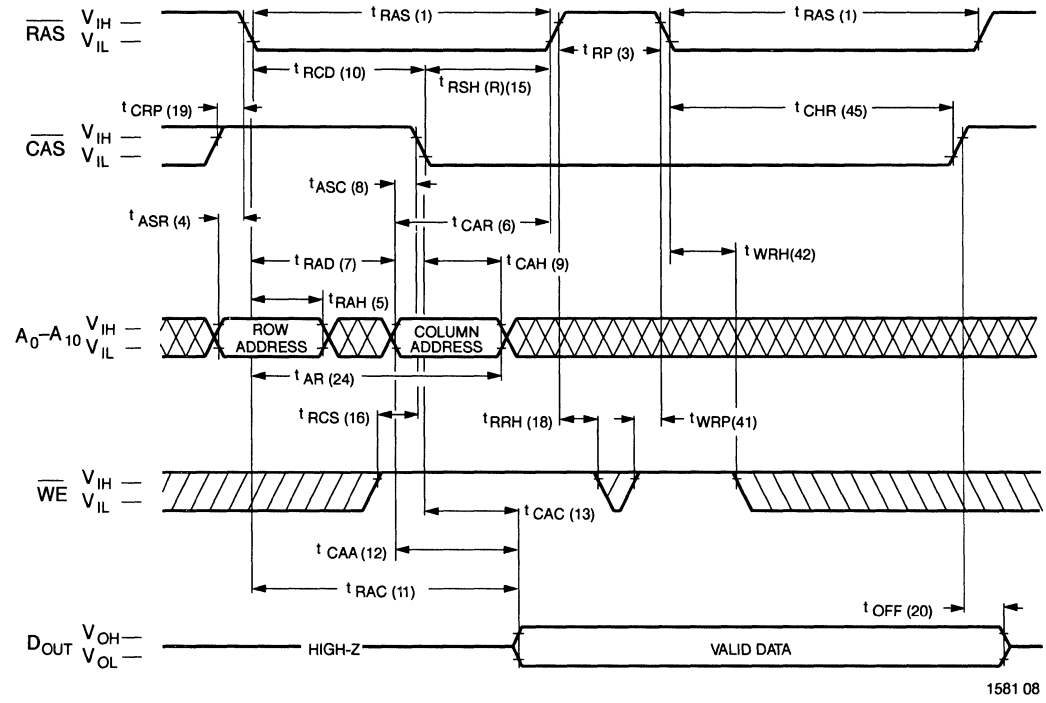
Waveforms of Fast Page Mode Write Cycle



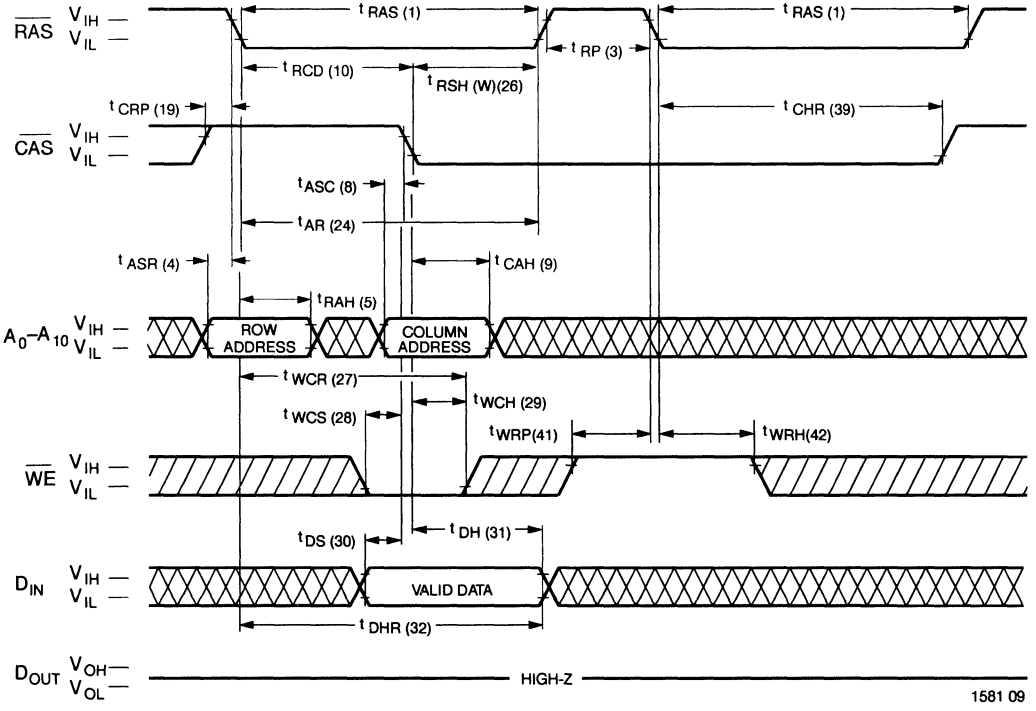
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



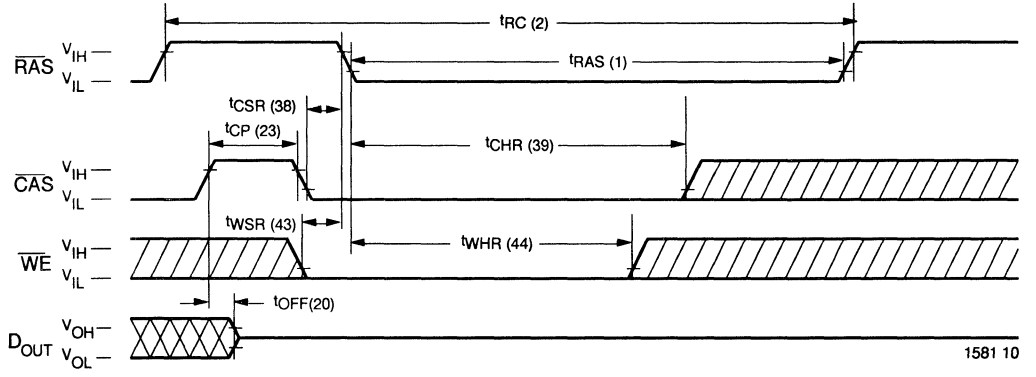
Waveforms of Hidden Refresh Cycle (Read)



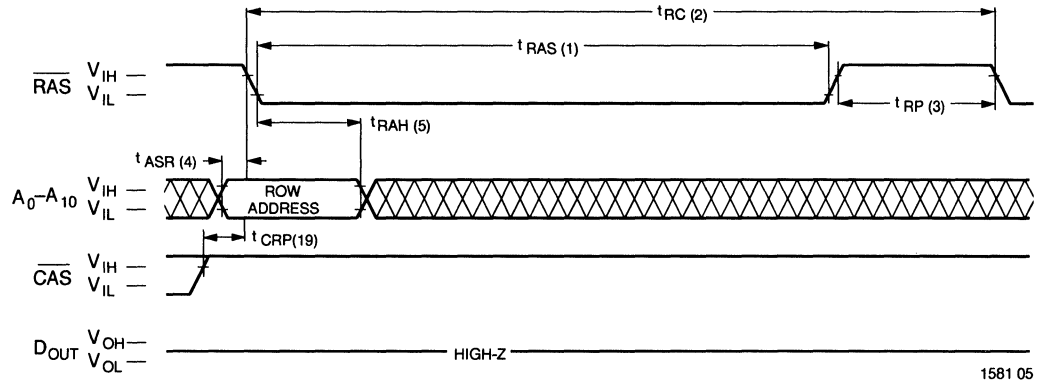
Waveforms of Hidden Refresh Cycle (Write)



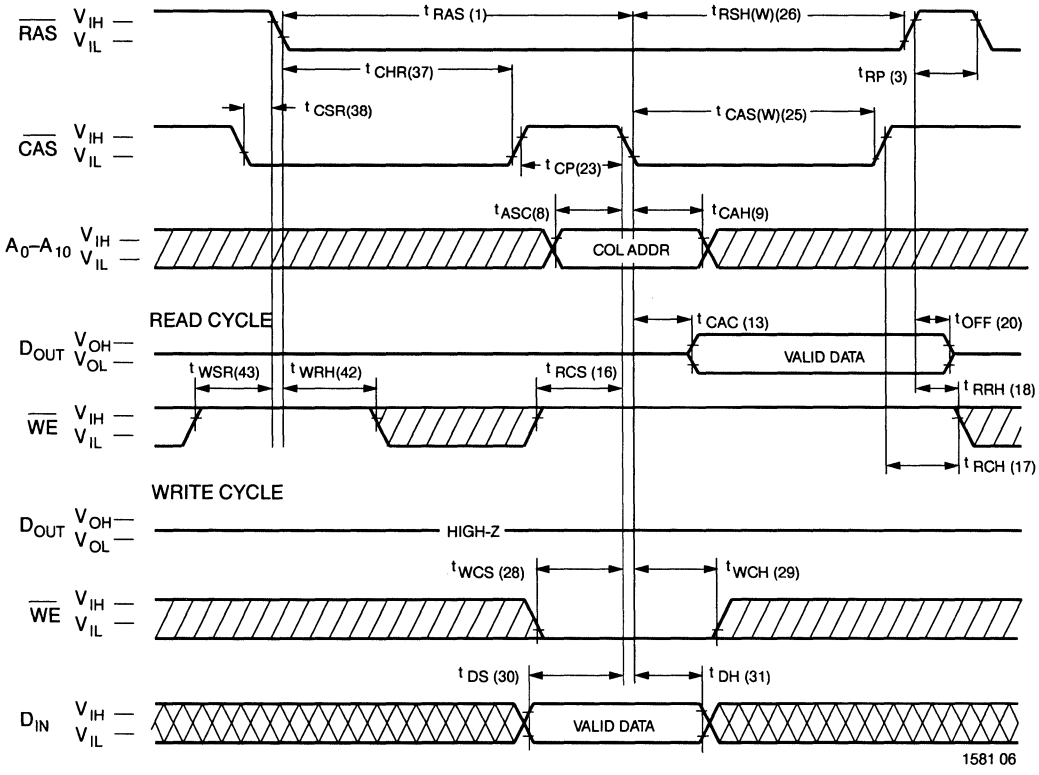
Test Mode Initiation Cycle



Waveforms of $\overline{RAS}$-Only Refresh Cycle



Waveforms of $\overline{CAS}$-Before-$\overline{RAS}$ Refresh Counter Test Cycle



Functional Description

The V400J8/9 are CMOS dynamic RAM modules optimized for high data bandwidth, low power applications. The V400J8/9 reads and writes data by multiplexing a 22-bit address into an 11-bit row and an 11-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address flows through an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal high during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum time specified by t_{AR}. Data Out becomes valid only when t_{RAC}, t_{CAA} and t_{CAC} are all satisfied. As a result, the access time is dependent on the timing relationships between t_{RAC}, t_{CAA} and t_{CAC}. For example, the access time is limited by t_{CAA} when t_{RAC} (min.) and t_{CAC} (min.) are both satisfied.

Write Cycle

A Write cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The write can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In a $\overline{CAS}$-controlled Write Cycle when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the output (D_{OUT}) pin will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

Refresh Cycle

To retain data, 1024 Refresh Cycles are required in each 16 ms period. There are two ways to Refresh the memory:

1. By selecting all 1024 address combinations of A0 through A10 each 16 ms, a refresh of all rows is completed. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.

2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V53C400 will use the output of an internal 10-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, D_{OUT} will remain in the High-Z state during the cycle.

A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter. The user can use the counter test mode to write consecutive data patterns (1024 Write cycles) and then verify the written data by applying 1024 consecutive Read cycles. In this mode, the V400J8/9 ignores external row/column addresses and takes the output from the internal counter instead.

Data Retention Mode

The V400J8/9 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V400J8/9 power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{[(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 1024

4

Fast Page Mode Operation

Fast Page Mode operation permits all 2048 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high.

Thus, access begins at the occurance of a valid column address rather than at the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as on output enable.

During Fast Page Mode operation, Read or Write cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is determined by the by the $\overline{CAS}$ rising edge. If the column address is valid after the rising edge of $\overline{CAS}$, the access is timed from the occurrance of the valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of over 20 MHz for applications that require high data rates like bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the data rate:

$$\text{Data Rate} = \frac{2{,}048}{t_{RC} + 2{,}047 \times t_{PC}}$$

Data Output Operation

The V400J8/9 Data Output pin (D_{OUT}) has a three-state capability and is controlled by $\overline{CAS}$. When $\overline{CAS}$ is high($\geq V_{IH}$), the output is in the High-Z state. Table 1 summarizes the D_{OUT} states possible for various memory cycles.

Power On

After application of the V_{DD} an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval). During power on, the V_{DD} current requirement of the V400J8/9 is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is Low during power on, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during power on to avoid current surges.

Table 1. V400J8/9 Data Output
Operation for Various Cycle Types

Cycle Type	D_{OUT} State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
$\overline{WE}$-Controlled Write Cycle (Late Write)	Active, not valid
Fast Page Mode Read Cycle	Data from Addressed Memory Cell
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

V400J32/36
4M x 32 & 4M x 36
CMOS MEMORY MODULES

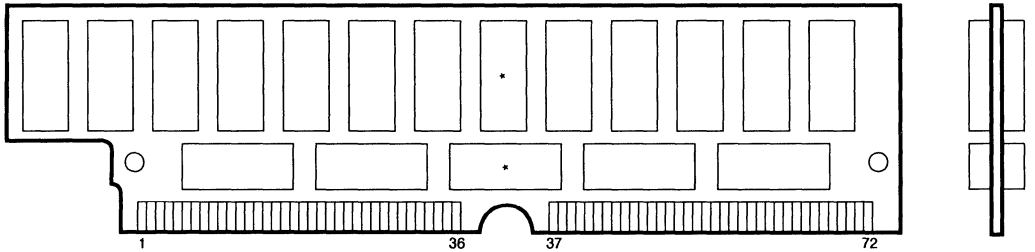
Features

- 4,194,304 x 36 bit organization (V400J36)
- 4,194,304 x 32 bit organization (V400J32)
- Utilizes 4M x 1 CMOS DRAMs
- Fast access times: 70 ns, 80 ns
- Fast Page mode operation
- CAS before RAS refresh, RAS only refresh, and Hidden refresh capability
- Single 5 V ±10% supply
- All I/O are fully TTL compatible
- Standard 72-lead single-in-line module
- 1024 Refresh Cycles every 16 msec

Description

The V400J32 Memory Module is organized as 4,194,304 x 32 bits and the V400J36 is orgranized as 4,194,304 x 36 bits in a 72-lead single-in-line module. The 4M x 32 memory module uses 32 4M x 1 DRAMs and the 4M x 36 memory module uses 36 4M x 1 DRAMs. The x32/36 modules are ideal for use in i486 systems where high memory density and fast access times are needed.

V400J32/36
Pin Configuration



*V400J36 only

1	VSS	19	A10	37	DQ17/NC*	55	DQ12
2	DQ0	20	DQ4	38	DQ35/NC*	56	DQ30
3	DQ18	21	DQ22	39	$\overline{VSS}$	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	VDD
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	VDD	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{W}$	65	DQ16
12	A0	30	VDD	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	*1
14	A2	32	A9	50	DQ27	68	*2
15	A3	33	NC	51	DQ10	69	*3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	*4
17	A5	35	DQ26/NC*	53	DQ11	71	NC
18	A6	36	DQ8/NC*	54	DQ29	72	VSS

*V400J32 only

V400J32/36

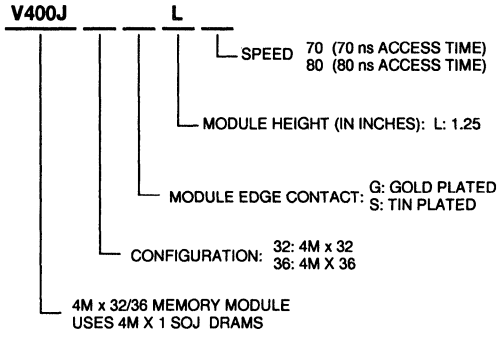
	-70	-80
*1	VSS	VSS
*2	NC	NC
*3	VSS	NC
*4	NC	VSS

* Presence detection. Pin connection change is available on request.

Device Usage Chart

Operating Temperature Range	Organization		Module Type	Access Time (ns)		Power
	4M x 32	4M x 36	S	70	80	Std
0°C–70°C	•	•	•	•	•	•

Part Number Information



Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) ..... –55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... –1.0 to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... –1.0 to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 21.6 W

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

Pin Names

Name	Description
A0–A10	Address Inputs
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobes
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobes
$\overline{W}$	Read/Write Input
DQ0–DQ35	Data In/Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

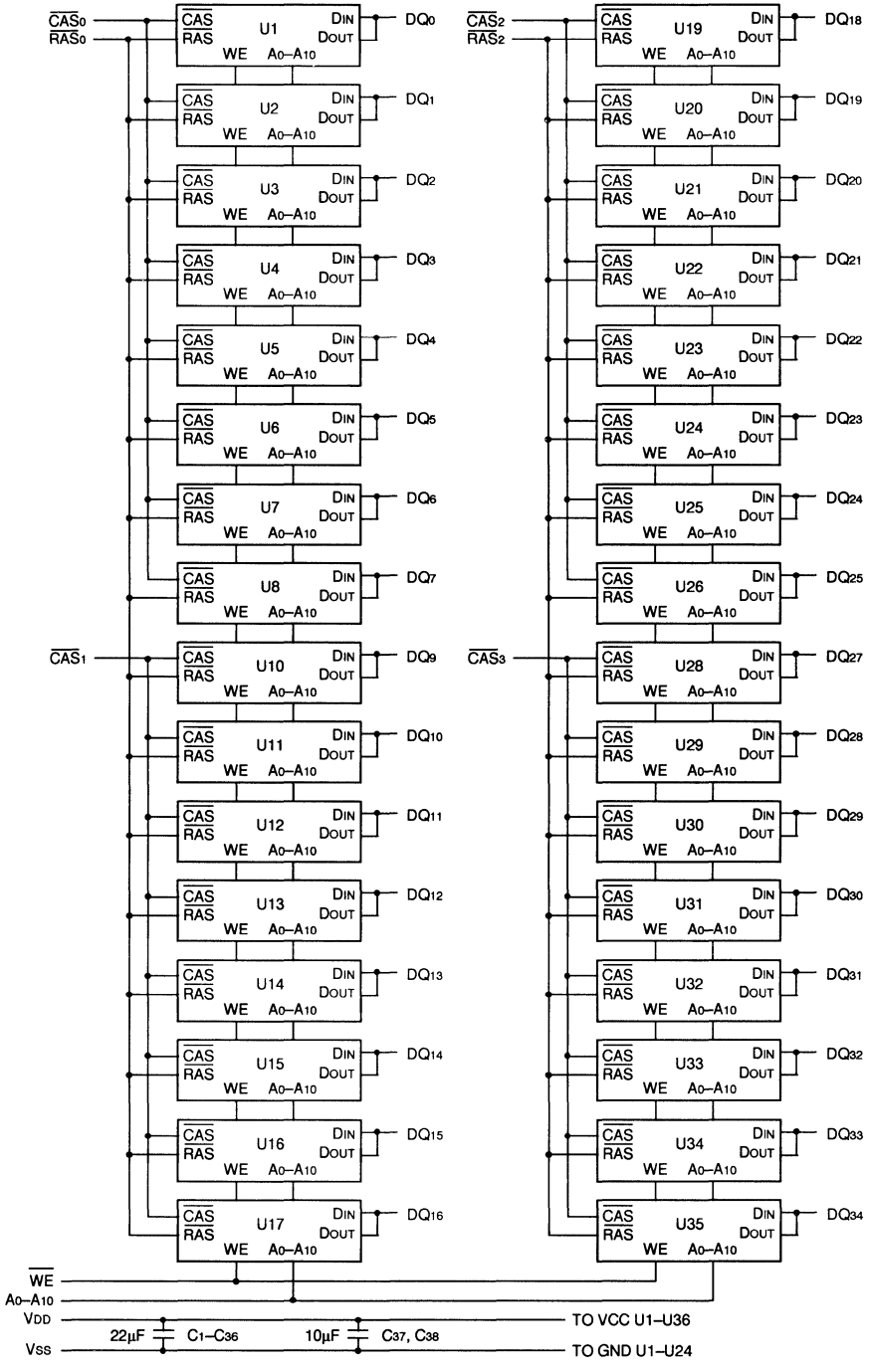
Capacitance*

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

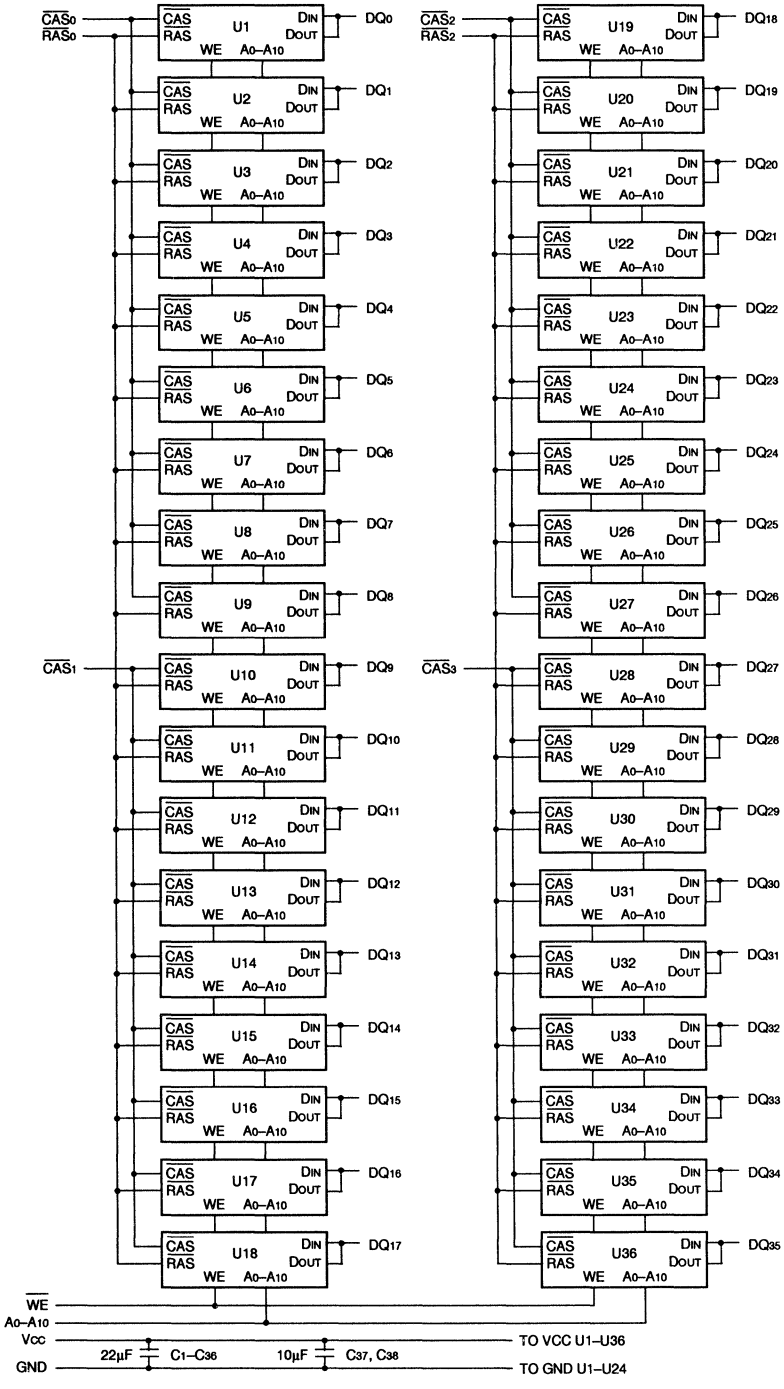
Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		195	pF
C_{IN}	Input Capacitance, $\overline{W}$		257	pF
$C_{IN(DQ)}$	Input Capacitance, Data Inputs		17	pF
$C_{IN(RAS)}$	Input Capacitance, $\overline{RAS0}$, $\overline{RAS2}$		131	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS0}$–$\overline{CAS3}$		68	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.4		µF

***Note:** Capacitance is sampled and not 100% tested

V400J32 Functional Diagram



V400J36 Functional Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time (ns)	V400J32		V400J36		Unit	Test Conditions	Notes
			Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–360	–360	–360	–360	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–20	20	–20	20	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating			3402		3780	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
I_{DD2}	V_{DD} Supply Current, TTL Standby			65		72	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh			3402		3780	mA	$t_{RC} = t_{RC}$ (min.)	2
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation			2590		2880	mA	Minimum Cycle	1, 2
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			32		36	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
V_{IL}	Input Low Voltage (all inputs)		–1	0.8	–1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)		2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4		V	I_{OH} = –5 mA	

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AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted.
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	70		80		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	130		150		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	25	60	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		20		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20	ns	6, 7
17	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		70		80	ns	6, 8, 9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40	ns	6, 7, 10
19	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	5		5		ns	16
20	t_{CH2QZ}	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	15	0	15	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		ns	
22	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	20	40	ns	11

AC Characteristics (Cont'd.)

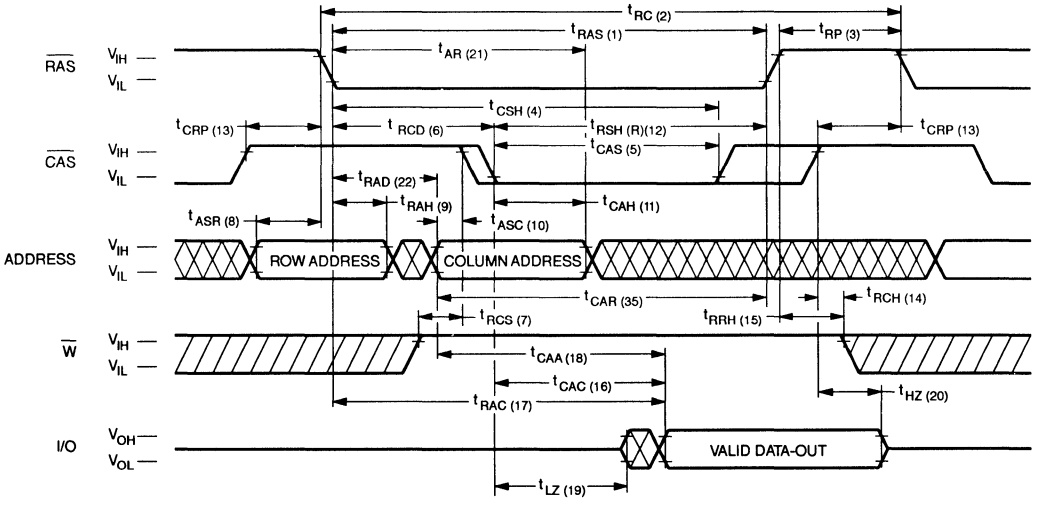
#	JEDEC Symbol	Symbol	Parameter	70		80		Unit	Notes
				Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		ns	12, 13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		ns	
30	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		ns	14
32	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW) Fast Page Mode R-M-W	75		75		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	50		55		ns	
34	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time (Fast Page)	10		10		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	45		45		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from $\overline{CAS}$ Precharge		45		45	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55		60		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		ns	
39	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		ns	
40	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		ns	
	t_T	t_T	Transition Time (Rise and Fall)	5	50	5	50	ns	15
		t_{RI}	Refresh Interval		16		16	ms	17

4

Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit and are not referenced to the output voltage levels.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

Waveforms of Read Cycle



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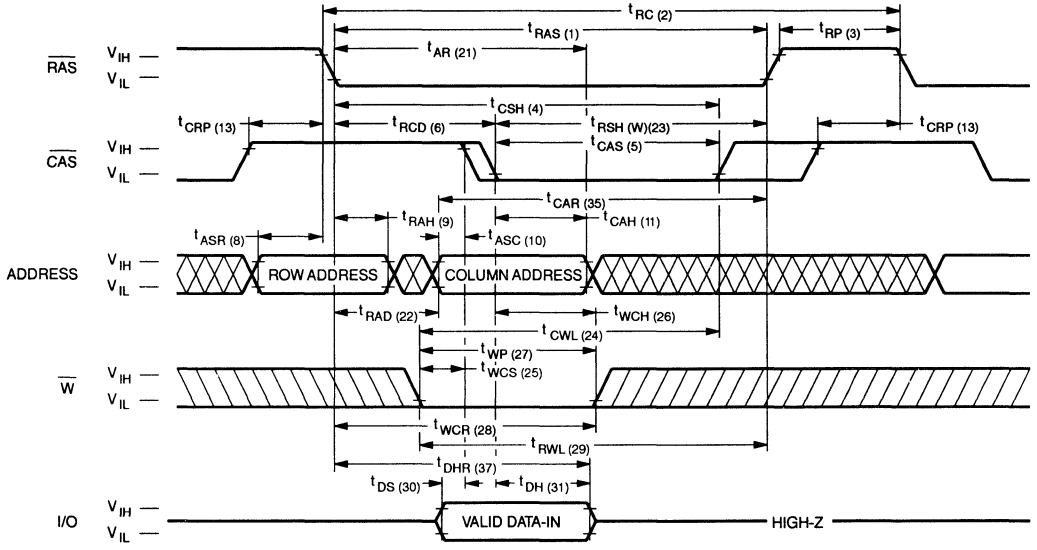
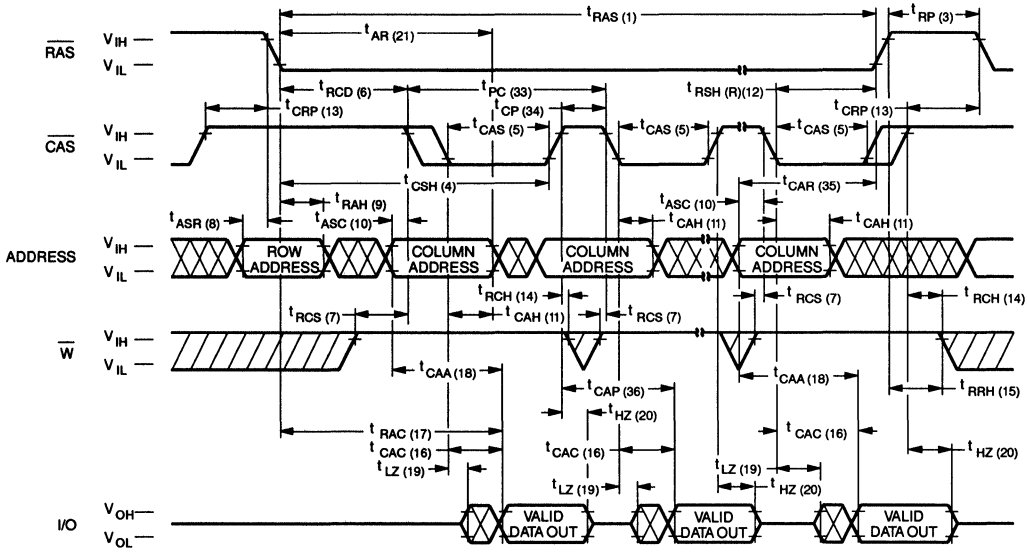
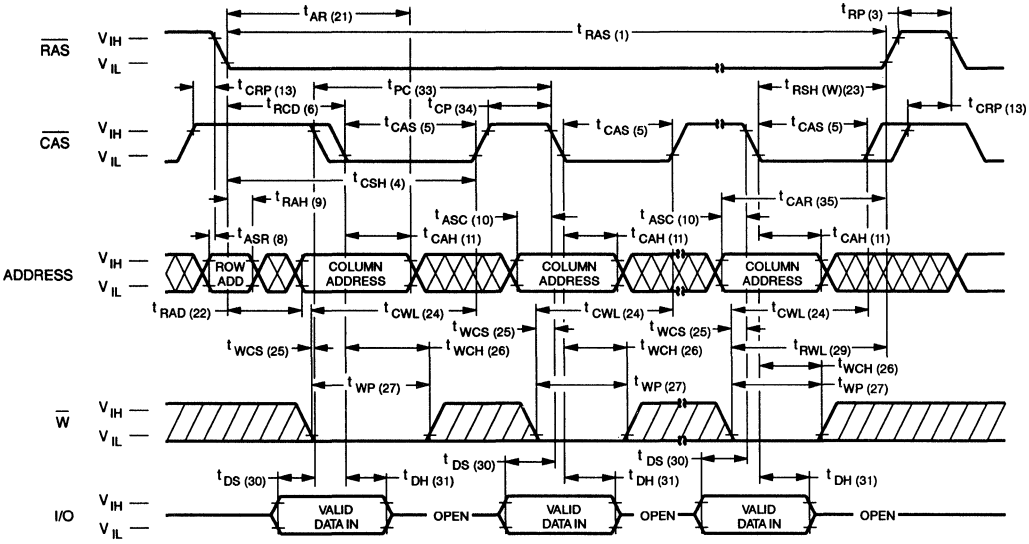
Waveforms of Early Write Cycle



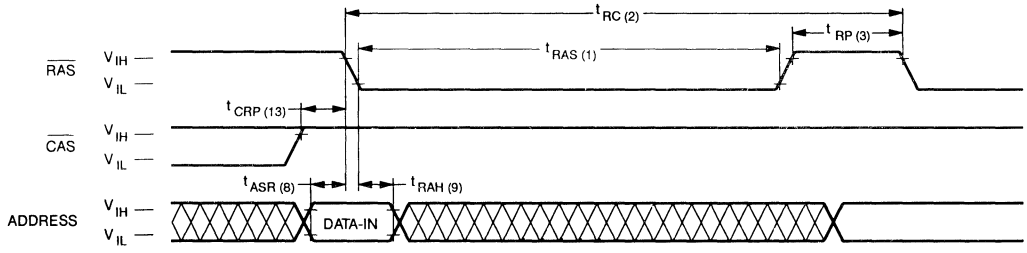
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle

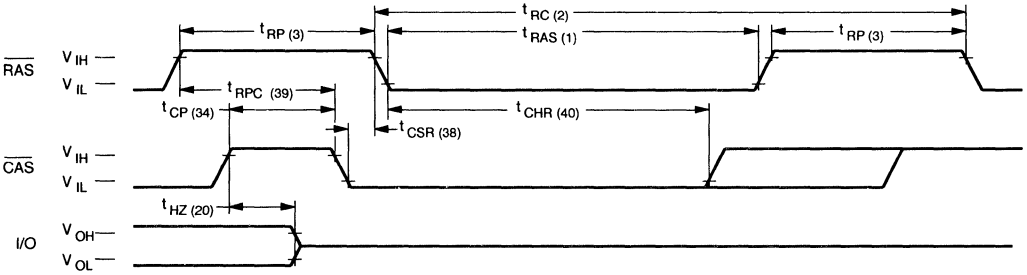


Waveforms of $\overline{RAS}$-Only Refresh Cycle



NOTE: $\overline{W}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



NOTE: $\overline{W}$, A_0–A_9 = Don't care

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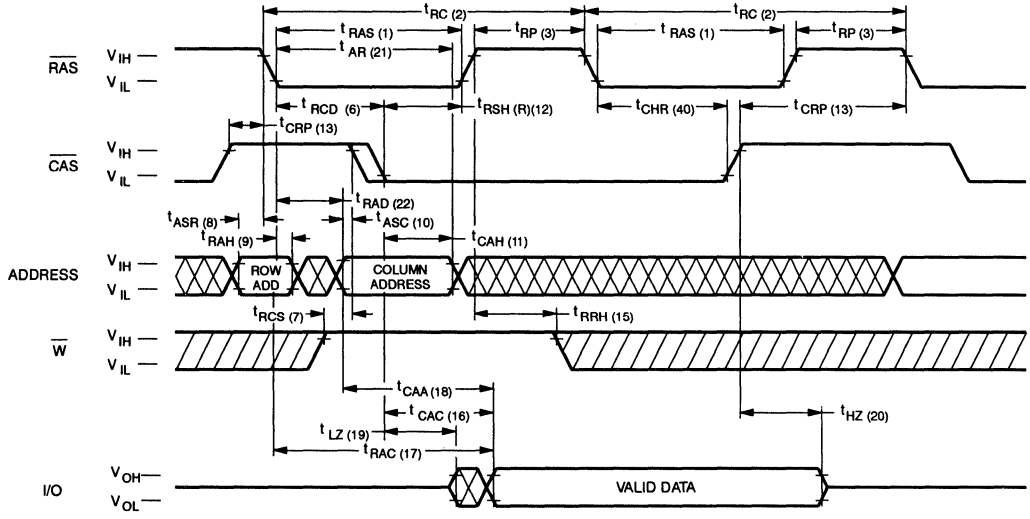
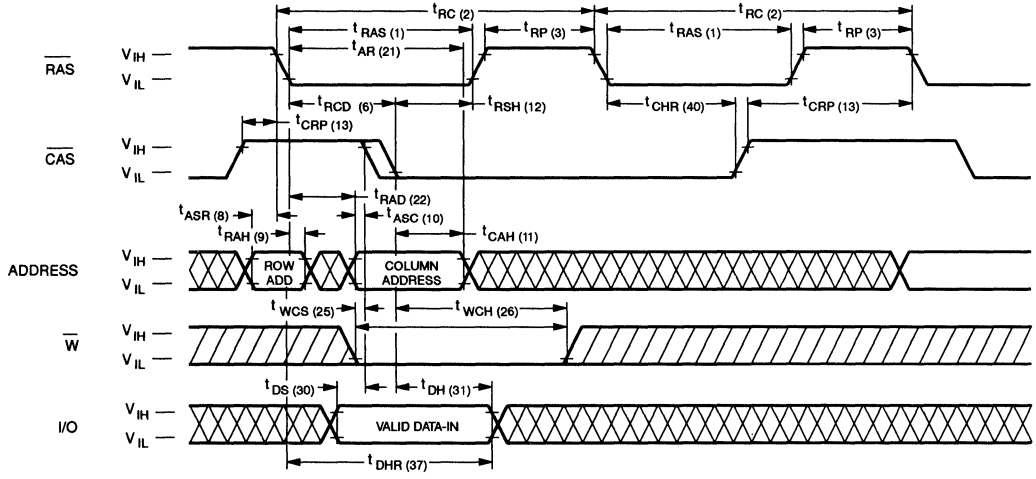
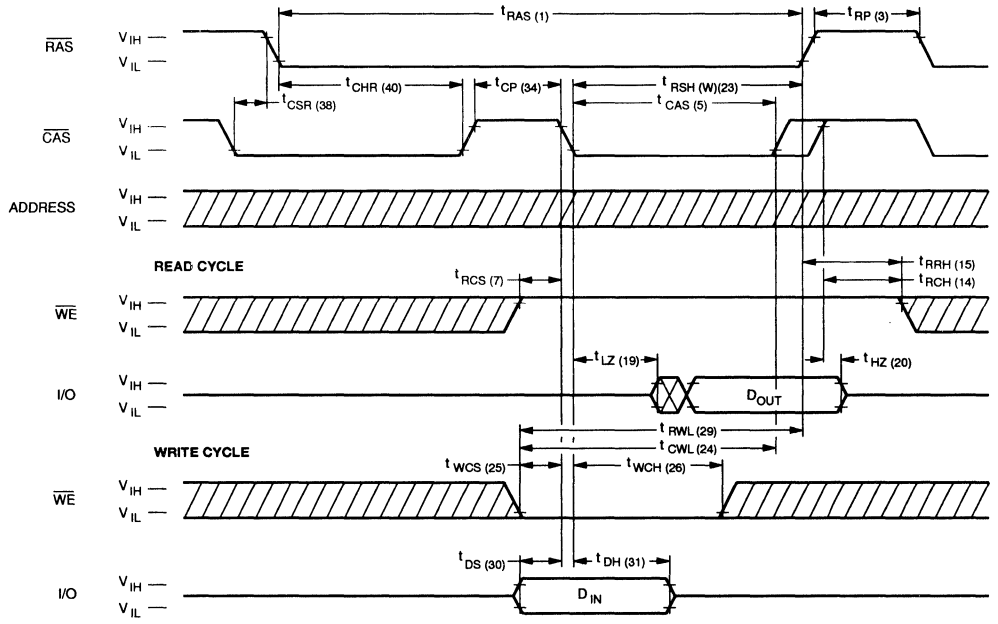
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



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HIGH PERFORMANCE V404J8/9	60/60L	70/70L	80/80L	10/10L
Max. $\overline{RAS}$ Access Time, (t_{RAC})	60 ns	70 ns	80 ns	100 ns
Max. Column Address Access Time, (t_{CAA})	30 ns	35 ns	40 ns	50 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	45 ns	50 ns	55 ns	65 ns
Min. Read/Write Cycle Time, (t_{RC})	120 ns	130 ns	160 ns	180 ns

LOW POWER V404J8/9L	60L	70L	80L	10L
Max. CMOS Standby Current, (I_{DD6})	0.8/2mA	0.8/1 mA	0.8/1 mA	0.8/1 mA

Features

- 1M x 8 and 1M x 9-bit organization
- Utilizes 1M x 4 and 1M x 1 CMOS DRAMs
- RAS access time: 60, 70, 80, 100 ns
- Low power dissipation
  - V404J8/9-80
    - — Operating Current – 160/230 mA max.
    - — TTL Standby Current – 4/6 mA max.
- Low CMOS Standby Current
  - V404J8/9 – 2/3 mA max.
  - V404J8/9L – 0.8/1 mA max.
- Battery Back-up Mode (V404J8/9L Only)
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh capability
- Refresh Interval
  - V404J8/9 – 1024 cycles/16ms
  - V404J8/9L – 1024 cycles/64ms
- Fast Page Mode for a sustained data rate greater than 20 MHz
- Available in standard 30-lead single-in-line module

Description

The V404J8/9 are high speed 1,048,576 x 8/9 bit CMOS dynamic random access memory modules. The V404J8/9 offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V404J8/9L).

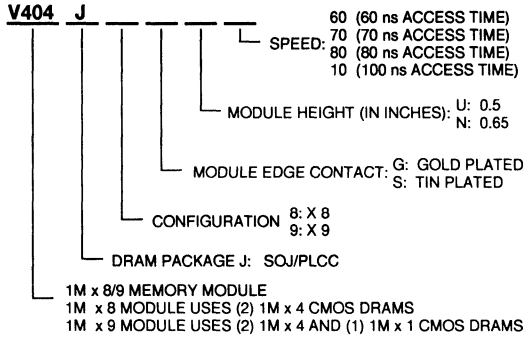
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 1024 bits within a row with cycle times as short as 45 ns. Because of static circuitry, the $\overline{CAS}$ clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V404J8/9L ideally suited for high performance computing systems.

The V404J8/9L offer a maximum data retention power of 6.6/8.3 mW when operating in CMOS standby mode and performing $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.

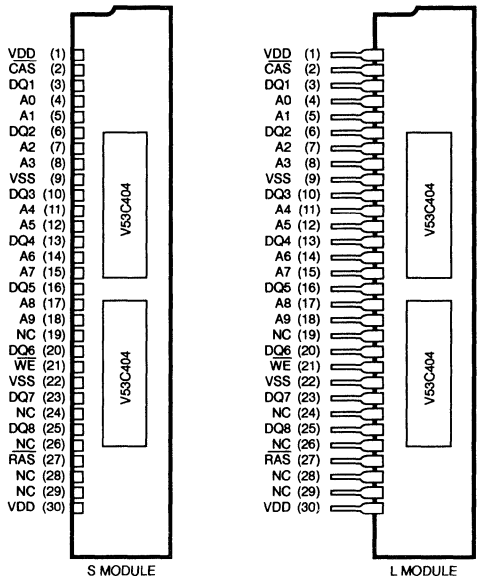
Device Usage Chart

Operating Temperature Range	Bit Organization		Module Type		Access Time (ns)				Power	
	x 8	x 9	S	L	60	70	80	100	Std	Low
0°C–70°C	•	•	•	•	•	•	•	•	•	•

Part Number Information



Pin Configuration x 8 Organization



Pin Names (x 8 Organization)

Name	Description
A0–A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobes
$\overline{WE}$	Write Enable
DQ1–DQ8	Data In/Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

Capacitance* (x8 Organization)

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		30	pF
C_{IN}	Input Capacitance, $\overline{RAS}$, $\overline{WE}$		30	pF
$C_{IN(DQ)}$	Input Capacitance, Data Inputs		15	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS}$		30	pF

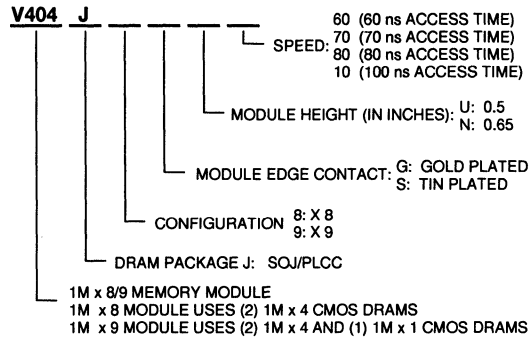
*Note: Capacitance is sampled and not 100% tested.

Absolute Maximum Ratings*

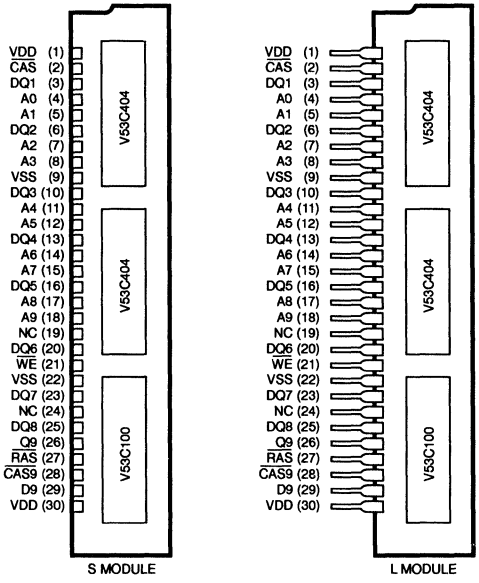
Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) .... –55°C to +125°C
Voltage Relative to V_{SS} ..... –1.0 to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 9.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Part Number Information



Pin Configuration x 9 Organization



Pin Names (x 9 Organization)

Name	Description
A0–A9	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobes
$\overline{WE}$	Write Enable
DQ1–DQ8	Data In/Data Out
D9	Data In
Q9	Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

Absolute Maximum Ratings*

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage Relative to V_{SS} .....–1.0 to +7.0 V
Data Out Current .....50 mA
Power Dissipation .....9.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

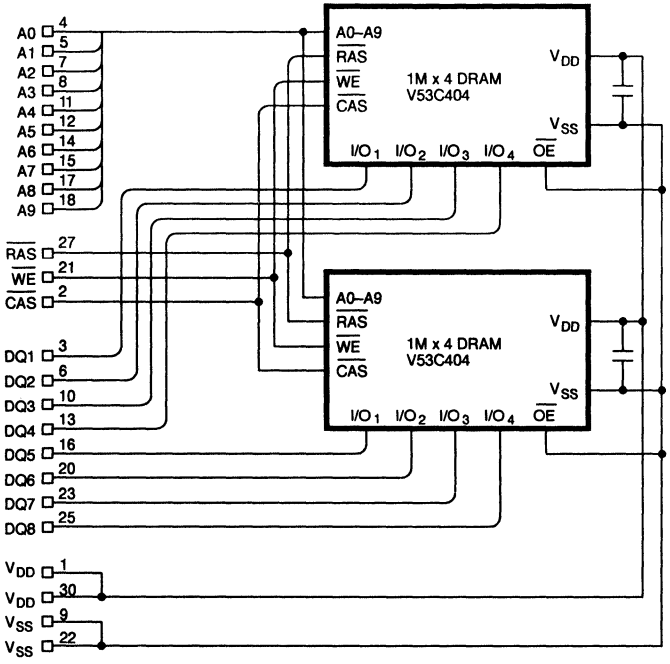
Capacitance* (x9 Organization)

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		30	pF
C_{IN}	Input Capacitance, $\overline{RAS}$, $\overline{WE}$		30	pF
$C_{IN(DQ)}$	Input Capacitance, Data Inputs		15	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS}$		30	pF
$C_{IN(CAS9)}$	Input Capacitance, $\overline{CAS9}$		10	pF
$C_{IN(D9)}$	Input Capacitance, D9		10	pF
$C_{O(Q9)}$	Output Capacitance, Q9		10	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.2		µF

*Note: Capacitance is sampled and not 100% tested.

Functional Diagram x 8 Organization



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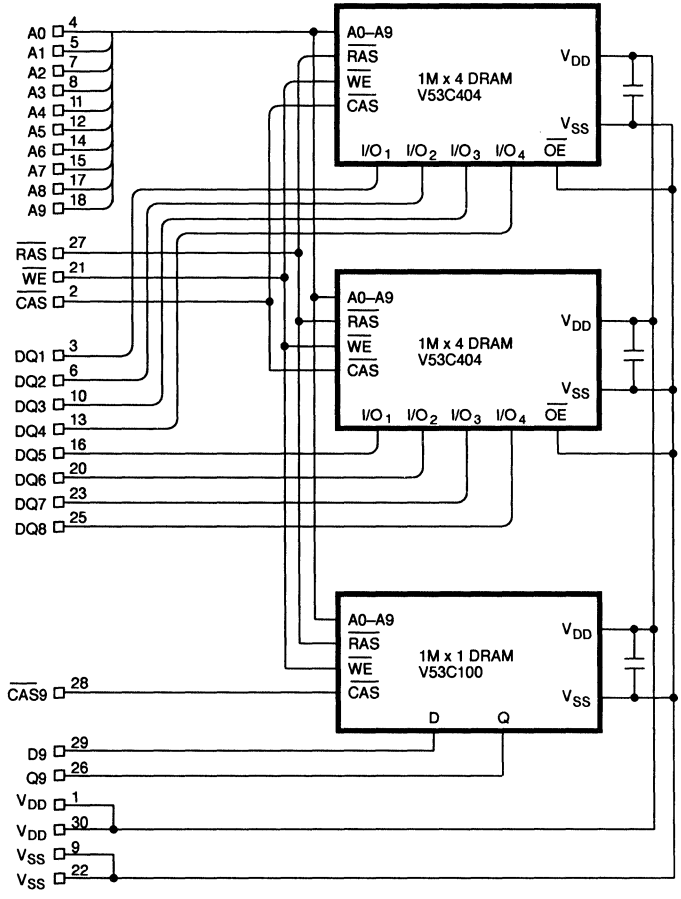
Functional Diagram x 9 Organization



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{DD} = 5 V ± 10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Power	Access Time	V404J8 Min.	V404J8 Max.	V404J9 Min.	V404J9 Max.	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)			–20	20	–30	30	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)			–10	10	–10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		60		190		280	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
			70		180		260			
			80		160		230			
			100		140		200			
I_{DD2}	V_{DD} Supply Current, TTL Standby				4		6	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh,		60		190		280	mA	$t_{RC} = t_{RC}$ (min.)	2
			70		180		260			
			80		160		230			
			100		140		200			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		60		190		270	mA	Minimum Cycle	1, 2
			70		160		250			
			80		140		200			
			100		120		175			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			10		13	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	
		LOW			8		10			
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD			2		3	mA	$\overline{RAS} \ge V_{DD} - 0.2$ V $\overline{CAS} \ge V_{DD} - 0.2$V other inputs ≥ V_{SS}	
		LOW			0.8		1			
I_{DD7}	Battery Back-up Data Retention Current (Only V404J8/9L)	LOW			1.2		1.5	mA	$\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle t_{RC} = 62.5 µs CMOS clock levels	18
V_{IL}	Input Low Voltage			–1.0	0.8	–1.0	0.8	V		3
V_{IH}	Input High Voltage			2.4	V_{DD}+1	2.4	V_{DD}+1	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage			2.4		2.4			I_{OH} = –5 mA	

4

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		100/100L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	60	75K	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	120		130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		50		60		70		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	60		70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	20	10K	20	10K	25	10K	ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20		20	50	20	60	25	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	15		20		20		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		15		20		20		25	ns	6,7
17	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		60		70		80		100	ns	6,8,9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		30		35		40		50	ns	6,7,10
19	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
20	t_{CH2QZ}	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	20	0	20	0	25	0	25	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	50		55		60		75		ns	
22	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	15	40	20	50	ns	11

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	60/60L		70/70L		80/80L		100/100L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	15		20		20		25		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		20		20		25		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	15		0		0		0		ns	12,13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	10		10		15		20		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	10		10		15		20		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	50		55		60		75		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15		20		20		25		ns	
30	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		15		20		ns	14
32	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	65		75		75		90		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		65		ns	
34	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		10		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	30		35		40		50		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		35		40		45		55	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	50		55		60		75		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	5		5		5		5		ns	
39	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5		5		5		5		ns	
40	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	15		15		15		15		ns	
41		t_{WRP}	$\overline{Write}$ to $\overline{RAS}$ Recharge Time	10		10		10		10		ns	
42		t_{WRH}	$\overline{Write}$ to $\overline{RAS}$ Hold Time	10		10		10		10		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
	t_{RI}		Refresh Interval (1024 Cycles)		16		16		16		16	ms	17

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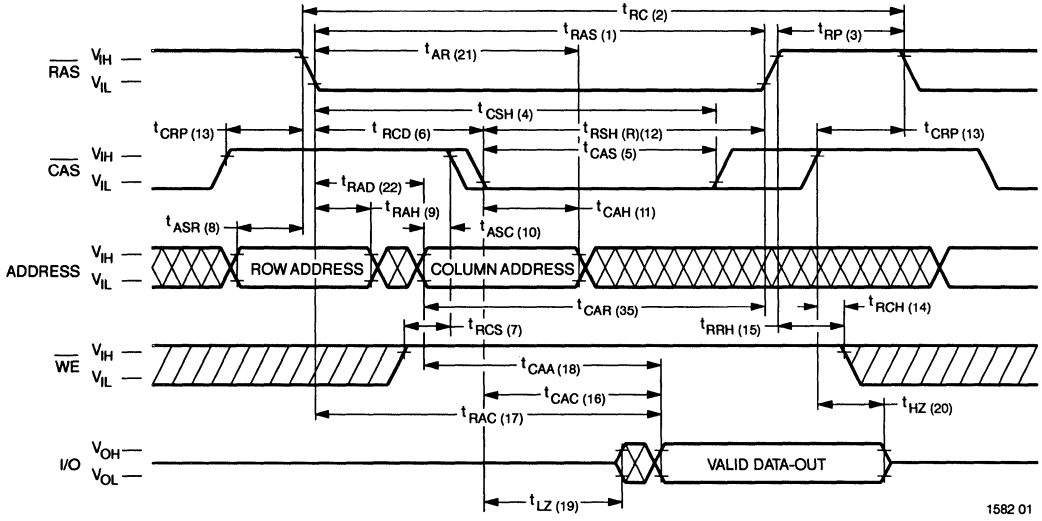
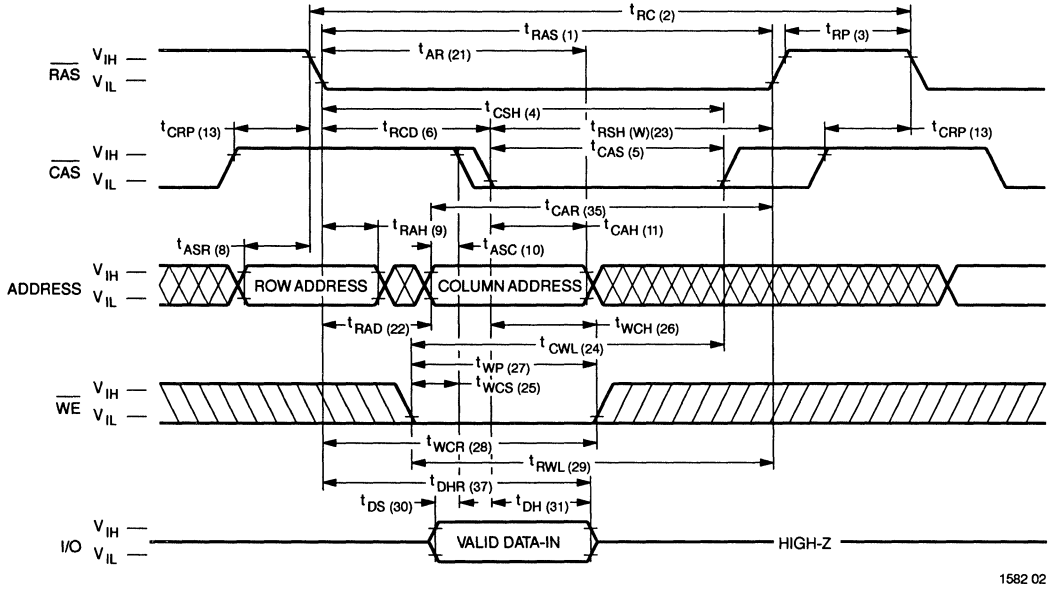
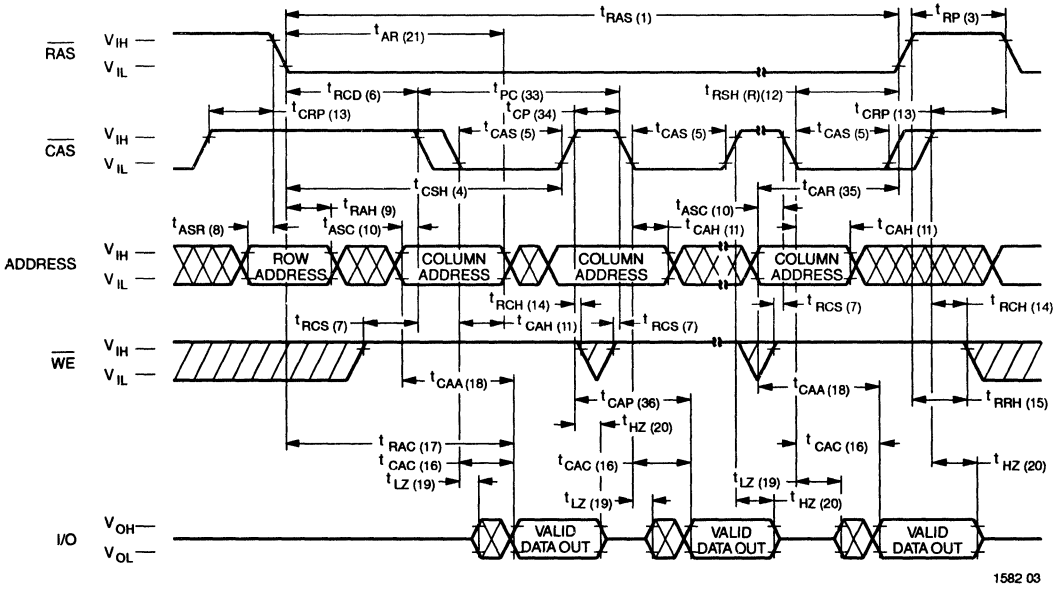
Waveforms of Read Cycle



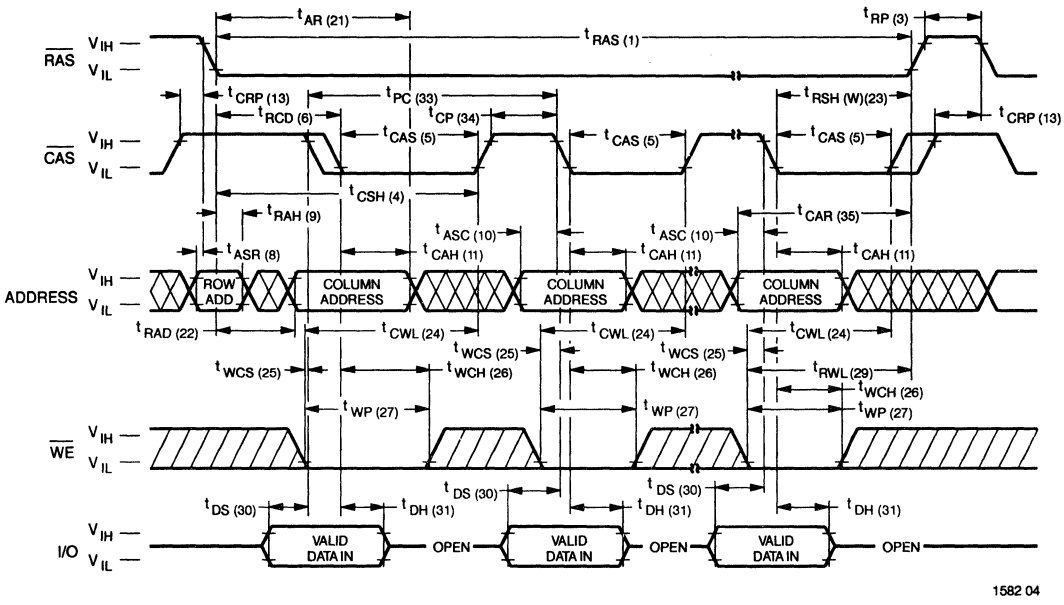
Waveforms of Early Write Cycle



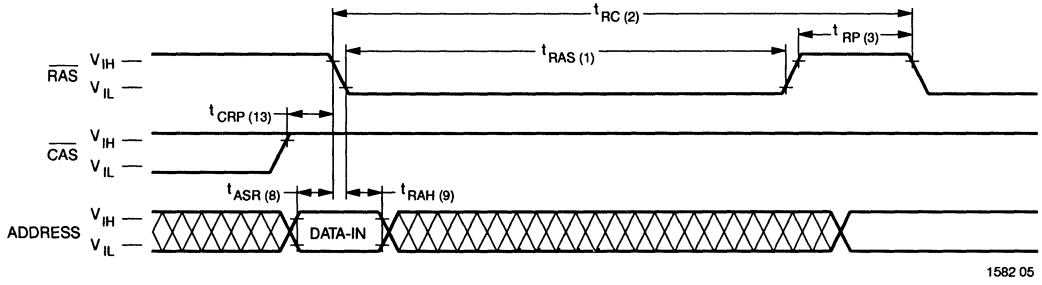
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle

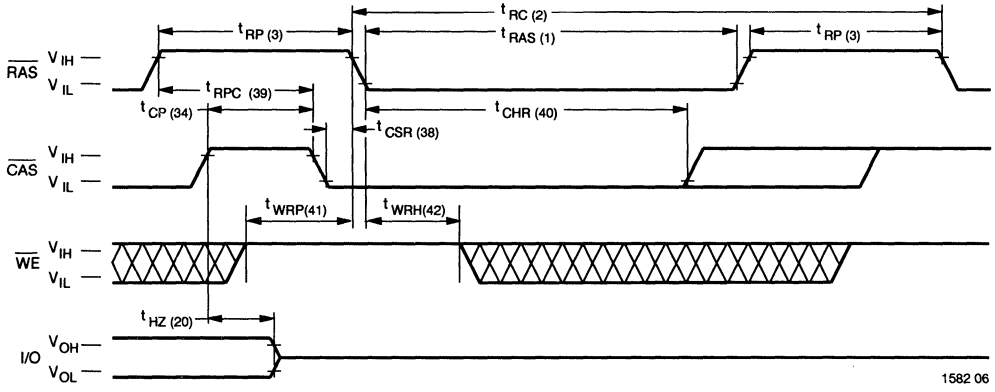


Waveforms of $\overline{RAS}$-Only Refresh Cycle



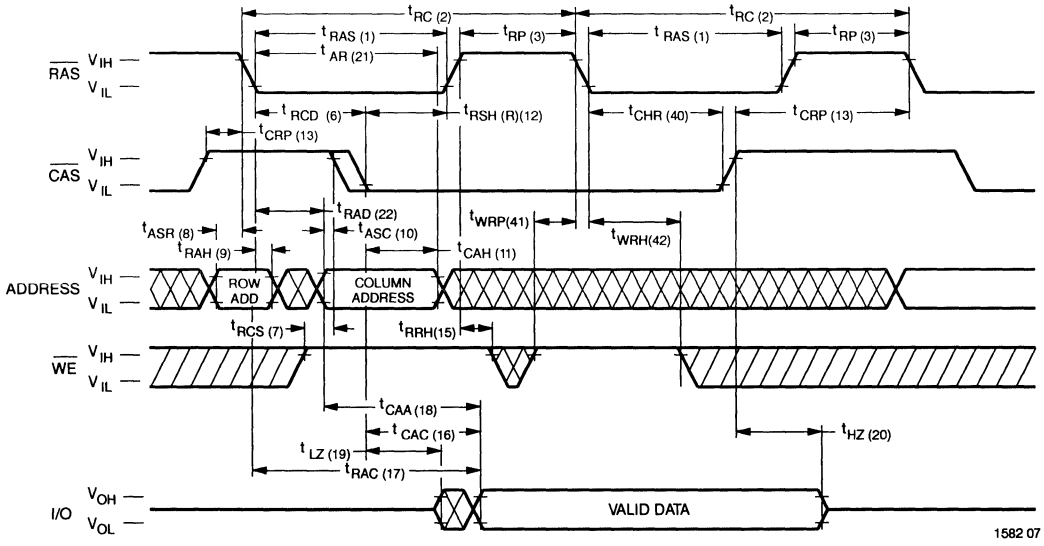
NOTE: $\overline{WE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

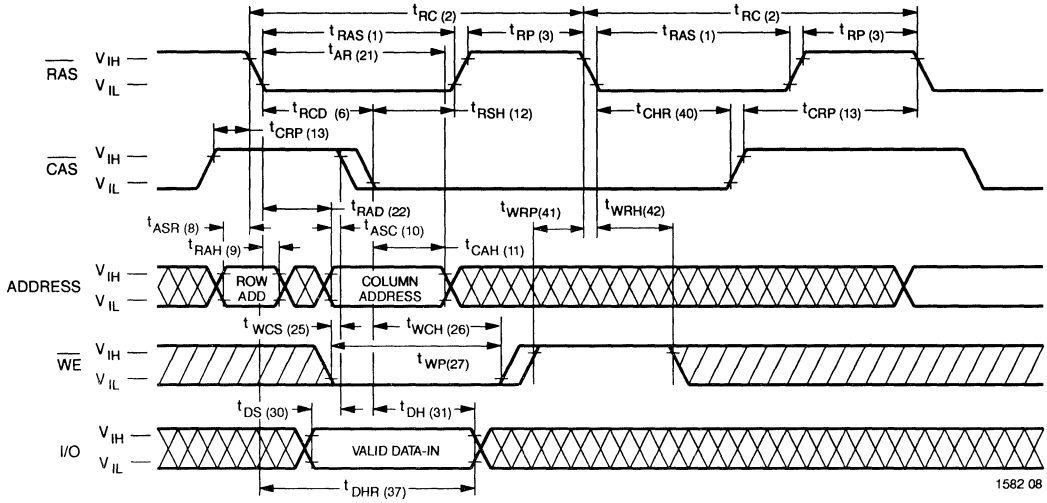


NOTE: A_0–A_9 = Don't care

Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



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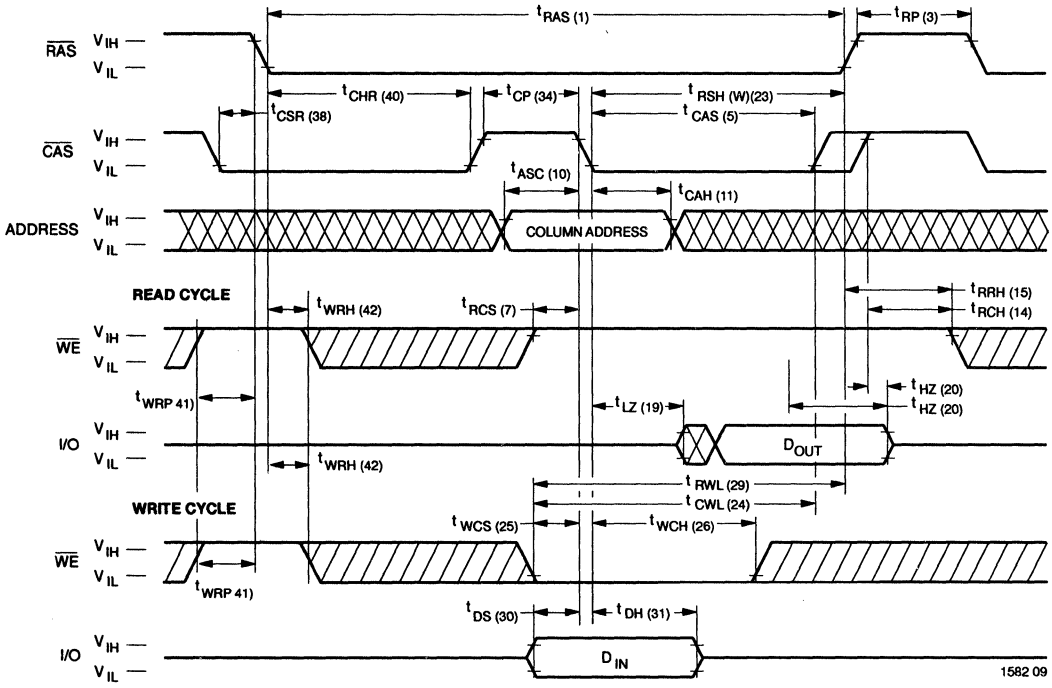
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit condition, and are not referenced to the output voltage levels.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
    t_{RC} = 62.5 µs (62.5 µs x 1024 = 64 ms)
    $t_{RAS} = t_{RAS}$ (min) to 1 µs
    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ $V_{IH} > V_{DD} - 0.2$ V
    $V_{IL} < 0.2$ V
    $\overline{WE}$ and $\overline{OE}$ $V_{IN} > V_{DD} - 0.2$ V
    All other inputs at stable V_{IH} or V_{IL}

4

Functional Description

The V404J8/9 are CMOS dynamic RAM modules for high data bandwidth, low power applications. The V404J8/9 reads and writes data by multiplexing an 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe ($\overline{RAS}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{CAS}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{CAS}$ edge occurs, the delay time from $\overline{RAS}$ to $\overline{CAS}$ has little effect on the access time.

Memory Cycle

A memory cycle is initiated by bringing $\overline{RAS}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum t_{RAS} time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time t_{RP}/t_{CP} has elapsed.

Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{WE}$) signal High during a $\overline{RAS}/\overline{CAS}$ operation. The column address must be held for a minimum specified by t_{AR}. Data Out becomes valid only when t_{OAC}, t_{RAC}, t_{CAA} and t_{CAC} are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by t_{CAA} when t_{RAC}, t_{CAC} and t_{OAC} are all satisfied.

Write Cycle

A Write Cycle is performed by taking $\overline{WE}$ and $\overline{CAS}$ low during a $\overline{RAS}$ operation. The column address is latched by $\overline{CAS}$. The Write Cycle can be $\overline{WE}$ controlled or $\overline{CAS}$ controlled depending on whether $\overline{WE}$ or $\overline{CAS}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. In the $\overline{CAS}$-controlled Write Cycle, when the leading edge of $\overline{WE}$ occurs prior to the $\overline{CAS}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{RAS}$ or $\overline{CAS}$ will maintain the output in the High-Z state.

In the $\overline{WE}$ controlled Write Cycle, $\overline{OE}$ must be in the high state and t_{OED} must be satisfied.

Refresh Cycle

To retain data, 1024 Refresh Cycles are required in each 16 ms period. There are two ways to refresh the memory:

1. By clocking each of the 1024 row addresses (A_0 through A_9) with $\overline{RAS}$ at least once every 16 ms. Any Read, Write, Read-Modify-Write or $\overline{RAS}$-only cycle refreshes the addressed row.
2. Using a $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle. If $\overline{CAS}$ makes a transition from low to high to low after the previous cycle and before $\overline{RAS}$ falls, $\overline{CAS}$-before-$\overline{RAS}$ refresh is activated. The V404J8/9 uses the output of an internal 10-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$-before-$\overline{RAS}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{CAS}$-before-$\overline{RAS}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

Data Retention Mode

The V404J8/9 offers a CMOS standby mode that is entered by causing the $\overline{RAS}$ clock to swing between a valid V_{IL} and an "extra high" V_{IH} within 0.2 V of V_{DD}. While the $\overline{RAS}$ clock is at the "extra high" level, the V404J8/9 power consumption is reduced to the low I_{DD6} level. Overall I_{DD} consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: t_{RC} = Refresh Cycle Time
t_{RX} = Refresh Interval / 1024

Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating t_{ASC} and t_T from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is t_{CAA} or t_{CAP} controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by t_{CAP}. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by t_{CAA}. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 20 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

Data Output Operation

The V404J8/9 Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time (t_{DS}) to be satisfied.

Power-On

After application of the V_{DD} supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the V_{DD} current requirement of the V404J8/9 is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and I_{DD} will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{DD} or be held at a valid V_{IH} during Power-On to avoid current surges.

Table 1. V404J8/9 Data Output
Operation for Various Cycle Types

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{CAS}$-Controlled Write Cycle (Early Write)	High-Z
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
$\overline{RAS}$-only Refresh	High-Z
$\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle	Data remains as in previous cycle
$\overline{CAS}$-only Cycles	High-Z

4

V404J32 and V404J36
1M x 32 and 1M x 36
CMOS MEMORY MODULES

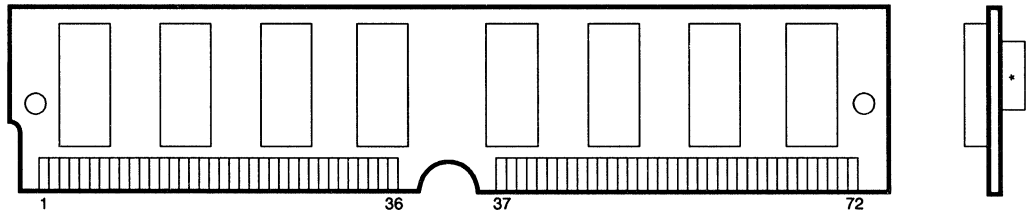
Features

- 1,048,576 x 32/36 bit organization
- Utilizes 1M x 4 CMOS DRAMs
- Fast access times: 80 ns, 100 ns
- Fast Page mode operation
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, and Hidden refresh capability
- Single 5 V ±10% supply
- All I/O are fully TTL compatible
- Standard 72-lead single-in-line module

Description

The V404J32 memory Module is organized as 1,048,576 x 32 bits in a 72-lead single-in-line module. The 1M x 32 memory module uses 8 Mosel-Vitelic 1M x 4 DRAMs. The V404J36 Memory Module is organized as 1,048,576 x 36 bits in a 72-lead single-in-line module. The 1M x 36 memory module uses 8 Mosel-Vitelic 1M x 4 DRAMs and 4 Mosel-Vitelic 1M x 1 DRAMs. The x36 modules are ideal for use in i486 systems where high memory density and fast access times are needed.

V404J32/36
Pin Configuration



* V404J36 only

1	VSS	19	NC	37	NC [DQ17]	55	DQ12
2	DQ0	20	DQ4	38	NC [DQ35]	56	DQ30
3	DQ18	21	DQ22	39	$\overline{VSS}$	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	VDD
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	VDD	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{W}$	65	DQ16
12	A0	30	VDD	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	*1
14	A2	32	A9	50	DQ27	68	*2
15	A3	33	NC	51	DQ10	69	*3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	*4
17	A5	35	NC [DQ26]	53	DQ11	71	NC
18	A6	36	NC [DQ8]	54	DQ29	72	VSS

V404J32/36

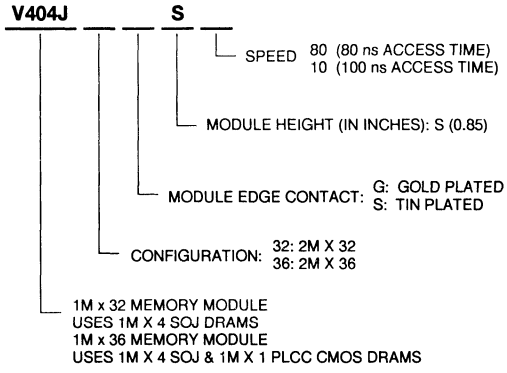
	-80	-10
*1	VSS	VSS
*2	VSS	VSS
*3	NC	VSS
*4	VSS	VSS

* Presence detection. Pin connection change is available on request.

Device Usage Chart

Operating Temperature Range	Organization		Module Type	Access Time (ns)		Power	
	1M x 32	1M x 36	S	80	100	Std	Low
0°C–70°C	•	•	•	•	•	•	•

Part Number Information



Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) ..... −55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... −1.0 to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... −1.0 to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 12.0 W

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

Pin Names

Name	Description
A0–A9	Address Inputs
$\overline{RAS}$, $\overline{RAS2}$	Row Address Strobes
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobes
$\overline{W}$	Read/Write Input
DQ0–DQ35	Data In/Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

Capacitance*

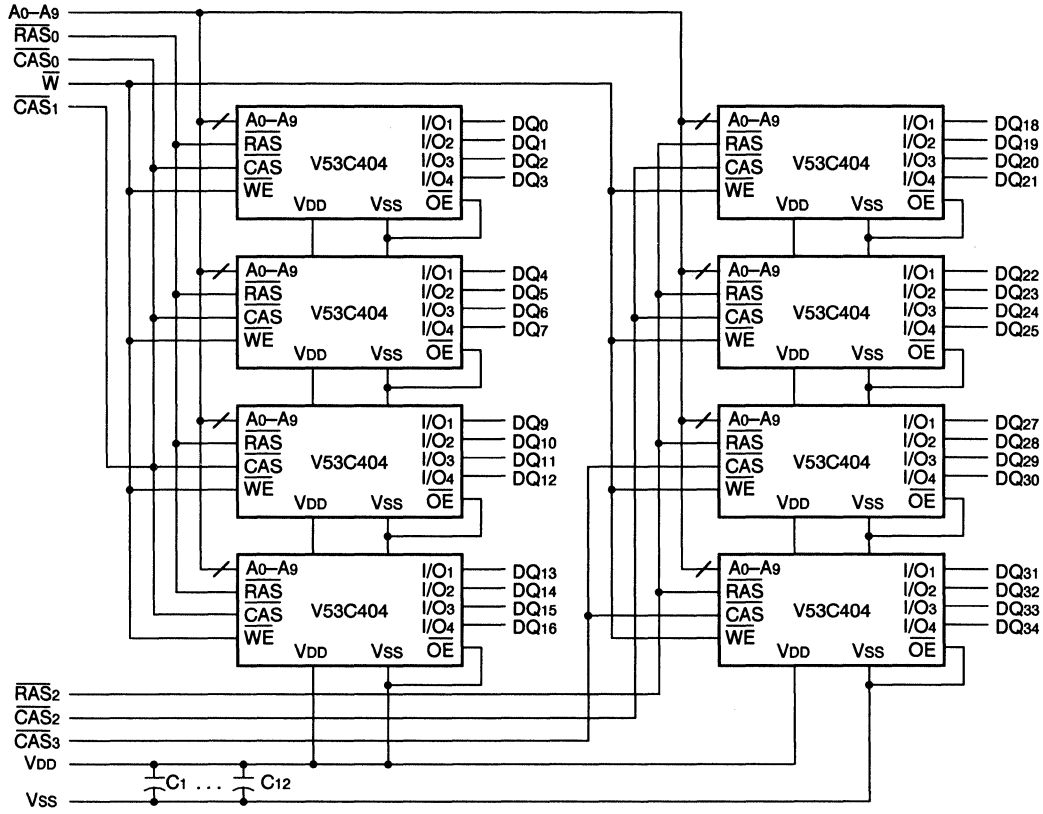
T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		90	pF
C_{IN}	Input Capacitance, $\overline{W}$		110	pF
$C_{(DQ)}$	Input/Output Capacitance, DQ0–DQ35		17	pF
$C_{IN(RAS)}$	Input Capacitance, $\overline{RAS0}$, $\overline{RAS2}$		65	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS0}$–$\overline{CAS3}$		50	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.2		µF

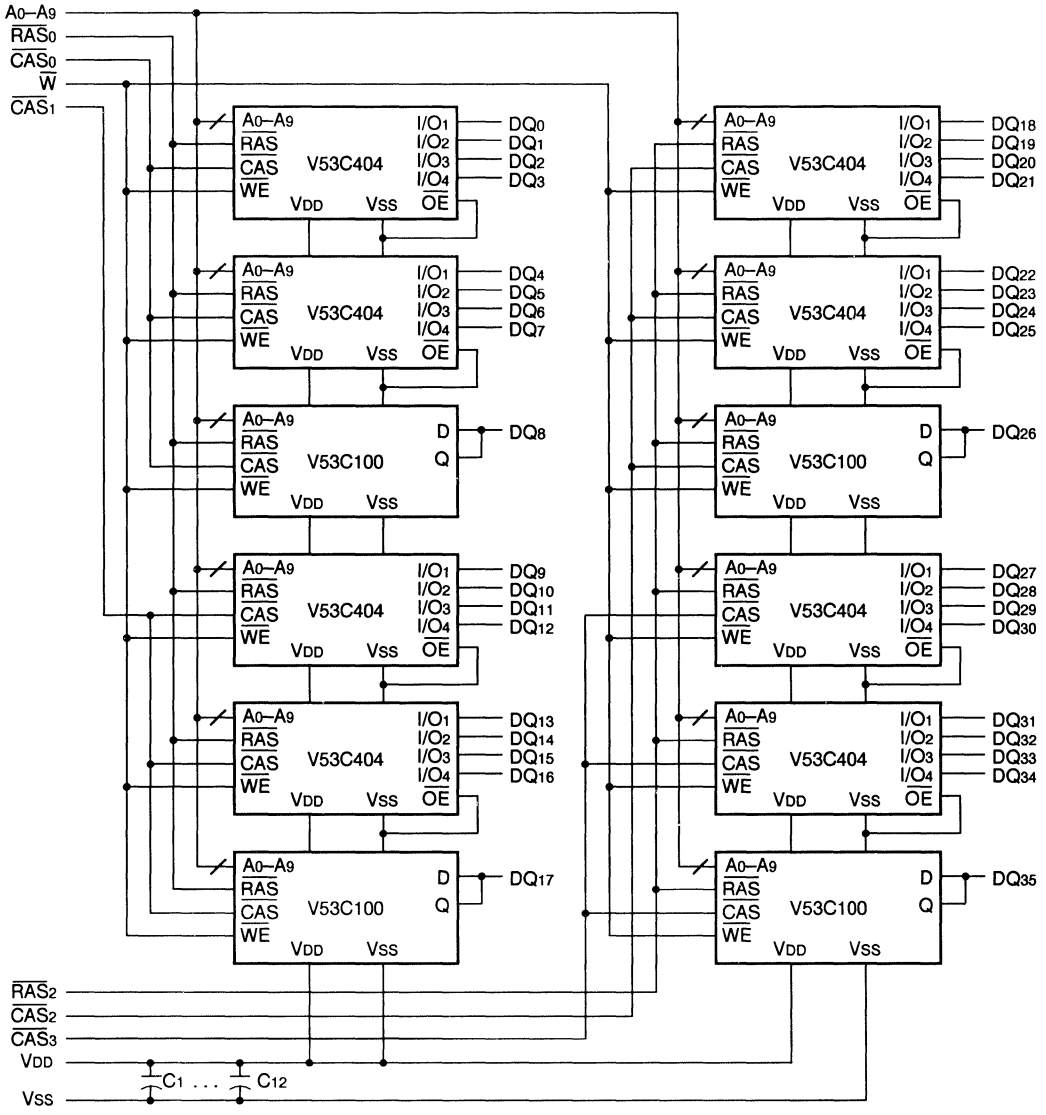
***Note:** Capacitance is sampled and not 100% tested

4

V404J32 Functional Diagram



V404J36 Functional Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Power	Access Time (ns)	V404J32 Min.	V404J32 Max.	V404J36 Min.	V404J36 Max.	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)			–80	80	–120	120	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)			–10	10	–10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		80		970		1080	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
			100		860		960			
I_{DD2}	V_{DD} Supply Current, TTL Standby	STD			27		30	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			22		24			
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh		80		970		1080	mA	$t_{RC} = t_{RC}$ (min.)	2
			100		860		960			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		80		680		760	mA	Minimum Cycle	1, 2
			100		630		700			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			36		40	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL}	1
		LOW			23		26		other inputs ≥ V_{SS}	
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD			18		20	mA	$\overline{RAS} \ge V_{DD}$–0.2 V, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			11.5		12.8			
V_{IL}	Input Low Voltage (all inputs)			–1	0.8	–1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)			2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage			2.4		2.4		V	I_{OH} = –5 mA	

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted.
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	160		190		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	70		80		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	25	60	30	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	15		20		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	20		25		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		15		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		25	ns	6, 7
17	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		80		100	ns	6, 8, 9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		40		45	ns	6, 7, 10
19	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	5		5		ns	16
20	t_{CH2QZ}	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	25	0	25	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	65		75		ns	
22	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	20	40	25	55	ns	11

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AC Characteristics (Cont'd.)

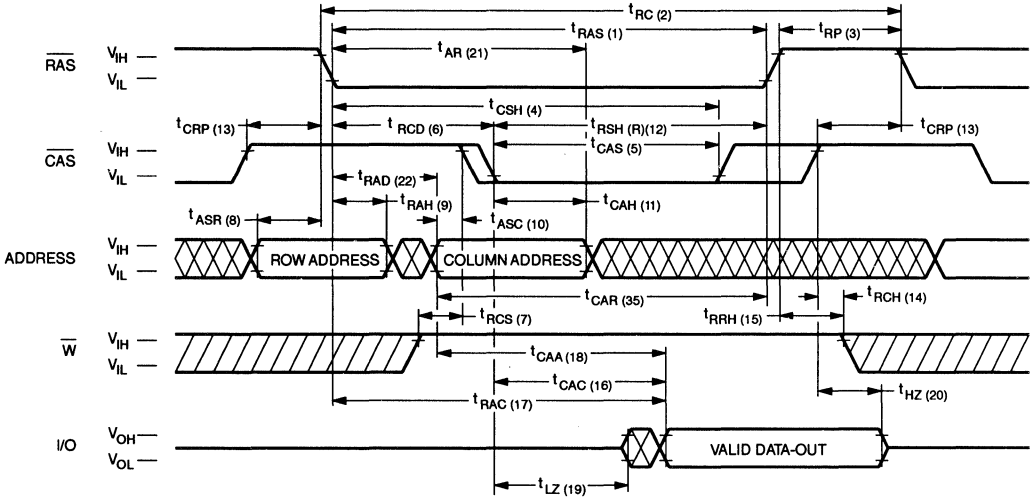
#	JEDEC Symbol	Symbol	Parameter	80/80L		10/10L		Unit	Notes
				Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		25		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		ns	12, 13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		20		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		20		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	60		75		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		ns	
30	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	20		25		ns	14
32	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	80		95		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	50		55		ns	
34	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	15		20		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	45		50		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		45		50	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	65		75		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		ns	
39	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		ns	
40	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (1024 Cycles)		16		16	ms	17

Notes:

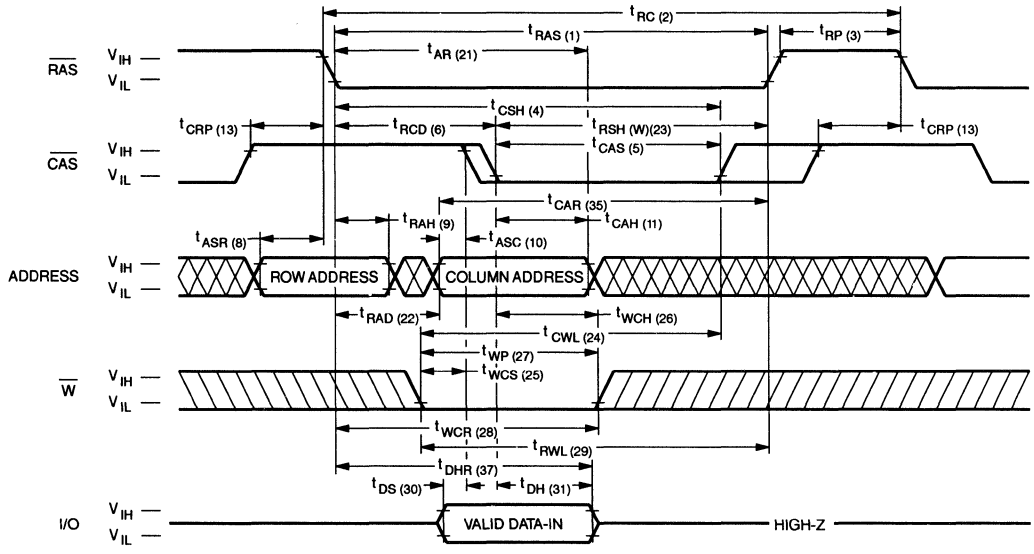
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit and are not referenced to the output voltage levels.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

4

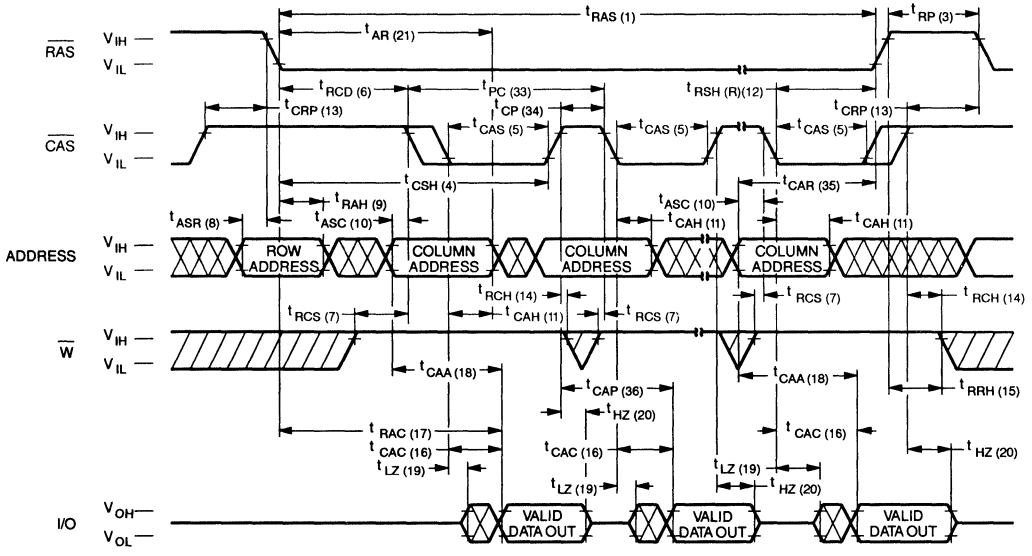
Waveforms of Read Cycle



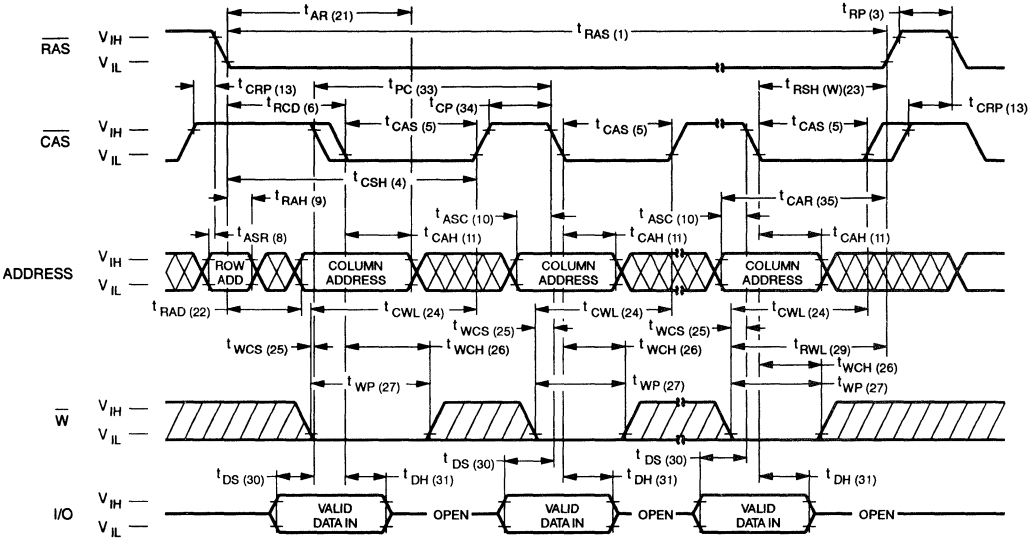
Waveforms of Early Write Cycle



Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle



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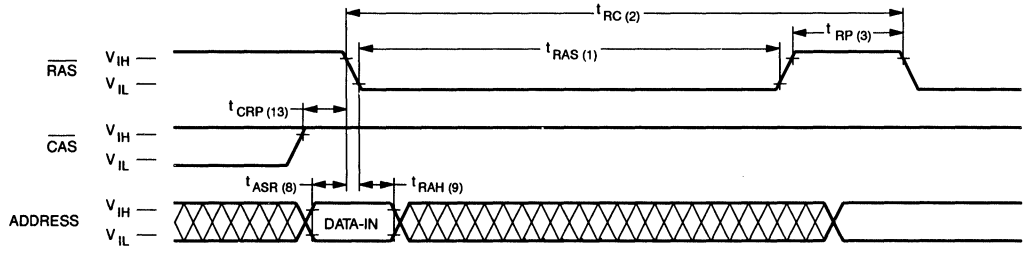
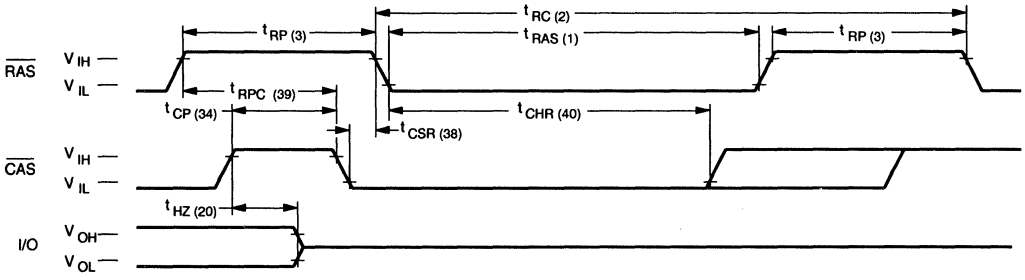
Waveforms of $\overline{RAS}$-Only Refresh Cycle



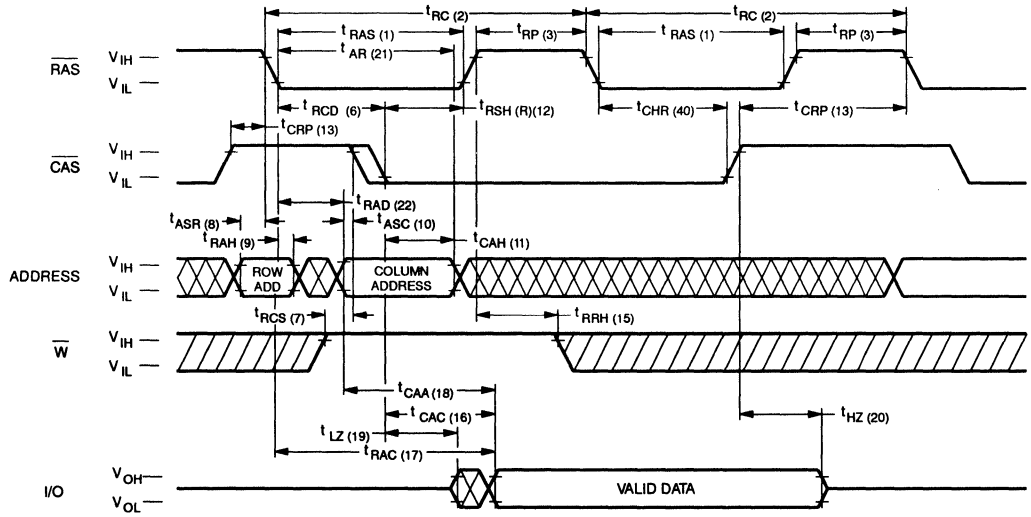
NOTE: $\overline{W}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

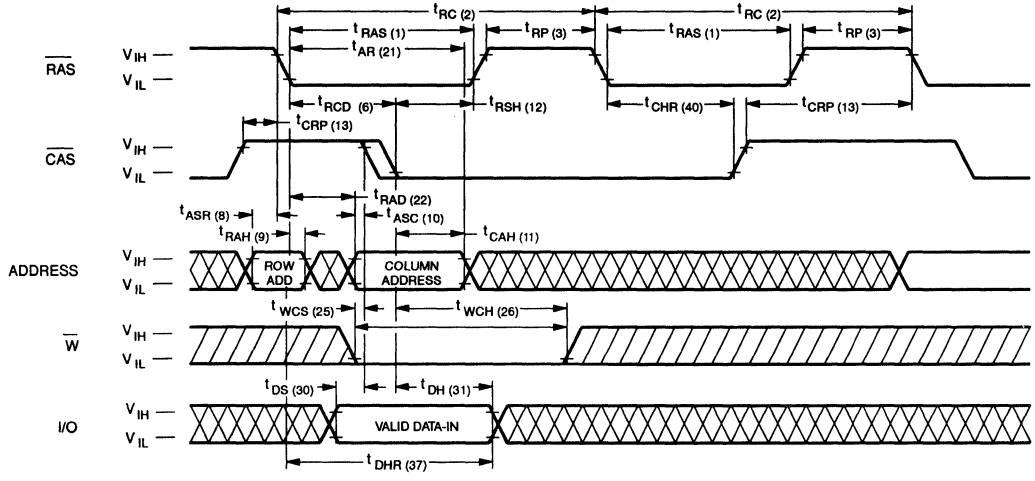


NOTE: $\overline{W}$, A_0 –A_9 = Don't care

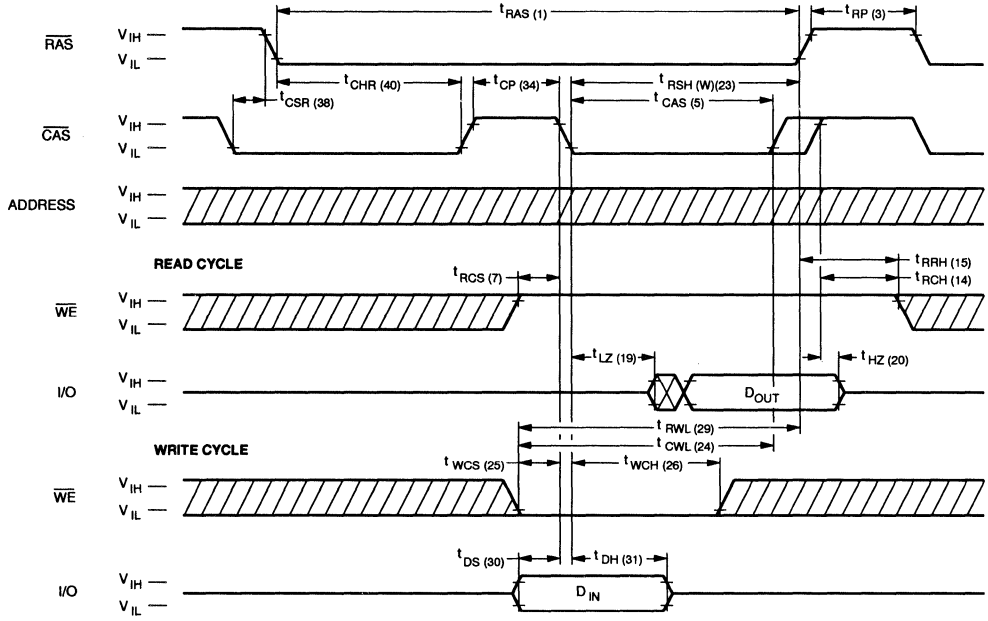
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



V404J232 and V404J236
2M x 32 and 2M x 36
CMOS MEMORY MODULES

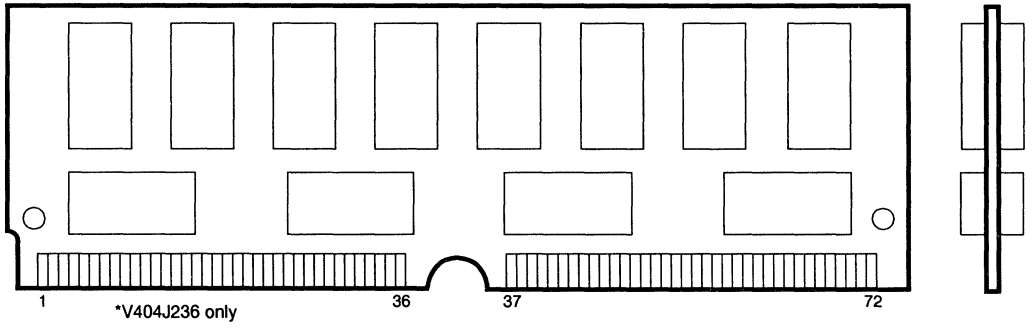
Features

- 2,097,152 x 32/36 bit organization
- Utilizes 1M x 4 CMOS DRAMs
- Fast access times: 70 ns, 80 ns
- Fast Page mode operation
- Low power dissipation
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{RAS}$ only refresh, and Hidden refresh capability
- Single 5 V ±10% supply
- All I/O are fully TTL compatible
- Standard 72-lead single-in-line module

Description

The V404J232 memory Module is organized as 2,097,152 x 32 bits in a 72-lead single-in-line module. The 2M x 32 memory module uses 16 Mosel-Vitelic 1M x 4 DRAMs. The V404J236 Memory Module is organized as 2,097,152 x 36 bits in a 72-lead single-in-line module. The 2M x 36 memory module uses 16 Mosel-Vitelic 1M x 4 DRAMs and 8 Mosel-Vitelic 1M x 1 DRAMs. The x36 modules are ideal for use in i486 systems where high memory density and fast access times are needed.

V404J232/236
Pin Configuration



1	VSS	19	NC	37	NC* [DQ17]	55	DQ12
2	DQ0	20	DQ4	38	NC* [DQ35]	56	DQ30
3	DQ18	21	DQ22	39	VSS	57	DQ13
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ31
5	DQ19	23	DQ23	41	$\overline{CAS2}$	59	VDD
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ32
7	DQ20	25	DQ24	43	$\overline{CAS1}$	61	DQ14
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ33
9	DQ21	27	DQ25	45	NC	63	DQ15
10	VDD	28	A7	46	NC	64	DQ34
11	NC	29	NC	47	$\overline{W}$	65	DQ16
12	A0	30	VDD	48	NC	66	NC
13	A1	31	A8	49	DQ9	67	*1
14	A2	32	A9	50	DQ27	68	*2
15	A3	33	NC	51	DQ10	69	*3
16	A4	34	$\overline{RAS2}$	52	DQ28	70	*4
17	A5	35	NC* [DQ26]	53	DQ11	71	NC
18	A6	36	NC* [DQ8]	54	DQ29	72	VSS

*NC for V404J232

V404J232/V404J236

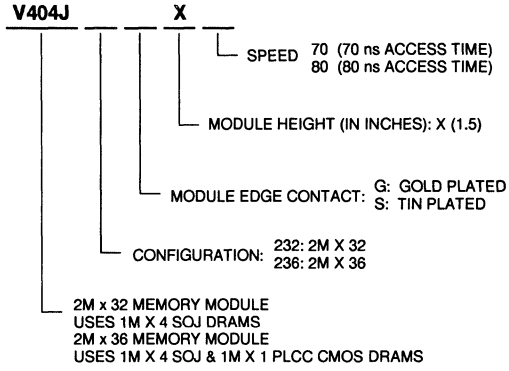
	-70	-80
*1	NC	NC
*2	NC	NC
*3	VSS	NC
*4	NC	VSS

* Presence detection. Pin connection change is available on request.

Device Usage Chart

Operating Temperature Range	Organization		Module Type	Access Time (ns)		Power
	2M x 32	2M x 36	S	70	80	S
0°C–70°C	•	•	•	•	•	•

Part Number Information



Absolute Maximum Ratings*

Ambient Temperature
Under Bias ..... −10°C to +80°C
Storage Temperature (plastic) ..... −55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} ..... −1.0 to +7.0 V
Voltage on V_{DD} relative to V_{SS} ..... −1.0 to +7.0 V
Data Out Current ..... 50 mA
Power Dissipation ..... 12.0 W

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

Pin Names

Name	Description
A0–A9	Address Inputs
$\overline{RAS}$, $\overline{RAS2}$	Row Address Strobes
$\overline{CAS0}$–$\overline{CAS3}$	Column Address Strobes
$\overline{W}$	Read/Write Input
DQ0–DQ35	Data In/Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

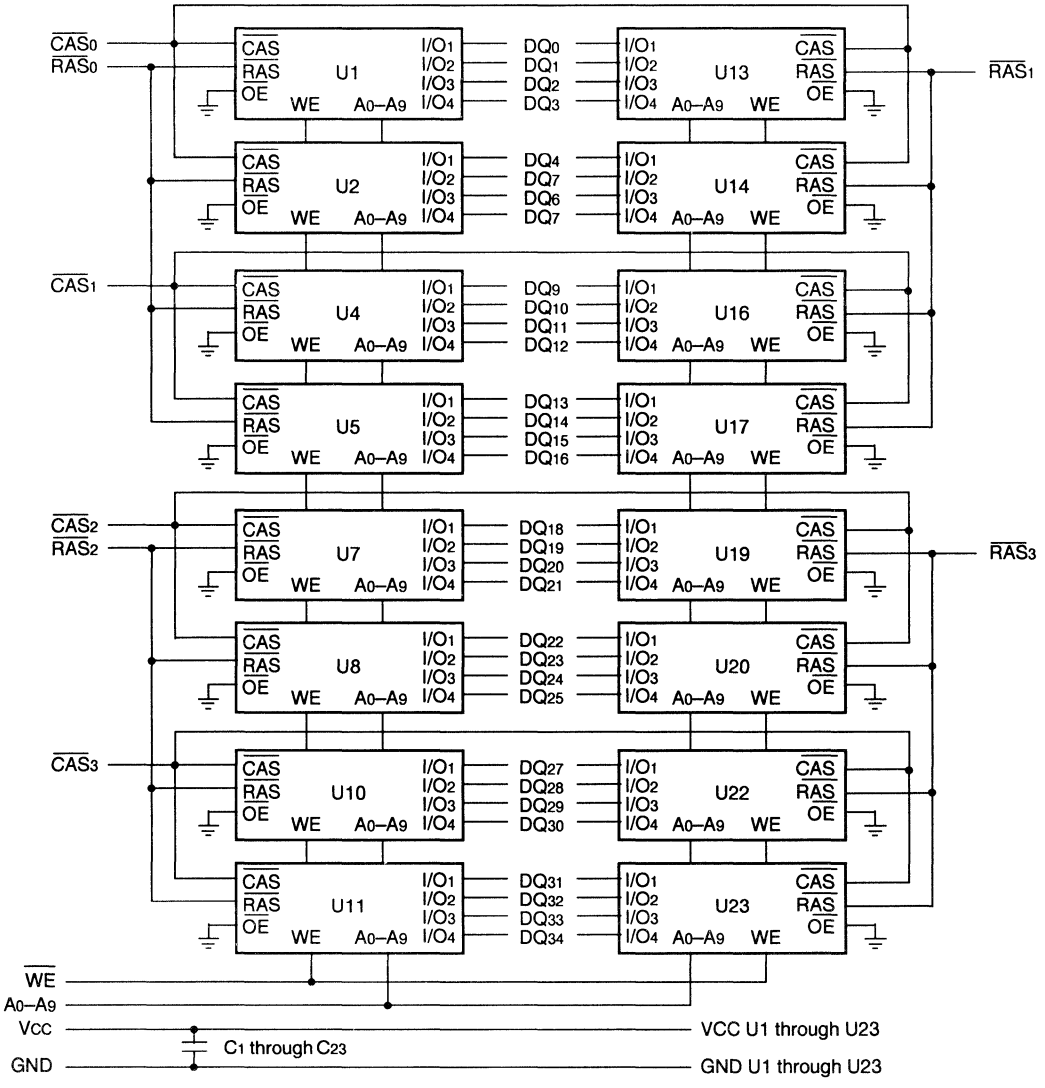
Capacitance*

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

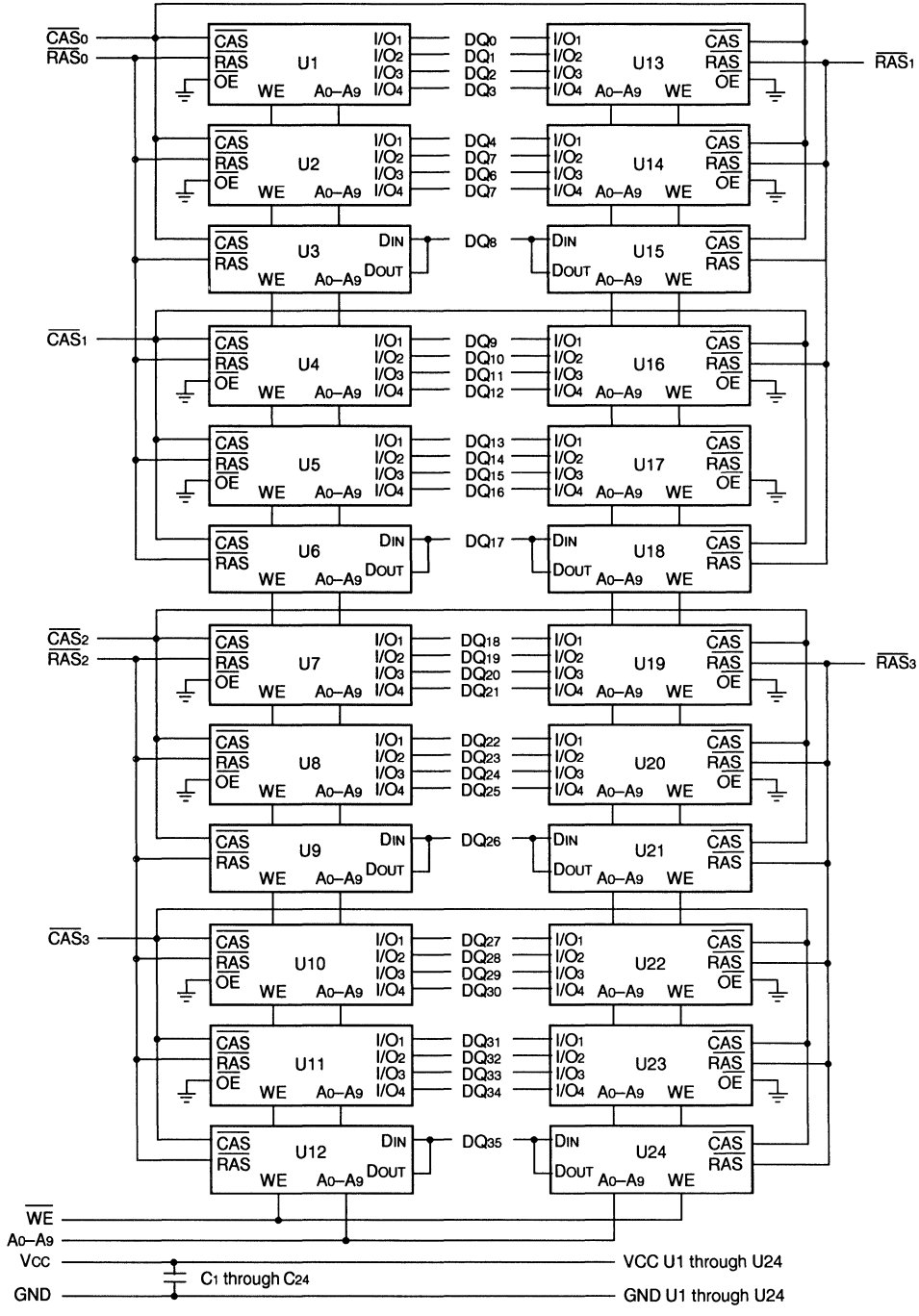
Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		180	pF
C_{IN}	Input Capacitance, $\overline{W}$		220	pF
$C_{(DQ)}$	Input/Output Capacitance, DQ0–DQ35		34	pF
$C_{IN(RAS)}$	Input Capacitance, $\overline{RAS0}$, $\overline{RAS2}$		130	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS0}$–$\overline{CAS3}$		100	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.2		µF

***Note:** Capacitance is sampled and not 100% tested

V404J232 Functional Diagram



V404J236 Functional Diagram



DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time (ns)	V404J232 Min.	V404J232 Max.	V404J236 Min.	V404J236 Max.	Unit	Test Conditions	Notes
I_{LI}	Input Leakage Current (any input pin)		–160	160	–240	240	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)		–20	20	–20	20	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating	70		1940		3240	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		80		1720		1920			
I_{DD2}	V_{DD} Supply Current, TTL Standby			54		60	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{DD3}	V_{DD} Supply Current,	70		1940		3240	mA	$t_{RC} = t_{RC}$ (min.)	2
	$\overline{RAS}$-Only Refresh	80		1720		1920			
I_{DD4}	V_{DD} Supply Current, Fast	70		1360		1520	mA	Minimum Cycle	1, 2
	Page Mode Operation	80		1260		1400			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled			72		80	mA	$\overline{RAS}$=V_{IH}, $\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
I_{DD6}	V_{DD} Supply Current, CMOS Standby			36		40	mA	$\overline{RAS} \ge V_{DD}$–0.2 V, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage (all inputs)		–1	0.8	–1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)		2.4	V_{DD} +1	2.4	V_{DD} +1	V		3
V_{OL}	Output Low Voltage			0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage		2.4		2.4		V	I_{OH} = –5 mA	

4

AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise noted.
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	70		80		Unit	Notes
				Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	130		150		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20		20	60	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		20		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20	ns	6, 7
17	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		70		80	ns	6, 8, 9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40	ns	6, 7, 10
19	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		0		ns	16
20	t_{CH2QZ}	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	25	0	25	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		ns	
22	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	20	40	ns	11

AC Characteristics (Cont'd.)

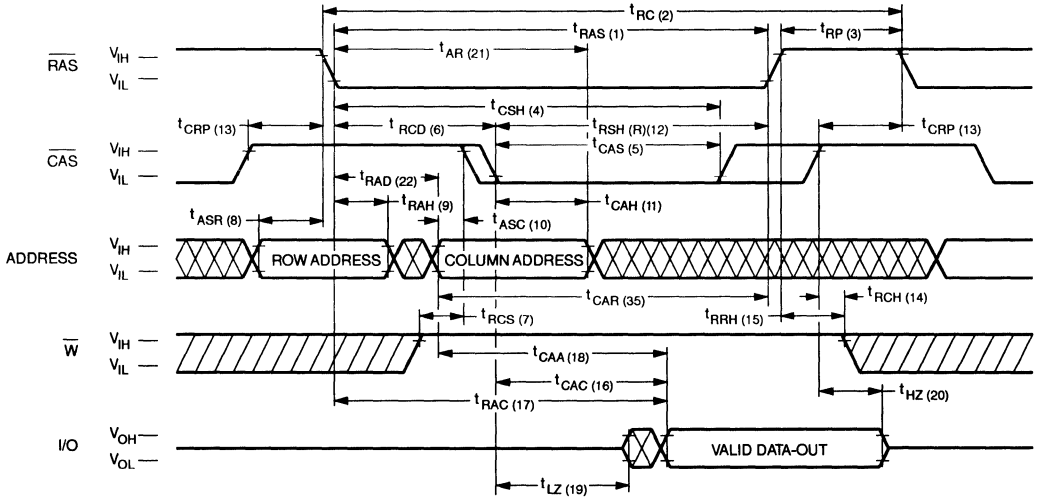
#	JEDEC Symbol	Symbol	Parameter	70		80		Unit	Notes
				Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15		15		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		ns	12, 13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		ns	
30	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	15		20		ns	14
32	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	75		80		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		55		ns	
34	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55		60		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	5		5		ns	
39	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	5		5		ns	
40	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	15		15		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (1024 Cycles)		16		16	ms	17

4

Notes:

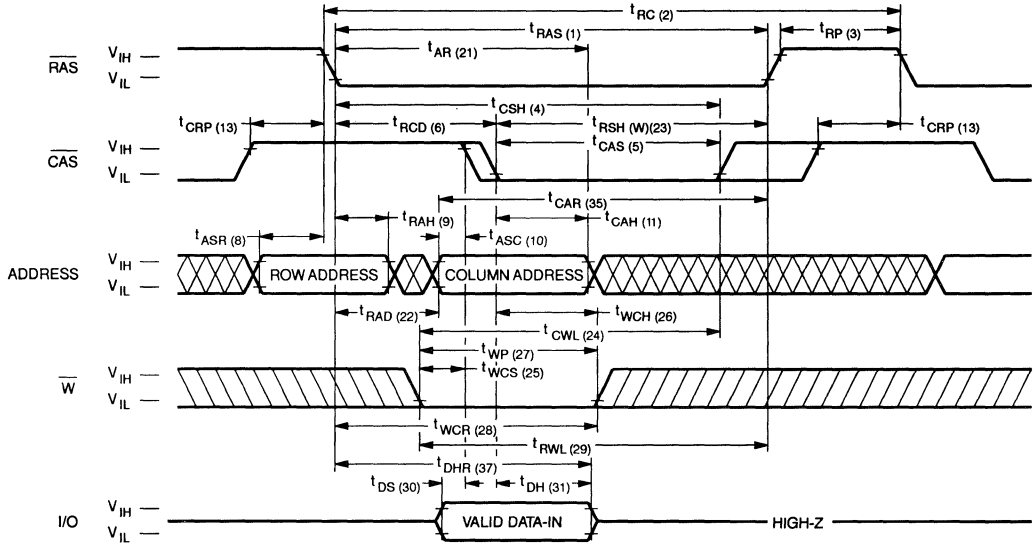
1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit and are not referenced to the output voltage levels.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

Waveforms of Read Cycle

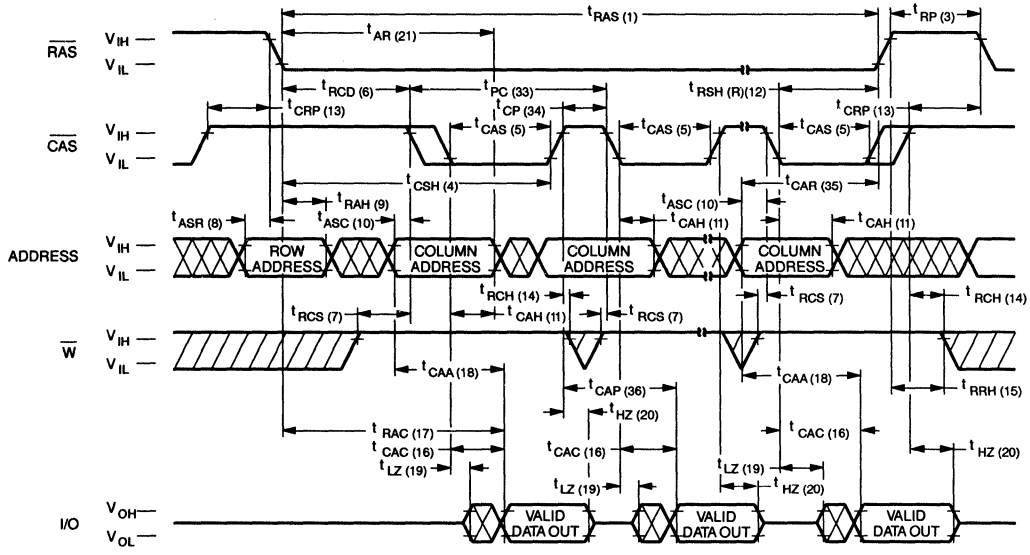


4

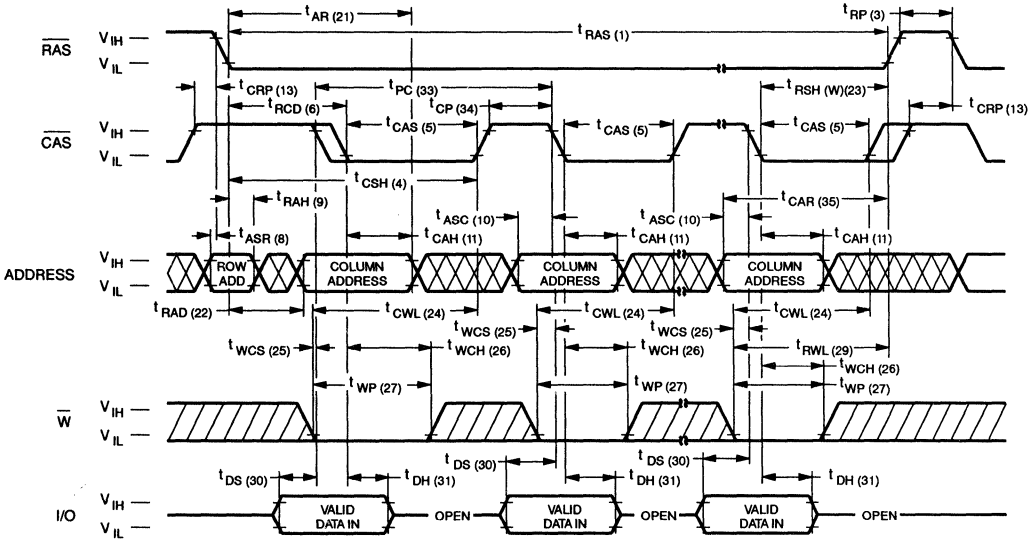
Waveforms of Early Write Cycle



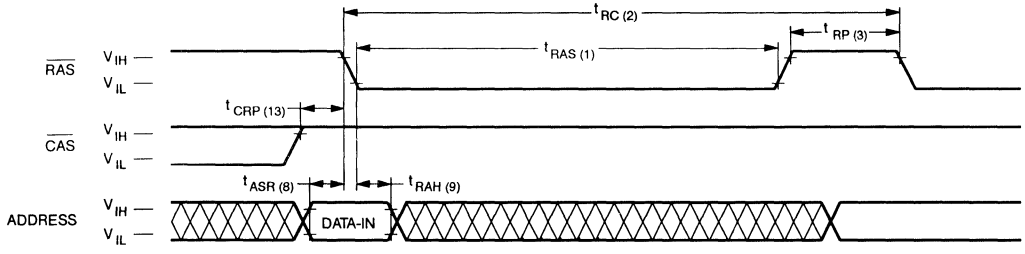
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle

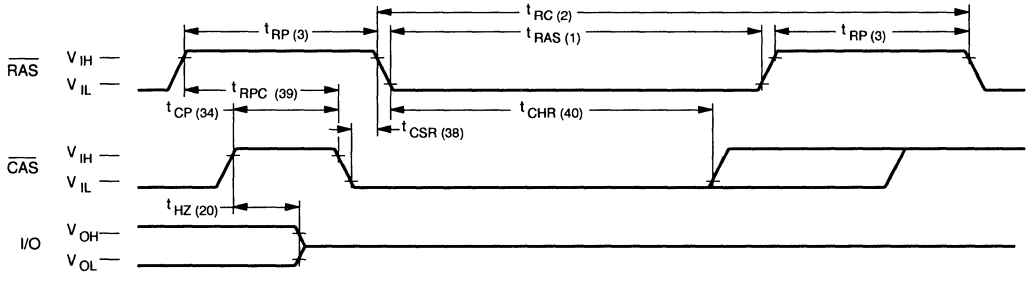


Waveforms of $\overline{RAS}$-Only Refresh Cycle



NOTE: $\overline{W}$ = Don't care

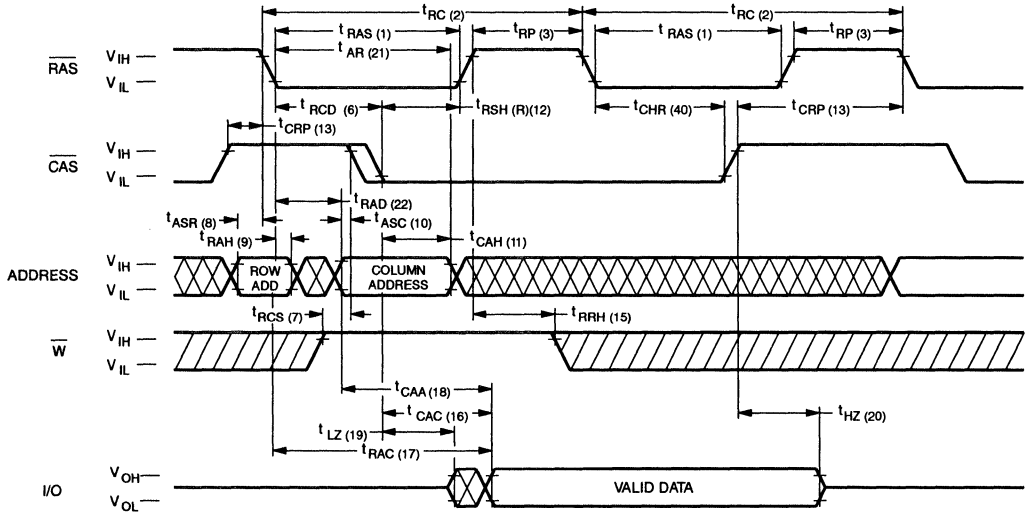
Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



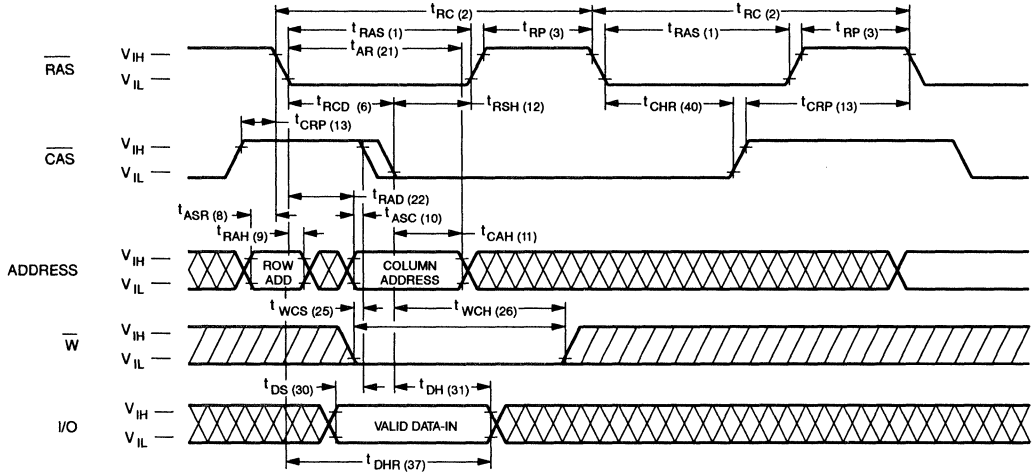
NOTE: $\overline{W}$, A_0–A_9 = Don't care

4

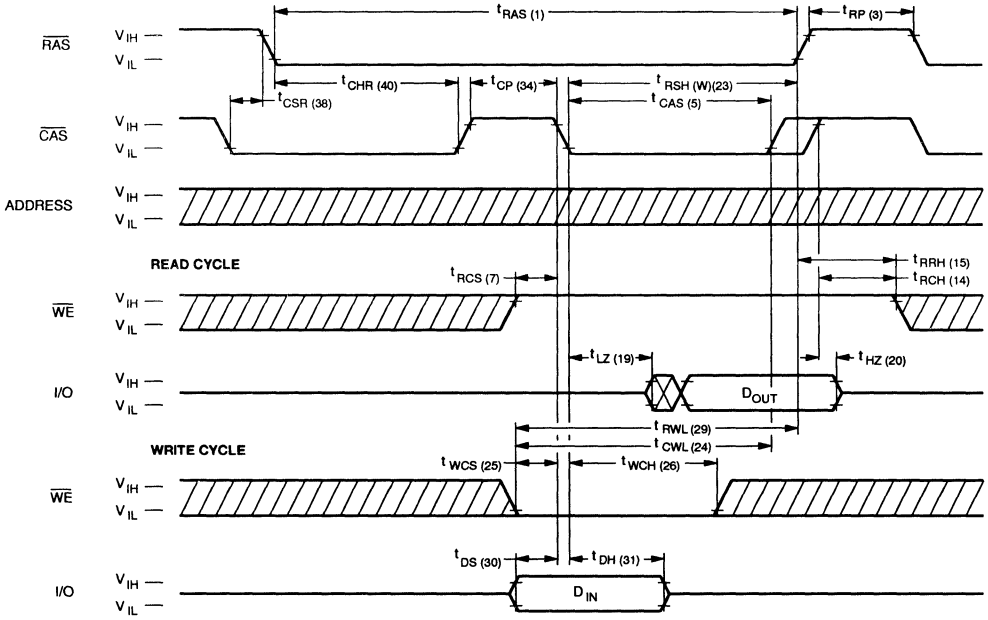
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



4

MS6264A
8K x 8 HIGH SPEED CMOS STATIC RAM

Features

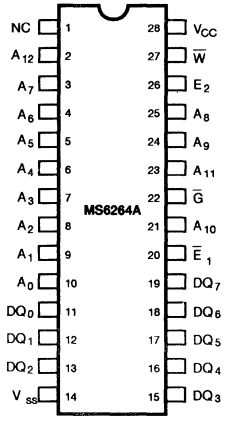
- High-speed – 15/20/25/35 ns
- Low Power dissipation:
  - — 825mW (Max.) Operating
  - — 550μW (Max.) Power Down
- 5V ± 10% supply
- Fully static operation
- TTL compatible I/O
- Three state outputs

Description

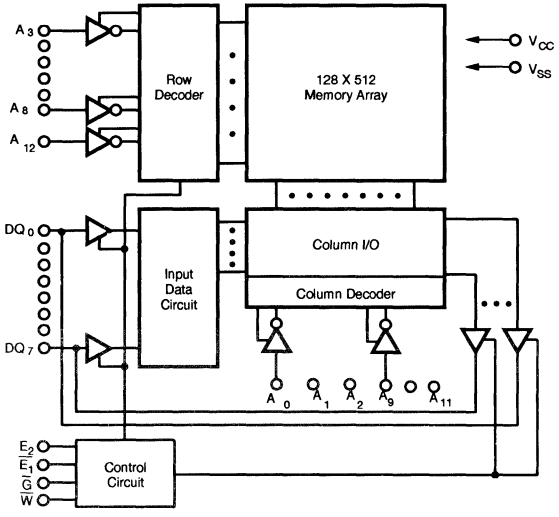
The MS6264A is a 65,536-bit static random access memory organized as 8,192 words by 8 bits and operates from a single 5 volt supply. All inputs and three-state outputs are TTL compatible and allow for direct interfacing with common I/O bus system. The MS6264A is available in the following standard 28-pin packages:

300 MIL Plastic DIP
300 MIL Small Outline J-Bend (SOJ)

Pin Configurations



Functional Block Diagram



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Pin Descriptions

A_0–A_{12} Address Inputs
These 13 address inputs select one of the 8192 x 8-bit words in the RAM.

$\overline{E1}$ Chip Enable 1 Input
E2 Chip Enable 2 Input
$\overline{E1}$ is active LOW and E2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0–DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

V_{SS} Ground

Truth Table

MODE	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

Absolute Maximum Ratings[1]

Symbol	Parameter		Rating	Unit
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-40 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability, and degrade performance characteristics.

Operating Range

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Capacitance[1]

(T_A = 25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

NOTE:
1. This parameter is guaranteed and not tested.

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS6264A Min.	Typ.(1)	Max.	Unit
V_{IL}	Guaranteed Input Low Voltage(2)		-0.3	—	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	—	6.0	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0V to V_{CC}	-2	—	2	µA
I_{OL}	Output Leakage Current	V_{CC}= Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V t o V_{CC}	-2	—	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	—	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -4mA	2.4	—	—	V
I_{CC}	Operating Power Supply Current	V_{CC}= Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, $F = F_{max}$(3)	—	—	150	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	—	—	20	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 \geq V_{CC}$ – 0.2V, $E_2 \leq$ 0.2V L(4)	—	—	100	µA
		$V_{IN} \geq$ VCC —0.2V OR $V_{IN} \leq$ 0.2V STD	—	—	3	mA

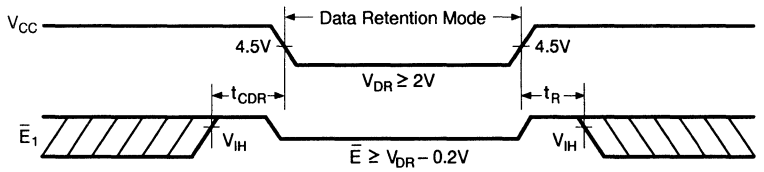
NOTES:
1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.
4. Low power version only.

Data Retention Characteristics (over the commercial operating range)

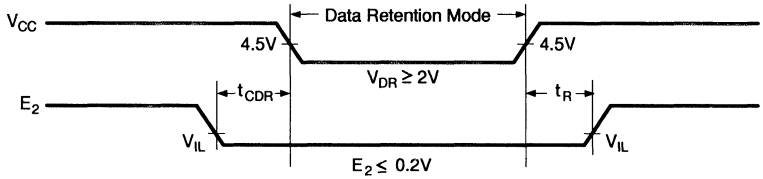
Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{E}_1 \geq V_{CC}$ – 0.2V, or $E_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V	2.0(3)	—	—	V
I_{CCDR}	Data Retention Current	$\overline{E}_1 \geq V_{CC}$ – 0.2V, or $E_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V	—	2	50(3)	µA
I_{IL}	Input Leakage Current		—	—	2	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	—	—	ns
t_R	Operation Recovery Time		t_{RC}(2)	—	—	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time
3. For low power version only

Low V_{CC} Data Retention Waveform ($\overline{E}$1 Controlled)



Low V_{CC} Data Retention Waveform (E2 Controlled)



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

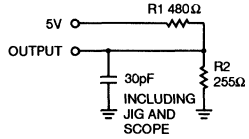


Figure 1.

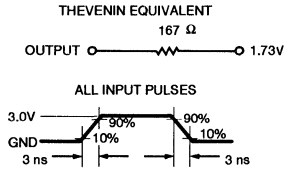


Figure 2.

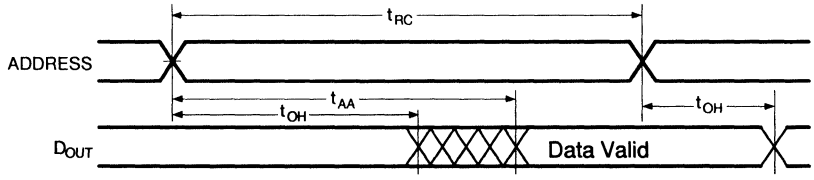
AC Electrical Characteristics (over the commercial operating range)

Read Cycle

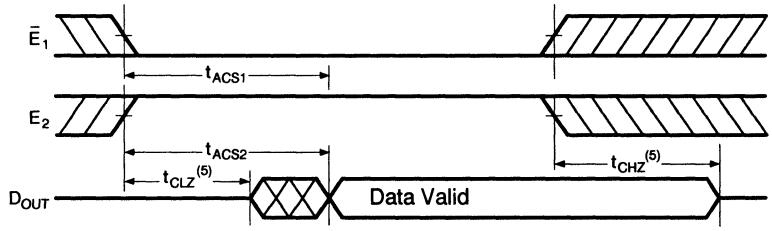
JEDEC Parameter Name	Parameter Name	Parameter	MS6264A-15		MS6264A-20		MS6264A-25		MS6264A-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	t_{RC}	Read Cycle Time	15	—	20	—	25	—	35	—	ns
t_{AVQV}	t_{AA}	Address Access Time	—	15	—	20	—	25	—	35	ns
t_{ELQV}	t_{ACS1}	Chip Enable Access Time	—	15	—	20	—	25	—	35	ns
t_{ELQV}	t_{ACS2}	Chip Enable Access Time	—	15	—	20	—	25	—	35	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	—	10	—	10	—	10	—	15	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	5	—	5	—	5	—	5	—	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	0	—	0	—	0	—	0	—	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	—	10	—	10	—	15	—	15	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	—	10	—	10	—	15	—	15	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns

Switching Waveforms (Read Cycle)

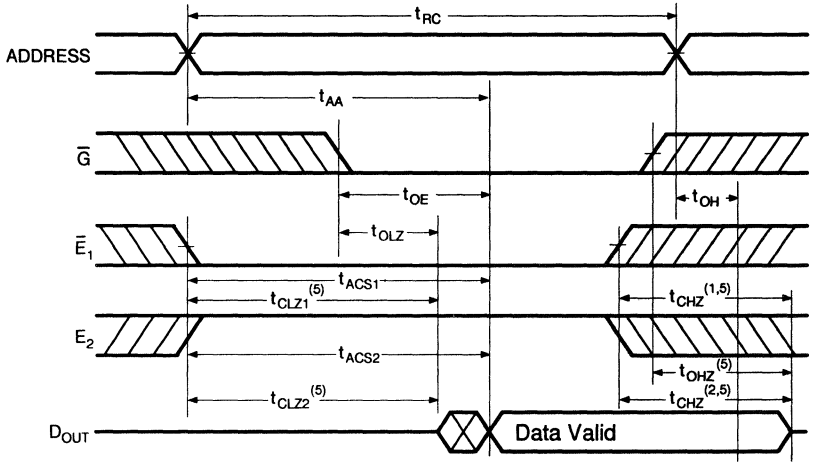
READ CYCLE 1[1, 2, 4]



READ CYCLE 2[1, 3, 4]



READ CYCLE 3[1]



NOTES:
1. $\overline{W}$ is high during all read cycles.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and /or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured +500mV from steady state with C_L = 5pF. This parameter is guaranteed and not 100% tested.

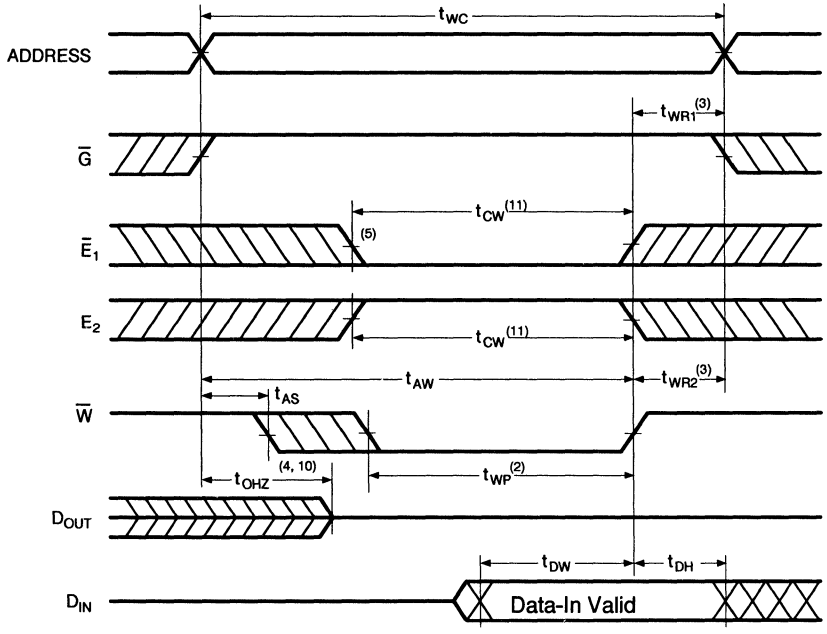
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

JEDEC Parameter Name	Parameter Name	Parameter	MS6264A-15		MS6264A-20		MS6264A-25		MS6264A-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	t_{WC}	Write Cycle Time	15	—	20	—	25	—	35	—	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	10	—	15	—	20	—	25	—	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	—	0	—	0	—	0	—	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	10	—	15	—	20	—	25	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width	10	—	15	—	20	—	20	—	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	15	0	15	0	20	0	20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	5	—	15	—	20	—	20	—	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	10	0	10	0	15	0	15	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	5	—	5	—	5	—	5	—	ns

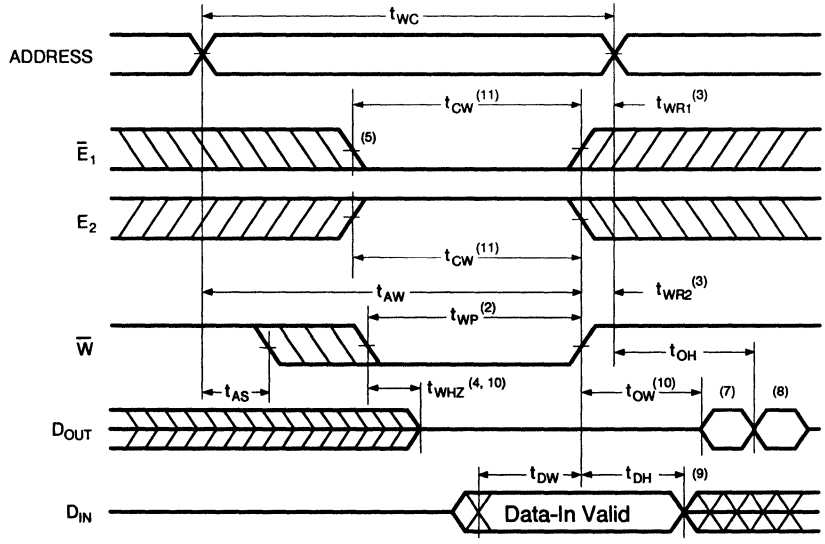
Switching Waveforms (Write Cycle)

WRITE CYCLE 1(1)



Switching Waveforms (Write Cycle)

WRITE CYCLE 2[1,6]



NOTES:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. t_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with CL = 5pF. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.
12. If $\overline{G}$ is LOW during a $\overline{W}$ controlled write cycle, the write pulse width must be the larger of twp or ($t_{WHZ} + t_{DW}$) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{G}$ is HIGH during a $\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

5

Ordering Information

Speed (ns)	Ordering Part Number	Package Reference No.	Temperature Range
15	MS6264A-15NC	28 Pin 300 mil Plastic DIP	0°C to +70°C
15	MS6264A-15RC	28 Pin 300 mil SOJ	0°C to +70°C
20	MS6264A-20NC	28 Pin 300 mil Plastic DIP	0°C to +70°C
20	MS6264A-20RC	28 Pin 300 mil SOJ	0°C to +70°C
25	MS6264A-25NC	28 Pin 300 mil Plastic DIP	0°C to +70°C
25	MS6264A-25RC	28 Pin 300 mil SOJ	0°C to +70°C
35	MS6264A-35NC	28 Pin 300 mil Plastic DIP	0°C to +70°C
35	MS6264A-35RC	28 Pin 300 mil SOJ	0°C to +70°C

MS62256A
32K x 8 HIGH SPEED CMOS STATIC RAM

Features

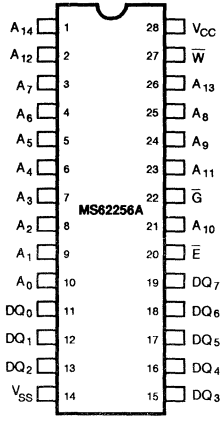
- High-speed – 20/25/35 ns
- Low Power dissipation:
  MS62256A
  900mW (Typ.) Operating
  50mW (Typ.) Standby
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V

Description

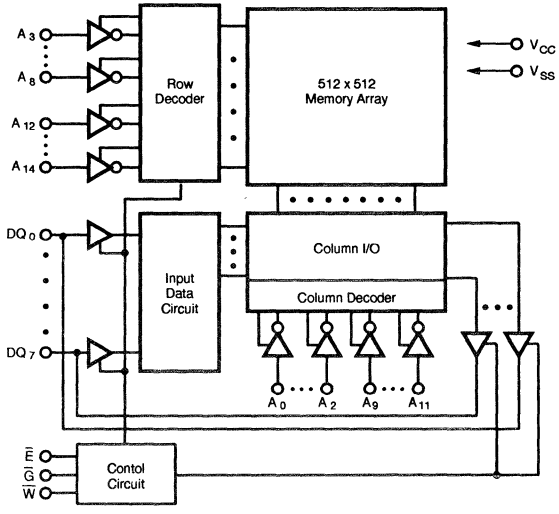
The MS62256A is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL-VITELIC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS62256A is available in the following standard 28-pin packages:

300 MIL Plastic DIP
300 MIL Small Outline J-Bend (SOJ)

Pin Configurations



Functional Block Diagram



5

Pin Descriptions

A_0 - A_{14} Address Inputs
These 15 address inputs select one of the 32768 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input
$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

VSS Ground

Truth Table

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Output Disabled	L	H	H	High Z
Write	L	X	L	D_{IN}

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Absolute Maximum Ratings (1)

Symbol	Parameter		Rating	Units
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-40 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability and degrade performance characteristics.

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS62256A Min.	Typ.(1)	Max.	Units
V_{IL}	Guaranteed Input Low Voltage(2,3)		–0.3	-	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0V to V_{CC}	–2	-	2	µA
I_{OL}	Output Leakage Current	V_{CC}= Max, $\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{IN} = 0V t o V_{CC}	–2	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -4mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC}= Max, $\overline{E}$ = V_{IL}, I_{DQ} = 0mA, F = F_{max}(4)	-	-	180	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, I_{DQ} = 0mA	-	-	35	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}$ ≥ V_{CC} – 0.2V V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	-	-	10	mA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (Min.) = –3.0V for pulse width ≤ 20ns
4. F_{MAX} = $1/t_{RC}$.

Capacitance(1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

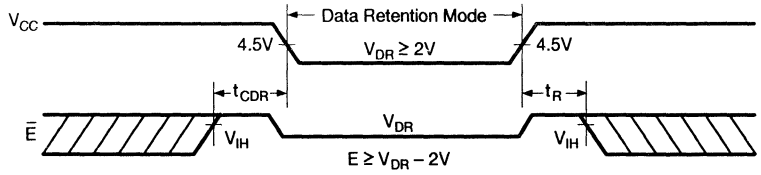
1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max(2)	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E}$ ≥ V_{CC}– 0.2V, V_{IN} ≥ V_{CC}– 0.2V or V_{IN} ≤ 0.2V	2.0(4)	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E}$ ≥ V_{CC}– 0.2V, V_{IN} ≥ V_{CC}– 0.2V or V_{IN} ≤ 0.2V	-	2	50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(3)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. V_{CC} = 3V
3. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

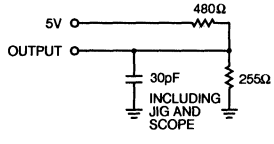


Figure 1a

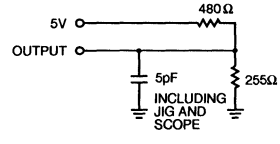


Figure 1b

Equivalent to:

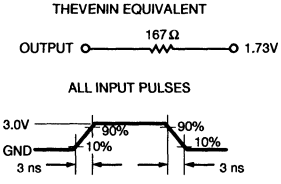


Figure 2

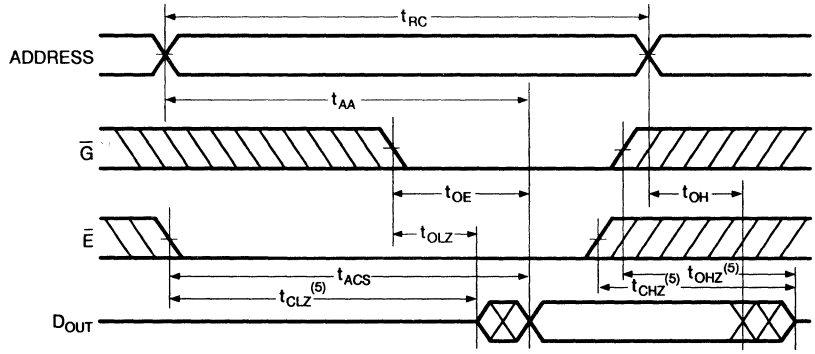
AC Electrical Characteristics (over the commercial operating range)

Read Cycle

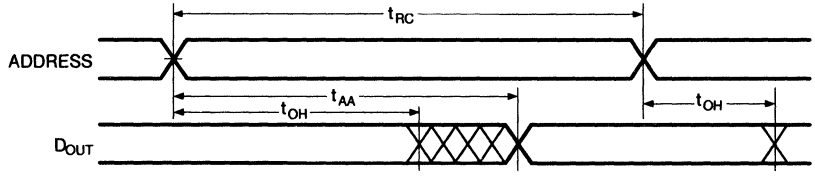
Jedec Parameter Name	Parameter Name	Parameter	MS62256A-20 Min.	MS62256A-20 Max.	MS62256A-25 Min.	MS62256A-25 Max.	MS62256A-35 Min.	MS62256A-35 Max.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time	20	-	25	-	35	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	20	-	25	-	35	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-	20	-	25	-	35	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-	8	-	12	-	15	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	3	-	5	-	5	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	0	-	0	-	0	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	-	8	-	10	-	15	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	7	-	10	-	15	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	3	-	5	-	5	-	ns

Switching Waveforms (Read Cycle)

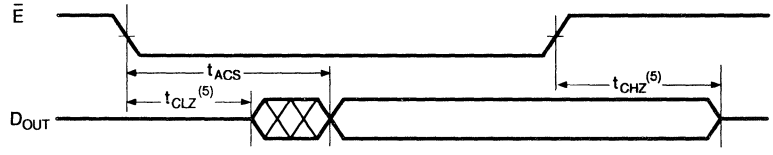
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]



READ CYCLE 3[1, 3, 4]



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

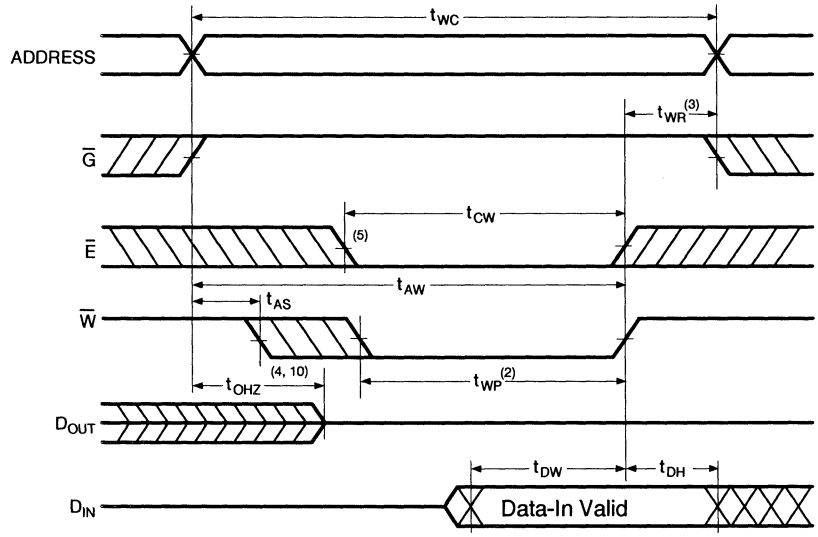
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

Jedec Parameter Name	Parameter Name	Parameter	MS62256A-20		MS62256A-25		MS62256A-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	t_{WC}	Write Cycle Time	20	-	25	-	35	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	15	-	20	-	25	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	0	-	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	15	-	20	-	25	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	15	-	15	-	20	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	0	-	0	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	8	0	13	0	15	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	10	-	13	-	15	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	ns

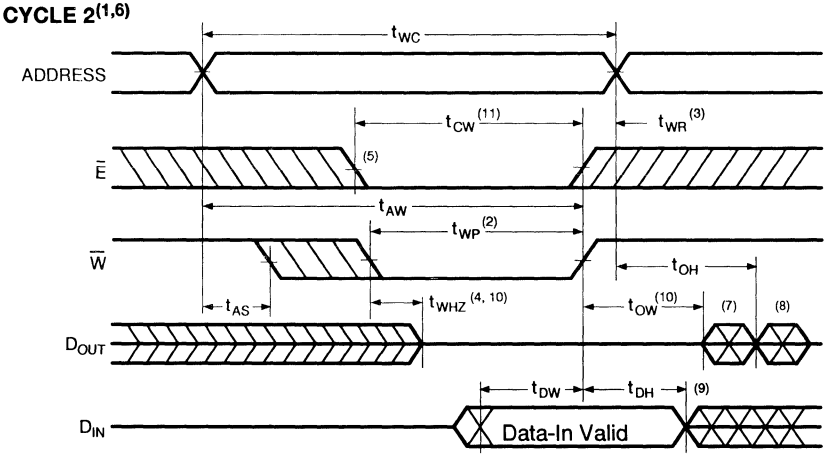
Switching Waveforms (Write Cycle)

WRITE CYCLE 1[1]



Switching Waveforms (Write Cycle)

WRITE CYCLE 2[1,6]



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the E low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

Ordering Information

Speeds	Ordering Part Number	Package	Temperature Range
20	MS62256A-20NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
20	MS62256A-20RC	28 Pin Small Outline J Bend	0°C to +70°C
25	MS62256A-25NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
25	MS62256A-25RC	28 Pin Small Outline J Bend	0°C to +70°C
35	MS62256A-35NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
35	MS62256A-35RC	28 Pin Small Outline J Bend	0°C to +70°C

MS62256H
32K x 8 HIGH SPEED CMOS STATIC RAM

ADVANCED INFORMATION

Features

- High-speed – 15/20/25/35 ns
- Low Power dissipation:
  MS62256HL
  1.1W (Max.) Operating
  1mW (Max.) Power down
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V

Description

The MS62256H is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL-VITELIC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS62256H is available in the following standard 28-pin packages:

600 MIL Plastic DIP
300 MIL Plastic DIP
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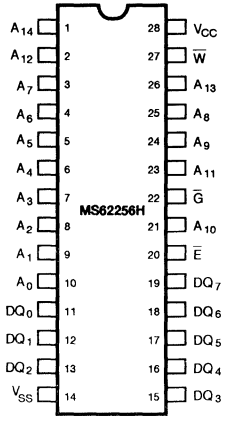
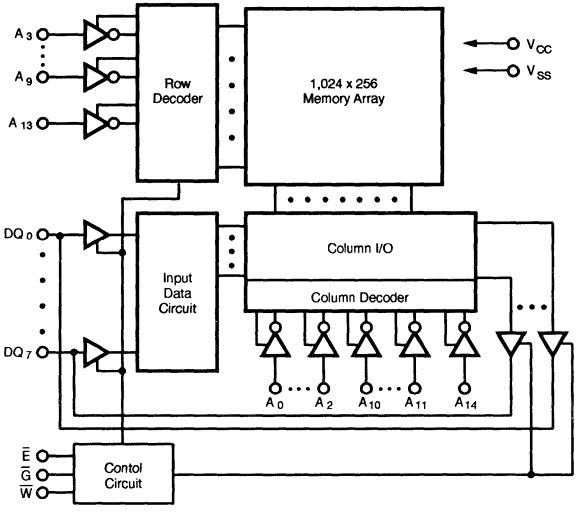
Pin Configurations



Functional Block Diagram



5

Pin Descriptions

A_0 - A_{14} Address Inputs
These 15 address inputs select one of the 32768 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input
$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

V_{SS} Ground

Truth Table

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Output Disabled	L	H	H	High Z
Write	L	X	L	D_{IN}

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Absolute Maximum Ratings (1)

Symbol	Parameter		Rating	Units
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-40 to +150	°C
P_D	Power Dissipation		1.2	W
I_{OUT}	DC Output Current		50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability and degrade performance characteristics.

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS62256H Min.	Typ.(1)	Max.	Units
V_{IL}	Guaranteed Input Low Voltage(2,3)		–0.3	-	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0V to V_{CC}	–2	-	2	µA
I_{OL}	Output Leakage Current	V_{CC}= Max, $\overline{E}$ = V_{IH} or $\overline{G}$ = V_{IH}, V_{IN} = 0V t o V_{CC}	–2	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -4.0mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC}= Max, $\overline{E}$ = V_{IL}, I_{DQ} = 0mA, F = F_{max}(4)	-	-	200	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, I_{DQ} = 0mA	-	-	40	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}$ ≥ V_{CC} – 0.2V	-	-	2	mA
		V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	-	-	130(5)	µA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (Min.) = –3.0V for pulse width ≤ 20ns
4. F_{MAX} = $1/t_{RC}$.
5. L version only.

Capacitance(1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

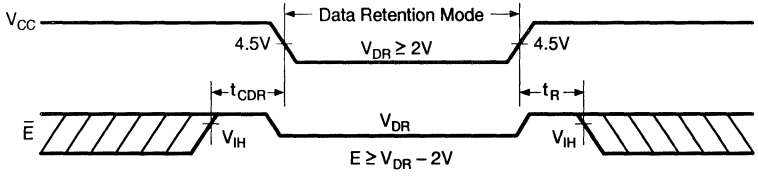
1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max(2)	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E}$ ≥ V_{CC}– 0.2V, V_{IN} ≥ V_{CC}– 0.2V or V_{IN} ≤ 0.2V	2.0(	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E}$ ≥ V_{CC}– 0.2V, V_{IN} ≥ V_{CC}– 0.2V or V_{IN} ≤ 0.2V	-	2	50(4)	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(3)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. V_{CC} = 3V
3. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

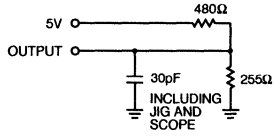


Figure 1a

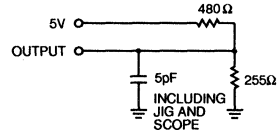


Figure 1b

Equivalent to:

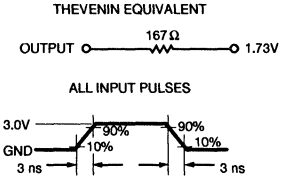


Figure 2

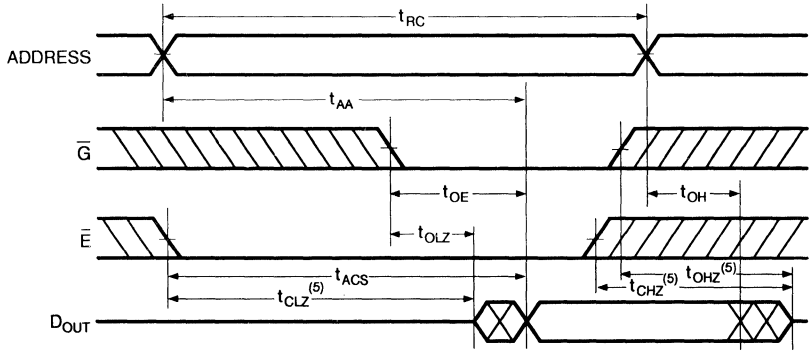
AC Electrical Characteristics (over the commercial operating range)

Read Cycle

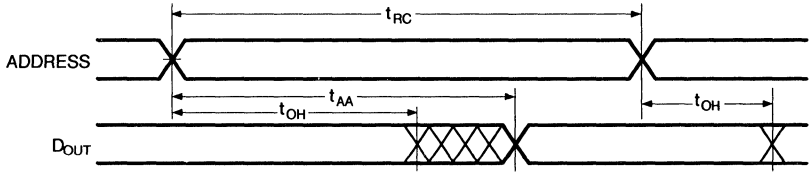
Jedec Parameter Name	Parameter Name	Parameter	MS62256H-15		MS62256H-20		MS62256H-25		MS62256H-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	t_{RC}	Read Cycle Time	15	-	20	-	25	-	35	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	15	-	20	-	25	-	35	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-	15	-	20	-	25	-	35	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-	8	-	10	-	12	-	15	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	5	-	5	-	5	-	5	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	0	-	0	-	0	-	0	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	-	8	-	8	-	10	-	15	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	8	-	8	-	10	-	15	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	3	-	5	-	5	-	5	-	ns

Switching Waveforms (Read Cycle)

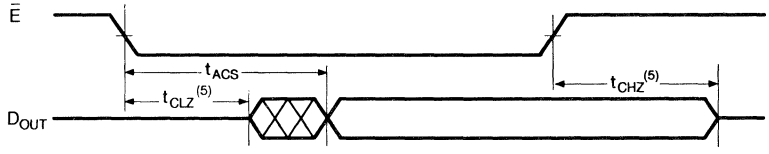
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]



READ CYCLE 3[1, 3, 4]



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

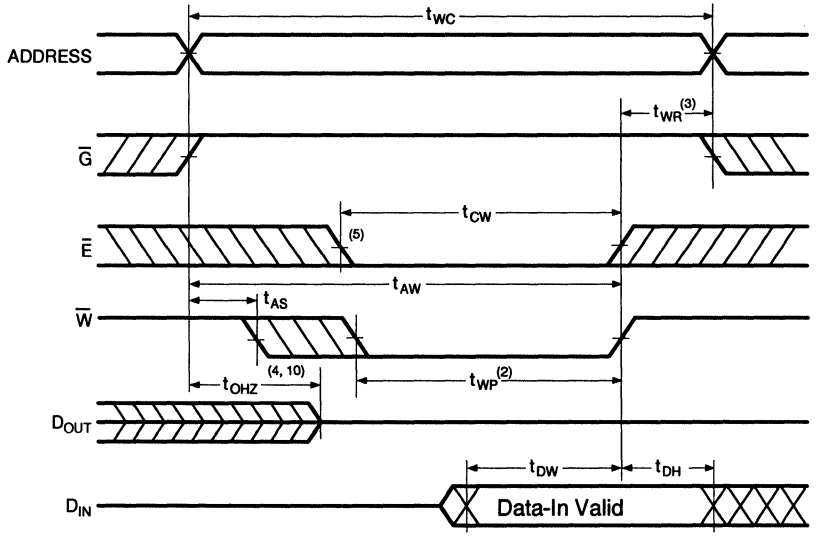
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

Jedec Parameter Name	Parameter Name	Parameter	MS62256H-15		MS62256H-20		MS62256H-25		MS62256H-35		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	t_{WC}	Write Cycle Time	15	-	20	-	25	-	35	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	10	-	15	-	20	-	25	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	0	-	0	-	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	10	-	15	-	20	-	25	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	12	-	12	-	15	-	20	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	0	-	0	-	0	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	10	0	10	0	13	0	15	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	8	-	10	-	13	-	15	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	0	-	0	-	0	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	8	0	8	0	10	0	-	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	3	-	3	-	3	-	0	-	ns

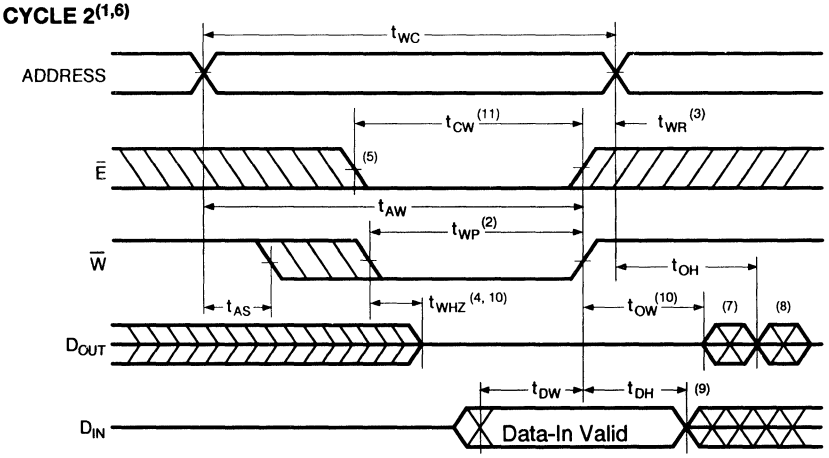
Switching Waveforms (Write Cycle)

WRITE CYCLE 1[1]



Switching Waveforms (Write Cycle)

WRITE CYCLE 2[1,6]



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the E low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b on page 4. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

5

Ordering Information

Speeds	Ordering Part Number	Package	Temperature Range
15	MS62256H-15NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
15	MS62256H-15RC	28 Pin Small Outline J Bend	0°C to +70°C
20	MS62256H-20NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
20	MS62256H-20RC	28 Pin Small Outline J Bend	0°C to +70°C
25	MS62256H-25NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
25	MS62256H-25RC	28 Pin Small Outline J Bend	0°C to +70°C
35	MS62256H-35NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
35	MS62256H-35RC	28 Pin Small Outline J Bend	0°C to +70°C

MS621002
256K x 4 CMOS STATIC RAM

Features

- Fast Access Times: 20/25/35 ns
- High Density 400-Mil SOJ
- Low Standby Power
- TTL Compatible I/O
- 5V ± 10% Supply
- Fully Static Operation
- Three State Output
- JEDEC Standard Pinout

Description

The MS621002 is a high speed 1M-bit static RAM organized as 256K x 4. Fully static in operation, the Chip Enable ($\overline{E}$) reduces power to the chip when HIGH. Standby power drops to its lowest level (I_{SB1}) when $\overline{E}$ is raised to within 0.2V of V_{CC}.

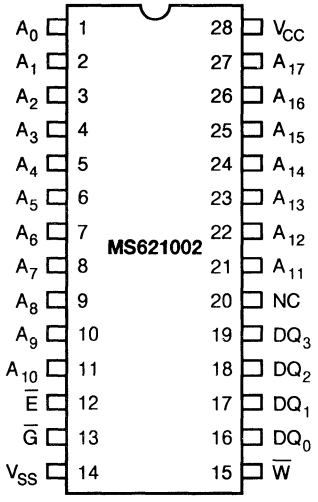
Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH.

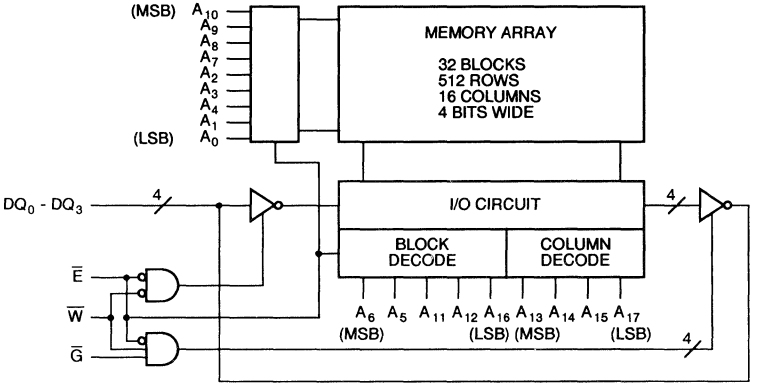
High frequency design techniques should be employed to obtain optimum performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

5

Pin Configuration



Functional Block Diagram



Pin Descriptions

A_0 - A_{17} Address Inputs
These 18 address inputs select one of the 256K x 4 bit segments in the RAM.

$\overline{E}$ Chip Enable Input
$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory locations.

DQ_0 - DQ_3 Data Input and Data Output Ports
These 4 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply
V_{SS} Ground

Truth Table

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Absolute Maximum Ratings (1)

Parameter Name	Parameter		Rating	Units
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	V
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	V
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-65 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	D C Output Current		±40(2)	mA

See Notes following "SWITCHING CHARACTERISTICS".

DC Electrical Characteristics (0°C to +70°C)

Parameter Name	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.5		5.5	V
V_{SS}	Supply Voltage		0		0	V
V_{IL}	Guaranteed Input LOW Voltage (3)		-0.5		0.8	V
V_{IH}	Guaranteed Input HIGH Voltage		2.2		V_{CC} + 0.5	V
I_{CC1}	Operating Current (4)	Output open, t_{CYCLE} = 20ns			130	mA
I_{CC1}	Operating Current (4)	Output open, t_{CYCLE} = 25ns			120	mA
I_{CC1}	Operating Current (4)	Output open, t_{CYCLE} = 35ns			100	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC}$-0.2V		0.1	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			5	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5V, V_{in} = 0V to V_{CC}	-2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5V, V_{in} = 0V to V_{CC}	-10		10	µA
V_{OH}	Output High Voltage	I_{OH} = -4.0mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA			0.4	V

See Notes following "SWITCHING CHARACTERISTICS".

Capacitance(1) T_A = 25°C, f = 1.0MHz

Parameter Name	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	I/O Capacitance	V_{DQ} = 0V	8	pF

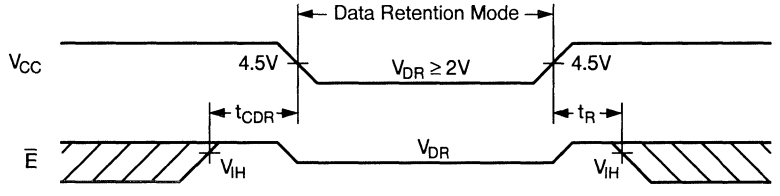
1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{E} \geq V_{CC}$-0.2V, $\overline{G} \geq V_{CC}$-0.2V, $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq$0.2V	2.0	-	5.5	V
I_{CCDR}	Data Retention Current	$\overline{E} \geq V_{CC}$-0.2V, $\overline{G} \geq V_{CC}$-0.2V, $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq$0.2V	-	-	500(2)	µA
t_{CDR}	Chip Deselected to Data		0	-	-	ns
	Retention Time	See Retention Waveform				
t_R	Operation Recovery Time		t_{RC}(3)	-	-	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. V_{CC} = 3V
3. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



5

AC Electrical Characteristics (over the commercial operating range) (6)

Parameter Name	Parameter	-20 Min.	-20 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Units
Read Cycle								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active (7), (8)	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z (7), (8)		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active (7), (8)	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z (7), (8)		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time (8)	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time (8)		20		25		35	ns
Write Cycle								
t_{WC}	Write Cycle Timing	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	12		15		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z (7), (8)		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active (7), (8)	3		3		3		ns

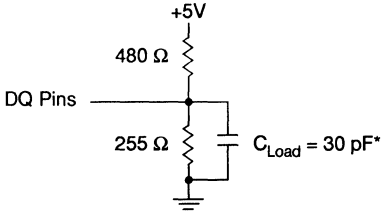
NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability, and degrade performance characteristics.
2. Output should not be shorted for more than 30 seconds.
3. Negative undershoot of up to 3.0V is permitted once per cycle.
4. I_{CC} is dependent upon output loading and cycle rates. Specified values are with output open, operating at specified cycle times.
5. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias}=0V and V_{CC}=5.0V.
6. Switching Characteristics measurements specified at "AC Test Conditions" levels.
7. Active output to High-Z and High-Z to active output tests specified for a ±200mV transition from steady levels into the test load.
8. Sample tested only.

AC Test Conditions

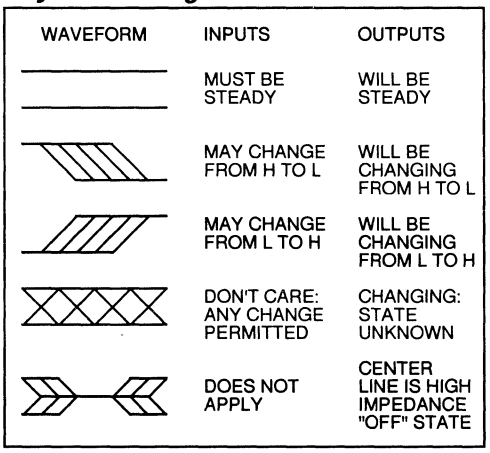
Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load, Timing Tests	See Figure Below

AC Test Load



* Includes scope and jig capacitance

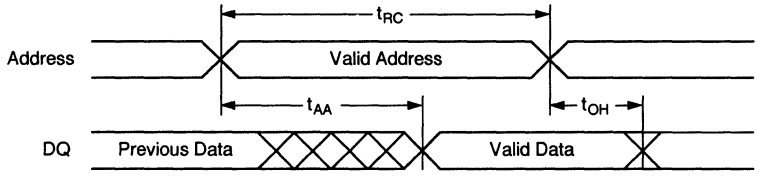
Key to Switching Waveforms



Switching Waveforms- Read Cycle

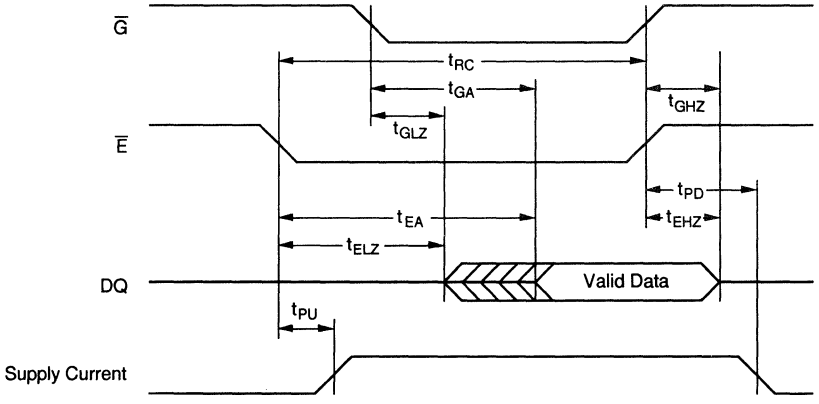
Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in Low-Z state and the data may not be valid.



Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data-out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Outputs will transition from High-Z to Valid Data-out. Data-out is valid after both t_{EA} and t_{GA} are met.

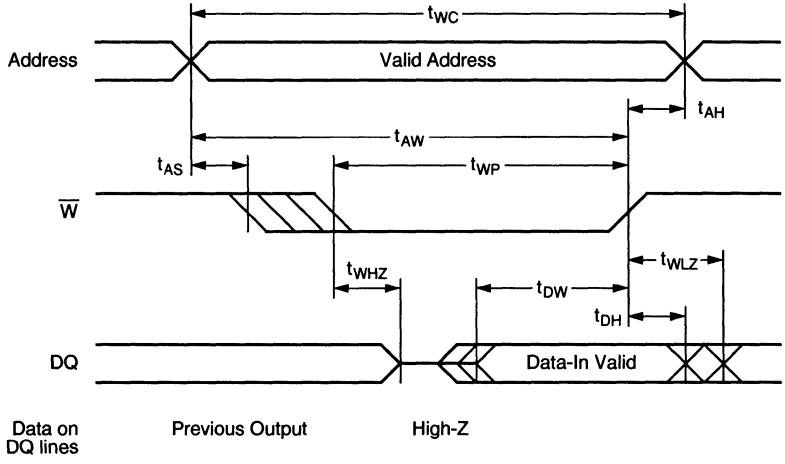


Switching Waveform - Write Cycle

Addresses must be stable during Write Cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

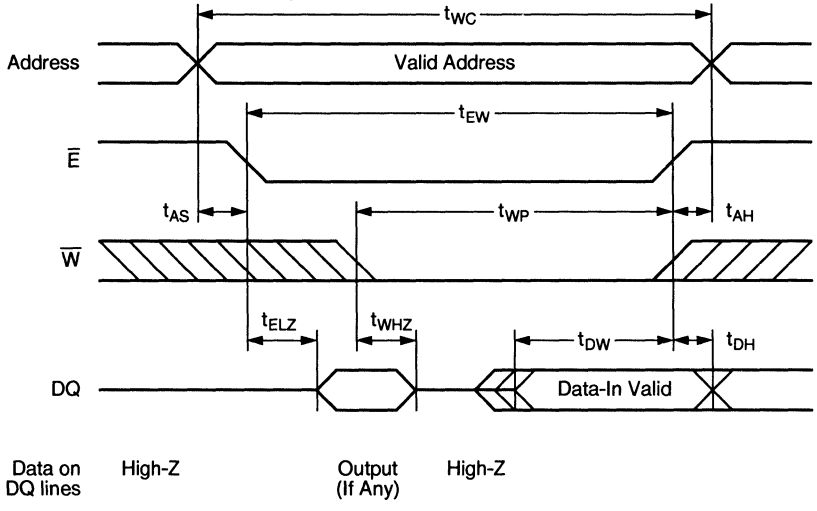
Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.



Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.



Ordering Information

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
20	MS621002-20KC	28 Pin 400 mil SOJ	0°C to +70°C
25	MS621002-25KC	28 Pin 400 mil SOJ	0°C to +70°C
35	MS621002-35KC	28 Pin 400 mil SOJ	0°C to +70°C

MOSEL-VITELIC **MS621008**

128K x 8 CMOS STATIC RAM

Features

- Fast Access Times: 20/25/35 ns
- High Density 400-Mil SOJ Package
- Low Standby Power
- TTL Compatible I/O
- 5V ± 10% Supply
- Fully Static Operation
- Three State Output
- JEDEC Standard Pinout

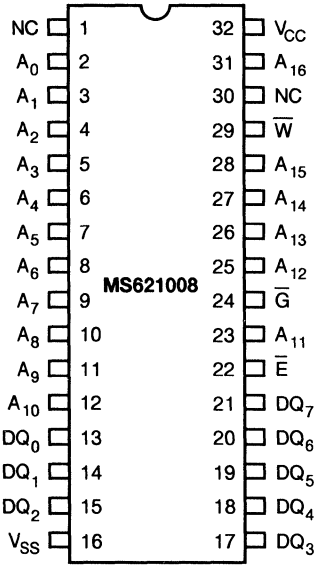
Description

The MS621008 is a high speed 1M-bit static RAM organized as 128K x 8. Fully static in operation, the Chip Enable ($\overline{E}$) control places the RAM in a low-power standby mode when inactive (HIGH). Standby power drops to its lowest level (I_{SB1}) when $\overline{E}$ is raised to within 0.2V of V_{CC}.

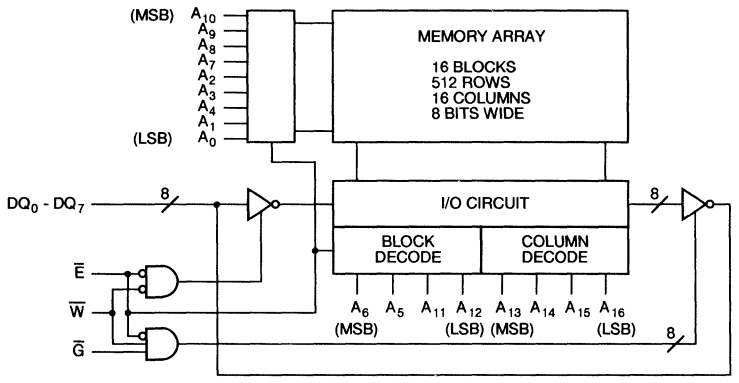
Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the address lines. The Output Enable Control ($\overline{G}$) can prevent bus contention.

High frequency design techniques should be employed to obtain optimum performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

Pin Configuration



Functional Block Diagram



Pin Descriptions

A_0 - A_{16} Address Inputs
These 17 address inputs select one of the 128K x 8 bit segments in the RAM.

$\overline{E}$ Chip Enable Input
$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory locations.

DQ_0 - DQ_7 Data Input and Data Output Ports
These 8 bidirectional ports are used to read data from and write data into the RAM.

V_{CC} Power Supply

V_{SS} Ground

Truth Table

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

Operation Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Absolute Maximum Ratings (1)

Parameter Name	Parameter		Rating	Units
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	V
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	V
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-65 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	D C Output Current		±40(2)	mA

See Notes following "SWITCHING CHARACTERISTICS".

DC Electrical Characteristics (0°C to +70°C)

Parameter Name	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage		4.5	5.0	5.5	V
V_{SS}	Supply Voltage		0	0	0	V
V_{IL}	Guaranteed Input LOW Voltage (3)		-0.5		0.8	V
V_{IH}	Guaranteed Input HIGH Voltage		2.2		V_{CC} + 0.5	V
I_{CC1}	Operating Current (4)	Output open, t_{CYCLE} = 20ns			150	mA
I_{CC1}	Operating Current (4)	Output open, t_{CYCLE} = 25ns			140	mA
I_{CC1}	Operating Current (4)	Output open, t_{CYCLE} = 35ns			120	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC}$-0.2V		0.1	2	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			10	mA
I_{LI}	Input Leakage Current	V_{in} = 0V to V_{CC}	-2		2	µA
I_{LO}	I/O Leakage Current	V_{in} = 0V to V_{CC}	-10		10	µA
V_{OH}	Output High Voltage	I_{OH} = -4.0mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0mA			0.4	V

See Notes following "SWITCHING CHARACTERISTICS".

Capacitance(1) T_A = 25°C, f = 1.0MHz

Parameter Name	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	I/O Capacitance	V_{DQ} = 0V	8	pF

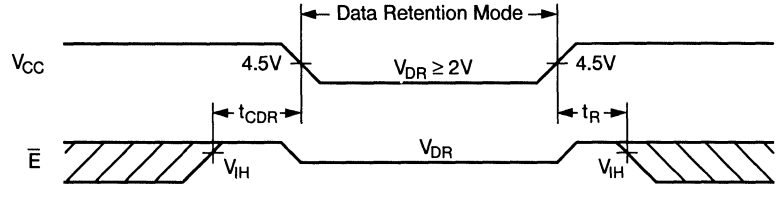
1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
V_{DR}	V_{CC} for Data Retention	$\overline{E} \geq V_{CC}$-0.2V, $\overline{G} \geq V_{CC}$-0.2V, $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E} \geq V_{CC}$-0.2V, $\overline{G} \geq V_{CC}$-0.2V, $V_{IN} \geq V_{CC}$-0.2V or $V_{IN} \leq 0.2V$	-	-	500(2)	µA
t_{CDR}	Chip Deselected to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(3)	-	-	ns

NOTES:
1. V_{CC} = 2V, T_A = +25°C
2. V_{CC} = 3V
3. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



AC Electrical Characteristics (over the commercial operating range) [6]

Parameter Name	Parameter	-20 Min.	-20 Max.	-25 Min.	-25 Max.	-35 Min.	-35 Max.	Units
Read Cycle								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [7], [8]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [7], [8]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [7], [8]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [7], [8]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [8]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [8]		20		25		35	ns
Write Cycle								
t_{WC}	Write Cycle Timing	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	12		15		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [7], [8]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [7], [8]	3		3		3		ns

NOTES:

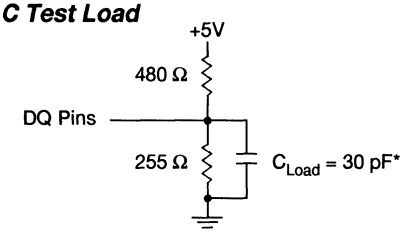
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability, and degrade performance characteristics.
2. Output should not be shorted for more than 30 seconds.
3. Negative undershoot of up to 3.0V is permitted once per cycle.
4. I_{CC} is dependent upon output loading and cycle rates. Specified values are with output open, operating at specified cycle times.
5. Capacitances are maximum values at 25°C measured at 1.0 MHz with V_{Bias}=0V and V_{CC}=5.0V.
6. Switching Characteristics measurements specified at "AC Test Conditions" levels.
7. Active output to High-Z and High-Z to active output tests specified for a ±200mV transition from steady levels into the test load.
8. Sample tested only.

5

AC Test Conditions

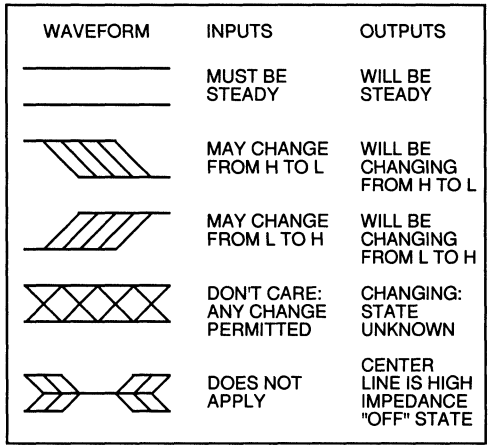
Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load, Timing Tests	See Figure Below

AC Test Load



* Includes scope and jig capacitance

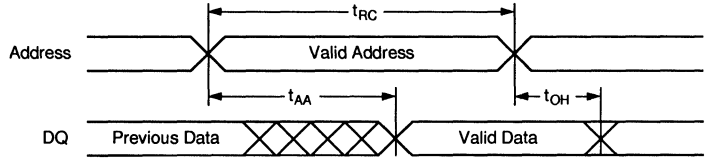
Key to Switching Waveforms



Switching Waveforms - Read Cycle

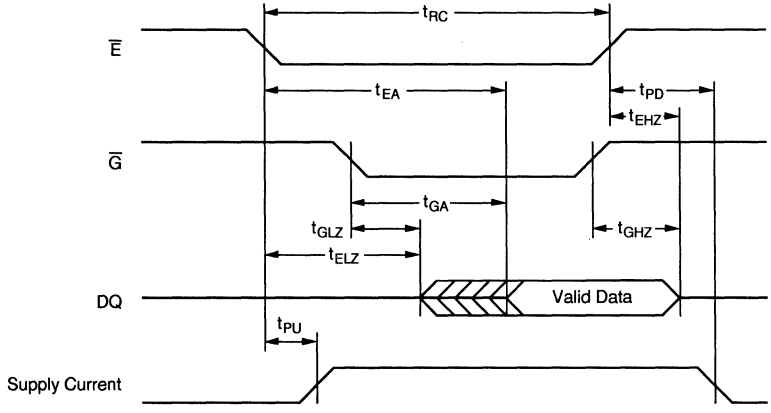
Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data-out implies that data lines are in Low-Z state but the data is not guaranteed to be valid until t_{AA}.



Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data-out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data-out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

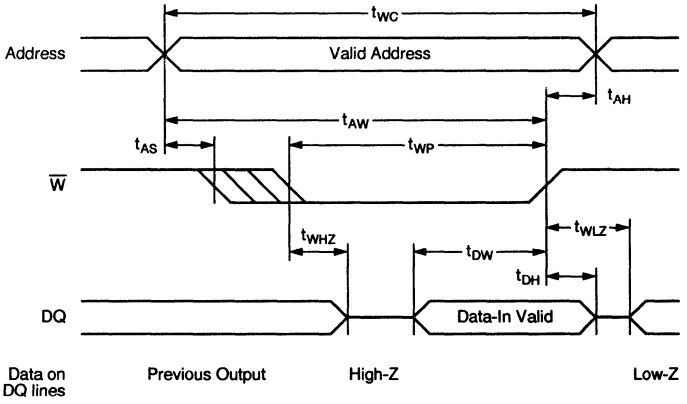


Switching Waveforms - Write Cycle

Addresses must be stable during Write Cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, The outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Writes cycles. This will prevent the MS62008's outputs from becoming active, preventing bus contention, thereby reducing system noise.

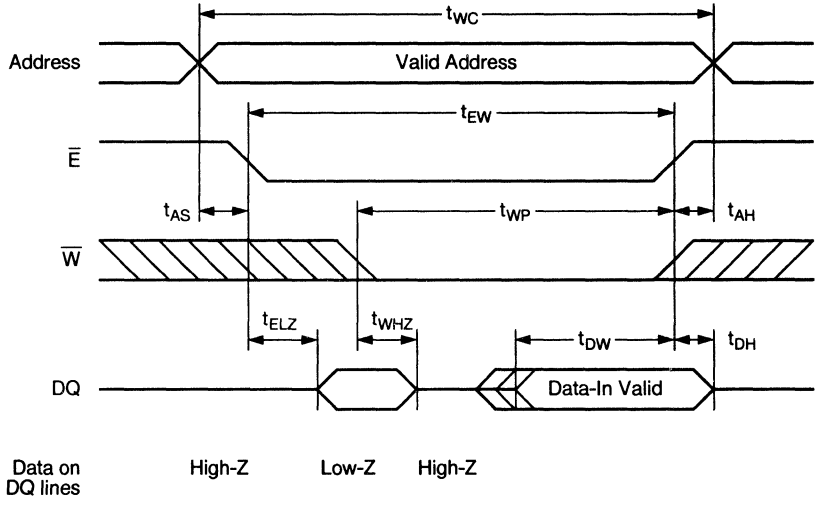
Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance, since both t_{WHZ} and t_{DW} timing specifications must be met.



Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.



Ordering Information

Speed (ns)	Ordering Part Number	Package Reference No.	Temperature Range
20	MS621008-20EC	32 pin 400 mil Plastic DIP	0°C to +70°C
25	MS621008-25EC	32 pin 400 mil Plastic DIP	0°C to +70°C
35	MS621008-35EC	32 pin 400 mil Plastic DIP	0°C to +70°C
20	MS621008-20KC	32 Pin 400 mil SOJ	0°C to +70°C
25	MS621008-25KC	32 Pin 400 mil SOJ	0°C to +70°C
35	MS621008-35KC	32 Pin 400 mil SOJ	0°C to +70°C

MS6516
2K x 8 CMOS STATIC RAM

Features

- Available in 100ns (Max.) version
- Automatic power-down when chip disabled
- Low power consumption (L-version): MS6516L
  - 385mW (Max.) Operating
  - 11mW (Max.) Standby
  - 55µW (Max.) Power-down
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Chip enable for simple memory expansion

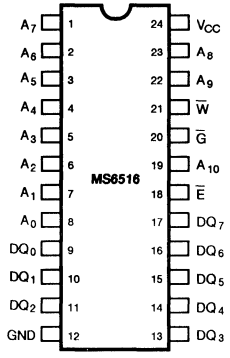
Description

The MS6516 is a high performance, low power CMOS static RAM organized as 2048 words by 8 bits. The device supports easy memory expansion with an active LOW chip enable ($\overline{E}$) as well as an active LOW output enable ($\overline{G}$) and three-state outputs. An automatic power-down feature is included which reduces the chip power by 85% in TTL standby mode, and by over 99% in full power-down mode.

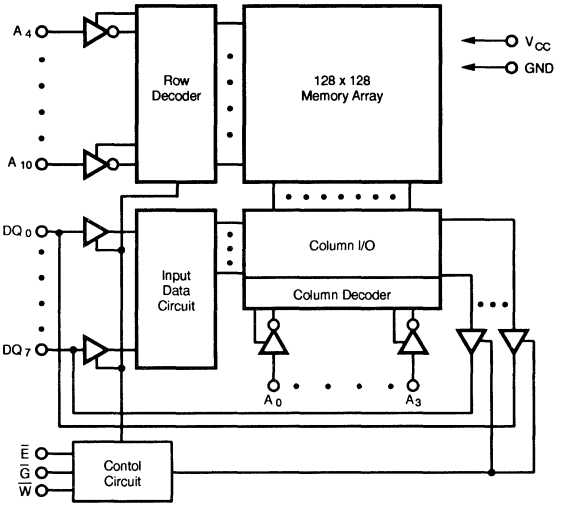
The device is manufactured in MOSEL-VITELIC's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MS6516 is available in the JEDEC standard 24 pin 600 mil wide DIP and small outline package.

Pin Configurations



Functional Block Diagram



Pin Descriptions

A_0 - A_{10} Address Inputs

These 11 address inputs select one of the 2048 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

Truth Table

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

Absolute Maximum Ratings (1)

Symbol	Parameter		Rating	Units
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	
$V_{I/O}$	Input/Output Voltage Applied		-0.3 to V_{CC} + 0.3	
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +85	°C
T_{STG}	Storage Temperature	Plastic	-40 to +125	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS6516L Min.	Typ.(1)	Max.	Units
V_{IL}	Guaranteed Input Low Voltage(2)		-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	-	V_{CC}+ 0.3	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0V to V_{CC}	-	-	10	µA
I_{OL}	Output Leakage Current	V_{CC}= Max, $\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH} ,V_{IN} = 0V t o V_{CC}	-	-	10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	-	0.21	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1.0mA	2.4	3.5	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, E = V_{IL}, $I_{I/O}$ = 0mA, F_{max}(3)	-	40	70	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, $I_{I/O}$ = 0mA	-	0.5	2	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}$ ≥ V_{CC} - 0.2V, $\overline{G}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	-	1	10	µA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. F_{MAX} = $1/t_{RC}$.

Capacitance[1] (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

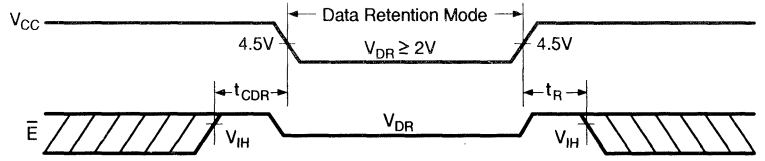
1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

Symbol	Parameter	Test Conditions	Min.	Typ.(2)	Max(3)	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E}$ = V_{CC}	2.0	-	-	V
I_{CCDR}	Data Retention Current	V_{IN} = 0V or V_{CC}	-	2	10	µA
t_{CDR}	Chip Deselect to Data Retention Time	V_{CC} = 2.0V, $\overline{E}$ = V_{CC}	0	-	-	ns
t_R	Operation Recovery Time	V_{IN} = 0V or V_{CC}	t_{RC}(2)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

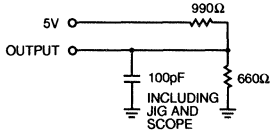


Figure 1a

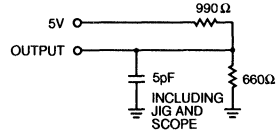
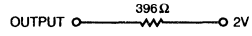


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

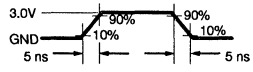


Figure 2

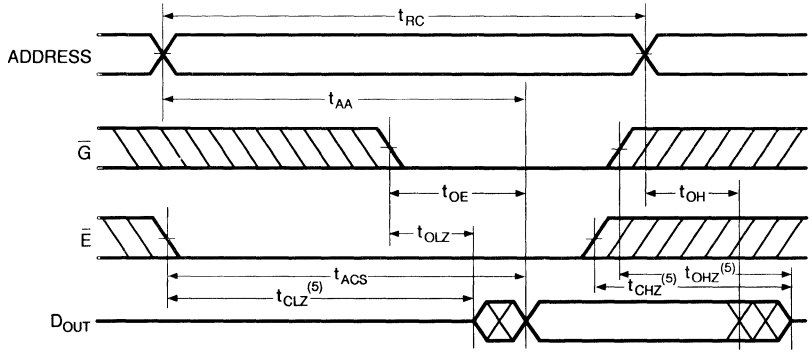
AC Electrical Characteristics (over the commercial operating range)

Read Cycle

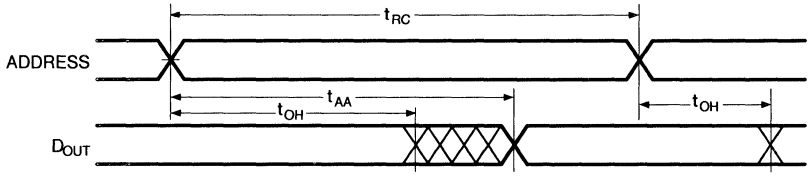
Jedec Parameter Name	Parameter Name	Parameter	-10 Min.	-10 Max.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time	100	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	100	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid	-	50	ns
t_{ELQX}	t_{CLZ}	Chip Enable to Output Low Z	5	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	0	40	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	ns

Switching Waveforms (Read Cycle)

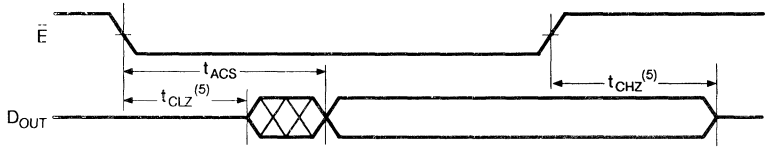
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]



READ CYCLE 3[1, 3, 4]



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

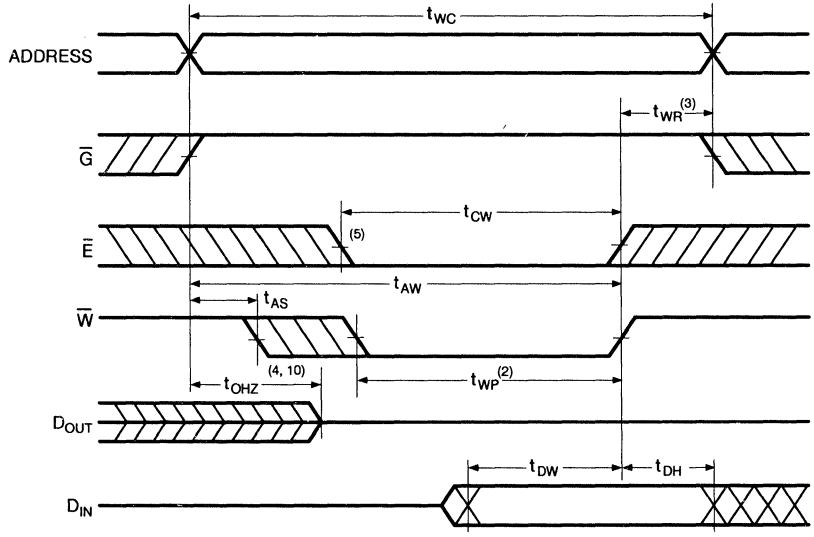
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

Jedec Parameter Name	Parameter Name	Parameter	-10 Min.	-10 Max.	Unit
t_{AVAX}	t_{WC}	Write Cycle Time	100	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	55	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	80	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	0	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	-	35	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	30	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	ns
t_{GHZQ}	t_{OHZ}	Output Disable to Output in High Z	0	35	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	0	-	ns

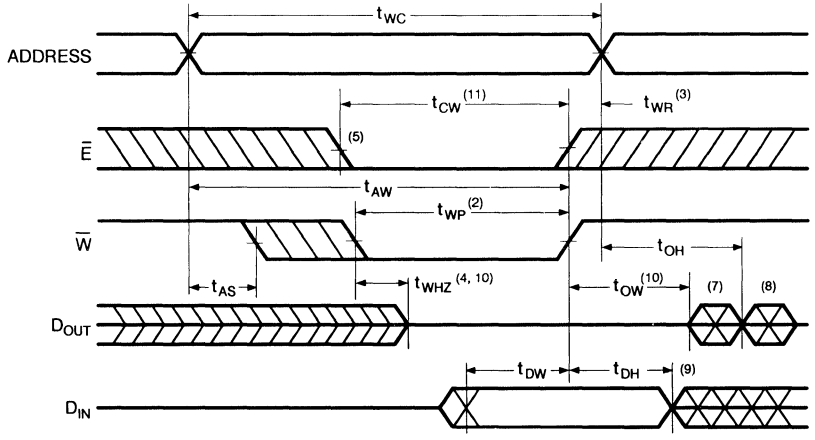
Switching Waveforms (Write Cycle)

WRITE CYCLE 1(1)



Switching Waveforms (Write Cycle)

WRITE CYCLE 2(1,6)



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the E low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

Ordering Information

Speed (Ns)	Ordering Part Number	Package Reference No.	Temperature Range
100	MS6516L-10PC	24 Pin 600 mil Plastic DIP	0°C to +70°C
100	MS6516L-10SC	24 Pin 300 mil Small Outline	0°C to +70°C

Features

- Available in 70/100 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:
  MS6264L
  — 467.5mW (Max.) Operating
  — 16.5mW (Max.) Standby
  — 500µW (Max.) Standby
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enable ($\overline{E}_1$ and E_2) for simple memory expansion
- Data retention as low as 2V

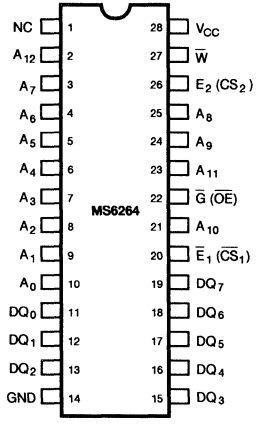
Description

The MS6264 is a high performance, low power CMOS static RAM organized as 8192 words by 8 bits. The device supports easy memory expansion with both an active LOW chip enable ($\overline{E}_1$) and an active High chip enable (E_2), as well as an active LOW output enable ($\overline{G}$) and tri-state outputs. An automatic power-down feature is included which reduces the chip power by 80% in TTL standby mode, and by over 95% in full power-down mode.

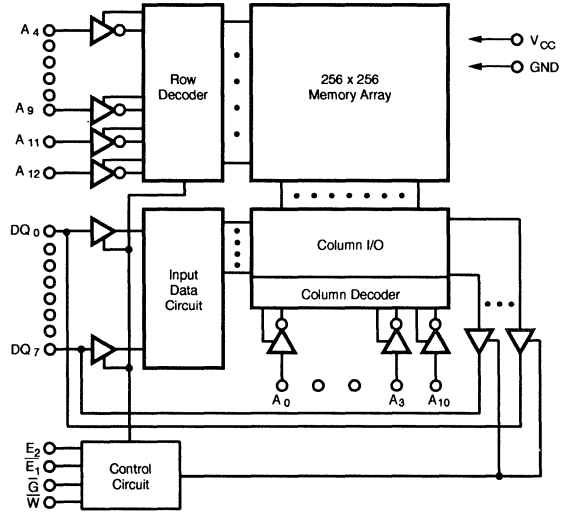
The device is manufactured in MOSEL-VITELIC's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MS6264 is packaged in the JEDEC standard 28 pin 600 mil wide DIP and 330 mil wide SOG.

Pin Configuration



Functional Block Diagram



Pin Descriptions

A_0 - A_{12} Address Inputs
These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input
E_2 Chip Enable 2 Input
E_1 is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

Truth Table

MODE	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

Absolute Maximum Ratings (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.3 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-40 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Capacitance (1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

6

DC Electrical Characteristics (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6264L MIN.	TYP.(1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		-0.3	-	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	-	6.0	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0V to V_{CC}	-2	-	2	µA
I_{OL}	Output Leakage Current	V_{CC}= Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V t o V_{CC}	-2	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 2.1mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC}= Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, F = F_{max}(3)	-	45	85	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	-	-	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$ $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	-	. 01	0.1	mA

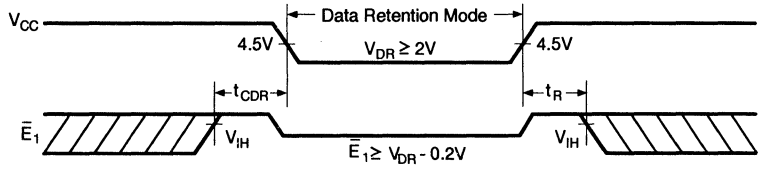
1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

Data Retention Characteristics (T_A = 0 to +70°C)

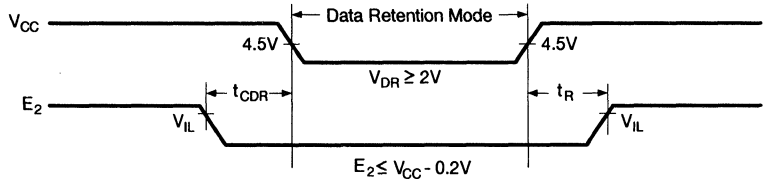
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX	UNITS
V_{DR}	V_{CC} for Data Retention	$E_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$E_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	-	2	50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(2)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform (1) ($\overline{E}_1$ Controlled)



Low V_{CC} Data Retention Waveform (2) (E_2 Controlled)



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

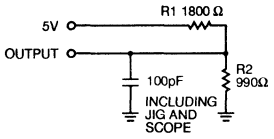


Figure 1a

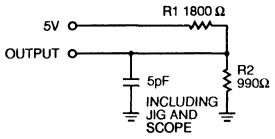
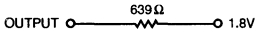


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

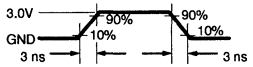


Figure 2

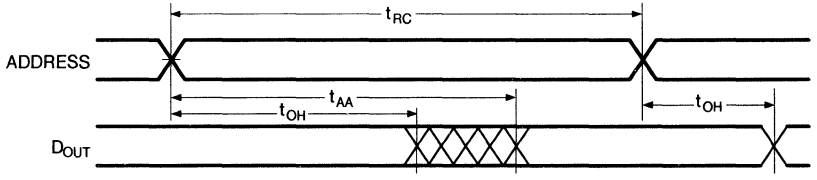
AC Electrical Characteristics (over the operating range)

READ CYCLE

JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS6264L-70 MIN.	TYP.	MAX.	MS6264L-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time		70	-	-	100	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time		-	-	70	-	-	100	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time	($\overline{E}_1$)	-	-	70	-	-	100	ns
t_{E2HQV}	t_{ACS2}	Chip Select Access Time	(E_2)	-	-	70	-	-	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		-	-	35	-	-	50	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z	($\overline{E}_1$)	5	-	-	5	-	-	ns
t_{E2HQX}	t_{CLZ2}	Chip Select to to Output Low Z	(E_2)	5	-	-	5	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		5	-	-	5	-	-	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output in High Z	($\overline{E}_1$)	0	-	35	0	-	35	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output in High Z	(E_2)	0	-	35	0	-	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	30	0	-	35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change		5	-	-	5	-	-	ns

Switching Waveforms (Read Cycle)

READ CYCLE 1(1,2,4)



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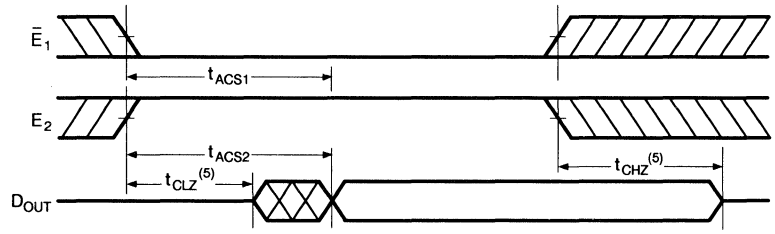
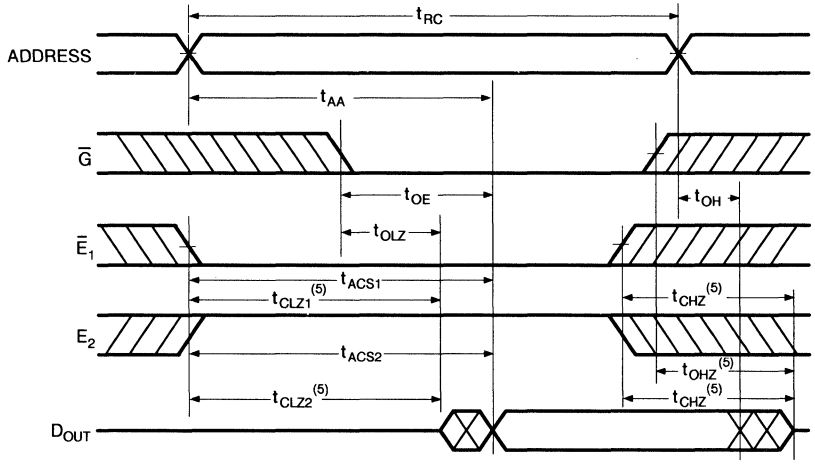
READ CYCLE 2[1,3,4]



READ CYCLE 3



Notes:

1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

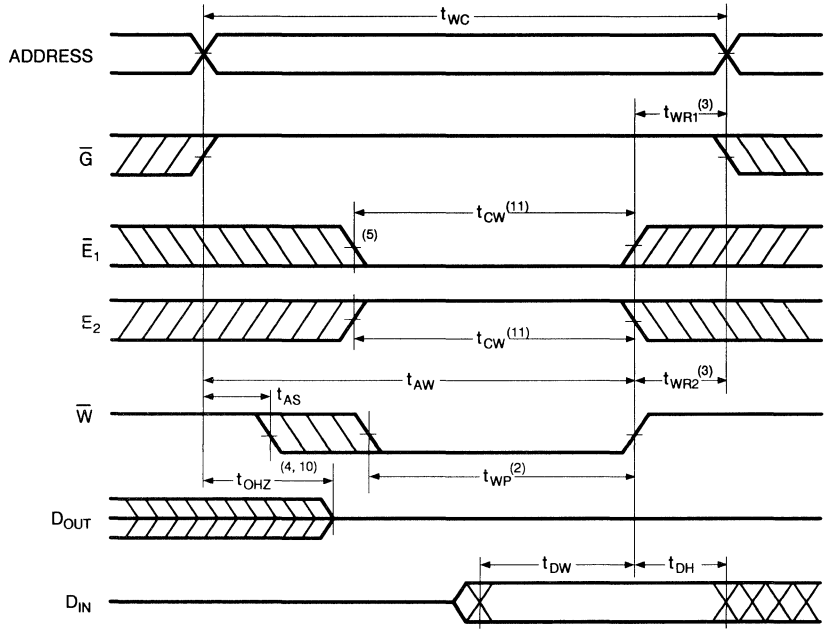
AC Electrical Characteristics (over the operating range)

WRITE CYCLE

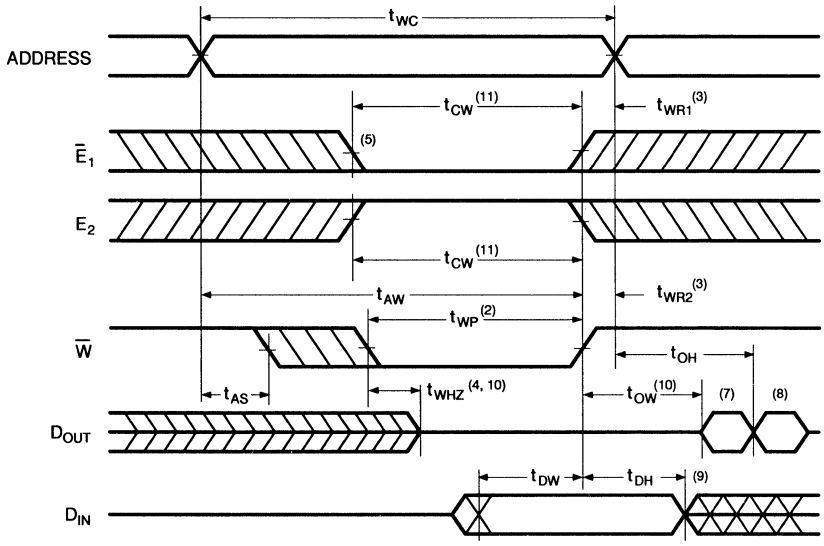
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER	MS6264L-70 MIN.	TYP.	MAX.	MS6264L-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	70	-	-	100	-	-	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	60	-	-	80	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	-	0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	65	-	-	80	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	40	-	-	60	-	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time $\overline{E}_1, W$	5	-	-	5	-	-	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time E_2	5	-	-	5	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	-	30	-	-	35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	30	-	-	40	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	-	0	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	-	30	0	-	35	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	-	-	5	-	-	ns

Switching Waveforms (Write Cycle)

WRITE CYCLE 1[1]



WRITE CYCLE 2[1,6]



Notes:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.

Ordering Information

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
70	MS6264L-70PC	28 pin 600 mil Plastic DIP	0°C to +70°C
70	MS6264L-70FC	28 pin 330 mil Small Outline	0°C to +70°C
100	MS6264L-10PC	28 pin 600 mil Plastic DIP	0°C to +70°C
100	MS6264L-10FC	28 pin 300 mil Small Outline	0°C to +70°C

MOSEL-VITELIC

MS6264N
8K x 8 CMOS STATIC RAM WITH 3.3V OPERATIONS

Features

- Available in 100 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:
  MS6264NL
  — 165mW (Max.) Operating
  — 30µW (Max.) Standby
- TTL compatible interface levels
- Single 3.3V power supply
- Fully static operation
- Three state outputs
- Two chip enable ($\overline{E}_1$ and E_2) for simple memory expansion
- Data retention as low as 2V

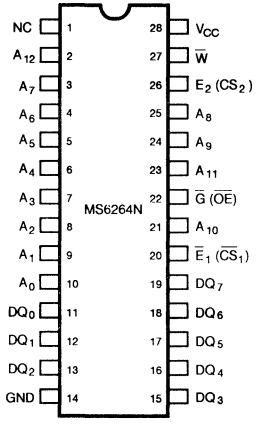
Description

The MS6264N is a high performance, low power CMOS static RAM organized as 8192 words by 8 bits. The device supports easy memory expansion with both an active LOW chip enable ($\overline{E}_1$) and an active High chip enable ($\overline{E}_2$), as well as an active LOW output enable ($\overline{G}$) and tri-state outputs. An automatic power-down feature is included which reduces the chip power by 80% in TTL standby mode, and by over 95% in full power-down mode.

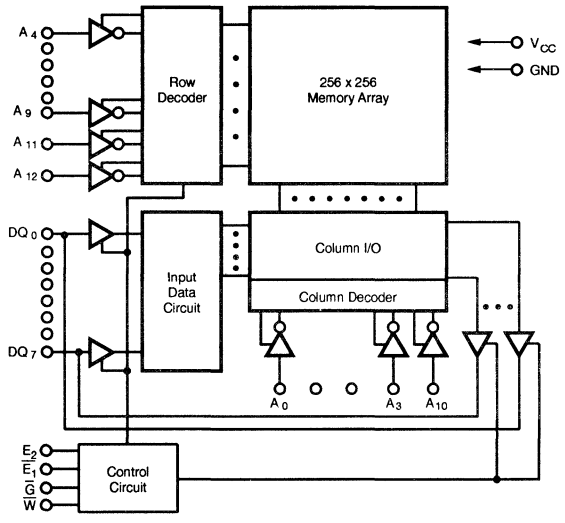
The device is manufactured in MOSEL-VITELIC's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MS6264N is packaged in the JEDEC standard 28 pin 600 mil wide DIP and 330 mil wide SOG.

Pin Configuration



Functional Block Diagram



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Pin Descriptions

A_0 - A_{12} Address Inputs
These 13 address inputs select one of the 8192 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input
E_2 Chip Enable 2 Input
E_1 is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

Truth Table

MODE	$\overline{W}$	$\overline{E}_1$	$\overline{E}_2$	$\overline{G}$	I/O OPERATION	V_{CC} CURRENT
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

Absolute Maximum Ratings (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.3 to +3.6	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	0.6	W
I_{OUT}	DC Output Current	8	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

RANGE	AMBIENT TEMPERATURE	V_{CC}
Commercial	0°C to +70°C	3.3V ± 10%

Capacitance (1) (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	V_{DQ} = 0V	8	pF

1. This parameter is guaranteed and not tested.

DC Electrical Characteristics (over the operating range)

PARAMETER NAME	PARAMETER	TEST CONDITIONS	MS6264NL MIN.	TYP.(1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		-0.3	-	+0.3	V
V_{IH}	Guaranteed Input High Voltage(2)		2.0	2.5	3.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}	-	-	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V to V_{CC}	-	-	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 1mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -0.5mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, $F = F_{max}$(3)	-	45	50	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	-	-	2	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$ $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	-	. 01	0.1	mA

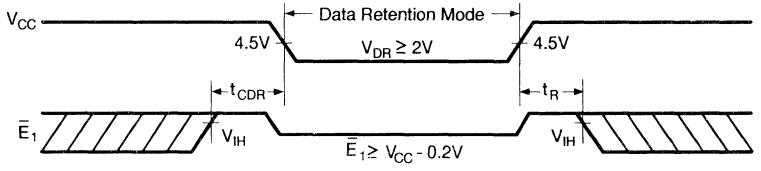
1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

Data Retention Characteristics (T_A = 0 to +70°C)

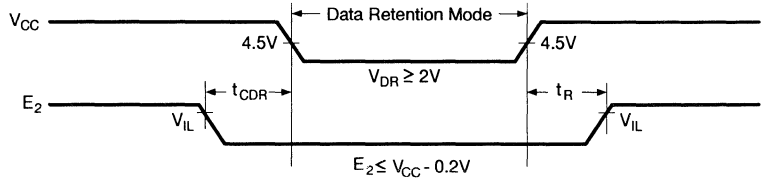
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNITS
V_{DR}	V_{CC} for Data Retention	$E_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	2.0	-	-	V
I_{CCDR}	Data Retention Current	$E_1 \geq V_{CC}$ - 0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$	-	2	50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(2)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform (1) ($\overline{E}_1$ Controlled)



Low V_{CC} Data Retention Waveform (2) (E_2 Controlled)



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AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V

AC Test Loads and Waveforms

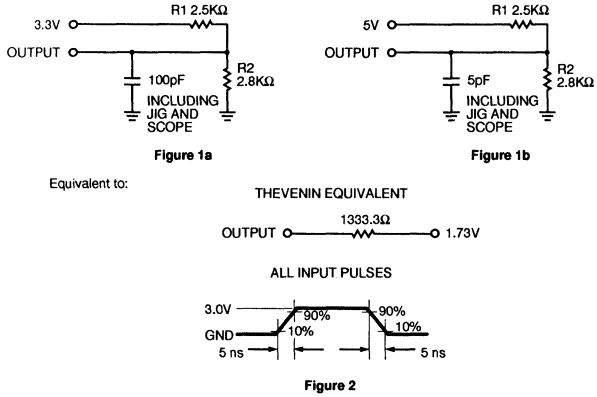
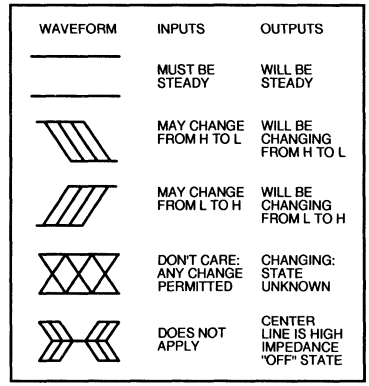


Figure 2

Key to Switching Waveforms



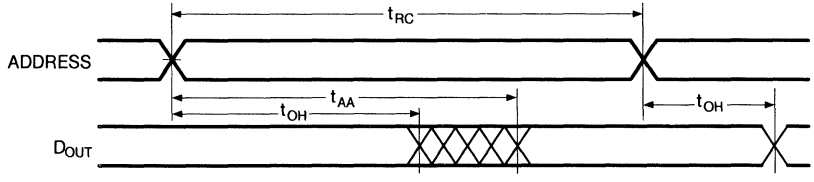
AC Electrical Characteristics (over the operating range)

READ CYCLE

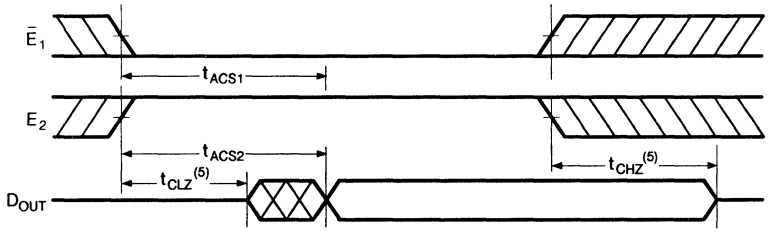
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS6264NL-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time		100	-	-	ns
t_{AVQV}	t_{AA}	Address Access Time		-	-	100	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time	($\overline{E}_1$)	-	-	100	ns
t_{E2HQV}	t_{ACS2}	Chip Select Access Time	(E_2)	-	-	100	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		-	-	50	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z	($\overline{E}_1$)	5	-	-	ns
t_{E2HQX}	t_{CLZ2}	Chip Select to to Output Low Z	(E_2)	5	-	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		5	-	-	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output in High Z	($\overline{E}_1$)	0	-	35	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output in High Z	(E_2)	0	-	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change		5	-	-	ns

Switching Waveforms (Read Cycle)

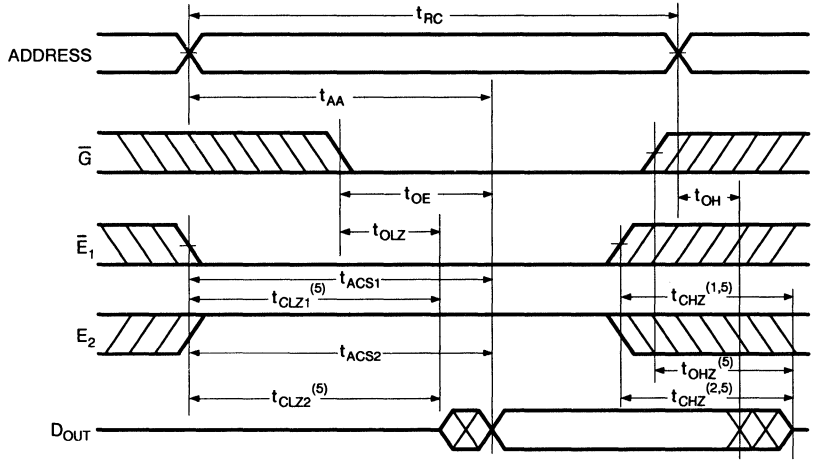
READ CYCLE 1(1,2,4)



READ CYCLE 2[1,3,4]



READ CYCLE 3[1,4]



Notes:

1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $\overline{E}_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

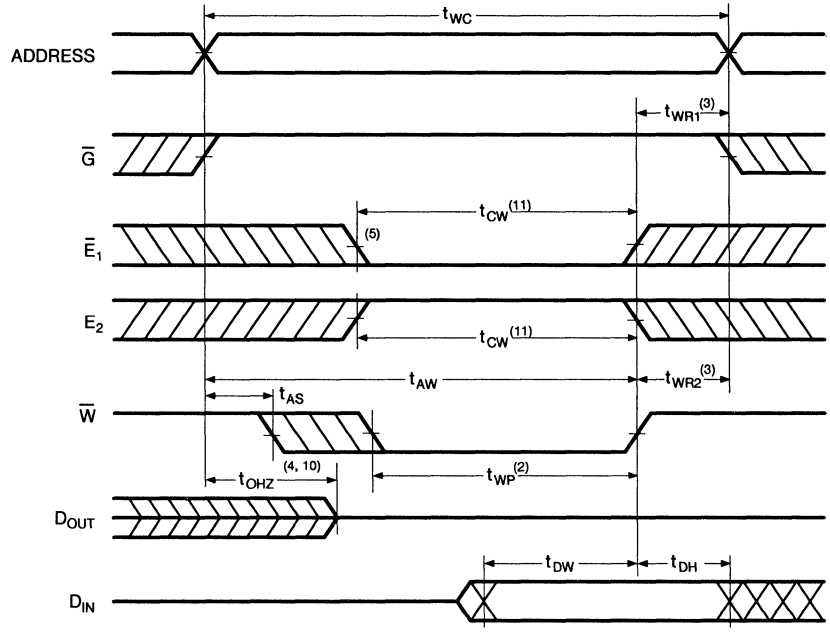
AC Electrical Characteristics (over the operating range)

WRITE CYCLE

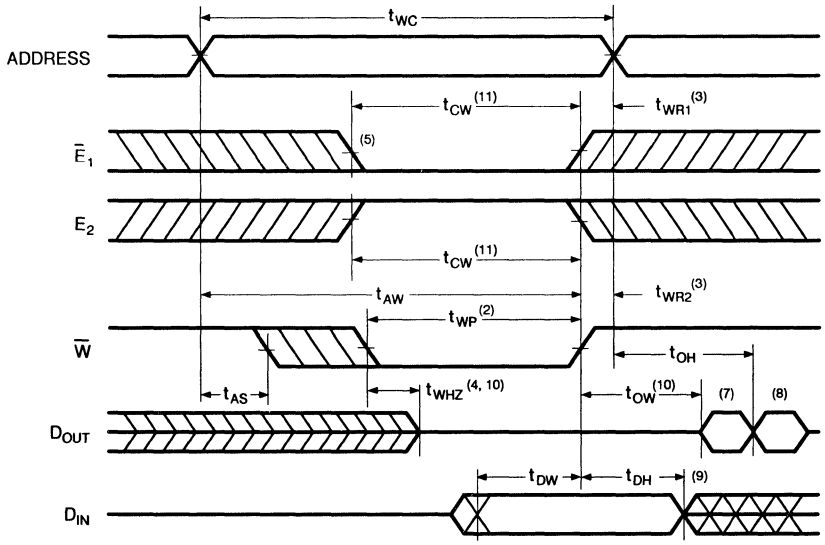
JEDEC PARAMETER NAME	PARAMETER NAME	PARAMETER		MS6264NL-10 MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time		100	-	-	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write		80	-	-	ns
t_{AVWL}	t_{AS}	Address Set up Time		0	-	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write		80	-	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width		60	-	-	ns
t_{WHAX}	t_{WR1}	Write Recovery Time	E_1, W	5	-	-	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time	E_2	5	-	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		-	-	35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap		45	-	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time		0	-	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		0	-	35	ns
t_{WHQX}	t_{OW}	End of Write to Output Active		5	-	-	ns

Switching Waveforms (Write Cycle)

WRITE CYCLE 1[1]



WRITE CYCLE 2[1,6]



Notes:

1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.

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Ordering Information

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
100	MS6264NL-10PC	28 pin 600 mil Plastic DIP	0°C to +70°C
100	MS6264NL-10FC	28 pin Plastic Small Outline	0°C to +70°C

MS6265
8K x 8 SLOW SPEED CMOS STATIC RAM
ULTRA LOW DATA RETENTION CURRENT

Features

- Available in 100 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:
  MS6265
  - 220mW (Max.) Operating
  - 5.5µW (Max.) Power Down
    16.6µW (Max.) Industrial Temp
  - 0.6µA (Max.) I_{CCDR}
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enable ($\overline{E}_1$ and E_2) for simple memory expansion
- 64K bit EPROM pin compatible
- Wide temperature range: -40 to + 85°C

Description

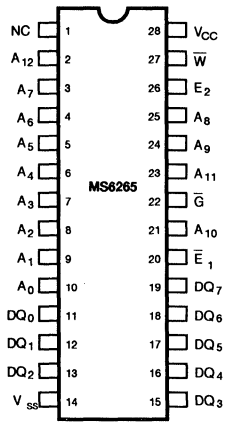
The MS6265 is a slow speed, very low data retention current, 64K bit static RAM, organized as 8192 x 8. The MS6265LL is designed to operate over industrial temperature range of -40°C to +85°C.

This SRAM is fully static in operation. Either of the chip enable controls ($\overline{E}1$ or E2) can be used to take the device to its low low data retention mode (I_{CCDR}).

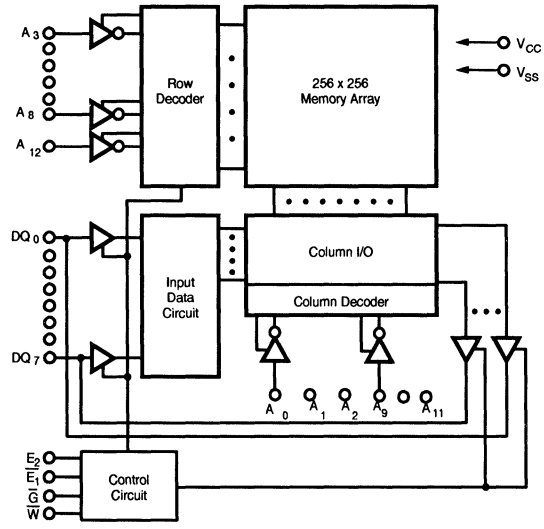
Write cycle occurs when chip enable $\overline{E}1$ is low, E2 is high, and write enable, $\overline{W}$, is low. Output enable control $\overline{G}$ has no control function in the write cycle.

Read Cycle occurs when chip enable $\overline{E}1$, is low, E2 is high, write enable $\overline{W}$ is high and output enable $\overline{G}$ is low.

Pin Configurations



Functional Block Diagram



Pin Descriptions

A_0 - A_{12} Address Inputs
These 13 address inputs select one of the 8192 X 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input
$\overline{E}_2$ Chip Enable 2 Input
E_1 is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected (in a standby power mode). The DQ pins are in the high-impedance state when the device is deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. With the output enable active and the chip selected and write enable inactive, read data will be present on the DQ pins. The DQ pins will be in the high impedance (three state) output mode when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip selected, $\overline{W}$ is HIGH and $\overline{G}$ LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

Vss Ground

TruthTable

Mode	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O Operation	V_{CC} Current
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

Absolute Maximum Ratings (1)

Symbol	Parameter		Rating	Units
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to Vcc + 0.3	V
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	V
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-55 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		±40(2)	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability and degrade performance characteristics.
2. Output should not be shorted for more than 30 seconds.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Special Commercial	-10°C to +70°C	5V ± 10%
Industrial	-40°C to +85°C	5V ± 10%

Capacitance(1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

1. This parameter is guaranteed and not tested.

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DC Electrical Characteristics (over the operating range)

Parameter Name	Parameter	Test Conditions	MS6265 Min.	Typ. (1)	Max	Units
V_{IL}	Guaranteed Input Low Voltage(2)		–0.3	-	0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	-	Vcc + 0.3	V
I_{IL}	Input Leakage Current	V_{IN} = 0V to V_{CC}, $E_2 \geq$ Vcc - 0.2V, $\overline{E}_1 \leq 0.2V$	-	-	1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V t o V_{CC}	-	-	1	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = –4mA	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC}= Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, $F = F_{max}$(3)	-	-	40	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	-	-	10	µA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 \geq V_{CC}$ – 0.2V, $E_2 \leq$ 0.2 $T_A \leq 70°C$	-	-	1	µA
		$V_{IN} \geq$ VCC -0.2V OR $V_{IN} \leq$ 0.2V $T_A \leq 85°C$	-	-	3	µA

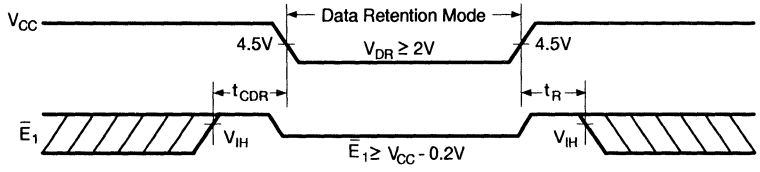
1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

Data Retention Characteristics (over the specified operating range)

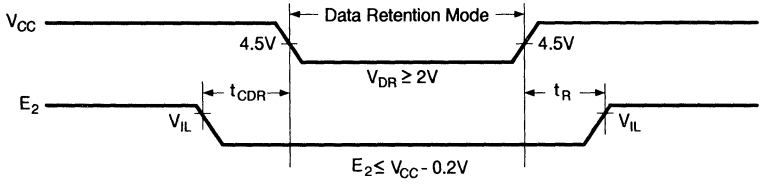
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E}_1 \geq V_{CC}$ – 0.2V, $E_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V		2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E}_1 \geq V_{DR}$ – 0.2V, $E_2 \leq$ 0.2V, $V_{IN} \geq V_{DR}$ – 0.2V or $V_{IN} \leq$ 0.2V	$T_A \leq 70°C$	-	-	0.6	µA(1)
			$T_A \leq 85°C$			2.0	µA(1)
I_{IL}	Input Leakage Current			-	-	2	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform		0	-	-	ns
t_R	Operation Recovery Time			t_{RC}(2)	-	-	ns

1. V_{DR} = 3V, T_A = Specified
2. t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform (1) ($\overline{E}_1$ Controlled)



Low V_{CC} Data Retention Waveform (2) ($\overline{E}_2$ Controlled)



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
———	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

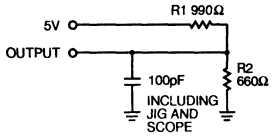


Figure 1a

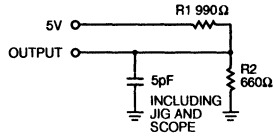


Figure 1b

Equivalent to:

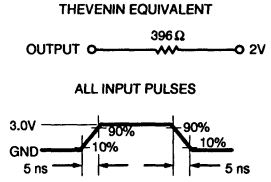


Figure 2

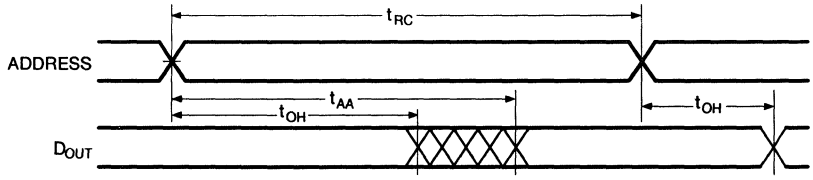
AC Electrical Characteristics (over the operating range)

Read Cycle

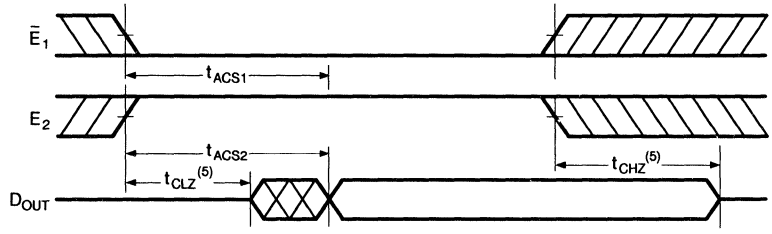
JEDEC Parameter Name	Parameter Name	Parameter	MS6265-10 Min.	MS6265-10 Max.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time	100	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	100	ns
t_{ELQV}	t_{ACS1}	Chip Enable Access Time	-	100	ns
t_{ELQV}	t_{ACS2}	Chip Enable Access Time	-	100	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-	40	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	10	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	-	30	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-	20	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	10	-	ns

Switching Waveforms (Read Cycle)

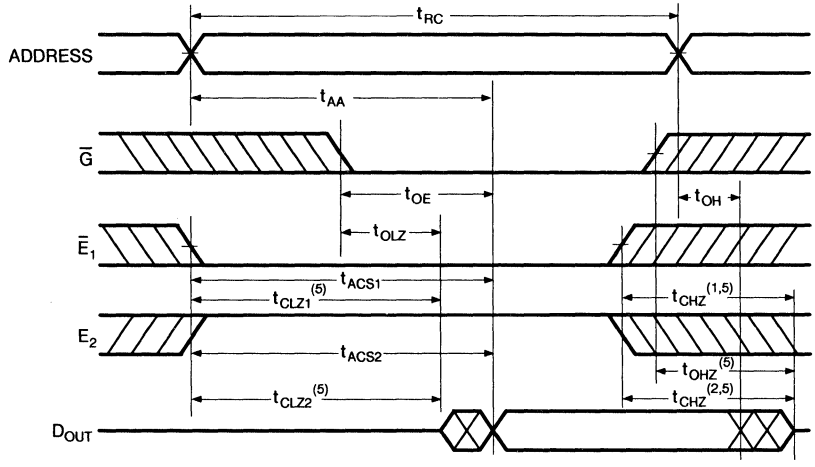
READ CYCLE 1[1,2,4]



READ CYCLE 2[1,3,4]



READ CYCLE 3[1,4]



NOTES:
1. $\overline{W}$ is high for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IH}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.

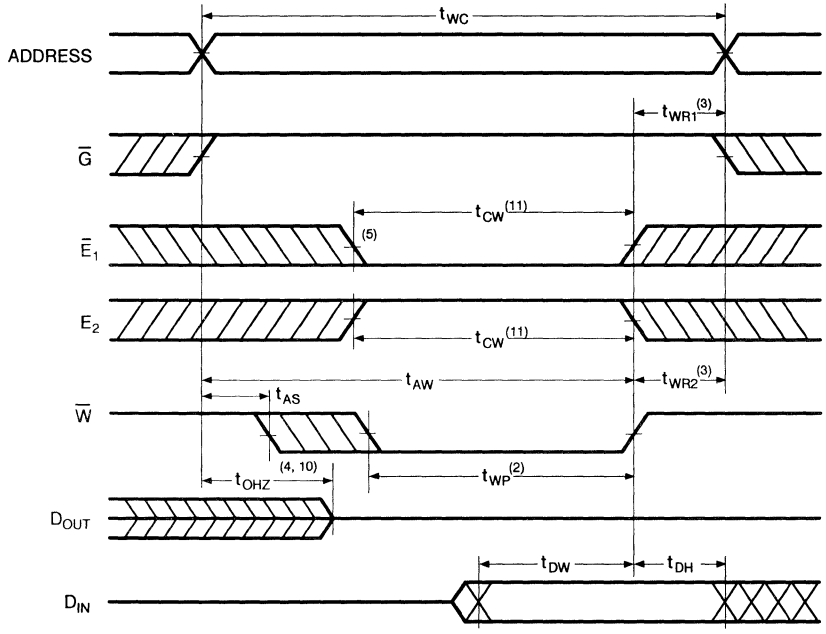
AC Electrical Characteristics (over the operating range)

Write Cycle

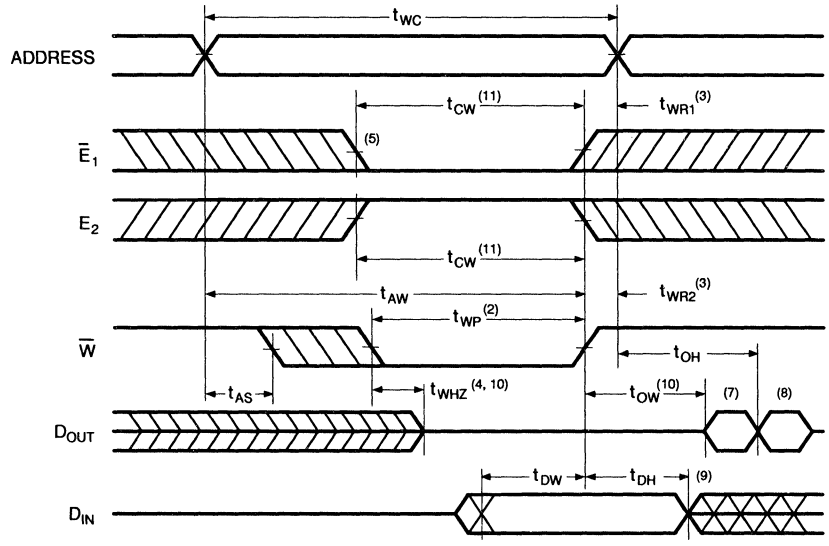
JEDEC Parameter Name	Parameter Name	Parameter	MS6265-10 Min.	MS6265-10 Max.	Unit
t_{AVAX}	t_{WC}	Write Cycle Time	100	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	90	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	20	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	90	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	60	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	10	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	20	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	50	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	20	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	10	-	ns

Switching Waveforms (Write Cycle)

WRITE CYCLE 1[1]



WRITE CYCLE 2[1,6]



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.

Ordering Information

Speed (ns)	Ordering Part Number	Package Reference No.	Temperature Range
100	MS6265-10NC	28 Pin 300 mil Plastic DIP	0°C to +70°C
100	MS6265-10FC	28 Pin 330 mil Small Outline	0°C to +70°C
100	MS6265-10PC	28 Pin 600 mil Plastic DIP	0°C to +70°C
100	MS6265-10PI	28 Pin 600 mil Plastic DIP	-40°C to + 85°C
100	MS6265-10FI	20 Pin 330 mil Small Outline	-40°C to + 85°C
100	MS6265-10NI	28 Pin 300 mil Plastic DIP	-40°C to + 85°C

MOSEL-VITELIC ***MS62256***
32K x 8 CMOS
STATIC RAM

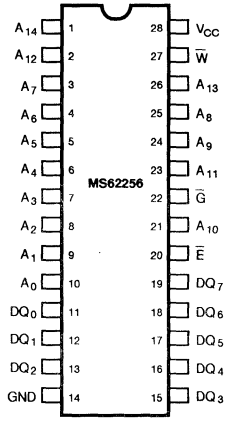
Features

- High-speed – 70/100 ns
- Low Power dissipation:
  MS62256L
  - 385mW (Max.) Operating
  - 550µW (Typ.) Power Down
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V

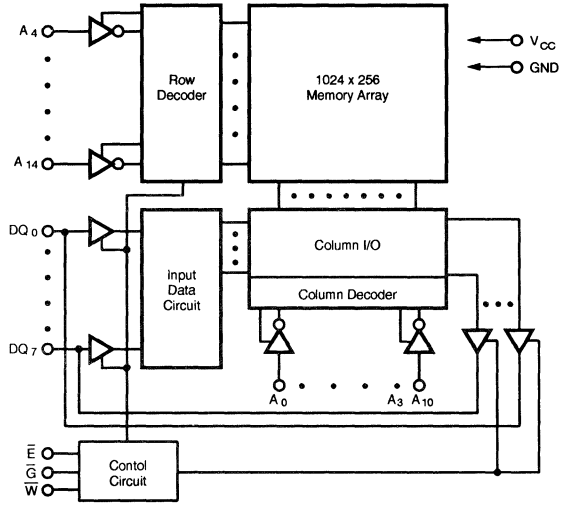
Description

The MS62256 is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with system I/O bus. The MS62256 is available in a standard 28-pin 600 mil plastic DIP and 330 mil SOG packages.

Pin Configurations



Functional Block Diagram



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Pin Descriptions

A_0 - A_{14} Address Inputs
These 15 address inputs select one of the 32768 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input
$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

Truth Table

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Output Disabled	L	H	H	High Z
Write	L	X	L	D_{IN}

Absolute Maximum Ratings (1)

Symbol	Parameter		Rating	Units
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-40 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions		-70 Min.	-70 Typ.(1)	-70 Max.	-10 Min.	-10 Typ.(1)	-10 Max.	Units
V_{IL}	Guaranteed Input LOW Voltage(2)(3)			–0.3	—	+0.8	–0.3	—	+0.8	V
V_{IH}	Guaranteed Input HIGH Voltage(2)			2.2	—	6.0	2.2	—	6.0	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{IN} = 0V to V_{CC}		–2	—	2	–2	—	2	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{IN} = 0V to V_{CC}		–2	—	2	–2	—	2	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2.1mA		—	—	0.4	—	—	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OH} = -1mA		2.4	3.5	—	2.4	—	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IL}, $I_{I/O}$ = 0mA, F=F_{max}(4)		—	—	80	—	—	70	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, $I_{I/O}$ = 0mA		—	—	3	—	—	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}$ ≥ V_{CC} – 0.2V	MS62256L	—	—	0.1	—	—	0.1	mA
		V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	MS62256	—	—	1	—	—	1	mA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (Min.) = –3.0V for pulse width ≤ 20ns
4. F_{MAX} = $1/t_{RC}$.

Capacitance(1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

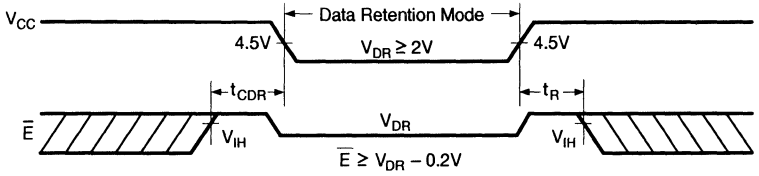
1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.(2)	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E}$ ≥ V_{CC}-0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V	-	2	50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Retention Waveform	t_{RC}(3)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. V_{CC} = 3V
3. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



6

AC Test Conditions

Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveform

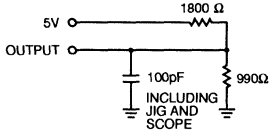


Figure 1a

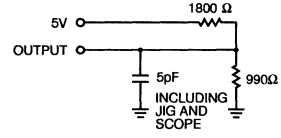


Figure 1b

Equivalent to:

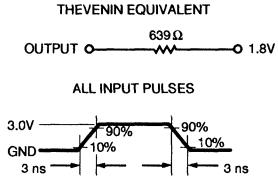


Figure 2

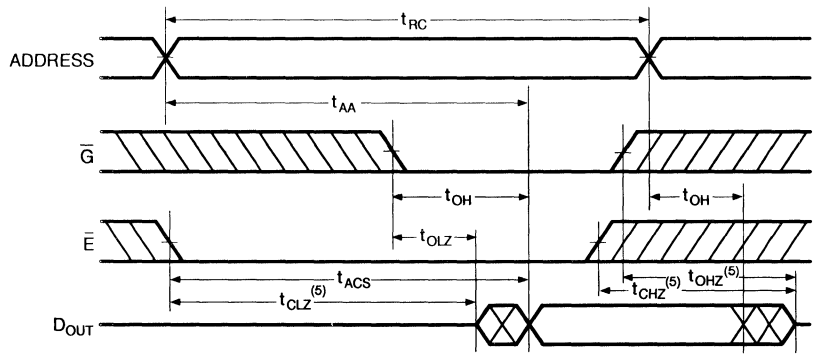
AC Electrical Characteristics (over the commercial operating range)

Read Cycle

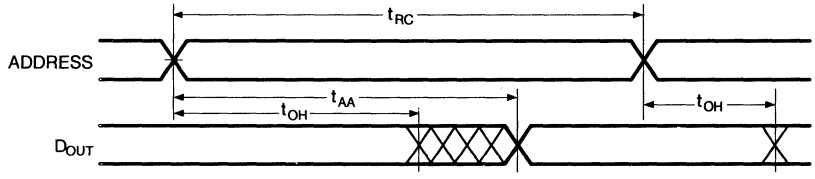
Jedec Parameter Name	Parameter Name	Parameter	MS62256-70 Min.	MS62256-70 Max.	MS62256-10 Min.	MS62256-10 Max.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time	70	-	100	-	ns
t_{AVQV}	t_{AA}	Address Access Time	-	70	-	100	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-	70	-	100	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-	40	-	50	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	5	-	10	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5	-	5	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	0	30	0	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5	-	10	-	ns

Switching Waveforms (Read Cycle)

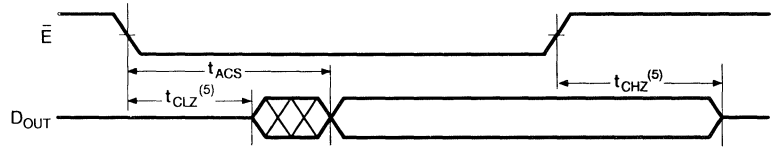
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]



READ CYCLE 3[1, 3, 4]



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

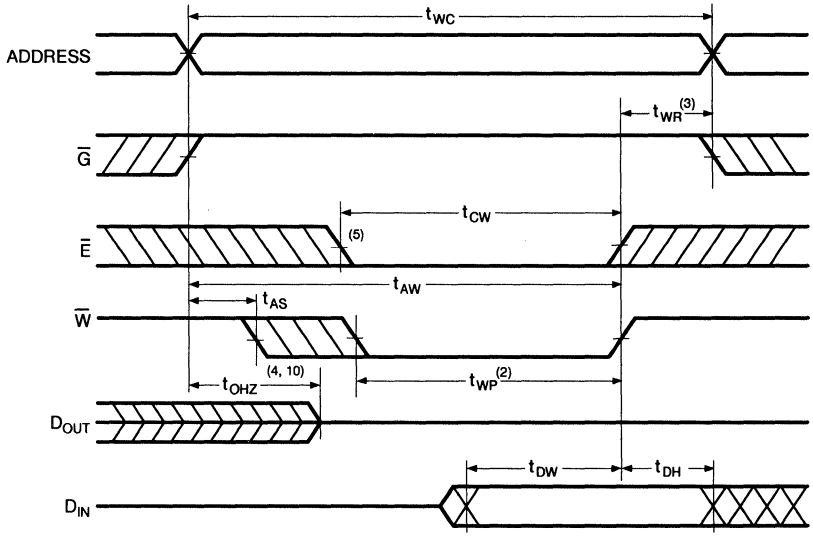
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

Jedec Parameter Name	Parameter Name	Parameter	MS62256-70		MS62256-10		Unit
			Min.	Max.	Min.	Max.	
t_{AVAX}	t_{WC}	Write Cycle Time	70	-	100	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	65	-	90	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	-	0	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	65	-	90	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	55	-	75	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	5	-	5	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	30	0	35	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	35	-	40	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	-	0	-	ns
t_{GHZQ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	40	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	5	-	5	-	ns

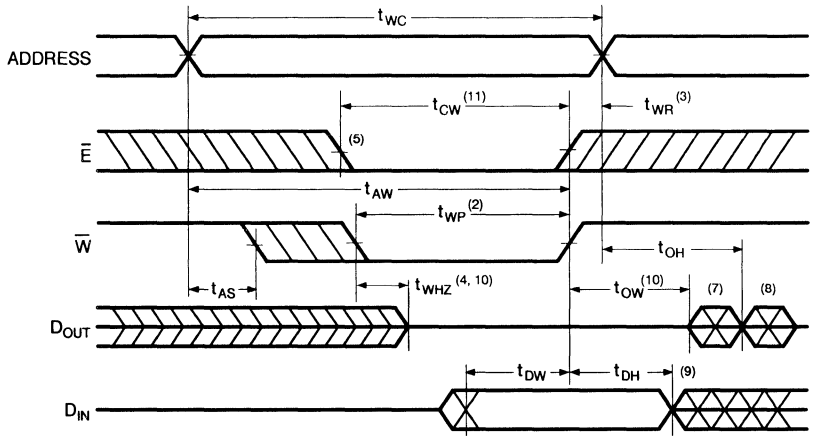
Switching Waveforms (Write Cycle)

WRITE CYCLE 1[1]



Switching Waveforms (Write Cycle)

WRITE CYCLE 2(1,6)



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

Ordering Information

Speed (Ns)	Ordering Part Number	Package Reference No.	Temperature Range
70	MS62256L-70FC	28 Pin 330 mil Small Outline	0°C to +70°C
70	MS62256L-70PC	28 Pin 600 mil Plastic DIP	0°C to +70°C
70	MS62256L-70NC	28 Pin 300 mil Plastic DIP	0°C to +70°C
100	MS62256L-10FC	28 Pin 330 mil Small Outline	0°C to +70°C
100	MS62256L-10PC	28 Pin 600 mil Plastic DIP	0°C to +70°C
100	MS62256L-10NC	28 Pin 300 mil Plastic DIP	0°C to +70°C

MOSEL-VITELIC ***MS62256N***

32K x 8 CMOS STATIC RAM WITH 3.3V OPERATIONS

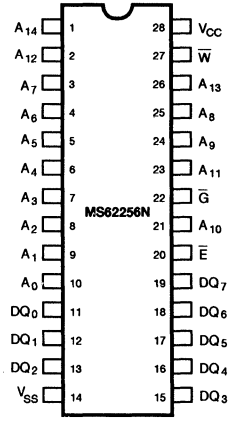
Features

- High-speed – 70/100 ns
- Low Power dissipation:
  MS62256NL
  - 200mW (Max.) Operating
  - 150µW (Typ.) Power Down
- Fully static operation
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V

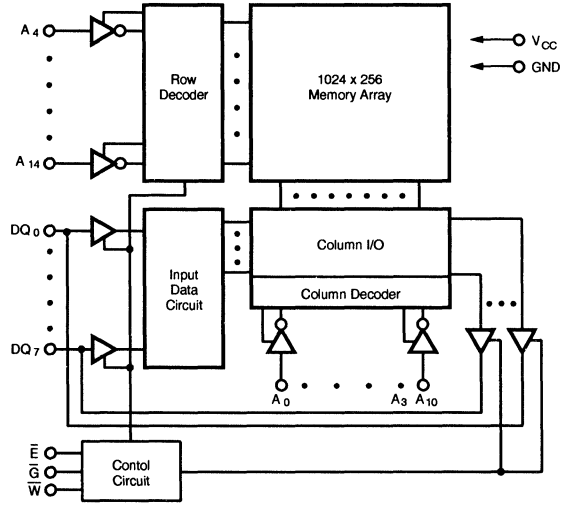
Description

The MS62256N is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 3.3 volt supply. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS62256N is available in a standard 300 mil SOJ and SOG.

Pin Configurations



Functional Block Diagram



Pin Descriptions

A_0 - A_{14} Address Inputs

These 15 address inputs select one of the 32768 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input

$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input

The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input

The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports

These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

Truth Table

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Output Disabled	L	H	H	High Z
Write	L	X	L	D_{IN}

Absolute Maximum Ratings (1)

Symbol	Parameter		Rating	Units
V_{CC}	Supply Voltage		-0.3 to 7	V
V_{IN}	Input Voltage		-0.3 to 7	
V_{DQ}	Input/Output Voltage Applied		-0.3 to 6	
T_{BIAS}	Temperature Under Bias	Plastic	-10 to +125	°C
T_{STG}	Storage Temperature	Plastic	-40 to +150	°C
P_D	Power Dissipation		1.0	W
I_{OUT}	DC Output Current		50	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V +10%, -5%

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions		-70 Min.	-70 Typ.(1)	-70 Max.	-10 Min.	-10 Typ.(1)	-10 Max.	Units
V_{IL}	Guaranteed Input Low Voltage(2)(3)			-0.3	—	+0.8	-0.3	—	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)			2.2	—	6.0	2.2	—	6.0	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0V to V_{CC}		—	—	2	—	—	2	µA
I_{OL}	Output Leakage Current	V_{CC}= Max, $\overline{E}$ = V_{IH}, or $\overline{G}$ = V_{IH}, V_{IN} = 0V to V_{CC}		—	—	2	—	—	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 1mA		—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -250µA		2.0	3.5	-	2.0	3.5	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IL}, $I_{I/O}$ = 0mA, F_{max}(4)		—	—	60	—	—	60	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, $I_{I/O}$ = 0mA		—	—	10	—	—	10	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}$ ≥ V_{CC} - 0.2V	MS62256N	—	—	2	—	—	2	mA
		V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V	MS62256NL	—	—	100	—	—	100	µA

1. Typical characteristics are at V_{CC} = 3.3V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (Min.) = −1.5V for pulse width ≤ 20ns
4. F_{MAX} = $1/t_{RC}$.

Capacitance(1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

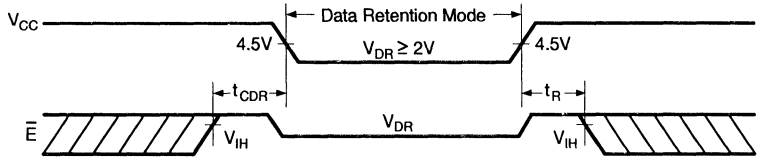
1. This parameter is guaranteed and not tested.

Data Retention Characteristics(1) (over the commercial operating range)

Symbol	Parameter	Test Conditions	Min.	Typ.(2)	Max(3)	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E}$ ≥ V_{CC}-0.2V, $\overline{G}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	2.0	-	-	V
I_{CCDR}	Data Retention Current	$\overline{E_T}$ ≥ V_{CC}-0.2V, $\overline{G}$ ≥ V_{CC} -0.2V, V_{IN} ≥ V_{CC}-0.2V or V_{IN} ≤ 0.2V	-	2	50	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(4)	-	-	ns

1. Applies to L verion only
2. V_{CC} = 2V, T_A = +25°C
3. V_{CC} = 3.3V
4. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveform

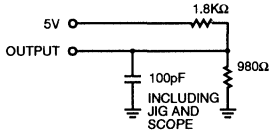


Figure 1a

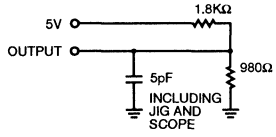
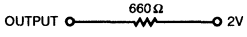


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

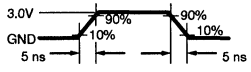


Figure 2

AC Electrical Characteristics (over the commercial operating range)

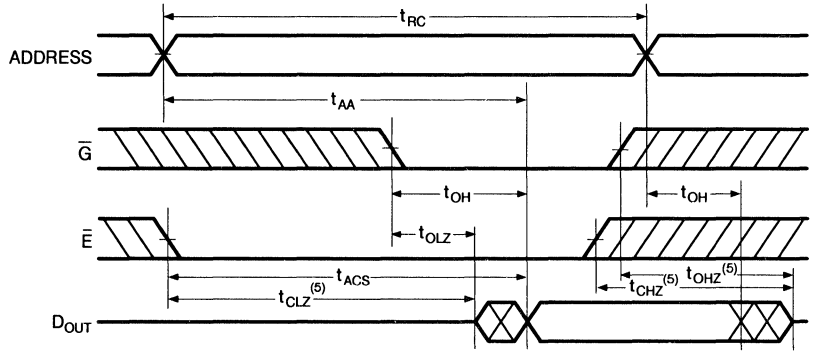
Read Cycle

Jedec Parameter Name	Parameter Name	Parameter	MS62256NL-70 Min.	MS62256NL-70 Max.	MS62256NL-10 Min.	MS62256NL-10 Max.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time	-	70	-	100	ns
t_{AVQV}	t_{AA}	Address Access Time	-	70	-	100	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-	70	-	100	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-	35	-	40	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	10	-	15	-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	0	-	0	-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	0	35	0	40	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	8	-	8	-	ns

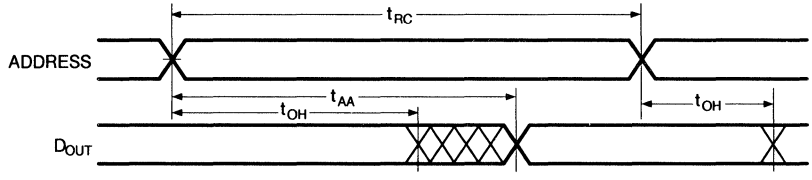
6

Switching Waveforms (Read Cycle)

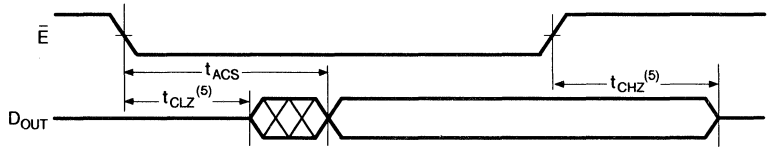
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]



READ CYCLE 3[1, 3, 4]



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

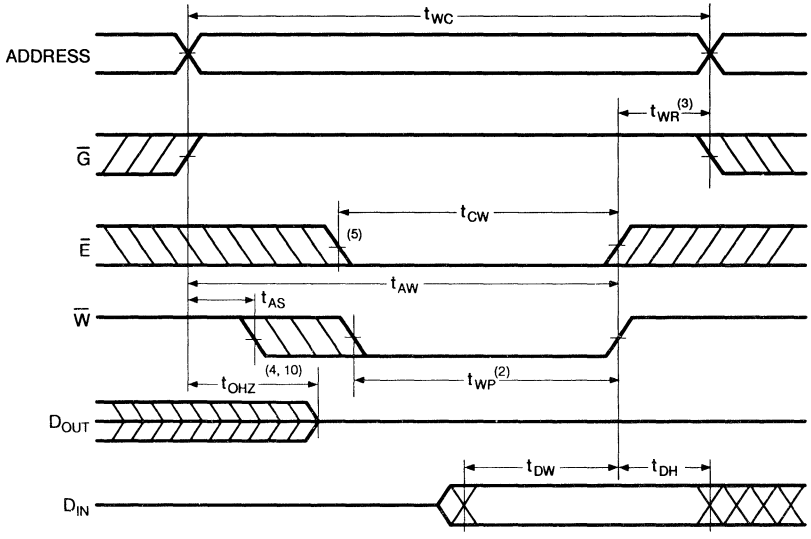
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

Jedec Parameter Name	Parameter Name	Parameter	MS62256NL-70		MS62256NL-10		Unit
			Min.	Max.	Min.	Max.	
t_{AVAX}	t_{WC}	Write Cycle Time	70	-	100	-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	55	-	85	-	ns
t_{AVWL}	t_{AS}	Address Set up Time	3	-	5	-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	45	-	65	-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	35	-	45	-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	5	-	7	-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0	30	0	35	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	30	-	35	-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	5	-	0	-	ns
t_{GHZQ}	t_{OHZ}	Output Disable to Output in High Z	0	35	0	40	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	6	-	8	-	ns

Switching Waveforms (Write Cycle)

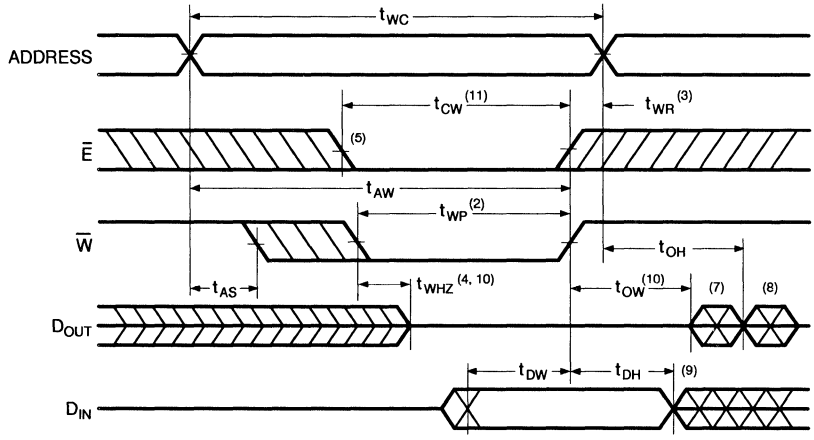
WRITE CYCLE 1[1]



6

Switching Waveforms (Write Cycle)

WRITE CYCLE 2(1,6)



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

Ordering Information

Speed (Ns)	Ordering Part Number	Package Reference No.	Temperature Range
70	MS62256NL-70SC	28 Pin 300 mil SOG	0°C to +70°C
70	MS62256NL-70RC	28 Pin 300 mil SOJ	0°C to +70°C
100	MS62256NL-10SC	28 Pin 300 mil SOG	0°C to +70°C
100	MS62256NL-10RC	28 Pin 300 mil SOJ	0°C to +70°C

MS62256C
32K x 8 CMOS STATIC RAM

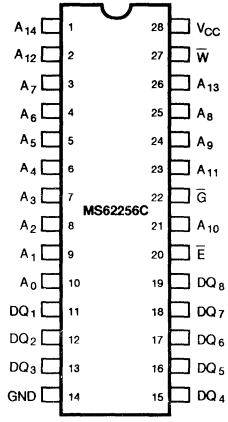
Features

- High-speed – 70/100 ns
- Low Power dissipation:
  - — 385mW (Max) Operating
  - — 16.5mW (Max) Standby
  - — 0.55mW (Max) Power-down
  - — 5μA (Max) I_{CCDR}
- Fully static operation
- All inputs and outputs directly TTL compatible
- Three state outputs
- Ultra low data retention supply current at V_{CC} = 2V
- Data retention as low as 2V

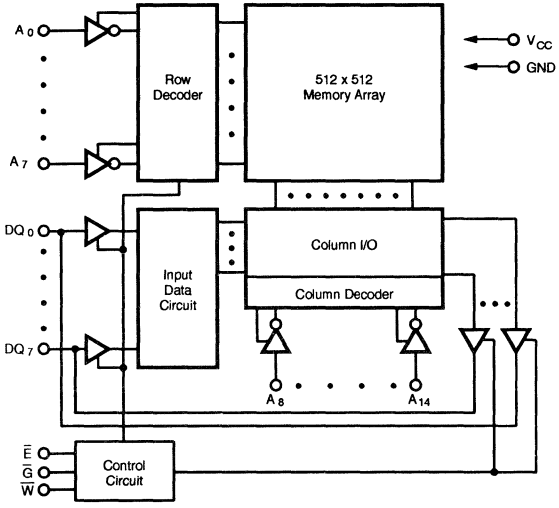
Descriptions

The MS62256C is a 262,144-bit static random access memory organized as 32,768 words by 8 bits and operates from a single 5 volt supply. It is built with MOSEL-VITELIC's high performance twin tub CMOS process. Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures. The MS62256C is available in a standard 28-pin 600 and 300 mil plastic DIP and 330 mil wide SOG.

Pin Configurations



Functional Block Diagram



6

Pin Descriptions

A_0 - A_{14} Address Inputs
These 15 address inputs select one of the 32,768 x 8-bit words in the RAM.

$\overline{E}$ Chip Enable Input
$\overline{E}$ is active LOW. The chip enable must be active to read from or write to the device. If it is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip enabled, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

Truth Table

Mode	$\overline{E}$	$\overline{G}$	$\overline{W}$	I/O Operation
Standby	H	X	X	High Z
Read	L	L	H	D_{OUT}
Read	L	H	H	High Z
Write	L	X	L	D_{IN}

Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Units
V_{CC}	Supply Voltage	–0.3 to 7	V
V_{IN}	Input Voltage	–0.3 to 7	
V_{DQ}	Input/Output Voltage Applied	–0.3 to 6	
T_{BIAS}	Temperature Under Bias	–10 to +125	°C
T_{STG}	Storage Temperature	–40 to +150	°C

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Temperature	V_{cc}
Commercial	0°C to +70°C	5V ± 10%

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions		-70 Min.	-70 Typ.(1)	-70 Max.	-10 Min.	-10 Typ.(1)	-10 Max.	Units
V_{IL}	Guaranteed Input LOW Voltage(2)(3)			–0.3	-	+0.8	–0.3	-	+0.8	V
V_{IH}	Guaranteed Input HIGH Voltage(2)			2.2	-	6	2.2	-	6	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0V to V_{CC}		–2	-	2	–2	-	2	µA
I_{OL}	Output Leakage Current	V_{CC}= Max, $\overline{E}$ = V_{IH}, V_{IN} = 0V t o V_{CC}		–2	-	2	–2	-	2	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 2.1mA		-	-	0.4	-	-	0.4	V
V_{OH}	Output HIGH Voltage	V_{CC}= Min, I_{OH} = –1mA		2.4	-	-	2.4	-	-	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IL}, $I_{I/O}$ = 0mA, F=F_{max}(4)		-	-	80	-	-	70	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}$ = V_{IH}, $I_{I/O}$ = 0mA		-	-	3	-	-	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}$ ≥ V_{CC} – 0.2V	MS62256CL	-	-	0.1	-	-	0.1	mA
			MS62256CLL			20			20	µA

1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. V_{IL} (Min.) = –3.0V for pulse width ≤ 20ns
3. F_{MAX} = $1/t_{RC}$.

Capacitance(1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$ = 0V	8	pF

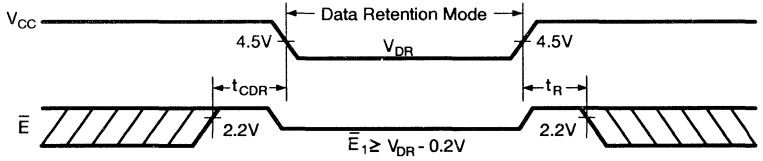
1. This parameter is guaranteed and not tested.

Data Retention Characteristics (over the commercial operating range)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E}$ ≥ V_{CC}-0.2V	2.0	-	5.5	V
I_{CCDR}	Data Retention Current MS62256C	V_{DR} = 3.0V, $\overline{E}$ ≥ V_{DR} – 0.2V	-	1.0	$10^{2)}$	µA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time		t_{RC}(3)	-	-	ns

1. V_{CC} = 2V, T_A = +25°C
2. V_{DR} = 3.0 V, T_A = 0°C to 40°C, I_{CCDR} = 5µA
3. t_{RC} = Read Cycle Time

Timing Waveform Low V_{CC} Data Retention Waveform



AC Test Conditions

Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	3ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

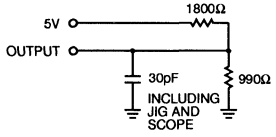


Figure 1a

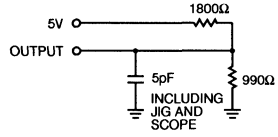
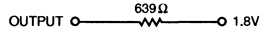


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

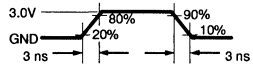


Figure 2

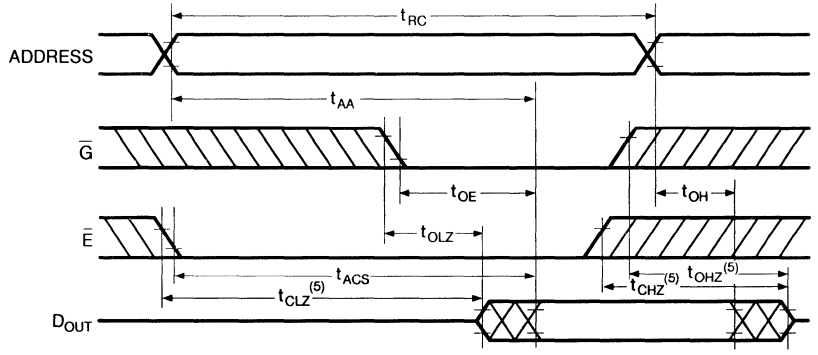
AC Electrical Characteristics (over the commercial operating range)

Read Cycle

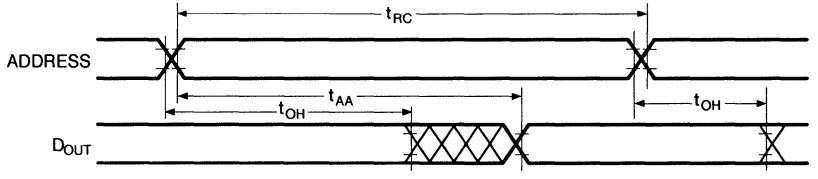
Jedec Parameter Name	Parameter Name	Parameter	MS62256C-70 Min.	Typ.	Max.	MS62256C-10 Min.	Typ.	Max.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time	70		-	100		-	ns
t_{AVQV}	t_{AA}	Address Access Time	-		70	-		100	ns
t_{ELQV}	t_{ACS}	Chip Enable Access Time	-		70	-		100	ns
t_{GLQX}	t_{OE}	Output Enable to Output Valid	-		40	-		50	ns
t_{EHQZ}	t_{CLZ}	Chip Enable to Output Low Z	10		-	10		-	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		-	5		-	ns
t_{EHQZ}	t_{CHZ}	Chip Disable to Output in High Z	-		30	-		35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	-		30	-		35	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change	5		-	10		-	ns

Switching Waveforms (Read Cycle)

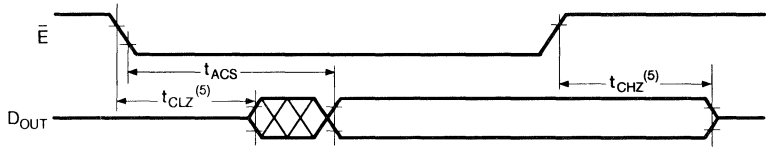
READ CYCLE 1[1]



READ CYCLE 2[1, 2, 4]



READ CYCLE 3[1, 3, 4]



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}$ transition low.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

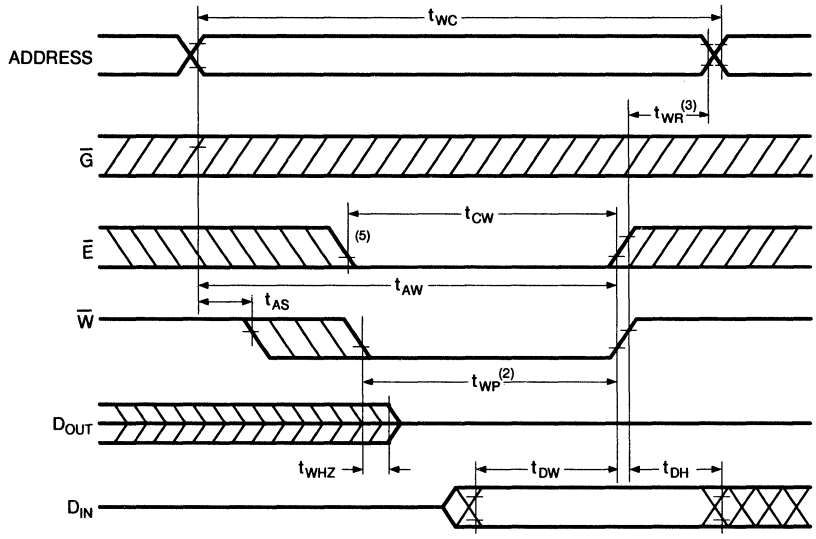
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

Jedec Parameter Name	Parameter Name	Parameter	MS62256C-70			MS62256C-10			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AVAX}	t_{WC}	Write Cycle Time	70		-	100		-	ns
t_{ELWH}	t_{CW}	Chip Enable to End of Write	65		-	90		-	ns
t_{AVWL}	t_{AS}	Address Set up Time	0		-	0		-	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	65		-	90		-	ns
t_{WLWH}	t_{WP}	Write Pulse Width	55		-	75		-	ns
t_{WHAX}	t_{WR}	Write Recovery Time	5		-	5		-	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	0		30	0		35	ns
t_{DVWH}	t_{DW}	Data Valid to End of Write	35		-	40		-	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0		-	0		-	ns
t_{GHZQ}	t_{OHZ}	Output Disable to Output in High Z	-		30	-		40	ns
t_{WHQX}	t_{OW}	Output Active from End of Write	5		-	5		-	ns

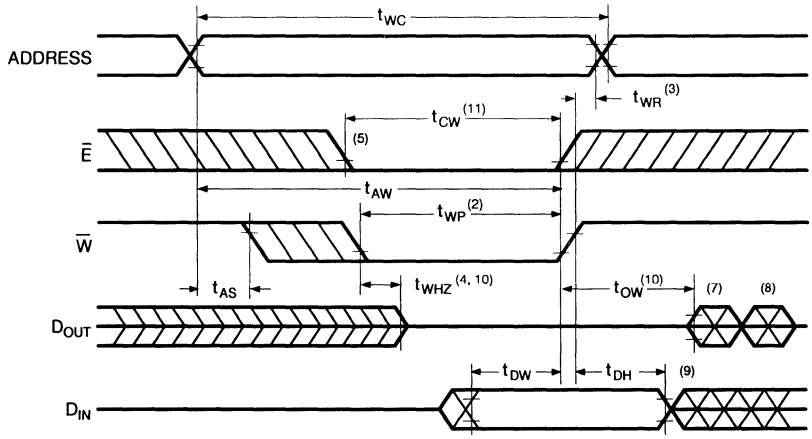
Switching Waveforms (Write Cycle)

WRITE CYCLE 1[1]



Switching Waveforms (Write Cycle)

Write Cycle 2[1,6]



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap $\overline{E}$ active and $\overline{W}$ low. Both signals must be active to initiate and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ low transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}$ is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.
11. t_{CW} is measured from $\overline{E}$ going low to the end of write.

Ordering Information

Speed (Ns)	Ordering Part Number	Package Reference No.	Temperature Range
70	MS62256CLL-70PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
70	MS62256CLL-70FC	28 Pin Plastic DIP	0°C to +70°C
70	MS62256CLL-70NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
100	MS62256CLL-10PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
100	MS62256CLL-10FC	28 Pin Plastic DIP	0°C to +70°C
100	MS62256CLL-10NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C

MS628128
1048576 (131,072 x 8)
CMOS STATIC RAM WITH
DATA RETENTION AND LOW POWER

ADVANCED INFORMATION

Features

- Available in 80/100/120 ns (Max.)
- Automatic power-down when chip disabled
- Lower power consumption:
  MS628128
  — 5.5mW (Max.) Power Down
  MS628128L
  — 1.1mW (Max.) Power Down
- TTL compatible interface levels
- Single 5V power supply
- Fully static operation
- Three state outputs
- Two chip enable ($\overline{E}_1$ and E_2) for simple memory expansion
- Data retention as low as 2V

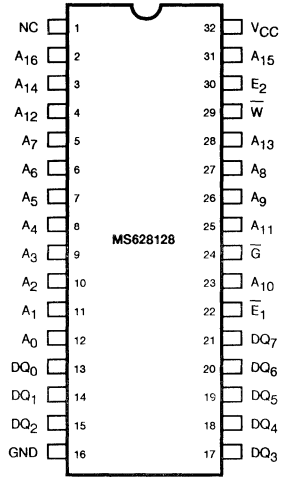
Description

The MS628128 is a high performance, low power CMOS static RAM organized as 131,072 words by 8 bits. The device supports easy memory expansion with both an active LOW chip enable ($\overline{E}_1$) and an active High chip enable (E_2), as well as an active LOW output enable ($\overline{G}$) and three state outputs. An automatic power-down feature is included which reduces the chip power by 80% in TTL standby mode, and by over 95% in full power-down mode.

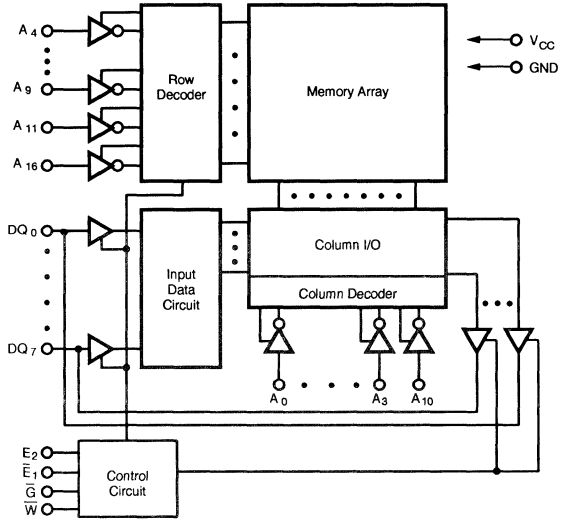
The device is manufactured in Mosel-Vitelic's high performance CMOS process and operates from a single 5V power supply. All inputs and outputs are TTL compatible. Data is retained to as low as V_{CC} = 2V.

The MS628128 is packaged in the JEDEC standard 32 pin 600 mil wide DIP and 525 mil wide SOP.

Pin Configurations



Functional Block Diagram



6

Pin Descriptions

A_0 - A_{16} Address Inputs
These 17 address inputs select one of the 131,072 x 8-bit words in the RAM.

$\overline{E}_1$ Chip Enable 1 Input
E_2 Chip Enable 2 Input
$\overline{E}_1$ is active LOW and E_2 is active HIGH. Both chip enables must be active to read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high-impedance state when deselected.

$\overline{G}$ Output Enable Input
The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{G}$ is inactive.

$\overline{W}$ Write Enable Input
The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{W}$ is HIGH and $\overline{G}$ is LOW, output data will be present at the DQ pins; when $\overline{W}$ is LOW, the data present on the DQ pins will be written into the selected memory location.

DQ_0 - DQ_7 Data Input/Output Ports
These 8 bidirectional ports are used to read data from or write data into the RAM.

V_{CC} Power Supply

GND Ground

Truth Table

Mode	$\overline{W}$	$\overline{E}_1$	E_2	$\overline{G}$	I/O Operation	V_{CC} Current
Not Selected	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
(Power Down)	X	X	L	X	High Z	I_{CCSB}, I_{CCSB1}
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

Absolute Maximum Ratings (1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–10 to +85	°C
T_{STG}	Storage Temperature	–45 to +125	°C

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Capacitance (1) T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$ = 0V	10	pF

1. This parameter is guaranteed and not tested.

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS628128 MIN.	MS628128 TYP.(1)	MS628128 MAX.	MS628128L MIN.	MS628128L TYP.(1)	MS628128L MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		-0.3	—	+0.8	-0.3	—	+0.8	V
V_{IH}	Guaranteed Input High Voltage(2)		2.2	—	V_{CC} +0.3	2.2	—	V_{CC} +0.3	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0V to V_{CC}	-1	—	1	-1	—	1	µA
I_{OL}	Output Leakage Current	V_{CC}= Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, or $\overline{G} = V_{IH}$, V_{IN} = 0V to V_{CC}	-2	—	2	-2	—	2	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 4mA	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -1mA	2.4	—	—	2.4	—	—	V
I_{CC}	Operating Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IL}$, $E_2 = V_{IH}$, I_{DQ} = 0mA, F = F_{max}(3)	—	—	80	—	—	80	mA
I_{CCSB}	Standby Power Supply Current	V_{CC} = Max, $\overline{E}_1 = V_{IH}$, or $E_2 = V_{IL}$, I_{DQ} = 0mA	—	—	3	—	—	3	mA
I_{CCSB1}	Power Down Power Supply Current	V_{CC} = Max, $\overline{E}_1 \geq V_{CC}$ –0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$ –0.2V or $V_{IN} \leq 0.2V$	—	—	1	—	—	0.2	mA

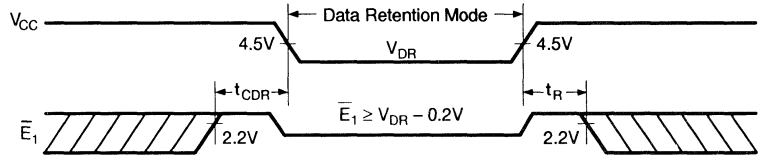
1. Typical characteristics are at V_{CC} = 5V, T_A = 25°C.
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3. $F_{MAX} = 1/t_{RC}$.

Data Retention Characteristics (1) (over the commercial operating range)

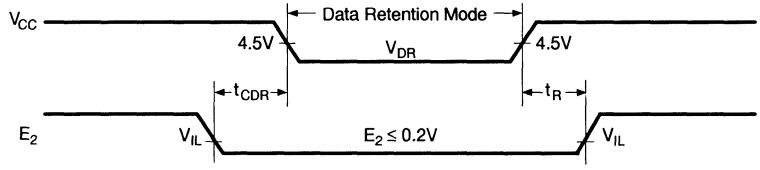
Symbol	Parameter	Test Conditions		Min.	Typ.(1)	Max	Units
V_{DR}	V_{CC} for Data Retention	$\overline{E}_1 \geq V_{CC}$–0.2V, $E_2 \leq 0.2V$, $V_{IN} \geq V_{CC}$–0.2V or $V_{IN} \leq 0.2V$		2.0	—	5.5	V
I_{CCDR}(1)	Data Retention Current	MS628128	Standard	—	—	0.5	mA
		MS628128L	L-Version	—	—	0.1	mA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform		0	—	—	ns
t_R	Operation Recovery Time			t_{RC}(2)	—	—	ns

1. $V_{CC} = V_{DR}$ = 3V
   $\overline{E}_1 \geq V_{DR}$ = 0.2V, $E_2 \geq V_{DR}$–0.2V or $E_2 \leq 0.2V$ (at E_1 controlled)
2. t_{RC} = Read Cycle Time

Low V_{CC} Data Retention Waveform (1) ($\overline{E}_1$ Controlled)



Low V_{CC} Data Retention Waveform (2) (E_2 Controlled)



AC Test Conditions

Input Pulse Levels	0.6V to 2.4V
Input Rise and Fall Times	5ns
Input and Output	Input: V_{IL} = 0.8V, V_{IH} = 2.2V
Timing Reference Level	Output: V_{OL} = 0.8V, V_{OH} = 2.0V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveform

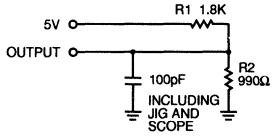


Figure 1a

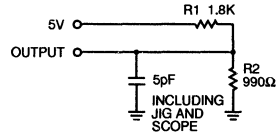
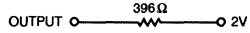


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

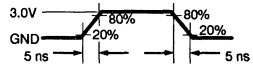


Figure 2

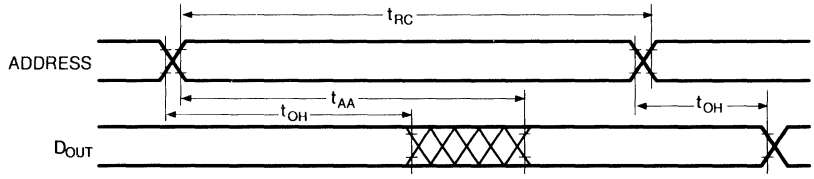
AC Electrical Characteristics (over the commercial operating range)

Read Cycle

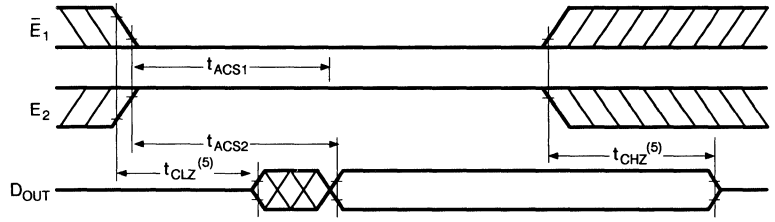
JEDEC Parameter Name	Parameter Name	Parameter		MS628128-80 MS628128L-80 MIN.	TYP.	MAX.	MS628128-10 MS628128L-10 MIN.	TYP.	MAX.	MS628128-12 MS628128L-12 MIN.	TYP.	MAX.	Unit
t_{AVAX}	t_{RC}	Read Cycle Time		80	—	—	100	—	—	120	—	—	ns
t_{AVQV}	t_{AA}	Address Access Time		—	—	80	—	—	100	—	—	120	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time	E_1	—	—	80	—	—	100	—	—	120	ns
t_{E2HQV}	t_{ACS2}	Chip Select Access Time	E_2	—	—	80	—	—	100	—	—	120	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		—	—	35	—	—	40	—	—	50	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z	E_1	10	—	—	10	—	—	10	—	—	ns
t_{E2HQX}	t_{CLZ2}	Chip Select to Output Low Z	E_2	10	—	—	10	—	—	10	—	—	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		5	—	—	5	—	—	5	—	—	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output in High Z	E_1	—	—	30	—	—	35	—	—	40	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output in High Z	E_2	—	—	30	—	—	35	—	—	40	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		—	—	30	—	—	30	—	—	40	ns
t_{AXQX}	t_{OH}	Output Hold from Address Change		10	—	—	10	—	—	10	—	—	ns

Switching Waveforms (Read Cycle)

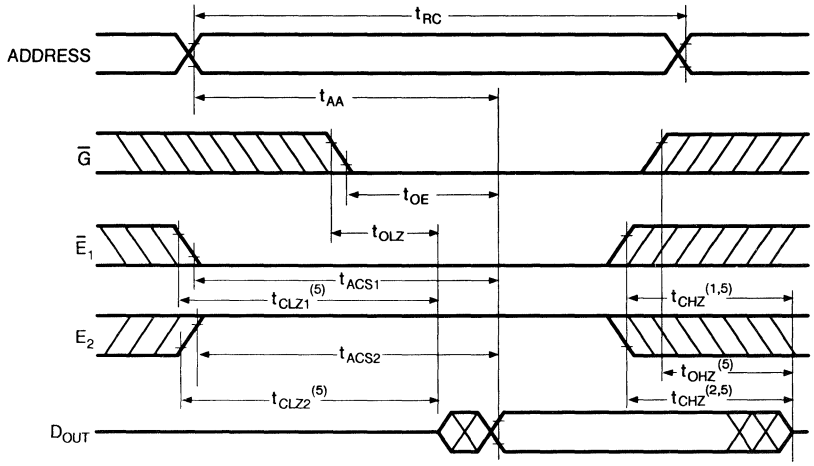
READ CYCLE 1[1, 2, 4]



READ CYCLE 2[1, 3, 4]



READ CYCLE 3[1, 4]



NOTES:
1. $\overline{W}$ is High for READ Cycle.
2. Device is continuously selected $\overline{E}_1 = V_{IL}$ and $E_2 = V_{IL}$.
3. Address valid prior to or coincident with $\overline{E}_1$ transition low and/or E_2 transition high.
4. $\overline{G} = V_{IL}$.
5. Transition is measured ± 500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed and not 100% tested.

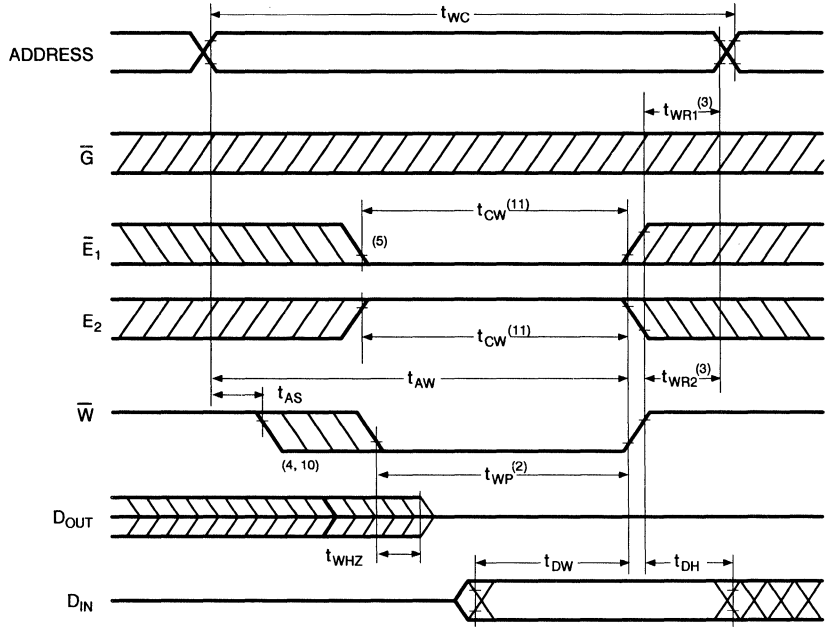
AC Electrical Characteristics (over the commercial operating range)

Write Cycle

JEDEC Parameter Name	Parameter Name	Parameter	MS628128-80 MS628128L-80			MS628128-10 MS628128L-10			MS628128-12 MS628128L-12			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
t_{AVAX}	t_{WC}	Write Cycle Time	80	—	—	100	—	—	120	—	—	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	60	—	—	80	—	—	85	—	—	ns
t_{AVWL}	t_{AS}	Address Set up Time	0	—	—	0	—	—	0	—	—	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	60	—	—	80	—	—	85	—	—	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	—	—	60	—	—	70	—	—	ns
t_{WHAX}	t_{WR1}	Write Recovery Time $\overline{E}_1, \overline{W}$	5	—	—	5	—	—	5	—	—	ns
t_{E2LAX}	t_{WR2}	Write Recovery Time E_2	5	—	—	5	—	—	5	—	—	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	—	—	30	—	—	35	—	—	40	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	30	—	—	40	—	—	45	—	—	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	—	—	0	—	—	0	—	—	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	—	—	30	—	—	35	—	—	40	ns
t_{WHQX}	t_{OW}	End of Write to Output Active	5	—	—	5	—	—	5	—	—	ns

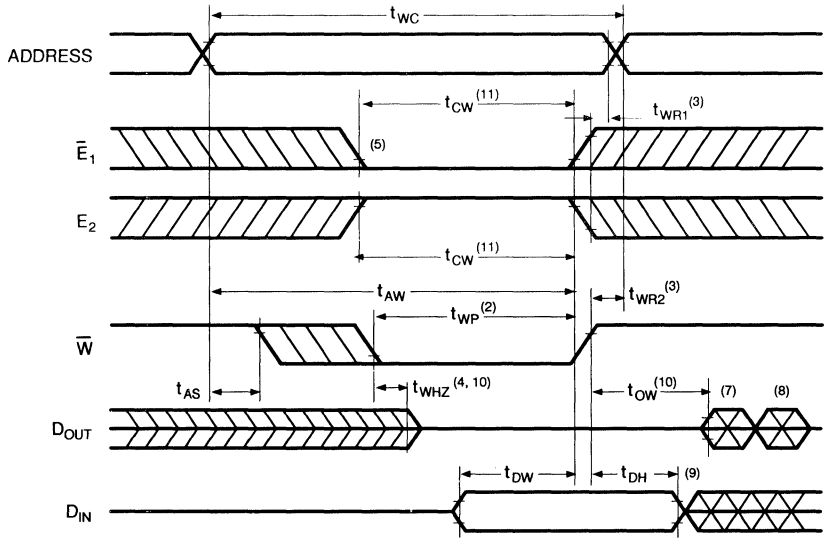
Switching Waveforms (Write Cycle)

WRITE CYCLE 1(1)



Switching Waveforms (Write Cycle)

WRITE CYCLE 2[1,6]



NOTES:
1. $\overline{W}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{E}_1$ and E_2 active and $\overline{W}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{E}_1$ or $\overline{W}$ going high or E_2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{E}_1$ low transition or the E_2 high transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, outputs remain in a high impedance state.
6. $\overline{G}$ is continuously low ($\overline{G} = V_{IL}$).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{E}_1$ is low and E_2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. Transition is measured ±500mV from steady state with C_L = 5pF as shown in Figure 1b. This parameter is guaranteed but not 100% tested.
11. t_{CW} is measured from the later of $\overline{E}_1$ going low or E_2 going high to the end of write.

6

Ordering Information

SPEED (ns)	ORDERING PART NUMBER	PACKAGE REFERENCE NO.	TEMPERATURE RANGE
80	MS628128-80PC	32 Pin 600 mil DIP	0°C to +70°C
80	MS628128-80FC	32 Pin 525 mil SOP	0°C to +70°C
80	MS628128L-80PC	32 Pin 600 mil DIP	0°C to +70°C
80	MS628128L-80FC	32 Pin 525 mil SOP	0°C to +70°C
100	MS628128-10PC	32 Pin 600 mil DIP	0°C to +70°C
100	MS628128-10FC	32 Pin 525 mil SOP	0°C to +70°C
100	MS628128L-10PC	32 Pin 600 mil DIP	0°C to +70°C
100	MS628128L-10FC	32 Pin 525 mil SOP	0°C to +70°C
120	MS628128-12PC	32 Pin 600 mil DIP	0°C to +70°C
120	MS628128-12FC	32 Pin 525 mil SOP	0°C to +70°C
120	MS628128L-12PC	32 Pin 600 mil DIP	0°C to +70°C
120	MS628128L-12FC	32 Pin 525 mil SOP	0°C to +70°C

MOSEL-VITELIC ***MS7200/7201A/7202A***
256 x 9, 512 x 9, 1K x 9
CMOS FIFO

Features

- First-In/First-Out static RAM based dual port memory
- Three densities in a x9 configuration
- Low power versions
- Includes empty, full, and half full status flags
- Direct replacement for industry standard Mostek and IDT
- Ultra high-speed 30 MHz FIFOs available with 33 ns cycle times.
- Fully expandable in both depth and width
- Simultaneous and asynchronous read and write
- Auto retransmit capability
- TTL compatible interface, single 5V ± 10% power supply
- Available in 28 pin 300 mil and 600 mil plastic DIP, 32 Pin PLCC and 330 mil SOG

Descriptions

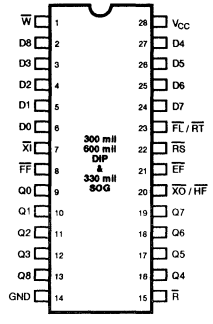
The MS7200/7201A/7202A are dual-port static RAM based CMOS First-In/First-Out (FIFO) memories organized in nine-bit wide words. The devices are configured so that data is read out in the same sequential order that it was written in. Additional expansion logic is provided to allow for unlimited expansion of both word size and depth.

The dual-port RAM array is internally sequenced by independent Read and Write pointers with no external addressing needed. Read and write operations are fully asynchronous and may occur simultaneously, even with the device operating at full speed. Status flags are provided for full, empty, and half-full conditions to eliminate data underflow and overflow. The x9 architecture provides an additional bit which may be used as a parity or control bit. In addition, the devices offer a retransmit capability which resets the Read pointer and allows for retransmission from the beginning of the data.

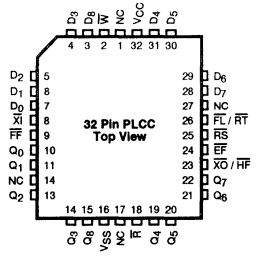
The MS7200/7201A/7202A are available in a range of frequencies from 10 to 30 MHz (33 - 100 ns cycle times). A low power version with a 500µA power down supply current is available. They are manufactured on Mosel-Vitelic's high performance 1.2µ CMOS process and operate from a single 5V power supply.

Pin Configurations

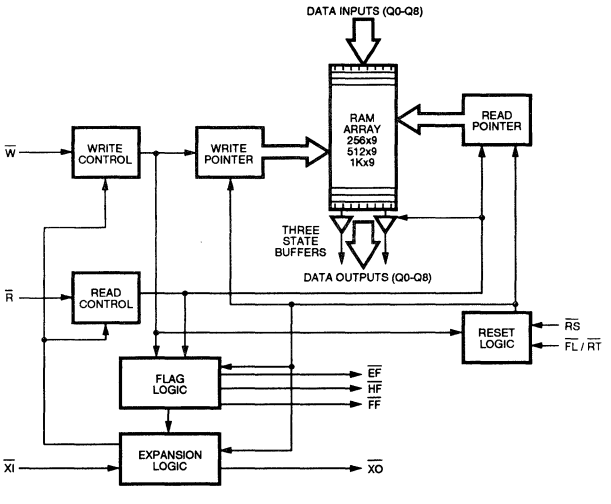
28-PIN PDIP



32-PIN PLCC



Block Diagram



7

Signal Descriptions

INPUTS:

Data In (D_0 - D_8)

These data inputs accept 9-bit data words for sequential storage in the FIFO during write operations.

CONTROLS:

Reset ($\overline{RS}$)

The reset input is active LOW. When asserted, the device is asynchronously reset, and both the read and write internal pointers are set to the first location in the FIFO. A Reset is required after power-up before a write operation can occur. Both Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be HIGH during Reset.

Read Enable ($\overline{R}$)

The read enable input is active LOW. As long as the Empty Flag ($\overline{EF}$) is not set, the read cycle is started on the falling edge of this signal. The data is accessed on a First-In/First-Out basis, independent of any write activity, and is presented on the Data Output pins (Q0 - Q8). When $\overline{R}$ goes HIGH the Data Output pins return to the high impedance state, and the read pointer is incremented. When the FIFO is empty or all of the data has been read, the Empty Flag will be set and further read operations are inhibited until a valid write operation has been performed.

Write Enable ($\overline{W}$)

The write enable input is active LOW. As long as the Full Flag ($\overline{FF}$) is not set, the write cycle is started on the falling edge of this signal. The data present on the Data Input pins (D0 - D8) is stored sequentially, independent of any read activity. When $\overline{W}$ goes HIGH the write cycle is terminated and the write pointer is incremented. When the maximum capacity of the FIFO has been reached the Full Flag will be set, and further write operations are inhibited until a valid read operation has been performed.

Expansion In ($\overline{XI}$)

This input pin serves two purposes. When grounded, it indicates that the device is being operated in the single device mode. In Depth Expansion mode, this pin is connected to the Expansion Out Output ($\overline{XO}$) of the previous device.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this pin acts as the retransmit input. A LOW pulse on this will reset the read pointer to the first memory location of the FIFO. The write pointer is unaffected. Both the read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must remain HIGH during the retransmit cycle.

In Depth Expansion mode this pin acts as a first load indicator. It must be grounded on the first device in the chain to indicate which device is the first to receive data.

OUTPUTS:

Data Output (Q_0 - Q_8)

A 9 bit data word from the FIFO is output on these pins during read operations. They are in the high impedance state whenever $\overline{R}$ is HIGH.

Empty Flag ($\overline{EF}$)

This output is active LOW. When all of the data has been read from the FIFO (defined as when the Read pointer is one location behind the Write pointer) this flag will be set. The Data Output pins will be forced into the high impedance state, and all further read operations will be inhibited until a valid write operation has been performed (which will reset this flag).

Full Flag ($\overline{FF}$)

This output is active LOW. To prevent data overflow, when the maximum capacity of the FIFO has been reached (defined as when the Write pointer is one location behind the Read pointer) this flag will be set. All further write operations will be inhibited until a valid read operation has been performed (which will reset this flag).

Expansion Out/Half Full Flag ($\overline{XO}/\overline{HF}$)

This dual-purpose output is active LOW. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this flag will be set at the falling edge of the next write operation after the FIFO has reached one-half of its maximum capacity. This flag will remain set as long as the difference between the read pointer and the write pointer is greater than one-half of the maximum capacity of the FIFO.

In Depth Expansion mode, this output is connected to the Expansion In Input of the next device in the chain. The Expansion Out pin provides a pulse to the next device in the chain when the last memory location has been reached.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Unit
V_{TERM}	Terminal Voltage with Repect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	Vcc
Commercial	0°C to + 70°C	5V ± 10%

Capacitance[1] T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4	pF
C_Q	Output Capacitance	V_{DQ} = 0V	6	pF

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS7200/7201A 7202A (-25, -35) Min.	Typ.	Max.	MS7200/7201A 7202A (-50, -80) Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		-	-	0.8	-	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	-	2.0	-	-	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0Vto V_{CC}	-1		1	-1		1	µA
I_{OL}	Output Leakage Current	V_{CC}= Max, R= V_{IH}, V_{IN} = 0V toV_{CC}	-10		10	-10		10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -2mA	2.4	-	-	2.4	-	-	V
I_{CC1}	Operating Power Supply Current	V_{CC} = Max, $I_{I/O}$ = 0mA, F = F_{max}	-	-	125	-	50	80	mA
I_{CC2}	Average Standby Current	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ = V_{IH}, $I_{I/O}$ = 0mA	-	-	15	-	5	8	mA
$I_{CCSB(S)}$	Power Down Power Supply Current (Standard Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ > V_{CC}-0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	5	-	-	5	mA
$I_{CCSB(L)}$	Power Down Power Supply Current (Low Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$> V_{CC}-0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	500	-	-	500	µA

Truth Tables

Single Device Configuration/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if flag is high.

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Unchanged	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 15.
$\overline{RS}$ = Reset Input. $\overline{FL}$/$\overline{RT}$ = First Load/Retransmit. $\overline{EF}$ = Empty Flag Output. $\overline{FF}$ Full Flag Output. $\overline{XI}$ = Expansion Input.

AC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	MS7200-25 MS7201A-25 MS7202A-25 Min.	Max.	MS7200-35 MS7201A-35 MS7202A-35 Min.	Max.	MS7200-50 MS7201A-50 MS7202A-50 Min.	Max.	MS7200-80 MS7201A-80 MS7202A-80 Min.	Max.	Units
f_S	Shift Frequency	–	30	–	22.2	–	15	–	10	MHz
Read Cycle										
t_{RC}	Read Cycle Time	33	–	45	–	65	–	100	–	ns
t_A	Access Time	–	25	–	35	–	50	–	80	ns
t_{RPW}	Read Pulse Width	25	–	35	–	50	–	80	–	ns
t_{RR}	Read Recovery Time	8	–	10	–	15	–	20	–	ns
t_{RLZ}[2]	Read Pulse Low to Data Bus at Low Z	5	–	5	–	10	–	10	–	ns
t_{RHZ}[2,3]	Read Pulse High to Data Bus at High Z	–	18	–	20	–	30	–	30	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	ns
Write Cycle										
t_{WC}	Write Cycle Time	33	–	45	–	65	–	100	–	ns
t_{WPW}[1]	Write Pulse Width	25	–	35	–	50	–	80	–	ns
t_{WR}	Write Recovery Time	8	–	10	–	15	–	20	–	ns
t_{DS}	Data Setup Time	15	–	18	–	30	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	5	–	10	–	ns
t_{WLZ}[2,3]	Write Pulse High to Data Bus at Low Z	5	–	10	–	15	–	20	–	ns
Flag Timing										
t_{REF}	Read Low to Empty Flag Low	–	25	–	30	–	45	–	60	ns
t_{RHF}	Read High to Half Full Flag High	–	33	–	45	–	65	–	100	ns
t_{RFF}	Read High to Full Flag High	–	25	–	30	–	45	–	60	ns
t_{WEF}	Write High to Empty Flag High	–	25	–	30	–	45	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	25	–	30	–	45	–	60	ns
t_{WHF}	Write Low to Half Full Flag Low	–	33	–	45	–	65	–	100	ns
t_{RPE}	Read Pulse Width After EF High	25	–	35	–	50	–	80	–	ns
t_{WPF}	Write Pulse Width After FF High	25	–	35	–	50	–	80	–	ns
Reset Timing										
t_{RSC}	Reset Cycle Time	33	–	45	–	65	–	100	–	ns
t_{RS}[1]	Reset Pulse Width	25	–	35	–	50	–	80	–	ns
t_{RSS}	Reset Set Up Time	25	–	35	–	50	–	80	–	ns
t_{RSR}	Reset Recovery Time	8	–	10	–	15	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	33	–	45	–	65	–	100	ns
t_{HFH}	Reset to Half Full Flag High	–	33	–	45	–	65	–	100	ns
t_{FFH}	Reset to Full Flag High	–	33	–	45	–	65	–	100	ns
Retransmit Timing										
t_{RTC}	Retransmit Cycle Time	33	–	45	–	65	–	100	–	ns
t_{RT}[1]	Retransmit Pulse Width	25	–	35	–	50	–	80	–	ns
t_{RTS}	Retransmit Set up Time	25	–	35	–	50	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	8	–	10	–	15	–	20	–	ns
Expansion Timing										
t_{XOL}	Read/Write to $\overline{XO}$ Low	–	25	–	35	–	50	–	80	ns
t_{XOH}	Read/Write to $\overline{XO}$ High	–	25	–	35	–	50	–	80	ns
t_{XI}	$\overline{XI}$ Pulse Width	25	–	35	–	50	–	80	–	ns
t_{XIS}	$\overline{XI}$ Set up Time	15	–	15	–	15	–	15	–	ns
t_{XIR}	$\overline{XI}$ Recovery Time	8	–	10	–	10	–	10	–	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.
3. Only applies to read data flow-through mode.

AC Test Conditions

Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5 ns
Timing Reference Level	1.5V

Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

AC Test Loads and Waveforms

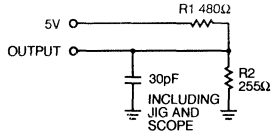


Figure 1a

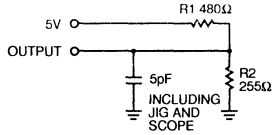
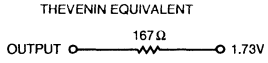


Figure 1b

Equivalent to:



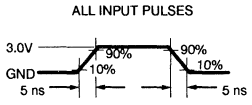
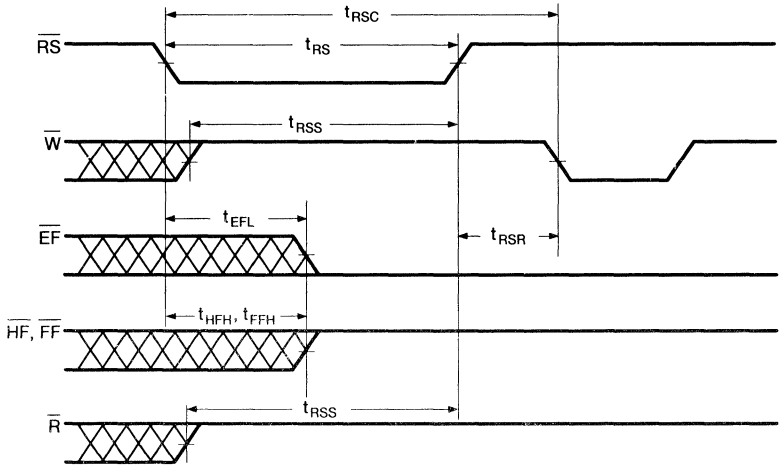


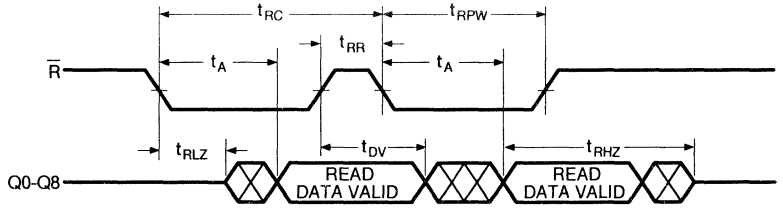
Figure 2

Timing Waveforms

RESET

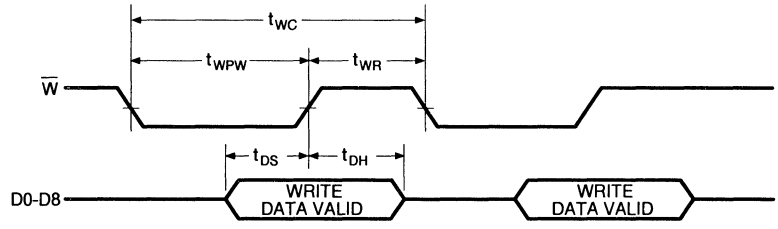


ASYNCHRONOUS READ OPERATION

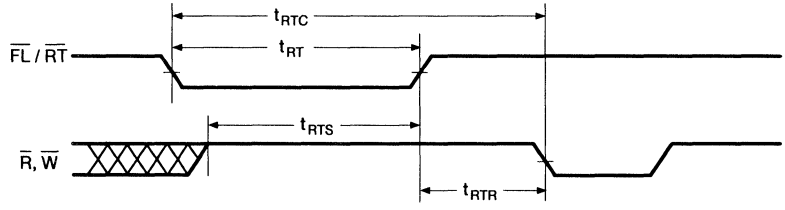


7

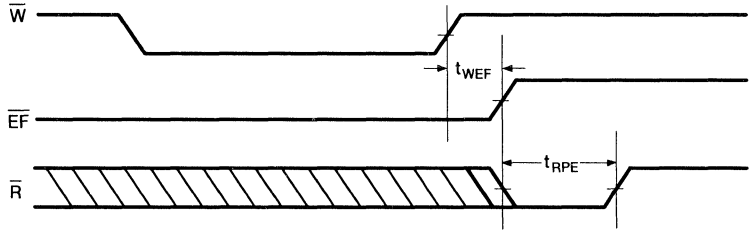
ASYNCHRONOUS WRITE OPERATION



RETRANSMIT

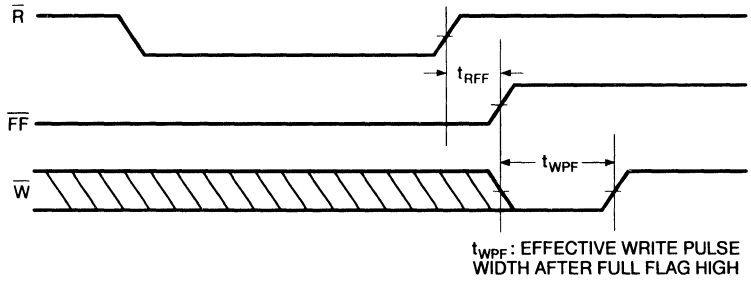


EMPTY FLAG TIMING

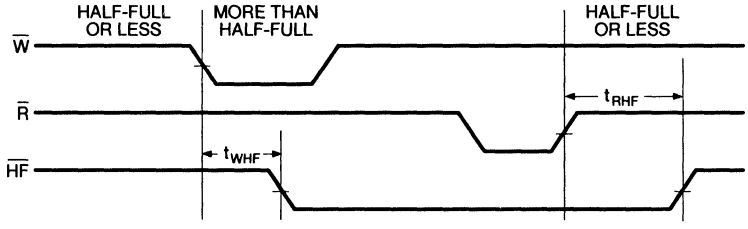


t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

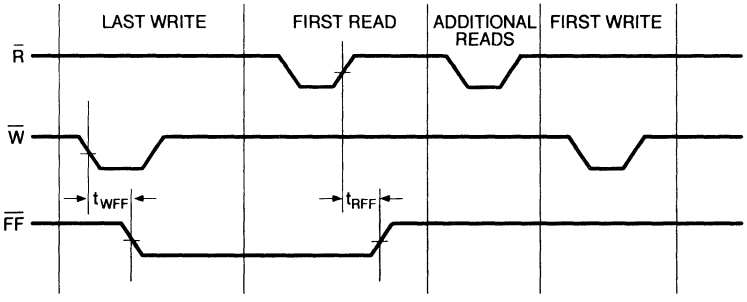
FULL FLAG TIMING



HALF-FULL FLAG TIMING



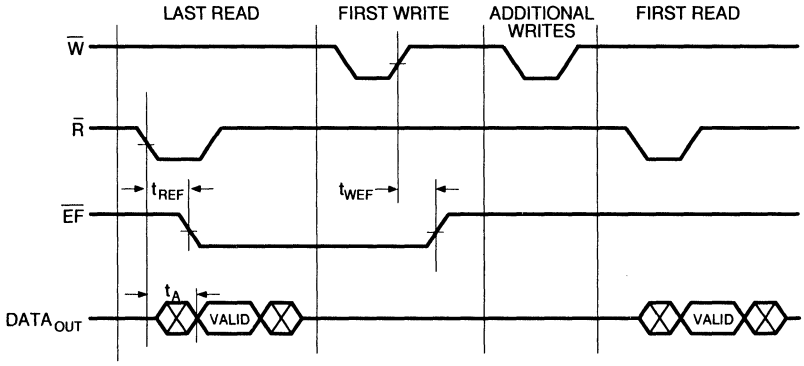
FULL FLAG FROM LAST WRITE TO FIRST READ



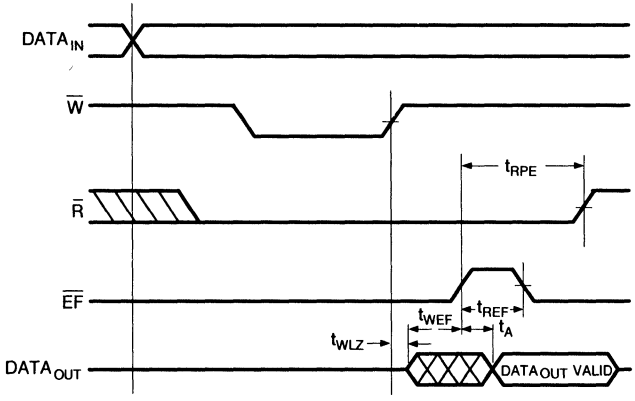
7

Timing Waveforms

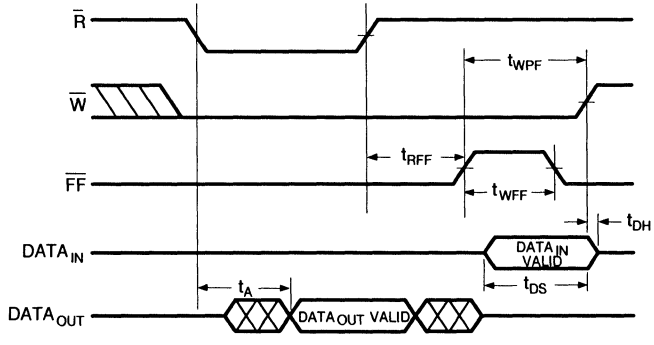
EMPTY FLAG FROM LAST READ TO FIRST WRITE



READ DATA FLOW-THROUGH MODE

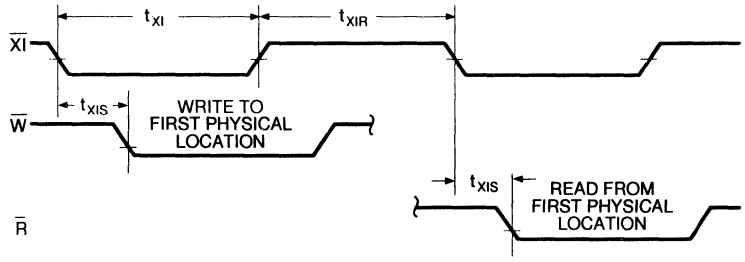


WRITE DATA FLOW-THROUGH MODE

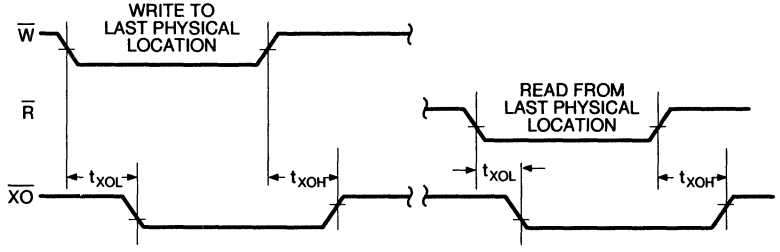


Timing Waveforms

EXPANSION IN



EXPANSION OUT



Operating Modes:

(Note: The7201A is used as example - these figures apply to all three devices, MS7200/7201A/ 7202A

Single Device Mode

When one MS7201A is used standalone in Single Device Mode, the Expansion In ($\overline{XI}$) control input pin must be grounded. See Figure 3.

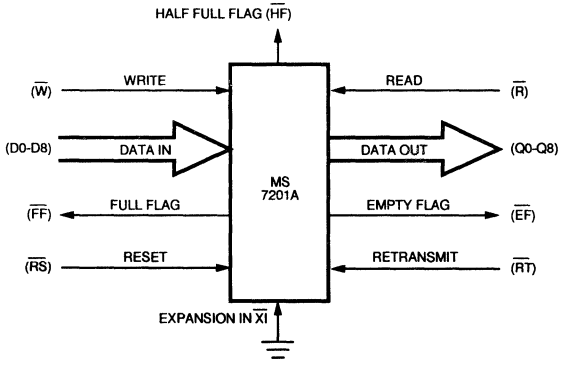


Figure 3. Single Device Mode

Width Expansion Mode

Word width may be expanded by connecting the corresponding control input signals of multiple devices together. The EMPTY, HALF FULL and FULL FLAGS ($\overline{EE}$, $\overline{HF}$ and $\overline{FF}$) can be detected by any particular device. Figure 4 shows an 18 bit wide configuration using two devices. They may be configured to any word width in this manner.

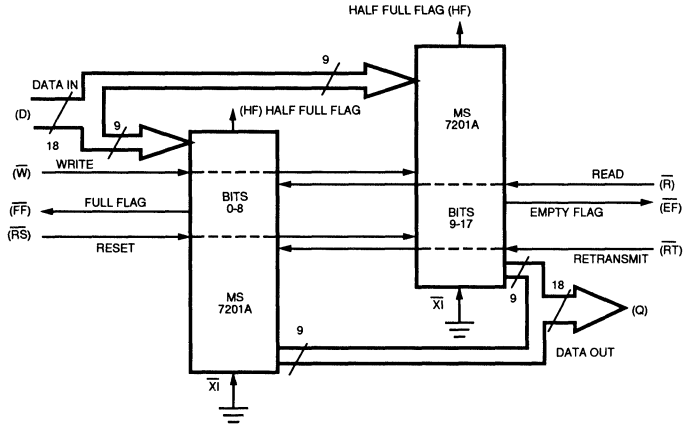


Figure 4. Width Expansion Mode

NOTES:
Flag detection is accomplished by monitoring the $\overline{EF}$, $\overline{HF}$ and $\overline{EF}$ pins on the device used in the Width Expansion Mode. Do not connect output control signals together.

Depth Expansion (Daisy Chain) Mode

Word depths may be expanded in multiples of 512 words by Daisy Chaining the devices together as follows:

1. The FIRST LOAD ($\overline{FL}$) control signal of the first device must be grounded. This FIFO represents word 1-512.
2. All other devices in the Daisy Chain must have the FIRST LOAD ($\overline{FL}$) control signal tied to V_{CC} in the inactive-high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be connected to the EXPANSION IN ($\overline{XI}$) pin of the next device as shown in Figure 5.
4. External logic is required to generate a common FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$) signal by ORing all of the $\overline{FF}$s together and ORing all of the $\overline{EF}$s together.
5. The RETRANSMIT ($\overline{RT}$) fuction and HALF FULL FLAG ($\overline{HF}$) are not available in Daisy Chain Mode.

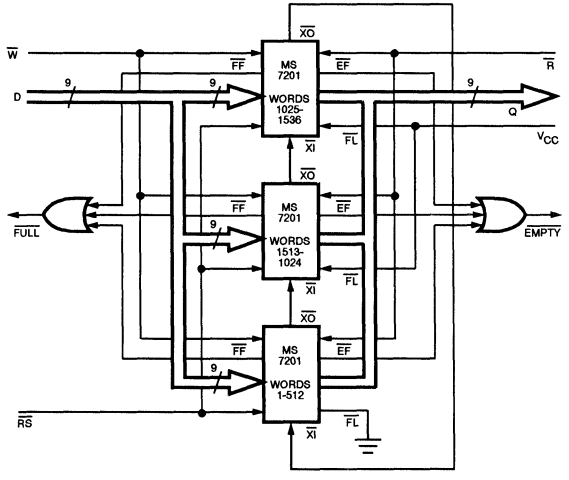


Figure 5. Diagram of a 1536 x 9 FIFO in Depth Expansion Mode

Bidirectional Mode

Data buffering between two systems can be achieved by pairing two FIFO arrays as shown in Figure 6. This allows each system to READ and WRITE shared data. The FULL FLAG ($\overline{FF}$) must be monitored on the FIFO where WRITE ENABLE ($\overline{W}$) is used and the EMPTY FLAG ($\overline{EF}$) must be monitored on the FIFO where READ ENABLE ($\overline{R}$) is used. Both Width Expansion and Depth Expansion Modes may be used in combination with Bidirectional Mode.

Compound Expansion Mode:

Both Width Expansion Mode and Depth Expansion (Daisy Chain) Mode can be used together to configure a large FIFO array (See Figure 4 and 5).

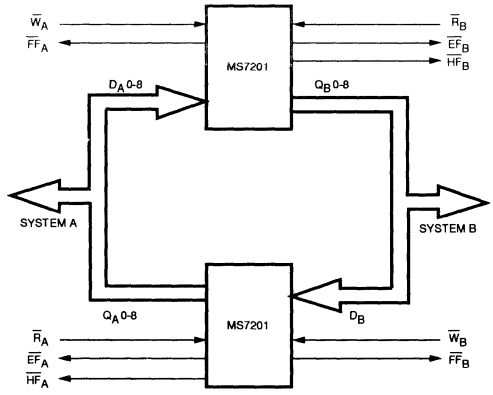


Figure 6. BiDirectional FIFO Mode

Ordering Information

Speed (Ns)	Ordering Part Number[1]			Package Reference No.	Temperature Range
25		MS7201A-25PC	MS7202A-25PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
25	MS7200-25NC	MS7201A-25NC	MS7202A-25NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
25	MS7200-25JC	MS7201A-25JC	MS7202A-25JC	32 Pin Plastic PLCC	0°C to +70°C
25	MS7200-25FC	MS7201A-25FC	MS7202A-25FC	28 Pin Small Outline - 330 mil	0°C to +70°C
35		MS7201A-35PC	MS7202A-35PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
35	MS7200-35NC	MS7201A-35NC	MS7202A-35NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
35	MS7200-35JC	MS7201A-35JC	MS7202A-35JC	32 Pin Plastic PLCC	0°C to +70°C
35	MS7200-35FC	MS7201A-35FC	MS7202A-35FC	28 Pin Small Outline - 330 mil	0°C to +70°C
50		MS7201A-50PC	MS7202A-50PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
50	MS7200-50NC	MS7201A-50NC	MS7202A-50NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
50	MS7200-50JC	MS7201A-50JC	MS7202A-50JC	32 Pin Plastic PLCC	0°C to +70°C
50	MS7200-50FC	MS7201A-50FC	MS7202A-50FC	28 Pin Small Outline - 330 mil	0°C to +70°C
80		MS7201A-80PC	MS7202A-80PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
80	MS7200-80NC	MS7201A-80NC	MS7202A-80NC	28 Pin Plastic DIP - 300 mil	0°C to +70°C
80	MS7200-80JC	MS7201A-80JC	MS7202A-80JC	32 Pin Plastic PLCC	0°C to +70°C
80	MS7200-80FC	MS7201A-80FC	MS7202A-80FC	28 Pin Small Outline - 330 mil	0°C to +70°C

[1] For the low power version, add L after part number and before dash information. For example, MS7200L-25PC.

MOSEL-VITELIC **MS7203/7204**

2K x 9, 4K x 9 CMOS FIFO

Features

- First-In/First-Out static RAM based dual port memory
- Two densities (2K and 4K) in a x9 configuration
- Low power versions
- Includes empty, full, and half full status flags
- Direct replacement for industry standard IDT plus 300 mil DIP and 330 mil SOG
- Ultra high-speed 33 MHz FIFOs available with 30 ns cycle times.
- Fully expandable in both depth and width
- Simultaneous and asynchronous read and write
- Auto retransmit capability
- TTL compatible interface, single 5V ± 10% power supply
- Available in 28 pin 300 mil and 600 mil plastic DIP, 28 Pin 330 mil SOG and 32 Pin PLCC

Description

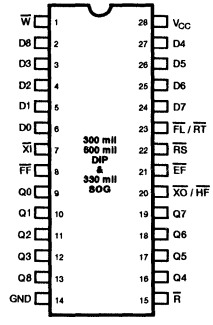
The MS7203/7204 are dual-port static RAM based CMOS First-In/First-Out (FIFO) memories organized in nine-bit wide words. The devices are configured so that data is read out in the same sequential order that it was written in. Additional expansion logic is provided to allow for unlimited expansion of both word size and depth.

The dual-port RAM array is internally sequenced by independent Read and Write pointers with no external addressing needed. Read and write operations are fully asynchronous and may occur simultaneously, even with the device operating at full speed. Status flags are provided for full, empty, and half-full conditions to eliminate data underflow and overflow. The x9 architecture provides an additional bit which may be used as a parity or control bit. In addition, the devices offer a retransmit capability which resets the Read pointer and allows for retransmission from the beginning of the data.

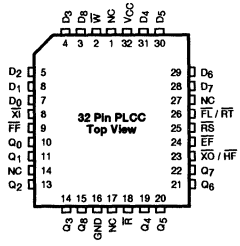
The MS7203/7204 are available in a range of frequencies from 10 to 33 MHz (30 - 100 ns cycle times). A low power version with a 500µA power down supply current is available. They are manufactured on Mosel-Vitelic's high performance CMOS process and operate from a single 5V power supply.

Pin Configuration

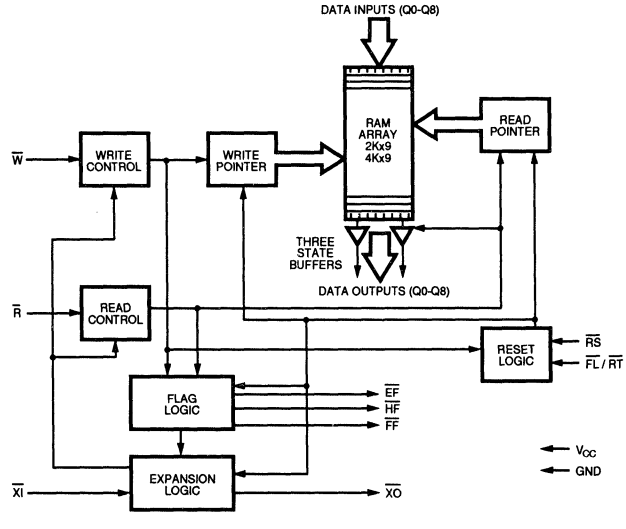
28-PIN PDIP & SOG



32-PIN PLCC



Block Diagram



Signal Descriptions

Inputs:

Data In (D_0 - D_8)

These data inputs accept 9-bit data words for sequential storage in the FIFO during write operations.

Controls:

Reset ($\overline{RS}$)

The reset input is active LOW. When asserted, the device is asynchronously reset, and both the read and write internal pointers are set to the first location in the FIFO. A Reset is required after power-up before a write operation can occur. Both Read Enable ($\overline{R}$) and Write Enable ($\overline{W}$) must be HIGH during Reset.

Read Enable ($\overline{R}$)

The read enable input is active LOW. As long as the Empty Flag ($\overline{EF}$) is not set, the read cycle is started on the falling edge of this signal. The data is accessed on a First-In/First-Out basis, independent of any write activity, and is presented on the Data Output pins (Q0 - Q8). When R goes HIGH the Data Output pins return to the high impedance state, and the read pointer is incremented. When the FIFO is empty or all of the data has been read, the Empty Flag will be set and further read operations are inhibited until a valid write operation has been performed.

Write Enable ($\overline{W}$)

The write enable input is active LOW. As long as the Full Flag ($\overline{FF}$) is not set, the write cycle is started on the falling edge of this signal. The data present on the Data Input pins (D0 - D8) is stored sequentially, independent of any read activity. When W goes HIGH the write cycle is terminated and the write pointer is incremented. When the maximum capacity of the FIFO has been reached the Full Flag will be set, and further write operations are inhibited until a valid read operation has been performed.

Expansion In ($\overline{XI}$)

This input pin serves two purposes. When grounded, it indicates that the device is being operated in the single device mode. In Depth Expansion mode, this pin is connected to the Expansion Out Output ($\overline{XO}$) of the previous device.

First Load/Retransmit ($\overline{FL}/\overline{RT}$)

This is a dual-purpose input. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this pin acts as the retransmit input. A LOW pulse on this will reset the read pointer to the first memory location of the FIFO. The write pointer is unaffected. Both the read enable ($\overline{R}$) and write enable ($\overline{W}$) inputs must remain HIGH during the retransmit cycle.

In Depth Expansion mode this pin acts as a first load indicator. It must be grounded on the first device in the chain to indicate which device is the first to receive data.

Outputs:

Data Output (Q_0 - Q_8)

A 9 bit data word from the FIFO is output on these pins during read operations. They are in the high impedance state whenever $\overline{R}$ is HIGH.

Empty Flag ($\overline{EF}$)

This output is active LOW. When all of the data has been read from the FIFO (defined as when the Read pointer is one location behind the Write pointer) this flag will be set. The Data Output pins will be forced into the high impedance state, and all further read operations will be inhibited until a valid write operation has been performed (which will reset this flag).

Full Flag ($\overline{FF}$)

This output is active LOW. To prevent data overflow, when the maximum capacity of the FIFO has been reached (defined as when the Write pointer is one location behind the Read pointer) this flag will be set. All further write operations will be inhibited until a valid read operation has been performed (which will reset this flag).

Expansion Out/Half Full Flag ($\overline{XO}/\overline{HF}$)

This dual-purpose output is active LOW. In single device mode (when Expansion In ($\overline{XI}$) is grounded) this flag will be set at the falling edge of the next write operation after the FIFO has reached one-half of its maximum capacity. This flag will remain set as long as the difference between the read pointer and the write pointer is greater than one-half of the maximum capacity of the FIFO.

In Depth Expansion mode, this output is connected to the Expansion In Input of the next device in the chain. The Expansion Out pin provides a pulse to the next device in the chain when the last memory location has been reached.

Absolute Maximum Ratings[1]

Symbol	Parameter	Condition	Unit
V_{TERM}	Terminal Voltage with Repect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	°C
T_{STG}	Storage Temperature	-60 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	Vcc
Commercial	0°C to + 70°C	5V ± 10%

Capacitance[1] T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Condition	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4	pF
C_Q	Output Capacitance	V_{DQ} = 0V	6	pF

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS7203, MS7204 (-20, -25, -35, -50, -80) Min.	Typ.	Max.	Units
V_{IL}	Input Low Voltage		-	-	0.8	V
V_{IH}	Input High Voltage		2.0	-	-	V
I_{IL}	Input Leakage Current	V_{CC}= Max, V_{IN} = 0Vto V_{CC}	-1		1	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, $\overline{R}$= V_{IH}, V_{IN} = 0V toV_{CC}	-10		10	µA
V_{OL}	Output Low Voltage	V_{CC} = Min, I_{OL} = 8mA	-	-	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min, I_{OH} = -2mA	2.4	-	-	V
I_{CC1}	Operating Power Supply Current	V_{CC} = Max, $I_{I/O}$ = 0mA, F = F_{max}	-	-	125	mA
I_{CC2}	Average Standby Current	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/ $\overline{RT}$ = V_{IH}, $I_{I/O}$ = 0mA	-	-	15	mA
$I_{CCSB(S)}$	Power Down Power Supply Current (Standard Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$ / $\overline{RT}$ > V_{CC}-0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	8	mA
$I_{CCSB(L)}$	Power Down Power Supply Current (Low Power)	V_{CC} = Max, $\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}$/ $\overline{RT}$ > V_{CC}-0.2V, V_{IN} > V_{CC}-0.2V or V_{IN} < 0.2V	-	-	2	mA

Truth Tables

Single Device Configuation/Width Expansion Mode

Mode	Inputs			Internal Status		Outputs		
	RS	RT	XI	Read Pointer	Write Pointer	EF	FF	HF
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment[1]	Increment[1]	X	X	X

NOTE:
1. Pointer will increment if flag is high.

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	RS	FL	XI	Read Pointer	Write Pointer	EF	FF
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset all Other Devices	0	1	(1)	Location Zero	Unchanged	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 5.
$\overline{RS}$ = Reset Input. $\overline{FL}$/$\overline{RT}$ = First Load/Retransmit. $\overline{EF}$ = Empty Flag Output. $\overline{FF}$ = Full Flag Output. $\overline{XI}$ = Expansion Input.

AC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	MS7203-20 MS7204-20 Min.	Max.	MS7203-25 MS7204-25 Min.	Max.	MS7203-35 MS7204-35 Min.	Max.	MS7203-50 MS7204-50 Min.	Max.	MS7203-80 MS7204-80 Min.	Max.	Units
f_S	Shift Frequency	–	33	–	28	–	22.2	–	15.3	–	10	MHz
Read Cycle												
t_{RC}	Read Cycle Time	30	–	35	–	45	–	65	–	100	–	ns
t_A	Access Time	–	20	–	25	–	35	–	50	–	80	ns
t_{RPW}	Read Pulse Width	20	–	25	–	35	–	50	–	80	–	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	15	–	20	–	ns
t_{RLZ}[2]	Read Pulse Low to Data Bus at Low Z	5	–	5	–	5	–	10	–	10	–	ns
t_{RHZ}[2,3]	Read Pulse High to Data Bus at High Z	–	15	–	15	–	20	–	30	–	30	ns
t_{DV}	Data Valid from Read Pulse High	5	–	5	–	5	–	5	–	5	–	ns
Write Cycle												
t_{WC}	Write Cycle Time	30	–	35	–	45	–	65	–	100	–	ns
t_{WPW}[1]	Write Pulse Width	20	–	25	–	35	–	50	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	15	–	20	–	ns
t_{DS}	Data Setup Time	10	–	10	–	18	–	30	–	40	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	5	–	10	–	ns
t_{WLZ}[2,3]	Write Pulse High to Data Bus at Low Z	10	–	10	–	10	–	15	–	20	–	ns
Flag Timing												
t_{REF}	Read Low to Empty Flag Low	–	25	–	25	–	30	–	45	–	60	ns
t_{RHF}	Read High to Half Full Flag High	–	30	–	35	–	45	–	65	–	100	ns
t_{RFF}	Read High to Full Flag High	–	25	–	25	–	30	–	45	–	60	ns
t_{WEF}	Write High to Empty Flag High	–	25	–	25	–	30	–	45	–	60	ns
t_{WFF}	Write Low to Full Flag Low	–	25	–	25	–	30	–	45	–	60	ns
t_{WHF}	Write Low to Half Full Flag Low	–	30	–	35	–	45	–	65	–	100	ns
t_{RPE}	Read Pulse Width After EF High	20	–	25	–	35	–	50	–	80	–	ns
t_{WPF}	Write Pulse Width After FF High	20	–	25	–	35	–	50	–	80	–	ns
Reset Timing												
t_{RSC}	Reset Cycle Time	30	–	35	–	45	–	65	–	100	–	ns
t_{RS}[1]	Reset Pulse Width	20	–	25	–	35	–	50	–	80	–	ns
t_{RSS}	Reset Set Up Time	25	–	30	–	35	–	50	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	15	–	20	–	ns
t_{EFL}	Reset to Empty Flag Low	–	30	–	35	–	45	–	65	–	100	ns
t_{HFH}	Reset to Half Full Flag High	–	30	–	35	–	45	–	65	–	100	ns
t_{FFH}	Reset to Full Flag High	–	30	–	35	–	45	–	65	–	100	ns
Retransmit Timing												
t_{RTC}	Retransmit Cycle Time	30	–	35	–	45	–	65	–	100	–	ns
t_{RT}[1]	Retransmit Pulse Width	20	–	25	–	35	–	50	–	80	–	ns
t_{RTS}	Retransmit Set up Time	25	–	30	–	35	–	50	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	15	–	20	–	ns
Expansion Timing												
t_{XOL}	Read/Write to XO Low	–	20	–	25	–	35	–	50	–	80	ns
t_{XOH}	Read/Write to XO High	–	20	–	25	–	35	–	50	–	80	ns
t_{XI}	XI Pulse Width	20	–	25	–	35	–	50	–	80	–	ns
t_{XIS}	XI Set up Time	10	–	10	–	15	–	15	–	15	–	ns
t_{XIR}	XI Recovery Time	10	–	10	–	10	–	10	–	10	–	ns

NOTES:
1. Pulse widths less than minimum value are not allowed.
2. Values guaranteed by design, not currently tested.
3. Only applies to read data flow-through mode.

AC Test Conditions

Input Pulse Levels	0V~ 3.0V
Input Rise and Fall Times	5 ns
Timing Reference Level	1.5V

AC Test Loads and Waveforms

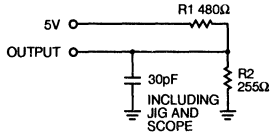


Figure 1a

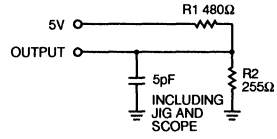
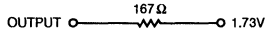


Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES

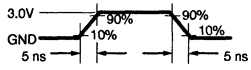


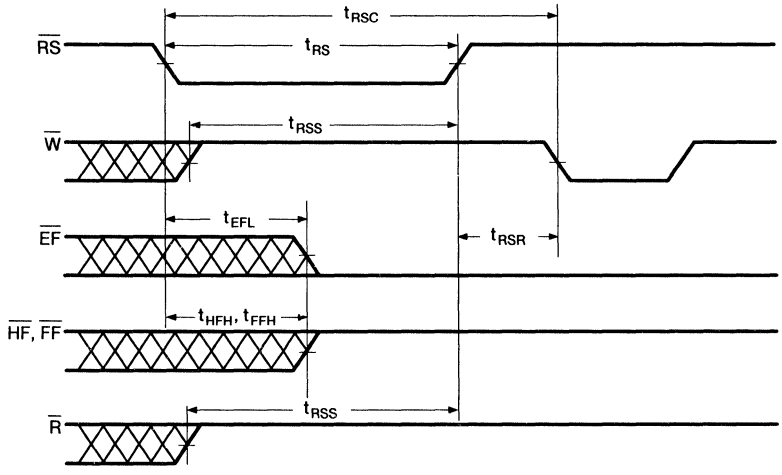
Figure 2

Key to Switching Waveforms

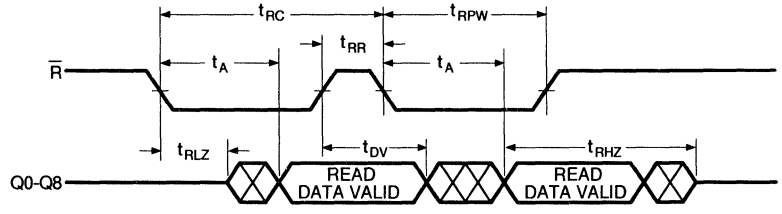
WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

Timing Waveforms

RESET

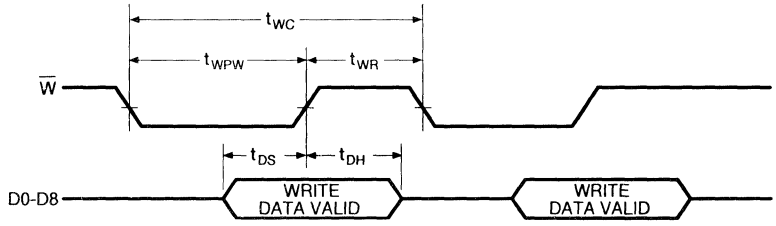


ASYNCHRONOUS READ OPERATION

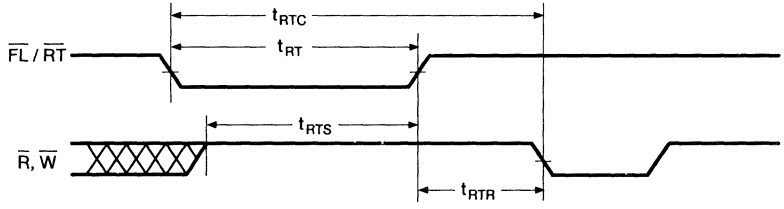


Timing Waveforms

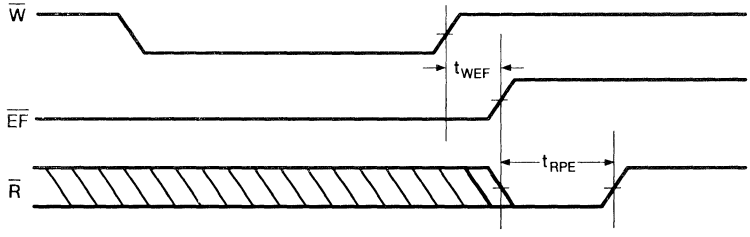
ASYNCHRONOUS WRITE OPERATION



RETRANSMIT



EMPTY FLAG TIMING

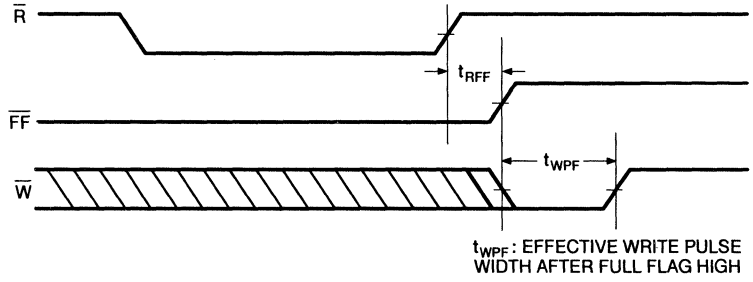


t_{RPE}: EFFECTIVE READ PULSE WIDTH AFTER EMPTY FLAG HIGH

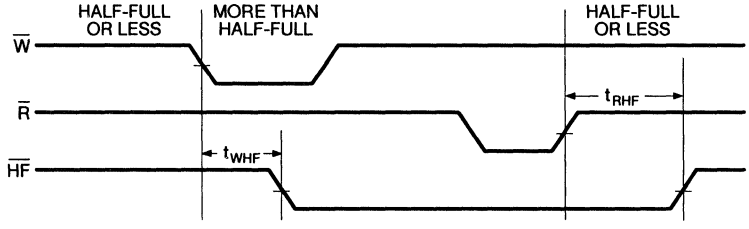
7

Timing Waveforms

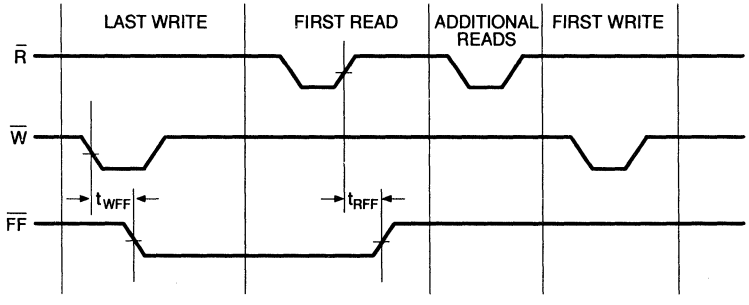
FULL FLAG TIMING



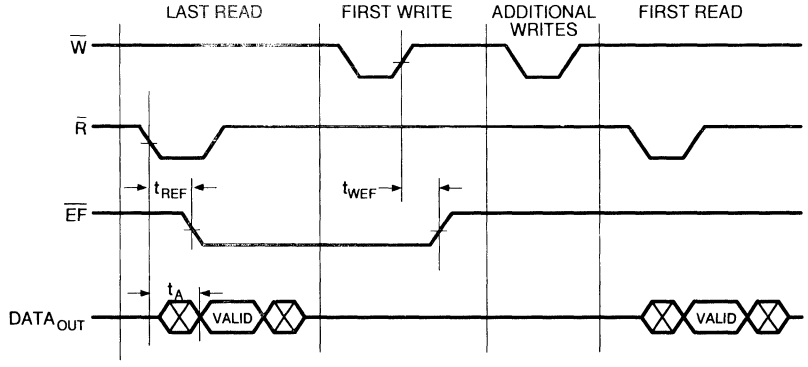
HALF-FULL FLAG TIMING



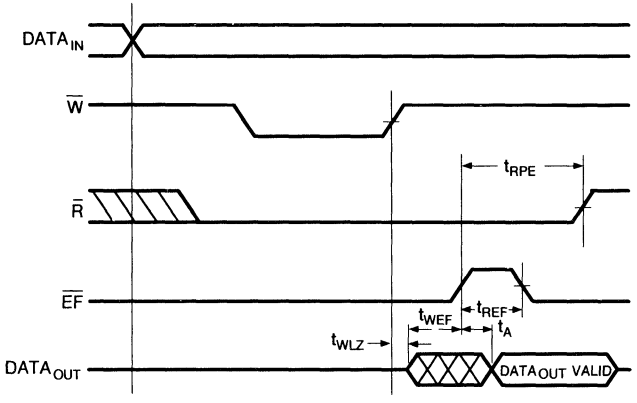
FULL FLAG FROM LAST WRITE TO FIRST READ



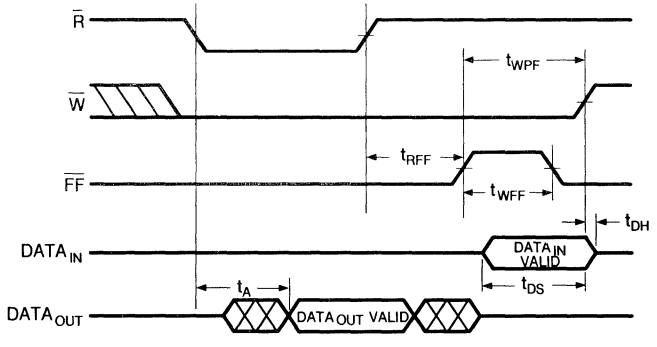
EMPTY FLAG FROM LAST READ TO FIRST WRITE



READ DATA FLOW-THROUGH MODE



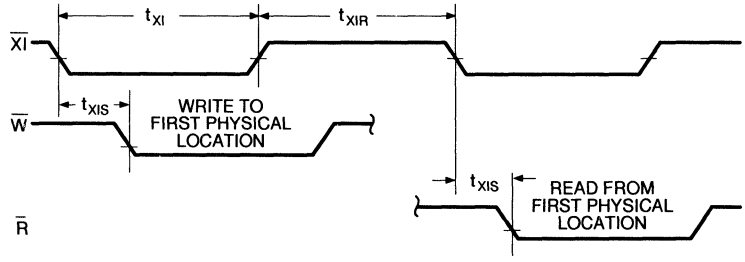
WRITE DATA FLOW-THROUGH MODE



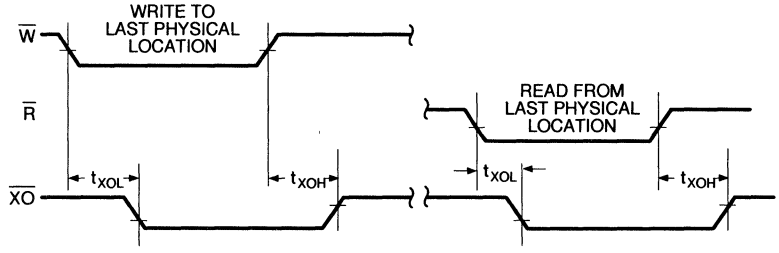
7

Timing Waveforms

EXPANSION IN



EXPANSION OUT



Operating Modes:

(Note: The7204 is used as example - these figures apply to both devices, MS7203/7204.

Single Device Mode

When one MS7204 is used standalone in Single Device Mode, the Expansion In ($\overline{XI}$) control input pin must be grounded. See Figure 3.

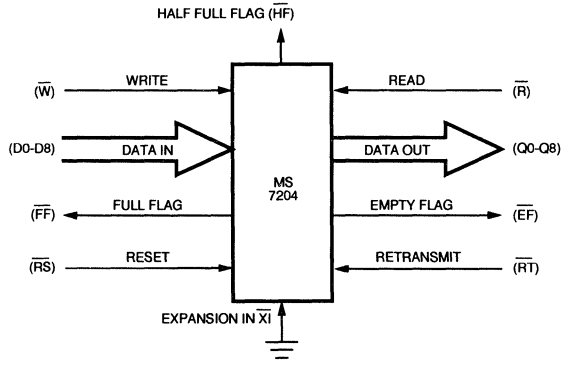


Figure 3. Single Device Mode

Width Expansion Mode

Word width may be expanded by connecting the corresponding control input signals of multiple devices together. The EMPTY, HALF FULL and FULL FLAGS (EE, HF and FF) can be detected by any particular device. Figure 4 shows an 18 bit wide configuration using two devices. They may be configured to any word width in this manner.

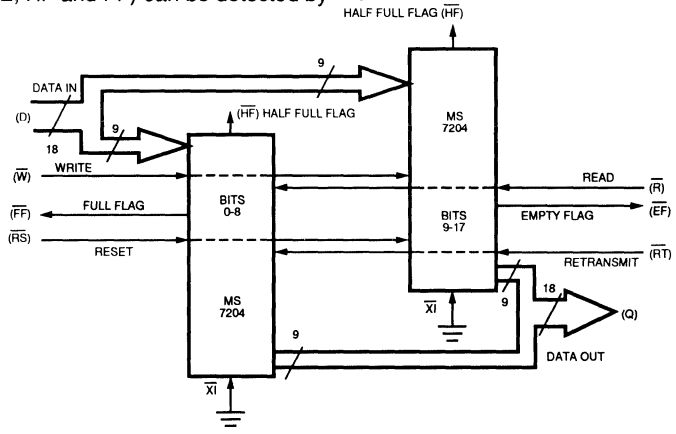


Figure 4. Width Expansion Mode

NOTES:

Flag detection is accomplished by monitoring the EF, HF and EF pins on the device used in the Width Expansion Mode. Do not connect output control signals together.

Depth Expansion Mode (Daisy Chain) Mode

Word depths may be expanded in multiples of 4096 words by Daisy Chaining the devices together as follows:

1. The FIRST LOAD (FL) control signal of the first device must be grounded. This FIFO represents word 1-4096.
2. All other devices in the Daisy Chain must have the FIRST LOAD (FL) control signal tied to V_{CC} in the inactive-high state.
3. The EXPANSION OUT (XO) pin of each device must be connected to the EXPANSION IN (XI) pin of the next device as shown in Figure 5.
4. External logic is required to generate a common FULL FLAG (FF) and EMPTY FLAG (EF) signal by ORing all of the FFs together and ORing all of the EFs together.
5. The RETRANSMIT (RT) fuction and HALF FULL FLAG (HF) are not available in Daisy Chain Mode.

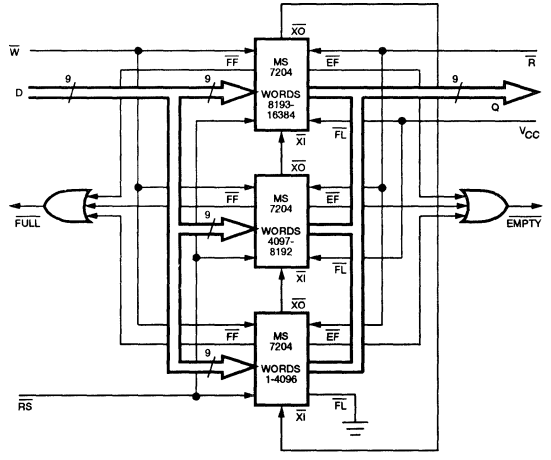


Figure 5. Diagram of a 16384 x 9 FIFO in Depth Expansion Mode

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Bidirectional Mode

Data buffering between two systems can be achieved by pairing two FIFO arrays as shown in Figure 6. This allows each system to READ and WRITE shared data. The FULL FLAG ($\overline{FF}$) must be monitored on the FIFO where WRITE ENABLE ($\overline{W}$) is used and the EMPTY FLAG ($\overline{EF}$) must be monitored on the FIFO where READ ENABLE ($\overline{R}$) is used. Both Width Expansion and Depth Expansion Modes may be used in combination with Bidirectional Mode.

Compound Expansion Mode:

Both Width Expansion Mode and Depth Expansion (Daisy Chain) Mode can be used together to configure a large FIFO array (See Figure 4 and 5).

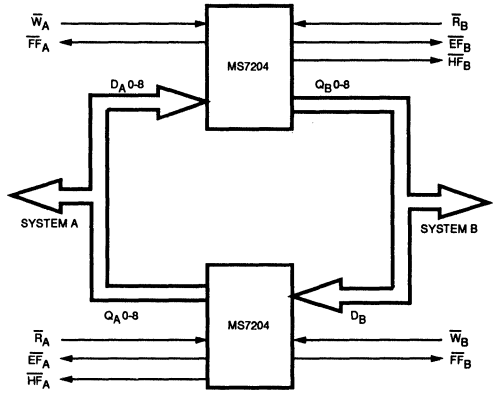


Figure 6. BIDirectional FIFO Mode

Ordering Information

Speed (Ns)	Ordering Part Number[1]		Package Reference No.	Temperature Range
20	MS7203-20PC	MS7204-20PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
20	MS7203-20NC		28 Pin Plastic DIP 300 mil	0°C to +70°C
20	MS7203-20JC	MS7204-20JC	32 Pin PLCC	0°C to +70°C
25	MS7203-25PC	MS7204-25PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
25	MS7203-25NC		28 Pin Plastic DIP 300 mil	0°C to +70°C
25	MS7203-25JC	MS7204-25JC	32 Pin PLCC	0°C to +70°C
35	MS7203-35PC	MS7204-35PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
35	MS7203-35NC	MS7204-35NC	28 Pin Plastic DIP 300 mil	0°C to +70°C
35	MS7203-35JC	MS7204-35JC	32 Pin PLCC	0°C to +70°C
35	MS7203-35FC	MS7204-35FC	28 Pin Small Outline 330 mil	0°C to +70°C
50	MS7203-50PC	MS7204-50PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
50	MS7203-50NC	MS7204-50NC	28 Pin Plastic DIP 300 mil	0°C to +70°C
50	MS7203-50JC	MS7204-50JC	32 Pin PLCC	0°C to +70°C
50	MS7203-50FC	MS7204-50FC	28 Pin Small Outline 330 mil	0°C to +70°C
80	MS7203-80PC	MS7204-80PC	28 Pin Plastic DIP - 600 mil	0°C to +70°C
80	MS7203-80NC	MS7204-80NC	28 Pin Plastic DIP 300 mil	0°C to +70°C
80	MS7203-80JC	MS7204-80JC	32 Pin PLCC	0°C to +70°C
80	MS7203-80FC	MS7204-80FC	28 Pin Small Outline 330 mil	0°C to +70°C

[1] For the low power version, add L after part number and before dash information. For example, MS7203L-25PC.

MOSEL-VITELIC ***MS76215 & MS76225***
512 x 18 & 1024 x 8 PARALLEL
SYNCHRONOUS FIFOs

Features

- Full CMOS clocked synchronous FIFOs
- Read and write clocks can be synchronous or asynchronous
- Master / Slave devices make depth and width expansion easy
- Two densities: 512 x 18 and 1024 x 18
- 20ns read / write cycle time
- Dual port memory architecture
- Five Flags for memory status:
  - Empty and Full Flags
  - Two Programmable Flags
  - Half Full Flag available in single device configuration
- Master device supplies all flag outputs in depth expansion
- Output Enable puts output in high impedance
- Available in 68-lead pin grid array (PGA), and plastic leaded chip carrier (PLCC)

Description

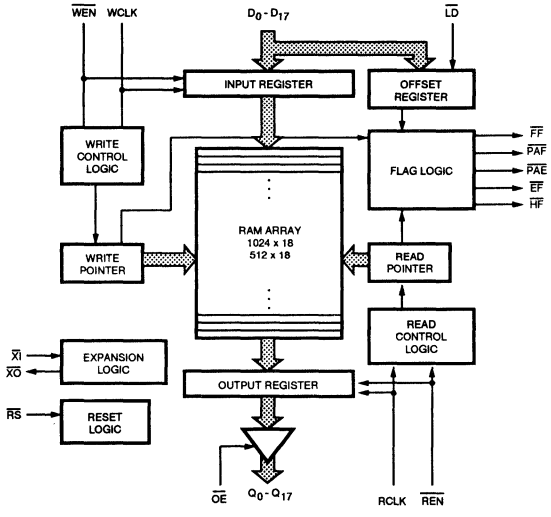
The MS76215 and MS76225 are clocked registered FIFOs that are particularly useful in synchronous design applications. This architecture allows for a user friendly part with a very high speed cycle time of 50MHz. The MS76215 and MS76225 are the master versions. Typical applications for these designs are data buffering for workstation graphics, interprocessor communications, and high speed LANs.

All four devices have 18-bit wide parallel data inputs and outputs. The input port is controlled by a free running clock (WCLK), and a write enable pin ($\overline{WEN}$). Data is written into the FIFO only when both the lock pin and write enable are active. The output port is controlled by separate clock (RCLK) and a read enable ($\overline{REN}$) pins. The read clock can be tied to the write clock for single clock operation or the two clocks can run independently. The devices also have an output enable ($\overline{OE}$) for three-state control of the output.

These FIFOs have a total of five flags. That is two fixed flags, Empty ($\overline{EF}$) and Full ($\overline{FF}$), two programmable flags, ($\overline{PAE}$) and ($\overline{PAF}$), plus a Half Full ($\overline{HF}$) flag available in single device operation. The programmable flags are programmed by asserting the Load ($\overline{LD}$) pin and clocking in the next two words on the inputs.

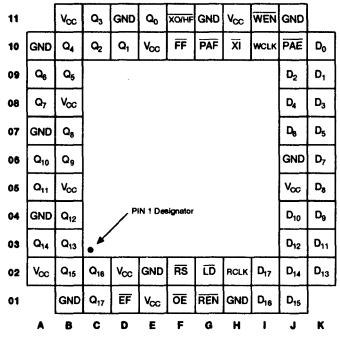
The MS76215 and MS76225 are both width and depth expandable. The pins $\overline{XI}$ and $\overline{XO}$ are required to expand the FIFOs in depth. To permit programmable flags in depth expansion, a master device (MS76215/25) controls the flags.

Functional Block Diagram

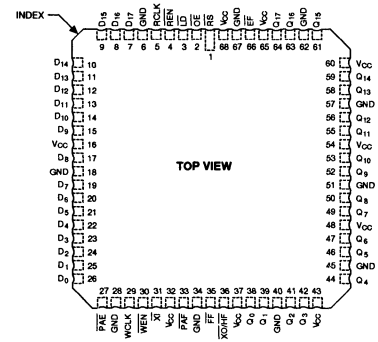


PinConfigurations

PGA TOP VIEW



PLCC TOP VIEW



Pin Descriptions

D_0-D_{17} Data Inputs
Data inputs for 18-bit wide data.

$\overline{RS}$ Reset
When $\overline{RS}$ is set low, internal read and write pointers are set to the first location of the RAM array, $\overline{FF}$ and $\overline{PAF}$ go high , and $\overline{PAE}$ and $\overline{EF}$ go low. A reset is required before an initial WRITE after power-up.

WCLK Write Clock
When $\overline{WEN}$ is enabled (low), a write cycle is initiated on the low-to-high transition of every WCLK clock, if the FIFO is not full.

$\overline{WEN}$ Write Enable
When $\overline{WEN}$ is low, data can be loaded into the FIFO on the low-to-high transition of every WCLK clock. When $\overline{WEN}$ is high, the FIFO holds the previous data. When the FIFO is full ($\overline{FF}$ = low), the internal WRITE operation is blocked.

RCLK Read Clock
When $\overline{REN}$ is enabled (low), data can be read on the outputs on the low-to-high transition of the read clock RCLK if the FIFO is not empty.

$\overline{REN}$ Read Enable
When $\overline{REN}$ is (low), data can be read from the FIFO on the low-to-high transition of every RCLK clock. When $\overline{REN}$ is high, the output register holds the previous data. When the FIFO is empty ($\overline{EF}$ = low), the internal READ operation is blocked.

$\overline{OE}$ Output Enable
When $\overline{OE}$ is enabled (low), the parallel output buffers receive data from the output register. When $\overline{OE}$ is disabled (high), the Q output bus is in a high impedance state.

$\overline{LD}$ Load
When $\overline{LD}$ is low, data on the inputs D_0-D_{17} is written to the offset and depth registers on the low-to-high transition of the WCLK.

$\overline{XI}$ Expansion Input
In the single device or width expansion configuration, $\overline{XI}$ is grounded. In the depth expansion configuration, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.

$\overline{FF}$ Full Flag
When $\overline{FF}$ goes low, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is high, the device is not full. $\overline{FF}$ is synchronized with WCLK.

$\overline{EF}$ Empty Flag
When $\overline{EF}$ goes low, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is high, the device is not empty. $\overline{EF}$ is synchronized with RCLK.

$\overline{PAF}$ Programmable Almost-Full Flag
When $\overline{PAF}$ is low, the device is almost full based on the programmable full offset. If there is no offset specified, the device is 7/8 full or more.

$\overline{PAE}$ Programmable Almost-Empty Flag
When $\overline{PAE}$ is low, the device is almost empty based on the programmable empty offset. If there is no offset specified, the device is empty to 1/8 full.

$\overline{XO}$/$\overline{HF}$ Expansion Out/Half-Full Flag
In the single device or width expansion configuration, the device is more than half full when $\overline{HF}$ is low. In the depth expansion configuration, a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the FIFO is filled.

Q_0-Q_{17} Outputs
Data outputs for 18-bit wide data.

V_{CC} Power Supply
Nine +5V power supply pins.

GND Ground
Ten ground pins

MS76500A
64K x 16 BI-DIRECTIONAL FIFO WITH PARITY GENERATOR/CHECKER

Features

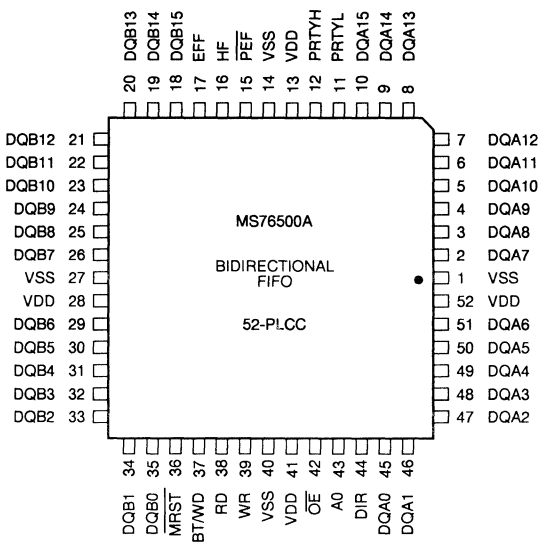
- 64 x 16 bi-directional FIFO
- A-port supports byte parity generation/checking
- B-port can be selected for 8 or 16-bit data width
- Three status flags - Empty/Full, Half Full and Parity Error
- 3-state outputs with output enable
- High performance - 25MHz and 33MHz cycle time
- Data Fall through mode
- All inputs and outputs are fully TTL compatible
- Single +5V power supply
- 52-pin PLCC
- High performance CMOS technology

Descriptions

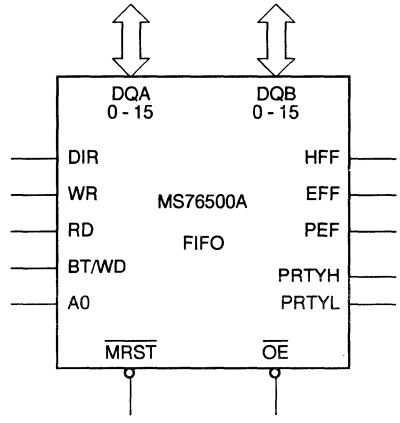
The MS76500A is an asynchronous 64 x 16 BiFIFO using a dual port RAM based architecture. The MS76500A has two 16-bit bi-directional data ports. User can select the direction by merely establishing a logic level at the control input. The A-port is equipped with parity checking/generation logic and supports byte parity. The B-port data width can be selected for 8-bit or 16-bit operation by a simple logic signal at a control pin.

The MS76500A provides FIFO status using Empty/Full, Half Full, and parity error flags. Fast access and read/write cycle times make it suitable for in many modern microprocessor applications. It is manufactured with high performance CMOS technology and is available in 52-pin PLCC package. All inputs and outputs are fully TTL compatible and it operates from a single +5V supply.

Pin Configuration
52-PIN PLCC



Logic Symbol



Pin Description

$\overline{MRST}$ (Master Reset, Input, Active Low)

The $\overline{MRST}$ input must be held LOW for the specified duration to initialize the FIFO. This input must return to HIGH and remain HIGH for normal operation. Master Reset does not affect the contents of the FIFO, only initialize the appropriate control elements. The following conditions prevail after reset:

a) the read and write pointers are cleared and point to the first location in the memory.
b) the EFF output is HIGH to indicate that the FIFO is empty.
c) the HFF output is LOW.
d) the FIFO output register is initialized to indicate LOW outputs.
e) the $\overline{PEF}$ is reset to HIGH.

LOW on the WR and RD inputs is recommended during the initialization. Any transients on these inputs may affect the pointers and interfere with the proper operation of the device.

WR (Write Control, Input, Active HIGH)

A LOW to HIGH transition of this input writes data into a FIFO location as determined by the write pointer. Data must conform to the specified setup and hold time requirements for reliable operation. Write operation terminates when the WR input returns to its quiescent LOW state. All attempts to write data into a full FIFO are ignored. It also should be noted that write and read operations are independent and asynchronous. Thus, write operations can be attempted without any regard to the read operations.

Write pointer updating occurs on the HIGH to LOW transition of the WR input. The flag outputs are combinatorially derived from the pointers. Thus, if there are 32 words in the FIFO because of the current write operation, the HFF output goes HIGH when the write operation terminates. Similarly, if there are 64 words in the FIFO because of the current write operation, the EFF output HIGH (FIFO full) after the write operation terminates.

RD (Read Control, Input, Active HIGH)

A LOW to HIGH transition of this input loads data from the FIFO location determined by the read pointer into the output register. The read operation terminates when the RD input returns quiescent LOW state. All read attempts from an empty FIFO are ignored and the output register remains unaffected. It also should be noted that read and write operations are independent and asynchronous. Thus, read operations can be attempted without any regard to the write operations.

Read pointer updating occurs on the HIGH to LOW transition of the RD input. The flag outputs are combinatorially derived from the pointers. Thus, if there are less than 32 words in the FIFO because of the current read operation, the Half Full flag output goes LOW after the read operation terminates. Similarly, if the EFF was HIGH because the FIFO was full, upon termination of the read operation, the EFF output will become LOW.

DIR (Direction Control, Input)

Logic level maintained at this input determines which one of the two data ports will be used for data input; LOW means that A-port is the input and B-port will be the output. On the other hand, HIGH on this input designates B-port as the input and A-port as the output. The DIR input also affects the PRTYL and PRTYH signals as described later.

It should be noted that this input is not stored on the chip and requires a stable level. For reliable operation, a read or write operation must not be in progress when the logic level on the DIR input needs changing.

DQA0 - DQA15 (A-port, Bi-directional)

These sixteen signals form the 16-bit A-port. If the DIR input is LOW, the A-port becomes the data input to the FIFO. If the DIR input is HIGH, data output from the FIFO is available on the A-port. When the A-port is used as the output port, the $\overline{OE}$ input controls the A-port buffers; LOW on $\overline{OE}$ input enables the buffers and HIGH disables the buffers into a high impedance state. The PRTYL and PRTYH signals are associated with the A-port and will be described later.

DQB0 - DQB15 (B-port, Bi-directional)

These sixteen signals form the 16-bit B-port. If the DIR input is HIGH, the B-port becomes the data input to the FIFO. If the DIR is LOW, B-port provides the data output from the FIFO. When the B-port is selected as the output port, the $\overline{OE}$ input controls the B-port buffers; LOW on $\overline{OE}$ enables the buffers and HIGH disables the buffers into a high impedance state.

The B-port may be controlled to be either 8-bit or 16-bit port depending on the logic level present at the BT/WD input. If the B-port is used as an 8-bit input port, then the information on DQB0 - DQB7 lines is used and lines DQB8 - DQB15 is ignored. On the other hand, if the B-port is used as an 8-bit output port, then the $\overline{OE}$ controls the DQB0 - DQB7

buffers and DQB8 - DQB15 buffers are forced unconditionally into a high impedance state.

BT/WD (Byte/Word select, Input)
The logic level on this input affects the B-port data width; LOW means the B-port is 16-bit wide and HIGH means 8-bit wide. It should be noted that the BT/WD input only defines the desired port width, the DIR input still specifies whether the B-port is an input or output.

It should be noted that this input is not stored on the chip and therefore a stable level must be maintained. For reliable operation, read or write operations should not be in progress when changing the logic level at this input. It is also recommended that the desired level on this input be established immediately following a reset operation.

A0 (Byte Select, Input)
This input controls the assembling words from bytes and splitting words into bytes for the B-port in the 8-bit mode.

When the B-port is an 8-bit output port and the A0 input is HIGH, the upper byte (bit8 - bit15) of the word read from the FIFO will be available on DQB0 - DQB7 respectively. On the other hand, if the A0 input is LOW, the lower byte (bit0 - bit7) of the word read from the FIFO will be available on the DQB0 - DQB7 respectively.

The A0 input is ignored if B-port is selected for 16-bit operation (B/W input LOW). The A0 input is not stored on the chip and therefore requires a stable logic level. When using the B-port in the 8-bit input mode, the WR input must be low when changing the level on the A0 input.

PRTYL (A-port lower byte parity, Bi-directional)
When the A-port is selected as the input port, PRTYL is used as an input. Information present on this signal is the parity bit for information present on DQA0 - DQA7. During a write operation, the on-chip parity checker performs an odd parity check. If there is a parity error PEF flag will be set to LOW. It should be noted that write operation proceeds as usual.

When the A-port is selected as the output port, the on-chip parity generator provides the odd parity for the byte present on DQA0 - DQA7 outputs on the PRTYL pin. It should be noted that the $\overline{OE}$ input controls the PRTYL output also. Moreover, resetting the device clears the FIFO output register. Therefore, the PRTYL will be high to reflect odd parity.

PRTYH (A-port upper byte parity, Bi-directional)
The operation of the PRTYH signal is identical to PRTYL signal described above except that DQA8 - DQA15 signals are used for parity checking and generation.

EFF (Empty/Full Flag, Output, Active High)
This output goes HIGH when the FIFO is empty. The FIFO is empty after a reset or all the information written into it had been read out. As soon a word is written into an empty FIFO all read attempts from an empty FIFO will be ignored, the EFF output will go LOW.

The EFF output also goes HIGH again if the FIFO contains 64 words that have not been read out (FIFO full). All write attempts into full FIFO will be ignored. When a word is read out from a full FIFO, the EFF goes LOW.

HFF (Half Full Flag, Output, Active High)
This output goes HIGH whenever the FIFO contains 32 or more words and remains HIGH until the words are read out to reach below the half full level.

$\overline{OE}$ (Output Enable, Input, Active Low)
This input controls the buffers associated with the A-port, B-port, PRTYL and PRTYH signals. When $\overline{OE}$ is LOW, the associated buffer will be enabled to drive the pin. If the $\overline{OE}$ is HIGH the associated buffers will be in a high impedance state.

$\overline{PEF}$ (A-port Parity Error Flag, Output, Active Low)
When the A-port is used as the input port, the on-chip odd parity checker checks the lower byte (DQA0 - DQA7) and the upper byte (DQA8 - DQA15) using the PRTYL and PRTYH signals as the corresponding parity check bit.

If there is a parity error in either byte, the PEF output goes LOW when the WR input goes from LOW to HIGH to start the write operation. It should be noted that writing into the FIFO itself is not affected by the parity error. Once the PEF is set, it can only be cleared by resetting the FIFO or making the A-port as the output port (DIR input HIGH).

VDD +5V power supply.

VSS Ground.

Bidirectional FIFO Architecture

The following figure shows the MS76500A bidirectional FIFO block diagram. The MS76500A bidirectional FIFO features a single bank of 64 x 16-bit FIFO core, I/O MUX data route multiplexers and the 8/16-bit MUX byte/word multiplexer and de-multiplexer. The DIR input controls the I/O MUX data route multiplexers.

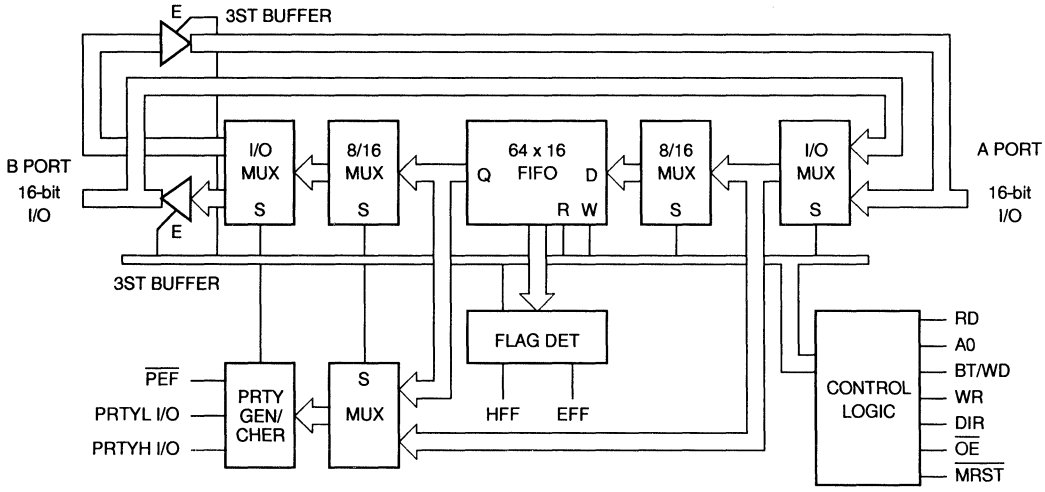
These multiplexers route the A or B port data to the FIFO core input, or the FIFO core output data to the B or A port. When the multiplexer selects the A port is an input port and the B port is an output port, the three-state output buffer at the A port is disabled regardless of the Output Control. The B port output buffer becomes active if the Output Control is LOW.

In the reverse direction, input data at the B port is routed to the FIFO core input while the three-state output buffer at the B port is disabled regardless of the Output Control, and output data from the FIFO core is routed to the A port. The A port output buffer become active if the Output Control is LOW.

The BT/WD byte/word multiplexer and de-multiplexer controls the B port input and output data width when the Byte/Word mode select input (BT/WD) is held at a logic HIGH. When the B port is programmed as an 8-bit input mode, only the low byte data at the B port is effective and the high byte data is ignored.

The A0 input addresses this input data to the low byte FIFO core or high byte core. When the A0 is LOW, the 8-bit data is addressed to the low byte FIFO core and when A0 is HIGH, input data is addressed to the high byte of the FIFO core. The data is written into the low byte or high byte FIFO core with an active write enable.

In the 8-bit output mode, the B port low byte output is effective port and high byte is in the three-state condition. The 16-bit output data from the FIFO core is de-multiplexed by the A0 byte select input. The low byte data from the FIFO core is selected and available if the A0 is LOW and the Output Enable is LOW. The high byte data is available when the A0 is HIGH and Output Enable is LOW. The M576500A operation truth table is shown on page 5.



BLOCK DIAGRAM

Truth Table (Operating Mode)

DIR	R	W	B/W	A0	Function
L	L	↑	X	X	16-bit wrlte to Port A
L	↑	L	L	X	16-bit read from Port B
L	↑	L	H	L	8-bit read from Port B (LSB)
L	↑	L	H	H	8-bit read from Port B (MSB)
H	L	↑	L	X	16-bit write to Port B
H	L	↑	H	L	8-bit write to Port B (LSB)
H	L	↑	H	H	8-bit write to Port B (MSB)
H	↑	L	X	X	16-bit read from Port A

Absolute Maximum Ratings (1)

Parameter Name	Parameter	Ratings	Units
V_{TERM}	Terminal Voltage with Rerspect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	V
T_{STG}	Storage Temperature	-45 to +120	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	D C Output Current	30	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute amximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Capacitance(1) T_A = 25°C, f = 1.0MHz

Parameter Name	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{DQ}	Output Capacitance	V_{DQ} = 0V	7	pF

1. This parameter is guaranteed and not tested.

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS76500A (-25, -30) Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.2		V_{CC} + 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{in} = 0V to V_{CC}	-10		10	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, V_{in} = 0V to V_{CC}	-10		10	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA A Port, I_{OL} = 4mA B Port and Flags			0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OL} = -4mA A Port, I_{OL} = 2mA B Port and Flags	2.4			V
I_{CC1}	Operating Current Supply Current	V_{CC} = Max, $I_{I/O}$ = 0mA, F = F_{max}			75	mA

AC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	MS76500A-25 Min.	MS76500A-25 Max.	MS76500A-30 Min.	MS76500A-30 Max.	Units
f_s	Shift Frequency	—	25	—	33	MHz
ReadCycle						
t_{RC}	Read Cycle Time	40	—	30	—	ns
t_A	Access Time	—	20	—	15	ns
t_{RPW}	Read Pulse Width	12	—	10	—	ns
t_{RR}	Read Recovery Time	12	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	3	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	40	—	30	—	ns
t_{WPW} (1)	Write Pulse Width	12	—	10	—	ns
t_{WR}	Write Recovery Time	12	—	10	—	ns
t_{DS}	Data Setup Time	2	—	1	—	ns
t_{DH}	Data Hold Time	4	—	3	—	ns
Flag Timing						
t_{REF}	Read High to Empty Flag High	—	15	—	12	ns
t_{RHF}	Read High to Half Full Flag Low	—	35	—	30	ns
t_{RFF}	Read High to Full Flag Low	—	22	—	20	ns
t_{WEF}	Write High to Empty Flag Low	—	22	—	20	ns
t_{WHF}	Write High to Half Full Flag High	—	35	—	30	ns
t_{RPE}	Read Pulse Width After EF High	—	22	—	20	ns
t_{PEV}	Write High to Parity Flag Valid	—	22	—	20	ns
t_{WFF}	Write High to Full Flag HIGH	—	22	—	20	ns
Reset Timing						
t_{RSC}	Reset Cycle Time	40	—	30	—	ns
t_{RS} (1)	Reset Pulse Width	25	—	25	—	ns
t_{RSS}	Reset Setup Time	25	—	25	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	ns
t_{EFH}	Reset to Empty Flag High	—	25	—	20	ns
t_{HFL}	Reset to Half Full Flag Low	—	25	—	25	ns
t_{FFD}	Reset to Data Clear	—	25	—	25	ns
t_{RSP}	Reset to Parity Bits High	—	25	—	20	ns

AC Electrical Characteristics (Continued)

Parameter Name	Parameter	MS76500A-25 Min.	MS76500A-25 Max.	MS76500A-30 Min.	MS76500A-30 Max.	Units
Direction Control Timing (DIR)						
t_{DRWS}	DIR Change to Read/Write High Setup	40	—	30	—	ns
t_{DRWH}	DIR Change to Read/Write High Hold	40	—	30	—	ns
t_{DPH}	DIR Change to Error-Flag High	25	—	25	—	ns
B/W Mode Timing (B/W)						
t_{MRWS}	B/W Mode Change to Read/Write High Setup	40	—	30	—	ns
t_{MRWH}	B/W Mode Change to Read/Write High Hold	40	—	30	—	ns
A0 Access Timing (A0)						
t_{A0RWS} (2)	A0 Access Time Setup Time	3	—	3	—	ns
t_{A0RWH} (2)	A0 Access Time Hold Time	8	—	5	—	ns
Output Enable Timing ($\overline{OE}$)						
t_{OEDHZ} (2)	$\overline{OE}$ High to Output High-Z	—	12	—	12	ns
t_{OEDLS}	$\overline{OE}$ Low to Output Low-Z	—	12	—	12	ns
Fall-Through Timing						
t_{WEF}	Write High to Empty Flag Low	—	25	—	20	ns
t_{FT}	Write High to Data Output Valid	10	35	10	30	ns

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Timing Reference Levels	1.5V

AC Test Loads and Waveforms

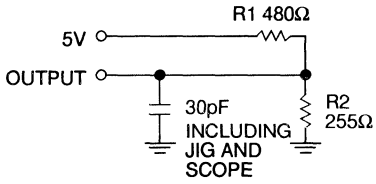


Figure 1a

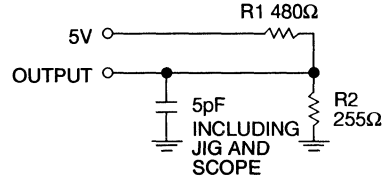
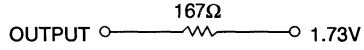


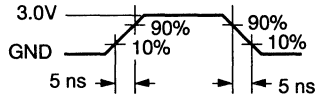
Figure 1b

Equivalent to:

THEVENIN EQUIVALENT



ALL INPUT PULSES



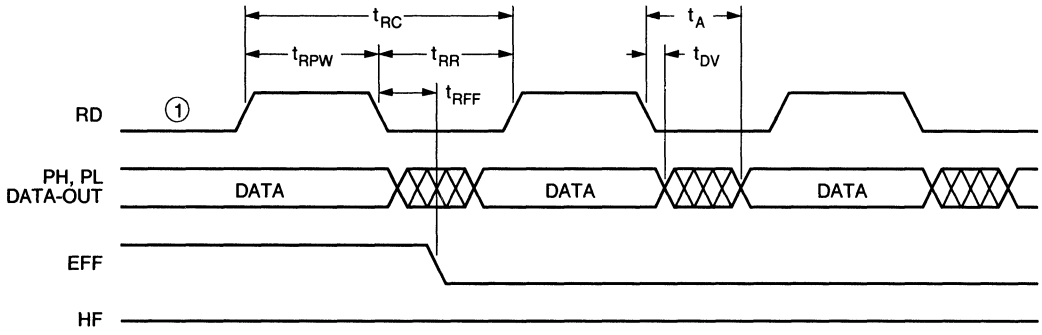
Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

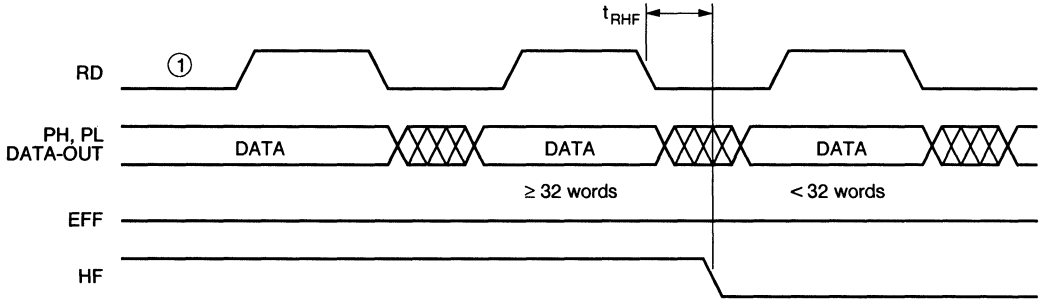
7

Timing Waveforms

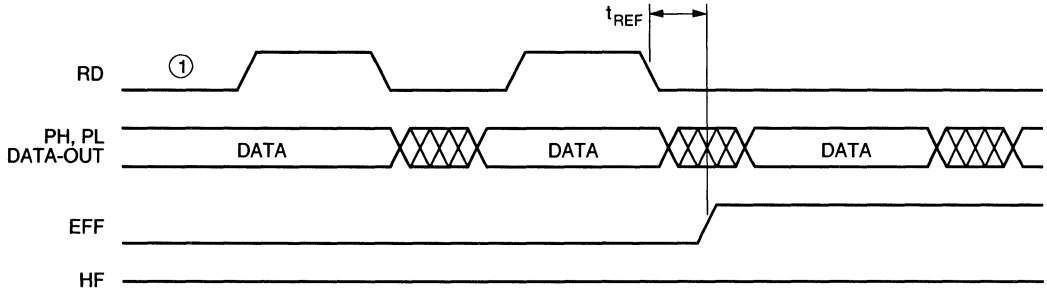
Data Out Timing - FIFO Contains 64 Words (1)



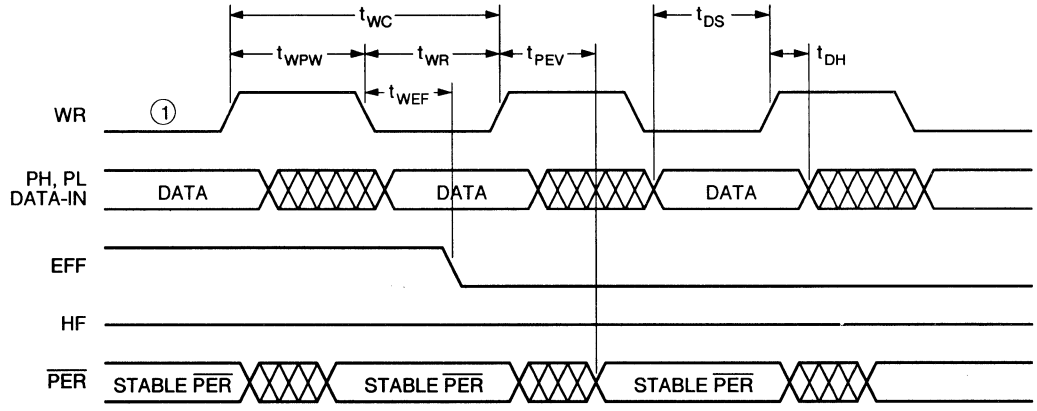
Data Out Timing - FIFO Contains 33 Data Words (1)



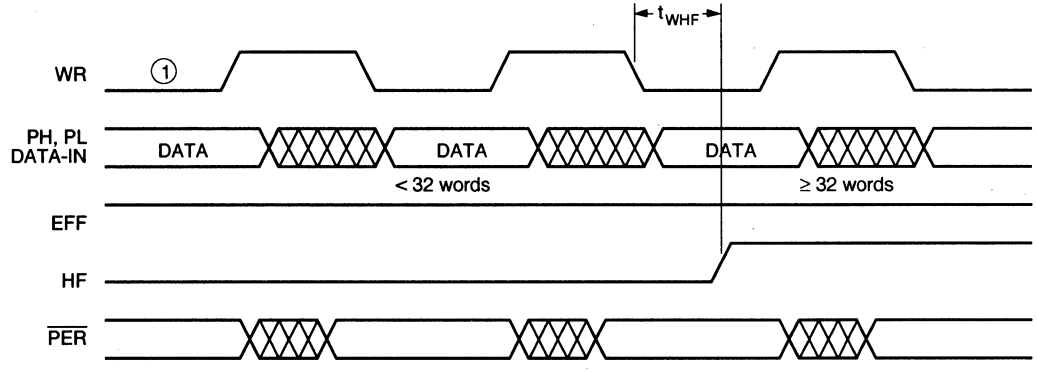
Data Out Timing - FIFO Contains 2 Data Words (1)



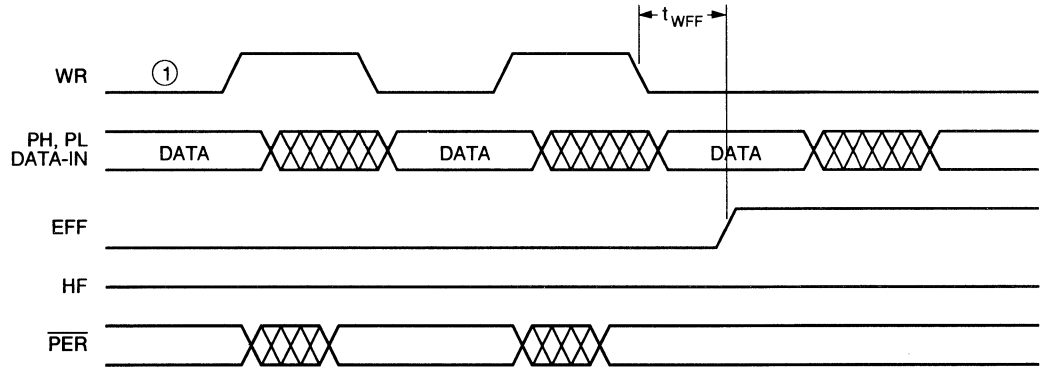
Data In Timing - FIFO Contains 0 Words (1)



Data In Timing - FIFO Contains 30 Data Words (1)

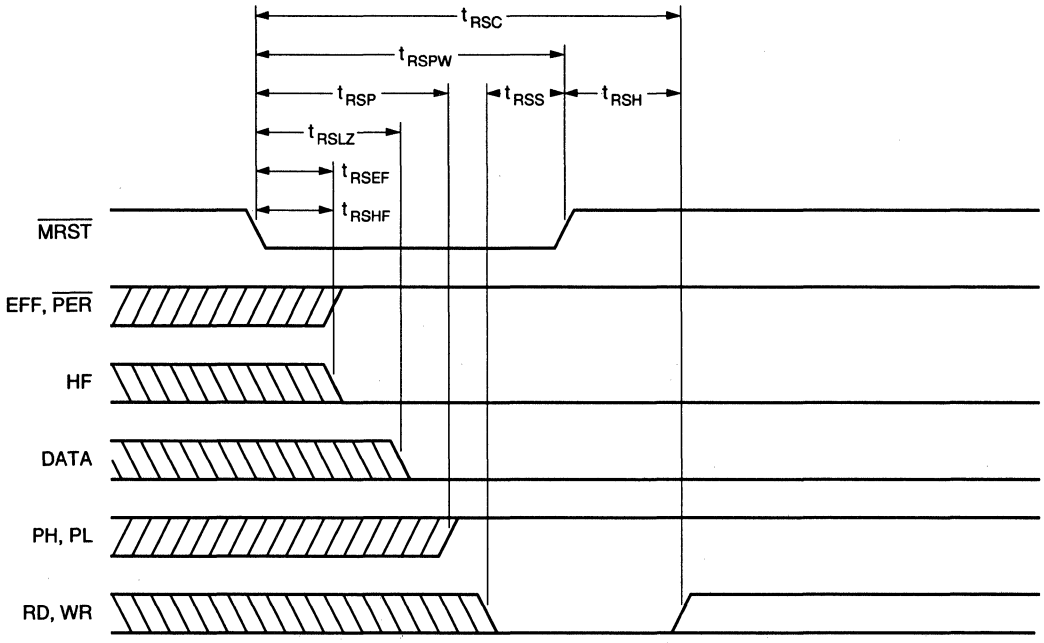


Data In Timing - FIFO Contains 62 Data Words (1)

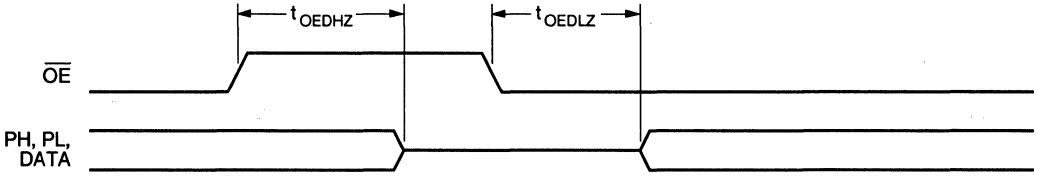


7

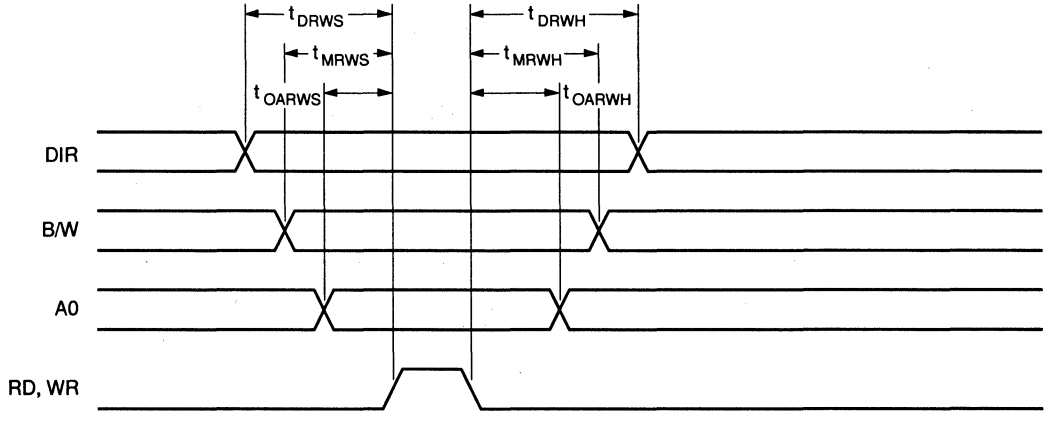
Master Reset Timing



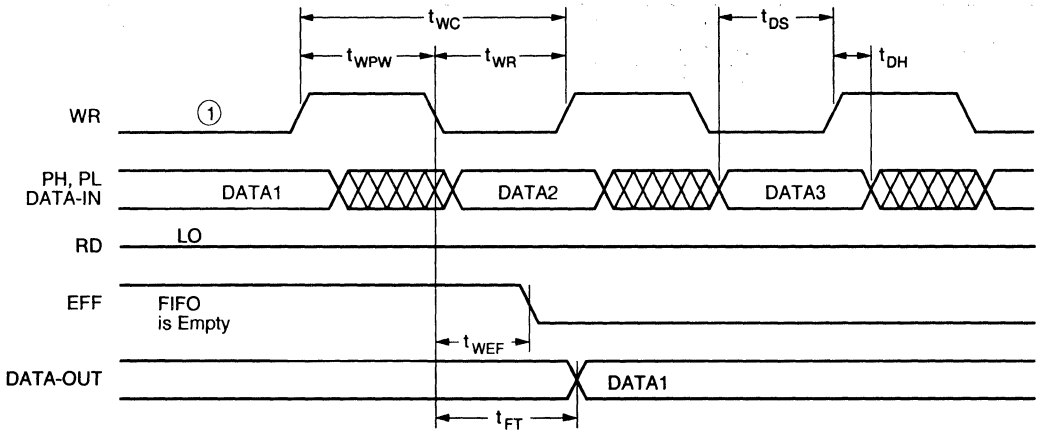
Output Enable Control Timing



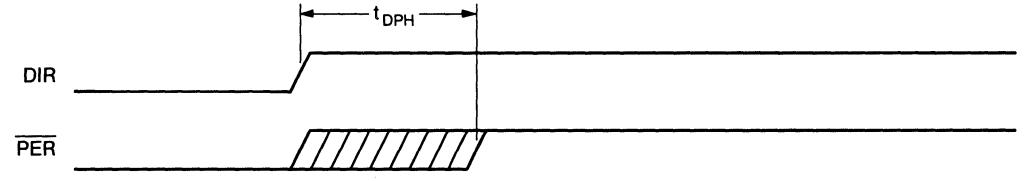
Miscellanious Control Timing



Data In Timing - FIFO Contains 0 Words (1)



Direction Change to Parity Flag Cleared Timing



7

Ordering Information

Speed (MHz)	Ordering Part Number[1)]	Package	Temperature Range
25	MS76500A-25JC	52 Pin Plastic PLCC	0°C to +70°C
30	MS76500A-30JC	52 Pin Plastic PLCC	0°C to +70°C

MS76502A
256 x 16 BI-DIRECTIONAL FIFO WITH PARITY GENERATOR/CHECKER

Features

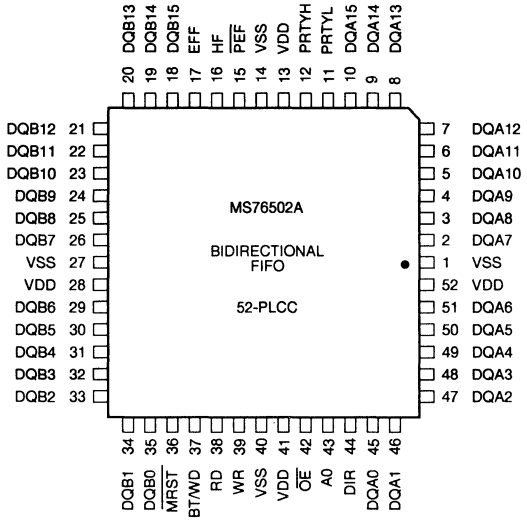
- 256 x 16 bi-directional FIFO
- A-port supports byte parity generation/checking
- B-port can be selected for 8 or 16-bit data width
- Three status flags - Empty/Full, Half Full and Parity Error
- 3-state outputs with output enable
- High performance - 25MHz and 33MHz cycle time
- Data Fall through mode
- All inputs and outputs are fully TTL compatible
- Single +5V power supply
- 52-pin PLCC
- High performance CMOS technology

Description

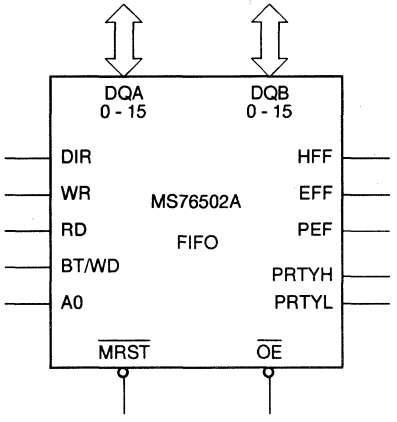
The MS76502A is an asynchronous 256 x 16 BiFIFO using a dual port RAM based architecture. The MS76502 has two 16-bit bi-directional data ports. User can select the direction by merely establishing a logic level at the control input. The A-port is equipped with parity checking/generation logic and supports byte parity. The B-port data width can be selected for 8-bit or 16-bit operation by a simple logic signal at a control pin.

The MS76502A provides FIFO status using Empty/Full, Half Full, and parity error flags. Fast access and read/write cycle times make it suitable for in many modern microprocessor applications. It is manufactured with high performance CMOS technology and is available in 52-pin PLCC package. All inputs and outputs are fully TTL compatible and it operates from a single +5V supply.

Pin Configuration
52-PIN PLCC



Logic Symbol



Pin Description

$\overline{MRST}$ (Master Reset, Input, Active Low)

The $\overline{MRST}$ input must be held LOW for the specified duration to initialize the FIFO. This input must return to HIGH and remain HIGH for normal operation. Master Reset does not affect the contents of the FIFO, only initialize the appropriate control elements. The following conditions prevail after reset:

a) the read and write pointers are cleared and point to the first location in the memory.
b) the EFF output is HIGH to indicate that the FIFO is empty.
c) the HFF output is LOW.
d) the FIFO output register is initialized to indicate LOW outputs.
e) the $\overline{PEF}$ is reset to HIGH.

LOW on the WR and RD inputs is recommended during the initialization. Any transients on these inputs may affect the pointers and interfere with the proper operation of the device.

WR (Write Control, Input, Active HIGH)

A LOW to HIGH transition of this input writes data into a FIFO location as determined by the write pointer. Data must conform to the specified setup and hold time requirements for reliable operation. Write operation terminates when the WR input returns to its quiescent LOW state. All attempts to write data into a full FIFO are ignored. It also should be noted that write and read operations are independent and asynchronous. Thus, write operations can be attempted without any regard to the read operations.

Write pointer updating occurs on the HIGH to LOW transition of the WR input. The flag outputs are combinatorially derived from the pointers. Thus, if there are 32 words in the FIFO because of the current write operation, the HFF output goes HIGH when the write operation terminates. Similarly, if there are 64 words in the FIFO because of the current write operation, the EFF output HIGH (FIFO full) after the write operation terminates.

RD (Read Control, Input, Active HIGH)

A LOW to HIGH transition of this input loads data from the FIFO location determined by the read pointer into the output register. The read operation terminates when the RD input returns quiescent LOW state. All read attempts from an empty FIFO are ignored and the output register remains unaffected. It also should be noted that read and write operations are independent and asynchronous. Thus, read operations can be attempted without any regard to the write operations.

Read pointer updating occurs on the HIGH to LOW transition of the RD input. The flag outputs are combinatorially derived from the pointers. Thus, if there are less than 32 words in the FIFO because of the current read operation, the Half Full flag output goes LOW after the read operation terminates. Similarly, if the EFF was HIGH because the FIFO was full, upon termination of the read operation, the EFF output will become LOW.

DIR (Direction Control, Input)

Logic level maintained at this input determines which one of the two data ports will be used for data input; LOW means that A-port is the input and B-port will be the output. On the other hand, HIGH on this input designates B-port as the input and A-port as the output. The DIR input also affects the PRTYL and PRTYH signals as described later.

It should be noted that this input is not stored on the chip and requires a stable level. For reliable operation, a read or write operation must not be in progress when the logic level on the DIR input needs changing.

DQA0 - DQA15 (A-port, Bi-directional)

These sixteen signals form the 16-bit A-port. If the DIR input is LOW, the A-port becomes the data input to the FIFO. If the DIR input is HIGH, data output from the FIFO is available on the A-port. When the A-port is used as the output port, the $\overline{OE}$ input controls the A-port buffers; LOW on $\overline{OE}$ input enables the buffers and HIGH disables the buffers into a high impedance state. The PRTYL and PRTYH signals are associated with the A-port and will be described later.

DQB0 - DQB15 (B-port, Bi-directional)

These sixteen signals form the 16-bit B-port. If the DIR input is HIGH, the B-port becomes the data input to the FIFO. If the DIR is LOW, B-port provides the data output from the FIFO. When the B-port is selected as the output port, the $\overline{OE}$ input controls the B-port buffers; LOW on $\overline{OE}$ enables the buffers and HIGH disables the buffers into a high impedance state.

The B-port may be controlled to be either 8-bit or 16-bit port depending on the logic level present at the BT/WD input. If the B-port is used as an 8-bit input port, then the information on DQB0 - DQB7 lines is used and lines DQB8 - DQB15 is ignored. On the other hand, if the B-port is used as an 8-bit output port, then the $\overline{OE}$ controls the DQB0 - DQB7

buffers and DQB8 - DQB15 buffers are forced unconditionally into a high impedance state.

BT/WD (Byte/Word select, Input)
The logic level on this input affects the B-port data width; LOW means the B-port is 16-bit wide and HIGH means 8-bit wide. It should be noted that the BT/WD input only defines the desired port width, the DIR input still specifies whether the B-port is an input or output.

It should be noted that this input is not stored on the chip and therefore a stable level must be maintained. For reliable operation, read or write operations should not be in progress when changing the logic level at this input. It is also recommended that the desired level on this input be established immediately following a reset operation.

A0 (Byte Select, Input)
This input controls the assembling words from bytes and splitting words into bytes for the B-port in the 8-bit mode.

When the B-port is an 8-bit output port and the A0 input is HIGH, the upper byte (bit8 - bit15) of the word read from the FIFO will be available on DQB0 - DQB7 respectively. On the other hand, if the A0 input is LOW, the lower byte (bit0 - bit7) of the word read from the FIFO will be available on the DQB0 - DQB7 respectively.

The A0 input is ignored if B-port is selected for 16-bit operation (B/W input LOW). The A0 input is not stored on the chip and therefore requires a stable logic level. When using the B-port in the 8-bit input mode, the WR input must be low when changing the level on the A0 input.

PRTYL (A-port lower byte parity, Bi-directional)
When the A-port is selected as the input port, PRTYL is used as an input. Information present on this signal is the parity bit for information present on DQA0 - DQA7. During a write operation, the on-chip parity checker performs an odd parity check. If there is a parity error PEF flag will be set to LOW. It should be noted that write operation proceeds as usual.

When the A-port is selected as the output port, the on-chip parity generator provides the odd parity for the byte present on DQA0 - DQA7 outputs on the PRTYL pin. It should be noted that the $\overline{OE}$ input controls the PRTYL output also. Moreover, resetting the device clears the FIFO output register. Therefore, the PRTYL will be high to reflect odd parity.

PRTYH (A-port upper byte parity, Bi-directional)
The operation of the PRTYH signal is identical to PRTYL signal described above except that DQA8 - DQA15 signals are used for parity checking and generation.

EFF (Empty/Full Flag, Output, Active High)
This output goes HIGH when the FIFO is empty. The FIFO is empty after a reset or all the information written into it had been read out. As soon a word is written into an empty FIFO all read attempts from an empty FIFO will be ignored, the EFF output will go LOW.

The EFF output also goes HIGH again if the FIFO contains 256 words that have not been read out (FIFO full). All write attempts into full FIFO will be ignored. When a word is read out from a full FIFO, the EFF goes LOW.

HFF (Half Full Flag, Output, Active High)
This output goes HIGH whenever the FIFO contains 32 or more words and remains HIGH until the words are read out to reach below the half full level.

$\overline{OE}$ (Output Enable, Input, Active Low)
This input controls the buffers associated with the A-port, B-port, PRTYL and PRTYH signals. When $\overline{OE}$ is LOW, the associated buffer will be enabled to drive the pin. If the $\overline{OE}$ is HIGH the associated buffers will be in a high impedance state.

$\overline{PEF}$ (A-port Parity Error Flag, Output, Active Low)
When the A-port is used as the input port, the on-chip odd parity checker checks the lower byte (DQA0 - DQA7) and the upper byte (DQA8 - DQA15) using the PRTYL and PRTYH signals as the corresponding parity check bit.

If there is a parity error in either byte, the PEF output goes LOW when the WR input goes from LOW to HIGH to start the write operation. It should be noted that writing into the FIFO itself is not affected by the parity error. Once the PEF is set, it can only be cleared by resetting the FIFO or making the A-port as the output port (DIR input HIGH).

VDD +5V power supply.

VSS Ground.

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Bidirectional FIFO Architecture

The following figure shows the MS76502A bidirectional FIFO block diagram. The MS76502A bidirectional FIFO features a single bank of 256 x 16-bit FIFO core, I/O MUX data route multiplexers and the 8/16-bit MUX byte/word multiplexer and de-multiplexer. The DIR input controls the I/O MUX data route multiplexers.

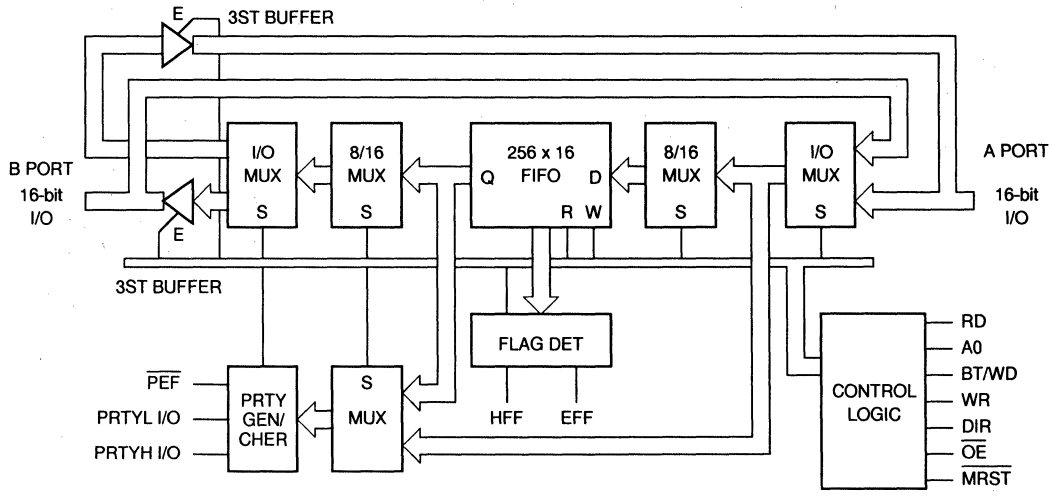
These multiplexers route the A or B port data to the FIFO core input, or the FIFO core output data to the B or A port. When the multiplexer selects the A port is an input port and the B port is an output port, the three-state output buffer at the A port is disabled regardless of the Output Control. The B port output buffer becomes active if the Output Control is LOW.

In the reverse direction, input data at the B port is routed to the FIFO core input while the three-state output buffer at the B port is disabled regardless of the Output Control, and output data from the FIFO core is routed to the A port. The A port output buffer become active if the Output Control is LOW.

The BT/WD byte/word multiplexer and de-multiplexer controls the B port input and output data width when the Byte/Word mode select input (BT/WD) is held at a logic HIGH. When the B port is programmed as an 8-bit input mode, only the low byte data at the B port is effective and the high byte data is ignored.

The A0 input addresses this input data to the low byte FIFO core or high byte core. When the A0 is LOW, the 8-bit data is addressed to the low byte FIFO core and when A0 is HIGH, input data is addressed to the high byte of the FIFO core. The data is written into the low byte or high byte FIFO core with an active write enable.

In the 8-bit output mode, the B port low byte output is effective port and high byte is in the three-state condition. The 16-bit output data from the FIFO core is de-multiplexed by the A0 byte select input. The low byte data from the FIFO core is selected and available if the A0 is LOW and the Output Enable is LOW. The high byte data is available when the A0 is HIGH and Output Enable is LOW. The M576502A operation truth table is shown on page 5.



Block Diagram

Truth Table (Operating Mode)

DIR	R	W	B/W	A0	Function
L	L	↑	X	X	16-bit write to Port A
L	↑	L	L	X	16-bit read from Port B
L	↑	L	H	L	8-bit read from Port B (LSB)
L	↑	L	H	H	8-bit read from Port B (MSB)
H	L	↑	L	X	16-bit write to Port B
H	L	↑	H	L	8-bit write to Port B (LSB)
H	L	↑	H	H	8-bit write to Port B (MSB)
H	↑	L	X	X	16-bit read from Port A

Absolute Maximum Ratings (1)

Parameter Name	Parameter	Rating	Units
V_{TERM}	Terminal Voltage with Rerspect to GND	-0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	-10 to +125	V
T_{STG}	Storage Temperature	-45 to +120	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	D C Output Current	30	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute amximum rating conditions for extended periods may affect reliability.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%

Capacitance(1) T_A = 25°C, f = 1.0MHz

Parameter Name	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	7	pF
C_{DQ}	Output Capacitance	V_{DQ} = 0V	7	pF

1. This parameter is guaranteed and not tested.

DC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	Test Conditions	MS76502A (-25, -30) Min.	Typ.	Max.	Unit
V_{IL}	Input LOW Voltage				0.8	V
V_{IH}	Input HIGH Voltage		2.2		V_{CC} + 0.3	V
I_{IL}	Input Leakage Current	V_{CC} = Max, V_{in} = 0V to V_{CC}	-10		10	µA
I_{OL}	Output Leakage Current	V_{CC} = Max, V_{in} = 0V to V_{CC}	-10		10	µA
V_{OL}	Output LOW Voltage	V_{CC} = Min, I_{OL} = 8mA A Port, I_{OL} = 4mA B Port and Flags			0.4	V
V_{OH}	Output HIGH Voltage	V_{CC} = Min, I_{OL} = -4mA A Port, I_{OL} = 2mA B Port and Flags	2.4			V
I_{CC1}	Operating Current Supply Current	V_{CC} = Max, $I_{I/O}$ = 0mA, F = F_{max}			75	mA

AC Electrical Characteristics (over the commercial operating range)

Parameter Name	Parameter	MS76502A-25 Min.	MS76502A-25 Max.	MS76502A-30 Min.	MS76502A-30 Max.	Units
f_s	Shift Frequency	—	25	—	33	MHz
f_s	Shift Frequency	—	25	—	33	MHz
ReadCycle						
t_{RC}	Read Cycle Time	40	—	30	—	ns
t_A	Access Time	—	20	—	15	ns
t_{RPW}	Read Pulse Width	12	—	10	—	ns
t_{RR}	Read Recovery Time	12	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	3	—	ns
Write Cycle						
t_{WC}	Write Cycle Time	40	—	30	—	ns
t_{WPW} (1)	Write Pulse Width	12	—	10	—	ns
t_{WR}	Write Recovery Time	12	—	10	—	ns
t_{DS} (2)	Data Setup Time	2	—	1	—	ns
t_{DH} (2)	Data Hold Time	4	—	3	—	ns
Flag Timing						
t_{REF}	Read High to Empty Flag High	—	15	—	12	ns
t_{RHF}	Read High to Half Full Flag Low	—	35	—	30	ns
t_{RFF}	Read High to Full Flag Low	—	22	—	20	ns
t_{WEF}	Write High to Empty Flag Low	—	22	—	20	ns
t_{WHF}	Write High to Half Full Flag High	—	35	—	30	ns
t_{RPE}	Read Pulse Width After EF High	—	22	—	20	ns
t_{PEV}	Write High to Parity Flag Valid	—	22	—	25	ns
t_{WFF}	Write High to Full Flag HIGH	—	22	—	20	ns
Reset Timing						
t_{RSC}	Reset Cycle Time	40	—	30	—	ns
t_{RS} (1)	Reset Pulse Width	25	—	25	—	ns
t_{RSS}	Reset Setup Time	25	—	25	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	ns
t_{EFH}	Reset to Empty Flag High	—	25	—	20	ns
t_{HFL}	Reset to Half Full Flag Low	—	25	—	25	ns
t_{FFD}	Reset to Data Clear	—	25	—	25	ns
t_{RSP}	Reset to Parity Bits High	—	25	—	20	ns

AC Electrical Characteristics (Continued)

Parameter Name	Parameter	MS76502A-25 Min.	MS76502A-25 Max.	MS76502A-30 Min.	MS76502A-30 Max.	Units
f_s	Shift Frequency	—	25	—	33	MHz
Direction Control Timing (DIR)						
t_{DRWS}	DIR Change to Read/Write High Setup	40	—	30	—	ns
t_{DRWH}	DIR Change to Read/Write High Hold	40	—	30	—	ns
t_{DPH}	DIR Change to Error-Flag High	25	—	25	—	ns
B/W Mode Timing (B/W)						
t_{MRWS}	B/W Mode Change to Read/Write High Setup	40	—	30	—	ns
t_{MRWH}	B/W Mode Change to Read/Write High Hold	40	—	30	—	ns
A0 Access Timing (A0)						
t_{A0RWS} (2)	A0 Access Time Setup Time	3	—	3	—	ns
t_{A0RWH} (2)	A0 Access Time Hold Time	8	—	5	—	ns
Output Enable Timing ($\overline{OE}$)						
t_{OEDHZ} (2)	$\overline{OE}$ High to Output High-Z	—	12	—	12	ns
t_{OEDLS}	$\overline{OE}$ Low to Output Low-Z	—	12	—	12	ns
Fall-Through Timing						
t_{WEF}	Write High to Empty Flag Low	—	25	—	20	ns
t_{FT}	Write High to Data Output Valid	10	35	10	30	ns

NOTES:
1. Pulse widths less than minimum values are not allowed.
2. Values guaranteed by design, not currently tested.

AC Test Conditions

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Timing Reference Levels	1.5V

AC Test Loads and Waveforms

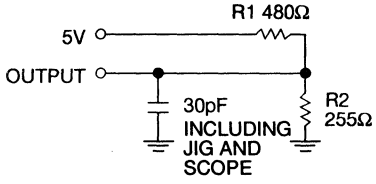


Figure 1a

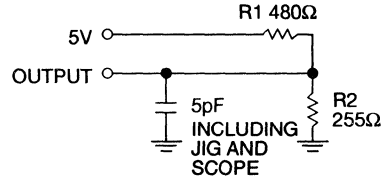
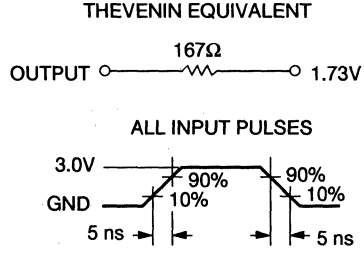


Figure 1b

Equivalent to:



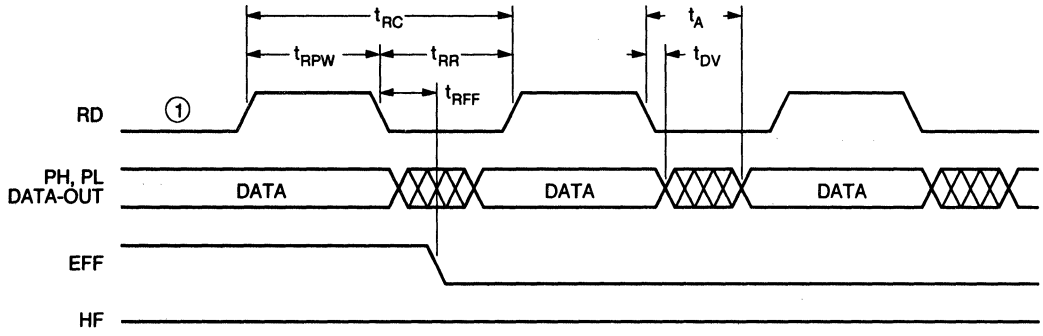
Key to Switching Waveforms

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

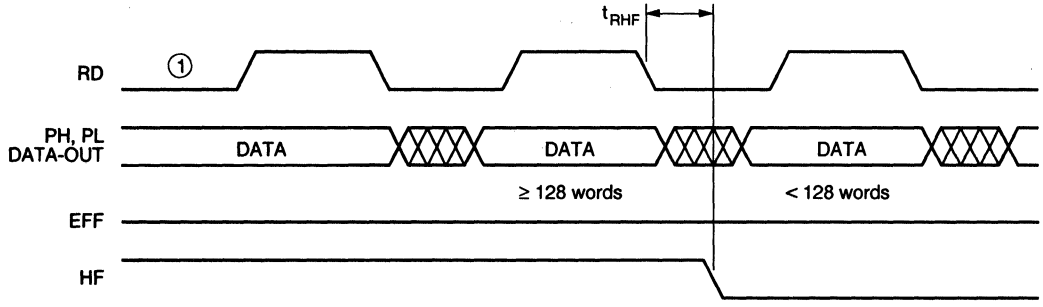
7

Timing Waveforms

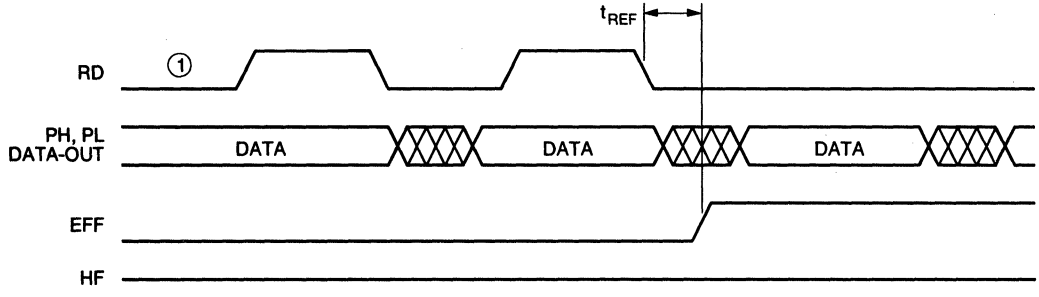
Data Out Timing - FIFO Contains 256 Words (1)



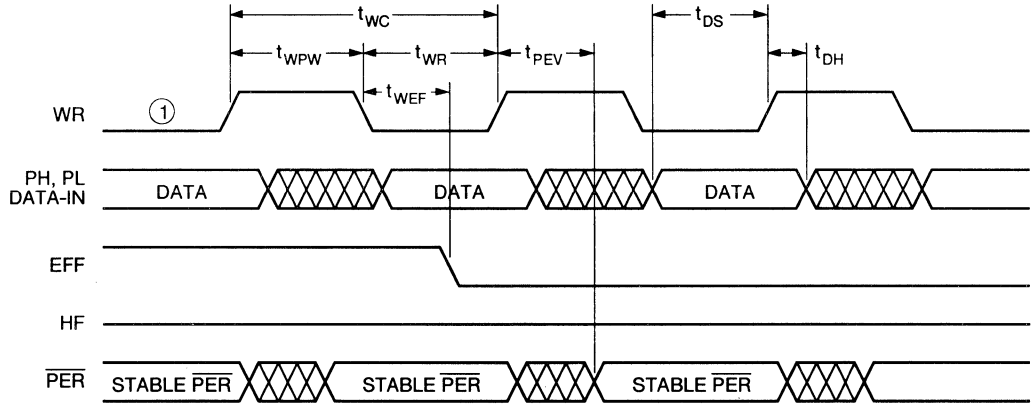
Data Out Timing - FIFO Contains 129 Data Words (1)



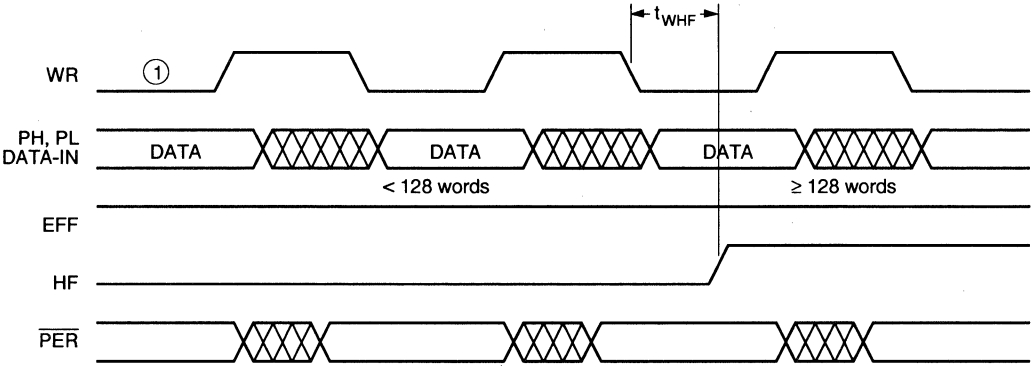
Data Out Timing - FIFO Contains 2 Data Words (1)



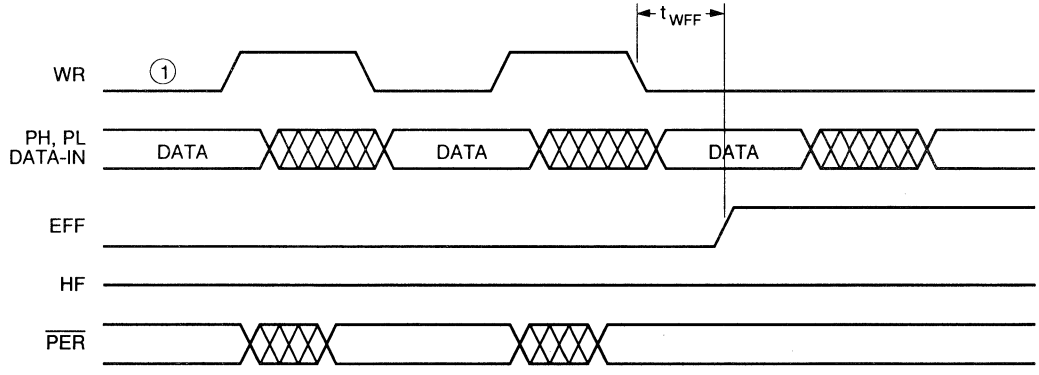
Data In Timing - FIFO Contains 0 Words (1)



Data In Timing - FIFO Contains 126 Data Words (1)

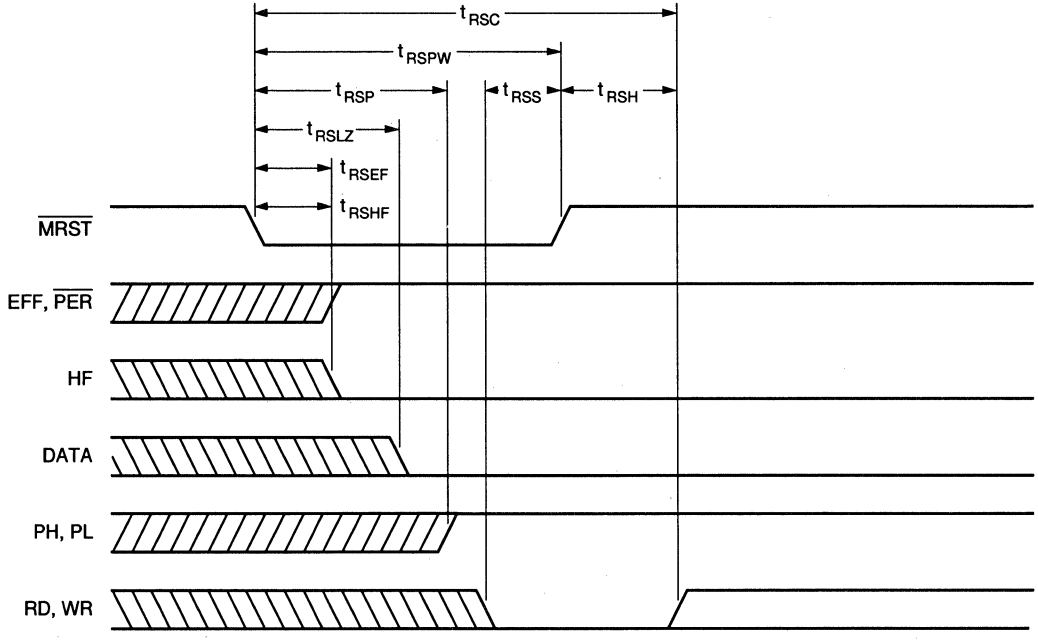


Data In Timing - FIFO Contains 254 Data Words (1)

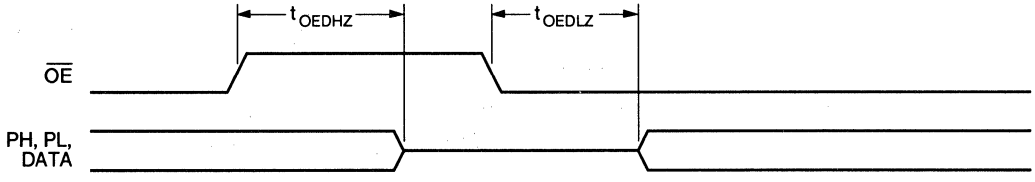


7

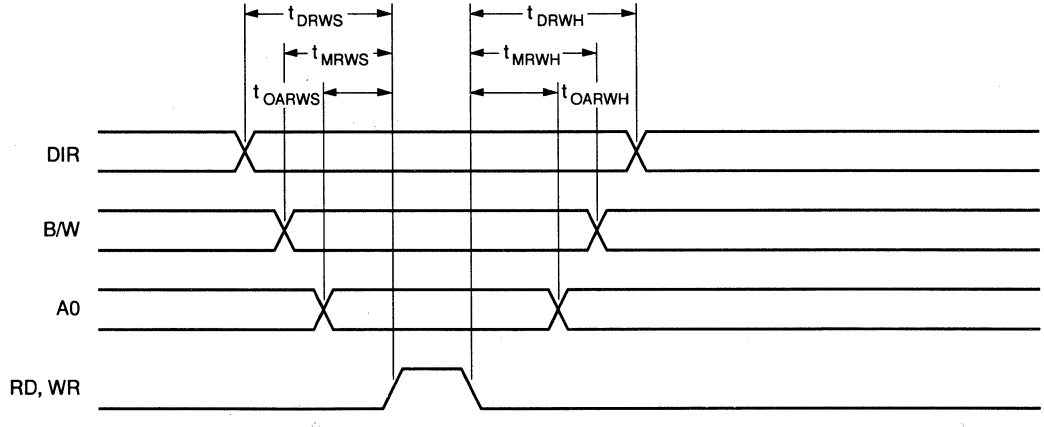
Master Reset Timing



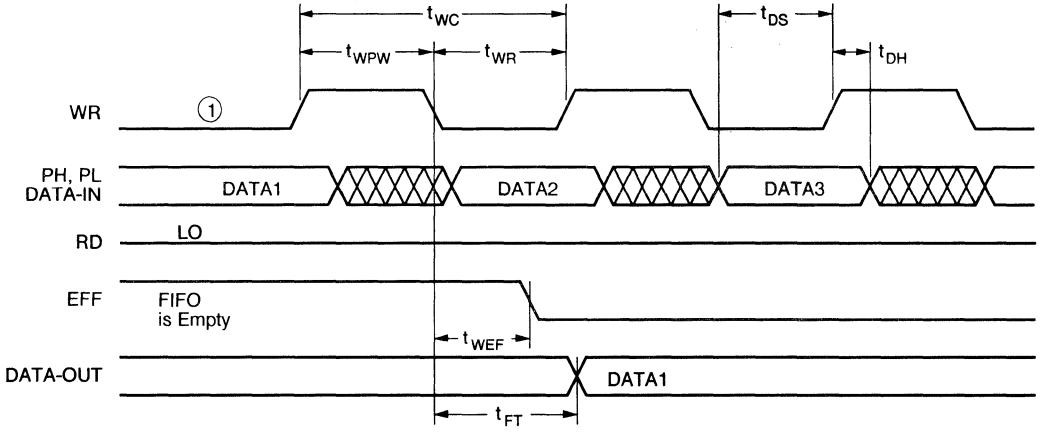
Output Enable Control Timing



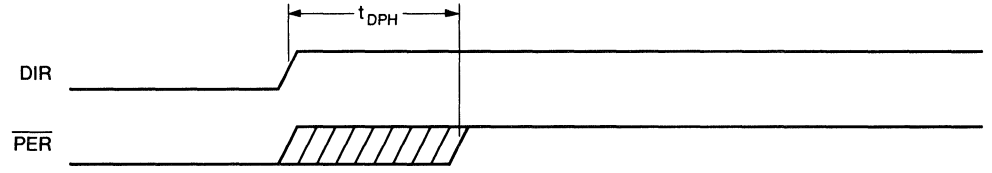
Miscellanious Control Timing



Data In Timing - FIFO Contains 0 Words (1)



Direction Change to Parity Flag Cleared Timing



7

Ordering Information

Speed (MHz)	Ordering Part Number[1)]	Package	Temperature Range
25	MS76502A-25JC	52 Pin Plastic PLCC	0°C to +70°C
30	MS76502A-30JC	52 Pin Plastic PLCC	0°C to +70°C

MOSEL-VITELIC MS76542
256 x 36 x 2
BIDIRECTIONAL FIFO

Features

- Fast cycle times - 25/30/35 ns
- Two 256 x 36 Bit FIFO Buffers
- Wide 36-bit word width
- Selectable 9/18/36-bit word width on port-B
- Fully Asynchronous port-to-port communications
- High speed, port-synchronous clocking mechanism
  - Edge triggered clocks
  - R/W, Enable, & Address pins sampled on the rising clock edge
  - Synchronous request acknowledge handshake (optional)
- Asynchronous output enables
- Dedicated FIFO status flags for Empty, Half-Full, & Full flags
- Programmable status flags for Almost Empty & Almost Full
- Mailbox registers with synchronized flags
- Data bypass function
- Data retransmit function
- Byte parity check
- TTL & CMOS compatible I/O
- Area efficient QFP package

Description

The MS76542 contains two FIFO buffers which operate in parallel but opposite directions for bidirectional data buffering. The two FIFO buffers are each organized as 256 words by 36 bits. The MS76542 is ideal for either wide unidirectional or bidirectional data applications, since component count and board area is reduced.

Each port has its own port-synchronous clock, but the two ports may operate asynchronously relative to each other. Data flow is initiated on a port by the rising edge of the appropriate clock and read/write control signals. Clock duty cycles can vary from 40% to 60% without sacrificing performance.

FIFO status flags monitor the extent to which the FIFO buffers have been filled. These include Empty, Almost Empty, Half Full, Almost Full, and Full flags for each FIFO. The Almost Empty and Empty Full flags are programmable over the entire FIFO depth, but are conveniently initialized to 8 locations from the respective boundaries at reset.

A synchronous request acknowledge handshake is provided on each port for FIFO data accesses. This request-acknowledge handshake resolves FIFO full and empty boundary conditions, when the two ports are operated asynchronously relative to each other.

Two mailbox registers provide a separate path for passing control status words between ports. Each mailbox has a flag which is synchronized to the reading port's clock. This mailbox function can facilitate the synchronization of data transfers between asynchronous systems.

A Data Bypass mode allows Port-A to directly transfer data to or from Port-B at reset. In this mode the device acts as a registered transceiver under Port-A control. For instance, a master processor on Port-A can use the Data Bypass feature to pass initialization or configuration information directly to or from a peripheral device on Port-B during a system start-up.

A word width select option is provided on Port B for 9 bit, 18 bit, or 36 bit data accesses. This allows word width matching between Port A and B with no additional logic; and ensures maximum utilization of bus bandwidths. A Byte Parity Check Flag on each port ensures data integrity. These flags initialize for odd data parity at reset, but may be reprogrammed for even or odd parity.

Signal Descriptions

Reset ($\overline{RS}$)

This input must be driven LOW for a specified period of time to initialize the device. After initialization, this input must return to HIGH for proper operation of the device.

When the $\overline{RS}$ input is LOW, the MS76542 is in data bypass mode of operation. See functional description for details.

After initialization, the control section of the MS76542 will be in the default state. See functional description for details.

A-Port Data Bus (D0A - D35A)

These 36 bi-directional signals form the A-port data bus. If the $\overline{OE}_A$ is HIGH, the A-port data bus receivers are enabled and the internal bus drivers are disabled. However, if the $\overline{OE}_A$ input is LOW, the internal A-port data bus drivers are unconditionally enabled to drive the bus.

During a FIFO write operation from the A-port, 36-bit information from this bus will be written into the FIFO#1. During this operation, the 36 bits present on this bus are treated as four 9-bit bytes (eight data bits and one parity bit). The four bytes of a 36-bit word are grouped as D0A - D8A, D9A - D17A, D18A- D26A, and D26A - D35A.

During a FIFO read operation, 36-bit read from FIFO 2 will be available on this bus. During read operations, the parity check logic treats D0A - D8A, D9A - D17A, D18A - D25A, and26A D35A as four parity protected bytes.

B-Port Data Bus (D0B - D35B)

These 36 bi-directional signals form the B-port data bus. If the $\overline{OE}_B$ is HIGH, the B-port data bus receivers are enabled and the internal bus drivers are disabled. However, if the $\overline{OE}_B$ input is LOW, the internal B-port data bus drivers are unconditionally enabled to drive the bus.

During a FIFO write operation from the B-port, 36-bit information from this bus will be written into the FIFO 2. During this operation, the 36 bits present on this bus are treated as four 9-bit bytes (eight data bits and one parity bit). The four bytes of a 36-bit word are grouped as D0B - D8B, D9B - D17B, D18B - D25B, and D26B - D35B.

During a FIFO read operation, 36-bit read from FIFO#1 will be available on this bus. During read operations, the parity check logic treats D0B - D8B, D9B - D17B, D18B - D25B, and D26B - D35B as four parity protected bytes.

During FIFO read and FIFO write operations only, the B-port bus width is determined by the WS0 - WS1 inputs. See functional description for details.

A-Port Clock (CK_A)

Free running A-Port clock input.

B-Port Clock (CK_B)

Free running B-Port clock input.

A-Port Read/Write Control ($R/\overline{W}_A$)

Logic level at this input is sampled by the LOW-to-HIGH transition of the CK_A input; HIGH specifies read and LOW specifies write. The actual read or write operation does not start until the EN_A input is sampled HIGH also.

A-Port Read/Write Enable (EN_A)

Logic level at this input is sampled by the LOW-to-HIGH transition of the CK_A input. If this input is sampled HIGH operation specified by the $R/\overline{W}_A$ input is performed.

B-Port Read/Write Control ($R/\overline{W}_B$)

Logic level at this input is sampled by the LOW-to-HIGH transition of the CK_B input; HIGH specifies read and LOW specifies write. The actual read or write operation does not start until the EN_B input is sampled HIGH also.

B-Port Read/Write Enable (EN_B)

Logic level at this input is sampled by the LOW-to-HIGH transition of the CK_B input. If this input is sampled HIGH operation specified by the $R/\overline{W}_B$ input is performed.

A-Port Control Register Address (A0A - A2A)

Logic level present on these three inputs is sampled by the LOW-to-HIGH transition of the CK_A input to select various registers according to the following table:

A0A	A1A	A2A	
L	L	L	$\overline{AF}$2 Flag Offset Register
L	L	H	$\overline{AE}$2 Flag offset Register
L	H	L	$\overline{AF}$1 Flag Offset Register
L	H	H	$\overline{AE}$1 Flag Offset Register
H	L	L	Odd/Even Parity Select
H	L	H	Select all flag offset registers
H	H	L	Mailbox
H	H	H	FIFO

B-Port Control Register Address (A0B)

Logic level present on this input is sampled by the LOW-to-HIGH transition of the CK_B input. If sampled HIGH, FIFO operation is selected. On the other hand, if sampled LOW, the mailbox is selected.

A-Port Output Enable ($\overline{OE}_A$)

LOW on this input unconditionally enables the A-port data bus drivers and HIGH unconditionally disables them input high impedance state.

B-Port Output Enable ($\overline{OE}_B$)

LOW on this input unconditionally enables the B-port data bus drivers and HIGH unconditionally disables them input high impedance state.

FIFO #1 Full Flag ($\overline{FF}$1)

LOW on this output indicates that the FIFO#1 is full and write operations into FIFO#1 are locked out. This output goes LOW on the LOW-to-HIGH transition of CK_A input for a write operation that will fill the FIFO#1. This flag will go HIGH on the HIGH-to-LOW transition of the CK_B input for a read operation from a full FIFO#1. This flag will be HIGH after reset.

FIFO #2 Full Flag ($\overline{FF}$2)

LOW on this output indicates that the FIFO#1 is full and write operations into FIFO#2 are locked out. This output goes LOW on the LOW-to-HIGH transition of CK_A input for a write operation that will fill the FIFO#2. This flag will go HIGH on the HIGH-to-LOW transition of the CK_B input for a read operation from a full FIFO#2. This flag will be HIGH after reset.

FIFO #1 Almost-Full Flag ($\overline{AF}$1)

LOW on this output indicates that the FIFO#1 has filled to a preset depth. The preset depth is determined by the values loaded into the $\overline{AF}$1 Flag Offset Register. After a reset, the default value is eight words from the FIFO#1 end boundary.

FIFO #2 Almost-Full Flag ($\overline{AF}$2)

LOW on this output indicates that the FIFO#2 has filled to a preset depth. The preset depth is determined by the values loaded into the $\overline{AF}$2 Flag Offset Register. After a reset, the default value is eight words from the FIFO#2 end boundary.

FIFO #1 Half-Full Flag ($\overline{HF}$1)

LOW on this output indicates that FIFO#1 is half full from the physical end boundary. This output goes LOW during a write operation on the LOW-to-HIGH transition of CK_A input that half fills the FIFO#1. This output goes HIGH during a read operation on the HIGH-to-LOW transition of the CK_B input from the half full FIFO#1.

FIFO #2 Half-Full Flag ($\overline{HF}$2)

LOW on this output indicates that FIFO#2 is half full from the physical end boundary. This output goes LOW during a write operation on the LOW-to-HIGH transition of CK_B input that half fills the FIFO#2. This output goes HIGH during a read operation on the HIGH-to-LOW transition of the CK_A input from the half full FIFO#2.

FIFO #1 Empty Flag ($\overline{EF}$1)

LOW on this output indicates that FIFO#1 contains no valid data. This flag goes LOW on the LOW-to-HIGH transition of CK_B input that empties the FIFO#1. This output goes HIGH on the LOW-to-HIGH transition of the CK_A input for write into empty FIFO#1.

FIFO #2 Empty Flag ($\overline{EF}$2)

LOW on this output indicates that FIFO#2 contains no valid data. This flag goes LOW on the LOW-to-HIGH transition of CK_A input that empties the FIFO#2. This output goes HIGH on the LOW-to-HIGH transition of the CK_B input for write into empty FIFO#2.

FIFO #1 Almost-Empty Flag ($\overline{AE}$1)

LOW on this output indicates that read operations from FIFO#1 reached to predetermined boundary. The predetermined boundary is determined by the value loaded into the $\overline{AE}$1 Flag Offset Register. After a reset, the default value is 8 locations from the beginning FIFO#1 boundary.

FIFO #2 Almost-Empty Flag ($\overline{AE2}$)
LOW on this output indicates that read operations from FIFO#2 reached to predetermined boundary. The predetermined boundary is determined by the value loaded into the $\overline{AE2}$ Flag Offset Register. After a reset, the default value is 8 locations from the beginning FIFO#2 boundary.

A-Port Parity Flag ($\overline{PF_A}$)
LOW on this output indicates that a parity error in one or more bytes of the information present on the A-Port data bus.

A-Port Parity Flag ($\overline{PF_B}$)
LOW on this output indicates that a parity error in one or more bytes of the information present on the B-Port data bus.

New Mail Alert Mailbox#1 ($\overline{MBF1}$)
LOW on this output indicates that information was written into Mailbox#1. When B-port reads the Mailbox#1, this output will go HIGH on the LOW-to-HIGH transition of the CK_B input. This is a status indicator only and does not inhibit mailbox operations.

New Mail Alert Mailbox #2 ($\overline{MBF2}$)
LOW on this output indicates that information was written into Mailbox#2. When A-port reads the Mailbox#2, this output will go HIGH on the LOW-to-HIGH transition of the CK_A input. This is a status indicator only and does not inhibit mailbox operations.

WS1	WS0	
L	L	9-bit
L	H	18-bit
H	X	36-bit

B-Port Word Width Select (WS0 - WS1)
Logic levels present on these two inputs specify the B-Port data width for FIFO operations only according to the following table. These pins have no effect on Data Bypass or Mailbox operations.

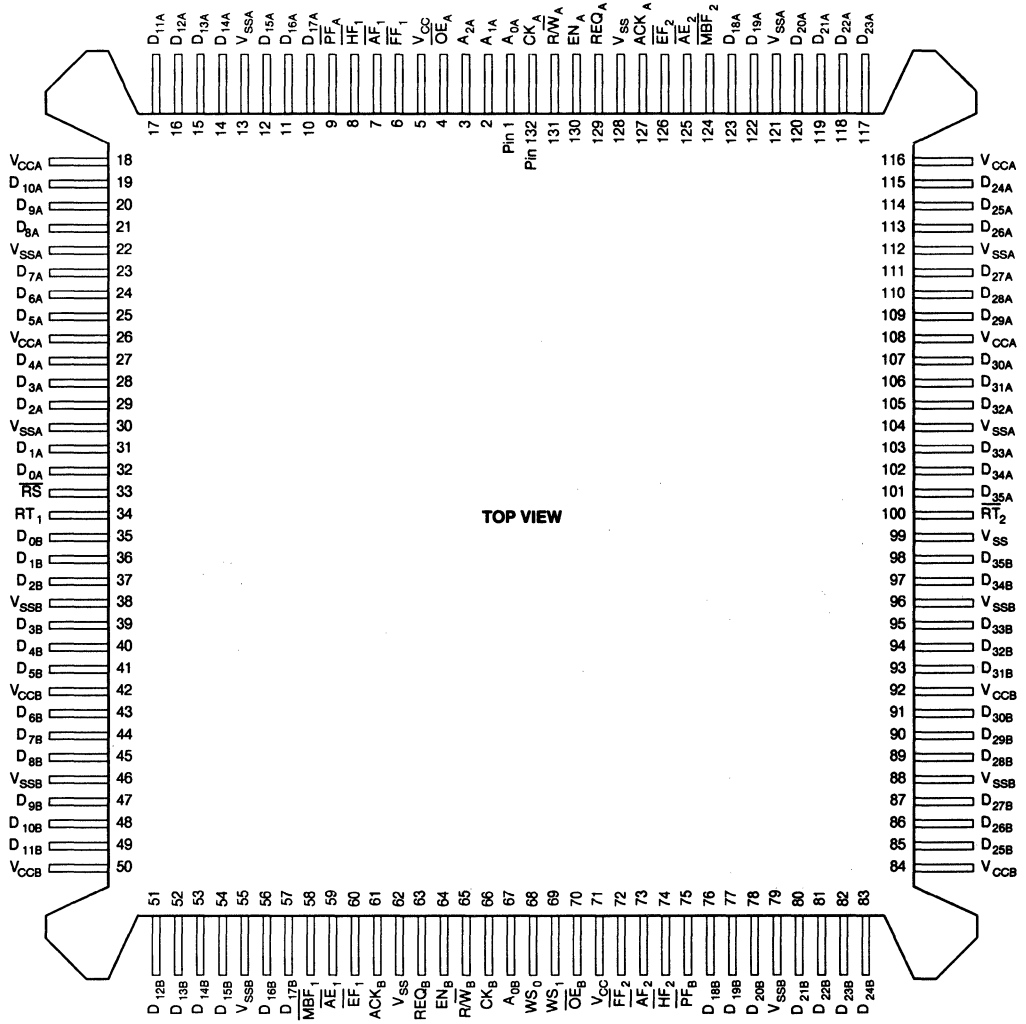
FIFO #1 Retransmit ($\overline{RT1}$)
If this input is sampled LOW by the LOW-to-HIGH transition of the CK_B input, the read pointer for FIFO#1 is reset to the first location. FIFO#1 write pointer is not effected. See Operational Description section for details on retransmit operation.

FIFO #2 Retransmit ($\overline{RT2}$)
If this input is sampled LOW by the LOW-to-HIGH transition of the CK_A input, the read pointer for FIFO#2 is reset to the first location. FIFO#2 write pointer is not effected. See Operational Description section for details on retransmit operation.

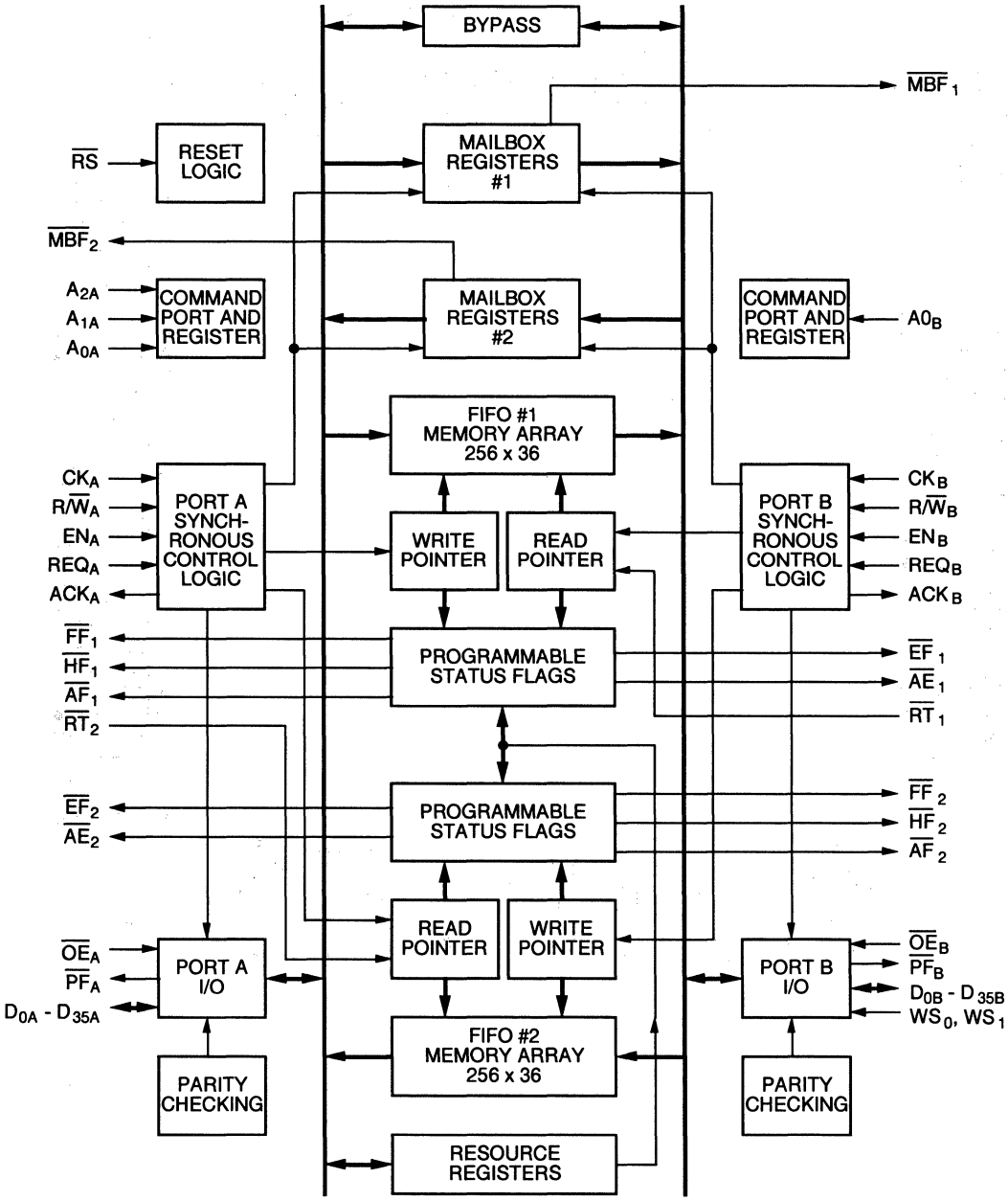
A-Port Handshake (REQA & ACKA)
These two signals are used for synchronous handshake by the A-Port. Detailed description is found in Operational Description section.

A-Port Handshake (REQB & ACKB)
These two signals are used for synchronous handshake by the B-Port. Detailed description is found in Operational Description section.

Pin Configurations



Functional Block Diagram



Absolute Maximum Ratings (1)

Parameter	Rating
Supply Voltage to V_{SS} Potential	-0.5V to 7V
Signal Pin Voltage to V_{SS} Potential [3]	-0.5V to V_{CC} + 0.5V
DC Output Current [2]	±40mA
Storage Temperature Range	-65°C to 150°C
Power Dissipation (Package Limit)	2 Watts (Quad Flat Pack)

Operating Range

Paramter Name	Parameter	Min	Max	Unit
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [3]	-0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

DC Electrical Characteristics (over operating range)

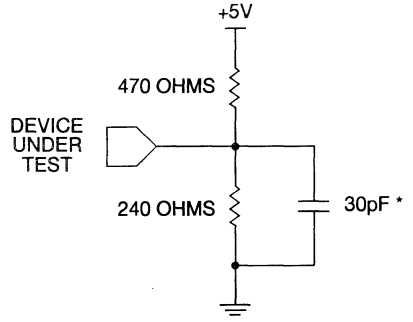
Parameter Name	Parameter	Test Conditions	Min	Max	Unit
I_{LI}	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	-10	10	µA
I_{LO}	I/O Leakage Current	$\overline{OE} \geq V_{IH}$, $0V \leq V_{OUT} \leq V_{CC}$	-10	10	µA
V_{OL}	Logic LOW Output Voltage	I_{OL} = 8.0mA		0.4	V
V_{OH}	Logic HIGH OutputVoltage	I_{OH} =-2.0mA	2.4		V
I_{CC}	Average Supply Current [4]	Measured at f_C = max		280	mA
I_{CC2}	Average Standby Supply Current [4]	All Inputs = V_{IHMIN} (Clock idle)			mA
I_{CC3}	Power-Down Supply Current [4]	All Inputs = V_{CC} - 0.2V (Clock idle)			mA

AC Test Conditions

Parameter	Rating
Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5ns
(10% to 90%)	
Output Reference Levels	1.5V
Input Timing Reference Levels	1.5V
Output Load, Timing Tests	See Loading

Capacitance [5, 6]

Parameter	Rating
C_{IN} (Input Capacitance)	8pF
C_O (OutputCapacitance)	8pF



* INCLUDES JIG AND SCOPE CAPACITANCES

7

AC Electrical Characteristics [7] V_{CC} = 5V ± 10%, T_A = 0°C to 70°C

Parameter Name	Description	-25		-30		-35		Unit
		Min	Max	Min	Max	Min	Max	
f_{CC}	Clock Cycle Frequency	—	40	—	33	—	28.5	MHz
t_{CC}	Clock Cycle Time	25	—	30	—	35	—	ns
t_{CH}	Clock High Time	10	—	12	—	15	—	ns
t_{CL}	Clock Low Time	10	—	12	—	15	—	ns
t_{DS}	Data Setup Time	11	—	13	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{ES}	Enable Setup Time [12]	11	—	13	—	15	—	ns
t_{EH}	Enable Hold Time [12]	0	—	0	—	0	—	ns
t_{RWS}	Read/Write Setup Time	13	—	15	—	18	—	ns
t_{RWH}	Read/Write Hold Time	0	—	0	—	0	—	ns
t_{RQS}	Request Setup Time [12]	15	—	18	—	21	—	ns
t_{RQH}	Request Hold Time [12]	0	—	0	—	0	—	ns
t_{AS}	Address Setup Time [12]	15	—	18	—	21	—	ns
t_{AH}	Address Hold Time [12]	0	—	0	—	0	—	ns
t_A	Data Output Access Time	—	15	—	20	—	25	ns
t_{ACK}	Acknowledge Access Time	—	17	—	20	—	25	ns
t_{OH}	Output Hold Time	5	—	5	—	5	—	ns
t_{ZX}	Output Enable Time, $\overline{OE}$ LOW to D_0 - D_{35} Low-Z [8]	5	—	5	—	5	—	ns
t_{XZ}	Output Disable Time, $\overline{OE}$ HIGH to D_0 - D_{35} High-Z [8]	—	15	—	20	—	25	ns
t_{EF}	Clock to $\overline{EF}$ Flag Valid (Empty Flag)	—	20	—	25	—	30	ns
t_{FF}	Clock to $\overline{FF}$ Flag Valid (Full Flag)	—	20	—	25	—	30	ns
t_{HF}	Clock to $\overline{HF}$ Flag Valid (Half-Full)	—	20	—	25	—	30	ns
t_{AE}	Clock to $\overline{AE}$ Flag Valid (Almost-Empty)	—	20	—	25	—	30	ns
t_{AF}	Clock to $\overline{AF}$ Flag Valid (Almost-Full)	—	20	—	25	—	30	ns
t_{MBF}	Clock to $\overline{MBF}$ Flag Valid (Mailbox Flag)	—	15	—	20	—	25	ns
t_{PF}	Data to Parity Flag Valid	—	17	—	20	65	25	ns
t_{RS}	Reset/Retransmit Pulse Width [13]	40/25	—	52/30	—	65/35	—	ns
t_{RSS}	Reset/Retransmit Setup Time [9]	20	—	25	—	30	—	ns
t_{RSH}	Reset/Retransmit Hold Time [9]	10	—	15	—	20	—	ns
t_{RF}	Reset Low to Flag Valid	—	35	—	40	—	45	ns
t_{FRL}	First Read Latency [10]	25	—	30	—	35	—	ns
t_{FWL}	First Write Latency [11]	25	—	30	—	35	—	ns
t_{BS}	Bypass Data Setup	15	—	18	—	21	—	ns
t_{BH}	Bypass Data Hold	5	—	5	—	5	—	ns
t_{BA}	Bypass Data Access	—	20	—	25	—	30	ns

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating tor transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions hr extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoot of 1.5V in amplitude is permitted for up to 10ns, once per cycle.
4. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading, and I_{CC} is also dependent on cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.
5. Sample tested only.
6. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0V.
7. Timing measurements performed at 'AC Test Condition' levels.
8. Values are guaranteed by design; not currently production tested.
9. t_{RSS} and/or t_{RSH} need not be met unless a rising edge of CKA occurs while ENA is being asserted, or else a rising edge of CK_A occurs while EN_B is being asserted.
10. t_{FWL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
11. t_{FWL} is the minimum first-read-to-first-write delay, following a full condition, which is required to assure successful writing of data.
12. t_{AS}, t_{AH} address setup times and hold times need only be satisfied at dock edges which occur while the corresponding enables are being asserted.
13. First number used only when CK_A or CK_B is enabled t_{RS} = t_{RSS} + t_{CH} + t_{RSH}.

Functional Description

Reset

The device is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken to LOW state. A reset is required after power up before the first write operation may occur. The MS76542 is fully ready for operation after reset. No device programming is required if the default states described below are acceptable.

A reset operation initializes the read address and write address pointers for FIFO#1 and FIFO#2 to those FIFO 's first memory locations. FIFO and mailbox status flags are updated to indicate an empty condition. In addition, the programmable-status-flag offset values are initialized to eight. Thus the $\overline{AE_1}/\overline{AE_2}$ flag gets asserted within eight locations of an empty condition, and the $\overline{AF_1}/\overline{AF_2}$ flag likewise gets asserted within eight locations of a full condition for FIFO#1/FIFO#2 respectively.

Bypass Operation

During reset (whenever $\overline{RS}$ is LOW) the device acts as a registered transceiver, bypassing the internal FIFO memories. Port A acts as the master port. A write or read operation on Port A during reset transfers data directly to or from Port B. Port B is considered to be the slave, and does not permit write or read operations during reset. The direction of the bypass data transmission is determined by the $R/\overline{W}_A$ control input, which does not get overridden by the $\overline{RS}$ input. The bypass capability may be used to pass initialization or configuration data directly between a master processor and a peripheral device at reset.

Address Modes

Address pins select the device resource to be accessed by each port.Port A has three resource register select inputs, A_{0A}, A_{1A}, and A_{2A}, which select between FIFO access, mailbox register access,flag offset value programming operating mode. Port B has a single address input A_{0B}, to select between FIFO access or mailbox register access. The status of the resource register select inputs is sampled at the rising edge of an enabled clock (CK_A or CK_B). Select input definitions are summarized in Table 1.

Table 1. Resource Register Addresses

A_{2A}	A_{1A}	A_{0A}	RESOURCE
			Port A
H	H	H	FIFO
H	H	L	Mailbox
H	L	H	$\overline{AF_2}$, $\overline{AE_2}$, $\overline{AF_1}$, $\overline{AE_1}$ Flag Offset Registers
H	L	L	Parity Mode Bit
L	H	H	$\overline{AE_1}$ Flag Offset Register
L	H	L	$\overline{AF_1}$ Flag Offset Register
L	L	H	$\overline{AE_2}$ FlagOffset Register
L	L	L	$\overline{AF_2}$ Flag Offset Register
A_{0B}			**RESOURCE**
			Port A
H			FIFO
L			Mailbox

FIFO Write

Port A writes to FIFO #1 and Port B writes to FIFO#2. A write operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held LOW; the FIFO address is selected; and the prescribed setup and hold times must also be observed on the data bus pins D0A - D3A5 or DQB0 - DQB35.

When a FIFO full conditions is reached write operations are locked out. Following the first read operation from a full FIFO, another memory location is freed up and the corresponding Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency (t_{FWL}) after the first read operation from a full FIFO, to ensure that correct read data is retrieved.

FIFO Read

Port A reads from FIFO#2, and Port B reads from FIFO #1. A read operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held HIGH; and the FIFO address is selected; and the prescribed setup and hold times are observed for all of these signals. Read data becomes valid on the data-bus pins by a time tA after the rising clock (CK_A or CK_B) edge, provided that the outputs are enabled.

$\overline{OE}_A$ and $\overline{OE}_B$ are assertive-LOW, asynchronous output enables. Their effect is only to enable or disable the output drivers of the respective Port. Disabling the outputs does not disable a read operation; data transmitted to the corresponding output register will remain available later, when the outputs are again enabled, unless subsequently overwrite.

When an empty condition is reached, read operations are locked out until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the corresponding empty flag ($\overline{EF}$) will be deasserted (HIGH). The first read operation should begin no earlier than a First Read Latency (t_{FRL}) after the first write to an empty FIFO, to ensure that correct read data is retrieved.

Dedicated FIFO Status Flags

Six dedicated FIFO status flags are included for full ($\overline{FF}_1$ and $\overline{FF}_2$), half-full ($\overline{HF}_1$ and $\overline{HF}_2$), and empty ($\overline{EF}_1$ and $\overline{EF}_2$) $\overline{FF}_1$, $\overline{HF}_1$, and $\overline{EF}_1$ indicate the status of FIFO #1; and $\overline{FF}_2$, $\overline{HF}_2$, and $\overline{EF}_2$ indicate the status of FIFO#2.

A full flag is asserted following the rising clock edge for a write operation that fills the FIFO. A full flag is deasserted following the falling clock edge for a read operation to a full FIFO. A half-full flag is updated following the rising clock edge of a read or write operation to a FIFO. An empty flag is asserted following the rising edge for a read operation that empties the FIFO. An empty flag is deasserted following the falling clock edge for a write operation to an empty FIFO.

Programmable Status Flags

Four programmable FIFO status flags are provided, two for almost-full ($\overline{AF}_1$ and $\overline{AF}_2$) and two for almost empty ($\overline{AE}_1$ and $\overline{AE}_2$). Thus, each port has two programmable flags to monitor the status of the two internal FIFO buffer memories. The offset values for these flags are initialized to eight locations from the respective FIFO boundaries during reset, but can be reprogrammed over the entire FIFO depth.

Flag offsets may be written or read through the Port A data bus. All four programmable FIFO status flag offsets can be set simultaneously through a single 36-bit status word; or, each programmable flag offset can be set individually, through one of four 8-bit status words. Table 3 illustrates the data format for flag-programming words.

Mailbox Operation

Two mailbox registers are provided for passing control/status words between ports. Each port can read its own mailbox and write to the other port's mailbox. Mailbox access is performed on the rising edge of the controlling FIFO's clock, with the mailbox address selected and the enable (EN_A or EN_B) HIGH. That is, writing to Mailbox Register#1, or reading from Mailbox Register#2, is the synchronized to CK_A; and writing to Mailbox Register#2, or reading from Mailbox Register#1, is synchronized to CK_B.

The $R/\overline{W}_{A/B}$ and $\overline{OE}_{A/B}$ pins control the direction and availability of mailbox register access. Each mailbox register has its own New-Mail-Alert Flag,which is synchronized to the reading port's clock. These New-Mail-Alert Flags are status indicators only, and cannot inhibit mailbox register read or write operations.

Request Acknowledge Handshake

An optional, synchronous, request-acknowledge handshake feature is provided for each port, to perform boundary synchronization between asynchronously-operated ports. The Request input ($REQ_{A/B}$) is sampled at a rising clock edge. With $REQ_{A/B}$ HIGH, $R/\overline{W}_{A/B}$ determines whether a FIFO read or FIFO write operation is being requested. The Acknowledge output ($ACK_{A/B}$) is updated during the following clock cycle(s).$ACK_{A/B}$ meets the setup and hold time requirements of the Enable input (EN_A or EN_B). Therefore, $ACK_{A/B}$ may be tied back to the enable input to directly gate FIFO accesses, at a slight decrease in maximum operating frequency.

The assertion of $ACK_{A/B}$ signifies that $REQ_{A/B}$ was asserted. However, $ACK_{A/B}$ does not depend logically on $EN_{A/B}$; and thus the assertion of $ACK_{A/B}$ does not prove that a FIFO write access or read access actually did occur. While $REQ_{A/B}$ and $EN_{A/B}$ are being held HIGH, $ACK_{A/B}$ may be considered as a synchronous, predictive boundary flag. That is

$ACK_{A/B}$ acts as a synchronized predictor of the full flag for write operations, or as a synchronized predictor of the empty flag for read operations. Outside the 'almost-empty' region, $ACK_{A/B}$ remains continuously HIGH. Within the 'almost-full' region or the 'almost-empty' region, $ACK_{A/B}$ occurs only on every third cycle, to prevent an overrun of the FIFO's actual full or empty boundaries and to ensure that the t_{FWL} (first write latency) and t_{FRL} (first read latency) specifications are satisfied before $ACK_{A/B}$ is received. The 'almost full region' is defined as that region, where the almost-full flag is being asserted, 'and the 'almost-empty region' as 'that region, where the almost-empty flag is being asserted.' Thus the extent of these 'almost' regions depends on how the system has programmed the offset values for the Almost-Full Flags and the Almost-Empty Flags. If the system has not programmed them, these offset values remain at their default values, eight in each case.

If a write attempt is unsuccessful because the corresponding FIFO is full, or if a read attempt is unsuccessful because the corresponding FIFO is empty, $ACK_{A/B}$ is not asserted in response to $REQ_{A/B}$.

If the REQ/ACK handshake is not used then the $REQ_{A/B}$ input may be used as a second enable input at a possible minor loss in maximum operating speed. In this case the $ACK_{A/B}$ output may be ignored.

WARNING: Whether or not the REQ/ACK hand shake is being used the $REQ_{A/B}$ input for a port must be asserted for the corresponding FIFO to operate.

Data Retransmit

A retransmit operation resets the read-address pointer of the corresponding FIFO(#1 or #2) back to the first FIFO physical location, so that data may be reread. The write pointer is not affected. The status flags are updated;and a block of up to 256 data words, which previously had been written and read from a FIFO, can be retrieved.The block to be retransmitted is bounced by the first FIFO location and the FIFO location addressed by the write pointer. FIFO#1 retransmit is initiated by strobing the $\overline{RT}_1$ pin LOW. FIFO#2 retransmit is initiated by strobing the $\overline{RT}_2$ pin LOW. Read and write operations to a FIFO should be stopped while the corresponding Retransmit signal is being asserted.

Parity Check

The parity Check Flags, $\overline{PF}_A$ and $\overline{PF}_B$, reflect the parity status of the data present on the corresponding port's data bus. The four bytes of a 36-bit word are grouped as D_0 - D_8, D_9 - D_{17}, D_{18} - D_{25}, and D_{26} - D_{35}; the parity of each 9-bit byte is individually checked, and the four single bit parity indications are logically ORed to produce the Parity-Flag output. Parity checking is initialized for odd parity at reset, but can be reprogrammed for even or odd parity during operation.

Word-Width Selection on Port B

The word width of data access on Port B is selected by the WS_1 and WS_0 control inputs. WS_1 is tied HIGH for 36-bit access.WS_1 and WS_0 are both tied LOW for single-byte access. For double-byte access, WS_1 is tied LOW and WS_0 is tied HIGH.

In the single-byte or double-byte access mode, FIFO write operations on Port B pack the data to form 36-bit words when viewed from Port A. Similarly, single-byte or double-byte FIFO read operations on Port B essentially unpack 36-bit words through a series of shift operations. FIFO status flags are updated following the last access which forms a complete 36-bit transfer.

Note that the word-width programming feature is only supported for FIFO accesses.Mailbox and Data Bypass operations do not support word-width

Table 2. Port B Word-Width Selection

WS_1	WS_0	PortB Data Width
H	H	36-Bit
H	L	36-Bit
L	H	18-Bit
L	L	9-Bit

36-BIT Mode (A_{2A}, A_{1A}, A_{0A}) = 1, 0, 1							
D_{34A} - D_{27A}		D_{25A} - D_{18A}		D_{16A} - D_{9A}		D_{7A} - D_{0A}	
X	$\overline{AF}_2$ Offset [1]	X	$\overline{AE}_2$ Offset [1]	X	$\overline{AF}_1$ Offset [1]	X	$\overline{AE}_1$ Offset [1]

8-BIT $\overline{AE}_1$ Flag (A_{2A}, A_{1A}, A_{0A}) = 0, 1, 1		
		D_{7A} - D_{0A}
X...	X	$\overline{AE}_1$ Offset [1]

8-BIT $\overline{AF}_1$ Flag (A_{2A}, A_{1A}, A_{0A}) = 0, 1, 0		
		D_{7A} - D_{0A}
X...	X	$\overline{AF}_1$ Offset [1]

8-BIT $\overline{AE}_2$ Flag (A_{2A}, A_{1A}, A_{0A}) = 0, 0, 1		
		D_{7A} - D_{0A}
X...	X	$\overline{AE}_2$ Offset [1]

8-BIT $\overline{AF}_2$ Flag (A_{2A}, A_{1A}, A_{0A}) = 0, 0, 0		
		D_{7A} - D_{0A}
X...	X	$\overline{AF}_2$ Offset [1]

Parity Mode (A_2, A_1, A_0) = 1, 0, 0 (Write Only)		
D_{0A}		
X...	X	Parity Mode [2]

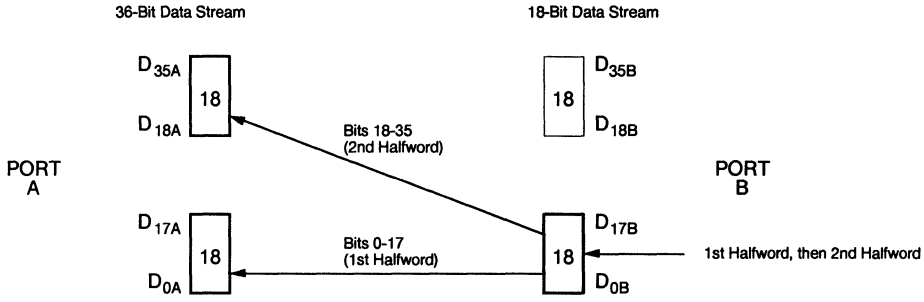
NOTES:
1. All four programmable-flag-offset values are initialized to eight (8) during a reset operation.
2. Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.

Table 3. Flag Programming Words

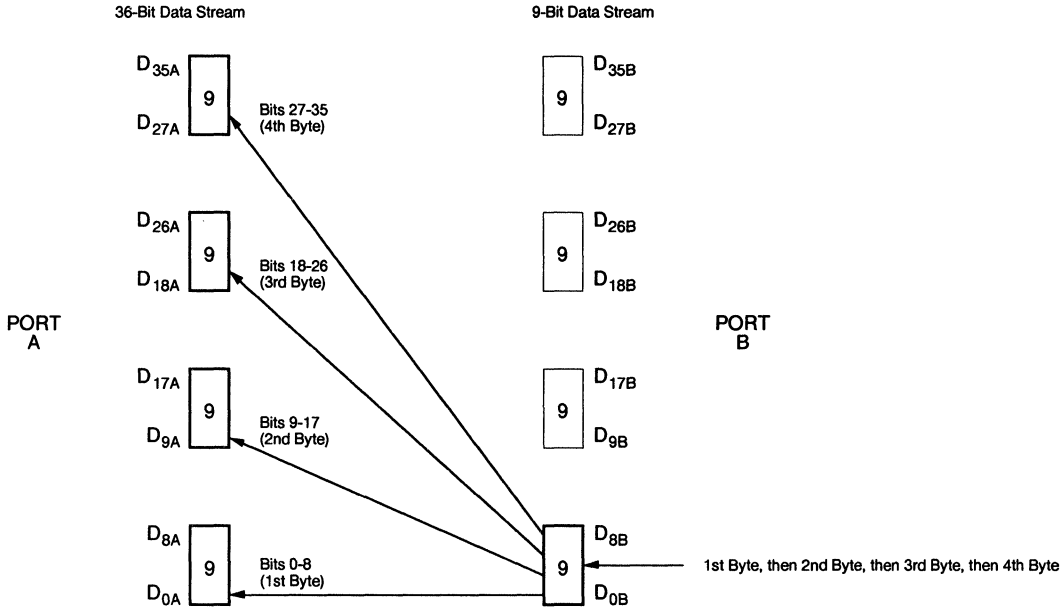
Flag	Valid Read Cycles Remaining				Valid Write Cycles Remaining			
	Flag = Low		Flag = High		Flag = Low		Flag = High	
	Mlin	Max	Mlin	Max	Mlin	Max	Mlin	Max
$\overline{FF}$	256	256	0	255	0	0	1	256
$\overline{AF}$	256-offset	256	0	255-offset	0	offset	offset + 1	256
$\overline{HF}$	129	256	0	128	0	127	128	256
$\overline{AE}$	0	offset	offset + 1	256	256-offset	256	0	255-offset
$\overline{EF}$	0	0	1	256	256	256	0	255

Table 4. Flag Definition Table

Port B Word-Width Selection



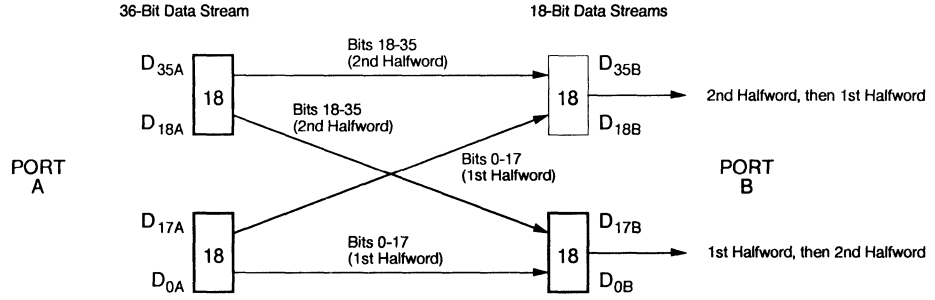
18-to-36 Defunneling Through FIFO #2



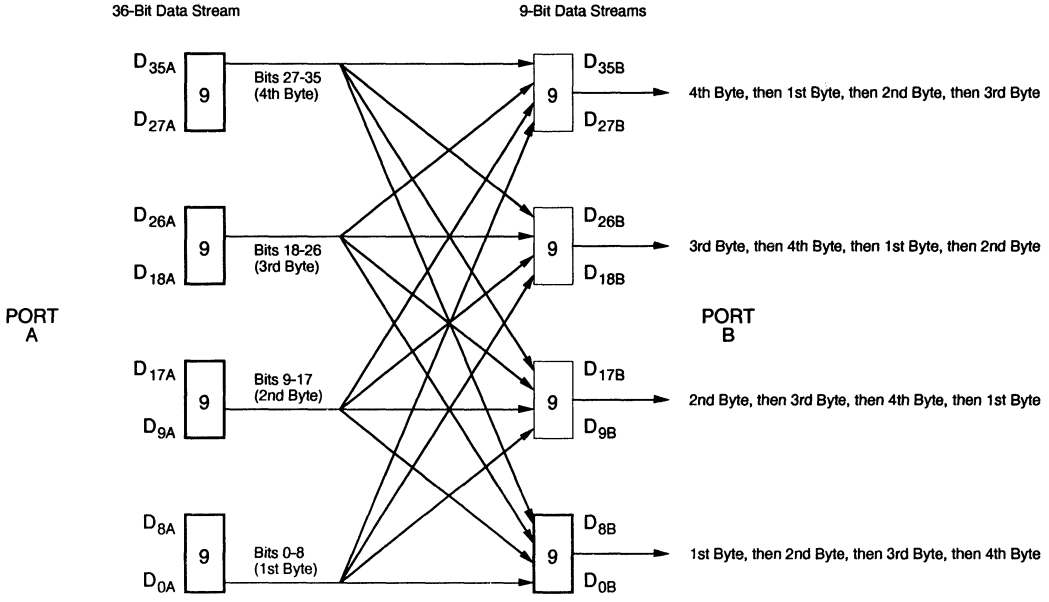
9-to-36 Defunneling Through FIFO #2

NOTES:
1. The heavy black borders on register segments indicate the only data paths used. The other byte segments of Port B do not participate in the data path during defunneling.
2. The defunneling process does not change the ordering of bits within a byte. Halfwords or bytes are transferred in parallel form from Port B to Port A.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attemping to send data. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.

Port B Word-Width Selection

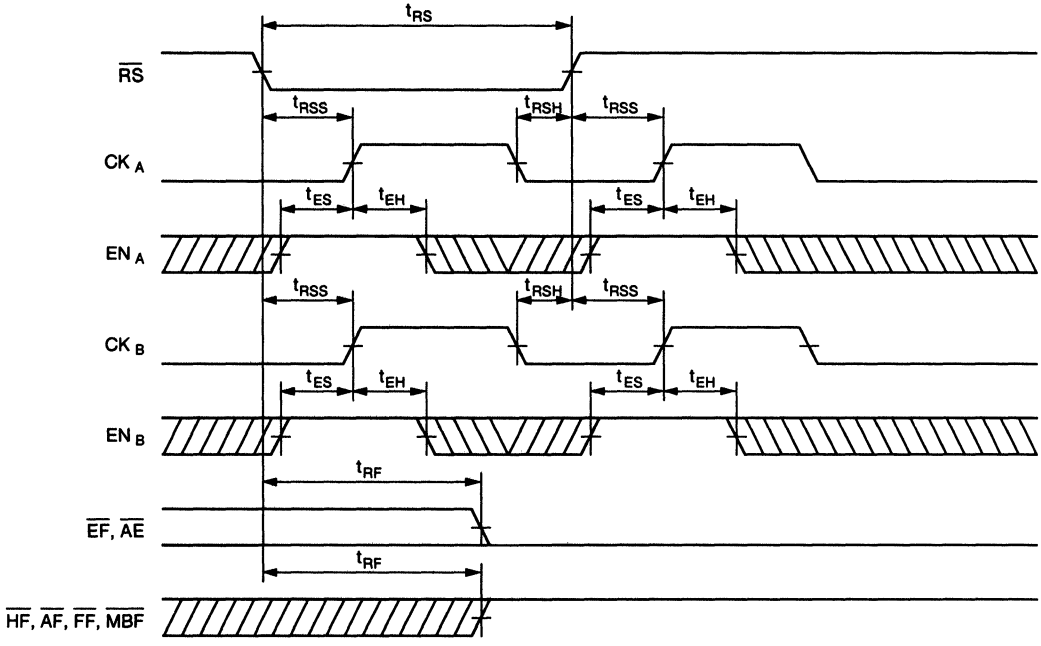


36-to-18 Funneling Through FIFO #1



36-to-9 Funneling Through FIFO #1

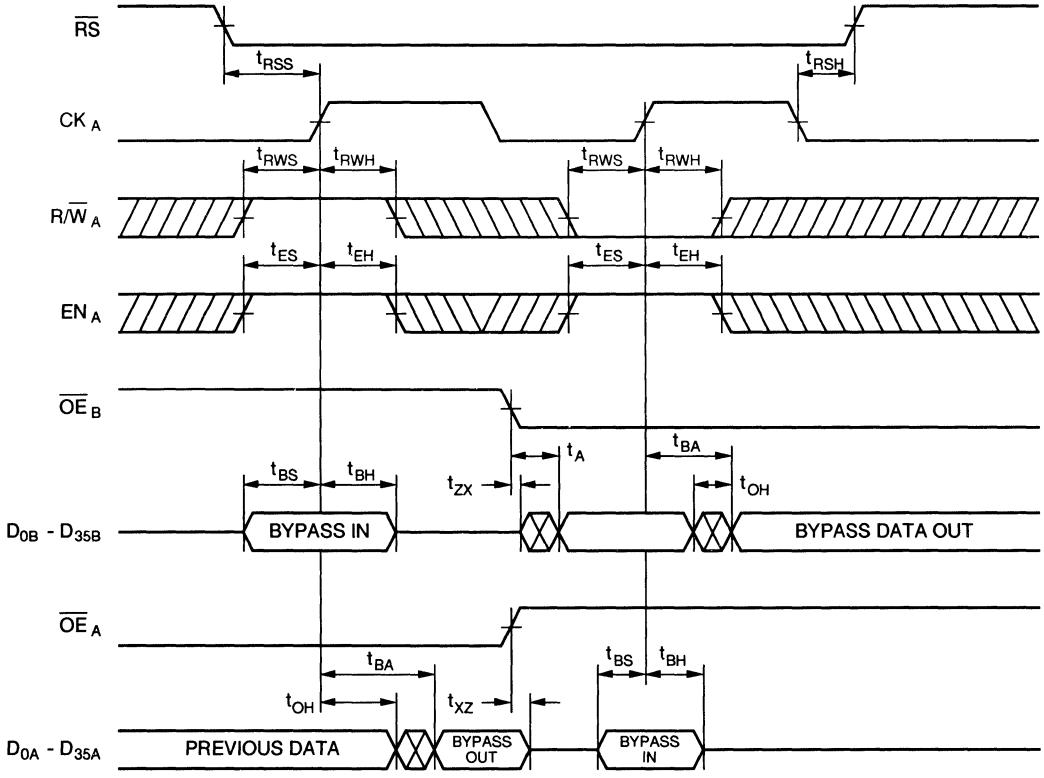
NOTES:
1. The heavy black borders on register segments indicate the main data path, suitable for most applications. Alternate paths feature a different ordering of bytes within a word, at Port B.
2. The funneling process does not change the ordering of bits within a byte. Halfwords or bytes are transferred in parallel form from Port A to Port B.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attemping to read D_{0B} - D_{35B}. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.



Reset Timing

NOTES:

1. $\overline{RS}$ overrides all other input signals, and operates asynchronously. $\overline{RS}$ operates whether or not EN_A and/or EN_B are asserted.
2. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A and/or CK_B occurs while that clock is enabled.
3. The parity check is initialized to odd byte parity at reset.
4. The $\overline{AE}$ and $\overline{AF}$ flag of offsets are initialized to eight locations from the boundary at reset.

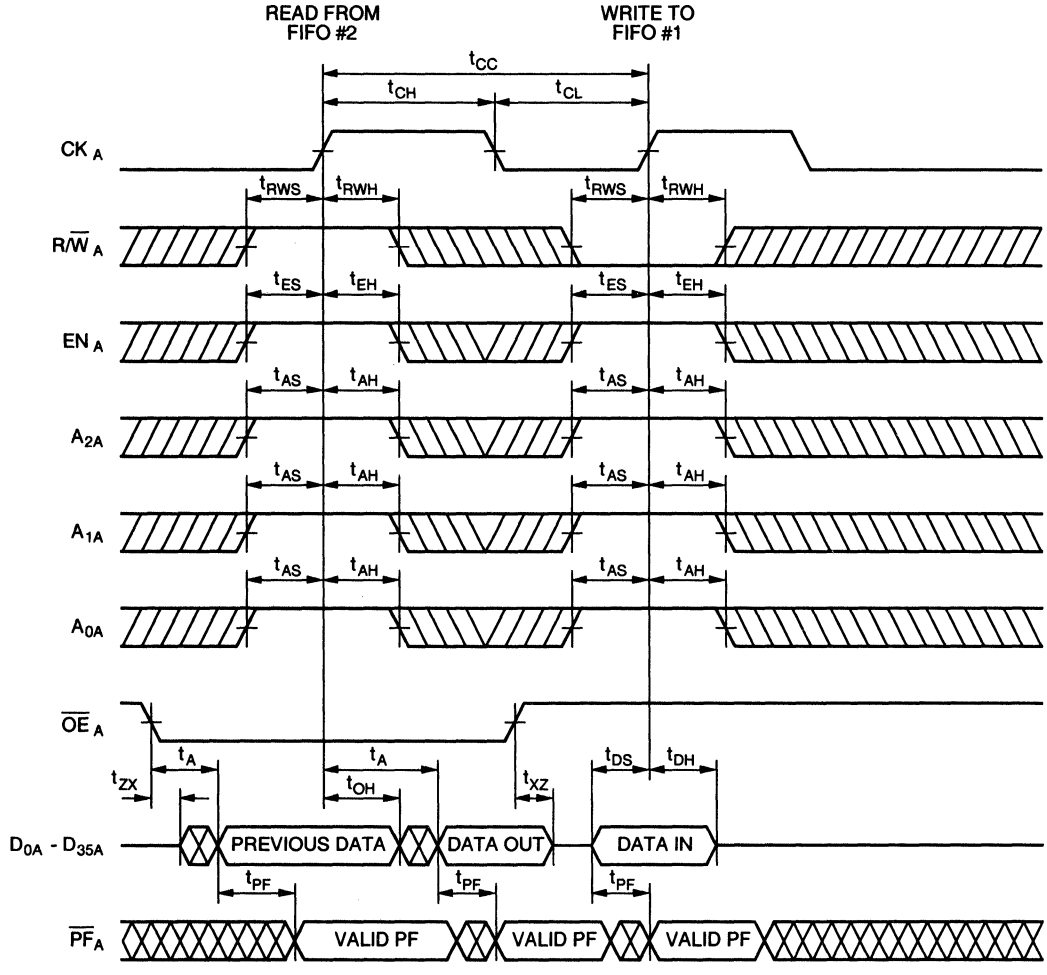


Data Bypass Timing

NOTES:

1. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A, or CK_B occurs while that clock is enabled.
2. Port A is considered the rnaster port for bypass operation. Thus, CK_A, $R/\overline{W}_A$, and EN_A control the transmission of data between ports at reset.

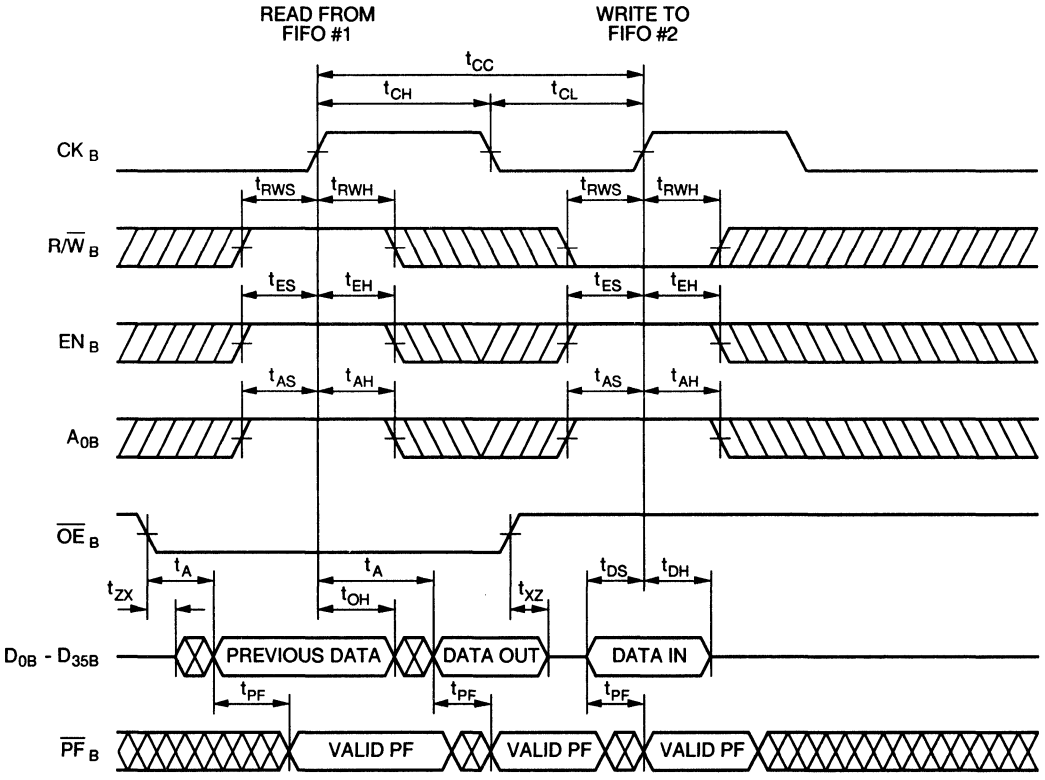
7



Port A FIFO Read/Write

NOTES:

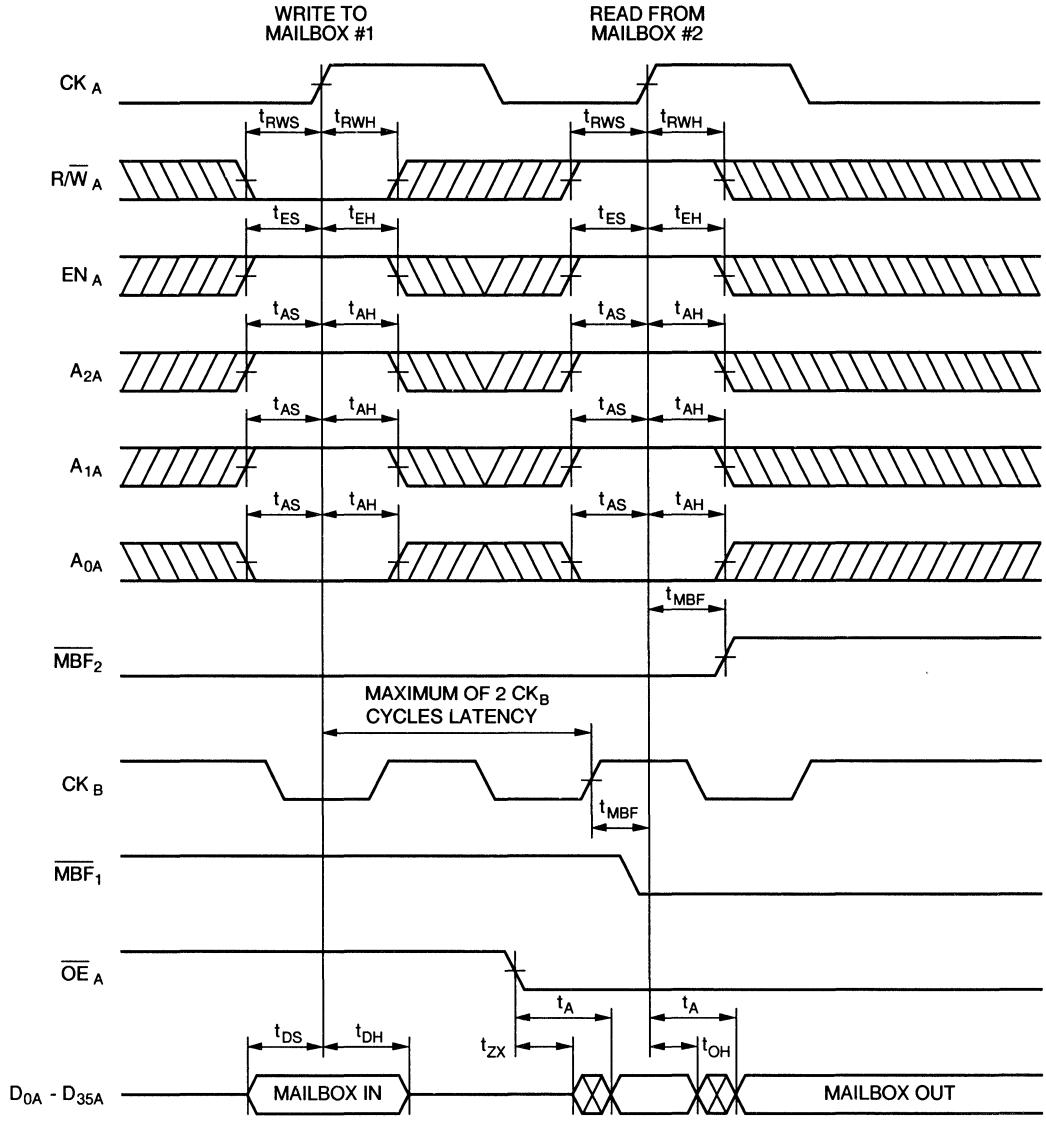
1. The Port A Parity Error Flag ($\overline{PF}_A$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_A$ does not gate read or write operations.
3. If $\overline{OE}_A$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #1.



Port B FIFO Read/Write

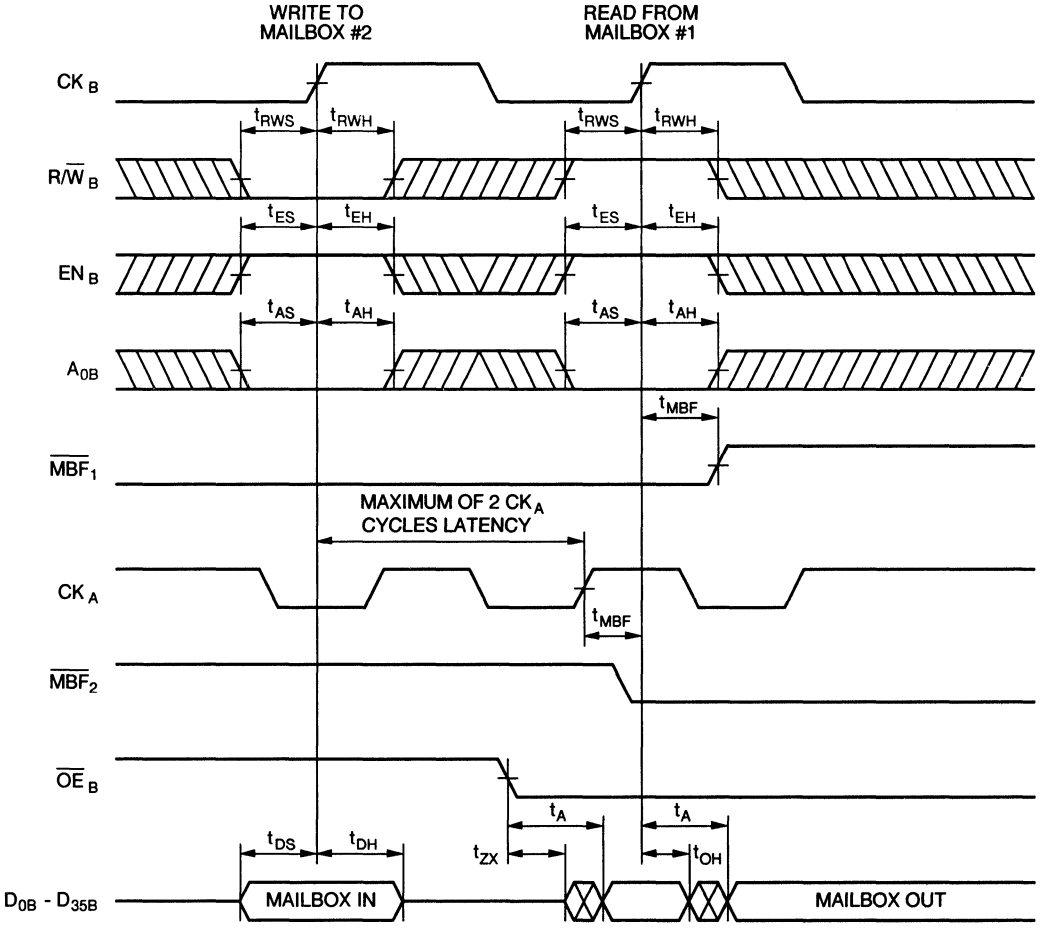
NOTES:
1. The Port B Parity Error Flag ($\overline{PF}_B$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_B$ does not gate read or write operations.
3. If $\overline{OE}_B$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #2.

7



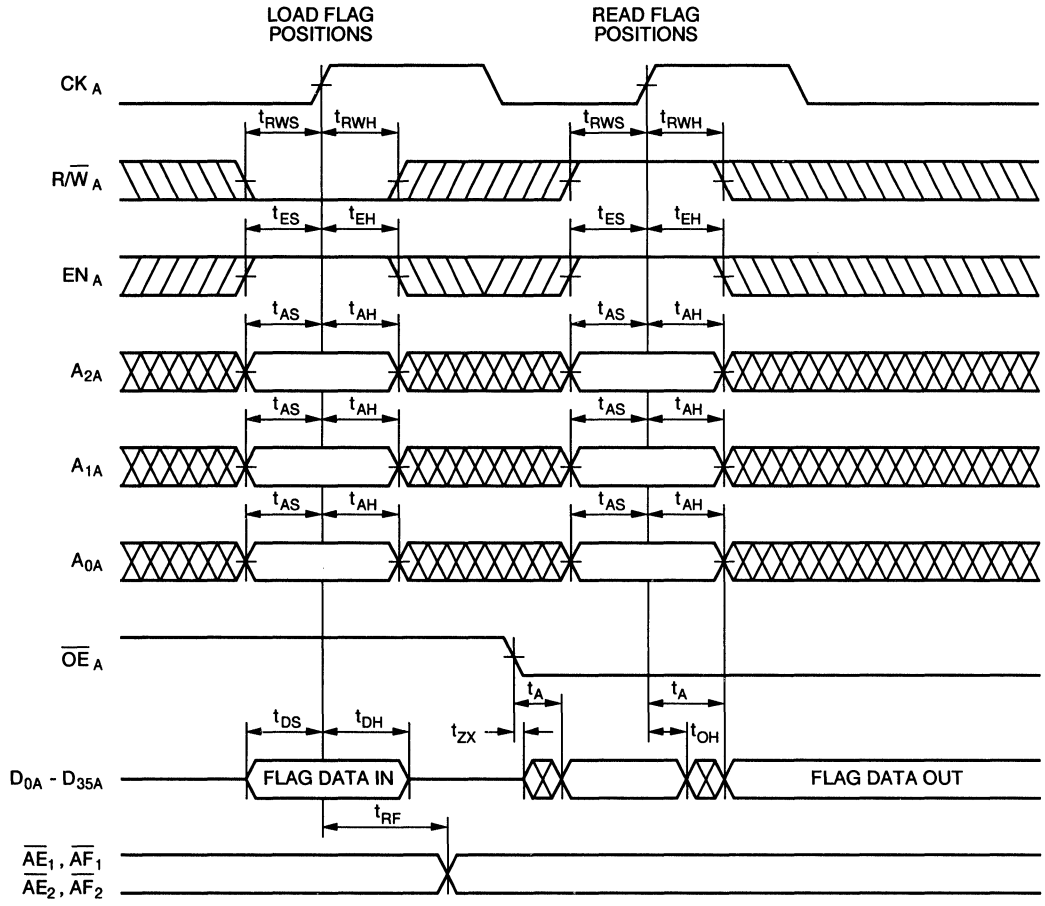
Port A Mailbox Access

NOTES:
1. Both edges ot $\overline{MBF_2}$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF_1}$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of 2 CK_B clock cycles of synchronization latency before $\overline{MBF_1}$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.



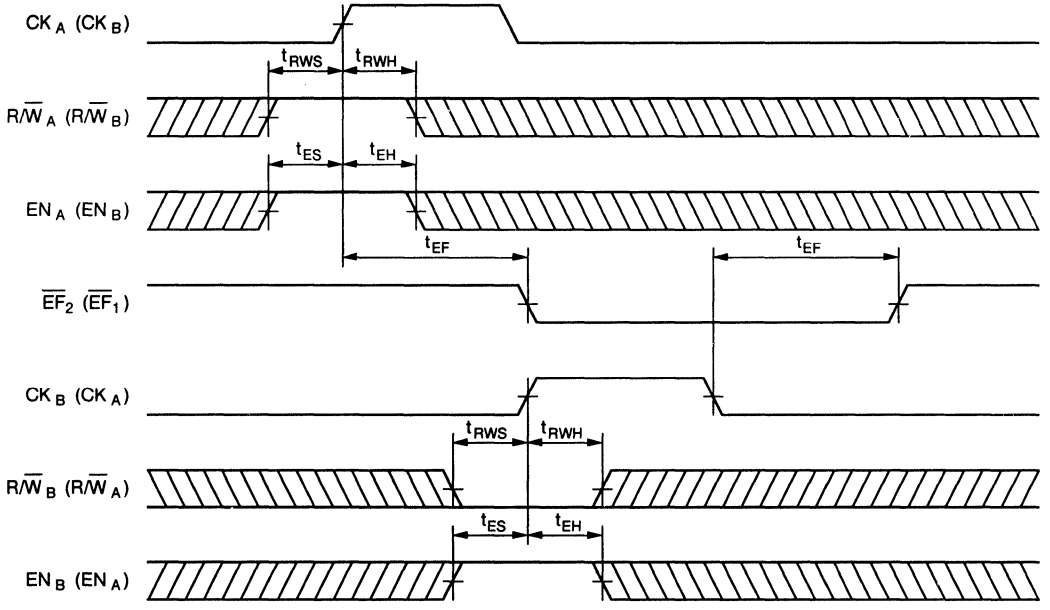
Port B Mailbox Access

NOTES:
1. Both edges ot $\overline{MBF}_2$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF}_1$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of 2 CK_A clock cycles of synchronization latency before $\overline{MBF}_2$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.



Flag Programming

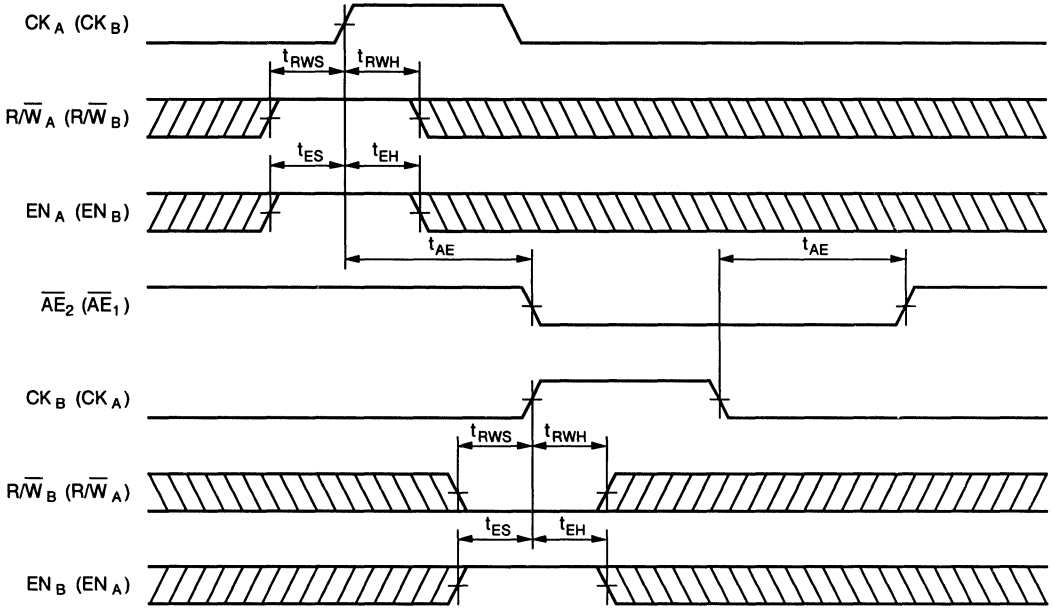
NOTES:
1. For valid flag address codes and data formats, see Table 3.
2. If flag status is altered by flag programming, the updated flags will be valid within a time t_{RF}.



Empty Flag Timing

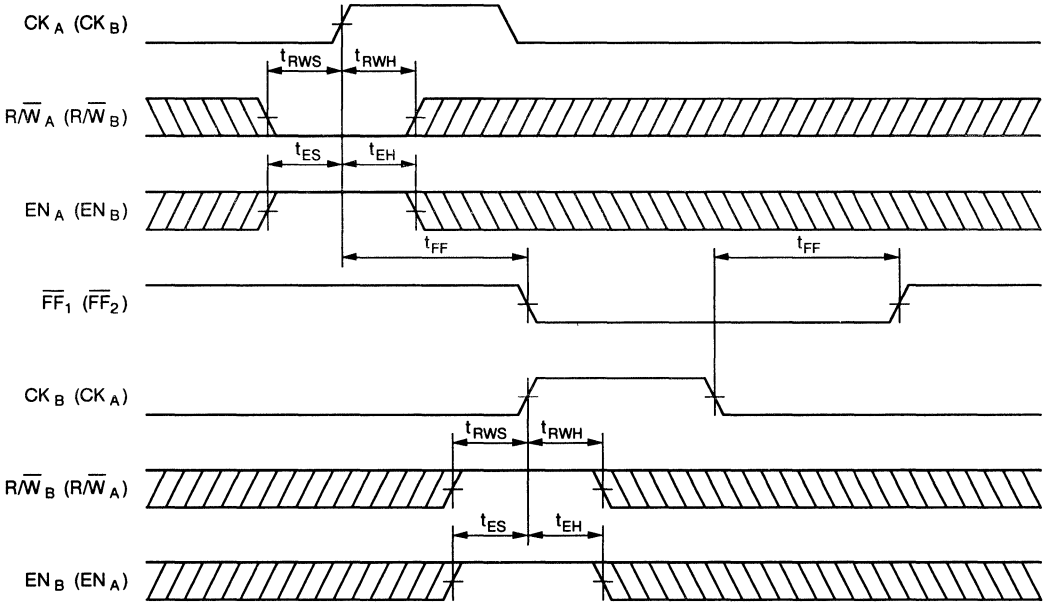
NOTE:
A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all HIGH for FIFO access.

7



Almost-Empty Flag Timing

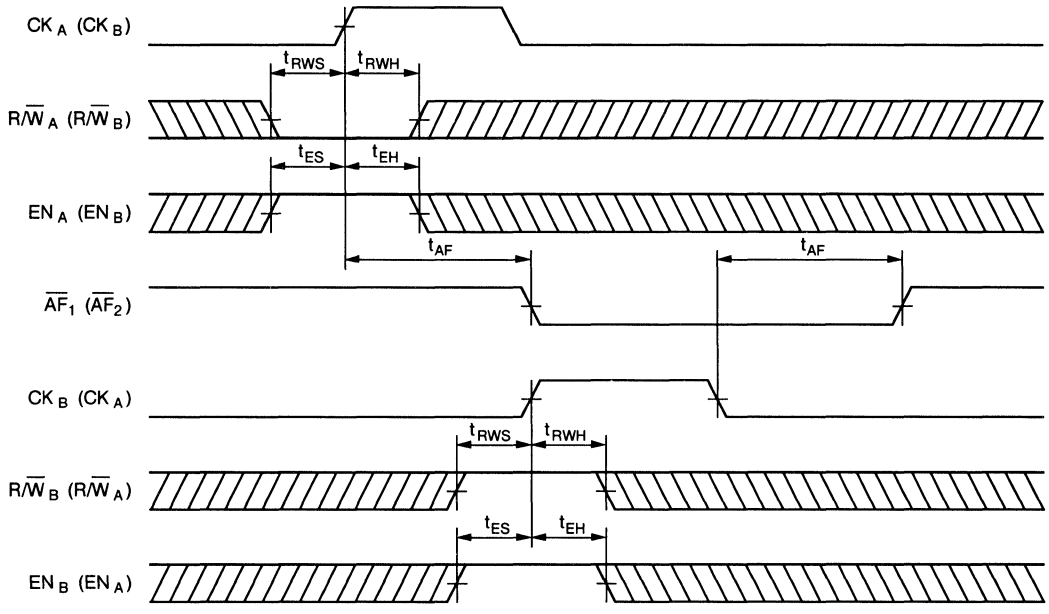
NOTE:
A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all HIGH for FIFO access.



Full Flag Timing

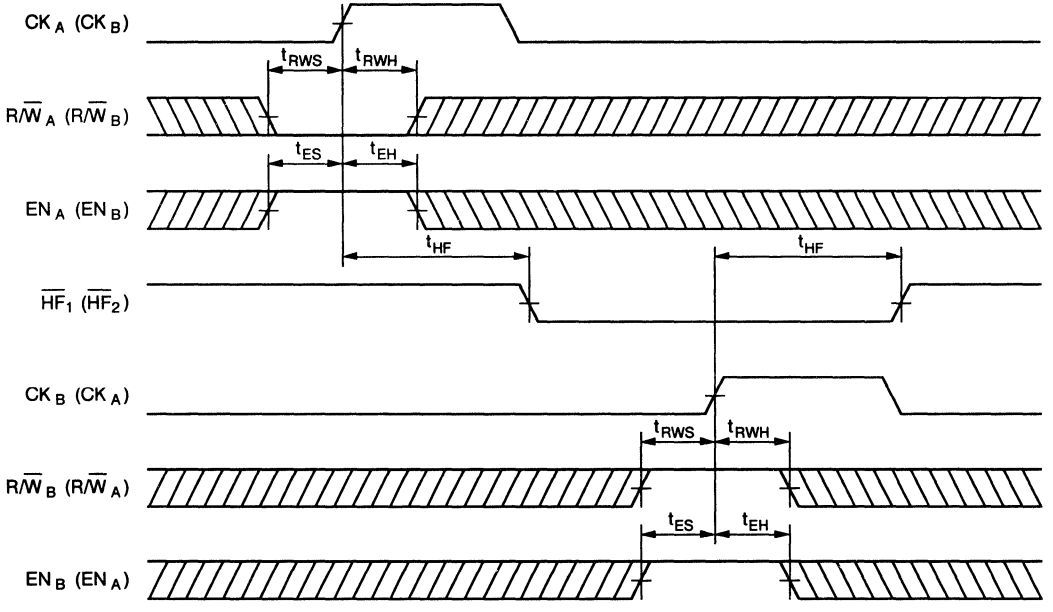
NOTE:
A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all HIGH for FIFO access.

7



Almost-Full Flag Timing

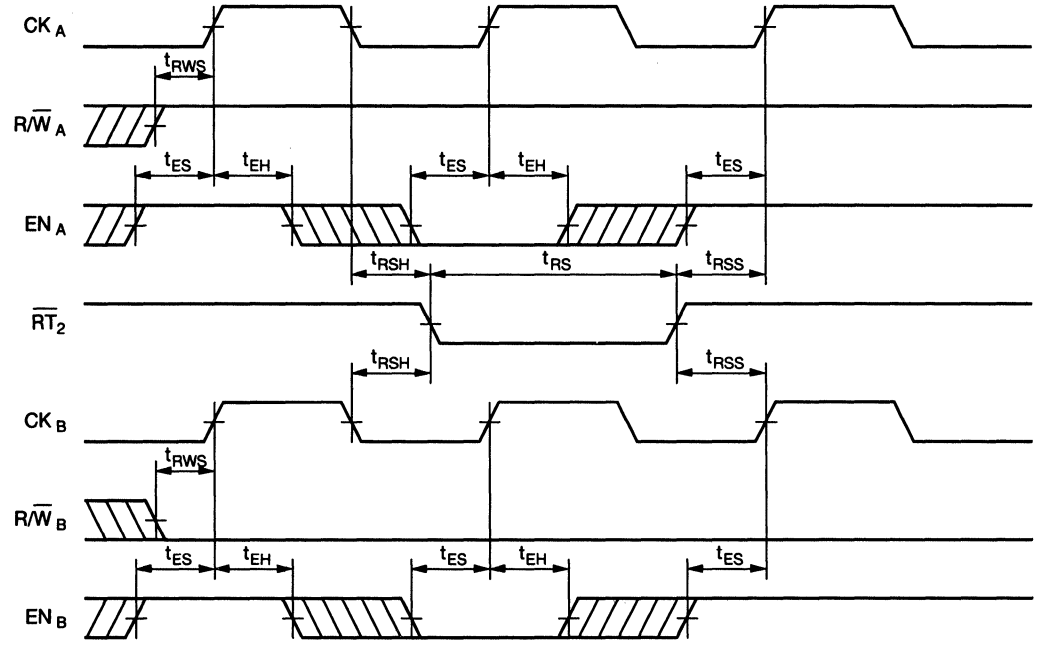
NOTE:
A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all HIGH for FIFO access.



Half-Full Flag Timing

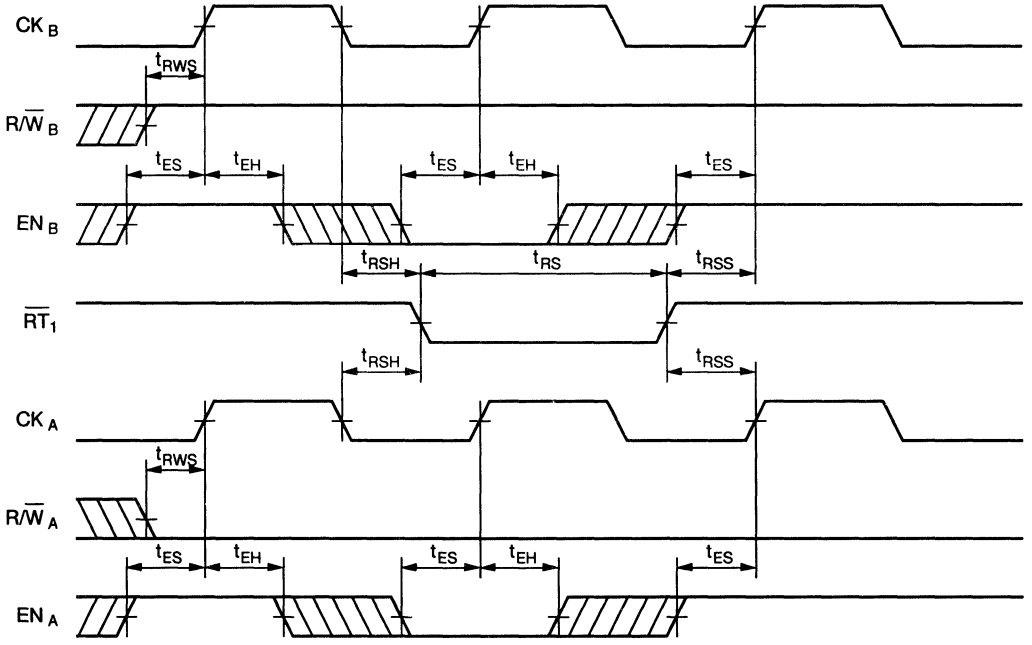
NOTE:
A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all HIGH for FIFO access.

7



FIFO #2 Retransmit

NOTES:
1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_2$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_2$ after a normal FIFO cycle.

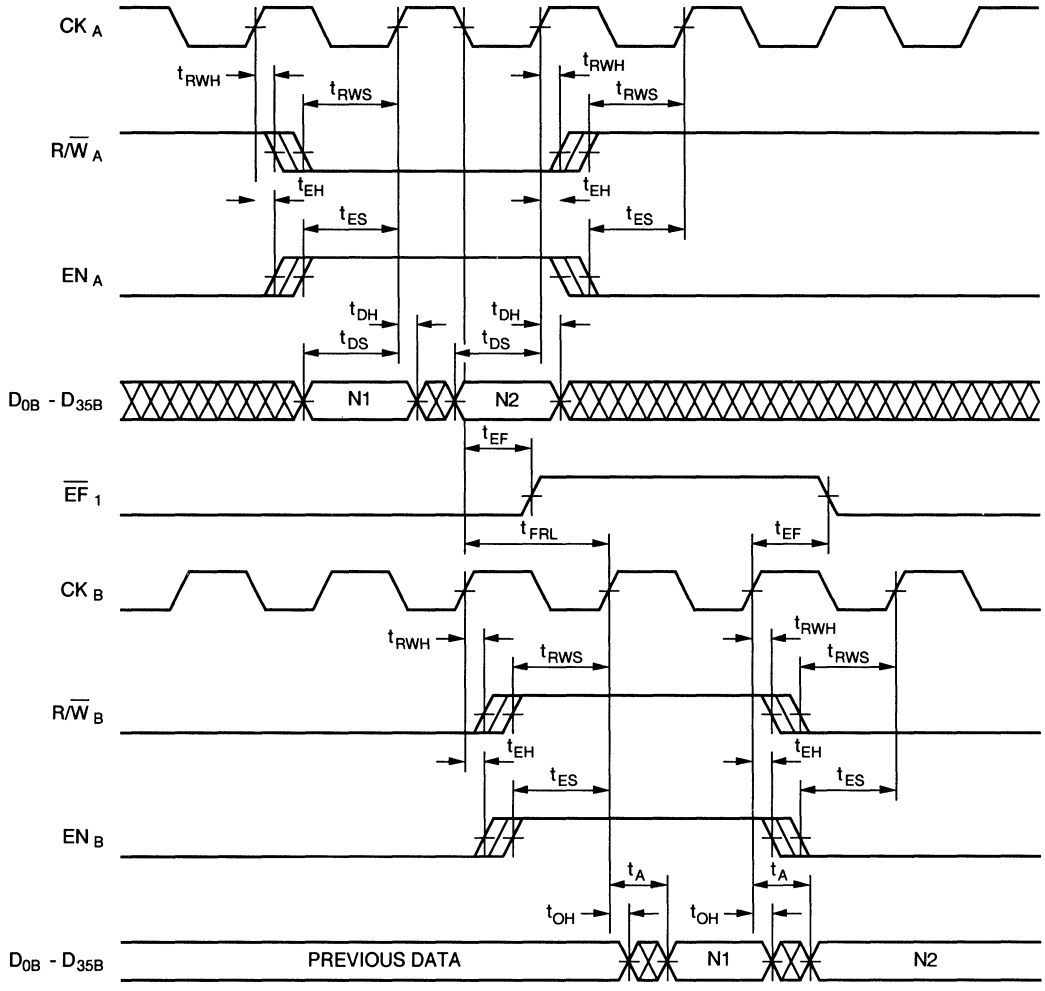


FIFO #1 Retransmit

NOTEs:

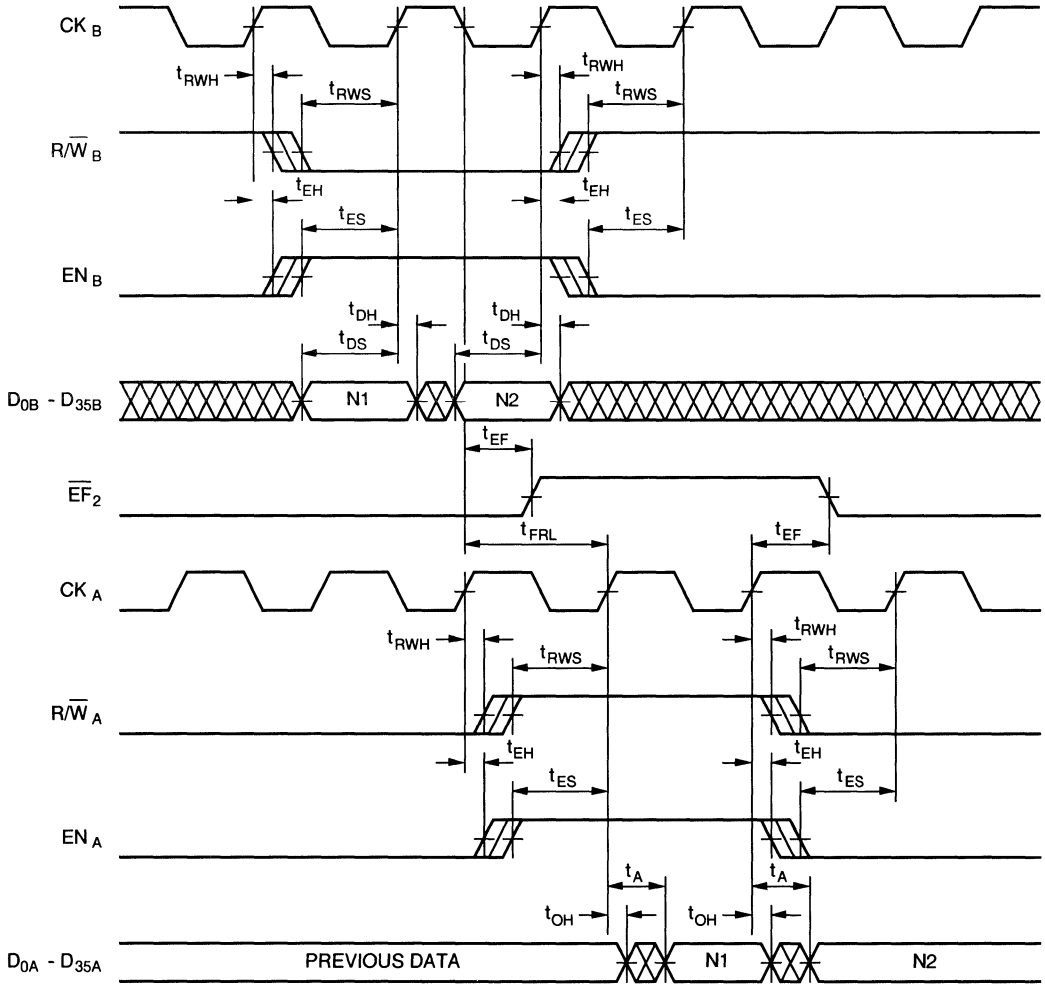
1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_1$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_1$ after a normal FIFO cycle.

7



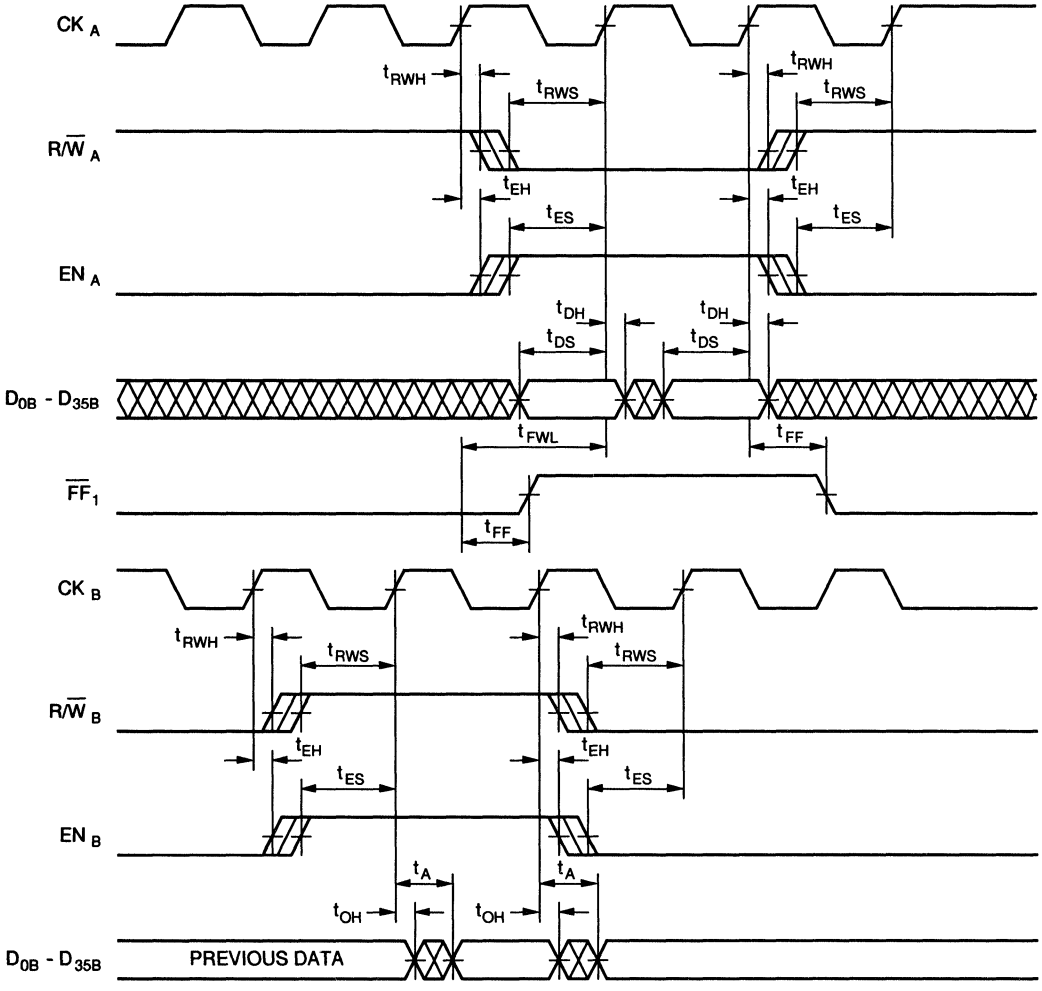
FIFO #1 Write and Read Operation In Near-Empty Region

NOTES:
1. A_{2A}, A_{1A}, A_{0A} and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - the first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.



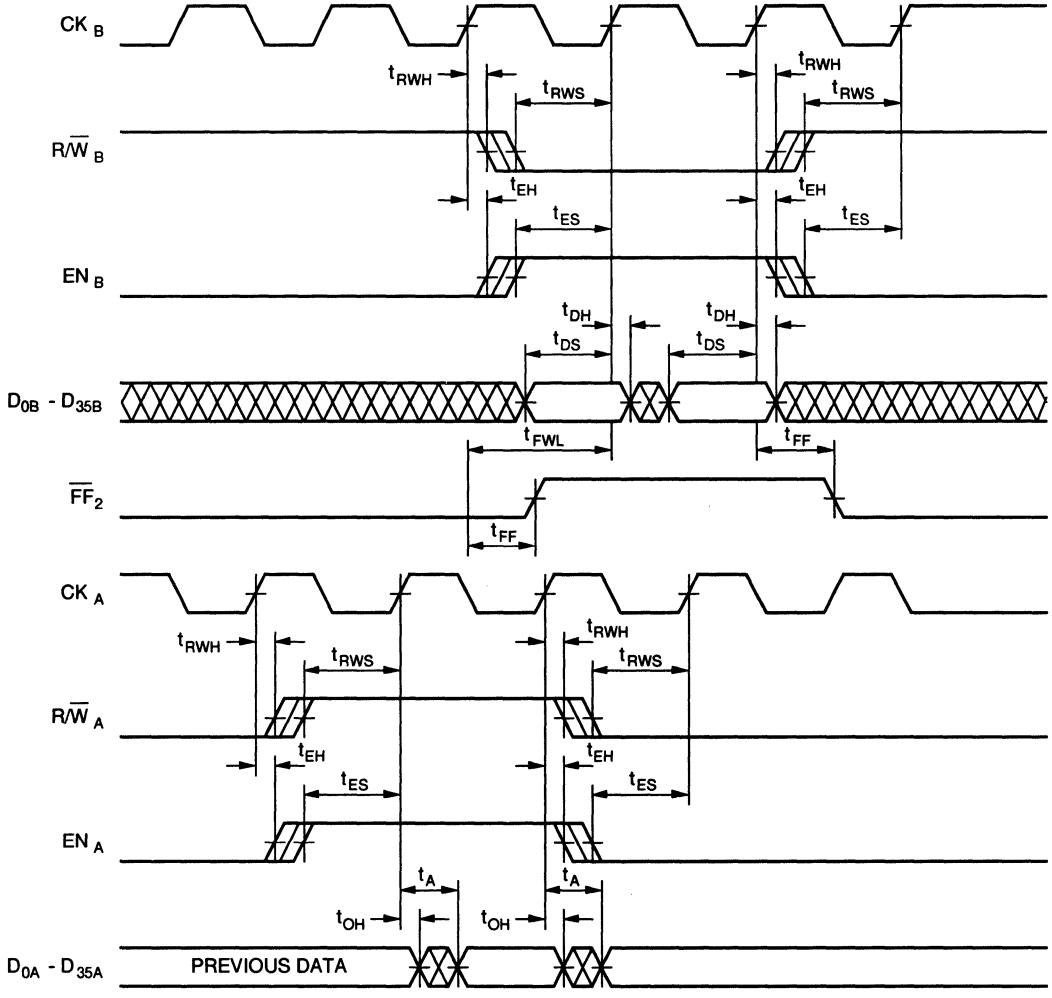
FIFO #2 Write and Read Operation In Near-Empty Region

NOTES:
1. A_{2A}, A_{1A}, A_{0A} and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - the first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.



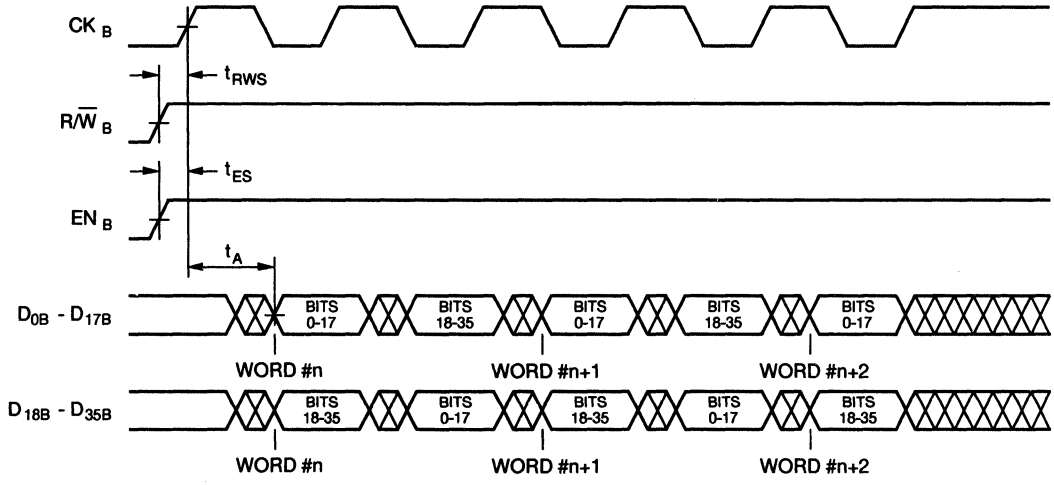
FIFO #1 Read and Write Operation In Near-Full Region

NOTES:
1. A_{2A}, A_{1A}, A_{0A} and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FWL} (First Write Latency) - the first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.



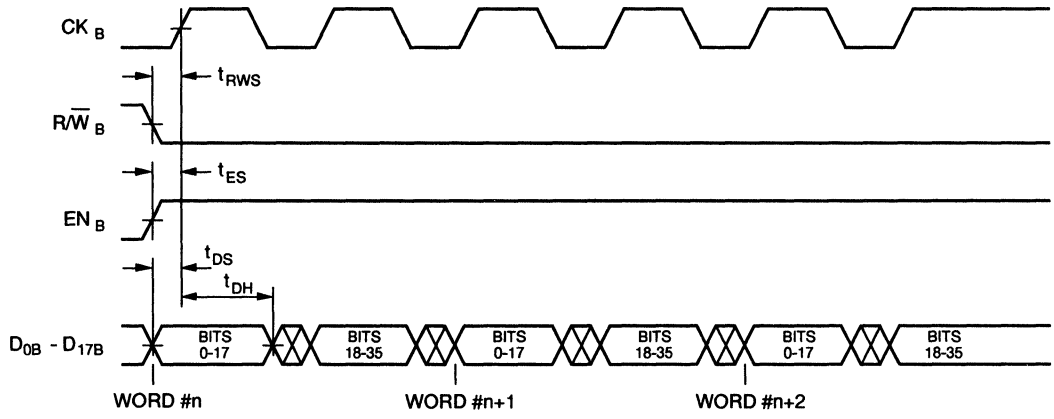
FIFO #2 Read and Write Operation In Near-Full Region

NOTES:
1. A_{2A}, A_{1A}, A_{0A} and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held LOW.
3. $\overline{OE}_B$ is held HIGH.
4. t_{FWL} (First Write Latency) - the first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.



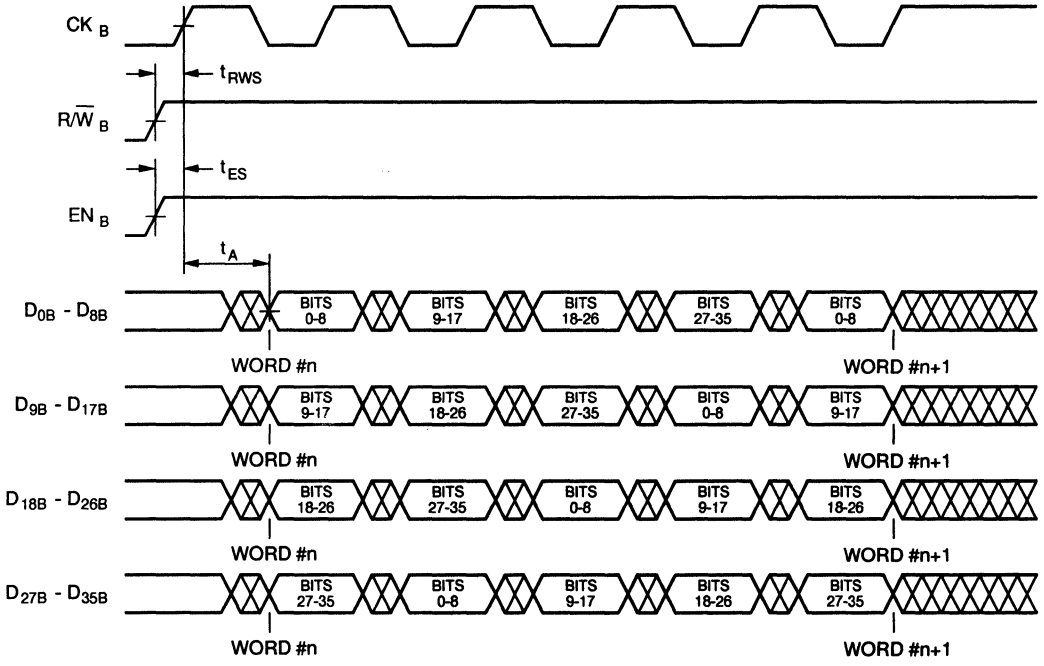
Port B Double-Byte FIFO #1 Read Access for 36-to-18 Funneling

NOTES:
1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.



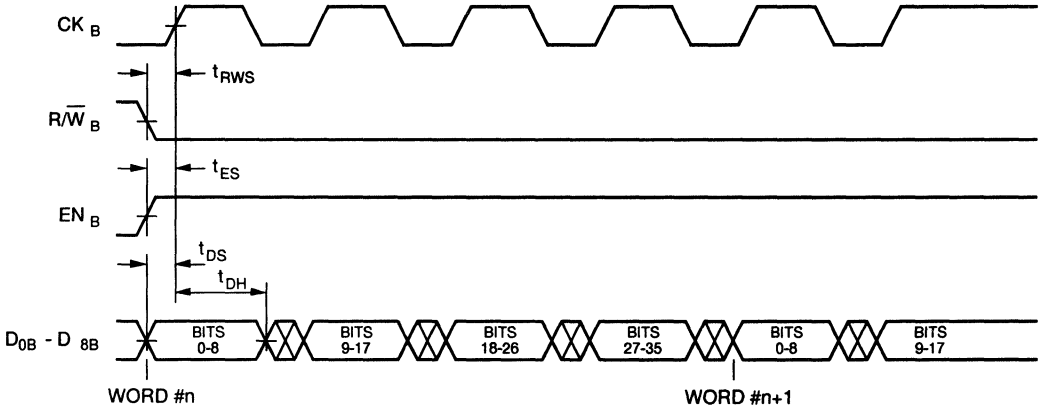
Port B Double-Byte FIFO #2 Write Access for 18-to-36 Defunneling

NOTES:
1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.



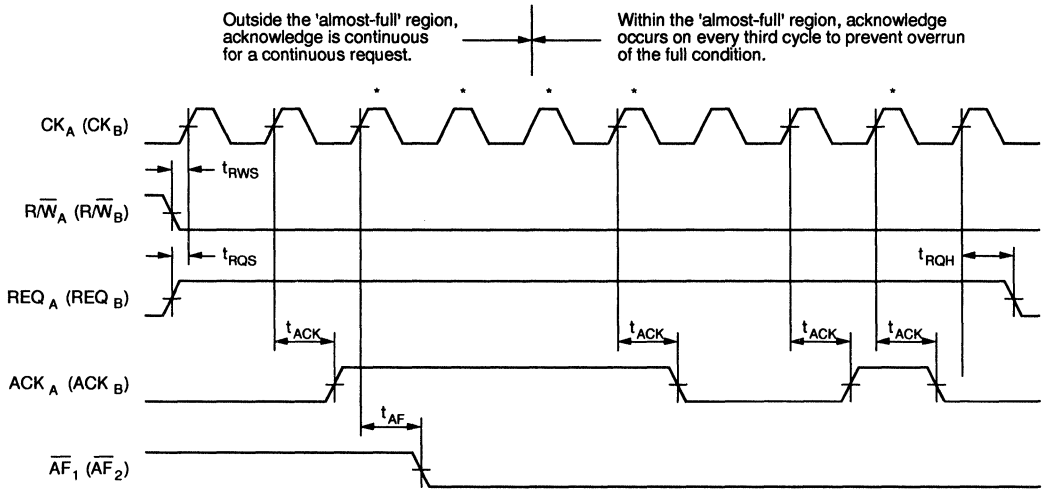
Port B Single-Byte FIFO #1 Read Access for 36-to-9 Funneling

NOTES:
1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held LOW.
3. WS_0 and WS_1 are both held LOW for single-byte access.



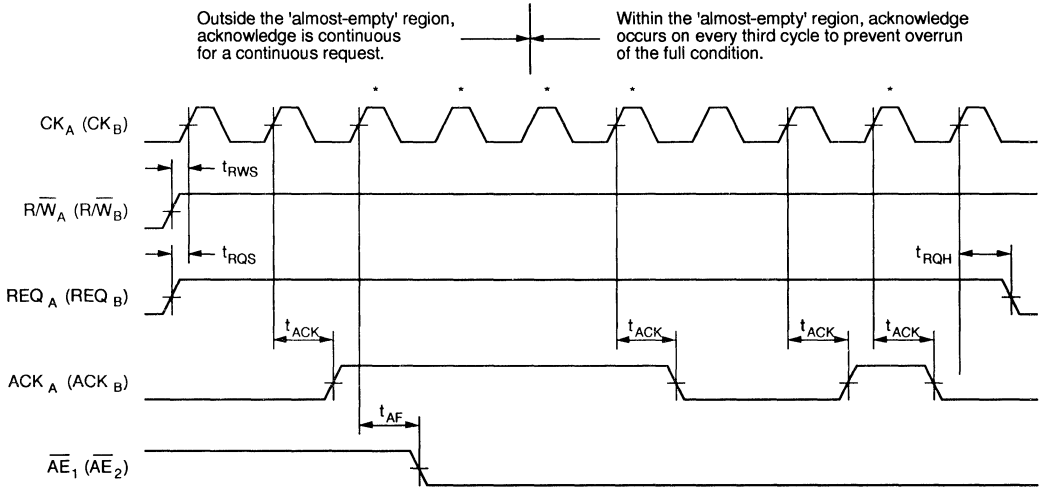
Port B Single-Byte FIFO #2 Write Access for 9-to-36 Defunneling

NOTES:
1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS_0 and WS_1 are both held LOW for single-byte access.



Write Request/Acknowledge Handshake

NOTES:
1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a write would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.



Read Request/Acknowledge Handshake

NOTES:
1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a read would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.

7

Ordering Information

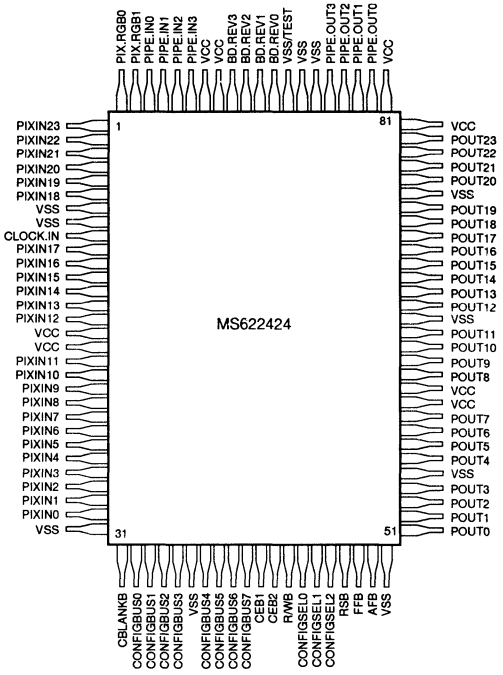
Speed	Ordering Part Number	Package	Temperature Range
25	MS76542-25QC	132 Pin Plastic Flat Pack	0°C to +70°C
30	MS76542-30QC	132 Pin Plastic Flat Pack	0°C to +70°C
35	MS76542-35QC	132 Pin Plastic Flat Pack	0°C to +70°C

MS622424
HIGH PERFORMANCE
8K x 24 BIT
CMOS COLOR MAP

Features

- Color Index Mode supports up to 8192 simultaneous colors out of 16.7 million total colors
- 24-bit RGB Mode allows full true color display
- High-speed operation capable of supporting resolutions up 1280 x 1024
- Available in 100-pin PQFP
- Unique "Write-Buffer" at MPU port permits dualport-like operation using an economical singleport memory core
- All TTL compatible inputs and outputs
- 70 MHz pipelined operation
- Standard MPU Interface

100-pin PQFP PIN CONFIGURATION Top View



Description

The MS622424 is a high performance, full CMOS, 8K x 24, 192K-bit pipelined static memory. This device is specifically designed for use as a color look-up table in high resolution video display systems. When two of these devices are operated in parallel at 70 MHz, the resulting system will be capable of supporting a display of 1280 x 1024 bit mapped color graphics with 13 bits per pixel in the Color Index Mode or 24 bits per pixel in the RGB Mode.

In the Color Index Mode, three internal 8Kx8's provide 8192 simultaneous colors from a 16.7 million color palette. The palette can be partitioned into several smaller palettes thereby supporting multiple window display. In the RGB Mode, the 24-bit input can be gamma corrected on one of three gamma correction tables. The 24-bit gamma corrected value will then be presented at the output.

This device is implemented in full CMOS for low power consumption, and is available in an 100-pin plastic quad-flat-pack.

Pin Descriptions

Pin Name	Description
PIXIN0–PIXIN23	These inputs are latched on the rising edge of CLOCK.IN. The PIXIN0–PIXIN23 can be utilized in two different modes. In the Color Index Mode, PIXIN0–PIXIN12 are used to look up a 24 bit color from a palette of 8192 colors; the higher order bits in this mode are ignored. In the RGB Mode, PIXIN0–PIXIN7, PIXIN8–PIXIN15, and PIXIN16–PIXIN23 will address a red, green, or blue color value, respectively, from the 8K color palette. Internally, the five higher order bits are appended to the 8-bit addresses to compose the necessary 13 bits to address 8K locations. The five appended bits can be one of three values:(1)11101, (2)11110, or (3)11111. These binary addresses are expressed with the most significant bit on the left. The RGB Mode and five higher order bits are determined by the values of PIX.RGB0 and PIX.RGB1.
PIX.RGB0–PIX.RGB1	These two input pins select Color Index Mode or RGB mode. The table below defines the selection associated with the values of these two bits. **PIX.RGB1 PIX.RGB0 SELECTION** 0 0 Color Index Mode 0 1 RGB Mode, 11101 + 8-bit address 1 0 RGB Mode, 11110 + 8-bit address 1 1 RGB Mode, 11111 + 8-bit address These two bits are latched on the rising edge of CLOCK.IN.
PIPE.IN0–PIPE.IN3	These four input pins are provided for the video timing signals such as CBLANKB and CSYNCB. Internally, these signals will go through the same number of pipeline stages as the pixel data. The video timing signals will subseqently appear at the PIPE.OUT outputs, and synchronized with the appropriate color data. These inputs are also latched by the rising edge of CLOCK.IN
CLOCK.IN	This is the clock input pin. The CLOCK.IN controls the latching output and subsequent processing of the pixel data and video timing signals.
POUT0–POUT23	Color information output pins. POUT0–POUT7, POUT8–POUT15, and POUT16–POUT23 are the red, green, and blue color data, respectively.
PIPE.OUT0–PIPE.OUT3	Video timing signals output pins. The output data is synchronized with the color data is output on these pins. Fig. 1 describes internal pipeline data path flow.
CEB1, CEB2	The chip enable input pins. MPU read and write cycles are performed by bringing either of these pins low. The falling edge of this signal latches information from the R/WB, CONFIGSEL, and CONFIGBUS pins.
R/WB	Read and write control input pins. When latched by the falling edge of CEB, this signal determines whether the following operation is a read or a write. A read operation is performed when this signal is high, and a write operation is performed when this signal is low.
CONFIGBUS0–CONFIGBUS7	These pins are used for data I/O. RAM and register data are input and output through these pins. These pins are used for read and write to/from RAM and register.
CONFIGSEL0–CONFIGSEL2	The device configuration input pins. These inputs specify the type of read or write operation to perform. The particular RAM or register operation is defined by the truth table. This information is latched on the falling edge of CEB.
CBLANKB	Blanking status output pin. This signal indicates to the device that a blanking period is taking place so it is therefore permissible to change data in the palette RAM.

Pin Descriptions (Cont'd)

Pin Name	Description
RSB	Reset input pin. This asynchronous system reset initializes state machines and resets the Address, Status, and Color Buffer registers. It also resets the Write FIFO so that it is empty of any contents. It resets command register bits CB2–CB7 and sets bits CB0–CB1. During a reset, CONFIGBUS0–CONFIGBUS7 are in tri-state.
AFB	The FIFO status output pin. This active low output indicates that the Write FIFO is half or almost full. This active low output can be programmed by a bit in the Command Register to indicate that the FIFO is at least half full or is almost full (eight or less empty locations left).
FFB	The FIFO status output pin. This active low output indicates that the Write FIFO is full.
V_{SS}/TEST	This pin should be grounded for normal operation.
BD.REV(0-3)	Board revision input pins. These input pins can be pull-up to V_{DD} or pull-down to V_{SS}. The BD.REV data can be read though the revision register.

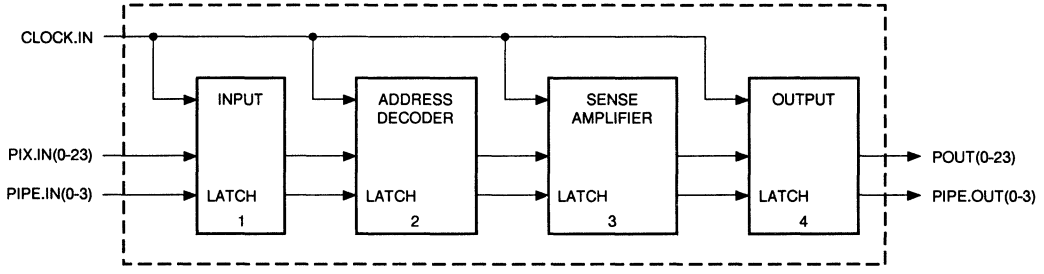
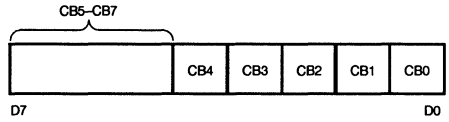


Figure 1. Internal Pipeline Data Path for Pixel and Pipe Input Data

8

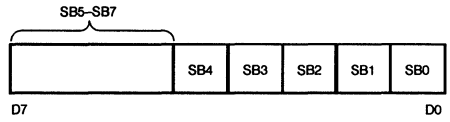
Internal Registers

Command Register ***The Command Register is an 8-bit register.***



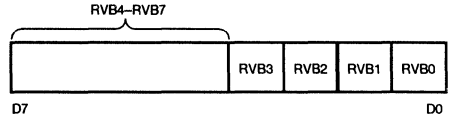
CB0	PIPE.IN0 reset	This bit is internally ANDed with PIPE.IN0 . Thus when CB0 is "0", then PIPE.OUT0 will always be "0"
CB1	PIPE.IN1 reset	This bit is internally ANDed with PIPE.IN1 . Thus when CB1 is "0", then PIPE.OUT1 will always be "0"
CB2	PIPE.IN2 set	This bit is internally ORed with PIPE.IN2 . Thus when CB2 is "1", then PIPE.OUT2 will always be "1"
CB3	PIPE.IN3 set	This bit is internally ORed with PIPE.IN3 . Thus when CB3 is "1", then PIPE.OUT3 will always be "1"
CB4	HFB/AFB	This bit programs the AFB flag indicator. When this bit is "0" the AFB pin will indicate that the FIFO is half full. When this bit is "1" AFB will indicate almost full.
CB5–CB7	Reserved	Reserved for internal use.

Status Register ***The Status Register is an 8-bit register.***



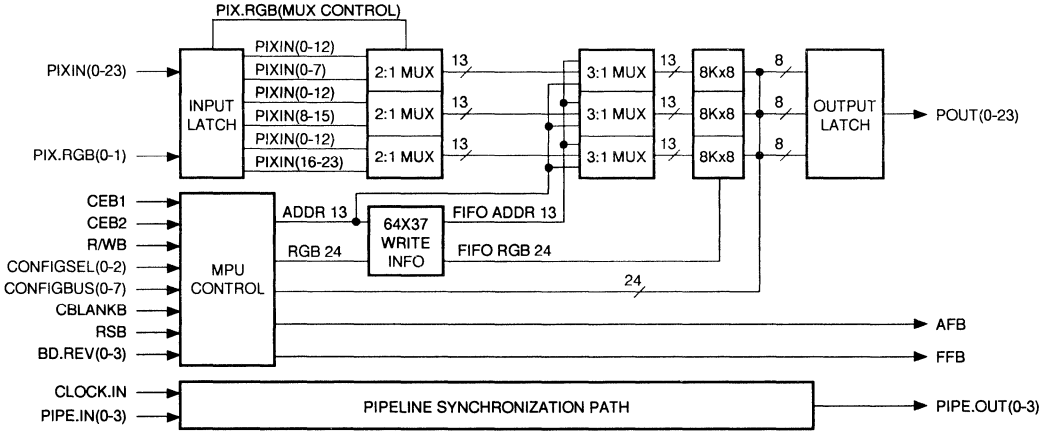
SB0	RGB0	LSB of RGB counter. RGB0 and RGB1 form two bits of a modulo three counter that determines which color is operated on(read only).
SB1	RGB1	MSB of RGB data counter(read only).
SB2	EFB	Empty Flag; Write FIFO is empty when this bit is low.
SB3	HFB/AFB	Half or Almost-Full Flag; Like the external AFB pin, this bit can be programmed by CB4 to indicate that the Write FIFO is at least half full or at least 7/8 full (eight or fewer empty locations left).
SB4	FFB	Full Flag; Write FIFO is full when this bit is low.
SB5–SB7	Reserved	Reserved for internal use.

Revision Register ***The Revision Register is an 8-bit register.***



RVB0	REV0	LSB of Revision Register. This register is mask programmed to indicate the revision number.
RVB1	REV1	Second bit of Revision Register.
RVB2	REV2	MSB of Revision Register.
RVB3	Reserved	Reserved for internal use.
RVB4–RVB7	REV4–7	Corresponds to board revision input BD.REV0–3

Functional Block Diagram



Functional Description

MPU Interface

The MPU interface allows the MPU to access the internal registers and the color map. The CONFIGSEL0–CONFIGSEL2 bits that are latched on the falling edge of CEB define the access mode. The access modes are defined in the table below. The R/WB pin is also latched on the falling edge of CEB and indicates a read operation when high and a write operation when low. These functions are illustrated in the truth table on the next page.

The RGB0 and RGB1 bits are the two bits of a modulo 3 counter, which determine which color(red, green, or blue, in that order) is selected. These two bits are reset by a write to either the high or low Address Register. In writes and reads to and from the color palette, the Address Register is incremented at the end of the RGB cycle.

During a read from the color palette, the color data output at POUT0–POUT23 may be disturbed because the address register will take over addressing of the color map. To prevent random color data from being displayed on the screen, the data at POUT0–POUT23 will be held at the value defined by the last valid pixel address for the duration of the read. A read of tne color palette should not be performed while the Write FIFO is not empty because it may contend with the FIFO to color map write. It is recommended that FIFO empty flag status always be checked before issuing color palette read instructions. If such a contention occurs, then the color palette read will interrupt the write cycle.

MPU Access Modes

CONFIGSEL<2:0>	MODE
000	Address Register low (R/W)
001	Address Register high (R/W)
010	Color Palette Buffer (R/W)
011	Command Register (R/W)
100	Status Register (read only)
101	Color Buffer Register (read only)
110	Revision register (read only)
111	Reserved

Write FIFO

The Write FIFO stores data and addresses that are written to the Color Palette Buffer and Address Registers. The FIFO is emptied by writing the data to the color map during a blanking period as indicated by CBLANKB. The host can write up to 64 locations that contain a 13-bit address and a 24-bit color before the FIFO becomes full. When the FIFO is full the full flag pin (FFB) goes low until at least one location of the FIFO is transferred to the color map. If the host attempts to write to the Color Palette Buffer while the FFB is active, then the device will transfer 4 locations from the FIFO to the color map in order to make room for the incoming data, regardless of the state of CBLANKB. This process may disturb the data in the pixel stream. To prevent random color data from being displayed on

Truth Table

R/WB	CONFIGSEL<2:0>	RGB1	RGB0	FUNCTION
0	000 0	x	x	Write Address Register Low, reset RGB Counter
0	001 1	x	x	Write Address Register High, reset RGB Counter (1)
0	010 2	0	0	Write Red Color Palette Buffer, increment RGB counter
0	010 2	0	1	Write Green Color Palette Buffer, increment RGB counter
0	010 2	1	0	Write Blue Color Data to Write FIFO, transfer register contents to Write FIFO, reset RGB counter, increment Address Register
0	011 3	x	x	Write Command Register
0	100 4	x	x	Invalid Operation
0	101 5	x	x	Invalid Operation
0	110 6	x	x	Invalid Operation
0	111 7	x	x	Invalid Operation
1	000 0	x	x	Read Address Register Low
1	001 1	x	x	Read Address Register High (2)
1	010 2	0	0	Read Red Color Palette, increment RGB counter (3)
1	010 2	0	1	Read Green Color Palette Buffer, increment RGB counter
1	010 2	1	0	Read Blue Color Palette Buffer, reset RGB counter, increment Address register
1	011 3	x	x	Read Command Register
1	100 4	x	x	Read Status Register
1	101 5	0	0	Read Red Color Buffer Register, increment RGB counter
1	101 5	0	1	Read Green Color Buffer Register
1	101 5	1	0	Invalid Operation
1	110 6	x	x	Read Revision Register
1	111 7	x	x	Invalid Operation

NOTE:
1. Only CONFIGBUS0–CONFIGBUS4 are recognized; the upper three bits are ignored.
2. Data is output to CONFIGBUS0–CONFIGBUS4 only. The upper three bits will output "0".
3. Reading the Red Color Palette may disturb the pixel stream.

the screen while the device performs these 4 writes, the data at POUT0–POUT23 will be held at the value defined by the last valid pixel address. When Pixel clock is much slower that 70 MHz, the operating frequency of MPU should also be slowed down accordingly in order to maintain the synchronization of FIFO operations

Color Buffer Register

The Color Buffer Register stores the red and green data that is written to the Color Palette Buffer. Thus if a complete red, green, blue write cycle is not completed(register data is not transferred to the Write FIFO), then the host can recover the red and green data it has written by reading the red and green Color Buffer Registers.

The host can recover the red and green data by first writing to the address register to reset the RGB counter. Then the red and green data can be recovered in two consecutive reads of the Color Buffer Register.

Absolute Maximum Ratings*

Symbol	Parameter	Rating	Units
V_{DD}	Supply Voltage	–0.5* to +7.0	V
V_T	Terminal Voltage with Respect to V_{SS}	–0.5* to V_{DD} +0.5	V
P_D	Power Dissipation 100% Duty Cycle	TBD	W
t_{OPR}	Operating Temperature	–10 to +85	°C
t_{STG}	Storage Temperature	–65 to +150	°C

*Note: Operation above absolute maximum rating can affect device reliability.

Capacitance*

T_A = 25°C, f = 1 MHz

Symbol	Parameter	Typ.	Max.	Unit
C_{IN}	Input Capacitance (V_{IN} = 0V)		5	pF
C_{OUT}	Output Capacitance (V_{OUT} = 0V)		8	pF

*Note: These parameters are sampled and not 100% tested.

Recommended DC and Operating Characteristics (1)

T_A = 0°C to 70°C, V_{DD} = 5.0V ± 5%, V_{SS} = 0V, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Units	Test Condition
V_{DD}	Supply Voltage	4.75	5.25	V	
V_{SS}	Supply Voltage	0.0	0.0	V	
V_{IH}	Input High Voltage	2.2	V_{DD}+.3	V	
V_{IL}	Input Low Voltage	–0.5*	+0.8	V	
I_{LI}	Input Leakage Current	–10	10	µA	V_{DD} = 5.25V, V_{IN} = V_{SS} to V_{DD}
I_{LO}	Output Leakage Current	–10	10	µA	V_{OUT} = V_{SS} to V_{DD}
I_{DD}	Dynamic Operating Current		300	mA	Outputs Open, f = fmax
V_{OL}	Output Low Voltage		0.4	V	Active Outputs Open, I_{OL} = 4.0 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = –1.0 mA

NOTE: 1. –3.5V for 20 ns pulse.

AC Test Loads

Signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0.0V to 3.0V, output loading as shown in the diagram below.

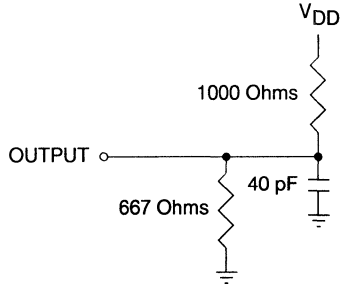


Figure 2. Output Load

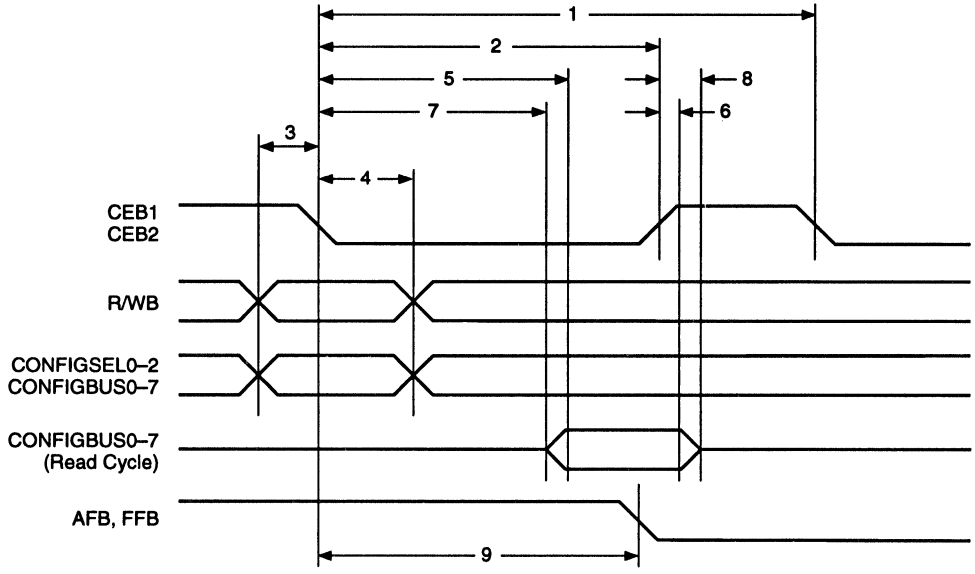
AC Test Conditions

(Applies to READ and WRITE Cycle Timing)

Input Pulse High Level	V_{IH} = 3.0V
Input Pulse Low Level	V_{IL} = 0.0V
Input Rise Time	t_R = 3 ns
Input Fall Time	t_F = 3 ns
Input and Output Reference Level	1.5V
Output Load	C_L = 40pF, 1 TTL
V_{DD}	5V ± 5%
T_A	0° to +70°C

8

Timing Waveforms of MPU Cycle



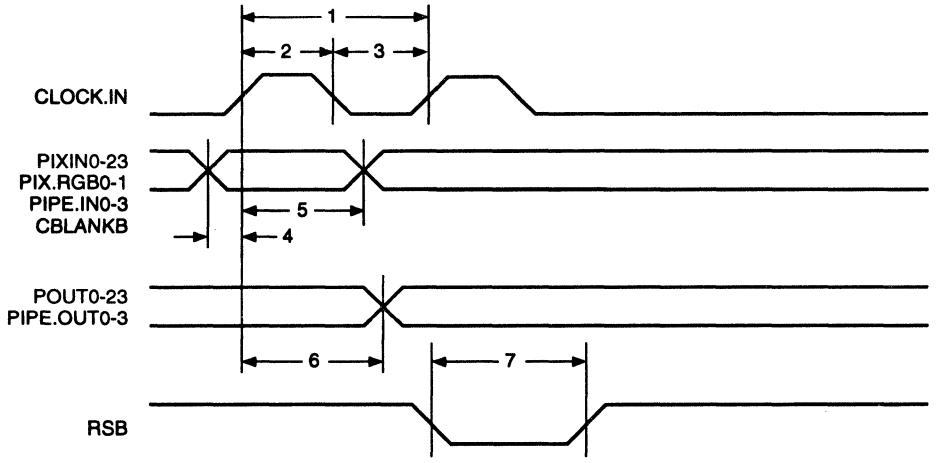
AC Characteristics

At recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
1	CEB Cycle Time	75			ns	
2	CEB Pulse Width	55			ns	
3	CONFIGSEL/BUS and R/WB Set-up before CEB low	0			ns	
4	CONFIGSEL/BUS and R/WBHold after CEB low	10			ns	
5	CONFIGBUS Data Access			55	ns	
6	CONFIGBUS Data Hold	5			ns	
7	CEB low to CONFIGBUS Lo-Z	10			ns	2, 3
8	CEB high to CONFIGBUS Hi-Z			10	ns	2, 3
9	Write cycle start to AFB, FFB low			60	ns	

NOTES:
1. Applicable to both the 70 MHz and 85 MHz specification.
2. This parameter is sampled and not 100% tested.
3. Transition is measured ± 500mV from low or high voltage with load (see Figure 2).

Timing Waveforms of Pixel Port, CBLANKB, and RESET



AC Characteristics

At recommended operating conditions, unless otherwise noted.

Symbol	Parameter	-70			-85			Unit	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.		
1	CLOCK.IN Cycle Time	14			11			ns	
2	CLOCK.IN Pulse Width high	5			4			ns	
3	CLOCK.IN Pulse Width low	5			4			ns	
4	Pixel Data Set-up before CLOCK.IN high	1			1			ns	
5	Pixel Data Hold after CLOCK.IN high	5			5			ns	
6	CLOCK.IN high to Data out	2		10	2		9	ns	
7	RSB Pulse width Low	30			30			ns	1

NOTES:
1. This signal can be completely asynchronous to the Pixel Port and the MPU Port.

8

MOSEL-VITELIC NEW BiFIFO ARCHITECTURE FOR HIGH PERFORMANCE APPLICATIONS

Introduction

BiFIFO Concept and its Major Benefits to Systems

The architectural evolution of First-In-First-Out (FIFO) buffers has come a long way in the last decade. Small bipolar FIFOs with 16 words by 4-bits organization emerged in the late 1970s. The architecture then was primarily shift-register oriented with unidirectional data bus. Even with bipolar technology, these FIFOs had relatively slow data transfer rate (typically less than 5 MHz). Since that time, CMOS technology and dual-ported static random access memory design methodology have brought to market many larger and faster parallel FIFOs. To date, CMOS FIFOs dominate this fast growing niche market with density up to 8K x 9 bits, and read access time of less than 20 ns. The main stream products on the market now are parallel FIFOs in density ranges from 1K x 9 to 4K x 9. With CMOS technology, access time is being pushed to as fast as 15 ns while the majority is in the 25 ns to 35 ns range. The trend, however, points toward even faster access time (below 10 ns). Data buses will grow wider (up to 36 bits) and are equipped with bi-directional capability. Byte parity generation and checking are emerging as necessity.

For most FIFO applications, system designers frequently use multiple parallel FIFO chips to implement two buffers, one to receive and one to send data. Such an implementation resembles a larger FIFO (twice the size) buffer with bi-directional data bus (or buses). This practice brought about the relatively new concept of BiFIFO (a FIFO with bi-directional and tri-stated data buses) The integration of two conventional and identically-sized FIFOs to form one BiFIFO brings about several key benefits. First and foremost, chip count is reduced by 50% just in the FIFO alone. Secondly, the bus transceivers are now absorbed on chip the BiFIFO. Thirdly, a BiFIFO lends itself to simplified controls and timing parameters. Moreover, a single BiFIFO consumes less power than its counterpart of two parallel FIFOs of equal density plus the necessary external bus transceivers. No doubt, the BiFIFO brings about a very cost effective solution for practically all data communications and networking applications.

New and Simple Architecture

Contemporary BiFIFOs are trending toward single bank, dual-ported SRAM architecture. This design approach results in a simple and user friendly device, something that is lacking in most if not all traditional FIFOs. It is important for the new generation of BiFIFOs to have straight forward handshakes and controls in order to simplify the design and integration efforts on the system level. Consequently, using BiFIFO will help minimize system design and debug time, and therefore, shorten the time to market. Bi-directional buses with tri-state control improve bus control efficiency and expansion flexibility.

System I/O Bottleneck & the Role of BiFIFO

The 32-bit microprocessors (CISC and RISC) are finding their way into more applications way beyond those of the personal computers. As system bus frequency approaching 40 MHz to 50 MHz range, most systems tend to be I/O bound. To maximize overall system performance, particularly the bandwidth of the data bus and address bus must keep pace with the speed of the processor. The classic I/O bottleneck found in the host bus as well as the local bus is getting worse not only due to higher frequency, but also due to the increased number of peripheral controllers that are connected to them. To solve this bottleneck problem, system designers frequently look to FIFO (and now, BiFIFO) as a means to cushion the impact of the speed of one bus (for example, the host CUP bus) on another (for example, the peripheral bus). The traditional function of FIFOs (and BiFIFOs) is to provide a buffering facility between two or more digital systems of widely differing operating frequencies.

Faster and wider BiFIFO buffers and multi-port RAMs will impact favorably data communication between controllers and processors. These specialty memories simplify design and can pump data through the bus at 25 MHz or faster in a burst. When used in a 16-bit wide bus, the throughput is equivalent to a blazing 50 Mbytes per second. This is one reason why FIFOs and particularly BiFIFOs are playing an increasing role in removing I/O bound syndrome for all system buses.

Combining Speed with Architecture

As the clock frequency of computer buses increases, so should be the data throughput throughout all of its functional blocks. When FIFO is chosen as part of the hardware solution, system designers prefer the dual-ported configuration which allows simultaneous read on one port and write on another. To further complement the architecture, higher performance of the FIFO can be derived from clever chip design of some key AC parameters, such as setup time, hold time, output enable time and data valid time.

By combining these optimized AC parameters with a single bank structure and data fall-through FIFO architecture, a 25 MHz BiFIFO like the Mosel-Vitelic MS76500A/502A can quite adequately handle many emerging high performance applications.

Mosel-Vitelic's New BiFIFO Family, the MS76500A/502A

Both the MS76500A and the MS76502A are dual-ported, single bank FIFOs with two 16-bit bi-directional buses (known as A-Port and B-Port). The dual-ported memory refers to the basic SRAM cell structure which makes possible read and write operations to be independently and asynchronously of the input and output. A simplified functional block diagram is shown in Figure 1. Far from simply combining two traditional FIFOs to form one BiFIFO, the MS76500A/502A are packed with a number of unique functions and features and yet maintain simple controls. What follows is an attempt to highlight the functional capability of this new BiFIFO family, and its targeted and potential applications.

BiFIFO Architecture

As stated before, the MS76500A and MS76502A are asynchronous BiFIFOs using dual-port SRAM architecture. Both devices have two 16-bit wide buses, called A-Port and B-Port. Anticipating the need for high data integrity on the host bus, the A-Port is equipped with byte parity generation and checking capability. On the other hand, the necessity of byte and double-byte transfer is provided on the B-Port, which is expected to be connected to the peripheral bus (or a local bus). Both the MS76500A and 502A have a fast data fall through operation.

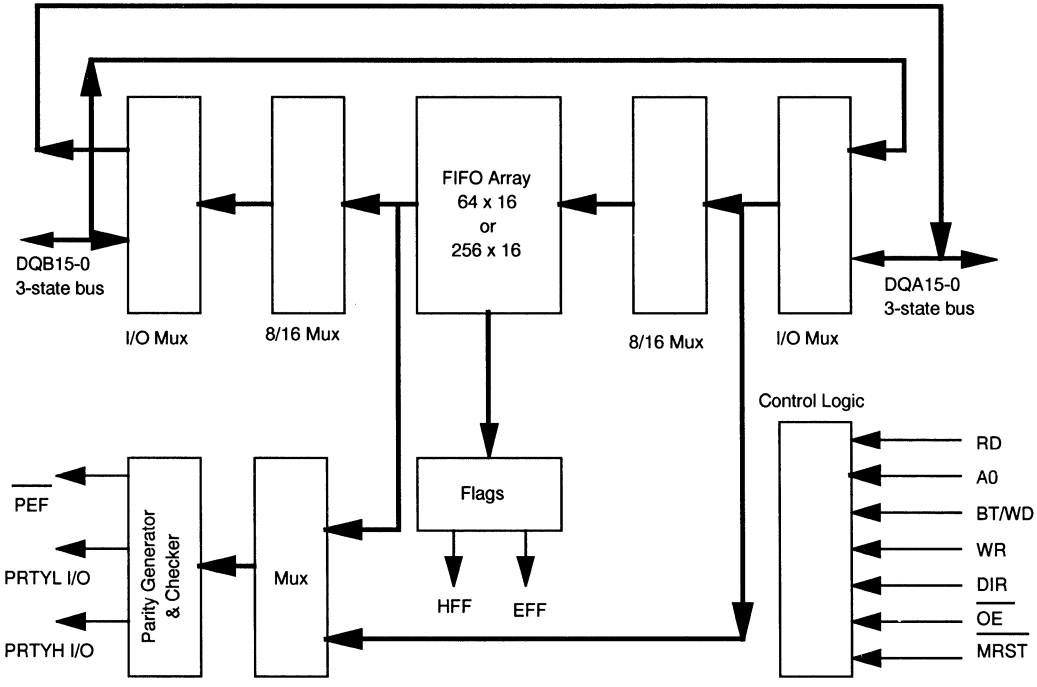


Figure 1. Functional Block Diagram of MOSEL MS76500A/502A

When the BiFIFO is initially empty, the time required for data to propagate from the input to the output is called the data fall-through time. The throughput (or data rate) at which data can be passed through the BiFIFO is governed by the fall-through time when the BiFIFO is empty or near empty and by the bubble back time when it is full or near full.

Two similar BiFIFOs can be used in parallel to form a 32-bit A-Port (plus byte parity bits) and B-Port. This expansion is virtually limitless, as the need for wider bus is deemed necessary. These BiFIFOs, however, are not intended for depth expansion.

Major Features

A summary of key features of the MS76500A/502A is listed below (all comments apply to both MS76500A and MS76502A, except as noted):

- Organization
  - 64 words by 16 bits (MS76500A)
  - 256 words by 16 bits (MS76502A)
- Bus structure: Two ports, A-Port and B-Port
  - Each Port (or bus) is 16-bit wide
  - Buses are bi-directional and respond to simple directional control
  - A-Port supports byte parity generation and checking
  - B-Port offers byte and word selectability
  - A-Port and B-Port have tri-stated outputs with output enable
- Status flags include:
  - Empty/Full, Half-Full and Parity Error
- Very high speed operations:
  - Fast cycle time of 25 MHz
  - A-Port data access = 25 ns max.
  - B-Port data access (byte or word) = 25 ns max.
  - Setup time = 3 ns max.
  - Hold time = 0 ns max
- Output drive current: 8 mA for A-Port and 4 mA for B-Port
- Data fall through design to achieve maximum throughput
- Low power consumption: 0.41W for MS76500A (maximum)
- Single 5V operation
- Surface mount packaging with 52-pin PLCC

Common and Different Features of the Two Buses

The design goal of this device was first and foremost to meet the need of high speed read and write to the FIFO, which operates at 25 MHz bandwidth. Each of the two bi-directional ports (or buses) are asynchronous and independent, in that one port can be in read mode while the other is in write mode simultaneously. The two ports share the same control logic which handles Write, Read, Output Enable, Master Reset, Direction control and Status flags.

The A-Port has parity generation and checking logic and the associated byte parity error flag outputs (PEF, PRTYL I/O and PRTYH I/O). The PEF is Parity Error Flag for the A-Port. When A-Port is used as input port, the parity checker checks the lower and upper bytes of data using the PRTYL and PRTYH signals as the respective parity check bit. If a parity error is found in either byte, PEF output will go LOW when WR input goes from LOW to HIGH to start the write operation. Once set, the PEF can be cleared by resetting the BiFIFO or making the A-Port as an output port by bringing DIR HIGH.

To accommodate byte and word handling, the B-Port was designed to provide byte selection capability, with which data can be packed or unpacked easily. This capability is supported by two control signals: A0 which selects the lower or higher order byte, and BT/WD which specifies 16-bit word or 8-bit byte data width on the bus.

Serious consideration was given to the data bus driving capability to make the MS76500A/502A more adaptable to the system bus environment on the one hand, and to maintain low power consumption on the other. The happy medium was chosen to provide 8 mA drive current on the A-Port and 4 mA on the B-Port. Despite of a total of 32 data input/output receivers and drivers, Mosel-Vitelic's CMOS technology has kept the total maximum operating power consumption to only 0.41 watt for the MS76500A, and only slightly higher for the MS76502A.

Upon first power up, the BiFIFO must be reset with the Master Reset signal. This causes the BiFIFO to start operation at a known state, which is empty.

Potential Applications of BiFIFO

The MS76500A/502A are intended for all the traditional applications of FIFO, buffering the difference in operating speeds of two buses. Due to its unique features of wider (16-bit) and bi-directional buses, fast access times and simple handshakes, the Mosel-Vitelic BiFIFO family is intended to be a single chip (or minimum chip count) solution to many high performance applications in data communications and networking. The fast access times in reading and writing have negated the need for very deep SRAM type of buffers. In fact,

applications which normally require very large (128K bytes or bigger) and high speed SRAMs (access time of 35 ns or faster), the DRAM-BiFIFO-based buffer implementation might prove to be a better solution due to lower cost and lower power than the SRAM counterpart. To demonstrate the basic and some what generic approach in using these BiFIFOs, four examples are illustrated in the next few pages.

Example 1: SCSI Hard Disk Caching in an EISA bus with Intel i82355

This example shows how the MS76500A BiFIFO plays an important role in a SCSI (Small Computer System Interface) adapter within an ESIA bus environment. As shown in Figure 2, a block diagram of a SCSI host adapter which contains an embedded 16-bit MCU, bus-mastering DMAC, SCSI interface and Data Cache Buffer (Disk Cache). The Data Cache Buffer is designed with two MS76500A BiFIFOs (identified as BiFIFO X and BiFIFO Y) and an expandable DRAM array. An Intel i82355 BMIC is used to handle the interface to the EISA bus.

Table 1 below specifies the data transfer rate of various buses within this sub-system.

As shown in the block diagram, one MS76500A (BiFIFO Y) sits between the i82355 BMIC and the DRAM-Disk-Cache. This BiFIFO Y handles a 16-bit data bus on its B-Port, to and from the BMIC at 40 Mbytes per second. On its A-Port, the 16-bit data bus and the two byte parity bits are transferred to/from the DRAM-Disk-Cache at 40 MBytes per second. That same bus is also tied to the A-Port of the second MS76500A, BiFIFO X. While the A-Port of BiFIFO X maintains the 40 MBytes per second throughput, its B-Port is only pumping at 5 MBytes per second to and from the SCSI Interface.

To prevent "bus-hogging" on the local bus and the ESIA bus, and to buffer the latency of the various buses, the BiFIFOs and the associated DRAM-Disk-Cache are used. This combination of BiFIFO and DRAM, called a DRAM-FIFO-based SCSI architecture, increases functionality and sophistication for high performance disk controllers.

This kind of architecture provides full-duplex data transfer. The SCSI adapter can execute a command to a peripheral device on the SCSI bus at the same time it is transferring data from a device to the host memory. Simply stated, read and write commands can be executed in parallel.

As can be seen in Figure 2, the DRAM-Disk-Cache is expandable from 256K x 9 to 16M x 9 to handle caching for multiple tracks, or multiple blocks of data in anticipation that it is needed by the host. This read-ahead approach enhances many Unix-based system where contiguous blocks of data are frequently used by the host CPU.

MS76500A/502A for RAID

For large client/server application, the SCSI adapter design illustrated in Figure 2 can be expanded to a disk array architecture, which is called RAID (Random Access Inexpensive Disks). Each SCSI Interface can handle up to 7 drives. There are different classes of RAIDs. The example shown represents a RAID 5. Depends on the magnitude of mass storage capacity needed, multiple SCSI Interfaces can be added (one MS76500A is needed for each SCSI Interface) as shown in Figure 3. This type of sub-system is fast emerging as the most cost effective mass storage solution for Unix-based systems, which support large on-line data base and/or transaction processing applications. The large DRAM-Disk-Cache effectively eliminates the seek time and other mechanical latency typically associated with drive drives. Super performance can be achieved as a result.

A few words about using the Intel BMIC with an external FIFO

When FIFO or BiFIFO is used externally as part of the transfer buffer (as is the case with our SCSI

From / To	To / From	Transfer Rate MB / sec.	Bus Width # bits
SCSI Interface	MS76500A (B-Port)	up to 5	8
MS76500A (A-Port)	DRAM Disk Cache	40 to 50	16 + 2 parity
DRAM Disk Cache	MS76500A (A-Port)	40 to 50	16 + 2 parity
MS76500A (B-Port)	i82355 BMIC	40	16
i82355 BMIC	EISA Bus	32	32

Table 1.

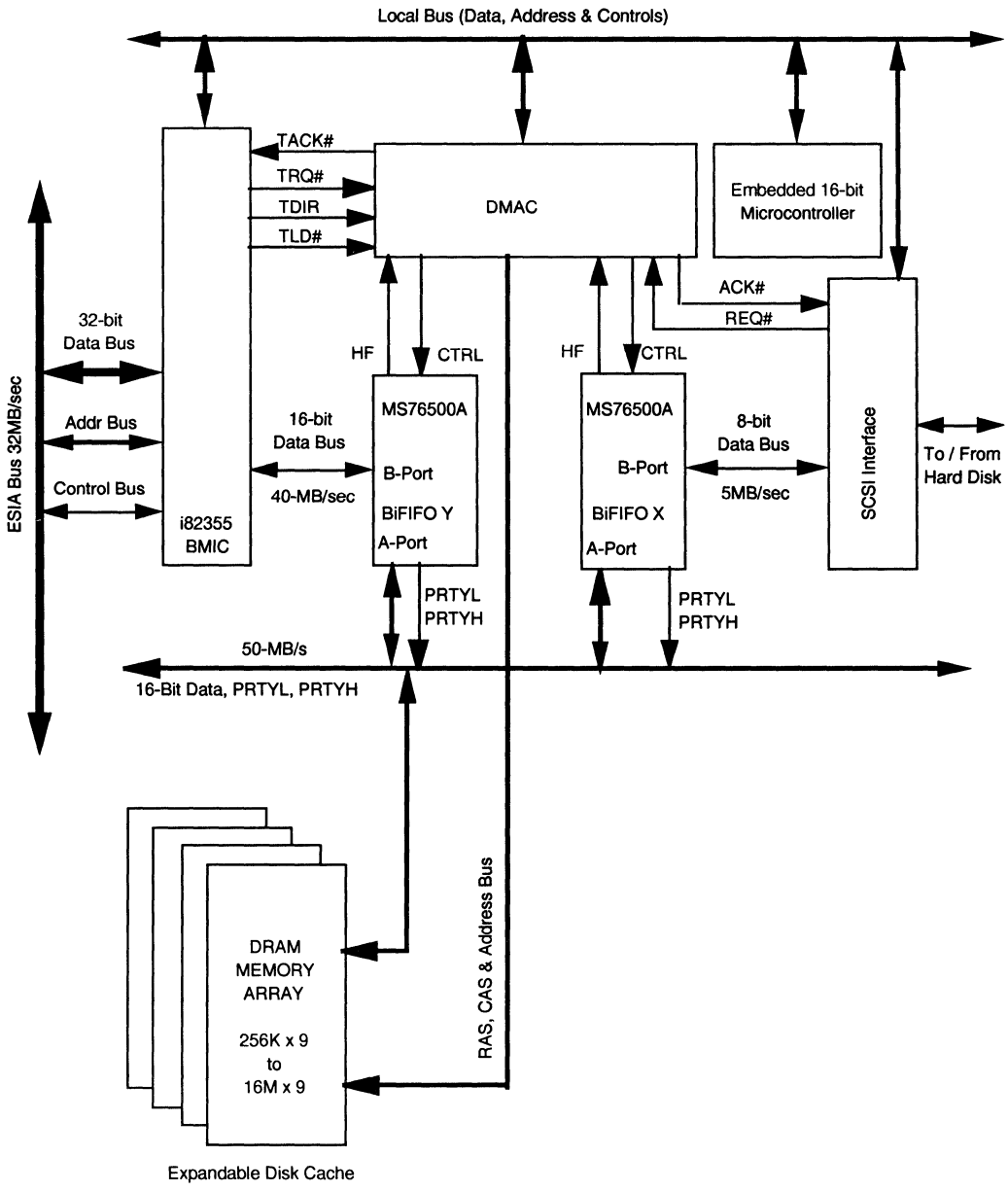


Figure 2. BiFIFO in EISA Host SCSI Adapter

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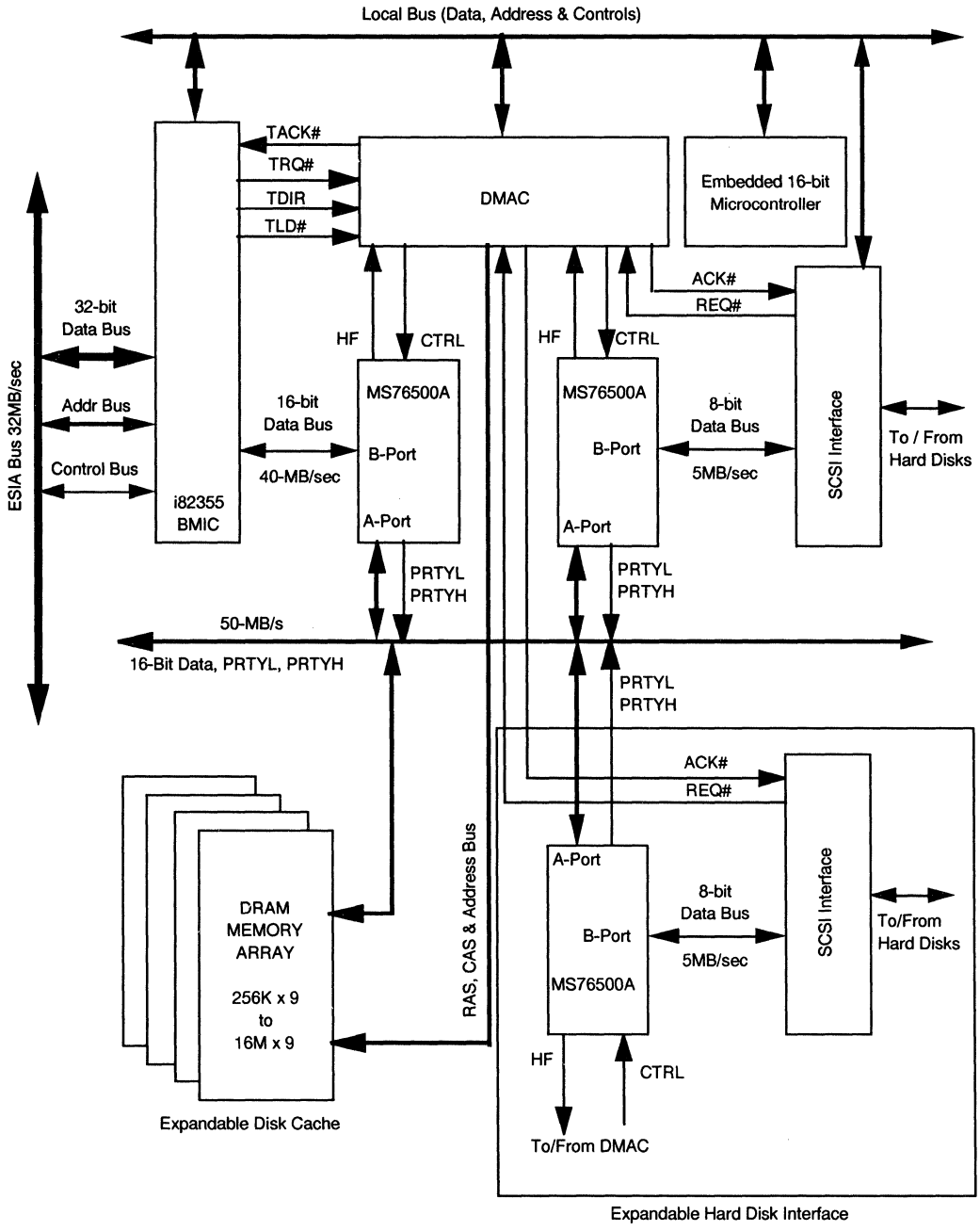


Figure 3. EISA Host SCSI Adapter - a RAID Architecture

example) to the Intel i82355 BMIC, certain design issues must be addressed. The following is a summary of a "tech-note" which was published by Intel (Reference Number: PER-0890) addressing this issue. By using the mentioned guide lines, one could side-step the potential problems caused by using the BMIC with an external FIFO.

The i82355 BMIC incorporates two independent states machines to control the transfer protocol of the EISA interface and the transfer buffer interface (in our SCSI example, it is the combined BiFIFO and DRAM-Disk Cache). During a transfer, the current transfer byte count information is only available to the EISA interface state machine. The EISA interface state machine signals the transfer buffer interface state machine (the DMAC in conjunction with the local 16-bit embedded MCU as shown in Figures 2 and 3) to shut down (stop) after the terminal count has been reached. Since the current byte count is available to the EISA interface state machine, it shuts down with the last byte (word or double-word) of transfer.

The manner in which the transfer buffer interface functions is described separately when it performs an EISA READ and EISA WRITE.

During EISA READ, the transfer buffer interface state machine (DMAC and the embedded MCU) receives the STOP signal from the EISA interface state machine while it is transferring data out of the i82355 internal 24-byte FIFO. The STOP signal is synchronized with the last word to be transferred, and the transfer buffer interface state machine (DMAC) shuts down with the last word transfer.

During EISA WRITE, the transfer buffer interface state machine (DMAC) receives the STOP signal after it has read data beyond the number of bytes to be transferred (over reads by a maximum of 28 bytes). The over read bytes are flushed from the i82355 internal FIFO when the next transfer is initiated.

To prevent this over read condition from occurring, either a hardware or a software solution must be deployed. The i82355 device software can be written to complete the current transfer before initiating the next transfer. This way only data from one transfer is in the i82355 internal FIFO at any given time. However, this solution may have a performance impact for some applications, and as such it may not be an ideal solution.

The illustrated SCSI example used a hardware solution which requires an external 22-bit byte counter and a separate D-Flip-Flop. The terminal count of the byte counter is used to set the D-Flip-Flop which in turn disables the i82355 read operation to its internal FIFO. The i82355 will continue to read (over read) stale data. The i82355 TEOP# signal is used to RESET the D-Flip-Flop which enables the i82355 reads to its internal FIFO.

Example 2: BiFIFO As Part Of Bus Snooping for MC68040

The MS76500A/502A BiFIFOs are natural off-the-shelf products which plays a very significant role in improving performance of the new generation of 32-bit CISC, such as the Motorola MC68040. Working in conjunction with a snoop-capable cache controller and decoder PALs (see Figure 4), an external write-through or write-back cache. This design is capable of exhibiting full use of the MC68040 snoop capability. It is noted that the external cache uses a BiFIFO (within the system interface block) to post writes to the system bus. Data stored in the BiFIFO is not snoop capable. To prevent a DMA read transfer from reading stale data, the data contained in the BiFIFO must be written to memory prior to the start of the DMA read snoop. This happens when a DMA read occurs while the BiFIFO contain posted write data.

The BiFIFO is also useful in a write-back cache implementation when a dirty cache line is replaced on a CPU read miss. This approach allows the write back of the data to be postponed until after the read is completed.

Emptying the system interface BiFIFO involves the use of a relinquish and retry termination to the DMA read transfer. The processor bus is taken away from the MC68040 to prevent further write cycles from occurring. The system bus is then grand to the processor node so that the cache controller may empty the system interface BiFIFO.

When the system interface BiFIFO is empty, the bus is returned to the DMA controller for the retried bus cycle. The first BiFIFO in the snoop controller provides a path between the system address bus and the processor address bus; the data BiFIFO in the system interface provides a path between the system data bus and the processor data bus.

The snoop controller signals a snoop operation to the MC68040, causing the MC68040 to source data on a cache hit. This data is presented to the system data bus through the data BiFIFO in the system interface. This operation concludes with the return of the processor bus to the MC68040 and with the snoop controller BiFIFOs being three-stated. The BiFIFOs allow the system timing to be de-coupled from the CPU timing. In more advanced systems, the

CPU may run at 2x (two times) the clock rate or higher.

When a DMA write occurs, the addresses are clocked into the BiFIFO. The BiFIFO is capable of storing up to 32 addresses before requiring the DMA controller to pause. The processor bus is requested so that the latched addresses appear on the processor bus. If an internal or an external cache hit occurs, then that cache line is invalidated. Using the BiFIFO allows the snooping process to be done efficiently with no wait states.

Example 3: MS76500A/502A in Local Area Network

Using the BiFIFO (MS76500A) and BMIC interface methodology as established earlier in the SCSI RAID application (Figure 3), a local area network adapter can be designed for the EISA environment. Figure 5 is an example of such an application.

When data is to be transferred onto the LAN adapter, the LAN controller arbitrates for the local processor bus. Once acquiring bus ownership, it transfer data from the LAN port into the BiFIFO and then the DRAM-cache when no re-processing is needed. If any re-formatting or processing is required, data from the LAN port is transferred

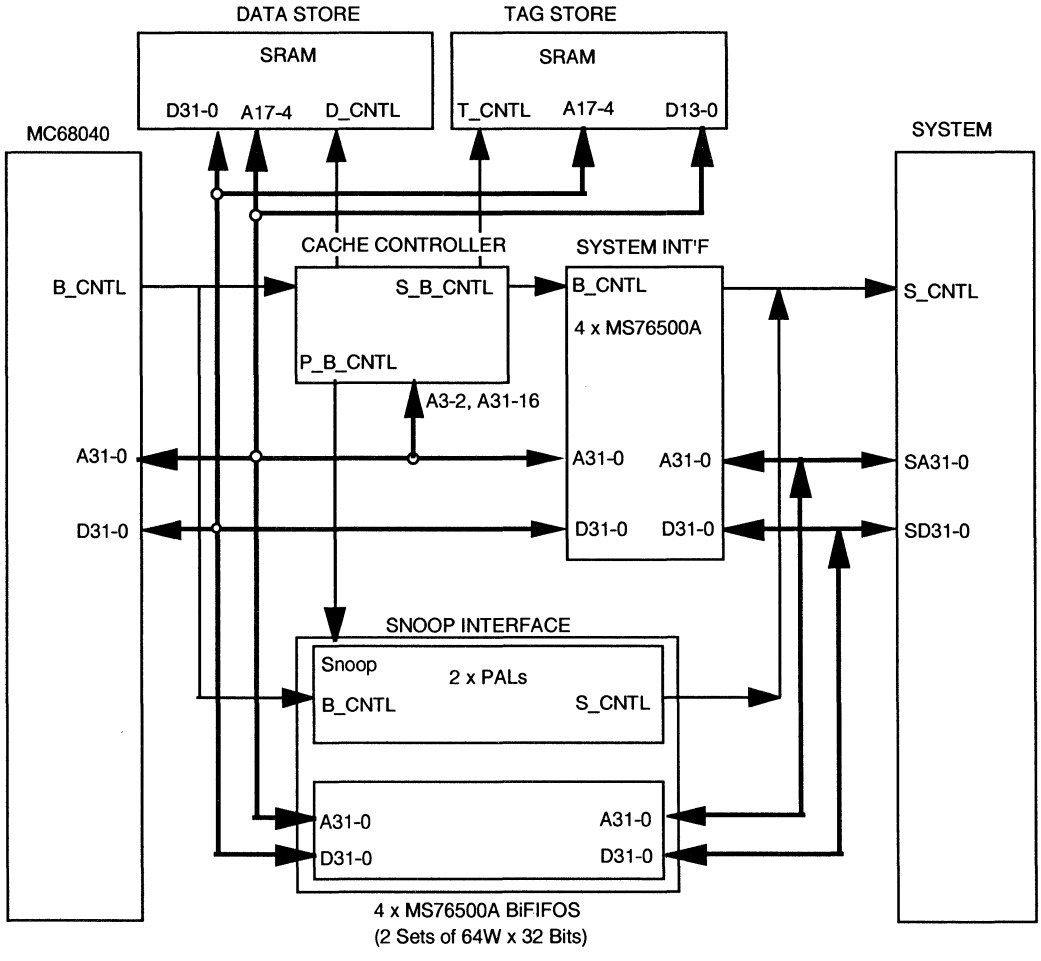


Figure 4. BiFIFOs As Part of Bus Snooping for MC68040

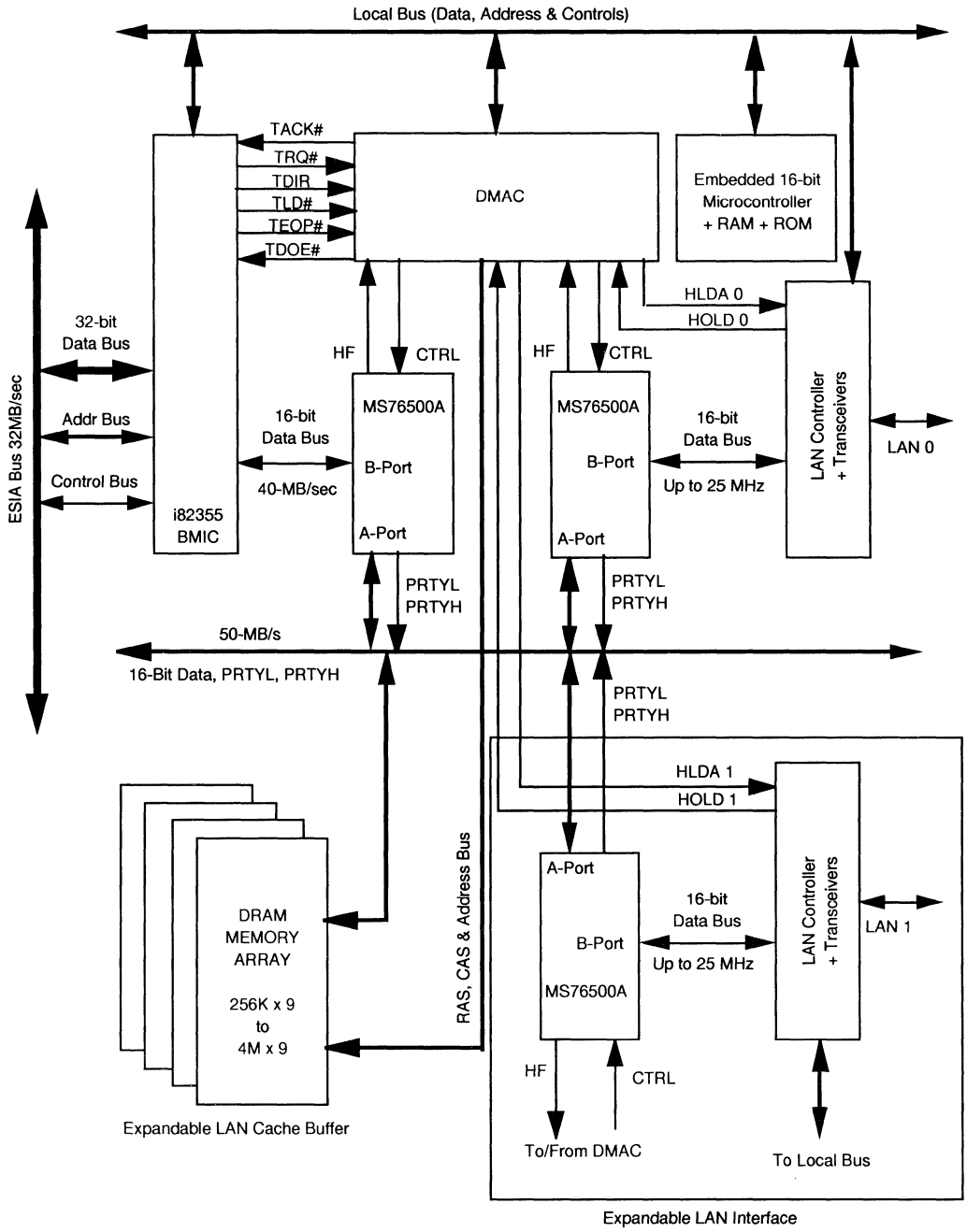


Figure 5. BiFIFO in A Local Area Network Adapter

directly to the local system memory for processing by the local processor. If data in local memory is to be sent onto the LAN port, it can directly read the data from RAM (local). When done, it updates the local processor mailbox in the shared system RAM and relinquishes the bus.

The local processor will process the packets which now resides in it local memory (RAM). If the data goes to a device on the EISA bus, the local processor then moves the data directly to the DRAM cache buffer and notifies the BMIC. The BMIC then transfers the data, bursting over the EISA bus from the DRAM cache buffer via the BiFIFO. If the data in local memory is to be translated for other LAN port (for example, LAN 1 in Figure 5) the local processor handles the translation and reformatted data is sent to LAN 1 controller through some form of mailbox setup. LAN 1 then arbitrates for local processor bus and directly transfers the data from the local memory to LAN 1.

Data arriving from the EISA is place into the DRAM-Cache buffer via the BiFIFO which buffers the difference in bus frequency. The cached data can be transferred to the LAN ports directly under the control of the DMAC and local processor. If the cached data has to be reformatted, the DMAC will pull in that data to it local memory and perform the formatting by the local processor at its discretion. After reformatting, the data is then forwarded to the selected LAN port.

Example 4: MS76500A/502A in SBus-VMEBus Adapter

There are several methods of providing a "bus-to-bus adapter" which connects a SBus to a VMEBus architecture. Perhaps the simplest and most inexpensive approach is by using a dual-ported SRAM, like the Mosel-Vitelic BiFIFO, as shown in Figure 6. In this SBus-to-VMEBus link, each side of the BiFIFO is a slave function on its respective bus with a "window" mapped into each bus' memory space. A transaction from one bus to another uses the BiFIFO as a mailbox. In the case of an Sbus-to VMEBus transaction, the SBus deposits information in the BiFIFO. The VMEBus then initiates a cycle to read memory, effectively transferring data from SBus to VMEBus. While this is simple, it is also slow and cumbersome; it requires multiple bus cycles on each side to move data from one bus to another. It also restricts the type of equipment that must exist on both sides of the adapter. Both the SBus and the VMEBus must have functional modules that can be bus masters to read/write the BiFIFO. In a SPARCstation application, this is not an issue on the SBus side. The required VMEBus master may not be available, cost effective, or even desirable in all VMEBus configurations, however.

Another hardware approach to linking an SBus to a VMEBus is to expand the adapter functions to include an integral VMEBus master (see Figure 7). This approach allows the SBus to become a master on the VMEbus through the adapter's integral VMEBus master. While this enhances communications from the SBus to VMEBus, it still relies on a "mailbox" memory scheme to pass data in the opposite direction, if data transfer from the VMEBus to SBus is required. This type of architecture has the advantage of including VMEBus master logic as part of the adapter hardware, but it still has the disadvantage of restricting direct writes from VMEBus to SBus. Many applications only require unidirectional data transfer between the two buses. In these cases, the adapter shown in Figure 6 may well be adequate. There are however, at least

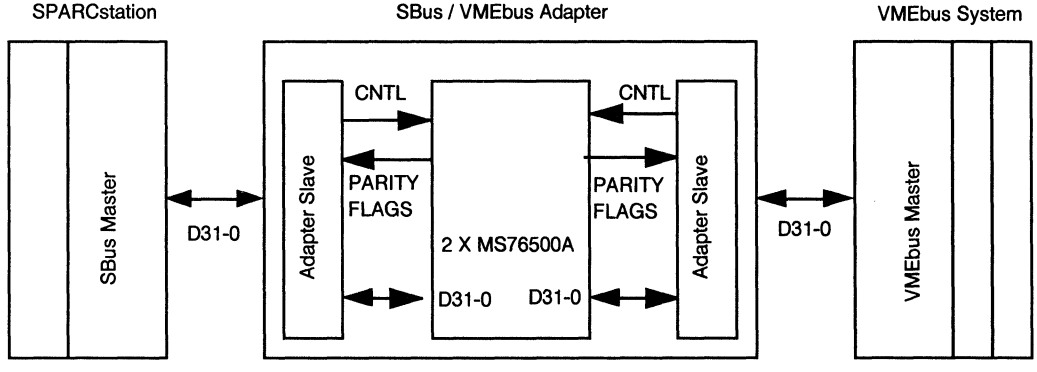


Figure 6. BiFIFO in SBus to VMEBus Adapter

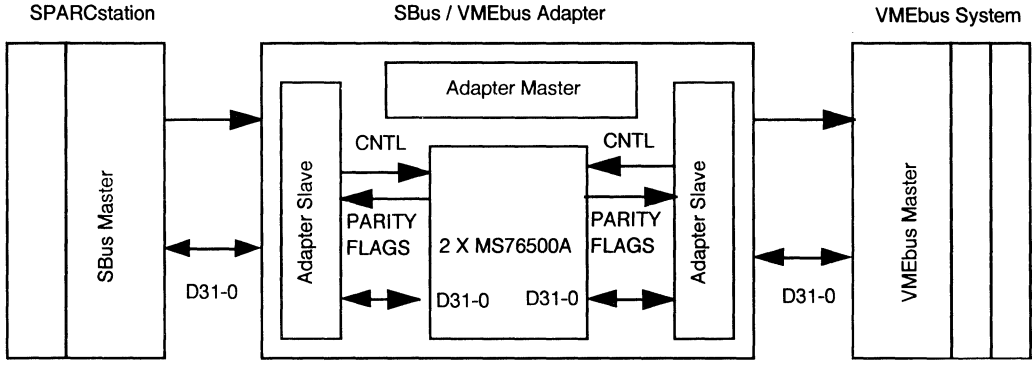


Figure 7. BiFIFO in SBus to VMEBus Adapter with VMEBus Master

as many or even more real-world applications in which it is desirable to write data directly from the VMEbus environment to the SPARCstation. A VMEBus hard disk controller is a good case. It is important and necessary for the disk subsystem to move data from the disk to the system memory at high speed. A link between SBus and VMEBus that require the disk controller to write a BiFIFO and the SPARCstation to subsequently "pick up" the data and move it to the SPARCstation's working memory would be very inefficient.

When direct read and write for both buses is necessary, a symmetrical or orthogonal adapter (with master and slave co-existing) is the answer. It involves more hardware, but it makes up in data transfer efficiency (read and write) in either and both directions (to and from SBus / VMEBus). The adapter master logic is assumed to be an ASIC with DMAC functions. See Figure 7 for a simplified functional block diagram.

The Real Benefits of Using BiFIFO

From the few applications examples mentioned in this article, it can be derived that BiFIFO earns its place in the design of multiple bus-based computer systems. It brings to the party some very unique attributes which directly impact the performance of the end system. Its true benefits are numerous, of which six most improtant ones are mentioned below:

1. The BiFIFO Helps eliminate "bus-hogging" by decoupling one part of a system from the other, and thus enhances overall system throughput.

2. For very large caching applications, such as SCSI host adapter, a BiFIFO can supplement the DRAM cache buffer by contributing the needed speed and parity generation and checking. Large amount of more expensive and power hungry SRAM would otherwise be necessary.

3. One BiFIFO is equivalent to two parallel FIFOs of similar size. In addition, the bi-directional bus transceivers are available on chip of the BiFIFO, which otherwise have to be provided externally. This adds more chip count and power consumption. The wider 16-bit bus of the MS76500A/502A further exacerbate the argument compared to the 8-bit parallel FIFO.

4. The Mosel-Vitelic BiFIFOs improve data integrity by providing byte parity generation and checking. The faster is the throughput of data transfer, the higher is the probability of transmission error. Parity generation and checking could not have come in more handily. A parity error output signal is available for the external monitoring.

5. Combing two (2) 8-bit parallel FIFOs, 16-bit bus transceivers and byte parity generation and checking logic, the Mosel-Vitelic BiFIFOs offer very cost effective solution all in one compact surface mount PLCC package.

6. De-mystifying the myth that FIFO and BiFIFO are difficult to use, due to tricky timing and controls,

the MS76500A/502A are equipped with straight forward, easy to use control parameters.

Conclusion

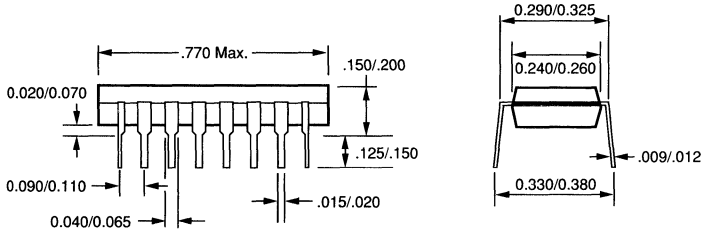
The I/O bottleneck has the crippling effect similar to that exists between CPU and main memory. The latter problem, by and large is being solved with high performance cache architecture and cache snooping.

The Mosel-Vitelic BiFIFO family is intended to be the high speed solution to the I/O bottleneck problem. As illustrated in the design examples of RAID, LAN, Cache-Snooping and SBus-VMEBus adapter, the Mosel-Vitelic BiFIFO is used to de-couple the bus from another bus. By doing so, it improves the performance (by removing bus hogging condition) of the overall system. For these and many other high performance sub-systems, the Mosel-Vitelic BiFIFO is expected to be an integral part.

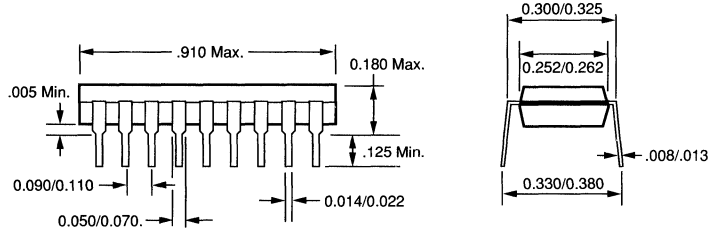
Part Number	Ordering Designation	Package	Page
MS6264	P	28-Pin 600 mil Plastic DIP #1	10-9
	F	28-Pin 330 mil SOG #2	10-11
MS6264A	N	28-Pin 300 mil Plastic DIP #1	10-8
	R	28-Pin 300 mil SOJ	10-12
MS6264N	P	28-Pin 600 mil Plastic DIP #1	10-9
	F	28-Pin 330 mil SOG #2	10-11
MS6265	N	28-Pin 300 mil Plastic DIP #2	10-8
	P	28-Pin 600 mil Plastic DIP #3	10-10
	F	28-Pin 330 mil SOG #1	10-10
MS6516	P	24-Pin 600 mil Plastic DIP	10-6
	S	24-Pin 300 mil SOG	10-7
MS7200	N	28-Pin 300 mil Plastic DIP #1	10-8
	F	28-Pin 330 mil SOG #2	10-11
	J	32-Pin Plastic Leaded Chip Carrier	10-17
MS7201A	N	28-Pin 300 mil Plastic DIP #1	10-8
	P	28-Pin 600 mil Plastic DIP #1	10-9
	F	28-Pin 330 mil SOG #2	10-11
	J	32-Pin Plastic Leaded Chip Carrier	10-17
MS7202A	N	28-Pin 300 mil Plastic DIP #1	10-8
	P	28-Pin 600 mil Plastic DIP #1	10-9
	F	28-Pin 330 mil SOG #2	10-11
	J	32-Pin Plastic Leaded Chip Carrier	10-16
MS7203	N	28-Pin 300 mil Plastic DIP #1	10-8
	P	28-Pin 600 mil Plastic DIP #1	10-9
	F	28-Pin 330 mil SOG #2	10-11
	J	32-Pin Plastic Leaded Chip Carrier	10-16
MS7204	N	28-Pin 300 mil Plastic DIP #1	10-8
	P	28-Pin 600 mil Plastic DIP #1	10-9
	F	28-Pin 330 mil SOG #2	10-11
	J	32-Pin Plastic Leaded Chip Carrier	10-16
MS62256	P	28-Pin 600 mil Plastic DIP #1	10-9
	N	28-Pin 300 mil Plastic DIP #1	10-8
	F	28-Pin 330 mil SOG #4	10-11
MS62256A	N	28-Pin 300 mil Plastic DIP #1	10-8
	R	28-Pin 300 mil SOJ	10-12
MS62256C	P	28-Pin 600 mil Plastic DIP #2	10-9
	F	28-Pin 330 mil SOG #3	10-11
MS62256N	P	28-Pin 600 mil Plastic DIP #1	10-9
	F	28-Pin 330 mil SOG #4	10-11
MS76215	J	68-Pin Plastic Leaded Chip Carrier 68-Pin Pin Grid Array (Call factory for package information)	10-19
MS76225	J	68-Pin Plastic Leaded Chip Carrier 68-Pin Pin Grid Array (Call factory for package information)	10-19

Part Number	Ordering Designation	Package	Page
MS76500A	J	52-Pin Plastic Leaded Chip Carrier	10-18
MS76502A	J	52-Pin Plastic Leaded Chip Carrier	10-18
MS76542	Q	132-Pin QFP	10-23
MS621002	K	32-Pin 400 mil SOJ	10-17
MS621008	E	32-Pin 400 mil Plastic DIP	10-15
	K	32-Pin 400 mil SOJ	10-17
MS622424	Q	100-Pin QFP	10-22
MS628128	P	32-Pin 600 mil Plastic DIP	10-15
	F	32-Pin 330 mil SOG	10-16
V52C4256	K	28-Pin 400 mil SOJ	10-12
	Z	28-Pin ZIP	10-13
V52C4258	K	28-Pin 400 mil SOJ	10-12
	Z	28-Pin ZIP	10-13
V52C8126	K	40-Pin Plastic SOJ	10-17
	Z	40-Pin Plastic ZIP	10-18
V52C8128	K	40-Pin Plastic SOJ	10-17
	Z	40-Pin Plastic ZIP	10-18
V52C8254	K	40-Pin Plastic SOJ	10-17
V52C8255	K	40-Pin Plastic SOJ	10-17
V52C8258	K	40-Pin Plastic SOJ	10-17
V53C256A	P	16-Pin 300 mil Plastic DIP, 1/2 Lead	10-4
	J	18-Pin Plastic Leaded Chip Carrier	10-5
V53C464A	P	18-Pin 300 mil Plastic DIP #1	10-4
	J	18-Pin Plastic Leaded Chip Carrier	10-5
V53C100F	P	18-Pin 300 mil Plastic DIP #2	10-4
	K	26/20-Pin 300 mil SOJ	10-5
V53C100H	P	18-Pin 300 mil Plastic DIP #2	10-4
	K	26/20-Pin 300 mil SOJ	10-5
V53C100N	P	18-Pin 300 mil Plastic DIP #2	10-4
	K	26/20-Pin 300 mil SOJ	10-5
V53C104A	P	20-Pin 300 mil Plastic DIP	10-5
	K	26/20-Pin 300 mil SOJ	10-5
V53C104F	P	20-Pin 300 mil Plastic DIP	10-5
	K	26/20-Pin 300 mil SOJ	10-5
V53C104H	P	20-Pin 300 mil Plastic DIP	10-5
	K	26/20-Pin 300 mil SOJ	10-5
V53C104N	P	20-Pin 300 mil Plastic DIP	10-5
	K	26/20-Pin 300 mil SOJ	10-5
V53C261	P	24-Pin 400 mil Plastic DIP	10-6
	Z	24-Pin ZIP	10-7

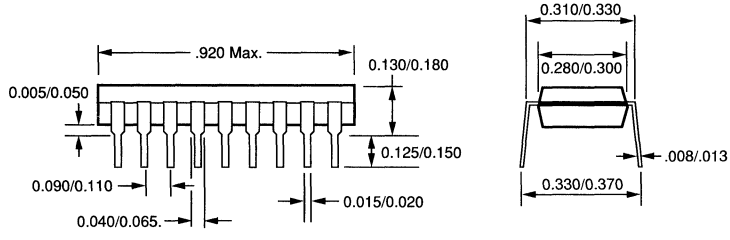
16-Pin 300 mil Plastic DIP, 1/2 Lead



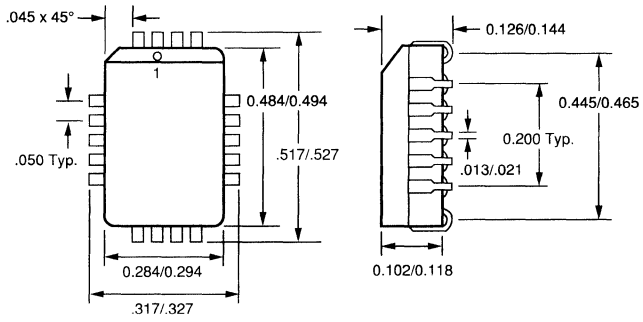
18-Pin 300 mil Plastic DIP #1



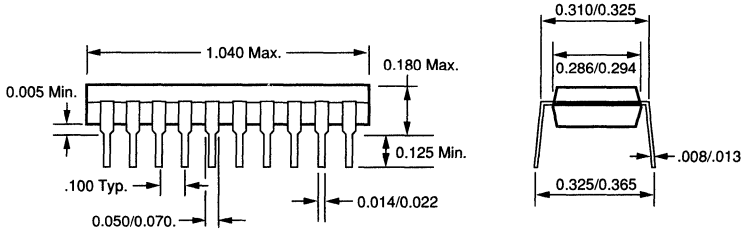
18-Pin 300 mil Plastic DIP #2



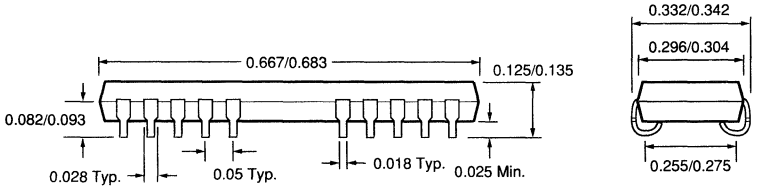
18-Pin Plastic Leaded Chip Carrier



20-Pin 300 mil Plastic DIP



26/20-Pin 300 mil SOJ



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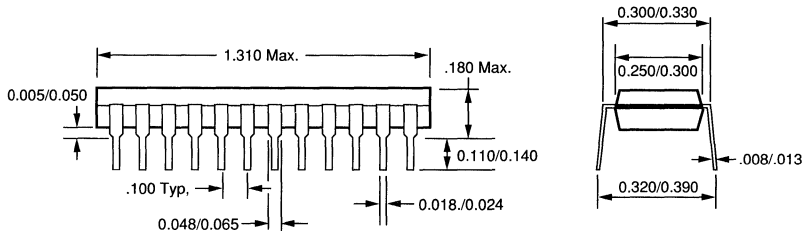
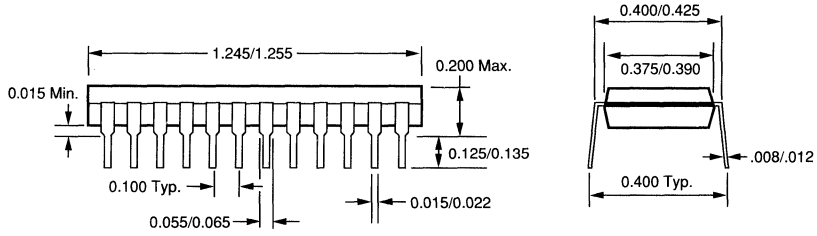
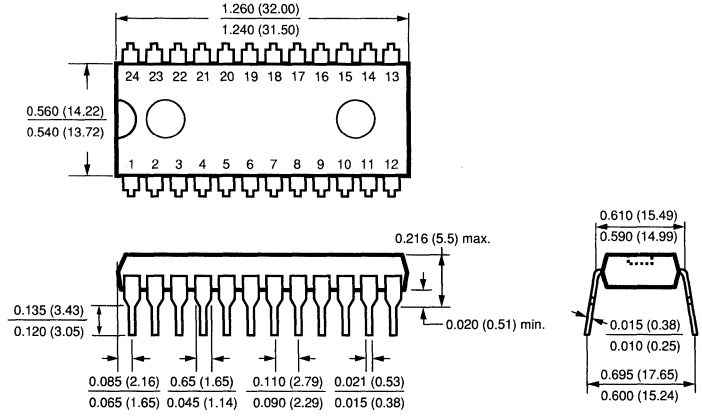
24-Pin 300 mil Plastic DIP



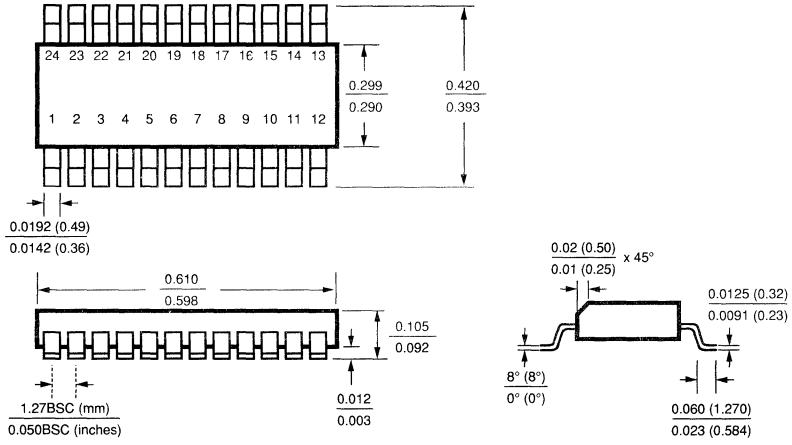
24-Pin 400 mil Plastic DIP



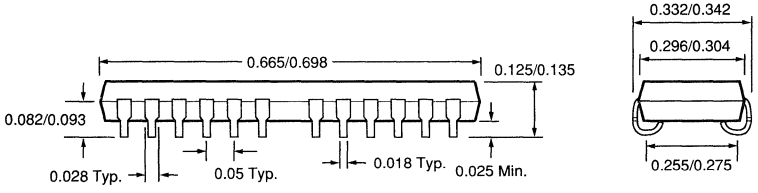
24-Pin 600 mil Plastic DIP



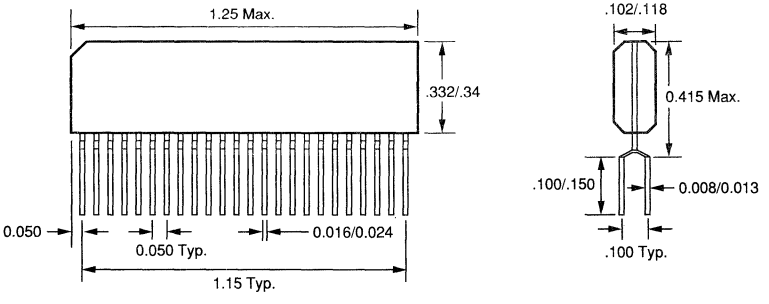
24-Pin 300 mil SOG



26/24-Pin 300 mil SOJ



24-Pin ZIP



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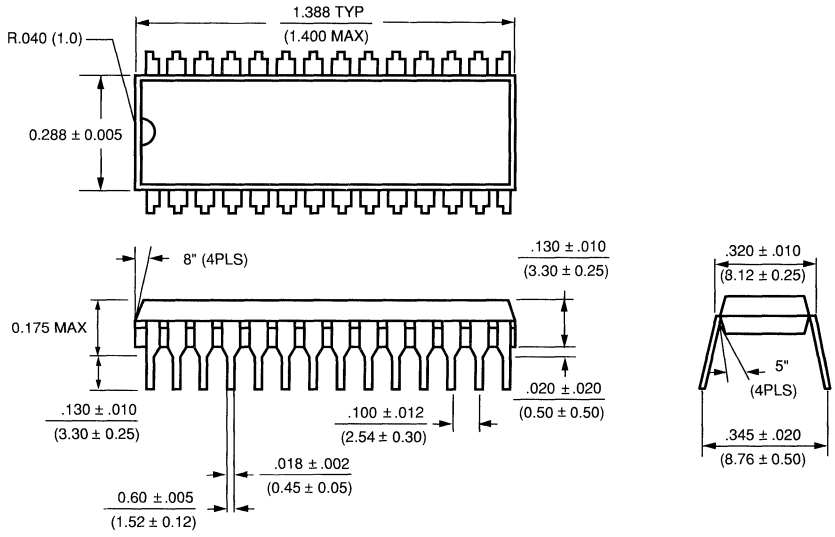
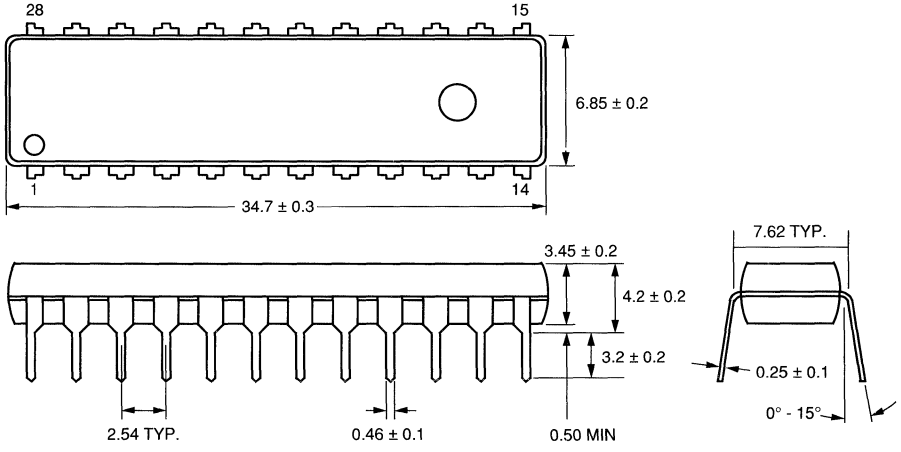
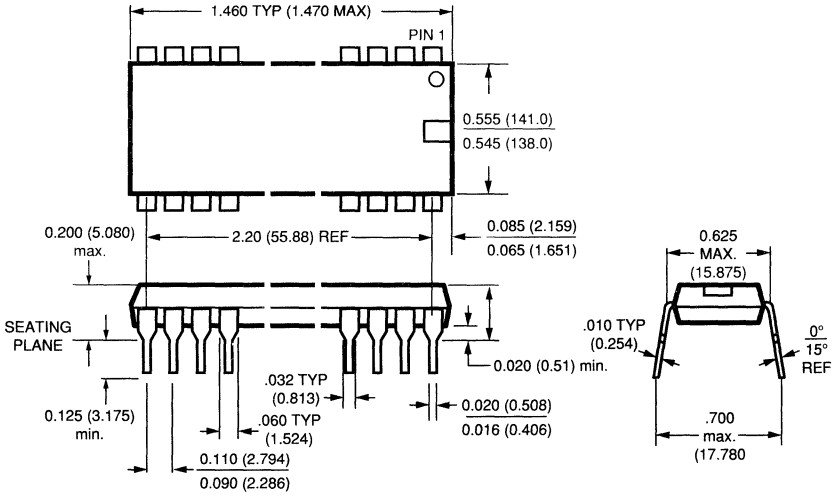
28-Pin 300 mil Plastic DIP #1



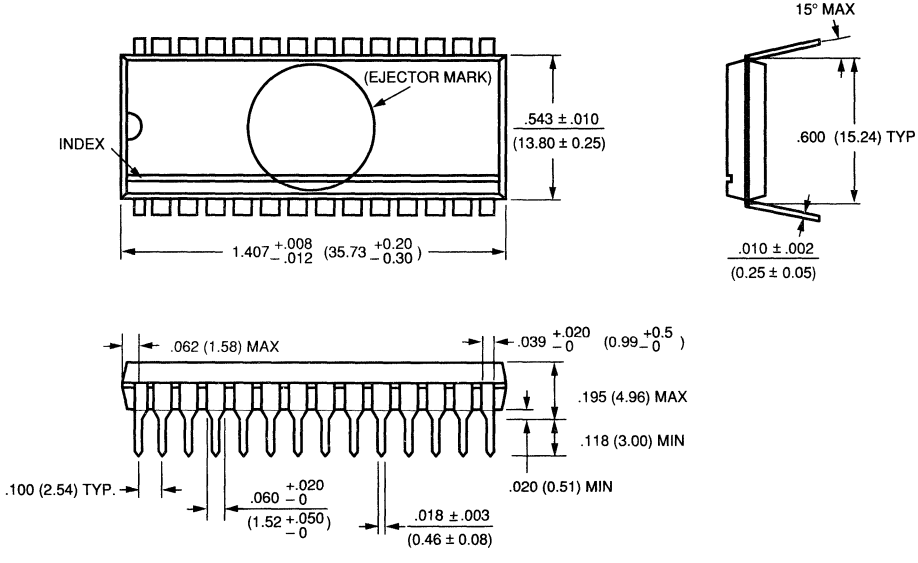
28-Pin 300 mil Plastic DIP #2



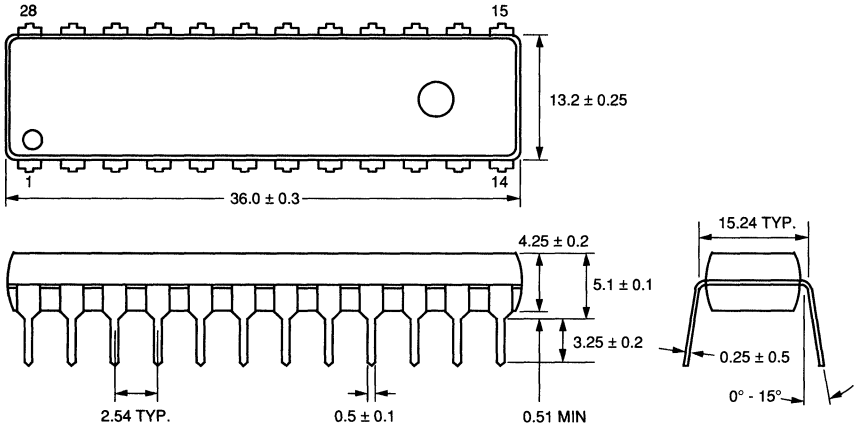
28-Pin 600 mil Plastic DIP #1



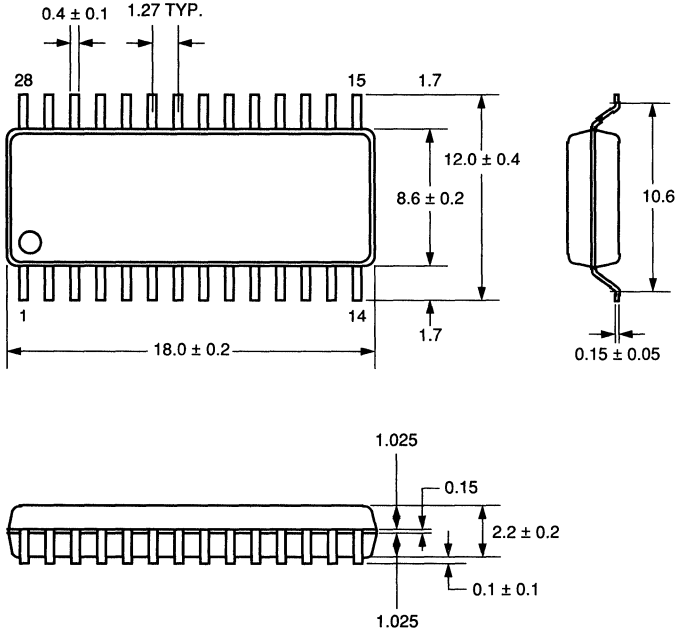
28-Pin 600 mil Plastic DIP #2



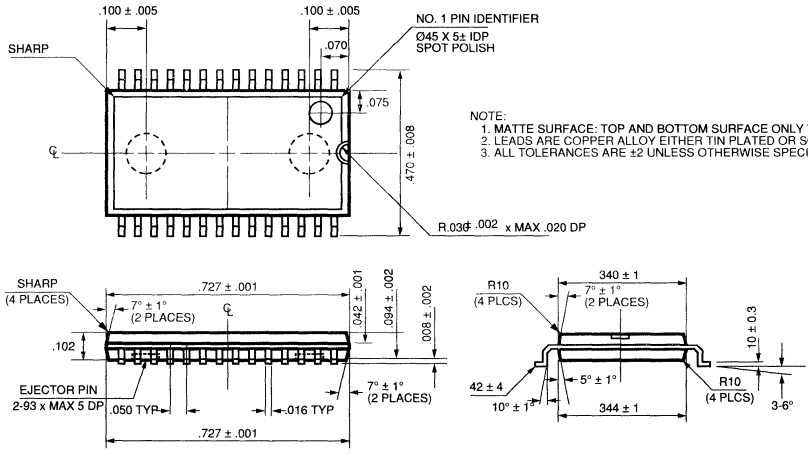
28-Pin 600 mil Plastic DIP #3



28-Pin 330 mil SOG #1

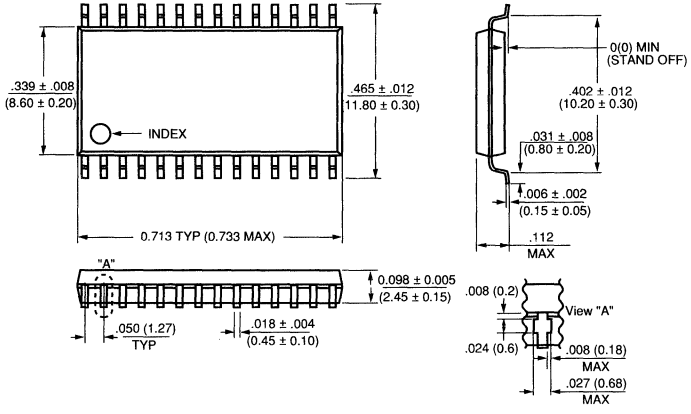


28-Pin 330 mil SOG #2



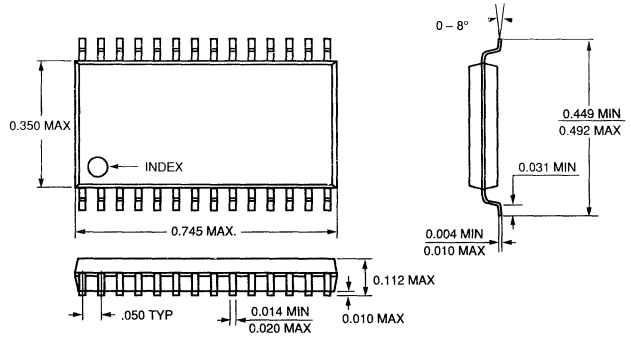
28-Pin 330 mil SOG #3

MS62256C



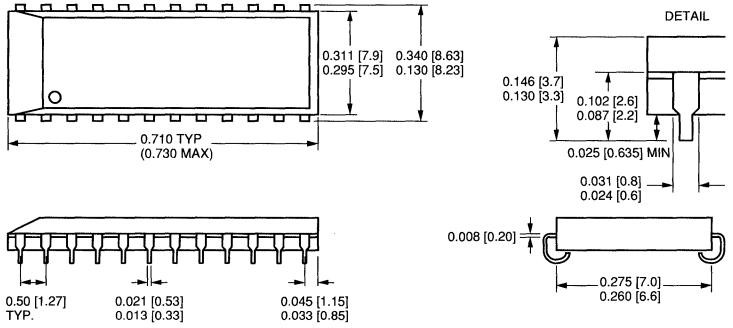
28-Pin 330 mil SOG #4

MS62256
MS62256N



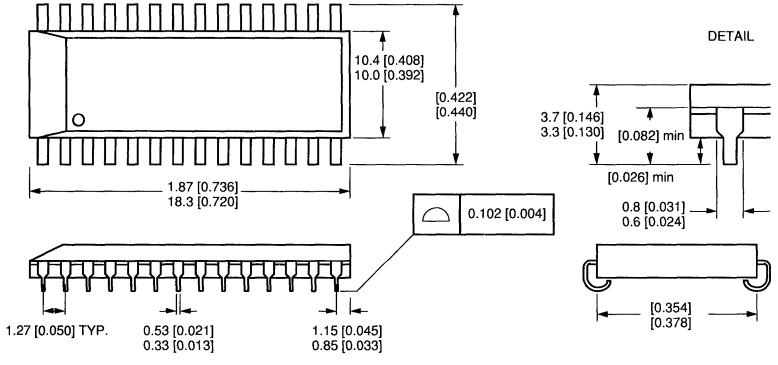
10

28-Pin 300 mil SOJ



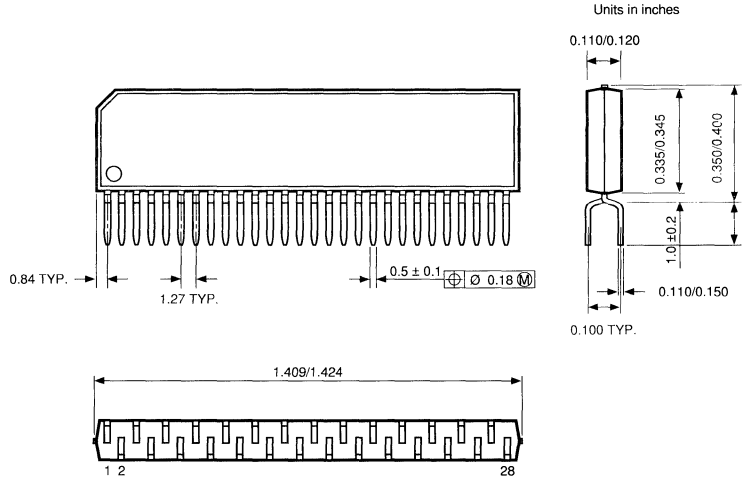
DIMENSIONS IN INCHES [MM]

28-Pin 400 mil SOJ

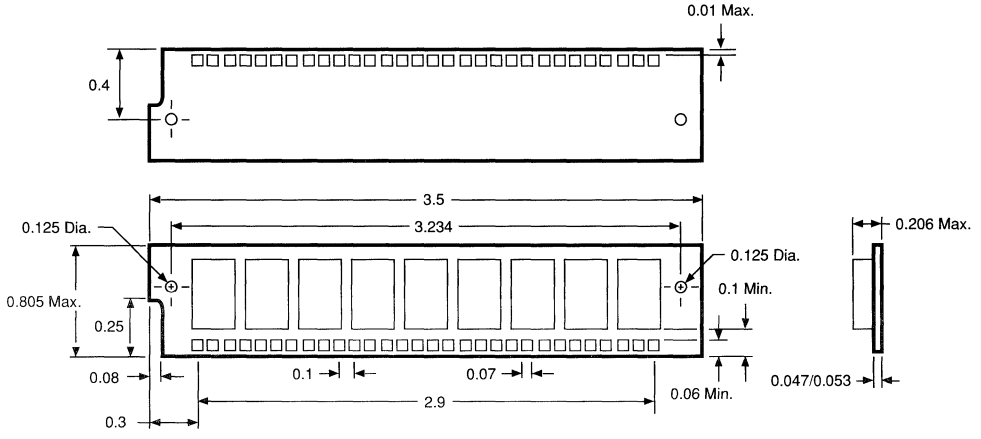


DIMENSIONS IN MM [INCHES]

28-Pin ZIP



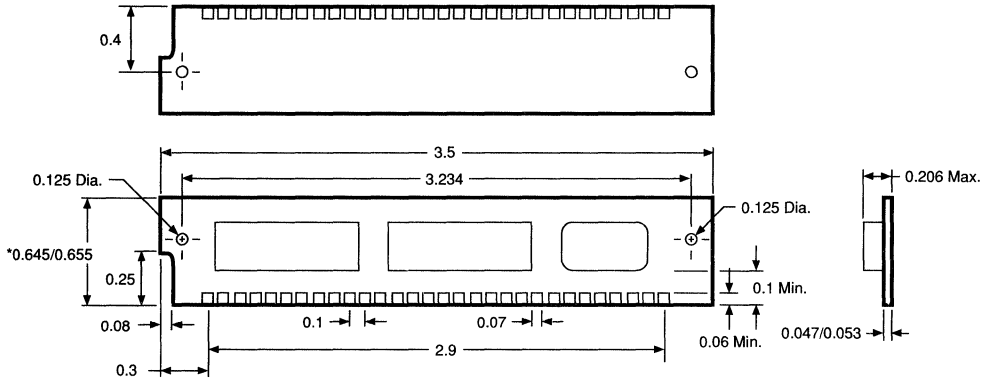
30-Pin SIMM #1



* Package dimensions subject to change without notice.

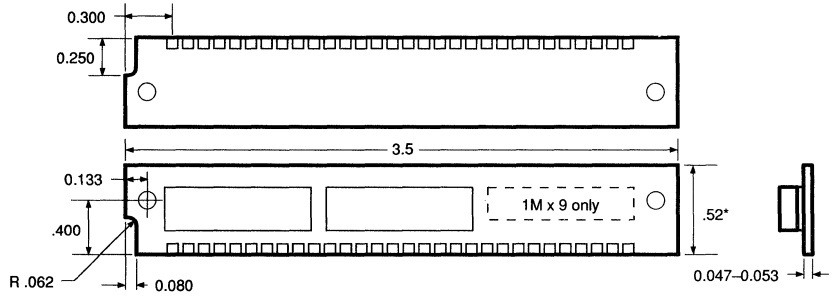
10

30-Pin SIMM #2



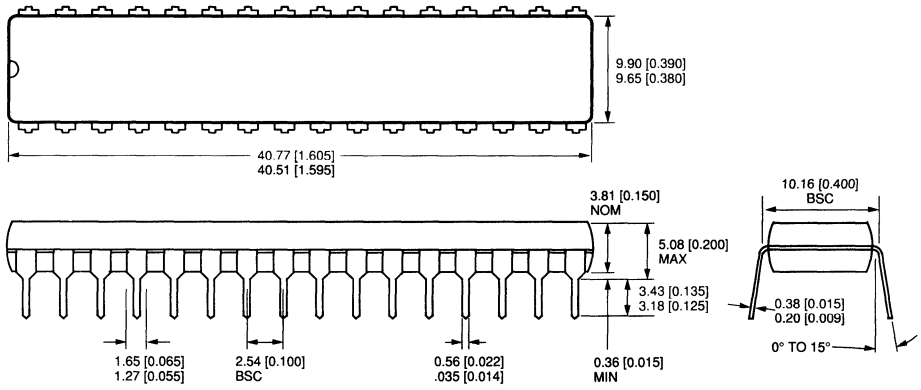
* 0.5" module also available
** Package dimensions subject to change without notice.

30-Pin S Module #3

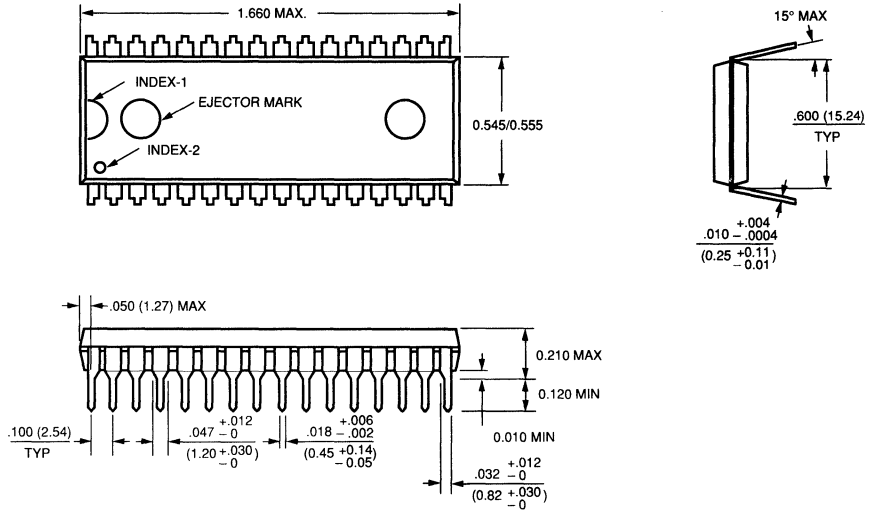


* 0.65" module also available
** Package dimensions subject to change without notice.

32-Pin 400 mil Plastic DIP

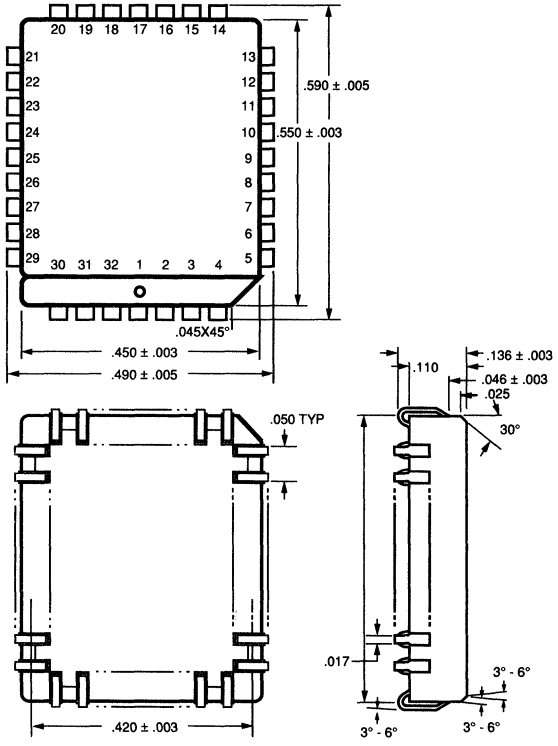


32-Pin 600 mil Plastic DIP



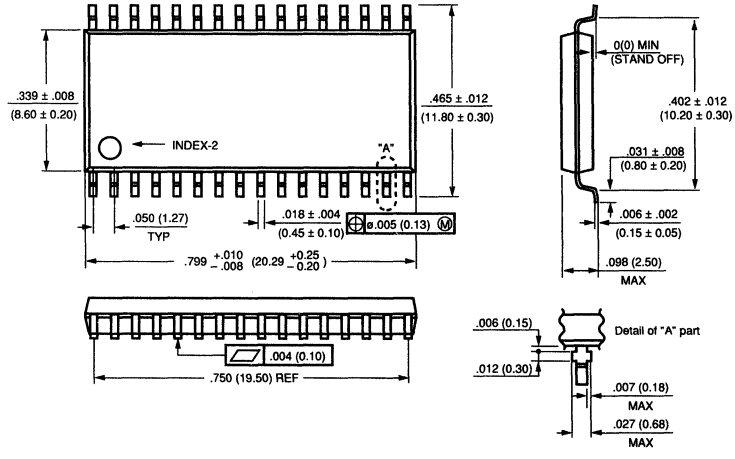
10

32-Pin Plastic Leaded Chip Carrier

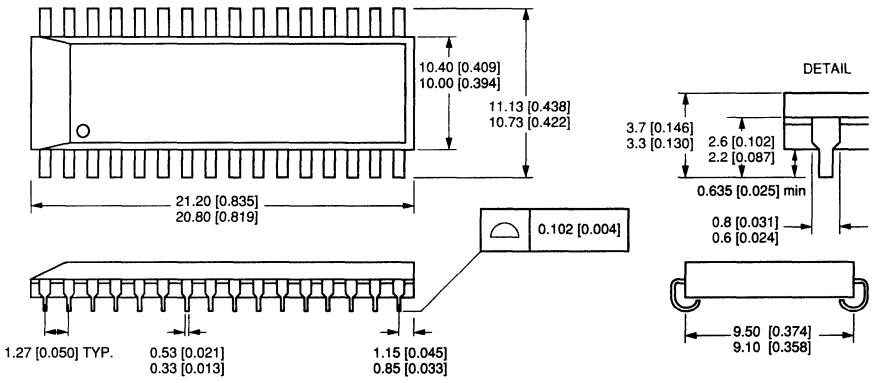


MS628128

32-Pin 330 mil SOG

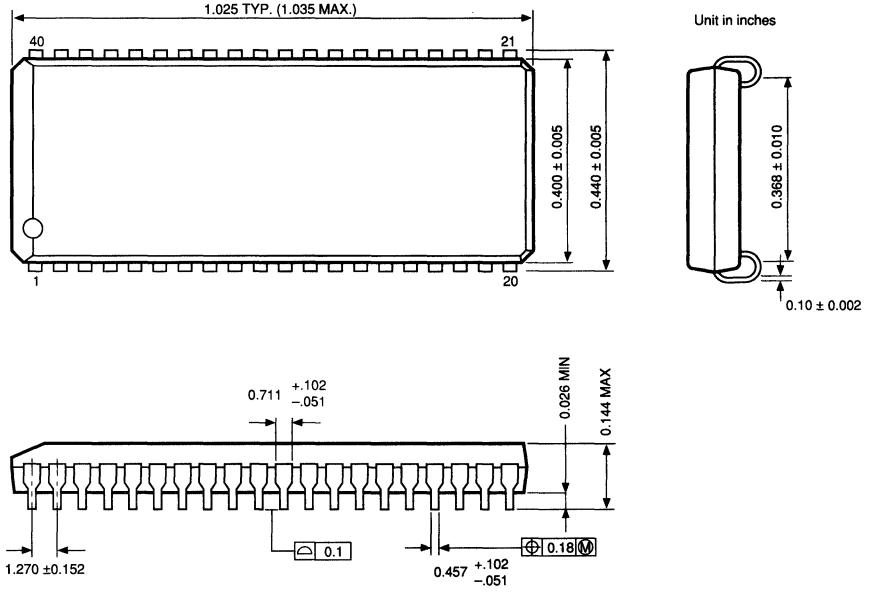


32-Pin 400 mil SOJ



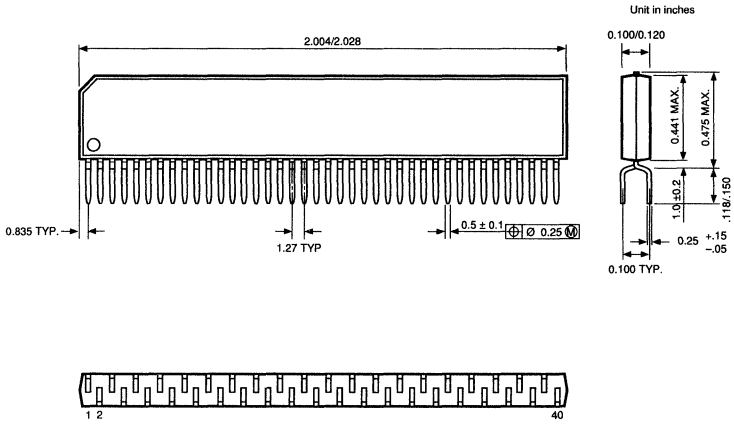
DIMENSIONS IN MM [INCHES]

40-Pin Plastic SOJ

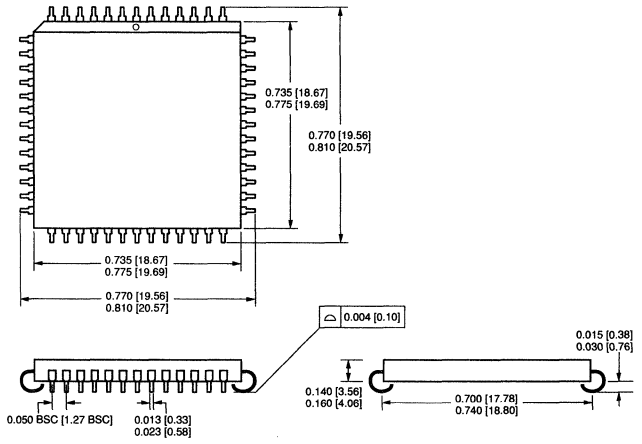


10

40-Pin Plastic ZIP

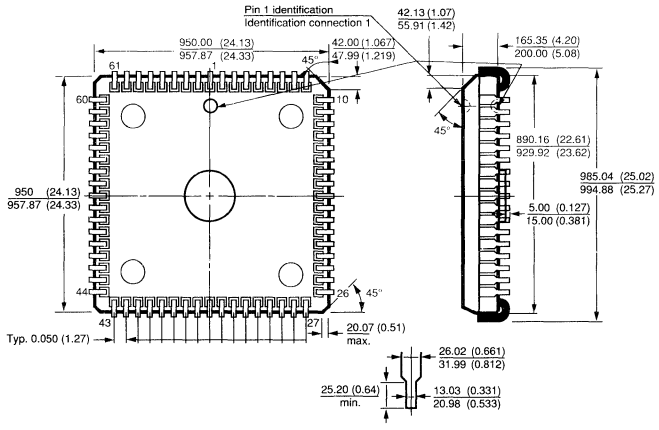


52-Pin Plastic Leaded Chip Carrier

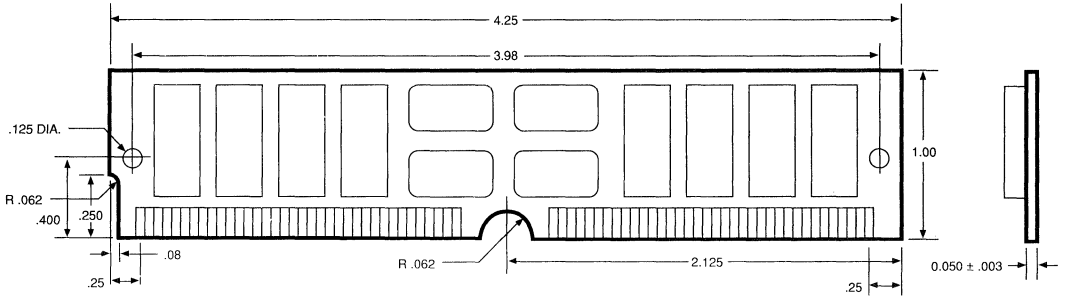


DIMENSIONS IN INCHES [MM]

68-Pin Plastic Leaded Chip Carrier

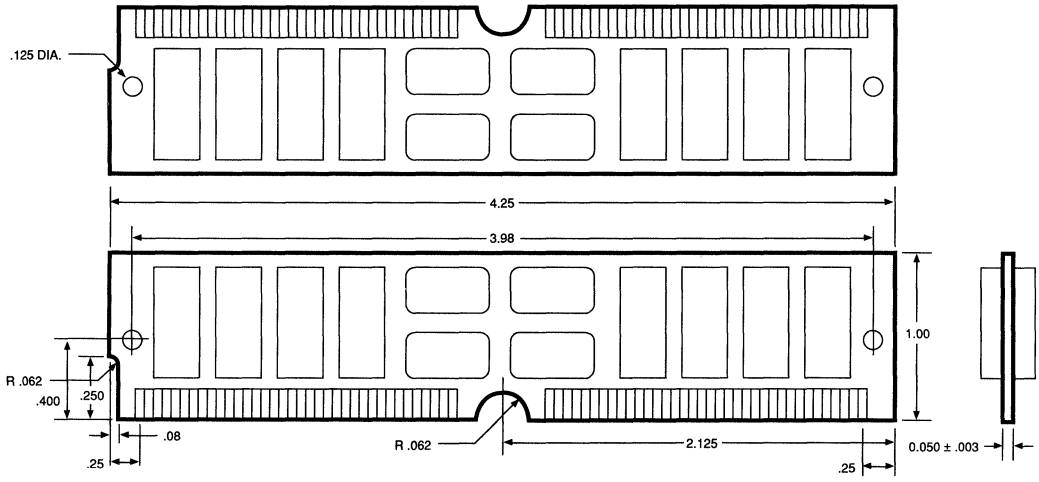


72-Pin SIMM #1



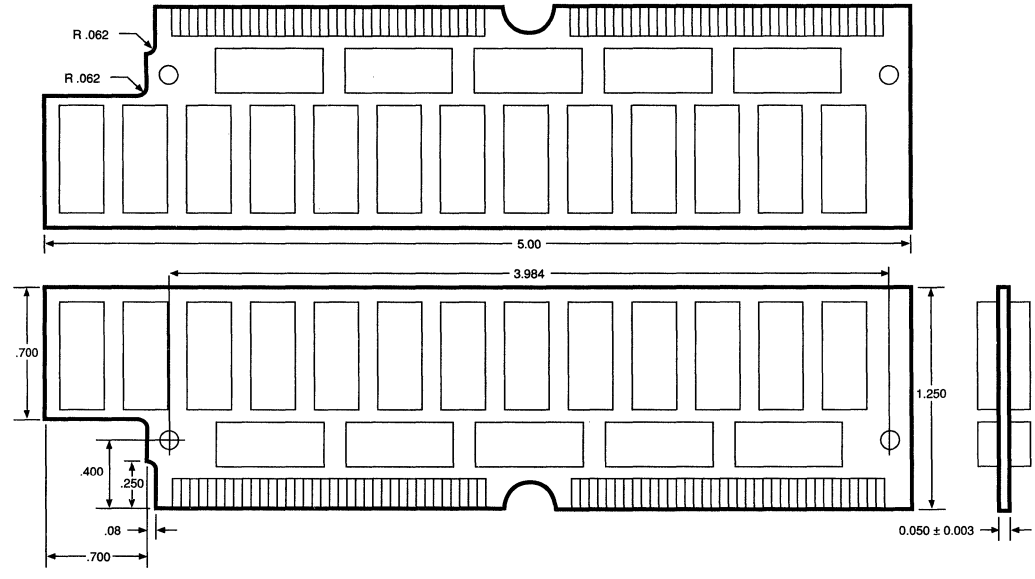
* Package dimensions subject to change without notice.

72-Pin SIMM #2



* Package dimensions subject to change without notice.

72-Pin SIMM #3



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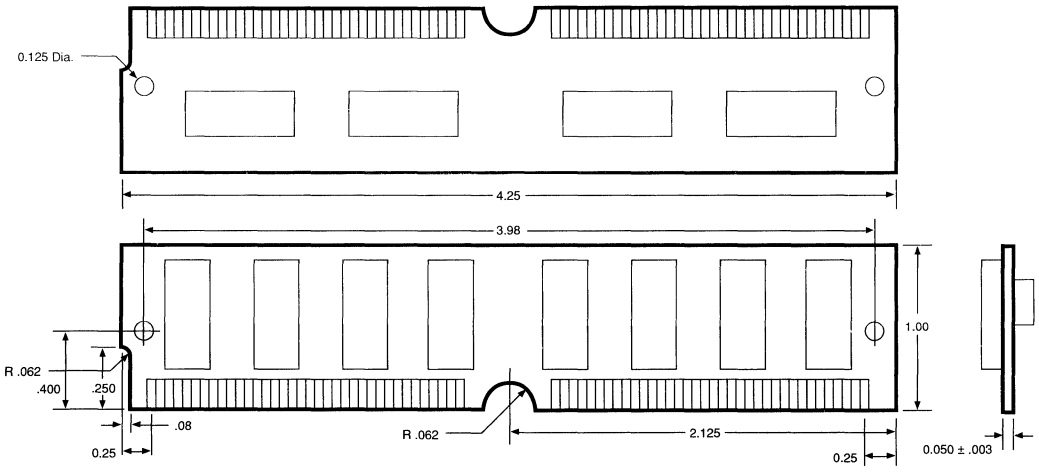

* Package dimensions subject to change without notice.

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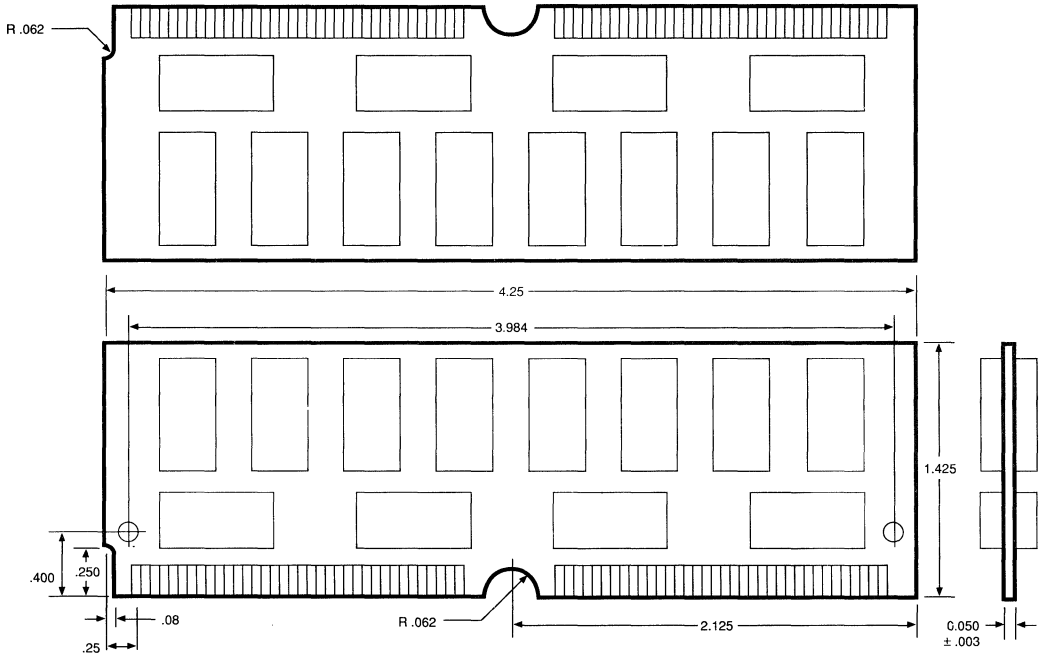
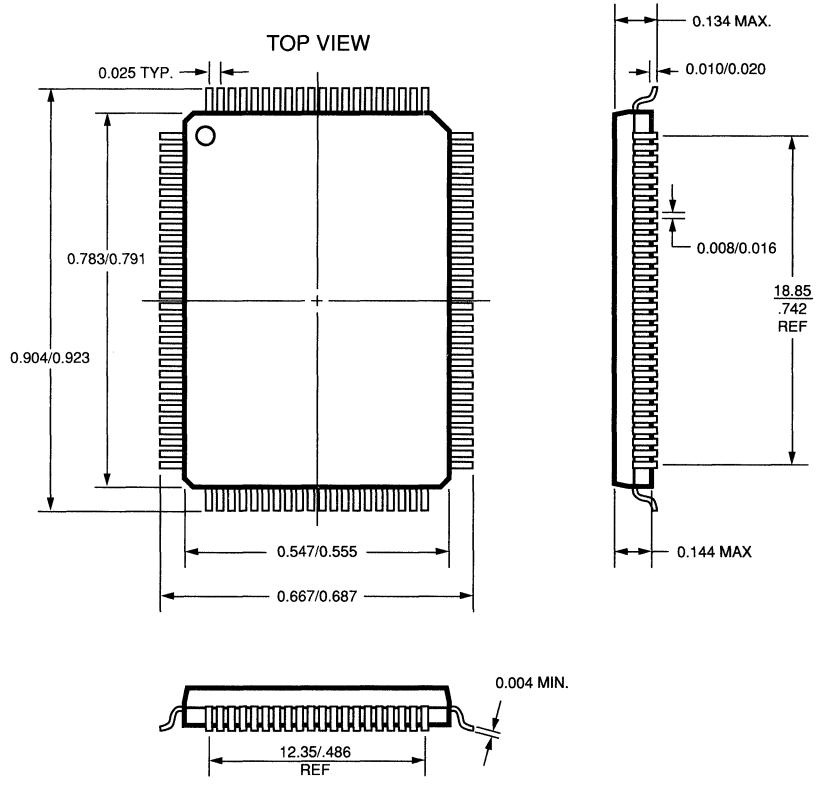
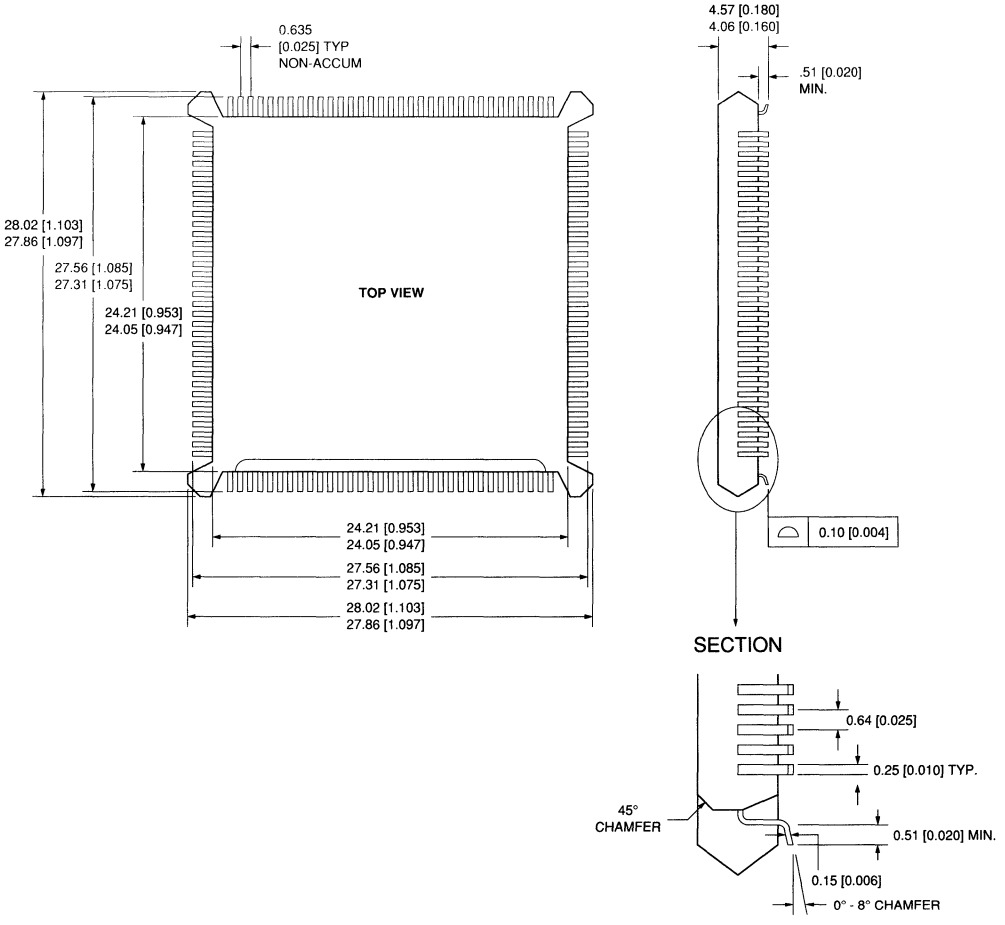


* Package dimensions subject to change without notice.

100-Pin QFP


TOP VIEW
0.025 TYP.
0.783/0.791
0.904/0.923
0.547/0.555
0.667/0.687
0.134 MAX.
0.010/0.020
0.008/0.016
18.85
.742
REF
0.144 MAX
0.004 MIN.
12.35/.486
REF

132-Pin QFP



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