AN-737A
Application Note

SWITCHED MODE POWER SUPPLIES-HIGHLIGHTING A 5-V, 40-A INVERTER DESIGN

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This application note identifies the features of various regulator circuits that are in use today in AC to DC power supplies. The note also illustrates how these circuits may be used as complementary building blocks in a system design. Primary emphasis is on switched mode regulators because they fill the present need for energy and space savings.

A complete 5-V, 40-A line operated inverter supply is described in detail including design procedures for the magnetic components. The inverter itself is a "state-of-the-art" design which features CMOS logic, high voltage power transistors, Schottky rectifiers and an opto-electronic coupler. It operates with a full load efficiency of 80% at a frequency of 20 kHz.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

There are many ways to build a power supply. The linear or "series pass" supply is one that has dominated the market for a long time. A more recent entry, the switched mode power supply, however, is coming of age. It has already replaced the linear regulator in many applications where high efficiency and small size are important considerations. In other cases, it is used in combination with linear regulators to obtain excellent regulation and transient response with improved efficiencies. Because the switched mode supply is now a proven design concept, it is being considered for use in most new designs and has become a very popular topic of conversation among design engineers.

In the first part of this article, the salient features of all types of dc power supplies are identified. A brief outline of several system approaches illustrating the most popular combinations of these circuits is presented. In the second part, the basic switched mode circuits are identified and a design example is presented. The example features a 120 V line operated 200 W inverter with a regulated output capable of supplying 40 A at 5 V.

Linear versus Switched Mode Supplies

Several voltage regulator circuits are available to the power supply designer. The most popular circuits in use today include:

1. Controlled Ferroresonant Transformer
2. SCR Phase Control
3. Linear Regulators
   a. Series
   b. Shunt
4. Switched Mode Regulators
   a. Switching Regulators
   b. Pulse Width Modulated (PWM) Inverters

In this article, switching regulators refer to one-transistor circuits whereas an inverter is considered to contain two transistors operating in a push-pull mode. The significant features of all these circuits are shown in Figure 1. In general, the table reflects typical size, cost, and performance data as found in current literature (magazines, technical brochures, etc.) Because the first three circuits all use bulky 60 Hz transformers for isolation between the line and load, they suffer the common disadvantage of large size. The switched mode regulators, however, operate above audio frequencies and use small 20 kHz power transformers. Because of the present emphasis on energy conservation, efficiency, and small size, the future appears bright for these switching supplies. The ferroresonant and SCR supplies are also making progress on the linear market, they are more efficient, and economical as well. The reason none of these supplies will completely replace the series regulator is also evident. The series regulator still offers the best regulation, ripple rejection, and transient response.

As shown in Figure 2, at the 100 W level, switching supplies cost more to build than series pass supplies. However, as was indicated earlier, they are still used at this power level and lower, when size is more important than cost. If we were to look at the characteristics of larger supplies, we would find that the performance data in Figure 1 remains basically the same. The size and weight numbers would tend to increase proportionally but the cost per watt has a tendency to decrease. Figure 2 offers a specific comparison between inverters and series pass regulators on this. The parts cost covers only the electronic components and heat sinks. Total parts cost is about $1/Watt at this level. Because inverter costs drop faster, they are more economical than series pass regulators at high power levels and cost about the same at the 200 to 300 W level. A couple of years ago, this break-even point was at the 500 W level.

Another advantage of transistor Switched Mode supplies is hold-up time which is better by an order of magnitude

Features	Ferroresonant	SCR	Series	Switching Regulator	Inverter
Major Advantage	Low Cost	Low Cost	Excellent Regulation	Small	Small
Major Disadvantage	Large	Poor Response	Poor Efficiency	Poor Response	Poor Response
*Cost (Electrical Parts)	$15	$15	$20	$25	$30
*Efficiency	80%	80%	30%	70%	70%
*Size (cu. in.)	600	200	300	70	70
*Weight (lbs.)	30	10	20	5	5
Regulation	3%	5%	0.1%	0.1	0.1
Ripple	160 mV	100 mV	5 mV	50 mV	50 mV
Maximum Power	2 kW	None	1 kW	200 W	1 kW
Transient Response	100 ms	100 ms	50 μs	1 ms	500 μs

*Note: These numbers apply to a 100 W supply.

FIGURE 1 – Comparative Features of DC Power Supplies in 1974

(20 ms versus 2 ms) due to high voltage energy storage. However, these supplies are more complex and generate more noise. Noise generation is roughly 10 times that of a series pass supply and since more sophisticated control circuitry is required, switches are also more difficult to design.

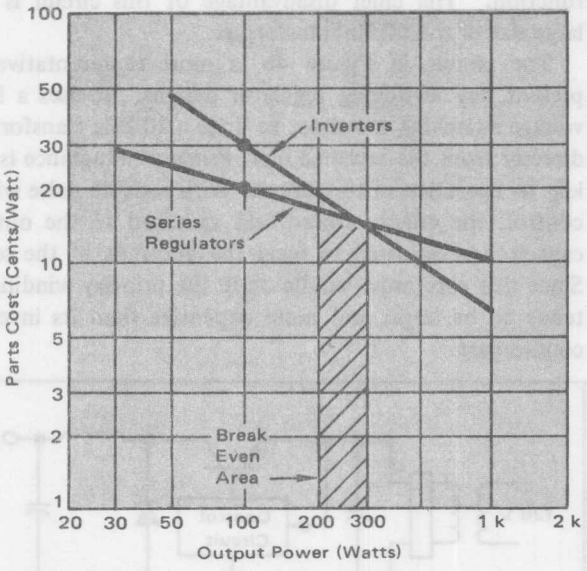


FIGURE 2 – Why Use Switching Supplies?

System Approaches

Now that the features and capabilities of various regulators have been reviewed, it is easier to understand the problem a designer faces in choosing which circuit or combination of circuits to use. The source of power is specified and would not be one of these design problems. When output power is 500 W or less, the single phase 120 V line is generally used. For larger supplies, three-phase power from a 208 V or 220 V source is used because energy storage in filter capacitors is more economical at these higher voltages. Tolerances on line voltage are typically +10% and -30%. Operation beyond these points can be prevented by voltage crowbars and shutdown circuits.

Before reviewing the popular circuit combination, it's well to consider the problem of power distribution. In a large system, such as a medium size TTL computer, up to 4 kW of power may be required at the 5 V level. This power capability may be designed into a large, centrally located supply or distributed in several smaller supplies at the "point of load". In the central supply, large bus bars are used to distribute the low-voltage, high-current power to the various bays and racks within the main frame. Distributed or "point of load" supplies may operate from the ac line or from a high voltage dc bus and supply from 50 to 250 Watts of power. There appears to be a general trend away from the single central supply to smaller distributed supplies at the 200 to 250 W level like the circuit shown in this note. Where a central supply is retained, it is used as a preregulator to power the high voltage bus. A ferroresonant supply is popular here because it also eliminates line transients. Of course, there are still many applications where all the power is for one load and it cannot be split up. In these cases, a single large regulated supply may be used or several small "current limited" supplies may be paralleled to make up the power.

Several possible system approaches to the design of a computer or industrial power supply are shown in Figure 3.[1] In each case there may be a requirement for multiple output voltages. The computer will use 5 V for the logic and 36 V, 48 V, and 100 V supplies for memories, read-

[1] See also reference #4

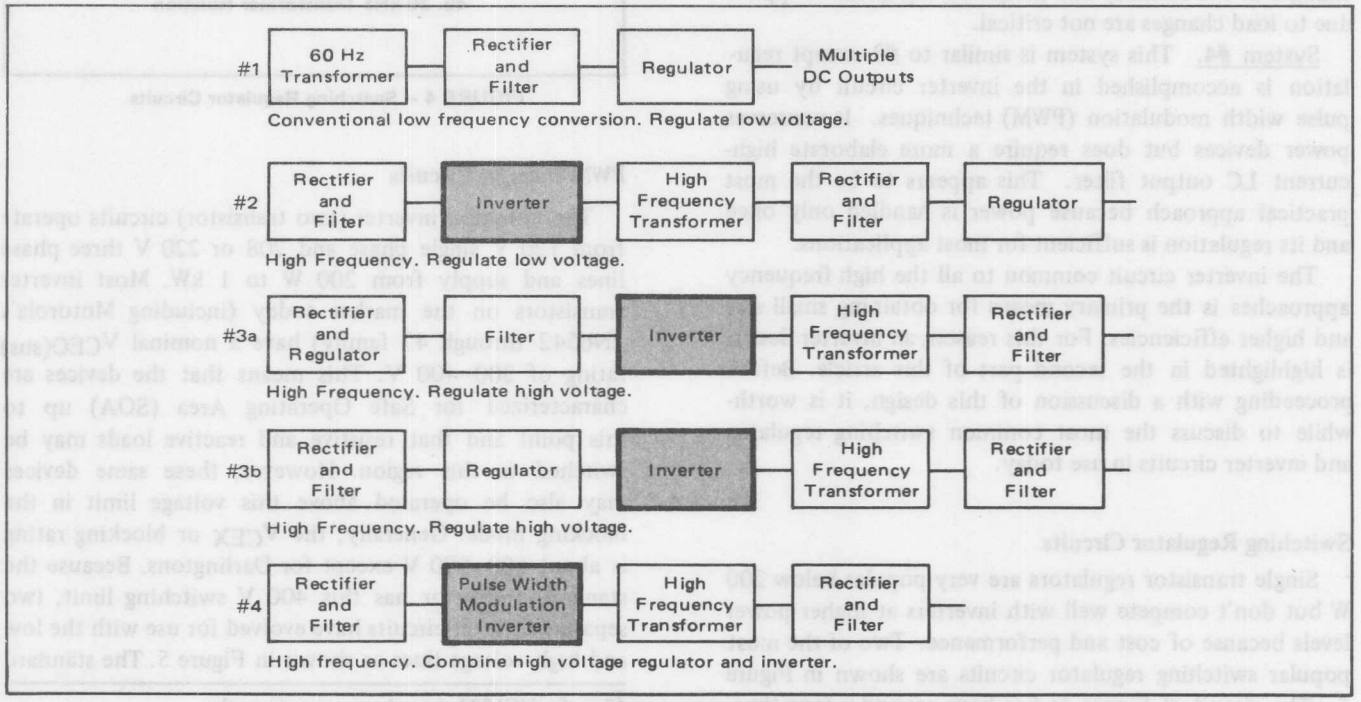


FIGURE 3 – Possible System Approaches

outs and peripheral equipment. Industrial systems generally have logic voltage requirements and may also need ±15 V and 24 V or 48 V for operational amplifiers and relay drivers. The advantages and disadvantages of each system are not too obvious, but can be brought out more clearly by some practical considerations. The first system uses a low frequency conversion technique while the remaining three systems operate at ultrasonic frequencies.

System #1. This is a conventional approach which uses a 60 Hz transformer or ferroresonant transformer to step down the line voltage for the rectifier and regulator circuits. It has been more economical in the past, but is bulky and generates more heat than the high frequency approaches.

System #2. This system uses the same building blocks required of all high frequency regulators but the sequence is varied. The line rectifier is followed by a high-voltage, high-frequency inverter and the regulation is accomplished at the low-voltage, high-current outputs of the inverter transformer. Each output can be individually regulated to provide precise voltage control over wide variations in load. There are two drawbacks to this approach: (1) several low-voltage, high-current regulators are required and (2), the efficiency will be lower than for the remaining approaches which regulate the high-voltage and low-current power.

System #3. This system uses high-voltage regulators to power the inverter which drives the low-voltage rectifiers and filters. The regulator may use SCR's for phase control (#3a) or high voltage transistors in either a linear or switching mode (#3b). Of the two approaches, the SCR may be preferred because of economy. In both this approach and approach #4, only one output can be regulated, usually the 5 V. This is not a serious drawback because line regulation is common to all outputs and slight changes in the memory and peripheral equipment supplies due to load changes are not critical.

System #4. This system is similar to #3 except regulation is accomplished in the inverter circuit by using pulse width modulation (PWM) techniques. It conserves power devices but does require a more elaborate high-current LC output filter. This appears to be the most practical approach because power is handled only once and its regulation is sufficient for most applications.

The inverter circuit common to all the high frequency approaches is the primary means for obtaining small size and higher efficiencies. For this reason, an inverter design is highlighted in the second part of this article. Before proceeding with a discussion of this design, it is worthwhile to discuss the most common switching regulator and inverter circuits in use today.

Switching Regulator Circuits

Single transistor regulators are very popular below 200 W but don't compete well with inverters at higher power levels because of cost and performance. Two of the most popular switching regulator circuits are shown in Figure 4. The circuit of Figure 4a has been around a long time. It uses a 60 Hz transformer for isolation and a low voltage switching transistor to supply a series of high frequency (20 kHz) power pulses to an LC filter. The duty cycle control circuit determines the average output voltage. It's popular today because it is simple to design and uses standard off-the-shelf components. Many of these circuits use a standard linear IC[2] regulator for the complete control function. The chief disadvantage of this circuit is the large size of the 60 Hz transformer.

The circuit in Figure 4b is more representative of present day switching regulator designs. It uses a high voltage switching transistor to drive a 20 kHz transformer directly from the rectified line. Primary inductance is the key to operation of this circuit. With variable pulse width control, the energy stored and switched to the output capacitor is adjusted to meet the demands of the load. Since this core must handle dc in the primary winding, it tends to be larger and more expensive than its inverter counterpart.

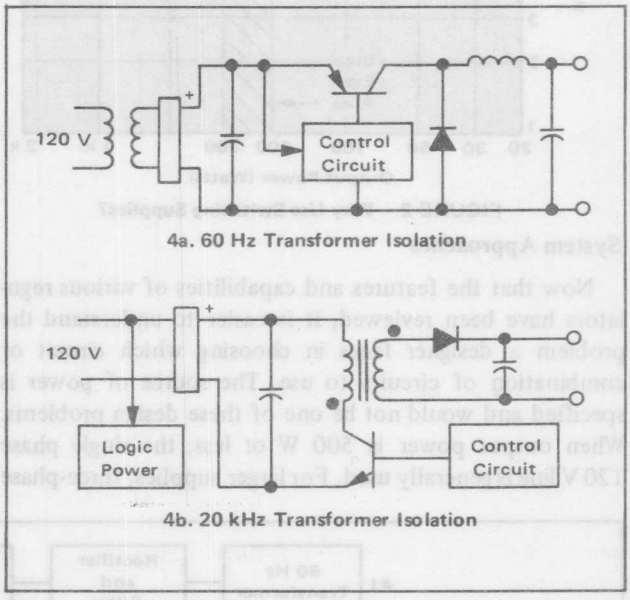


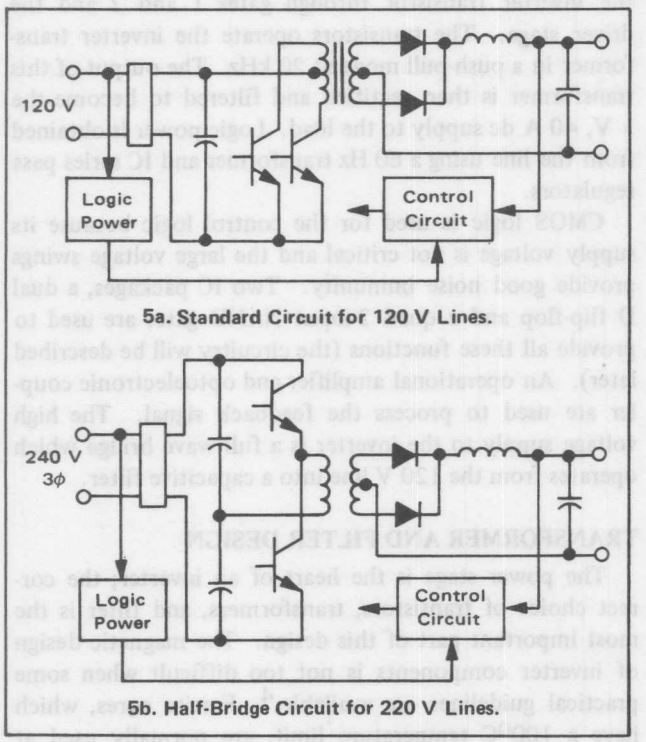
FIGURE 4 – Switching Regulator Circuits

PWM Inverter Circuits

The common inverter (two transistor) circuits operate from 120 V single phase and 208 or 220 V three phase lines and supply from 200 W to 1 kW. Most inverter transistors on the market today (including Motorola's 2N6542 through 47 family) have a nominal $V_{CEO(sus)}$ rating of 300-400 V. This means that the devices are characterized for Safe Operating Area (SOA) up to this point and that resistive and reactive loads may be switched in this region. However, these same devices may also be operated above this voltage limit in the blocking mode. Generally, the V_{CEX} or blocking rating is about 600-800 V except for Darlingtons. Because the standard transistor has this 400 V switching limit, two separate inverter circuits have evolved for use with the low and high voltage lines as shown in Figure 5. The standard

[2]See the MC1723 data sheet as an example.

inverter is used when 120 V power is available and the half bridge is generally chosen for 220 V applications. Both circuits operate in a similar fashion by alternately switching power to the 20 kHz transformer. The transformer output is rectified and the amplitude and duty cycle of the output voltage pulses determine the average output voltage. Because the output pulses are modulated to provide regulation, these circuits are known as pulse width modulated (PWM) inverters.



5a. Standard Circuit for 120 V Lines.

5b. Half-Bridge Circuit for 220 V Lines.

FIGURE 5 – Inverter Circuits

The transistor waveforms in Figure 6 represent the switching sequence for both circuits shown in Figure 5. Here it is easy to see why the dual voltage ratings of inverter transistors is important. In the standard inverter, the transistor switches collector current pulses (load current times the turns ratio) from the peak line voltage of 170 V. After some dead time, the opposite transistor is energized and the original must block twice the line voltage due to autotransformer action. In the half bridge operating from 220 V, the collector voltages are almost identical.[3] The dc bus is 340 V peak but each filter capacitor is charged to only 170 V. The transistors switch current at 170 V as before and again must block twice this voltage when the opposite side is energized. Actual waveforms are slightly different from the theoretical. The current pulse may have a spike on the leading edge and a slight positive slope due to the magnetizing current. An inductive kick during turn-off is usually present on the voltage waveform with some ringing during the dead time. These last effects are minimized by using an RC snubber across the primary to absorb the leakage reactance spikes and dampen the ringing.

Because the input filter capacitors in the half bridge must handle high RMS currents, these circuits tend to be

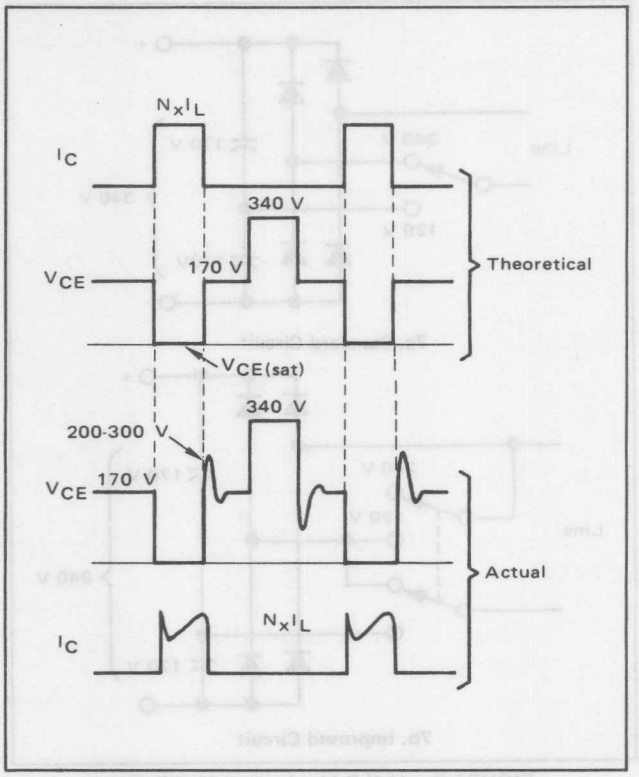


FIGURE 6 – Waveforms of Inverter Transistors

more expensive than the standard push-pull, but remain currently more popular for two reasons. One is that a coupling capacitor may be used to reduce transformer saturation problems (see reference 13 for the formula) and the second is that they can be made to conveniently operate from either 120 or 220 V (domestic or foreign). In these dual voltage designs, the capacitors are used as voltage doublers as shown in Figure 7. However, as the RMS currents are quite high in the 120 V mode, it is recommended that an additional switch contact be used to parallel the rectifier diodes as shown. The Motorola diode assemblies with ratings from 1 to 20 A are excellent for this application as the individual diodes are matched and will share current well.

The control circuits for these inverters may be located at the load or on the primary side of the transformer. Generally, power for these circuits is obtained from the ac line using either a free-running inverter or a standard 60 Hz transformer and series pass regulator. In the half bridge, the control circuits are grounded at the load. Voltage sense for the feedback signal is direct and transformers are used to couple the drive signals to the power transistors. The standard inverter may use this system or ground the control circuits at the power transistors. This latter approach simplifies the drive circuits and generally improves switching efficiency. Isolation is maintained by using an optoelectronic coupler in the feedback loop.

[3]For additional information on the half bridge inverter, see references #9, #10, and #13.

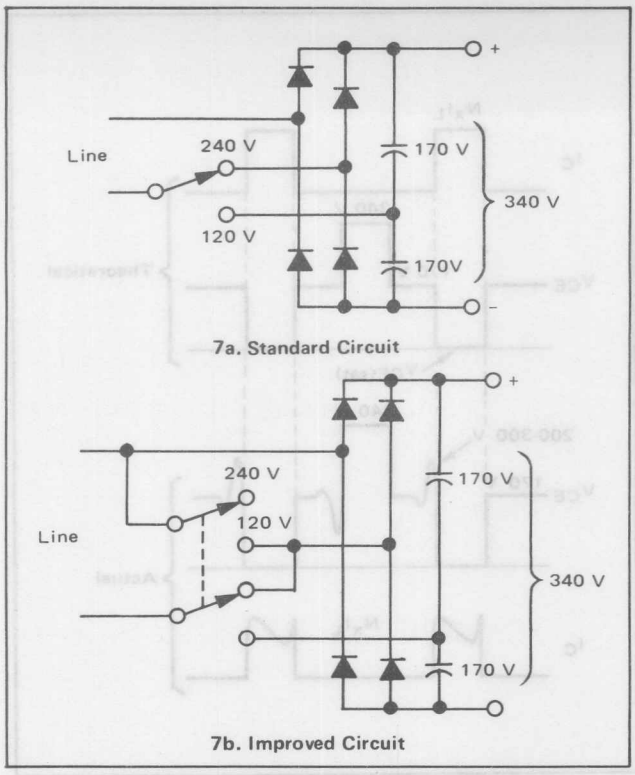


FIGURE 7 – Half Bridge Inverter Modified to Accept 120 or 240 V Inputs

A 5 V-40 A INVERTER SUPPLY EXAMPLE

This example deals with the design and performance of a 200 W inverter supply. The design specifications are as follows:

Input: 120 Vac ±10% @ 60 Hz
Output: 5 V @ 40 A (50 A capability; wire size, etc.)
Line/Load Regulation: ±1% (Half load to full)
Ripple: 120 Hz 10 mV_{RMS}
40 kHz 10 mV_{RMS} (Switching Frequency 20 kHz)
Ambient Temperature: 0-70°C
Efficiency: 70%

The standard inverter configuration is used with the control circuits on the primary side and an optoelectronic coupler for feedback. The block diagram is shown in Figure 8. The oscillator (an astable multivibrator) generates clock pulses which alternately set the outputs of the phase splitter (a bistable flip-flop) high. These clock pulses also enable a timing circuit in the pulse width control (a one-shot or monostable multivibrator). The splitter provides the mean for alternating these control pulses to the inverter transistor through gates 1 and 2 and the driver stage. The transistors operate the inverter transformer in a push-pull mode at 20 kHz. The output of this transformer is then rectified and filtered to become the 5 V, 40 A dc supply to the load. Logic power is obtained from the line using a 60 Hz transformer and IC series pass regulators.

CMOS logic is used for the control logic because its supply voltage is not critical and the large voltage swings provide good noise immunity. Two IC packages, a dual D flip-flop and a quad 2-input NAND gate, are used to provide all these functions (the circuitry will be described later). An operational amplifier and optoelectronic coupler are used to process the feedback signal. The high voltage supply to the inverter is a full wave bridge which operates from the 120 V line into a capacitive filter.

TRANSFORMER AND FILTER DESIGN

The power stage is the heart of an inverter; the correct choice of transistors, transformers, and filter is the most important part of this design. The magnetic design of inverter components is not too difficult when some practical guidelines are available.[4] Ferrite cores, which have a 100°C temperature limit, are normally used at 20 kHz because they have very little core loss. This loss increases slightly with 0.5 mil nickel-iron cores such as Permalloy and Orthonol, which must be used for higher

[4]See also reference #8.

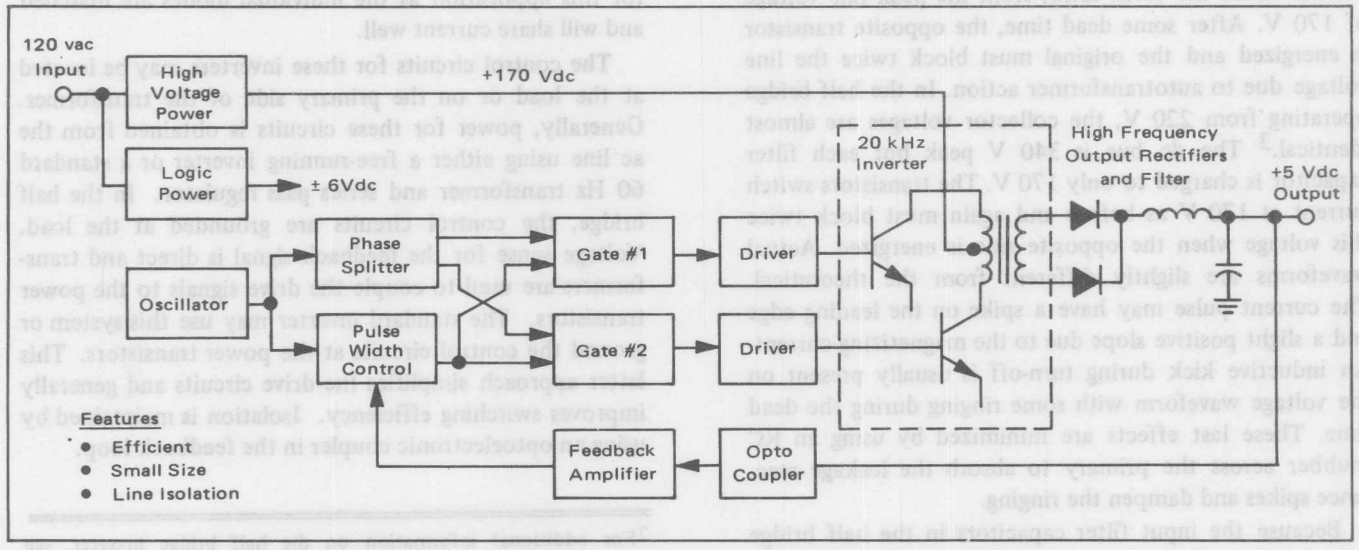


FIGURE 8 – Block Diagram 5-V, 50-A Line Operated Switched Mode Power Supply

temperature applications. For transformers, the best coupling comes from toroids, with pot cores a close second. Since toroids are difficult to wind and pot cores tend to trap heat (ferrite is a ceramic and a good insulator), C and E cores are generally used above 200 W. In addition to being easy to wind with bobbins, these latter cores facilitate the use of foil or strap to improve the winding efficiency of high current secondaries (> 50 A).

POWER TRANSFORMER

In this design, efficiency was more important than size and an oversize pot core was used for the transformer to obtain the following advantages:

1. Few turns required to operate at low flux densities
2. Low core loss (operate at 20% of B_m)
3. Low copper loss (minimized turns)
4. Good coupling
5. Relatively easy to wind (the #10 secondary was somewhat difficult to shape)

In transformer design, the turns ratio and wire size are calculated first, then the core is selected. The information in Figure 9 of transformer waveforms at low line is used to find the required turns ratio. The information required includes:

1. Low line voltage
2. Input ripple
3. Output voltage
4. Minimum dead time (and frequency)
5. Output rectifier and filter losses

The low line specification of 110 V and 20 V ripple voltage (peak-to-peak) gives a minimum dc input to the primary windings of 130 V. With 5 μs of dead time between pulses, the duty cycle is 80% and 6 V pulses are required at the filter to obtain 5 V output. Assuming the rectifier drops (0.5 V) and filter loss at full load is 1 V, the secondary voltage pulses must be 7 V minimum. An additional 10% safety factor (0.7 V) is recommended to make up for miscellaneous input rectifier, transistor, and transformer losses. The required turns ratio (N), is therefore:

$$N = V_p/V_s = 130\ V/7.7\ V = 16.8 \simeq 16 \qquad (1)$$

With the turns ratio and the control logic set to limit duty cycle to 80%, the supply stayed in regulation at 110 V and dropped out with the line at 100 V.

Some wire tables recommend using 1000 CM/A (circular mils per ampere) or 1000 A/sq inch but most designers use anywhere from 300 to 500 CM/A as a guideline. With 50 A in the secondary and a 16:1 turns ratio, primary current pulses are about 3 A. Since both windings are center-tapped, current pulses cannot exceed a 50% duty cycle. Therefore, the wire size was chosen for RMS values of 35 A and 2 A. Number 10 (12,000 CM) was chosen for the secondary and number 20 (1000 CM) for the primary. Two number 13 (6000 CM) or four number 16 (3000 CM) were considered to make the secondary easier to wind, but the pot core does not have space available to bring out the interconnections.

To determine the proper core and number of turns three steps are required as follows:[5]

Step 1. Find the minimum core size and choose a core using

$$A_c A_w \geq \frac{2P_o}{f\,B_m} \times 10^{11}\ CM\ cm^2 \qquad (2)$$

where A_c = core area (cm^2)
A_w = window area (CM)
P_o = output power
f = frequency
B_m = saturation flux density (gauss)

A typical ferrite material has $B_m = 3000$ gauss. For this 200 W, 20 kHz inverter

$$A_c A_w \geq \frac{2 \times 250 \times 10^{11}}{20\ k \times 3\ k} = 0.83 \times 10^6\ CM\ cm^2$$

[5]The equations are from reference #7.

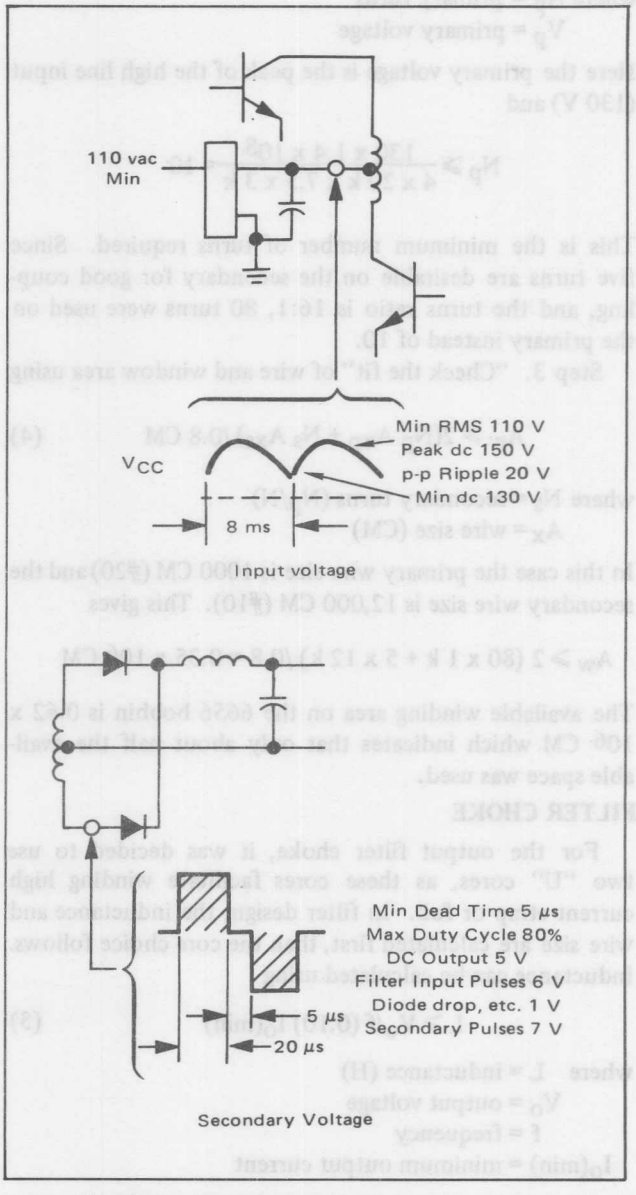


FIGURE 9 – Transformer Waveforms at Low Line

Two cores available from the Ferroxcube catalog with size information are listed in Table 1.

TABLE I – Ferroxcube Cup Cores

Core Number	A_c cm^2	A_w* in^2	A_w CM	A_cA_w CM $cm^2 \times 10^6$
4229	2.7	0.22	0.22×10^6	0.6
6656	7.5	0.62	0.62×10^6	4.6

*Note: This is the area available on the standard bobbin.

Because the formula uses the conservative wire rating of 1000 CM/A, it would be possible to use the 4229 core for this design. However, since it is desirable to operate well below B_m to minimize core loss, the 6656, which is oversize by a factor of five, is used.

Step 2. Find the required primary turns using

$$N_p \geq \frac{V_p \times 10^8}{4 f A_c B_m} \qquad (3)$$

where N_p = primary turns
V_p = primary voltage

Here the primary voltage is the peak of the high line input (130 V) and

$$N_p \geq \frac{130 \times 1.4 \times 10^8}{4 \times 20\,k \times 7.5 \times 3\,k} = 10$$

This is the minimum number of turns required. Since five turns are desirable on the secondary for good coupling, and the turns ratio is 16:1, 80 turns were used on the primary instead of 10.

Step 3. "Check the fit" of wire and window area using

$$A_w \geq 2(N_p A_{xp} + N_s A_{xs}) / 0.8 \text{ CM} \qquad (4)$$

where N_s = secondary turns (N_p/N)
A_x = wire size (CM)

In this case the primary wire size is 1000 CM (#20) and the secondary wire size is 12,000 CM (#10). This gives

$$A_w \geq 2\,(80 \times 1\,k + 5 \times 12\,k)\,/0.8 = 0.35 \times 10^6 \text{ CM}$$

The available winding area on the 6656 bobbin is 0.62×10^6 CM which indicates that only about half the available space was used.

FILTER CHOKE

For the output filter choke, it was decided to use two "U" cores, as these cores facilitate winding high current strap or foil. In filter design, the inductance and wire size are calculated first, then the core choice follows. Inductance can be calculated using

$$L \geq V_o/f\,(0.10)\,I_o(\text{min}) \qquad (5)$$

where L = inductance (H)
V_o = output voltage
f = frequency
I_o(min) = minimum output current

In this case, the minimum output current was chosen to be 20 A (just less than half load). The frequency is 40 kHz at this point (from the full wave rectifiers); therefore

$$L \geq \frac{5}{40\,k\,(0.10)20} \simeq 60\,\mu H$$

The 0.10 factor limits choke current variations to 10% at light loads. To conserve space, it is possible to allow 100% current variations and use a 6 μH choke. However, most designs follow the 10% guideline.

Wire size is determined using 500 CM/A as the guide. The choke current can be 50 A continuous, so two 1.125" by 10 mil copper strap were used for the winding. Strap or foil is easier to wind than the large wire and is also preferred as it will lie close to the core for good magnetic coupling.

Four steps are required to choose the core and determine the proper number of turns and the required air gap size as follows.[6]

Step 1. Find the minimum core size and choose a core using

$$A_cA_w \geq \frac{A_x\,LI \times 10^8}{0.8\,B_m} \qquad (6)$$

where I = Saturation current level

Ferrites used for U cores have B_m = 3800. For this design, it was already determined that a 60 μH, 50 A choke is required and that the strap size is 22,500 CM (2.25" x 10 mil"). Therefore

$$A_cA_w \geq \frac{22.5\,k \times 60\,\mu \times 50 \times 10^8}{0.8 \times 3800} = 2.3 \times 10^6 \text{ CM cm}^2$$

Ferroxcube catalog information on two possible U cores is shown in Table II.

The 1F10 core is a good choice here, but a 1F5 was used instead as it was available.

Step 2. Find the required number of turns using

$$N = \frac{LI}{A_cB_M} \times 10^8 \qquad (7)$$

In this case, A_c = 6.45 and

$$N = \frac{60\,\mu \times 50 \times 10^8}{6.45 \times 3800} = 14 \text{ turns}$$

Step 3. "Check the fit" of wire and window area using

$$A_w \geq NA_x/0.8 \qquad (8)$$

which gives

The core used has a window area of 5.0×10^6 CM which allows plenty of room for this winding. Mylar tape was used to insulate the layers.

[6]The equations are from reference #7.

TABLE II – Ferroxcube U-U Cores

Core Number	A_c cm^2	A_w* in^2	A_cA_w CM $cm^2 \times 10^6$
1F10	2.04	1.5	3.0
1F5	6.45	5.0	32

*Note: Obtained from inside core dimensions.

Step 4. Determine the air gap required to prevent saturation using

$$l_g = \frac{0.4\pi NI}{B_M} - \frac{l_m}{\mu} \qquad (9)$$

where l_g = air gap length (cm)
l_m = magnetic path length (cm)
μ = core permeability

Using the catalog, we find that only 3C5 material is available for this U core configuration (with $\mu = 2000$) and that $l_m = 31.5$ cm. Therefore,

$$l_g = \frac{0.4\pi \times 14 \times 50}{3800} - \frac{31.5}{2000}$$

$$= 230 \times 10^{-3} - 15 \times 10^{-3} = 215 \times 10^{-3} \text{ cm}$$

Converting l_g to inches gives a required gap of 80 mils or 40 on each side of the core. It should be noted that the gap reluctance is much higher than the core reluctance (230:15) and that it therefore is controlling L and I. This being the case, if the gap is doubled, L halves and I doubles. If the turns are doubled, L increases by 4 (N^2) and I is halved. Therefore, if both the turns and gap are doubled, I remains the same but L doubles. When there is additional winding space available, it is possible to increase the inductance by filling this area even though the gap must be increased appropriately to prevent saturation at the rated current.

In this case, these relationships were used to check the magnetic design just completed. 140 turns (instead of 14) of light wire were placed on the core and it was gapped at 80 mils. L and I were then measured at relatively low test levels resulting in 6 mH of inductance which saturated just over 5 A. Thus, the calculated 14 turns give us 60 μH at 50 A.

Filter Capacitor

With the completion of the transformer and filter designs, the remaining passive component required in the power stage is the output filter capacitor. The size of this capacitor is determined using[7]

$$C \geq \frac{(V_{in} - V_o)V_o}{2Lf^2 V_{in} v_o} \times 10^6 \ \mu F \qquad (10)$$

where C = capacitor size (μF)
V_{in} = filter input voltage (V)
V_o = filter output voltage (V)
v_o = peak to peak output ripple at the switching frequency (V)

There is no dependance on load in this formula, as only the changes in inductor current must be filtered out. These changes are dependent only on voltage, inductance and frequency and not on the average inductor (or load) current. With a nominal 160 V in to the 16:1 power transformer, the input amplitude to the filter is 10 V. Ripple frequency is 40 kHz and the ripple specification is 10 mV (RMS) or 28 mV peak to peak. This gives

$$C \geq \frac{(10 - 5)\ 5 \times 10^6}{2 \times 60\ \mu\ (40\ k)^2\ 10 \times 28\ m} = 460\ \mu F$$

A 500 μF four terminal (high frequency) capacitor could be used but a lower cost standard aluminum electrolytic was chosen instead. Because series resistance and inductance are higher with the standard, a larger size (2000 μF) was required to obtain the desired performance.

POWER STAGE

The power stage is comprised of the following circuits:

1. High voltage power supply
2. Logic power supply
3. Drivers
4. Power transformer and transistors (inverter)
5. Output rectifiers and filter

The schematic of these circuits is shown in Figure 10. A bridge rectifier and capacitive filter are connected directly to the 120 Vac line to form the high voltage supply. The output is 160 Vdc with $\approx$ 20 V peak-to-peak of 120 Hz ripple. These voltage variations are attenuated 60 dB by the control circuits resulting in $\approx$ 10 mV of low frequency ripple at the load.

The logic supplies are obtained using a 15 W filament transformer, bridge rectifier, and filter to operate ±6 V three terminal IC regulators (the MC7806 and 7906). The logic is connected between these two low-voltage supplies.

The two voltages are used with a push-pull drive stage to provide both positive and negative base drive to the inverter transistors. When the logic signal is high, the 2.0 A MPS-U51 saturates and supplies 1 A to the base of the 2N6306 inverter power transistor. When the logic is low, the 1.5 A MPS-U95 darlington operates in a current limited mode during storage time and then applies -5 V to the base to hold the inverter transistor off. Figure 11 shows this base current waveform at rated load. Storage time is under 2 μs with these fast switching Uniwatt▲ drivers and will increase slightly at lighter loads.

Power Transistors

Motorola 2N6544 power transistors were used in the inverter because they are fast and economical. These transistors have an 8 A current rating, but are specified for beta and switching speed and used here at 3 A of collector current. The switching sequence and load lines at full load of these devices (before and after shaping) are shown in Figure 12. A current spike observed during turn-on was contained using 80 μH of inductance on a common pot core in series with each collector. This improved the load line and reduced turn-on losses in

[7] This equation is from reference #3.

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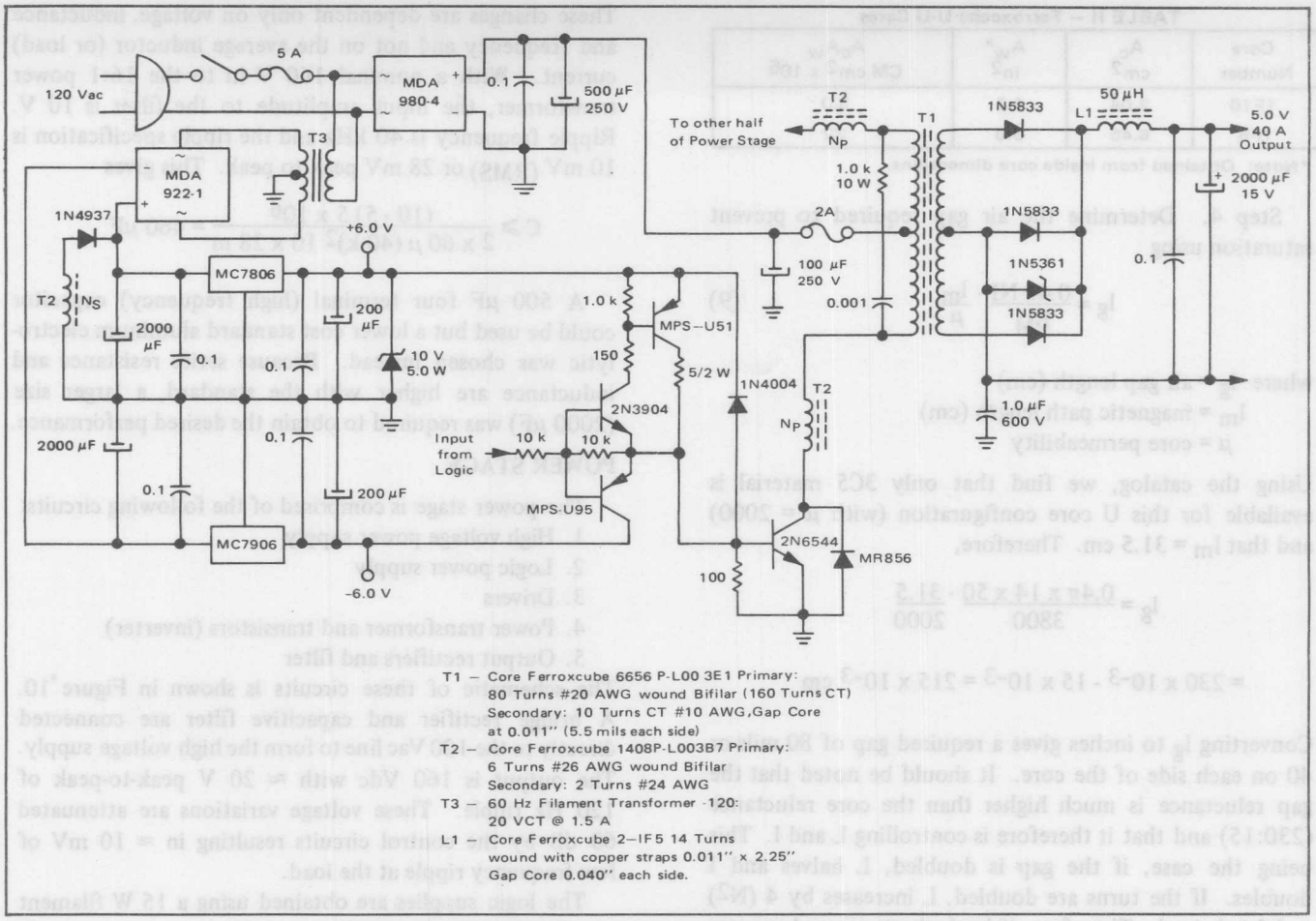

T1 – Core Ferroxcube 6656 P-L00 3E1 Primary: 80 Turns #20 AWG wound Bifilar (160 Turns CT) Secondary: 10 Turns CT #10 AWG, Gap Core at 0.011" (5.5 mils each side)

T2 – Core Ferroxcube 1408P-L003B7 Primary: 6 Turns #26 AWG wound Bifilar Secondary: 2 Turns #24 AWG

T3 – 60 Hz Filament Transformer -120: 20 VCT @ 1.5 A

L1 – Core Ferroxcube 2–IF5 14 Turns wound with copper straps 0.011" x 2.25" Gap Core 0.040" each side.

FIGURE 10 – Power Inverter Stage For Line Operated 5-V – 40-A Supply

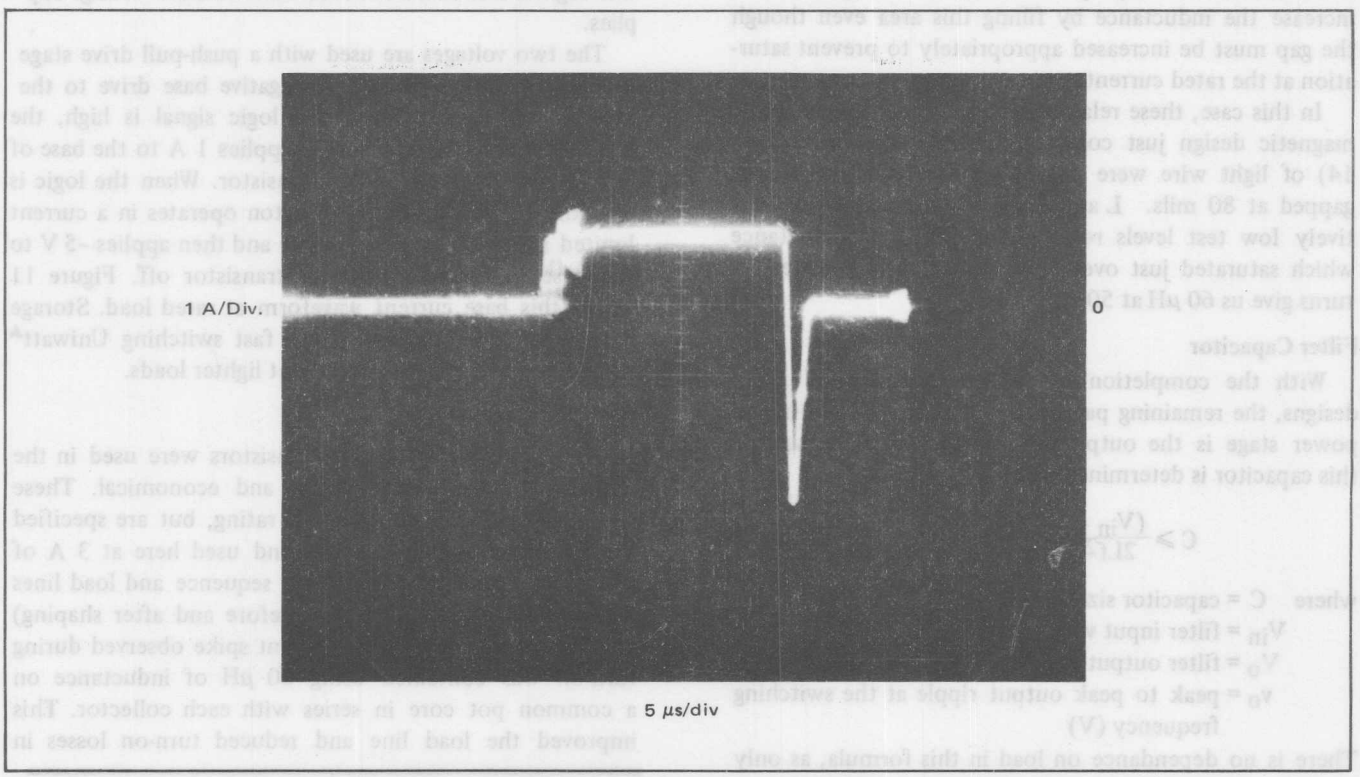

FIGURE 11 – Base Current

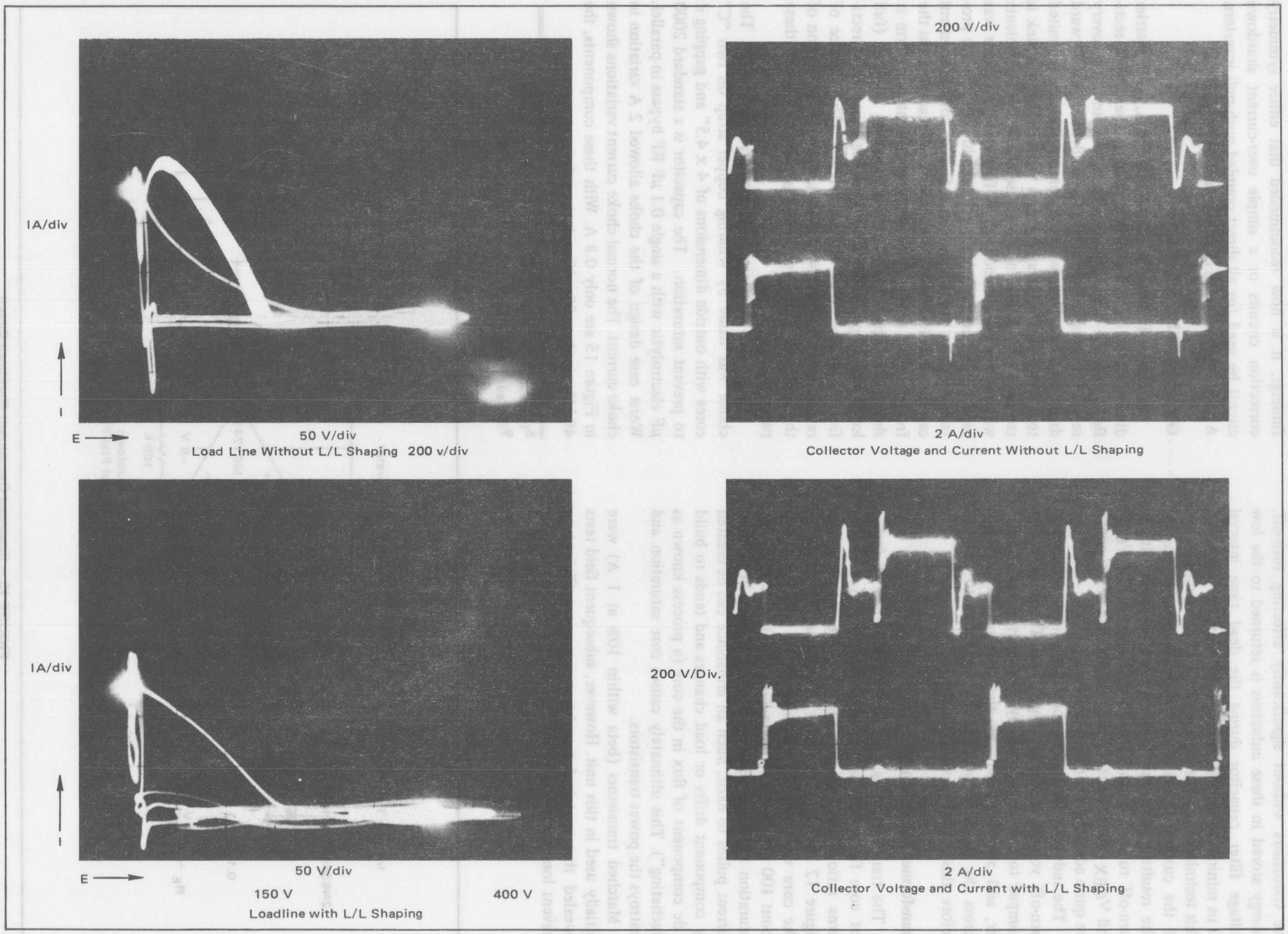

FIGURE 12 – Load Lines

the transistors without significantly affecting turn-off. Energy stored in these inductors is returned to the low voltage filter capacitor during the dead time interval (5 μs minimum) by the secondary winding on this core.[8] This technique therefore affords very efficient suppression of the current spikes with controlled voltage clamps. The resulting load line shows resistive switching during turn-off to 150 V and blocking to 400 V. The V_{CEO} and V_{CEX} ratings on this device are 300 and 650 V which are quite adequate for this application.

The inductive kick from the core can be observed as turn-off voltage spikes in Figure 12. These spikes are clamped to twice the supply by diodes across each transistor, and are "snubbed" by the standard RC network across the primary to allow the transistors to turn off before this voltage level is reached.

Transformer Saturation

The transformer, as discussed earlier, is a 2.5" ferrite pot core from Ferroxcube, hand wound with a 16-to-1 turns ratio. The collector current pulses of 2.5 A in Figure 12 therefore represent a load current of 40 A. The core was gapped empirically at 10 mils to provide about 100 mA of magnetizing current. This increases the saturation level and allows a slight imbalance in primary current pulses to exist. Such an imbalance can be created by component drifts or load changes and tends to build a dc component of flux in the core (a process known as "racheting"). This ultimately causes core saturation and destroys the power transistors.

Matched transistors (beta within 10% at 1 A) were initially used in this unit. However, subsequent field tests revealed that matched transistors are not sufficient to prevent long term transformer saturation. Based on these findings, it is now recommeded that either symmetry correction circuits or a simple over-current shutdown circuit be used for all direct coupled push-pull inverters. A suggested shutdown circuit is shown in Figure 13.

Output Rectifiers and Filter

Because efficiency is important, 50 A, 30 V barrier diodes (Motorola 1N5833) are used as the output rectifiers, although they are more expensive than fast recovery rectifiers. These diodes are fast and have low forward drops (0.5 V). However, junction temperature is limited to 100°C and for this reason, a fairly large heat sink is required (0.5°C/W) to operate safely in 70°C ambients without forced air cooling. A free wheeling diode was used but carries little current. All three diodes are protected against voltage transients (a 1 μs voltage transient can cause shorts) by a 27 V, 5 W zener placed across the free-wheeling diode. The rectifier current waveform is shown in Figure 14. The peak current is 40 A (full load) and drops to half during the dead time (each rectifier shares the filter choke current). The absence of reverse recovery spikes in this picture is an indication of the excellent high speed blocking characteristics of these parts.

The output filter elements were discussed earlier. The choke was made by winding copper strap on two "C" cores with outside dimensions of 4 x 4.5" and gapping it to prevent saturation. The capacitor is a standard 2000 μF electrolytic with a single 0.1 μF RF bypass in parallel. Worst case design of the choke allowed 2 A variation in choke current. The normal choke current variations shown in Figure 15 are only 0.8 A. With these components, the 40 kHz ripple is 25 mV peak to peak.

[8]For additional information, see references #1, 2, and 12.

[9]For additional information, see reference #11

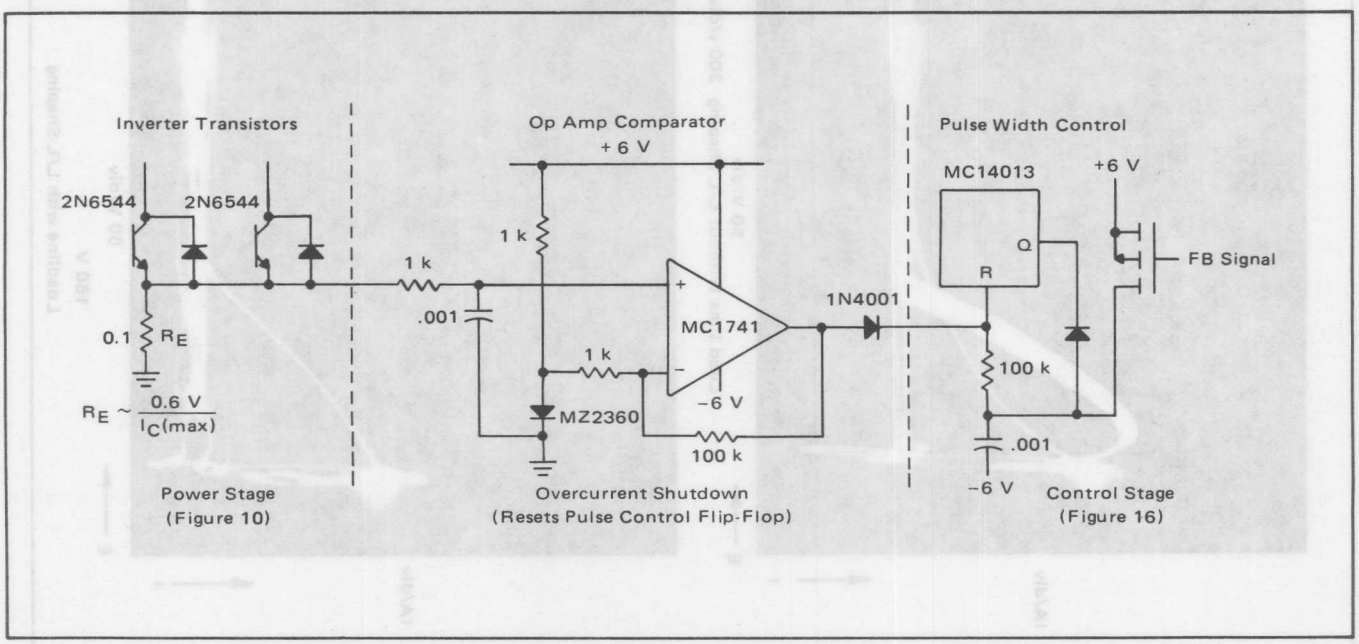

FIGURE 13 – Suggested Overcurrent Shutdown Circuit

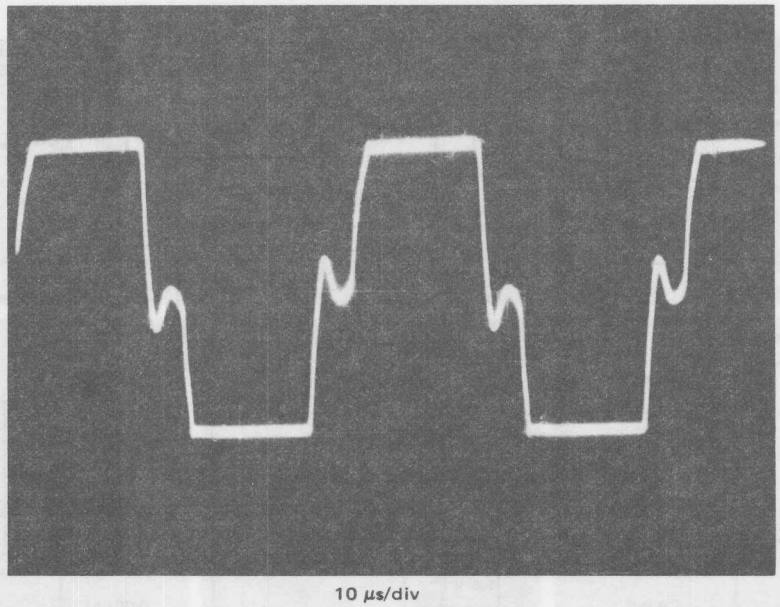

FIGURE 14 – Secondary Current

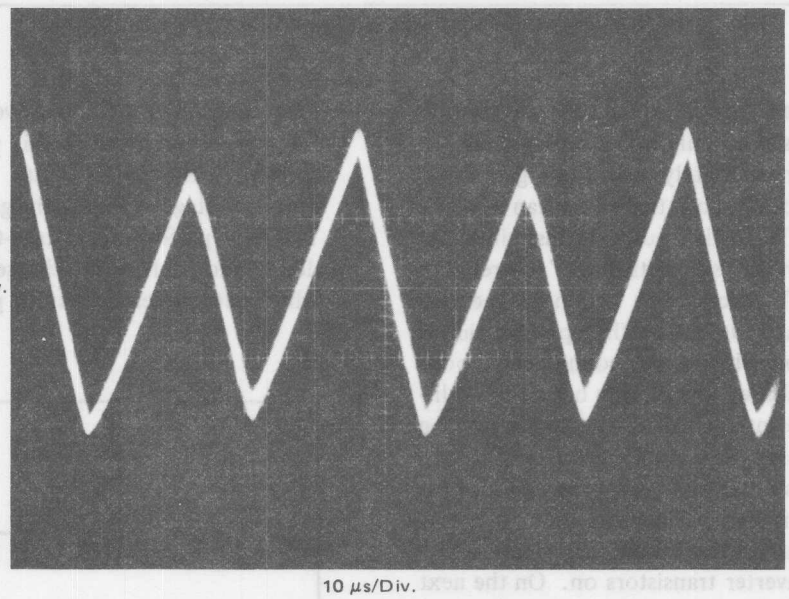

FIGURE 15 – Filter Inductor Current

CONTROL STAGE DETAILS

The basic functions of the control stage were discussed earlier in the block diagram section. The schematic of this stage is shown in Figure 16. The various circuits required for the control function include:

1. Oscillator
2. Phase splitter
3. Pulse width control
4. Gates
5. Opto isolation
6. Feedback amplifier

Functions 1 and 4 are obtained from a single CMOS package, the MC14001 quad 2-input NOR gate. A second CMOS package (the MC14013), a dual D flip-flop is used to implement functions 2 and 3. Two other dual-in-line IC packages, the 4N28 optoelectronic coupler and the MC1741 operational amplifier, contain the circuits used to implement functions 5 and 6.

The phase splitter is a flip-flop which operates in the toggle mode with $\overline{Q}$ connected to D. The pulse control flip-flop operates as a one shot and resets itself when the FET current charges the 0.001 μF timing capacitor to half

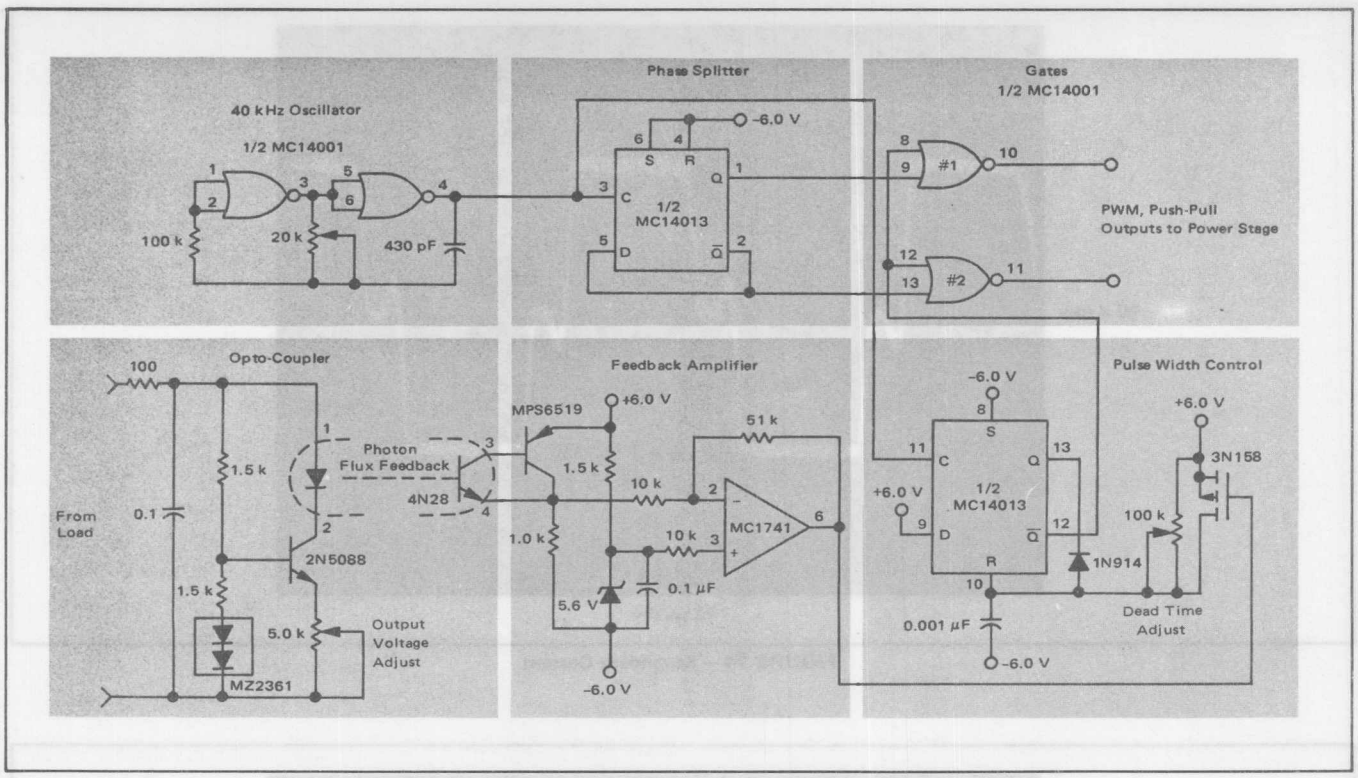

FIGURE 16 – Logic Schematic for Line Operated 5-V, 40-A Supply

the supply. The gates are enabled (high out) and turn on one of the power transistors only when both inputs are low. Since the splitter alternately causes one gate input to be low and then the other, both transistors can never be on at the same time. To further guard against simultaneous conduction and high "shoot through" currents, a resistor across the FET forces reset action in the one shot to occur in 20 μs, 5 μs before the opposite side is enabled. Because the one shot is also connected to both gates, it introduces inhibiting action even before the splitter changes state. The interaction of the stages may be easier to see in the timing diagram (Figure 17). Positive clock pulses toggle the splitter and enable the one shot (or pulse width control circuit). When the control is low and the Q output of the splitter is low, gate #1 is enabled and turns one of the inverter transistors on. On the next clock pulse, the control will go low again and the Q output of the splitter will be high ($\overline{Q}$ low). At this time, gate #2 is enabled and the remaining inverter transistor turns on.

The pulse width of the control circuit determines the output voltage and it in turn is controlled by the feedback elements in this closed loop system. The optoelectronic coupler makes use of the LED to sense output voltage changes and feed back a signal to the photo transistor and operational amplifier. The operational amplifier gain determines how good the line and load regulation will be and how much ripple reduction to expect. Too much gain will cause instability and high output ripple content. The excessive ripple is created when the pulse width control vacillates from wide to narrow pulses without ever settling on the appropriate width for the given line and load conditions. To improve stability, a low frequency filter is often added at this point (such as the RC filter shown at the LED input). The operational amplifier output voltage is fed to the gate of a P-channel MOSFET. The FET performs a voltage-to-current conversion in this design and controls the charge rate of the timing capacitor which determines the output pulse width.

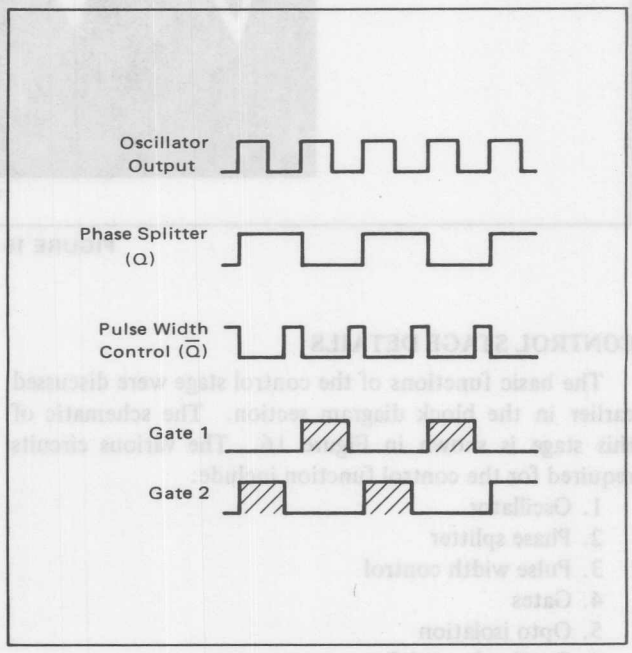

Figure 17 – Timing Diagram

Performance Data

The main features of this supply are that it is efficient and small. Some size was sacrificed in this design, in three areas specifically, to improve efficiency:

1. The barrier diode heat sink. Forced air cooling would reduce this size.
2. The inverter transformer. A large core which operates at low flux densities was used to reduce core losses.
3. The 60 Hz low voltage power transformer. A free running inverter could have been used.

Efficiency was measured with 40 A load current at 5 V. The input voltage and current waveforms are shown in Figure 18 and contain the information required to calculate input power. Assuming the input voltage is constant during current conduction:

$$P_{in} = \frac{V_{IN(peak)}}{T} \int_0^T Idt \qquad (11)$$

where P_{in} = average input power
$V_{IN(peak)}$ = peak input voltage
$\int Idt$ = area of the current pulse
T = half cycle period

with $V_{IN(peak)}$ = 165 V, T = 8.3 ms and counting 15 sq cm at 4 A and 0.2 ms per cm gives

$$P_{in} = \frac{165}{8.3\ m} (15 \times 4 \times 0.2\ m) = 240\ W$$

The efficiency therefore is

$$\eta = \frac{P_o}{P_{in}} = \frac{5\ V \times 40\ A}{240} \approx 83\% \qquad (12)$$

The total power loss in this design is about 40 W. Of this about 20 W is lost to the output rectifiers and 5 W to each IC regulator and both base resistors (another 15 W total): There was no noticeable heat rise in either the transformer or the power transistors.

This design also features line and load isolation which is made possible by the inverter transformer and optoelectronic coupler for feedback. Output voltage readings under the specified line and load variations are shown in Table III.

TABLE III – Output Voltage Readings

$V_{IN(RMS)}$	I_o	V_o
110	40	5.009
120	40	5.046
130	40	5.062
110	20	5.057
120	20	5.080
130	20	5.092

Using this data, and defining regulation as

$$\%\ Reg = \frac{\Delta V_o}{V_o} \times 100 \qquad (13)$$

gives

1. Line regulation at 40 A = 1.1% (53 mV)
2. Load Regulation at 120 V = 0.7% (34 mV)
3. Combined regulation = 1.7% (83 mV)

These figures represent the typical performance that can be obtained from this type of supply of 1% regulation before stability becomes a problem.

The ripple content of the output voltage at rated load is shown in Figure 19. In Figure 19A the 120 Hz ripple is 20 mV peak-to-peak or less than 10 mV_{RMS}. Input ripple was 20 V and with gain optimized, a 60 dB reduction was obtained. To further reduce 120 Hz ripple, the input filter capacitor would have to be increased. In Figure 19A, the 40 kHz ripple is also 20 mV peak-to-peak. In the previous filter design section, it was pointed out that this is strictly a function of the output filter elements. However, with practical high frequency limits of present components, the best designs can only reduce this num-

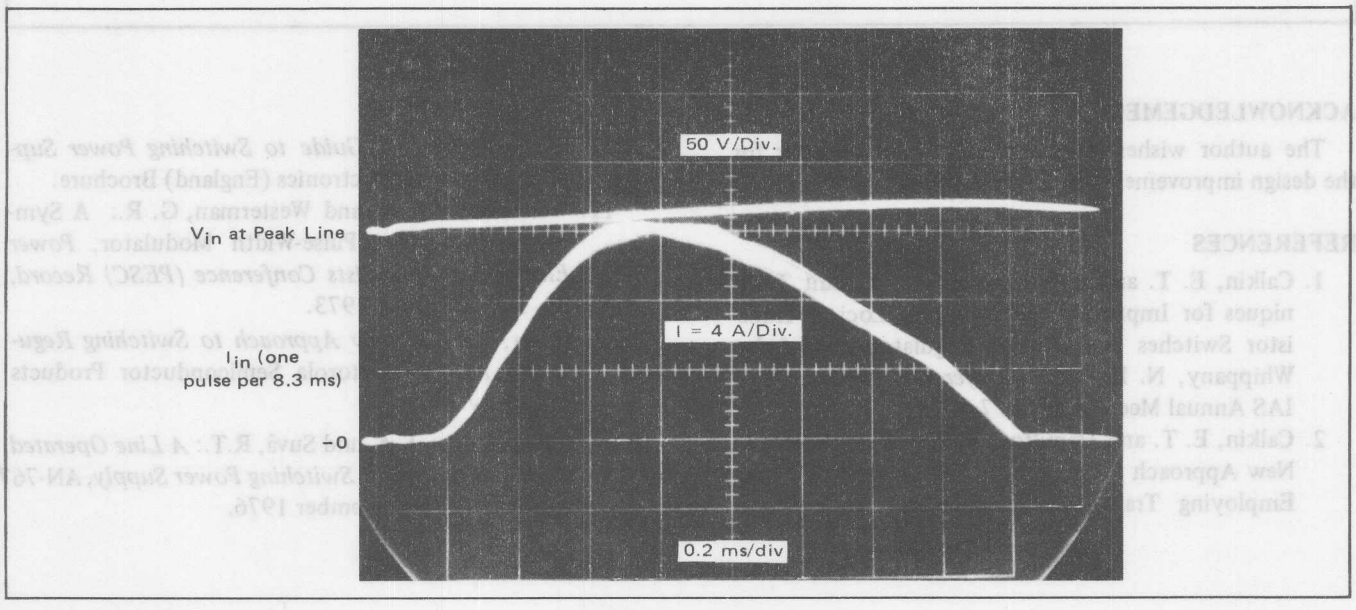

FIGURE 18 – Efficiency

ber to about 5 mV. Noise spikes, which are difficult to see in the pictures, were approximately 200 mV peak-to-peak. The spikes couple through the interwinding capacity of the filter inductor and are attenuated slightly by the 0.1 μF ceramic bypass capacitor. Further reduction would require an additional high frequency LC filter.

The overall performance of this regulator is quite good. The 10 mV ripple is more than adequate to drive standard TTL logic loads of small computers. In addition, several of these circuits could be operated from a dc bus between 140 and 200 V to supply the power requirements of a larger computer or industrial system. The 80% efficiency is exceptional. The completed supply required about 400 cubic inches and weighed about 10 pounds (see Figure 20). A further reduction in size and weight is possible with smaller heat sinks, forced air cooling and some sacrifice in efficiency by using a smaller inverter transformer and filter choke.

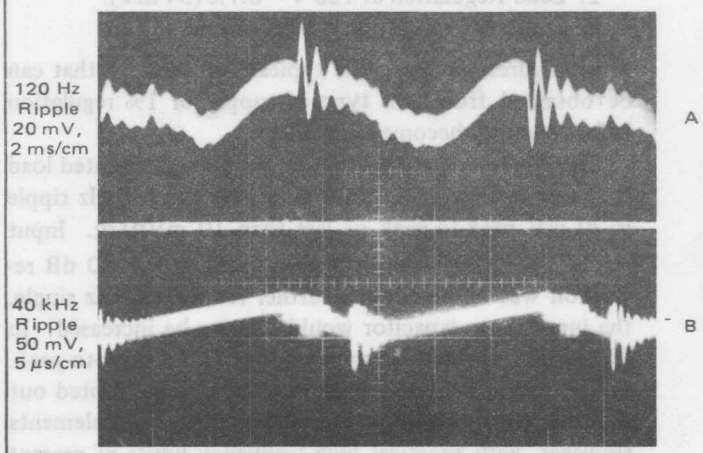

FIGURE 19 – Output Ripple

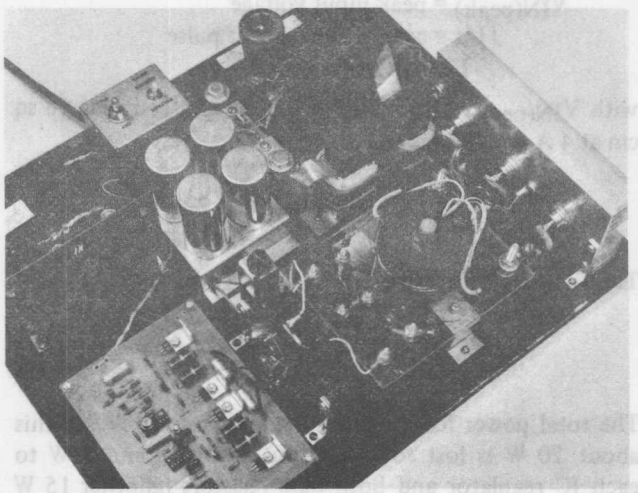

FIGURE 20 – Complete Supply

ACKNOWLEDGEMENT

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REFERENCES

1. Calkin, E. T. and Hamilton, B. H.: Circuit Techniques for Improving the Switching Loci of Transistor Switches in Switching Regulators, Bell Labs, Whippany, N. H., *IEEE Conference Record,* 1972 IAS Annual Meeting, pp. 477-484.
2. Calkin, E. T. and Hamilton, B. H.: A Conceptually New Approach for Regulated DC to DC Converters Employing Transistor Switches and Pulse Width Control, Bell Labs, Whippany, N. H., *IEEE Conference Record,* 1972 IAS Annual Meeting, pp. 485-494.
3. RS 011a: Designing Switching Regulators, *Cornell-Dubilier Bulletin 201.68,* Copyright 1973.
4. Okada, R. H.: *Switching Power Supplies,* RO Associates Brochure, Copyright 1973.
5. Turnbull, J: Ferrite Cores, *Electronic Products,* pp. 53-55, May 15, 1972.
6. Lisbin, D. M.: Slash Converter Design Time, *Electronic Design,* pp. 130-134, January 4, 1974.
7. Ferroxcube: *Magnetic Design Manual,* Bulletin 550, Copyright 1971.
8. Magnetics: *How to Select the Proper Core,* Bulletin 10A-5.
9. Dudley, B. W. and Peck, R. D.: High Efficiency Switching Regulators, *Hewlett-Packard Journal,* Vol. 25, No. 4, December 1973.
10. Burchall, M.: *A Guide to Switching Power Supplies,* Advanced Electronics (England) Brochure.
11. Weischedel, H. R. and Westerman, G. R.: A Symmetry Correcting Pulse-Width Modulator, *Power Electronics Specialists Conference (PESC) Record,* pp. 249-253, June 1973.
12. Haver, R.J.: *A New Approach to Switching Regulators,* AN-719 Motorola Semiconductor Products Inc., May 1974.
13. Gutmann, Dr. J. A. and Suvã, R.T.: *A Line Operated, Regulated 5 V/50 A Switching Power Supply,* AN-767, Motorola SPG, September 1976.

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