AN-770

Application Note

DATA ACQUISITION NETWORKS WITH NMOS AND CMOS

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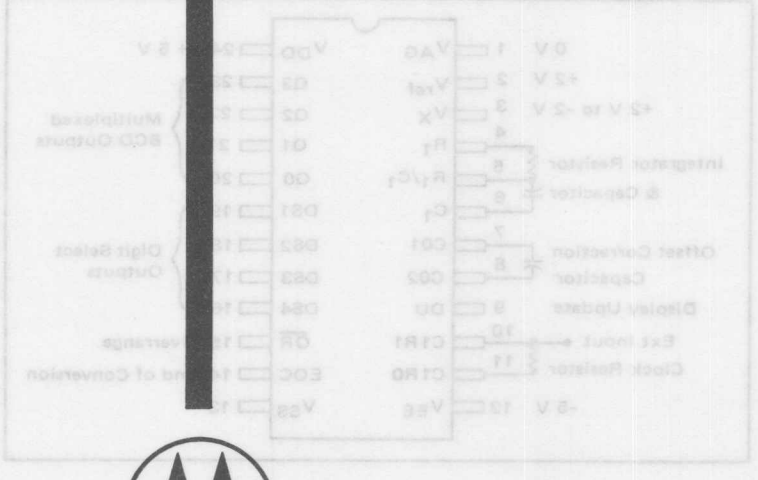
This article describes an eight-channel data acquisition network (DAN) using the Motorola MC14433 CMOS A/D converter and the M6800 microprocessor family. The A/D conversion technique used with the MC14433 is a modified dual ramp featuring auto-zero, auto-polarity, and high input impedance. Both hardware and M6800 software are shown for the DAN.



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DATA ACQUISITION NETWORKS WITH NMOS AND CMOS

LSI technology is making it easier and less expensive to design and build complex electronic systems. This fact holds true for Data Acquisition Networks (DANs) due to the new single chip A/Ds and microprocessor systems. Thus, it is now feasible to build your own data acquisition network instead of buying a completed system, and thereby save money.

This article discusses an eight-channel DAN using the Motorola MC14433 CMOS A/D converter and the M6800 microprocessor. The number of channels can be expanded or reduced very simply. In addition to the eight channel DAN the program for a single channel system is shown. The inputs to the system, positive or negative polarity, are multiplexed with a CMOS analog multiplexer.

MC14433 A/D CONVERTER

The MC14433 is a single chip 3½ digit A/D converter using a modified dual ramp technique of A/D conversion. Housed in a 24 pin package it features auto-polarity, auto-zero and a high input impedance. Figure 1 shows the pin diagram of the MC14433.

The output of the MC14433 is 3½ digit multiplexed BCD with the MSD containing not only the half digit but also polarity of the input, overrange and underrange information. Figure 2 describes the decoding for the MSD. The digit selects for the multiplexed BCD have interdigit blanking to ensure correct BCD data during the time that the digit select is true.

The A/D converter is ratiometric and requires an external reference voltage. This reference voltage is 2.000 volts for the 1.999 volt range and 200 mV for a 199.9 mV full scale input. Both the unknown and reference inputs and analog ground are high impedance inputs. Other external components required are clock resistor, integrator resistor and capacitor, and offset capacitor. Precision components are not required.

Of particular interest for the data acquisition systems are the display update (DU) and the end of conversion (EOC) pins. The EOC pin indicates the end of one conversion cycle and the start of the next conversion by a positive pulse one-half clock period long. The display update pin is an input to the chip which allows the data to be strobed into the output latches. If at least one positive edge is received prior to the ramp down cycle, new data is strobed to the display. In a stand alone A/D system, EOC is connected to DU.

Also of significance to the data acquisition network is the input polarity detection sequence for the MC14433. Polarity for the current conversion cycle is determined in the previous conversion cycle. Thus if the polarity is reversed, a second conversion cycle must be made in order to obtain a correct measurement.

The MC14433 requires two power supplies. The total voltage across the device must not exceed 18 volts. Pin 13 is the reference level for the output circuitry of the MC14433. If this pin is tied to 0 volts, the BCD output, digit select and EOC will swing from 0 volts to V_{DD}. If however, pin 13 is tied to V_{EE}, the output swing will be from V_{EE} to V_{DD}.

The clock for the MC14433 is internal to the chip, requiring only a single external resistor to set the frequency. An external clock may be used by driving pin 10.

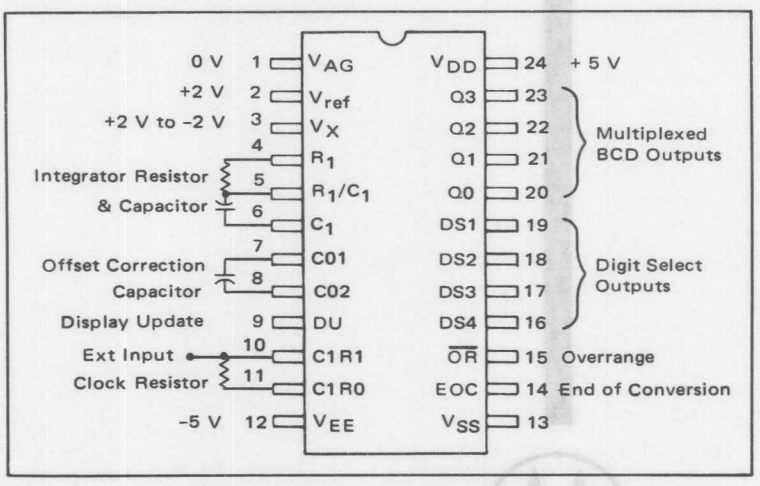

FIGURE 1 – MC14433 Pin Assignment

TRUTH TABLE

Coded Condition of MSD	Q3	Q2	Q1	Q0	BCD to 7 Segment Decoding	
+0	1	1	1	0	Blank	
−0	1	0	1	0	Blank	
+0 UR	1	1	1	1	Blank	
−0 UR	1	0	1	1	Blank	
+1	0	1	0	0	4 → 1	Hook up
−1	0	0	0	0	0 → 1	only seg b
+1 OR	0	1	1	1	7 → 1	and c to
−1 OR	0	0	1	1	3 → 1	MSD

Notes for Truth Table
Q3 – ½ digit, low for "1", high for "0"
Q2 – Polarity: "1" = positive, "0" = negative
Q0 – Out of range condition exists if Q0 = 1. When used in conjunction with Q3 the type of out of range condition is indicated, i.e., Q3 = 0 → OR or Q3 = 1 → UR.

When only segment b and c of the decoder are connected to the ½ digit of the display, 4, 0, 7 and 3 appear as 1.

FIGURE 2 – MSD Coding

The total conversion time for the MC14433 is approximately 16400 clock periods. This conversion time includes the auto-zero cycle and the unknown input measurement cycle. The clock frequency may be operated up to about 400 kHz producing a conversion time of 40 ms.

MPU

The Motorola microprocessor system devices used are the MC6800 MPU, MCM6810 RAM, MCM6830 ROM and MC6820 PIA (peripheral interface adapter). The following is a brief description of the basic MPU system as it pertains to the A/D systems presented later in this application note.

The Motorola MPU system uses a 16-bit address bus and an 8-bit data bus. The 16-bit address bus provides 65,536 possible memory locations which may be either storage devices (RAM, ROM, etc.) or interface devices (PIA, etc.). The basic MPU contains two 8-bit accumulators, one 16-bit index register, a 16-bit program counter, a 16-bit stack pointer, and an 8-bit condition code register. The condition code register indicates carry, half carry, interrupt, zero, minus, and 2's complement overflow. Figure 3 shows a functional block of the MC6800 MPU.

The MPU uses 72 instructions with six addressing modes which provide 197 different operations in the MPU. A summary of each instruction and function with the appropriate addressing mode is shown in the MC6800 data sheet.

The RAMs used in the system are static and contain 128 8-bit words for scratch pad memory while the ROM is mask programmable and contains 1024 8-bit words. The ROM and RAM, along with the remainder of the MPU system components, operate from a single +5 volt power supply; the address bus, data bus and PIAs are TTL compatible.

The MPU system requires a 2ϕ non-overlapping clock such as the MC6875* with a lower frequency limit of 100 kHz and an upper limit of 1 MHz.

*MC6875 to be introduced second quarter 1977

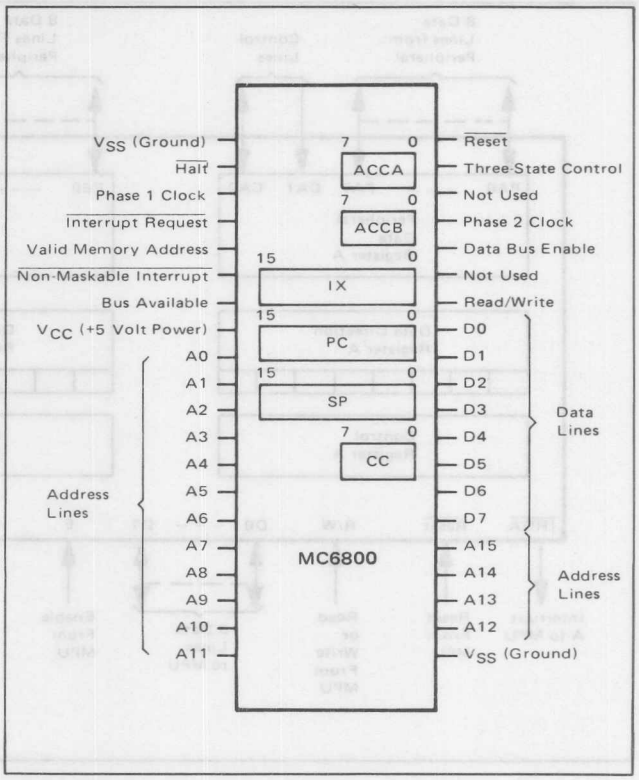

FIGURE 3 – MPU Pin Functions

The PIA is the interface device used between the address and data buses and the analog sections of the A/D. Each PIA contains two essentially identical 8-bit interface ports. These ports (A side, B side) each contain three internal registers that include the data register which is the interface from the data bus to the A/D, the data direction register which programs each of the eight lines of the data register as either an input or an output, and the control register which, in addition to other functions, switches the data bus between the data register and the data direction register. Each port to the PIA contains two addition pins, CA1 and CA2, for interrupt capability and extra I/O lines. The functions of these lines are programmable with the remaining bits of the control register. Figure 4 shows a functional block of the MC6820 PIA.

Each PIA requires four address locations in memory. Two addresses access either of the two (A or B sides) data/data direction registers while the remaining two addresses access either of the two control registers. These addresses are decoded by the chip select and register select lines of the PIA which are connected to the MPU address bus. Selection between the data register and data direction register is made by programming a "1" or "0" in the third least significant bit of each control register. A logic "0" accesses the data direction register while a logic "1" accesses the data register.

By programming "0"s in the data direction register each corresponding line performs as an input, while "1"s in the data direction register make corresponding lines act as outputs. The eight lines may be intermixed between inputs and outputs by programming different combinations of

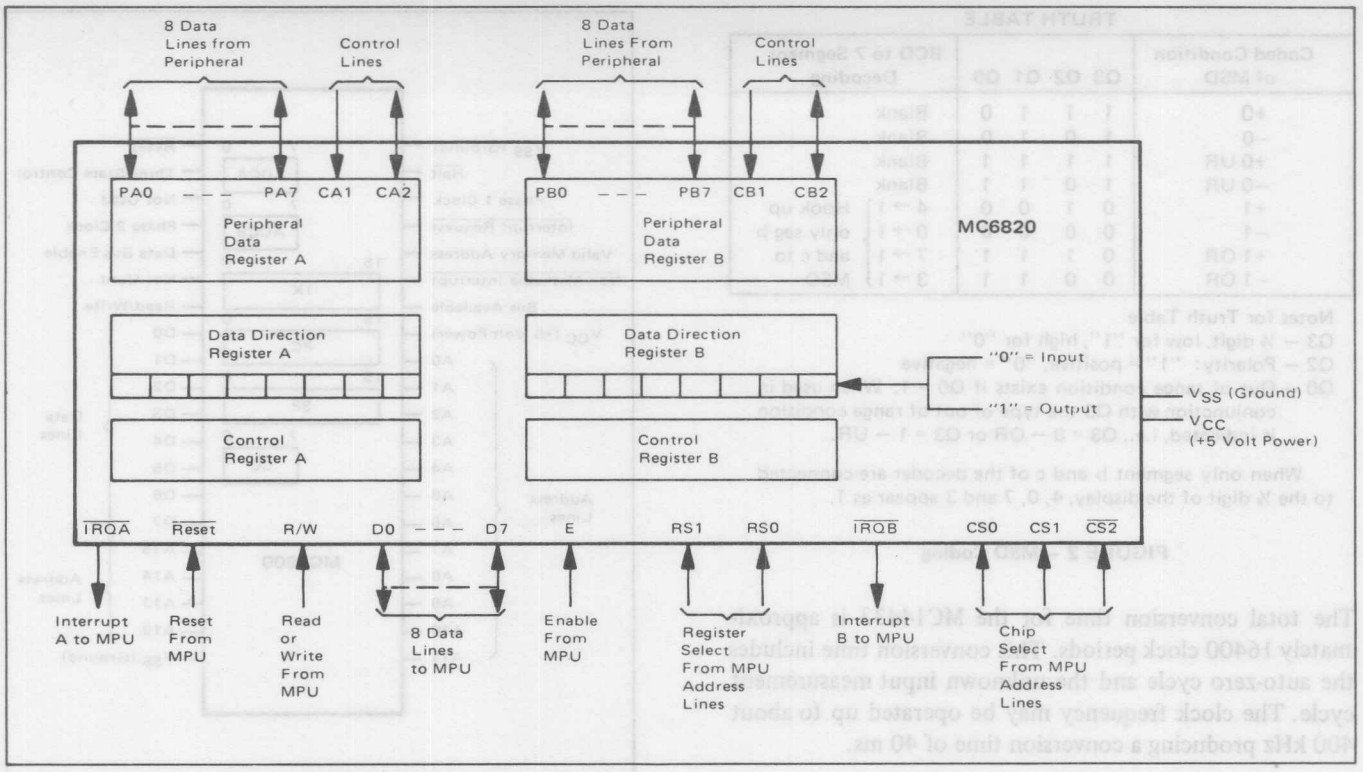

FIGURE 4 – PIA Functions

"1"s and "0"s into the data direction register. At the beginning of the program the I/O configuration is programmed into the data direction register, after which the control register is programmed to select the data register for I/O operation.

8-CHANNEL DATA ACQUISITION NETWORK

Figures 5 and 6 are the flow diagram for the 8-channel data acquisition network. Figure 5 shows the basic operation of the program while Figure 6 provides more detail on the A/D conversion routine. These flow diagrams relate to the actual software shown in Figure 8. The hardware required for the data acquisition is shown in Figure 9; as can be seen, it is fairly simple, consisting of the MC14433, MC1403* reference, MC14051B analog multiplexer, and an MC6820 PIA. The PIA is used as the interface between the microprocessor address and the data bus to the A/D. The microprocessor and associated memory are not shown due to a wide variety of forms possible depending upon the task that the total system is performing.

The reference for the MC14433 is an MC1403 bandgap reference which provides an output voltage of 2.5 volts. This voltage is divided down by the 20 kΩ pot to the 2.000 volt reference required by the MC14433. If a 200 mV reference is used, full scale for the DAN will be 199.9 mV.

The analog multiplexing required to handle the eight input channels is provided by a MC14051B CMOS multiplexer. This device selects one of eight inputs with a 3-bit binary code. The device is capable of switching dual polarity (plus or minus inputs) with a single polarity control voltage.

*MC1403 to be introduced first quarter 1977.

The MC14433 BCD output and digit select outputs are connected to the B side of the PIA as shown in lines 21-28 of the software routine. These lines of the software are comment lines only and do not result in code for the microprocessor. The B side data register of the PIA is labeled throughout the program as PIA1BD while the control register is labeled PIA1BC. The control I/O lines (CB1 and CB2) of the B side PIA are connected to EOC and DU of the MC1433.

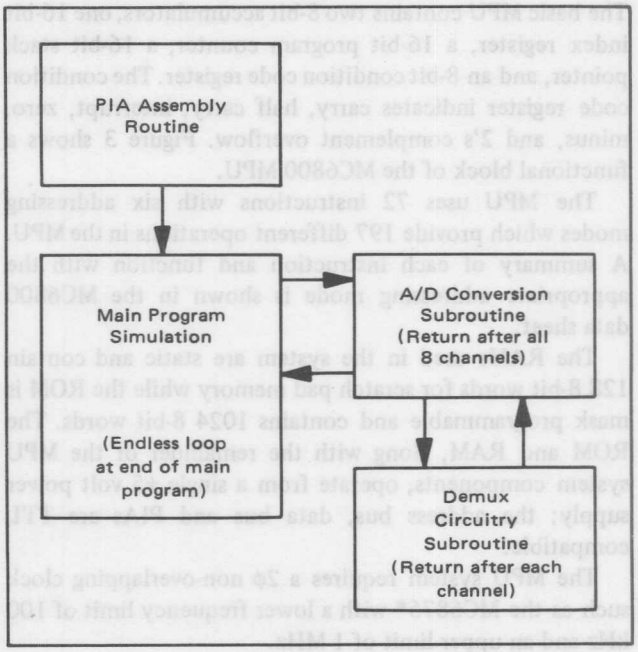

FIGURE 5 – Basic Operation of 8 Channel DAN

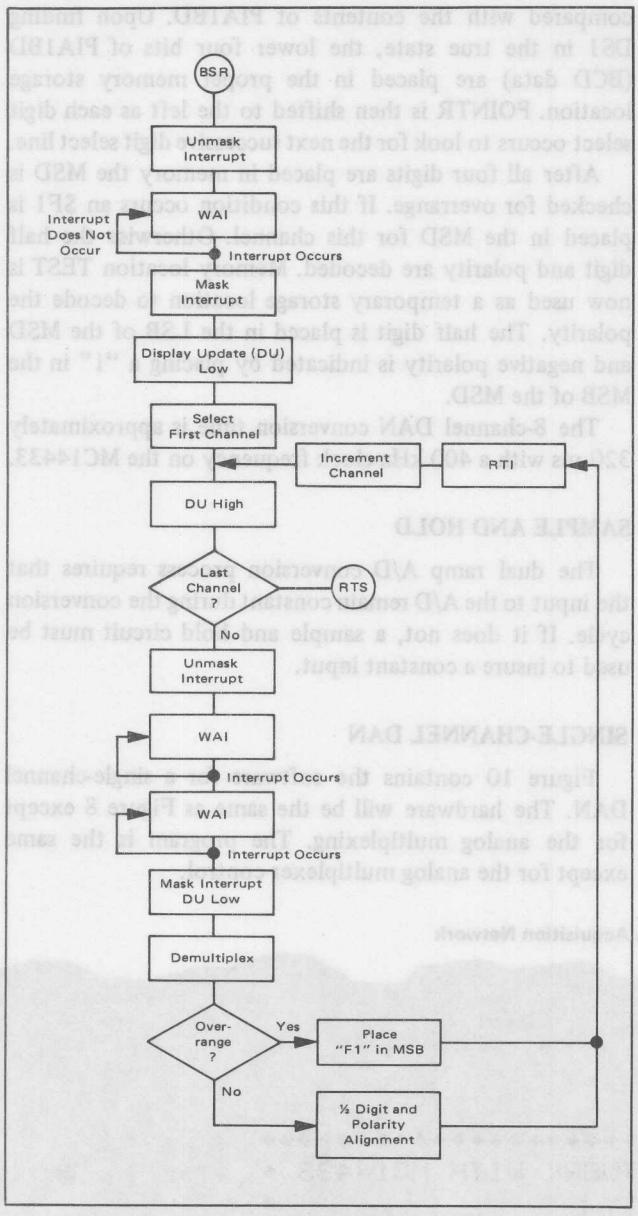

FIGURE 6 – A/D Conversion Subroutine Flow Chart

The first executable instruction for the program is in line 55 and starts a section called PIA assembly. The PIA sets the A side data register as all outputs and the B side data register as all inputs. From there the program goes to the main program simulation which, as its name implies, is a simulation of the user's main program. At such time in the user's program that some analog information is required, the A/D conversion subroutine starting in line 75 is executed. This routine synchronizes the program with the A/D conversion cycle and selects the first channel to be measured.

After the A/D conversion cycle for the first channel is completed the microprocessor is interrupted by the EOC of the MC14433. The interrupt program of line 88 is then executed; this demultiplexes the BCD output of the MC14433 and stores the data in memory. After completing the interrupt program the microprocessor returns to the A/D conversion subroutine and the next channel is selected. When the measurement of channel 2 is completed, the interrupt program is then executed and the resulting data stored away in memory. This procedure is repeated until all eight channels are read, after which the MPU returns to the main program. At this point the data obtained in the A/D conversion subroutine may be processed as required.

Looking at the software for the 8-channel data acquisition network in more detail, program storage of the final results begins in memory location $0010. Each BCD character is stored in the four LSBs of these memory locations. See Figure 7 for explanation of data storage. Each of the eight channel readings requires four memory

Channel Number	Memory Address	Digit	Data Example	Input Voltage
1	0010	MSD	01	1.729 V
	0011		07	
	0012		02	
	0013	LSD	09	
2	0014	MSD	F1	Overrange
	0015		09	
	0016		09	
	0017	LSD	09	
3	0018	MSD	08	-0.130 V
	0019		01	
	001A		03	
	001B	LSD	00	
4	001C	MSD	09	-1.130 V
	001D		01	
	001E		03	
	001F	LSD	00	
5	0020	MSD	00	0.000 V
	0021		00	
	0022		00	
	0023	LSD	00	
6	0024	MSD	01	1.000 V
	0025		00	
	0026		00	
	0027	LSD	00	
7	0028	MSD	F1	Overrange
	0029		09	
	002A		09	
	002B	LSD	09	
8	002C	MSD	09	-1.000 V
	002D		00	
	002E		00	
	002F	LSD	00	

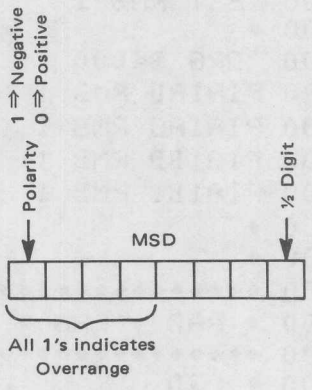

FIGURE 7 – Data Storage Definition

locations with the MSD occupying the first of each sequence of four memory locations. The index register is used to keep track of the next storage location for the BCD information. At the end of each channel's conversion cycle the index register points to the MSD of that channel. This address is also stored at memory location called STORL.

Memory location TEST has two purposes; the first is for keeping track of which WAI was executed when the MPU was in the interrupt routine. This is required since more than one A/D conversion cycle is required for each channel. For the first channel three EOC pulses are required, while the remaining channels require only two A/D conversion cycles. The extra A/D conversion cycle in the first channel is used to synchronize the A/D converter to the MPU system. The second A/D conversion cycle in the first channel and the first conversion cycle of the remaining channels ensure that the polarity is correct for the current input. This is required since the MC14433 determines polarity in the previous conversion cycle.

Since the display update pin is edge triggered it must be taken high and low again in each conversion cycle when the data is to read by the MPU. The DU pin is taken high prior to the WAI for the measurement and low in the interrupt routine after the EOC occurs.

As mentioned previously, the multiplexed BCD data from the MC14433 is demultiplexed in the interrupt routine. A "1" is placed in bit 4 of POINTR which is compared with the contents of PIA1BD. Upon finding DS1 in the true state, the lower four bits of PIA1BD (BCD data) are placed in the proper memory storage location. POINTR is then shifted to the left as each digit select occurs to look for the next successive digit select line.

After all four digits are placed in memory the MSD is checked for overrange. If this condition occurs an $F1 is placed in the MSD for this channel. Otherwise the half digit and polarity are decoded. Memory location TEST is now used as a temporary storage location to decode the polarity. The half digit is placed in the LSB of the MSD and negative polarity is indicated by placing a "1" in the MSB of the MSD.

The 8-channel DAN conversion time is approximately 320 ms with a 400 kHz clock frequency on the MC14433.

SAMPLE AND HOLD

The dual ramp A/D conversion process requires that the input to the A/D remain constant during the conversion cycle. If it does not, a sample and hold circuit must be used to insure a constant input.

SINGLE-CHANNEL DAN

Figure 10 contains the software for a single-channel DAN. The hardware will be the same as Figure 8 except for the analog multiplexing. The program is the same except for the analog multiplexer control.

FIGURE 8 – 8-Channel Data Acquisition Network

```
 1.000  NAM DWA36
 2.000  OPT MEM,OTAPE
 3.000 *
 4.000 *
 5.000 *********************************************************
 6.000 * 8 CHANNEL DATA AQUISTION NETWORK WITH MC14433 *
 7.000 *                WITH AUTOPOLARITY                      *
 8.000 *********************************************************
 9.000 *
10.000  ORG $0000
11.000 STORL RMB 2          POINTER FOR DATA STORAGE LOCATION
12.000 POINTR RMB 1                POINTER FOR DIGIT SELECT
13.000 TEST RMB 1
14.000 *
15.000  ORG $4000
16.000 PIA1AD RMB 1              A SIDE,DATA REGISTER
17.000 PIA1AC RMB 1              A SIDE,CONTROL REGISTER
18.000 PIA1BD RMB 1              B SIDE,DATA REGISTER
19.000 PIA1BC RMB 1              B SIDE,CONTROL REGISTER
20.000 *
21.000 *                      **PIA CONFIGURATION**
22.000 *********************************************************
23.000 * PA7 * PA6 * PA5 * PA4 * PA3 * PA2 * PA1 * PA0 *
24.000 *********************************************************
25.000 * LSD                MSD * MSB                  LSB *
26.000 *********************************************************
27.000 *    DIGIT SELECT       *          BCD            *
28.000 *********************************************************
```

```
29.000 *
30.000 *          RESULTS STORED IN LOCATIONS $0010-$002F.
31.000 *             EACH CHANNEL OCCUPIES FOUR CONSECUTIVE
32.000 *             MEMORY LOCATIONS WITH MSD FIRST.
33.000 *             NEGATIVE POLARITY INDICATED VIA A
34.000 *             "1" IN MSB OF THE MSD.
35.000 *             OVERRANGE INDICATION VIA AN "F1" IN
36.000 *             MSD OF EACH CHANNEL.
37.000 *
38.000 *
39.000 *
40.000 *          CHANNEL SELECTION VIA PIA1AD.
41.000 *             CHANNEL NUMBER IS CODED IN A BINARY
42.000 *             FORM FOR CHANNELS 0-7.
43.000 *
44.000 *
45.000 *
46.000 *
47.000 *
48.000 *
49.000 *
50.000 *
51.000 *
52.000 *
53.000 *
54.000 *
55.000  ORG $0800                  PIA ASSEMBLY
56.000  CLR TEST
57.000  CLR PIA1BC                 PIA ASSEMBLY
58.000  CLR PIA1BD           B SIDE INPUTS
59.000  CLR PIA1AC
60.000  LDA A #$FF
61.000  STA A PIA1AD         A SIDE OUTPUTS
62.000  LDA A #$34
63.000  STA A PIA1BC
64.000  STA A PIA1AC
65.000  LDS #$08F0
66.000  CLI
67.000 *
68.000 *
69.000  NOP                          MAIN PROGRAM SIMULATION
70.000  JSR CONVRT
71.000 END NOP
72.000  BRA END
73.000 *
74.000 *
75.000 CONVRT LDX #$000C             CONVERSION SUBROUTINE
76.000  STX 0000
77.000  LDA B #$04
78.000  STA B TEST
79.000  LDA A PIA1BD
80.000  LDA A #$37
81.000  STA A PIA1BC
82.000  WAI
```

FIGURE 8 – 8-Channel Data Acquisition Network

```
 83.000  LDA B #$07
 84.000 N STA B PIA1AD
 85.000  LDA A #$02
 86.000  STA A TEST
 87.000  LDA A #$37
 88.000  STA A PIA1BC
 89.000  WAI
 90.000  NOP
 91.000  WAI
 92.000  DEC B
 93.000  BPL N
 94.000  RTS
 95.000 *
 96.000 *
 97.000 *
 98.000  ORG $0850                    INTERRUPT ROUTINE
 99.000  LDA A #$3F
100.000  STA A PIA1BC
101.000  LSR TEST
102.000  BCC FIRST
103.000  LDA A #$34
104.000  STA A PIA1BC
105.000 BEGIN LDA A #$10
106.000  STA A POINTR
107.000  LDX $0000
108.000 NEXT LDA A PIA1BD
109.000  ROR TEST
110.000  ADD B TEST
111.000  TAB
112.000  AND A POINTR
113.000  BEQ NEXT
114.000  ASL POINTR
115.000  AND B #$0F
116.000  STA B 4,X
117.000  INX
118.000  BCC NEXT
119.000  LDA A 0,X                 OVERRANGE TEST
120.000  TAB
121.000  AND A #$0B
122.000  CMP A #$03
123.000  BEQ OVRNGE
124.000  CLR TEST                HALF DIGIT AND POLARITY
125.000  AND B #$0C                   ALIGNMENT
126.000  LSR B
127.000  LSR B
128.000  LSR B
129.000  ROR TEST
130.000  ADD B TEST
131.000  COM B
132.000  AND B #$81
133.000  STA B 0,X
134.000  BRA FINE
135.000 OVRNGE LDA A #$F1              OVERRANGE ROUTINE
136.000  STA A 0,X
```

FIGURE 8 – 8-Channel Data Acquisition Network

```
137.000 FINE STX STORL
138.000  RTI
139.000 FIRST LDA A PIA1BD   DUMMY LOAD TO CLR INTERRUPT
140.000  RTI
141.000  ORG $0350              HARDWARE INTERRUPT VECTOR
142.000  FDB $03F0
143.000  MON
```

FIGURE 8 – 8-Channel Data Acquisition Network

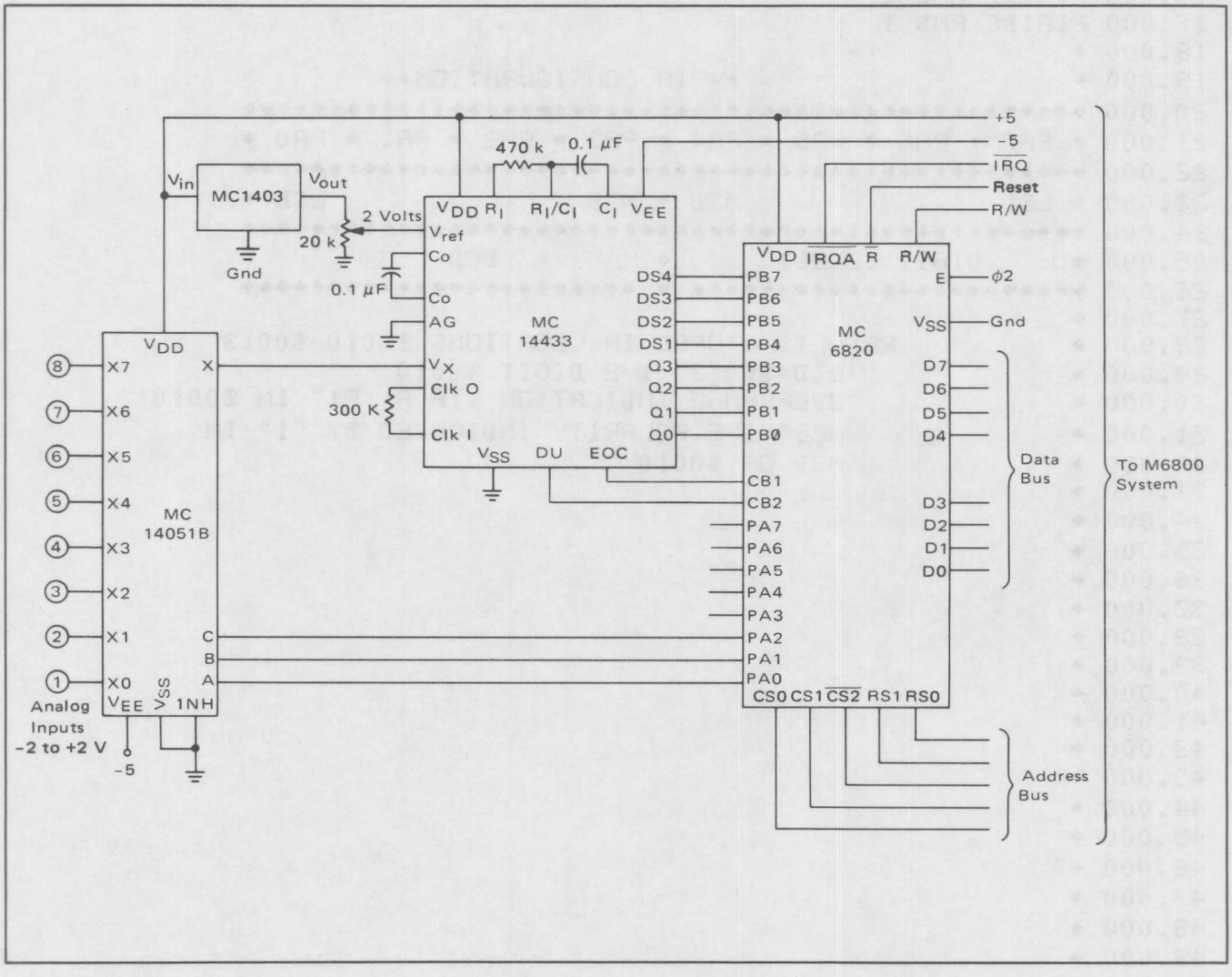

FIGURE 9 – 8-Channel Data Acquisition Hardware

```
 1.000  NAM DWA35
 2.000  OPT MEM,OTAPE
 3.000 *
 4.000 *                    *********
 5.000 *                    *MC14433*
 6.000 *******************************************************
 7.000 * SINGLE CHANNEL DATA ACQUISITION NETWORK WITH *
 8.000 *                  AUTOPOLARITY                  *
 9.000 *******************************************************
10.000 *
11.000  ORG $0002
12.000 POINTR RMB 1                  POINTER FOR DIGIT SELECT
13.000 TEST RMB 1
14.000 *
15.000  ORG $4002
16.000 PIA1BD RMB 1
17.000 PIA1BC RMB 1
18.000 *
19.000 *                     **PIA CONFIGURATION**
20.000 *******************************************************
21.000 * PA7 * PA6 * PA5 * PA4 * PA3 * PA2 * PA1 * PA0 *
22.000 *******************************************************
23.000 * LSD                MSD * MSB                LSB *
24.000 *******************************************************
25.000 *     DIGIT SELECT       *          BCD           *
26.000 *******************************************************
27.000 *
28.000 *          RESULTS STORED IN LOCATIONS $0010-$0013
29.000 *             LSD=$0013  1/2 DIGIT $0010
30.000 *             OVERRANGE INDICATION VIA A "F1" IN $0010
31.000 *             NEGATIVE POLARITY INDICATED BY "1" IN
32.000 *             MSB OF $0010
33.000 *
34.000 *
35.000 *
36.000 *
37.000 *
38.000 *
39.000 *
40.000 *
41.000 *
42.000 *
43.000 *
44.000 *
45.000 *
46.000 *
47.000 *
48.000 *
49.000 *
50.000 *
51.000 *
52.000 *
53.000 *
54.000 *
```

FIGURE 10 – Single-Channel Data Acquisition Network

```
55.000 *
56.000 *
57.000 *
58.000  ORG $0800
59.000  CLR TEST
60.000  CLR PIA1BC                  PIA ASSEMBLY
61.000  CLR PIA1BD
62.000  LDA A #$34
63.000  STA A PIA1BC
64.000  LDS #$08F0
65.000  CLI
66.000 *
67.000 *
68.000  NOP                         MAIN PROGRAM SIMULATION
69.000  JSR CONVRT
70.000 END NOP
71.000  BRA END
72.000 *
73.000 *
74.000 CONVRT LDX #$0010      CONVERSION SUBROUTINE
75.000  LDA B #$04
76.000  STA B TEST
77.000  LDA A PIA1BD DUMMY LOAD TO CLEAR INTERRUPT
78.000  LDA A #$3F
79.000  STA A PIA1BC
80.000  WAI
81.000  NOP
82.000  WAI
83.000  NOP
84.000  WAI
85.000  RTS
86.000 *
87.000 *
88.000  ORG $0850             BEGINING OF INTERRUPT PROGRAM
89.000  CLC
90.000  LSR TEST
91.000  BCC DELAY
92.000  LDA A #$34
93.000  STA A PIA1BC
94.000 BEGIN LDA A #$10
95.000  STA A POINTR
96.000 NEXT LDA A PIA1BD
97.000  TAB
98.000  AND A POINTR
99.000  BEQ NEXT
100.000  ASL POINTR
101.000  AND B #$0F
102.000  STA B 0,X
103.000  INX
104.000  BCC NEXT
105.000  LDA A $0010          OVERRANGE CHECK
106.000  TAB
107.000  AND A #$0B
108.000  CMP A #$03
```

FIGURE 10 — Single-Channel Data Acquisition Network

```
109.000  BEQ OVRNGE
110.000  CLR TEST          HALF DIGIT AND POLARITY
111.000  AND B #$0C         ALIGNMENT
112.000  LSR B
113.000  LSR B
114.000  LSR B
115.000  ROR TEST
116.000  ADD B TEST
117.000  COM B
118.000  AND B #$81
119.000  STA B $0010
120.000  BRA FINE
121.000 OVRNGE LDA A #$F1          OVERRANGE ROUTINE
122.000  STA A $0010
123.000 FINE STX STORL
124.000  RTI
125.000 DELAY LDA A PIA1BD
126.000  RTI
127.000  ORG $08F8
128.000  FDB $0850
129.000  MON
```

FIGURE 10 — Single-Channel Data Acquisition Network

REFERENCES

Aldridge, Don: *"Analog-To-Digital Conversion Techniques with the M6800 Microprocessor System"*, AN757, Motorola Semiconductor Products Inc.

M6800 Microprocessor Applications Manual, Motorola Semiconductor Products Inc.

M6800 Microprocessor Programming Reference Manual, Motorola Semiconductor Products Inc.

MC6800, MC6820 Data Sheets, *M6800 Microcomputer System Design Data,* Motorola Semiconductor Products Inc.

MC1403/1503 Data Sheet, Motorola Semiconductor Products Inc.

MC14051B Data Sheet, Motorola Semiconductor Products Inc.

MC14433 Data Sheet, Motorola Semiconductor Products Inc.

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