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Application Note

CMOS MONOSTABLE MULTIVIBRATORS

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Monostable multivibrators provide controllable time intervals, and consequently, find applications in virtually all segments of the electronics industry. This note describes the theory and operations of the MC14538B, a high-precision monostable multivibrator that incorporates both digital and linear CMOS technology in a single, monolithic circuit. Applications of the MC14538B are also described.

MOTOROLA Semiconductor Products Inc.

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INTRODUCTION

A monostable multivibrator is defined as a device with a stable quiescent state as well as a quasi-stable transition state. The output of the monostable can remain indefinitely in the stable state, until an input trigger causes a transition into the temporary or quasi-stable state. After an interval, T, the output will return to the quiescent state and remain there until the next trigger pulse. Thus, the monostable provides a pulse of controllable time T after an input trigger.

Motorola has two monostable multivibrators (one shots) in the CMOS technology: the MC14528B and the precision MC14538B. These are dual, retriggerable/resettable monostables and are pin-for-pin compatible. The MC14528B and MC14538B use standard CMOS digital techniques. In addition, the MC14538B also uses low power linear techniques in the form of CMOS voltage comparators. This linear/digital combination allows more precise control of the output pulse width over temperature, supply variation and from part to part. This application note will concentrate on the operation and characteristics of the MC14538B.

THEORY OF OPERATION

The block diagram of the MC14538B is shown in Figure 1, with circuit operation following.

As shown in Figures 1 and 2, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until $V_{ref\ 1}$ is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals $V_{ref\ 2}$, comparator C2 changes state, causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

It should be noted that in the quiescent state C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the MC14538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

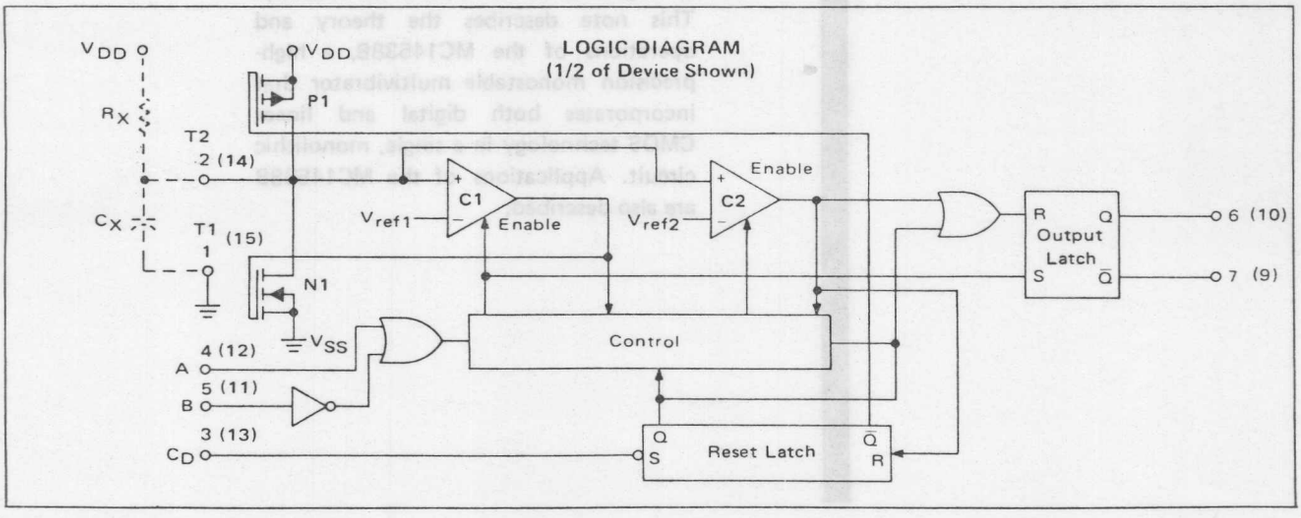

FIGURE 1 – Block Diagram of the MC14538B

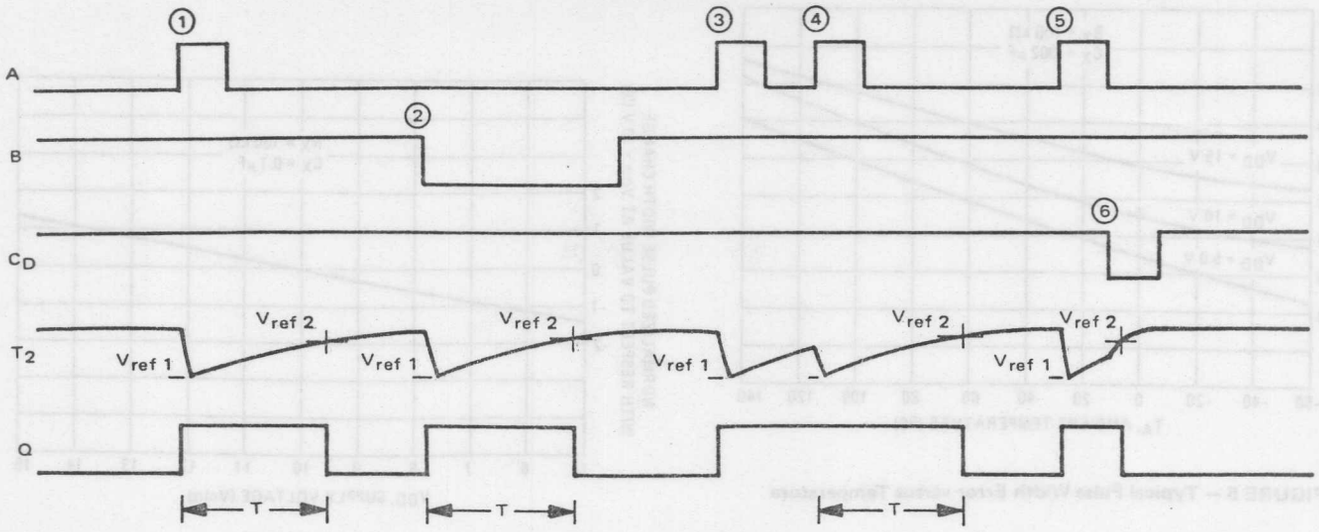

FIGURE 2 – Timing Diagram

RESET OPERATION

The MC14538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor P1. When the voltage on the capacitor reaches $V_{ref\ 2}$, the reset latch will clear, and will then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

RETRIGGER OPERATION

The MC14538B is retriggered if a valid trigger occurs followed by another valid trigger before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from $V_{ref\ 1}$, but has not yet reached $V_{ref\ 2}$, will cause an increase in output pulse width T. When a valid retrigger is initiated (see Figure 2), the voltage at T2 will again drop to $V_{ref\ 1}$ before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, (determined via R_X and C_X), has occurred, after the last valid retrigger.

ACCURACY

One primary feature of the MC14538B is the very good reproducibility of output pulse width. As shown in Figures 3, 4, and 5, when substituting one part for another, the

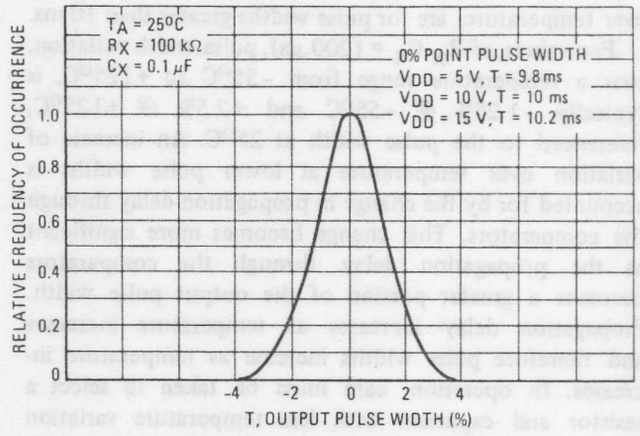

FIGURE 3 – Typical Normalized Distribution of Units for Output Pulse Width

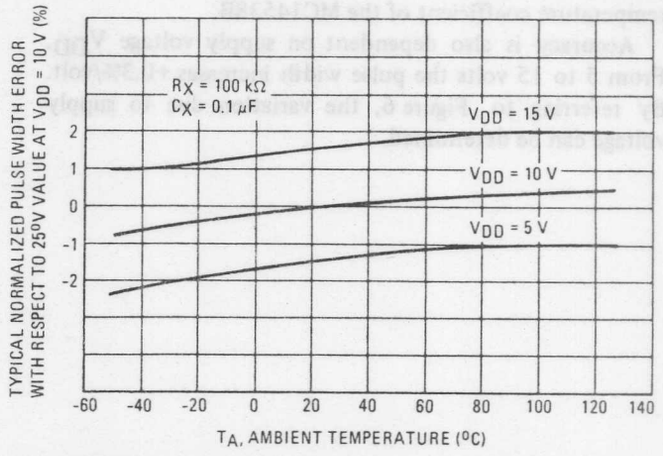

FIGURE 4 – Typical Pulse Width Error versus Temperature

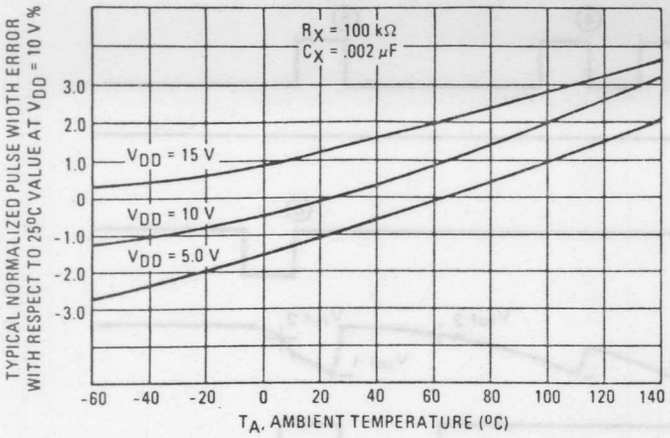

FIGURE 5 – Typical Pulse Width Error versus Temperature

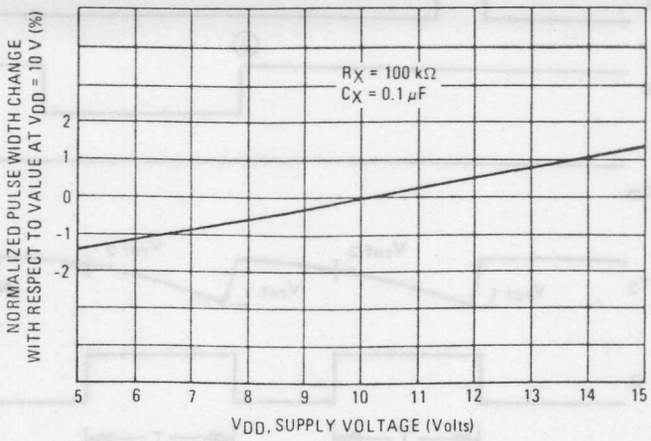

FIGURE 6 – Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

standard deviation of the distribution of pulse widths is ±1%, with guaranteed maximum variation set at ±5%.

Due to the ratiometric design of the comparator thresholds, the pulse width variation, over a temperature range from -55°C to +125°C, is held to, typically, -0.7% @ -55°C and 0.4% @ 125°C, referenced to the pulse width at 25°C. These values of pulse width variation, over temperature, are for pulse widths greater than 10 ms.

For values of R_X C_X = (200 μs), pulse width variation, over a temperature range from -55°C to +125°C, is typically -1.25% @ -55°C and +2.5% @ +125°C, referenced to the pulse width at 25°C. An increase of variation over temperature at lower pulse widths is accounted for by the change in propagation delay through the comparators. This change becomes more significant as the propagation delay through the comparators becomes a greater portion of the output pulse width. Propagation delay increases as temperature increases and therefore pulse widths increase as temperature increases. In operation, care must be taken to select a resistor and capacitor with less temperature variation than is expected from the monostable circuit. For additional stability, selection of a capacitor with a negative temperature coefficient would tend to offset the positive temperature coefficient of the MC14538B.

Accuracy is also dependent on supply voltage V_{DD}. From 5 to 15 volts the pulse width increases +0.3%/volt. By referring to Figure 6, the variation due to supply voltage can be determined.

PULSE WIDTH FORMULA

For ease of design, a pulse width formula was "designed in" such that T = RC. As shown in Figure 7, this formula is accurate to typically 10% from 100 μs to well over 1 second. For time constants less than 100 μs, the propagation delay of the MC14538B will become significant, affecting the accuracy of the T = RC formula. Inherent capacitance seen at pin 2 (and 14) amounts to typically 25 pF, and adds to the error of the formula when using small capacitor values. When pulse widths less than 10 μs are required it is recommended that the MC14528B be used.

Leakage current effects on the output pulse width become apparent for large values of resistance and capacitance. Reverse junction leakage into the MC14538B limits external resistance as does leakage of the capacitor. Humidity and circuit board contamination can also cause leakage currents. As long as these effects are taken into consideration, resistor values well into the tens of megohms can be used for R_X. However, for a production design, 1 megohm is recommended as a maximum value. A value of 1 megohm will insure that leakage effects, both into the MC14538B and due to circuit board characteristics, will have little effect on output pulse width.

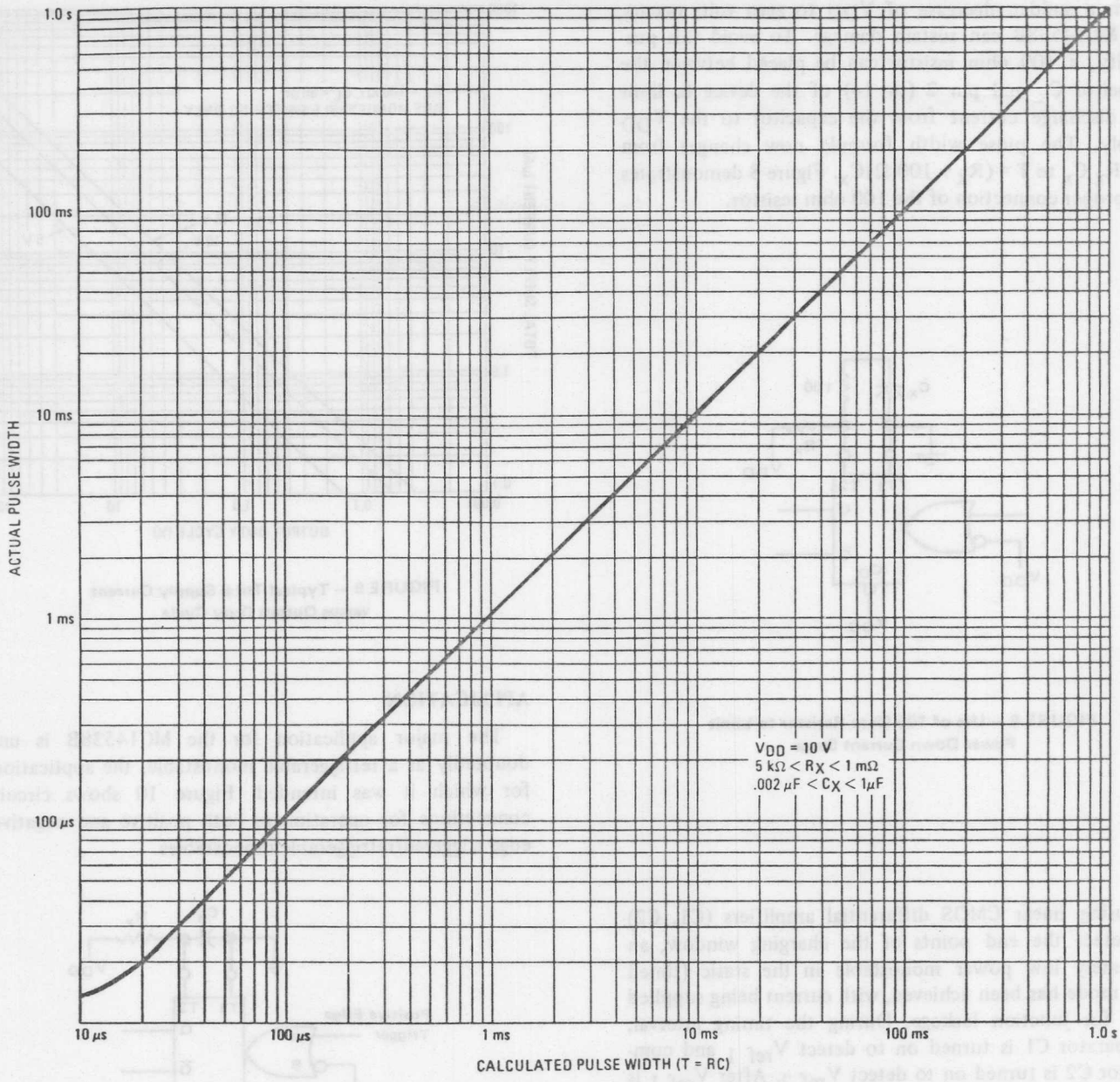

FIGURE 7 – Typical Pulse Width versus T = RC

The minimum resistor to be used for timing is limited due to the internal resistance (R_{int}, typically 300 ohms) used to limit capacitor discharge currents. Resistors under 5 k ohms have a noticeable effect on the capacitor discharge voltage curve due to a voltage divider action set up by the two resistances R_X and R_{int}. If R_X is too small, the capacitor will not be allowed to discharge to the lower threshold, and the MC14538B will cease to function correctly. Large capacitance values can cause problems due to the large amount of energy stored. When a system containing the MC14538B (or MC14528B) is powered down, the capacitor voltage may discharge from V_{DD} through the standard protection diodes at pin 2 or 14. Current through the protection diodes should be limited to 10 mA and therefore the discharge time of the V_{DD} supply must not be faster than $(V_{DD})\cdot(C)/(10\ mA)$. For example, if V_{DD} = 10 V and C_X = 10 μF, the V_{DD} supply should discharge no faster than (10 V) x (10 μF)/(10 mA) = 10 ms. This is normally not a problem since power supplies are heavily filtered and cannot discharge at this rate.

When a sudden decrease of V_{DD} to zero volts occurs, the MC14538B can sustain damage. To avoid this possibility, a 100 ohm resistor can be placed between the capacitor C_X and pin 2 (or 14) of the device to limit the discharge current from the capacitor to the V_{DD} supply. The pulse width formula now changes from $T = R_X C_X$ to $T = (R_X + 100\ \Omega)C_X$. Figure 8 demonstrates the proper connection of the 100 ohm resistor.

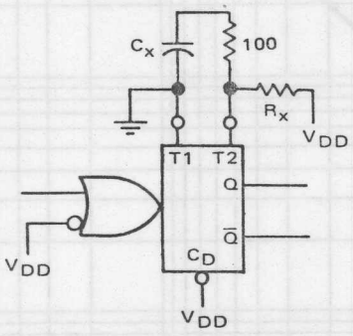

FIGURE 8 – Use of 100 Ohm Resistor to Limit Power Down Current Surge

By using linear CMOS differential amplifiers (C1, C2) to detect the end points of the charging window, an extremely low power monostable in the static (timed out) mode has been achieved, with current being supplied only for junction leakage. During the timing interval, comparator C1 is turned on to detect $V_{ref\ 1}$ and comparator C2 is turned on to detect $V_{ref\ 2}$. After $V_{ref\ 1}$ is detected, comparator C1 is turned off. After $V_{ref\ 2}$ is detected, comparator C2 is turned off and a low power state is once again restored. As the output pulse width T is increased to a greater duty cycle, the total supply current increases, due to comparator C2 being in the "on" state for a larger percentage of the time. The active state leakage referred to in the data sheet is the current being drawn by comparator C2. This is measured by connecting a voltage source to the timing node T2, triggering the input and lowering the voltage of T2 below $V_{ref\ 1}$, then measuring the current into pin 16. Figure 9 shows how total supply current increases with output duty cycle.

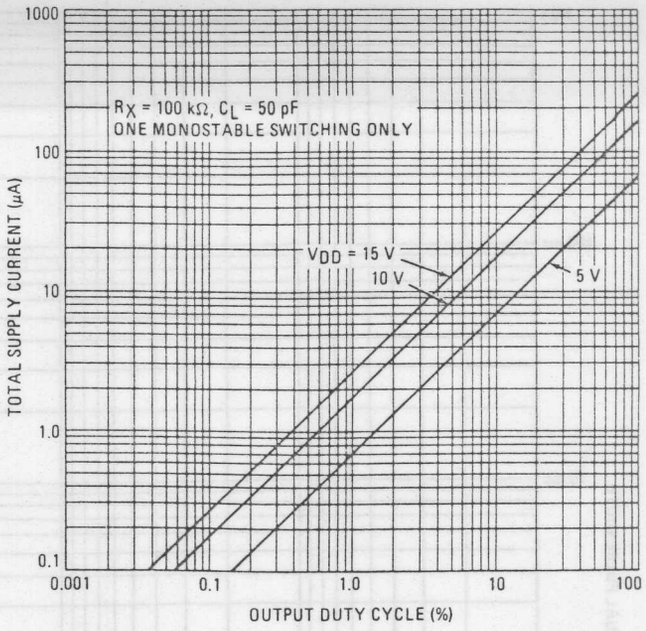

FIGURE 9 – Typical Total Supply Current versus Output Duty Cycle

APPLICATION

The major application for the MC14538B is undoubtedly as a retriggerable monostable, the application for which it was intended. Figure 10 shows circuit connections for operation as both positive and negative edge triggered/retriggerable monostables.

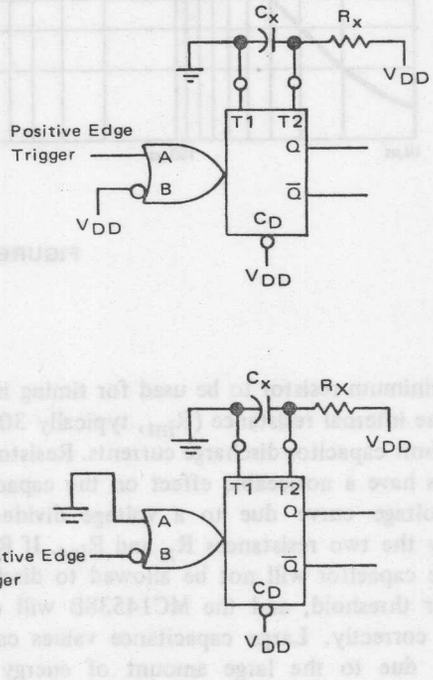

FIGURE 10 – Retriggerable Monostables Circuitry

When a non-retriggerable monostable is required, the MC14538B can easily be connected, as Figure 11, for either positive or negative edge triggering. No additional components are required to cause this retriggerable monostable to operate in the non-retriggerable mode. The connection from the output to the unused trigger input inhibits triggering until the output pulse has been completed.

Due to the fact that the capacitor is completely discharged when power to the MC14538B is off, and that in the quiescent state the capacitor is fully charged, the MC14538B (and MC14528B) will typically exhibit an output pulse when power is applied to the circuit of Figure 10. This pulse is equal to the time required for the capacitor, C_X, to charge through R_X to the upper trip point. For the MC14528B this can be significantly longer than the normal pulse width.

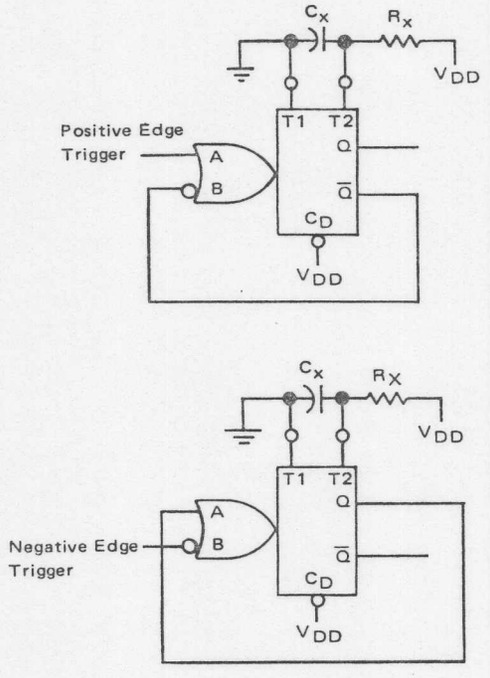

FIGURE 11 – Non-retriggerable Monostables Circuitry

This power-up output pulse can usually be eliminated by the change in the monostable circuit shown in Figure 12. In this circuit the timing capacitor C_X is connected from pin 2, or 14, to V_{DD} instead of being tied to V_{SS} as is normally done. In both cases, pins 1 and 15 should be externally grounded to V_{SS}.

With this connection, the capacitor is discharged in both the power-down condition and in quiescent operation. When the monostable is triggered, C_X "charges" to ground through pin 2 until the $V_{ref\ 1}$ threshold is reached, after which, C_X begins to discharge back to $V_{ref\ 2}$. Thus, internal circuitry operates identically and the voltage waveform at pin 2 (or 14) is the same.

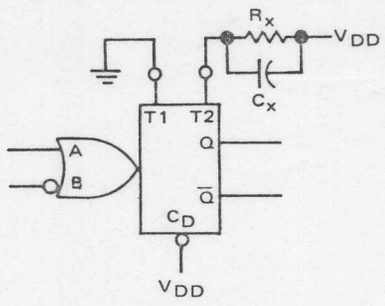

FIGURE 12 – Elimination of Power-Up Pulse Width

TACHOMETER APPLICATION

The circuit in Figure 13 shows a useful application for a precision monostable: that of a tachometer or analog frequency indicator. With the values shown, the MC14538B operates as a monostable with an output pulse width of 6 ms duration. This pulse drives a transistor which in turn supplies current to a meter movement. The meter averages the current pulses, giving an indication of frequency. The reciprocal of the 6 ms PW is 167 Hz. As the trigger input approaches that frequency, the monostable's output approaches a steady dc level. Full-scale meter calibration should be made at 167 Hz. This frequency is equivalent to 10,020 RPM (60 s x 167 cycles).

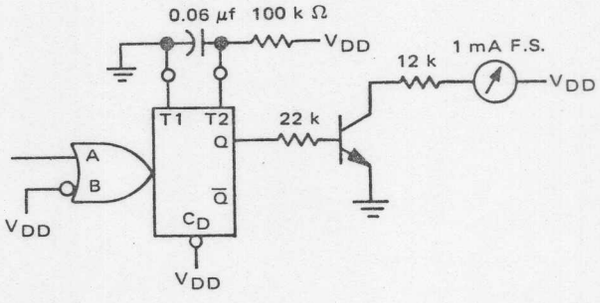

FIGURE 13 – Precision Analog Tachometer

When the circuit is used as an engine RPM indicator where the trigger inputs are derived from the distributor, the output frequency will depend not only on the engine RPMs, but also on the number of cylinders. For instance, an 8 cylinder engine, running at 1248 RPM, would generate triggers at the rate of (1248/60) x 8 = 167 Hz. This would produce a full-scale deflection, implying 10,020 RPM, instead of 1248 RPM. Since the trigger inputs were increased by a factor of 8, the duty cycles of the output should be reduced by a factor of 8. The 6 ms output should be decreased to (6 ms/8 =) 750 µs. R_X and/or C_X can be changed, accordingly, for engines with various numbers of cylinders and spark plugs.