AN-862
Application Note

INTERFACING DIGITAL CIRCUITS TO THYRISTOR CONTROLLED AC LOADS

This article describes the interfacing of triacs with integrated circuit drivers (e.g. logic gates) for the control of AC power loads. Included are the more popular logic families, such as TTL (including LSTTL) and CMOS with both positive and negative supply voltages. Examples of circuit isolation with opto-coupling are provided and the use of microprocessors as driving elements is discussed. Utilization of interfacing NPN and PNP transistors for thyristors requiring higher drive current is covered.

THYRISTORS

Thyristors are available as unidirectional devices (SCR's) or bidirectional devices (triacs). The SCR (Silicon Controlled Rectifier) conducts current in one direction only (from anode to cathode) in response to a positive-going gate signal. The gate signal causes a current flow from gate to cathode and will turn on the SCR only with the anode is positive with respect to the cathode. When the anode is negative, the SCR is in its blocking state. (See Figure 1a.)

Once the SCR has been triggered on, it will remain in the on state as long as the anode current remains above a specified minimum holding level (I_H), even if the triggering gate signal is removed. If the anode current drops below this "holding" current (I_H), the SCR unlatches (turns off). With an AC load, this happens at the end of the positive half cycle of anode voltage, resulting in a pulsating DC anode current in response to an AC anode voltage.

For AC load requirements, triacs are normally employed. The triac can be thought of as two SCR's connected in an inverse-parallel arrangement with one common gate lead. (See Figure 1b.). Without a gate trigger signal the device will be in its off state, resulting in a high impedance between terminals MT1 and MT2. When the triac is triggered on, a low MT1-MT2 impedance results. Typically, in the "on" condition, a triac (or SCR) will drop one to two volts across its main terminals at rated current.

Once turned on, the triac, like the SCR, will stay on whether or not the gate signal is present, until the current flowing through it drops below the holding current (I_H). This happens at the end of every half cycle of applied 60Hz. If a continuous "on" (low impedance) state is desired, the triac must be triggered at the beginning of every half cycle, or a continuous gate signal must be present.

The triac can be triggered on by either a positive or negative gate signal, on either the positive or negative half-cycle of applied MT2 voltage. This provides convenient triggering regardless of the gate trigger signal polarity, or MT2 voltage polarity. Triggering sensitivity, however, is determined by the polarity relationship between the trigger signal and the MT2 voltage. In Figure 2, this relationship is divided into four quadrants depicting the possible phase relations between the trigger signal and the MT2 voltage. Quadrant IV, where the gate is positive and MT2 is negative, is the least sensitive one; therefore, other quadrants of operation should be considered when adequate gate trigger current might be a problem. Use of a negative gate will assure triggering in quadrants II and III.

Quadrants II and III operation is particularly desirable when the triac is driven by 1C logic— not only because less gate trigger current is required in

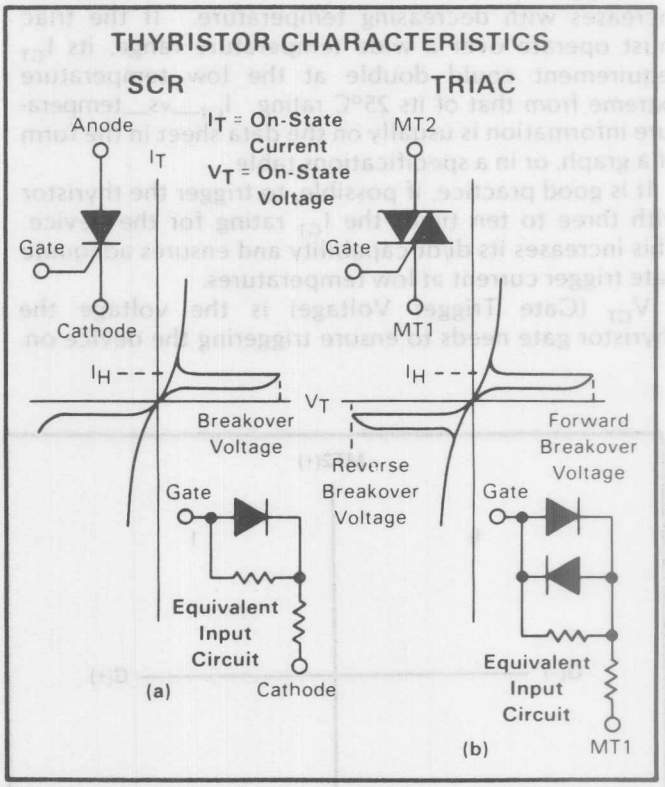

Figure 1. Static characteristics of SCRs **(a)** and Triacs **(b)**. In the absence of a gate signal, very little current flows through either device if the anode or MT2 voltage (SCR and Triac, respectively) remains below the breakover points (normal operating condition). When an appropriate gate trigger current is applied (see text), the devices go into conduction, resulting in a very low resistance across them. Turn-off can be achieved only by reducing the anode or MT2 current below the holding current, I_H.

these more sensitive quadrants, but also because IC power dissipation is reduced since an "active low" output from the IC is used for triggering.

There are other advantages to operating in Quadrants II and III. Since the rate of rise of on-state current of a triac (di/dt) is a function of how hard the triac's gate is turned on, a given IC output in Quadrants II and III will produce a greater di/dt capability than in the less sensitive Quadrant IV. Moreover, harder gate turn-on could reduce di/dt failure caused by localized junction burn-out that occurs when the thyristor tries to conduct too much current just after triggering, before the entire device has a chance to turn on. One additional advantage of quadrant II and III operation is that devices specified in all four quadrants are generally more expensive than devices specified in quadrants I, II and III due to the additional testing involved and the resulting lower yields.

Using Triacs

Once the triac load requirements are defined, an appropriate device selection can be made by referring to the triac current ratings of Table 1.

Two important thyristor parameters are gate trigger current (I_{GT}) and gate trigger voltage (V_{GT}).

I_{GT} (Gate Trigger Current) is the amount of gate trigger current required to turn the device "on". I_{GT} has a negative temperature coefficient— that is, the trigger current required to turn the device on increases with decreasing temperature. If the triac must operate over a wide temperature range, its I_{GT} requirement could double at the low temperature extreme from that of its 25°C rating. I_{GT} vs temperature information is usually on the data sheet in the form of a graph, or in a specifications table.

It is good practice, if possible, to trigger the thyristor with three to ten times the I_{GT} rating for the device. This increases its di/dt capability and ensures adequate gate trigger current at low temperatures.

V_{GT} (Gate Trigger Voltage) is the voltage the thyristor gate needs to ensure triggering the device on. This voltage is needed to overcome the input threshold voltage of the device. To prevent thyristor triggering, gate voltage should be kept to approximately 0.4V or less.

Like I_{GT}, V_{GT} increases with decreasing temperature.

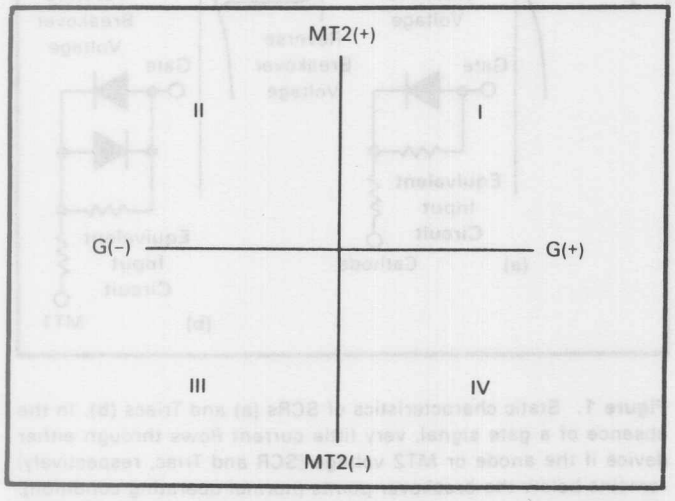

Figure 2. The Four Quadrants of Triac Operation. A Triac may be triggered into conduction by either a positive or negative-going gate signal, with either a positive or negative voltage applied between MT2 and MT1.

TABLE 1.
Triacs with Various Current Ratings

Sensitive Gate Triacs — Triac	$I_{T(RMS)}$
MAC92, 92A, 93, 93A	0.6 A
2N6068A, B-75A, B	4 A
MAC228, A	8 A
Non-sensitive Gate Triacs — Triac	**$T_{T(RMS)}$**
MAC91, A	0.6
2N6068-75	4.0
2N6342-49	8.0
2N6342A-49A	12
MAC15, A Series	15
MAC223, A Series	25
2N6157-65	30
2N5441-46	40

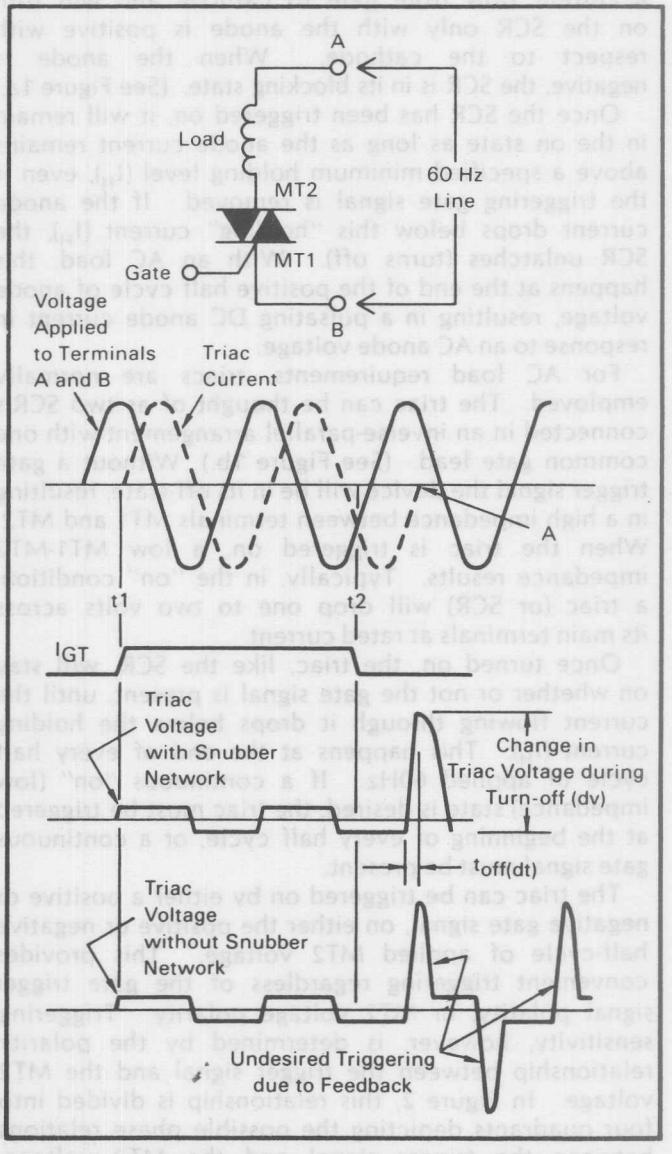

Figure 3. Inductive load Triac circuit and equivalent waveforms.

Inductive Load Switching

Switching of inductive loads, using triacs, may require special consideration in order to avoid false triggering. This false-trigger mechanism is illustrated in Figure 3 which shows an inductive circuit together with the accompanying waveforms.

As shown, the triac is triggered "on", at t1, by the positive gate current (I_{GT}). At that point, triac current flows and the voltage across the triac is quite low since the triac resistance, during conduction, is very low.

From point t1 to t2 the applied I_{GT} keeps the triac in a conductive condition, resulting in a continuous sinusoidal current flow that leads the applied voltage by 90°, due to the inductive nature of the circuit.

At t2, I_{GT} is turned off, but triac current continues to flow until it reaches a value that is less than the sustaining current (I_H), at point A. At that point, triac current is cut off and triac voltage is at a maximum. Some of that voltage is fed back to the gate via the internal capacitance (from MT2 to gate) of the triac.

TTL-TO-THYRISTOR INTERFACE

The subject of interfacing requires a knowledge of the output characteristics of the driving stages as well as the input requirements of the load. This section describes the driving capabilities of some of the more popular TTL circuits and matches these to the input demands of thyristors under various practical operating conditions.

TTL Circuits with Totem-Pole Outputs (e.g. MC5400 series)

The configuration of a typical totem-pole connected TTL output stage is illustrated in Figure 5a. This stage is capable of "sourcing" current to a load, when the load is connected from V_{out} to ground, and of "sinking" current from the load when the latter is connected from V_{out} to V_{cc}. If the load happens to be the input circuit of a triac (gate to MT_1), the triac will be operating in quadrants I and IV (gate goes positive) when connected from V_{out} to ground, and of "sinking" II and III (gate goes negative) when connected from V_{out} to V_{cc}.

Quadrant I-IV Operation

Considering first the gate-positive condition, Figure 5b,

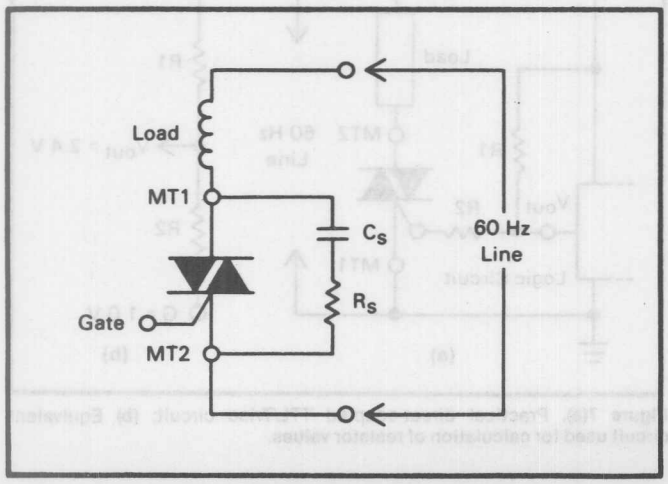

Figure 4. Triac with snubber network.

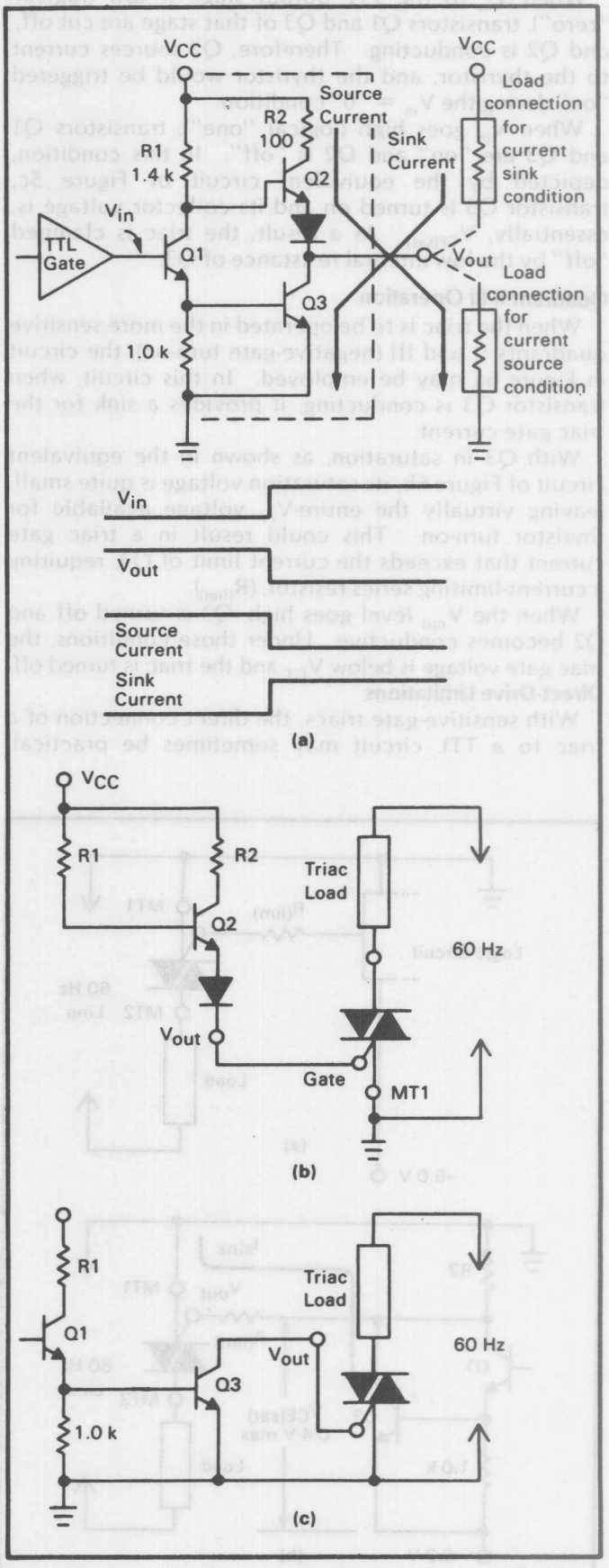

Figure 5(a). Totem-pole output circuit of MC5400-type TTL logic, together with voltage and current waveforms; **(b)** Equivalent circuit for triggering Triac with a positive voltage—Triac-on condition; **(c)** Triac-off condition.

the operation of the circuit is as follows:

When V_{in} to the TTL output stage is low (logical "zero"), transistors Q1 and Q3 of that stage are cut off, and Q2 is conducting. Therefore, Q2 sources current to the thyristor, and the thyristor would be triggered "on" during the V_{in} = "0" condition.

When V_{in} goes high (logical "one"), transistors Q1 and Q3 are "on" and Q2 is "off". In this condition, depicted by the equivalent circuit of Figure 5c, transistor Q3 is turned on and its collector voltage is, essentially, $V_{CE(sat)}$. As a result, the triac is clamped "off" by the low internal resistance of Q3.

Quadrant II-III Operation

When the triac is to be operated in the more sensitive quadrants II and III (negative-gate turn-on), the circuit in Figure 6a may be employed. In this circuit, when transistor Q3 is conducting, it provides a sink for the triac gate current.

With Q3 in saturation, as shown in the equivalent circuit of Figure 6b, its saturation voltage is quite small, leaving virtually the entire-V_{cc} voltage available for thyristor turn-on. This could result in a triac gate current that exceeds the current limit of Q3, requiring a current-limiting series resistor, ($R_{(lim)}$).

When the V_{out} level goes high, Q3 is turned off and Q2 becomes conductive. Under those conditions, the triac gate voltage is below V_{GT} and the triac is turned off.

Direct-Drive Limitations

With sensitive-gate triacs, the direct connection of a triac to a TTL circuit may sometimes be practical. However, the limitations of such circuits must be recognized.

For example:

For TTL circuits, the "high" logic level is specified as 2.4 volts. In the circuit of Figure 5a, transistor Q2 is capable of supplying a short-circuit output current (I_{sc}) of 20 to 55mA (depending on the tolerances of R1 and R2, and on the h_{FE} of Q2). Although this is adequate to turn a sensitive-gate triac "on", the specified 2.4-volt (high) logic level can only be maintained if the sourcing current is held to a maximum of 0.4mA — far less than the current required to turn on any thyristor. Thus, the direct connection is useful only if the driver need not activate other logic circuits in addition to a triac.

A similar limiting condition exists in the Logic "0" condition of the output, when the thyristor is to be clamped "off". In this condition, Q3 is conducting and V_{out} equals the saturation voltage ($V_{CE(sat)}$) of Q3. TTL specifications indicate that the low logic level (logic "0") may not exceed 0.4 volts, and that the sink current must be limited to 16mA in order not to exceed this value. A higher value of sink current would cause ($V_{CE(sat)}$) to rise, and could trigger the thyristor "on".

Circuit Design Considerations

Where a 5400-type TTL circuit is used solely for controlling a triac, with positive-gate turn-on (quadrants I-IV), a sensitive gate triac may be directly coupled to the logic output, as in Figure 5. If the correct logic levels must be maintained, however, a couple of resistors must be added to the circuit, as in Figure 7a. In this diagram, R1 is a pull-up which allows the circuit to source more current during a high logical output. Its value must be large enough, however, to limit the sinking current below the 16mA maximum when V_{out} goes low so that the logical zero level of 0.4 volts is not exceeded.

Resistor R2, a voltage divider in conjunction with R1, insures V_{OH} (the "high" output voltage) to be 2.4V or greater.

The resistor values may be calculated as follows:
For a supply voltage of 5V and a maximum sinking

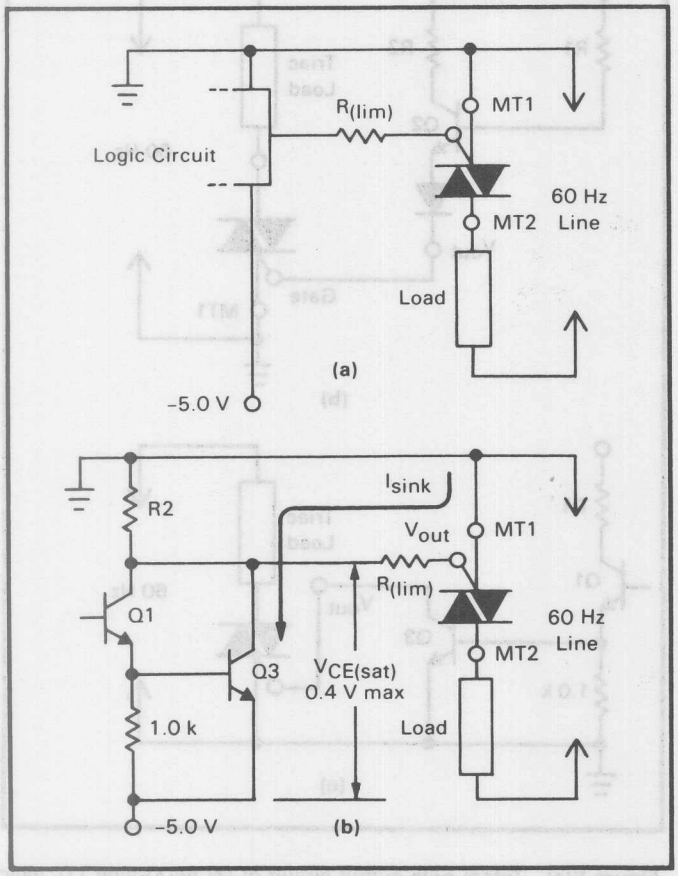

Figure 6(a). TTL Circuit for quadrant II and III Triac operation requiring negative V_{GT}; **(b)** Schematic illustrates Triac turn-on condition, V_{out} = Logical "0".

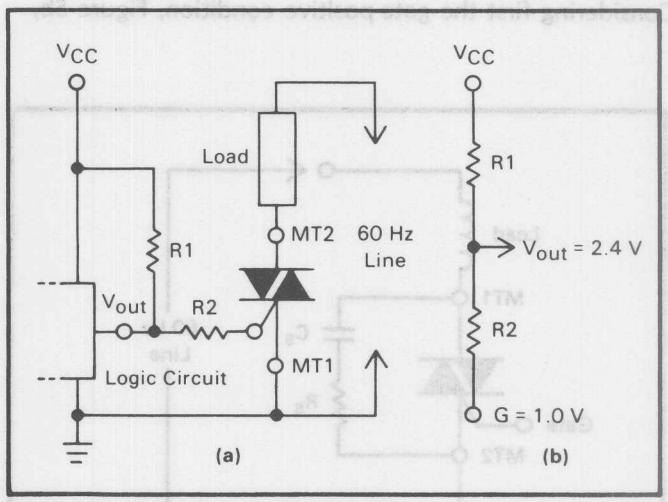

Figure 7(a). Practical direct-coupled TTL/Triac circuit; **(b)** Equivalent circuit used for calculation of resistor values.

current of 16mA:

$$R_1 \geq V_{cc}/16mA \geq 5/0.016 \geq 312\Omega$$

Thus, 330Ω ¼ W-resistor may be used. Assuming R_1 to be 330Ω and a thyristor gate "on" voltage (V_{GT}) of 1V the equivalent circuit of Figure 7b exists during the logical "1" output level. Since the logical "1" level must be maintained at 2.4 volts, the voltage drop across R_2 must be 1.4V. Therefore,

$$R_2 = 1.4/I_R = 1.4/V_{R_1/R_2} = 1.4/(2.6/330) \cong 175\Omega$$

A 180Ω-resistor may be used for R_2. If the V_{GT} is less than 1 volt, R_2 may need to be larger.

The MAC92A, 93A and 2N6068B triacs are compatible devices for this circuit arrangement, since they are guaranteed to be triggered on by 5mA, whereas the current through the circuit of Figure 7b is approximately 8MA, (V_{R_1}/R_1).

When the triac is to be turned on by a negative gate voltage, as in Figure 6b, the purpose of the limiting resistor $R_{(lim)}$ is to hold the current through transistor Q3 to 16mA. With a 5V supply, a triac V_{GT} of 1V and a maximum sink current of 16mA

$$R_{(lim)} = (V_{cc} - V_{GT})/I_{sink} = (5 - 1)/0.016 \geq 250\Omega$$

In practice, a 270Ω, ¼ W resistor may be used.

Open Collector TTL Circuit

The output section of an open-collector TTL gate is shown in Figure 8a.

A typical logic gate of this kind is the MC5401 Quad 2-input NAND gate circuit. This logic gate also has a maximum sink current of 16mA (V_{OL} = 0.4V max.) because of the Q1-(sat) limitations. If this logic gate is to source any current, a pull-up-collector resistor, R_1 (Figure 8b) is needed. When this TTL gate is used to trigger a thyristor, R_1 should be chosen to supply the maximum trigger current available from the TTL circuit (≈16mA, in this case). The value of R_1 is calculated in the same way and for the same reasons as in Figure 7. If a logical "1" level must be maintained at the TTL output (2.4V min.), the entire circuit of Figure 7 should be used.

For direct drive (logical "0") quadrants II and III triggering, the open collector, negative supplied (−5V) TTL circuit of Figure 9 can be used. Resistor R_1 can have a value of 270Ω, as in Figure 6. Resistor R_2 ensures that the triac gate is referenced to MT1 when the TTL gate goes high (off), thus preventing unwanted turn-on. An R_2 value of about 1K should be adequate for sensitive gate triacs and still draw minimal current.

Circuits utilizing Schottky TTL are generally designed in the same way as TTL circuits, although the current source/sink capabilities may be slightly different.

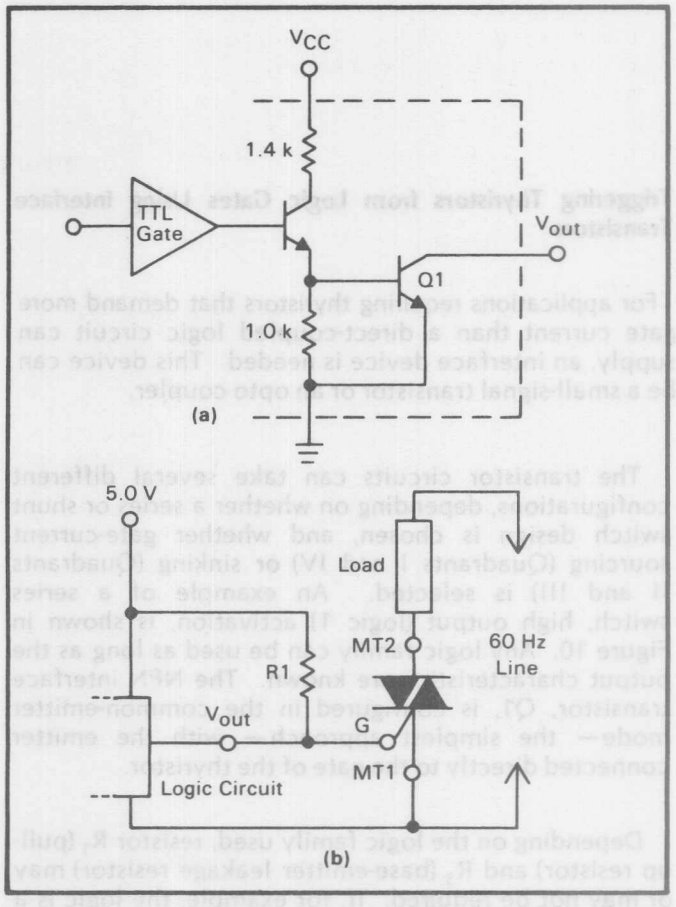

Figure 8(a). Output section of open-collector TTL; **(b)** For current sourcing, a pullup resistor, R1, must be added.

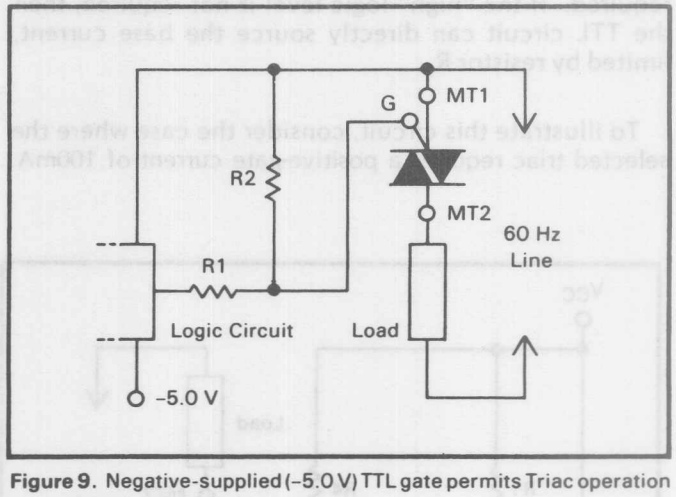

Figure 9. Negative-supplied (-5.0 V) TTL gate permits Triac operation in quadrants II and III.

Triggering Thyristors from Logic Gates Using Interface Transistors

For applications requiring thyristors that demand more gate current than a direct-coupled logic circuit can supply, an interface device is needed. This device can be a small-signal transistor or an opto coupler.

The transistor circuits can take several different configurations, depending on whether a series or shunt switch design is chosen, and whether gate-current sourcing (Quadrants I and IV) or sinking (Quadrants II and III) is selected. An example of a series switch, high output (logic 1) activation, is shown in Figure 10. Any logic family can be used as long as the output characteristics are known. The NPN interface transistor, Q1, is configured in the common-emitter mode— the simplest approach— with the emitter connected directly to the gate of the thyristor.

Depending on the logic family used, resistor R_1 (pull-up resistor) and R_3 (base-emitter leakage resistor) may or may not be required. If, for example, the logic is a typical TTL totem-pole output gate that must supply 5mA to the base of the NPN transistor and still maintain a "high" (2.4V) logic output, then R_1 and R_2 are required. If the "high" logic level is not required, then the TTL circuit can directly source the base current, limited by resistor R_2.

To illustrate this circuit, consider the case where the selected triac requires a positive-gate current of 100mA.

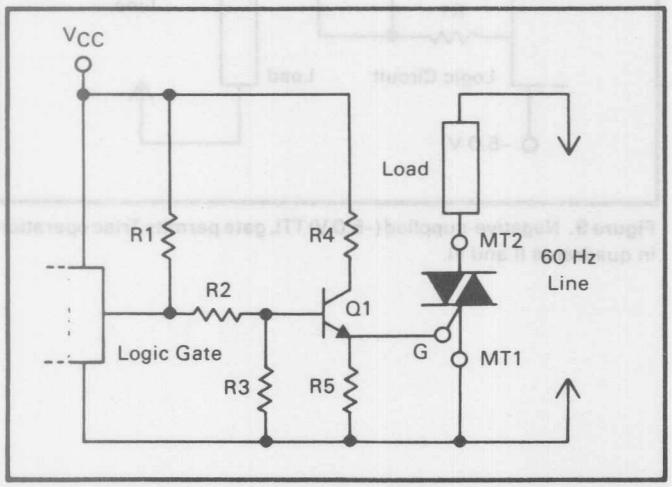

Figure 10. Series switch, high output (Logic "1").

The interface transistor, a popular 2N4401, has a specified minimum h_{FE} (at a collector current of 150mA) of 100. To ensure that this transistor is driven hard into saturation, under "worse case" (low temperature) conditions, a forced h_{FE} of 20 is chosen— thus, 5mA of base current. For this example, the collector supply is chosen to be the same as the logic supply (+5V); but for the circuit configuration, it could be a different supply, if required. The collector-resistor, R_4, is simply:

$$R_4 = (V_{cc} - V_{CE(SAT)} - V_{GT(TYP)})/I_{GT}$$
$$= (5 - 1 - 0.9)/100mA = 40\Omega$$

A 39ohm 1W resistor is then chosen, since its actual dissipation is about 0.4W.

If the "logic 1" output level is not important, then the base limiting resistor R_2 is required, and the pull-up resistor R_1 is not. Since the collector resistor of the TTL upper totem-pole transistor, Q2, is about 100Ω, this resistor plus R_2 should limit the base current to 5mA. Thus R_2 calculates to:

$$R_2 = [(V_{CC} - V_{BE} - V_{GT})/5mA] - 100\Omega$$
$$= [(5 - 0.7 - 0.9)/0.005]\,100\Omega$$
$$\approx 560\Omega \text{ (specified)}$$

When the TTL output is low, the lower transistor of the totem-pole, Q3, is a clamp, through the 560Ω resistor, across the 2N4401; and, since the 560Ω resistor is relatively low, no leakage-current shunting resistor, R_3, is required.

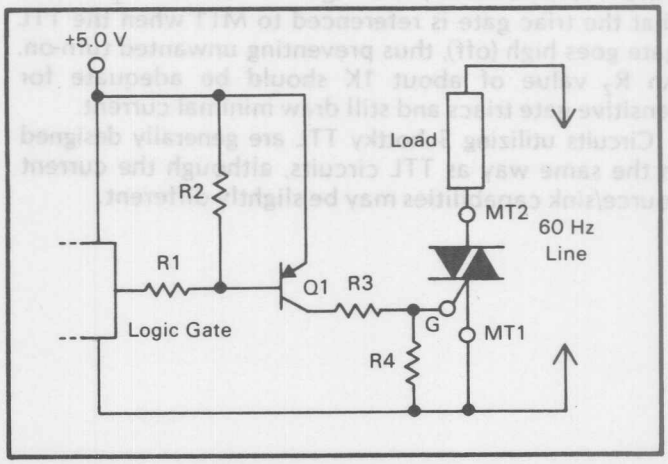

Figure 11. Low-Logic activation with interface transistor.

In a similar manner, if the TTL ouput must remain at "logic 1" level, the resistor R_1 can be calculated as described earlier (R_3 may or may not be required).

For low-logic activation (logic "0"), the circuit of Figure 11 can be used. In this example, the PNP-interface transistor 2N4403, when turned on, will supply positive-gate current to the thyristor. To ensure that the high logic level will keep the thyristor off, the logic gate and the transistor emitter must be supplied with the same power supply. The base resistors, as in the previous example, are dictated by the output characteristics of the logic family used. Thus if a TTL gate circuit is used, it must be able to sink the base current of the PNP transistor (I_{OL}(MAX) = 16mA).

When thyristor operation in quadrants II and III is desired, the circuits of Figure 12 and 13 can be used; Figure 12 is for high logic output activation and Figure 13 is for low. Both circuits are similar to those of Figures 10 and 11, but with the transistor polarity and power supplies reversed.

Figure 12 sinks current from the thyristor gate through a switched NPN transistor whose emitter is referenced to a negative supply. The logic circuit must also be referenced to this negative supply to ensure that transistor Q_1 is turned off when required; thus, for TTL gates, V_{EE} would be $-5V$.

In Figure 13, the logic-high bus, which is now ground, is the common ground for both the logic, and the thyristor and the load. As in the first example (Figure 10), the negative supply for the logic circuit ($-V_{EE}$) and the collector supply for the PNP transistor need not be the same supply. If, for power-supply current limitations, the collector supply is chosen to be another supply ($-V_{cc}$), it must be within the V_{CEO} ratings of the PNP transistor. Also, the power dissipation of collector resistor, R_4, is a function of $-V_{CC}$ —the lower $-V_{CC}$, the lower the power rating.

the four examples shown use gate-series switching to activate the thyristor and load (when the interface transistor is off, the load is off). Shunt-switching can also be used if the converse is required, as shown in Figures 14 and 15. In Figure 14, when the logic output is high, NPN transistor, Q_1, is turned on, thus clamping the gate of the thyristor off. To activate the load, the logic output goes low, turning off Q_1 and allowing positive gate current, as set by resistor R_3, to turn on the thyristor.

In a similar manner, quadrants II and III operation is derived from the shunt interface circuit of Figure 15.

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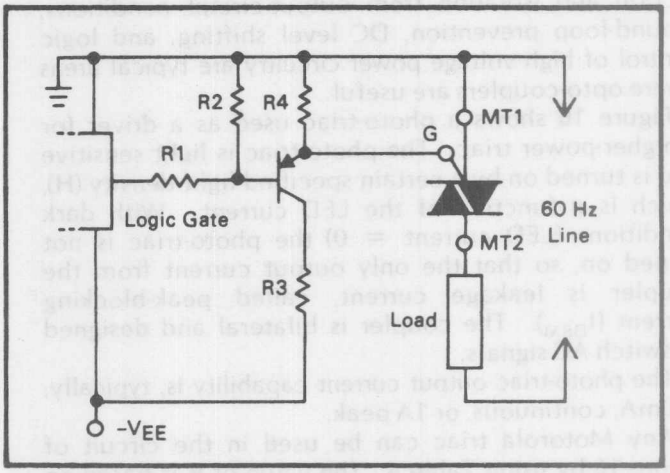

Figure 13. Low-logic output activation.

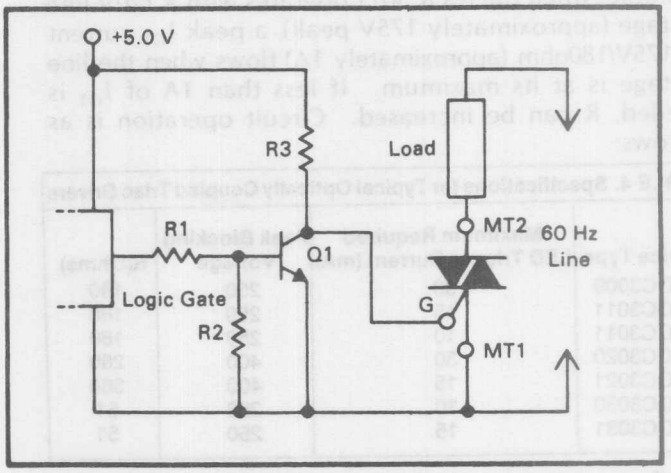

Figure 14. Shunt-interface circuit (high-logic output).

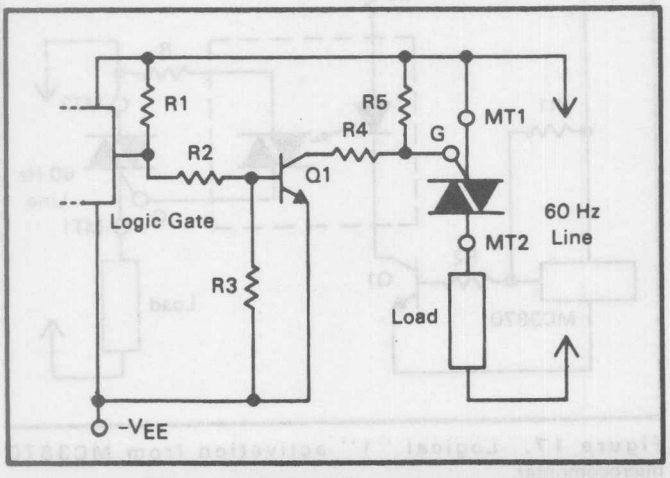

Figure 12. High-logic output activation.

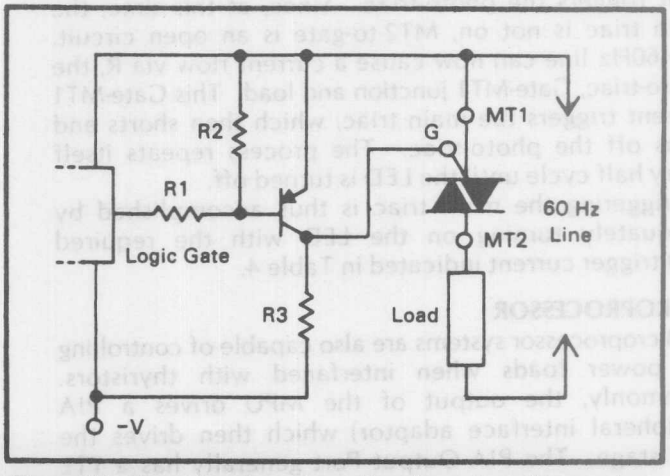

Figure 15. Shunt-interface circuit (Quadrants I and III operation).

OPTICAL ISOLATORS/COUPLERS

An Optoelectronic isolator combines a light-emitting device and a photo detector in the same opaque package that provides ambient light protection. Since there is no electrical connection between input and output, and the emitter and detector cannot reverse their roles, a signal can pass through the coupler in one direction only.

Since the opto-coupler provides input circuitry protection and isolation from output-circuit conditions, ground-loop prevention, DC level shifting, and logic control of high voltage power circuitry are typical areas where opto-couplers are useful.

Figure 16 shows a photo-triac used as a driver for a higher-power triac. The photo-triac is light sensitive and is turned on by a certain specified light density (H), which is a function of the LED current. With dark conditions (LED current = 0) the photo-triac is not turned on, so that the only output current from the coupler is leakage current, called peak-blocking current (I_{DRM}). The coupler is bilateral and designed to switch AC signals.

The photo-triac output current capability is, typically, 100mA, continuous, or 1A peak.

Any Motorola triac can be used in the circuit of Figure 16 by using Table 4. The value of R is based on the photo-triac's current-handling capability. For example, when the MOC3011 operates with a 120V line voltage (approximately 175V peak), a peak I_{GT} current of 175V/180ohm (approximately 1A) flows when the line voltage is at its maximum. If less than 1A of I_{GT} is needed, R can be increased. Circuit operation is as follows:

TABLE 4. Specifications for Typical Optically Coupled Triac Drivers

Device Type	Maximum Required LED Trigger Current (mA)	Peak Blocking Voltage	R(Ohms)
MOC3009	30	250	180
MOC3011	15	250	180
MOC3011	10	250	180
MOC3020	30	400	260
MOC3021	15	400	360
MOC3030	30	250	51
MOC3031	15	250	51

When an op-amp, logic gate, transistor or any other appropriate device turns on the LED, the emitted light triggers the photo-triac. Since, at this time, the main triac is not on, MT2-to-gate is an open circuit. The 60Hz line can now cause a current flow via R, the photo-triac, Gate-MT1 junction and load. This Gate-MT1 current triggers the main triac, which then shorts and turns off the photo-triac. The process repeats itself every half cycle until the LED is turned off.

Triggering the main triac is thus accomplished by adequately turning on the LED with the required LED-trigger current indicated in Table 4.

MICROPROCESSOR

Microprocessor systems are also capable of controlling AC power loads when interfaced with thyristors. Commonly, the output of the MPU drives a PIA (peripheral interface adaptor) which then drives the next stage. The PIA Output Port generally has a TTL

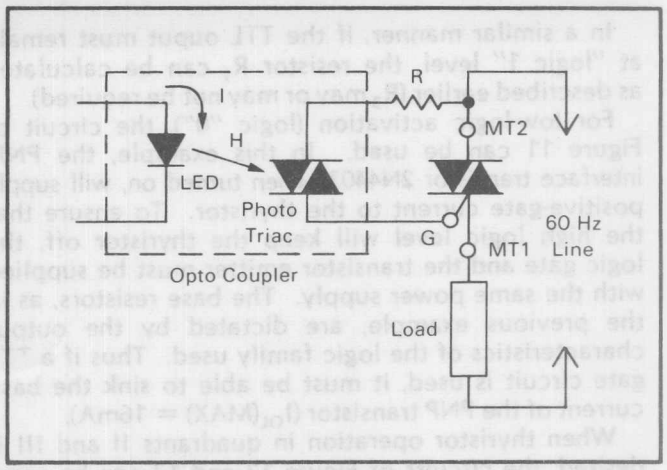

Figure 16. Optically-coupled Triac driver is used to drive a higher-power Triac.

compatible output with significantly less current source and sink capability than standard TTL. (MPU's and PIA's are sometimes constructed together on the same chip and called microcontrollers or microcomputers.)

When switching AC loads from microcomputers, it is good practice to optically isolate them from unexpected load or AC line phenomenon to protect the computer system from possible damage. In addition, optical isolation will make UL recognition possible.

A typical TTL-compatible microcomputer, such as the MC3870 offers the following specifications:

$I_{OH} = 300\ \mu A\ (V_{OH} = 2.4V)$

$I_{OL} = 1.8\ mA\ (V_{OL} = 0.4V)$

$V_{CC} = 5.0V$

Since this is not adequate for driving the opto-coupler directly (10mA for the MOC3011), an interface transistor is necessary.

The circuit of Figure 17 may be used for thyristor triggering from the 3870 logical "1".

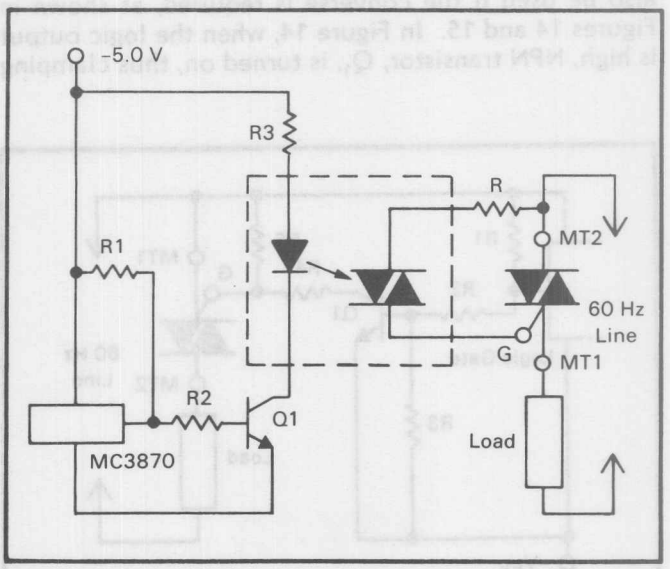

Figure 17. Logical "1" activation from MC3870 microcomputer.

The interface transistor, again, can be the 2N4401. With 10mA of collector current (for the MOC3011) and a base current of 0.75mA, the $V_{CE(sat)}$ will be approximately 0.1V.

R_1 can be calculated as in a previous example, Specifically:

1.8mA (maximum I_{OL} for the 3870) > $5V/R_1$; $R_1 > 2.77K$

R_1 can be 3K 1/4W

With a base current of 0.75mA, R_1 will drop (0.75mA) (3K) or 2.25V. This causes a V_{OH} of 2.75V, which is within the logical "1" range.

$R_2 = [2.75V - V_{BE}(on)]/I_B = (2.75 - 0.75)/0.75 = 2.66K$

R_2 can be a 2.7K, ¼ W resistor.

R_3 must limit I_C to 10mA:

$$R_3 = [5V - V_{CE}(sat) - V_F(diode)/10mA]$$
$$= (5 - 0.1 - 1.2)/10mA = 370\Omega$$

Since R_3 is relatively small, no base-emitter leakage resistor is required.

Figure 18 shows logical "0" activation. Resistor values are calculated in a similar way.

THE CMOS INTERFACE

Another popular logic family, CMOS, can also be used to drive thyristors.

As shown in Figure 19a, the output stage of a typical CMOS Gate consists of a P-channel MOS device connected in series with an N-channel device (drain-to-drain), with the gates tied together and driven from a

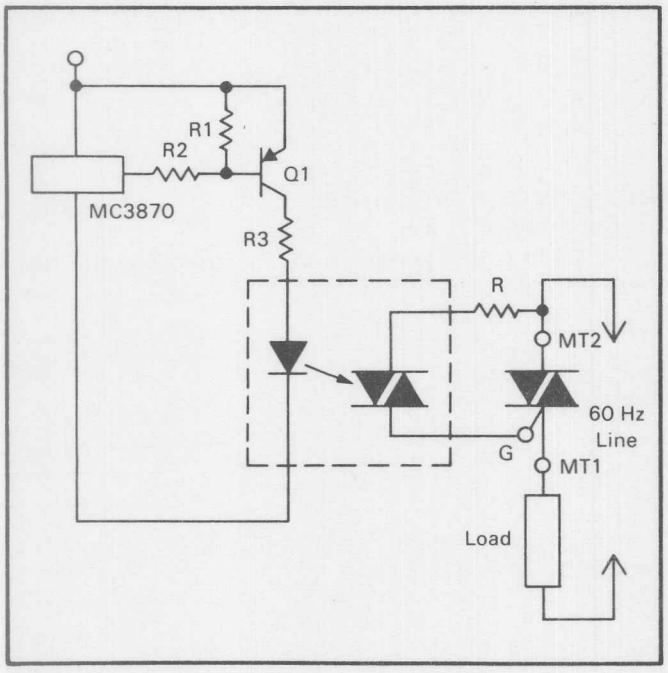

Figure 18. Logical "0" activation.

common input signal. When the input signal goes high, logical 1, the P-channel device is essentially "off" and conducts only leakage current (I_{DSS}), on the order of picoamps. The N-channel unit is forward-biased and, although it has a relatively high "on" resistance ($R_{DS(on)}$), the drain-to-source voltage of the N-channel device (V_{DS}) is very low (essentially zero) because of the very low drain current (V_{DSS}) flowing through the device. Conversely, when the input goes low (zero), the P-channel device is turned fully "on", the N-channel device is "off" and the output voltage will be very near V_{DD}.

When interfacing with transistors or thyristors, the CMOS Gate is current-limited mainly by its relatively high "on" resistance, the DC resistance between drain and source, when the device in turned on.

The equivalent circuits for sourcing and sinking current into an external load is shown in Figures 19b and 19c. Normally, when interfacing CMOS to CMOS, the logic outputs will be very near their absolute maximum states (V_{DD} or 0.0V) because of the extremely small load currents. With other types of loads (e.g. triacs), the current, and the resulting output voltage, is dictated by the simple voltage divider of $R_{DS(on)}$ and the load resistor R_L, where $R_{DS(on)}$ is the total series and/or parallel resistance of the devices comprising the NOR and NAND function.

Interfacing CMOS gates with thyristors requires a knowledge of the "on" resistance of the gate in the source and sink conditions. The on-resistance of CMOS devices is not normally specified on data sheets.

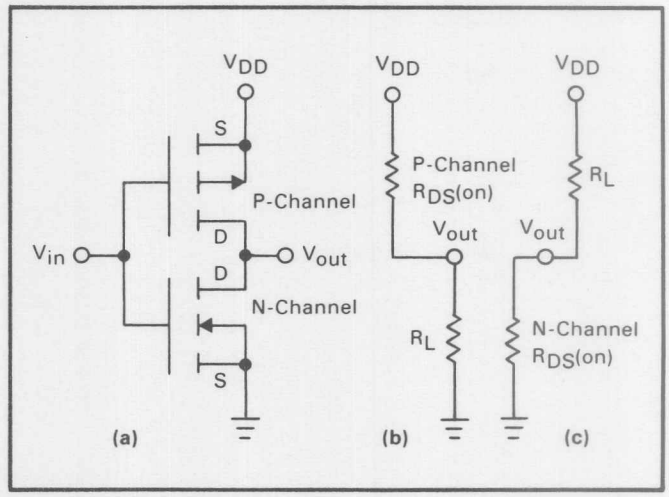

Figure 19(a). Output section of a typical CMOS gate; **(b)** Equivalent current-sourcing circuit is activated when V_{in} goes low, turning the P-channel device fully on; **(c)** Equivalent current sinking circuit is activated when the input goes high and turns the N-channel device on.

It can easily be calculated, however, from the output drive currents, which are specified. The drive (source/sink) currents of typical CMOS gates at various supply voltages are shown in Table 2. From this information, the *on* resistance for "worse case" design is calculated as follows:

For the source condition

$$R_{DS(ON)(max)} = (V_{DD} - V_{OH})/I_{OH(min)}$$

Similarly, for the sink current condition:

$$R_{DS(ON)(max)} = V_{OL}/I_{OL(min)}$$

Values of $R_{DS(ON)}$ for the various condition shown in Table 2 are tabulated in Table 3.