MOTOROLA
Semiconductor Products Inc.

AN-874
Application Note

MACROCELL ARRAYS: CONCEPT — FEATURES — CAD INTERFACE

High technology array-based products offer the advantages of custom LSI circuits, yet overcome the problems of high costs and long design cycles. Recent developments in Array technology make use of Macrocell building blocks rather than primitive gates for easier design and higher performance. Additional developments in computer-aided-design customer interface systems simplify the job of developing Array circuit options. This note examines Motorola's Macrocell Array concept with special emphasis on the CAD user interface.

MACROCELL ARRAYS — AN ALTERNATIVE TO CUSTOM LSI

The semiconductor industry has developed three basic approaches to help satisfy the demand for digital Large-Scale Integrated (LSI) circuits:

1. Standard off-the-shelf products
2. Custom circuits
3. Gate arrays

The first approach represents the lowest cost option for the LSI user because such circuits are normally sold in relatively large quantities to the entire industry, thereby benefitting from the cost advantage of large-volume manufacture. However, because of the high risk factor involved in having the industry adopt a particular LSI circuit as a standard (thereby permitting large-volume sales), the line of standard LSI circuits is limited.

The second approach provides each customer with exactly the circuits he needs (usually on a proprietary basis), but the cost per circuit is quite high unless the volume requirements are large enough to amortize the relatively high development costs. Moreover, development time of complex custom circuits can be on the order of 1 to 2 years.

The third approach involves a standard array of a large number of gate circuits diffused into a silicon chip. The circuit designer provides the semiconductor manufacturer with an interconnecting metallization pattern that converts these basic gates into functional custom circuits. This approach represents a trade-off between development cost and time on the one hand, and performance on the other hand. Performance is compromised because of the necessity for using a gate as the basic building block for LSI circuits. This results in longer propagation delays, compared with similar functions using ECL series-gating techniques (for example), and usually involves a relatively inefficient use of chip real estate.

To supplement the three techniques described above, Motorola has developed the Macrocell approach toward custom LSI — an approach that circumvents the excessive cost and time factor of custom circuits, and reduces the deficiencies of the conventional gate arrays.

THE MACROCELL ARRAY CONCEPT

Motorola's Macrocell Array products provide a means for economical high performance custom LSI logic circuits. Performance is achieved by the combination of an advanced MOSAIC I oxide-isolated bipolar integrated circuit process and a series gated emitter-coupled logic (ECL) macrocell circuit technology. Advantages of the macrocell array concept include:

1. Proprietary custom LSI circuits
2. Quick design turn-around time
3. MSI complexity macrocell logic blocks rather than primitive gates
4. Computer-Aided-Design (CAD) customer interface
5. Family of array products so array size, performance, power dissipation, and package can be optimized to match the system need
6. Common macrocell library, design rules, and CAD interface for all arrays

MCA1200 ECL, the first macrocell array product, consists of 106 logic blocks called macrocells. The circuit has 48 Major (M) macrocells, 32 Interface (I) macrocells, and 26 Output (O) macrocells organized as shown in Figure 1. Each M, I, and O block contains transistors and resistors that can be interconnected with metal patterns to perform logic functions. For example, one M macrocell metal pattern makes a multiplexer, another a dual flip-flop, another an OR-AND gate structure, another an adder, etc. A predefined macrocell library contains 85 different M, I, and O logic functions available to the array option designer.

The Macrocell Array concept is based on careful use of two metal layers. Metal defining the macrocell logic function is restricted to first layer metal directly over the cell area. Vertical routing channels are also on first layer metal in columns between macrocells, see Figure 1.

Second layer metal contains all horizontal routing channels which run directly over macrocells. All interconnections to macrocell I/O ports are made to second layer horizontal channels, and interconnections between first and second layer metal are made in the columns between macrocells. A strength of the macrocell array concept is a uniform X-Y routing grid across the array surface.

Additional first and second layer metal is required to reach each I/O bonding pad, distribute power, and route ECL reference voltages to the macrocells. However, this is fixed overhead metal common to all array options, and is automatically handled by the CAD user interface system. The option designer is only required to supply data unique to the logic function.

A major benefit of ECL circuit design is the ability to use series gated structures. Each major (M) macrocell contains 52 transistors and 48 resistors as illustrated with the Half Cell Schematic in Figure 2. Interconnecting transistors and resistors with different metal patterns enable the circuit to perform a wide variety of different logic functions.

Each major macrocell can be divided into two independent half cells, an upper and a lower half. This allows the option designer to place, for example, a 4-input Exclusive OR gate (½ of H11 in the Macrocell Library) into the upper half of a major macrocell and a full adder (½ of H52) into the lower half. The functional complexity of a major macrocell ranges from simple gates to complex MSI logic elements. Figure 3 illustrates the interconnection of components to form a 4-input Exclusive OR gate and Figure 4 is an example of a dual full adder.

MCA500ALS, the first TTL compatible macrocell array, builds on a proven macrocell concept, yet is optimized to meet the speed, power dissipation, packaging, power supply, and logic level requirements of the LS TTL market.

The MCA500ALS Macrocell Array consists of 77 logic blocks called macrocells. Each circuit has 24 major (M) macrocells, 26 Input (I) macrocells, and 27 Output (O) macrocells organized as shown in Figure 5. Input and output macrocells do usable gating logic in addition to translating between TTL signals and ECL macrocells. A predefined macrocell library contains 80 different M, I, and O logic functions all available to the engineer designing an LSI circuit (macrocell array option). Option designers have the freedom to select a macrocell function for any M, I or O location in Figure 5, but cannot switch cell types. For example, a major M macrocell dual flip-flop could be placed in any or all M macrocells, but not placed in an I or O location. Figure 6 is a listing of several macrocell logic functions according to macrocell type.

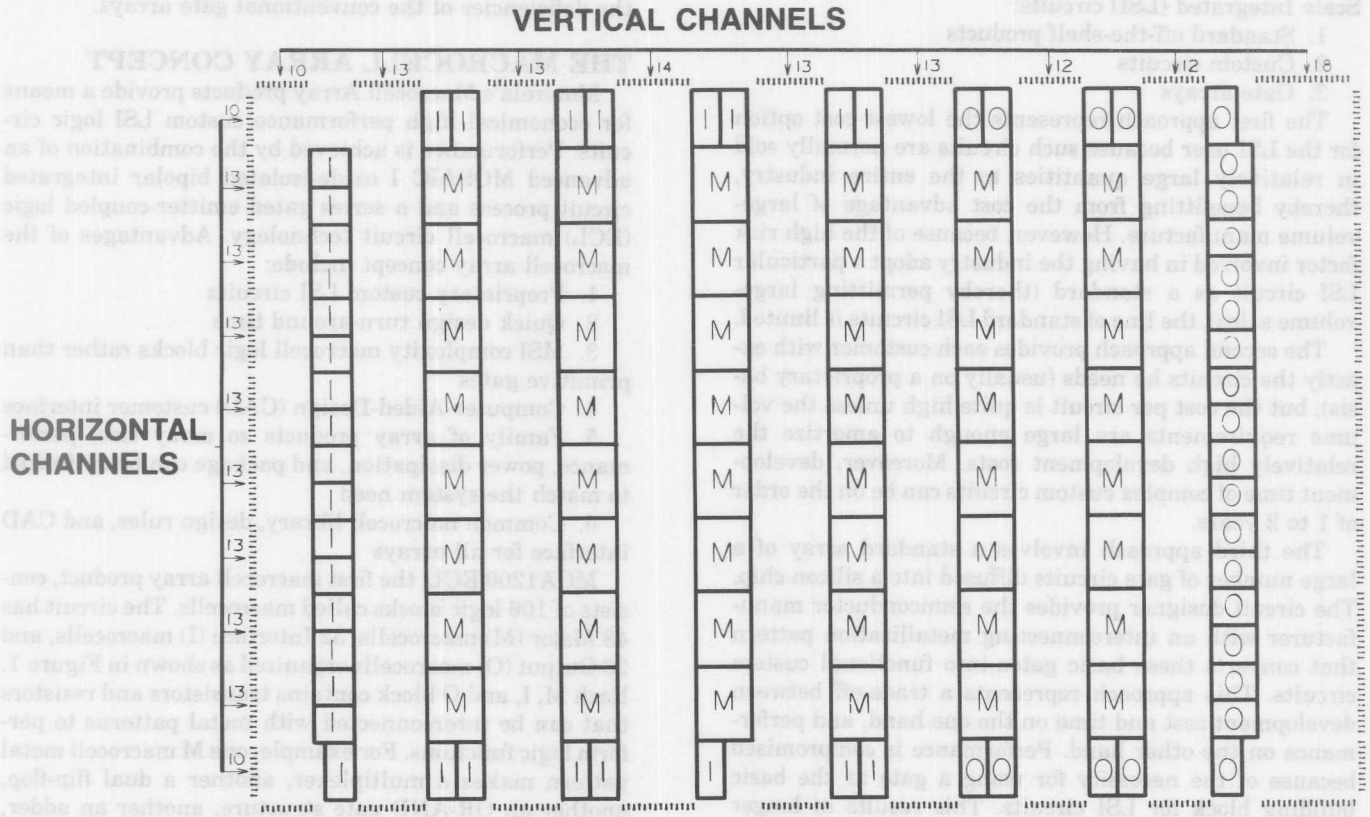


FIGURE 1 — MCA1200ECL Macrocell Array Metal Interconnect Channels

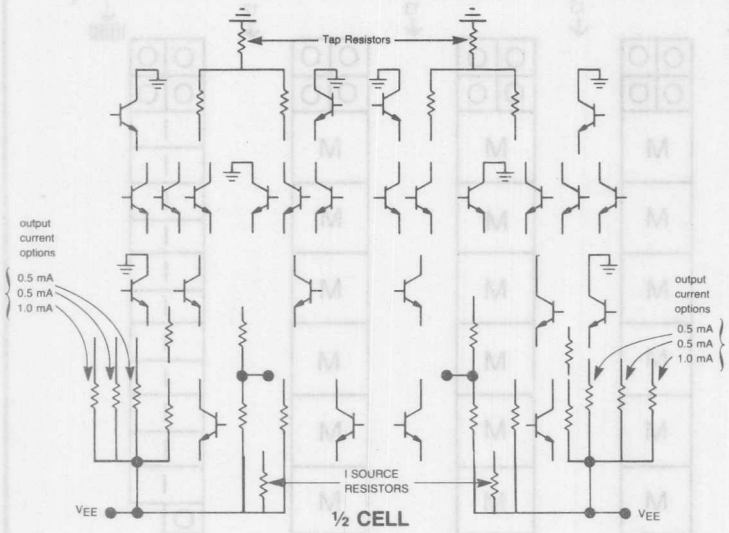
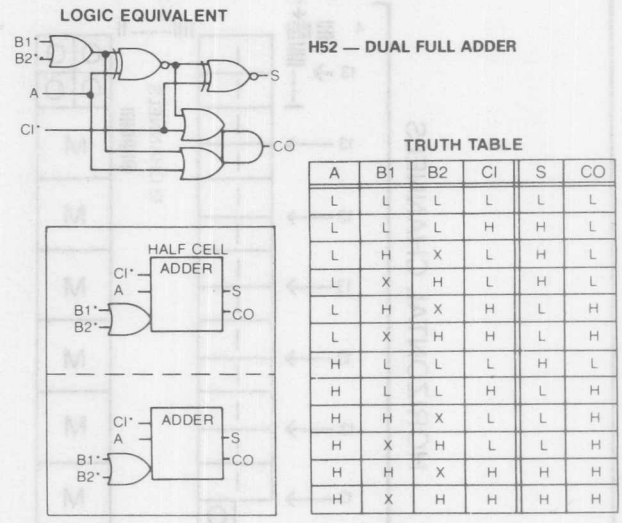
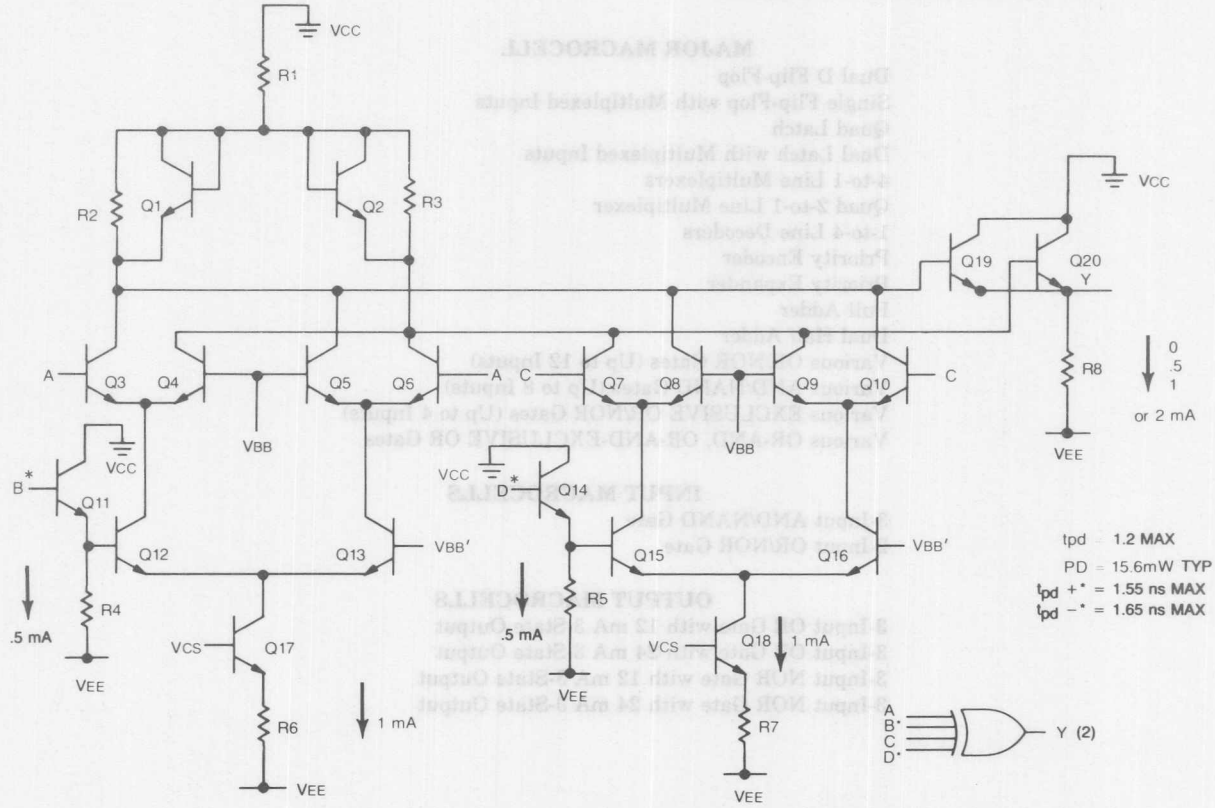


FIGURE 2 — Half Cell Schematic (1/2 of Major Cell)



A	B1	B2	CI	S	CO
L	L	L	L	L	L
L	L	L	H	H	L
L	H	X	L	H	L
L	X	H	L	H	L
L	H	X	H	L	H
L	X	H	H	L	H
H	L	L	L	H	L
H	L	L	H	L	H
H	H	X	L	L	H
H	X	H	L	L	H
H	H	X	H	H	H
H	X	H	H	H	H

FIGURE 4 — Two Full Adders can be placed in one major cell



$$Y = A\bar{B}CD + \bar{A}BCD + AB\bar{C}D + ABC\bar{D} + A\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}CD + A\bar{B}\bar{C}D$$

FIGURE 3 — Schematic of 4 input Exclusive OR Gate (1/2 H11)

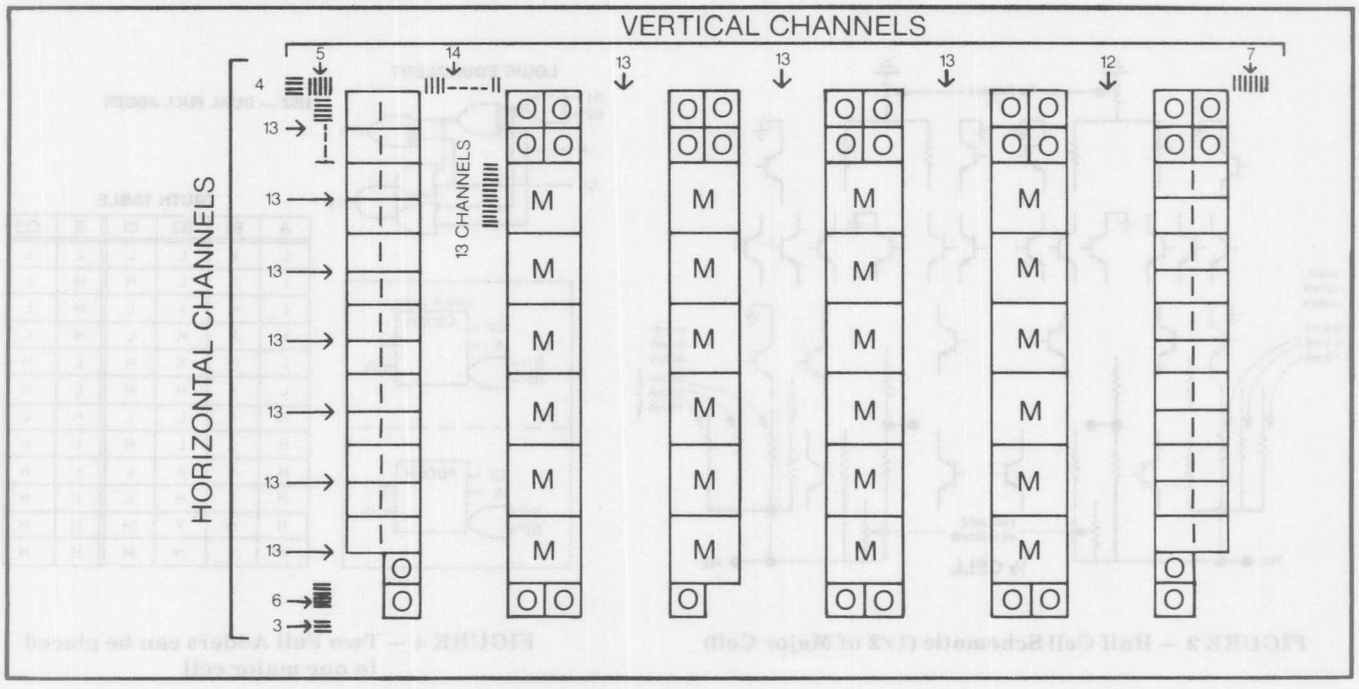


FIGURE 5 — MCA500ALS Macrocell layout shows the relative positions of macrocells within the array. Horizontal and vertical routing channels connect macrocells, much as a printed circuit board layout.

MAJOR MACROCELL

Dual D Flip-Flop
Single Flip-Flop with Multiplexed Inputs
Quad Latch
Dual Latch with Multiplexed Inputs
4-to-1 Line Multiplexers
Quad 2-to-1 Line Multiplexer
1-to-4 Line Decoders
Priority Encoder
Priority Expander
Full Adder
Dual Half Adder
Various OR/NOR Gates (Up to 12 Inputs)
Various AND/NAND Gates (Up to 8 Inputs)
Various EXCLUSIVE OR/NOR Gates (Up to 4 Inputs)
Various OR-AND, OR-AND-EXCLUSIVE OR Gates

INPUT MACROCELLS

3-Input AND/NAND Gate
2-Input OR/NOR Gate

OUTPUT MACROCELLS

3-Input OR Gate with 12 mA 3-State Output
3-Input OR Gate with 24 mA 3-State Output
3-Input NOR Gate with 12 mA 3-State Output
3-Input NOR Gate with 24 mA 3-State Output

FIGURE 6 — Macrocell Logic Functions are a Focus Point to Understand the Macrocell Array Concept. A Predefined Macrocell Library Contains the Logic Blocks Common to Digital System Designs.

MCA500ALS MACROCELL ARRAY FEATURES

Basic features of the MCA500ALS Macrocell Array are itemized in Table 1. Most features are easily understood, however a few require additional explanation.

Items 4 and 5 break the 27 output macrocells into groups of 24 output drivers and three 3-state control macrocells. The MCA500ALS array can have a maximum of 24 output signals each of which has a TTL compatible 3-state control input. Three-state control macrocells convert internal M macrocell logic levels to 3-state control signals. Output and 3-state control macrocells use the same macrocell library functions and only differ with respect to circuit use. Any of the 27 O macrocells can be output drivers up to a maximum of 24.

Items 6 and 7 are for comparison purposes. It is difficult to specify a maximum gate count without defining which macrocells are used. Dual adders result in the highest gate count at 533 equivalent gates. A more typical usage would be flip-flop macrocells which yield a 389 gate count. Realize with macrocells, gates can be both OR/NOR or AND/NAND with true and complement outputs. This is more efficient than having only one gate type; for example a 3-input NAND, to do all logic. Also, M and I macrocell outputs can be wire ORed together with routing channels for additional logic power.

TABLE 1 — Basic MCA500ALS Array Features

1. Total Macrocells	77
2. Major Macrocells	24
3. Input Macrocells	26
4. Output Macrocells	24
5. Three-State Control Macrocells	3
6. Max Equivalent Gates — Adders	533
7. Max Equivalent Gates — Flip-Flops	389
8. Power Dissipation — All Cells Used	1.0 Watt Typ
9. Power Per Gates (389 Typ)	2.6 MW Typ
10. Die Size	165 × 183 Mils
11. Internal Gate Delay	2.5 ns Typ
12. Average M Macrocell Delay	2.8 ns Typ
13. Equivalent Gate Delay	1.4 ns Typ
14. Input Macrocell Delay	3.2 ns Typ
15. Output Macrocell Delay	10.0 ns Typ
16. I Macrocell Input Current	LS TTL
17. O Macrocell Drive — Up To 10	24 mA
18. O Macrocell Drive — Any Output	8.0 mA
19. Output Logic Levels	LS TTL
20. Horizontal Routing Channels	108
21. Vertical Routing Channels	82
22. Dual-In-Line Packages	28, 40, 48 Pins
23. Leadless LSI Package	68 Pin
24. Ambient Temperature Range	0–70° C
25. Operating Junction Temperature	0–115° C
26. Absolute Maximum Junction Temperature	150° C
27. Power Supply	+5.0 Volts ± 5%
28. Customer Interface	CAD

Items 8 and 9 show typical power figures, again for comparison purposes. Most of the MCA500ALS array power dissipation is due to TTL output drivers. ECL macrocells doing most of the logic consume only a few hundred milliwatts. Power dissipation can be controlled by the number of outputs used and by selecting between 8.0 and 24 mA output drive. Power per gate is calculated by dividing 1.0 watt by a typical gate usage. Realize that internally gates operate at a much lower power and the Item 9 figure includes output drivers.

Items 11, 12 and 13 define M macrocell performance. If a major macrocell is used as a simple OR/NOR gate, propagation delay is typically 2.5 ns. More important in an LSI circuit design is macrocell delay. Average delay through a full macrocell is typically 2.8 ns. Since macrocells average the equivalent of two gate levels, the effective M macrocell gate delay is a very fast 1.4 ns.

Items 20 and 21 define the number of horizontal and vertical routing channels available for interconnecting macrocells, see Figure 1. Channel density coupled with Motorola's excellent automatic place and route CAD programs should allow full array utilization to be successfully routed.

Table 2 provides a comparison of key parameters for three members of the Macrocell array family. Future additions to the family will include a 2500 equivalent gate ECL compatible array (MCA2500ECL) and a 2800 equivalent gate TTL compatible array (MCA2800ALS).

TABLE 2 — Macrocell Array Comparison Chart

PARAMETER	MCA 1200 ECL	MCA 600 ECL	MCA 500 ALS	MCA 1300 ALS
1. MAXIMUM EQUIVALENT GATES	1192	652	533	1280
2. MAJOR MACROCELLS	48	24	24	60
3. INTERFACE/INPUT MACROCELLS	32	25	26	40
4. OUTPUT MACROCELLS	26	18	24	40
5. MAXIMUM GATE DELAY	1.2 nS	1.2 nS	4.0 nS	4.0 nS
6. POWER DISSIPATION	4 WATTS	2.5 WATTS	1.0 WATTS	1.4 WATTS
7. PACKAGE	68 LEADLESS	28,40 DIL 68 LEADLESS	28,40,48 DIL 68 LEADLESS	40,48 DIL 68, 84 LEADLESS
8. TEMPERATURE RANGE	0–70° C	0–70° C	0–70° C	0 - 70°C
9. I/O INTERFACE	MECL 10,000	MECL 10,000	LSTTL	LSTTL
10. DESIGN INTERFACE	CAD	CAD	CAD	CAD

MACROCELL ARRAY ADVANTAGES

Macrocell arrays have made advantages over arrays using only simple gates, especially when designing an LSI circuit function. First is performance. ECL series gated structures provide the highest performance logic for a given integrated circuit process. Logic functions that would require two to four stages of delay with primitive gates can be designed with macrocell series gates using a single delay stage. For example, a full adder macrocell requires only 1.4 times the delay of a simple gate. Another advantage of ECL structures is low output impedance which make macrocells less vulnerable to metal capacitance and fanout loading than other logic types.

A second advantage is logic flexibility. The circuit designer has access to all common logic elements in a library. Gate types include OR/NOR, AND/NAND, EXCLUSIVE OR/NOR, OR AND, OR AND INVERT structures, plus a full selection of MSI logic blocks. Equally important, macrocells are optimized to do each logic function. Flip-flops are designed as flip-flops rather than an interconnection of 6 or 7 gates. Reset, gated clock, and complementary Q and $\overline{Q}$ outputs are all integrated into the master-slave design. While possible to have a CAD library that helps convert simple gates into complex logic elements, it only partially compensates for the inherent advantages of hardware macrocells.

Third is the ability to specify logic performance. Each macrocell is performance specified according to logic function. An M36 (4 to 1 Multiplexer) will have the same maximum delay regardless of where it is placed in the array. In an array where only gate delays are specified, a complex multiplexer performance would be dependent on gate placement and interconnect metal, thus difficult to specify or design with prior to actual place and route.

Fourth is routability. The macrocell array concept has proven to be highly routable compared to many designs using only simple gates. Fewer routing channels are required since MSI logic elements are all defined within macrocells and do not require valuable routing area. Automatic route and place software in Motorola's Macrocell Array Computer-Aided-Design Customer Interface has successfully 100% placed and routed array designs using 90 to 95% of the macrocell locations. With manual assistance, macrocell array designs approaching 100% of the macrocell positions have been successfully routed.

Fifth is human interface. Since the mid-1960s engineers have been designing digital logic systems by selecting SSI and MSI logic circuits from a data book, placing them on a circuit board, and interconnecting package pins with circuit board runs. The same skills are utilized in a Macrocell Array design except the circuit board is condensed into a very high performance LSI integrated circuit.

MACROCELL ARRAY CAD INTERFACE

A Motorola developed CAD system provides the critical interface between Motorola's Bipolar LSI Operations in Mesa, Arizona and engineers doing MCA option development. The CAD system is contained in a Motorola corporate computer system and operates through telephone lines to graphics equipment (Tektronix 4014 Computer Display Terminal and 4662 or 4663 plotter) at the user's location.

The Macrocell Array CAD system provides the following benefits:

1. All worksheets for option development.
2. Interactive graphics for accepting design information. Option data can be digitized on the plotter or entered through the CRT screen.
3. Error checking to catch design rule violations.
4. Simulation programs to verify logic accuracy and metal interconnects.
5. Documentation of an option design by plotting both logic and metal interconnect.
6. Test programming aids through simulation and fault grade.
7. Dynamic simulation to verify ac performance.
8. Converts test vectors generated in simulation to a format required by the automatic test equipment for functional testing.
9. Converts the final macrocell selection and interconnects into a format compatible with equipment making the metal and via interconnect masks.
10. Array plots for final design verification.
11. Macrocell Array automatic place and route software to simplify option development.

Each MCA option is customized by selecting macrocell functions from the library and placing them in cell locations on the array chip, and by interconnecting macrocells to each other and to I/O bonding pads. Cell placement and routing can be entered manually through the CRT terminal and/or plotter, generated automatically with place and route software in the CAD system, or a combination of both manual and automatic to optimize a particular design. Although the CAD system flags design rule violations, MCA macrocell selection, placement and routing accuracy remains the user's responsibility.

A final user design requirement is to provide a functional test sequence. The CAD helps again by allowing the designer to exercise a possible test sequence with a simulated model of the array. It also provides a fault grade program which allows the user to determine any array logic not tested by a given test sequence.

The CAD flow diagram in Figure 7 provides more detail on CAD system operation. Starting with a development contract in the upper right corner, Motorola and the array customer agree on number of options, time schedules, and business terms. At this point, the user receives a password into a Motorola computer system and is able to access CAD software over phone lines on a time share arrangement. CAD software includes interface to the 4014 graphics system, MCA operating system with the macrocell library and routing data entry, simulation based on LOGCAP software, interface to Motorola CALMA graphics and final test systems, and the MCA automatic route and placement program.

While using graphics equipment, the option designer follows a sequence of design steps. The following list is based on Motorola's automatic place and route software:

1. Define logic function in terms of macrocells.
2. Build a CAD net file describing all interconnect paths between macrocells and I/O pads.
3. Generate test sequence files defining inputs, outputs, and logic level forcing functions.
4. Run a CAD simulation checking the interconnect net list against the test sequence.
5. Run fault grade to qualify the test sequence ability to check circuit functionality.
6. Correct test sequence or step 2 net file, if needed.
7. Use the automatic place and route software to generate a macrocell array option layout, and plot the final results.
8. Manually route any interconnects not covered by routing software.
9. Finalize the option design by selecting input pull-down resistors (MECL I/O arrays only), selecting special macrocell output currents, and final checking for design rule violations.
10. Run dynamic simulation to verify ac performance.
11. Notify Motorola the design is complete.

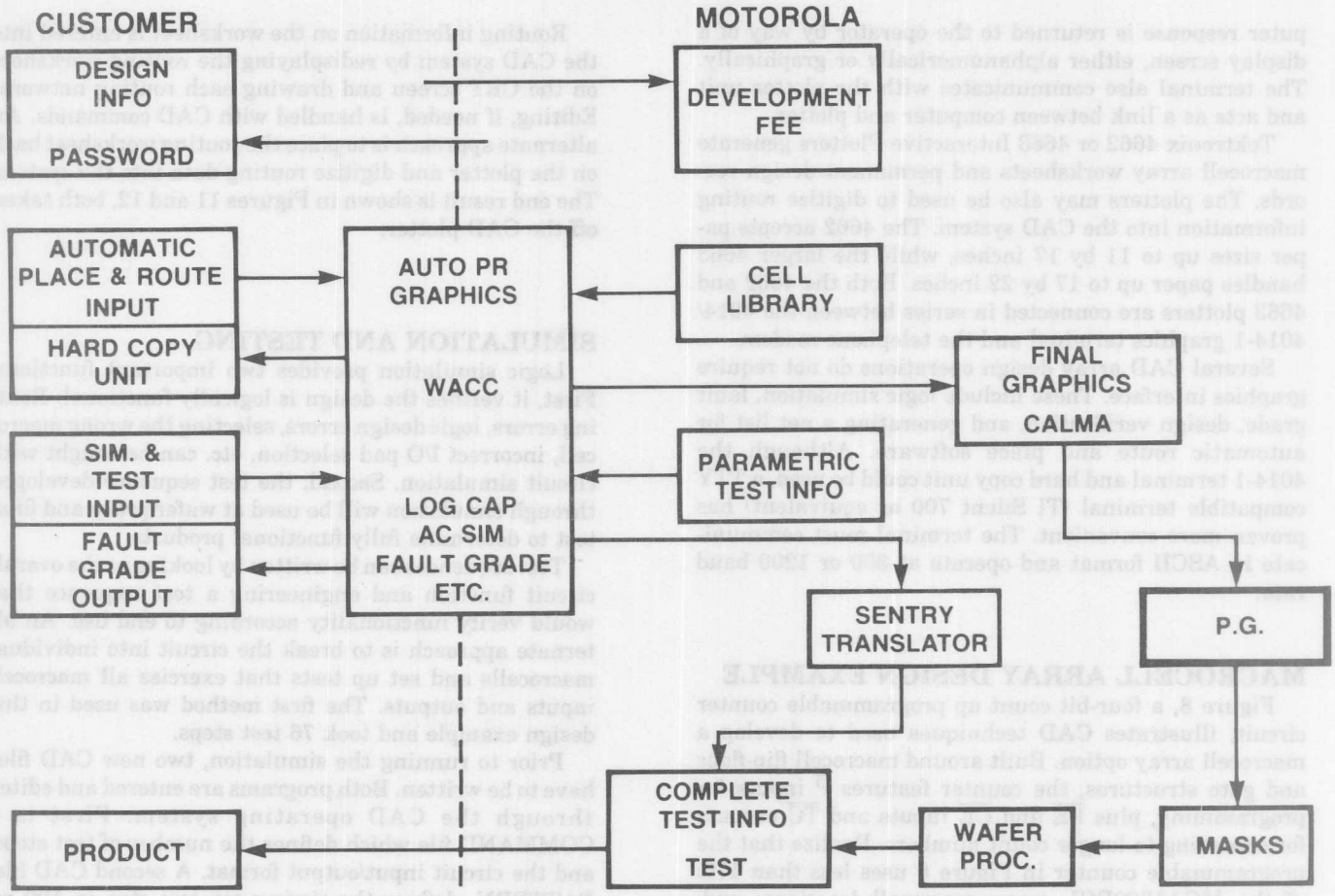


FIGURE 7 — Macrocell Array Option Development Flow

After the customer's option design is complete, Motorola translates option data to semiconductor metal and via mask sets through a CALMA graphics system. Wafer processing is then completed using wafers which can be produced in quantity and banked waiting for customizing metal. Finished wafers are tested at wafer probe using the customer defined test sequence located in the CAD system and Motorola added parametric testing. Packaged parts are final tested and good parts shipped for customer evaluation.

An important feature of the MCA CAD system is the ability to handle all design operations unique to manufacturing an integrated circuit product. Option design work performed by the customer including logic definition, placement, metal routing, and test tables are all common to designing a printed circuit board. The CAD system handles interconnecting transistors and resistors into logic blocks, selection of first and second layer metal, metal widths and spacing, via locations and sizes, power distribution, shorting unused gate inputs, and other IC related tasks.

HARDWARE DESCRIPTION

Macrocell array CAD software is resident on IBM compatible computer systems located in Scottsdale, Arizona at the Motorola Western Area Computer Center (WACC). CAD software is available to macrocell array customers on a time-share basis over normal telephone lines or datacomm network at 300 or 1200 baud data rates.

The following hardware is required at the user's location:

1. Tektronix 4014 or 4014-1 Computer Display Terminal.
2. Tektronix 4662 or 4663 Interactive Digital Plotter.
3. Tektronix 4952 Joystock (optional).
4. 300 baud or 1200 baud modem.
5. TTY compatible keyboard — printer terminal.

The 4014/4014-1 Computer Display Terminal permits the user to interface with WACC computers in a manner understandable by both computer and human operator. By typing on the keyboard, a macrocell array option designer can instruct CAD software to perform various macrocell array design functions. The CAD system com-

puter response is returned to the operator by way of a display screen, either alphanumerically or graphically. The terminal also communicates with the plotter unit and acts as a link between computer and plotter.

Tektronix 4662 or 4663 Interactive Plotters generate macrocell array worksheets and permanent design records. The plotters may also be used to digitize routing information into the CAD system. The 4662 accepts paper sizes up to 11 by 17 inches, while the larger 4663 handles paper up to 17 by 22 inches. Both the 4662 and 4663 plotters are connected in series between the 4014/4014-1 graphics terminal and the telephone modem.

Several CAD array design operations do not require graphics interface. These include logic simulation, fault grade, design verification, and generating a net list for automatic route and place software. Although the 4014-1 terminal and hard copy unit could be used, a TTY compatible terminal (TI Silent 700 or equivalent) has proven more convenient. The terminal must communicate in ASCII format and operate at 300 or 1200 baud rate.

MACROCELL ARRAY DESIGN EXAMPLE

Figure 8, a four-bit count up programmable counter circuit, illustrates CAD techniques used to develop a macrocell array option. Built around macrocell flip-flops and gate structures, the counter features $\overline{P}$ inputs for programming, plus $\overline{PE}$ and $\overline{CE}$ inputs and $\overline{TC}$ outputs for cascading to longer count numbers. Realize that the programmable counter in Figure 8 uses less than 17% of the MCA1200ECL array macrocell locations; and, therefore, is a CAD example only and not intended to represent a practical use of the array.

Due to circuit simplicity, automatic route and place software was bypassed. Manual route and place also allows a better graphic representation of the various CAD design phases. The CAD system is first used for macrocell placement. After logging on with a Motorola assigned account and password, the CAD program LAYOUT is initialized. LAYOUT establishes an option design name and draws an array outline on the graphics CRT screen. CAD placement commands list the required macrocell types along the right-hand CRT screen side. Additional placement commands position each macrocell in the selected location on chip, and provide for editing if needed. After placement the CRT screen would appear as Figure 9.

Following macrocell placement, a routing worksheet, see Figure 10, can be drawn on the CAD plotter. The worksheet, expanded to the upper right quadrant for clarity, contains routing channel tic marks for both horizontal and vertical channels, package pin numbers, macrocell names, and macrocell I/O port designations with respect to routing channel placement.

With a relatively simple circuit like the 4-bit programmable counter, routing can be drawn off-line, directly on the worksheet. Placement is not critical since there are more than enough routing channels and the need for changing macrocell placement is unlikely. After routing the worksheet according to array design rules, the circuit is ready for input to the CAD system.

Routing information on the worksheet is entered into the CAD system by redisplaying the routing worksheet on the CRT screen and drawing each routing network. Editing, if needed, is handled with CAD commands. An alternate approach is to place the routing worksheet back on the plotter and digitize routing data into the system. The end result is shown in Figures 11 and 12, both taken off the CAD plotter.

SIMULATION AND TESTING

Logic simulation provides two important functions. First, it verifies the design is logically functional. Routing errors, logic design errors, selecting the wrong macrocell, incorrect I/O pad selection, etc. can be caught with circuit simulation. Second, the test sequence developed through simulation will be used at wafer probe and final test to determine fully functional products.

Test sequences can be written by looking at the overall circuit function and engineering a test sequence that would verify functionality according to end use. An alternate approach is to break the circuit into individual macrocells and set up tests that exercise all macrocell inputs and outputs. The first method was used in this design example and took 76 test steps.

Prior to running the simulation, two new CAD files have to be written. Both programs are entered and edited through the CAD operating system. First is a COMMAND file which defines the number of test steps, and the circuit input/output format. A second CAD file, PATTERN, defines the timing per test step in 100 picosecond increments. It also defines the logic state of each input. COMMAND and PATTERN files are entered with either the 4014 graphics terminal or a printer terminal. The printer terminal is recommended for simulation because it prints hard copy results more conveniently than the graphics plotter.

Fault grade measures the simulation test sequence with respect to exercising every macrocell input and output. This is accomplished by sequentially forcing each node to a logic 1 or logic 0 while running the simulation test sequence and checking that the fault can be detected at test outputs. Fault grade program output lists all tested nodes and those not detected with faults.

Successfully completing simulation means the difficult part of option design is done. Remaining CAD operations take care of circuit details and provide a final check for design rule violations. LAYOUT, the program initially used for macrocell placement and array routing, also has commands for completing the design.

In either case with manual routing as shown in the program counter example or with automatic route and place as outlined earlier, the Macrocell Array CAD system successfully bridges the gap between logic designers and IC manufacturer. The customer uses design talent to develop an end product with modern high performance LSI circuits while the IC supplier is able to handle a large number of custom circuit functions with minimum design resources.

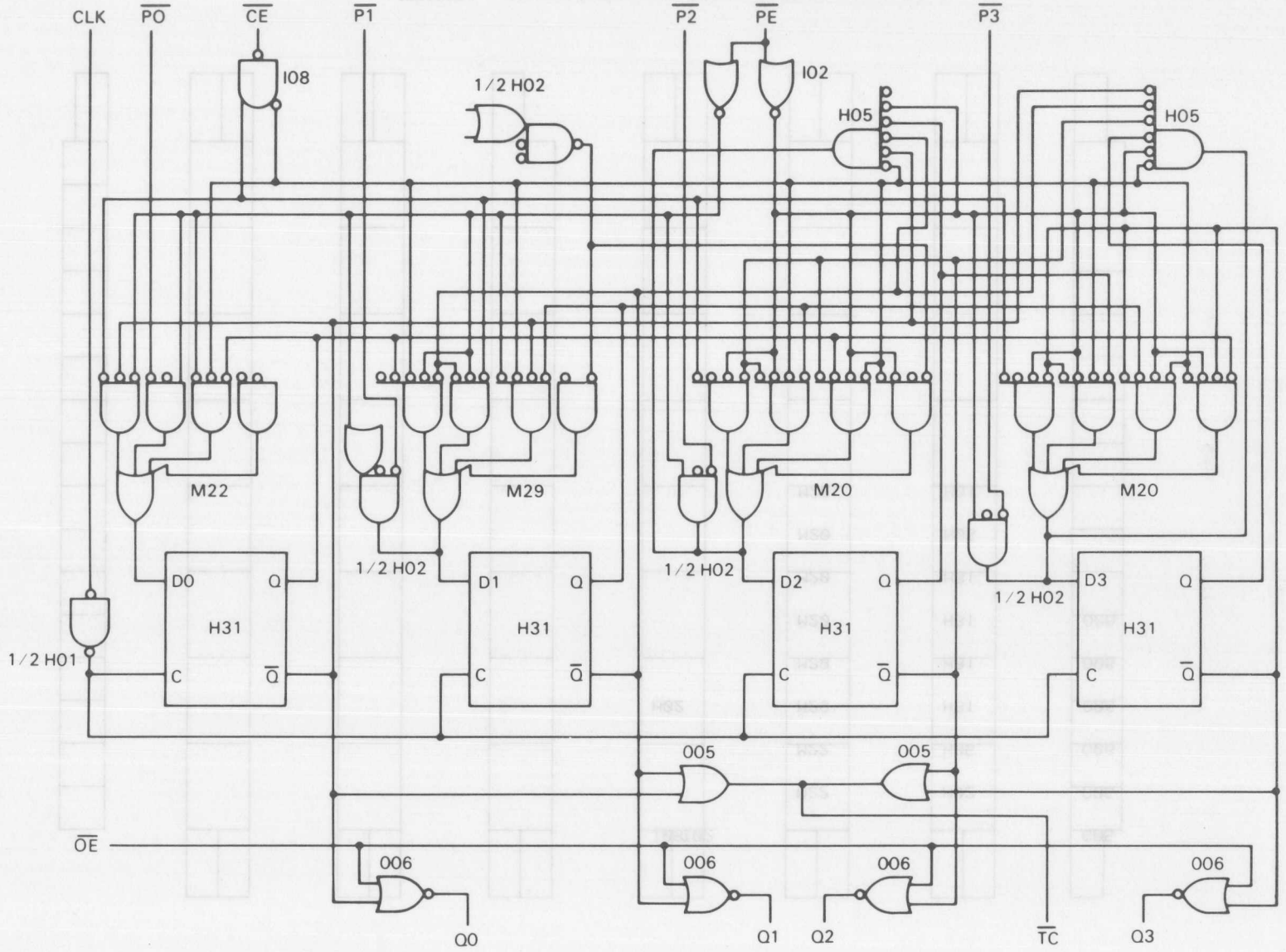


FIGURE 8 — 4-Bit Programmable Counter

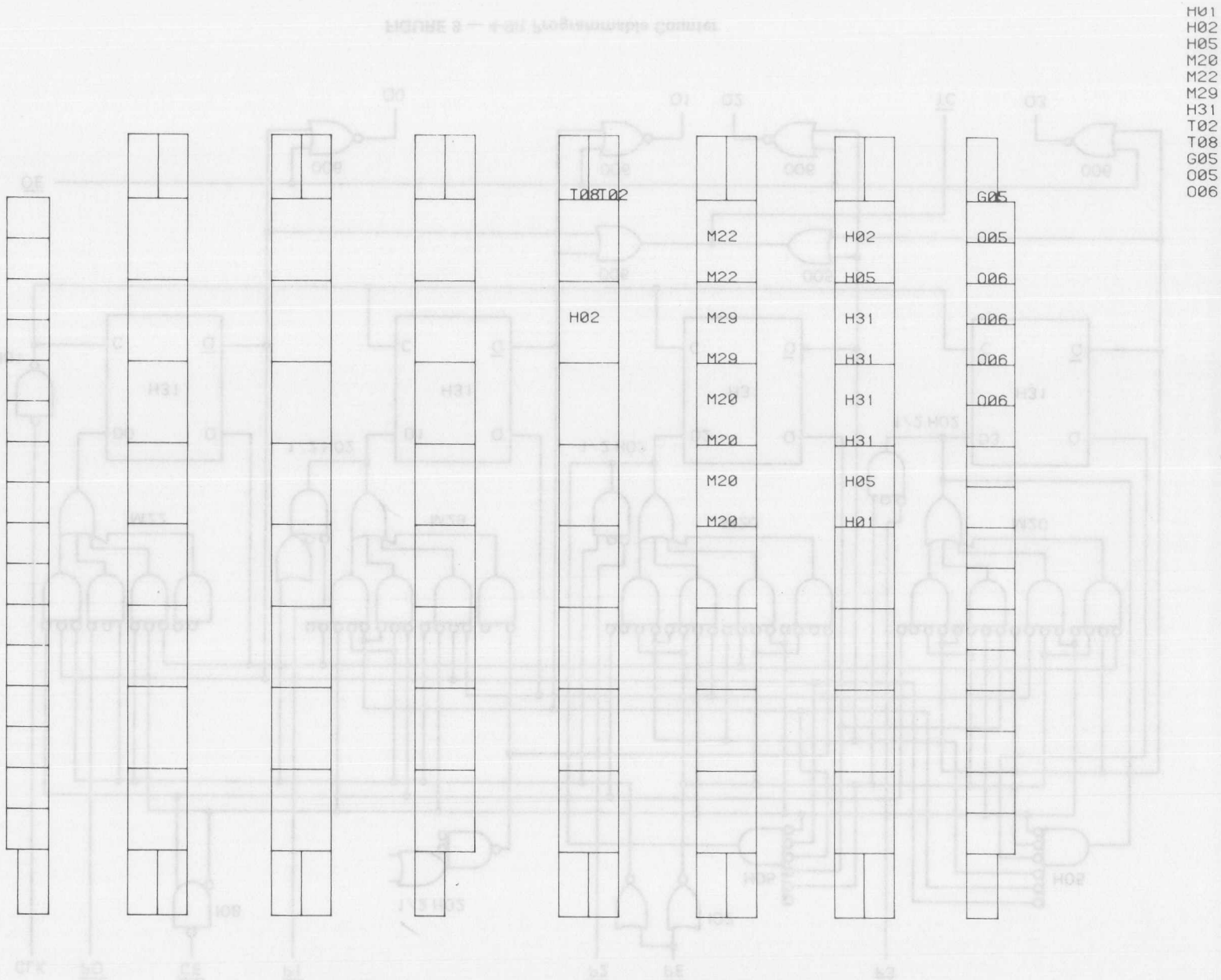


FIGURE 9 — Macrocell Placement Diagram 4-Bit Programmable Counter

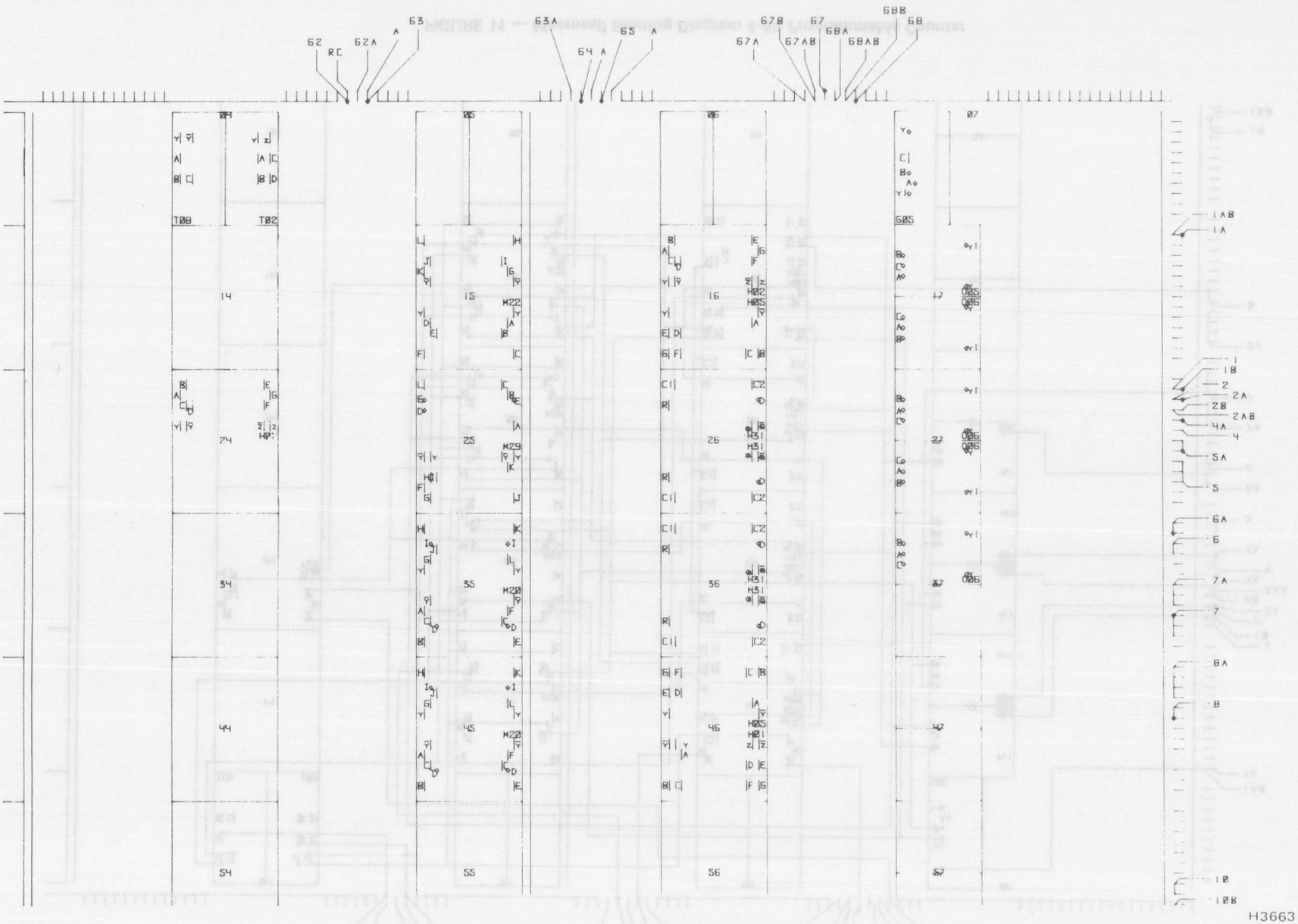


FIGURE 10 — Macrocell Routing Worksheet 4-Bit Programmable Counter

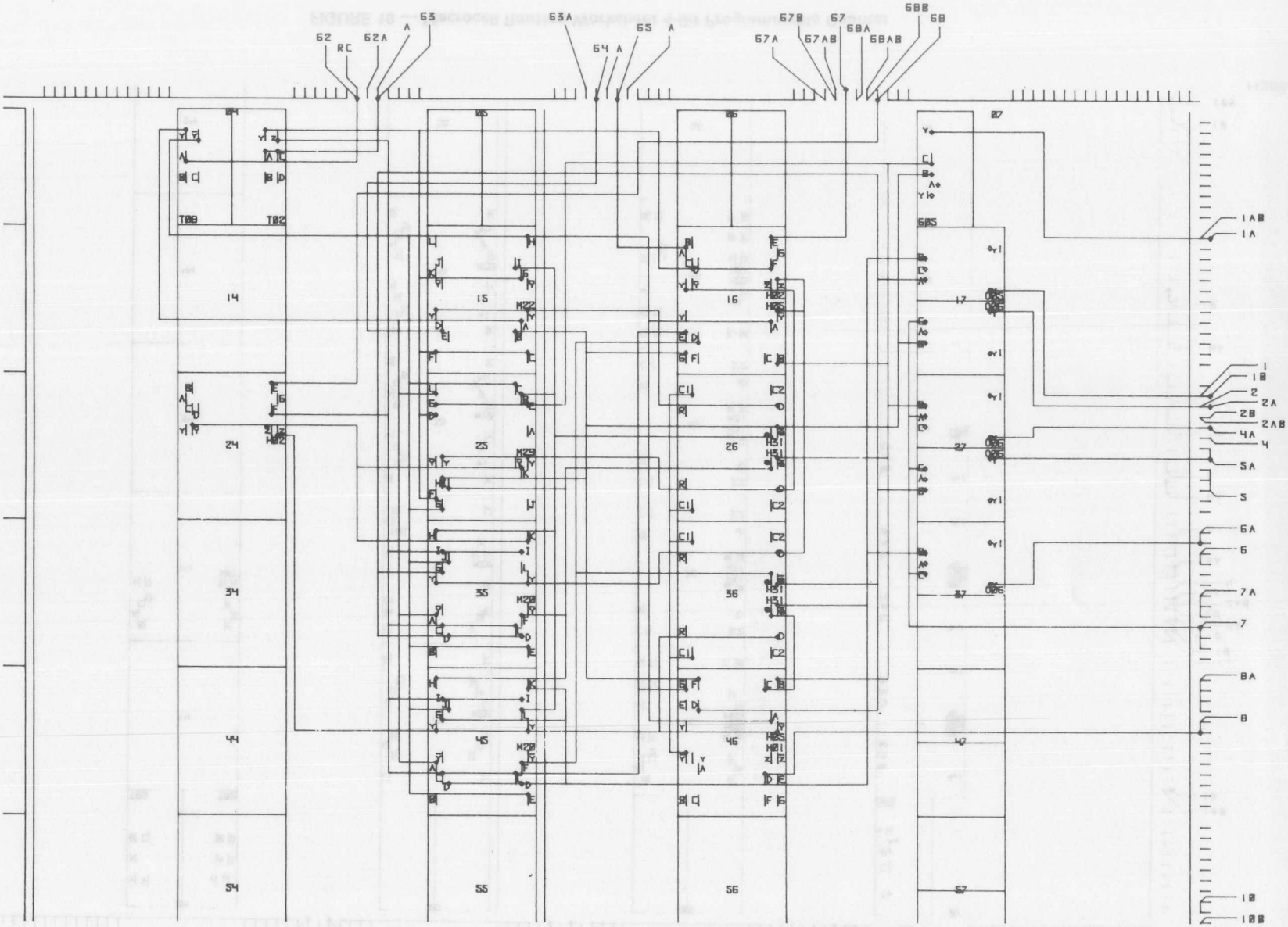


FIGURE 11 — Macrocell Routing Diagram 4-Bit Programmable Counter

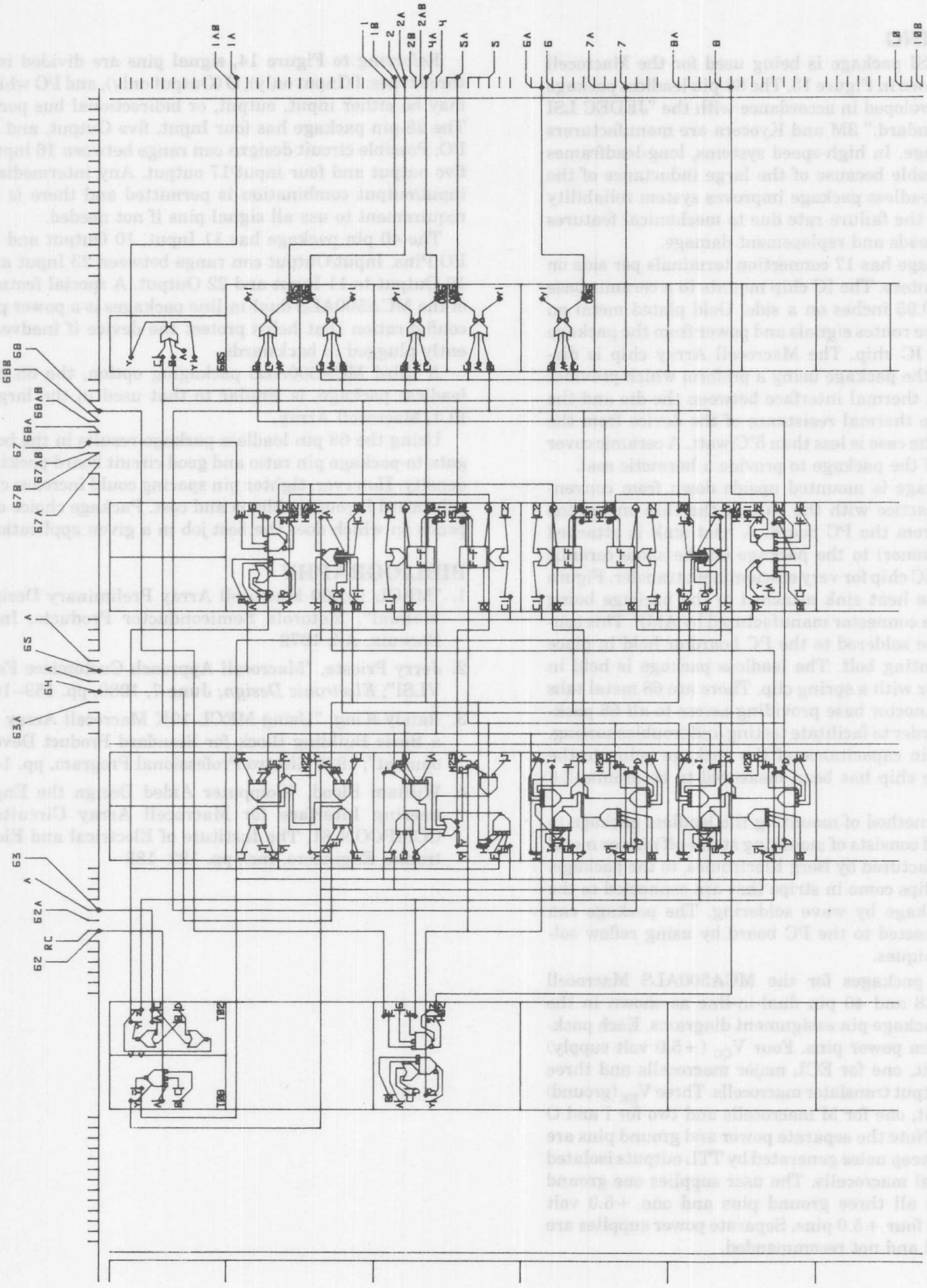


FIGURE 12 — Macrocell Logic Diagram 4-Bit Programmable Counter

PACKAGING

A new LSI package is being used for the Macrocell Array as shown in Figure 13. The 68-pin leadless package has been developed in accordance with the "JEDEC LSI package standard." 3M and Kyocera are manufacturers of the package. In high-speed systems, long-leadframes are not suitable because of the large inductance of the leads. The leadless package improves system reliability by reducing the failure rate due to mechanical features of bending leads and replacement damage.

The package has 17 connection terminals per side on 0.05-inch centers. The IC chip mounts to a ceramic base measuring 0.95 inches on a side. Gold plated metal on the base piece routes signals and power from the package edge to the IC chip. The Macrocell Array chip is die-attached to the package using a preform which provides an excellent thermal interface between the die and the ceramic. The thermal resistance of the device from the junction to the case is less than 5°C/watt. A ceramic cover fits on top of the package to provide a hermetic seal.

The package is mounted upside down from conventional IC practice with the base of the chip on the top side away from the PC board. A heat sink is attached (by the customer) to the package on the same ceramic piece as the IC chip for very efficient heat transfer. Figure 13 shows the heat sink attached to the package being mounted in a connector manufactured by AMP. This connector can be soldered to the PC board or held in place with a mounting bolt. The leadless package is held in the connector with a spring clip. There are 68 metal tabs near the connector base providing access to all 68 package pins in order to facilitate testing and troubleshooting. The input pin capacitance of the package going to the input on the chip has been measured to be around 2.5 pF.

Another method of mounting the leadless package to the PC board consists of mounting stand-off pins or metal clips, manufactured by Berg Electronics, to the package. The metal clips come in strips that are connected to the leadless package by wave soldering. The package can now be connected to the PC board by using reflow soldering techniques.

Primary packages for the MCA500ALS Macrocell Array are 28 and 40 pin dual-in-line as shown in the Figure 14 package pin assignment diagrams. Each package has seven power pins. Four V_{CC} (+5.0 volt supply) pins are split, one for ECL major macrocells and three for Input/Output translator macrocells. Three V_{EE} (ground) pins are split, one for M macrocells and two for I and O macrocells. Note the separate power and ground pins are designed to keep noise generated by TTL outputs isolated from internal macrocells. The user supplies one ground reference to all three ground pins and one +5.0 volt supply to all four +5.0 pins. Separate power supplies are not required and not recommended.

Referring to Figure 14, signal pins are divided into three types; I (Input only), O (Output only), and I/O which may be either input, output, or bidirectional bus ports. The 28-pin package has four Input, five Output, and 12 I/O. Possible circuit designs can range between 16 input/five output and four input/17 output. Any intermediate input/output combination is permitted and there is no requirement to use all signal pins if not needed.

The 40 pin package has 11 Input, 10 Output and 12 I/O Pins. Input/Output can range between 23 Input and 10 Output to 11 Input and 22 Output. A special feature of the MCA500ALS dual-in-line packages is a power pin configuration that helps protect the device if inadvertently plugged in backwards.

A third MCA500ALS packaging option, the 68 pin leadless package, is similar to that used in the larger ECL Macrocell Array.

Using the 68 pin leadless package results in the best gate-to-package pin ratio and good circuit board packing density. However, tighter pin spacing could increase circuit board layout problems and cost. Package choice depends on which does the best job in a given application.

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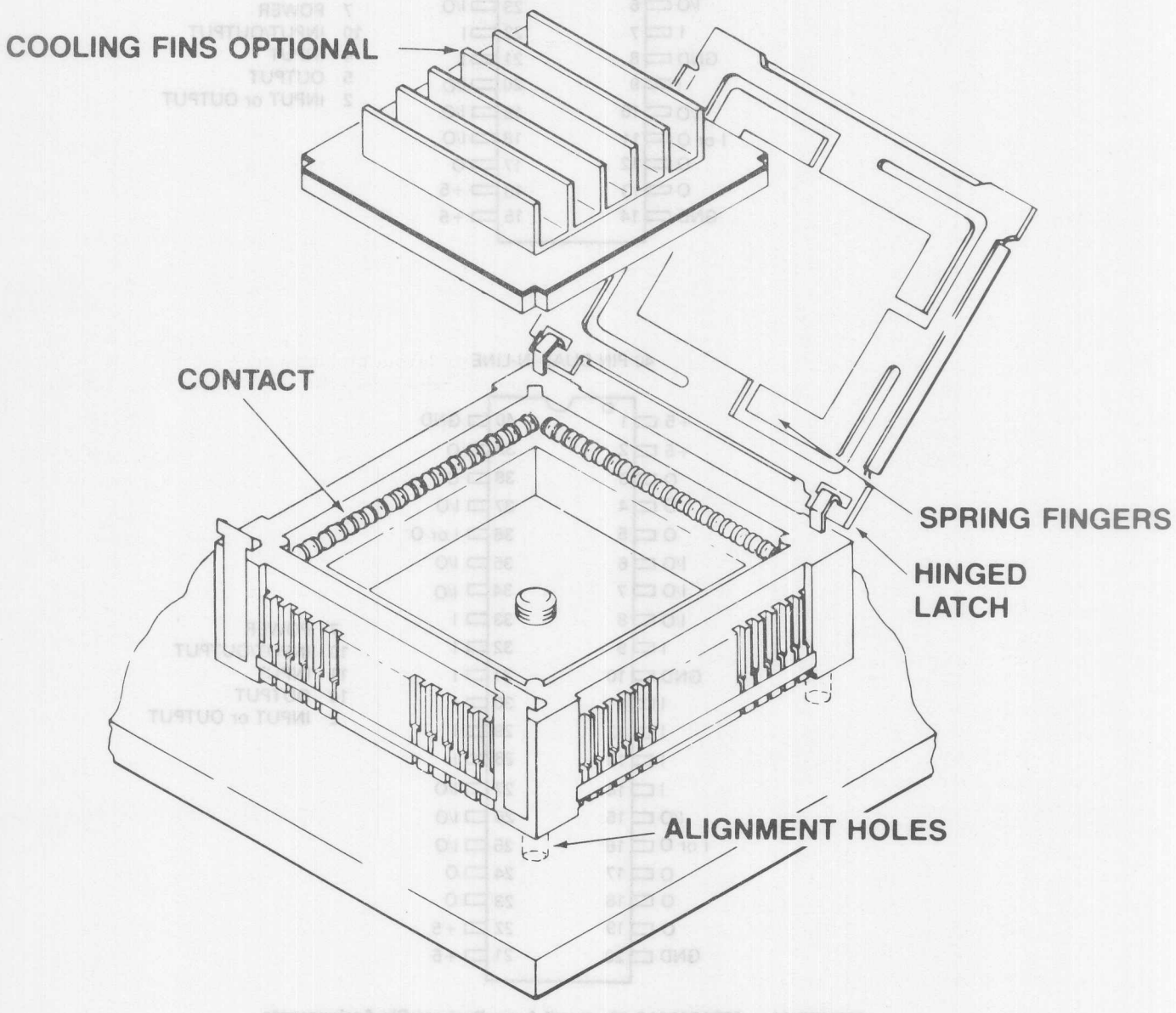
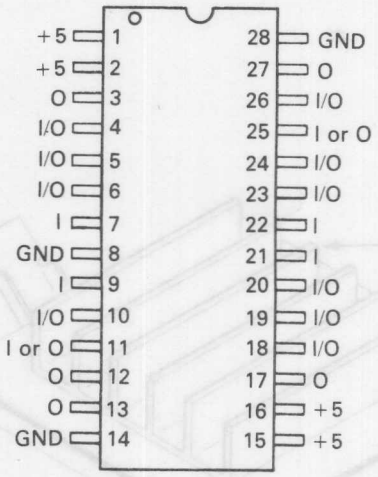


JEDEC Type A
FIGURE 13 — Leadless Package With Connector

28 PIN DUAL-IN-LINE



7 POWER
10 INPUT/OUTPUT
4 INPUT
5 OUTPUT
2 INPUT or OUTPUT

40 PIN DUAL-IN-LINE

7 POWER
10 INPUT/OUTPUT
11 INPUT
10 OUTPUT
2 INPUT or OUTPUT

FIGURE 14 — MCA500ALS Macrocell Array Package Pin Assignments

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