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APPLICATION NOTE

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Page, Nibble, and Static Column Modes: High-Speed, Serial-Access Options on 1M-Bit + DRAMs

The 1M-bit and higher density DRAMs offered by Motorola, in addition to operating in a standard mode at advertised access times, have special operating modes that will significantly decrease access time. These are page, nibble, and static column modes. All three modes are available in the 1M × 1 configuration; page and static column modes are also available on the 256K × 4 configuration. Read, write, and read-write operations can be mixed and performed in any order while these devices are operating in either random or special mode.

The comments that follow refer specifically to successive read operations for page, nibble, and static column modes on the 1M × 1 device. The read operation is chosen for sake of simplicity in illustrating these special operating modes. However, decreased access times will occur for all operations, performed in any order, when the device is operated in any of these modes. General operating comments apply to the 256K × 4 device as well.

All of these special operating modes are useful in applications that require high-speed serial access. Typical examples include video bit map graphics monitors or RAM disks. Page mode is the standard, available since the days of the 16K × 1 DRAM. Static column is the latest mode to be made available on DRAMs, and nibble mode first appeared somewhere in between. Page and static column offer the same column location access, but operate somewhat differently. Nibble is unlike either of the other modes, but faster than both in its niche. All modes are initiated after a standard read or write is performed.

Page and static column modes allow access to any of 1024 column locations on a specific row, while nibble allows access to a maximum of four bits. The location of the first bit in nibble mode determines the other bits to be accessed. Nibble mode allows the fastest access of the three devices (t_{NCAC}), all other parameters held equal, at about 1/4 the standard (t_{RAC}) rate. Page and static column access times (t_{CAC}, t_{AA}) are, respectively, about 1/3 and 1/2 the standard rate.

Cycle time is a better indicator of relative speed improvement, since it measures the minimum time between any two successive reads. Cycle time is approximately 1/4 for nibble and 1/3 for page and static column modes, with respect to a

Table 1. Operating Characteristic Comparison

Parameter		Page	Nibble	Static Column	Random
Access Time (ns)*	t_{CAC}	25	—	—	—
	t_{NCAC}	—	20	—	—
	t_{AA}	—	—	45	—
	t_{RAC}	—	—	—	85
Cycle Time (ns)*	t_{PC}	50	—	—	—
	t_{NC}	—	40	—	—
	t_{SC}	—	—	50	—
	t_{RC}	—	—	—	165
Accessible Bits		1024	4	1024	All
Order of Accessible Bits		Random	Fixed	Random	Random
Conditions	$\overline{RAS}$	Active	Active	Active	Cycle
	$\overline{CAS}$ or $\overline{CS}$**	Cycle	Cycle	Active	Cycle
	Addresses	Cycle	N/A	Cycle	Cycle
	Outputs	Cycle	Cycle	Active	Cycle
Time to Read 4 Bits (ns)*		235	205	235	660
Time to Read 1024 Unique Bits (ns)*		51,235	70,400	51,235	168,960

*Values for a 1M × 1 85-ns device.

**$\overline{CS}$ on Static Column.

Page: 4 bit read = $t_{RAC} + 3t_{PC}$
1024 bit read = $t_{RAC} + 1023t_{PC}$

Nibble: 4 bit read = $t_{RAC} + 3t_{NC}$
1024 bit read = $256 \cdot (t_{RAC} + 3t_{NC} + t_{RP})$

Static Column: 4 bit read = $t_{RAC} + 3t_{SC}$
1024 bit read = $t_{RAC} + 1023t_{SC}$

Random: 4 bit read = $4t_{RC}$
1024 bit read = $1024t_{RC}$

random cycle time of 165 nanoseconds. When operated in these high-speed modes, users will typically access most or all of the bits available to that mode, once the mode has been initiated. Thus the best measure of speed for nibble mode is the rate at which four bits are read, while the rate at which 1024 bits are read is the best measure of page or static column mode. When the actual operating conditions are considered, as described elsewhere, the difference between t_{CAC}, t_{NCAC}, and t_{AA} measurements hold relatively little significance.

Page mode is slightly more difficult to interface in a system than static column mode due to extra $\overline{CAS}$ pulses that are required in page mode. Static column generates less noise than page mode, because output buffers and $\overline{CS}$ are always active in this mode. Noise transients, generated every time $\overline{CAS}$ is cycled from inactive to active, are thus eliminated in the static column mode.

PAGE MODE

Page mode allows faster access to any of the 1024 column locations on a given row, typically at one third the standard (t_{RAC}) rate for randomly-performed operations. Page mode consists of cycling the $\overline{CAS}$ clock from active (low) to inactive (high) and back, and providing a column address, while holding the $\overline{RAS}$ clock active (low). A new column location can be accessed with each $\overline{CAS}$ cycle (t_{PC}).

Page mode is initiated with a standard read or write operation. Row address is latched by the $\overline{RAS}$ clock transition to active, followed by column address and $\overline{CAS}$ clock active. Performing a $\overline{CAS}$ cycle (t_{PC}) and supplying a column address while $\overline{RAS}$ clock remains active constitutes the first page mode cycle. Subsequent page mode cycles can be performed as long as $\overline{RAS}$ clock is active. The first access (data valid) occurs at the standard rate (t_{RAC}). All of the read operations in page mode following the initial operation are measured at the faster rate (t_{CAC}), provided all other timing minimums are maintained (see Figure 1a). Page mode cycle time determines how fast successive bits are read (see Figure 1b).

NIBBLE MODE

Nibble mode allows serial access to two, three, or four bits of data at a much higher rate than random operations (t_{RAC}). Nibble mode consists of cycling the $\overline{CAS}$ clock while holding the $\overline{RAS}$ clock active, like page mode. Internal row and column address counters increment at each $\overline{CAS}$ cycle, thus no external column addresses are required (unlike page or static column modes). After cycling $\overline{CAS}$ three times in nibble mode, the address sequence repeats and the same four bits are accessed again, in serial order, upon subsequent cycles of $\overline{CAS}$:

00, 01, 10, 11, 00, 01, 10, 11, . . .

Nibble mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CAS}$ clock. Performing a $\overline{CAS}$ cycle (t_{NC}) while $\overline{RAS}$ clock remains active constitutes the first nibble mode cycle. Subsequent nibble mode cycles can be performed as long as the $\overline{RAS}$ clock is held active. The first access (data out) occurs at the standard rate (t_{RAC}). All of the read operations in nibble mode following the initial operation are measured at the faster rate (t_{NCAC}), provided all other timing minimums are maintained (see Figure 2a). Nibble mode cycle time determines how fast successive bits are read (see Figure 2b).

STATIC COLUMN MODE

This mode is useful in applications that require less noise than page mode. Output buffers are always on when the device is in this mode and $\overline{CS}$ clock is not cycled, resulting in fewer transients and simpler operation. It allows faster access to any of the 1024 column addresses on a given row, typically at half the standard (t_{RAC}) rate for randomly performed operations. Static column consists of changing column addresses while holding the $\overline{RAS}$ and $\overline{CS}$ clocks active. A new column location can be accessed with each static column cycle (t_{SC}).

Static column mode operation is initiated with a standard read or write cycle. Row address is latched by $\overline{RAS}$ clock transition to active, followed by column addresses and $\overline{CS}$ clock. Performing an address cycle (t_{SC}) while $\overline{RAS}$ and $\overline{CS}$ clocks remain active constitutes the first static column cycle. Subsequent static column cycles can be performed as long as the $\overline{RAS}$ and $\overline{CS}$ clocks are held active. The first access (data out) occurs at the standard (t_{RAC}) rate. All of the read operations in static column following the initial operation are measured at the faster rate (t_{AA}), provided all other timing minimums are maintained (see Figure 3a). Static column cycle time determines how fast successive bits are read (see Figure 3b).

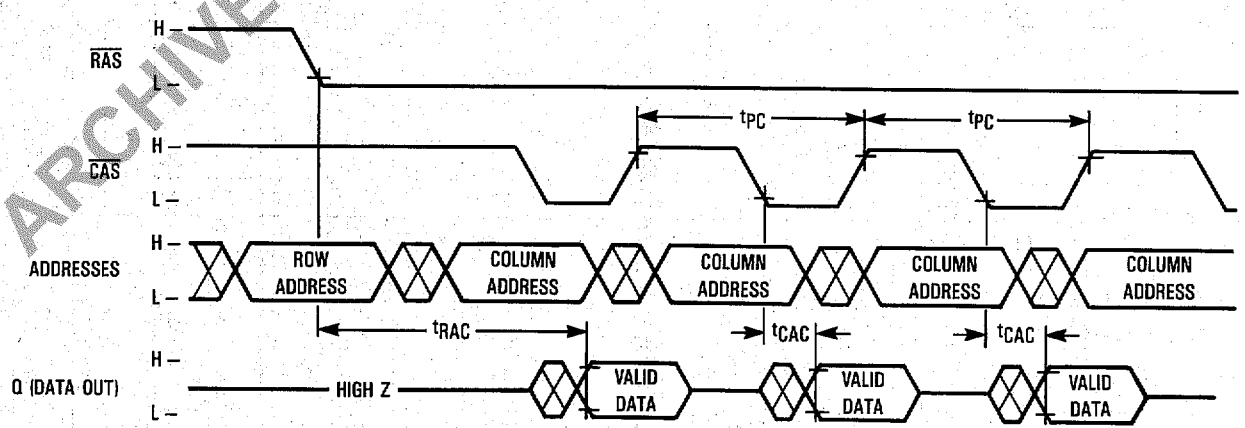

Figure 1a. Page Mode Read Cycle

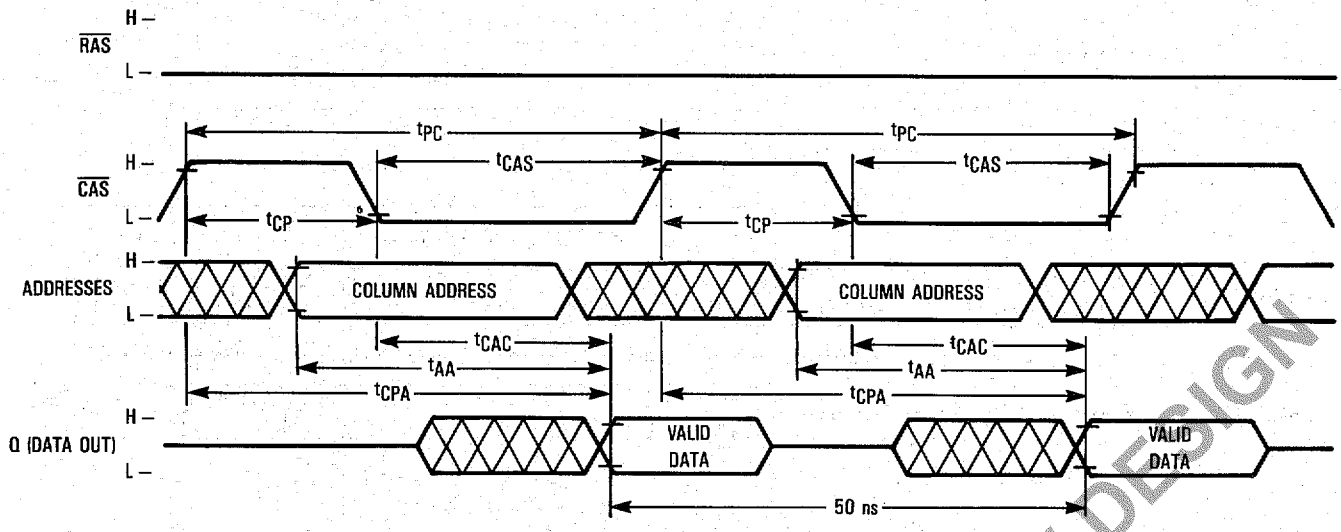

Figure 1b. Page Mode Cycle Minimum Timing

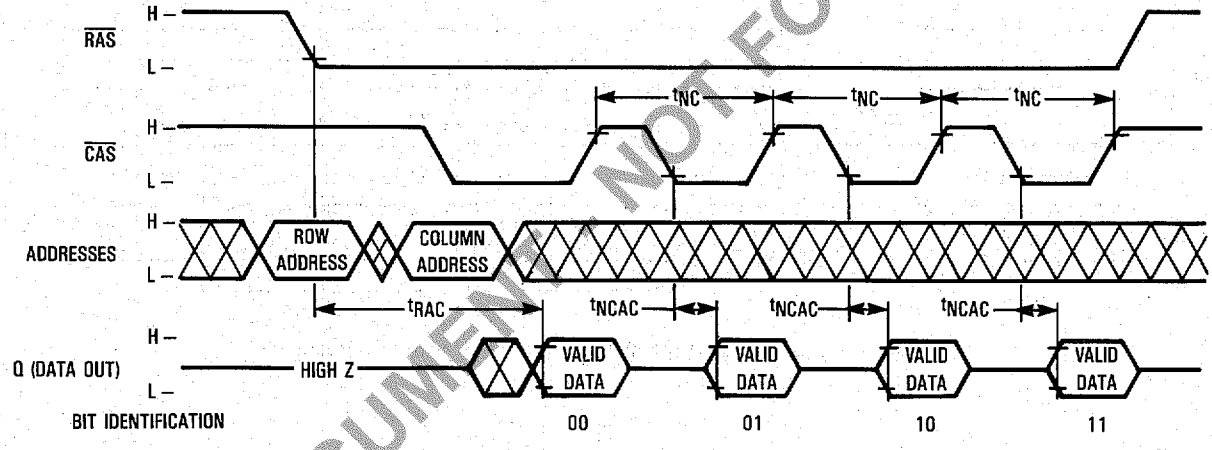

Figure 2a. Nibble Mode Read Cycle

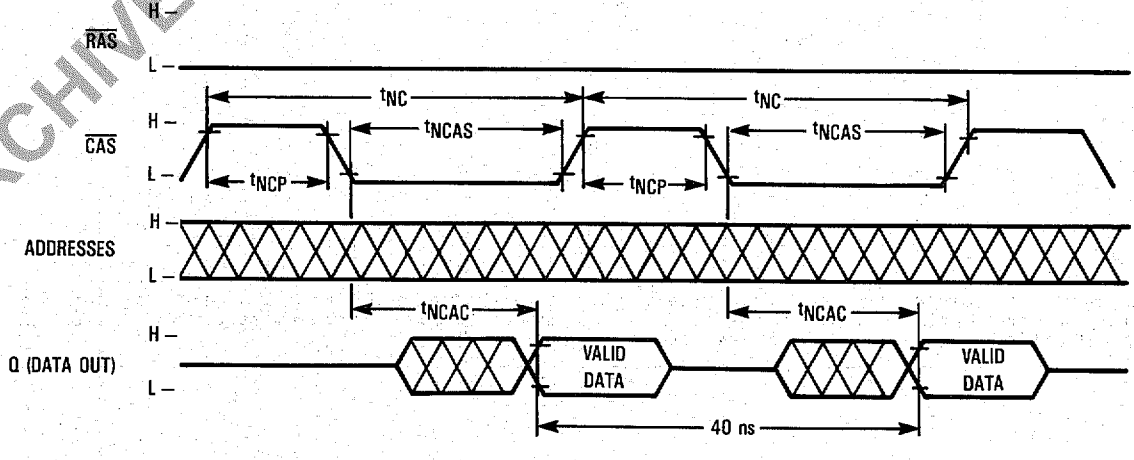

Figure 2b. Nibble Mode Cycle Minimum Timing

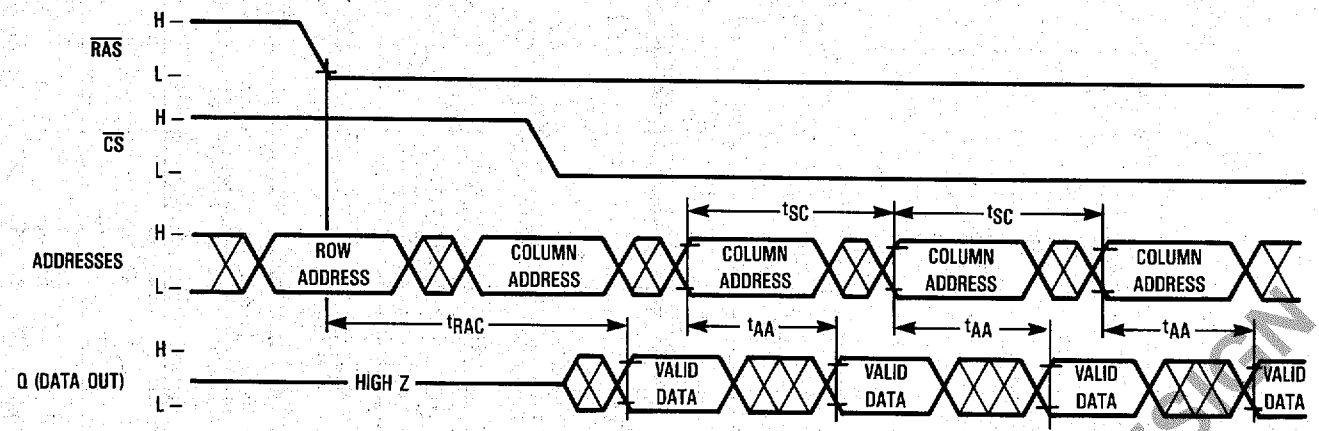

Figure 3a. Static Column Mode Read Cycle

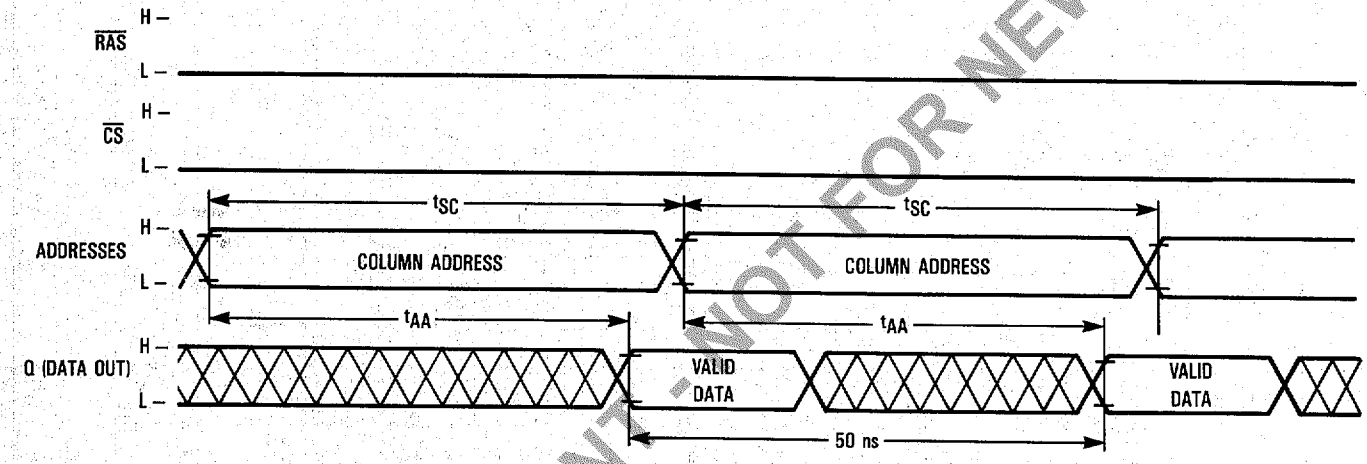

Figure 3b. Static Column Mode Cycle Minimum Timing

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