AR254/D

Phase-Locked Loop Design Articles

- "Analyze, Don't Estimate, Phase-Lock-Loop Performance"
- "Optimize Phase-Lock Loops To Meet Your Needs—Or Determine Why You Can't"
- "Suppress Phase-Lock-Loop Sidebands Without Introducing Instability"
- "Programmable Calculator Computes PLL Noise, Stability"

Analyze, don't estimate, phase-lock-loop

performance of type-2, third-order systems. You can do the job with a programmable-calculator in 48 steps, or less.

Phase-lock loops certainly have many uses, especially in frequency synthesizers, but exact mathematical calculation of their transfer functions is difficult. This is particularly true for type-2, third-order systems (Fig. 1), which don't produce steady-state phase errors for step-position or velocity signal inputs. However, a small programmable calculator, the HP-25, easily—and exactly—determines the complete loop transfer function in 48 steps. In addition, the program data reveals the noise reduction you can expect for the loop's voltage-controlled oscillator (VCO), as well as the loop's stability.

Most other design approaches must resort to second-order loop approximations to simplify calculations; a more exact method manually would take too long.

Unlike a type-1 loop, a type-2 loop has two *true* integrators within the loop—a VCO and an integrator/filter after the phase detector. Replacing the integrator/filter with a passive-RC, low-pass filter results in the more common type-1 response, which doesn't have the phase coherence for step and velocity inputs between the two signal inputs to the phase comparator that the type-2 has.

Moreover, a third-order loop—the order is usually determined by the transfer function of the integrator/filter ($F_{(s)}$)—can reduce VCO noise substantially, without increasing reference-frequency sidebands in the output signal. These sidebands hamper simpler loop-circuit performance.

The transfer function of a generalized phase-lock loop can be represented as follows (Fig. 2):

$$\frac{\theta_o(s)}{\theta_i(s)} = \frac{G_{(s)}}{1 + G_{(s)}H_{(s)}} \qquad (1)$$

where, from Fig. 1

$$G_{(s)} = (K_p)(F_{(s)})(K_v/s) \qquad (2)$$

and

$$H_{(s)} = 1/N. \qquad (3)$$

The phase comparator transfer function is K_p and N is a digital counter/divider factor.

A typical integrator/filter built around an op amp (Fig. 3) has a transfer function determined by the amplifier-circuit's closed-loop gain,

$$A_{CL} = -\frac{Z_f}{Z_1},$$

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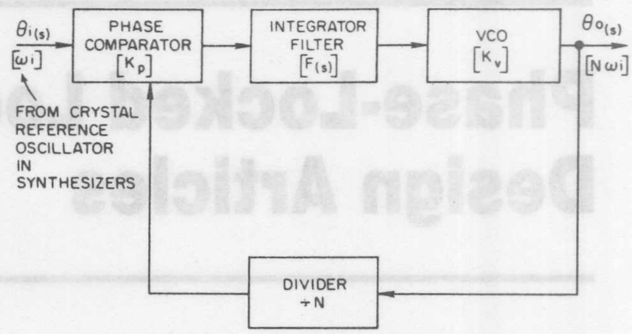
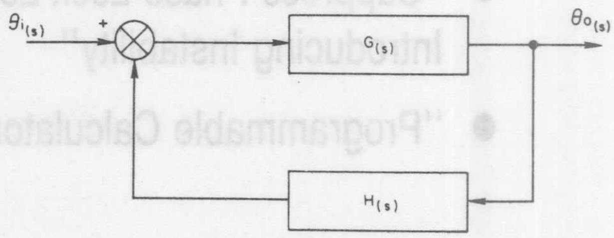
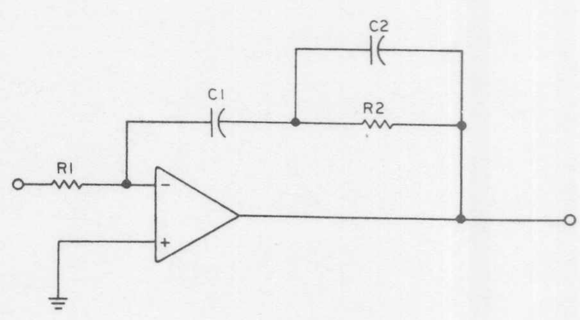


1. **A type-2 phase-lock loop** has two true integrators—the integrator/filter (F_s) and the VCO (K_v). Replacing the integrator/filter with a passive-RC network converts the circuit to a type-1 system.



2. **The phase-lock loop's generalized open-loop transfer function,** $G_{(s)}$ $H_{(s)}$, has a third-order denominator—from which the circuit's name is derived.



3. **An integrator/filter circuit** can be built with a wideband op amp and RC feedback network.

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Table 1. Third order type-2 PLL

Display: Line	Display: Code	Key Entry	Remarks	Registers
00				R_0
01	15 73	(g)π		
02	61	x		
03	02	2		R_1 T_1
04	61	x		
05	23 07	STO 7		
06	24 03	RCL 3		R_2 T_2
07	61	x		
08	01	1		
09	15 09	(g)→P		R_3 T_3
10	23 04	STO 4		
11	22	R↓		
12	24 02	RCL 2		R_4
13	24 07	RCL 7		
14	61	x		
15	32	CHS		R_5 $\frac{K_p K_v}{N}$
16	01	1		
17	32	CHS		
18	15 09	(g)→P		R_6
19	24 04	RCL 4		
20	71	÷		
21	24 05	RCL 5		R_7
22	61	x		
23	24 01	RCL 1		
24	71	÷		
25	24 07	RCL 7		
26	15 02	(g) x^2		
27	71	÷		
28	23 04	STO 4		
29	14 08	(f) log		
30	02	2		
31	00	0		
32	61	x	$G_{j\omega}H_{j\omega}$	
33	74	R/S		
34	22	R↓		
35	21	$x \gtrless y$		
36	41	−	$\angle\theta$	
37	74	R/S		
38	24 04	RCL 4		
39	14 09	(f)→R		
40	01	1		
41	51	+		
42	15 09	(g)→P		
43	15 22	(g)1/x		
44	14 08	(f) log		
45	02	2		
46	00	0		
47	61	x	e/en	
48	13 00	GTO 00		
49				

where $Z_1 = R_1$ (4)

Z_f = impedance of feedback network

The transform of the feedback network is

$$Z_f(s) = \frac{s(C_1+C_2)+\frac{1}{R_2}}{sC_1(sC_2+\frac{1}{R_2})}, \tag{5}$$

and the integrator/filter transfer function is then

$$F_{(s)} = \frac{s(C_1+C_2)+\frac{1}{R_2}}{C_1R_1(sC_2+\frac{1}{R_2})}, \tag{6}$$

Multiply Eq. 6 by R_2/R_2, then

$$F_{(s)} = \frac{s(C_1R_2+C_2R_2)+1}{sC_1R_1(sC_2R_2+1)} \tag{7}$$

or

$$F_{(s)} = \frac{sT_2+1}{sT_1(sT_3+1)}, \tag{8}$$

where

$$T_1 = R_1C_1$$
$$T_2 = R_2(C_1 + C_2)$$
$$T_3 = R_2C_2$$

The open-loop transfer function of Fig. 2 is $G_{(s)}H_{(s)}$; therefore, from Eqs. 2, 3 and 8

$$G_{(s)}H_{(s)} = \frac{s(T_2)(K_vK_p)+K_vK_p}{s^3NT_1T_3 + s^2NT_1} \tag{9}$$

Note the third-order denominator, from which the circuit's name—third-order-loop—is derived. Note also the deletion of the minus sign: the circuit configuration (a phase inverter) provides the negative feedback. Both K_p and K_v are positive.

If you substitute $j\omega$ for s in Eq. 9, you can get the equation for plotting the magnitude and phase of the circuit's open-loop gain as a function of frequency:

$$G_{(j\omega)}H_{(j\omega)} = -\frac{j\omega(T_2)\ (K_vK_p)\ +\ K_vK_p}{j\omega^3NT_1T_3\ +\ \omega^2NT_1} \tag{10}$$

Step	Instructions	Input Data/ Units	Keys			Output Data/ Units
1	Enter program					
2	Store T_1	R_1	ENTER			
		C_1	X	STO	1	
	T_2	C_1	ENTER			
		C_2	+			
		R_2	X	STO	2	
	T_3	R_2	ENTER			
		C_2	X	STO	3	
	$(K_p K_v)/N$	K_p	ENTER			
		K_v	X			
		N	÷	STO	5	
3	Calculate	F	(f)	PRGM	R/S	$G_{j\omega}H_{j\omega}$
			R/S			$\angle\theta$
			R/S			(e/en)
4	Repeat step 3 for other values of frequency, F					

Table 2. Calculated loop response

Frequency Hz	Open-loop response dB	Open-loop response $\angle\theta$	Loop response to VCO noise dB
100	116.01	−179.94	−116.01
1000	76.01	−179.44	−76.01
10,000	36.06	−174.44	−35.92
94,650	0*	−139.85	3.27
100,000	−0.71	−138.58	3.30**
1,000,000	−26.25	−139.59	0.32
10,000,000	−63.21	−174.68	0.01

*Unity-gain point **Maximum overshoot

A servo-loop damping factor that appears in lower-order loops is not defined in third-order loops. Instead you determine stability by the phase margin between −180° and the phase at a frequency where the gain is unity in the open-loop gain function, $G_{j\omega}H_{j\omega}$. The larger the phase margin, the more stable the system. A phase margin of about 45° produces an adequately damped loop. More than 45° means greater stability and, of course, the system may oscillate when the margin approaches zero.

Feedback also reduces noise

Not only does feedback determine the system's stability, but it also delineates its noise-output characteristics. When running free, the VCO is considerably more "noisy" than is the circuit's reference crystal oscillator. But the circuit's feedback loop substantially reduces the VCO's output-noise spectrum, especially, at low frequencies. This particular reduction is fortunate, because the VCO's noise output has 1/f characteristics: high-frequency noise tends to fall off without outside help, but the low frequency needs the help.

An approximate expression for the loop's output phase noise is

$$\sqrt{[(|e/e_n|)(e_v)]^2 + [(N)(e_x)]^2}, \tag{11}$$

where e_x = crystal-oscillator noise.
e_v = VCO noise.
(e/e_n) = loop's response to VCO noise.

And the loop's response to the VCO noise is

$$(e/e_n) = \frac{1}{1 + G_{(s)}H_{(s)}} \tag{12}$$

Although $G_{(s)}H_{(s)}$ determined from Eq. 9 is complex, only the magnitude of (e/e_n) from Eq. 12 is used in Eq. 11. Note: The greater the open-loop transfer function, $G_{(s)}H_{(s)}$, the smaller the (e/e_n), and the lower the loop's output noise. However, note also that the reference crystal oscillator's noise contribution is multiplied by the divider constant, N, though, hopefully, the crystal-oscillator noise is low.

In addition, you can get a check on the system's stability by plotting the loop's response to VCO noise (e/e_n), obtained from Eq. 12, versus frequency. You'll find that the curve has a high-pass response with a 12-dB/octave slope. For best stability, any overshoot at the cutoff frequency should be less than 6 dB. Of course, lower overshoot represents higher stability.

Clearly, the loop's mathematical analysis depends mainly upon calculation of $G_{(j\omega)}H_{(j\omega)}$ in Eq. 10.

Now comes the program

To make the calculator program simpler, rewrite Eq. 10 as follows:

$$G_{(j\omega)}H_{(j\omega)} = \frac{K_vK_p}{NT_1\omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right] \tag{13}$$

Table 1 contains the program that solves Eq. 13. It provides both the magnitude and phase angle, $\angle\theta$, of the open-loop response, $G_{(j\omega)}H_{(j\omega)}$, given T_1, T_2, T_3, K_pK_v/N and frequency, $f(\omega = 2\pi f)$. The open-loop response magnitude is given in dB and its phase in degrees. Also, the magnitude of the loop's VCO noise response (Eq. 12) is given in dB. If answers in dB aren't required, however, seven steps can be eliminated.

To see how the program works, consider a 960-MHz transmitter recently proposed for a Navy application. It calls for a phase-lock loop with the following characteristics to generate the 960 MHz:

$$\begin{aligned} N &= 64 \\ R_1 &= 10{,}000\ \Omega \\ C_1 &= 4700 \times 10^{-12}\ \text{F} \\ R_2 &= 330\ \Omega \\ C_2 &= 470 \times 10^{-12}\ \text{F} \\ K_p &= 0.25\ \text{V/rad} \\ K_v &= 3 \times 10^9\ \text{(rad/s)/V} \end{aligned}$$

The stable crystal-oscillator reference frequency used is 15 MHz. The frequency divider and phase comparator are built with ECL logic. From the circuit component values and transfer constants we obtain:

$$\begin{aligned} T_1 &= 4.7 \times 10^{-5}\ \text{s} \\ T_2 &= 1.706 \times 10^{-6}\ \text{s} \\ T_3 &= 1.551 \times 10^{-7}\ \text{s} \\ (K_vK_p)/N &= 11.72 \times 10^6/\text{s} \end{aligned}$$

The calculator program provided the results in Table 2. Note that the phase margin at unity gain corresponding to 94,650 Hz is 40.15°; thus the loop is fairly stable. Further, the loop's response to VCO noise shows a maximum overshoot of 3.30 dB at 100,000 Hz, which confirms the loop's stability (less than 6-dB overshoot). If the phase margin is too small or you want overdamped loop operation, the program allows you to check the effects of parameter changes and get the performance you want, quickly. However, keep all additional circuit poles above the area of interest, since they reduce phase margin and stability. In addition, don't ignore the effects of stray capacitances. And use a high-gain op amp with a wide frequency response and a VCO with a wide modulation bandwidth. ■■

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Optimize phase-lock loops to meet your needs—or determine why you can't

The time constants of a PLL's integrator/filter are the keys to controlling a loop's performance. In the integrator/filter, you can trade off circuit parameters most easily to meet your needs. The other loop components (Fig. 1) have simple, real-valued transfer functions (K_v, K_p, N) that can't be changed as easily. But the integrator/filter's transfer function (F_s), detailed in Fig. 1c is the source of the high-order complex function in the following equation for open-loop gain:

$$G(j\omega)\,H(j\omega) = \frac{K_v K_p}{N T_1 \omega^2}\left[\frac{-j\omega T_2 - 1}{j\omega T_3 + 1}\right], \quad (1)$$

where

T_1, T_2, T_3 = time constants defined in Fig. 1c, seconds

K_p = phase-detector gain constant, volts/radian

K_v = voltage-controlled-oscillator (VCO) sensitivity, radians/second/volt

N = frequency devisor

$\omega = (2\pi f)$ frequency, radians

Usually, K_p, K_v and N are given, but you can choose T_1, T_2 and T_3 to give you the loop performance you want. Generally, of course, you want the loop to be stable, to attenuate the reference frequency and to reduce VCO noise. But stability, being an absolute necessity, gets priority. The other two requirements, unfortunately, are inversely dependent and must be traded off against each other.

A damping factor to control stability as in simpler second-order loops can't be readily defined in the third-order loop of Fig. 1. Instead, the phase margin

In ED No. 10, May 10, 1978, p. 120, A. B. Przedpelski advised: "Analyze, don't estimate, phase-lock-loop performance." He showed how to calculate the performance of a given type-2, third-order PLL system with a 48-step program for an HP-25 programmable calculator. This article will show you how to optimize such a PLL to your requirements. But you will discover that you may not be able to get all requirements simultaneously. Compromises may be necessary.

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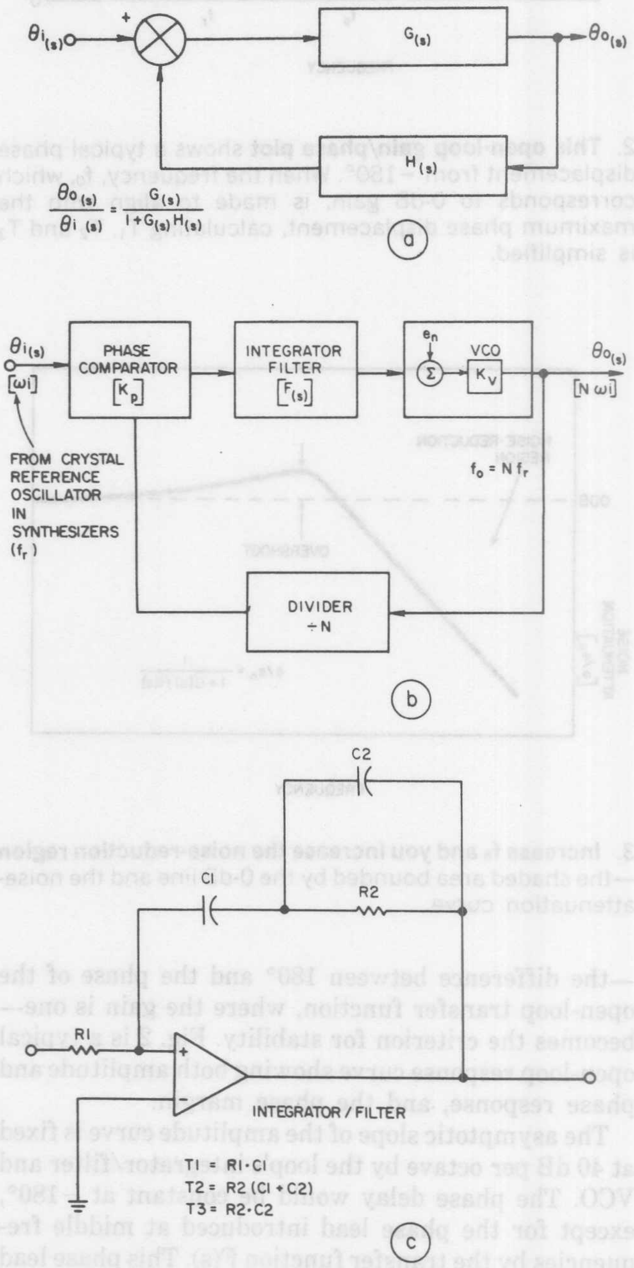

1. **A phase-lock loop** (a) with two integrators (b) is classified type 2. And the order—third, in this case—is established by the characteristics of the integrator/filter (c). Time constants T_1, T_2 and T_3 determine the integrator/filter's detailed performance.

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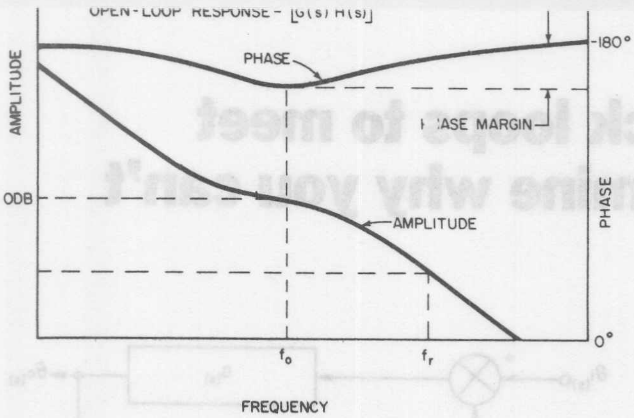
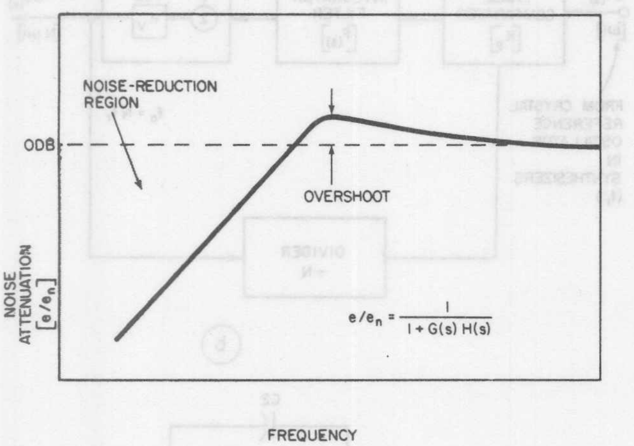


2. **This open-loop gain/phase plot** shows a typical phase displacement from −180°. When the frequency, f_0, which corresponds to 0-dB gain, is made to align with the maximum phase displacement, calculating T_1, T_2 and T_3 is simplified.



3. **Increase f_0 and you increase the noise-reduction region**—the shaded area bounded by the 0-dB line and the noise-attenuation curve.

—the difference between 180° and the phase of the open-loop transfer function, where the gain is one—becomes the criterion for stability. Fig. 2 is a typical open-loop response curve showing both amplitude and phase response, and the phase margin.

The asymptotic slope of the amplitude curve is fixed at 40 dB per octave by the loop's integrator/filter and VCO. The phase delay would be constant at −180°, except for the phase lead introduced at middle frequencies by the transfer function F(s). This phase lead provides the phase margin that ensures loop stability.

45°—a good compromise

The phase margin should be between 30° and 70° for most applications. The larger the phase margin, the more stable the loop. But a large phase margin pression capability. Thus, a phase margin of about 45° is a good compromise between desired stability and the other generally undesired effects.

Ideally, a phase comparator provides an error signal that is proportional to the phase difference between its two inputs, and nothing else. But in practice, some of the reference frequency, f_r, always leak through the comparator, which frequency modulates the output signal to produce undesirable sideband frequencies. Shifting the open-loop gain-amplitude curve of G (jω) H (jω) Fig. 2 to the left would attenuate f_r and the sidebands. But such a shift also would weaken the circuit's VCO-noise suppression capability.

A typical VCO noise-reduction plot is shown in Fig. 3. Noise attenuates in the region that lies to the left of the curve and below the 0-dB line (shown cross-hatched). The unity-gain frequency, f_0, defines the noise reduction: It's directly proportional to f_0. Clearly, then, shifting the G (jω) H (jω) curve to the right by increasing f_0 will also increase the VCO noise-reduction region—which is opposite the requirement for reducing the sidebands. Thus, as so often happens, you must compromise. Locate the point of minimum phase shift (inflection point of the phase response, Fig. 2) exactly at f_0, the unity-gain value.

The inflection point is strategic

Locating f_0 at the phase inflection point is strategically valuable, because it will help solve for the value of T_1. But first you must determine T_3. Accordingly, from Eq. 1 the phase margin, ϕ, is

$$\phi = \tan^{-1}\omega\, T_2 - \tan^{-1}\omega\, T_3 + 180°. \qquad (2)$$

Differentiate ϕ with respect to ω and set the result equal to zero to locate ω_0, and the result is

$$\frac{d\phi}{d\omega} = \frac{T_2}{1 + (\omega T_2)^2} - \frac{T_3}{1 + (\omega\, T_3)^2} = 0 \qquad (3)$$

Solving Eq. 3 then gives you

$$\omega_0 = \frac{1}{\sqrt{T_2\, T_3}}\,. \qquad (4)$$

And substituting Eq. 4 into Eq. 2 gives you

$$\tan\phi = \frac{T_2 - T_3}{2\sqrt{T_2 T_3}} \qquad (5)$$

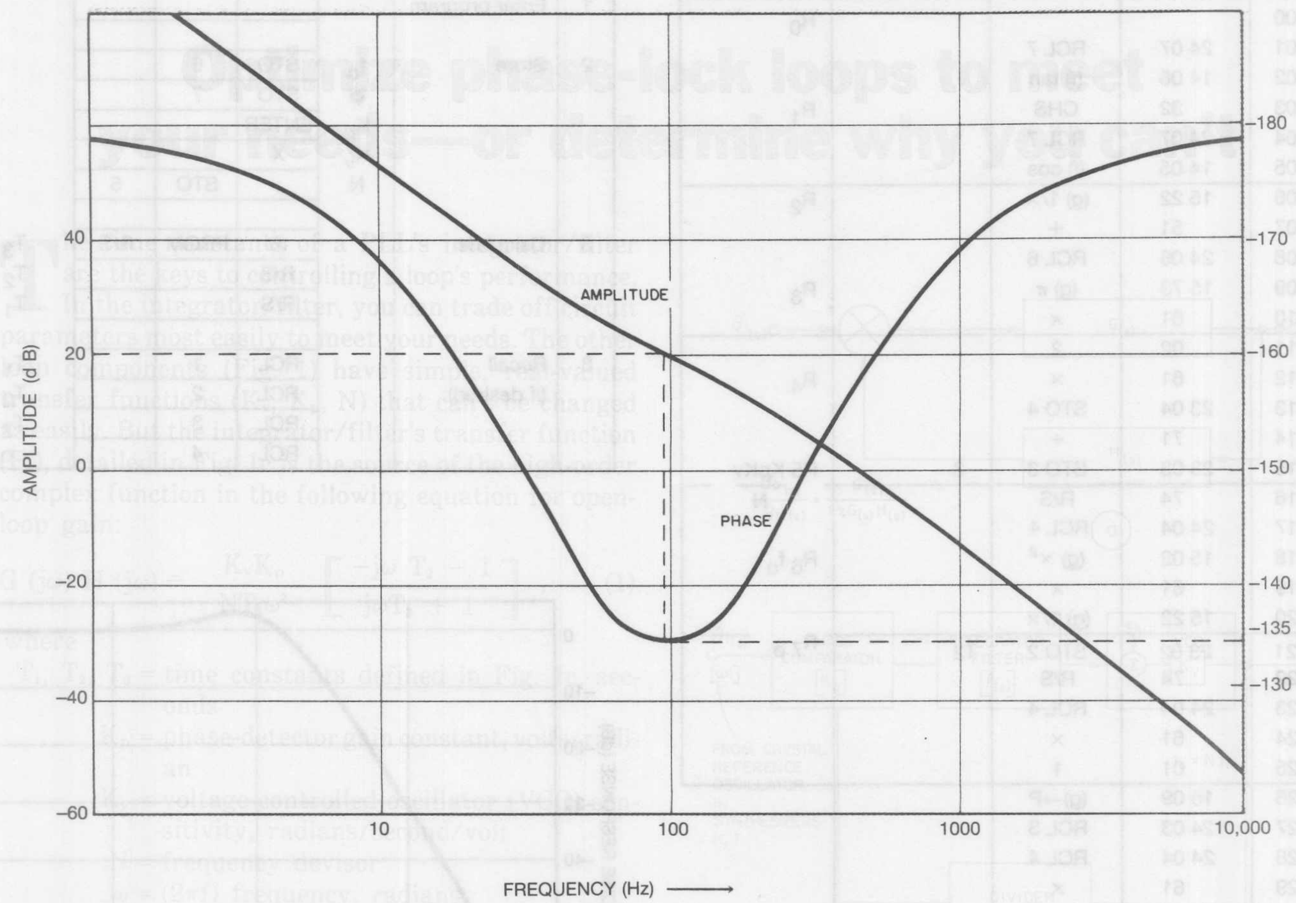
Finally, plug Eq. 4 into Eq. 5 and re-arrange to get

$$T_3 = \frac{\sec\phi - \tan\phi}{\omega_0} \qquad (6)$$

Then re-arrange Eq. 5 to get

$$T_2 = \frac{1}{\omega_0{}^2 T_3} \qquad (7)$$

Since you want the gain to be one at the phase-



4. **This plot of a PLL's open-loop transfer function** confirms the design-parameter choices—a 45° phase margin at an f_0 of 100 Hz and unity gain. The loop is stable, but some adjustments may be desirable.

inflection point, solve for T_1 in Eq. 1 with $G(j\omega)\,H(j\omega) = 1$; as result,

$$T_1 = \frac{K_p K_v}{N\omega^2}\left[\frac{j\omega\ T_2 + 1}{j\omega\ T_3 + 1}\right] \qquad (8)$$

The 41 steps

The program in the table solves Eqs. 6, 7 and 8 in 41 steps with an HP-25 programmable calculator. Of course, the program can be adapted to other programmable calculators.

To illustrate the program's procedure, consider a PLL that must produce an output of 16.95 MHz from a 5-kHz reference, f_r. The phase comparator, VCO and divider transfer functions are as follows:

$$K_p = 0.19 \text{ V/rad}$$
$$K_v = 10.6 \times 10^6 \text{ rad/s/V}$$
$$N = 3390$$

For stability, start with a phase margin of 45° and an f_0 of about 1/50 of f_r. Thus, with

$$\phi = 45°$$

and

$$f_0 = 5000/50$$
$$= 100 \text{ Hz},$$

calculate T_1, T_2 and T_3 with the program: You get

$$T_1 = 3.63 \times 10^{-3}\text{s}$$
$$T_2 = 3.84 \times 10^{-3}\text{s}$$
$$T_3 = 6.59 \times 10^{-4}\text{s}$$

But with those time constants you would need components with nonstandard values. However, if you select standard capacitors and resistors as follows:

$C_1 = 0.33\ \mu\text{F}$, $R_1 = 12\ \text{k}\Omega$,
$C_2 = 0.068\ \mu\text{F}$, $R_2 = 10\ \text{k}\Omega$,

you get the following time constants:

$$T_1 = 3.96 \times 10^{-3}\text{s}$$
$$T_2 = 3.98 \times 10^{-3}\text{s}$$
$$T_3 = 6.8 \times 10^{-4}\text{s}$$

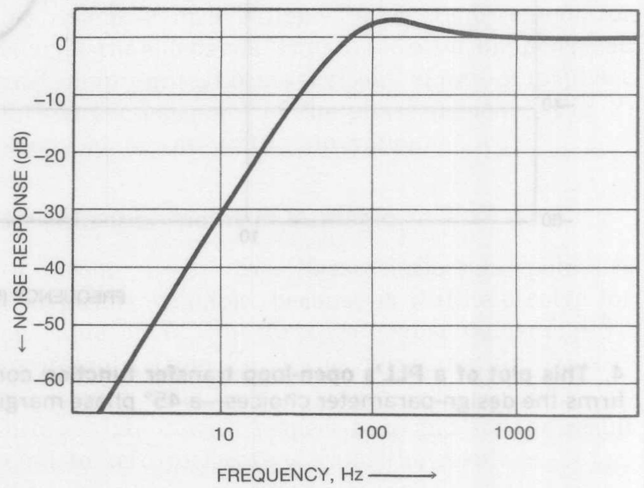
which are close enough for a first try.

Verifying the results

To verify the results, the open-loop transfer function, $G(j\omega)\,H(j\omega)$, and noise response, e/e_n, were calculated with the program provided in the previous

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0
01	24 07	RCL 7		
02	14 06	(f) tan		
03	32	CHS		R_1
04	24 07	RCL 7		
05	14 05	(f) cos		
06	15 22	(g) 1/×		R_2
07	51	+		
08	24 06	RCL 6		
09	15 73	(g) π		R_3
10	61	×		
11	02	2		
12	61	×		R_4
13	23 04	STO 4		
14	71	÷		
15	23 03	STO 3	3	R5 $\frac{K_pK_v}{N}$
16	74	R/S		
17	24 04	RCL 4		
18	15 02	(g) $\times^2$		R_6 f_o
19	61	×		
20	15 22	(g) 1/×		
21	23 02	STO 2	T2	R_7 ø
22	74	R/S		
23	24 04	RCL 4		
24	61	×		
25	01	1		
26	15 09	(g)→P		
27	24 03	RCL 3		
28	24 04	RCL 4		
29	61	×		
30	01	1		
31	15 09	(g)→P		
32	21	x ≷ y		
33	22	R↓		
34	71	÷		
35	24 04	RCL 4		
36	15 02	(g) $\times^2$		
37	71	÷		
38	24 05	RCL 5		
39	61	×		
40	23 01	STO 1	T_1	
41	13 00	GTO 00		

Step	Instructions	Input Data/Units	Keys			Output Data/Units
1	Enter program					
2	Store	f_o	STO	6		
		ϕ	STO	7		
		K_p	ENTER			
		K_v	X			
		N	:	STO	5	
3	Calculate		(f)	PRGM	R/S	T_3
			R/S			T_2
			R/S			T_1
3	Recall (if desired)		RCL	1		T_1
			RCL	2		T_2
			RCL	3		T_3
			RCL	4		o



5. **The noise-response calculation** corresponding to Fig. 4 shows that VCO noise is attenuated below about 70 Hz.

article and plotted in Figs. 4 and 5. The curves confirm that the design is stable with a maximum phase margin of 45° at a frequency where the open-loop gain is about unity. And the VCO noise-reduction curve shows a moderate 3.2-dB overshoot with noise frequencies below about 70 Hz in the attenuation region.

Still, adjustments may be desired. For instance, if you want more reference-frequency (f_r) attenuation, the G (jω) H (jω) curve can be shifted to the left. Move f_o one decade (to about 10 Hz) and you'll increase the f_r attenuation by 40 dB. Or, if noise frequencies above 70 Hz are bothersome, you can shift the G (jω) H (jω) curve to the right by increasing f_o.

If you still aren't satisfied, you can change the phase margin. Reduce the margin and you improve both f_r and VCO-noise attenuation—but then you lose some stability.■■

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Suppress phase-lock-loop sidebands without introducing instability

Phase-lock loops: Part Three

The first two parts of this series showed how to analyze and then optimize type-2, third-order PLL systems and provided simple calculator programs for an HP-25 to do the otherwise tedious computations.[1,2] *This article takes you a step further and shows how to suppress sidebands, especially undesired when the PLL is used in frequency-synthesis systems.*

Frequency synthesis, a major application of the phase-lock loop (PLL), always involves PLL-performance compromise: keeping loop bandwidth as wide as possible to reduce acquisition time and voltage-controlled oscillator noise, and at the same time suppressing reference-frequency sidebands that can pass through wide bandwidths (Fig. 1).

Fortunately, the reference frequency is considerably above the required loop bandwidth in most cases, which alleviates the sideband problem to some extent. But for heavy suppression of undesired sidebands, extra filtering is necessary. However, it must be done carefully so as not to introduce loop instability. Three filtering circuits, none of which reduce bandwidth or VCO-noise attenuation can help solve the problem. In fact, an active LP-filtering technique, the most versatile and efficient of the three, is programmed on an HP-25 to speed the design.

All methods assume that the PLL, a type-2 third-order loop,[1] meets all requirements[2] except adequate reference-frequency sideband suppression. The three approaches include RC, active-notch and active-LP filtering. The PPL's phase margin serves as a measure of loop stability, since the damping-factor concept isn't applicable to third-order loops:[2] phase margins between 30° and 45° are minimum criteria for stable operation. And the filter's action in reducing the feedforward gain, $G(j\omega)$, at the sideband frequencies is the criterion for the suppression effectiveness.

Since $H(j\omega)$ is equal to $1/N$, a constant, then the open-loop gain, $G(j\omega)H(j\omega)$ in Eq. 1, can be used as a measure of this sideband-suppression effectiveness:

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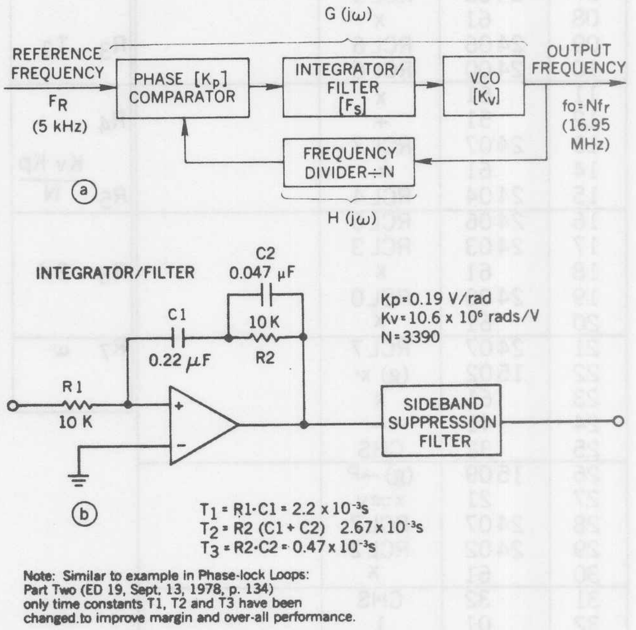

1. **A phase-lock-loop frequency synthesizer** (a) generates 16.95 MHz from a crystal-oscillator reference frequency of 5 kHz. To help suppress sidebands, a sideband-suppression filter is added in tandem with the output of the loop's original integrator/filter circuit (b).

Table 1. Filter suppression/phase margin tradeoffs

Circuit	Phase margin	Phase margin deterioration	First-sideband reduction	Second-sideband reduction
Original	44°	—	—	—
RC low-pass RC = 3 x 10^{-4}	32	12°	20 dB	26 dB
Notch filter				
Q = 10	44	0	∞*	0
Q = 1	43	1	∞*	1.5
Q = 0.1	31	13	∞*	16.5
Second-order active				
d = 0.707	34	10	28	40
d = 0.1	42	2	28	40

*Theoretical—actual value about 40 dB.

$$G(j\omega)H(j\omega) = \frac{K_v\ K_p}{NT_1\omega^2}\left[\frac{j\omega T_2\ +1}{j\omega T_3\ +1}\right], \quad (1)$$

K_p = gain constant of the phase detector,
K_v = VCO sensitivity,

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Table 2. Third-order PLL with two-pole low-pass filter

Display Line	Display Code	Key Entry	Remarks	Registers
00				R_0 ω_o
01	24 00	RCL 0		
02	15 02	(g) x^2		
03	24 07	RCL 7		R_1 T_1
04	15 02	(g) x^2		
05	41	—		
06	23 04	STO 4		R_2 T_2
07	24 03	RCL 3		
08	61	x		
09	24 06	RCL 6		R_3 T_3
10	24 00	RCL 0		
11	61	x		
12	51	+		R_4
13	24 07	RCL 7		
14	61	x		
15	24 04	RCL 4		R_5 $\frac{K_v K_p}{N}$
16	24 06	RCL 6		
17	24 03	RCL 3		
18	61	x		R_6 2d
19	24 00	RCL 0		
20	61	x		
21	24 07	RCL 7		R_7 ω
22	15 02	(g) x^2		
23	61	x		
24	41	—		
25	32	CHS		
26	15 09	(g) →P		
27	21	x⇌y		
28	24 07	RCL 7		
29	24 02	RCL 2		
30	61	x		
31	32	CHS		
32	01	1		
33	32	CHS		
34	15 09	(g) →P		
35	22	R↓		
36	51	+	∠ Phase margin	
37	74	R/S		
38	22	R↓		
39	71	÷		
40	24 05	RCL 5		
41	61	x		
42	24 01	RCL 1		
43	71	÷		
44	24 07	RCL 7		
45	15 02	(g) x^2		
46	71	÷		
47	24 00	RCL 0		
48	15 02	(g) x^2		
49	61	x	$\lvert G_S H_S \rvert$	

Step	Instructions	Input Data/Units	Keys			Output Data/Units
1	Enter program					
2	Store	ω_o	STO	0		
		T_1	STO	1		
		T_2	STO	2		
		T_3	STO	3		
		K_v	ENTER			
		K_p	x			
		N	÷	STO	5	
		d	ENTER	2	x	
			STO	6		
3	Enter	ω	STO	7		
4	Calculate		(f)	PRGM	R/S	∠Phase margin
			R/S			$\lvert G(s)\,H(s)\rvert$
5	Repeat steps 3 and 4 for other values of frequency, ω					

N = counter divide ratio,

T_1, T_2, T_3 = integrator/filter time constants.

Simple but limited

The simplest approach adds in series with the Integrator/Filter an RC low-pass section (Fig. 2a), whose cutoff frequency is larger than the upper end of the loop's bandwidth. For illustration, let the value of RC be 3×10^{-4} s for the frequency-synthesizer example outlined in Fig. 1. (A larger value would reduce sidebands more, but would also decrease the phase margin too much.) With a value of 3×10^{-4} s, the phase margin remains within a "safe" 30°-to-45°.

The open-loop transfer function then becomes:

$$G(j\omega)H(j\omega) = \frac{K_vK_p}{NT_1\omega^2}\left[\frac{-j\omega T_2-1}{j\omega(T_3+T_4)+1+\omega^2T_3T_4}\right], \quad (2)$$

where T_4 is the additional RC time constant.

Solving Eq. 1 at frequencies of 5 and 10 kHz shows that the first sideband (at 5 kHz) is reduced a respectable 20 dB and the second sideband (at 10 kHz) even more to 26 dB. But the phase margin also is reduced to a marginal 32° (Table 1).

However, an active RC notch filter[3] (Fig. 2) gives much more attenuation at the first sideband (5 kHz) and is more flexible in some applications. Its gain is

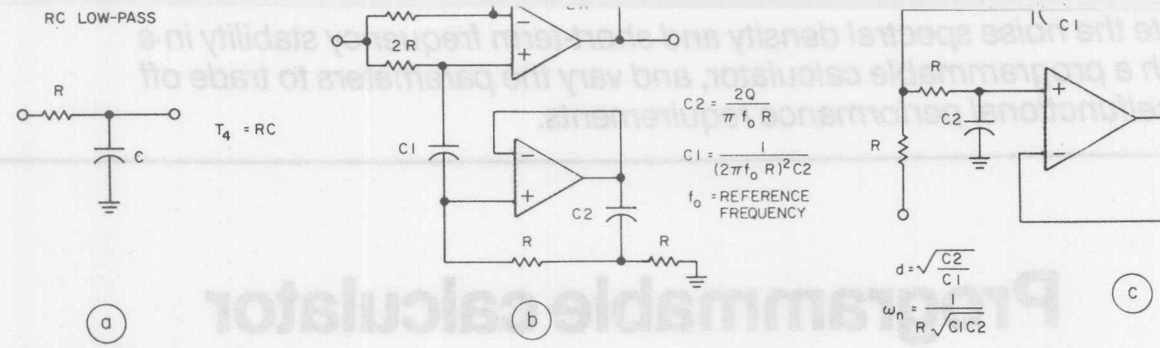
$$A(j\omega) = \frac{1}{j\omega\left[\frac{\omega_o}{Q(\omega^2-\omega_o^2)}\right]+1}, \quad (3)$$

where ω_o = the notch frequency ($2\pi f_o$), Q = the circuit Q.

The open-loop transfer function, the product of Eqs. 1 and 3, is

$$G(j\omega)H(j\omega) = \frac{K_vK_p}{NT_1\omega^2} \times \left[\frac{-j\omega T_2-1}{j\omega\left(T_3-\frac{\omega_o}{Q(\omega^2-\omega_o^2)}\right)+\omega^2T_3\left(\frac{\omega_o}{Q(\omega^2-\omega_o^2)}\right)+1}\right], \quad (4)$$

Although the notch frequency ω_o must be fixed at the reference frequency, the value of Q can vary. Theoretically, the reference frequency receives infinite attenuation. Actually, only about 40 dB can be realized, even under ideal conditions. Evaluation of Eq. 4 for Q's of 10, 1 and 0.1 shows that high Q values produce negligible phase-margin deterioration, but



2. **Many filter configurations can be used** to suppress sidebands. The simplest is a low-pass RC circuit (a). Somewhat more flexible is an active RC notch filter (b). But of all filters, a second-order active low-pass filter (c) is most versatile, since two of its parameters are independently adjustable.

attenuation of the second harmonic of the reference frequency is small or zero (Table 1). At a Q of 0.1, however, the second harmonic is reduced 16.5 dB, but then the phase margin suffers.

Most versatile, however, is a second-order, active, low-pass filter with variable damping (Fig. 2c). Its gain (with "s" functions of its more familiar form replaced by $j\omega$) is:[3]

$$A(j\omega) = \frac{\omega_n^2}{-\omega^2 + 2dj\omega\omega_n + \omega_n^2}, \qquad (5)$$

where ω_n = the filter's natural pole frequency,
d = the filter's damping factor.

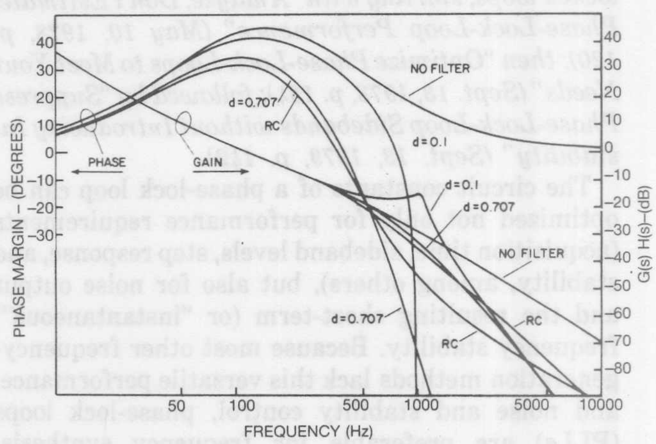
This time, multiplying Eqs. 1 and 5, the over-all open-loop transfer function becomes

$$G(j\omega)H(j\omega) = \frac{\omega_n^2 K_v K_p}{NT_1\omega^2} \times \left[\frac{-j\omega T_2 - 1}{j\omega[2d\omega_n + T_3(\omega_n^2 - \omega)] + [\omega_n^2 - \omega^2 - 2dT_3\omega_n\omega^2]}\right] \qquad (6)$$

If ω_n is chosen to be 6283 ($2\pi \times 1000$) at damping factors of 0.707 (Butterworth response) and 0.1 (16-dB peak Chebyshev), Eq. 6 gives the same sideband attenuation for both damping factors, but the high-ripple Chebyshev deteriorates the phase margin least (Table 1 and Fig. 3).

Since both the pole frequency and the damping factor can be varied in Eq. 5, the circuit it represents is most versatile. Therefore, Eq. 6 is programmed for easy solution on an HP-25 (Table 2) in 49 steps. However, for easier stability evaluation, the program solves directly for the phase margin—the difference between 180° and the open-loop transfer-function angle—rather than the phase angle itself.

Clearly, the simple RC circuit is least efficient. It gives the least sideband attenuation and the largest phase-margin deterioration. The notch filter, although theoretically capable of very high attenuation of the first sidebands only with very small phase-margin deterioration, generally requires component tolerances too critical for other than some special applications. The more complex, active, second-order low-pass filter, however, can be tailored to most applications—illustrating an often observed design phenomenon: the more complex the circuit the better the performance. Of course, then, more complex filter circuits than those used in the examples may offer even better solutions to sideband reduction. ■■



3. **A plot of open-loop gain and phase response** of the system in Fig. 1 compares sideband suppression at 5 and 10 kHz without an extra filter with that of a simple RC and an active, second-order filter.

References

1. Przedpelski, A.B., "Analyze, Don't Estimate, Phase-lock-loop Performance of Type-2, Third-order Systems," *Electronic Design*, May 10, 1978, p. 120.

2. Przedpelski, A.B., "Optimize Phase-lock Loops to Meet Your Needs," *Electronic Design*, Sept. 13, 1978, p. 134.

3. Stout, D.F., and Kaufman, M., *Operational Amplifier Circuit Design*, McGraw-Hill, NY, 1976.

Calculate the noise spectral density and short-term frequency stability in a PLL with a programmable calculator, and vary the parameters to trade off the noise/functional performance requirements.

Programmable calculator computes PLL noise, stability

This article is the fourth by the author on phase-locked loops, starting with "Analyze, Don't Estimate, Phase-Lock-Loop Performance" (May 10, 1978, p. 120); then "Optimize Phase-Lock-Loops to Meet Your Needs" (Sept. 13, 1978, p. 134); followed by "Suppress Phase-Lock-Loop Sidebands without Introducing Instability" (Sept. 13, 1979, p. 142).

The circuit constants of a phase-lock loop can be optimized not only for performance requirements (acquisition time, sideband levels, step response, and stability, among others), but also for noise output and the resulting short-term (or "instantaneous") frequency stability. Because most other frequency-generation methods lack this versatile performance, and noise and stability control, phase-lock loops (PLLs) are preferable for frequency synthesis. Moreover, a programmable HP-19C (or 21C) calculator with the proper program makes the design tradeoffs between noise effects and functional performance requirements relatively easy to determine.

A properly designed frequency synthesizer derived from a PLL (Fig. 1, top) will offer a high degree of flexibility and long-term frequency stability. In a PLL, the frequency of the stable reference oscillator (say, a quartz-crystal circuit) can be multiplied by a precisely controlled factor over a very wide range. Although the PLL may seem more complicated than the conventional so-called frequency-multiplier circuit (Fig. 1, bottom), in practice, the PLL is more efficient, more compact, and considerably wider in bandwidth. All the advantages increase as the multiplication factor increases.

In most PLL frequency synthesizers, the primary concern is the functional performance—a problem that has been treated extensively.[1] Even the theoretical aspects of phase noise in low-noise signal sources have been extensively covered.[2,3,4] However,

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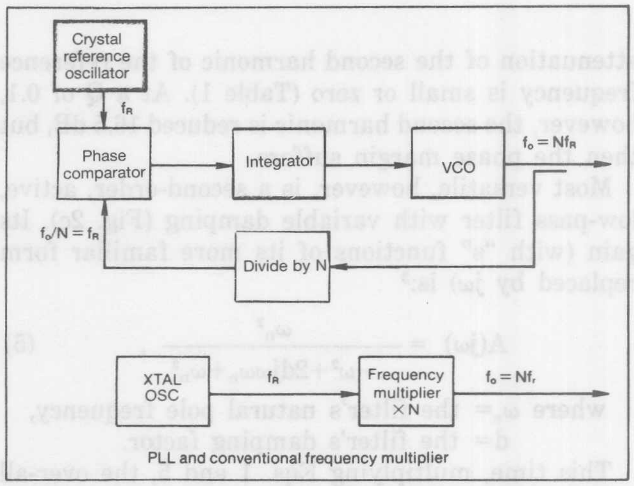
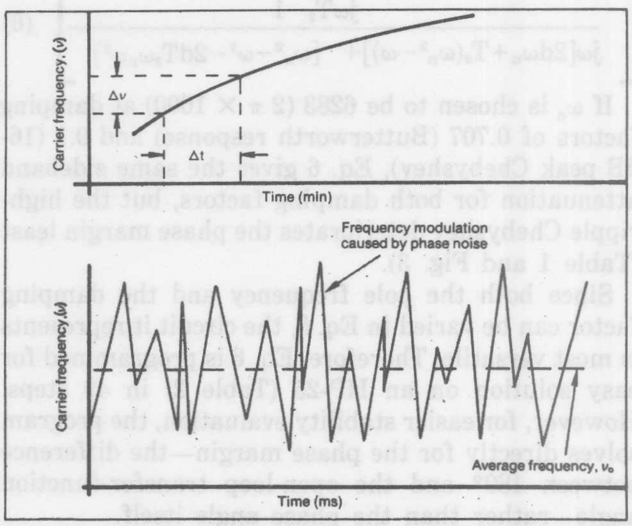


1. Although the PLL frequency multiplier (top) looks more complex than the conventional multiplier (bottom), it is in fact more compact and more flexible, and can handle a much wider frequency range.



2. Short-term frequency stability can be far worse (bottom) than the long-term average of a PLL system (top).

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specific methods for calculating the noise and short-term frequency stability and details of the tradeoffs are generally not available, except for some recent work by the National Bureau of Standards on low-noise signal sources.[5,6,7]

Short-term (or "instantaneously" sampled) frequency stability, in the millisecond range, is particularly important for accuracy in position-finding applications, as in LORAN navigation and various radar and sonar Doppler systems. Even though frequency drift over a short time generally is less than the average long-term frequency drift, instantaneously measured samples show much wider variations in the frequency swings caused by phase noise in the signal source (Fig. 2).

The overall phase-noise, or spectral-density output, $S_{\phi(\omega)0}$, of a PLL[8] is found by

$$S_{\phi(\omega)0} = S_{\phi(\omega)VCO}\left|\frac{1}{1+G(\omega)H(\omega)}\right|^2 + S_{\phi(\omega)REF}\left|\frac{G(\omega)}{1+G(\omega)H(\omega)}\right|^2,$$

where $S_{\phi(\omega)VCO}$ is the open-loop spectral density of phase fluctuations in the PLL's voltage-controlled oscillator (VCO) and $S_{\phi(\omega)REF}$ is the equivalent spectral density of fluctuations in the reference oscillator. These phase fluctuations are measured in rad^2/Hz, but generally plotted in dBc, which is $10 \log_{10} S_{\phi(\omega)}$. More commonly, however, vendor-supplied phase-noise data, designated $\mathcal{L}(\omega)$, and also measured in dBc, are for single-sideband noise. (The dBc designation is defined as $10 \log_{10}$ of the ratio between the output from a spectrum analyzer with a 1-Hz bandwidth and the signal's carrier level.) Accordingly,

$$\mathcal{L}(\omega) = 10 \log_{10}(½)S_{\phi(\omega)} \text{ (per rad}^2\text{)},$$

assuming that

$$\mathcal{L}(-\omega) = \mathcal{L}(\omega).$$

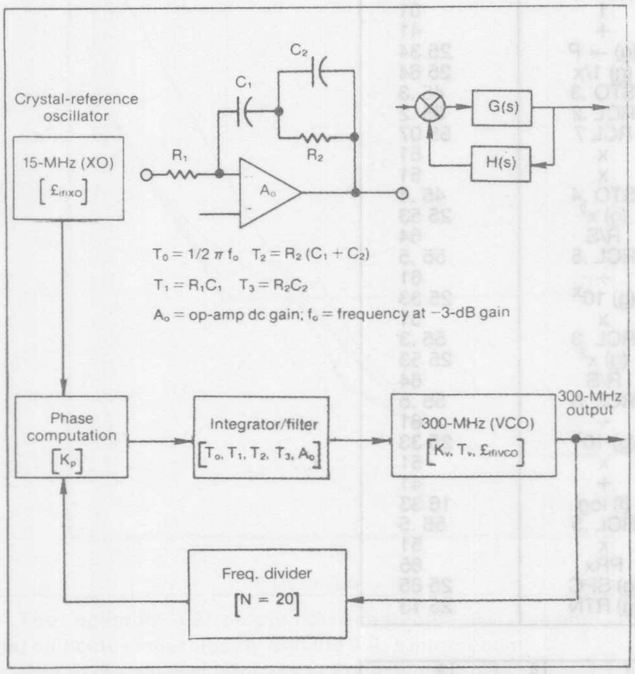
Therefore, to convert $\mathcal{L}(\omega)$ data to "straight" $S_{\phi(\omega)}$ data, add 3 dB to the $\mathcal{L}(\omega)$ data and take the antilog.

An HP-19C program (see "Noise in a 5th-order PLL") calculates this single-sideband noise, where $G(\omega)H(\omega)$ is the open-loop gain of the PLL.[1] The feedback path, $H(\omega)$, is simply 1/N; and $G(\omega)$ equals

$$\frac{(K_pK_v/\omega T_1)\,(jwT_2 + 1)}{j\left[\omega^2(\omega^2 \frac{T_o}{A_o} T_vT_3 - T_3 - T_v) + \frac{1}{A_oT_1}\right] + \omega(\omega^2 T_vT_3 - 1)}$$

Optimized for functional performance, the following circuit constants are used for a typical PLL (Fig. 3):

$A_o = 320{,}000$
$T_o = 7.96 \times 10^{-4}$ s
$T_v = 1.59 \times 10^{-7}$ s
$T_1 = 2.408 \times 10^{-5}$ s
$T_2 = 2.491 \times 10^{-6}$ s
$T_3 = 4.700 \times 10^{-7}$ s
$K_p = 314 \times 10^6$ V/rad
$K_v = 0.16$ rad/V
$N = 20$.



3. For a fifth-order PLL, four of the time constants are determined by the integrator/filter circuit, and the fifth is determined by the VCO.

The single-sideband phase noise, when calculated by the program for a range of so-called Fourier frequencies (offsets from a carrier, $f = \omega/2\pi$), can be plotted as in Fig. 4 (dotted line). Although this output phase noise can be reduced by varying circuit constants to increase the loop's bandwidth, proceed with caution, because other desirable operating characteristics (such as circuit stability or speed of response) could be compromised. The program, however, offers an easy way to determine how systematic changes in the parameters affect noise.

Oscillator noise should be low

In addition to the calculated PLL noise, Fig. 4 shows a plot of the SSB-noise characteristics of the circuit's VCO and crystal-reference oscillator. The oscillators are the main source of phase noise in a PLL. The information for plotting their noise can be obtained from the manufacturers of the oscillators, or from measurements made by the user.

Where noise reduction is of prime importance, select oscillators that generate minimum noise and have noise spectral densities that complement each other (as in Fig. 5). The point at which the two curves

Noise in 5th order PLL

Step	Instructions	Input Data/Units	Keys		Output Data/Units
1	Enter program				
2	Store	T_0	STO	0	
		T_1	STO	1	
		T_2	STO	2	
		T_3	STO	3	
		T_v	STO	4	
		K_p	STO	5	
		K_{vo}	STO	6	
		N	STO	7	
		Ao	STO	8	
		180	STO	9	
		10	STO	.5	
3	Calculate	f	GSB	0	
		$S\phi_{ref}$	R/S		
		$S\phi_{vto}$	R/S		$S\phi o$
4	Repeat step 3 for other Fourier frequencies				

Note: Enter $S\phi_{ref}$ and $S\phi_{vto}$ in dB. $S\phi o$ answer is in dB.

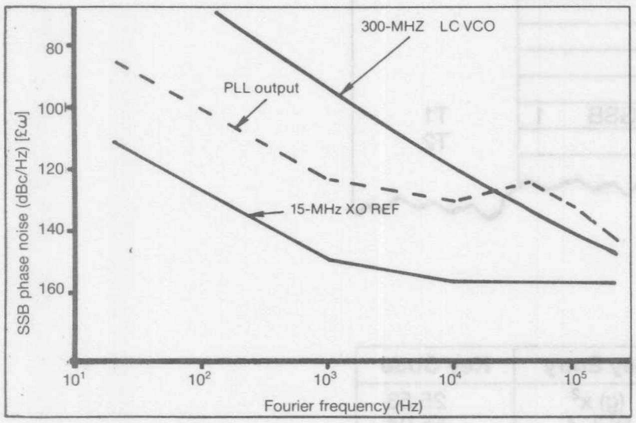
Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00	050	RCL 9	55 09
002	PRx	65	051	—	31
003	(g) DEG	25 24	052	STO .1	45 .1
004	(g) π	25 63	053	R ↓	12
005	x	51	054	÷	61
006	2	02	055	RCL 5	55 05
007	x	51	056	x	51
008	STO .0	45 .0	057	RCL 6	55 06
009	(g) x^2	25 53	058	x	51
010	RCL 0	55 00	059	RCL 7	55 07
011	x	51	060	÷	61
012	RCL 8	55 08	061	RCL 1	55 01
013	÷	61	062	÷	61
014	RCL 4	55 04	063	RCL .0	55 .0
015	x	51	064	÷	61
016	RCL 3	55 03	065	STO .2	45 .2
017	x	51	066	RCL .1	55 .1
018	RCL 3	55 03	067	x ⇌ y	11
019	—	31	068	(f) → R	16 34
020	RCL 4	55 04	069	1	01
021	—	31	070	+	41
022	RCL .0	55 .0	071	(g) → P	25 34
023	(g) x^2	25 53	072	(g) 1/x	25 64
024	x	51	073	STO .3	45 .3
025	RCL 8	55 08	074	RCL .2	55 .2
026	RCL 1	55 01	075	RCL 7	55 07
027	x	51	076	x	51
028	(g) 1/x	25 64	077	x	51
029	+	41	078	STO .4	45 .4
030	RCL .0	55 .0	079	(g) x^2	25 53
031	(g) x^2	25 53	080	R/S	64
032	RCL 3	55 03	081	RCL .5	55 .5
033	x	51	082	÷	61
034	RCL 4	55 04	083	(g) 10^x	25 33
035	x	51	084	x	51
036	1	01	085	RCL .3	55 .3
037	—	31	086	(g) x^2	25 53
038	RCL .0	55 .0	087	R/S	64
039	x	51	088	RCL .5	55 .5
040	CHS	22	089	÷	61
041	(g) → P	25 34	090	(g) 10^x	25 33
042	x ⇌ y	11	091	x	51
043	RCL 2	55 02	092	+	41
044	RCL .0	55 .0	093	(f) log	16 33
045	x	51	094	RCL .5	55 .5
046	1	01	095	x	51
047	(g) → P	25 34	096	PRx	65
048	R ↓	12	097	(g) SPC	25 65
049	+	41	098	(g) RTN	25 13

REGISTERS

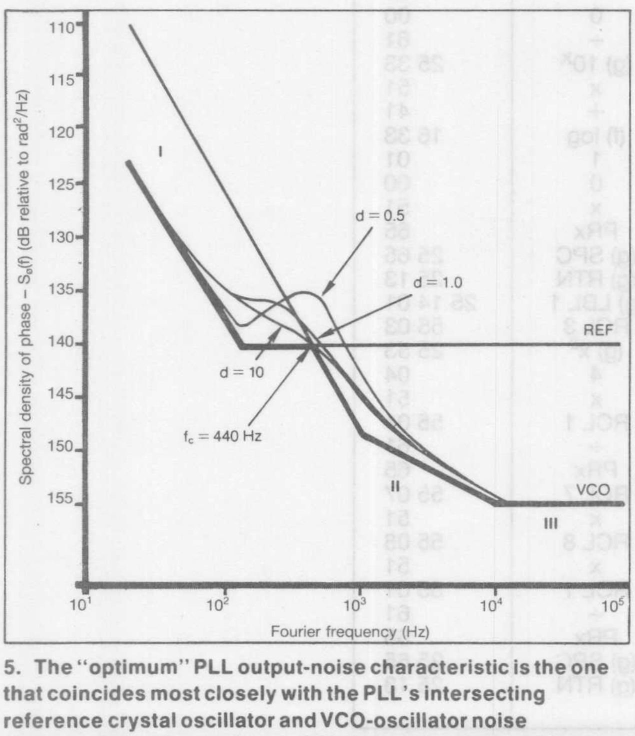
0	1	2	3	4	5	6	7	8	9
T_0	T_1	T_2	T_3	T_v	K_p	K_{vo}	N	A_o	180
S0	S1	S2	S3	S4	.5	S6	S7	S8	S9
					10				

cross is called the crossover frequency (f_c). This frequency is an important parameter for optimizing a PLL's noise characteristics.

In Fig. 5, the VCO noise-distribution plot is divided into three characteristic regions. High-quality oscillators generally exhibit this spectral-density relationship. In region I, $S_{\phi(f)}$ is typically proportional to $1/f^3$, so-called flicker-frequency noise; in region II, $S_{\phi(f)}$ is proportional to $1/f^2$, so-called white-frequency noise; and in region III, $S_{\phi(c)}$ is constant, so-called white-phase noise. Beyond region III, the bandwidth limitation of the circuit attenuates the



4. A PLL is optimized for performance characteristics, such as stability, response time, and sideband levels; but the noise characteristics generally fall where they may, as exemplified in this plot of a fifth-order PLL.



5. The "optimum" PLL output-noise characteristic is the one that coincides most closely with the PLL's intersecting reference crystal oscillator and VCO-oscillator noise characteristics (heavy lines). A high damping-factor value (such as d = 10) makes the best correspondence with this criterion.

noise to negligible levels.

Region I noise stems from fluctuations in oscillator-circuit frequency-control components; region II, from thermal noise in the oscillator's gain element; and region III, from additive thermal noise from other elements of the circuit (including the gain element).

A plot of the optimum phase-noise characteristic of a PLL would coincide with the lower parts of the two oscillator curves (heavy lines in Fig. 5).

The type-2, second-order PLL circuit in Fig. 6 helps to illustrate how closely this condition can be approached. This circuit can be generalized by relating the integrator's time constants (T_1 and T_2) and the VCO's and phase comparator's transfer coefficients (K_v and K_p) with a damping factor (d), and with the reference and VCO crossover frequency ($f_c = \omega_c/2\pi$), as follows:

$$d = (T/2)\ \sqrt{K_pK_v/T_1};\ d >> 1$$
$$T_2 = 4d^2/\omega_c$$
$$T_1 = T_2K_pK_v/\omega_c.$$

When these circuit parameters are considered together with the circuit's open-loop gain (note: $H(\omega) = 1$),

$$G(\omega)H(\omega) = \frac{K_pK_v}{T_1\omega^2}\,(-j\omega T_2 - 1),$$

and substituted in the phase-noise equation for $S_{\phi(\omega)0}$, the PLL's spectral density becomes

$$S_{\phi(\omega)0} = S_{\phi(\omega)VCO}\left[\frac{1}{\left(1 - \frac{\omega_c^2}{4d^2\omega^2}\right) + \left(\frac{\omega_c^2}{\omega}\right)}\right] + S_{\phi(\omega)REF}\left[\frac{\left(\frac{1}{2d}\right)^2\left(\frac{\omega_c}{\omega}\right)^2 + \left(\frac{\omega_c}{\omega}\right)^2}{\left(1 - \frac{\omega_c^2}{4d^2\omega^2}\right) + \left(\frac{\omega_c}{\omega}\right)^2}\right]$$

The "Optimizing PLL Phase Noise" program, with its subroutine 0, solves this equation for any Fourier frequency ($f = \omega/2\pi$). In Fig. 5, solutions are shown for damping-factor values (d) of 0.5, 1.0, and 10.

The largest damping factor (d = 10) causes the noise curve to approach the "optimum" noise characteristic most closely—when it lies completely between the VCO/reference-oscillator lines and as closely as possible to the lower lines. To satisfy this criterion, the curve generally passes through the frequency crossover point previously mentioned. Larger damping values than 10 will provide little further improvement. In fact, a larger damping value would slow response more than it would lower the noise output. Special cases may require low damping

Optimizing PLL phase noise

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Enter program			
2	Store	fc	STO 2	
		d	STO 3	
		Kp	STO 7	
		Kv	STO 8	
3	Calculate phase noise	f	GSB 0	
		Sφvco	R/S	
		Sφref	R/S	Sφo
4	Repeat step 3 for other values of Fourier frequency			
5	Calculate time constants		GSB 1	T1
				T2

Note: —Sφvco, Sφref and Sφo in dB

Subroutine 0 must be performed before the time constants can be calculated with subroutine 1

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 0	25 14 00	038	(g) x^2	25 53
002	PRx	65	039	RCL 4	55 04
003	(g) π	25 63	040	+	41
004	x	51	041	RCL 5	55 05
005	2	02	042	÷	61
006	x	51	043	R/S	64
007	(g) 1/x	25 64	044	1	01
008	RCL 2	55 02	045	0	00
009	(g) π	25 63	046	÷	61
010	x	51	047	(g) 10^x	25 33
011	2	02	048	x	51
012	x	51	049	+	41
013	STO 1	45 01	050	(f) log	16 33
014	x	51	051	1	01
015	(g) x^2	25 53	052	0	00
016	STO 4	45 04	053	x	51
017	RCL 3	55 03	054	PRx	65
018	(g) x^2	25 53	055	(g) SPC	25 65
019	÷	61	056	(g) RTN	25 13
020	4	04	057	(g) LBL 1	25 14 01
021	÷	61	058	RCL 3	55 03
022	STO 6	45 06	059	(g) x^2	25 53
023	CHS	22	060	4	04
024	1	01	061	x	51
025	+	41	062	RCL 1	55 01
026	(g) x^2	25 53	063	÷	61
027	RCL 4	55 04	064	PRx	65
028	+	41	065	RCL 7	55 07
029	STO 5	45 05	066	x	51
030	(g) 1/x	25 64	067	RCL 8	55 08
031	R/S	64	068	x	51
032	1	01	069	RCL 1	55 01
033	0	00	070	÷	61
034	÷	61	071	PRx	65
035	(g) 10^x	25 33	072	(g) SPC	25 65
036	x	51	073	(g) RTN	25 13
037	RCL 6	55 06			

REGISTERS

0	1	2	3	4	5	6	7	8	9
		fc	d				Kp	Kv	

factors—a value of 1 or even 0.5—to get a faster response or the special noise-distribution shapes that these lower damping factors produce.

After the phase-noise characteristics (based on the f_c of the oscillators and a selected damping factor) have been calculated, a second part of the optimizing program (subroutine 1) can then be used to calculate the time constants T_1 and T_2 for the given K_p and K_v of a type-2 second-order PLL.

Determining a PLL's short-term frequency stability requires integration of the spectral density of the phase fluctuations to obtain the so-called Allan variance (a dimensionless measure of stability, where σ_y^2 is $\Delta f/f$ in a short sample period). Thus

$$\sigma_y^2(\tau, f_h) = \frac{2}{(\tau\nu\pi)^2} \int_0^{f_h} S_{\phi(f)} \sin^4 (\pi f \tau) df,$$

where τ is the sampling time (in seconds), ν is the long-term average frequency (in Hz), and f_h is the bandwidth, or maximum excursion of the offset from the carrier (the maximum Fourier frequency).

Figure 7 (top) shows the relationship between frequency or phase and the frequency spectral-noise densities, along with the resultant short-term frequency stabilities, for several distinct types of phase or frequency noise. A typical complex signal source (such as a PLL) could have a combined short-term frequency stability as in Fig. 7 (bottom). But such noise types generally do not obey simple integer-power curves and, therefore, pose a problem: The Allan equation does not have a closed-form solution for fractional powers, so it cannot be used directly. Nevertheless, very accurate answers can be obtained with Simpson's Rule and a programmable calculator.

Although the Allan equation requires integration over the Fourier frequency range of 0 to f_h, the low-frequency limit of 0 Hz cannot be used in a log-log Simpson's Rule integration. Fortunately, frequencies below $(2\pi\tau_h)^{-1}$, where τ_h is the longest sampling time, do not contribute appreciably to the value of the Allan variance. The longest sampling time for short-term effects is generally 1 s; therefore, for a measuring-system bandwidth of 1000 Hz, just the Fourier frequencies between about 0.16 and an f_h of 1000 Hz need be considered. (Since the manufacturer did not supply data below 2 Hz for the reference oscillator and VCO used in Fig. 5; a new oscillator with data to 0.1 Hz was substituted in Fig. 8, top.)

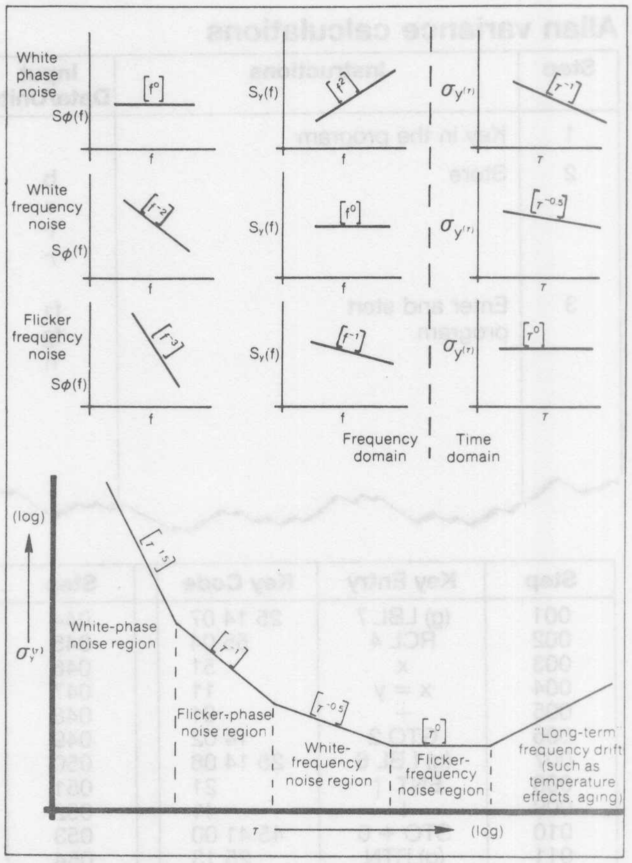
As shown in Fig. 7 (bottom) and Fig. 8 (top), the phase-noise curves can be approximated with straight-line segments. The segments are plotted on semilog paper with $S_{\phi(f)}$ measured in dBc on the vertical axis. Therefore, the segments,

$$y = ax^b,$$

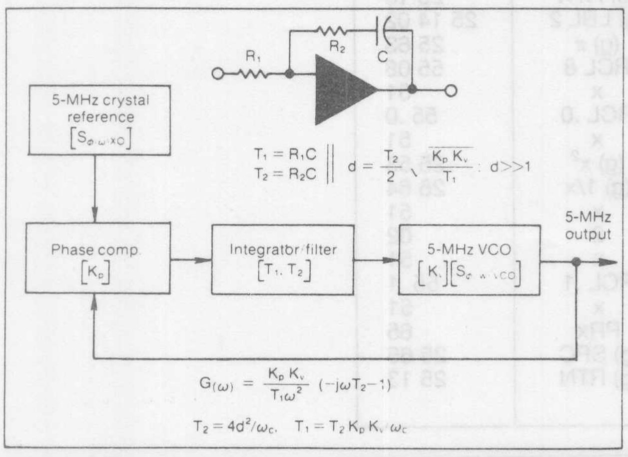
can be established from the end points on their phase-noise curves—where $S_{\phi(f_1)}$ and $S_{\phi(f_2)}$ correspond to the low-frequency (f_1) and the high-frequency (f_2) end points, as follows:

$$b = \frac{S_{\phi(f_1)} - S_{\phi(f_2)}}{10 (\log f_1 - \log f_2)}$$

and



7. **The distribution of the different types of frequency and phase noise can be expressed as line segments that represent powers of frequency or time (top), and the overall distribution of a system can be shown by combining appropriate segments (bottom).**



6. **The phase-output noise in this type-2 second-order PLL can be optimized by adjusting the damping factor (d) in relation to the oscillator-noise crossover frequency (f_c).**

Allan variance calculations

Step	Instructions	Input Data/Units	Keys	Output Data/Units
1	Key in the program			
2	Store	b	STO 7	
		a	STO .1	
		ν	STO .0	
		τ	STO 8	
3	Enter and start program	f1	ENT ↑	
		f2	ENT ↑	
		n	GSB .3	$\sigma^2 y$

Step	Key Entry	Key Code	Step	Key Entry	Key Code
001	(g) LBL 7	25 14 07	044	RCL 4	55 04
002	RCL 4	55 04	045	STO + 5	45 41 05
003	x	51	046	RCL 5	55 05
004	x ⇌ y	11	047	GSB 0	13 00
005	÷	61	048	GSB 6	13 06
006	GTO 2	14 02	049	(g) RTN	25 13
007	(g) LBL 6	25 14 06	050	(g) LBL 5	25 14 05
008	ENT ↑	21	051	3	03
009	+	41	052	RCL 0	55 00
010	STO + 0	45 41 00	053	GTO 7	14 07
011	(g) RTN	25 13	054	(g) LBL 0	25 14 00
012	(g) LBL 3	25 14 03	055	(g) RAD	25 23
013	STO 3	45 03	056	STO 6	45 06
014	R ↓	12	057	(g) π	25 63
015	STO 2	45 02	058	x	51
016	R ↓	12	059	RCL 8	55 08
017	STO 1	45 01	060	x	51
018	GSB 0	13 00	061	(f) sin	16 42
019	STO 0	45 00	062	(g) x^2	25 53
020	RCL 2	55 02	063	(g) x^2	25 53
021	GSB 0	13 00	064	RCL 6	55 06
022	STO +0	45 41 00	065	RCL 7	55 07
023	RCL 2	55 02	066	(f) y^x	16 54
024	RCL 1	55 01	067	x	51
025	STO 5	45 05	068	(g) DEG	25 24
026	—	31	069	(g) RTN	25 13
027	RCL 3	55 03	070	(g) LBL 2	25 14 02
028	÷	61	071	(g) π	25 63
029	STO 4	45 04	072	RCL 8	55 08
030	0	00	073	x	51
031	STO 9	45 09	074	RCL .0	55 .0
032	(g) LBL 8	25 14 08	075	x	51
033	GSB 4	13 04	076	(g) x^2	25 53
034	STO + 0	45 41 00	077	(g) 1/x	25 64
035	2	02	078	x	51
036	STO + 9	45 41 09	079	2	02
037	RCL 3	55 03	080	x	51
038	RCL 9	55 09	081	RCL .1	55 .1
039	(f) x = y	16 61	082	x	51
040	GTO 5	14 05	083	PRx	65
041	GSB 4	13 04	084	(g) SPC	25 65
042	GTO 8	14 08	085	(g) RTN	25 13
043	(g) LBL 4	25 14 04			

REGISTERS

0	1	2	3	4	5	6	7	8	9
							b	τ	
.0 ν	.1 α	.2	.3	.4	.5	S6	S7	S8	S9

$$a = 10^{\left(\frac{S_{\phi(f_1)} - 10\, b \log f_1}{10}\right)}.$$

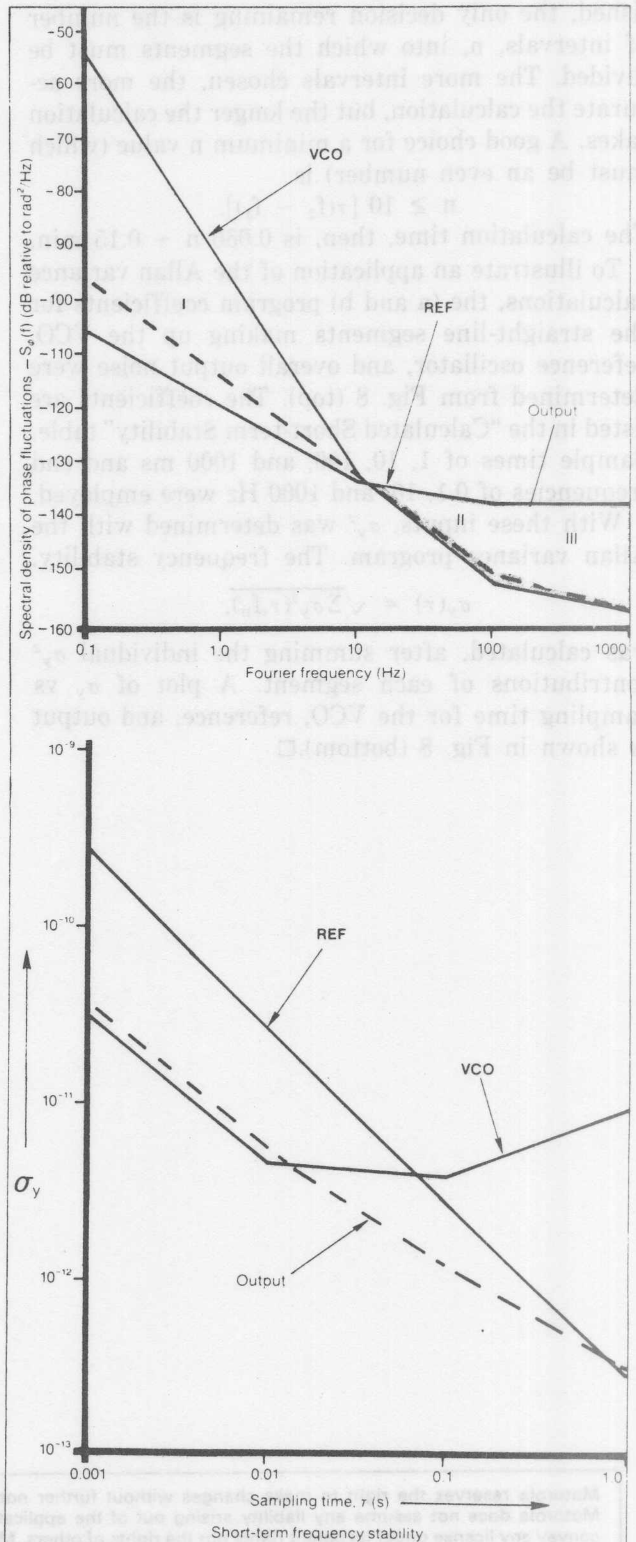
With coefficients a and b established for each line segment, the contributions of each segment to the overall Allan variance $\sigma_y{}^2$ can be calculated with the approximate Allan equation,

$$\sigma_y{}^2(\tau, f) = \frac{2a}{(\tau\nu\pi)^2} \int_{f_1}^{f_2} f^b \sin^4(\pi f \tau)\, df,$$

by a modified Simpson's Rule program supplied by Hewlett-Packard (HP-19C/29C *Applications' Book*, 1977). The Simpson's Rule is incorporated into the

Calculated short-term stability

Device	Segment I				
Reference oscillator	f_1 = 0.1 Hz, f_2 = 10 Hz; a = 1.26×10^{-12}, b = −1.40				
	T/n	0.001/10	0.01/10	0.1/20	1/100
	σy^2	1.10×10^{-27}	1.05×10^{-25}	4.80×10^{-25}	1.76×10^{-26}
Voltage-controlled oscillator	f_1 = 0.1 Hz, f_2 = 10 Hz; a = 5.01×10^{-10}, b = −3.90				
	T/n	0.001/10	0.01/10	0.1/20	1/100
	σy^2	4.49×10^{-27}	4.39×10^{-25}	1.34×10^{-23}	8.10×10^{-23}
PLL output	f_1 = 0.1 Hz, f_2 = 100 Hz; a = 4.64×10^{-12}, b = −1.83				
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	σy^2	2.43×10^{-24}	1.46×10^{-23}	1.19×10^{-24}	8.21×10^{-26}
Device	**Segment II**				
Reference oscillator	f_1 = 10 Hz, f_2 = 100 Hz; a = 1.26×10^{-13}, b = −0.40				
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	σy^2	3.27×10^{-23}	8.22×10^{-23}	7.56×10^{-25}	7.56×10^{-27}
Voltage-controlled oscillator	f_1 = 10 Hz, f_2 = 100 Hz; a = 6.31×10^{-12}, b = −2.00				
	T/n	0.001/10	0.01/20	0.1/100	1/1000
	σy^2	1.59×10^{-24}	1.06×10^{-23}	1.63×10^{-25}	1.27×10^{-27}
PLL output	f_1 = 100 Hz, f_2 = 1000 Hz; a = 2.51×10^{-14}, b = −0.70				
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	σy^2	1.04×10^{-21}	1.00×10^{-23}	1.01×10^{-25}	1.01×10^{-27}
Device	**Segment III**				
Reference oscillator	f_1 = 100 Hz, f_2 = 1000 Hz; a = 2.00×10^{-14}, b = 0.00				
	T/n	0.001/20	0.01/100	0.1/1000	1/10,000
	σy^2	6.08×10^{-20}	5.47×10^{-22}	5.47×10^{-24}	5.47×10^{-26}
Voltage-controlled oscillator	f_1 = 100 Hz, f_2 = 1000 Hz; a = 6.31×10^{-15}, b = −0.50				
	T/n	0.001/20	0/01/100	0.1/1000	1/10,000
	σy^2	8.88×10^{-22}	8.27×10^{-24}	8.28×10^{-26}	



8. The phase-noise characteristics of the reference oscillator and the VCO can be expressed with three straight-line segments (I, II, and III); and the PLL output, by two (top). The short-term stability in terms of the Allan variance can then be calculated by keying the required coefficients as determined from the coordinates of these line-segment ends into the calculator (see Table) and plotting the results (bottom).

complete program for an HP-19C calculator—"Allan Variance Calculations." With a, b, ν, and τ established, the only decision remaining is the number of intervals, n, into which the segments must be divided. The more intervals chosen, the more accurate the calculation, but the longer the calculation takes. A good choice for a minimum n value (which must be an even number) is

$$n \geq 10\,[\tau(f_2 - f_1)].$$

The calculation time, then, is 0.056 n + 0.15 min.

To illustrate an application of the Allan variance calculations, the (a and b) program coefficients for the straight-line segments making up the VCO, reference oscillator, and overall output noise were determined from Fig. 8 (top). The coefficients are listed in the "Calculated Short-term Stability" table. Sample times of 1, 10, 100, and 1000 ms and end frequencies of 0.1, 10, and 1000 Hz were employed.

With these inputs, σ_y^2 was determined with the Allan variance program. The frequency stability,

$$\sigma_y(\tau) = \sqrt{\Sigma\sigma_y^2(\tau,f_h)},$$

was calculated, after summing the individual σ_y^2 contributions of each segment. A plot of σ_y vs sampling time for the VCO, reference, and output is shown in Fig. 8 (bottom).□

Acknowledgments

The author wishes to thank Dr. D. Halford and Dr. Fred L. Walls of the National Bureau of Standards, whose constructive discussions contributed to a more insightful understanding of the problems involved in working with PLL noise and short-term frequency stability.

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Printed in Great Britain by Tavistock Press (Bedford) Ltd. 2000 9/87