The Phase Locked Loop IC as a Communication System Building Block

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INTRODUCTION

The phase locked loop has been found to be a useful element in many types of communication systems. It is used in two fundamentally different ways: (1) as a demodulator, where it is used to follow phase or frequency modulation and (2) to track a carrier or synchronizing signal which may vary in frequency with time.

When operating as a demodulator, the phase locked loop may be thought of as a matched filter operating as a coherent detector. When used to track a carrier, it may be thought of as a narrow-band filter for removing noise from a signal.

Recently, a phase locked loop has been built on a monolithic integrated circuit, incorporating the basic elements necessary for operation: a double balanced phase detector and a highly linear voltage controlled oscillator, the frequency of which can be varied with either a resistor or capacitor.

BASIC PHASE LOCK LOOP OPERATION

Figure 1 shows the basic blocks of a phase locked loop. The input signal e_i is a sinusoid of arbitrary frequency, while the VCO output signal, e_o, is a sinsuoid of the same frequency as the input but of arbitrary phase. If

$$e_i = \sqrt{2}\, E_i \sin [\omega_o t + \theta_1(t)] \quad (1)$$

$$e_o = \sqrt{2}\, E_o \cos [\omega_o t + \theta_2(t)] \quad (2)$$

the output of the multiplier (phase detector) is

$$\begin{aligned} e_d &= e_i \bullet e_o \\ &= 2E_iE_o \sin [\omega_o t + \theta_1(t)] \bullet \cos [\omega_o t + \theta_2(t)] \\ &= E_iE_o \sin [\theta_1(t) - \theta_2(t)] + E_iE_o \sin [2\omega_o t + \theta_1(t) + \theta_2(t)] \end{aligned} \quad (3)$$

the low pass filter of the loop removes the ac components of the multiplier output; the dc term is seen to be a function of the phase angle between the VCO and the input signal.

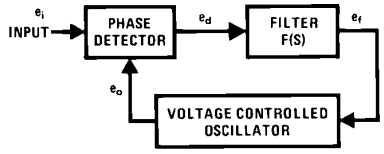

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FIGURE 1. Basic Phase Locked Loop

The output of the VCO is related to its input control voltage by

$$\dot{\theta}_2(t) = K_o e_f \quad (4)$$

for $e_f = 0$, Let $\dot{\theta}_2 = \omega\theta$, then

$$\theta_2(t) = \int e_f(t)\, dt \quad (5)$$

It can be seen that the action of the VCO is that of an integrator in the feedback loop when the phase locked loop is considered in servo theory.

A better understanding of the operation of the loop may be obtained by considering that initially, the loop is not in lock, but that the frequency of the input signal e_i and VCO e_o are very close in frequency. Under these conditions e_d will be a beat note, the frequency of which is equal to the frequency difference of e_o and e_i. This signal is also applied to the VCO input, since it is low enough to pass through the filter. The instantaneous frequency of the VCO is therefore changing and at some point in time, if the VCO frequency equals the input frequency, lock will result. At this instant, e_f will assume a level sufficient to hold the VCO frequency in lock with the input frequency. If the tuning of the VCO is changed (such as by varying the value of the tuning capacitor) the frequency output of the VCO will attempt to change; however, this will result in an instantaneous change in phase angle between e_i and e_o, resulting in a change in the dc level of e_d which will act to maintain frequency lock: no average frequency change will result.

Similarly, if e_i changes frequency, an instantaneous change will result in a phase change between e_i and e_o and hence a dc level change in e_d. This level shift will change the frequency of the VCO to maintain lock.

The amount of phase error resulting from a given frequency shift can be found by knowing the ''dc'' loop gain of the system. Considering the phase detector to have a transfer function:

$$E_d = K_D (\theta_1 - \theta_2)$$

and the voltage controlled oscillator to have a transfer function:

$$\dot{\theta}_2 = K_o e_f \quad (6)$$

or taking the Laplace transform

$$\theta_2 (s) = \frac{K_o e_f}{s} \quad (7)$$

the phase of the VCO output will be proportional to the integral of the control voltage.

Combining these equations:

$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_oK_d F(s)}{s + K_oK_D F(s)} \quad (8)$$

$$\frac{\theta_1(s) - \theta_2(s)}{\theta_1(s)} = \frac{s}{s + K_oK_D F(s)} \quad (9)$$

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Application of the final value theorem of Laplace transforms yields

$$\lim_{t \to \infty} \theta_1(s) - \theta_2(s) = \lim_{s \to 0} \frac{s^2\,\theta_1(s)}{s + K_o K_D\,F(s)} \qquad (10)$$

With a step change in phase of the input $\Delta\theta_1$, the Laplace transform of the input is

$$\theta_1(s) = \frac{\Delta\theta_1}{s} \text{ which gives } \theta_e(s) = \theta_1(s) - \theta_2(s)$$

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} \frac{s\Delta\theta_1}{s + K_o K_D\,F(s)} = 0 \qquad (11)$$

the loop will eventually track out any change of input phase, and there will be no phase error in the steady state solution.

If the input is a step in frequency, of magnitude $\Delta\omega$, the change in input phase will be a ramp:

$$\theta_1(s) = \Delta\omega/s^2$$

substitution of this value θ, into (10) results in

$$\lim_{t \to \infty} \theta_e(t) = \lim_{s \to 0} \frac{\Delta\omega}{s + K_o K_D\,F(s)} = \frac{\Delta\omega}{K_o K_D\,F(o)} \qquad (12)$$

this result shows the resulting phase error is dependent on the magnitude of the frequency step and the ''dc'' loop gain $K_o K_D$, which is also called the velocity error coefficient K_v. It should be noted that the dimensions of $K_o K_D$ are 1/sec. This can also be seen by considering K_D = volts/radian, while K_o = radians/sec/volt. The product is

$$\frac{\text{volts}}{\text{radian}} \times \frac{\text{radians/sec}}{\text{volt}} = \frac{1}{\text{sec}}$$

this can be thought of as the ''dc'' loop gain. (Note that additional dc gain between the phase detector and the voltage controlled oscillator will increase the loop gain and hence reduce the steady state phase error resulting from a change in frequency of the input).

THE LOOP FILTER

In working with phase locked loops, it is necessary to consider not only the ''dc'' performance described above, but the ''ac'' or transient performance which is governed by the components of the loop filter placed between the phase detector and the voltage controlled oscillator. In fact, it is this loop filter that makes the phase locked loop so powerful: only a resistor and capacitor are all that is needed to produce an arbitrarily narrow bandwidth at any selected center frequency.

The simplest filter is a single capacitor, *Figure 2*, and is used for wide bandwith applications, such as where wideband data modulation must be followed. The transfer function of the filter is simply:

$$\frac{e_f}{e_d} = \frac{1}{1 + sR_1\,C_1} \qquad (13)$$

substitution into (8) results in

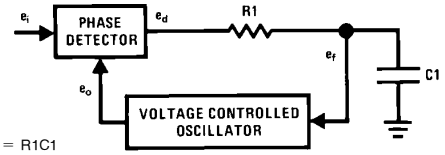
$$\frac{\theta_2(s)}{\theta_1(s)} = \frac{K_o K_D/\tau_1}{s^2 + s/\tau_1 + K_o K_D/\tau_1} \qquad (14)$$

$$\tau_1 = R_1\,C_1$$

In terms of servo theory, the damping factor and natural frequencies are

$$\omega_n = \left[\frac{K_o K_D}{R_1\,C_1}\right]^{1/2} \qquad (15)$$

$$\zeta = \frac{1}{2}\left[\frac{1}{(R_1\,C_1\,K_o K_D)}\right]^{1/2} \qquad (16)$$



τ_1 = R1C1

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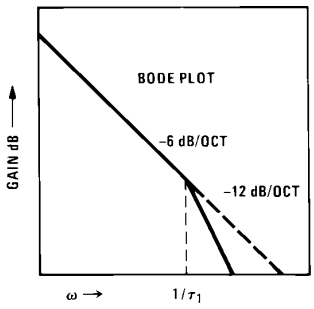

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FIGURE 2. Phase Locked Loop with Simple Filter

From this it can be seen that large time constants for $R_1\,C_1$ or high loop gain will reduce the damping factor and hence decrease stability. Therefore, if a narrow bandwidth is desired, the damping factor will become very small and instability will result. It is not possible to adjust bandwidth, loop gain, and damping independently with this simple filter.

With the addition of a damping resistor R_2 as shown in *Figure 3*, it is possible to choose bandwidth, damping factor and loop gain independently; the transfer function of this filter is

$$\frac{e_d}{e_f} = \frac{1 + s\tau_2}{1 + s\tau_1} \tag{17}$$

the loop transfer function becomes:

$$\frac{\theta_2(s)}{\theta_z(s)} = \frac{K_o K_D (s\,\tau_2 + 1)(\tau_1 + \tau_2)}{s^2 + s(1 + K_o K_d\,\tau_2)/\tau_1 + K_o K_D/\tau_1} \tag{18}$$

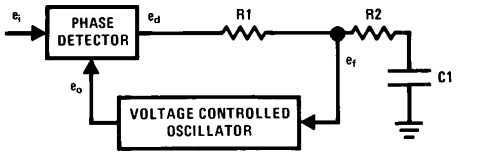
the loop natural frequency is

$$\omega_n = \left[\frac{K_o K_D}{\tau_1}\right]^{1/2} \tag{19}$$

while the damping factor becomes

$$\zeta = \frac{1}{2}\left[\frac{1}{\tau_1 K_o K_D}\right]^{1/2}\left[1 + \tau_2 K_o K_D\right] \tag{20}$$

$$\cong \frac{\omega_n \tau_2}{2} \tag{21}$$



τ_1 = R1C1 τ_2 = R2C1 TL/H/7363–4

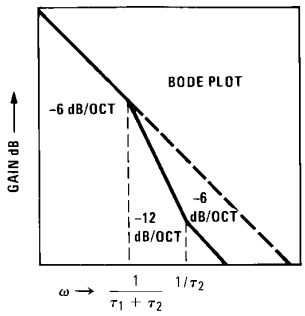


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FIGURE 3. Phase Locked Loop with Damping Resistor Added

In practice, for a fixed loop gain $K_o K_D$, the natural frequency of the loop may be chosen and will be dependent mainly on τ_1, since $\tau_2 \ll \tau_1$ in most cases. Then, according to (21), damping may be determined by τ_2 and for all practical purposes, will be an independent adjustment. These equations are plotted in *Figures 4* and *5* and may be used for design purposes.

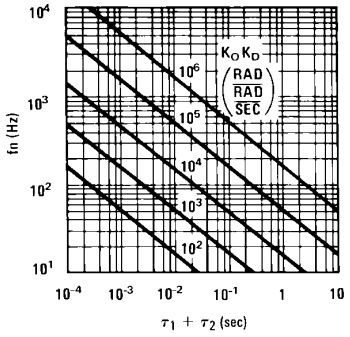

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FIGURE 4. Filter Time Constant vs Natural Frequency

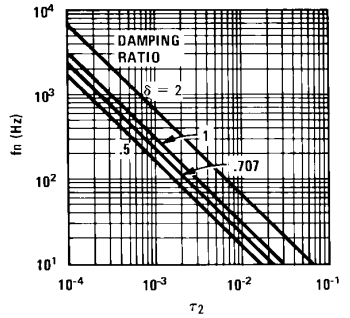

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FIGURE 5. Damping Time Constant vs Natural Frequency

DESIGN CONSIDERATIONS

Considering the above discussion, there are really two primary considerations in designing a phase locked loop. The use to which the loop is to be put will affect the design criterion of the loop components. The two primary factors to consider are:

1. Loop gain. As pointed out previously, this affects the phase error between the input signal and the voltage controlled oscillator for a given frequency shift of the input signal. It also determines the ''hold in range'' of the loop providing no components of the loop go into limiting or saturation. This is because the loop will remain in lock as long as the phase difference between the input and the VCO is less than $\pm 90°$. The higher the loop gain, the further the input can change in frequency before the 90° phase error is reached. The hold in range is

$$\Delta\omega_H = \pm K_o K_D \tag{22}$$

(providing saturation or limiting does not occur).

2. Natural Frequency. The bandwidth of the loop is determined by the filter components R_1, R_2 and C_1, and the loop gain. Since the loop gain is normally selected by the criterion in 1. above, the filter components are used to select the bandwidth. The selection of loop bandwidth may be governed by several things: noise bandwidth, modulation rates if the loop is to be used as an FM de-

modulator, pull-in time and hold-in range. There are two conflicting requirements that will have an affect on loop bandwidth:

(a) Loop bandwidth must be as narrow as possible to minimize output phase jitter due to external noise.

(b) The loop bandwidth should be made as large as possible to minimize transient error due to signal modulation, output jitter due to internal oscillator (VCO) noise, and to obtain best tracking and acquisition properties.

These two principles are in direct opposition and, depending on what it is that the loop is to accomplish, an optimum solution will lie somewhere between the two extremes.

If the phase locked loop is to be used to demodulate frequency modulation, the design should proceed with the criterion of b above. It is necessary to provide sufficient loop bandwidth to accommodate the expected modulation. It must be remembered that at all times, the loop must remain in lock, (peak phase error less than 90°), even under extremes of modulation, such as peaks or step changes in frequency.

For the case of sinusoidal frequency modulation, the peak phase error as a function of frequency deviation and damping factor is shown in *Figure 6*.

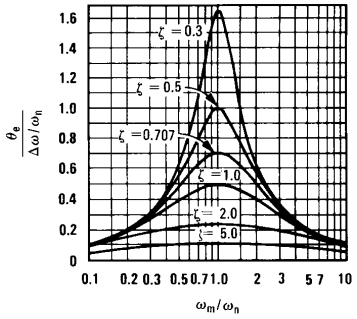

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FIGURE 6. Steady-State Peak Phase Error Due to Sinusoidal FM (High-Gain, Second-Order Loop)

It can be seen that the maximum phase error occurs when the modulating frequency ω_m equals the loop natural frequency ω_n; if the loop has been designed with a damping factor of 0.707, the peak phase error (in radians) will be 0.71 $\Delta\omega/\omega_n$ ($\Delta\omega$ = frequency deviation). From this plot, it is possible to choose ω_n for a given deviation and modulation frequency.

If the loop is to demodulate frequency shift keying (FSK), it must follow step changes in frequency. The filter components must then be chosen in accordance with the transient phase error shown in *Figure 7*. It must be remembered that the loop filter must be wide enough so the loop will not lose lock when a step change in frequency occurs: the greater the frequency step, the wider the loop filter must be to maintain lock.

There is some frequency-step limit below which the loop does not skip cycles, but remains in lock, called the ''pull-out frequency'' ω_{po}. Viterbi has analyzed this and his results are shown in *Figure 8*, which plots normalized pull out frequency for various damping factors for high gain second order loops. Peak phase errors for other types of input signals are shown in *Figures 8* and *9*.

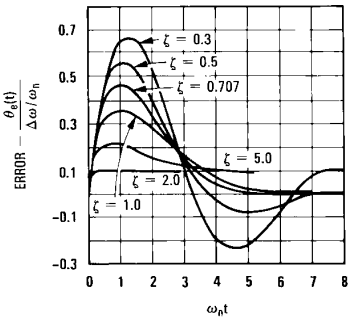

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FIGURE 7. Transient Phase Error $\theta_e(t)$ Due to a Step in Frequency $\Delta\omega$. (Steady-State Velocity Error, $\Delta\omega/K_v$, Neglected)

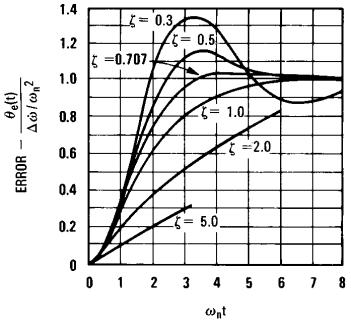

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FIGURE 8. Transient Phase Error $\theta_e(t)$ Due to a Ramp in Frequency $\Delta\omega$. (Steady-State Acceleration Error, $\Delta\omega/\omega_n^2$, Included. Velocity Error, $\Delta\omega t/K_v$, Neglected)

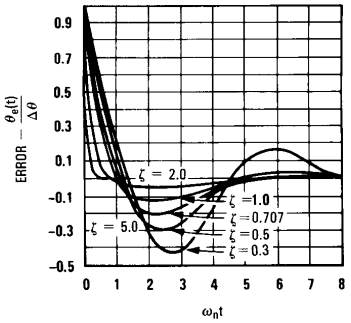

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FIGURE 9. Phase Error $\theta_e(t)$ Due to a Step in Phase $\Delta\theta$

In designing loops to track a carrier or synchronizing signal, it is desirable to make the loop bandwidth narrow so that phase error due to external noise will be small. However, it is necessary to make the loop bandwidth wide enough so that any frequency jitter on the input signal will be followed.

NOISE PERFORMANCE

Since one of the main uses of phase locked loops is to demodulate or track signals in noise, it is helpful to look at how noise affects the operation of the phase locked loop.

The phase locked loop, as mentioned earlier, may be thought of as a filter with a fixed, adjustable bandwidth. We have seen how to calculate the loop natural frequency ω_n (15), (19), and the damping factor ζ (16), (20). Without going through a derivation, the loop noise bandwidth B_L may be shown to be

$$B_L = \int_o^\infty |H(j\omega)|^2 \, df = \frac{\omega_n}{2}\left[\zeta + \frac{1}{4\zeta}\right] \text{Hz} \qquad (23)$$

for a high gain, second order loop. This equation is plotted in *Figure 10*. It should be noted that the dimensions of noise bandwidth are cycles per second while the dimensions of ω_n are radians per second.

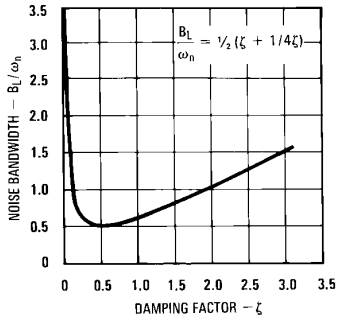

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FIGURE 10. Loop-Noise Bandwidth (For High-Gain, Second-Order Loop)

Noise threshold is a difficult thing to analyze in a phase locked loop, since we are talking about a statistical quantity. Noise will show up in the input signal as both amplitude and phase modulation. It can be shown that near optimum performance of a phase locked loop can be obtained if a limiter is used ahead of the phase detector, or if the phase detector is allowed to operate in limiting. With the use of a limiter, amplitude modulation of the input signal by noise is removed, and the noise appears as phase modulation. As the input signal to noise ratio decreases, the phase jitter of the input signal due to noise increases, and the probability of losing lock due to instantaneous phase excersions will increase. In practice it is nearly impossible to acquire lock if the signal to noise ratio in the loop $(SNR)_L = 0$ dB. In general, $(SNR)_L$ of $+6$ dB is needed for acquisition. If modulation or transient phase error is present, a higher signal to noise ratio is needed to acquire and hold lock.

A computer simulation performed by Sanneman and Rowbotham has shown the probability of skipping cycles for various loop signal to noise ratios for high gain, second order loops. Their data is shown in *Figure 11*.

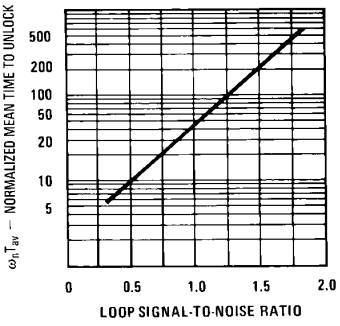

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FIGURE 11. Unlock Behavior of High-Gain, Second-Order Loop, $\zeta = 0.707$

When designing the loop filter components, enough bandwidth in the loop must be allowed for instantaneous phase change due to input noise. In the previous section, the filter was selected on the basis that the peak error due to modulation would be less than 90° (so the loop would not loose lock). However, if noise is present, the peak phase error will increase due to the noise. So if the loop is not to lose lock on these noise peaks the peak allowable error due to modulation must be reduced to something less, on the order of 40° to 50°.

LOCKING

Initially, a loop is unlocked and the VCO is running at some frequency. If a signal is applied to the input, locking may or may not occur depending on several things.

If the signal is within the bandwidth of the loop filter, locking will occur without a beat note being generated or any cycles being skipped. This frequency is given by

$$\Delta\omega_L = \frac{K_o K_D \tau_2}{\tau_1 + \tau_2} \approx 2\zeta\omega_n \qquad (24)$$

If the frequency of the input signal is further away from the VCO frequency, locking may still occur, with a beat note being generated. The greatest frequency that can be pulled in is called the ''pull in frequency'' and is found from the approximation

$$\Delta\omega_P \approx \sqrt{2}\left(2\zeta\omega_n K_o K_D - \omega_n^2\right)^{1/2} \qquad (25)$$

which works well for moderate and high gain loops $(\omega_n/K_oK_D < 0.4)$.

An approximate expression for pull in time (the time required to achieve lock from some frequency offset $\Delta\omega$) is given by:

$$T_P \approx \frac{(\Delta\omega)^2}{2\zeta\omega_n^3}$$

A MONOLITHIC PHASE LOCKED LOOP

A complete phase locked loop has been built on a monolithic integrated circuit. It features a very linear voltage controlled oscillator and a double balanced phase detector.

A simplified schematic of this voltage controlled oscillator is shown in *Figure 12*. Q_2 is a voltage controlled current source whose collector current is a linear function of the control voltage e_f. Initially Q_5 is OFF and the collector current of Q_2 passes through D_2 and changes C in a linear fashion. The voltage across C is therefore a ramp, and continues to increase until Q_7 is turned ON; this turns OFF Q_8, causing Q_9 and Q_{11} to turn ON. This in turn turns ON Q_5. With Q_5 ON, the anode of D_1 is clamped close to $-V_{CC}$ and D_2 stops conducting, since its cathode is more positive than its anode.

All of the current supplied by Q_2 is diverted through D_1 and Q_3, which sets up an equal current in Q_4. This current is supplied by the charged capacitor C (which now discharges linearly), causing the voltage across it to decrease. This continues until a lower trip point is reached and Q_7 turns OFF and the cycle repeats. Due to the matching of Q_3 and Q_4, the charge current of C is equal to the discharge current and therefore the duty cycle is very nearly 50%. *Figure 13* shows the wave forms at (1) and (2).

Figure 14 shows the double balanced phase detector and amplifier used in the microcircuit. Transistors Q_1 through Q_4 are switched with the output of the VCO, while the input

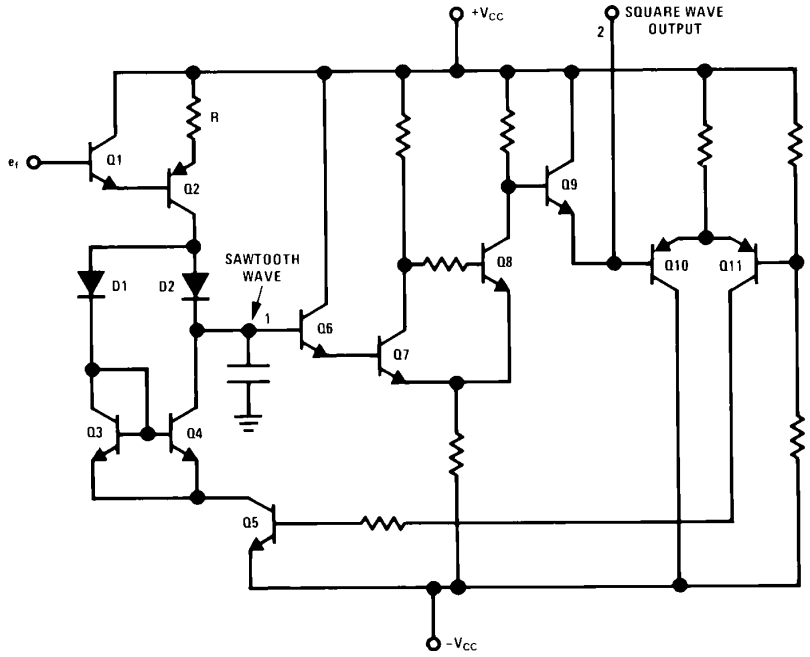

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FIGURE 12. Simplified Voltage Controlled Oscillator

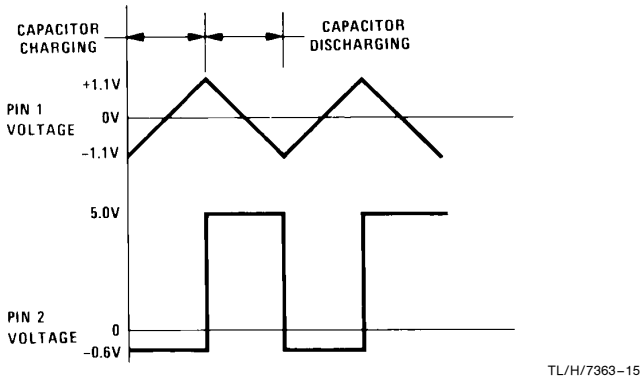

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FIGURE 13. VCO Waveforms

signal is applied to the bases of Q_5 and Q_6. The output current in resistors R_3 and R_4 is then proportional to the difference in phase between the VCO output and the input; the ac component of this current will be at twice the frequency of the VCO due to the full wave switching action transistors Q_1 through Q_4. The waveforms of *Figure 15* illustrate how the phase detector works. Diodes D_1 and D_2 serve to limit the peak to peak amplitude of the collector voltage. The output of the phase detector is further amplified by Q_{10} and Q_{11}, and is taken as a voltage at pin 7.

R_8 serves as the resistive portion of the loop filter, and additional resistance and capacitance may be added here to fix the loop bandwidth. For use as an FM demodulator, the voltage at pin 7 will be the demodulated output; since the dc level here is fairly high, a reference voltage has been provided so that an operational amplifier with differential input can be used for additional gain and level shifting.

The complete microcircuit, called the LM565, is shown in *Figure 16*.

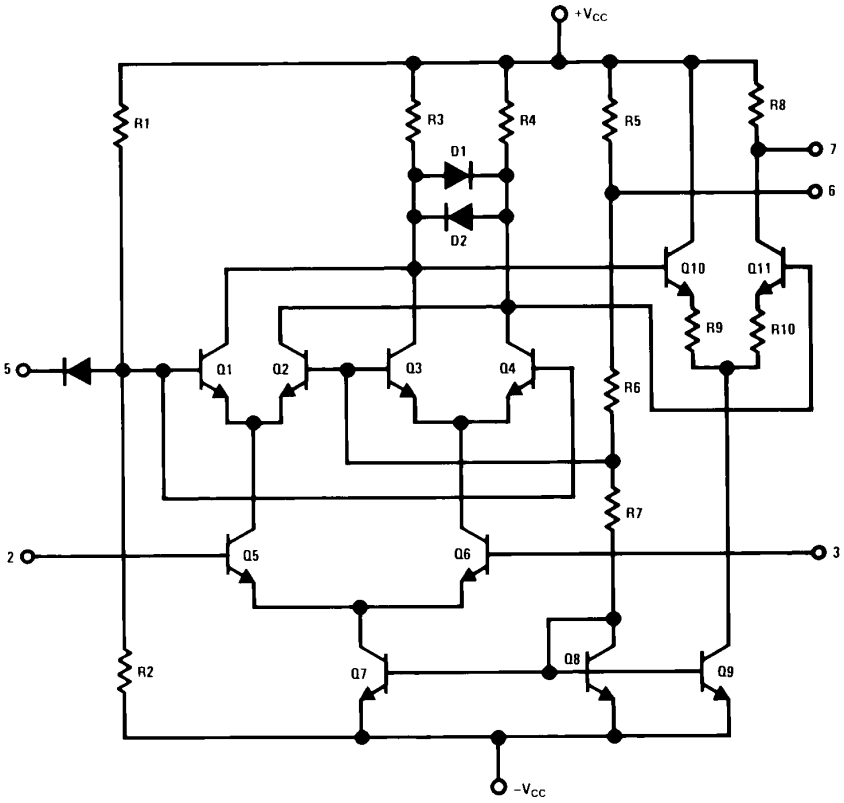

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FIGURE 14. Phase Detector and Amplifier

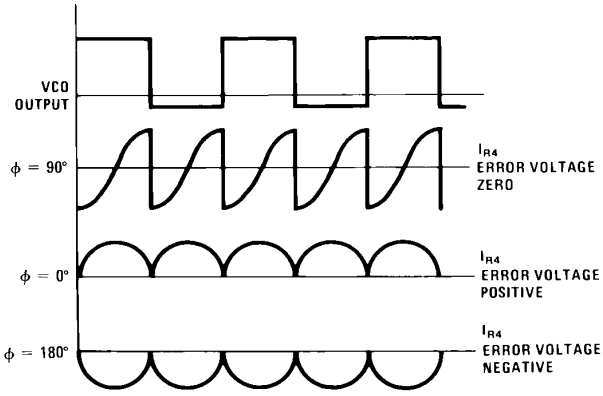

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FIGURE 15. Phase Detector Waveforms, Showing Limit Cases for Phase Shift between Input and VCO Signals

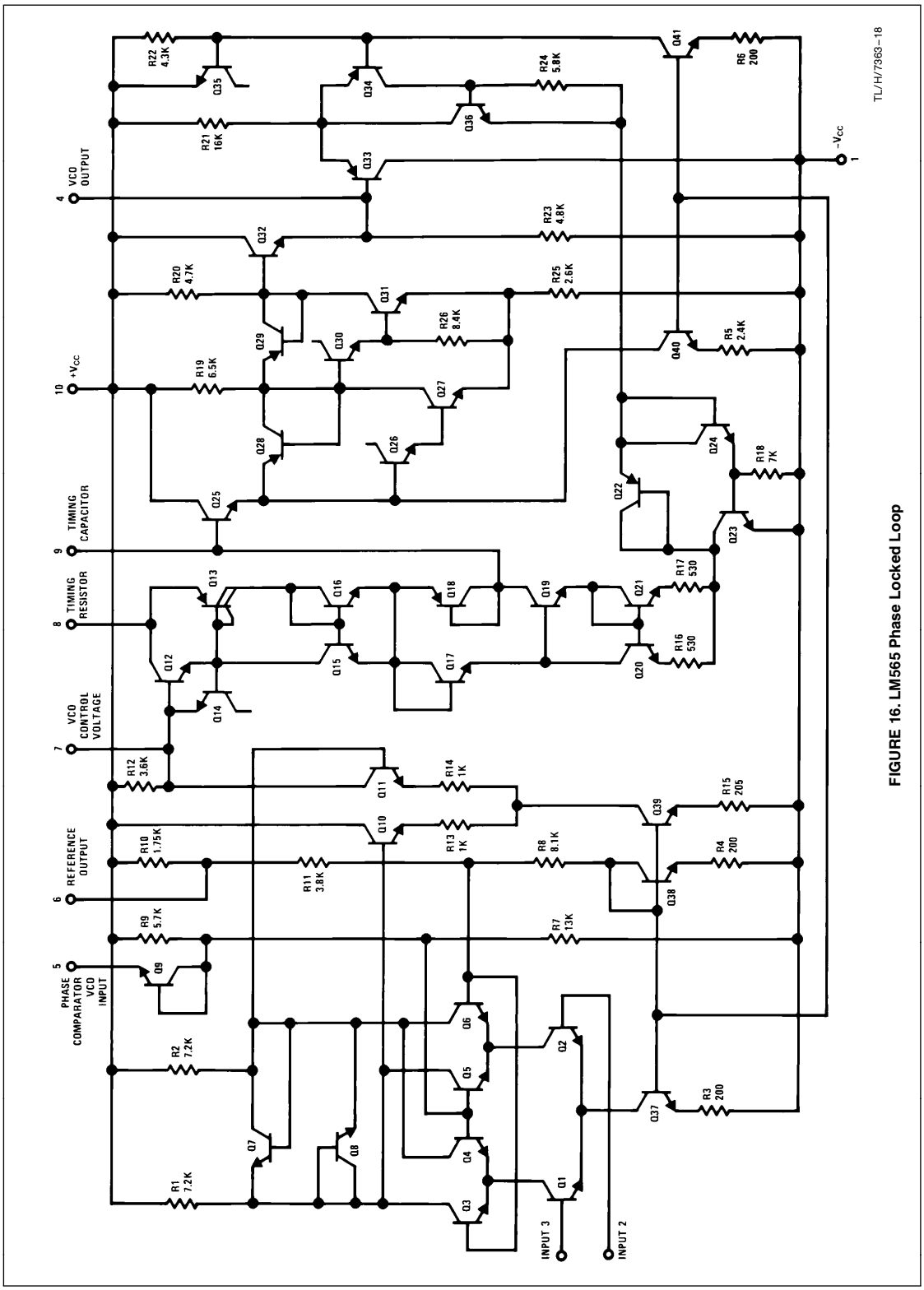

FIGURE 16. LM565 Phase Locked Loop

USING THE LM565

Some of the important operating characteristics of the LM565 are shown in the table below ($V_{CC} = \pm 6V$, $T_A = 25°C$).

Phase Detector	
Input Impedance	5 kΩ
Input Level for Limiting	10 mV
Output Resistance	3.6 kΩ
Output Common Mode Voltage	4.5V
Offset Voltage (Between pins 6 and 7)	100 mV
Sensitivity K_D	.68V/rad
Voltage Controlled Oscillator	
Stability	
Temperature	200 ppm/°C
Supply Voltage	200 ppm/%
Square Wave Output Pin 4	5.4 V_{pp}
Triangle Wave Output Pin 9	2.4 V_{pp}
Maximum Operating Frequency	500 kHz
Sensitivity K_o	4.1 f_o rad/sec/V (f_o: osc, freq. in Hz)
Closed Loop Performance	
Loop Gain K_oK_D	2.8 f_o/sec
Demod. Output, ±10% Deviation	300 mV
(A 0.001 μF capacitor is needed between pins 7 and 8 to stop parasitic oscillations).	

To best illustrate how the LM565 is used, several applications are covered in detail, and should provide insight into the selection of external components for use with the LM565.

IRIG CHANNEL DEMODULATOR

In the field of missile telemetry, it is necessary to send many channels of relatively narrow band data via a radio link. It has been found convenient to frequency modulate this information on a set of subcarriers with center frequencies in the range of 400 Hz to 200 kHz. Standardization of these frequencies was undertaken by the Inter-Range Instrumentation Group (IRIG) and has resulted in several sets of subcarrier channels, some based on deviations that are a fixed percentage of center frequency and other sets that have a constant deviation regardless of center frequency. IRIG channel 13 has been selected as an example to demonstrate the usefulness of the LM565 as an FM demodulator.

IRIG Channel	13
Center Frequency	14.5 kHz
Max Deviation	±7.5%
Frequency Response	220 Hz
Deviation Ratio	5

Since with a deviation of ±10%, the LM565 will produce approximately 300 mV peak to peak output, with a deviation of 7.5% we can expect an output of 225 mV. It is desirable to amplify and level shift this signal to ground so that plus and minus output votages can be obtained for frequency shifts above and below center frequency.

An LM107 can be used to provide the necessary additional gain and the level shift. In *Figure 17*, R_4 is used to set the output at zero volts with no input signal. The frequency of the VCO can be adjusted with R_3 to provide zero output voltage when an input signal is present.

The design of the filter network proceeds as follows:

It is necessary to choose ω_n such that the peak phase error in the loop is less than 90° for all conditions of modulation. Allowing for noise modulation at low levels of signal to noise, a desirable peak phase error might be 1 radian or 57 degrees, leaving a 33 degree margin for noise. Assuming sinusoidal modulation, *Figure 6* can be used to estimate the peak normalized phase error. It will be necessary to make several sample calculations, since the normalized phase error is a function of ω_n.

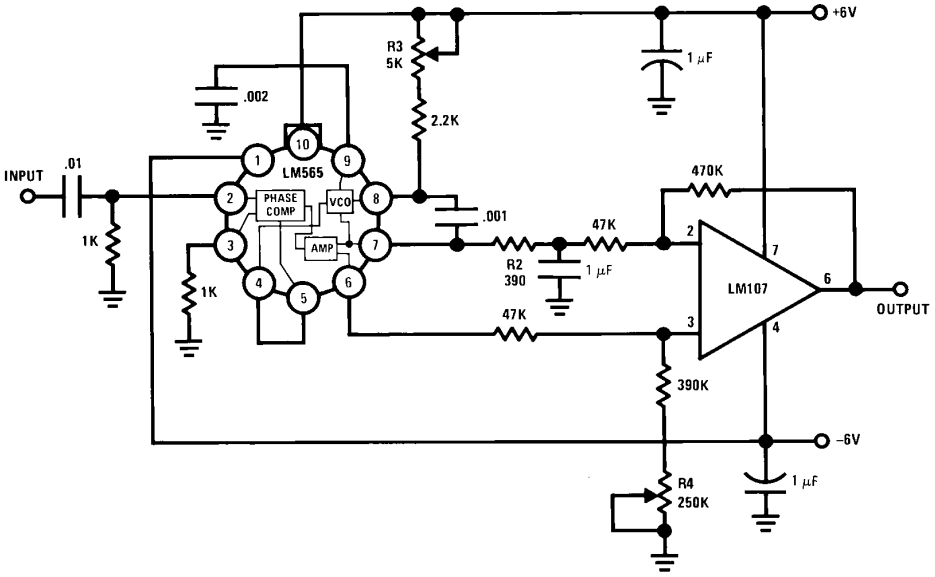

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FIGURE 17. IRIG Channel 13 Demodulator

Selecting a worst case of $\omega_n/\omega_m = 1$, $\omega_n = 2\pi \times 220$ Hz; selecting a damping factor of 0.707,

$$\frac{\theta}{\Delta\omega/\omega_n} = 0.702$$

or

$$\theta_e = 0.702\,\frac{\Delta\omega}{\omega_n} = 0.702\,\frac{2\,\pi \times 1088\ \text{Hz}}{2\,\pi \times 220\ \text{Hz}} = 3.45\ \text{radians}$$

this is unacceptable, since it would throw the loop out of lock, so it is necessary to try a higher value of ω_n. Let $\omega_n = 2\pi$x 500 Hz, then $\omega_m/\omega_n = 0.44$, and

$$\theta_e = 0.44\,\frac{\Delta\omega}{\omega_n} = 0.44 \times \frac{2\,\pi \times 1088}{2\,\pi \times 500} = 0.95\ \text{radians}$$

this should be a good choice, since it is close to 1 radian. Operating at 14.5 kHz, the LM565 has a loop gain K_oK_D of

$$2.28 \times 14.5 \times 10^3 = 33 \times 10^3\ \text{sec}$$

the value of the loop filter capacitor, C_1, can be found from *Figure 4*:

$$\tau_1 + \tau_2 = 3.5 \times 10^{-3}\ \text{sec}$$

from *Figure 5*, the value of τ_2 can be found (for a damping factor of 0.707)

$$\tau_2 = 4.4 \times 10^{-4}\ \text{sec}$$

$$\tau_1 = (35 - 4.4) \times 10^{-4}\ \text{sec} = 31.4 \times 10^{-4}\ \text{sec}$$

$$C_1 = \frac{\tau_1}{R} = \frac{31.4 \times 10^{-4}\ \text{sec}}{3.6\ \text{k}\Omega} \cong 1\ \mu\text{F}$$

$$R_2 = \frac{4.4 \times 10^{-4}\ \text{sec}}{1 \times 10^{-6}\ \mu\text{F}} = 440\Omega$$

Looking at *Figure 10*, the noise bandwidth B_L can be estimated to be

$$B_L = 0.6\,\omega_n = 0.6 \times 3150\ \text{rad/sec} = 1890\ \text{Hz}$$

the complete circuit is shown in *Figure 17*. Measured performance of the circuit is summarized below with a fully modulated signal as described above and an input level of 40 mVrms:

f 3 dB	200
ζ	0.8
Output Level	770 mVrms
Distortion	0.4%
Signal to Noise at verge of loss of lock (bandwidth of noise = 100 kHz)	−8.4 dB

It will be noted that the loop is capable of demodulating signals lower in level than the noise; this is not in disagreement with earlier statements that loss of lock occurs at signal to noise ratios of approximately +6 dB because of the bandwidths involved. The above number of −8.4 dB signal to noise for threshold was obtained with a noise spectrum 100 kHz wide. The noise power in the loop will be reduced by the ratio of loop noise bandwidth to input noise bandwidth

$$\frac{B_{LOOP}}{B_{INPUT}} = \frac{1890\ \text{Hz}}{100\ \text{kHz}} = 0.02\ \text{or}\ -17\ \text{dB}$$

the equivalent signal to noise in the loop is −8.4 dB +17 dB = +8.6 dB which is close to the above-mentioned limit of +6 dB. It should also be noted that loss of lock was noted with full modulation of the signal which will degrade threshold somewhat (although the measurement is more realistic).

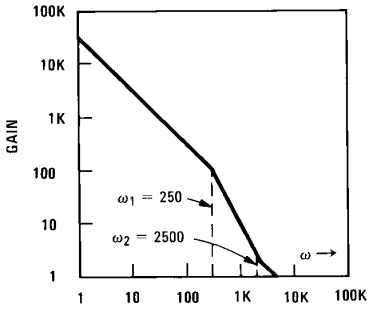

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FIGURE 18. Bode Plot for Circuit of *Figure 17*

FSK DEMODULATOR

Frequency shift keying (FSK) is widely used for the transmission of Teletype information, both in the computer peripheral and communications field. Standards have evolved over the years, and the commonly used frequencies are as follows:

a)	mark	2125	Hz
	space	2975	Hz
b)	mark	1070	Hz
	space	1270	Hz
c)	mark	2025	Hz
	space	2225	Hz

(a) is commonly used as subcarrier tones for radio Teletype, while b) and c) are used as carriers for data transmission over telephone and land lines.

As a design example, a demodulator for the 2025 Hz and 2225 Hz mark and space frequencies will be discussed.

Since this is an FM system employing square wave modulation, the natural frequency of the loop must be chosen again so that peak phase errors do not exceed 90° under all conditions. *Figure 7* shows peak phase error for a step in frequency; if a damping factor of 0.707 is selected, the peak phase error is

$$\frac{\theta_e}{\Delta\omega/\omega_n} = 0.45$$

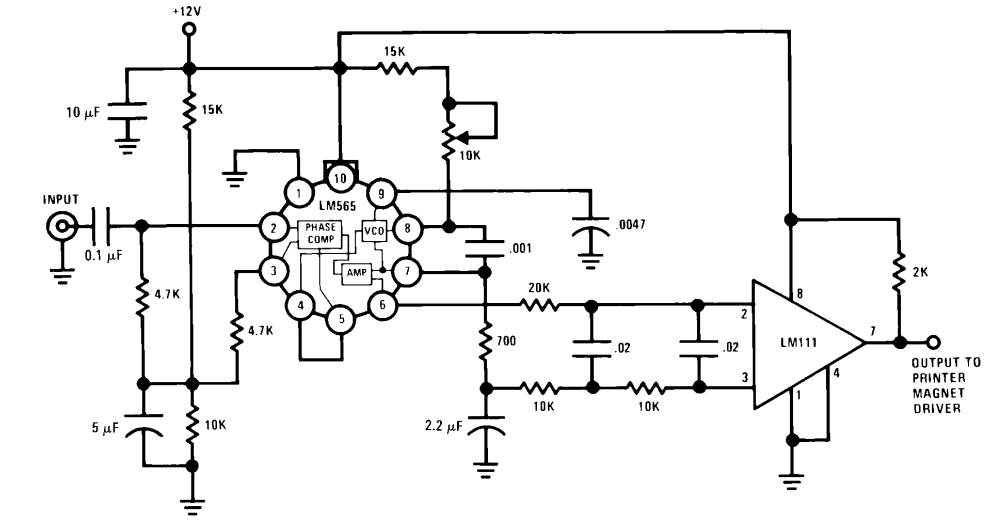

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FIGURE 19. FSK Demodulator (2025–2225 cps)

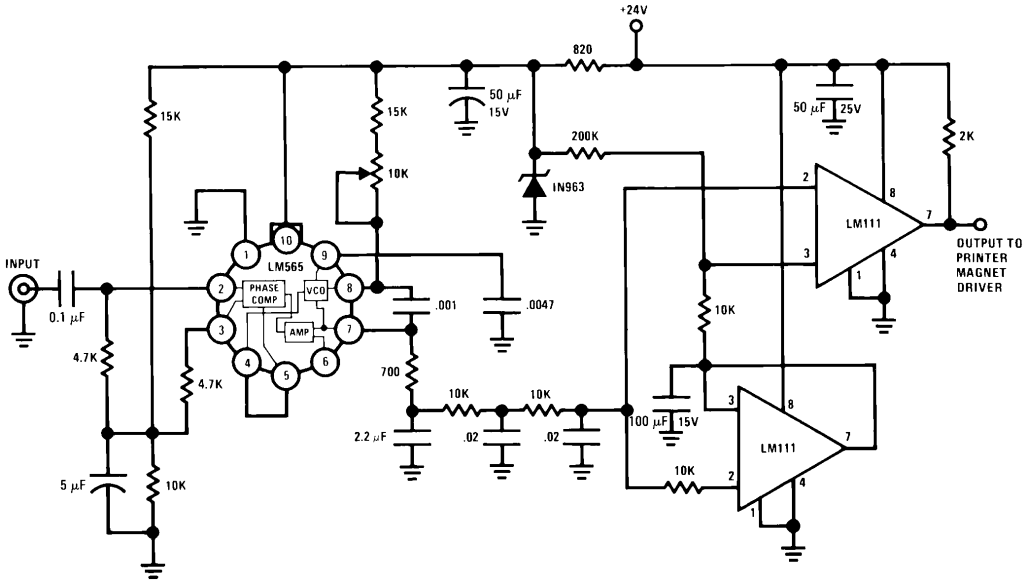

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FIGURE 20. FSK Demodulator with DC Restoration

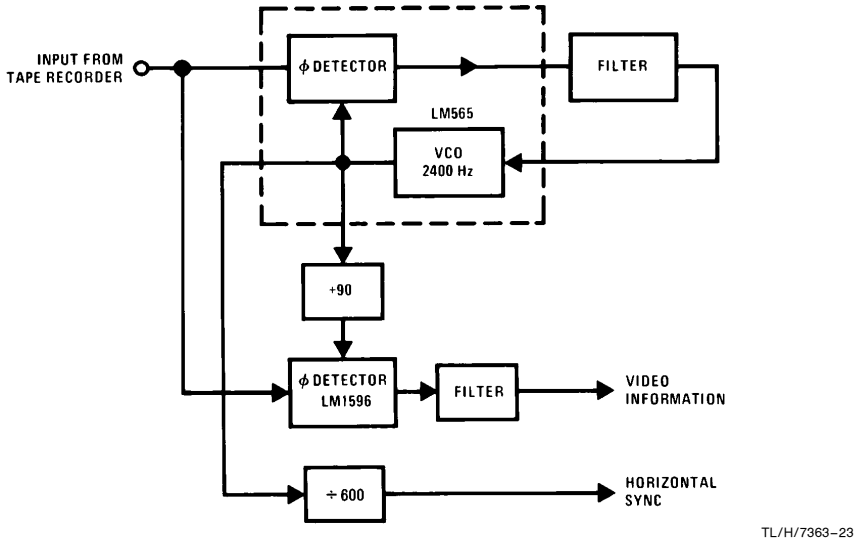

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FIGURE 21. Block Diagram of Weather Satellite Demodulator

or

$$\theta_e = 0.45 \frac{\Delta\omega}{\omega_n}$$

$$\omega_n = 0.45 \frac{\Delta\omega}{\theta_e}$$

in our case, $\Delta\omega = 2\pi \times 200$ Hz $= 1250$, if $\theta_e = 1$ radian,

$$\omega_n = 0.45 \frac{1250 \text{ rad/sec}}{1 \text{ radian}} = 500 \text{ rad/sec}$$

$$f_n = 80 \text{ Hz}$$

The final circuit is shown in *Figure 19*. The values of the loop filter components ($C_1 = 2.2\ \mu F$ and $R_1 = 700\Omega$) were changed to accommodate a keying rate of 300 baud (150 Hz), since the values calculated above caused too much roll off of a square wave modulation signal of 150 Hz. The two 10k resistors and 0.02 μF capacitors at the input to the LM111 comparator provide further filtering of the carrier, and hence smoother operation of the circuit.

A problem encountered with this simple demodulator is that of dc drift. The frequency must be adjusted to provide zero volts to the input of the comparator so that with modulation, switching occurs. Since the deviation of the signal is small (approximately 10%), the peak to peak demodulated output is only 150 mV. It should be apparent that any drift in frequency of the VCO will cause a dc change and hence may lock the comparator in one state or the other. A circuit to overcome this problem is shown in *Figure 20*. While using the same basic demodulator configuration, an LM111 is used as an accurate peak detector to provide a dc bias for one input to the comparator. When a ''space'' frequency is transmitted, and the output at pin 7 of the LM565 goes negative and switching occurs, the detected and filtered voltage of pin 3 to the comparator will not follow the change. This is a form of ''dc restorer'' circuit: it will track changes in drift, making the comparator self compensating for changes in frequency, etc.

WEATHER SATELLITE PICTURE DEMODULATOR

As a last example of how a phase locked loop can be used in communications systems, a weather satellite picture demodulator is shown. Weather satellites of the Nimbus, ESSA, and ITOS series continually photograph the earth from orbits of 100 to 800 miles. The pictures are stored immediately after exposure in an electrostatic storage vidicon, and read out during a succeeding 200 second period. The video information is AM modulated on a 2.4 kHz subcarrier which is frequency modulated on a 137.5 MHz RF carrier. Upon reception, the output from the receiver FM detector will be the 2.4 kHz tone containing AM video information. It is common practice to record the tone on an audio quality tape recorder for subsequent demodulation and display. The 2.4 kHz subcarrier frequency may be divided by 600 to obtain the horizontal sync frequency of 4 Hz.

Due to flutter in the tape recorder, noise during reception, etc., it is desirable to reproduce the 2.4 kHz subcarrier with a phase locked loop, which will track any flutter and instability in the recorder, and effectively filter out noise, in addition to providing a signal large enough for the digital frequency divider. In addition, an in phase component of the VCO signal may be used to drive a synchronous demodulator to detect the video information. A block diagram of the system is shown in *Figure 21*, and a complete schematic in *Figure 22*.

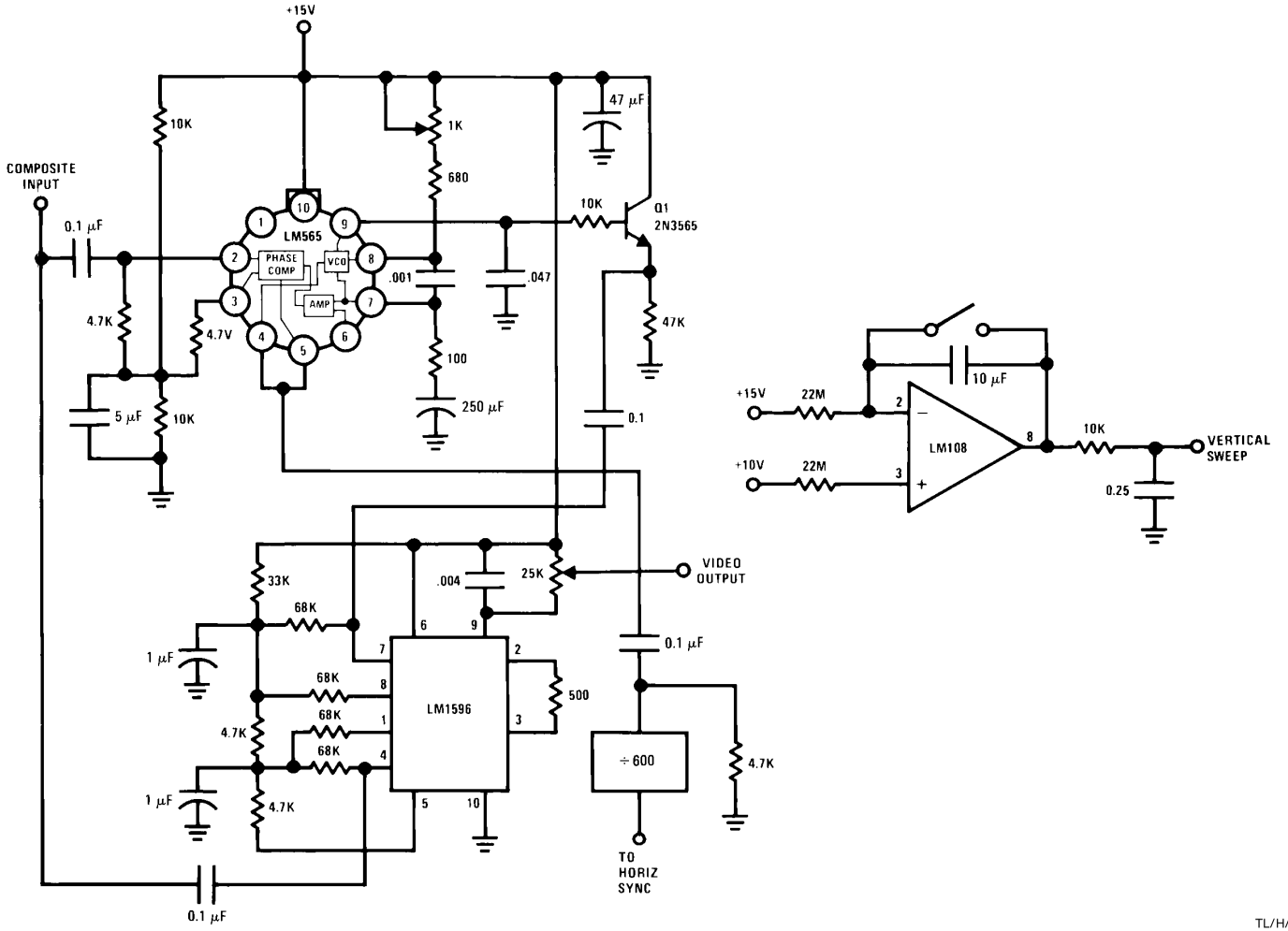

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FIGURE 22. Weather Satellite Picture Demodulator

The design of the loop parameters was based on the following objectives

$$f_n = 10 \text{ Hz}, \omega_n = 75 \text{ rad/sec}$$

$$B_L = 40 \text{ Hz (from } \textit{Figure 10}\text{)}$$

the complete loop filter, calculated from *Figures 4* and *5*, is shown in *Figure 22*. When the loop is in lock and the free running frequency of the VCO is 2.4 kHz, the VCO square wave at pin 4 of the 565 will be in quadrature (90°) with the input signal; however, the zero crossings of the triangle wave across the timing capacitor will be in phase, and if their signal is applied to a double balanced demodulator, such as an LM1596, switching will occur in the demodulator in phase with the 2.4 kHz subcarrier. The double balanced demodulator will produce an output proportional to the amplitude of the subcarrier applied to its signal input. An emitter follower, Q_1, is used to buffer the triangle wave across the timing capacitor so excessive loading does not occur.

The demodulated video signal from the LM1596 is taken across a 25k potentiometer and filtered to a bandwidth of 1.4 kHz, the bandwidth of the transmitted video. Depending on the type of display to be used (oscilloscope, slow scan TV monitor, facsimile reproducer), it may be necessary to further buffer or amplify the signal obtained. If desired, another load resistor may be used between pin 6 and VCO to obtain a differential output; an operational amp could then be used to provide more gain, level shift, etc.

A vertical sweep circuit is shown using an LM308 low input current op amp as a Miller rundown circuit. The values are chosen to produce an output voltage ramp of −4.5V/220 sec, although this may be adjusted by means of the 22 meg. charging resistor. If an oscilloscope is used as a readout, the horizontal sync can be supplied to the trigger input with the sweep set to provide a total sweep time of something less than 250 ms. A camera is used to photograph the 200 second picture.

SUMMARY AND CONCLUSIONS

A brief review of phase lock techniques has been presented and several design tools have been presented that may be useful in predicting the performance of phase locked loops.

A phase locked loop integrated circuit has been described and several applications have been given to illustrate the use of the circuit and the design techniques presented.

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3. Andrew Viterbi, ''Principles of Coherent Communication'', *McGraw-Hill*, 1966.

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