MM58167B Real Time Clock Design Guide

National Semiconductor
Application Note 353
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The MM58167B is a real-time 24-hour format clock with input/output structure and control lines that facilitate interfacing to microprocessors. It provides a reliable source of calendar data from milliseconds through months, as well as 6 bytes plus 2 nibbles of RAM, which are available to the user if the alarm (compare) interrupt is not used. The MM58167B features low power consumption (typically 4.5 microamperes at 3-volt supply) during battery backed mode, flexible interrupt structure (alarm and repetitive), and a fast internal update rate (1 kHz). Systems utilizing this device include, personal computers, process control, security, and data acquisition.

This application note covers hardware interface to microprocessors, clock interrupts, oscillator operation, accuracy, calibration techniques, software, and battery back-up considerations.

Hardware Description Overview

1.0 *Figure 1* is a functional block diagram of the MM58167B. It can be subdivided into the following sections:

1.1 Oscillator

The oscillator consists of an internal inverter to which the user connects a 32.768 kHz crystal, bias resistor and capacitors, to form a Pierce parallel resonant circuit.

1.2 Prescaler

The prescaler divides the 32.768 kHz oscillator down to 1 kHz using pulse swallowing techniques. The 1 kHz pulse rate is the incrementing signal for the timekeeping counters.

Block Diagram

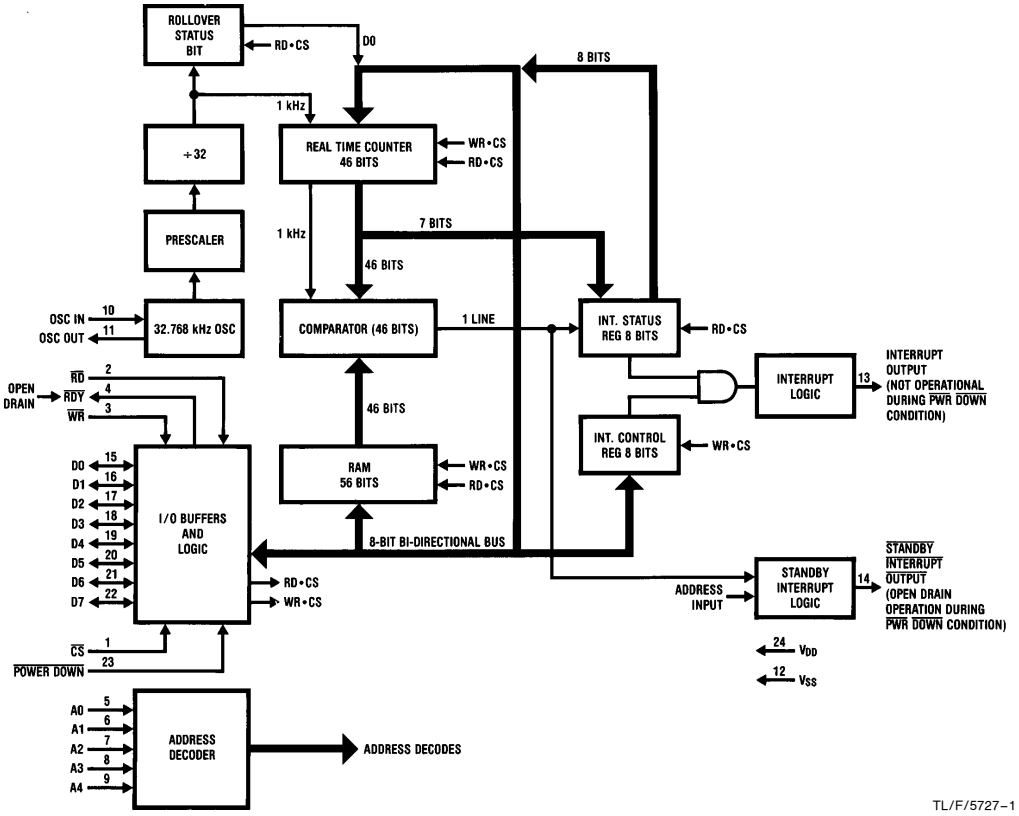

FIGURE 1

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Hardware Description Overview (Continued)

1.3 Timekeeping Counters

The timekeeping section consists of a 14-stage BCD counter, each stage having read/write capability. The counters keep time in a 24-hour format. *Figure 6* shows the counter detail of calendar-date-time format.

1.4 Rollover Status

A rollover status bit (read only) informs the user that invalid data may have been read, due to the counters being incremented during a counter read or between successive counter reads. This situation occurs because the counters are clocked asynchronously with respect to the microprocessor.

1.5 RAM

14 nibbles of RAM are provided for alarm (compare) interrupt or general storage. The nibbles are packed 2 per address except for 2 locations, address 08 and 0D (HEX). The nibble at address 08 appears in the high order 4 bits, while the nibble at address 0D appears in the low order 4 bits. See memory map *Figure 2* for details.

Address In HEX	D7 D6 D5 D4	D3 D2 D1 D0
8	Milliseconds	No RAM Exists
9	Tenths of Seconds	Hundredths of Seconds
A	Tens of Seconds	Units of Seconds
B	Tens of Minutes	Units of Minutes
C	Tens of Hours	Units of Hours
D	No RAM Exists	Day of Week
E	Tens Day of Month	Units Day of Month
F	Tens of Months	Units of Months

FIGURE 2. RAM Memory Map

1.6 Comparator

A 46-bit comparator compares values in RAM against the counters to provide an alarm (compare) interrupt. When a compare occurs, the main interrupt will be activated if the D0 bit of the interrupt control register was set. The standby interrupt will be activated if a ''1''was written to address 16 hex.

1.7 Interrupt Hardware

Interrupt hardware consists of two interrupt outputs. The main interrupt and the standby interrupt. The main interrupt is an active high push-pull output. The standby interrupt is an active low open drain output. For the main interrupt, an 8-bit control register allows the user to select from 1 to 7 interrupt rates, as well as an alarm. An 8-bit status register informs the user which of the 8 interrupts occurred. A one-bit control register enables/disables the standby interrupt. The standby interrupt is activated only for the alarm condition. A 46-bit comparator matches the timekeeping counters against RAM for the alarm interrupt.

1.8 Input/Output and Control Lines

The input/output structure consists of a 5-bit address bus and 8-bit bidirectional data bus. The control lines are chip select, power down, read and write. In addition, a ready output is provided for those microprocessors that have wait-state capability and meet the timing requirements of the ready signal. The power down input acts as a chip select of opposite polarity. It differs from the chip select in that it will TRI-STATE® the main interrupt output while the chip select does not TRI-STATE the interrupt. The power down input is intended to facilitate deselecting the chip for battery backed operation. Chip select, read and write are active low controls. The ready output is active low open drain and is caused by chip select and the negative-going-edge of read or write (it is an internal one-shot). If the ready output is not used as a control line when interfacing to a microprocessor, it may be left open circuit.

Detail Descriptions

OSCILLATOR

Figure 3 represents the internal and external circuitry that comprise the oscillator. The inverter, which is the heart of the oscillator, is designed to consume minimum power. The inverter has a typical gain of 30 at 1 kHz and 4 at 30 kHz. The oscillator input may be driven from an external source. If this is desired, the input should swing rail-to-rail and be approximately a 50% duty cycle. The oscillator output pin is open circuit for this case. The external oscillator circuit may be constructed using a CMOS inverter or N-FET (see *Figures 4a* and *4b*). Referring to *Figure 3*, the external 20 MΩ resistor biases the inverter in its active region. The internal feedback resistor may be too large in value to guarantee reliable biasing.

The external series resistor is to protect the crystal from being overdriven and possibly damaged. Manufacturers of these crystals specify maximum power that the crystal can dissipate. It is this rating which determines what value of series resistor should be used. The two external capacitors are effectively in series with each other (from an A.C. viewpoint). This total value comprises the load capacitance (typically 9 to 13 picofarad) specified by the crystal manufacturer at the crystal's oscillating frequency. The rule of thumb in choosing these capacitors is:

$$1/\text{load capacitance} = 1/C1 + 1/C2$$

C2 is greater than C1 (typically two to four times)

C1 is usually trimmed to obtain the 32768 Hertz frequency.

The start-up time of this oscillator may vary from two to seven seconds (empirical observation) and is due to the high ''Q'' of the crystal. Typical waveform values monitored at the oscillator output are observed to be 3 volts peak to peak riding on a 2.5 volt D.C. level (for $V+ = 5$ volts).

CHOOSING THE CRYSTAL

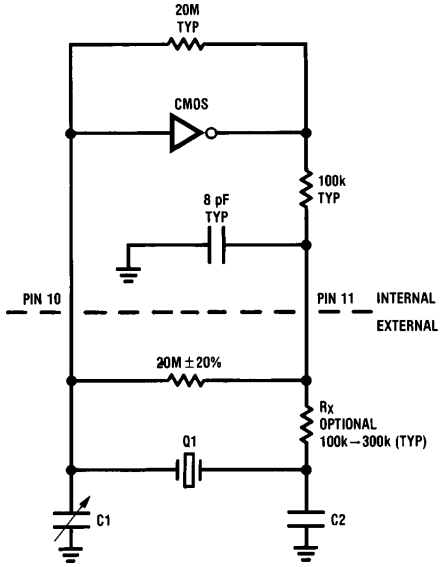
The below parameters describe the crystal to be used

Parallel Resonant, tuning fork (N cut) or XY Bar

$Q > = 35{,}000$

Load Capacitance (CL)	9 to 13 Picofarad
Power Rating	20 Microwatt Max.
Accuracy	User Choice
Temperature Coefficient	User Choice

Detail Descriptions (Continued)



Q1 = 32,768 Hz

Mnfg.	Tel.#
RCD	800-228-8108
Saronix	415-856-6900
Reeves-Hoffman	717-243-5929

C1 = 5 ⟶ 30 pf
Circuit Specialists
Part# 275-0430-005
Tel.# 1-800-528-1417
Johanson #9613 or #9410-3 pc.
Tel.# 201-334-2676
C2 = 15 ⟶ 20 pf mica

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FIGURE 3. Oscillator Circuit and Recommended Connections

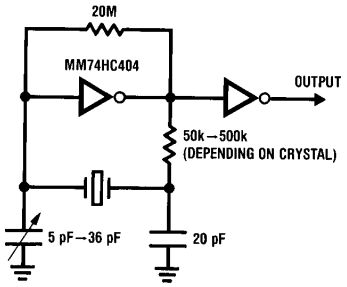

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FIGURE 4a

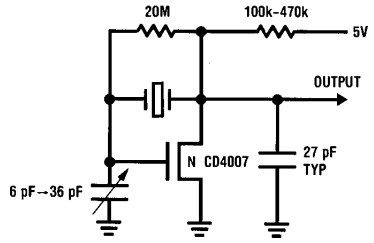

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FIGURE 4b

When used with a crystal, the accuracy of the oscillator circuit over voltage and temperature is about +/− 10 PPM. Voltage variations cause about 50% of the inaccuracy and temperature variations account for the other half. This inaccuracy results in an error of about 5 minutes per year. Errors due to external components must be taken into account by the user. If an external oscillator is used, then it determines the accuracy of the clock. The oscillator input pin (pin 10), is a high impedance node that is susceptible to 'noise'. The usual result is the clock gains time at a high rate (on the order of seconds per hour or greater). This noise is usually the result of coupling from pin 9 which is a low order address bit if tied directly to a microprocessor bus. Suggestions to alleviate this condition are:

1. Gate pin 9 with chip select.
2. Use a slow rise and fall time non inverting buffer such as a CMOS to drive pin 9. If this choice is made, similar CMOS should drive the write and read strobes to avoid timing conflicts.
3. Use an external oscillator and drive pin 10 with a low impedance device (CMOS or transistor), leave pin 11 open circuit.
4. Connect all oscillator components as close as possible to pins 10 and 11.

CALIBRATION

To calibrate the oscillator the following method is suggested. The one second repetitive interrupt is activated. This is done by first connecting the interrupt (pin 13) of the clock to the interrupt of the microprocessor. Next a short program is written that sets bit D2 of the interrupt control register, and then enters a loop that wastes time while awaiting an interrupt. The interrupt service routine only needs to read the interrupt status register, which clears the interrupt, and then returns. The result is a 1 second periodic signal at pin 13.

The flow chart of *Figure 5* is an example of the detail steps. A time event meter is used to measure the time interval between successive positive going edges of the interrupt output while adjusting the variable capacitor C1. This period will be 1 second when the oscillator is at 32,768 Hertz.

Detail Descriptions (Continued)

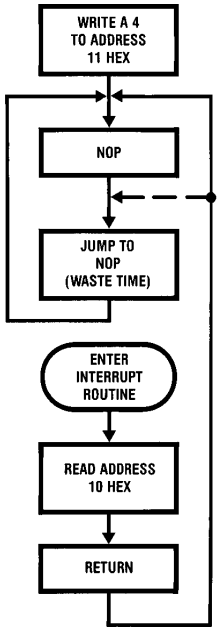

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FIGURE 5. Flow Chart for Calibration Using the 1 Hz Repetitive Interrupt

If the 32,768 Hertz is to be measured directly, then a HI impedance LO capacitance amplifier or comparator or CMOS gate should be connected to the oscillator output pin to prevent the measuring instrument from offsetting the frequency of the oscillator. This addition is permanently a part of the oscillator circuit and must be battery backed if the clock is battery backed. The reason for battery backing this buffer is to ensure that its input impedance does not change during the power down operation which could result in the oscillator stopping or being offset in frequency.

PRESCALER OPERATION

The 32,768 Hertz signal is divided to an even 32,000 Hertz using pulse swallowing techniques. This is accomplished by dropping three pulses every 128 counts of the 32,768 Hertz signal. The resulting 32 kHz is then divided to produce 1 kHz which is the internal incrementer for the rest of the timekeeper. This 1 kHz waveform is nonmonotonic with respect to individual periods. As a result, there are 750 short and 250 long periods within a one second interval.

The short period is 1/1024 seconds, and the long period is [1/1024 + 3/32768] seconds. As a result, the milliseconds, hundredths and tenths of seconds ''jitter''. The inaccuracy on an individual period basis is about 91 microseconds. The period and number of clock edges are correct over one second within the accuracy of the crystal oscillator. The ten thousandths of seconds counter referred to in the data sheet counts milliseconds. The 1 second and slower signals are jitter free. Refer to *Figure 6* for counter block diagram.

TIMEKEEPING COUNTERS

The timekeeping counters are intended to work with valid BCD values. In general, if illegal codes are entered then no guarantee is given for recovery. As shown in *Figure 6*, the timekeeping stages are arranged as a ripple counter. The month, day of month, and day of week counters count 1 through N. The milliseconds through hours counters count 0 through N. The rollover of a counter stage increments the next higher order counter. This rollover takes place when the highest allowed value plus one is decoded. For example, in a 30-day month, the day of month counter would decode the value 31, reset to one and increment the month counter. If the highest allowed value plus one is written to a counter, the counter will reset when the write is removed and ''may'' increment the next higher order counter.

For example, if February 29 is written to the clock, the read back will be a ''1'' in the day of month counter and the month may read ''3''. However, for leap year use, February 31 may be written. If this is done on Mar 1 at 0 (hours through milliseconds), then the clock will read March 1 after 24 hours. In this way, the value Feb 31 could be used as an indication that the date is really Feb 29. Refer to *Figures 7A 7B,* and *7C* for flowcharts of a program and alarm interrupt bit map that take leap year into account. Note that the software implemented leap year counter is accurate at least through the year 2048. For a perpetual calendar, a more sophisticated algorithm would be needed.

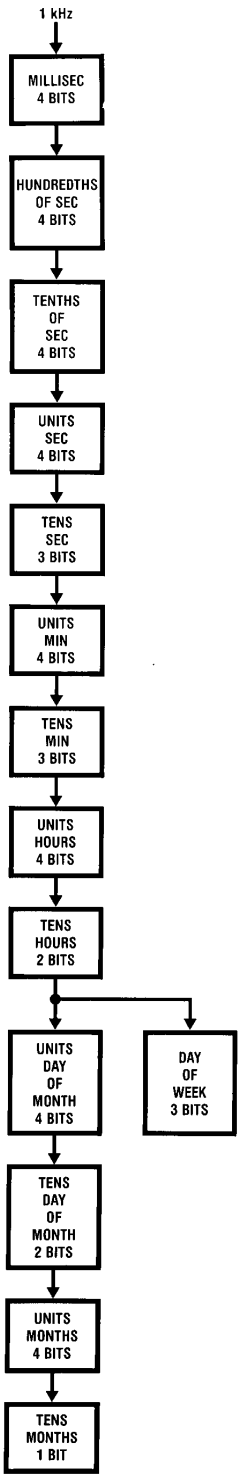

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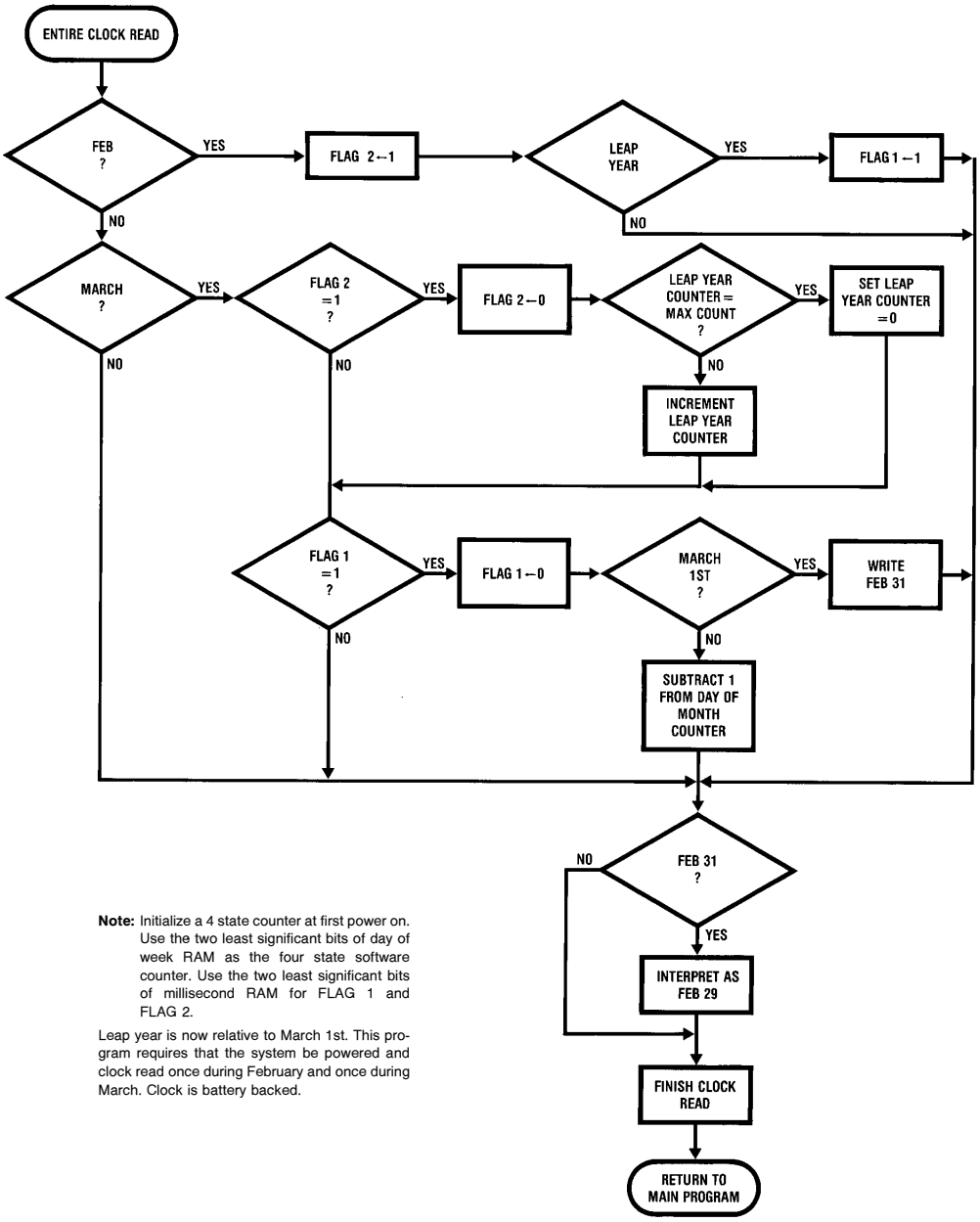
FIGURE 6. BCD Timekeeping Counters



Note: Initialize a 4 state counter at first power on. Use the two least significant bits of day of week RAM as the four state software counter. Use the two least significant bits of millisecond RAM for FLAG 1 and FLAG 2.

Leap year is now relative to March 1st. This program requires that the system be powered and clock read once during February and once during March. Clock is battery backed.

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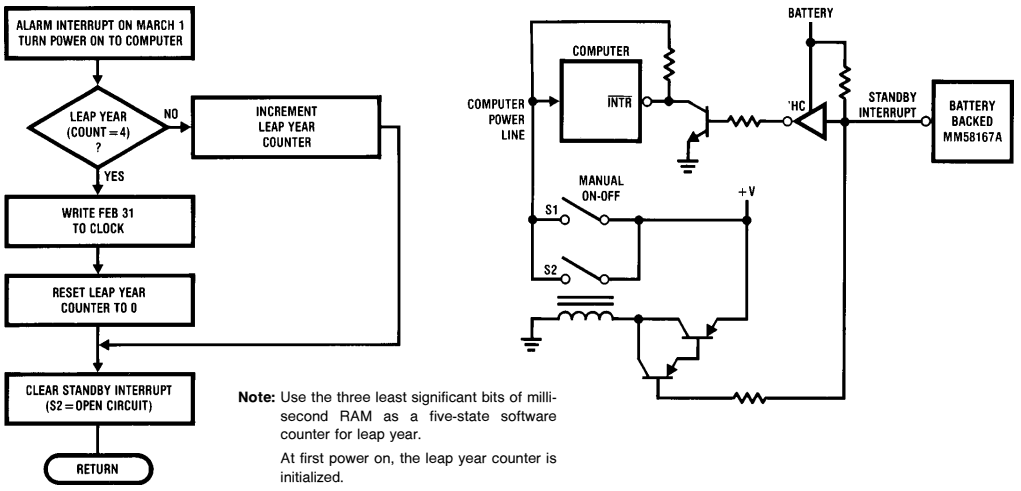
FIGURE 7A. Leap Year Flow Chart



Note: Use the three least significant bits of milli-second RAM as a five-state software counter for leap year.

At first power on, the leap year counter is initialized.

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FIGURE 7B. Leap Year Flow Chart and Hardware

Function	Address					DATA							
						Hi Nibble				Lo Nibble			
	4	3	2	1	0	7	6	5	4	3	2	1	0
Milliseconds	0	1	0	0	0	0	0	0	0	No RAM Exists			
Hundredths and Tenths of Seconds	0	1	0	0	1	0	0	0	0	0	0	0	0
Seconds	0	1	0	1	0	0	0	0	0	0	0	0	0
Minutes	0	1	0	1	1	0	0	0	0	0	0	0	0
Hours	0	1	1	0	0	0	0	0	0	0	0	0	0
Day of Week	0	1	1	0	1	No RAM Exists				1	1	X	X
Day of Month	0	1	1	1	0	0	0	0	0	0	0	0	1
Months	0	1	1	1	1	0	0	0	0	0	0	1	1

FIGURE 7C. Clock RAM Bit Map For Alarm Interrupt on March 1@ 0 Hrs

INTERRUPTS

The MM58167B has two interrupt output pins. The main interrupt (pin 13) is active ''high'', and is active when the power down pin is ''high''. When power down (pin 23) is low, the main interrupt output is TRI-STATE. The second interrupt is the ''standby interrupt'' and is an active low open drain requiring a pull up resistor to VDD. This interrupt is always powered. Refer to *Figure 8* for typical sink current versus voltage out characteristics. Separate control bits exist for the two interrupts. The main interrupt offers two modes of operation which may be combined. Mode 1 is the interactive repetitive interrupt. For this case, a logic 1 is written to one or more bits in the control register (address 11 hex) from D1 through D7, a logic 0 is written into the D0 position. Refer to *Figure 9* for bit configuration of the interrupt control and status registers.

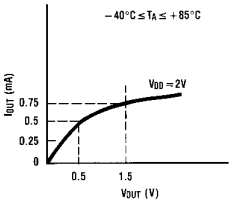

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FIGURE 8. Typical Curve of I vs V of Standby Interrupt

As a result, the clock chip provides an interactive repetitive interrupt, that occurs when the selected counter rolls over. That is, the user must clear the interrupt so the next one can be recognized. This is done by reading the interrupt status register (address 10 hex). This read results in the user obtaining the interrupt status (which interrupt occurred) and the clearing of the interrupt output as well as the status register. It is the positive-going-edge of the read strobe which causes the preceding. This clearing action precludes polling the status register. For precision timing, the positive-going-edge of the repetitive interrupt should be used as a trigger. The one-per-second through one-per-month repetitive interrupts will be as accurate as the setting of the crystal oscillator. The ten-per-second interrupt will be accurate to about 91 microseconds. Refer to prescaler description for more detail.

The second mode of main interrupt is the ''compare'' or ''alarm''. In this case, a specific value is entered in the RAM of the clock. When the time keeping counter(s) match that value, the interrupt becomes active. Refer to *Figure 11* for a typical example. *Figures 9* and *10* show internal interrupt logic and waveforms. In addition to a specific one time interrupt (alarm), a repetitive interrupt can be achieved by reprogramming the selected RAM location with a future event value. The rule of thumb for an ''alarm'' interrupt is: All nibbles of higher order than specified are set to C hex (always compare). All nibbles lower than specified are set to ''zero''.

A programming example of the fastest interrupt rate obtainable (500 per second) is given in *Figure 12*. This program written in NSC800™ code (Z80) sets ''always compare'' conditions (CC hex) in RAM locations 9 through C, E and F. RAM location D which corresponds to the day of the week counter (a single digit), is set to C. RAM location 8 is set to 0. When the first interrupt occurs, the service routine reads the status register and sets the value 2 into RAM location 8. At succeeding interrupts, the values 4, 6, 8 are set into location 8 and the sequence repeats.

If an interrupt is activated and the interrupt occurs during battery backed operation (power down), the main interrupt output will be active high when system power returns.

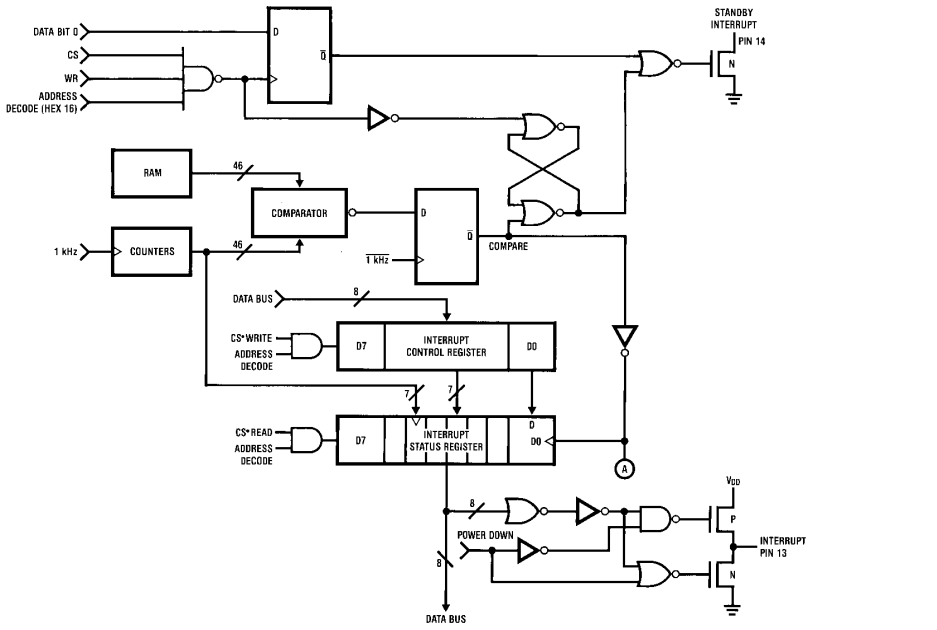

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FIGURE 9. Interrupt Registers and Logic

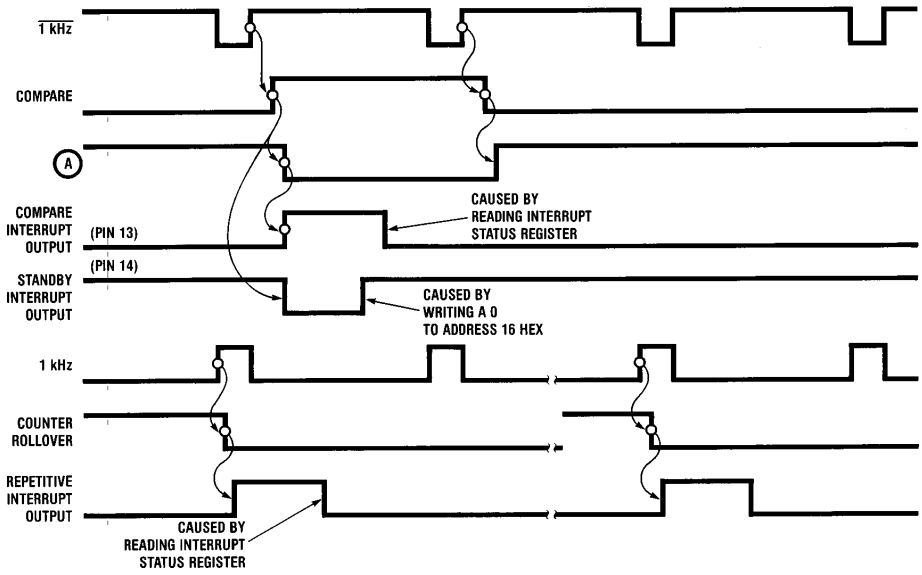

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FIGURE 10. Internal Interrupt Timing

Function	Address					DATA							
						Hi Nibble				Lo Nibble			
	4	3	2	1	0	7	6	5	4	3	2	1	0
Milliseconds	0	1	0	0	0	0	0	0	0	No RAM Exists			
Hundredths and Tenths of Seconds	0	1	0	0	1	0	0	0	0	0	0	0	0
Seconds	0	1	0	1	0	0	0	0	0	0	0	0	0
Minutes	0	1	0	1	1	0	0	1	0	0	0	1	0
Hours	0	1	1	0	0	0	0	0	1	0	0	0	0
Day of Week	0	1	1	0	1	No RAM Exists				1	1	X	X
Day of Month	0	1	1	1	0	1	1	X	X	1	1	X	X
Months	0	1	1	1	1	1	1	X	X	1	1	X	X

FIGURE 11. Ram Mapping for Alarm Interrupt at 10:22:00 Every Day

```
                NAME ('I500Hz')
                TITLE 58167 500HZ REPETITIVE INTERRUPT (10/13/83)

                ;THIS PROGRAM IS FOR USE WITH THE 58167 POWER DOWN BOARD
                ;INTERFACED TO THE NSC888 BOARD. CODE IS NSC800.
                ;A 500HZ SIGNAL IS GENERATED AT THE INTERRUPT PIN (13).
                ;THIS SIGNAL IS GENERATED USING THE COMPARE INTERRUPT
                ;AND UPDATING THE ''RAM'' FOR THE NEXT INTERRUPT


                                        ORG 0800H

4092                            RESET EQU 04092H
4091                            CONT  EQU 04091H
4090                            STAT  EQU 04090H
408F                            MON   EQU 0408FH
408E                            DOM   EQU 0408EH
408D                            DOW   EQU 0408DH
408C                            HRS   EQU 0408CH
408B                            MIN   EQU 0408BH
408A                            SEC   EQU 0408AH
4089                            HT    EQU 04089H
4088                            MIL   EQU 04088H
101C                            VEC1  EQU 0101CH
101D                            VEC2  EQU 0101DH


0800'   3E 00                    INIT:   LD      A,0             ;SET UP INTRPT FOR NSC888
0802'   32 101C                            LD      (VEC1),A        ;         *
0805'   3E 09                              LD      A,009H          ;         *
0807'   32 101D                            LD      (VEC2),A        ;         *
080A'   3E 08                              LD      A,8             ;         *
080C'   D3 BB                              OUT     (0BBH),A        ;         *
080E'   31 1FFF                            LD      SP,01FFFH       ;INIT STACK POINTER
0811'   3E FF                              LD      A,0FFH
0813'   32 4092                           LD      (Reset),A       ;RESET ALL CLOCK COUNTERS
0816'   3E 00                              LD      A,0
0818'   32 4091                           LD      (CONT),A        ;CLEAR INTRPT CONTROL
081B'   3A 4090                           LD      A,(STAT)        ;CLEAR ANY PENDING INTRPT
081E'   3E CC                              LD      A,0CCH          ;SET RAM FOR INTRPT
0820'   32 408F                           LD      (MON),A
0823'   32 408E                           LD      (DOM),A
0826'   32 408D                           LD      (DOW),A
0829'   32 408C                           LD      (HRS),A
082C'   32 408B                           LD      (MIN),A
082F'   32 408A                           LD      (SEC),A
0832'   32 4089                           LD      (HT),A
0835'   3E 00                              LD      A,0
0837'   32 4088                           LD      (MIL),A
083A'   3E 01                              LD      A,1
083C'   32 4091                           LD      (CONT), A        ;SET COMPARE INTRPT
083E'   FB                                EI
0840'   00                      NOP:    NOP
0841'   C3 0840                          JP      NOP             ;WASTE TIME AWAITING
                                                                ;INTERRUPT
                                ;INTERRUPT SERVICE ROUTINE GETS THE VALUE IN THE
                                ;MILLISECOND RAM, TEST FOR 8. IF YES THEN SET RAM
                                ;EQUAL TO 0, CLEAR INTERRUPT AND RETURN.
                                ;IF NO, ADD 2 TO RAM MILLISECOND,
                                ;CLEAR INTERRUPT AND RETURN.
                                ;''REMEMBER'' RAM MILLISECONDS IS ''HIGH'' ORDER NIBBLE
                                ;ONLY

                                        ORG 0900H

0900'   3A 4088                    LD      A,(MIL)                 ;GET RAM MILLSEC
0903'   E6 F0                      AND     0F0H                    ;MASK
0905'   FE 80                      CP      080H                    ;? RAM=8
0907'   CA 0912'                   JP      Z,ZERO
090A'   C6 20                      ADD     A,020H
090C'   32 4088                    LD      (MIL),A
090F'   C3 0917'                   JP      RETRN
0912'   3E 00            ZERO:   LD      A,0
0914'   32 4088                    LD      (MIL),A
0917'   3A 4090           RETRN: LD      A,(STAT)                ;CLEAR INTRPT
091A'   FB                        EI
091B'   C9                        RET

                                        END
```

FIGURE 12. NSC800 Assembly Code for 500 Hz Interrupt

STANDBY INTERRUPT

A ''1'' written to address 16 hex enables the standby interrupt and a ''0'' disables it. This interrupt also becomes active when a match exists between time keeping counter(s) and a value written into RAM. The standby interrupt can be cleared as soon as it is recognized. The user should ensure that a delay of one millisecond or greater exists prior to reenabling the standby interrupt. This delay is necessary because of the internal signal level which causes the interrupt. If this delay does not occur, then the standby interrupt becomes reactivated until the internal latched compare goes away, which occurs at the next 1 kHz clock. *Figure 10* illustrates interrupt timing.

RAM

RAM is organized as shown in *Figure 2*. There are 4 bits of RAM for each BCD counter. The RAM may be used as general purpose or for an alarm interrupt. It is possible under certain conditions to perform the compare interrupt and use selected bits of the RAM for general purpose storage. Any RAM position that is set for the 'always compare' condition allows the user to manipulate the 2 LO order bits in each nibble. However, the 2 high order bits in each nibble position must be maintained as logic 1'S. For example, the user may have an alarm interrupt that does not use the day of the week as a condition for interrupt. Therefore the 2 low order bits might be used as a 4 state software counter to keep track of leap year. Reading and writing the RAM is the same as any standard RAM.

HARDWARE INTERFACE CONSIDERATIONS

There are four basic methods of interfacing the MM58167B to a microprocessor. They are memory mapped, microprocessor ports (for single chip microprocessors like the 8048), peripheral adapter, and separate latches. The advantage of memory mapped interface is use of all memory reference instructions. The disadvantages are the processor may need to be ''wait-stated'' and the environment is noisier with respect to the crystal oscillator. Refer to *Figure 13* for typical bus interface.

Microprocessors that have separate ports (16 are sufficient) offer the capability to interface directly without ''wait-stating'', or additional device count. Eight of the port bits (data) need to be bidirectional for this interface. *Figure 14* indicates port interface. Programmable peripheral interface devices such as the 8255A or NSC810 afford the user the advantage of timing control by data bit manipulation, as well as a less noisy environment with respect to the oscillator circuit. *Figure 15* depicts the 8255A and NSC810 interface.

External latches may be used in place of the programmable peripheral interface device. This results in higher package count but easier troubleshooting. Also, the latches do not have to be manipulated through a control register. *Figure 16* illustrates the external latch approach. For the peripheral approaches, address, data, chip select, read and write strobes are manipulated by controlling the data bus bits via program execution. The peripheral interface approach facilitates calibration of the oscillator because the chip select, read strobe, and address lines can be set to steady state logic levels. Refer to calibration techniques for more detail.

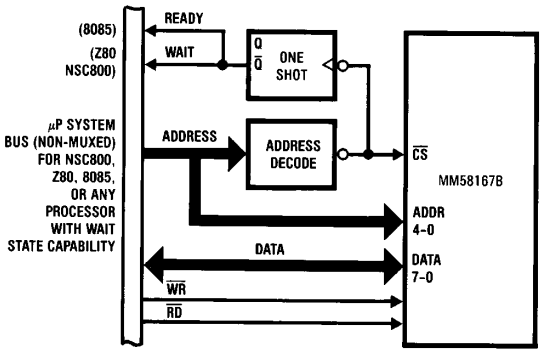

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FIGURE 13. Typical μP Bus Interface

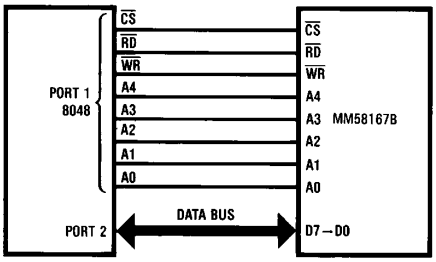

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FIGURE 14. MM58167B Interfaced to Single Chip Microcomputer

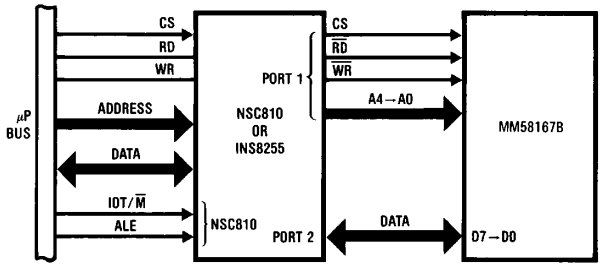

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FIGURE 15. MM58167B Interfaced to μP Through Peripheral Adapter

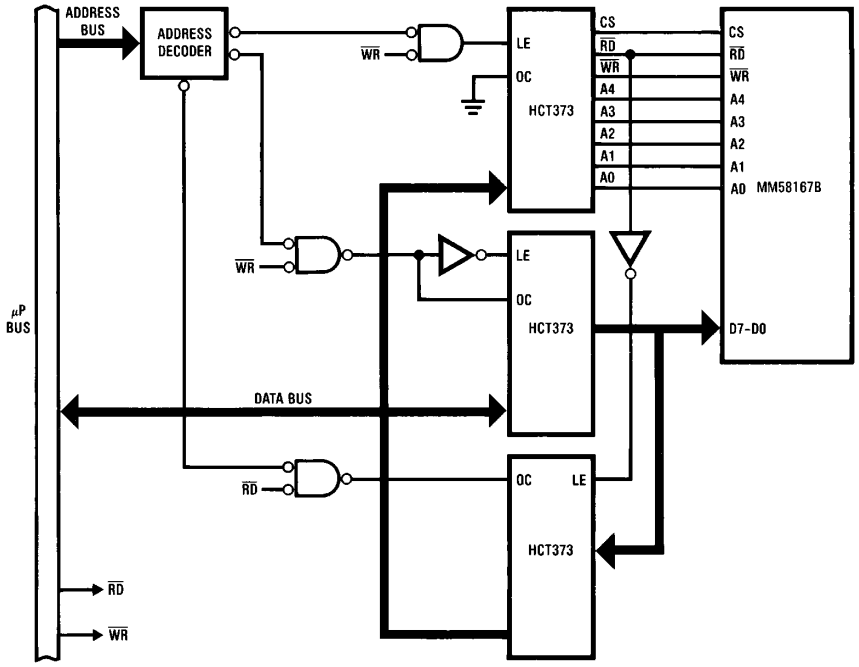

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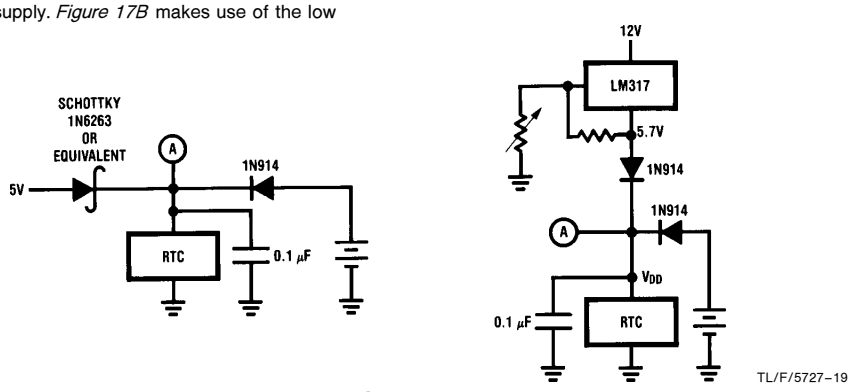
FIGURE 16. MM58167B Interfaced to μp Using TRI-STATE Latches

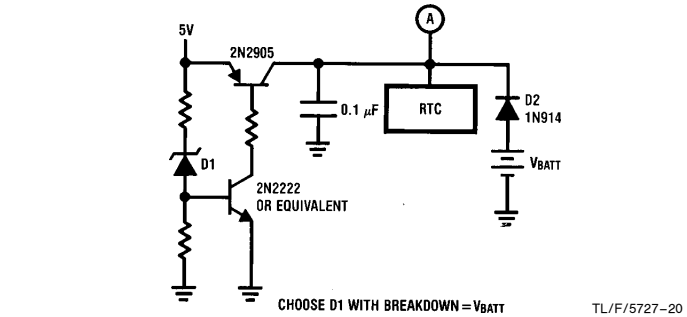
POWER DOWN/BATTERY BACKED CONSIDERATIONS

Battery back up of the clock may be considered by the user to maintain time during power failure, provide a ''wake-up'' alarm, save the time that power failure occurred, calculate how long power failure lasted. The first step in providing a battery backed system is to isolate the system supply from the battery. This is to ensure that the battery is not discharged by the system supply when power failure occurs. *Figure 17* shows two techniques to achieve isolation. *Figure 17A* is implemented using diodes to isolate. In one case a Schottky diode is used to guarantee minimum voltage drop loss, while in the other case an adjustable voltage regulator (LM317) is used from a higher voltage and regulated to about 5.7 volts. A 1N914 diode in series with the regulator achieves the 5 volts for the clock. The Schottky diode has a drop of about 0.3 volts. Thus the V+ of the clock is typically at 4.7 volts. The user must be cautious about input signals not exceeding the 4.7 volt V+, since the clock is a CMOS device. This situation could arise if the devices driving the inputs of the clock were CMOS and received power from the 5 volt system supply. *Figure 17B* makes use of the low saturation of a PNP transistor (0.1 volt) to take care of the above situation. The NPN transistor is used to achieve isolation. The zener diode ensures that the circuit stops conducting and appears open circuit before the battery switches in.

Some basic considerations must be adhered to in a power down situation where the real time clock is battey backed. One is to ensure no spurious write strobes accompanied by a chip select occur during power down or power up. Another is to guarantee the system is stable when selecting/deselecting the clock. Also, any legitimate write-in-progress should be completed. To accomplish this, hardware is implemented such that early power failure is detected (usually a comparator detects DC failure, a retriggerable one-shot detects AC failure) See *Figures 18* and *19*. At this point the clock chip is deselected. The worst case is the power fails faster than the detection circuit can cause deselection. When power returns, the hardware detects power on, but the system must be stable before communication is allowed with the real-time-clock.



A



B

FIGURE 17. Isolating System Supply from Battery

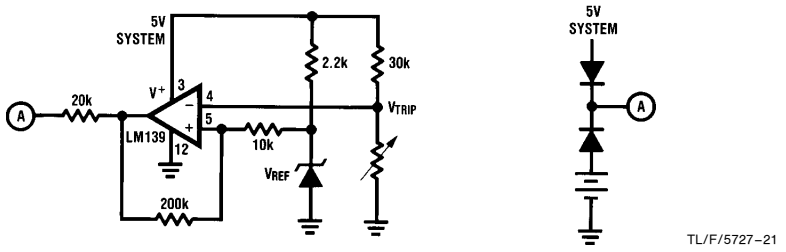


FIGURE 18. Sensing D.C. Failure Using a Comparator

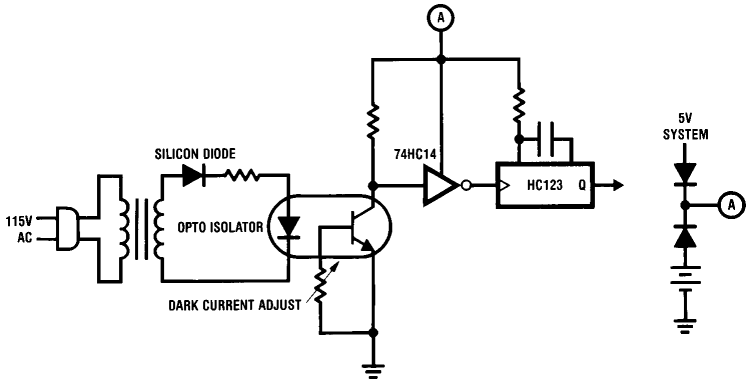


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FIGURE 19. Sensing AC Line Failure Using Retriggerable One Shot

The 5-volt system supply rise and fall time characteristics during power turn on and power failure must be known. Care should be taken to allow a legitimate write in progress to be completed. This is necessary because a ''short write'' could cause erroneous data to be entered to the clock. If the clock is used as a ''read only'' device (except for initialization of calendar and time), the circuitry to allow a write in progress to be completed does not have to be considered. For this situation, a switch in series with the write strobe could be implemented such that the write line to the clock is ''tied high'' after initialization.

To sense system DC power failure a comparator and voltage reference may be used. *Figure 20*, detail 1, shows the comparator and voltage reference configured such that the comparator output is ''low'' when 5-volt system power is greater than 4.6 volts. If possible, the power fail trip point should be referenced to a lightly loaded (fast collapse) DC supply, preferably higher than the 5-volt system. This would allow early sense of power failure. When using comparators, the output may oscillate as the trip point is approached. The oscillation is caused by noise on the DC line appearing at the input to the comparator when at or near the trip voltage. The cleaner the supply, the less chance of oscillation. In all cases, hysteresis should be used to minimize oscillations. Note that the 20 kohm pull-up resistor is connected to the battery backed node, while the LM139 V+ pin is connected to the 5-volt system supply. Used this way, the comparator does not draw any current except leakage from the battery and the output remains high during power down.

To sense AC failure, a retriggerable one-shot may be used. The RC time out may be adjusted to allow for one or more cycles of 60 Hertz to be missed. Using this approach, the Q output of the one-shot is always high while 60 Hertz is present. When a cycle is missed the one-shot times out and Q goes low. *Figure 19* shows AC sensing. This technique could cause a spurious deselect of the clock if a ''glitch'' occurs on the AC line resulting in a missed cycle.

For this application, the circuit shown in *Figure 20* was implemented. The MM58167B was interfaced to the NSC800 in memory mapped locations. A demo program was written to exercise the clock, and display time, date and calendar. Power was switched on and off at irregular intervals, to test the battery backed circuitry. The results were that the clock kept correct time. Battery backed current for all circuitry was 10 microamp. For general consideration, this circuitry allows a chip select in progress to be completed.

FUNCTIONAL OPERATION OF *FIGURE 22*

Power up sequencing consists of the LM139 (comparator) making a high to low transition when the 5-volt system supply exceeds 4.6 volts. This transition triggers the 0.5 second one-shot causing its output to be low and removes the low reset on the D flip-flop through nand gate J. The output of the 2 microsecond one-shot is ''don't care'' once the comparator switches from high to low. After 0.5 seconds, the system is assumed to be stable, and the D flip-flop output which was reset is clocked high by the low to high transition of the 0.5 second one-shot. Thus, the clock chip is enabled allowing normal communication with the microprocessor.

The power down sequence consists of the comparator making a low to high transition when the 5-volt supply is less than 4.6 volts. If no chip select is present, the D flip-flop is reset through nand gate J, causing pin 23 of the clock to be low (deselected). If a legitimate chip select was in progress, the reset action through nand gate J would be delayed by the low level of the 2-microsecond one-shot.

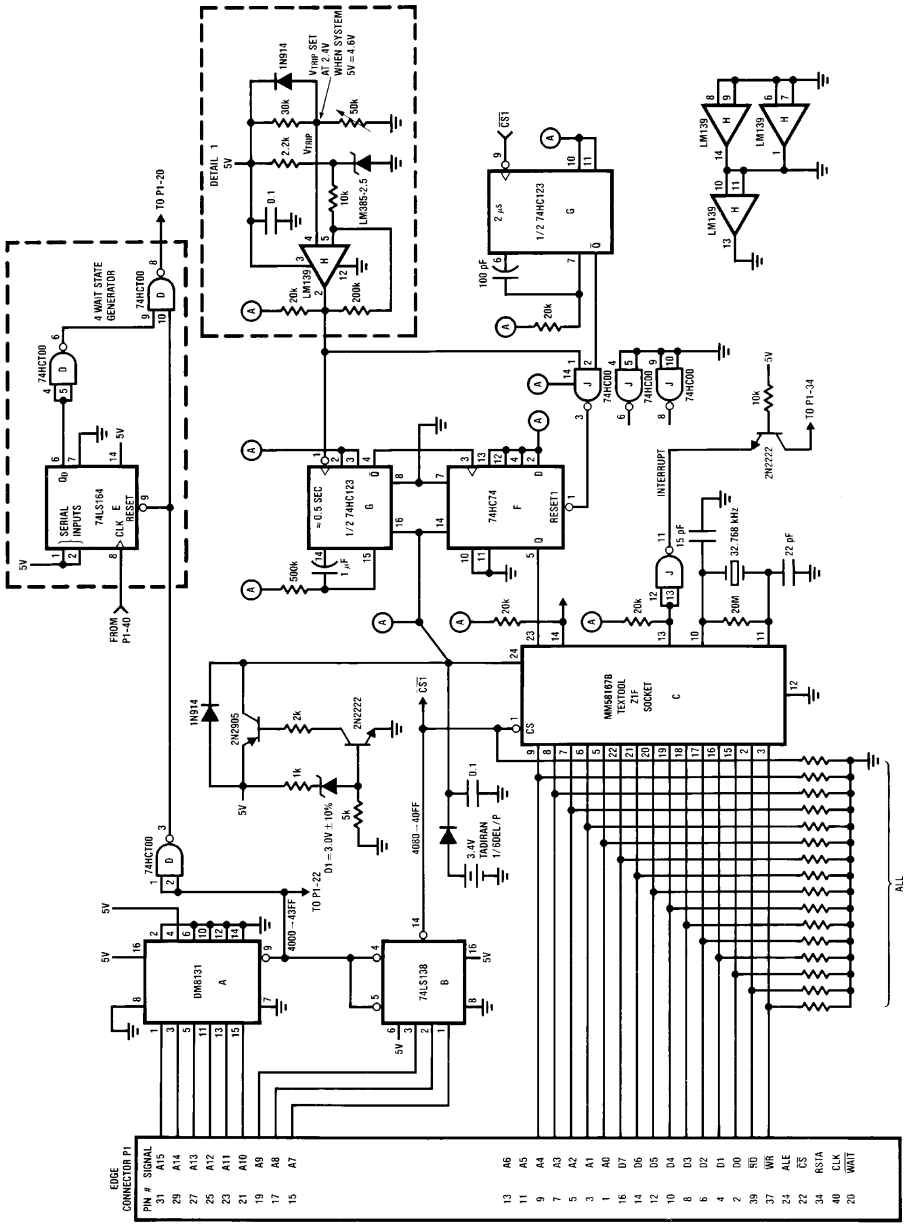

FIGURE 20. Detailed Schematic of Power Down Circuitry, and Interface to NSC888 Board

A wait state generator was implemented using the chip select as the sensing signal. This was necessary to comply with NSC800 wait state timing. The wait generator provides 2 microseconds of access time, which is more than adequate to meet clock chip timing requirements. Pull-down resistors were added to all clock input pins to guarantee no floating inputs during power down. This ensures that the CMOS clock does not draw excessive current from the battery during power down. A diode isolates 5-volt system from the battery (A 3.4-volt Tadiran nonrechargeable lithium cell was used in this application). The battery is isolated from the 5-volt supply using a circuit comprised of PNP and NPN transistors along with a zener diode. The zener diode value was selected such that the combined voltage drop of the zener and the base emitter of the NPN transistor was greater than the battery voltage. This ensures no current will be drawn from the battery by the 5-volt supply when power failure occurs.

The battery is non rechargeable, but allows up to 10 microamps of charge current without damaging the cell. An LM139 voltage comparator and LM385-2.5 voltage reference were used to sense the 5-volt system supply. The trip point was adjusted such that when the 5-volt supply dropped to 4.6 volts, the comparator switched from low to high. Observation of the comparator output showed oscillation, but caused no malfunction. The duration of the oscillation was about 100 microseconds. Burst noise on the 5-volt supply was about 0.5 volts peak to peak. For the circuitry implemented, the 5-volt supply should fall no faster than 1 volt per millisecond. This rate allows 100 microseconds for deselect to take place while the supply is falling from 4.6 volts to 4.5 volts. Thus, deselect occurs while the system is stable.

Miscellaneous

TEST MODE

The test mode applies the oscillator output to the input of the millisecond counter. This affords faster testing of the chip. This mode is intended for factory testing, where a programmable pulse generator is used. A pulse rate of 50 kHz may be used in this mode. The pulse should swing rail to rail and be a square wave. Apply the pulses to the oscillator input pin, leaving the oscillator output pin open circuit. The basic sequence would be to write values to the counters, enter test mode and apply a known number of pulses. Next, read the counters using normal read sequence.

GO COMMAND

A write to address 15 hex (data is a ''don't care'') will clear the seconds through milliseconds counters. If the value in the seconds counter is equal to or greater than 40 when the GO command is executed, then the minute counter will be incremented.

RESET COMMAND

Writing the value FF hex to address 12 hex causes the hours through milliseconds counters to be reset to zero. The day of week, day of month, and month counters are set to 1.

Writing the value FF hex to address 13 hex causes the RAM to be cleared.

GENERAL TIMING CONSIDERATIONS:

To guarantee a valid read/write without using the ready output, the following criteria must be met.

Read Operation

When reading, a deselect time of 500 nanoseconds must occur between counter reads. Read strobe width must not exceed 800 microseconds. The deselect condition is: $\overline{CS}$ = 1 or ($\overline{RD}$) • ($\overline{WR}$) = 1.

1. Address setup before RD = 100 ns min
2. CS to RD = 0 min
3. Read strobe width = 950 ns min
4. Address hold after read = 50 ns min
5. Deselect time = 500 ns min

Write Operation

1. Address set up before WR = 100 ns min
2. CS to WR = 0 ns min
3. WR and data must be coincident for 950 ns min
4. Data hold after WR = 110 ns min
5. Address hold after WR = 50 ns min

If the ready output is used to guarantee read write operation, then the following recommendations are made. Referencing the April 1982 data sheet, during a read, the ready line makes its positive transition 100 nanoseconds before data is valid. (Not shown in the data sheet.) The user should not use this signal to latch data into an external latch. If this signal is used to wait state a microprocessor, then a critical examination of the microprocessor timing with respect to when it terminates its wait stated cycle must be made. This examination must also include any set-up time the processor needs prior to reading data. Also, note that the ready output (per the data sheet) negative-going-edge occurs 150 nanoseconds after the read or write strobe has gone low. Check microprocessor timing to ensure that the ready signal would be recognized as a ''wait-signal''.

It is not advised to perform sequential reading by connecting chip select and read low and cycling through the counters by changing address lines. The reason is that it is possible to cause an internal latch to ''flip,'' the result being an error in timekeeping.

SOFTWARE CONSIDERATIONS

Reading the Counters

A read of one counter plus the rollover status bit or all the counters plus the rollover bit must be done within 800 microseconds. If the rollover status bit is a ''1'' then a complete read of counter(s) must be performed again. The 800 microsecond value is conservative. If the time between the read of any counter(s) and the rollover status bit exceeds 800 microseconds, then the status bit will always be set. The order of reading must be counter(s) first, then rollover status bit. This is because the positive going edge of the read strobe clears the status bit. Refer to *Figure 23*. The status bit is enabled for a period of 150 microsecond maximum at a rate of 1 kHz. If during this 150 microsecond period a counter(s) read occurs, the status bit will be set. This is true no matter how often the rollover status is read during that time period. Each rollover status read resets the status bit, but any counter read within the 150 microsecond period will set the rollover status bit. If the counters are read after a repetitive interrupt, then allow 150 microseconds (conservative) from the sense of the interrupt to the read of the counters (ripple delay time) and the data will be valid. If the counters are read after a compare interrupt, the read can occur immediately and will be valid.

Writing the Counters

The counters may be written to in any order, because the write overrides the internal increment. If it is desired to write all the counters without increments occurring in between writes, then the complete write operation must be performed within 800 microseconds. As long as valid BCD values (with respect to the specific counter) are written, no other counter is affected by the write. In general, writing the high order to low order counters is the conservative approach. This method is less susceptible to increments between writes for cases where the writing takes greater than 800 microseconds. For initialization of time, if the ''GO'' command is issued prior to any write, then 10 milliseconds are available to write from months through tenths and hundredths of seconds without any effect due to internal incrementing.

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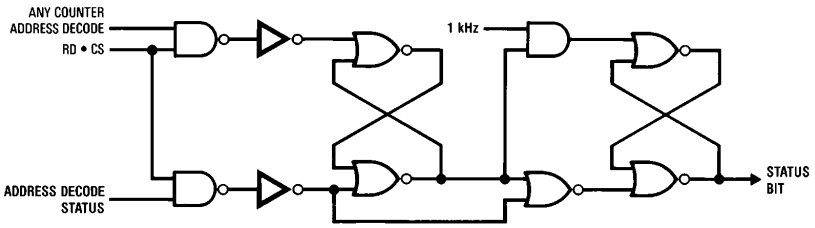

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FIGURE 21. Rollover Status Bit Logic

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