Selecting Input/Output Options On COPS™ Microcontrollers

National Semiconductor
Application Note 401
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March 1985

INTRODUCTION

There are a variety of user selectable input and output options available on COPS when the ROM is masked. These options are available to help the user tailor the I/O characteristics of the Microcontroller to the application. This application note is intended to provide the user a guide to the options: What are they? When and how to use which ones? The paper is generally written without reference to a specific device except when examples are given. It must be remembered that any given generic COPS Microcontroller has a subset of all the possible options available and that a given pin might not have all possible options. A reference to the device data sheet will determine which options are available for a specific device and a specific pin of that device.

INPUT/OUTPUT OPTIONS

Table I summarizes the I/O capability of NMOS-COPS, in general. However, some of the options have different configuration in CMOS-COPS. Data sheets provide information on the I/O options associated with the CMOS-COPS.

I. OUTPUTS

The following discussion provides detailed information on the capabilities of the mask-programmable output options available on COPS.

A. STANDARD OUTPUT

This option is a simple, straightforward, logic compatible output used for simple logic interface. It is available on SO, SK and all D and G outputs, It is recommended to be used as a default option for all but SO, SK outputs.

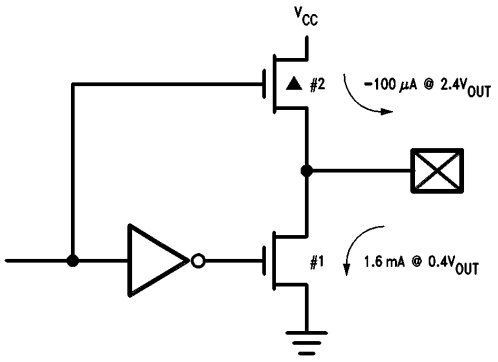

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FIGURE 1. Standard Output

Figure 1 shows the standard output configuration. The enhancement mode device to ground is good at sinking current (sinks 1–2 mA) and is compatible with the sinking requirement of 1 TTL load (1.6 mA at 0.4V). It will meet the "low" voltage requirement of CMOS logic. All output options use this device (device #1) for current sinking. On the other hand, the relatively high impedance depletion-mode device (device #2) to V_{CC} provides low current sourcing capability (100 μA at 2.4V). This pullup is sufficient to provide the source current for a TTL high level and will go to V_{CC} to meet the "high" voltage requirements of CMOS logic. An external resistor to V_{CC} may be required to interface to other external devices requiring higher sourcing capability.

An interface example to a common emitter NPN transistor is given below:

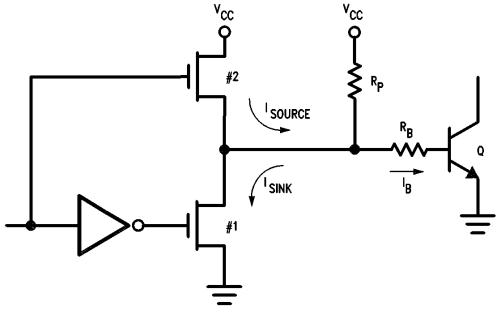

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FIGURE 2

R_B is needed to limit transistor's base current if $I_{source} > I_{B(max)}$.

R_p helps generate base drive if the I_{source} is not sufficient. The disadvantage of R_p is the introduction of more power dissipation. The temperature effects on the reverse saturation current I_{CBO} causes I_C to shift. I_{CBO} approximately doubles for every 10°C temperature rise. The effect of changes in I_{CBO} reduces off state margin and increases power dissipation in the off state.

However, in a typical device, the current supplied by R_p will swamp out any effects on I_{CBO}. Another parameter found to be decreasing linearly with temperature is V_{BE}:

$$\Delta V_{BE} = V_{BE_2} - V_{BE_1} = -k(T_2 - T_1)$$

where $k \approx 2$ mV/°C, T in °C.

Now let's consider a practical example:

LOW SOURCE CURRENT OUTPUT:

Standard output, COP420, device #2.

The selected transistor is 2N3904.

DESIGN CONSIDERATIONS:

a. Q is in saturation during ON-state.

b. Q's collector current $I_C = 100$ mA

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TABLE I

	Default	Standard	Push-Pull	High Sink	Very High Sink	LED	Hi-Current LED	TRI-STATE® Push-Pull	Hi Current TRI-STATE Push-Pull	Open Drain
SO	Push-Pull	Logic Compatible; Non MICROWIRE™	MICROWIRE Higher Drive, Faster X'sition							External Pull Up
SK	Push-Pull	Logic Compatible; Non MICROWIRE	MICROWIRE Higher Drive Faster Transition							External Pull Up
D	Standard	Logic Compatible		L Parts Only 15 mA	L Parts Only 30 mA					External Pull Up, Standard, Hi Sink or V.H.S. Pull Down
G	Standard	Logic Compatible; Inputs		L Parts Only 15 mA	L Parts Only 30 mA					External Pull-Up, Standard, Hi Sink or V.H.S. Pull Down
L	Standard	Logic Compatible; Inputs, TRI-LEVEL				Hi Source 1.5 mA TRI-LEVEL	L Parts Only Higher Source 3 mA TRI-LEVEL	MICROBUS™ Meets TRI-STATE Spec. TRI-LEVEL	L Parts Only Meets TRI-STATE Spec. TRI-LEVEL	External Pull Up TRI-LEVEL
H	Standard	Logic Compatible Inputs								External Pull Up
R	Standard	Logic Compatible; Inputs, TRI-LEVEL	Higher Drive Faster Transition TRI-LEVEL					Meets TRI-STATE Spec TRI-LEVEL		External Pull Up TRI-LEVEL

c. Assuming a ''forced'' of 10 for Q. This is a standard value for β to insure saturation.

For an $I_C = 100$ mA, $\beta = 10$, we have $I_B \geq 10$ mA. The low current standard output certainly cannot provide $I_B \geq 10$ mA. Therefore, a pullup resistor (R_p) is required.

d. Now we need to select the minimum allowed value for R_p. The sinking ability of COPS output will determine R_p. We must sink the pullup current to a $V_{OUT} < V_{BE}$ in order to hold Q off. Also, note that

$$\frac{\Delta V_{BE}}{\Delta T} = -2 \text{ mV/°C}.$$

e. Assuming the worst case is at V_{CC} (max) and High-temperature (let $\Delta T = 20°C \Rightarrow \Delta V_{BE} = -40$ mV). From $V_{BE(ON)}$ Vs. I_C curve, *Figure 3*:

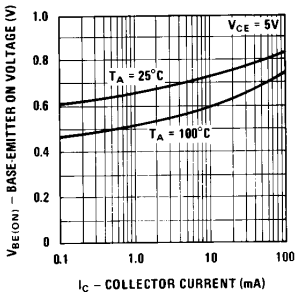

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FIGURE 3. 2N3904 I/V

at 100 mA, 25°C, $V_{BE} \cong 0.85$V.

So, our $V_{BE(45°C)} = 0.85 - 0.04 \cong 0.81$V.

There is not margin here for process V_{BE} variations so we can allow 200 mV of slope,

$V_{BE} = 0.61$V (worst case)

f. Having $V_{BE} = 0.61$V, we go to COPS sink graph and draw a vertical line at $V_{OUT} = V_{BE} = 0.61$V. *Figure 4* below:

Output Sink Current

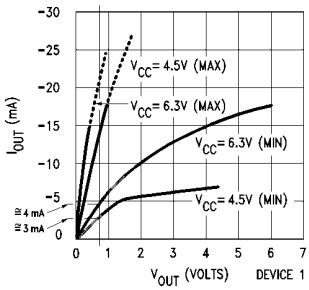

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FIGURE 4

This will tell us, at $V_{out} = V_{BE}$, how much current can be sinked to keep Q ''OFF''. The intersection of $V_{CC} = 6.3$ (MIN) and $V_{BE} = 0.61$V gives us $I_{sink} = 4$ mA.

g. Now calculate R_p.

$$R_p \geq \frac{6.3 - 0.61}{4} \text{k} \geq 1.42\text{k}$$

$$\text{the actual standard } R_p\ (\pm 10\%) = \frac{1.42}{0.9}$$

$$= 1.6\text{k} \pm 10\%$$

h. Using the value of R_p, let's calculate the current through R_p at $V_{CC} = 4.5$V(MIN).

$$I_{RP} = \frac{4.5 - 0.61}{1.42} \text{mA} = 2.74 \text{ mA}$$

Which is less than sink ability of device (3 mA from *Figure 4*) at $V_{CC} = 4.5$V, $V_{out} = 0.61$V.

i. Now calculate the available source current. Here we use $V_{BE(max)}$ which is the worst case, and low temperature.

Let T (ambient) = 10°C.

From V_{BE} vs. I_C curve, *Figure 3*:

$V_{BE} \cong 0.83$V at 25°C

$V_{BE} \cong 0.83 + 2$ mv/°C $\times$ 15 = 0.86V at 10°C.

Using this value of V_{BE}, we go to COP420 Standard Output source current curve (*Figure 5*), and draw a vertical line at $V_{BE} = 0.86$V. The intersection of this line and $V_{CC} = 4.5$(MIN) gives an $I_{source} = 325\ \mu$A.

Standard Output
Source Current

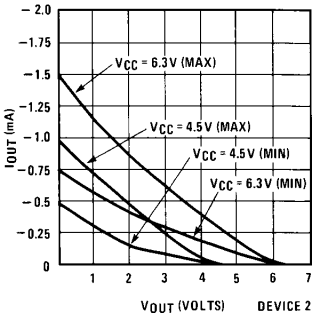

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FIGURE 5

This is low but typical of N-channel low current standard output.

Contribution of R_p

$$I_{RP} = \underbrace{\frac{4.5 - 0.86}{(1.6)\ (1.1)}}_{R_{p(max)}} = 2.07 \text{ mA}$$

$I_B(\text{min}) \cong 2.07 + 0.325 = 2.3$ mA

This is our worst case base drive, but we needed 10 mA.

What can we do to get the base drive we need?

1. We can use above design and allow Q to come out of saturation. The disadvantage is that Q's power dissipation increases.

2. Or use a Darlington configuration (Process 05). In such a configuration only first stage of Darlington can be saturated (not output stage). This will introduce a slightly higher power dissipation. Note that for a process 05 transistor, the forced β is 1000.

3. Use a high source type output such as TRI-STATE output. If we draw a vertical line at $V_{BE} = 0.86$, we get a source current of $\cong$ 6 mA at $V_{CC} = 4.5$(MIN) *Figure 6*, which gives us a worst case

$$I_{B(min)} = 8.07 \text{ mA}.$$

TRI-STATE Output Source Current

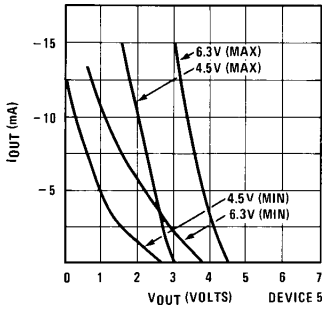

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FIGURE 6

CAUTION On TRI-STATE graph the intersection of $V_{out} = B_{BE} = 0.86$V and $V_{CC} = 6.3$V(MAX) curve (*Figure 6*) would result in an $I_{B(Max)} = 50-60$ mA, which is way too much to handle. In this case there is a need for a series current limiting R_B to kill some of the worst case $I_{B(max)}$.

4. There is a high current Standard-L option on some COPS (i.e., COP4XL, L-port) which provides sufficient source current.

5. N-channel output can generally sink better than source. PNP transistor can be used instead of NPN. The same analysis applies and in general will show better overdirve capabilities.

As shown in *Figure 7*, the D_0 output which has a standard output option, is driving the base of the PNP transistor. Assuming $V_{CC} = 4.5$V (for COP402), $V_{BE} = 1.0$V, and a worst case base drive requirement of 3.0 mA. We see that we must supply 200 μA to the base-emitter resistor to turn the transistor on:

$$1.0\text{V}/5.1\text{k} = 200\ \mu\text{A}$$

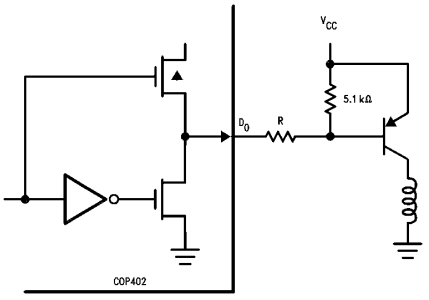

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FIGURE 7. PNP Drive

From the output sink current curve on the COP402 data sheet, we find that, at 1.0V the D-line can sink 3.2 mA. To calculate the value of the current limiting resistor,

$$R = (V_{CC} - V_{BE} - V_{D0})/I$$

When $V_{CC} = 6.3$V, the D0 output can sink more than enough current at 0.3V, and if the $V_{BE} = 0.7$V, we can calculate the maximum D_0 output current:

$$I = (V_{CC} - V_{BE} - V_D)/R$$
$$= (6.3 - 0.7 - 0.3)/780 = 6.3 \text{ mA}.$$

Using the Standard Output Option for Bidirectional I/O (G-port)

The standard output is good at sinking current, but rather weak at sourcing it. Therefore, by using the Standard Drive configuration and outputting 1's to the port, an external source may easily overdrive the port drivers with the added bonus of a built-in pullup. While the depletion-mode device provides sufficient current for a TTL high level, yet can be pulled low by an external source, thus allowing the same pin to be used as an input and output. Data written to the ports is statically latched and remains unchanged until rewritten. As inputs the lines are non-latching (*Figure 8*).

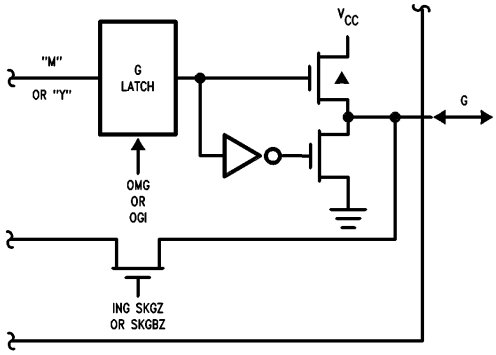

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FIGURE 8. G Port Characteristics

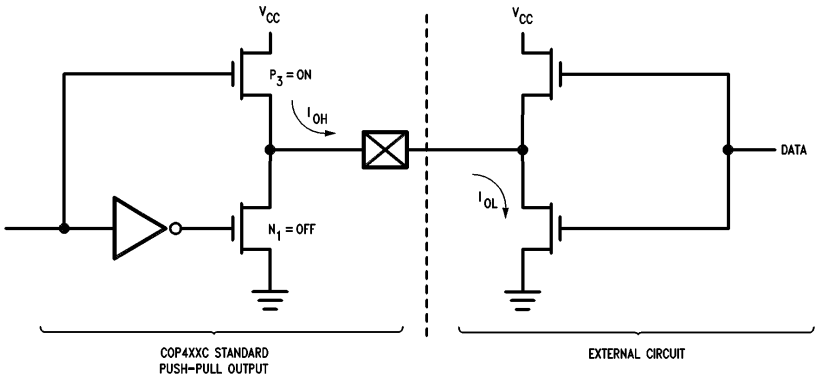

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FIGURE 9

When writing a ''0'' to the port, the enhancement-mode device to ground overcomes the high pullup and provides TTL current sinking capability. While writing a ''1'' the depletion-mode device behaves as internal pullup maintaining the ''1'' level indefinitely. In this situation, an input device capable of overriding the small amount of current supplied by the pull-up device can be read. This feature provides maximum user flexibility in selecting input/output lines with minimum external components.

In CMOS-COPS the low current push-pull output has even much weaker source current capability and this make it easier to be overriden.

Referring to *Figure 9*.

Note that $I_{OL} > I_{OH}$, otherwise transistors or buffers must be used.

For COP424C/444C, standard push-pull

@ $V_{CC} = 4.5V, V_{out} = 0V$, $I_{OH(min)} = 30\ \mu A$
$I_{OH(max)} = 330\ \mu A$

@ $V_{CC} = 2.4V, V_{out} = 0V$, $I_{OH(min)} = 6\ \mu A$
$I_{OH(max)} = 80\ \mu A$

While in NMOS (COP420L), Standard output:

@ $V_{CC} = 4.5V, V_{OH} = 2.0V$, $I_{OH(min)} = 30\ \mu A$
$I_{OH(max)} = 250\ \mu A$

@ $V_{CC} = 6.3V, V_{OH} = 2.0V$, $I_{OH(min)} = 75\ \mu A$
$I_{OH(max)} = 480\ \mu A$

As we see, both in CMOS and NMOS it is easier to override I_{OH}. Note that the standard output option is available with standard, high, or very high sink current capability (''L'' parts only). The pulldown device is bigger for the high/very high current standard output. The sourcing current is the same. These three choices provide some control over current capability.

B. OPEN-DRAIN OUTPUT

This option uses the same enhancement-mode device to ground as the standard output with the same current sinking capability. It does not contain a load device to V_{CC}, allowing external pullup as required by the user's application. The sinking ability of device #1 determines the minimum allowed external pullup. The analysis discussed earlier for Standard Output options equally applies here. Available on SO, SK, and all D, G, and L outputs.

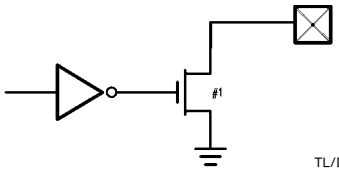

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FIGURE 10. Open-Drain Output

The open-drain option makes the ports G and L very easy to drive when they are used as inputs. This option is commonly used for high noise margin inputs, unusual logic level inputs as from a diode isolated keyboard, analog channel expansion, and direct capacitive touch-panel interface. Available with standard, high or very high sink capability (''L'' parts only).

C. PUSH-PULL OUTPUT

The push-pull output differs from the standard output configuration in having an enhancement-mode device in parallel with the depletion-load device to V_{CC}, providing greater current sourcing capability (better drive) and faster rise and fall times when driving capacitive loads.

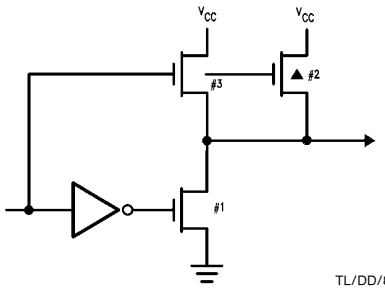

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FIGURE 11. Push-Pull Output

If a push-pull output is interfaced to an external transistor, a current-limiting resistor must be placed in series with the base of the transistor to avoid excessive source current flow out of the push-pull output. This option is generally for MICROWIRE Serial Data exchange.

It is available on SO, SK only and is recommended to be used as a default option for these outputs. A few points must be kept in mind when using SO, SK for MICROWIRE interface.

The data sheet specifies the propagation delay for a certain test condition (i.e., V_{CC} = 5V, V_{OH} = 0.4V, Loading = 50 pF, etc.).

In practice, actual delay varies according to actual input capacitive loading (typical 7–10 pF per IC input), total wire capacitance and PCB stray capacitance connected to the SI input. Thus, if actual total capacitive loading is too large to satisfy the delay time relationships ($t_d = t_{SK} - t_r$; t_d = actual delay time, t_{Sk} = the instruction cycle time, t_r = the finite SK rise time), either slow down SK cycle time or add a pullup resistor to speed up SK "0" to "1" transition or use an external buffer to drive the large load. Besides the timing requirement, system supply and fan-out/fan-in requirements have to be considered, too.

If devices of different types are connected to the same serial interface, the output driver of the controller must satisfy all the input requirements of each device. Briefly, for devices that have incompatible input levels or source/sink requirements to exchange data, external pullups or buffers are necessary to provide level shifting or driving. Unreliable operation might occur during data transfer, otherwise. For a 100 pF load, a standard COPS Microcontroller may use a 4.7k external resistor, with the output "low" level increased by less than 0.2V. For the same load the low power COPS may use a 22k resistor; with the SO, SK output "low" level increased by less than 0.1V.

D. STANDARD L OUTPUT

Same as Standard Output, but may be disabled. Available on L-outputs only.

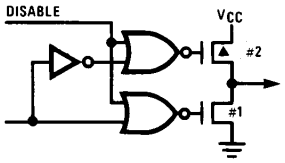

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FIGURE 12. Standard L Output

When this option is implemented on the L-port and the L-drivers are disabled to use the L lines as inputs, the disabled depletion-mode device cannot be relied on to source sufficient current to pull an input to a logic high. There are two ways to use L lines as inputs (having standard L option):

The first method requires that the drivers be disabled. In this case the lines are floating in an undefined state. The external circuitry must provide good logic levels both high and low to the input pins. The inputs are then read by the INL instruction. The second method is similar to the technique used for the G-port. The drivers are enabled and a"1" must be written to the Q register.

The external circuitry will then be required only to pull the lines low to a logic "0". The line will pull up to a "1" itself. The INL instruction is used as before to read the lines.

E. LED DIRECT DRIVE OUTPUT

In this configuration, the depletion-load device to V_{CC} is paralleled by an enhancement-mode device to V_{CC} to allow for the greater current sourcing capacity required by the segments of an LED display. Source current is clamped to prevent excessive source current flow.

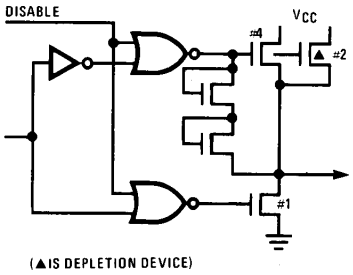

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FIGURE 13. LED (L output) NMOS-COPS

This configuration can be disabled under program control by resetting bit 2 (EN^2) of the enable register to provide simplified display segment blanking.

However, while both enhancement-mode devices are turned off in the disabled mode, the depletion-load device to V_{CC} will still source up to 0.125 mA. As in the case of Standard L output, again this current is not sufficient to pull an input to a logic "1".

The drivers must be disabled and the lines must be pulled high and low externally, whenever they are used as inputs.

Example #1:

When COPS outputs are used to drive loads directly, the power consumed in the outputs must be considered in the maximum power dissipation of the package.

Figure 14 shows an LED segment obtaining its source current from L_0 output and D_0 sinking the current. In this configuration all the power required to drive the LED with the exception of the portion consumed by the LED itself, is consumed within the chip. Assuming COP404L is the driving device:

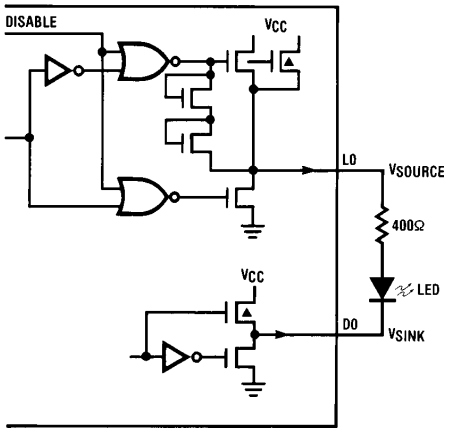

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FIGURE 14. LED Drive

If we assume the V_{source} is not inserted, the device has a V_{CC} of 9.5V, and that the voltage drop across the LED is 2.0V.

We can calculate the power dissipation in these outputs. The minimum current that D_0 can sink at 1.0V is 35 mA (COP404L data sheet). L_0 can source up to 35 mA at 3.0V. Therefore, the power dissipation for the L_0 output could be: $(9.5 - 3.0)\ (0.035) = 227$ mW. The power in the D_0 output is $(1)(0.035) = 35$ mW.

Now let us calculate the current limiting resistor. Referring to COP404L L_0–L_7 output source current curves, at $V_{CC} = 9.5$V the minimum current curve peaks at $I = 6.0$ mA and $V_{source} = 4.8$V. The current curve is actually very flat between 4.0 and 5.0 volts. For maximum current, we need to set the voltage on the L pin equal to 4.8V at 6.0 mA. The D line will sink this current at 0.4V. Therefore, the resistor and LED must make up the difference:

$$V_I = V_D + IR + V_{LED}$$

$$4.8 = 0.4 + 0.006R + 2.0$$

$$R = 400\Omega$$

At the other end of the curve, when the L line sources the maximum current, assume the LED and the D line will have the same voltage drop.

$$V_I = 0.4 + IR + 2.0$$

$$V_I = 2.4 + IR$$

From the current curve, we see that at 6.4V the L line will source 10 mA. Therefore: $V_I = 2.4 + (0.01)\ (400) = 6.4$V.

Example #2:

Let's consider a different configuration.

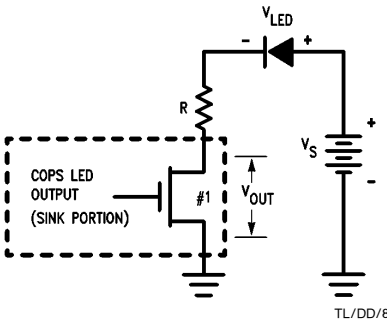

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FIGURE 15. LED DRIVE

Now we calculate the series current limiting resistor R. The circuit has two non-linear devices to be considered; the output device and the LED.

The LED in this example is NSC5050. Looking at I/V curve, the device has a threshold 1.6V. Also, note that for $V_{LED} > 1.6$V the I/V curve is very linear (*Figure 17*).

Because of this, the LED characteristic can be modeled as a sharp threshold device with a non-zero source resistance (normally I/V curve is LOG looking).

From ON part of curve,

$$R_S = \frac{1.9 - 1.7}{0.05} = 4\Omega$$

We can neglect R_S as well (only $R_S \ll R$). Our model is simply a voltage source for the LED when

$I = 0$ for $V_{LED} < V_{TH}$

$I = \infty$ for $V_{LED} > V_{TH}$

Design Procedure:

1. $I_{LED(min)} = \dfrac{V_{S(min)} - (V_{LED(max)} + V_{OUT(max)})}{R(max)}$

We need endpoints of the load line.

a. @$V_{out} = 0 \Rightarrow I_{LED(min)} = \dfrac{V_{S(min)} - V_{LED(max)}}{R(max)}$

b. @$V_{out} + V_{LED(max)} = V_S \Rightarrow I = 0$
($V_{LED(max)} = 2$V)

2. Plot a and b

Assuming an $I_{min} = 7$ mA, $V_{S(min)} = 4.5$V

from 1 $R_{(max)} = 357\Omega$

Draw the load line with slope $-1/357$ crossing

$V_{out} = V_S - V_{LED(max)} = 4.5 - 2 = 2.5$V.

(*Figure 16*).

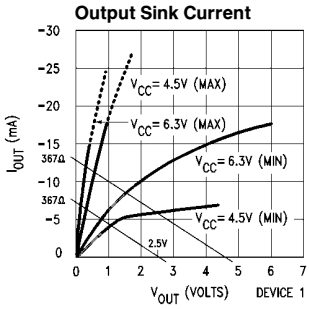

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FIGURE 16. COP420

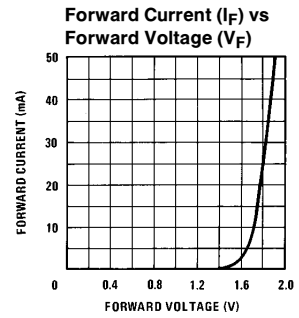

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FIGURE 17. LED I/V Characteristic

The intersection of this load line and V_{CC} = 4.5V (min) curve, we find an actual value of $I_{(min)}$ = 4.25 mA.

To determine I_{max} (at R = 357Ω) we draw a parallel load line intersecting V_{out} = 6.3 − 2.0 = 4.3V and find that @ V_{CC} = 6.3V, $I_{(max)}$ = 13 mA.

3. From above calculations we observe that our $I_{(min)}$ (actual) is way off. Let's try to rotate our first load line around V_{out} = 2.5V to increase I_{min} and then check I_{max} and R. (*Figure 18*).

Let's go for an I_{min} (actual) = 6 mA. This will give us R = 89Ω and the max. plot goes off the graph to = 36 mA.

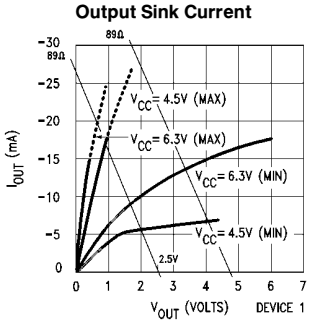

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FIGURE 18. COP420

Comments:

1. The design must be a compromise between the two extremes (battery life should also be considered).

2. The lower the LED threshold the better. (The load line moves further up the device curve.)

F. TRI-STATE PUSH-PULL OUTPUT

This option is specifically available to meet the specifications of National's MICROBUS, outputting data over the data bus to a host CPU. It has two enhancement-mode devices to ground and V_{CC}.

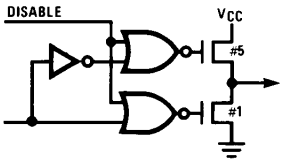

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FIGURE 19. TRI-STATE Push Pull (L output)

The TRI-STATE logic can disable both enhancement-mode devices to free the MICROBUS data lines for input operation.

CAUTION Never try to pull against the TRI-STATE Output (too much source current) with the drivers enabled and Q register previously loaded with ''1''. The choices we have are mentioned earlier. Either TRI-STATE L-port or use Standard L output option.

II. INPUTS

COPS inputs may be programmed either with a depletion load device to V_{CC} or floating (Hi-Z input). All inputs are TTL/CMOS compatible. Hi-Z inputs should not be left floating; they should be connected to the output of a ''high'' and ''low'' driving device if active or to V_{CC} and ground if unused. Especially when using CMOS COPS (very high impedance inputs), the open inputs can float to any voltage. This will cause incorrect logic function and more power dissipation. Also, the CMOS inputs are more susceptible to static charge which causes gate oxide rupture and destroys the device. Unlike inputs, the outputs should be left open to allow the output switch without drawing any DC current. Another precaution is powering up the device. Never apply power to inputs or TRI-STATE outputs before both V_{CC} and ground are connected. This will forward bias input protection diodes, causing excessive diode currents. It will also power the device.

Special care must be practiced when interfacing a CMOS-COPS input to an analog IC, powered by different supply voltages. Avoid overvoltage conditions resulting

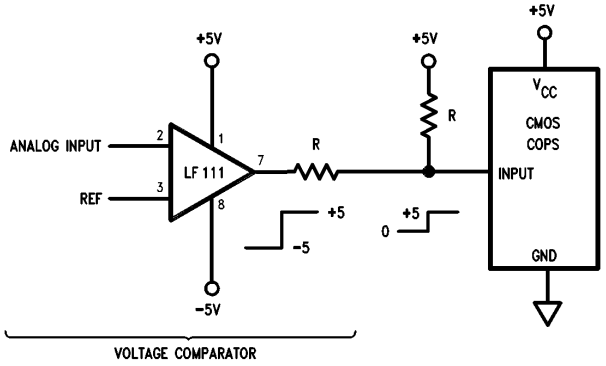

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FIGURE 20

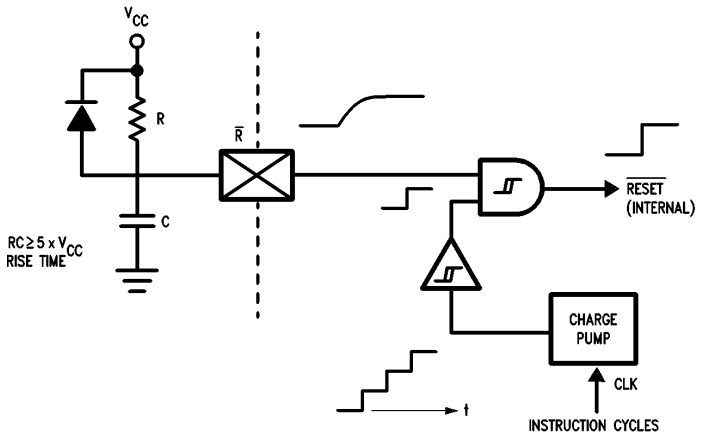

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FIGURE 21

from such situations. As an example, consider the interface of a CMOS-COPS with the LF111 voltage comparator:

When the low level ''−5V'' appears on the comparator's output, the COPS input is pulled low below ''logic low'' of ''0V''. This will cause damage if the comparator sinks enough current. The use of a current-limiting resistor in series with the input is helpful. A better solution is to use a voltage divider as shown in *Figure 20*. Any time a low level appears on the comparator's output, a total voltage drop of 10V will appear across both resistors each dropping 5V, causing the input to sit at 0V. Whenever the output goes high, the resistors will not drop any voltage (no current through the resistors) and a logic high of 5V will appear on the input. To reduce power dissipation introduced by resistors, the resistor value must be high (>100k), because the CMOS inputs have very high input impedance.

$\overline{\text{RESET}}$ INPUT

All COPS Microcontroller have internal reset circuitry. Internally there is an AND gate with one input coming from the $\overline{\text{RESET}}$ input, and the second input connected to a charge pump circuitry. In the Charge pump circuit, a tiny capacitor is being charged upon execution of each internal instruction cycle. When the voltage across this internal capacitor reaches a high logic level, the second input of the AND gate is released.

The Reset logic will initialize (clear) the device upon power-up if the power supply rise time is less than 1 ms and greater than 1 μs. With a slowly rising power supply, the part may start running before V_{CC} is within the guaranteed range. In this case, the user must provide an external RC network and diode shown in *Figure 21* above. The external RC network is there to hold the $\overline{\text{RESET}}$ pin below V_{IL} until V_{CC} reaches at least $V_{CC(min)}$. The desired response is shown in *Figure 22*.

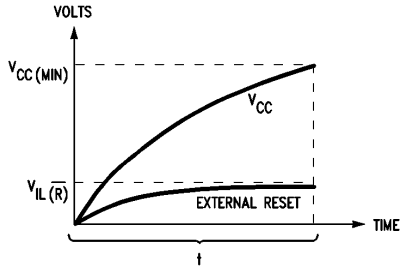

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FIGURE 22

t = 500-600 instruction cycles (8 msec)
for COPxxxL

t = 900–1000 instruction cycles (4 msec)
for COPxxxC

The diode is included in the reset circuitry to cause a "forced Reset" when the power supply goes away and recovers quickly. In such a situation the diode helps discharge the capacitor quickly. Otherwise, if the power failure occurs for a short time, the capacitor will not be fully discharged and the chip will continue operation with incorrect data.

Note that on the CMOS COPS, the internal charge pump circuitry can be disabled when using a very slow clock (<32 kHz) [option 23 = 1]. This is necessary, because one can run from DC to 4 μs instruction cycle time (fully static). In such a situation external RC network discussed earlier must be used.

INPUT PROTECTION DEVICES

All inputs and I/O pins have input protection circuitry. This circuitry is there regardless of any option selected. It is the first circuitry encountered at the pin.

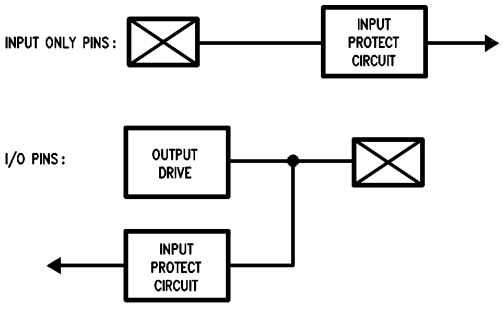

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FIGURE 23

For NMOS and XMOS devices, the circuits are of the form:

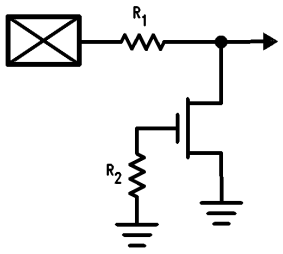

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FIGURE 24

This is a standard circuit defined for the process. R_1 is on the order of 200Ω. R_2 is around 300Ω (note that the R values are not precise).

This circuit is functionally equivalent to:

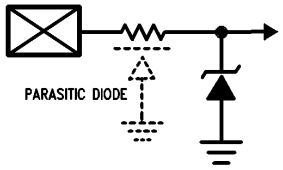

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FIGURE 25

The zener breakdown is around 10–15V; the gate breakdown is 50V.

CONCLUSION

All COPS Microcontrollers have a number of I/O options necessary to implement dedicated control functions in a wide variety of applications. The flexibility to select different options allows the user to tailor within limits, the I/O characteristics of the Microcontroller to the system. Thus, the user can optimize COPS for the system, thereby achieving maximum capability and minimum cost. This application note deals with the basic functionality of COPS I/O characteristics and does not address electrical differences among the various COPS devices.

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