

Application Issues for the DP8465 Family of Data Synchronizers

National Semiconductor
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This application note covers National's first generation hard disk data synchronizers and separators, i.e., the DP8465, DP8462, DP8461, DP8455 and DP8451, citing some common PLL application concerns and describing some techniques to enhance performance.

FRACTIONAL HARMONIC LOCK

The frequency discrimination capacity of the digital phase detector within the data separator/synchronizer is suppressed whenever a pulse gate technique is employed. Although this pulse gating technique is a standard in disk drive applications and is necessary in order to allow the PLL to remain phase locked to randomly spaced disk data bits, it essentially causes the phase detector to behave as would an analog quadrature multiplier, i.e., the capture range of the loop takes on the finite value related to the loop bandwidth. Under ordinary circumstances, this is quite acceptable; however, it does permit the PLL to become susceptible to a form of quasi-stable false lock to fractional harmonics of the input frequency. (For example, a typical lock null for this phenomenon would be where the VCO stabilizes at 5/6 or 6/5 of its nominal frequency.) The conditions for occurrence of this are:

- 1) Pulse gate in use;
- 2) Periodic pattern is present (i.e., preamble);
- 3) Perturbation occurs either during or just prior to the periodic pattern, causing the VCO to swing outside of the dynamic capture range of the loop.

Since the capture range in a typical disk PLL configuration is on the order of $\pm 2\%$ of the data rate, it can be seen that

harmonic lock could easily occur given an adequate perturbation of the loop. Typical causes of perturbations would be media defects and spurious noise pulses, among others, but the most commonly seen occurrence within soft-sectored systems is where an attempt is made to "read" through the write splice region on the disk (zone where the head write current is either switched on or off) during a sector search operation. Although recovery from harmonic lock will occur readily if the read operation is terminated (all National's currently released disk data synchronizers incorporate frequency discrimination when locking to the reference input), systems which exhibit fractional harmonic lock during a sector search may experience extended latency time as the search routine repeatedly tries to find the desired sector.

The soundest solution to harmonic data lock is the incorporation of a sector search routine which asserts Read Gate only within a preamble field, in conjunction with the use of a PLL which employs frequency acquisition during the lock sequence. National's DP8451 and DP8461 are designed for this type of application, employing frequency lock for the standard MFM preamble (2T, when T is equal to the VCO period). The DP8462 allows optional frequency lock for both 2, 7 preamble types (3T or 4T). National's most recent stand-alone data synchronizer, the DP8459, can accommodate frequency lock (also optional) with any standard preamble type (1T, 2T, 3T or 4T). The DP8459 also incorporates zero-phase start at the assertion of Read Gate, minimizing the phase disturbance at the beginning of a read operation.

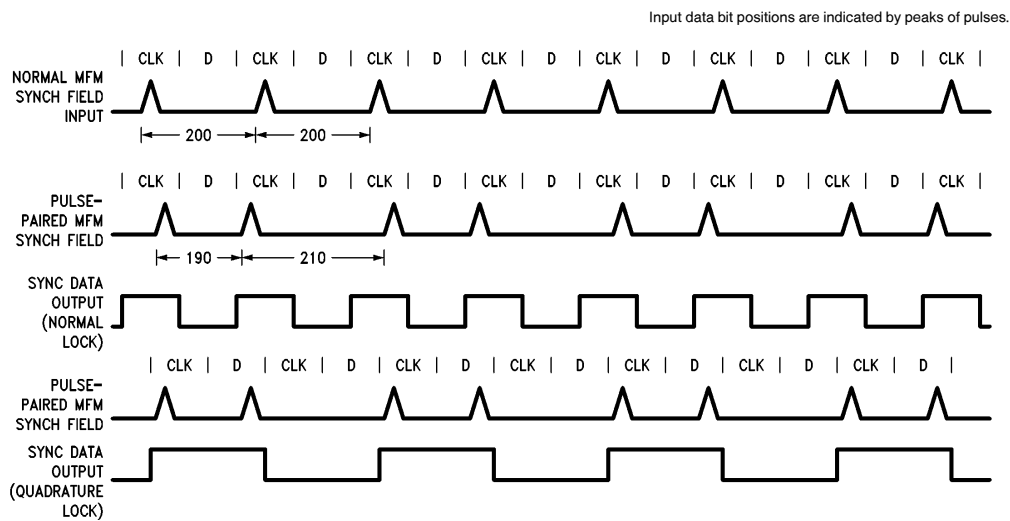


FIGURE 1. Timing Diagram of PLL Quadrature Lock within a Symmetrically Pulse-Paired Synch Field

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Within systems where it becomes evident that the reading of write splices is consistently producing sector-not-found errors, while at the same time it is not possible to either modify the sector search algorithm (in order to avoid the splices) or to make hardware modifications, the PLL can be made less sensitive to the write splice disturbance by the lowering of the loop bandwidth. This is recommended only as an interim solution until firmware or hardware accommodations can be made.

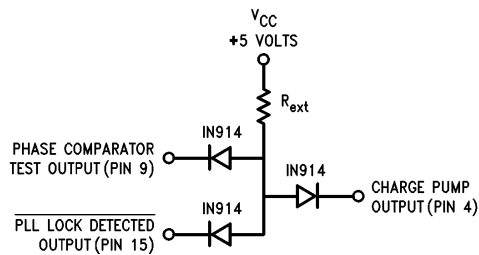
QUADRATURE LOCK

Another form of false lock may also occur (pulse gate in use) within a periodic disk pattern (preamble) given one additional condition; the periodic disk pattern being presented to the PLL exhibits a pulse-pairing phenomenon (typically introduced by the data channel electronics); see *Figure 1*. Within this particular pattern, PLL has the potential to lock to the correct frequency while remaining caught on a phase null 90 degrees from nominal. In this case, each pair of bits is interpreted by the PLL as residing in two directly adjacent windows (actually a violation of most recording codes) with the two subsequent windows empty. Although the bits appear to be greatly shifted within these windows, the phase corrections produced complement each other and average to a filtered DC value of zero. This repeating pattern is thus self-sustaining.

Quadrature lock is unique in that it is more likely to occur within a relatively well designed, noise-free system environment. The reason for this is that the randomizing effect noise ordinarily has on the data stream has been minimized, preserving the purity of the pulse paired pattern and thus increasing the probability of this form of lock. Again, this form of lock is generally only seen within the preamble, and may occur within either soft or hard sectored systems. Easily recognized waveform patterns seen at the separator/synchronizer outputs would be (1) the Synchronized Data Output exhibits a 110011001100 . . . pattern instead of the standard 1010101010 . . . preamble pattern; (2) the Phase Comparator Test output pulse width consistently remains at approximately half of the VCO period (nominal width should be 7–12 nanoseconds); (3) -Lock Detected does not become active (low).

The most robust solution to this phenomenon (as in the section on harmonic false lock, above) is to incorporate a hard or pseudo hard-sectored search algorithm in conjunction with a data separator/synchronizer which employs frequency acquisition within the preamble as do the DP8451, DP8461, DP8462 and DP8459. The frequency acquisition mode allows no residual phase or frequency error within the PLL when locked, and thus the possibility of both quadrature and harmonic lock is eliminated.

A “bootstrap” hardware technique to avoid quadrature lock can be incorporated with the DP8465/55 devices, which do not incorporate preamble frequency lock internally (see *Figure 2*). This technique involves the inclusion of four passive elements external to the chip, which will deliberately force the window to shift away from the 90 degree phase null when (and only when) quadrature lock occurs. The passive network is automatically disabled once the PLL detects preamble lock. Although a recommended value is given for the resistor in this support circuit, some experimenting may be required in determining an optimum value for use within any particular system.



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Recommended value for R_{ext} :
 $10 [R_{rate} || R_{boost}] \leq R_x \leq 20 [R_{rate} || R_{boost}]$

FIGURE 2. External Circuitry Used to Insure Correct PLL Lock to a Pulse-Paired Synchronization Field

VCO JITTER

The inherent purity of the VCO's operating frequency is a key element in the accuracy of the data separator/synchronizer window generation. Any "jitter" present in the VCO frequency (any modulation of the period of the waveform by noise or any other source) will degrade the performance of the PLL. Within National's initially released DP8451/55/61/62/65 data separators-synchronizers, it has been found that maintaining a value of R_{rate} at or below 820Ω has a stabilizing effect on the jitter performance of the VCO circuitry. We recommend the following guidelines be followed in the selecting of charge pump resistors and loop filter components for these circuits (see Table I):

- 1) An 820Ω value resistor should be substituted for the originally recommended value of $1.5\text{ k}\Omega$.
- 2) Although this new R_{rate} value is below the original DP8451/55/61/62/65 specification limit, a substitute

requirement has been placed on both R_{rate} and R_{boost} to maintain proper circuit operation:

$$R_{rate} \parallel R_{boost} \geq 350\Omega$$

(i.e., the parallel value of R_{rate} and R_{boost} should not fall below 350Ω .)

- 3) If the inclusion of an 820Ω value for R_{rate} means a component change within an existing system (i.e., the user had been employing some higher value), all other component values associated with the loop filter must also be modified in order to maintain the original PLL response characteristics within the disk data field:

Define: $M = R_{rate}(\text{old})/820$ [eg., $(1500/820)$]. Then,

$$CLF1' = CLF1 * M$$

$$CLF2' = CLF2 * M$$

$$RLF1' = RLF1 / M$$

- 4) Additionally, in the cases where the Quadrature lock circuitry are in use:

$$R_{ext}' = R_{ext} / M$$

TABLE I. Data Separator/Synchronizer Reference List

Device	Synchronized Codes	Separated Codes	Frequency Lock	Window Centering Trim
DP8461	MFM; 1, N	MFM	Reference & 2T (MFM)	None
DP8462	2, 7 MFM; 1, N	None	Reference; 2, 7 (3T or 4T, Optional)	Optional
DP8465	2, 7 MFM; 1, N	MFM	Reference	None
DP8451	MFM; 1, N	None	Reference, 2T (MFM)	None
DP8455	2, 7 MFM; 1, N	None	Reference	None
DP8459	1, N; 2, 7; MFM; GCR	None	All (1T-4T, Optional)	5-Bit Digital Strobe

Note 1: DP8461 and DP8451 pinouts match the DP8465 and DP8455, respectively; for use with hard and psuedo-hard sectoring only.

Note 2: DP8462 incorporates optional frequency acquisition for 2, 7 synchronization fields, but may be used as a data synchronizer for any disk code.

Note 3: DP8451 and DP8455 also available in PCC package (20 pin).

PRINTED CIRCUIT BOARD LAYOUT RECOMMENDATIONS

As with any high-frequency analog circuitry, care should be taken in PC board layout when using the DP8465 family of data synchronizers. The following is a list of practical guidelines intended to help insure sound, trouble-free operation with these devices.

- 1) Establish a local V_{CC} island or net, separate from the main V_{CC} plane, to which the device and its associated passive components can be connected. V_{CC} supply filtering should be liberal and in very close proximity to the chip. The electrical lead length of the filter capacitance between the V_{CC} and ground pins themselves should be as short as possible (minimizing lead inductance). Inclusion of a quality high-frequency capacitor, such as a 1000 pF silver-mica capacitor, in parallel with a ceramic 0.1 μ F capacitor, is recommended. (Note: the chip is particularly sensitive to inadequately filtered switching supply noise.)
- 2) Effective capacitive bypassing of the R_{boost} and R_{rate} pins directly to the V_{CC} pin is very important. Again, use quality, high-frequency capacitors and maintain the shortest possible electrical lead length.
- 3) Use the main digital ground plane for all grounding associated with the device. The ground pin and the PG1 pin should tie directly to this plane.
- 4) Do not locate the chip in a region of the PC board where large ground plane currents are expected.
- 5) Locate all passive components associated with the chip as close to their respective device pins as possible.
- 6) Orient the chip's external passive components so as to minimize the length of the ground-return path between each component's ground plane tie point and the chip's ground pin. (Ground noise at the loop filter components, RLF1, CLF1 and CLF2, which is not identically present at the ground pin (common mode), is coupled through the filter components into the VCO control voltage pin.)
- 7) Include no planing whatsoever (V_{CC} or ground) directly between adjacent pins. This will minimize parasitic capacitance at each pin. Planing between the two pin rows, however, is recommended (directly beneath the package).
- 8) Avoid running signal traces between pins.
- 9) Run no digital signal lines between or adjacent to the analog pins or signal traces (pins 1 through 7 and PG3) in order to avoid capacitive coupling of digital transients.
- 10) Minimize the total lead length of the C_{VCO} capacitor. Inductance in this path degrades VCO performance, as does parasitic pin capacitance.
- 11) Do not place any bypass filtering at the R_{VCO} pin (minor coupling of the VCO waveform into this pin is normal and acceptable).
- 12) Eliminate negative-going voltage transients (undershoot) at the digital input pins (pre-termination of driving lines may be necessary) to avoid drawing transient input-clamp-diode current from the device pins.
- 13) Minimize digital output loading; i.e., if outputs must drive large loads or long lines, employ buffers.
- 14) Allow unused digital output pins to float, unconnected to any net.
- 15) Avoid locating the chip within strong electromagnetic fields. If possible, choose the "quietest" region of the board.
- 16) If chip socketing is desired, use a low-profile, low mutual capacitance, low resistance, forced-insertion type (socket-strips are recommended). Avoid the use of "ZIP-DIP's".
- 17) Do not use wire-wrap interconnect, even in an evaluation set-up.
- 18) Make allowance for pin-to-pin capacitance when determining C_{VCO} (Typically 4–5 pF) from data sheet formula.

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