Development of an Extensive SPICE Macromodel for "Current-Feedback" Amplifiers

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ABSTRACT

A current-feedback amplifier macromodel has been developed which simulates the more common small-signal effects such as small-signal transient response and frequency response as well as temperature effects, noise, and power supply rejection ratio. Also modeled are large-signal effects such as non-linear input transfer characteristics and input/output slew rate limiting.

Detailed descriptions of each stage in the model will be presented with examples of model performance and correlation to actual device behavior.

INTRODUCTION

With the increasing complexity and shorter design cycles of today's designs, computer modeling with SPICE (Simulation Program with Integrated Circuit Emphasis) is becoming more popular. This is especially true with high-speed designs utilizing the latest in current-feedback amplifiers. However, an accurate, detailed macromodel for current-feedback amplifiers with good convergence characteristics has not yet been available.

MACROMODELING PHILOSOPHY

The philosophy used in creating this macromodel was a desire to design a model that would simulate the typical behavior of a current-feedback amplifier to within 10% of typical parameters while executing much faster than a device level model. Also, the macromodel would act as a development platform for effects not normally included in other models such as temperature effects, noise, and many of the other second and third order effects that are characteristic in current-feedback amplifiers such as the LM6181.

THE LM6181

National Semiconductor's monolithic current-feedback amplifier, the LM6181, offers the designer an amplifier with the high-performance advantages of current-feedback topology without the high cost associated with hybrid devices. The LM6181 has a bandwidth of 100 MHz, slew rate of 2000 V/μs, settling time of 50 ns (0.1%), and 100 mA of output current drive. A special output stage allows the LM6181 to directly drive a 50Ω or 75Ω back-terminated coax cable. To understand how this device functions, a description of current-feedback amplifiers is in order.

CURRENT-FEEDBACK AMPLIFIERS

Figure 1 shows the block diagram for the current-feedback amplifier. The main difference when compared to voltage-feedback amplifiers (VFA's) is that in the current-feedback topology, a unity gain buffer drives the inverting input. Since this is an inherently low impedance, the feedback error signal is treated as a current rather than a voltage. During input transients, an error current will flow into or out of the input buffer. This current is then mirrored to a current-to-voltage converter (Zt(s)) which consists of a large ($\approx$ 2 MΩ) transimpedance and an output buffer. Since the large transimpedance is analogous to the large voltage gain of VFA's, the output voltage is servo'ed to a value which causes the current through Rf and Rg to cancel the current in the input buffer.

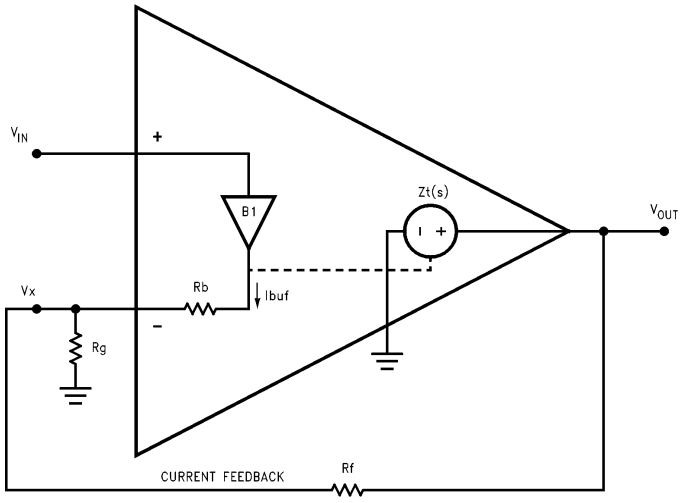

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FIGURE 1. Block Diagram of a Current-Feedback Amplifier

ANALYSIS OF CURRENT-FEEDBACK TOPOLOGY

From the simplified current-feedback amplifier schematic in *Figure 2*, it can be observed that the inverting (−IN) terminal is driven by a unity gain buffer stage. Transistors Q3 and Q4 make up the high-impedance input (+IN) to the buffer while Q5 and Q9 comprise a push-pull stage whose low output impedance is determined by $V_T/(I_C Q5 + I_C Q9) = V_T/(I1 + I2)$ assuming I1 and I2 are equal. The function of the input buffer is to drive the inverting input to the same voltage as the non-inverting input much like a voltage-feedback amplifier does via negative feedback. Transistors Q6, Q7, Q8, Q10, Q11 and Q12 form a pair of Wilson current mirrors which transfer the output current of the input buffer to a high-impedance (Zt) node. The equivalent capacitance (C_C) at this node is charged to the value of the output voltage. This voltage is then conveyed to a second buffer made up of Q14, Q15, Q17 and Q18 which drives the output pin of the amplifier. Short-circuit current limiting is performed by transistors Q19 and Q20. Back on the input of the amplifier, Q1 and Q2 provide a slew rate enhancement effect. For low closed-loop gains and large input steps these transistors turn on and increase the current available to the input buffer. This causes a transient increase in the current available to charge the compensation capacitor via the current mirrors, resulting in a faster slew rate for low gains. Now that the simplified circuit has been described, it will be informative to analyze the block diagram for the model.

By summing the currents at node Vx in *Figure 1* and using the fact that $V_O = I_{buf} \times Zt(s)$, the transfer function of the non-inverting configuration can be determined to be:

$$\frac{V_o}{V_{in}} = \left(1 + \frac{Rf}{Rg}\right) \times \left[\frac{1}{1 + \dfrac{Rf + \left[1 + \dfrac{Rf}{Rg}\right] \times Rb}{Zt(s)}}\right] \quad (1)$$

where Zt(s) is the open-loop transimpedance as a function of complex frequency. Notice, in equation 1, the $1 + Rf/Rg$ term on the left is the standard closed-loop voltage gain equation for non-inverting amplifiers while the term on the right is an error term. The $1 + Rf/Rg$ in the error term is the noise gain of the amplifier and Rb is the input buffer's quiescent output impedance ($\approx 30\Omega$ for the LM6181). If Zt(s) is assumed to be large, the error term goes to 1. The closed-loop bandwidth is defined as the frequency at which the magnitude of the error term equals $1/\sqrt{2}$ (−3 dB). If Zt(s) is approximated to be a single pole function, then:

$$Zt(s) = \frac{Zt(dc)}{1 + s \times Zt(dc) \times C_C} \quad (2)$$

where C_C is the value of the internal compensation capacitor in *Figure 2*. By substituting equation 2 for Zt(s) in equa-

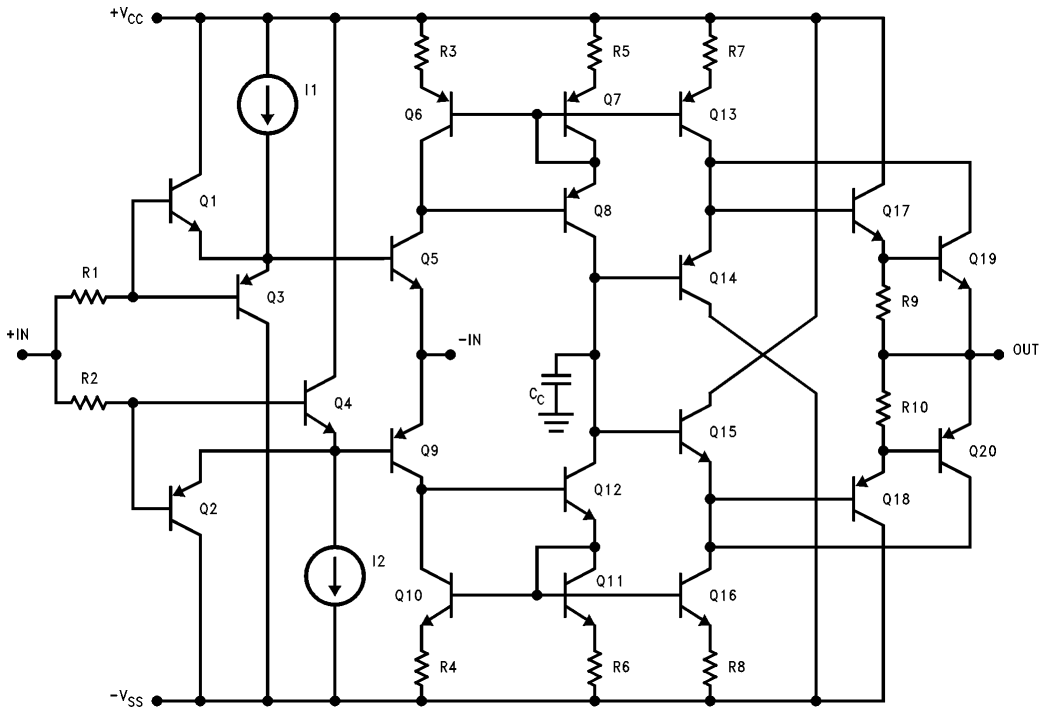

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FIGURE 2. LM6181 Simplified Circuit

tion 1 and assuming Zt(dc) is much larger than Rf, the closed-loop bandwidth can now be found to be:

$$bw = \frac{1}{2 \times \pi \times C_C \left[Rf + \left(1 + \frac{Rf}{Rg} \right) \times Rb \right]} \quad (3)$$

If the input buffer output resistance (Rb) times the noise gain of the amplifier (1 + Rf/Rg) is assumed to be small compared to Rf, equation 3 reduces to:

$$bw = \frac{1}{2 \times \pi \times C_C \times Rf} \quad (4)$$

Notice that the ideal closed-loop bandwidth in equation 4 is dependent only on the value of the internal compensation capacitor (C_C) and the feedback impedance (Rf). A recommended value for Rf is usually specified in the manufacturer's datasheet (Rf = 820Ω for the LM6181). Therefore, if the above assumptions are valid, there is theoretically no reduction in bandwidth as Rg is decreased to increase closed-loop gain.

Another special feature of the current-feedback amplifier is the theoretical absence of slew-rate limiting. Since the total output current of the input buffer is available to charge the compensation capacitor (C_C), the slew rate is proportional to the output voltage [4].

$$SR = \frac{I_{buf}}{C_C} = \frac{V_{OUT}}{C_C \times Rf} \quad (5)$$

This simplified analysis is adequate for small closed-loop gains; however, since Rb is typically several tens of ohms, the bandwidth and slew rate will be less than ideal for large gains. Also, there are slew-rate characteristics associated with the input buffer that are dominated by the slew-rate enhancement transistors (Q1 and Q2 in *Figure 2*) and stray package capacitances. All these second order effects are included in the macromodel input stage to achieve accurate simulation results.

THE INPUT STAGE

Figure 3 shows the macromodel input stage which performs many important functions such as the simulation of input buffer output impedance, input/output slew rate, supply voltage dependent input bias current and offset voltage, input capacitance, CMRR and noise [2]. Voltage-controlled current-sources GI1 and GI2 establish the input buffer's output impedance depending on supply voltage. For a given supply voltage, these current-sources can be determined by rearranging the standard bipolar transistor output resistance equation:

$$I1 = I2 = \frac{k \times T}{2 \times q \times Rb} \quad (6)$$

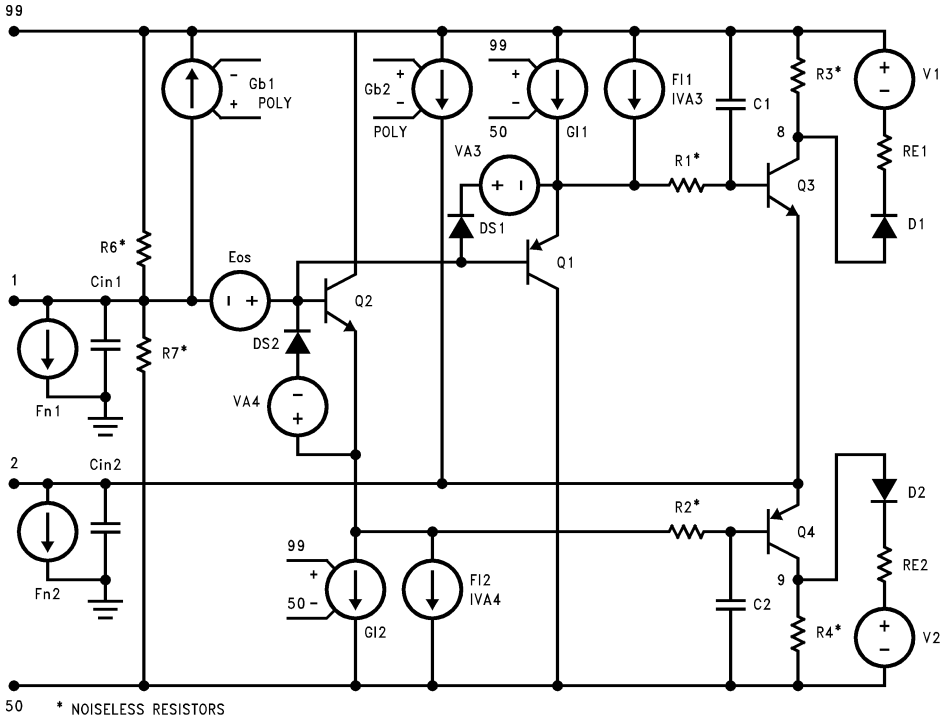

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FIGURE 3. Macromodel Input Stage. Simulates Input Impedances, Input Errors, CMRR, Input/Output Slew Rate, Input Capacitance, and Noise.

Rb is the output impedance of the input buffer and may be approximated with:

$$Rb = \frac{Zt}{A_{VOL}} \quad (7)$$

where A_{VOL} is the differential open-loop voltage gain of the amplifier from input to output. Equation 7 can be derived by shorting Rg and solving the transfer function in Equation 1.

The input stage slew rate is controlled by R1, R2, C1 and C2. The total current available to charge the capacitors C1 and C2 determines the maximum slew rate of the input stage. To reduce the number of PN junctions in the model, the slew rate enhancement transistors were modeled with diodes DS1 and DS2 and current-sources FI1 and FI2.

Input bias currents are simulated with polynomial-controlled current-sources Gb1 and Gb2 which are dependent on both supply voltage and temperature. Current-source Gb2 also models the residual input current (Ib) caused by imbalances in the input buffer as well as the error current caused by the input common mode voltage. The latter is called Inverting Input Bias Current Common Mode Rejection and is designated IbCMR on most datasheets. Fn1 and Fn2 transfer the current from the noise-current sources to the inputs of the amplifier.

The offset voltage-source, Eos, provides a supply voltage dependent input offset voltage and reflects the error voltages from the power supply rejection ratio stage, the thermal effect stage, and the noise-voltage source. Below is a diagram of the Eos polynomial-source and the effects that correspond to each term.

```
Eos 3 1 POLY(5) 99 50 45 0 47 0 57 0 59 0 61 -2.8E-3 9.3E-5 1 1 1 1
```

Input Offset Voltage Constant

Input Offset Voltage Supply Dependence

Positive Power Supply Rejection Ratio (PSRR+)

Negative Power Supply Rejection Ratio (PSRR−)

Input Offset Voltage Temperature Dependence

Input Referred Noise Voltage

Stray capacitance at the inputs of the amplifier modeled by $C_{in}1$ and $C_{in}2$ has a dramatic effect on the peaking in the amplifier's high frequency response. Common Mode Rejection Ratio can be modeled in the input stage by properly setting the early voltage (Vaf) of the input transistor models. A good starting point for the value of the early voltage is given by:

$$Vaf = \frac{2 \times V_T}{10^{\left[\frac{CMRR(db)}{20}\right]}} \quad (8)$$

Also, in the transistor model, a value for beta (BF) should be chosen. It should be large enough so that the base currents do not interfere with the input bias currents of the model, but not so large as to cause convergence problems during simulation.

The output of the input stage is the sum of the currents flowing through R3 and R4. The voltage across R3 and R4 is softly clamped by the V1, RE1, D1 and V2, RE2, D2 strings respectively. This effectively limits the current to the second stage yet still allows the second stage slew rate to increase for large input signals.

THE SECOND STAGE

The second stage of the macromodel *(Figure 4)* provides the open-loop transimpedance, the first pole, output clamping and supply dependent quiescent supply current. The voltage-controlled current-source G1 is controlled by a second order polynomial equation which calculates the current through R3 and R4 and reflects the sum directly into the second stage. By making the polynomial coefficients equal to the reciprocal of R3 and R4, the DC transimpedance of the model is simply equal to the value of R5. The dominant pole and output slew rate is established with capacitor C3 which is comparable in function to C_C in the LM6181 simplified circuit. Output clamping is performed with two diodes (D3–D4) each in series with a voltage-source (V3–V4). Clamping should be done here at the gain stage to prevent node 15 from reaching several thousands of volts which could cause convergence problems during simulation. Quiescent current is modeled with the combination of I3 and the R8–R9 series resistors. As the supply voltage increases, the current through R8 and R9 will increase ef-

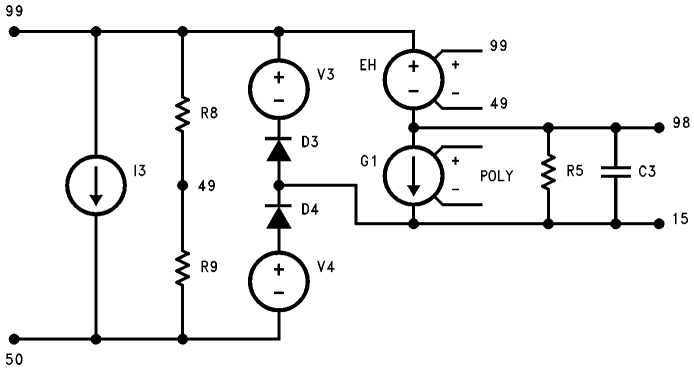

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FIGURE 4. The Macromodel Second Stage Models Open-Loop Transimpedance, First Pole, Output Swing Limiting, and Quiescent Supply Current.

fectively simulating that behavior in the real device. The value for resistors R8 and R9 can be calculated by dividing the change in supply voltage by the change in supply current ($\Delta V_S/\Delta I_S$) anywhere within the operating range of the amplifier. Current-source I3 is evaluated by taking the total supply current at a given voltage and subtracting off the current through all other significant supply loads. These loads are R8, GI1, GI2, and R3 so that:

$$I3 = Ivs\ @\ 15V - \frac{15}{R8} - 3 \times I1 \quad (9)$$

The $3 \times I1$ comes from the fact that the currents through GI1, GI2 and R3 are equal. Resistors R8 and R9 also act as a voltage divider and establish a common-mode voltage (V_H) for the model directly between the rails. If the supply rails are symmetrical, i.e., $\pm$15V, node 49 will be at zero volts. Voltage-controlled voltage-source EH measures the voltage across R8 and subtracts an equal voltage from the positive supply rail to provide a stiff point between the rails (node 98) to which many other stages in the model are referenced.

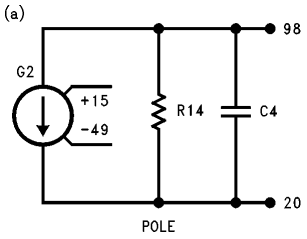
FREQUENCY-SHAPING STAGES

In keeping with the philosophy of providing a macromodel that is as accurate as possible, it has been determined that the model must be capable of easily accommodating as many poles and zeros that are necessary to precisely shape the magnitude and phase response of the model [5]. This is accomplished with telescopic frequency-shaping stages that each have unity DC gain making it easier to add poles and zeros without changing the DC gain of the model. The LM6181 macromodel has four high frequency pole stages and no zero stages, however, each of the three types of frequency-shaping stages will be discussed in detail should the reader wish to develop macromodels for other amplifiers.

The first type of frequency-shaping stage is a pole. In *Figure 5a*, resistor R14 is set to 1 kΩ. This value is chosen to reduce the thermal noise associated with this resistor and to simplify the calculations for the other components in the stage. Current-source G2 is controlled by the output voltage from the previous stage and its g_m is set to the reciprocal of R14 or 10^{-3} to maintain unity DC gain of the stage. Capacitor C4 rolls off the gain at high frequencies and is set with the standard pole equation: $C = 1/(2 \times \pi \times f_P \times R)$ where f_P is the -3 dB frequency of the pole in Hz.

Even though SPICE will attempt to process a bare zero stage, in the real world, such a circuit is actually non-causal and SPICE may not converge because an ideal inductor can generate an infinite voltage if the current though it changes instantaneously. To introduce a zero in the frequency response of the model, a pole must be combined with the zero to form a zero/pole or a pole/zero stage. The circuit for the zero/pole stage is shown in *Figure 5b*. This stage will have unity DC gain if the g_m of G5 is set to the reciprocal of R19. As the frequency increases, L1's impedance starts to increase until R18 dominates causing the gain to level off.

The last type of frequency-shaping stage is the pole/zero circuit shown in *Figure 5c*. As the frequency increases, the gain starts at unity and decreases until the impedance of the capacitor is negligible compared to its series resistor. For more information on poles and zeros, see references [7] and [8].



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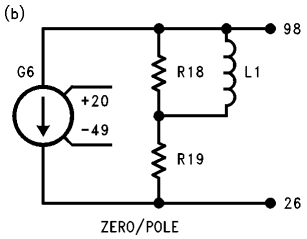
$$R14 = 1\ k\Omega$$

$$G2 = \frac{1}{R14} = 10^{-3}$$

$$C4 = \frac{1}{2 \times \pi \times f_P \times R14}$$



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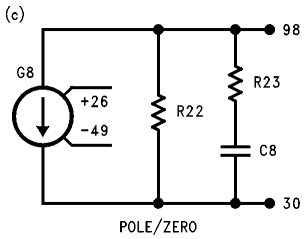
$$R19 = 1\ k\Omega$$

$$G6 = \frac{1}{R19} = 10^{-3}$$

$$R18 = \left(\frac{f_p}{f_z} - 1\right) \times R19$$

$$L1 = \frac{R18}{2 \times \pi \times f_P}$$



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$$R22 = 1\ k\Omega$$

$$G8 = \frac{1}{R22} = 10^{-3}$$

$$R23 = \frac{R22}{\frac{f_z}{f_p} - 1}$$

$$C8 = \frac{1}{2 \times \pi \times f_z \times R2}$$

FIGURE 5. Macromodel Frequency-Shaping Stages

PSRR STAGE

Power supply rejection ratio is a parameter that many vendors have previously neglected in their SPICE models. Since AC power supply impedance is extremely critical in high-speed amplifier designs, both DC and AC PSRR were included in this model so that the designer can explore the effects of supply bypassing. The PSRR stage (see *Figure 6*) consists of two attenuation circuits controlled by the voltage from each rail to ground whose gains increase at 20 dB per decade.

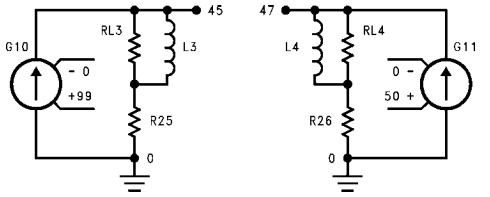

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FIGURE 6. Macromodel PSRR Stage

The signals generated at nodes 45 and 47 are directly reflected to the input of the amplifier via the second and third terms of the Eos polynomial-controlled source. Since the PSRR stages are referenced to ground, a large offset voltage will be developed if the model is operated from asymmetrical supplies. This compromise was necessary in order to include the PSRR effects; however, if operation on asymmetrical supplies is required, the PSRR effects can be disabled by changing the second and third polynomial terms in Eos from 1 to 0. For example, change:

```
Eos 3 1 POLY(5) 99 50 45 0 47 0 57 0 59 61 −2.8E-3 9.3E-5 1 1 1 1
```

to:

```
Eos 3 1 POLY(5) 99 50 45 0 47 0 57 0 59 61 −2.8E-3 9.3E-5 0 0 1 1
```

To set the component values in the PSRR stages, R25 and R26 are arbitrarily chosen to be 10Ω The g_m's of the current sources are set so that the DC gain of each stage is equal to the DC value of the PSRR or:

$$G10 = 10^{\frac{PSRR}{20}} \times \left[\frac{1}{R25}\right] \quad (10)$$

where PSRR is the typical DC rejection ratio in dB. The inductors, L3 and L4, determine the 3 dB frequency of each stage and can be set with:

$$L = \frac{R}{2 \times \pi \times f_{3dB}} \quad (11)$$

Resistors RL3 and RL4 cancel the zeros associated with the inductors at a frequency above the unity gain frequency of the amplifier. This helps with transient convergence when simulating inductive or resistive power supply lines.

THERMAL EFFECTS

The predominant thermal effects of a current-feedback amplifier are the change in offset voltage and input bias current as a function of temperature. The macromodel stages in *Figure 7* are used to simulate these effects by utilizing the SPICE temperature dependent resistor model which is controlled with the equation [9]:

$$R(\Omega) = <value> \times (1 + TC1 \times (T - Tnom) + TC2 \times (T - Tnom)^2) \quad (12)$$

where <value> is the value of the resistor at Tnom (usually 27°C), T is the temperature in °C, TC1 is the linear temperature coefficient, and TC2 is the quadratic temperature coefficient. The equation will fit a quadratic curve through three points in a temperature graph by solving three equations with three unknowns. Since SPICE will give an error message if a resistor goes negative at any temperature, an offset bias is added to the resistor value whose voltage is then subtracted from the respective input error source (Gb1, Gb2, or Eos).

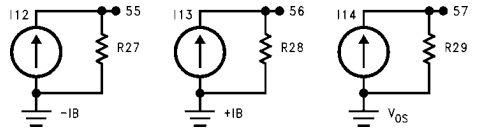

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FIGURE 7. Macromodel Thermal Effect Stages

The voltages generated at nodes 55, 56, and 57 are scaled and used to control the input error sources Gb2, Gb1, and Eos respectively. The simulated results compare quite closely to the typical curves for the actual device as can be seen in *Figures 16* and *17*.

NOISE STAGES

The addition of noise effects to any macromodel is similar to the techniques used for input offset voltage and drift. The total amplifier noise is lumped together and referred to the input of the model. Before noise sources are added, however, the model has to be rendered essentially noiseless. This is easier than it sounds, though, because noise adds vectorially. The total contribution of several noise sources can be found by:

$$En_{total} = \sqrt{(En1)^2 + (En2)^2 + (En3)^2 \ldots}$$

So, a latent noise source within the model will have to be reduced to only ¼ of the desired noise level to maintain an accuracy of less than 3% ($\sqrt{1 + 0.25^2} = 1.03$). Most of the latent amplifier model noise comes from thermal noise generated by large-value resistors commonly used in macromodels. To reduce this noise, the resistor values are scaled so their thermal noise is negligible compared to the desired noise of the amplifier. If resistor scaling is not possible, as was the case with several resistors in the input stage of the LM6181 macromodel, a *noiseless resistor* can be used. A noiseless resistor is created by utilizing a voltage-controlled current-source (G device) with the same input and output terminals whose g_m is set to the reciprocal of the required value of resistance (see *Figure 3* and the LM6181 netlist). The only caveat with using noiseless resistors is that a current-source is considered an open circuit when SPICE calculates the initial bias point of the circuit. Therefore, at least one other device must be connected to the nodes of the noiseless resistor to avoid ''floating node'' errors.

Now that the macromodel is rendered essentially noiseless, lumped noise sources can be added and referred to the input sources. *Figure 8* shows the equivalent noise model which consists of an ideal noiseless amplifier, two noise-current generators (i_{n+} and i_{n-}), from each input to ground and a noise-voltage generator (e_n) in series with non-inverting input.

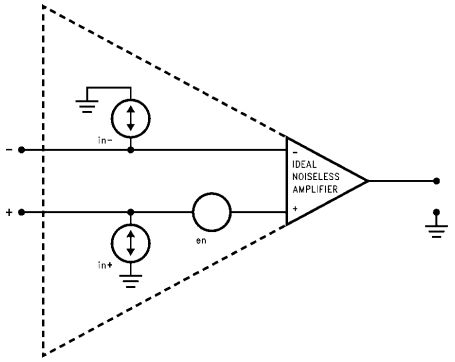

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FIGURE 8. Equivalent Amplifier Noise Model

The noise-current generators are called Fn1 and Fn2 in the macromodel input stage *(Figure 3)*, while the noise-voltage generator is included in the Eos polynomial-controlled source. The noise voltage or current which is actually referred to the input generators comes from separate noise source stages in the macromodel.

The noise-voltage circuit *(Figure 9)* generates both 1/f and white noise by using a 0.1V voltage-source which lightly biases a diode-resistor series combination. White noise is simply the thermal noise-current generated in the resistor which follows the spectral power density (per unit bandwidth) equation below:

$$i_n^2 = \frac{4 \times k \times T}{\text{Resistance}} \qquad (14)$$

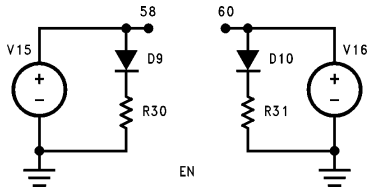

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FIGURE 9. Macromodel Noise Voltage Stage

where i_n is the noise-current through the resistor, k is Boltzmann's constant (1.381×10^{-23}), and T is the temperature in °K (°C + 273.2°). By taking the square root of both sides of the equation and multiplying by resistance, the required value of resistance can be found for a given noise-voltage spectral density with:

$$R = \frac{e_n^2}{2 \times 4 \times k \times T} \qquad (15)$$

where e_n is the white noise voltage of the amplifier per $\sqrt{\text{Hz}}$. The "2" in the denominator comes from the fact that the voltage is taken differentially across two identical circuits of the noise-voltage source (nodes 58 and 60). The reason for using two identical circuits is so that a DC voltage would not be created which would be seen as an offset voltage on the input.

Flicker noise or 1/f noise-voltage comes from the SPICE diode model. By setting the flicker noise exponent (AF) to 1 and properly setting the flicker noise coefficient (KF), the resulting noise voltage will accurately simulate the 1/f noise-voltage spectral density with the correct "corner frequency". Equation 16 shows the noise-current that results from the SPICE diode model where Id is the DC diode current and the $2 \times q \times Id$ term is negligible compared to the 1/f noise of the amplifier.

$$i_n^2 = 2 \times q \times Id + KF \times \frac{Id^{AF}}{\text{FREQUENCY}} \qquad (16)$$

To determine the value for KF in the macromodel, the following equation can be used:

$$KF = \frac{Ea^2}{R^2 \times Id \times 2} \qquad (17)$$

where Ea is the noise-voltage spectral density of the amplifier at 1 Hz and Id is the DC current through the diode which can be determined with the standard Schottky diode equation. Again, the "2" in the denominator comes from the fact that the noise output is taken differentially across two identical circuits.

The white portion of the amplifier's noise current is modeled by utilizing the thermal noise current of a resistor in series with a zero volt voltage-source (see *Figure 10*).

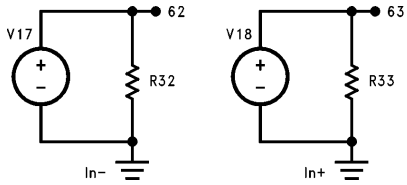

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FIGURE 10. Macromodel White Noise-Current Generators

Since the noise-current through each of the resistors is measured with the voltage-sources and directly referred to the respective current-controlled current-source on the input, the value for each resistor can be found by rearranging Equation 14 or:

$$R = \frac{4 \times k \times T}{i_n^2} \qquad (18)$$

The i_n term is the broad-band or white noise-current spectral density at the respective input of the amplifier.

To simulate the 1/f component of the noise-current, the flicker noise coefficient (KF) in the model for each pair of input transistors is set to obtain the correct corner frequency. In the LM6181 macromodel, KF is set to 4.13×10^{-13} for Q1 and Q2 while KF is set to 6.7×10^{-14} for Q3 and Q4. The flicker noise exponent (AF) is left at its default value of 1.

The macromodel's noise curves are compared to the actual amplifier's curves in *Figures 18* through *21*. The simulation results are quite close to the actual noise characteristics of the amplifier. For more information on calculating and modeling amplifier noise, see references [3] and [9].

OUTPUT STAGE

After the input signal is amplified and frequency shaped, it is further processed by the output stage shown in *Figure 11*. The output stage performs three important functions, namely, simulation of output impedance, short-circuit current limiting, and dynamic supply current.

The intermediate output signal appears at the output of the last frequency-shaping stage as a high-source-impedance voltage referenced to V_H. Voltage-controlled voltage-source, E1, level shifts the intermediate output signal down from the positive rail and provides the output drive for the model. Output impedance is modeled with the combination of R35 and L5. Resistor R35 simulates the DC output impedance which determines the behavior of the model when driving heavy loads. Additionally, inductor L5 models the characteristic rise in output impedance as a function of frequency which is common to the emitter-follower output stage found in many amplifiers. Since an ideal inductor as modeled by SPICE has infinite Q, a bare inductor in the signal path can cause convergence problems if the current through it can change instantaneously. To lower the Q of the inductor and prevent convergence problems during simulation, a large value resistor, RL5, is placed across L5. Capacitor CF1 models stray capacitance across the feedback resistor which dramatically affects the high frequency response of the amplifier.

Short-circuit current limiting is also a necessary feature of any good amplifier macromodel. The diodes D5 and D6 each in series with a voltage-source V5 and V6 accomplish this function by effectively clamping the maximum voltage across R35. The value of the voltage-sources can be set with the following equation which was derived with the Schottky diode equation and summing the currents at node 40 assuming the output is shorted to ground.

$$V = R35 \times I_{SC} - \ln\left[\frac{V_{CC} - R35 \times I_{SC}}{I_S \times Zofr} + 1\right] \times V_T \quad (19)$$

The term Zofr is the output impedance of the last frequency shaping stage (1 kΩ in this case), I_S is the saturation current of the diode, and V_T is the thermal voltage k × T/q. Although it appears that the appropriate parameters are included in the equation, no attempt was made to model the dependence of short-circuit current on supply voltage or temperature.

Another behavior that is often not included in op-amp macromodels is dynamic supply current. If the output of the model is driven by an ideal voltage-source, the simulated output current of the model appears to come from nowhere, i.e., the supply currents do not change. This apparent violation of the second law of thermodynamics has been solved with diodes D7–D8, current-sources F5–F6, and associated circuitry. Since it is important to keep non-linear devices, such as diodes, out of the signal path, only an ideal ammeter, VA8, was inserted in the output driver to sense the sinking or sourcing of output current. Current-controlled current-source F5 mirrors the current sensed by VA8 and forces an equal current through either D7 or D8 depending on its polarity. If current is being sourced into the load, the current flows from the positive rail through E1 and VA8 to the output node and no supply current correction is necessary. However, if the output stage is sinking current from the load, the current flows from the output node up through VA8 and E1 into the positive rail. To compensate for this, F5 forces an equal current through D7 and ammeter VA7. This current is then mirrored to current-source F6 which pulls an equal amount of current out of the positive rail and forces it into the negative rail. Therefore, if the output stage is sourcing current, it appears to come from the positive rail, whereas current that is sinking from the load appears to go into the negative rail. The net result of all these extra devices is an output stage which closely models the behavior of the real amplifier.

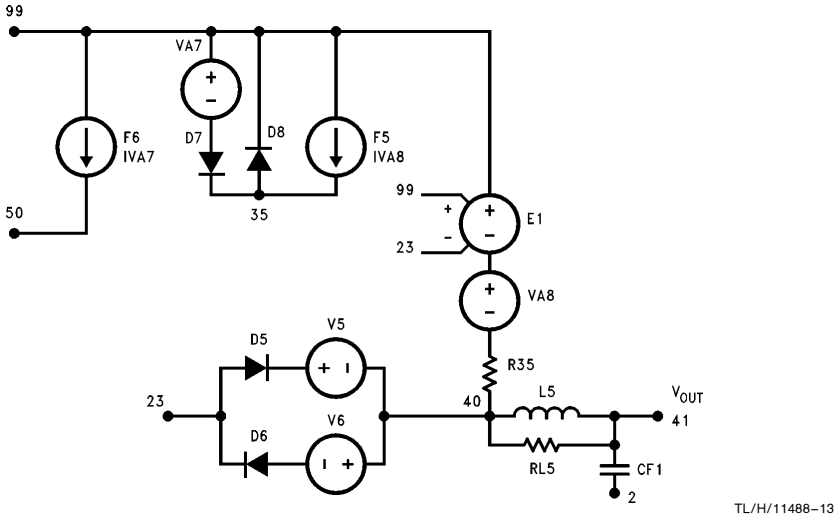

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FIGURE 11. Macromodel Output Stage

LM6181 Macromodel Netlist

```
****************************************
*LM6181 CURRENT FEEDBACK OP-AMP MACRO-MODEL
****************************************
*
*connections:     non-inverting input
*                 |  inverting input
*                 |  |  positive power supply
*                 |  |  |  negative power supply
*                 |  |  |  |  output
*                 |  |  |  |  |
*                 |  |  |  |  |
.SUBCKT LM6181    1  2  99 50 41
*
*Features:              (TYP.)
*High bandwidth =      100 MHz
*High slew rate =      2000 V/µs
*Current Feedback Topology
*NOTE: Due to the addition of PSRR effects, model must be operated
*      with symmetrical supply voltages. To avoid this limitation
*      and disable the PSRR effects, see Eos below.
*
********** INPUT STAGE **********
*
GI1 99  5 POLY(1) 99 50 243.75U 2.708E-6
GI2  4 50 POLY(1) 99 50 243.75U 2.708E-6
FI1 99  5 VA3 100
FI2  4 50 VA4 100
Q1 50 3 5 QPN
Q2 99 3 4 QNN
GR1  5 6 5 6 2.38E-4
*^4.2K noiseless resistor
C1  6 99 .468P
GR2 4 7 4 7 2.38E-4
*^4.2K noiseless resistor
C2  7 50 .468P
GR3 99 8 99 8 1.58E-3
*^633ohm noiseless resistor
V1 99 10 .3
RE1 10 30 130
D1 30 8 DX
GR4 50  9 50 9 1.58E-3
*^633ohm noiseless resistor
V2  11 50 .3
RE2 11 31 150
D2  9 31 DX
Q3  8 6 2 QNI
Q4  9 7 2 QPI
DS1 3 12 DY
VA3 12 5 0
DS2 13 3 DY
VA4 4 13 0
GR6 1 99 1 99 5E-8
*^20MEG noiseless resistor
GR7  1 50 1 50 5E-8
*^20MEG noiseless resistor
GB1  1 99 POLY(2) 99 50 56 0 -1.2E-6 4E-8 1E-3
FN1  1  0 V18 1
GB2 99  2 POLY(3) 99 50 1 49 55 0 18.5E-6 -1.5E-7 -1E-7 -1E-6
FN2  2  0 V17 1
EOS 3  1 POLY(5) 99 50 45 0 47 0 57 0 59 61 -2.8E-3 9.3E-5 1 1 1 1
*To run on asymmetrical supplies, change to 0..... ^ ^
```

```
CIN1 1  0 2P
CIN2 2  0 5.75P
*
******** SECOND STAGE **********
*
I3 99 50 4.47M
R8 99 49 7.19K
R9 49 50 7.19K
V3 99 16 1.7
D3 15 16 DX
D4 17 15 DX
V4 17 50 2.0
EH 99 98 99 49 1
G1 98 15 POLY(2) 99 8 50 9 0 1.58E-3 1.58E-3
*Fp1 = 27.96 KHz
R5 98 15 2.372MEG
C3 98 15 2.4P
*
********* POLE STAGE ***********
*
*Fp = 250 MHz
G2 98 20 15 49 1E-3
R14 98 20 1K
C4 98 20 .692P
*
********* POLE STAGE ***********
*
*Fp = 250 MHz
G3 98 21 20 49 1E-3
R15 98 21 1K
C5 98 21 .692P
*
********* POLE STAGE ***********
*
*Fp = 275 MHz
G4 98 22 21 49 1E-3
R16 98 22 1K
C6 98 22 .5787P
*
********* POLE STAGE ***********
*
*Fp = 500 MHz
G5 98 23 22 49 1E-3
R17 98 23 1K
C7 98 23 .3183P
*
********* PSRR STAGE ***********
*
G10 0 45 99 0 1.413E-4
L3 44 45 26.53U
R25 44  0 10
RL3 44 45 10K
G11  0 47 50 0 1.413E-4
L4  46 47 2.27364U
R26 46  0 10
RL4 46 47 10K
```

```
*
******** THERMAL EFFECTS **********
*
I12  0 55 1
R27  0 55 10 TC = 3.453E-3 7.93E-5
I13  0 56 1E-3
R28  0 56 1.5 TC = 9.303E-4 8.075E-5
I14  0 57 1E-3
R29  0 57 3.34 TC = 3.111E-3
*
********* NOISE SOURCES ***********
*
V15 58  0 .1
D9  58 59 DN
R30 59  0 726.4
V16 60  0 .1
D10 60 61 DN
R31 61  0 726.4
V17 62  0 0
R32 62  0 73.6
V18 63  0 0
R33 63  0 1840
*
********* OUTPUT STAGE ***********
*
F6 99 50 VA7 1
F5 99 35 VA8 1
D7 36 35 DX
VA7 99 36 0
D8 35 99 DX
E1 99 37 99 23 1
VA8 37 38 0
R35 38 40 50
V5 33 40 5.3V
D5 23 33 DX
V6 40 34 5.3V
D6 34 23 DX
CF1 41 2 2.1P
L5 40 41 31N
RL5 40 41 100K
*
********* MODELS USED ***********
*
.MODEL QNI NPN(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 6.7E-14)
.MODEL QPI PNP(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 6.7E-14)
.MODEL QNN NPN(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 4.13E-13)
.MODEL QPN PNP(IS = 1E-14 BF = 10E4 VAF = 62.9 KF = 4.13E-13)
.MODEL DX D(IS = 1E-15)
.MODEL DY D(IS = 1E-17)
.MODEL DN D(KF = 1.667E-9 AF = 1 XTI = 0 EG = .3)
.ENDS
```

SIMULATION ACCURACY

The real test of a macromodel is how the simulation results compare with the real-world device. The table below shows some of the amplifier parameters and how the simulation compares to actual device behavior. As can be seen, the goal of a 10% match between the model and the actual device was achieved.

A good figure of merit for a macromodel is the accuracy of its small-signal transient response. *Figures 14* and *15* show the small-signal response of the real LM6181 and the simulation output. Notice that the simulated over-shoot and frequency of ringing closely match that of the actual device. This is due to the accurate modeling of the frequency response and output impedance capabilities of the model.

CONCLUSION

A truly comprehensive SPICE compatible macromodel for current-feedback amplifiers has been developed. The macromodel includes effects such as accurate input transfer response, accurate AC response, temperature effects, DC and AC PSRR, and noise. Even with the addition of all these features, the macromodel's simulation speed is still more than twice as fast as a device level micromodel. The speed advantage of this macromodel mainly comes from the fact that it converges extremely well. Since careful attention was paid to convergence during the development of the model, there is no difficulty establishing a bias point or dealing with large input signals. With detailed and accurate vendor supplied macromodels such as the one described in this paper, the designer can easily verify the effects of strays and amplifier limitations in his circuit.

Parameter	Typical Value	Simulation Results	% Error
$Z_{t(dc)}$ RI = 1 kΩ	127 dBΩ	126.6 dBΩ	4.5%
$BW_{3\ dB}$ A_V = −1 RI = 1 kΩ	100 MHz	103.9 MHz	3.9%
I_{B+}	1.5 μA	1.5 μA	0.0%
I_{B-}	−4.0 μA	−4.0 μA	0.0%
V_{OS}	−3.34 mV	−3.3 mV	1.2%
Isupp	7.5 mA	7.7 mA	2.7%
Pulse Resp. Overshoot	35%	34.8%	0.6%
Slew Rate V_{IN} = ±10V	1400 V/μs	1468 V/μs	4.8%
I_{SC}	130 mA	136.8 mA	5.2%
e_n	5 nV/$\sqrt{Hz}$	4.9 nV/$\sqrt{Hz}$	2.0%
i_{n+}	3 pA/$\sqrt{Hz}$	2.96 pA/$\sqrt{Hz}$	1.3%
i_{n-}	16 pA/$\sqrt{Hz}$	15.1 pA/$\sqrt{Hz}$	5.6%

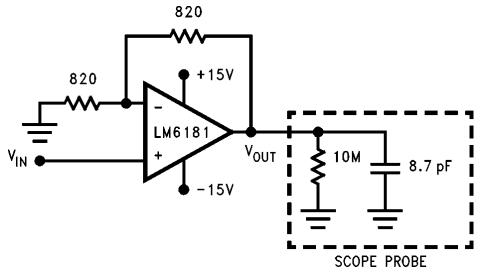

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FIGURE 12. Non-inverting amplifier. $A_V = +2$. It is very important to include a model of the scope probe on the output of the amplifier to obtain reasonable results from the simulation.

```
*LM6181 Small-Signal Response. Av = +2.
*Rf = Rg = 820ohm.
*
XAR1 3 2 7 4 6 LM6181
VP  7 0  15V
VN  4 0 -15V
VIN 3 0 PULSE (-.2V .2V 40N .2N .2N)
RF  6 2 820ohm
RI  2 0 820ohm
RL  6 0 10MEG
CL  6 0 8.7pF
.LIB CF.LIB
.OPTIONS RELTOL = .0001 CHGTOL = 1E-20
.TRAN/OP .1N 200N
.PROBE
.END
```

FIGURE 13. Non-Inverting Amplifier Netlist [9]

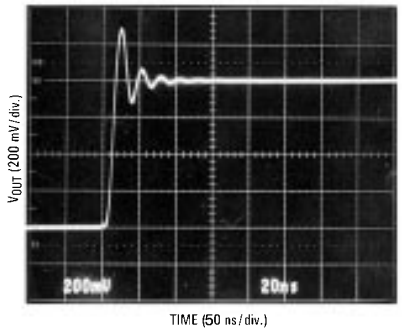

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FIGURE 14. LM6181 Small-Signal Transient Response

LM6181 Small-Signal Response
$A_V = +2$
$Rf = Rg = 820\Omega$

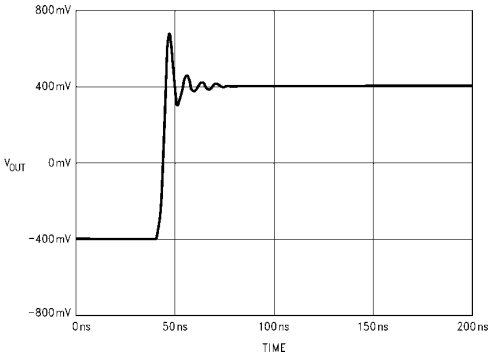

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FIGURE 15. LM6181 Simulated Transient Response

LM6181
V_{OS}, $+I_B$, $-I_B$ vs Temperature

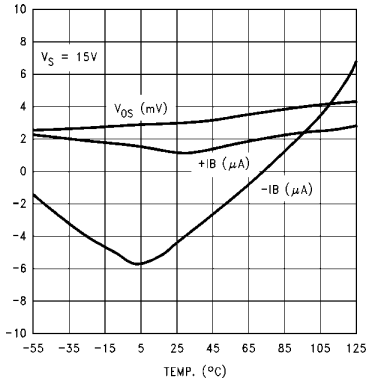

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FIGURE 16. LM6181 Temperature Effects

LM6181 V_{OS}, $+I_B$, $-I_B$

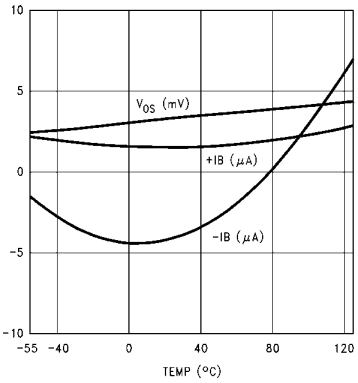

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FIGURE 17. LM6181 Simulated Temperature Effects

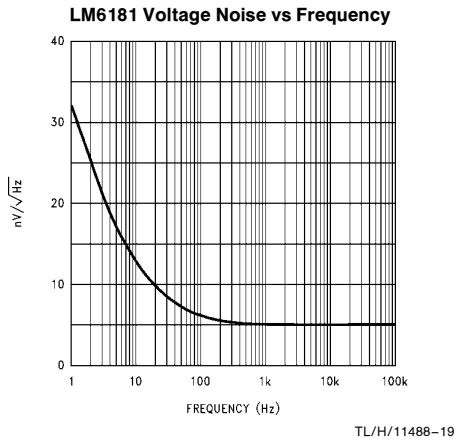

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FIGURE 18. LM6181 Voltage-Noise Response

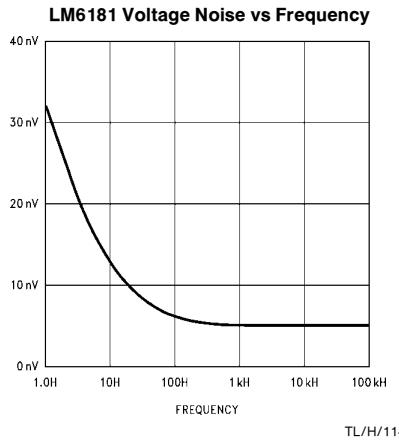

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FIGURE 19. LM6181 Simulated Voltage-Noise Response

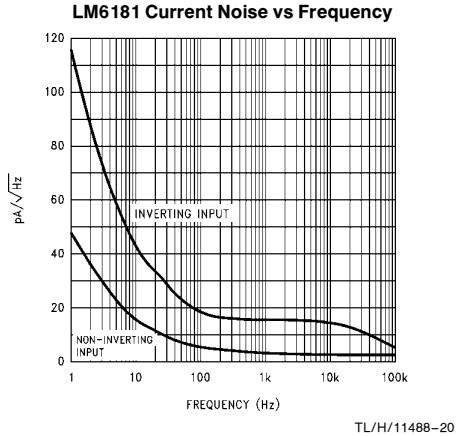

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FIGURE 20. LM6181 Current-Noise Response

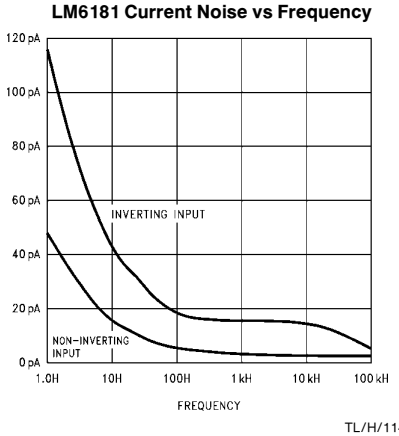

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FIGURE 21. LM6181 Simulated Current-Noise Response

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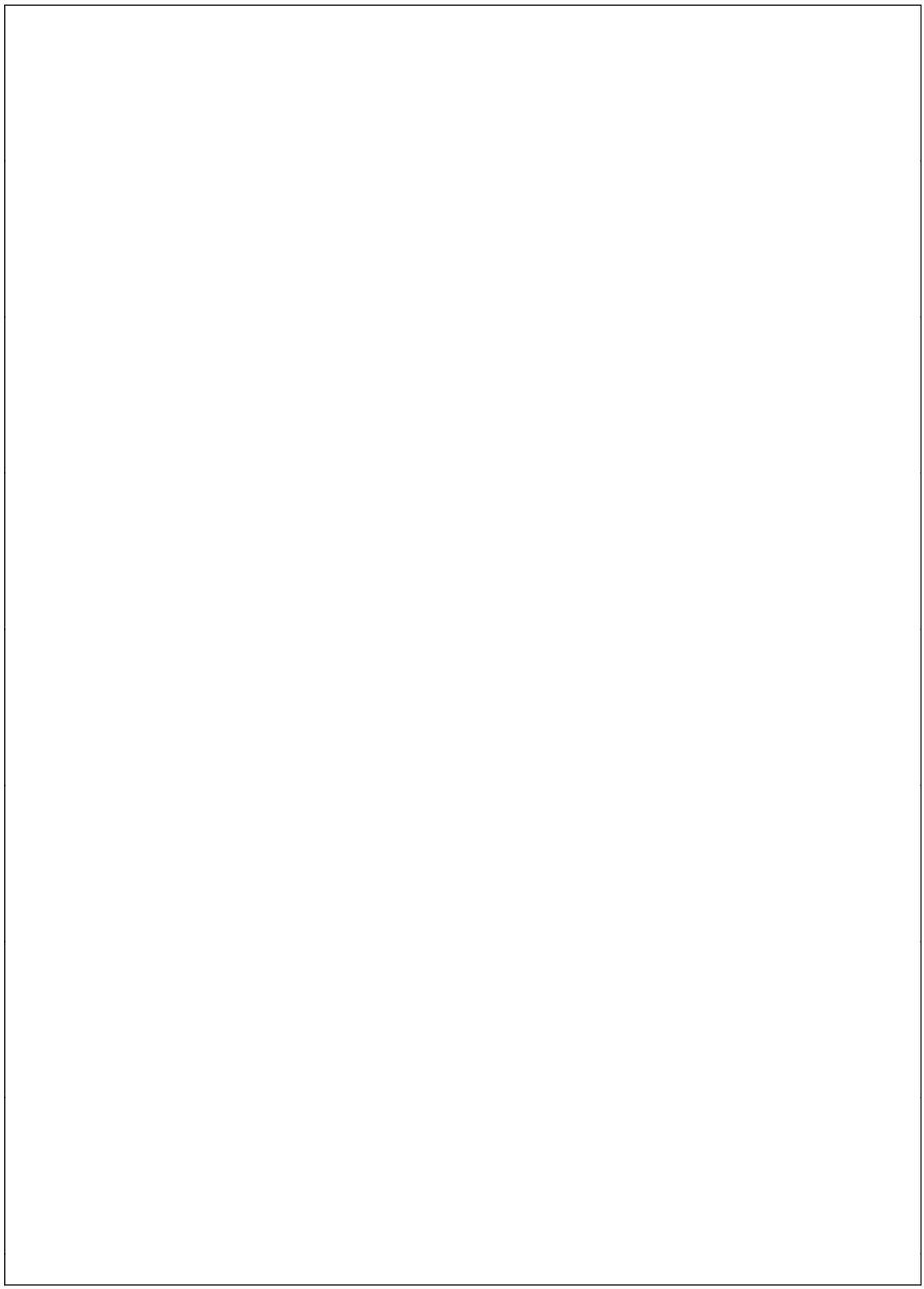

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