1982

ADVANCED SCHOTTKY DATABOOK

NATIONAL SEMICONDUCTOR CORPORATION

Advanced Schottky

The DM54/74AS family of devices are designed to meet the needs of system designers who require the ultimate in speed. AS achieves the fastest prop delays bipolar technology can offer (2 ns per gate). The AS family also offers significant reduction in power dissipation (8 mw per gate) over present Schottky (54/74S) with toggle rate capability of up to 200 MHz.

The AS family is TTL pinout compatible and offers Schottky (54/74S) drive capability with better fan out, higher noise immunity and faster operation.

For maximum design flexibility and elimination of special drawings, the AS family will be introduced with $\pm$ 10% V_{CC} over the military and commercial full temp range as standard product. Furthermore, all switching characteristics are guaranteed over the full temperature and V_{CC} range.

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Numerical Index

Section 1 — Advanced Schottky

Numerical Index (continued)

National Semiconductor

ADVANCED SCHOTTKY

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC} (1) 7V
Input Voltage, V_I: All Inputs 7V
I/O Ports 5.5V
Off State (High Level) Voltage Applied to Open-Collector Outputs 7V
High Level Voltage Applied to 3-State Outputs 5.5V
Operating Free-Air Temperature Range:
SN54AS −55°C to 125°C
SN74AS 0°C to 70°C
Storage Temperature Range −65°C to 150°C

Recommended Operating Conditions

Parameter		Standard Output			Buffer Output			Bus Driver Output			Unit
		Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
Supply Voltage	54/74AS	4.5	5.0	5.5	4.5	5.0	5.5	4.5	5.0	5.5	V
High Level Input Voltage, V_{IH}	54/74AS	2.0			2.0			2.0			V
Low Level Input Voltage, V_{IL}	54/74AS			0.8			0.8			0.8	V
High Level Output Current, I_{OH} (2)	54AS			−2.0			−12			−40	mA
	74AS			−2.0			−15			−48	mA
High Level Output Voltage, V_{OH} (3)	54/74AS			5.5			5.5			5.5	V
Low Level Output Current, I_{OL}	54AS			20			32			40	mA
	74AS			20			48			48	mA
Operating Free-Air Temperature, T_A	54AS	−55		125	−55		125	−55		125	°C
	74AS	0		70	0		70	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Parameter		Conditions		Standard Output			Buffer Output			Bus Driver Output			Unit
				Min	Typ(4)	Max	Min	Typ(4)	Max	Min	Typ(4)	Max	
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2			−1.2			−1.2	V
V_{OH}	High Level Output Voltage (2)	I_{OH} = MAX V_{CC} = 4.5V					2.4	3.2		2			V
		I_{OH} = −2.0mA		V_{CC}−2V			V_{CC}−2V			V_{CC}−2V			V
I_{OH}	High Level Output Current (3)	V_{CC} = 4.5V V_{OH} = 5.5V				0.1			0.1			0.1	mA
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5		0.35	0.5		0.35	0.5	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5V V_I = 7V				0.1			0.1			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_I = 2.7V				20			20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5			−0.5			−0.5	mA
I_O	Output Current (5)	V_{CC} = 5.5V V_O = 2.25V		−30		−110	−30		−110		−150		mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied (6)	V_{CC} = 5.5V V_O = 2.7V							50			50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied (6)	V_{CC} = 5.5V V_O = 0.4V	I/O Ports						−0.5			−0.5	mA
			Non-I/O						−50			−50	μA
I_{CC}	Supply Current (7)	V_{CC} = 5.5V											mA

NOTE 1: Voltage values are with respect to network ground terminal.
NOTE 2: Does not apply to open-collector outputs.
NOTE 3: Applies only to open-collector outputs.
NOTE 4: All typical numbers are at V_{CC} = 5V, T_A = 25°C.
NOTE 5: The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit current, I_{OS}.
NOTE 6: Applies only to TRI-STATE outputs.
NOTE 7: Refer to individual data sheet for I_{CC} limits.

National Semiconductor

Preliminary

DM54AS00/DM74AS00 Quad 2-Input NAND Gates

Features

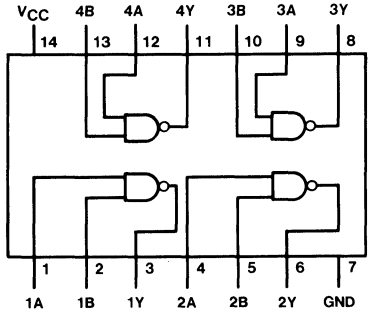
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterpart.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54AS00 (J) 74AS00 (J,N)

Recommended Operating Conditions

Parameter	DM54/74AS00			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		2.2	3.2	mA
			Outputs Low		11.2	16.1	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS00			DM74AS00			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1	2.5	5.5	1	2.5	4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1	1.5	4	1	1.5	3	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS02/DM74AS02 Quad 2-Input NOR Gates

Features

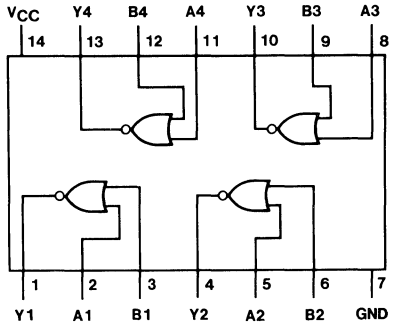
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{A + B}$



54AS02 (J) 74AS02 (J,N)

1

Recommended Operating Conditions

Parameter	DM54/74AS02			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		4.1	5.9	mA
			Outputs Low		13.1	18.8	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS02			DM74AS02			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1	2.5	5.5	1	2.5	4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1	1.5	4	1	1.5	3	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS04/DM74AS04 Hex Inverters

Features

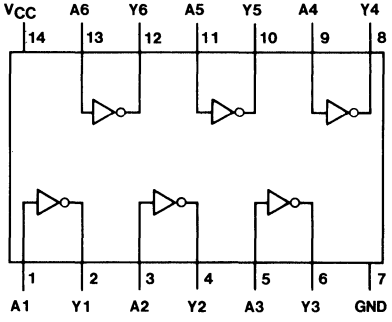
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{A}$



54AS04 (J) 74AS04 (J,N)

Recommended Operating Conditions

Parameter	DM54AS04			DM74AS04			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−2			−2	mA
Low Level Output Current, I_{OL}			20			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3	4.8	mA
			Outputs Low		14	24.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS04			DM74AS04			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1	2.5	5.5	1	2.5	4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1	1.5	4	1	1.5	3	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

National Semiconductor

Preliminary

DM54AS08/DM74AS08 Quad 2-Input AND Gates

Features

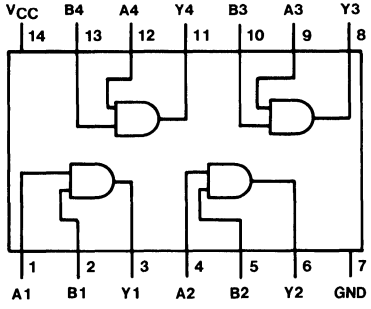
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = AB$



54AS08 (J) 74AS08 (J,N)

Recommended Operating Conditions

Parameter	DM54/74AS08			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		6.4	9.3	mA
			Outputs Low		15.7	22.7	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS08			DM74AS08			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.5	3	6.5	1.5	3	5.5	ns
T_{PHL}, Propagation delay time. High to low level output		2	3.5	6.5	2	3.5	5.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS10/DM74AS10 Triple 3-Input NAND Gates

Features

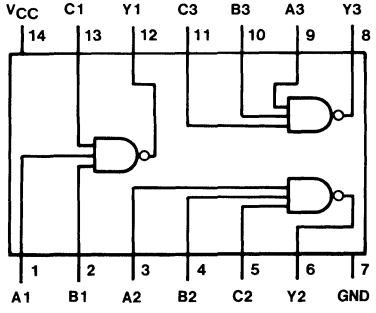
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{ABC}$



54AS10 (J) **74AS10 (J,N)**

1

Recommended Operating Conditions

Parameter	DM54/74AS10			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.7	2.4	mA
			Outputs Low		8.4	12.1	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS10			DM74AS10			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1	2.5	5.5	1	2.5	4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1	1.5	4	1	1.5	3	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS11/DM74AS11 Triple 3-Input AND Gates

Features

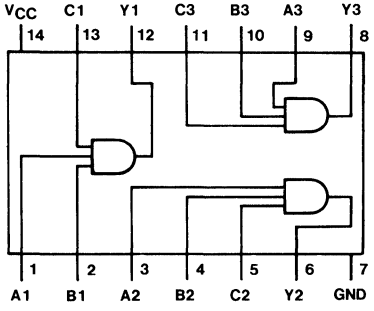
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

Y = ABC



54AS11 (J) 74AS11 (J,N)

Recommended Operating Conditions

Parameter	DM54/74AS11			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		4.8	7.0	mA
			Outputs Low		11.8	17.0	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS11			DM74AS11			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.5	3	6.5	1.5	3	5.5	ns
T_{PHL}, Propagation delay time. High to low level output		2	3.5	6.5	2	3.5	5.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS20/DM74AS20 Dual 4-Input NAND Gates

Features

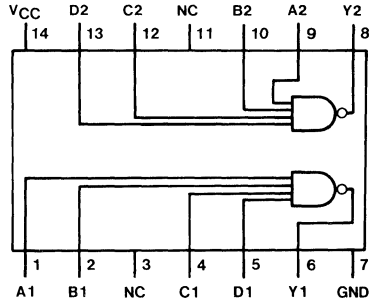
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{ABCD}$



54AS20 (J) 74AS20 (J,N)

Recommended Operating Conditions

Parameter	DM54/74AS20			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.1	1.6	mA
			Outputs Low		5.6	8.1	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS20			DM74AS20			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1	2.5	5.5	1	2.5	4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1	1.5	4	1	1.5	3	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS21/DM74AS21 Dual 4-Input AND Gates

Features

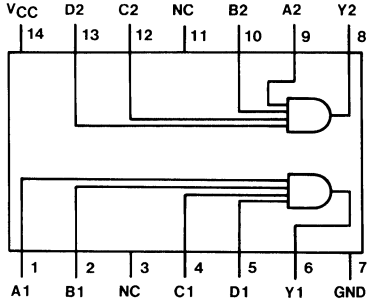
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

Y = ABCD



54AS21 (J) 74AS21 (J,N)

Recommended Operating Conditions

Parameter	DM54/74AS21			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		3.2	4.6	mA
			Outputs Low		7.9	11.3	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS21			DM74AS21			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.5	3	6.5	1.5	3	5.5	ns
T_{PHL}, Propagation delay time. High to low level output		2	3.5	6.5	2	3.5	5.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS27/DM74AS27 Triple 3-Input NOR Gates

Features

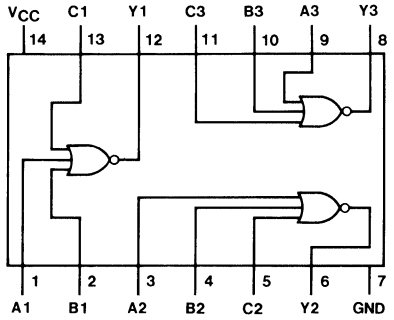
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$$Y = \overline{A+B+C}$$



54AS27 (J) 74AS27 (J,N)

Recommended Operating Conditions

Parameter	DM54/74AS27			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		4.5	6.4	mA
			Outputs Low		11.2	16.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS27			DM74AS27			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1	2.5	5.5	1	2.5	4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1	1.5	4	1	1.5	3	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS30/DM74AS30 8 Input NAND Gate

Features

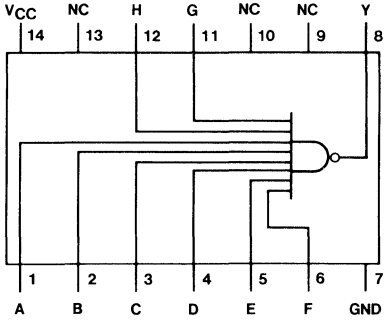
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{ABCDEFGH}$



54AS30 (J) 74AS30 (J,N)

Recommended Operating Conditions

Parameter	DM54/74AS30			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−1.0	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		1.0	1.5	mA
			Outputs Low		3.1	4.5	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS30			DM74AS30			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1	2.5	5.5	1	2.5	4.5	ns
T_{PHL}, Propagation delay time. High to low level output		1	1.5	4	1	1.5	3	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS32/DM74AS32 Quad 2-Input OR Gates

Features

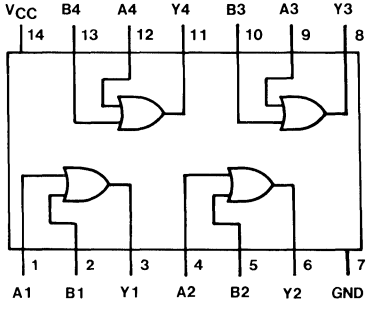
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = A + B$



54AS32 (J) · 74AS32 (J,N)

Recommended Operating Conditions

Parameter	DM54/74AS32			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		8.3	12.0	mA
			Outputs Low		17.6	25.4	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS32			DM74AS32			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.5	3	6.5	1.5	3	5.5	ns
T_{PHL}, Propagation delay time. High to low level output		2	3.5	6.5	2	3.5	5.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS74/DM74AS74 Dual D Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54AS74 is a dual edge-triggered flip-flops. Each flip-flop has individual D, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the D input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

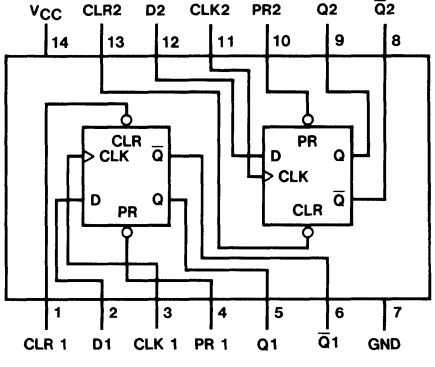
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-For-Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over S74 at Approximately Half the Power.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS74 (J) 74AS74 (J,N)

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Q_0 = Previous Condition of Q
* = This condition is nonstable; it will not persist when preset and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54AS74			DM74AS74			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock frequency, f_{CLOCK}		0		100	0		100	MHz
Width of Clock Pulse, T_W	High	4			4			ns
	Low	6			5			ns
Pulse Width T_W, Preset & Clear	Low	4			4			ns
Data Setup Time, T_{SU}	High	3			2			ns
	Low	4			3			ns
PRE or CLR Setup Time		3			2			ns
Data Hold Time, T_H		2↑			1↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

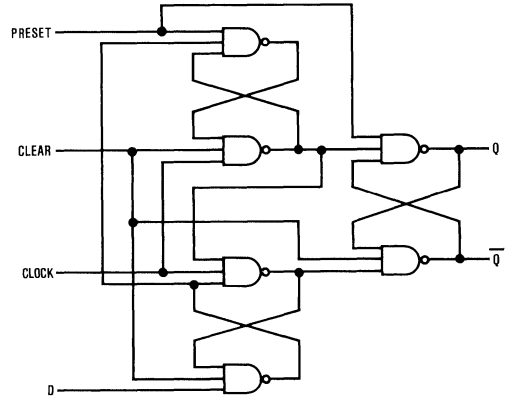
	Parameter		Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V I_I = −18mA			−1.2	V
V_{OH}	High Level Output Voltage		I_{OH} = −2mA	V_{CC}−2			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V V_{IH} = 2V I_{OL} = 20mA		0.35	0.5	V
I_I	Max High Input Current		V_{CC} = 5.5V V_{IH} = 7V			0.1	mA
I_{IH}	High Level Input Current	Clock, D	V_{CC} = 5.5V V_{IH} = 2.7V			20	μA
		Preset, Clear				40	μA
I_{IL}	Low Level Input Current	Clock, D	V_{CC} = 5.5V V_{IL} = 0.4V			−0.5	mA
		Preset, Clear				−1.0	mA
I_O	Output Drive Current		V_{CC} = 5.5V V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current		V_{CC} = 5.5V		10.5	16	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS74			DM74AS74			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	100	125		100	125		MHz
T_{PLH}	Preset or clear	Q or $\overline{Q}$		3.2	4.5	8.0	3.2	4.5	7.1	ns
T_{PHL}				3.5	6	11.5	3.5	6	10.5	ns
T_{PLH}	Clock	Q or $\overline{Q}$		3.8	6	8.5	3.8	6	7.8	ns
T_{PHL}				4.4	6	10.5	4.4	6	9.2	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



National Semiconductor

Preliminary

DM54AS109/DM74AS109 Dual J-$\overline{K}$ Positive-Edge-Triggered Flip-Flops with Preset and Clear

General Description

The DM54AS109 is a dual edge-triggered flip flops. Each flip flop has individual J, $\overline{K}$, clock, clear and preset inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input J or $\overline{K}$ is transferred to the Q output on the positive going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive going pulse. When the clock input is at either the high or low level, the J, $\overline{K}$ input signal has no effect.

Asynchronous preset and clear inputs will set or clear Q output respectively upon the application of low level signal.

The J$\overline{K}$ design allows operation as a D flip flop by tying the J and $\overline{K}$ inputs together.

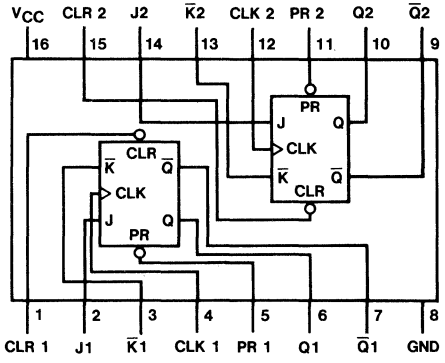
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and LS TTL Counterpart.
- Improved AC Performance Over S109 at Approximately Half the Power.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS109 (J) 74AS109 (J,N)

Function Table

Inputs					Outputs	
PR	CLR	CK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition, Q_0 = Previous Condition of Q
* This condition is nonstable; it will not persist when present and clear inputs return to their inactive (high) level. The output levels in this condition are not guaranteed to meet the V_{OH} specification.

Recommended Operating Conditions

Parameter		DM54AS109			DM74AS109			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock Frequency, fCLOCK		0		90	0		90	MHz
Pulse Width T_W	Clock High	4			4			ns
	Clock Low	5			5			ns
Pulse Width T_W, Preset & Clear		4			4			ns
Data Setup Time, T_{SU}	J or $\overline{K}$	3			3			ns
	PRE or CLR inactive	2			2			
Data Hold Time, T_H		1↑			1↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

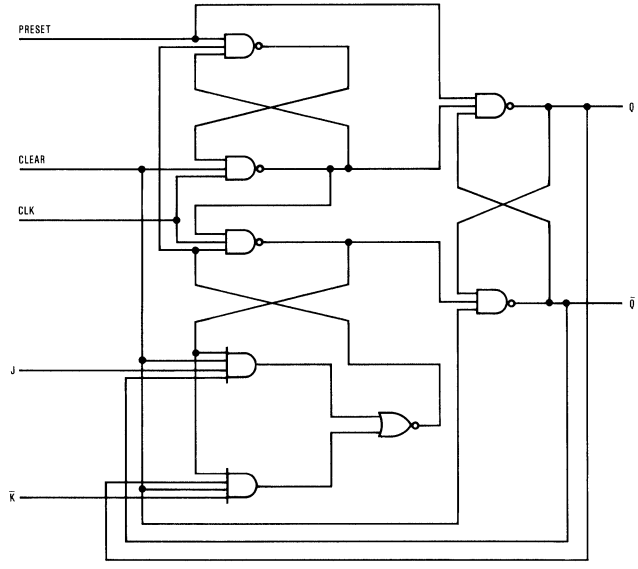
	Parameter		Conditions	Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V I_I = −18mA			−1.2	V
V_{OH}	High Level Output Voltage		I_{OH} = −2mA	V_{CC} −2			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V V_{IH} = 2V I_{OL} = 20mA		0.35	0.5	V
I_I	Max High Input Current		V_{CC} = 5.5V V_{IH} = 7V			0.1	mA
I_{IH}	High Level Input Current	Clock, J, $\overline{K}$	V_{CC} = 5.5V V_{IH} = 2.7V			20	μA
		Preset, Clear				40	
I_{IL}	Low Level Input Current	Clock, J, $\overline{K}$	V_{CC} = 5.5V V_{IL} = 0.4V			−0.5	mA
		Preset, Clear					
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current		V_{CC} = 5.5V		11.5	17	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS109			DM74AS109			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	90	125		90	125		MHz
T_{PLH}	Preset or clear	Q or $\overline{Q}$		3.2	4.5	9.0	3.2	4.5	8.0	ns
T_{PHL}				3.5	6	11.5	3.5	6	10.5	ns
T_{PLH}	Clock	Q or $\overline{Q}$		3.8	6	9.0	3.8	6	8.0	ns
T_{PHL}				4.4	6	10.5	4.4	6	9.2	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-3.

Logic Diagram



National Semiconductor

Preliminary

DM54AS151/DM74AS151 8-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. A Strobe input is provided which, when at the high level, disables all data inputs and forces the Y output to the low state and the W output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

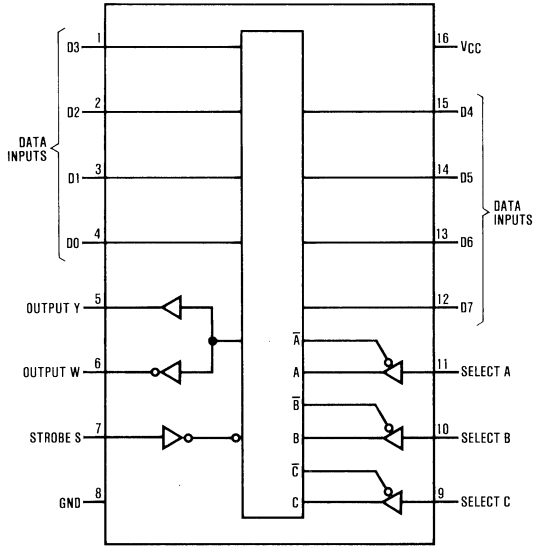
Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS and Schottky Family Counterpart.
- Improved Output Transient Handling Capability.

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54AS151	−55°C to 125°C
DM74AS151	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54AS151 (J) 74AS151(J,N)

Function Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level L = Low Level X = Don't Care
D0 thru D7 = the level of the respective D input

Recommended Operating Conditions

Parameter	DM54AS151			DM74AS151			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5		5.5	4.5		5.5	V
High Level Input Voltage, V_{IH}	2.0			2.0			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

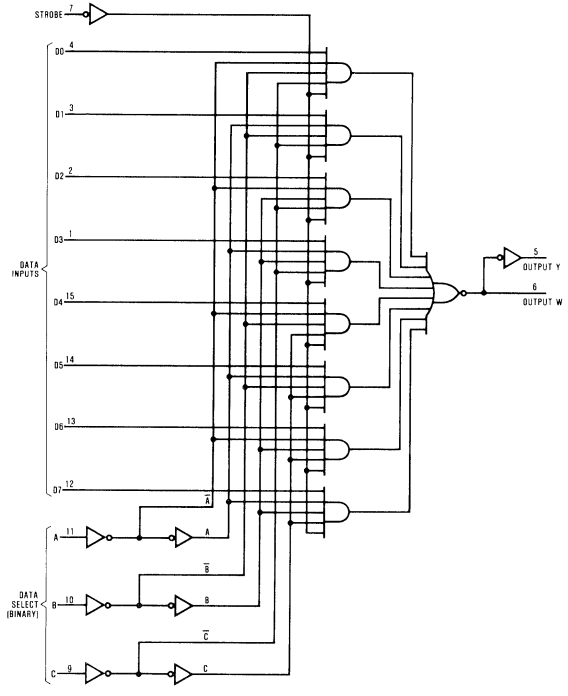
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = MAX		2.4	3.2		V
		IOH = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 20mA			.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	A,B,C			−1.0	mA
			All others			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Date Inputs = 3.0V Select Inputs = 3.0V Strobe Inputs = 3.0V			26	45	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS151			DM74AS151			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	1	5	9.5	1	5	8.5	ns
t_{PHL}, High to low Level Output				1	5	9.5	1	5	8.5	ns
t_{PLH}, Low to high Level Output		W		1	4.5	8.5	1	4.5	7.5	ns
t_{PHL}, High to low Level Output				1	4.5	8.0	1	4.5	7.0	ns
t_{PLH}, Low to high Level Output	Data	Y		1	3	6.0	1	3	5.0	ns
t_{PHL}, High to low Level Output				1	4	8.0	1	4	7.0	ns
t_{PLH}, Low to high Level Output		W		1	3	6.0	1	3	5.0	ns
t_{PHL}, High to low Level Output				1	2.5	5.0	1	2.5	4.5	ns
t_{PLH}, Low to high Level Output	Strobe	Y		1	5	9.5	1	5	8.5	ns
t_{PHL}, High to low Level Output				1	5	9.0	1	5	8.0	ns
t_{PLH}, Low to high Level Output		W		1	4.5	7.5	1	4.5	7.0	ns
t_{PHL}, High to low Level Output				1	4.5	8.5	1	4.5	7.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

Logic Diagram



National Semiconductor

Preliminary

DM54AS153/DM74AS153 Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and a non-inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the low state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

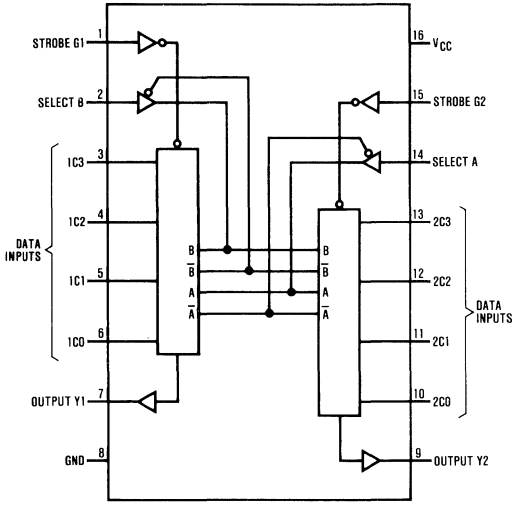
Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS and Schottky Family Counterpart.
- Improved Output Transient Handling Capability.

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54AS153	−55°C to 125°C
DM74AS153	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54AS153 (J) 74AS153 (J,N)

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections
H = High Level L = Low Level X = Don't Care

Recommended Operating Conditions

Parameter	DM54AS153			DM74AS153			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

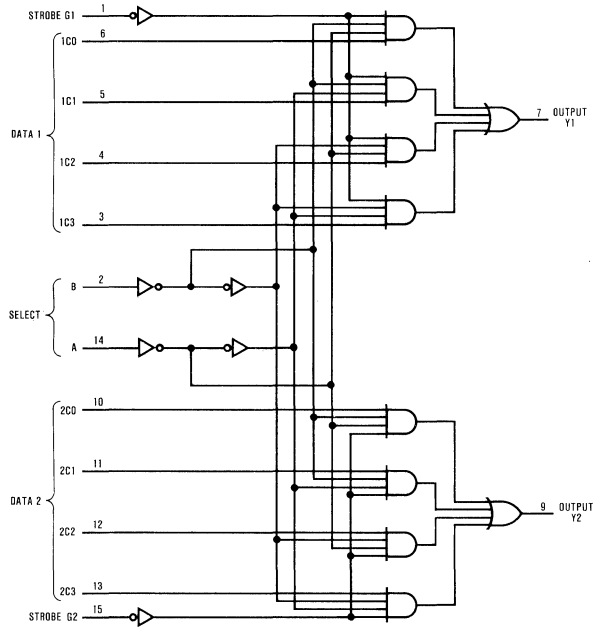
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = MAX		2.4	3.2		V
		I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IN} = 0.4V	A, B			−1.0	mA
			All others			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs high		17	30	mA
			Outputs low		25	45	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS153			DM74AS153			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	1	5.5	10.0	1	5.5	9.0	ns
t_{PHL}, High to low Level Output				1	4.5	8.5	1	4.5	7.5	ns
t_{PLH}, Low to high Level Output	Data	Y		1	3.5	6.5	1	3.5	6.0	ns
t_{PHL}, High to low Level Output				1	3	6.0	1	3	5.0	ns
t_{PLH}, Low to high Level Output	Strobe	Y		1	5.5	10.0	1	5.5	9.0	ns
t_{PHL}, High to low Level Output				1	4.5	8.5	1	4.5	7.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

Logic Diagram



National Semiconductor

Preliminary

DM54AS/DM74AS157,158 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The AS157 presents true data whereas the AS158 presents inverted data to minimize propagation delay time.

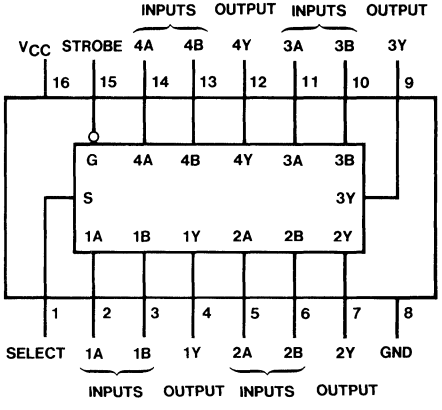
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS157 (J) 74AS157 (J,N)

54AS158 (J) 74AS158 (J,N)

Function Table

Inputs				Output Y	
Strobe	Select	A	B	S157	S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54/74AS157,158			Unit
	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			V
Low Level Input Voltage, V_{IL}			0.8	V
High Level Output Current, I_{OH}			−2	mA
Low Level Output Current, I_{OL}			20	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

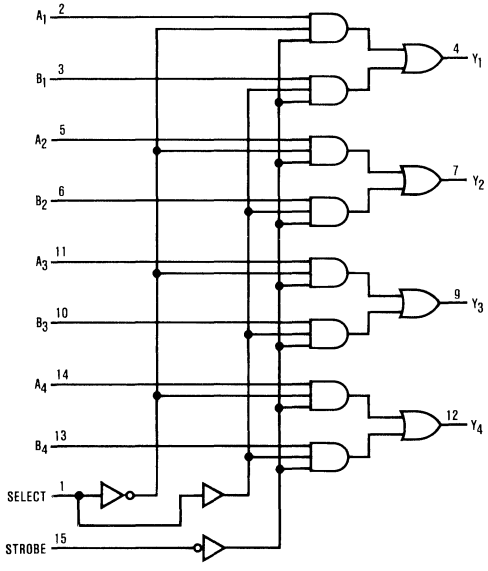
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	Select			1.0	mA
			All others			0.5	
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	54/74AS157		19.0	27.4	mA
			54/74AS158		15.6	22.5	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

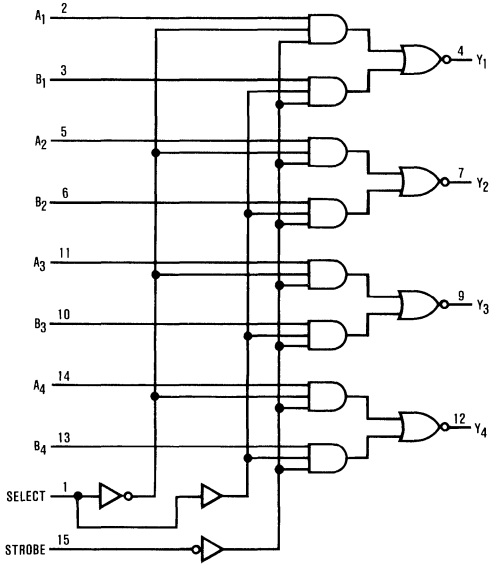
Parameter		From (Input)	To (Output)	Conditions	DM54AS157,158			DM74AS157,158			Unit
					Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time. Low to High Level Output	157	Data	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	1.5	3	6.0	1.5	3	5.0	ns
	158				1	2.5	6	1	2.5	5.0	
T_{PHL}, Propagation Delay Time. High to Low Level Output	157				1.5	3.5	6.5	1.5	3.5	5.5	
	158				1	2	4.5	1	2	3.5	
T_{PLH}, Propagation Delay Time. Low to High Level Output	157	Strobe	Y		2.5	6.5	11.0	2.5	6.5	10.0	
	158				2	5.5	10.0	2	5.5	9.0	
T_{PHL}, Propagation Delay Time. High to Low Level Output	157				2.5	4.5	8.5	2.5	4.5	7.5	
	158				1.5	3	7.0	1.5	3	6.0	
T_{PLH}, Propagation Delay Time. Low to High Level Output	157	Select	Y		2.5	7.5	12.0	2.5	7.5	11.0	
	158				2.5	6.5	12.0	2.5	6.5	11.0	
T_{PHL}, Propagation Delay Time. High to Low Level Output	157				3.5	7.5	12.0	3.5	7.5	11.0	
	158				3	6.0	11.0	3	6.0	10.0	

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

Logic Diagrams



AS157



AS158

National Semiconductor

Preliminary

DM54AS/DM74AS160,161,162,163 Synchronous Four-Bit Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for application in high speed counting designs. The AS160 and AS162 are four-bit decade counters, while the AS161 and AS163 are four-bit binary counters. The AS160 and AS161 clear asynchronously, while the AS162 and AS163 clear synchronously. The carry output is decoded to prevent spikes during normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable, that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with set up data after the next clock pulse regardless of the levels of enable input. Low to high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs.

The AS160 and AS161 clear function is asynchronous. A low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs. These two counters are provided with a clear on power-up feature. The AS162 and AS163 clear function is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low to high transitions at the clear input of the AS162 and AS163 are also permissible regardless of the levels of logic on the clock, enable or load inputs.

The carry look ahead circuitry provides for cascading counters for n bit synchronous application without additional gating. Instrumental in accomplishing this function are two count-enable inputs (P and T) and a ripple carry output. Both count-enable inputs must be high to count. The T input is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high level output pulse with a duration approximately equal to the high level portion of QA output. This high level overflow ripple carry pulse can be used to enable successive cascaded stages. High to low level transitions at the enable P or T inputs of the AS160 through AS163, may occur regardless of the logic level on the clock.

The AS160 through AS163 feature a fully independent clock circuit. Changes made to control inputs (enable P or T, or load) that will modify the operating mode will have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

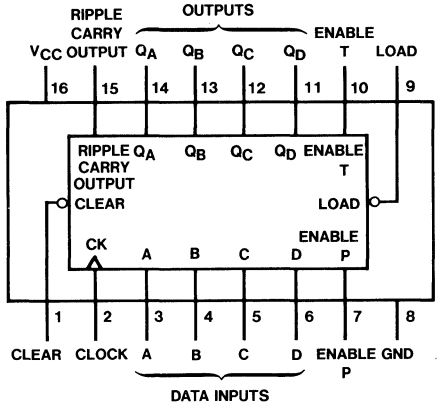
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Shottky TTL Process.
- Functionally and Pin For Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously programmable.
- Internal look ahead for fast counting.
- Carry output for n-bit cascading.
- Synchronous counting.
- Load control line.
- ESD inputs.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS160 (J) 74AS160 (J,N)
54AS161 (J) 74AS161 (J,N)
54AS162 (J) 74AS162 (J,N)
54AS163 (J) 74AS163 (J,N)

Recommended Operating Conditions

Parameter		DM54AS 160,161,162,163			DM74AS 160,161,162,163			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock Frequency, f_{CLOCK}		0		85	0		100	MHz
tsetup, Set-up time	Data; A, B, C, D	4	2		4	2		ns
	En P, En T	6	3		6	3		ns
	Load	6	3		6	3		ns
	Clear (Only for 162 & 163)	12	6.5		12	6.5		ns
Set-up 1 (Only for 160 & 161)	Clear	8	4		8	4.0		ns
thold, Hold time	Data; A, B, C, D	0	−1.5		0	−1.5		ns
	En P, En T	0	−2.5		0	−2.5		ns
	Load	0	−2.5		0	−2.5		ns
	Clear (Only for 162 & 163)	0	−3.5		0	−3.5		ns
Hold 0 (Only for 160 & 161)	Clear	0	−1.5		0	−1.5		ns
Width of Clock or Clear Pulse, T_W		6	3.5		5	3.5		ns

Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V	DATA, CLR, CLK, EN P LOAD, EN T			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V	CLR, CLK, DATA BUS			−.5	mA
			LOAD, ENT			−1.0	
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V	−30		−110	mA
I_{CC}		V_{CC} = 5.5V			40	53	mA

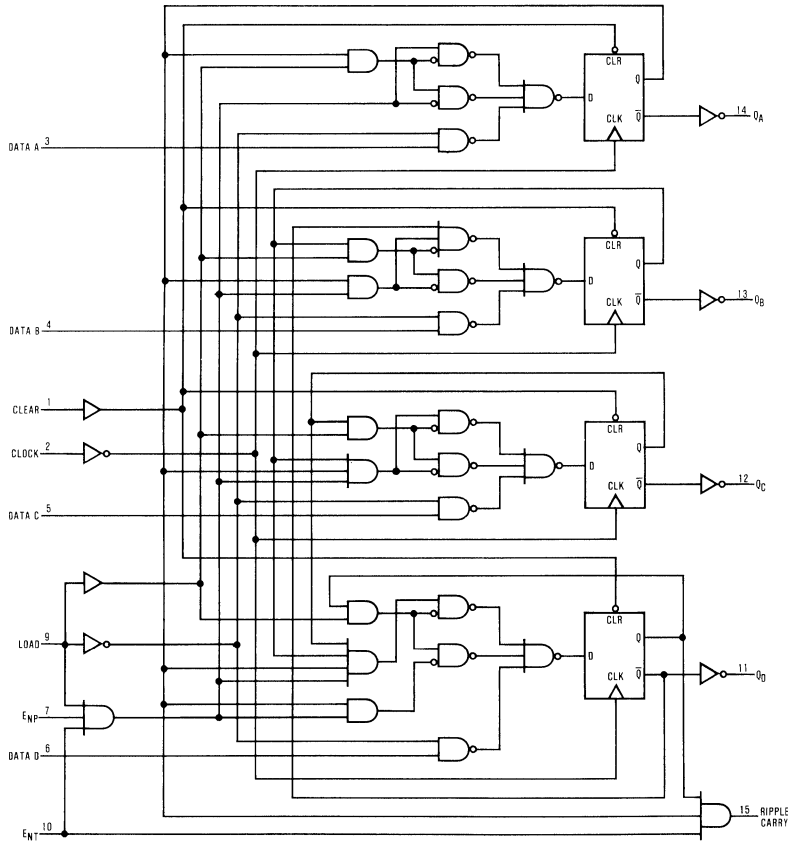
Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS 160, 161, 162, 163			DM74AS 160, 161, 162, 163			Unit
				Min	Typ	Max	Min	Typ	Max	
fmax, Max. clock freq.			V_{CC} = 4.5 to 5.5V R_L = 500 Ω C_L = 50 pF	85	145		100	145		MHZ
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Ripple Carry		2	7	15.5	2	7	12.5	ns
T_{PHL}, Propagation delay time. High to low level output. With Load High				2	6	13	2	6	11	ns
With Load Low				3	10	22	3	10	18	ns
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Any Q		2	5	11	2	5	9	ns
T_{PHL}, Propagation delay time. High to low level output.				2	6	13	2	6	11	ns
T_{PLH}, Propagation delay time. Low to high level output.	En T	Ripple Carry		1	3	6.5	1	3	5.5	ns
T_{PHL}, Propagation delay time. Low to high level output.				1	4	9	1	4	7.5	ns
T_{PHL}, Propagation delay time. High to low level output.	Clear	Any Q		2	7	15.5	2	7	12.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-3.

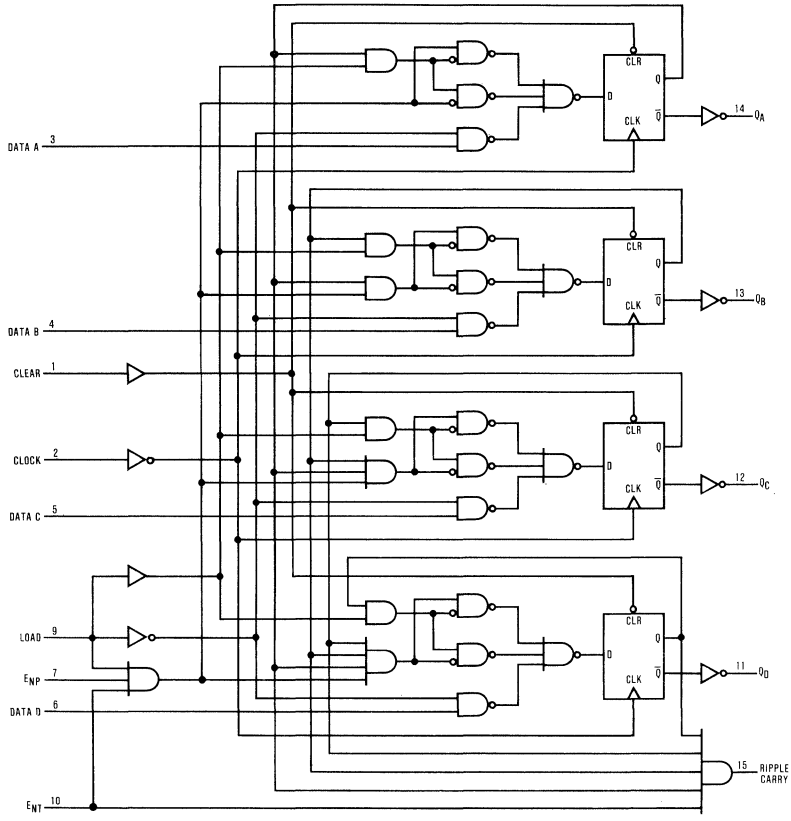
Logic Diagrams

AS160



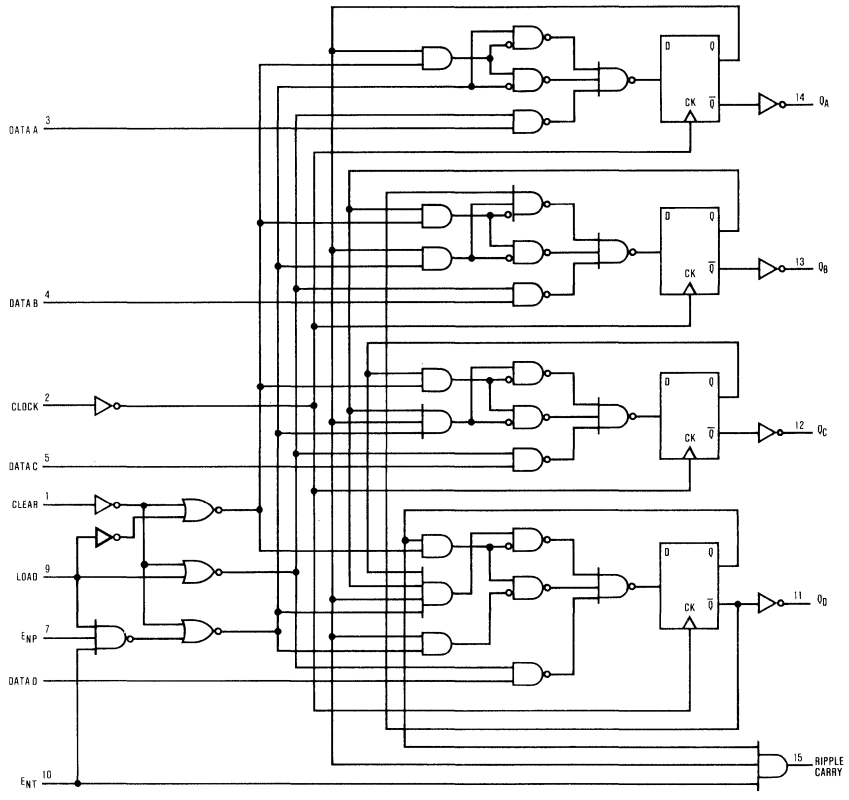
Logic Diagrams

AS161



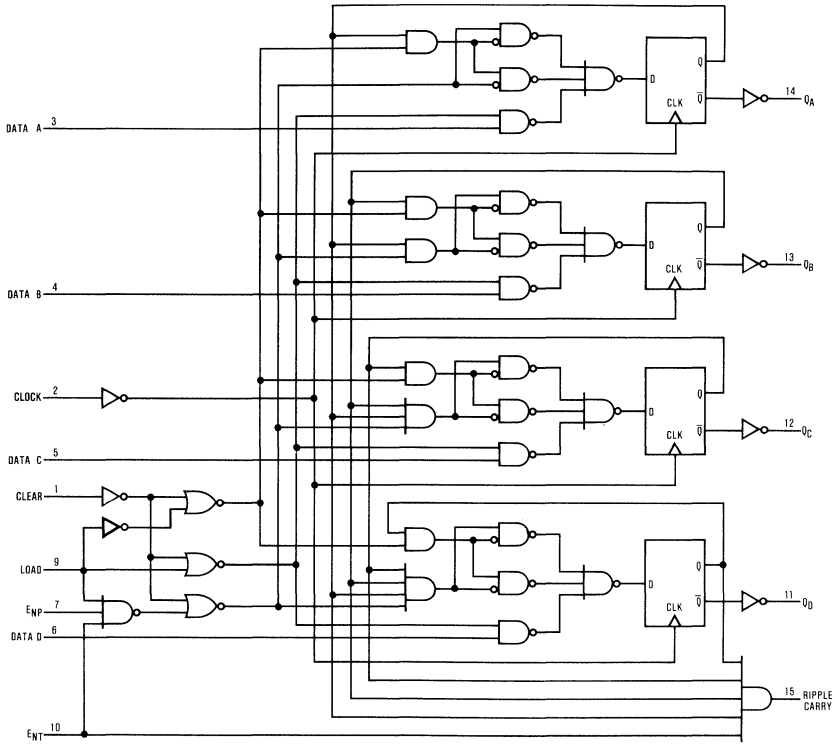
Logic Diagrams

AS162



Logic Diagrams

AS163



National Semiconductor

Preliminary

DM54AS/DM74AS168,169
Synchronous Four Bit Up/Down Counters

General Description

These synchronous presettable counters feature an internal carry look ahead for cascading in high speed counting applications. The AS168 is a four-bit decade up/down counter and the AS169 is a four-bit binary up/down counter. The carry output is decoded to prevent spikes during normal mode of counting operation. Synchronous operation is provided so that outputs change coincident with each other when so instructed by count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive going) edge of clock input waveform.

These counters are fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input T is fed forward to enable the carry outputs. The carry output thus enabled will produce a low level output pulse with a duration approximately equal to the high portion of the QA output when counting up, and approximately equal to the low portion of the QA output when counting down. This low level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input.

The control functions for these counters are fully synchronous. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) which modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

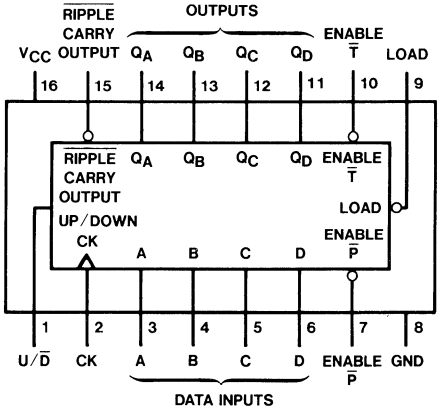
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.
- Synchronously Programmable.
- Internal Look Ahead for Fast Counting.
- Carry Output for N-bit Cascading.
- Synchronous Counting.
- Load Control Line.
- ESD Inputs.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS168 (J) **74AS168 (J,N)**

54AS169 (J) **74AS169 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS168,168			DM74AS168,169			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−2			−2	mA
Low Level Output Current, I_{OL}				20			20	mA
Clock Frequency, f_{CLOCK}		0		85	0		100	MHz
tsetup, Set-up time	Data; A, B, C, D	4	2		4	2		ns
	En $\overline{P}$, En $\overline{T}$	6	3		6	3		ns
	Load	6	3		6	3		ns
	U/$\overline{D}$	10	5		10	5.0		ns
thold, Hold time	Data; A, B, C, D	0	−1.5		0	−1.5		ns
	En $\overline{P}$, En $\overline{T}$	0	−2.5		0	−2.5		ns
	Load	0	−2.5		0	−2.5		ns
	U/$\overline{D}$	0	−4.5		0	−4.5		ns
Width of Clock Pulse, T_W		6	3.5		5	3.5		ns

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameters	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.5	V
V_{OH}	High Level Output Voltage	I_{OH} = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 5.5V, I_{OL} = 20mA			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 4.5V, V_{IH} = 2.7V	U/$\overline{D}$, CLK, LOAD, DATA, EN $\overline{P}$, EN $\overline{T}$			20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V	CLK, DATA, EN$\overline{P}$			−0.5	mA
			LOAD, EN $\overline{T}$ U/$\overline{D}$			−1.0	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−110	mA
I_{CC}		V_{CC} = 5.5V			46	63	mA

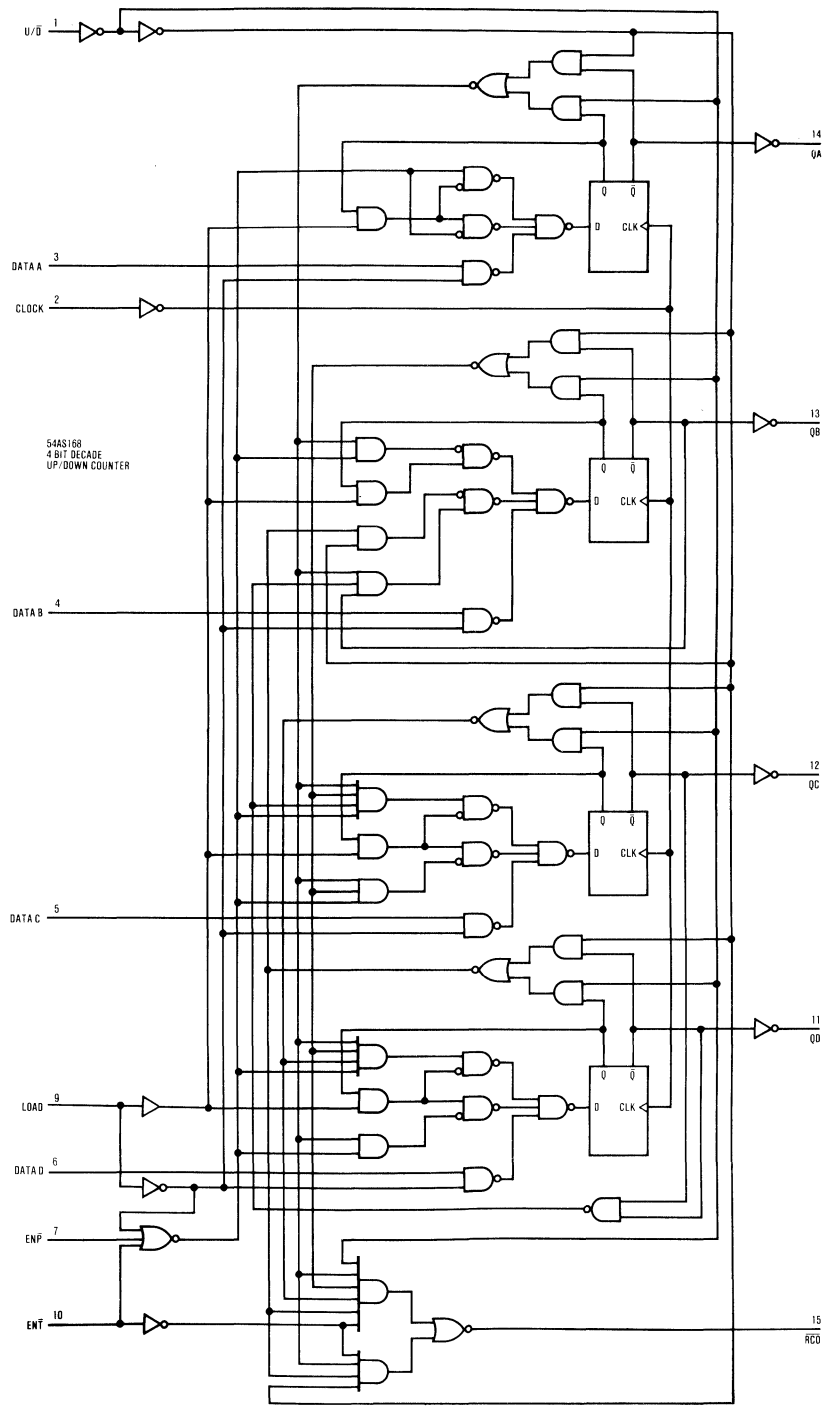
Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS168,169			DM74AS168,169			Unit
				Min	Typ	Max	Min	Typ	Max	
fmax, Max. clock freq.			V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF	85	145		100	145		MHz
T_{PLH}, Propagation delay time. Low to high level output. With Load Low	Clock	$\overline{\text{Ripple}}$ Carry		3	9.5	21	3	9.5	17	ns
With Load High				2	5.5	12	2	5.5	10	ns
T_{PHL}, Propagation delay time. High to low level output.				2	7.5	16.5	2	7.5	13.5	ns
T_{PLH}, Propagation delay time. Low to high level output.	Clock	Any Q		2	5	11	2	5	9	ns
T_{PHL}, Propagation delay time. High to low level output.				2	6	13	2	6	11	ns
T_{PLH}, Propagation delay time. Low to high level output.	En T	$\overline{\text{Ripple}}$ Carry		1	3	6.5	1	3.0	5.5	ns
T_{PHL}, Propagation delay time. High to low level output.				1	4	9	1	4	7.5	ns
T_{PLH}, Propagation delay time. Low to high level output.	U/$\overline{\text{D}}$ (Note 2)	$\overline{\text{Ripple}}$ Carry		2	7.5	16.5	2	7.5	13.5	ns
T_{PHL}, Propagation delay time. High to low level output.				3	10.5	23	3	10.5	19	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-3.

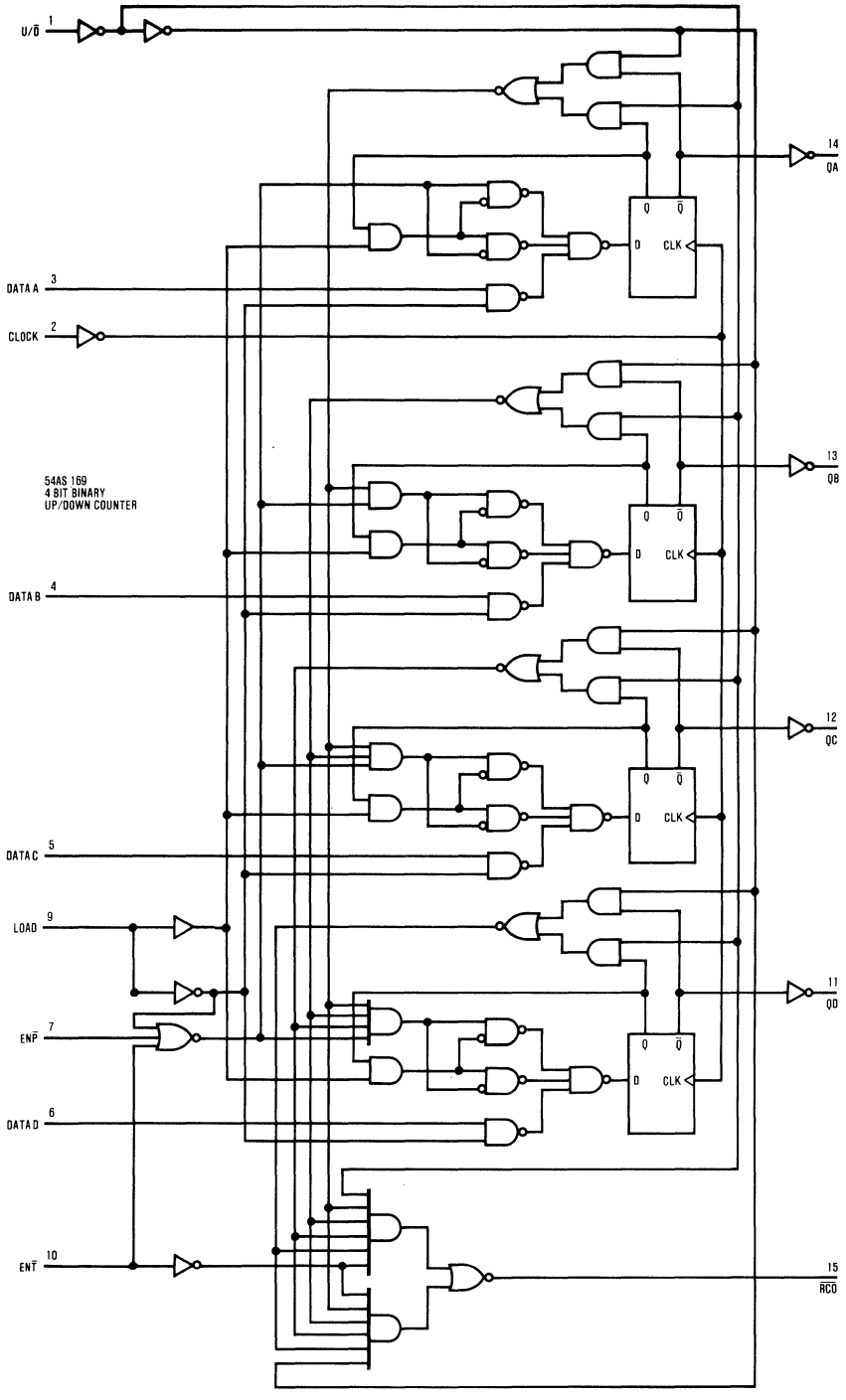
NOTE 2: Propagation delay time from up/down to ripple carry must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum (0), the ripple carry output transition will be in phase. If the count is maximum (9 for AS168 or 15 for AS169), the ripple carry output will be out of phase.

Logic Diagram



DM54AS/DM74AS168

Logic Diagram



DM54AS/DM74AS169

National Semiconductor

Preliminary

DM54AS/DM74AS174,175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Both have an asynchronous clear input, and the quad (175) version features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

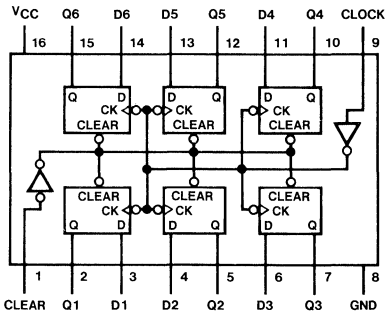
Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Pin and Functional compatible with LS and Schottky family counterpart.
- Typical clock frequency maximum is 80 MHz.
- Switching performance guaranteed over full temperature and V_{CC} supply range.
- 54AS174 contains six flip-flops with separate D inputs and Q outputs.
- 54AS175 contains four flip-flops with separate D inputs and both Q and $\overline{Q}$ outputs.

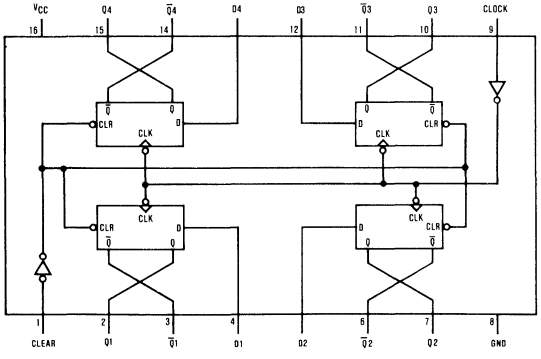
Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54AS174/175	−55°C to 125°C
DM74AS174/175	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagrams



54AS174 (J) 74AS174 (J,N)



54AS175 (J) 74AS175 (J,N)

Function Table

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$*
L	X	X	L	L
H	↑	H	H	H
H	↑	L	L	L
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
* applies to 54AS175/74AS175 only

Recommended Operating Conditions

Parameter	DM54AS174,175			DM74AS174,175			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−2			−2	mA
Low Level Output Current, I_{OL}			20			20	mA
Pulse Width, t_W Clock	5			4			ns
Clear	5			4			
Setup Time, t_{SETUP} Data Input	4			3			ns
Clear Inactive State	4			3			
Hold Time, t_{HOLD} Data Input	0			0			ns
Clear Active State	0			0			
Clock frequency, f_{CLOCK}	0		100	0		125	MHZ

Electrical Characteristics over recommended operating free air temperature range (Note 1)

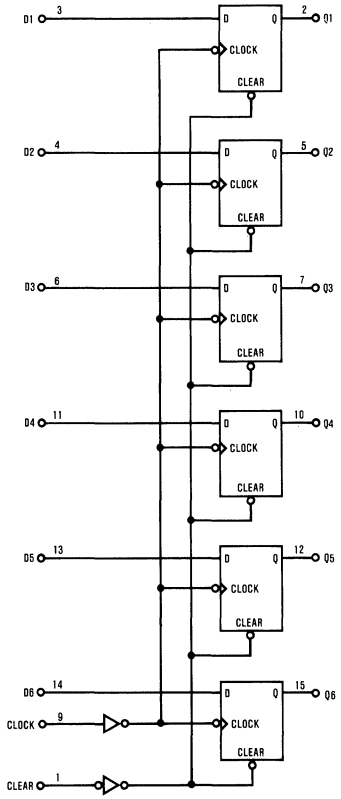
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V I_{OH} = −2		V_{CC}−2	V_{CC}−1.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = 20mA			.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V = 2.25V		−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Clock = 3.0V Clear = .4V D Inputs = 3.0V	AS174		46	83	mA
			AS175		33	60	

Switching Characteristics over recommended operating free air temperature range (Note 1)

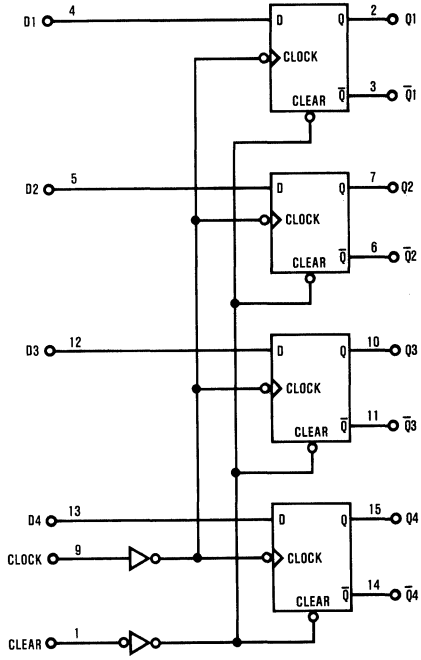
Parameter	Conditions	54AS174,175			74AS174,175			Unit
		Min	Typ	Max	Min	Typ	Max	
f_{MAX}, Maximum Clock Frequency		100	160		125	160		MHz
t_{PLH}, Propagation Delay Time, Low to high Level Output From Clear (175 Only)		1	5.0	9.5	1	5.0	8.5	ns
t_{PHL}, Propagation Delay Time, High to low Level Output From Clear	R_L = 500 Ω C_L = 50pF V_{CC} = 4.5 to 5.5V	1	5.5	10.0	1	5.5	9.0	ns
t_{PLH}, Propagation Delay Time, Low to high Level Output From Clock		1	4	8.0	1	4.0	7.0	ns
t_{PHL}, Propagation Delay Time, High to low Level Output From Clock		1	4	8.0	1	4.0	7.0	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-3.

Logic Diagrams



54AS174/74AS174



54AS175/74AS175

National Semiconductor

Preliminary

DM54AS/DM74AS230,231
TRI-STATE® Bus Drivers/Receivers

General Description

This family of Advanced Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines down to 133 ohms. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The AS230 is organized as 4 bit buffers inverting & 4 bit buffers non inverting. The AS231 is organized as two 4 bit wide inverting buffers with separate complementary output control buffers.

The TRI-STATE circuitry contains a feature that maintains the buffers in TRI-STATE until the power supply (V_{CC}) is greater than 3V. This feature prevents the buffers from glitching the system bus during power up or down.

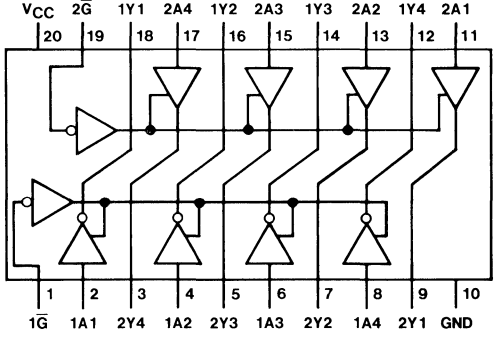
Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Switching Performance over Low Power Schottky Counterpart.
- Functional and Pin Compatible with Low Power Schottky Counterpart.
- Switching Response Specified into 500 ohm and 50pF.
- Low Level Drive Current 74AS = 48mA, 54AS = 40mA
- Glitch Free Bus During Power Up/Down
- Specified to Interface with CMOS at $V_{OH} = V_{CC} - 2V$.

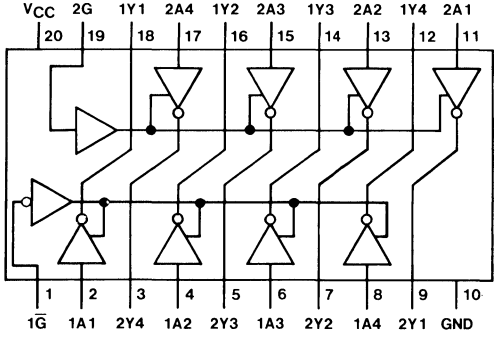
Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagrams



54AS230 (J) 74AS230 (J,N)



54AS231 (J) 74AS231 (J,N)

Recommended Operating Conditions

Parameter	DM54AS 230,231			DM74AS 230,231			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −48mA V_{CC} = 4.5V		2			V
		I_{OH} = −2.0mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = −48mA			0.35	0.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−0.5	mA
I_{OZH}	High Level TRI-STATE® Output Current	V_{CC} = 5.5V, V = 2.7V				50	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V_O = 0.4V				−50	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{CC}	54/74AS230 Supply Current	V_{CC} = 5.5V	Outputs High		38		mA
			Outputs Low		68		
			TRI-STATE		35		
I_{CC}	54/74AS231 Supply Current	V_{CC} = 5.5V	Outputs High		38		mA
			Outputs Low		68		
			TRI-STATE		35		

Switching Characteristics over recommended operating free air temperature range (Note 1,2)

Parameter	From (Input)	To (Output)	Conditions	DM54AS230			DM74AS230			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	1A	1Y	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF		3.5			3.5		ns
t_{PHL}					3.5			3.5		
t_{PLH}	2A	2Y			4.0			4.0		ns
t_{PHL}					4.3			4.3		
t_{PZH}	$\overline{G}$	Y			9			9		ns
t_{PZL}					10			10		
t_{PHZ}					7			7		
t_{PLZ}					7			7		

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From (Input)	To (Output)	Conditions	DM54AS231			DM74AS231			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	A	Y	V_{CC} = 4.5 to 5.5V, R_L = 500 Ω, C_L = 50 pF		3.5			3.5		ns
t_{PHL}					3.5			3.5		
t_{PZH}	$\overline{G}$ or G	Y			9			9		ns
t_{PZL}					10			10		
t_{PHZ}					7			7		
t_{PLZ}					7			7		

NOTE 1: See notes pg. 1-2, figures pg. 2-2.

National Semiconductor

Preliminary

DM54AS/DM74AS240,241,242,243,244 TRI-STATE® Bus Drivers/Receivers

General Description

This family of Advance Schottky TRI-STATE Bus circuits are designed to provide either bidirectional or unidirectional buffer interface in Memory, Microprocessor, and Communication Systems. The output characteristics of the circuits have low impedance sufficient to drive terminated transmission lines down to 133 ohms. The input characteristics of the circuits likewise have a high impedance so it will not significantly load the transmission line. The package contains eight TRI-STATE buffers organized with four buffers having a common TRI-STATE enable gate. The AS240, 241 and 244 are eight wide in a 20 pin package, and may be used as a 4 wide bidirectional or eight wide unidirectional. The AS242 and 243 are organized four wide bidirectional in a 14 pin package. The buffer selection includes inverting and non-inverting, with enable or disable TRI-STATE control. The TRI-STATE circuitry contains a feature that maintains the buffers in TRI-STATE until the power supply (V_{CC}) is greater than 3V. This feature prevents the buffers from glitching the system bus during power up or down.

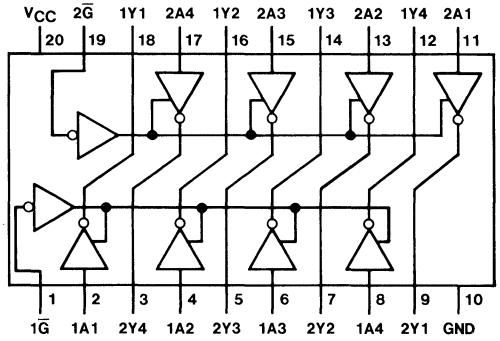
Features

- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Improved Switching Performance with Less Power Dissipation compared with Schottky Counterpart.
- Functional and Pin Compatible with 54/74LS and Schottky Counterpart.
- Switching Response Specified Into 500 ohm and 50pF.
- Glitch Free Bus During Power Up/Down.
- Specified to Interface with CMOS at $V_{OH} = V_{CC} - 2V$.

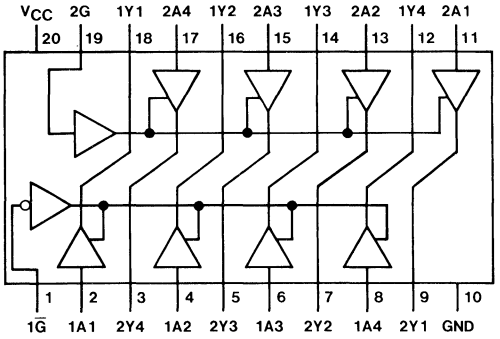
Absolute Maximum Ratings

Supply Voltage, V_{CC}	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagrams

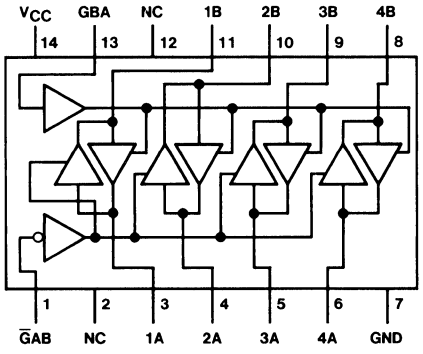


54AS240 (J) 74AS240 (J,N)

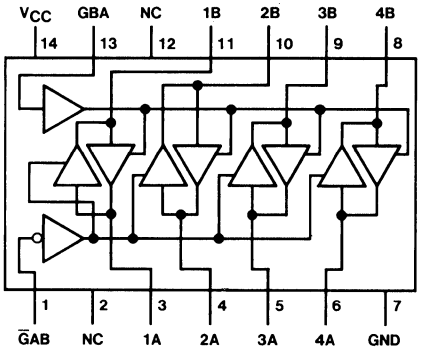


54AS241 (J) 74AS241 (J,N)

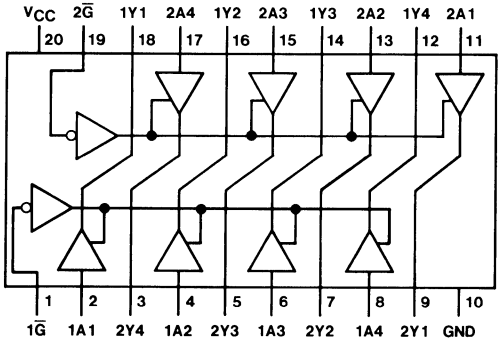
Connection Diagrams



54AS242 (J) 74AS242 (J,N)



54AS243 (J) 74AS243 (J,N)



54AS244 (J) 74AS244 (J,N)

Recommended Operating Conditions

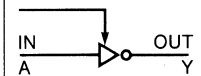
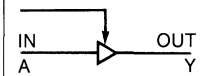
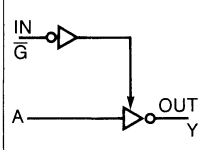
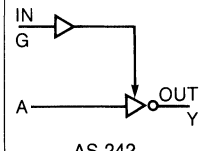
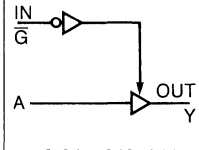
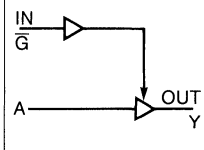
Parameter	DM54AS 240,241,242,243,244			DM74AS 240,241,242,243,244			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			48			64	mA

* Applies to 74AS-1 options.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = −3mA		2.4	3.2		V
		V_{CC} = 4.5V, I_{OH} = −15mA		2.0	2.3		
		I_{OH} = −2mA		V_{CC}−2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = Max			.35	.55	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V				−500	μA
I_{OZH}	High Level TRI-STATE® Output Current	V_{CC} = 5.5V, V = 2.7V				50	μA
I_{OZL}	Low Level TRI-STATE Output Current	V_{CC} = 5.5V, V = .4V				−50	μA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{CC}	54/74AS240 Supply Current	V_{CC} = 5.5V	Outputs High		11	19	mA
			Outputs Low		47	85	
			TRI-STATE		23	46	
I_{CC}	54/74AS241 Supply Current	V_{CC} = 5.5V	Outputs High		12	24	mA
			Outputs Low		53	90	
			TRI-STATE		33	66	
I_{CC}	54/74AS242 Supply Current	V_{CC} = 5.5V	A Port Outputs High		18	36	mA
			A Port Outputs Low		36	61	
			TRI-STATE		24	48	
I_{CC}	54/74AS243 Supply Current	V_{CC} = 5.5V	A Port Outputs High		22	44	mA
			A Port Outputs Low		43	86	
			TRI-STATE		33	66	
I_{CC}	54/74AS244 Supply Current	V_{CC} = 5.5V	Outputs High		11	22	mA
			Outputs Low		52	90	
			TRI-STATE		34	68	

Switching Characteristics over recommended operating free air temperature range (Notes 1, 2)

Parameter (Propagation Delay Time)	Circuit Configuration	74AS			54AS			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Low-to-High Level Output	 AS 240, 242	1	3.5	7	1	3.5	6	ns
T_{PHL}, High-to-Low Level Output		1	3.5	7	1	3.5	6	ns
T_{PLH}, Low-to-High Level Output	 AS 241, 243, 244	1	4	8	1	4	7	ns
T_{PHL}, High-to-Low Level Output		1	4	8	1	4	7	ns
T_{PZL}, Output Enable to Low Level	 AS 240, 242	2	7	13.5	2	7	12	ns
T_{PZH}, Output Enable to High Level		2	6	11	2	6	10	ns
T_{PLZ}, Output Disable From Low Level		3	8	15	3	8	13.5	ns
T_{PHZ}, Output Disable From High Level		1	4	8	1	4	7	ns
T_{PZL}, Output Enable to Low Level	 AS 242	3	8	15	3	8	13.5	ns
T_{PZH}, Output Enable to High Level		2	7	13.5	2	7	12	ns
T_{PLZ}, Output Disable From Low Level		3	9	16.5	3	9	15	ns
T_{PHZ}, Output Disable From High Level		2	6	11	2	6	10	ns
T_{PZL}, Output Enable to Low Level	 AS 241, 243, 244	2	7	13.5	2	7	12	ns
T_{PZH}, Output Enable to High Level		2	6	11	2	6	10	ns
T_{PLZ}, Output Disable From Low Level		3	8	15	3	8	13.5	ns
T_{PHZ}, Output Disable From High Level		2	4	8	2	4	7	ns
T_{PZL}, Output Enable to Low Level	 AS 241, 242	3	8	15	3	8	13.5	ns
T_{PZH}, Output Enable to High Level		2	7	13.5	2	7	12	ns
T_{PLZ}, Output Disable From Low Level		3	9	16.5	3	9	15	ns
T_{PHZ}, Output Disable From High Level		2	6	11	2	6	10	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-2.

NOTE 2: Switching characteristic conditions are V_{CC} = 4.5V to 5.5V, R_L = 500Ω, C_L = 50pF

National Semiconductor

Preliminary

DM54AS251/DM74AS251 TRI-STATE® 8-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-eight data sources as a result of a unique three-bit binary code at the Select inputs. Two complementary outputs provide both inverting and non-inverting buffer operation. An Output Control input is provided which, when at the high level, places both outputs in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

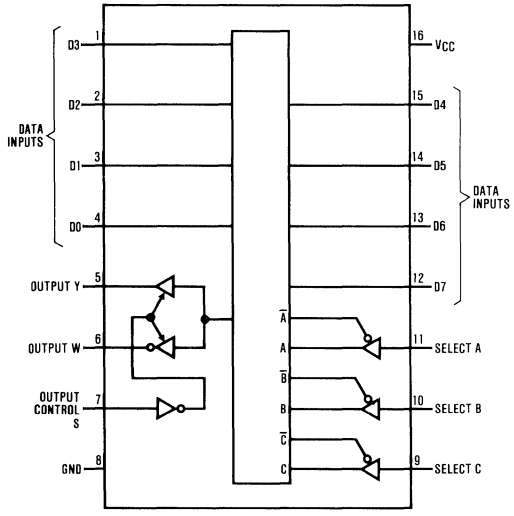
Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS and Schottky Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54AS251	−55°C to 125°C
DM74AS251	0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54AS251 (J) **74AS251 (J,N)**

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level, X = Don't Care
Z = High Impedance (Off)
D0 thru D7 = The Level of the Respective D Input

Recommended Operating Conditions

Parameter	DM54AS251			DM74AS251			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

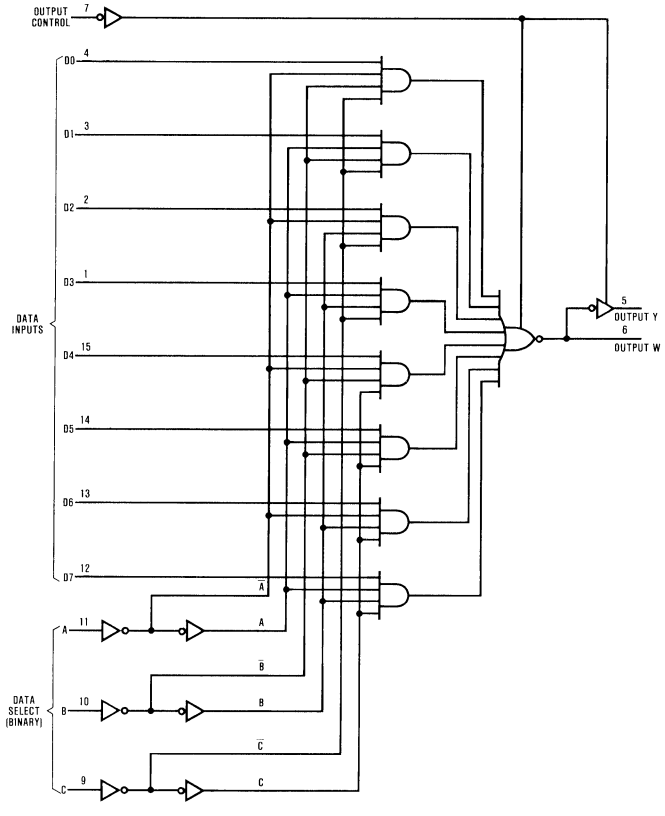
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2mA		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	A, B, C			−1.0	mA
			All others			−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7v				50	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} =0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Data Inputs = 3.0V Select Inputs = 3.0V Control Inputs = 3.0V			28	48	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS251			DM74AS251			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	2	5	9.5	2	5	8.5	ns
t_{PHL}, High to low Level Output				2	5	9.5	2	5	8.5	ns
t_{PLH}, Low to high Level Output		W		2	4.5	8.5	2	4.5	7.5	ns
t_{PHL}, High to low Level Output				2	4.5	8.5	2	4.5	7.5	ns
t_{PLH}, Low to high Level Output	Data	Y		1	3	6.0	1	3	5	ns
t_{PHL}, High to low Level Output				1	4	8.0	1	4	7	ns
t_{PLH}, Low to high Level Output		W		1	3	6.0	1	3	5	ns
t_{PHL}, High to low Level Output				1	2.5	4.5	1	2.5	4.5	ns
t_{ZH}, Output Enable Time to High Level	Output Control	Y		2	5	9.5	2	5	8.5	ns
t_{ZL}, Output Enable Time to Low Level				2	6	11.0	2	6	10.0	ns
t_{ZH}, Output Enable Time to High Level		W		2	5	9.5	2	5	8.5	ns
t_{ZL}, Output Enable Time to Low Level				2	6	11.0	2	6	10.0	ns
t_{HZ}, Output Disable Time From High Level		Y		1	3	6.0	1	3	5.0	ns
t_{LZ}, Output Disable Time From Low Level				1	4	8.0	1	4	7.0	ns
t_{HZ}, Output Disable Time From High Level		W		1	3	6.0	1	3	5.0	ns
t_{LZ}, Output Disable Time From Low Level				1	4	8.0	1	4	7.0	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-2.

Logic Diagram



National Semiconductor

Preliminary

DM54AS253/DM74AS253 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select Inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and a non-inverting Tri-state output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

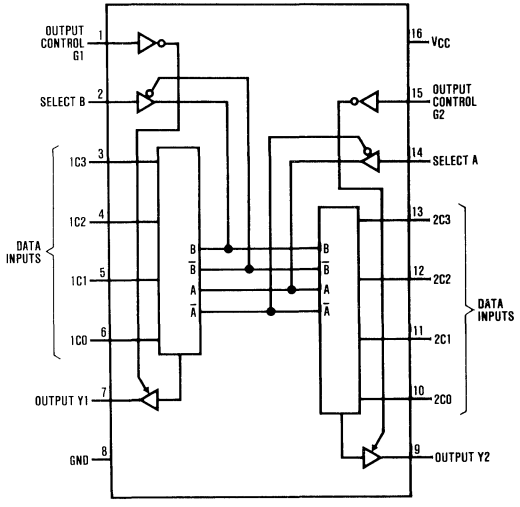
Features

- Advanced Oxide-Isolated Ion-Implanted Schottky TTL Process.
- Switching Performance is Guaranteed Over Full Temperature and V_{CC} Supply Range.
- Pin and Functional Compatible with LS and Schottky Family Counterpart.
- Improved Output Transient Handling Capability.
- Output Control Circuitry Incorporates Power-Up Tri-State Feature.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54AS253	−55°C to 125°C
DM74AS253	0° to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54AS253 (J) **74AS253 (J,N)**

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Recommended Operating Conditions

Parameter	DM54AS253			DM74AS253			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

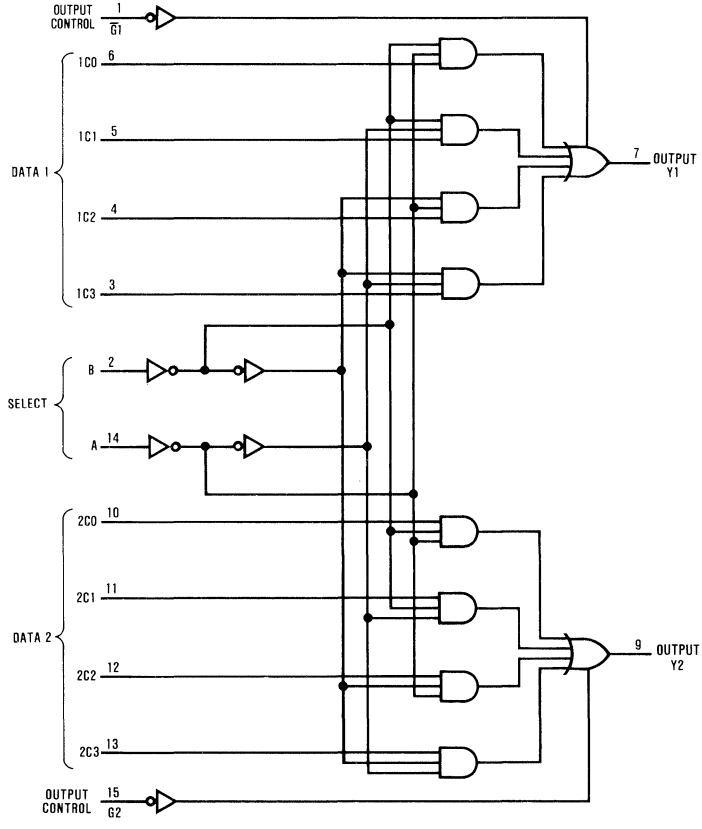
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		I_{OH} = −2mA		V_{CC}-2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	A, B			−1.0	mA
			All others			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, v_{OUT} = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs high		17	29	mA
			Outputs low		25	43	
			Outputs disabled		28	48	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS253			DM74AS253			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	2	6	11.0	2	6	10.0	ns
t_{PHL}, High to low Level Output				1	4.5	8.5	1	4.5	7.5	ns
t_{PLH}, Low to high Level Output	Data			1	3.5	7.0	1	3.5	6.0	ns
t_{PHL}, High to low Level Output				1	3	6.0	1	3	5.0	ns
t_{ZH}, Output Enable Time to High Level	Output Control	Y		1	5	9.5	1	5	8.5	ns
t_{ZL}, Output Enable Time to Low Level				2	6	11.0	2	6	10.0	ns
t_{HZ}, Output Disable Time From High Level				1	3	6.0	1	3	5.0	ns
t_{LZ}, Output Disable Time From Low Level				1	4	8.0	1	4	7.0	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-2

Logic Diagram



National Semiconductor

Preliminary

DM54AS/DM74AS257,258 TRI-STATE® Quad 2-Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four TRI-STATE outputs that can interface directly with data lines of bus-organized systems. A 4-bit word selected from one of two sources is routed to the four outputs. The AS257 presents true data whereas the AS258 presents inverted data to minimize propagation delay time.

This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 300 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

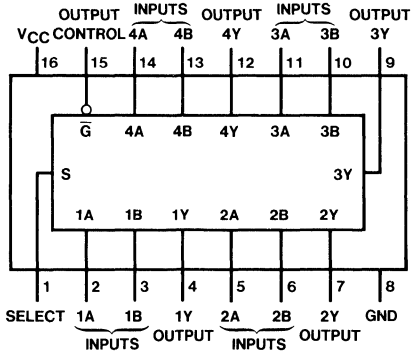
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky, Low Power Schottky, and Advanced Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky, Low Power Schottky, and Advanced Low Power Schottky Counterparts.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Expand any data input point.
- Multiplex dual data buses.
- General four functions of two variables (one variable is common).
- Source programmable counters.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS257 (J) 74AS257 (J,N)
54AS258 (J) 74AS258 (J,N)

Function Table

Inputs				Output Y	
Output Control	Select	A	B	AS257	AS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

1

Recommended Operating Conditions

Parameter	DM54AS257,258			DM74AS257,258			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

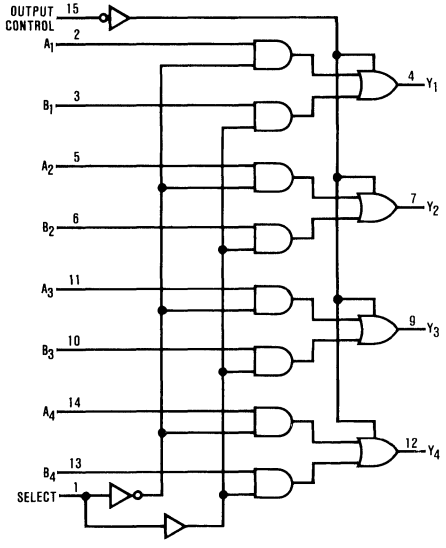
Parameter			Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage		V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage		V_{CC} = 4.5V, I_{OH} = MAX		2.4	3.2		V
			I_{OH} = −2mA		V_{CC} −2V			V
V_{OL}	Low Level Output Voltage		V_{CC} = 4.5V, I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current		V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current		V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current		V_{CC} = 5.5V V_{IL} = 0.4V	Select			−1	mA
				All others			−0.5	
I_O	Output Drive Current		V_{CC} = 5.5V, V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied		V_{CC} = 5.5V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_{CC} = 5.5V V_O = 0.4V				−50	μA
I_{CCH}	Supply Current	AS257	V_{CC} = 5.5V Outputs Open	Outputs High		12.9	18.6	mA
		AS258				8.8	12.6	mA
I_{CCL}	Supply Current	AS257		Outputs Low		20.9	30.1	mA
		AS258				16.8	24.2	mA
I_{CCZ}	Supply Current	AS257		Outputs Disabled		22.2	31.9	mA
		AS258				17.5	25.2	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

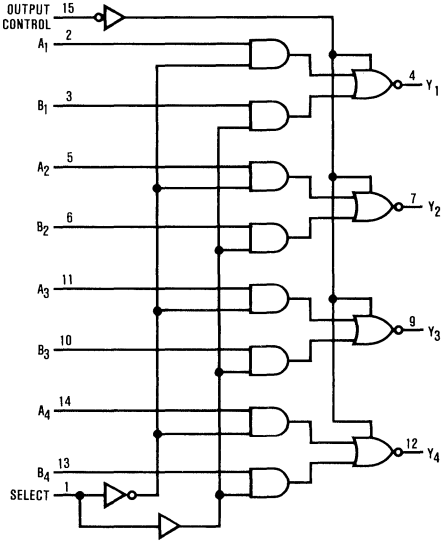
Parameter		From	To	Conditions	DM54AS257,258			DM74AS257,258			Unit
					Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation Delay Time. Low to high Level Output	257	Data	Any Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	1.5	3.5	6.5	1.5	3.5	5.5	ns
	258				1.5	3	6.0	1.5	3	5.0	
T_{PHL}, Propagation Delay Time. High to low Level Output	257				1.5	3.5	7.0	1.5	3.5	6.0	
	258				1	2	5.0	1	2.0	4.0	
T_{PLH}, Propagation Delay Time. Low to high Level Output	257	Select	Any Y		3	5.5	12.0	3	8	13.0	
	258				3	6.5	12.0	3	6.5	11.0	
T_{PHL}, Propagation Delay Time. High to low Level Output	257				3.5	7.5	14.0	3.5	7.5	12.5	
	258				2.5	6	11.0	2.5	6	10.0	
T_{ZH}, Output Enable Time to High Level	257	Output Control	Any Y		2	4	8.0	2	4	7.0	
	258				2	4	8.0	2	4	7.0	
T_{ZL}, Output Enable Time to Low Level	257				2.5	5.5	10.0	2.5	5.5	9.0	
	258				3	6	11.0	3	6	10.0	
T_{HZ}, Output Disable Time. From High Level	257	Output Control	Any Y		1.5	3.5	7.0	1.5	3.5	6.0	
	258				1.5	3.5	7.0	1.5	3.5	6.0	
T_{LZ}, Output Disable Time From Low Level	257				2	4	8.0	2	4	7.0	
	258				2.5	5.5	10.0	2.5	5.5	9.0	

NOTE 1: See notes pg. 1-2, figures pg. 2-2.

Logic Diagrams



54/74AS257



54/74AS258

National Semiconductor

Preliminary

DM54AS352/DM74AS352 Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Strobe inputs and an inverting output buffer. The Strobe inputs, when at the high level, disable their associated data inputs and force the corresponding output to the high state. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

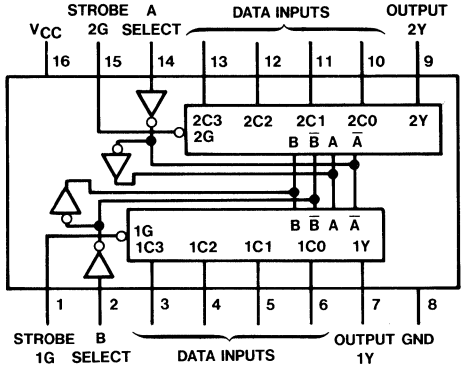
Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process.
- Switching performance is guaranteed over full temperature and V_{CC} supply range.
- Pin and functional compatible with the LS and Schottky Family counterpart.
- Improved output transient handling capability.

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54AS352	−55°C to 125°C
DM74AS352	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54AS352 (J) 74AS352 (J,N)

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections
H = High Level, L = Low Level, X = Don't Care

Recommended Operating Conditions

Parameter	DM54AS352			DM74AS352			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5		5.5	4.5		5.5	V
High Level Input Voltage, V_{IH}	2.0			2.0			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

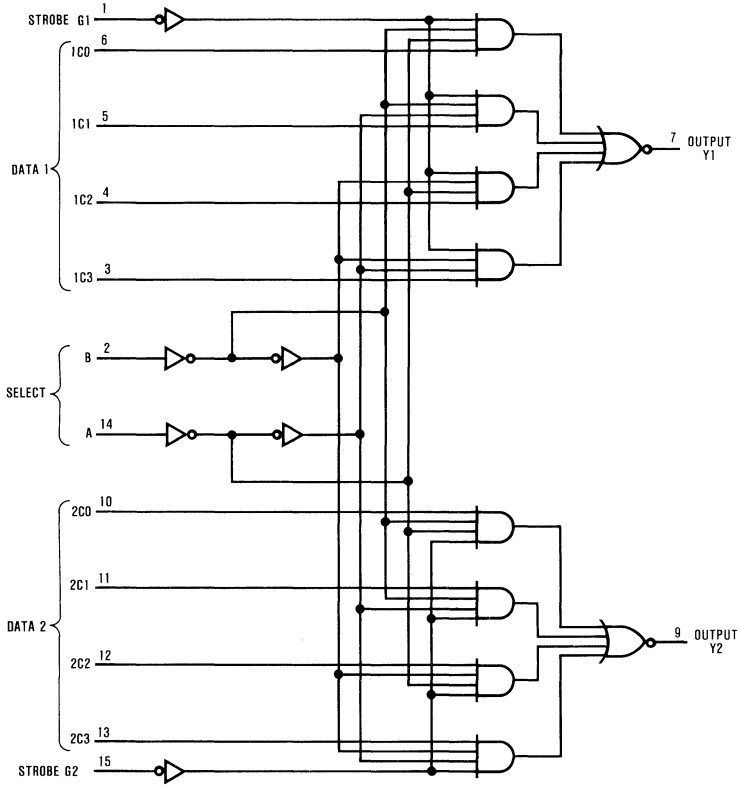
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		IOH = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	A, B			−1.0	mA
			All others			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs high		21	36	ma
			Outputs low		28	48	

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS352			DM74AS352			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	1	4.5	8.5	1	4.5	7.5	ns
t_{PHL}, High to low Level Output				1	4.5	8.5	1	4.5	7.5	ns
t_{PLH}, Low to high Level Output	Data			1	3	6.0	1	3	5.0	ns
t_{PHL}, High to low Level Output				1	2.5	6.0	1	2.5	5.0	ns
t_{PLH}, Low to high Level Output	Strobe			1	4.5	8.5	1	4.5	7.5	ns
t_{PHL}, High to low Level Output				1	4.5	8.5	1	4.5	7.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

Logic Diagram



National Semiconductor

Preliminary

DM54AS353/DM74AS353 TRI-STATE® Dual 4-Line to 1-Line Data Selector/Multiplexer

General Description

This Data Selector/Multiplexer contains full on-chip decoding to select one-of-four data sources as a result of a unique two-bit binary code at the Select inputs. Each of the two Data Selector/Multiplexer circuits have their own separate Select, Data, and Output Control inputs and an inverting TRI-STATE output buffer. The Output Control inputs, when at the high level, place the corresponding output in the high impedance Off state. In order to prevent bus access conflicts, output disable times are shorter than output enable times. The Select input buffers incorporate internal overlap features to ensure that select input changes do not cause invalid output transients.

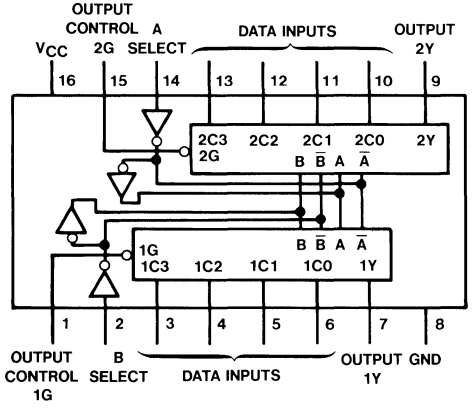
Features

- Advanced Oxide-isolated Ion-implanted Schottky TTL process.
- Switching performance is guaranteed over full temperature and V_{CC} supply range.
- Pin and functional compatible with LS and Schottky Family counterpart.
- Improved output transient handling capability.
- Output Control circuitry incorporates power-up TRI-STATE feature.

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	7.0V
Operating Free Air Temperature Range	
DM54AS353	−55°C to +125°C
DM74AS353	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	+300°C

Connection Diagram



54AS353 (J) 74AS353 (J,N)

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Address inputs A and B are common to both sections
H = High Level. L = Low Level. X = Don't Care.
Z = High Impedance State

Recommended Operating Conditions

Parameter	DM54AS353			DM74AS353			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5		5.5	4.5		5.5	V
High Level Input Voltage, V_{IH}	2.0			2.0			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−1.0			−2.6	mA
Low Level Output Current, I_{OL}			12			24	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

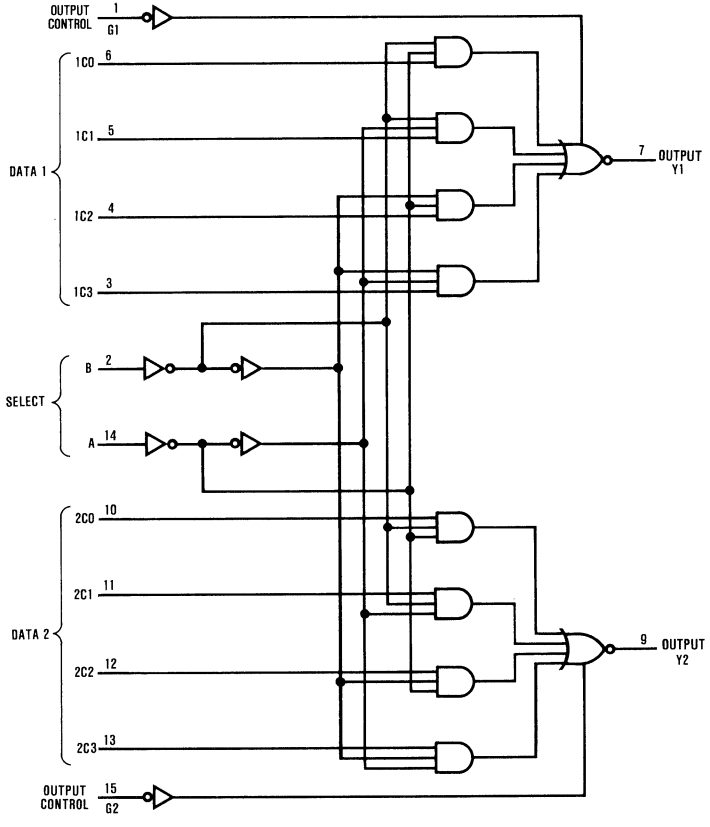
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_{IN} = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = Max		2.4	3.2		V
		IOH = −2mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = Max			.35	.50	V
I_I	Input Current at Max Input Voltage	V_{CC} = 5.5V, V_{IN} = 7V				100	μA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IN} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IN} = 0.4V	A, B			−1.0	mA
			All others			−0.5	
I_O	Output Drive Current	V_{CC} = 5.5V, V_{OUT} = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Bias	V_{CC} = 5.5V, V_{OUT} = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Bias	V_{CC} = 5.5V, V_{OUT} = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs high		21	36	mA
			Outputs low		28	48	
			Outputs disabled		29	50	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS353			DM74AS353			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}, Low to high Level Output	Select	Y	V_{CC} = 4.5 to 5.5V, C_L = 50 pF, R_L = 500 Ω	1	4.5	8.5	1	4.5	8.5	ns
t_{PHL}, High to low Level Output				1	4.5	8.5	1	4.5	8.5	ns
t_{PLH}, Low to high Level Output	Data			1	3	6.0	1	3	6.0	ns
t_{PHL}, High to low Level Output				1	2.5	6.0	1	2.5	6.0	ns
t_{ZH}, Output Enable Time to High Level	Output Control			2	5	9.5	2	5	8.5	ns
t_{ZL}, Output Enable Time to Low Level				2	6	11.0	2	6	10.0	ns
t_{HZ}, Output Disable Time From High Level				1	3	6.0	1	3	5.0	ns
t_{LZ}, Output Disable Time From Low Level				1	4	8.0	1	4	7.0	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-2.

Logic Diagram



National Semiconductor

Preliminary

DM54AS373/DM74AS373 Octal D-Type Transparent Latches

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the AS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

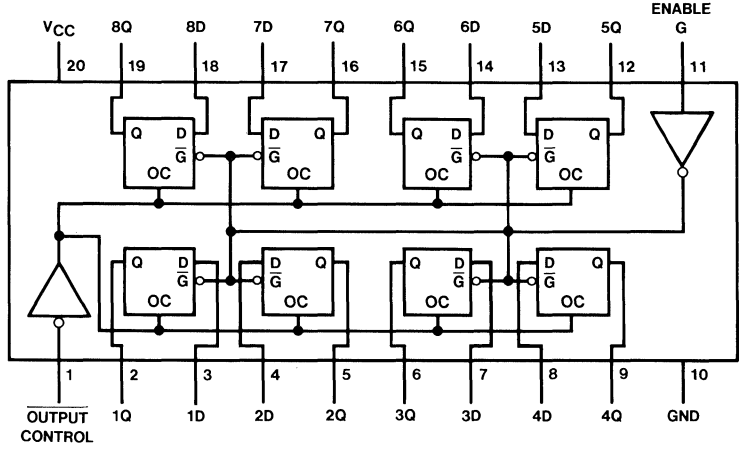
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin For Pin Compatible with LS and ALS TTL Counterparts.
- Improved AC Performance Over LS and ALS TTL Counterparts.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS373	−55°C to 125°C
DM74AS373	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS373 (J) 74AS373 (J,N)

Recommended Operating Conditions

Parameter	DM54AS373			DM74AS373			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Width of Enable Pulse, High							ns
Data Setup Time, T_{SU}							ns
Data Hold Time, T_H							ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V I_{OH} = MAX		2.4	3.2		V
		I_{OH} = −2.0mA		V_{CC}−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		65.0		mA
			Outputs Low		71.6		mA
			Outputs Disabled		76.0		mA

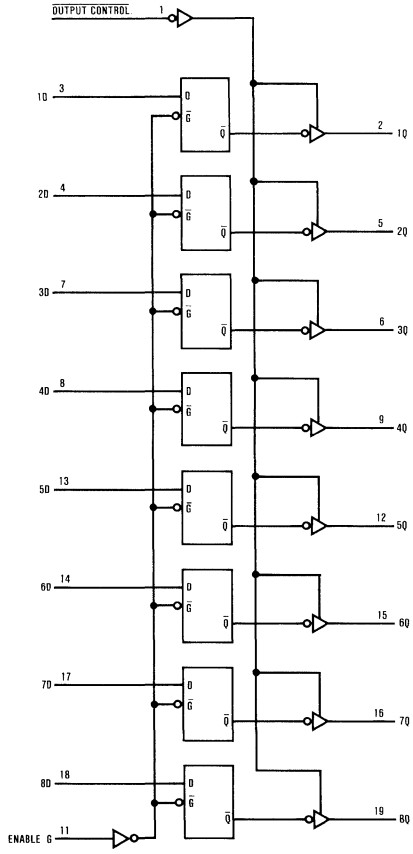
Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS373			DM74AS373			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		4.5			4.5		ns
T_{PHL}					4			4		ns
T_{PLH}	Enable	Any Q			7			7		ns
T_{PHL}					5			5		ns
T_{PZH}	Output Control	Any Q			3.5			3.5		ns
T_{PZL}					5			5		ns
T_{PHZ}					3.5			3.5		ns
T_{PLZ}					5.5			5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

Preliminary

DM54AS374/DM74AS374 Octal D-Type-Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole three-state output designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

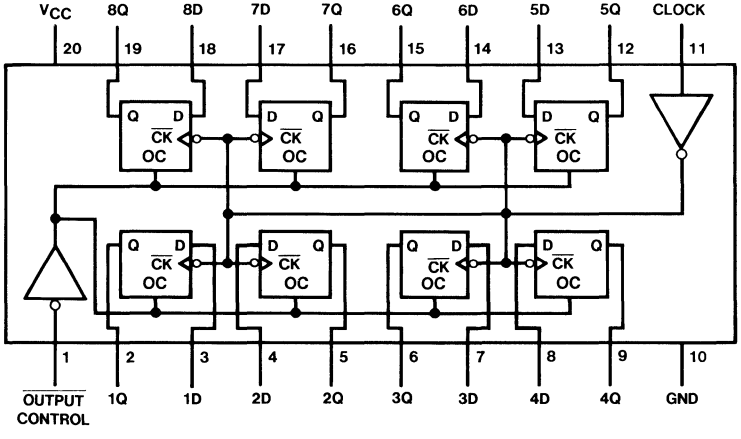
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with LS and ALS TTL Counterparts.
- Improved AC Performance Over LS and ALS TTL Counterparts.
- TRI-STATE® Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS374	−55°C to 125°C
DM74AS374	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS374 (J) 74AS374 (J,N)

Recommended Operating Conditions

Parameter		DM54AS374			DM74AS374			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		90	0		110	MHz
Width of Clock Pulse, T_W	High	5.5			4.5			ns
	Low	5.5			4.5			ns
Data Setup Time, T_{SU}			2↑			2↑		ns
Data Hold Time, T_H			2↑			2↑		ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

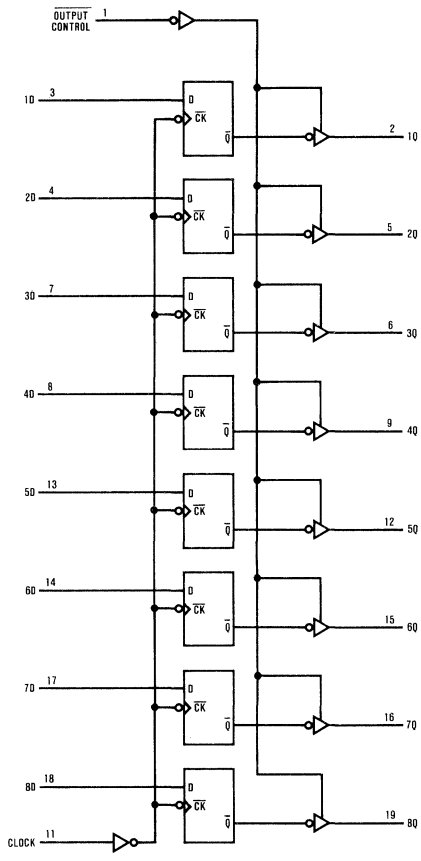
Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V I_{OH} = MAX		2.4	3.2		V
		I_{OH} = −2.0mA		VCC−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		84.6		mA
			Outputs Low		98.7		mA
			Outputs Disabled		98.2		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS374			DM74AS374			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	90	167		110	167		MHz
T_{PLH}	Clock	Any Q			5.5			5.5		ns
T_{PHL}					6			6		ns
T_{PZH}	Output Control	Any Q			3.5			3.5		ns
T_{PZL}					5			5		ns
T_{PHZ}					3.5			3.5		ns
T_{PLZ}					5.5			5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

Preliminary

DM54AS533/DM74AS533
Octal D-Type Transparent Latches With Inverted Outputs

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the AS533 are transparent D-type latches meaning that while the enable (G) is high the $\overline{Q}$ outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

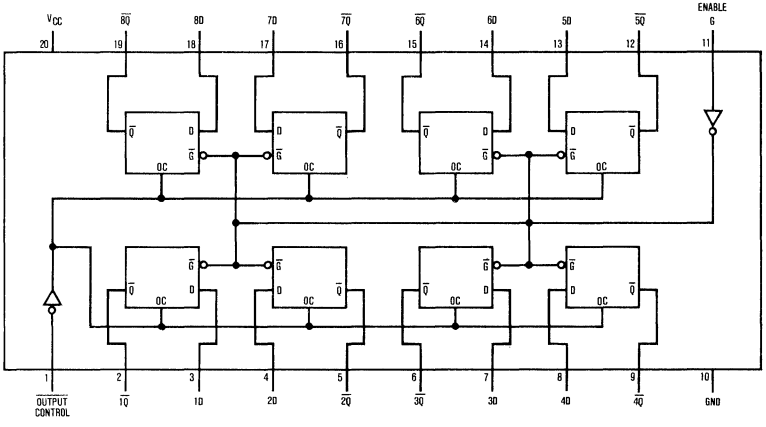
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS533	−55°C to 125°C
DM74AS533	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS533 (J) **74AS533 (J,N)**

Recommended Operating Conditions

Parameter	DM54AS533			DM74AS533			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Width of Enable Pulse, High or Low							ns
Data Setup Time, T_{SU}							ns
Data Hold Time, T_H							ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

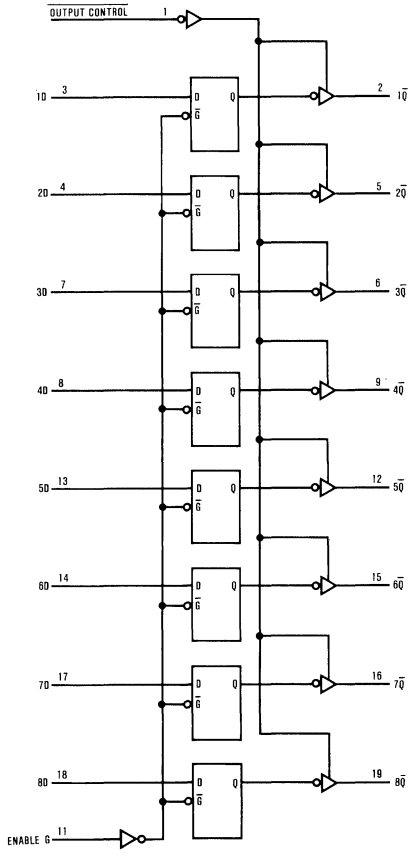
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V, I_{OH} = MAX		2.4	3.2		V
		I_{OH} = −2.0mA		VCC−2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V, I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V, V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{VO} = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High		10	15	mA
			Outputs Low		17	26	mA
			Outputs Disabled		18.5	28	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS533			DM74AS533			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\overline{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		5.5			5.5		ns
T_{PHL}					4			4		ns
T_{PLH}	Enable	Any $\overline{Q}$			7			7		ns
T_{PHL}					5			5		ns
T_{PZH}	Output Control	Any $\overline{Q}$			3.5			3.5		ns
T_{PZL}					5			5		ns
T_{PHZ}					3.5			3.5		ns
T_{PLZ}					5.5			5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

Output Control	Enable G	D	Output $\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low state, H = High State, X = Don't Care
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

Preliminary

DM54AS534/DM74AS534 Octal D-Type Edge-Triggered Flip-Flops With Inverted Outputs

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS534 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the $\overline{Q}$ outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

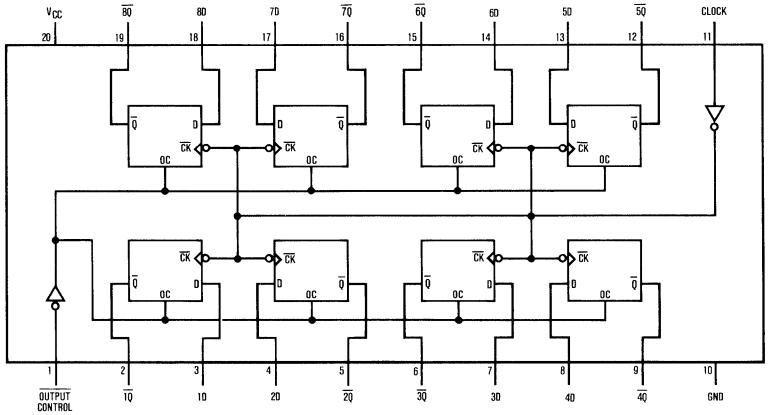
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS534	−55°C to 125°C
DM74AS534	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS534 (J) 74AS534 (J,N)

Recommended Operating Conditions

Parameter		DM54AS534			DM74AS534			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0			0			MHz
Width of Clock Pulse, T_W	High		3			3		ns
	Low		3			3		ns
Data Setup Time, T_{SU}			2↑			2↑		ns
Data Hold Time, T_H			2↑			2↑		ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

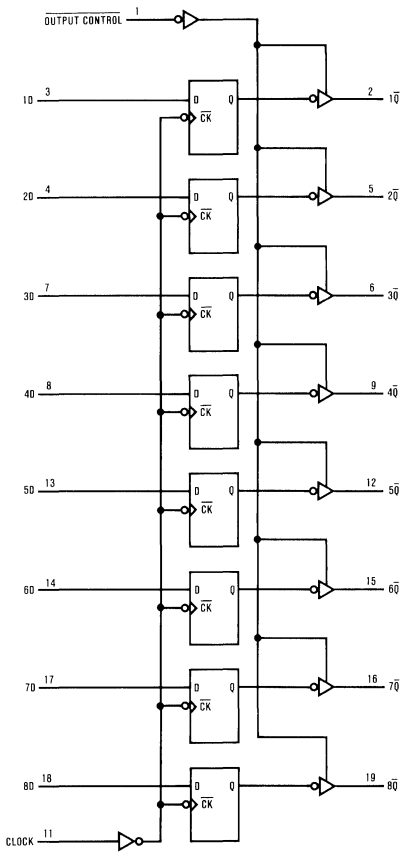
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V I_{OH} = MAX		2.4	3.2		V
		I_{OH} = −2.0mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled				mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS534			DM74AS534			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		167			167		MHz
T_{PLH}	Clock	Any $\overline{Q}$			5.5			5.5		ns
T_{PHL}					6			6		ns
T_{PZH}	Output Control	Any $\overline{Q}$			3.5			3.5		ns
T_{PZL}					5			5		ns
T_{PHZ}					3.5			3.5		ns
T_{PLZ}					5.5			5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

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National Semiconductor

Preliminary

DM54AS573/DM74AS573 Octal D-Type Transparent Latches

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the AS573 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

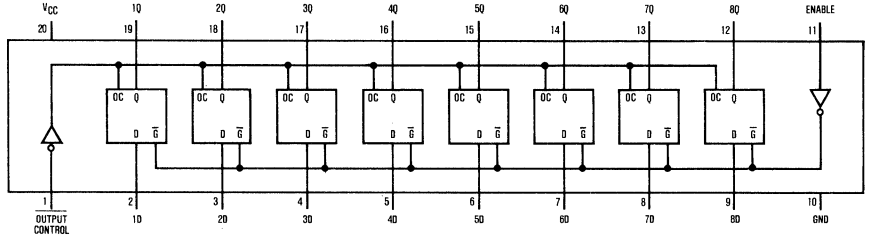
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with S373.
- Improved AC Performance Over S373 at Approximately Half the Power.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS573	−55°C to 125°C
DM74AS573	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS573 (J) **74AS573 (J,N)**

Recommended Operating Conditions

Parameter	DM54AS573			DM74AS573			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Width of Enable Pulse, High or Low							ns
Data Setup Time, T_{SU}							ns
Data Hold Time, T_H							ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −2mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		65		mA

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Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS573			DM74AS573			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		4.5			4.5		ns
T_{PHL}					4			4		ns
T_{PLH}	Enable	Any Q			7			7		ns
T_{PHL}					5			5		ns
T_{PZH}	Output Control	Any Q			3.5			3.5		ns
T_{PZL}					5			5		ns
T_{PHZ}					3.5			3.5		ns
T_{PLZ}					5			5		ns

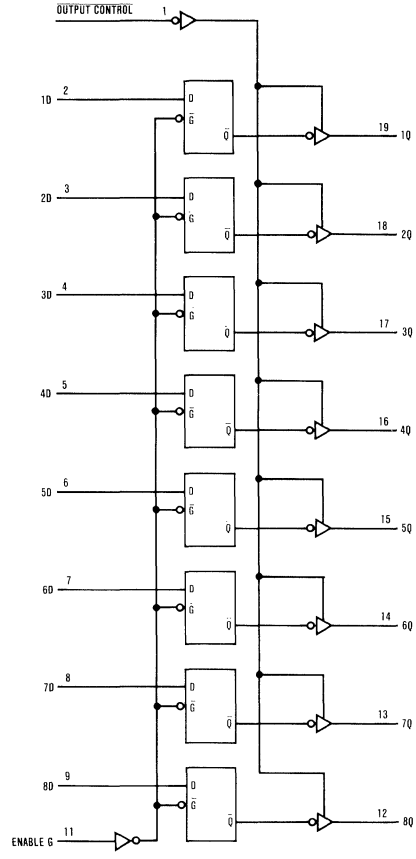
NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Function Table

$\overline{\text{Output}}$ Control	Enable G	D	Output Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

Logic Diagram



National Semiconductor

Preliminary

DM54AS574/DM74AS574 Octal D-Type Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS574 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

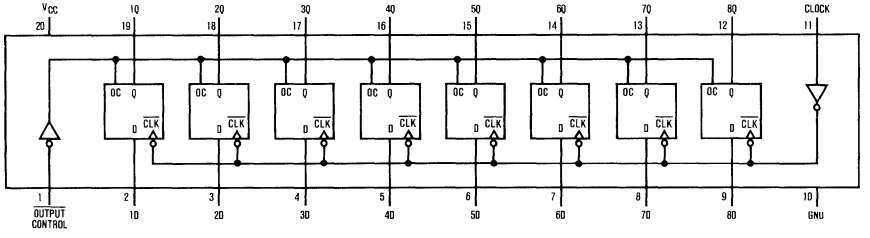
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally Equivalent with S374.
- Improved AC Performance Over S374 at Approximately Half the Power.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS574	−55°C to 125°C
DM74AS574	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS574 (J) **74AS574 (J,N)**

Function Table

$\overline{\text{Output Control}}$	Clock	D	Output Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

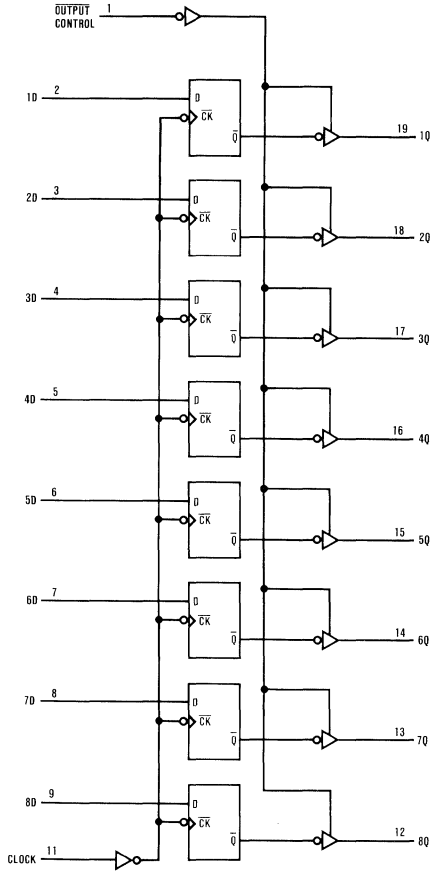
L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

Recommended Operating Conditions

Parameter		DM54AS574			DM74AS574			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0			0			MHz
Width of Clock Pulse, T_W	High							ns
	Low							ns
Data Setup Time, T_{SU}								ns
Data Hold Time, T_H								ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Logic Diagram



Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −2mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		84		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS574			DM74AS574			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		160			160		MHz
T_{PLH}	Clock	Any Q		1	5.5		1	5.5		ns
T_{PHL}				2	6		2	6		ns
T_{PZH}	Output Control	Any Q		1	3.5		1	3.5		ns
T_{PZL}				1	5		1	5		ns
T_{PHZ}	Output Control	Any Q		1	3.5		1	3.5		ns
T_{PLZ}				1	5.5		1	5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

National Semiconductor

Preliminary

DM54AS575/DM74AS575 Octal D-Type Edge-Triggered Flip-Flops with Synchronous Clear

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS575 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

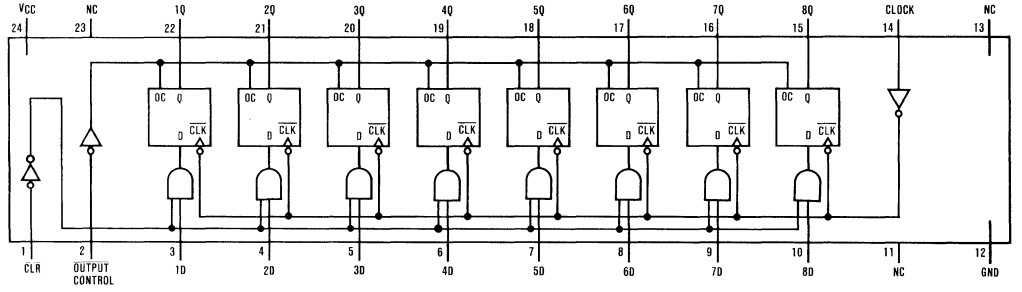
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Synchronous Clear

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS575	−55°C to 125°C
DM74AS575	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS575 (J) **74AS575 (J,N)**

Function Table

$\overline{\text{Output}}$ Control	$\overline{\text{CLR}}$	Clock	D	Output Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q_0
H	X	X	X	Z

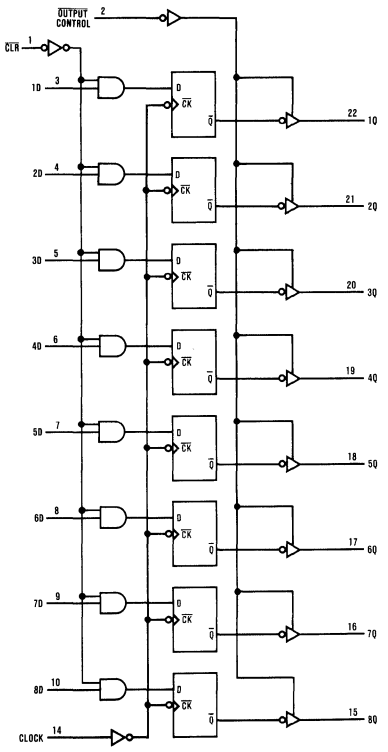
L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q
NC = No Internal Connection

Recommended Operating Conditions

Parameter		DM54AS575			DM74AS575			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0			0			MHz
Width of Clock Pulse, T_W	High							ns
	Low							ns
Data Setup Time, T_{SU}	DATA							ns
	$\overline{CLR}$							
Data Hold Time, T_H	DATA							ns
	$\overline{CLR}$							

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Logic Diagram



Electrical Characteristics over recommended operating free air temperature range (Note 1)

Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −2mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		84		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS575			DM74AS575			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		167			167		MHz
T_{PLH}	Clock	Any Q			5.5			5.5		ns
T_{PHL}					6			6		ns
T_{PZH}	Output Control	Any Q			3.5			3.5		ns
T_{PZL}					5			5		ns
T_{PHZ}	Output Control	Any Q			3.5			3.5		ns
T_{PLZ}					5.5			5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

National Semiconductor

Preliminary

DM54AS576/DM74AS576 Octal D-Type Edge-Triggered Flip-Flops With Inverted Outputs

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS576 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

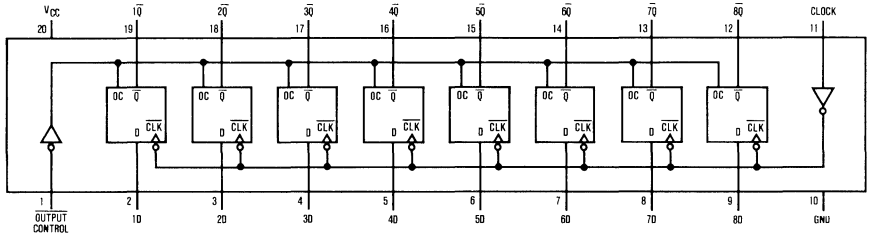
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS576	−55°C to 125°C
DM74AS576	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS576 (J) **74AS576 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS576			DM74AS576			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0			0			MHz
Width of Clock Pulse, T_W	High							ns
	Low							ns
Data Setup Time, T_{SU}								ns
Data Hold Time, T_H								ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

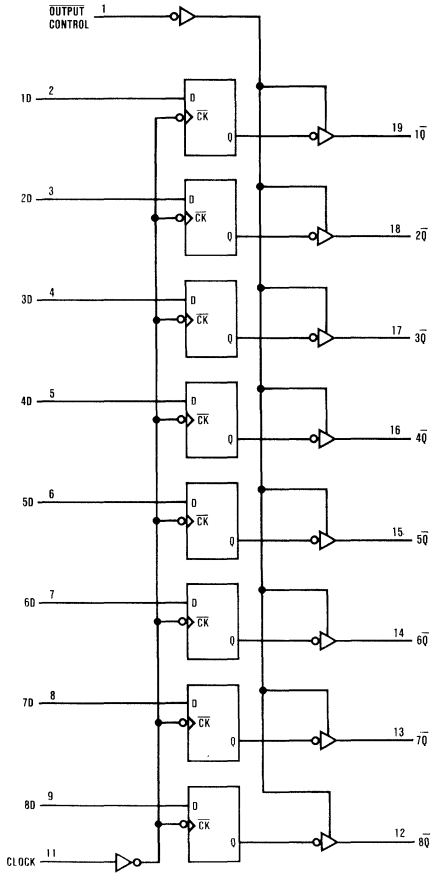
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −2mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		84		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS576			DM74AS576			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		167			167		MHz
T_{PLH}	Clock	Any $\overline{Q}$		1	5.5		1	5.5		ns
T_{PHL}				2	6		2	6		ns
T_{PZH}	Output Control	Any $\overline{Q}$		1	3.5		1	3.5		ns
T_{PZL}				1	5		1	5		ns
T_{PHZ}				1	3.5		1	3.5		ns
T_{PLZ}				1	3.5		1	5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

$\overline{\text{Output}}$ Control	Clock	D	Output $\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

Preliminary

DM54AS577/DM74AS577 Octal D-Type Edge-Triggered Flip-Flops With Inverted Outputs and Synchronous Preset

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS577 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the $\overline{D}$ inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

When the $\overline{PRE}$ is held ion during a positive transition of the clock the $\overline{Q}$ outputs of the flip flops will go low.

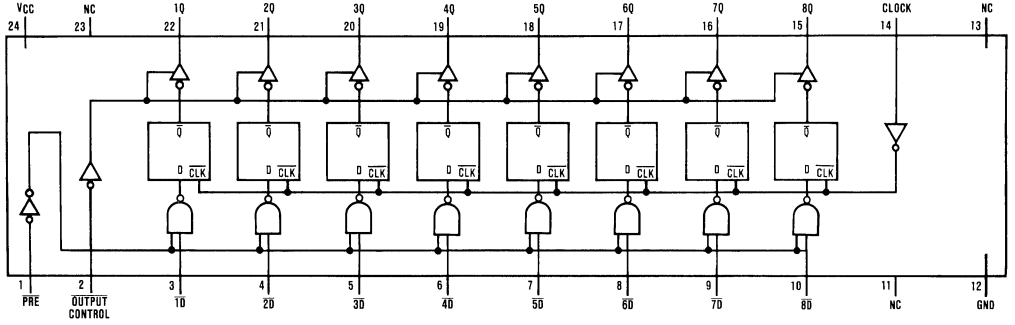
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Synchronous Preset

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS577	−55°C to 125°C
DM74AS577	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS576 (J) 74AS576 (J,N)

Recommended Operating Conditions

Parameter		DM54AS577			DM74AS577			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0			0			MHz
Width of Clock Pulse, T_W	High							ns
	Low							ns
Data Setup Time, T_{SU}	Data							ns
	$\overline{PRE}$							ns
Data Hold Time, T_H	Data							ns
	$\overline{PRE}$							ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −2mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		84		mA

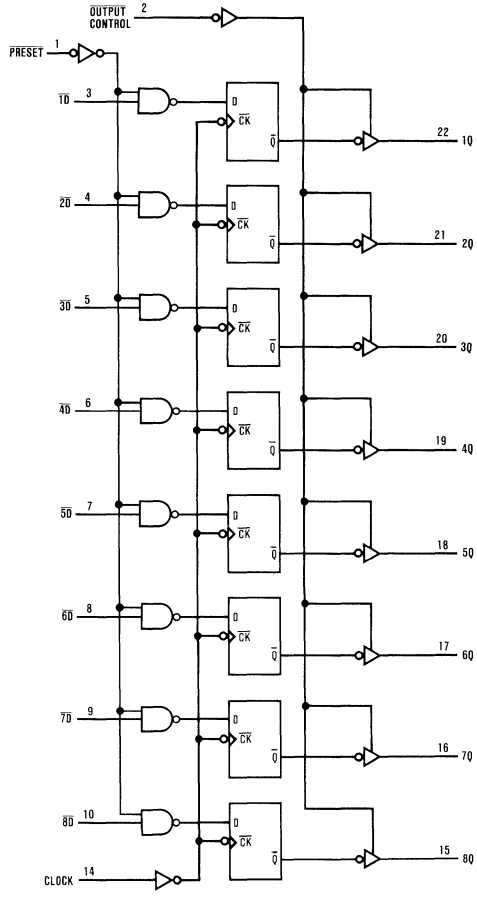
Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS577			DM74AS577			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		167			167		MHz
T_{PLH}	Clock	Any $\overline{Q}$		1	5.5		1	5.5		ns
T_{PHL}				2	6		2	6		ns
T_{PZH}	Output Control	Any $\overline{Q}$		1	3.5		1	3.5		ns
T_{PZL}				1	5		1	5		ns
T_{PHZ}				1	3.5		1	3.5		ns
T_{PLZ}				1	5.5		1	5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

Output Control	$\overline{PRE}$	Clock	$\overline{D}$	Output $\overline{Q}$
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	$\overline{Q}_0$
H	X	X	X	Z

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

Preliminary

DM54AS580/DM74AS580 Octal D-Type Transparent Latches With Inverted Outputs

General Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the AS580 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

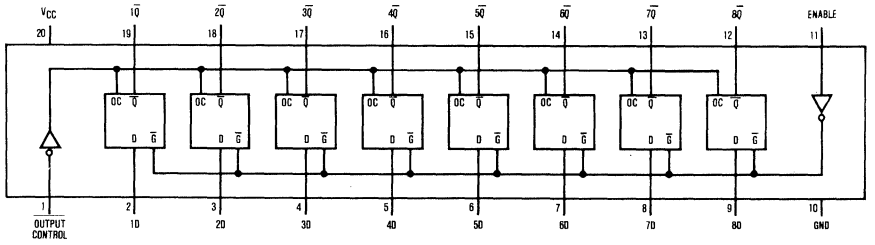
Features

- Switching Specifications at 50pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced, Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS580	−55°C to 125°C
DM74AS580	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS580 (J) **74AS580 (J,N)**

Recommended Operating Conditions

Parameter	DM54AS580			DM74AS580			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Width of Enable Pulse, High or Low							ns
Data Setup Time, T_{SU}							ns
Data Hold Time, T_H							ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

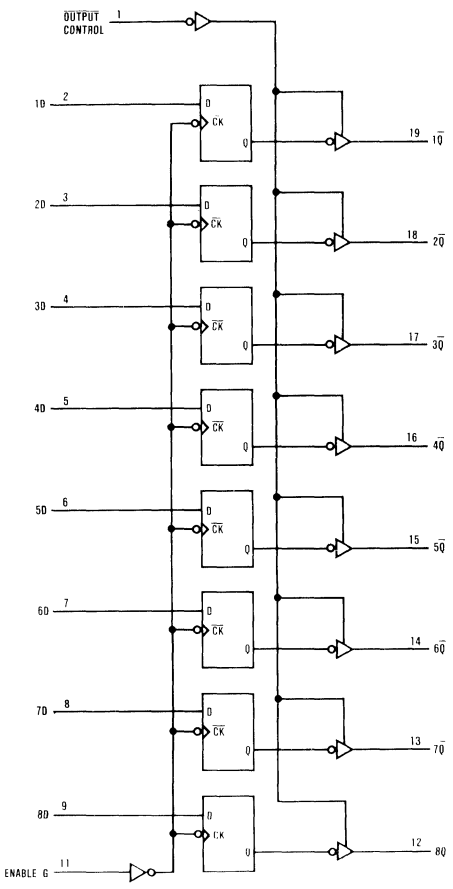
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −2mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		71		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS580			DM74AS580			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\bar{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	1	5.5		1	5.5		ns
T_{PHL}				1	4		1	4		ns
T_{PLH}	Enable	Any $\bar{Q}$		2	7		2	7		ns
T_{PHL}				1	5		1	5		ns
T_{PZH}	Output Control	Any $\bar{Q}$		1	3.5		1	3.5		ns
T_{PZL}				1	5		1	5		ns
T_{PHZ}				1	3.5		1	3.5		ns
T_{PLZ}				1	5.5		1	5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

Output Control	Enable G	D	Output $\bar{Q}$
L	H	H	L
L	H	L	H
L	L	X	$\bar{Q}_0$
H	X	X	Z

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
$\bar{Q}_0$ = Previous Condition of $\bar{Q}$

1

National Semiconductor

Preliminary

DM54AS646,648/DM74AS646,648 Octal Bus Transceivers and Registers

General Description

These bus transceivers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these devices with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the AS646,648 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input bus data is stored.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

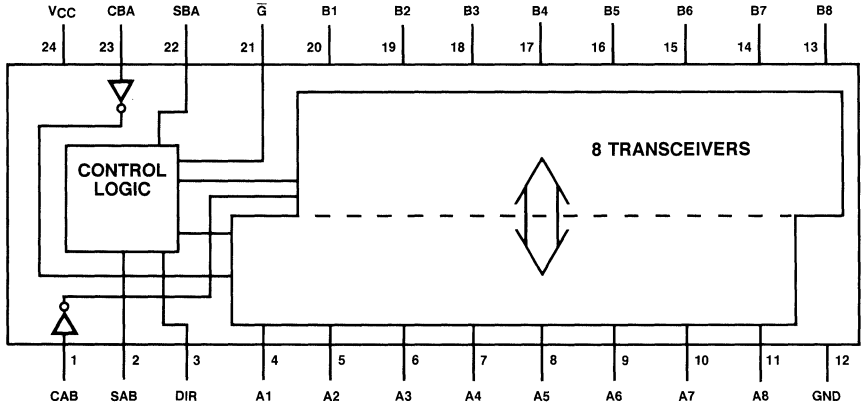
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with LS TTL Counterpart.
- TRI-STATE® Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

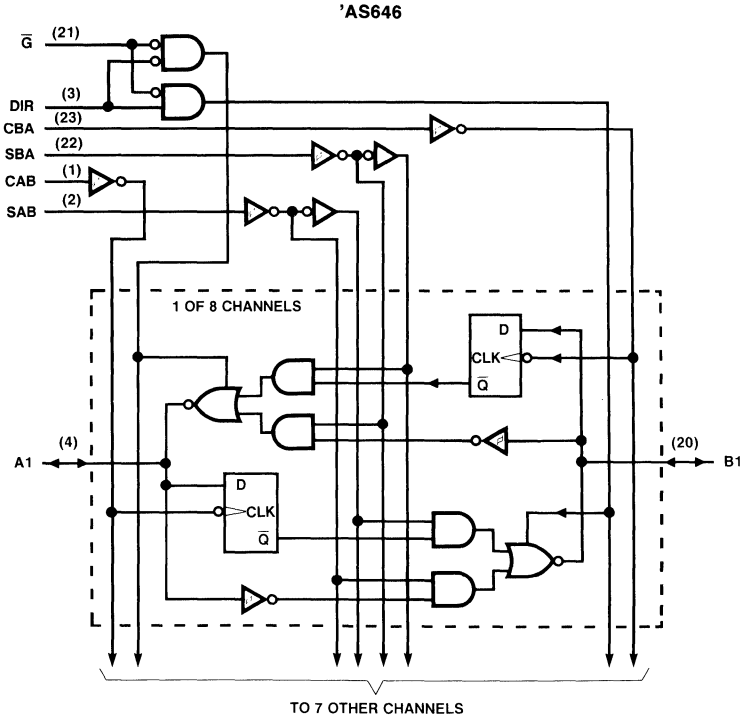
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS646,648	−55°C to 125°C
DM74AS646,648	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

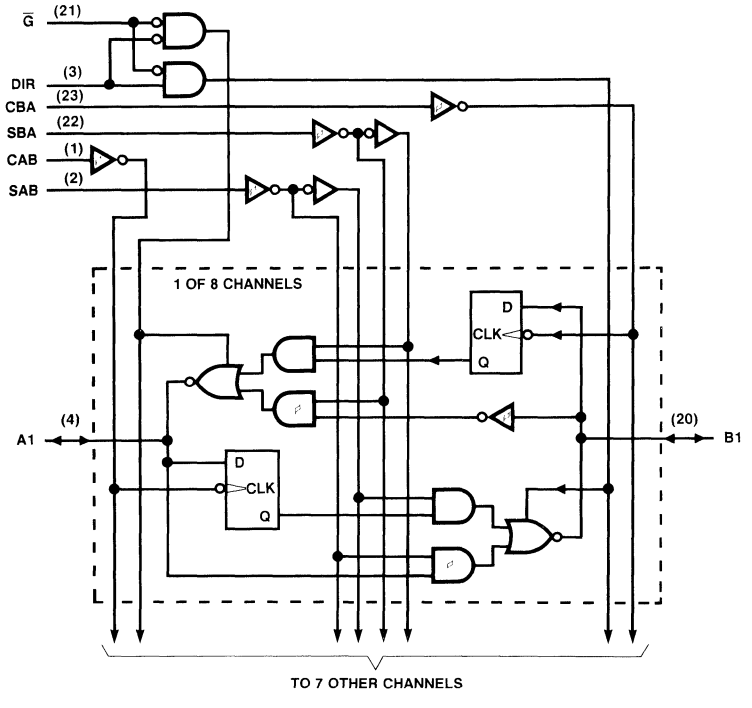


Block Diagram (positive logic)

'AS646

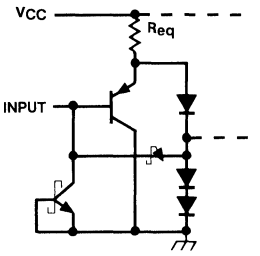


'AS648



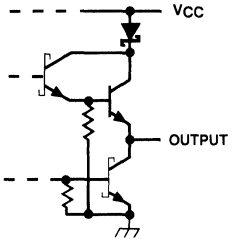
Schematics of Inputs and Outputs

EQUIVALENT OF ALL OTHER INPUTS



A and B: R_{eq} - 10 kΩ NOM
CAB and CBA: R_{eq} - 10 k NOM
ALL OTHER: 5 kΩNOM

TYPICAL OF ALL 'AS646, 'AS648 OUTPUTS



1

Recommended Operating Conditions

Parameter		DM54AS646,648			DM74AS646,648			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		100	MHz
Width of Clock Pulse, T_W	High	5			5			ns
	Low	5			5			ns
Data Setup Time, T_{SU}		5↑			5↑			ns
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics

over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX V_{IH} = V_{IH} MIN	I_{OH} = MAX	2.4	3.2		V
		I_{OH} = −2.0mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V V_{IL} = V_{IL} MIN	I_{OL} = MAX		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−0.5	mA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open and Disabled	'AS648		130	175	mA
			'AS646		150	200	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From (Input)	To (Output)	Conditions	DM54AS646			DM74AS648			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Clock	Bus	R_L = 500 Ω, C_L = 50pF. See Note 2		6.5	10		6.5	10	ns
t_{PHL}					5.5	8		5.5	8	ns
t_{PLH}	Bus	Bus			3.0	5		2.5	4	ns
t_{PHL}					3.5	6		3	5	ns
t_{PLH}	Select, with bus input high	Bus			4	7		4	7	ns
t_{PHL}					3.5	6		3	6	ns
t_{PLH}	Select, with bus input low				5	8		5	8	ns
t_{PHL}					5	8		5	8	ns
t_{PZH}	Enable $\overline{G}$	Bus			8	11		8	11	ns
t_{PZL}					8	11		8	11	ns
t_{PZH}	Direction DIR				8	11		8	11	ns
t_{PZL}					8	11		8	11	ns
t_{PHZ}	Enable $\overline{G}$	Bus	R_L = 500 Ω, C_L = 50pF.		8	10		7	10	ns
t_{PLZ}					8	10		7	10	ns
t_{PHZ}	Direction DIR				8	10		7	10	ns
t_{PLZ}					8	10		7	10	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Function Table

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'AS646	'AS648
H	X	H or L	H or L	X	X	Input	Input	Isolation	Isolation
	X	↑	↑	X	X			Store A and B Data	Store A and B Data
L	L	X	X	X	L	Output	Input	Real Time B Data to A Bus	Real Time $\overline{B}$ Data to A Bus
	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real Time A Data to B Bus	Real Time $\overline{A}$ Data to B Bus
	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data B Bus

H — high level; L — low level; X — irrelevant; ↑ — low-to-high level transition

*The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

National Semiconductor

Preliminary

DM54AS651,652/DM74AS651,652 Octal Bus Transceivers and Registers

General Description

These bus transceivers feature totem-pole three-state output designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these devices with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The registers in the AS651,652 are edge-triggered D-type flip-flops. On the positive transition of the clock (CAB or CBA), the input data is stored.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

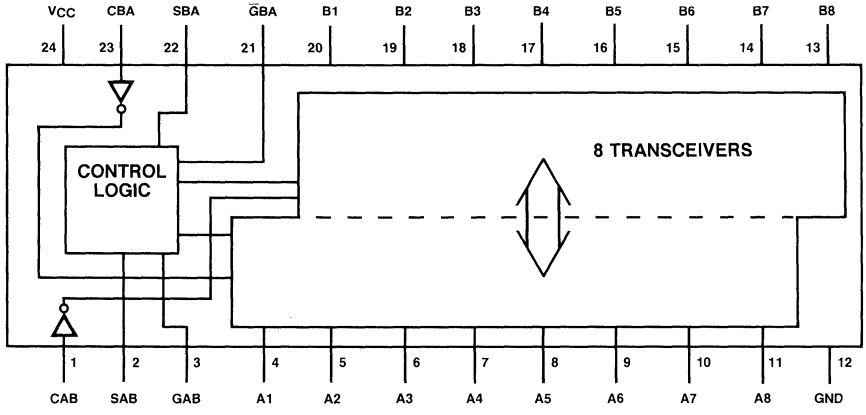
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin-for-Pin Compatible with LS TTL Counterpart.
- TRI-STATE® Buffer-Type Outputs Drive Bus Lines Directly.

Absolute Maximum Ratings

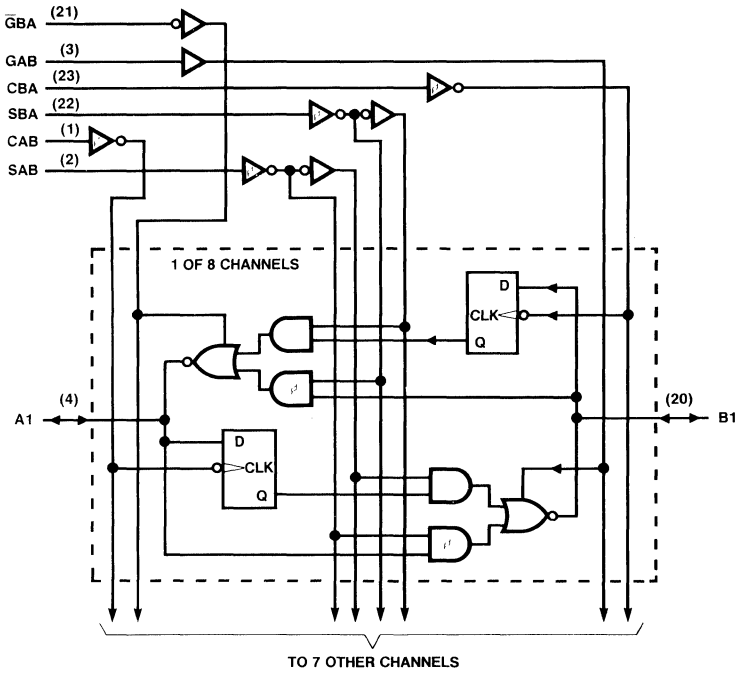
Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS651,652	−55°C to 125°C
DM74AS651,652	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

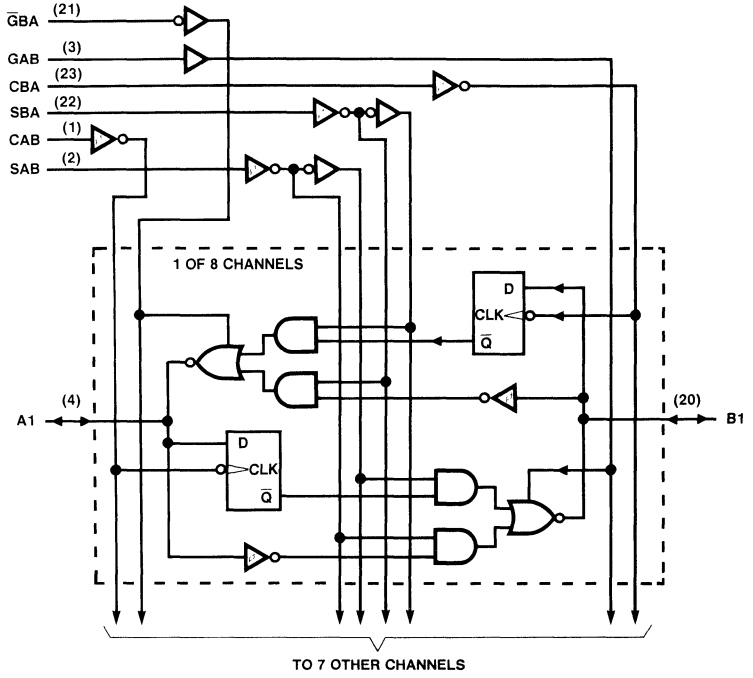


Block Diagram (positive logic)

'AS651

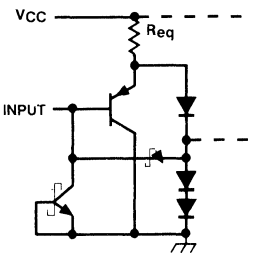


'AS652



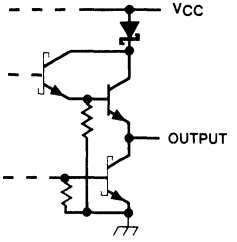
Schematics of Inputs and Outputs

EQUIVALENT OF ALL OTHER INPUTS



A and B: R_{eq} - 10 kΩ NOM
CAB and CBA: R_{eq} - 10 k NOM
ALL OTHER: 5 kΩNOM

TYPICAL OF ALL 'AS651, 'AS652 OUTPUTS



Recommended Operating Conditions

Parameter		DM54AS651,652			DM74AS651,652			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0		100	0		100	MHz
Width of Clock Pulse, T_W	High	5			5			ns
	Low	5			5			ns
Data Setup Time, T_{SU}		5↑			5↑			ns
Data Hold Time, T_H		0↑			0↑			ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX V_{IH} = V_{IH} MIN	I_{OH} = MAX	2.4	3.2		V
		I_{OH} = −2.0mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V V_{IL} = V_{IL} MIN	I_{OL} = MAX		0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−0.5	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open and Disabled	'AS651		130	175	mA
			'AS652		150	200	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From (Input)	To (Output)	Conditions	'AS651			'AS652			Unit
				Min	Typ	Max	Min	Typ	Max	
t_{PLH}	Clock	Bus	$R_L = 500\ \Omega$, $C_L = 50pF$. See Note 2		6.5	10		6.5	10	ns
t_{PHL}					5.5	8		5.5	8	ns
t_{PLH}	Bus	Bus			2.5	4		3	5	ns
t_{PHL}					3	5		3.5	6	ns
t_{PLH}	Select, with bus input high	Bus			4	7		4	7	ns
t_{PHL}					3.5	6		3.5	6	ns
t_{PLH}	Select, with bus input low				5	8		5	8	ns
t_{PHL}					5	8		5	8	ns
t_{PZH}	Enable $\overline{G}BA$	A Bus			7	10		7	10	ns
t_{PZL}					7	10		7	10	ns
t_{PZH}	Enable GAB	B Bus			8	11		8	11	ns
t_{PZL}					8	11		8	11	ns
t_{PHZ}	Enable $\overline{G}BA$	A Bus	$R_L = 500\ \Omega$ $C_L = 50pF$.		7	9		7	9	ns
t_{PLZ}					7	9		7	9	ns
t_{PHZ}	Enable GAB	B Bus			8	10		8	10	ns
t_{PLZ}					8	10		8	10	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Function Table

INPUTS						DATA I/O*		OPERATION OR FUNCTION	
GAB	$\overline{G}BA$	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'AS651	'AS652
L L	H H	H or L ↑	H or L ↑	X X	X X	Input	Input	Isolation Store A and B Data	Isolation Store A and B Data
L L	L L	X X	X H or L	X X	L H	Output	Input	Real Time $\overline{B}$ Data to A Bus Stored $\overline{B}$ Data to A Bus	Real Time B Data to A Bus Stored B Data to A Bus
H H	H H	X H or L	X X	L H	X X	Input	Output	Real Time $\overline{A}$ Data to B Bus Stored $\overline{A}$ Data to B Bus	Real Time A Data to B Bus Stored A Data B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored $\overline{A}$ Data to B Bus & Stored $\overline{B}$ Data to A Bus	Stored A Data to B Bus & Stored B Data to A Bus

H — high level L — low level X — irrevelant ↑ — low-to-high-level transition

*The data output functions may be enabled or disabled by various signals at the GAB and $\overline{G}BA$ inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

National Semiconductor

Preliminary

DM54AS804A/DM74AS804A Hex 2-Input NAND Drivers

Features

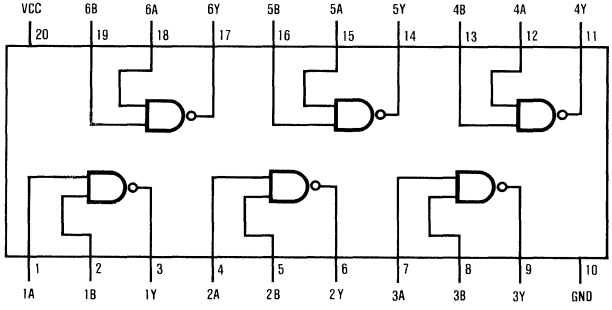
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Advanced Low Power Schottky TTL Counterpart.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54AS804A (J) 74AS804A (J,N)

Recommended Operating Conditions

Parameter	DM54AS804A			DM74AS804A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
		I_{OH} = −3mA		2.4			
		I_{OH} = MAX		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX V_{IH} = 2V			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−150		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		2.5	4	mA
			Outputs Low		16	27	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS804A			DM74AS804A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high level output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.0	2.2	4.5	1.0	2.2	3.5	ns
T_{PHL}, Propagation delay time. High to low level output		1.0	2.6	4.5	1.0	2.6	3.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS805A/DM74AS805A Hex 2-Input NOR Drivers

Features

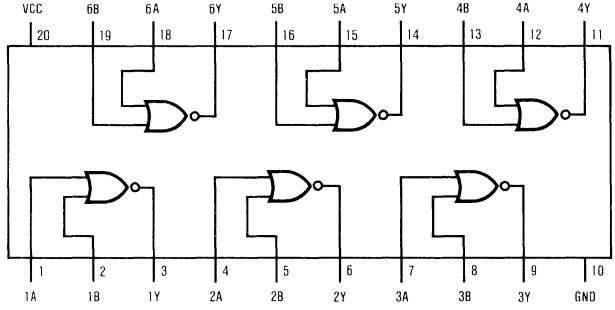
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Advanced Low Power Schottky TTL Counterpart.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{A+B}$



54AS805A (J) 74AS805A (J,N)

Recommended Operating Conditions

Parameter	DM54AS805A			DM74AS805A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4mA		V_{CC}−2			V
		I_{OH} = −3mA		2.4			
		I_{OH} = MAX		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−150		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		5	9	mA
			Outputs Low		18	32	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS805A			DM74AS805A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.0	2.3	4.5	1.0	2.3	4.0	ns
T_{PHL}, Propagation delay time. High to low Level Output		1.0	2.8	4.5	1.0	2.8	4.0	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS808A/DM74AS808A Hex 2-Input AND Drivers

Features

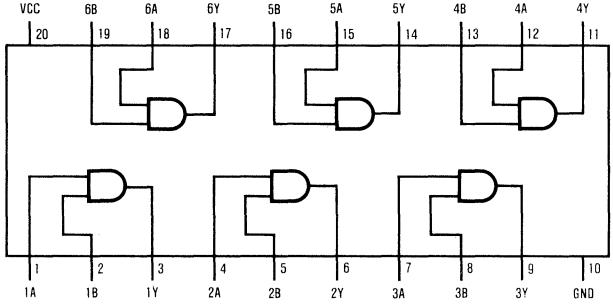
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Advanced Low Power Schottky TTL Counterpart.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = \overline{AB}$



54AS808A (J) **74AS808A (J,N)**

Recommended Operating Conditions

Parameter	DM54AS808A			DM74AS808A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −.4mA		V_{CC}−2			V
		I_{OH} = −3mA		2.4			
		I_{OH} = MAX		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−150		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		6.5	11	mA
			Outputs Low		19	32	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS808A			DM74AS808A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.0	3.4	6.0	1.0	3.4	5.0	ns
T_{PHL}, Propagation delay time. High to low Level Output		1.0	3.6	6.0	1.0	3.6	5.0	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

Preliminary

DM54AS832A/DM74AS832A Hex 2-Input OR Drivers

Features

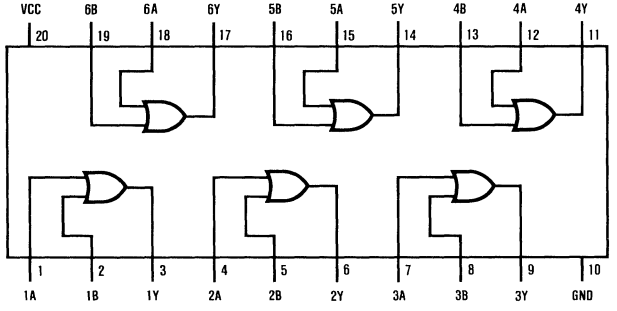
- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- Functionally and Pin for Pin Compatible with Schottky and Low Power Schottky TTL Counterpart.
- Improved AC Performance Over Schottky and Low Power Schottky Counterparts.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS	−55°C to 125°C
DM74AS	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram

$Y = A+B$



54AS832A (J) 74AS832A (J,N)

Recommended Operating Conditions

Parameter	DM54AS832A			DM74AS832A			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Current, I_{OH}			−40			−48	mA
Low Level Output Current, I_{OL}			40			48	mA

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V, I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	I_{OH} = −.4mA		V_{CC}−2			V
		I_{OH} = −3mA		2.4			
		I_{OH} = MAX		2			
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V, V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V, V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V, V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V	V_O = 2.25V		−150		mA
I_{CC}	Supply Current	V_{CC} = 5.5V	Outputs High		9	15	mA
			Outputs Low		22	36	mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	Conditions	DM54AS832A			DM74AS832A			Unit
		Min	Typ	Max	Min	Typ	Max	
T_{PLH}, Propagation delay time. Low to high Level Output	V_{CC} = 4.5 to 5.5V R_L = 500 Ω, C_L = 50 pF.	1.0	3.6	7.0	1.0	3.6	5.5	ns
T_{PHL}, Propagation delay time. High to low Level Output		1.0	4.1	6.5	1.0	4.1	5.5	ns

NOTE 1: See notes pg. 1-2, figures pg. 2-1.

National Semiconductor

DM54AS873/DM74AS873
Dual 4-Bit D-Type Transparent Latches

General Description

These Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the AS873 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output conrol does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

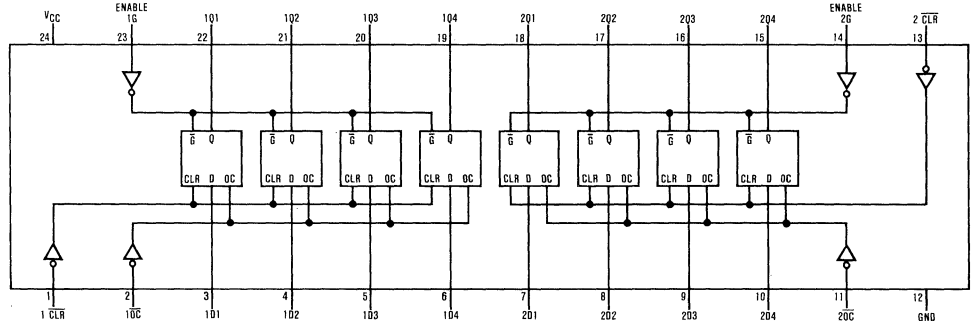
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS873	−55°C to 125°C
DM74AS873	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS873 (J) **74AS873 (J,N)**

Recommended Operating Conditions

Parameter	DM54AS873			DM74AS873			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Pulse Width, T_W Enable High Clear Low							ns
Data Setup Time, T_{SU}							ns
Data Hold Time, T_H							ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

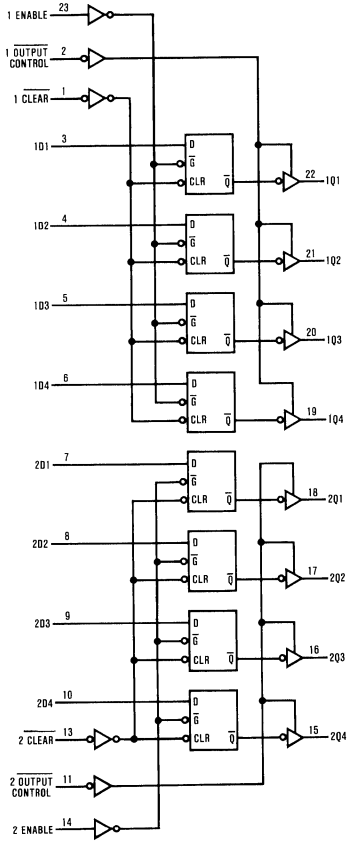
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −400μA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		80		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS873			DM74AS873			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any Q	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	1	4.5		1	4.5		ns
T_{PHL}				1	4		1	4		ns
T_{PLH}	Enable	Any Q		2	7		2	7		ns
T_{PHL}				1	5		1	5		ns
T_{PZH}	Output Control	Any Q		1	3.5		1	3.5		ns
T_{PZL}				1	5		1	5		ns
T_{PHZ}				1	3.5		1	3.5		ns
T_{PLZ}				1	5.5		1	5.5		ns
T_{PHL}	Clear	Any Q		2	6		2	6		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

$\overline{CLR}$	D	EN	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	H
H	L	H	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

DM54AS874/DM74AS874
Dual 4-Bit D-Type Edge-Triggered Flip-Flops

General Description

These Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS874 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

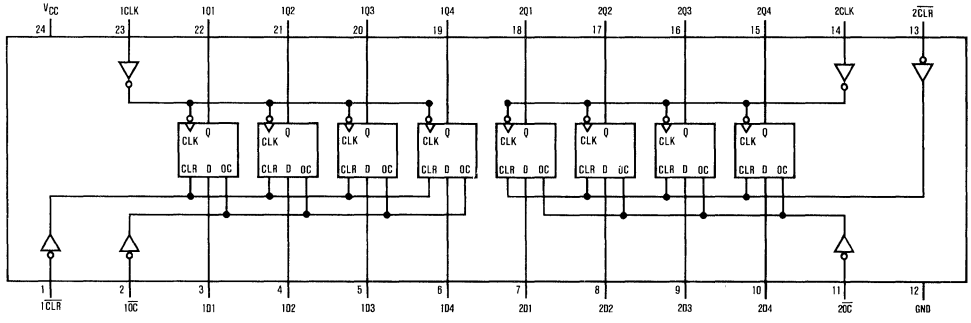
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS874	−55°C to 125°C
DM74AS874	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS874 (J) **74AS874 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS874			DM74AS874			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0			0			MHz
Width of Clock Pulse, T_W	High							ns
	Low							ns
Width of Clear Pulse, T_W	Low							ns
Data Setup Time, T_{SU}								ns
Data Hold Time, T_H								ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

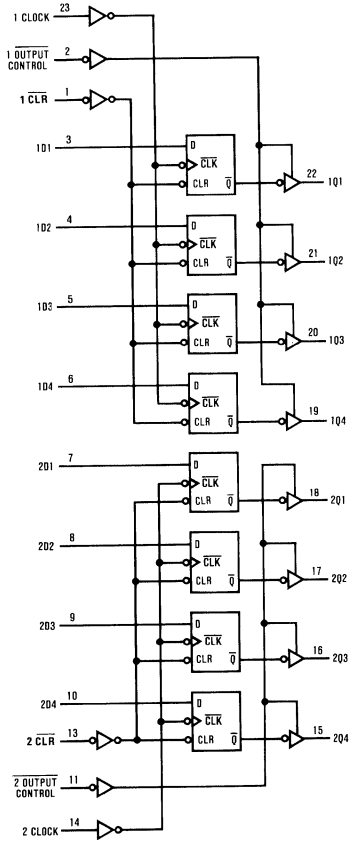
Parameter		Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −400μA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		100		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS874			DM74AS874			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		167			167		MHz
T_{PLH}	Clock	Any Q		1	5.5		1	5.5		ns
T_{PHL}				2	6		2	6		ns
T_{PZH}	Output Control	Any Q		1	3.5		1	3.5		ns
T_{PZL}				1	5		1	5		ns
T_{PHZ}				1	3.5		1	3.5		ns
T_{PLZ}				1	5.5		1	5.5		ns
T_{PHL}	Clear	Any Q		2	7		2	7		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

DM54AS876/DM74AS876 Dual 4-Bit D-Type Edge-Triggered Flip-Flops With Inverted Outputs

General Description

These inverting Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS876 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

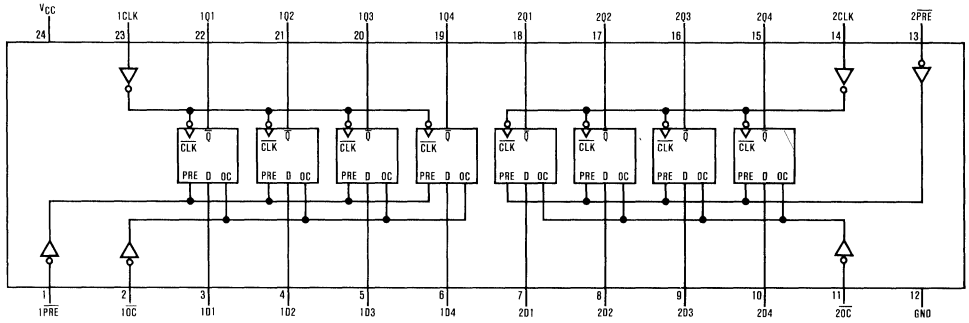
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS876	−55°C to 125°C
DM74AS876	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS876 (J) **74AS876 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS876			DM74AS876			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0			0			MHz
Width of Clock Pulse, T_W	High							ns
	Low							ns
Width of Preset Pulse, T_W	Low							ns
Data Setup Time, T_{SU}								ns
Data Hold Time, T_H								ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −400μA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		100		mA

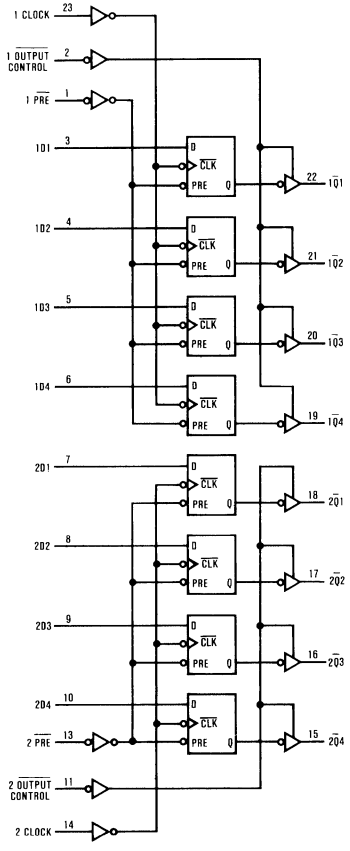
Switching Characteristics

over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS876			DM74AS876			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		167			167		MHz
T_{PLH}	Clock	Any $\overline{Q}$		1	5.5		1	5.5		ns
T_{PHL}				2	6		2	6		ns
T_{PZH}	Output Control	Any $\overline{Q}$		1	3.5		1	3.5		ns
T_{PZL}				1	5		1	5		ns
T_{PHZ}				1	3.5		1	3.5		ns
T_{PLZ}				1	5.5		1	5.5		ns
T_{PHL}	Preset	Any $\overline{Q}$		2	7		2	7		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

$\overline{PRE}$	D	CLK	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

Preliminary

DM54AS878/DM74AS878 Dual 4-Bit D-Type Edge-Triggered Flip-Flops with Synchronous Clear

General Description

These Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS878 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

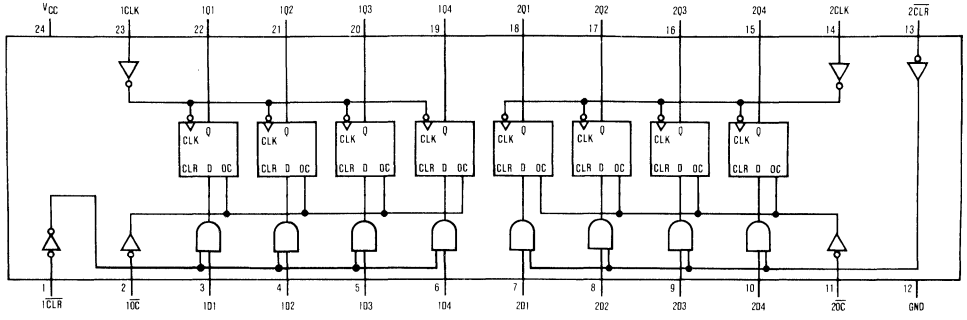
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.
- Synchronous clear.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS878	−55°C to 125°C
DM74AS878	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS878 (J) **74AS878 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS878			DM74AS878			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−12	mA
Low Level Output Current, I_{OL}				32			48	mA
Clock frequency, f_{CLOCK}		0			0			MHz
Width of Clock Pulse, T_W	High							ns
	Low							ns
Data Setup Time, T_{SU}	Data							ns
	$\overline{CLR}$							ns
Data Hold Time, T_H	Data							ns
	$\overline{CLR}$							ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

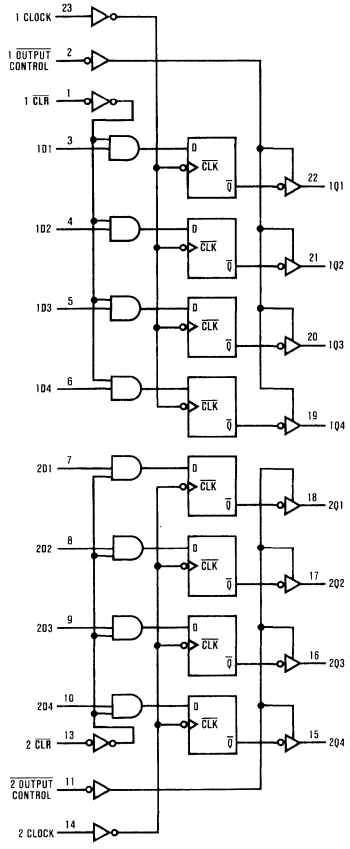
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −400μA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		100		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS878			DM74AS878			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		167			167		MHz
T_{PLH}	Clock	Any Q			5.5			5.5		ns
T_{PHL}					6			6		ns
T_{PZH}	Output Control	Any Q			3.5			3.5		ns
T_{PZL}					5			5		ns
T_{PHZ}					3.5			3.5		ns
T_{PLZ}					5.5			5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

$\overline{CLR}$	D	CLK	$\overline{OC}$	Q
X	X	X	H	Z
L	X	↑	L	L
H	H	↑	L	H
H	L	↑	L	L
H	X	L	L	Q_0

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
Q_0 = Previous Condition of Q

National Semiconductor

Preliminary

DM54AS879/DM74AS879 Dual 4-Bit D-Type Edge-Triggered Flip-Flops With Inverted Outputs and Synchronous Preset

General Description

These inverting Dual 4-Bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the AS879 are edge-triggered inverting D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the complement of the logic states that were set up at the D inputs.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

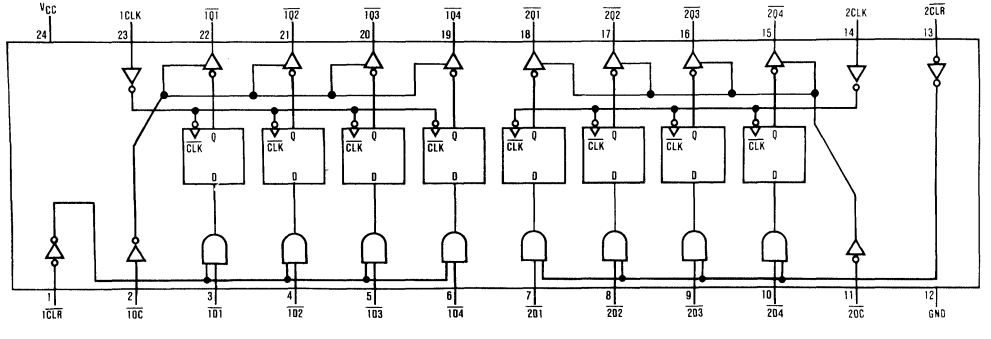
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.
- Synchronous Preset.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS879	−55°C to 125°C
DM74AS879	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS879 (J) **74AS879 (J,N)**

Recommended Operating Conditions

Parameter		DM54AS879			DM74AS879			Unit
		Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}		2			2			V
Low Level Input Voltage, V_{IL}				0.8			0.8	V
High Level Output Voltage, V_{OH}				5.5			5.5	V
High Level Output Current, I_{OH}				−12			−15	mA
Low Level Output Current, I_{OL}				32			32	mA
Clock frequency, f_{CLOCK}		0			0			MHz
Width of Clock Pulse, T_W	High							ns
	Low							ns
Width of Preset Pulse, T_W	Low							ns
Data Setup Time, T_{SU}	Data							ns
	$\overline{PRE}$							ns
Data Hold Time, T_H	Data							ns
	$\overline{PRE}$							ns

The (↑) arrow indicates the positive edge of the Clock is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

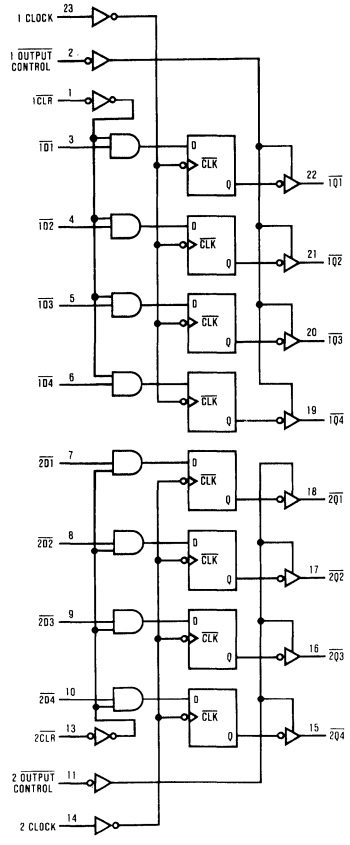
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −400μA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OH} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		100		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS879			DM74AS879			Unit
				Min	Typ	Max	Min	Typ	Max	
F_{MAX}			V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF		167			167		MHz
T_{PLH}	Clock	Any $\overline{Q}$		1	5.5			5.5		ns
T_{PHL}				2	6			6		ns
T_{PZH}	Output Control	Any $\overline{Q}$		1	3.5			3.5		ns
T_{PZL}				1	5			5		ns
T_{PHZ}				1	3.5			3.5		ns
T_{PLZ}				1	5.5			5.5		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram



Function Table

$\overline{PRE}$	D	CLK	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	↑	L	H
H	H	↑	L	L
H	L	↑	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
↑ = Positive Edge Transition
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

National Semiconductor

DM54AS880/DM74AS880 Dual 4-Bit D-Type Transparent Latches With Inverted Outputs

General Description

These Dual 4-Bit inverting registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight inverting latches of the AS880 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the complement of the data (D) inputs. When the enable is taken low the output will be latched at the complement of the level of the data that was set up.

A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches. That is, the old data can be retained or new data can be entered even while the outputs are off.

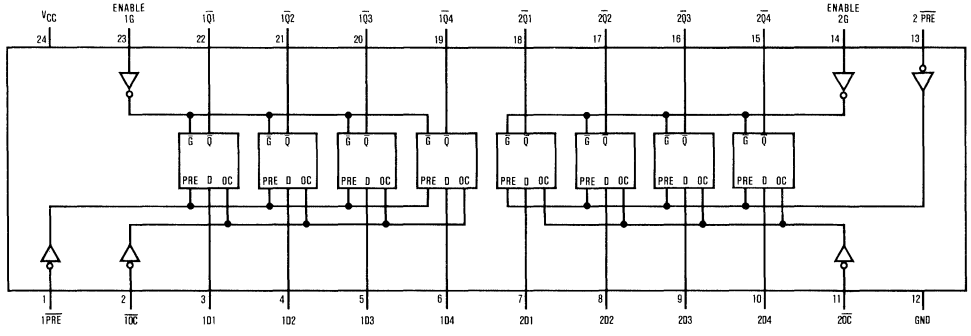
Features

- Switching Specifications at 50 pF.
- Switching Specifications Guaranteed Over Full Temperature and V_{CC} Range.
- Advanced Oxide-Isolated, Ion-Implanted Schottky TTL Process.
- 3-State Buffer-Type Outputs Drive Bus Lines Directly.
- Space Saving 300 Mil Wide Package.

Absolute Maximum Ratings

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54AS880	−55°C to 125°C
DM74AS880	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

Connection Diagram



54AS880 (J) **74AS880 (J,N)**

Recommended Operating Conditions

Parameter	DM54AS880			DM74AS880			Unit
	Min	Nom	Max	Min	Nom	Max	
Supply Voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
High Level Input Voltage, V_{IH}	2			2			V
Low Level Input Voltage, V_{IL}			0.8			0.8	V
High Level Output Voltage, V_{OH}			5.5			5.5	V
High Level Output Current, I_{OH}			−12			−15	mA
Low Level Output Current, I_{OL}			32			48	mA
Pulse Width, T_W Enable Preset Low							ns ns
Data Setup Time, T_{SU}							ns
Data Hold Time, T_H							ns

The (↓) arrow indicates the negative edge of the enable is used for reference.

Electrical Characteristics over recommended operating free air temperature range (Note 1)

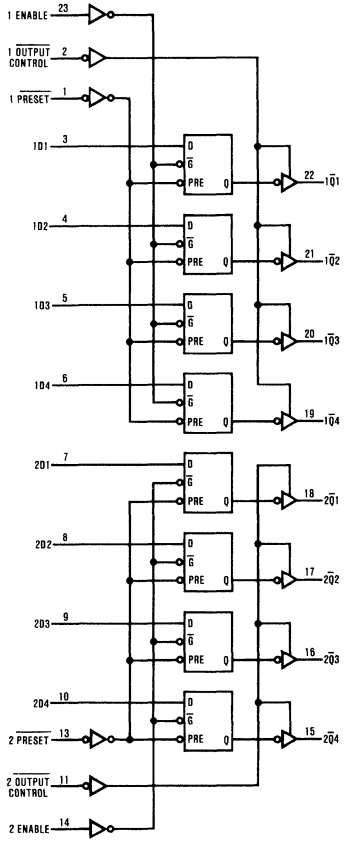
	Parameter	Conditions		Min	Typ	Max	Unit
V_{IK}	Input Clamp Voltage	V_{CC} = 4.5V I_I = −18mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = 4.5V V_{IL} = V_{IL} MAX I_{OH} = MAX		2.4	3.3		V
		I_{OH} = −2mA		V_{CC} −2			V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.5V V_{IH} = 2V I_{OL} = MAX			0.35	0.5	V
I_I	Max High Input Current	V_{CC} = 5.5V V_{IH} = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = 5.5V V_{IH} = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = 5.5V V_{IL} = 0.4V				−0.5	mA
I_O	Output Drive Current	V_{CC} = 5.5V V_O = 2.25V		−30		−110	mA
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 2.7V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = 5.5V V_{IH} = 2V V_O = 0.4V				−50	μA
I_{CC}	Supply Current	V_{CC} = 5.5V Outputs Open	Outputs High				mA
			Outputs Low				mA
			Outputs Disabled		86		mA

Switching Characteristics over recommended operating free air temperature range (Note 1)

Parameter	From	To	Conditions	DM54AS880			DM74AS880			Unit
				Min	Typ	Max	Min	Typ	Max	
T_{PLH}	Data	Any $\overline{Q}$	V_{CC} = 4.5V to 5.5V R_L = 500 Ω C_L = 50 pF	1	5.5		1	5.5		ns
T_{PHL}				1	4		1	4		ns
T_{PLH}	Enable	Any $\overline{Q}$		2	7		2	7		ns
T_{PHL}				1	5		1	5		ns
T_{PZH}	Output Control	Any $\overline{Q}$		1	3.5		1	3.5		ns
T_{PZL}				1	5		1	5		ns
T_{PHZ}				1	3.5		1	3.5		ns
T_{PLZ}				1	5.5		1	5.5		ns
T_{PHL}	Preset	Any $\overline{Q}$		2	6		2	6		ns

NOTE 1: See notes pg. 1-2, figures pg. 2-4.

Logic Diagram

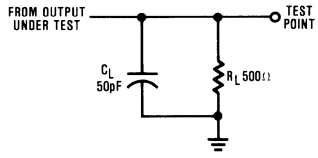


Function Table

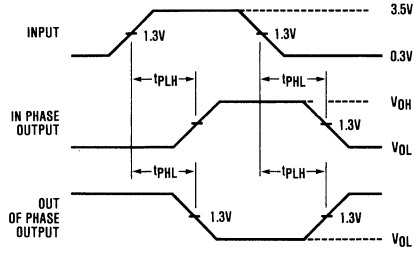
$\overline{PRE}$	D	EN	$\overline{OC}$	$\overline{Q}$
X	X	X	H	Z
L	X	X	L	L
H	H	H	L	L
H	L	H	L	H
H	X	L	L	$\overline{Q}_0$

L = Low State, H = High State, X = Don't Care
Z = High Impedance State
$\overline{Q}_0$ = Previous Condition of $\overline{Q}$

Test Waveforms



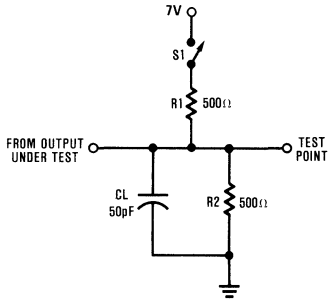
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



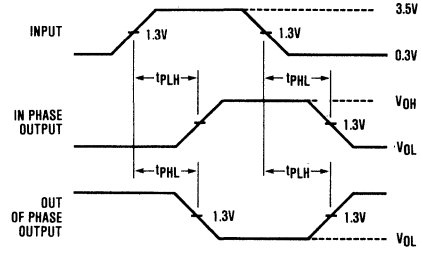
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

2

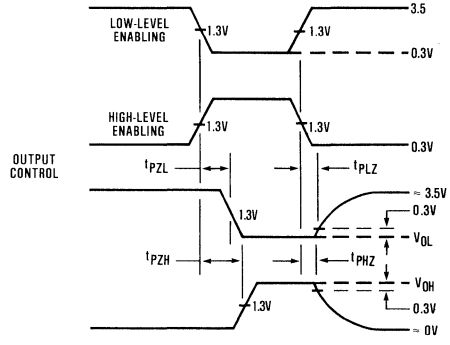
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.



LOAD CIRCUIT FOR TRI-STATE OUTPUTS



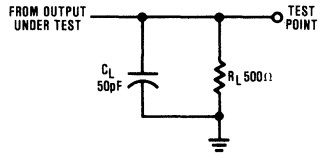
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



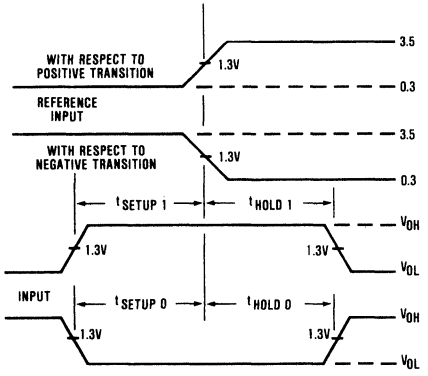
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS

Parameter	S1 Switch Position
T_{PLH}	OPEN
T_{PHL}	OPEN
T_{PHZ}	OPEN
T_{PZH}	OPEN
T_{PLZ}	CLOSED
T_{PZL}	CLOSED

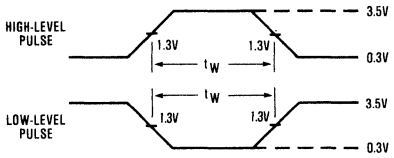
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.



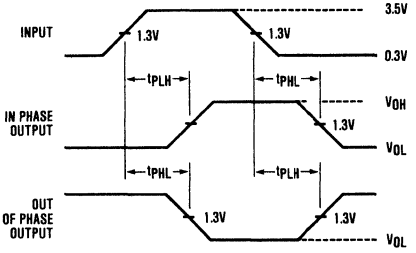
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES

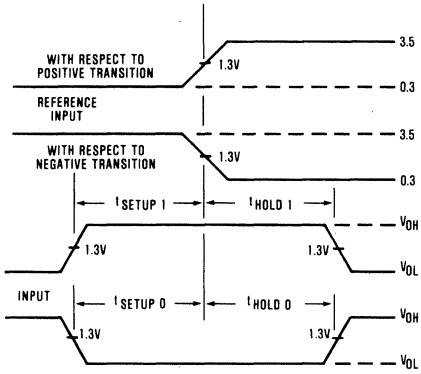


VOLTAGE WAVEFORMS PULSE WIDTHS

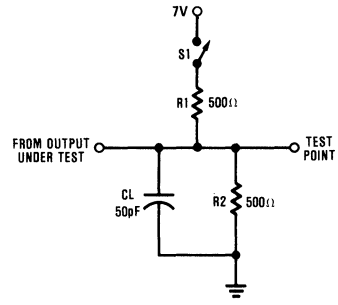


VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

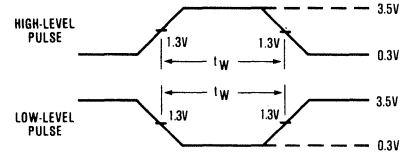
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, Z_{OUT} = 50 Ω, $t_r = t_f$ = 2ns.



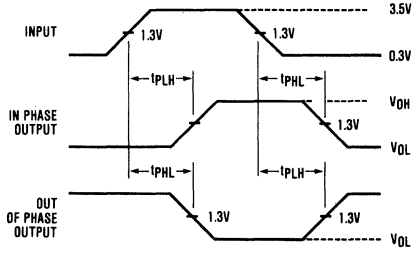
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



LOAD CIRCUIT FOR TRI-STATE OUTPUTS

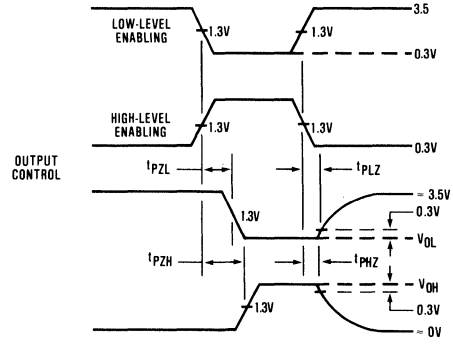


VOLTAGE WAVEFORMS PULSE WIDTHS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

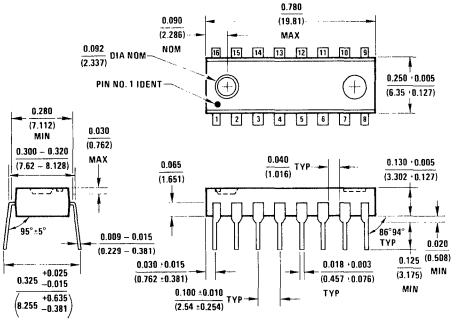
Parameter	S1 Switch Position
T_{PLH}	OPEN
T_{PHL}	OPEN
T_{PHZ}	OPEN
T_{PZH}	OPEN
T_{PLZ}	CLOSED
T_{PZL}	CLOSED



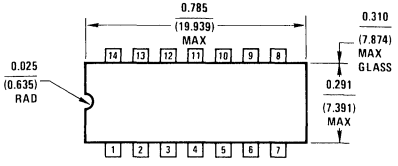
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, TRI-STATE OUTPUTS

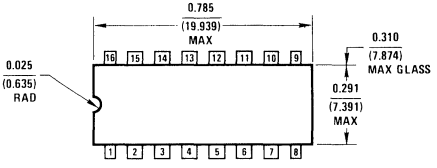
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1MHz, $Z_{OUT} = 50\ \Omega$, $t_r = t_f = 2$ns.

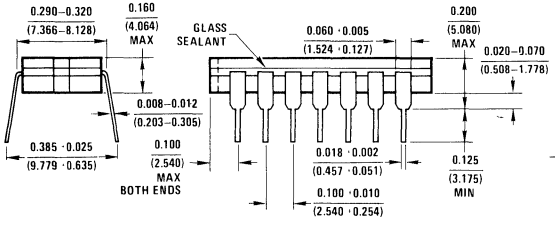
Appendices/Physical Dimensions



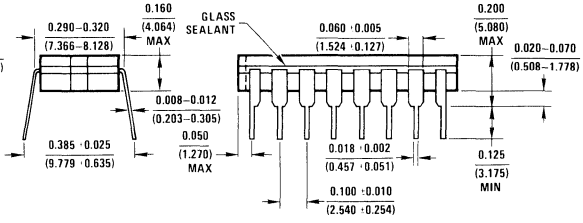
NS Package N16E
16-Lead Molded DIP (N)





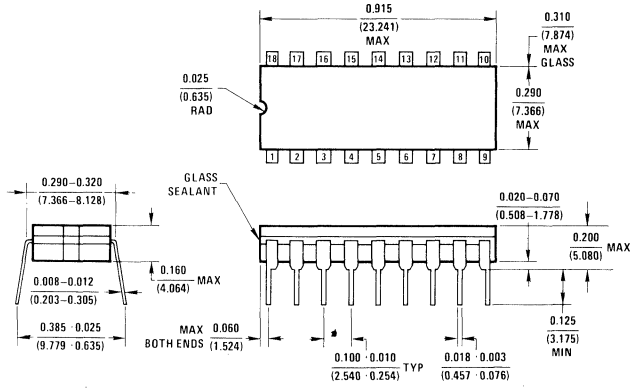


NS Package J14A
14-Lead Cavity DIP (J)

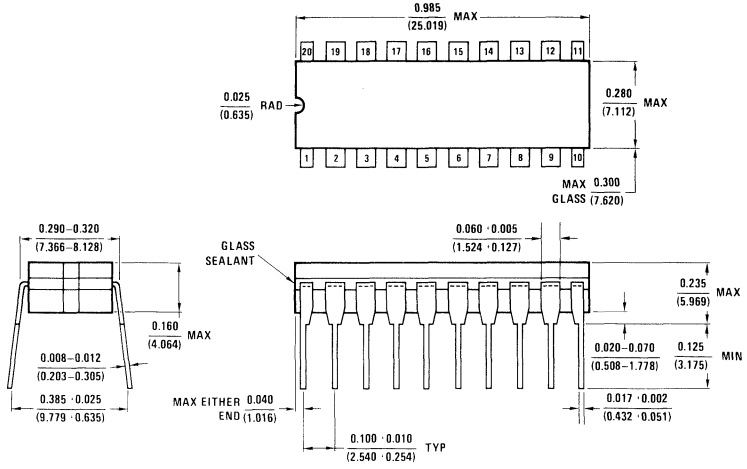


NS Package J16A
16-Lead Cavity DIP (J)

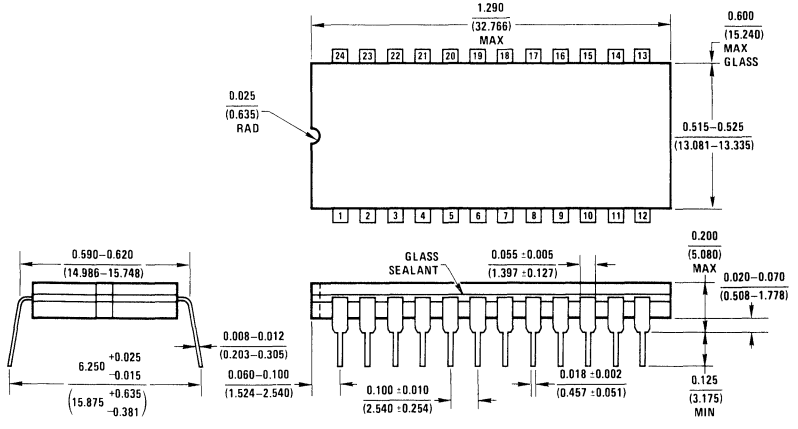
3



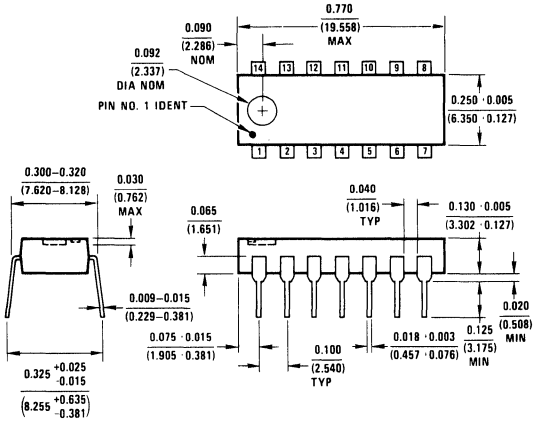
NS Package J18A
18-Lead Cavity DIP (J)



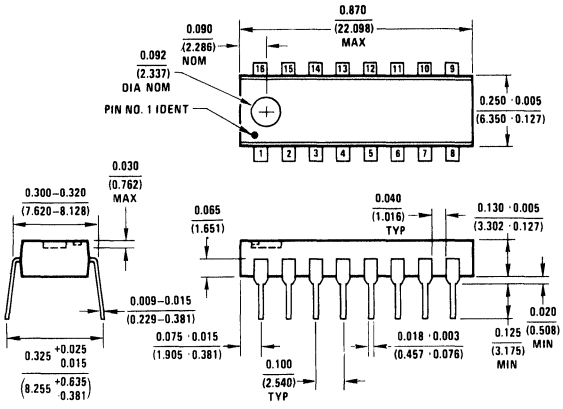
NS Package J20B
20-Lead Cavity DIP (J)



NS Package J24A
24-Lead Cavity DIP (J)



NS Package N14A
14-Lead Molded DIP (N)



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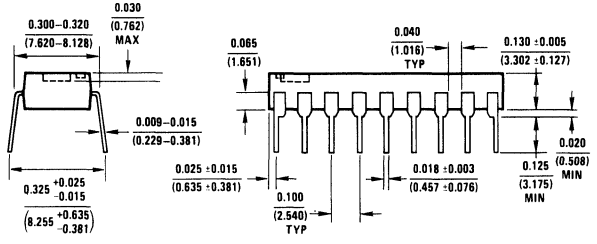
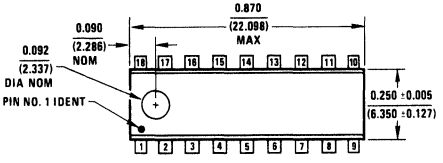
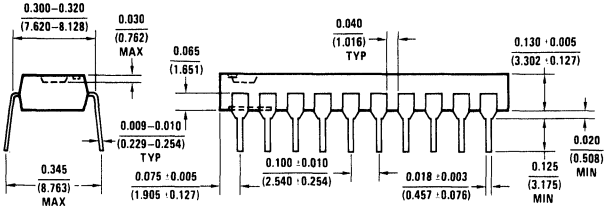
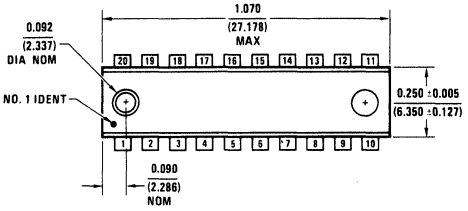
16-Lead Molded DIP (N)



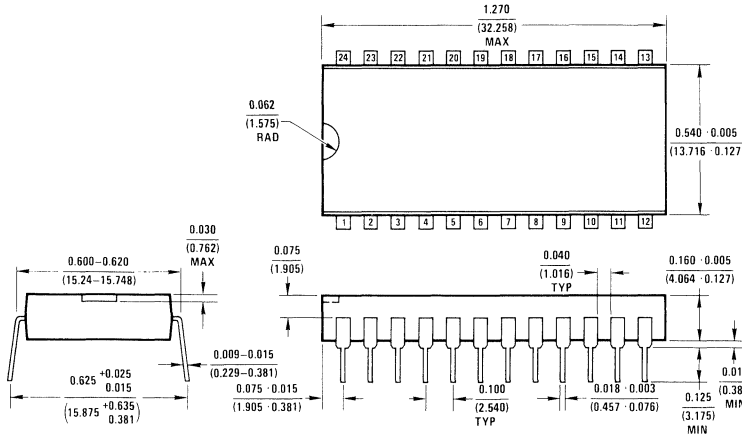


NS Package N18A
18-Lead Molded DIP (N)

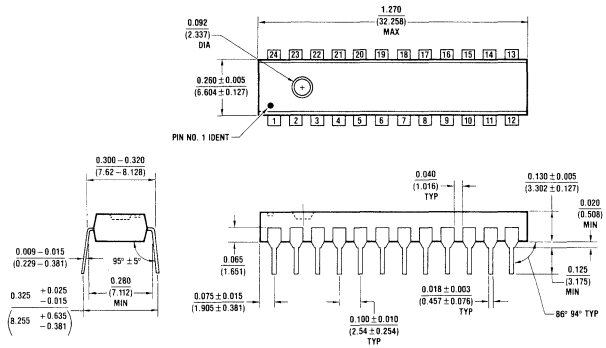




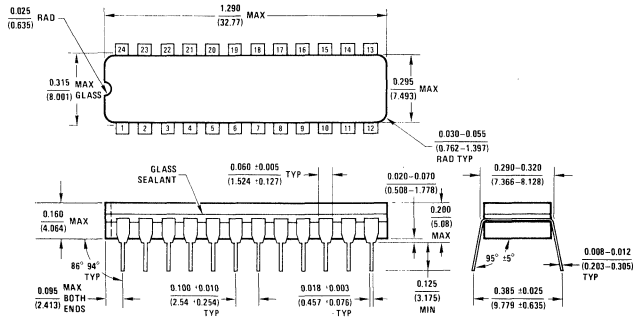
NS Package N20A
20-Lead Molded DIP (N)



NS Package N24A
24-Lead Molded DIP (N)



NS Package N24C
24-Lead Molded DIP (N)



NS Package J24F
24-Lead CERDIP (J)

Notes

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