1984

LOGIC DATABOOK

VOLUME I

National Semiconductor

LOGIC
DATABOOK
VOLUME I

NATIONAL SEMICONDUCTOR CORPORATION

- *MM54HC/74HC/54HCT/74HCT High Speed microCMOS Family*
- *CD4000 Family*
- *MM54C/74C Family*
- *CMOS LSI/VLSI*

LOGIC
DATABOOK
VOLUME I

TRADEMARKS

Following is the most current list of National Semiconductor Corporation's trademarks and registered trademarks.

Abuseable™
Anadig™
ANS-R-TRAN™
Auto-Chem Deflasher™
BI-FET™
BI-FET II™
BI-LINE™
BIPLAN™
BLC™
BLX™
Brite-Lite™
CIM™
CIMBUS™
Clock✓Chek™
COMBO™
COPS™ microcontrollers
DATACHECKER®
DENSPAK™
DIB™
Digitalker®
DISCERN™
DNR™
DPVM™
ELSTAR™
E-Z-LINK™
GENIX™
HEX 3000™
INFOCHEX™
Integral ISE™
Intelisplay™
ISE™
ISE/06™
ISE/08™
ISE/16™
ISE/32™
Macrobus™
Macrocomponent™
Meat✓Chek™
Microbus™ data bus (adjective)
MICRO-DAC™
μtalker™
Microtalker™
MICROWIRE™
MICROWIRE/PLUS™
MOLE™
MST™
National®
NAX800™
Nitride Plus™
Nitride Plus Oxide™
NML™
NOBUS™
NSC800™
NSX-16™
NS-XC-16™
NTERCOM™
NURAM™
OXISS™
Perfect Watch™
Pharma✓Chek™
PLAN™
Polycraft™
POSitalker™
QUAD3000™
RAT™
RTX-16™
Script✓Chek™
Shelf-Chek™
SERIES/800™
SERIES 32000™
SPIRE™
STAR™
Starlink™
STARPLEX™
STARPLEX II™
SuperChip™
SYS32™
TAPE-PAK™
TDE™
Telegate™
The National Anthem®
Time✓Chek™
TLC™
Trapezoidal™
TRI-CODE™
TRI-POLY™
TRI-SAFE™
TRI-STATE®
XMOS™
XPU™
Z STAR™
883B/RETS™
883S/RETS™

PAL® and PALASM™ are trademarks of and are used under license from Monolithic Memories, Inc.
DEC™, VAX™ and Unibus™ are trademarks of Digital Equipment Corp.
Intellec®, MULTIBUS® and MULTIMODULE™ are trademarks of Intel Corp.
Z80® is a trademark of Zilog Corp.
UNIX™ is a trademark of AT&T Bell Laboratories.

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation 2900 Semiconductor Drive Santa Clara, California 95051 Tel: (408) 721-5000 TWX: (910) 339-9240

Introduction

This comprehensive databook provides information on National Semiconductor's advanced CMOS logic families MM54HC/74HC high speed, CD4000, MM54C/74C and the many unique CMOS LSI products. The MM54HC/74HC family utilizes microCMOS technology to achieve the input and power supply characteristics of CMOS with the high speed and large output drive of low power Schottky. The MM54HC/74HC family has the same pinout as equivalent 54LS/74LS; in addition, many popular CD4000 series logic functions are offered where no equivalent TTL function exists.

The MM54HCT/74HCT is a subfamily of MM54HC/74HC offering TTL inputs. These MM54HCT/74HCT devices offer convenient TTL level translation to CMOS for those places in the system where only TTL levels are provided.

The CD4000 series is National Semiconductor's extensive line of CD40XXB and CD45XXB series devices. These parts meet the standard JEDEC "B-Series" specifications.

The popular MM54C/74C series logic family metal-gate CMOS technology is pin-for-pin and function-for-function equivalent to the 54/74 family of TTL devices. Unique special function LSI devices in this family are compatible with MM54HC/74HC and CD4000 series.

CMOS LSI offers the design engineer unique solutions to achieving high density low power systems. These LSI devices utilize both microCMOS silicon-gate and metal-gate technologies to offer the design engineer the best solution at the lowest cost.

National provides the highest Quality and Reliability in CMOS Logic and LSI. This databook provides detailed descriptions of Military/Aerospace Radiation Hardened Programs, Quality Enhancement and extensive Reliability Reports. We are proud of our success, which sets a standard for others to achieve. Our company-wide programs to achieve perfection will continue so that customers can continue to rely on National Semiconductor's integrated circuits and products.

Einleitung

Dieses ausführliche Datenbuch enthält alle Informationen über die modernen CMOS-Logikfamilien von National Semiconductor, nämlich über die Typenreihen MM54HC/74HC, CD4000, MM54C/74C, außerdem über viele andere CMOS-LSI-Produkte. Die Hochgeschwindigkeits-Logikfamilie MM54HC/74HC basiert auf der microCMOS-Technologie, die die Eigenschaften der CMOS-Technik in bezug auf die Stromaufnahme und das Eingangsverhalten mit der Geschwindigkeit sowie der Ausgangs-Treiberkapazität von Low-Power-Schottky-Bausteinen vereinigt. Die MM54HC/74HC-Typen besitzen die gleichen Anschlußbelegung wie die äquivalenten 54LS/74LS-Bausteine, außerdem werden viele Funktionen der CD4000-Familie angeboten, für die keine entsprechende TTL-Ausführung existiert.

Die Serie MM54HCT/74HCT ist ein Teil der MM54HC/74HC-Familie und besitzt TTL-kompatible Eingänge. Daher eignen sich diese Bausteine insbesondere für die Pegelanpassung zwischen CMOS- und TTL-ICs, z. B. wenn Schaltungsteile nur in TTL ausgeführt werden können. Die CD4000-Serie von National Semiconductor besteht aus den Bauelementen der CD40XXB- und CD45XXD-Familien. Diese Typen entsprechen den Spezifikationen der B-Serie nach JEDEC.

Die weit verbreitete Logikfamilie MM54C/74C in Metall-Gate-Technologie ist anschluß- und funktionskompatibel zu den Bausteinen der 54/74-TTL-Familie. Einige LSI-Bauelemente mit Spezial-funktionen in dieser Familie sind kompatibel mit Bausteinen der MM54HC/74HC- bzw. CD4000-Familien.

CMOS-LSI-Bausteine bieten dem Entwicklungsingenieur Lösungsmöglichkeiten in Form von Systemen mit hoher Schaltungsdichte bei geringer Stromaufnahme. Diese LSI-Schaltungen werden mit Hilfe der microCMOS-Silicon-Gate- oder Metall-Gate-Technologie hergestellt und ermöglichen optimale Schaltungsauslegung bei geringsten Kosten.

National Semiconductor kann bei CMOS-LSI- sowie Logikschaltungen Bauelemente höchster Qualität und Zuverlässigkeit anbieten. Dieses Datenbuch enthält detaillierte Beschreibungen der Programme für strahlenfeste Bauelemente für Militär sowie Luft und Raumfahrt, der Qualitätsverbesserung, außerdam Zuverlässigkeitsreports. Wir sind stolz auf unseren Erfolg, der Standards setzt, die für andere erstrebenswert sind. Unsere Firmenprogramme, die zum Ziel haben, Zuverlässigkeit und Qualität zu perfektionieren, werden kontinuierlich fortgeführt, so daß die Kunden sich auf die Produkte und integrierten Schaltungen von National Semiconductor auch zukünftig verlassen können.

Introduction

Ce databook très complet regroupe toutes les informations les plus récentes concernant les familles logiques CMOS de National Semiconductor, la MM54HC/74HC rapide, la CD4000, la MM54C/74C, ainsi que de nombreux produits originaux LSI CMOS. La famille MM54HC/74HC, réalisée en technologie microCMOS combine les caractéristiques d'entrée et d'alimentation de la CMOS avec la vitesse et la sortance de la low-power Schottky. La famille 54HC/74HC présente le même brochage que la famille équivalente 54LS/74LS; de plus, la très populaire famille CD4000 offre un choix de fonctions logiques sans équivalent en TTL.

La famille 54HCT/74HCT, sous-ensemble de la famille MM54HC/74HC, dispose d'entrées compatibles TTL. Ces circuits MM54HCT/74HCT éffectuent un translation de niveau TTL-CMOS lorsque des portes TTL attaquent des fonctions logiques CMOS dans le système.

La famille CD4000 de National Semiconductor est constituée par les séries de circuits CD40XXB et CD45XXB. Ces circuits sont conformes aux spécifications standard JEDEC 'Série B'.

La famille logique Série MM54C/74C réalisée en technologie CMOS porte-métallique est équivalente broche pour broche et fonction pour fonction à la famille de circuits TTL 54/74. Les circuits LSI de cette famille, réalisant des fonctions spéciales uniques, sont compatibles avec les Séries MM54HC/74HC et CD4000.

Les circuits LSI CMOS offrent aux ingénieurs de conception des solutions avantageuses leur permettant de réaliser des systèmes à haute densité et consommant peu. Ces circuits LSI sont réalisés en technologies microCMOS porte-silicium et en CMOS porte-métallique, afin que l'ingénieur de conception dispose de la meilleure solution au moindre coût.

National procure la meilleure qualité et la meilleure fiabilité en logique CMOS et en LSI. Ce Databook fournit une description détaillée des Programmes d'exposition aux radiations dans les domaines militaire et spatial, ainsi que des rapports d'amélioration de la qualité et de la fiabilité. Nous sommes fiers de notre succès, qui introduit un standard que nous envient nos concurrents. Ces programmes de qualité sont exécutés à l'échelle de la société toute entière en vue d'atteindre la perfection: ils seront poursuivis afin que nos clients puissent continuer à faire confiance aux circuits intégrés et aux produits National Semiconductor.

Introduzione

Il Databook sui dispositivi logici CMOS della National Semiconductor contiene informazioni, dettagliate ed aggiornate, sulla famiglia ad alta velocità MM54HC/74HC, sulla famiglia CD4000, MM54C/74C e su molti prodotti LSI CMOS. La famiglia MM54HC/74HC, in particolare utilizza una tecnologia microCMOS per assommare alle caratteristiche di assorbimento e di Ingresso/Uscita tipiche del CMOS quelle di elevata velocità e capacità di pilotaggio della tecnologia bipolare "Low Power Schottky". I dispositivi della famiglia MM54HC/74HC sono pin compatibili con gli equivalenti dispositivi TTL; nella stessa ne sono compresi altri che riprendono, funzionalmente, i più diffusi dispositivi CD4000 ove non esista un equivalente TTL.

La MM54HCT/74HCT rappresenta una sottofamiglia della HC, ed offre compatibilità TTL sugli ingressi. La HCT trova ideale impiego nei sistemi ove esistano solamente livelli TTL e si debbano impiegare dispositivi CMOS, come traslatori di livello. La famiglia CD4000 della National comprende la maggior parte delle funzioni più diffuse sia CD40XX che CD45XX. Tutti i dispositivi soddisfano le specifiche JEDEC per la serie "B".

La nota famiglia MM54C/74C, realizzata in tecnologia CMOS "metal gate" è equivalente "pin-to-pin" e funzionalmente alla famiglia di dispositivi TTL 54/74. Speciali dispositivi LSI, compresi in questa famiglia sono compatibili con le serie MM54HC/74HC e CD4000. I dispositivi LSI CMOS offrono ai progettisti soluzioni uniche per sistemi ove sia richiesta alta integrazione e basso assorbimento. Questi LSI sono realizzati sia in tecnologia microCMOS che "metal gate" per offrire sempre la miglior soluzione ai costi più ridotti.

La National offre la massima qualità ed affidabilità per i suoi prodotti logici CMOS e dispositivi LSI. Questo Databook fornisce una descrizione dettagliata dei programmi "Radiation Hardened" per dispositivi militari ed aerospaziali, i miglioramenti della qualità oltre a completi rapporti sull'affidabilità dei componenti. Siamo fieri del nostro successo che fissa nuovi traguardi, per altri, da raggiungere. Il nostro programma, che coinvolge tutta la società per il raggiungimento della perfezione elettrica è in pieno svolgimento; con ciò i nostri clienti possono continuare a riporre la massima fiducia nei prodotti della National Semiconductor.

Table of Contents

Section 1—CMOS AC Switching Test Circuits and Timing Waveforms

Section 2—CMOS Application Notes

MM54HC/MM74HC Application Notes

CD4000, MM54C/MM74C Application Notes

LSI/VLSI Application Notes

Table of Contents (Continued)

LSI/VLSI Application Notes (Continued)

Section 3—MM54HC/MM74HC Data Sheets

Analog Switches

Arithmetic Functions

Buffers/Drivers

Counters

Table of Contents (Continued)

Table of Contents (Continued)

Table of Contents (Continued)

Section 4—MM54HCT/MM74HCT Data Sheets

Table of Contents (Continued)

Section 5—CD4XXX Series CMOS Logic

Table of Contents (Continued)

Table of Contents (Continued)

Table of Contents (Continued)

Section 6—MM54CXXX/MM74CXXX Series

Table of Contents (Continued)

Table of Contents (Continued)

Section 7—LSI/VLSI CMOS

Table of Contents (Continued)

Section 8—Appendices/Physical Dimensions

Alphanumeric Index

Alphanumeric Index (Continued)

Alphanumeric Index (Continued)

Alphanumeric Index (Continued)

Alphanumeric Index (Continued)

Alphanumeric Index (Continued)

Alphanumeric Index (Continued)

Alphanumeric Index (Continued)

Alphanumeric Index (Continued)

Section 1

CMOS AC Switching Test Circuits and Timing Waveforms

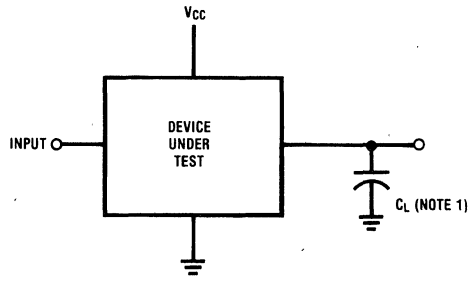
1

Section Contents

AC Parameter Definitions

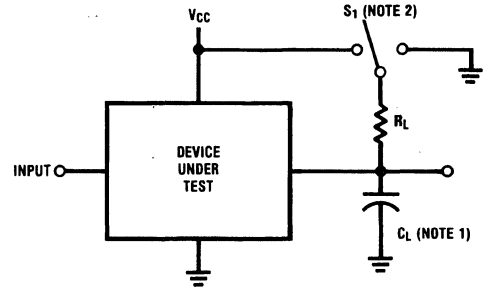
f_{MAX}	Operating frequency. This is the fastest speed that a circuit can be toggled.
t_{PHL}	Propagation delay from input to output; output going high to low.
t_{PLH}	Propagation delay from input to output; output going low to high.
t_{PZH}	Enable propagation delay time. This is measured from the input to the output going to an active high level from TRI-STATE®.
t_{PZL}	Enable propagation delay time. This is measured from the input to the output going to an active low level from TRI-STATE.
t_{PHZ}	Disable propagation delay time to the output going from an active high level to TRI-STATE.
t_{PLZ}	Disable propagation delay time to the output going from an active low level to TRI-STATE.
t_W	Input signal pulse width.
t_S	Input setup time. This is the time that data must be present prior to clocking input transitioning.
t_H	Input hold time. This is the time that data must remain after clocking input has transitioned.
t_{REM}	Clock removal time. This is the time that an active clear or enable signal must be removed before the clock input transitions. (Sometimes called recovery time)
t_r	Input signal rise time.
t_f	Input signal fall time.
t_{TLH}	Output rise time (transition time low to high)
t_{THL}	Output fall time (transition time high to low)

MM54HC/MM74HC AC Switching Test Circuits and Timing Waveforms



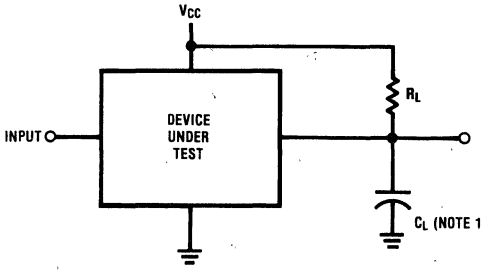
TL/F/5376–1

Test Circuit for Push Pull Outputs



TL/F/5376–2

Test Circuit for TRI-STATE and Open Drain Output Tests (Notes 2 and 3)



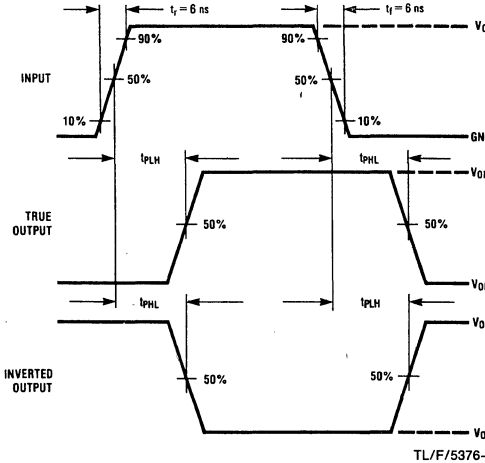
TL/F/5376–3

Test Circuit for Open Drain Outputs

Note 1: C_L includes load and test jig capacitance. See data sheets for values.

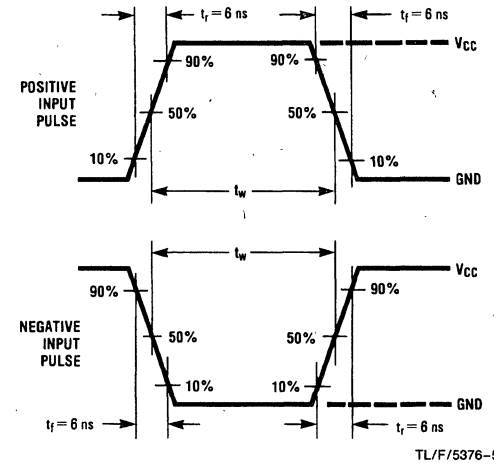
Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = Gnd for t_{PZH}, and t_{PHZ} measurements.

Note 3: For open drain devices S1 = V_{CC} and measurements are same as t_{PZL} and t_{PLZ}.



TL/F/5376–4

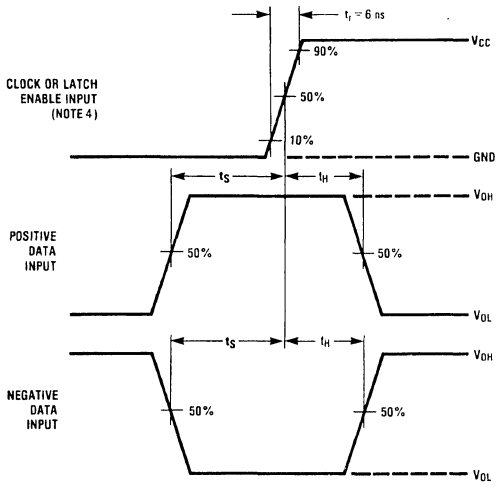
Propagation Delay Waveforms



TL/F/5376–5

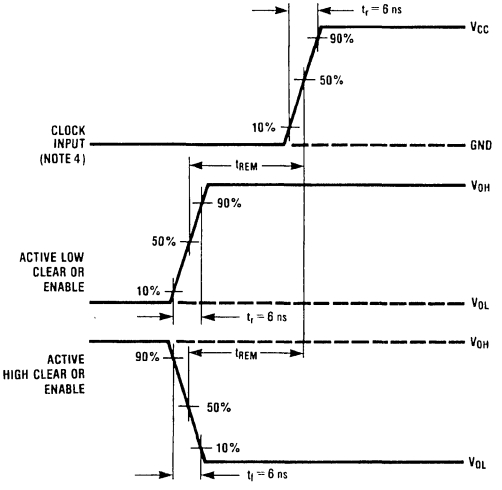
Input Pulse Width Waveforms

MM54HC/MM74HC AC Switching Test Circuits and Timing Waveforms (Continued)



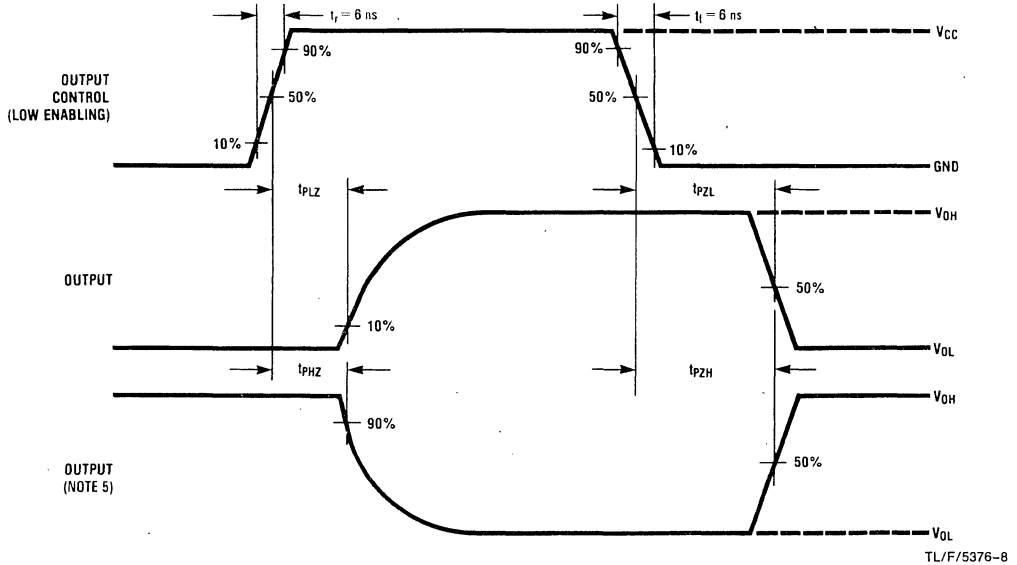
TL/F/5376–6

Setup and Hold Time Waveforms



TL/F/5376–7

Removal Time Waveforms



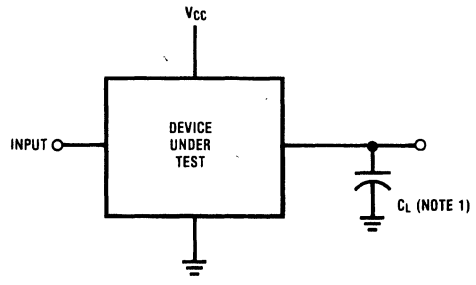
TL/F/5376–8

TRI-STATE Output Enable and Disable Waveforms

Note 4: Waveform for negative edge sensitive circuits will be inverted

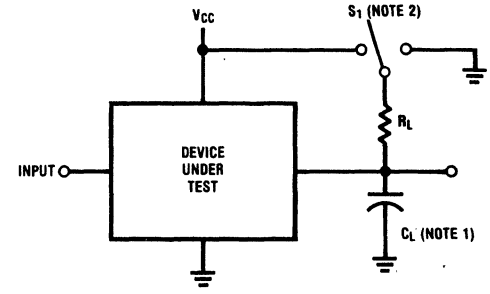
Note 5: This waveform is applicable to both TRI-STATE and open drain switching time measurements.

MM54HCT/MM74HCT AC Switching Test Circuits and Timing Waveforms



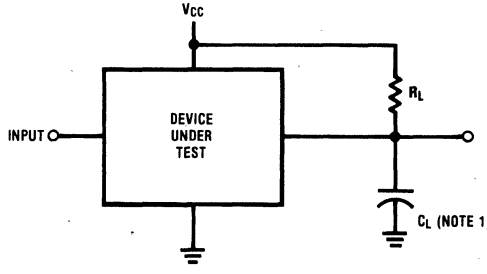
TL/F/5376-26

Test Circuit for Push Pull Outputs



TL/F/5376-27

Test Circuit for TRI-STATE and Open Drain Output Tests (Notes 2 and 3)



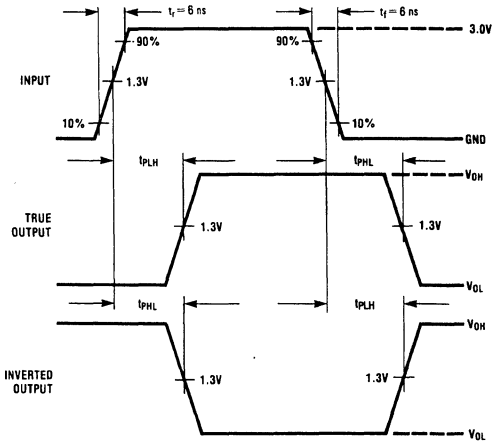
TL/F/5376-28

Test Circuit for Open Drain Outputs

Note 1: C_L includes load and test jig capacitance.

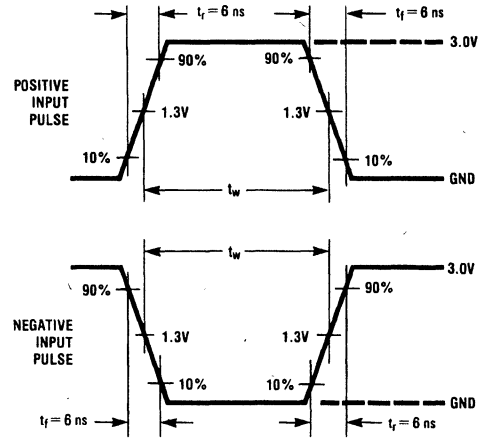
Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = Gnd for t_{PZH}, and t_{PHZ} measurements.

Note 3: For open drain circuits S1 = V_{CC} and measurements are the same as t_{PZL} and t_{PLZ}.



TL/F/5376-9

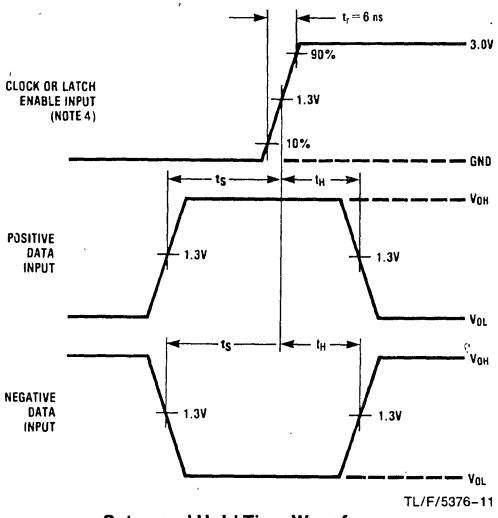
Propagation Delay Waveforms



TL/F/5376-10

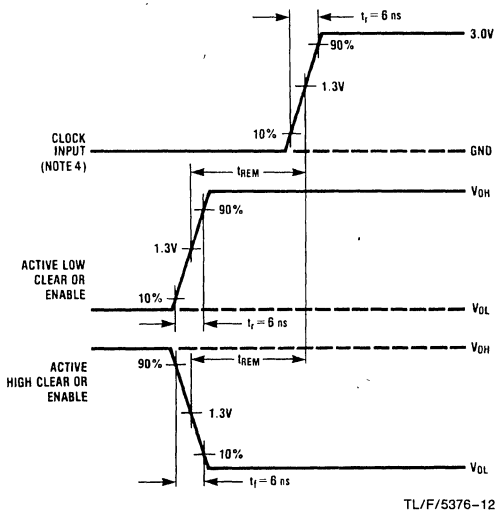
Input Pulse Width Waveforms

MM54HCT/MM74HCT AC Switching Test Circuits and Timing Waveforms (Continued)



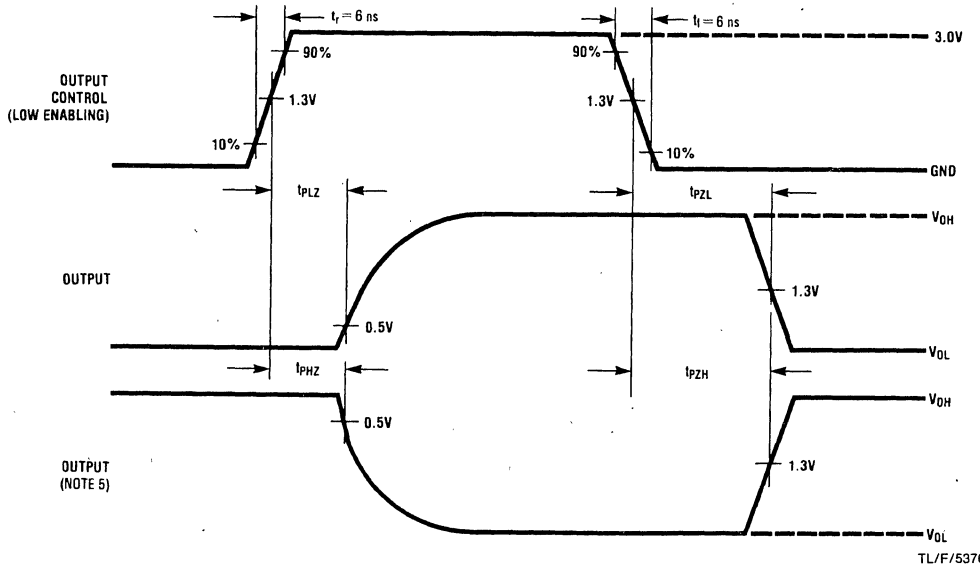
TL/F/5376–11

Setup and Hold Time Waveforms



TL/F/5376–12

Removal Time Waveforms



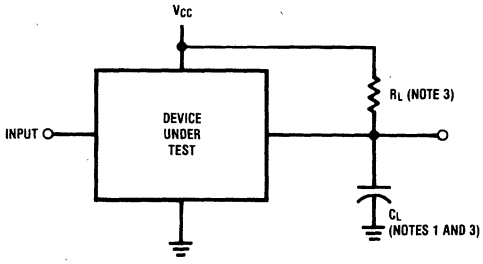
TL/F/5376–13

TRI-STATE Output Enable and Disable Waveforms

Note 4: Waveform for negative edge sensitive circuits will be inverted.

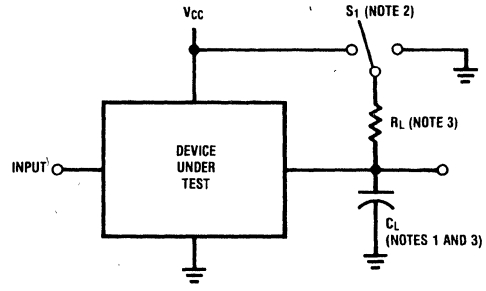
Note 5: This waveform is applicable to both TRI-STATE and open drain switching time measurements.

CD4000 AC Switching Test Circuits and Timing Waveforms



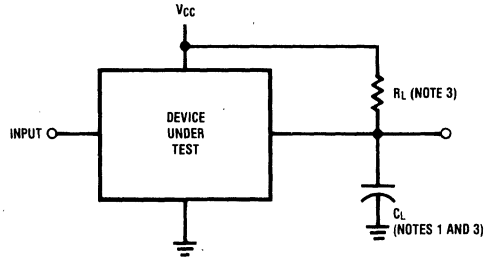
TL/F/5376–15

Test Circuit for Push Pull Outputs



TL/F/5376–16

Test Circuit for TRI-STATE Output Tests



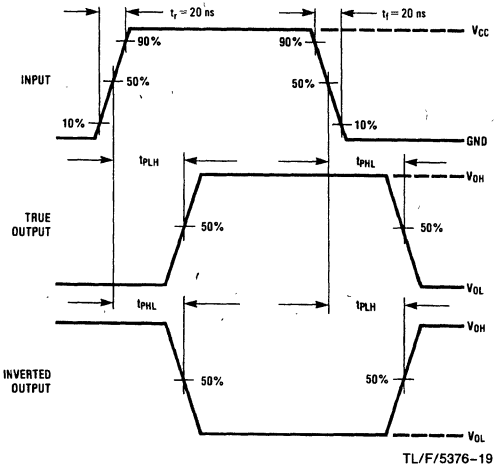
TL/F/5376–14

Test Circuit for Open Drain Outputs

Note 1: C_L includes load and test jig capacitance.

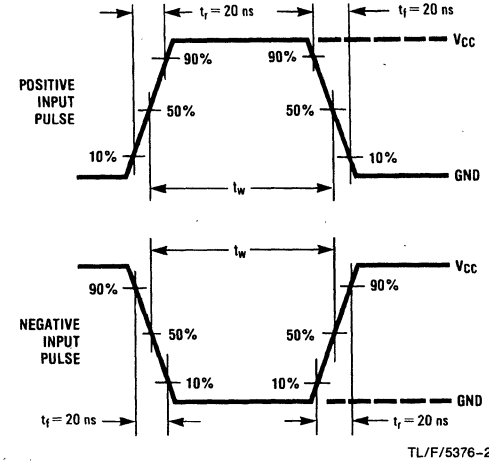
Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = Gnd for t_{PZH}, and t_{PHZ} measurements.

Note 3: See individual data sheet for component values.



TL/F/5376–19

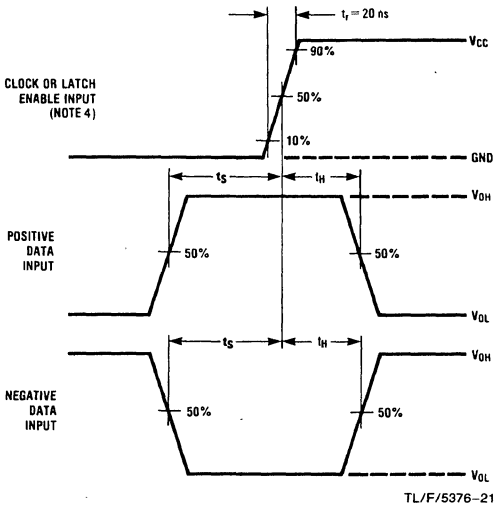
Propagation Delay Waveforms



TL/F/5376–20

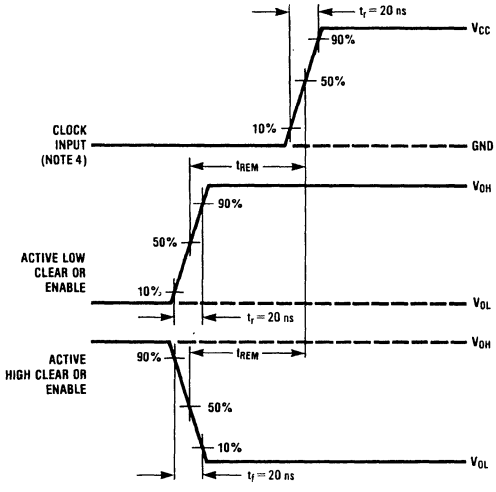
Input Pulse Width Waveforms

CD4000 AC Switching Test Circuits and Timing Waveforms (Continued)



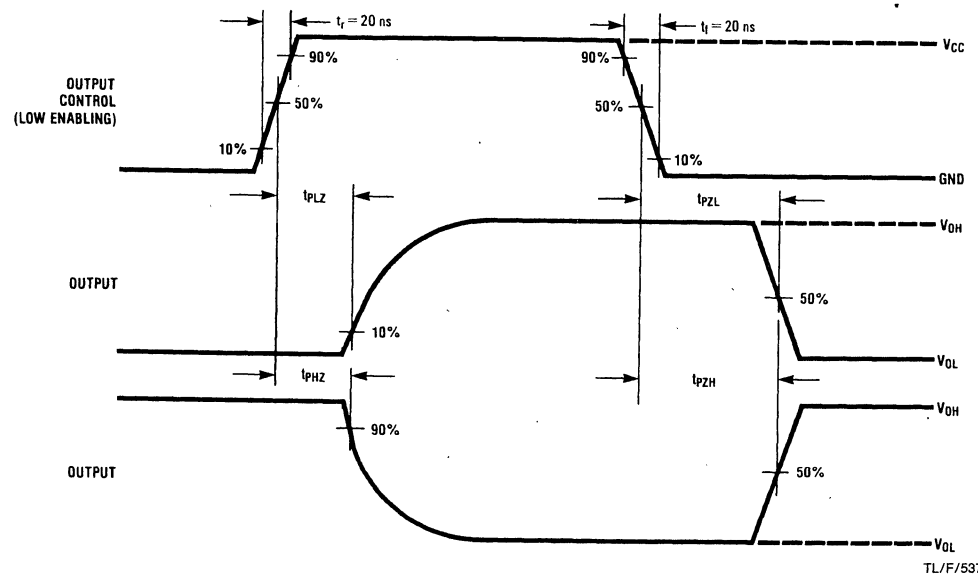
TL/F/5376–21

Setup and Hold Time Waveforms



TL/F/5376–22

Removal Time Waveforms

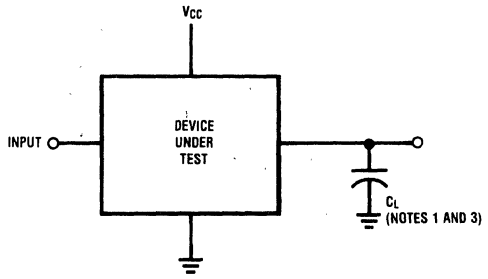


TL/F/5376–23

TRI-STATE Output Enable and Disable Waveforms

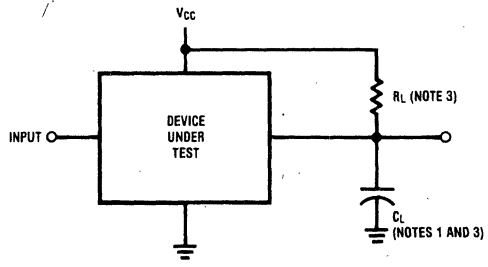
Note 4: Waveform for negative edge sensitive circuits will be inverted.

MM54C/MM74C AC Switching Test Circuits and Timing Waveforms



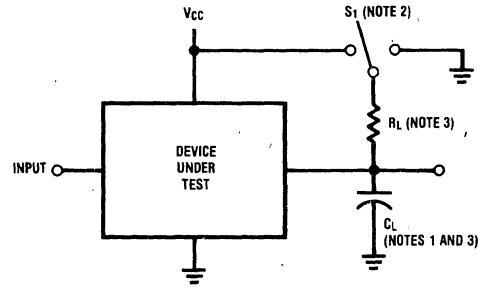
TL/F/5376–17

Test Circuit for Push Pull Outputs



TL/F/5376–29

Test Circuit for Open Drain Outputs



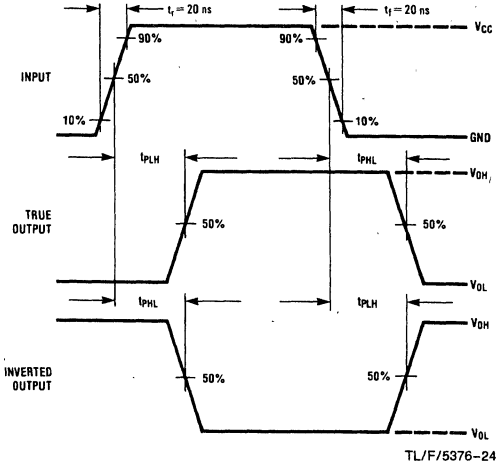
TL/F/5376–18

Test Circuit for TRI-STATE Output Tests

Note 1: C_L includes load and test jig capacitance.

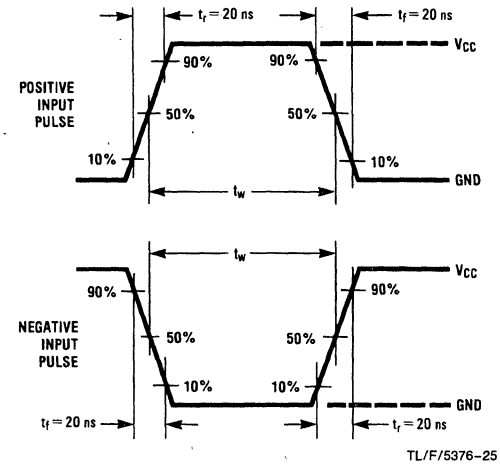
Note 2: S1 = V_{CC} for t_{PZL}, and t_{PLZ} measurements.
S1 = Gnd for t_{PZH}, and t_{PHZ} measurements.

Note 3: See individual data sheet for component values.



TL/F/5376–24

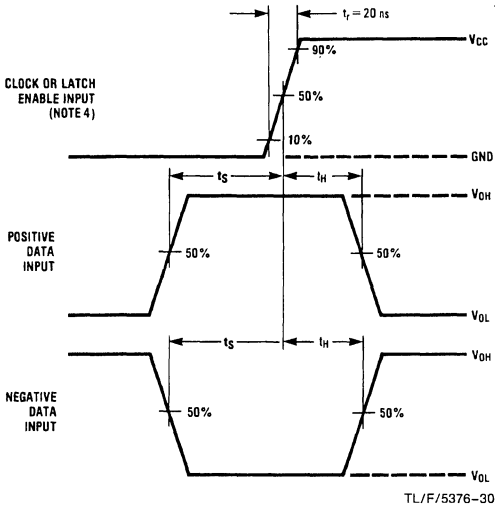
Propagation Delay Waveforms



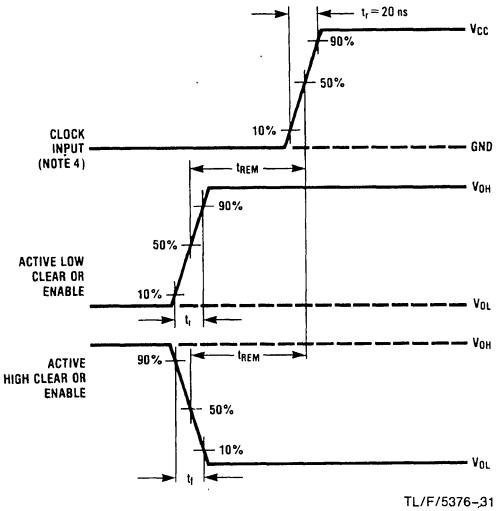
TL/F/5376–25

Input Pulse Width Waveforms

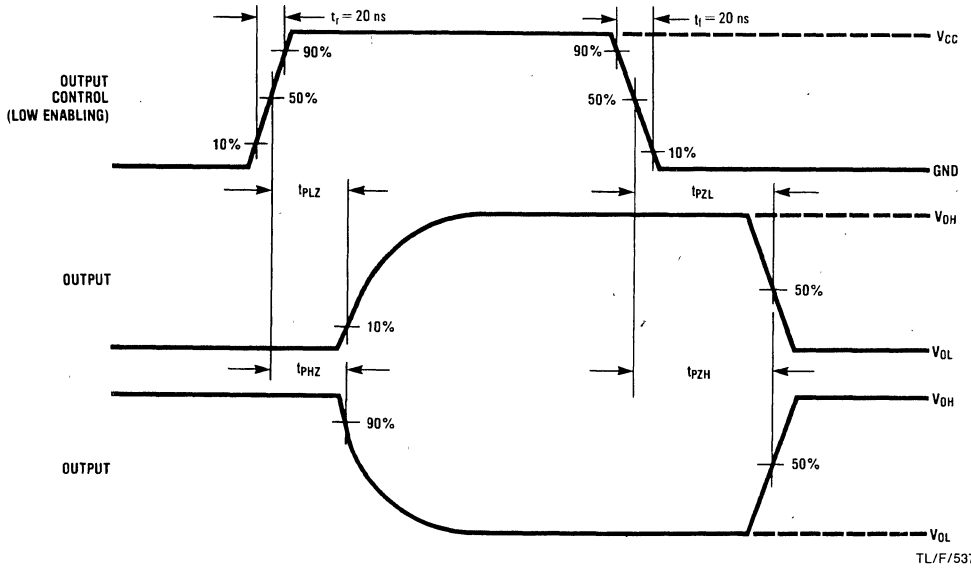
MM54C/MM74C AC Switching Test Circuits and Timing Waveforms (Continued)



Setup and Hold Time Waveforms



Removal Time Waveforms



TRI-STATE Output Enable and Disable Waveforms

Note 4: Waveform for negative edge sensitive circuits will be inverted.

Section 2
CMOS Application Notes

2

Section Contents

CMOS, the Ideal Logic Family

National Semiconductor
Application Note 77
Stephen Calebotta
January 1983

INTRODUCTION

Let's talk about the characteristics of an ideal logic family. It should dissipate no power, have zero propagation delay, controlled rise and fall times, and have noise immunity equal to 50% of the logic swing.

The properties of CMOS (complementary MOS) begin to approach these ideal characteristics.

First, CMOS dissipates low power. Typically, the static power dissipation is 10 nW per gate which is due to the flow of leakage currents. The active power depends on power supply voltage, frequency, output load and input rise time, but typically, gate dissipation at 1MHz with a 50 pF load is less than 10mW.

Second, the propagation delays through CMOS are short, though not quite zero. Depending on power supply voltage, the delay through a typical gate is on the order of 25 to 50 ns.

Third, rise and fall times are controlled, tending to be ramps rather than step functions. Typically, rise and fall times tend to be 20 to 40% longer than the propagation delays.

Last, but not least, the noise immunity approaches 50%, being typically 45% of the full logic swing.

Besides the fact that it approaches the characteristics of an ideal logic family and besides the obvious low power battery applications, why should designers choose CMOS for new systems? The answer is cost.

On a component basis, CMOS is still more expensive than TTL. However, system level cost may be lower. The power supplies in a CMOS system will be cheaper since they can be made smaller and with less regulation. Because of lower currents, the power supply distribution system can be simpler and therefore, cheaper. Fans and other cooling equipment are not needed due to the lower dissipation. Because of longer rise and fall times, the transmission of digital signals becomes simpler making transmission techniques less expensive. Finally, there is no technical reason why CMOS prices cannot approach present day TTL prices as sales volume and manufacturing experience increase. So, an engineer about to start a new design should compare the system level cost of using CMOS or some other logic family. He may find that, even at today's prices, CMOS is the most economical choice.

National is building two lines of CMOS. The first is a number of parts of the CD4000A series. The second is the 54C/74C series which National introduced and which will become the industry standard in the near future.

The 54C/74C line consists of CMOS parts which are pin and functional equivalents of many of the most popular parts in the 7400 TTL series. This line is typically 50% faster than the 4000A series and sinks 50% more current. For ease of design, it is spec'd at TTL levels as well as CMOS levels, and there are two temperature ranges available: 54C, −55°C to +125°C or 74C, −40°C to +85°C. Table I compares the port parameters of the 54C/74C CMOS line to those of the 54L/74L low power TTL line.

TABLE I. Comparison of 54L/74L Low Power TTL and 54C/74C CMOS Port Parameters

FAMILY	V_{CC}	V_{IL} MAX	I_{IL} MAX	V_{IH} MIN	I_{IH} 2.4V	V_{OL} MAX	I_{OL}	V_{OH} MIN	I_{OH}	t_{pd0} TYP	t_{pd1} TYP	P_{DISS}/GATE STATIC	P_{DISS}/GATE 1 MHz, 50 pF LOAD
54L/74L	5	0.7	0.18 mA	2.0	10 μA	0.3	2.0 mA	2.4	100μA	31	35	1 mW	2.25 mW
54C/74C	5	0.8	–	3.5	–	0.4	*360μA	2.4	*100μA	60	45	0.00001 mW	1.25 mW
54C/74C	10	2.0	–	8.0	–	1.0	**10μA	9.0	**10μA	25	30	0.00003 mW	5 mW

*Assumes interfacing to low power TTL.

**Assumes interfacing to CMOS.

CHARACTERISTICS OF CMOS

The aim of this section is to give the system designer not familiar with CMOS, a good feel for how it works and how it behaves in a system. Much has been written about MOS devices in general. Therefore, we will not discuss the design and fabrication of CMOS transistors and circuits.

The basic CMOS circuit is the inverter shown in Figure 2-1. It consists of two MOS enhancement mode transistors, the upper a P-channel type, the lower an N-channel type.

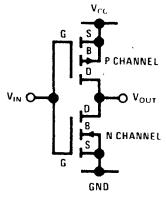


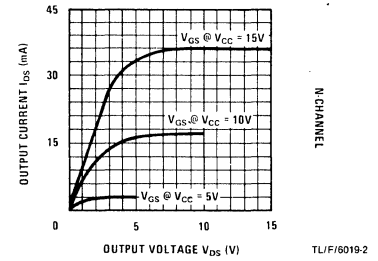
FIGURE 2-1. Basic CMOS Inverter.

The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and Ground depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomeclature has been retained with the introduction of the 54C/74C line of CMOS. V_{CC} and Ground is the nomenclature we shall use throughout this paper.

The logic levels in a CMOS system are V_{CC} (logic "1") and Ground (logic "0"). Since "on" MOS transistor has virtually no voltage drop across it if there is no current flowing through it, and since the input impedance to CMOS device is so high (the input characteristic of an MOS transistor is essentially capacitive, looking like a $10^{12}\Omega$ resistor shunted by a 5 pF capacitor), the logic levels seen in a CMOS system will be essentially equal to the power supplies.

Now let's look at the characteristic curves of MOS transistors to get an idea of how rise and fall times, propagation delays and power dissipation will vary with power supply voltage and capacitive loading. Figure 2-2 shows the characteristic curves of N-channel and P-channel enhancement mode transistors.

There are a number of important observations to be made from these curves. Refer to the curve of V_{GS} = 15V (Gate to Source Voltage) for the N-channel transistor. Note that for a constant drive voltage V_{GS}, the transistor behaves like a current source for V_{DS}'s (Drain to Source Voltage) greater than $V_{GS} - V_T$ (V_T is the threshold voltage of an MOS transistor). For V_{DS}'s below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Note also that for lower V_{GS}'s, there are similar curves except that the magnitude of the I_{DS}'s are significantly smaller and that in fact, I_{DS} increases approximately as the square of increasing V_{GS}. The P-channel transistor exhibits essentially identical, but complemented, characteristics.



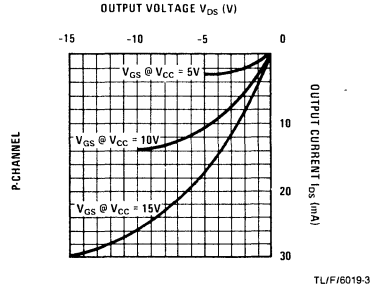


FIGURE 2-2. Logical "1" Output Voltage vs Source Current.

If we try to drive a capacitive load with these devices, we can see that the initial voltage change across the load will be ramp-like due to the current source characteristic followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. Referring this to our basic CMOS inverter in Figure 2-1, as V_{DS} approaches zero, V_{OUT} will approach V_{CC} or Ground depending on whether the P-channel or N-channel transistor is conducting.

Now if we increase V_{CC} and, therefore, V_{GS} the inverter must drive the capacitor through a larger voltage swing. However, for this same voltage increase, the drive capability (I_{DS}) has increased roughly as the square of V_{GS} and, therefore, the rise times and the propagation delays through the inverter as measured in Figure 2-3 have decreased.

So, we can see that for a given design, and therefore fixed capacitive load, increasing the power supply voltage will increase the speed of the system.

Increasing V_{CC} increases speed but it also increases power dissipation. This is true for two reasons. First, CV^2f power increases. This is the power dissipated in a CMOS circuit, or any other circuit for that matter, when driving a capacitive load.

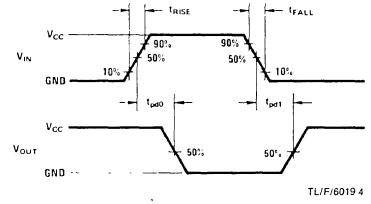


FIGURE 2-3. Rise and Fall Times and Propagation Delays as Measured in a CMOS System.

For a given capacitive load and switching frequency, power dissipation increases as the square of the voltage change across the load.

The second reason is that the VI power dissipated in the CMOS circuit increases with V_{CC} (for V_{CC}'s $> 2V_T$). Each time the circuit switches, a current momentarily flows from V_{CC} to Ground through both output transistors. Since the threshold voltages of the transistors do not change with increasing V_{CC}, the input voltage range through which the upper and lower transistors are conducting simultaneously increases as V_{CC} increases. At the same time, the higher V_{CC} provides higher V_{GS} voltages which also increase the magnitude of the I_{DS} currents. Incidently, if the rise time of the input signal was zero, there would be no current flow from V_{CC} to Ground through the circuit. This current flows because the input signal has a finite rise time and, therefore, the input voltage spends a finite amount of time passing through the region where both transistors conduct simultaneously. Obviously, input rise and fall times should be kept to a minimum to minimize VI power dissipation.

Let's look at the transfer characteristics, Figure 2-4, as they vary with V_{CC}. For the purposes of this discussion we will assume that both transistors in our basic inverter have identical but complementary characteristics and threshold voltages. Assume the threshold voltages, V_T, to be 2V. If V_{CC} is less than the threshold voltage of 2V, neither transistor can ever be turned on and the circuit cannot operate. If V_{CC} is equal to the threshold voltage exactly then we are on the curve Figure 2-4a. We appear to have 100% hysteresis. However, it is not truly hysteresis since both output transistors are off and the output voltage is being held on the gate capacitances of succeeding circuits. If V_{CC} is somewhere between one and two threshold voltages (Figure 2-4b), then we have diminishing amounts of "hysteresis" as we approach V_{CC} equal to $2V_T$ (Figure 2-4c). At V_{CC} equal to two thresholds we have no "hysteresis" and no current flow through both the upper and lower transistors during switching. As V_{CC} exceeds two thresholds the transfer curves begin to round off (Figure 2-4d). As V_{IN} passes through the region where both transistors are conducting, the currents flowing through the transistors cause voltage drops across them giving the rounded characteristic.

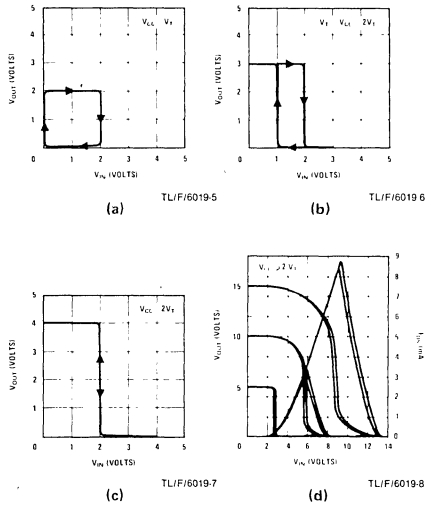


FIGURE 2-4. Transfer Characteristics vs V_{CC}.

Considering the subject of noise in a CMOS system, we must discuss at least two specs: noise immunity and noise margin.

National's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 0.45 V_{CC} or less away from V_{CC} or Ground typically will not propagate through the system as an erroneous logic level. This does not mean that no signal at all will appear at the output of the first circuit. In fact, there will be an output signal as a result of the spurious input, but it will be reduced in amplitude. As this signal propagates through the system, it will be attenuated even more by each circuit it passes through until it finally disappears. Typically, it will not change any signal to the opposite logic level. In a typical flip flop, a 0.45 V_{CC} spurious pulse on the clock line would not cause the flop to change state.

National also guarantees that its CMOS circuits have a 1V DC noise margin over the full power supply range and temperature range and with any combination of inputs. This is simply a variation of the noise immunity spec only now a specific set of input and output voltages have been selected and guaranteed. Stated verbally, the spec says that for the output of a circuit to be within 0.1 V_{CC} volts of a proper logic level (V_{CC} or Ground), the input

can be as much as 0.1 V_{CC} plus 1V away from power supply rail. Shown graphically we have:

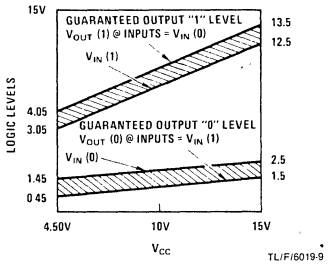


FIGURE 2-5. Guaranteed CMOS DC Margin Over Temperature as a Function of V_{CC}. CMOS Guarantees 1V.

This is similar in nature to the standard TTL noise margin spec which is 0.4V.

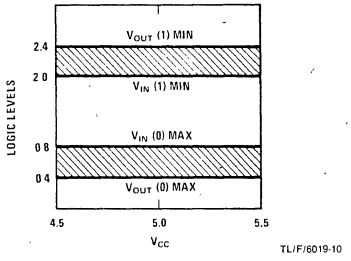


FIGURE 2-6. Guaranteed TTL DC Margin Over Temperature as a Function of V_{CC}. TTL Guarantees 0.4V.

For a complete picture of V_{OUT} vs V_{IN} refer to the transfer characteristic curves in Figure 2-4.

SYSTEM CONSIDERATIONS

This section describes how to handle many of the situations that arise in normal system design such as unused inputs, paralleling circuits for extra drive, data bussing, power considerations and interfaces to other logic families.

Unused inputs: simply stated, unused inputs should not be left open. Because of the very high impedance ($\sim 10^{12}\Omega$), a floating input may drift back and forth between a "0" and "1" creating some very intriguing system problems. All unused inputs should be tied to V_{CC}, Ground or another used input. The choice is not completely arbitrary, however, since there will be an effect on the output drive capability of the circuit in question. Take, for example, a four input NAND gate being used as a two input gate. The internal structure is shown in Figure 3-1. Let inputs A & B be the unused inputs.

If we were going to tie the unused inputs to a logic level, inputs A & B would have to be tied to V_{CC} to enable the other inputs to function. That would turn on the lower A and B transistors and turn off the upper A and B transistors. At most, only two of the upper transistors could ever be turned on. However, if inputs A and B were tied to input C, the input capacitance would triple, but each time C went low, the upper A, B and C transistors would turn on, tripling the available source current. If input D was low also, all four of the upper transistors would be on.

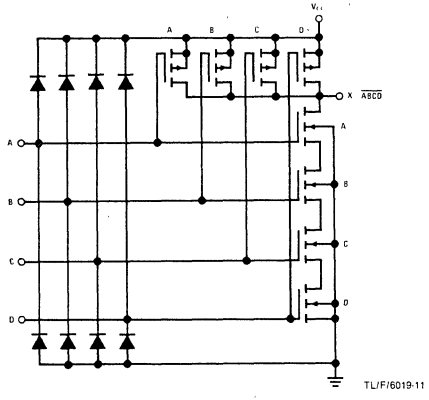


FIGURE 3-1. MM74C20 Four Input NAND Gate.

So, tying unused NAND gate inputs to V_{CC} (Ground for NOR gates) will enable them, but tying unused inputs to other used inputs guarantees an increase in source current in the case of NAND gates (sink current in the case of NOR gates). There is no increase in drive possible through the series transistors. By using this approach, a multiple input gate could be used to drive a heavy current load such as a lamp or a relay.

Parallel gates: depending on the type of gate, tying inputs together guarantees an increase in either source or sink current but not both. To guarantee an increase in both currents, a number of gates must be paralleled as in Figure 3-2. This insures that there are a number of parallel combinations of the series string of transistors (Figure 3-1), thereby increasing drive in that direction also.

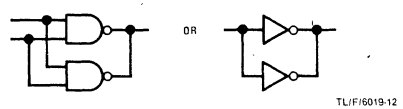


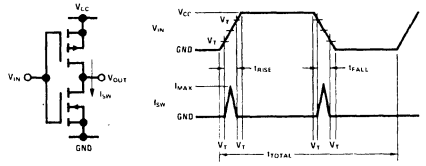
FIGURE 3-2. Paralleling Gates or Inverters Increases Output Drive in Both Directions.

Data bussing: there are essentially two ways to do this. First, connect ordinary CMOS parts to a bus using transfer gates (part no. CD4016C). Second,

and the preferred way, is to use parts specifically designed with a CMOS equivalent of a TRI-STATE® output.

Power supply filtering: since CMOS can operate over a large range of power supply voltages (3V to 15V), the filtering necessary is minimal. The minimum power supply voltage required will be determined by the maximum frequency of operation of the fastest element in the system (usually only a very small portion of any system operates at maximum frequency). The filtering should be designed to keep the power supply voltage somewhere between this minimum voltage and the maximum rated voltage the parts can tolerate. However, if power dissipation is to be kept to a minimum, the power supply voltage should be kept as low as possible while still meeting all speed requirements.

Minimizing system power dissipation: to minimize power consumption in a given system, it should be run at the minimum speed to do the job with the lowest possible power supply voltage. AC and DC transient power consumption both increase with frequency and power supply voltage. The AC power is described as CV^2f power. This is the power dissipated in a driver driving a capacitive load. Obviously, AC power consumption increases directly with frequency and as the square of the power supply. It also increases with capacitive load, but this is usually defined by the system and is not alterable. The DC power is the VI power dissipated during switching. In any CMOS device during switching, there is a momentary current path from the power supply to ground, (when $V_{CC} > 2V_T$) Figure 3-3.



VI POWER IS GIVEN BY:

$P_{VI} = V_{CC} \times \frac{1}{2} I_{MAX} \times$ RISE TIME TO PERIOD RATIO

RISE TIME TO PERIOD RATIO $= \frac{V_{CC} - 2V_T}{V_{CC}} \times \frac{t_{RISE} + t_{FALL}}{t_{TOTAL}}$

WHERE $\frac{1}{t_{TOTAL}}$ = FREQUENCY

$P_{VI} = 1/2\,(V_{CC} - 2V_T)\, I_{CC\,MAX}\,(t_{RISE} + t_{FALL})$ FREQ.

TL/F/6019-13

FIGURE 3-3. DC Transient Power.

The maximum amplitude of the current is a rapidly increasing function of the input voltage which in turn is a direct function of the power supply voltage. See Figure 2-4d.

The actual amount of VI power dissipated by the system is determined by three things: power supply voltage, frequency and input signal rise time. A very important factor is the input rise time. If the rise time is long, power dissipation increases since the current path is established for the entire period that the input signal is passing through the region between the threshold voltages of the upper and lower transistors. Theoretically, if the rise time were zero, no current path would be established and the VI power would be zero. However, with a finite rise time there is always some current flow and this current flow increases rapidly with power supply voltage.

Just a thought about rise time and power dissipation. If a circuit is used to drive many loads, its output rise time will suffer. This will result in an increase in VI power dissipation in every device being driven by that circuit (but not in the drive circuit itself). If power consumption is critical, it may be necessary to improve the rise time of that circuit by buffering or by dividing the loads in order to reduce overall power consumption.

So, to summarize the effects of power supply voltage, input voltage, input rise time and output load capacitance on system power dissipation, we can say the following:

1. **Power supply voltage:** CV^2f power dissipation increases as the square of power supply voltage. VI power dissipation increases approximately as the square of the power supply voltage.
2. **Input voltage level:** VI power dissipation increases if the input voltage lies somewhere between Ground plus a threshold voltage and V_{CC} minus a threshold voltage. The highest power dissipation occurs when V_{IN} is at 1/2 V_{CC}. CV^2f dissipation is unaffected.
3. **Input rise time:** VI power dissipation increases with longer rise times since the DC current path through the device is established for a longer period. The CV^2f power is unaffected by slow input rise times.
4. **Output load capacitance:** the CV^2f power dissipated in a circuit increases directly with load capacitance. VI power in a circuit is unaffected by its output load capacitance. However, increasing output load capacitance will slow down the output rise time of a circuit which in turn will affect the VI power dissipation in the devices it is driving.

INTERFACES TO OTHER LOGIC TYPES

There are two main ideas behind all of the following interfaces to CMOS. First, CMOS outputs should satisfy the current and voltage requirements of the other family's inputs. Second, and probably most important, the other family's outputs should swing as near as possible to the full voltage range of the CMOS power supplies.

P-Channel MOS: there are a number of things to watch for when interfacing CMOS and P-MOS. The first is the power supply set. Most of the more popular P-MOS parts are specified with 17 to 24V power supplies while the maximum power supply voltage for CMOS is 15V. Another problem

is that unlike CMOS, the output swing of a push-pull P-MOS output is significantly less than the power supply voltage across it. P-MOS swings from very close to its more positive supply (V_{SS}) to quite a few volts above its more negative supply (V_{DD}). So, even if P-MOS uses a 15V or lower power supply set, its output swing will not go low enough for a reliable interface to CMOS. There are a number of ways to solve this problem depending on the configuration of the system. We will discuss two solutions for systems that are built totally with MOS and one solution for systems that include bipolar logic.

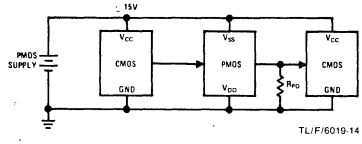
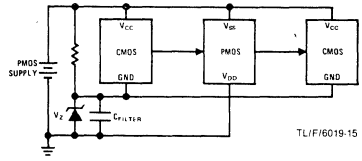


FIGURE 3-4. A One Power Supply System Built Entirely of CMOS and P-MOS.

First, MOS only. P-MOS and CMOS using the same power supply of less than 15V, Figure 3-4.

In this configuration CMOS drives P-MOS directly. However, P-MOS cannot drive CMOS directly because of its output will not pull down close enough to the lower power supply rail. R_{PD} (R pull down) is added to each P-MOS output to pull it all the way down to the lower rail. Its value is selected such that it is small enough to give the desired RC time constant when pulling down but not so small that the P-MOS output cannot pull it virtually all the way up to the upper power supply rail when it needs to. This approach will work with push-pull as well as open drain P-MOS outputs.

Another approach in a purely MOS system is to build a cheap zener supply to bias up the lower power supply rail of CMOS, Figure 3-5.

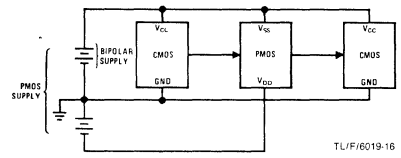


Use a bias supply to reduce the voltage across the CMOS to match the logic swing of the P-MOS. Make sure the resulting voltage across the CMOS is less than 15V.

FIGURE 3-5. A P-MOS and CMOS System Where The P-MOS Supply is Greater Than 15V.

In this configuration the P-MOS supply is selected to satisfy the P-MOS voltage requirement. The bias supply voltage is selected to reduce the total voltage across the CMOS (and therefore its logic swing) to match the minimum swing of the P-MOS outputs. The CMOS can still drive P-MOS directly and now the P-MOS can drive CMOS with no pull-down resistors. The other restrictions are that the total voltage across the CMOS is less than 15V and that the bias supply can handle the current requirements of all the CMOS. This approach is useful if the P-MOS supply must be greater than 15V and the CMOS current requirement is low enough to be done easily with a small discrete component regulator.

If the system has bipolar logic, it will usually have at least two power supplies. In this case, the CMOS is run off the bipolar supply and it interfaces directly to P-MOS, Figure 3-6.

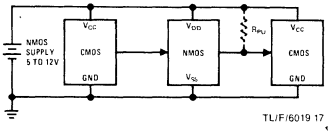


Run the CMOS from the bipolar supply and interface directly to P-MOS

FIGURE 3-6. A System With CMOS, P-MOS and Bipolar Logic.

N-Channel MOS: interfacing to N-MOS is somewhat simpler than interfacing to P-MOS although similar problems exist. First, N-MOS requires lower power supplies than P-MOS, being in the range of 5V to 12V. This is directly compatible with CMOS. Second, N-MOS logic levels range from slightly above the lower power supply rail to about 1 to 2V below the upper rail.

At the higher power supply voltages, N-MOS and CMOS can be interfaced directly since the N-MOS high logic level will be only about 10 to 20 percent below the upper rail. However, at lower supply voltages the N-MOS output level will be down 20 to 40 percent below the upper rail and something may have to be done to raise it. The simplest solution is to add pull up resistors on the N-MOS outputs as shown in Figure 3-7.



Both operate off same supply with pull up resistors optional from N-MOS to CMOS

FIGURE 3-7. A System With CMOS and N-MOS Only.

TTL, LPTTL, DTL: two questions arise when interfacing bipolar logic families to CMOS. First, is the bipolar family's logic "1" output voltage high enough to drive CMOS directly?

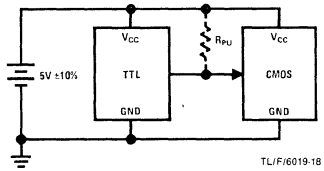
TTL, LPTTL, and DTL can drive 74C series CMOS directly over the commercial temperature range without external pull up resistors. However, TTL and LPTTL cannot drive 4000 series CMOS directly (DTL can) since 4000 series specs do not guarantee that a direct interface with no pull up resistors will operate properly.

DTL and LPTTL manufactured by National (NS LPTTL pulls up one diode drop higher than the LPTTL of other vendors) will also drive 74C directly over the entire military temperature range. LPTTL manufactured by other vendors and standard TTL will drive 74C directly over most of the mil temperature range. However, the TTL logic "1" drops to a somewhat marginal level toward the lower end of the mil temperature range and a pull up resistor is recommended.

According to the curve of DC margin vs V_{CC} for CMOS in Figure 2-5, if the CMOS sees an input voltage greater than $V_{CC} - 1.5V$ ($V_{CC} = 5V$), the output is guaranteed to be less than 0.5V from Ground. The next CMOS element will amplify this 0.5V level to the proper logic levels of V_{CC} or Ground. The standard TTL logic "1" spec is a V_{OUT} min. of 2.4V sourcing a current of 400μA. This is an extremely conservative spec since a TTL output will only approach a one level of 2.4V under the extreme worst case conditions of lowest temperature, high input voltage (0.8V), highest possible leakage currents (into succeeding TTL devices), and V_{CC} at the lowest allowable (V_{CC} = 4.5V).

Under nominal conditions (25°C, V_{IN} = 0.4V, nominal leakage currents into CMOS and V_{CC} = 5V) a TTL logic "1" will be more like $V_{CC} - 2V_D$, or $V_{CC} - 1.2V$. Varying only temperature, the output will change by two times −2mV per °C, or −4 mV per °C. $V_{CC} - 1.2V$ is more than enough to drive CMOS reliably without the use of a pull up resistor.

If the system is such that the TTL logic "1" output can drop below $V_{CC} - 1.5V$, use a pull up resistor to improve the logic "1" voltage into the CMOS.



Pull up resistor, R_{PU}, is needed only at the lower end of the Mil temperature range.

FIGURE 3-8. TTL to CMOS Interface.

The second question is, can CMOS sink the bipolar input current and not exceed the maximum value of the bipolar logic zero input voltage? The logic "1" input is no problem.

The LPTTL input current is small enough to allow CMOS to drive two loads directly. Normal power TTL input currents are ten times higher than those in LPTTL and consequently the CMOS output voltage will be well above the input logic "0" maximum of 0.8V. However, by carefully examining the CMOS output specs we will find that a two input NOR gate can drive one TTL load, albeit somewhat marginally. For example, the logical "0" output voltage for both an MM74C00 and MM74C02 over temperature is specified at 0.4V sinking 360μA (about 420μA at 25°C) with an input voltage of 4.0V and a V_{CC} of 4.75V. Both schematics are shown in Figure 3-9.

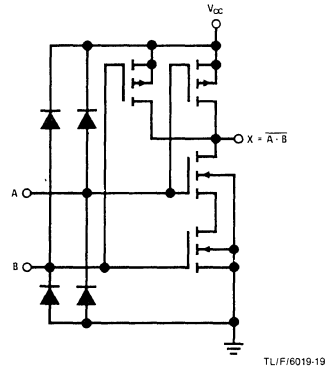


FIGURE 3-9a. MM74C00.

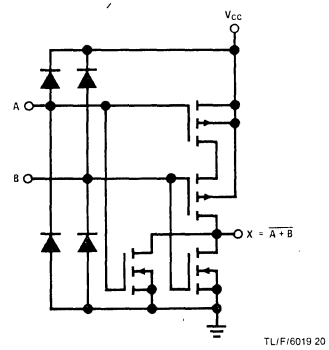


FIGURE 3-9b. MM74C02.

Both parts have the same current sinking spec but their structures are different. What this means is that either of the lower transistors in the MM74C02 can sink the same current as the two lower series transistors in the MM74C00. Both MM74C02 transistors together can sink twice the specified current for a given output voltage. If we allow the output voltage to go to 0.8V, then a MM74C02 can sink four times 360μA, or 1.44 mA which is nearly 1.6 mA. Actually, 1.6 mA is the maximum

spec for the TTL input current and most TTL parts run at about 1 mA. Also, 360μA is the minimum CMOS sink current spec, the parts will really sink somewhere between 360 and 540μA (between 2 and 3 LPTTL input loads). The 360μA sink current is specified with an input voltage of 4.0V. With an input voltage of 5.0V, the sink current will be about 560μA over temperature, making it even easier to drive TTL. At room temperature with an input voltage of 5V, a CMOS output can sink about 800μA. A 2 input NOR gate, therefore, will sink about 1.6 mA with a V_{OUT} of about 0.4V if both NOR gate inputs are at 5V.

The main point of this discussion is that a common 2 input CMOS NOR gate such as an MM74C02 can be used to drive a normal TTL load in lieu of a special buffer. However, the designer must be willing to sacrifice some noise immunity over temperature to do so.

TIMING CONSIDERATIONS IN CMOS MSIs

There is one more thing to be said in closing. All the flip-flops used in CMOS designs are genuinely edge sensitive. This means that the J-K flip-flops do not "ones catch" and that some of the timing restrictions that applied to the control lines on MSI functions in TTL have been relaxed in the 74C series.

CMOS Linear Applications

National Semiconductor
Application Note 88
Gene Taajes
July 1973

PNP and NPN bipolar transistors have been used for many years in "complementary" type of amplifier circuits. Now, with the arrival of CMOS technology, complementary P-channel/N-channel MOS transistors are available in monolithic form. The MM74C04 incorporates a P-channel MOS transistor and an N-channel MOS transistor connected in complementary fashion to function as an inverter.

Due to the symmetry of the P- and N-channel transistors, negative feedback around the complementary pair will cause the pair to self bias itself to approximately 1/2 of the supply voltage. Figure 1 shows an idealized voltage transfer characteristic curve of the CMOS inverter connected with negative feedback. Under these conditions the inverter is biased for operation about the midpoint in the linear segment on the steep transition of the voltage transfer characteristic as shown in Figure 1.

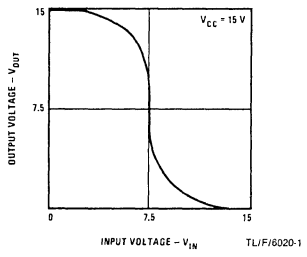


FIGURE 1. Idealized Voltage Transfer Characteristics of an MM74C04 Inverter.

Under AC conditions, a positive going input will cause the output to swing negative and a negative going input will have an inverse effect. Figure 2 shows 1/6 of a MM74C04 inverter package connected as an AC amplifier.

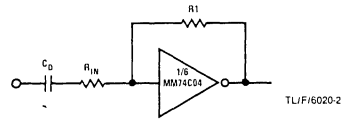


FIGURE 2. A 74CMOS Invertor Biased for Linear Mode Operation.

The power supply current is constant during dynamic operation since the inverter is biased for Class A operation. When the input signal swings near the supply, the output signal will become distorted because the P-N channel devices are driven into the non-linear regions of their transfer characteristics. If the input signal approaches the supply voltages, the P- or N-channel transistors become saturated and supply current is reduced to essentially zero and the device behaves like the classical digital inverter.

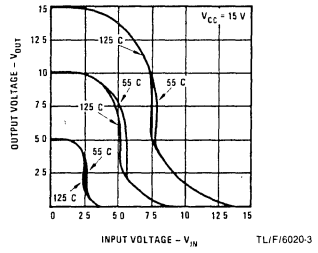


FIGURE 3. Voltage Transfer Characteristics for an Inverter Connected as a Linear Amplifier.

Figure 3 shows typical voltage characteristics of each inverter at several values of the V_{CC}. The shape of these transfer curves are relatively constant with temperature. Temperature affects for the self biased inverter with supply voltage is shown in Figure 4. When the amplifier is operating at 3 volts, the supply current changes drastically as a function of supply voltage because the MOS transistors are operating in the proximity of their gate-source threshold voltages.

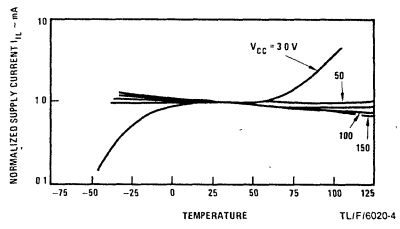


FIGURE 4. Normalized Amplifier Supply Current Versus Ambient Temperature Characteristics.

Figure 5 shows typical curves of voltage gain as a function of operating frequency for various supply voltages.

Output voltages can swing within millivolts of the supplies with either a single or dual supply.

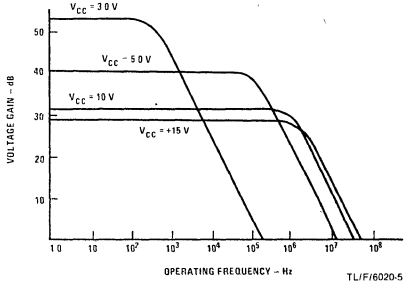


FIGURE 5. Typical Voltage Gain Versus Frequency Characteristics for Amplifier Shown in Figure 2.

APPLICATIONS

Cascading Amplifiers for Higher Gain.

By cascading the basic amplifier block shown in Figure 2 a high gain amplifier can be achieved. The gain will be multiplied by the number of stages used. If more than one inverter is used inside the feedback loop (as in Figure 6) a higher open loop gain is achieved which results in more accurate closed loop gains.

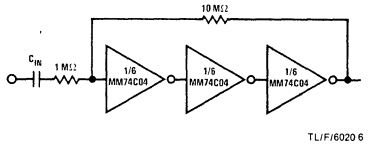


FIGURE 6. Three CMOS Inverters Used as an X10 AC Amplifier.

Post Amplifier for Op Amps.

A standard operational amplifier used with a CMOS inverter for a Post Amplifier has several advantages. The operational amplifier essentially sees no load condition since the input impedance to the inverter is very high. Secondly, the CMOS inverters will swing to within millivolts of either supply. This gives the designer the advantage of operating the operational amplifier under no load conditions yet having the full supply swing capability on the output. Shown in Figure 7 is the LM4250 micropower Op Amp used with a 74C04 inverter for increased output capability while maintaining the low power advantage of both devices.

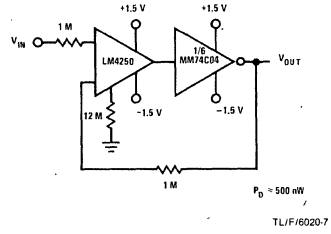


FIGURE 7. MM74C04 Inverter Used as a Post Amplifier for a Battery Operated Op Amp.

The MM74C04 can also be used with single supply amplifier such as the LM324. With the circuit shown in Figure 8, the open loop gain is approximately 160 dB. The LM324 has 4 amplifiers in a package and the MM74C04 has 6 amplifiers per package.

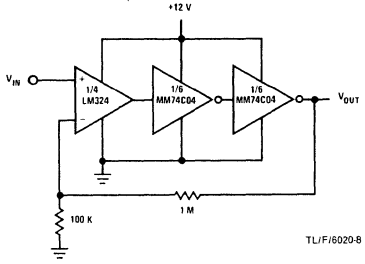
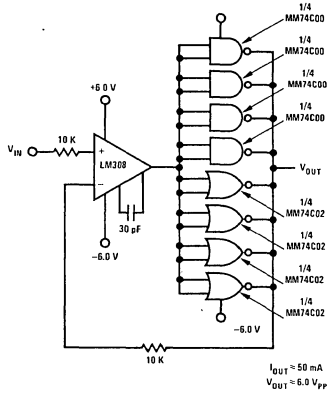


FIGURE 8. Single Supply Amplifier Using a CMOS Cascade Post Amplifier with the LM324.

CMOS inverters can be paralleled for increased power to drive higher current loads. Loads of 5.0 mA per inverter can be expected under AC conditions.

Other 74C devices can be used to provide greater complementary current outputs. The MM74C00 NAND Gate will provide approximately 10 mA

from the V_{CC} supply while the MM74C02 will supply approximately 10 mA from the negative supply. Shown in Figure 9 is an operational amplifier using a CMOS power post amplifier to provide greater than 40 mA complementary currents.



TL/F/6020-9

FIGURE 9. MM74C00 and MM74C02 Used as a Post Amplifier to Provide Increased Current Drive.

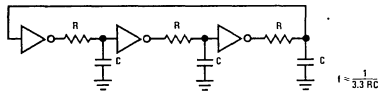
Other Applications.

Shown in Figure 10 is a variety of applications utilizing CMOS devices. Shown is a linear phase shift oscillator and an integrator which use the CMOS devices in the linear mode as well as a few circuit ideas for clocks and one shots.

Conclusion

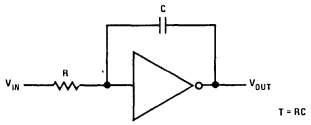
Careful study of CMOS characteristics show that CMOS devices used in a system design can be used for linear building blocks as well as digital blocks.

Utilization of these new devices will decrease package count and reduce supply requirements. The circuit designer now can do both digital and linear designs with the same type of device.



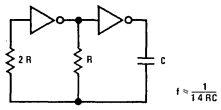
TL/F/6020-10

Phase Shift Oscillator Using MM74C04



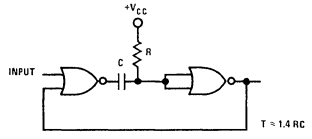
Integrator Using Any Inverting CMOS Gate

TL/F/6020-11



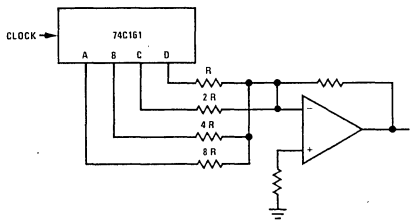
Square Wave Oscillator

TL/F/6020-12



One Shot

TL/F/6020-13



TL/F/6020-14

Staircase Generator

FIGURE 10. Variety of Circuit Ideas Using CMOS Devices.

54C/74C Family Characteristics

National Semiconductor
Application Note 90
Thomas P. Redfern
August 1973

INTRODUCTION

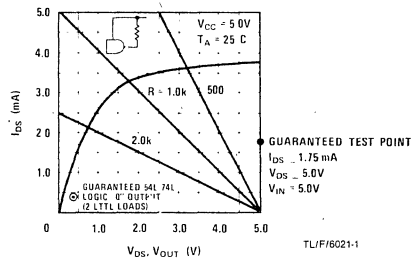
The purpose of this 54C/74C Family Characteristics application note is to set down, in one place, all those characteristics which are common to the devices in the MM54C/MM74C logic family. The characteristics which can be considered to apply are:

1. Output voltage-current characteristics
2. Noise characteristics
3. Power consumption
4. Propagation delay (speed)
5. Temperature characteristics

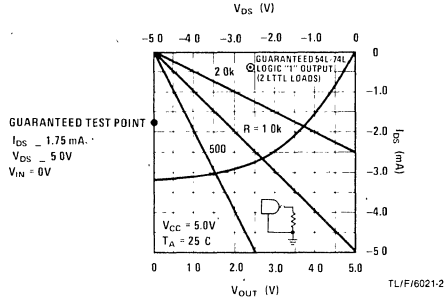
With a good understanding of the above characteristics the designer will have the necessary tools to optimize his system. An attempt will be made to present the information in as simple a manner as possible to facilitate its use. This coupled with the fact that 54C/74C has the same function and pin-out as standard series 54L/74L will make the application of CMOS to digital systems very straightforward.

OUTPUT CHARACTERISTICS

Figure 1 and Figure 2 show typical output drain characteristics for the basic inverter used in the 54C/74C family. For more detailed information on the operation of the basic inverter the reader is directed to application note AN-77, "CMOS, The Ideal Logic Family." Although more complex gates, and MSI devices, may be composed of combinations of parallel and series transistors the considerations that govern the output characteristics of the basic inverter apply to these more complex structures as well.

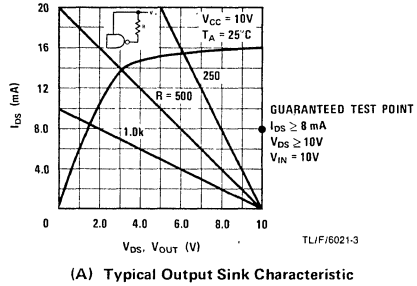


(A) Typical Output Sink Characteristic (N-Channel)

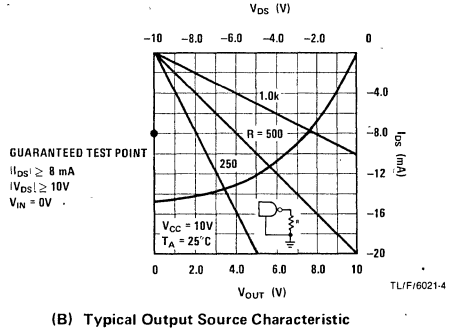


(B) Typical Output Source Characteristic (P-Channel)

FIGURE 1



(A) Typical Output Sink Characteristic (N-Channel)



(B) Typical Output Source Characteristic (P-Channel)

FIGURE 2

The 54C/74C family is designed so that the output characteristics of all devices are matched as closely as possible. To ensure uniformity all devices are tested at four output conditions (see Figures 1 and 2). These points are:

V_{CC} = 5.0V	V_{IN} = 5.0V $I_{DS} \geq$ 1.75 mA $V_{DS} \geq$ 5.0V	V_{IN} = 0V $\|I_{DS}\| >$ 1.75 mA $\|V_{DS}\| >$ 5.0V
V_{CC} = 10V	V_{IN} = 10V $I_{DS} \geq$ 8.0 mA $V_{DS} \geq$ 10V	V_{IN} = 0V $\|I_{DS}\| \geq$ 8.0 mA $\|V_{DS}\| \geq$ 10V

Note that each device data sheet guarantees these points in the table of electrical characteristics.

The output characteristics can be used to determine the output voltage for any load condition. Figures 1 and 2 show load lines for resistive loads to V_{CC} for sink currents and to GND for source currents. The intersections of this load line with the drain characteristic in question gives the output voltage. For example at V_{CC} = 5.0V, V_{OUT} = 1.5V (typ) with a load of 500Ω to ground.

These figures also show the guaranteed points for driving two 54L/74L standard loads. As can be seen there is typically ample margin at V_{CC} = 5.0V.

In the case where the 54C/74C device is driving another CMOS device the load line is coincident with the I_{DS} = 0 axis and the output will then typically switch to either V_{CC} or ground.

NOISE CHARACTERISTICS

Definition of Terms

Noise Immunity: The noise immunity of a logic element is that voltage which applied to the input will cause the output to change its output state.

Noise Margin: The noise margin of a logic element is the difference between the guaranteed logical "1" ("0") level output voltage and the guaranteed logical "1" ("0") level input voltage.

The transfer characteristic of Figure 3 shows typical noise immunity and guaranteed noise margin for a 54C/74C device operating at V_{CC} = 10V. The typical noise immunity does not change with voltage and is 45% of V_{CC}.

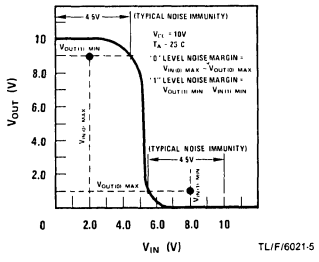


FIGURE 3. Typical Transfer Characteristic

All 54C/74C devices are guaranteed to have a noise margin of 1.0V or greater over all operating conditions (see Figure 4).

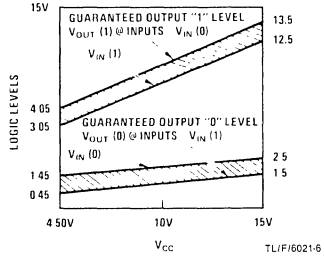


FIGURE 4. Guaranteed Noise Margin Over Temperature vs V_{CC}

Noise immunity is an important device characteristic. However, noise margin is of more use to the designer because it very simply defines the amount of noise a system can tolerate under any circumstances and still maintain the integrity of logic levels.

Any noise specification to be complete must define how measurements are to be made. Figure 5 indicates two extreme cases; driving all inputs simultaneously and driving one input at a time. Both conditions must be included because each represents one worst case extreme.

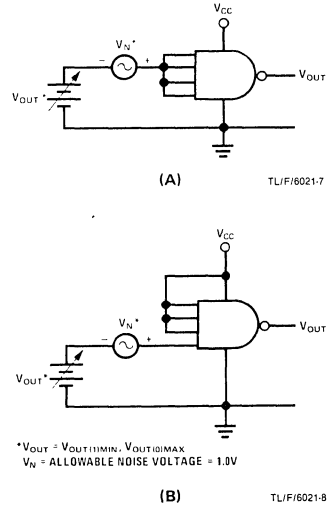


FIGURE 5. Noise Margin Test Circuits

To guarantee a noise margin of 1.0V, all 54C/74C devices are tested under both conditions. It is important to note that this guarantees that every node within a system can have 1.0V of noise, in logic "1" or logic "0" state, without malfunctioning. This could not be guaranteed without testing for both conditions in Figure 5.

POWER CONSUMPTION

There are four sources of power consumption in CMOS devices: (1) leakage current (2) transient power due to load capacitance (3) transient power due to internal capacitance and (4) transient power due to current spiking during switching.

The first, leakage current, is the easiest to calculate and is simply the leakage current times V_{CC}. The data sheet for each specific device specifies this leakage current.

The second, transient power due to load capacitance, can be derived from the fact that the energy stored on a capacitor is $1/2\ CV^2$. Therefore every time the load capacitance is charged or discharged this amount of energy must be provided by the CMOS device. The energy per cycle is then $2\ [(1/2)\ CV_{CC}^2] = CV_{CC}^2$. Energy per unit time, or power, is then $CV_{CC}^2\ f$, where C is the load capacitance and f is the frequency.

The third, transient power due to internal capacitance takes exactly the same form as the load capacitance. Every device has some internal nodal capacitance which must be charged and discharged. This then represents another power term which must be considered.

The fourth, transient power due to switching current, is caused by the fact that whenever a CMOS device goes through a transition, with $V_{CC} \geq 2\ V_T$, there is a time when both N-channel and P-channel devices are both conducting. An expression for this current is derived in application note AN-77. The expression is:

$$P_{VI} = \frac{1}{2}\ (V_{CC} - 2\ V_T)\ I_{CCMAX}\ (t_{RISE} + t_{FALL})\ f$$

where:

V_T = threshold voltage

$I_{CC(MAX)}$ = peak non-capacitive current during switching

f = frequency

Note that this expression, like the capacitive power term is directly proportional to frequency. If the P_{VI} term is combined with the term arising from the internal capacitance, a capacitance C_{PD} may be defined which closely approximates the no load power consumption for a CMOS device when used in the following expression:

$$\text{Power (no load)} = C_{PD}\ V_{CC}^2\ f$$

The total power consumption is then simplified to:

$$\text{Total Power} = (C_{PD} + C_L)\ V_{CC}^2\ f + I_{LEAK}\ V_{CC} \quad (1)$$

The procedure for obtaining C_{PD} is to measure the no load power at V_{CC} = 10V vs frequency and calculate the value of C_{PD} which corresponds to the measured power consumption. This value of C_{PD} is given on each 54C/74C data sheet and with equation (1) the computation of power consumption is straightforward.

To simplify the task even further Figure 6 gives a graph of normalized power vs frequency for different power supply voltages. To obtain actual power consumption find the normalized power for a particular V_{CC} and frequency, then multiply by $C_{PD} + C_L$.

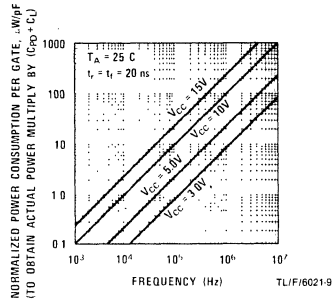


FIGURE 6. Normalized Typical Power Consumption vs Frequency

As an example let's find the total power consumption for an MM74C00 operating at f = 100 kHz, V_{CC} = 10V and C_L = 50 pF. From the curve, normalized power per gate equals 10μW/pF. From the data sheet C_{PD} = 12 pF; therefore, actual power per gate is:

$$\frac{\text{power}}{\text{gate}} = \frac{10\mu W}{pF} \times (12\ pF + 50\ pF) = \frac{0.62\ mW}{\text{gate}}$$

$$\text{total power} = \frac{\text{no. of gates}}{\text{package}} \times \frac{\text{power}}{\text{gate}} + I_{LEAKAGE} \times V_{CC}$$

$$= 4 \times 0.62\ mW + 0.01\mu A \times 10V \cong 2.48\ mW$$

Up to this point the discussion of power consumption has been limited to simple gate functions. Power consumption for an MSI function is more complex but the same technique just derived applies. To demonstrate the technique let's compute the total power consumption of a MM74C161, four bit binary counter, at V_{CC} = 10V, f = 1 MHz and C_L = 50 pF on each output.

The no load power is still given by P (no load) = $C_{PD}\ V_{CC}^2\ f$. This demonstrates the usefulness of the concept of the internal capacitance, C_{PD}. Even through the circuit is very complex and has many nodes charging and discharging at various rates, all of the effects can be easily lumped into one easy to use term, C_{PD}.

Calculation of transient power due to load capacitance is a little more complex since each output is switched at one half the rate of the previous output: Taking this into account the complete expression for power consumption is:

$$P_{TOTAL} = \underbrace{C_{PD} V_{CC}^2 f}_{\text{no load power}} + \underbrace{C_L V_{CC}^2 \frac{f}{2}}_{\text{output power of 1st stage}} + \underbrace{C_L V_{CC}^2 \frac{f}{4}}_{\text{2nd stage}}$$

$$+ \underbrace{C_L V_{CC}^2 \frac{f}{8}}_{\text{3rd stage}} + \underbrace{2 C_L V_{CC}^2 \frac{f}{16}}_{\text{4th stage \& carry output}} + \underbrace{I_L V_{CC}}_{\text{leakage term}}$$

This reduces to:

$$P_{TOTAL} = (C_{PD} + C_L) V_{CC}^2 f + I_L V_{CC}$$

From the data sheet C_{PD} = 90 pF and I_L = 0.05μA. Using Figure 6 total power is then:

$$P_{TOTAL} = (90 \text{ pF} + 50 \text{ pF}) \times \frac{100\mu W}{pF} + 0.05 \times 10^{-6} \times 10V \cong 14 \text{ mW}$$

This demonstrates that with more complex devices the concept of C_{PD} greatly simplifies the calculation of total power consumption. It becomes an easy task to compute power for different voltages and frequencies by use of Figure 6 and the equations above.

PROPAGATION DELAY

Propagation delay for all 54C/74C devices is guaranteed with a load of 50 pF *and input rise and fall times of 20 ns.* A 50 pF load was chosen, instead of 15 pF as in the 4000 series, because it is representative of loads commonly seen in CMOS systems. A good rule of thumb, in designing with CMOS, is to assume 10 pF of interwiring capacitance. Operating at the specified propagation delay would allow 5 pF fanout for the 4000 series while 54C/74C has a fanout of 40 pF. A fanout of 5 pF (one gate input) is all but useless, and specified propagation delay would most probably not be realized in an actual system.

Operating at loads other than 50 pF poses a problem since propagation is a function of load capacitance. To simplify the problem Figure 7 has been generated and gives the slope of the propagation delay vs load capacitance line (Δt_{pd}/pF) as a function of power supply voltage. Because

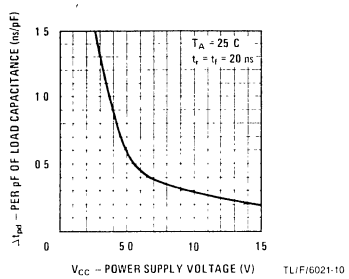


FIGURE 7. Typical Propagation Delay per pF of Load Capacitance vs Power Supply

the propagation delay for zero load capacitance is not zero and depends on the internal structure of each device, an offset term must be added that is unique to a particular device type. Since each data sheet gives propagation delay for 50 pF the actual delay for different loads can be computed with the aid of the following equation:

$$t_{pd}\Big|_{C_L = C} = (C - 50) \text{ pF} \times \frac{\Delta t_{pd}}{pF} + t_{pd}\Big|_{C_L = 50 \text{ pF}}$$

where:

C = Actual load capacitance

$t_{pd}\Big|_{C_L = 50 \text{ pF}}$ = propagation delay with 50 pF load, (specified on each device data sheet)

$\frac{\Delta t_{pd}}{pF}$ = Value obtained from Figure 7.

As an example let's compute the propagation delay for an MM74C00 driving 15 pF load and operating with a V_{CC} = 5.0V. The equation gives:

$$t_{pd}\Big|_{C_L = 15 \text{ pF}} = (15 - 50) \text{ pF} \times 0.57 \frac{ns}{pF} + 50 \text{ ns}$$

$$= -20 \text{ ns} + 50 \text{ ns} = 30 \text{ ns}$$

The same formula and curves may be applied to more complex devices. For example the propagation delay from data to output for an MM74C157 operating at V_{CC} = 10V and C_L = 100 pF is:

$$t_{pd}\Big|_{C_L = 100 \text{ pF}} = (100 - 50)\ 0.29 \text{ ns} + 70 \text{ ns}$$

$$= 14.5 + 70 \cong 85 \text{ ns}$$

It is significant to note that this equation and Figure 7 apply to *all* 54C/74C devices. This is true because of the close match in drive characteristics of every device including MSI functions, i.e., the slope of the propagation delay vs load capacitance line at a given voltage is typically equal for all devices. The only exception is high fan-out buffers which have a smaller $\Delta t_{pd}/pF$.

Another point to consider in the design of a CMOS system is the affect of power supply voltage on propagation delay. Figure 8 shows propagation delay as a function of V_{CC} and propagation delay times power consumption vs V_{CC} for an MM74C00 operating with 50 pF load at f = 100 kHz.

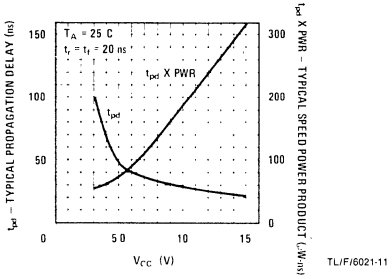


FIGURE 8. Speed Power Product and Propagation Delay vs V_{CC}

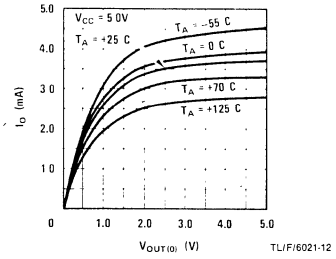
Above V_{CC} = 5.0V note the speed power product curve approaches a straight line. However the t_{pd} curve starts to "flatten out." Going from *V_{CC} = 5.0V to V_{CC} = 10V gives a 40% decrease in propagation delay and going from V_{CC} = 10V to V_{CC} = 15V only decreases propagation delay by 25%.* Clearly for V_{CC} > 10V a small increase in speed is gained by a disproportionate increase in power. Conversely, for small decreases in power below V_{CC} = 5.0V large increases in propagation delay result.

Obviously it is optimum to use the lowest voltage consistent with system speed requirements. However in general it can be seen from Figure 8 that the best speed power performance will be obtained in the V_{CC} = 5.0V to V_{CC} = 10V range.

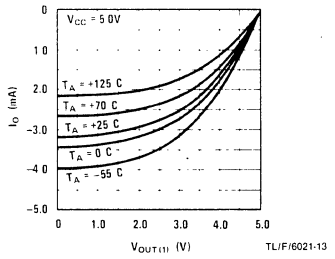
TEMPERATURE CHARACTERISTICS

Figures 9 and 10 give temperature variations in drain characteristics for the N-channel and P-channel devices operating at V_{CC} = 5.0V and V_{CC} = 10V respectively. As can be seen from these curves the output sink and source current decreases as temperature increases. The affect is almost linear and can be closely approximated by a temperature coefficient of −0.3% per degree centigrade.

Since the t_{pd} can be entirely attributed to rise and fall time, the temperature dependance of t_{pd} is a function of the rate at which the output load capacitance can be charged and discharged. This in turn is a function of the sink/source current which was shown above to vary as −0.3% per degree centigrade. Consequently we can say that t_{pd} varies as −0.3% per degree centigrade. Actual measurements of t_{pd} with temperature verifies this number.

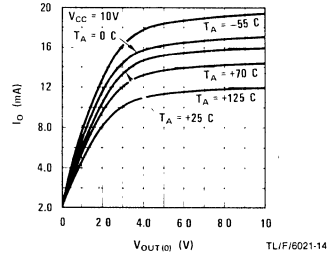


(A) Typical Output Drain Characteristic (N-Channel)

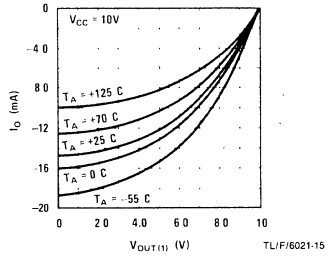


(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 9



(A) Typical Output Drain Characteristic (N-Channel)



(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 10

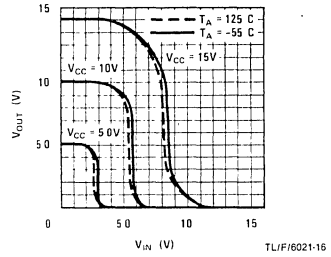


FIGURE 11. Typical Gate Transfer Characteristics

The drain characteristics of Figure 9 and 10 show considerable variation with temperature. Examination of the transfer characteristics of Figure 11 indicates that they are almost independent of temperature. The transfer characteristic is not dependent on temperature because although both the N-channel and P-channel device characteristics change with temperature these changes track each other closely. The proof of this tracking is the temperature independance of the transfer characteristics. Noise margin and maximum/minimum logic levels will then not be dependent on temperature.

As discussed previously power consumption is a function of C_{PD}, C_L, V_{CC}, f and $I_{LEAKAGE}$. All of these terms are essentially constant with temperature except $I_{LEAKAGE}$. However, the leakage current specified on each 54C/74C device applies across the entire temperature range and therefore represents a worst case limit.

CMOS Oscillators

National Semiconductor
Application Note 118
Mike Watts
October 1974

INTRODUCTION

This note describes several square wave oscillators that can be built using CMOS logic elements. These circuits offer the following advantages:

- Guaranteed startability
- Relatively good stability with respect to power supply variations
- Operation over a wide supply voltage range (3V to 15V)
- Operation over a wide frequency range from less than 1 Hz to about 15 MHz
- Low power consumption (see AN-90)
- Easy interface to other logic families and elements including TTL

Several RC oscillators and two crystal controlled oscillators are described. The stability of the RC oscillator will be sufficient for the bulk of applications; however, some applications will probably require the stability of a crystal. Some applications that require a lot of stability are:

1. Timekeeping over a long interval. A good deal of stability is required to duplicate the performance of an ordinary wrist watch (about 12 ppm). This is, of course, obtainable with a crystal. However, if the time interval is short and/or the resolution of the timekeeping device is relatively large, an RC oscillator may be adequate. For example: if a stopwatch is built with a resolution of tenths of seconds and the longest interval of interest is two minutes, then an accuracy of 1 part in 1200 (2 minutes x 60 seconds/minute x 10 tenth/second) may be acceptable since any error is less than the resolution of the device.

2. When logic elements are operated near their specified limits. It may be necessary to maintain clock frequency accuracy within very tight limits in order to avoid exceeding the limits of the logic family being used, or in which the timing relationships of clock signals in dynamic MOS memory or shift register systems must be preserved.

3. Baud rate generators for communications equipment.

4. Any system that must interface with other tightly specified systems. Particularly those that use a "handshake" technique in which Request or Acknowledge pulses must be of specific widths.

LOGICAL OSCILLATORS

Before describing any specific circuits, a few words about logical oscillators may clear up some recurring confusion.

Any odd number of inverting logic gates will oscillate if they are tied together in a ring as shown in *Figure 1.* Many beginning logic designers have discovered this (to their chagrin) by inadvertently providing such a path in their designs. However, some people are confused by the circuit in *Figure 1* because they are accustomed to seeing sinewave oscillators implemented with positive feedback, or amplifiers with non-inverting gain. Since the concept of phase shift becomes a little strained when the inverters remain in their linear region for such a short period, it is far more straightforward to analyze the circuit from the standpoint of ideal switches with finite propagation delays rather than as amplifiers with 180° phase shift. It then becomes obvious that a "1" chases itself around the ring and the network oscillates.

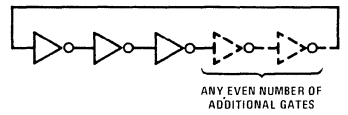


FIGURE 1. Odd Number of Inverters will Always Oscillate

The frequency of oscillation will be determined by the total propagation delay through the ring and is given by the following equation.

$$f = \frac{1}{2nTp}$$

Where:

f = frequency of oscillation
Tp = Propagation delay per gate
n = number of gates

This is not a practical oscillator, of course, but it does illustrate the maximum frequency at which such an oscillator will run. All that must be done to make this a useful oscillator is to slow it down to the desired frequency. Methods of doing this are described later.

To determine the frequency of oscillation, it is necessary to examine the propagation delay of the inverters. CMOS propagation delay depends on supply voltage and load capacitance. Several curves for propagation delay for National's 74C line of CMOS gates are reproduced in *Figure 2.* From these, the natural frequency of oscillation of an odd number of gates can be determined.

An example may be instructive.

Assume the supply voltage is 10V. Since only one input is driven by each inverter, the load capacitance on each inverter is at most about 8 pF. Examine the curve in *Figure 2c* that is drawn for V_{CC} = 10V and extrapolate it down to 8 pF. We see that the curve predicts a propagation delay of about 17 ns. We can then calculate the frequency of oscillation for three inverters using the expression mentioned above. Thus:

$$f = \frac{1}{2 \times 3 \times 17 \times 10^{-9}} = 9.8\ \text{MHz}$$

Lab work indicates this is low and that something closer to 16 MHz can be expected. This reflects the conservative nature of the curves in *Figure 2.*

Since this frequency is directly controlled by propagation delays, it will vary a great deal with temperature, supply voltage, and any external loading, as indicated by the graphs in *Figure 2.* In order to build a usefully stable oscillator it is necessary to add passive elements that determine oscillation frequency and minimize the effect of CMOS characteristics.

STABLE RC OSCILLATOR

Figure 3 illustrates a useful oscillator made with three inverters. Actually, any inverting CMOS gate or combination of gates could be used. This means left over portions

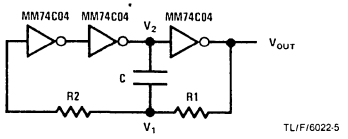


FIGURE 3. Three Gate Oscilaltor

of gate packages can be often used. The duty cycle will be close to 50% and will oscillate at a frequency that is given by the following expression.

$$f \cong \frac{1}{2\ R1\ C\left(\frac{0.405\ R2}{R1 + R2} + 0.693\right)}$$

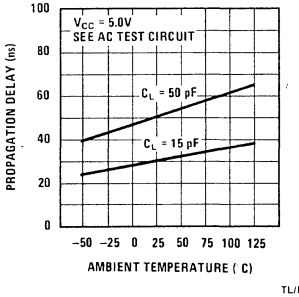
Another form of this expression is:

$$f \cong \frac{1}{2C\ (0.405\ R_{eq} + 0.693\ R1)}$$

Where:

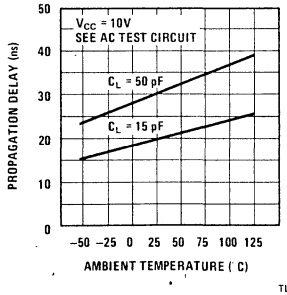
$$R_{eq} = \frac{R1\ R2}{R1 + R2}$$

Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



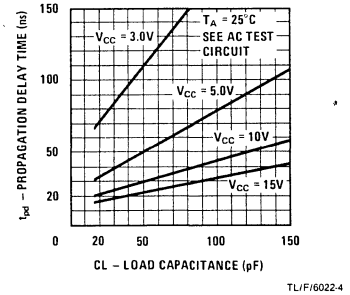
(a)

Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02, MM74C02, MM54C04/MM74C04



(b)

Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02, MM74C02, MM54C04/MM74C04



(c)

FIGURE 2. Propagation Delay for 74C Gates

The following three special cases may be useful.

$$\text{If } R1 = R2 = R \qquad f \cong \frac{0.559}{RC}$$

$$\text{If } R2 \ggg R1 \qquad f \cong \frac{0.455}{RC}$$

$$\text{If } R2 \lll R1 \qquad f \cong \frac{0.722}{RC}$$

Figure 4 illustrates the approximate output waveform and the voltage V_1 at the charging node.

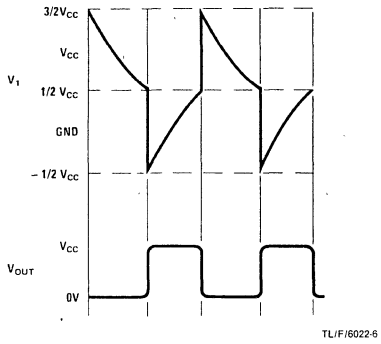


FIGURE 4. Waveforms for Oscillator in Figure 3

Note that the voltage V_2 will be clamped by input diodes when V_1 is greater than V_{CC} or more negative than ground. During this portion of the cycle current will flow through R2. At all other times the only current through R2 is a very minimal leakage term. Note also that as soon as V_1 passes through threshold (about 50% of supply) and the input to the last inverter begins to change, V_1 will also change in a direction that reinforces the switching action; i.e., providing positive feedback. This further enhances the stability and predictability of the network.

This oscillator is fairly insensitive to power supply variations due largely to the threshold tracking close to 50% of the supply voltage. Just how stable it is will be determined by the frequency of oscillation; the lower the frequency the more stability and vice versa. This is because propagation delay and the effect of threshold shifts comprise a smaller portion of the overall period. Stability will also be enhanced if R1 is made large enough to swamp any variations in the CMOS output resistance.

TWO GATE OSCILLATOR WILL NOT NECESSARILY OSCILLATE

A popular oscillator is shown in *Figure 5a.* The only undesirable feature of this oscillator is that it may not oscillate. This is readily demonstrated by letting the value of C go to zero. The network then degenerates into *Figure 5b,* which obviously will not oscillate. This illustrates that there is some value of C1 that will not force the network to oscillate. The real difference between this two gate oscillator and the three gate oscillator is that the former must be forced to oscillate by the capacitor while the three gate network will always oscillate willingly and is simply slowed down by the capacitor. The three gate network will always oscillate, regardless of the value of C1 but the two gate oscillator will not oscillate when C1 is small.

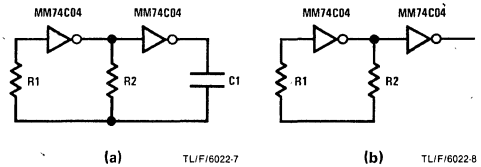


FIGURE 5. Less Than Perfect Oscillator

The only advantage the two gate oscillator has over the three gate oscillator is that it uses one less inverter. This may or may not be a real concern, depending on the gate count in each user's specific application. However, the next section offers a real minimum parts count oscillator.

A SINGLE SCHMITT TRIGGER MAKES AN OSCILLATOR

Figure 6 illustrates an oscillator made from a single Schmitt trigger. Since the MM74C14 is a hex Schmitt trigger, this oscillator consumes only one sixth of a package. The remaining 5 gates can be used either as ordinary inverters like the MM74C04 or their Schmitt trigger characteristics can be used to advantage in the normal manner. Assuming these five inverters can be used elsewhere in the system, *Figure 6* must represent the ultimate in low gate count oscillators.

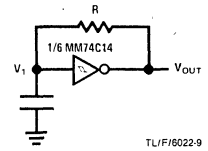


FIGURE 6. Schmitt Trigger Oscillator

Voltage V_1 is depicted in *Figure 7* and changes between the two thresholds of the Schmitt trigger. If these thresholds were constant percentages of V_{CC} over the supply voltage range, the oscillator would be insensitive to variations in V_{CC}. However, this is not the case. The thresholds of the Schmitt trigger vary enough to make the oscillator exhibit a good deal of sensitivity to V_{CC}.

Applications that do not require extreme stability or that have access to well regulated supplies should not be bothered by this sensitivity to V_{CC}. Variations in threshold can be expected to run as high as four or five percent when V_{CC} varies from 5V to 15V.

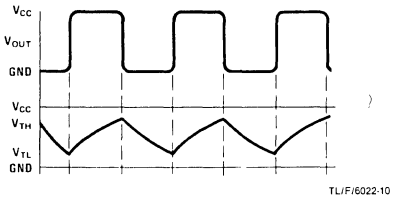


FIGURE 7. Waveforms for Schmitt Trigger Oscillator in Figure 6

A CMOS Crystal Oscillator

Figure 8 illustrates a crystal oscillator that uses only one CMOS inverter as the active element. Any odd number of inverters may be used, but the total propagation delay through the ring limits the highest frequency that can be obtained. Obviously, the fewer inverters that are used, the higher the maximum possible frequency.

CONCLUSIONS

A large number of oscillator applications can be implemented with the extremely simple, reliable, inexpensive and versatile CMOS oscillators described in this note. These oscillators consume very little power compared to most other approaches. Each of the oscillators requires less than one full package of CMOS inverters of the MM74C04 variety. Frequently such an oscillator can be built using leftover gates of the MM74C00, MM74C02, MM74C10 variety. Stability superior to that easily attainable with TTL oscillators is readily attained, particularly at lower frequencies. These oscillators are so versatile, easy to build, and inexpensive that they should find their way into many diverse designs.

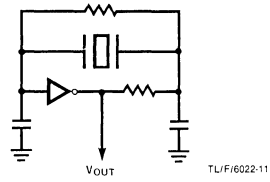


FIGURE 8. Crystal Oscillator

Using the CMOS Dual Monostable Multivibrator

National Semiconductor
Application Note 138
Thomas P. Redfern
May 1975

INTRODUCTION

The MM54C221/MM74C221 is a dual CMOS monostable multivibrator. Each one-shot has three inputs (A, B and CLR) and two outputs (Q and $\overline{Q}$). The output pulse width is set by an external RC network.

The A and B inputs trigger an output pulse on a negative or positive input transition respectively. The CLR input when low resets the one-shot. Once triggered the A and B inputs have no further control on the output.

THEORY OF OPERATION

Figure 1 shows that in its stable state, the one-shot clamps C_{EXT} to ground by turning N1 ON and holds the positive comparator input at V_{CC} by turning N2 OFF. The prefix N is used to denote N-channel transistors.

The signal, G, gating N2 OFF also gates the comparator OFF thereby keeping the internal power dissipation to an absolute minimum. The only power dissipation when in the stable state is that generated by the current through R_{EXT}. The bulk of this dissipation is in R_{EXT} since the voltage drop across N1 is very small for normal ranges of R_{EXT}.

To trigger the one-shot the CLR input must be high. The gating, G, on the comparator is designed such that the comparator output is high when the one-shot is in its stable state. With the CLR input high the clear input to FF is disabled allowing the flip-flop to respond to the A or B input. A negative transition on A or a positive transition on B sets Q to a high state. This in turn gates N1 OFF, and N2 and the comparator ON.

Gating N2 ON establishes a reference of 0.63 V_{CC} on the comparator's positive input. Since the voltage on C_{EXT} can not change instantaneously V1 = 0V at this time. The comparator then will maintain its one level on the output. Gating N1 OFF allows C_{EXT} to start charging through R_{EXT} toward V_{CC} exponentially.

Assuming a perfect comparator (zero offset and infinite gain) when the voltage on C_{EXT}, V1, equals 0.63 V_{CC} the comparator output will go from a high state to a low state resetting Q to a low state. *Figure 2* is a timing diagram summarizing this sequence of events.

This diagram is idealized by assuming zero rise and fall times and zero propagation delay but it shows the basic operation of the one-shot. Also shown is the effect of taking the CLR input low. Whenever CLR goes low FF

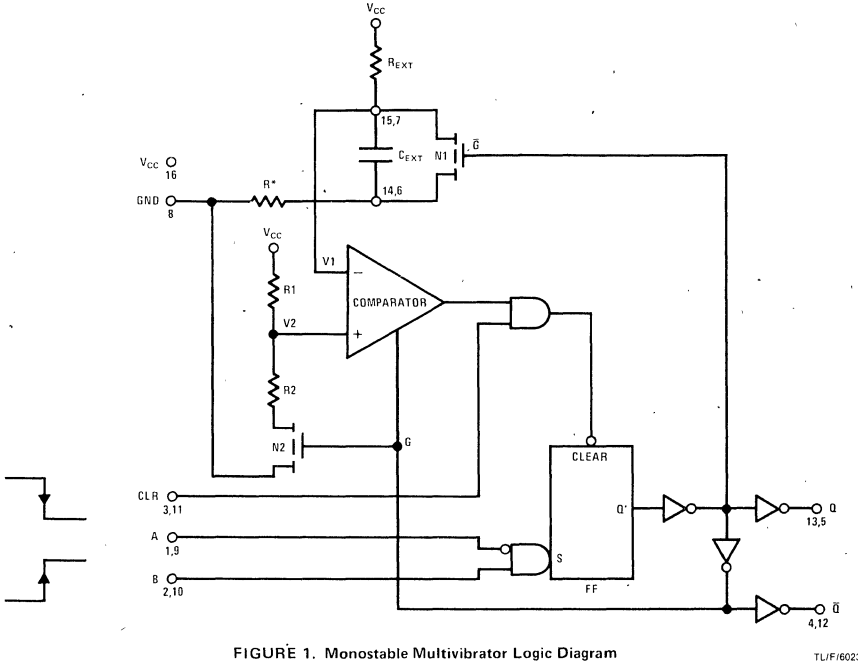


FIGURE 1. Monostable Multivibrator Logic Diagram

TL/F/6023 1

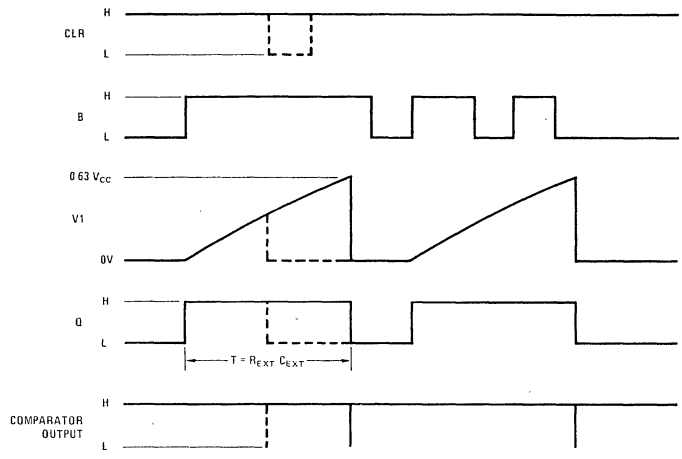


FIGURE 2. One-Shot Timing Diagram

is reset independent of all other inputs. *Figure 2* also shows that once triggered, the output is independent of any transitions on B (or A) until the cycle is complete.

The output pulse width is determined by the following equation:

$$V1 = V_{CC}\ (1 - e^{-T/R_{EXT}\,C_{EXT}}) = 0.63\ V_{CC} \qquad (1)$$

Solving for t gives:

$$T = R_{EXT}\ C_{EXT}\ \ln (1/0.37) = R_{EXT}\ C_{EXT} \qquad (2)$$

A word of caution should be given in regards to the ground connection of the external capacitor (C_{EXT}). It should always be connected as shown in *Figure 1* to pin 14 or 6 and never to pin 8. This is important because of the parasitic resistor R*. Because of the large discharge current through R*, if the capacitor is connected to pin 8, a four layer diode action can result causing the circuit to latch and possibly damage itself.

ACCURACY

There are many factors which influence the accuracy of the one-shot. The most important are:

a. Comparator input offset
b. Comparator gain
c. Comparator time delay
d. Voltage divider R1, R2
e. Delays in logic elements
f. ON impedance of N1 and N2
g. Leakage of N1
h. Leakage of C_{EXT}
i. Magnitude of R_{EXT} and C_{EXT}

The characteristics of C_{EXT} and R_{EXT} are, of course, not determined by the characteristics of the one-shot. In order to establish the accuracy of the one-shot, devices were tested using an external resistance of 10 kΩ and various capacitors. A resistance of 10 kΩ was chosen because the leakage and ON impedance of transistor N1 have a minimal effect on accuracy with this value of resistance.

Two values of C_{EXT} were chosen, 1000 pF and 0.1μF. These values give pulse widths of 10μs and 1000μs with R_{EXT} = 10 kΩ.

Figures 3 and 4 show the resulting distributions of pulse widths at 25°C for various power supply voltages. *Because propagation delays, at the same power supply voltage, are the same independent of pulse width, the shorter the pulse width the more the accuracy is*

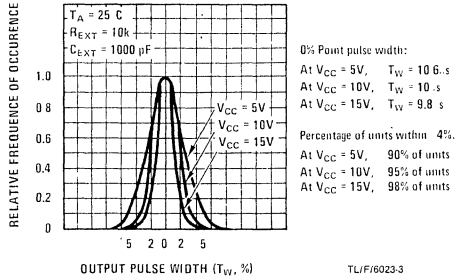


FIGURE 3. Typical Pulse Width Distribution for 10μs Pulse.

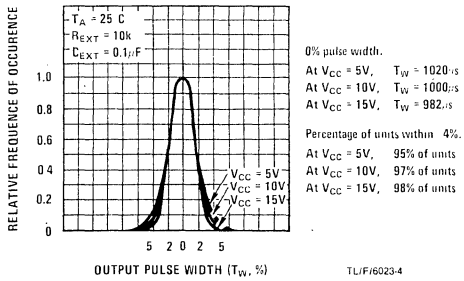


FIGURE 4. Typical Pulse Width Distribution for 1000μs Pulse.

affected by propagation delay. *Figures 3 and 4* clearly show this effect. As pointed out in application note AN-90, 54C/74C Family Characteristics, propagation delay is a function of V_{CC}. *Figure 3*, (Pulse Width = 10μs) shows much greater variation with V_{CC} than *Figure 4* (Pulse Width = 1000μs). This same information is shown in *Figures 5 and 6* in a different format. In

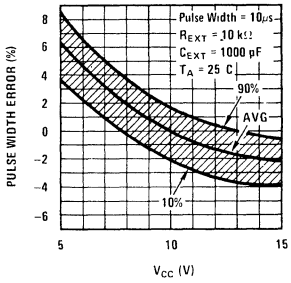


FIGURE 5. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 10μs).

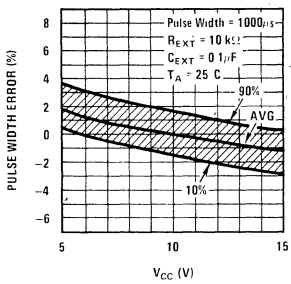


FIGURE 6. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 1000μs).

these figures the percent deviation from the average pulse width at 10V V_{CC} is shown vs V_{CC}. In addition to the average value the 10% and 90% points are shown. These percentage points refer to the statistical distribution of pulse width error. As an example, at V_{CC} = 10V for 10μs pulse width, 90% of the devices have errors of less than +1.7% and 10% have errors less than −2.1%. In other words, 80% have errors between +1.7% and −2.1%.

The minimum error can be obtained by operating at the maximum V_{CC}. A price must be paid for this and this price is, of course, increased power dissipation.

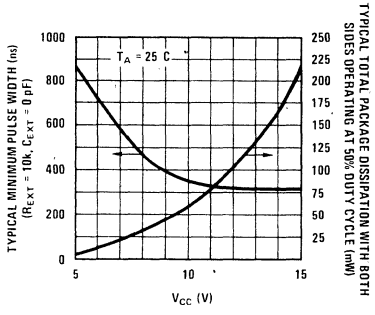


FIGURE 7. Typical Minimum Pulse Width and Power Dissipation vs V_{CC}.

Figure 7 shows typical power dissipation vs V_{CC} operating both sides of the one-shot at 50% duty cycle. Also shown in the same figure is typical minimum pulse width vs V_{CC}. The minimum pulse width is a strong function of internal propagation delays. *It is obvious from these two curves that increasing V_{CC} beyond 10V will not appreciably improve inaccuracy due to propagation delay but will greatly increase power dissipation.*

Accuracy is also a function of temperature. To determine the magnitude of its effects the one-shot was tested at temperature with the external resistance and capacitance maintained at 25°C. The resulting variation is shown in *Figures 8 and 9.*

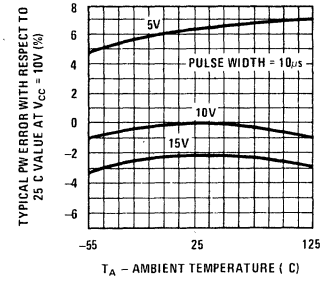


FIGURE 8. Typical Pulse Width Error vs Temperature (PW = 10μs).

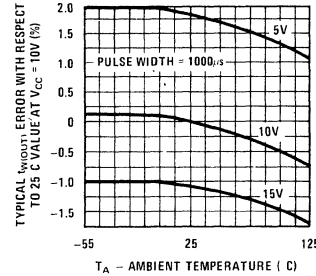


FIGURE 9. Typical Pulse Width Error vs Temperature (PW = 1000μs).

Up to this point the external timing resistor, R_{EXT}, has been held fixed at 10 kΩ. In actual applications other values may be necessary to achieve the desired pulse width. The question then arises as to what effect this will have on accuracy.

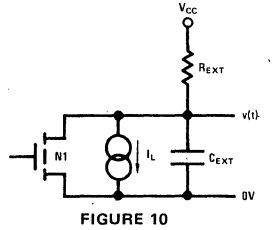


FIGURE 10

As R_{EXT} becomes larger and larger the leakage current on transistor N1 becomes an ever increasing problem. The equivalent circuit for this leakage is shown in *Figure 10.*

v(t) is given by:

$$v(t) = (V_{CC} - I_L R_{EXT})(1 - e^{-t_L/R_{EXT} C_{EXT}})$$

As before, when $v(t) = 0.63 V_{CC}$, the output will reset. Solving for t_L gives:

$$t_L = R_{EXT} C_{EXT} \ln\left(\frac{V_{CC} - I_L R_{EXT}}{0.37 V_{CC} - I_L R_{EXT}}\right) \quad (3)$$

Using T as defined in Equation 2 the pulse width error is:

$$\text{PW Error} = \frac{t_L - T}{T} \times 100\%$$

Substituting Equations 2 and 3 gives:

$$\text{PW Error} = \frac{R_{EXT} C_{EXT} \ln\left(\frac{V_{CC} - I_L R_{EXT}}{0.37 V_{CC} - I_L R_{EXT}}\right) - R_{EXT} C_{EXT} \ln(1/0.37)}{R_{EXT} C_{EXT} \ln(1/0.37)}$$

PW Error is plotted in *Figure 11* for V_{CC} = 5, 10 and 15V. As expected, decreasing V_{CC} causes PW Error to increase with fixed I_L. Note that the leakage current, although here assumed to flow through N1, is general and could also be interpreted as leakage through C_{EXT}. See MM54C221/MM74C221 data sheet for leakage limits.

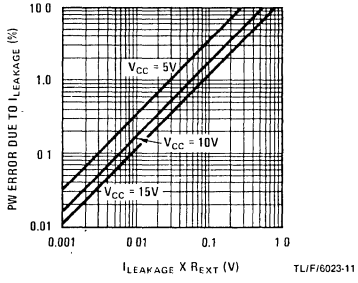


FIGURE 11. Percentage Pulse Width Error Due to Leakage.

To demonstrate the usefulness of *Figure 11* an example will be most helpful. Let us assume that N1 has a leakage of 250 x 10^{-9} amps, C_{EXT} has leakage of 150 x 10^{-9} amps, output pulse width = 0.1 seconds and V_{CC} = 5V. What R_{EXT} C_{EXT} should be used to guarantee an error due to leakage of less than 5%.

From *Figure 11* we see that to meet these conditions R_{EXT} $I_L < 0.14V$.

Then:

$$R_{EXT} < 0.14/(250 + 150) \times 10^{-9}$$

$$< 350\ k\Omega$$

Choosing standard component values of 250 kΩ and 0.004μF would satisfy the above conditions.

We have just defined the limitation on the maximum size of R_{EXT}. There is a corresponding limit on the minimum size that R_{EXT} can assume. This is brought about because of the finite ON impedance of N1. As R_{EXT} is made smaller and smaller the amount of voltage across N1 becomes significant. The voltage across N1 is:

$$V_{N1} = V_{CC} r_{ON}/(R_{EXT} + r_{ON}) \quad (4)$$

The output pulse width is defined by:

$$v(t_O) = (V_{CC} - V_{N1})(1 - e^{-t_O/R_{EXT} C_{EXT}}) + V_{N1} = 0.63 V_{CC}$$

Solving for t_O gives:

$$t_O = R_{EXT} C_{EXT} \ln\left(\frac{V_{CC} - V_{N1}}{0.37 V_{CC}}\right)$$

Pulse Width Error is then:

$$\text{PW Error} = \frac{t_O - T}{T} \times 100\%$$

Substituting Equations 2 and 4 gives:

$$= \frac{R_{EXT} C_{EXT} \ln\left(\frac{V_{CC} - V_{N1}}{0.37 V_{CC}}\right) - R_{EXT} C_{EXT} \ln(1/0.37)}{R_{EXT} C_{EXT} \ln(1/0.37)}$$

This function is plotted in *Figure 12* for r_{ON} of 50Ω, 25Ω and 16.7Ω. These are the typical values of r_{ON} for a V_{CC} of 5V, 10V and 15V respectively.

As an example, assume that the pulse width error due to r_{ON} must be less than 0.5% operating at V_{CC} = 5V. The typical value of r_{ON} for V_{CC} = 5V is 50Ω. Referring to

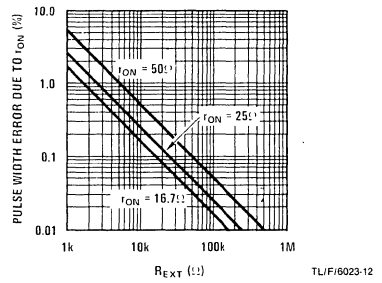


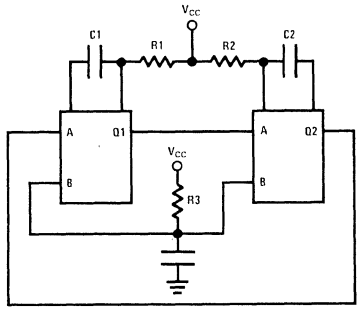
FIGURE 12. Percentage Pulse Width Error Due to Finite r_{ON} of Transistor N1 vs R_{EXT}.

the 50Ω curve in *Figure 12*, R_{EXT} must be greater than 10 kΩ to maintain this accuracy. At V_{CC} = 10V, R_{EXT} must be greater than 5 kΩ as can be seen from the 25Ω curve in *Figure 12.*

Although clearly shown on the MM54C221/MM74C221 data sheet, it is worthwhile, for the sake of clarity, to point out that the parasitic capacitance between pins 7 (15) and 6 (14) is typically 15 pF. This capacitor is in parallel with C_{EXT} and must be taken into account when accuracy is critical.

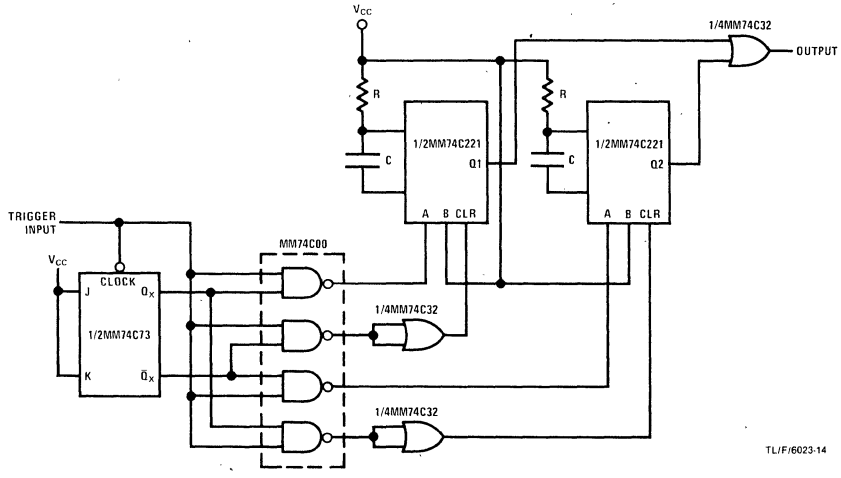
TYPICAL APPLICATIONS

Basic One-Shot Oscillator



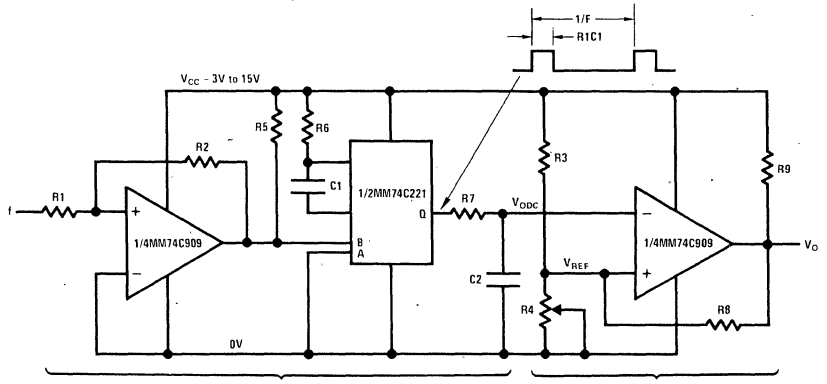
TL/F/6023-13

Retriggerable One-Shot



TL/F/6023-14

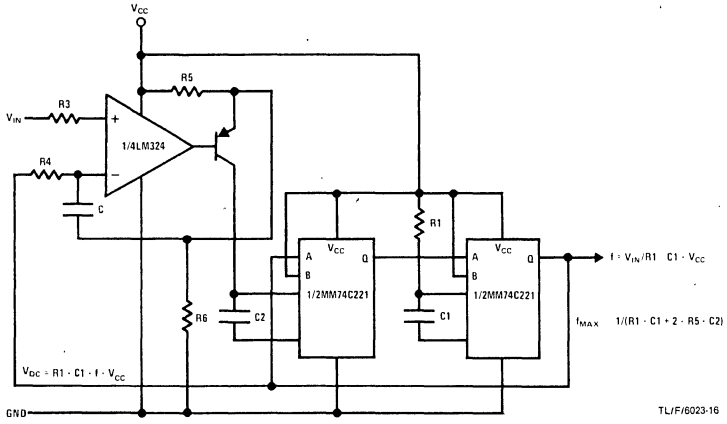
Frequency Magnitude Comparator



TL/F/6023-15

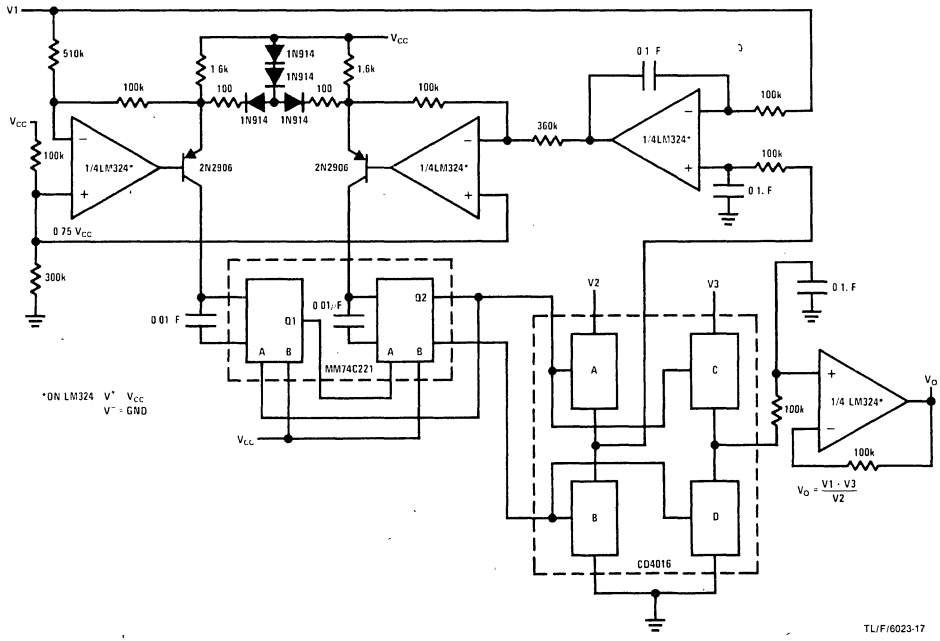
TYPICAL APPLICATIONS (Continued)

Linear VCO



TL/F/6023-16

Analog Multiplier/Divider



TL/F/6023-17

CMOS Schmitt Trigger —a Uniquely Versatile Design Component

National Semiconductor
Application Note 140
Gerald Buurma
June 1975

INTRODUCTION

The Schmitt trigger has found many applications in numerous circuits, both analog and digital. The versatility of a TTL Schmitt is hampered by its narrow supply range, limited interface capability, low input impedance and unbalanced output characteristics. The Schmitt trigger could be built from discrete devices to satisfy a particular parameter, but this is a careful and sometimes time-consuming design.

The CMOS Schmitt trigger, which comes six to a package, uses CMOS characteristics to optimize design and advance into areas where TTL could not go. These areas include: interfacing with op amps and transmission lines, which operate from large split supplies, logic level conversion, linear operation, and special designs relying on a CMOS characteristic. The CMOS Schmitt trigger has the following advantages:

- High impedance input ($10^{12}\Omega$ typical)
- Balanced input and output characteristics
  - Thresholds are typically symmetrical to 1/2 V_{CC}
  - Outputs source and sink equal currents
  - Outputs drive to supply rails
- Positive and negative-going thresholds show low variation with respect to temperature
- Wide supply range (3–15V), split supplies possible
- Low power consumption, even during transitions
- High noise immunity, 0.70 V_{CC} typical

Applications demonstrating how each of these characteristics can become a design advantage will be given later in the application note.

ANALYZING THE CMOS SCHMITT

The input of the Schmitt trigger goes through a standard input protection and is tied to the gates of four stacked devices. The upper two are P-channel and the lower two are N-channel. Transistors P3 and N3 are operating in the source follower mode and introduce hysteresis by feeding back the output voltage, out', to two different points in the stack.

When the input is at 0V, transistors P1 and P2 are ON, and N1, N2 and P3 are OFF. Since out' is high, N3 is ON and acting as a source follower, the drain of N1, which is the source of N2, is at $V_{CC}-V_{TH}$. If the input voltage is ramped up to one threshold above ground transistor N1 begins to turn ON, N1 and N3 both being ON form a voltage divider network biasing the source of N2 at roughly half the supply. When the input is a threshold above 1/2 V_{CC}, N2 begins to turn ON and regenerative switching is about to take over. Any more voltage on the input causes out' to drop. When out' drops, the source of N3 follows its gate, which is out', the influence of N3 in the voltage divider with N1 rapidly diminishes, bringing out' down further yet. Meanwhile P3 has started to turn ON, its gate being brought low by the rapidly dropping out'. P3 turning ON brings the source of P2 low and turns P2 OFF. With P2 OFF, out' crashes down. The snapping action is due to greater than unity loop gain through the stack caused by positive feedback through the source follower transistors. When the input is brought low again an identical process occurs in the upper portion of the stack and the snapping action takes place when the lower threshold is reached.

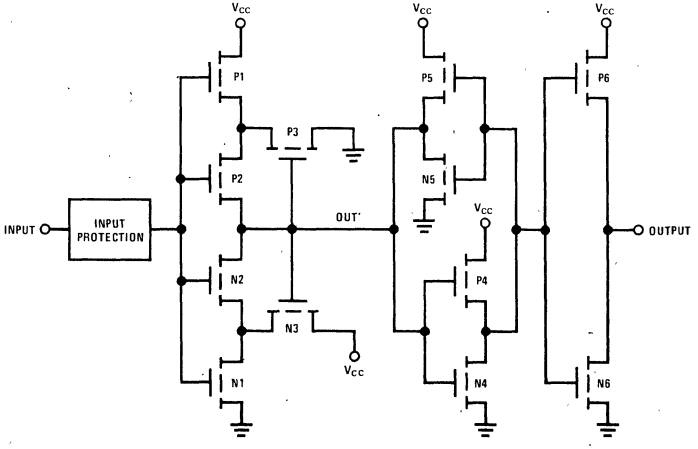


FIGURE 1. CMOS Schmitt Trigger

TL/F/6024-1

Out' is fed into the inverter formed by P4 and N4; another inverter built with very small devices, P5 and N5, forms a latch which stabilizes out'. The output is an inverting buffer capable of sinking 360μA or two LPTTL loads.

The typical transfer characteristics are shown in *Figure 2*; the guaranteed trip point range is shown in *Figure 3*.

WHAT HYSTERESIS CAN DO FOR YOU

Hysteresis is the difference in response due to the direction of input change. A noisy signal that traverses the threshold of a comparator can cause multiple transitions at the output, if the response time of the comparator is less than the time between spurious effects. A Schmitt trigger has two thresholds: any spurious effects must be greater than the threshold difference to cause multiple transitions. With a CMOS Schmitt at V_{CC} = 10V there is typically 3.6V of threshold difference, enough hysteresis to overcome almost any spurious signal on the input.

A comparator is often used to recover information sent down an unbalanced transmission line. The threshold of the comparator is placed at one half the signal amplitude (See *Figure 4b*). This is doen to prevent slicing level distortion. If a 4μs wide signal is sent down a transmission line a 4μs wide signal should be received or signal distortion occurs. If the comparator has a threshold above half the signal amplitude, then positive pulses sent are shorter and negative pulses are lengthened (See *Figure 4c*). This is called slicing level distortion. The Schmitt trigger does have a positive offset, V_{T+}, but it also has a negative offset V_{T-}. In CMOS these offsets are approximately symmetrical to half the signal level so a 4μs wide pulse sent is also recovered (see *Figure 4d*). The recovered pulse is delayed in time but the length is not changed, so noise immunity is achieved and signal distortion is not introduced because of threshold offsets.

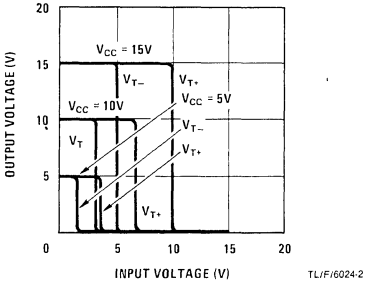


FIGURE 2. Typical CMOS Transfer Characteristics for Three Different Supply Voltages.

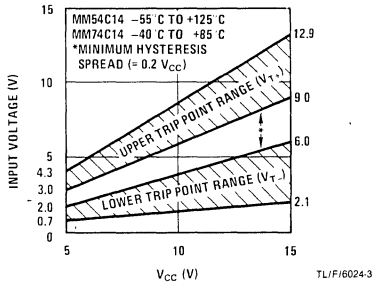


FIGURE 3. Guaranteed Trip Point Range.

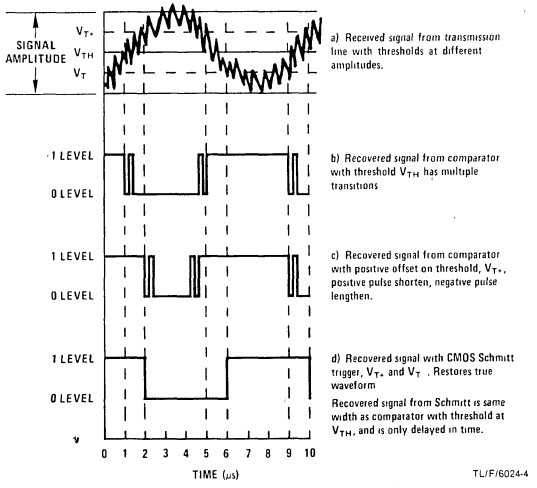
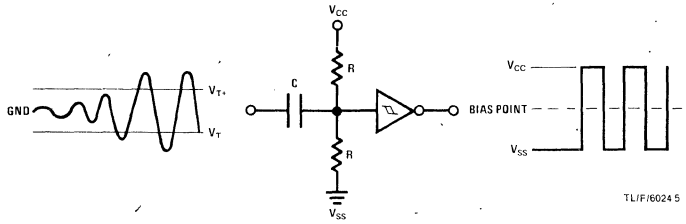
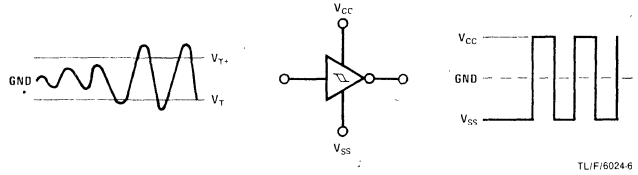


FIGURE 4. CMOS Schmitt Trigger Ignores Noise



a) Capacitor impedance at lowest operating frequency should be much less than R||R = 1/2R.



b) By using split supply (±1.5 to ±7.5) direct interface is achieved.

FIGURE 5. Sine to Square Wave Converter with Symmetrical Level Detection.

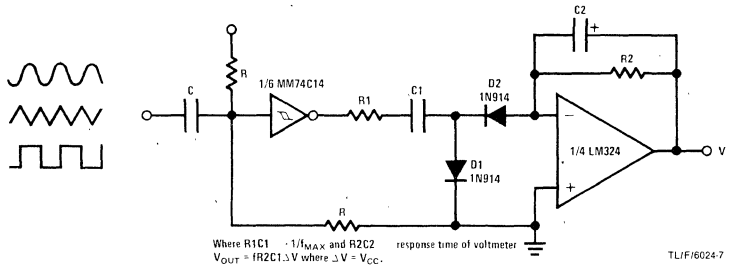


FIGURE 6. Diode Dump Tach Accepts any Input Waveform.

APPLICATIONS OF THE CMOS SCHMITT

Most of the following applications use a CMOS Schmitt characteristic to either simplify design or increase performance. Some of the applications could not be done at all with another logic family.

The circuit in *Figure 5a* is the familiar sine to square wave converter. Because of input symmetry the Schmitt trigger is easily biased to achieve a 50% duty cycle. The high input impedance simplifies the selection of the biasing resistors and coupling capacitor. Since CMOS has a wide supply range the Schmitt trigger could be powered from split supplies (see *Figure 5b*). This biases the mean threshold value around zero and makes direct coupling from an op amp output possible.

In *Figure 4*, we see a frequency to voltage converter that accepts many waveforms with no change in output voltage. Although the energy in the waveforms are quite different, it is only the frequency that determines the output voltage. Since the output of the CMOS Schmitt pulls completely to the supply rails, a constant voltage swing across capacitor C1 causes a current to flow through the capacitor, dependent only on frequency. On positive output swings, the current is dumped to ground through D1. On negative output swings, current is pulled from the inverting op amp node through D2 and transformed into an average voltage by R2 and C2.

Since the CMOS Schmitt pulls completely to the supply rails the voltage change across the capacitor is just the supply voltage.

Schmitt triggers are often used to generate fast transitions when a slowly varying function exceeds a predetermined level. In *Figure 7*, we see a typical circuit, a light activated switch. The high impedance input of the CMOS Schmitt trigger makes biasing very easy. Most photo cells are several kΩ brightly illuminated and a couple MΩ dark. Since CMOS has a $10^{12}\Omega$ typical input impedance, no effects are felt on the input when the output changes. The selection of the biasing resistor is just the solution of a voltage divider equation.

A CMOS application note wouldn't be complete without a low power application. *Figure 8* shows a simple RC oscillator. With only six R's and C's and one Hex CMOS trigger, six low power oscillators can be built. The square wave output is approximately 50% duty cycle because of the balanced input and output characteristics of CMOS. The output frequency equation assumes that $t_1 = t_2 >> t_{pd0} + t_{pd1}$.

We earlier saw how the CMOS Schmitt increased noise immunity on an unbalanced transmission line. *Figure 9* shows an application for a balanced or differential transmission line. The circuit in *Figure 7a* is CMOS EXCLUSIVE OR, the MM74C86, which could also be built from inverters, and NAND gates. If unbalanced information is generated on the line by signal crosstalk or external noise sources, it is recognized as an error.

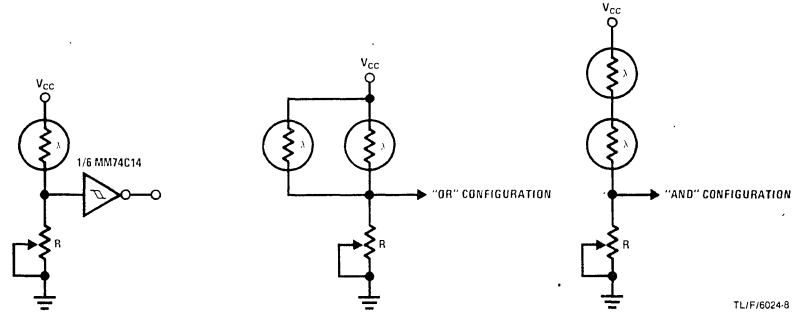


FIGURE 7. Light Activated Switch couldn't be Simpler. The Input Voltage Rises as Light Intensity Increases, when V_{T+} is Reached, the Output will go Low and Remain Low until the Intensity is Reduced Significantly.

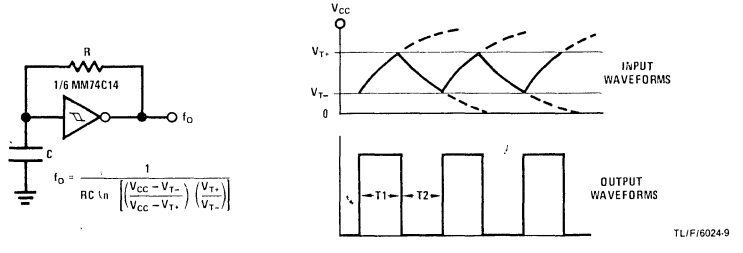
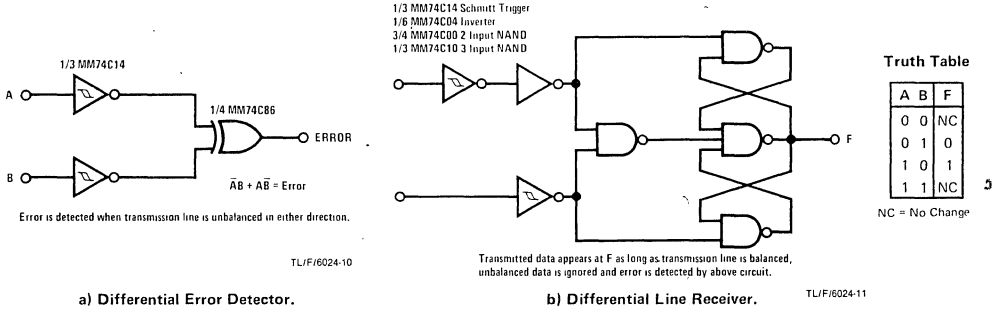


FIGURE 8. Simplest RC Oscillator? Six R's and C's make the CMOS Schmitt into Six Low Power Oscillators. Balanced Input and Output Characteristics give the Output Frequency a Typically 50% Duty Cycle.



a) Differential Error Detector. **b) Differential Line Receiver.**

FIGURE 9. Increase Noise Immunity by using the CMOS Schmitt Trigger to Demodulate a Balanced Transmission Line.

The circuit in *Figure 9b* is a differential line receiver that recovers balanced transmitted data but ignores unbalanced signals by latching up. If both circuits of *Figure 9* were used together, the error detector could signal the transmitter to stop transmission and the line receiver would remember the last valid information bit when unbalanced signals persisted on the line. When balanced signals are restored, the receiver can pick up where it left off.

The standard voltage range for CMOS inputs is V_{CC} +0.3V and ground −0.3V. This is because the input protection network is diode clamped to the supply rails. Any input exceeding the supply rails either sources or sinks a large amount of current through these diodes. Many times an input voltage range exceeding this is desirable; for example, transmission lines often operate from ±12V and op amps from ±15V. A solution to this problem is found in the MM74C914. This new device has an uncommon input protection that allows the input signal to go to 25V above ground, and 25V below V_{CC}. This means that the Schmitt trigger in the sine to square wave converter, in *Figure 5b*, could be powered by ±1.5V supplies and still be directly compatible with an op amp powered by ±15V supplies.

A standard input protection circuit and the new input protection are shown in *Figure 10*. The diodes shown have a 35V breakdown. The input voltage can go positive until reverse biased D2 breaks down through forward bias D3, which is 35V above ground. The input voltage can go negative until reverse biased D1 breaks down through forward bias D2, which is 35V below V_{CC}. Adequate input protection against static charge is still maintained.

CMOS can be linear over a wide voltage range if proper consideration is paid to the biasing of the inputs. *Figure 11* shows a simple VCO made with a CMOS inverter, acting as an integrator, and a CMOS Schmitt, acting as a comparator with hysteresis. The inverter integrates the positive difference between its threshold and the input voltage V_{IN}. The inverter output ramps up until the positive threshold of the Schmitt trigger is reached. At that time, the Schmitt trigger output goes low, turning on the transistor through R_s and speeding up capacitor C_s. Hysteresis keeps the output low until the integrating capacitor C is discharged through R_D. Resistor R_D should be kept much smaller than RC to keep reset time negligible. The output frequency is given by

$$f_O = \frac{V_{TH} - V_{IN}}{(V_{T+} - V_{T-})\ R_{CC}}.$$

The frequency dependence with control voltage is given by the derivative with respect to V_{IN} So,

$$\frac{d\ f_O}{d\ V_{IN}} = \frac{-1}{(V_{T+} - V_{T-})\ RC},$$

where the minus sign indicates that the output frequency increases as the input is brought further below the inverter threshold. The maximum output frequency occurs when V_{IN} is at ground and the frequency will decrease as V_{IN} is raised up and will finally stop oscillating at the inverter threshold, approximately 0.55 V_{CC}.

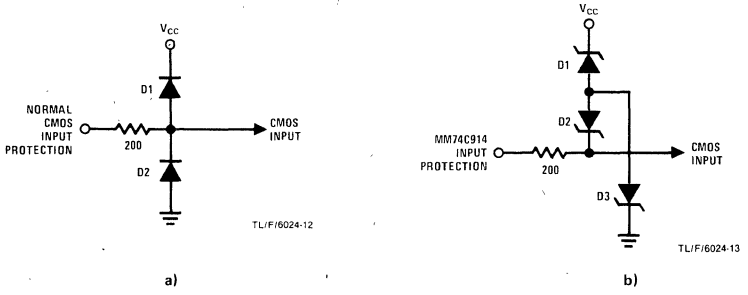


FIGURE 10. Input Protection Diodes, in a) Normally Limit the Input Voltage Swing to 0.3V above V_{CC} and 0.3V below Ground. In b) D2 or D1 is Reverse Biased Allowing Input Swings of 25V above Ground or 25V below V_{CC}.

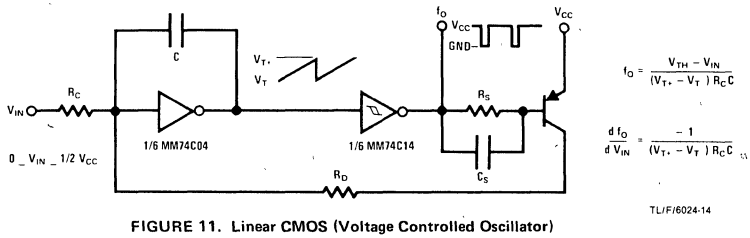


FIGURE 11. Linear CMOS (Voltage Controlled Oscillator)

The pulses from the VCO output are quite narrow because the reset time is much smaller than the integration time. Pulse stretching comes quite naturally to a Schmitt trigger. A one-shot or pulse stretcher made with an inverter and Schmitt trigger is shown in *Figure 12.* A positive pulse coming into the inverter causes its output to go low, discharging the capacitor through the diode D1. The capacitor is rapidly discharged, so the Schmitt input is brought low and the output goes positive. Check the size of the capacitor to make sure that inverter can fully discharge the capacitor in the input pulse time, or

$$I_{SINK\ INVERTER} > \frac{C\,\Delta V}{\Delta T} + \frac{\Delta V}{R}$$

where $\Delta V = V_{CC}$ for CMOS, and ΔT is the input pulse width.

For very narrow pulses, under 100 ns, the capacitor can be omitted and a large resistor will charge up the CMOS gate capacitance just like a capacitor.

When the inverter input returns to zero, the blocking diode prevents the inverter from charging the capacitor and the resistor must charge it from its supply. When the input voltage of the Schmitt reaches V_{T+}, the Schmitt output will go low sometime after the input pulse has gone low.

THE SCHMITT SOLUTION

The Schmitt trigger, built from discrete parts, is a careful and sometimes time-consuming design. When introduced in integrated TTL, a few years ago, many circuit designers had renewed interest because it was a building block part. The input characteristics of TTL often make biasing of the trigger input difficult. The outputs don't source as much as they sink, so multivibrators don't have 50% duty cycle, and a limited supply range hampers interfacing with non 5V parts.

The CMOS Schmitt has a very high input impedance with thresholds approximately symmetrical to one half the supply. A high voltage input is available. The outputs sink and source equal currents and pull directly to the supply rails.

A wide threshold range, wide supply range, high noise immunity, low power consumption, and low board space make the CMOS Schmitt a uniquely versatile part.

Use the Schmitt trigger for signal conditioning, restoration of levels, discriminating noisy signals, level detecting with hysteresis, level conversion between logic families, and many other useful functions.

The CMOS Schmitt is one step closer to making design limited only by the imagination of the designer.

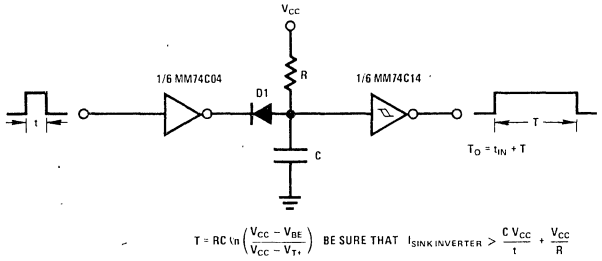


FIGURE 12. Pulse Stretcher. A CMOS Inverter Discharges a Capacitor, a Blocking Diode allows Charging through R only. Schmitt Trigger Output goes Low after the RC Delay.

Using National Clock Integrated Circuits in Timer Applications

National Semiconductor
Application Note 143
November 1975

INTRODUCTION

The following is a description of a technique which allows the use of the National MM5309; MM5311, MM5312 and MM5315 clock integrated circuits as timers in industrial and consumer applications. What will be presented is the basic technique along with some simple circuitry and applications.

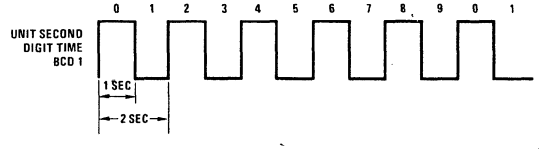
BASIC TECHNIQUE

When first approaching the problem of using clock chips for timers, the most obvious technique is to attempt to compare the display data with preset BCD numbers. Because of the multiplexing and number of data bits this technique, while possible, is unwieldy and requires a large number of components.

An easier method is to use one or more demultiplexed BCD lines as control waveforms whose edges determine timer data. In *Figure 1* we examine the 1-bit of the BCD data of the units second time.

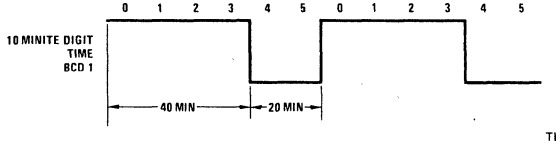
From this waveform we observe a one second wide pulse every two seconds. If we look at the 4-bit of the 10 minutes digit we find a pulse which is 20 minutes wide and occurs once each hour.

Figure 3 is a chart showing the various pulses and their widths for all digits and the useful BCD lines.



TL/D/7397-1

FIGURE 1. 1 Second Pulse Every 2 Seconds



TL/D/7397-2

FIGURE 2. 20 Minute Pulse Every Hour

BCD	PULSE RATE	PULSE WIDTH	BCD	PULSE RATE	PULSE WIDTH
	1 Sec Digit			10 Sec Digit	
1	1 every 2 sec	1 sec*	1	1 every 20 sec	10 sec*
2			2	1 every min	20 sec
4	1 every 10 sec	4 sec	4	1 every min	20 sec
8	1 every 10 sec	2 sec	8		
	1 Min Digit			10 Min Digit	
1	1 every 2 min	1 min*	1	1 every 20 min	10 min*
2			2	1 every hr	20 min
4	1 every 10 min	4 min	4	1 every hr	20 min
8	1 every 10 min	2 min	8		
	Units Hrs Digit (12 Hr Mode)			Units Hrs Digit (24 Hr Mode)	
1	1 every 2 hrs	1 hr*	1	1 every 2 hrs	1 hr*
2			2		
4	1 every 12 hrs	4 hrs	4		
8	1 every 12 hrs	4 hrs	8		
	10 Hrs Digit (12 Hr Mode)			10 Hrs Digit (24 Hr Mode)	
1			1	1 every 24 hrs	10 hrs
2	1 every 12 hrs	9 hrs	2	1 every 24 hrs	4 hrs
4	1 every 12 hrs	9 hrs			
8	1 every 12 hrs	9 hrs			

*Square waves

TL/D/7397-3

FIGURE 3

SIMPLE DEMULTIPLEXING

In the simple case where, for example, a four hour wide pulse each day is desired, perhaps to turn on lights in the evening, a simple demultiplexing scheme using one diode is shown in *Figure 4.* When power is applied, the internal multiplex circuitry will strobe each digit until the digit with the diode connected is accessed. This digit will sink the multiplex charging current and stop the multiplex scanning. Thus, the BCD outputs now present the data from the selected digit. The waveforms as previously discussed are presented at the BCD lines. Note that these pulses are negative true for all BCD outputs.

An advantage of this type of timer over mechanical types is the elimination of line power drop outs. The circuit shown in *Figure 5* will maintain timing to within a few percent during periods of power line failure, but automatically return to the 60 Hz line for timing as soon as power is restored.

MORE COMPLEX APPLICATIONS

Where it is desired to maintain the display, or in more complex timing of the "10 seconds every two hours" variety, external demultiplexing shown in *Figure 6* can be used. In this figure the BCD lines are demultiplexed with MM74C74 flip-flops. Examining the waveforms of these circuits we see two edges which allow the 10 second each two hours timing. These are differentiated by the NAND and INVERTERS and the first edge sets and the second resets the S-R flip-flop. The output of the flip-flop is ten seconds wide every two hours. By examining the edges of the *Figure 3* entries any combination of timings can be obtained with the circuit of *Figure 6.*

LOW FREQUENCY WAVEFORM GENERATION

The asterisked BCD lines in *Figure 3* are those waveforms which are symmetric. By the use of the simple diode demultiplexing scheme previously discussed we

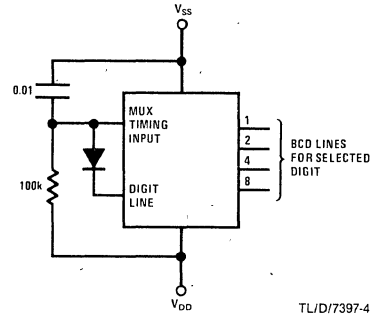


FIGURE 4

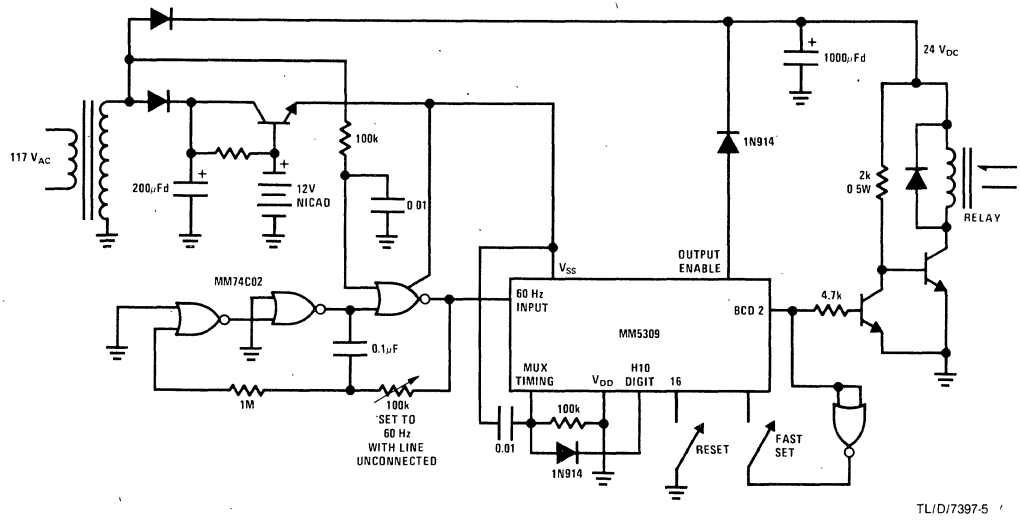


FIGURE 5. Fail-Safe Automatic Lights Timer. Four Hours Each 24 Hours

easily obtain square waves with periods of two seconds, two minutes, twenty minutes and two hours. In other cases, where the waveforms are asymmetric, a simple flip-flop can square, while dividing by two, these waveforms producing other low frequency square waves as long as one per two days.

SUMMARY

We have shown some simple low cost timer and waveform generating examples using National clock integrated circuits. Because of the vast number of timing applications possible, this can in no way be looked at as the limit of clock-timer circuits. Use of the Reset on the MM5309 and MM5315 or the use of clocks in conjunction with programmable counters such as the MM74C161 allows other possibilities to meet specific applications. Also the clock chips themselves can run on frequencies other than 50 or 60 Hz (actually from dc to 10 kHz) which can allow scaling of the waveforms presented in *Figure 3* to different timing rates.

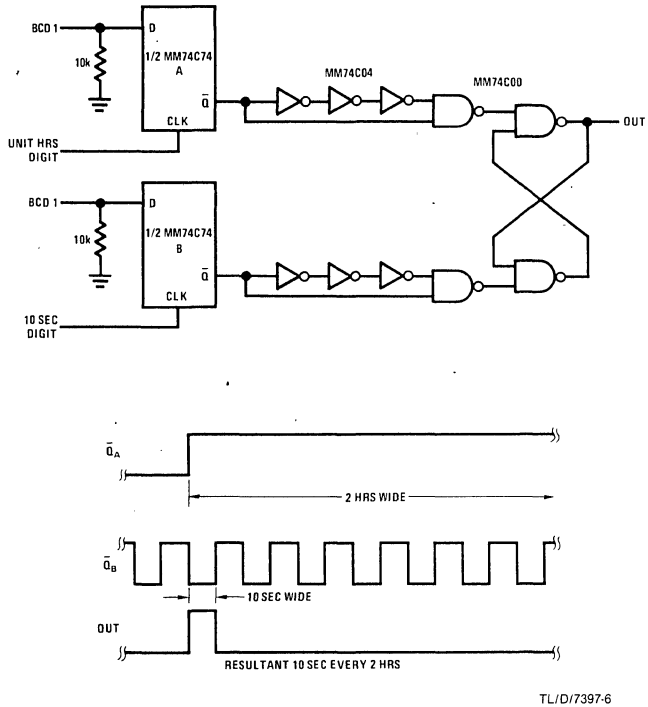


FIGURE 6. More Universal Demultiplexing Technique

Designing with MM74C908, MM74C918 Dual High Voltage CMOS Drivers

National Semiconductor
Application Note 177
Jen-yen Huang
March 1977

INTRODUCTION

By combining the merits of both CMOS and bipolar technologies on a single silicon chip, the MM74C908, MM74C918 provides the following distinguished features as general purpose high voltage drivers.

- Wide supply voltage range (3V to 18V)
- High noise immunity (typ 0.45 V_{CC})
- High input impedance (typ $10^{12}\Omega$)
- Extremely low standby power consumption (typ 750 nW at 15V)
- Low output "ON" resistance (typ 8Ω)
- High output drive capability ($I_{OUT} \geq 250$ mA at $V_{OUT} = V_{CC} - 3V$, and $T_j = 65^\circ C$)
- High output "OFF" voltage

Among these, the first 4 are typical and unique characteristics of CMOS technology which are fully utilized in this circuit to achieve all the design advantages in a typical CMOS system.

The high output currents and low "ON" resistance are achieved through the use of an NPN Darlington pair at the output stage.

The MM74C908 is housed in an 8-lead epoxy dual-in-line package, which can dissipate at least 1.14W. The higher power version, MM74C918, comes in a 14-lead epoxy dual-in-line package, with power capability up to a minimum of 2.27W.

The circuitry for each of the 2 identical sections is shown in *Figure 1*.

With both inputs sitting at logical "1" level, the output of the inverter is also at logical "1", which prevents the P-channel transistor from being turned "ON"; therefore, the output is in its "OFF" state. Only a small amount of leakage current can flow.

On the other hand, when one or both of the inputs is at logical "0" level, the output of the inverter is also at logical "0", which turns on the P-channel transistor and, hence, the Darlington pair.

POWER CONSIDERATION

To assure junction temperature of 150°C or less, the on-chip power consumption must be limited to within the power handling capability of the packages. In *Figure 2*, the maximum power dissipation on-chip is shown as a function of ambient temperature for both MM74C908 and MM74C918. These curves are generated from (1) at $T_j = T_{j(MAX)} = 150^\circ C$.

$$T_j = T_A + P_D \theta_{jA} \quad (1)$$

where T_j = junction temperature
T_A = ambient temperature
P_D = power dissipation
θ_{jA} = thermal resistance between junction and ambient

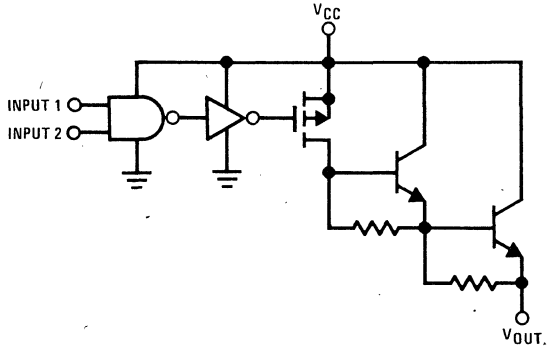


FIGURE 1 TL/F/6025-1

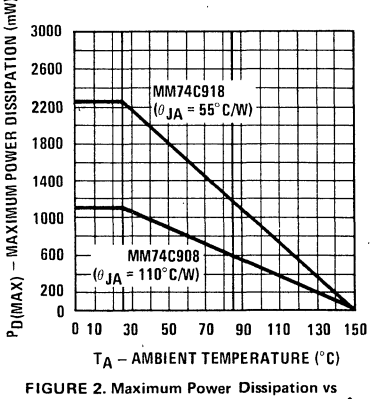
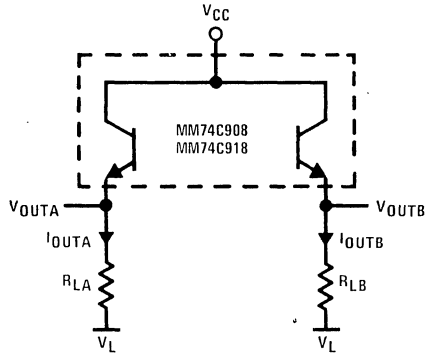


FIGURE 2. Maximum Power Dissipation vs Ambient Temperature

TL/F/6025-2

A general application circuit for the MM74C908, MM74C918 is as shown in *Figure 3*.



TL/F/6025-3

FIGURE 3

For both sections A and B;

$$I_{OUT} = \frac{V_{CC} - V_L}{R_{ON} + R_L} \quad (2)$$

The device "ON" resistance, R_{ON}, is a function of junction temperature, T_j. The worst-case R_{ON} as a function of T_j is given in (3).

$$R_{ON} = 9\,[1 + 0.008\,(T_j - 25)] \quad (3)$$

The total power dissipation in the device also consists of normal CMOS power terms (due to leakage current, internal capacitance, switching etc.) which are insignificant compared to the power dissipated at the output stages. Thus, the output power term defines the allowable limits of operation and is given by:

$$P_D = P_{DA} + P_{DB} = I^2_{OUTA} \cdot R_{ON} + I^2_{OUTB} \cdot R_{ON} \quad (4)$$

Given R_{LA} and R_{LB}, (1), (2), (3), (4) can be used to calculate P_D, T_j, etc. through iteration.

For example, let $V_L = 0V$, $V_{CC} = 10V$, $R_{LA} = 100\Omega$, $R_{LB} = 50\Omega$, $T_A = 25°C$, $\theta_{jA} = 110°C/W$.

Assume:

$R_{ON} = 12.28\Omega$

By (2):

$$I_{OUTA} = \frac{10}{12.28 + 100} = 0.089A$$

$$I_{OUTB} = \frac{10}{12.28 + 50} = 0.161A$$

By (4):

$$P_D = (0.089)^2 \cdot 12.28 + (0.161)^2 \cdot 12.28 = 0.41W$$

By (1):

$T_j = 70.5°C$

And by (3):

$R_{ON} = 12.28\Omega$

DESIGN TECHNIQUE

In a typical design, R_L must be chosen to satisfy the load requirement (e.g., a minimum current to turn on a relay) and at the same time, the power consumed in the driver package must be kept below its maximum power handling capability.

To minimize the design effort, a graphical technique is developed, which combines all the parameters in one plot, which can be used efficiently to obtain an optimal design.

Assume $T_A = 25°C$ and that both sections of the MM74C908 in *Figure 3* are operating under identical conditions. The maximum allowable package dissipation is:

$$P_D = 2\,(V_{CC} - V_{OUT}) \times I_{OUT} = \frac{1}{110}\,(150 - T_A) = 1.14W \quad (6)$$

where $T_j = 150°C$, $\theta_{jA} = 110°C/W$ are used in (1) per the data sheet.

Thus, the maximum power allowed in each section is:

$$P_D = (V_{CC} - V_{OUT}) \times I_{OUT} = 0.57W$$

A constant power curve $P_D = 0.57W$ can then be plotted as shown in *Figure 4*. The circuit must operate below this curve. Any voltage-current combination beyond it (in the shaded region) will not guarantee T_j to be lower than 150°C.

For any given R_L, a load line (7) can be superimposed on *Figure 4*.

$$I_{OUT} = \frac{1}{R_L}\,(V_{CC} - V_L) - \frac{1}{R_L}\,(V_{CC} - V_{OUT}) \quad (7)$$

The slope of this load line is $-1/R_L$ and it intersects with the vertical and horizontal axes at $1/R_L\,(V_{CC} - V_L)$ and $V_{CC} - V_L$ respectively.

Given V_{CC} and V_L, a minimum R_L can be obtained by drawing the load line tangent to the constant power curve. In *Figure 4*, at $V_{CC} - V_L = 5V$ the line intersects I_{OUT} axis at $I_{OUT} = 450$ mA. Thus, $R_{L(MIN)} = 5V/450$ mA $= 11.1\Omega$. Any R_L value below this will move the intersecting point up and cause a section of the load line to extend into the shaded region. Therefore, the junction temperature can exceed $T_{j(MAX)} = 150°C$ in the worst case if the circuit operates on such a section of the load line.

Whether this situation will occur or not is determined by both the value of $V_{CC} - V_L$ and the R_{ON} range of the drivers.

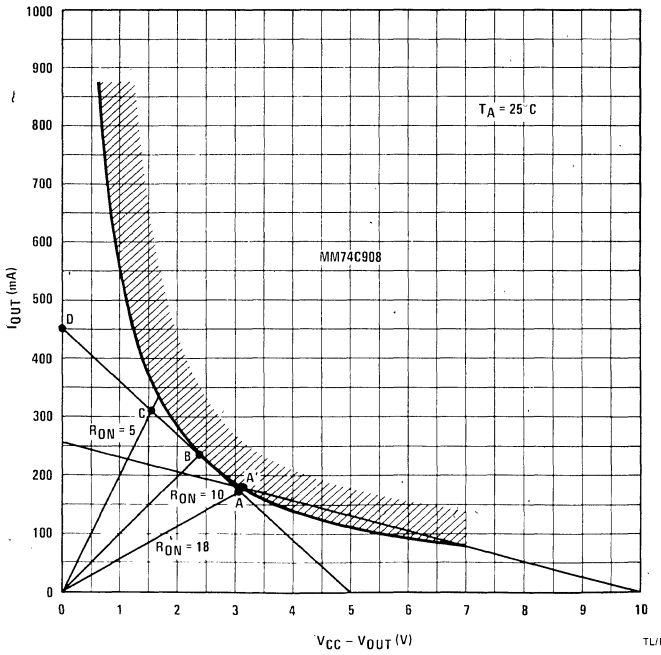


FIGURE 4

By (3), at $T_j = 150°C$ $R_{ON(MAX)} = 18\Omega$, this is a straight line* passing through the origin with a slope of $I_{OUT}/(V_{CC} - V_{OUT}) = 1/18$ mho and intersects the load line at point A. Similarly, point B and C can be found for typical (~10Ω) and minimum (~5Ω) R_{ON} at $T_j = 150°C$.

For $V_{CC} - V_L = 5V$, the tangent point falls between A and C. Hence, $R_L \geq 11.1\Omega$ calculated above must be satisfied; otherwise, part of the load line within the specified R_{ON} range will extend into the shaded region and therefore, $T_j \geq 150°C$ may occur.

For $V_{CC} - V_L = 10V$, however, a section of the load line can go beyond the $P_D = 0.57W$ curve without affecting the safe operation of the circuit. By inspection of *Figure 4*, the reason is clear—the load line extends into the shaded region only outside of the specified R_{ON} range (to the right of point A'). Within the R_{ON} range, the load line lies below the $P_D = 0.57W$ curve, thus, a safe operation.

To a first approximation**, the section of the load line between A and C is the operating range for the circuit at $V_{CC} - V_L = 5V$ and $R_L = 11.1\Omega$. Hence, the available current and voltage ranges for this circuit are $310\ mA \geq I_{OUT} \geq 172\ mA$ and $3.4V \geq V_{OUT} \geq 1.9V$, respectively.

Thus, by simply drawing no more than 3 straight lines, one obtains all of the following immediately:

1. All the necessary design information (e.g., minimum R_L, minimum available I_{OUT} and V_{OUT}, etc.)
2. Operating characteristics of the circuit as a whole, including the effect of different R_{ON} values due to process variations, thus, a better insight into the circuit operation.
3. Most importantly, a guarantee that the circuit will be operating in the safe region, $(T_j \leq 150°C)$.

For different ambient temperatures or for different power considerations, *Figure 4* can be applied by properly scaling the I_{OUT} axis. (Note that $I_{OUT} \propto T_j - T_A$ and $I_{OUT} \propto P_D$).

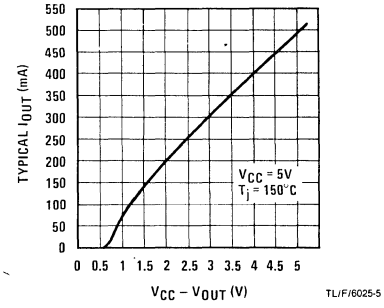


FIGURE 5. Typical I_{OUT} vs Typical V_{OUT}

*Strictly speaking, R_{ON} is a non-linear function of I_{OUT}. A typical R_{ON} characteristic at $T_j = 150°C$ is shown in *Figure 5*. The non-linear characteristic near the origin is due to the fact that the output NPN transistor is not saturated. As soon as saturation is reached ($I_{OUT} \sim 150$ mA) the curve becomes a straight line which extrapolates back to the origin. For practical design purposes, it is sufficient to consider R_{ON} as a linear function of I_{OUT}.

**Note that as the operating point on the load line moves away from the $P_D = 0.57W$ curve, (away from the tangent point in this case), the actual junction temperature drops. Therefore, at point A, for example, the device is actually running cooler than $T_j = 150°C$, even in the worst case. Hence, R_{ON} value drops below 18Ω and the actual operating point is slightly different from A.

To further simplify the design, a family of such curves has been generated as shown in *Figure 6*. Each of these curves corresponds to a particular T_A and P_D (per driver) as indicated, and similar to the P_D = 0.57W curve in *Figure 4*, is generated from (6) by using appropriate T_A values. The application of these curves is illustrated as follows:

Example 1

1. In *Figure 3*, assume that the two drivers in the MM74C908 package are to operate under identical conditions. Find minimum R_L at T_A = 25°C, 45°C, 65°C and 85°C for both $V_{CC} - V_L$ = 5V and $V_{CC} - V_L$ = 10V.

   Then plot $R_{L(MIN)}$ vs T_A.

   a) $V_{CC} - V_L$ = 5V

   By constructing the load lines tangent to the curves for T_A = 25°C, 45°C, 65°C and 85°C, $R_{L(MIN)}$ for each case can be obtained through the vertical coordinate for the intersection points as shown in *Figure 6*. These are calculated in Table I.

   Note that the same results (within graphical error) can be obtained analytically by letting $dR_L/dR_{ON} = 0$. It can be shown that

$$R_{L(MIN)} = \frac{(V_{CC} - V_L)^2}{4X\ (\text{Max Power Per Driver})} \qquad (8)$$

   b) $V_{CC} - V_L$ = 10V

   The $R_{L(MIN)}$ given in (8) may not be a true minimum if the tangent point does not fall inside the specified R_{ON} region. The actual $R_{L(MIN)}$ can be obtained as shown in *Figure 7*. The calculations and results are given in Table II.

   Note that the $R_{L(MIN)}$ values in Table II are lower than those given by (8). This corresponds to the section on each of the 4 load lines in *Figure 7* which extends beyond the power limit curve at each associated temperature. However, this section on each load line is outside the specified R_{ON} range. Within the R_{ON} range, load lines are below the power limits; therefore, safe operation is guaranteed.

   The $R_{L(MIN)}$ vs T_A plot is as shown in *Figure 8*.

   All the curves generated so far are restricted to $P_D \leq 0.57W$ due to our simplifying assumption that both drivers are operating identically. In *Figure 9* a few more curves are added to account for the general situation in which only the restriction $P_{DA} + P_{DB} \leq 1.14W$ is required, (i.e., P_{DA} can be different from P_{DB}). Application of *Figure 9* is illustrated as follows:

TABLE I

T_A	25°C	45°C	65°C	85°C
I_{OUT} @ D1, 2, 3, 4 (mA)	450	375	310	240
$R_{L(MIN)} = \frac{5}{I_{OUT} @ D1, 2, 3, 4}$ (Ω)	11.1	13.3	16.1	20.8

TABLE II

T_A	25°C	45°C	65°C	85°C
I_{OUT} @ D1, 2, 3, 4 (mA)	261	230	197	166
$R_{L(MIN)} = \frac{10}{I_{OUT} @ D1, 2, 3, 4}$ (Ω)	38.3	43.5	50.8	60.2

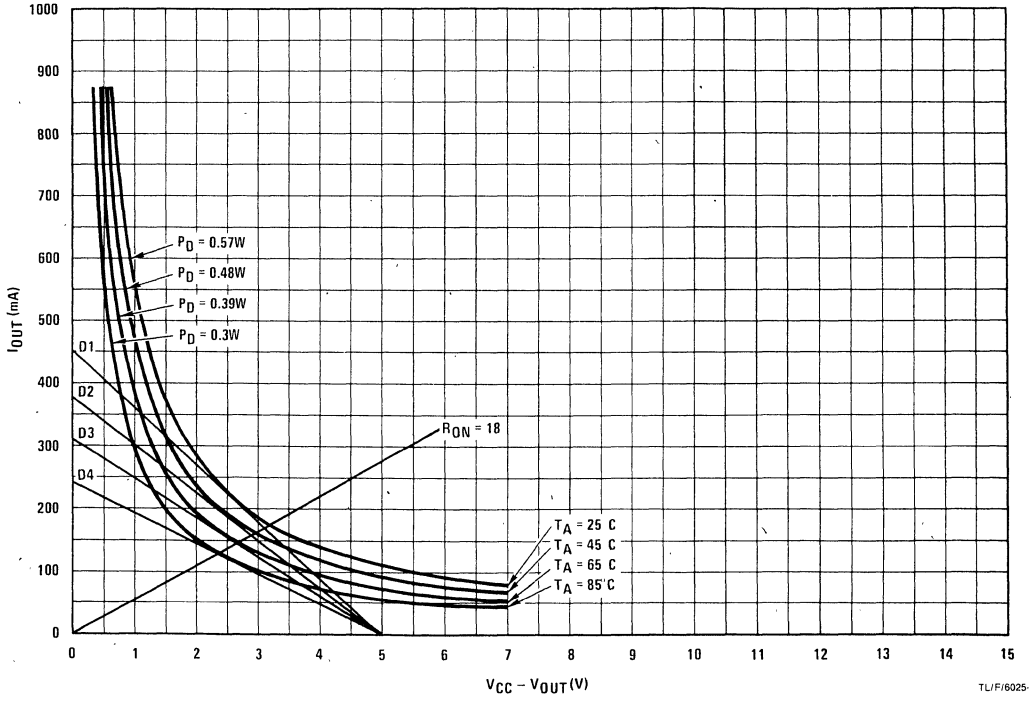


FIGURE 6

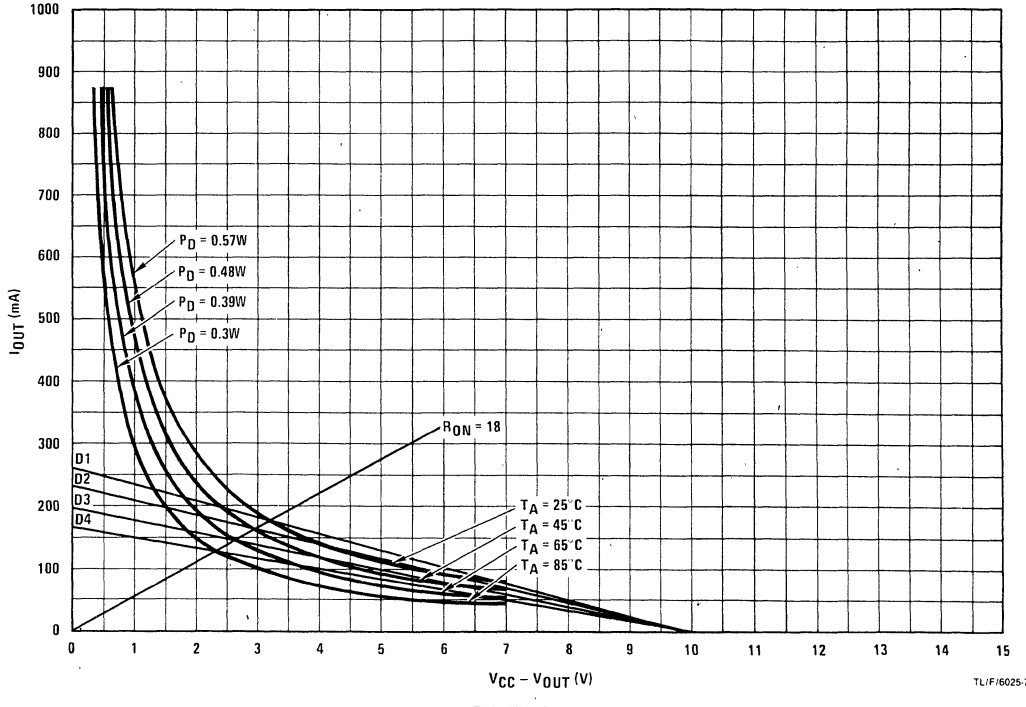


FIGURE 7

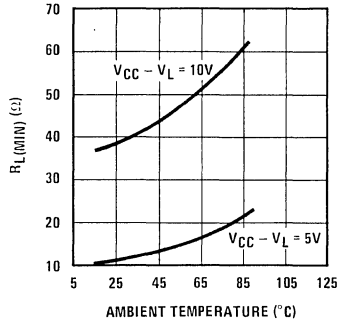


FIGURE 8

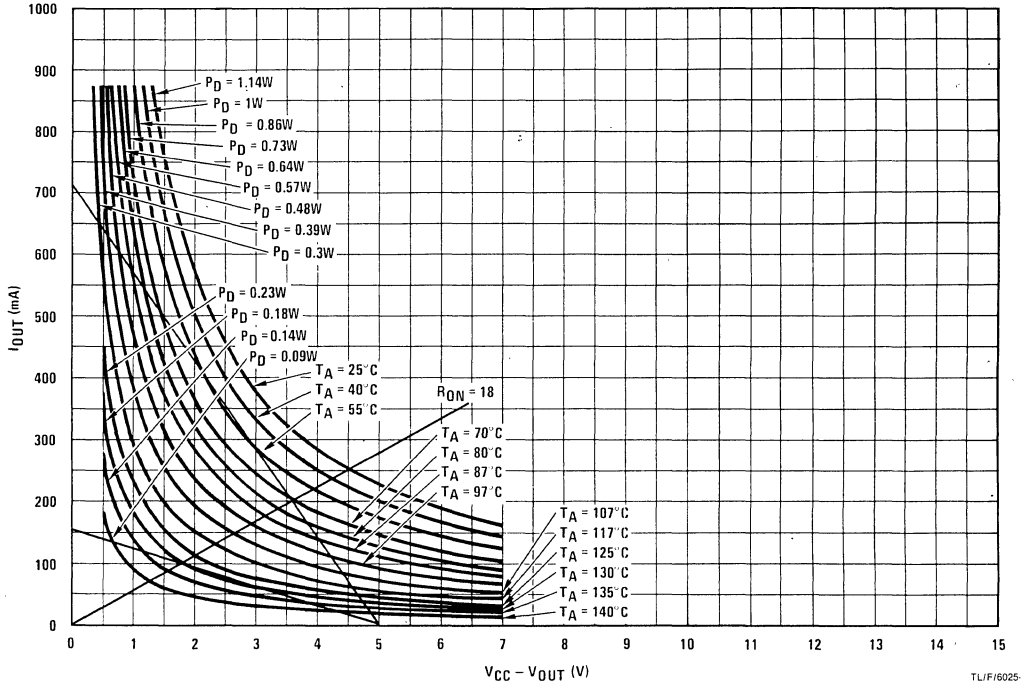


FIGURE 9

Example 2

In *Figure 3*, assume that driver A has to deliver 200 mA to its load while driver B needs only 100 mA. Design R_{LA} and R_{LB} for $V_{CC} - V_L = 5V$.

By inspection of *Figure 4*, units with high R_{ON} values will not be able to deliver 200 mA. However, since section B does not need the same amount of drive, we can reduce the power consumed in this section to compensate for the higher power ($> 0.57W$) required in section A.

The design procedure follows:

Section A

1. Draw a load line intersecting $R_{ON} = 18\Omega$ line at $I_{OUT} = 200$ mA.
2. This load line intersects the I_{OUT} axis at $I_{OUT} = 710$ mA and is tangent to $P_{DA} \simeq 0.9W$ curve, thus $R_{LA} \cong 5V/710\ mA = 7.1\Omega$ will guarantee both $P_{DA} \leq 0.9W$ and $I_{OUTA} \geq 200$ mA.

Section B

1. Draw a load line intersecting $R_{ON} = 18\Omega$ line at $I_{OUT} = 100$ mA.
2. Similar to (2) above, it is seen immediately that $R_{LB} \cong 5V/150\ mA = 33.3\Omega$ will guarantee $I_{OUTB} \geq 100$ mA and $P_{DB} \leq 0.18W$.

Since $P_{DA} + P_{DB} \leq 0.9 + 0.18 < 1.14W$

$R_{LA} = 7.1\Omega$
$R_{LB} = 33.3\Omega$

satisfy all the requirements in this problem.

The design in Example 2 illustrated the simple and straight-forward use of the curves and the result meets all the problem requirements. However, it should be noted that there is not much design margin left for tolerance in resistances and other circuit parameters. The reason is obvious—we are pushing at the power limit of the MM74C908 package—and the solutions are simple:

a) Increase V_{CC} supply
b) Use the higher power package MM74C918.

The design for higher V_{CC} is identical to that in Example 2 and will not be repeated here.

For the 14-lead higher power (2.27W) MM74C918, $\theta_{jA} = 55°C/W$, this is exactly half that of the 8-lead MM74C908. Therefore, by scaling the I_{OUT} axis by a factor of 2, the same family of curves in *Figure 9* can be applied directly. This is shown in *Figure 10*. (Note that the slope of the $R_{ON} = 18\Omega$ line has been adjusted to the new scale).

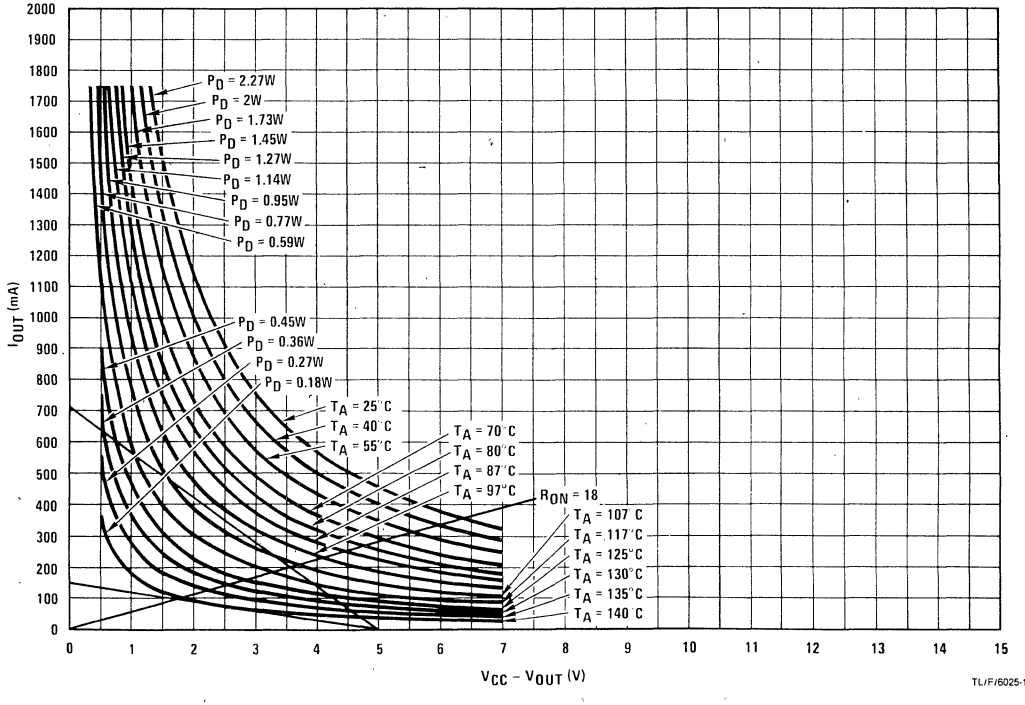


FIGURE 10

By drawing the same load lines, it is found that:

$R_{LA} \cong 5V/710\ mA = 7.1\Omega$
guarantees $P_{DA} \leq 0.9W$

and

$R_{LB} \cong 5V/150\ mA = 33.3\Omega$
guarantees $P_{DB} \leq 0.18W$

$P_{DA} + P_{DB} \leq 1.08W$

which is way below the maximum power 2.27W available. Therefore, both R_{LA} and R_{LB} can be lowered to account for tolerance in the resistors. Consider specifically the following example:

Example 3

Assume driver A, B of the MM74C918 have to deliver 250 mA and 150 mA, respectively, to its load. Design R_{LA} and R_{LB} at $V_{CC} - V_L = 10V$.

Driver A

1. In *Figure 11*, draw the load line intersecting $R_{ON} = 18\Omega$ at $I_{OUT} = 250$ mA.
2. This load line intersects the I_{OUT} axis at 450 mA. Thus, by inspection $R_{LA} \cong 10V/450\ mA \cong 22.2\Omega$ guarantees $P_{DA} \leq 1.14W$.

Driver B

1. Draw the load line intersecting $R_{ON} = 18\Omega$ at $I_{OUT} = 150$ mA.
2. This load line intersects the I_{OUT} axis at 210 mA. Thus, by inspection $R_{LB} \cong 10V/210\ mA = 47.6\Omega$ guarantees $P_{DB} \leq 0.4W$.

Since $P_{DA} + P_{DB} \leq 1.14 + 0.4 = 1.8W$, while the package is capable of delivering 2.27W, both R_{LA} and R_{LB} can be lower than the above values and the circuit still operates safely. By picking the closest standard resistance values:

$R_{LA} = 20\Omega$
$R_{LB} = 43\Omega$

For 5% tolerance in these values,

$19\Omega \leq R_{LA} \leq 21\Omega$
$40.85\Omega \leq R_{LB} \leq 45.15\Omega$

Thus:

$$I_{OUTA(MIN)} \geq \frac{10V}{18\Omega + 21\Omega} = 256.4\ mA > 250\ mA$$

$$I_{OUTB(MIN)} \geq \frac{10V}{18\Omega + 45.15\Omega} = 158.3\ mA > 150\ mA$$

$$P_{DA(MAX)} \leq \left(\frac{10V}{18\Omega + 19\Omega}\right)^2 \cdot 18\Omega = 1.31W$$

$$P_{DB(MAX)} \leq \left(\frac{10V}{18\Omega + 40.85\Omega}\right)^2 \cdot 18\Omega = 9.52W$$

$P_{DA(MAX)} + P_{DB(MAX)} \leq 1.31 + 0.52 < 2.27W$

Therefore:

$R_{LA} = 20\Omega$ (1.5W, 5%)
$R_{LB} = 43\Omega$ (1W, 5%)

will guarantee satisfactory performance of the circuit.

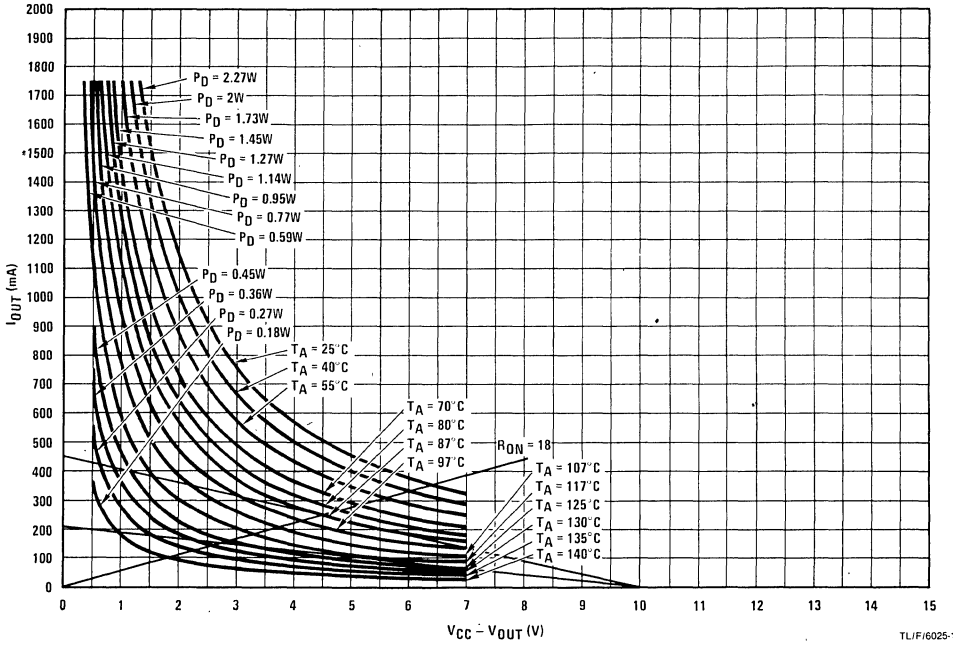


FIGURE 11

APPLICATIONS

Like most other drivers, the MM74C908, MM74C918 can be used to drive relays, lamps, speakers, etc. These are shown in *Figure 12*. (To suppress transient spikes at turn-off, a diode as shown as *Figure 12a* is recommended at the relay coil or any other inductive load.)

However, the MM74C908, MM74C918 offers a unique CMOS feature that is not available in drivers from other logic families—extremely low standby power. At V_{CC} = 15V, power dissipation per package is typically 750 nW when the outputs are not drawing current. Thus, the drivers can be sitting out on line (a telephone line, for example) drawing essentially zero current until activated—an ideal feature for many applications.

The dual feature and the NAND function of the driver design can also be used to advantage as shown in the following applications:

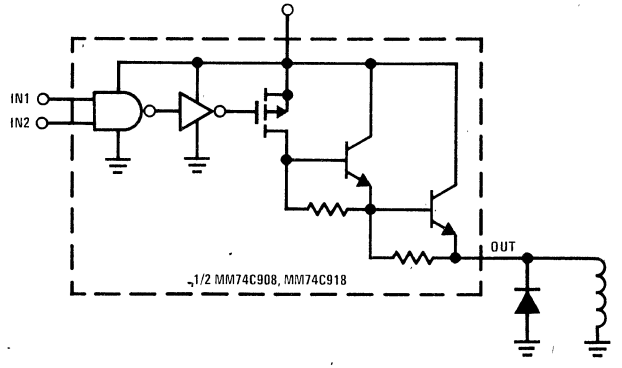


FIGURE 12a. Relay Driver

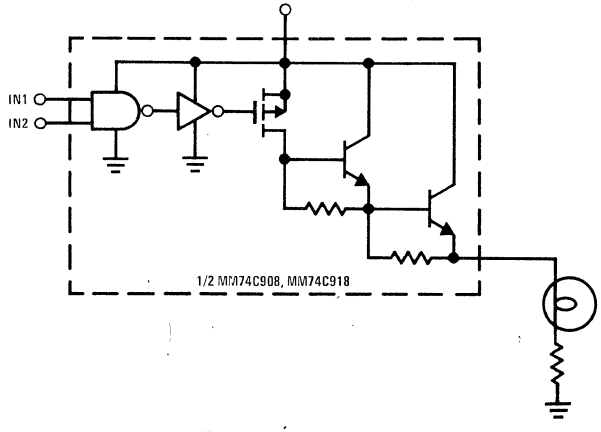


FIGURE 12b. Lamp Driver

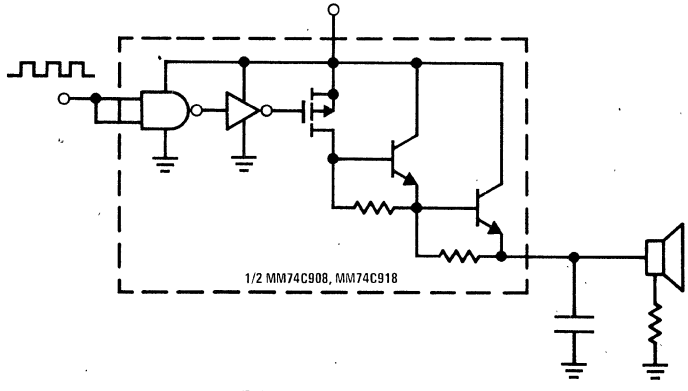


FIGURE 12c. Speaker Driver

In *Figure 13*, the 2 drivers in the package are connected as a Schmitt trigger oscillator, where R1 and R2 are used to generate hysteresis. R3 and C are the inverting feedback timing elements and R4 is the pull-down load for the first driver. Because of its current capability, the circuit can be used to drive an array of LEDs or lamps. If resistor R4 is replaced by an LED (plus a current limiting resistor), the circuit becomes a double flasher with the 2 LEDs flashing out of phase. This is shown in *Figure 14*.

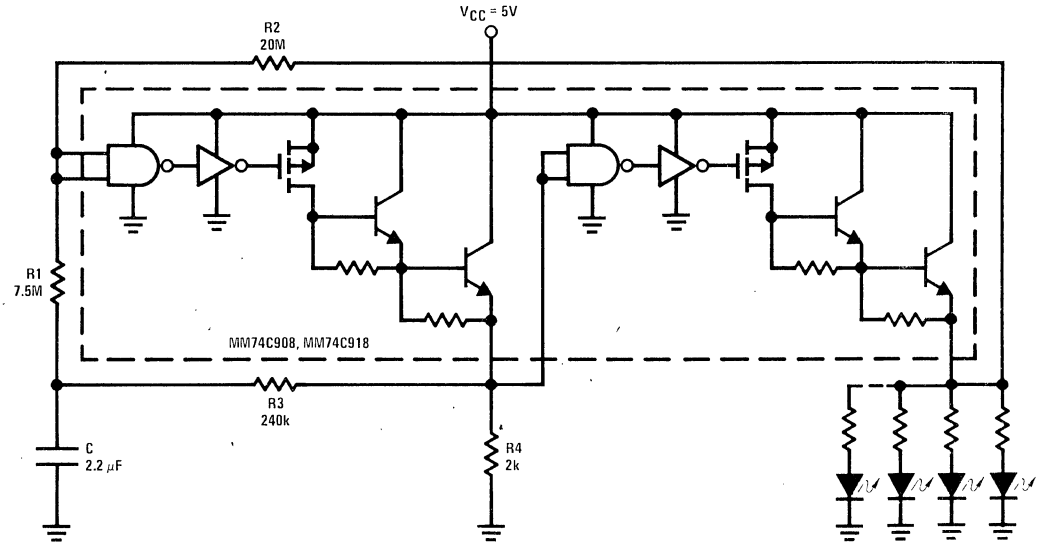


FIGURE 13. High Drive Oscillator/Flasher

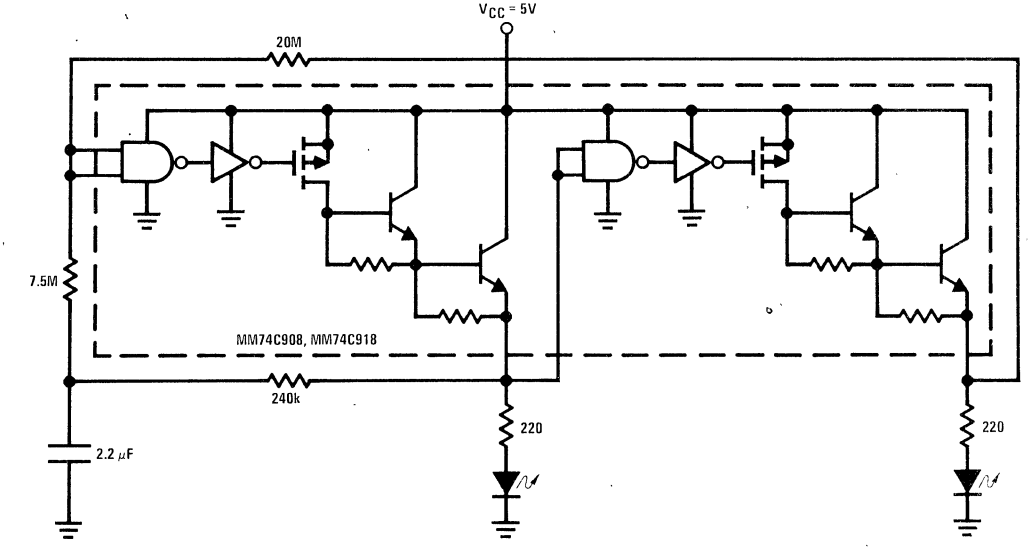


FIGURE 14. Out of Phase Double Flasher

Another oscillator circuit using only 1/2 of the package and 4 passive components is shown in *Figure 15*. Assume V_I is slightly below the input trip point, the driver is "ON" and charging both V_O and V_I until V_I reaches the trip point, V_T, when the driver starts to turn "OFF". V_O can be made much higher than V_I at this instance by adjusting the component values such that $R_fC_f >> (R_{ON}||R_L)C_L$. Since V_O is higher than V_I, V_I is still going up, although the driver is "OFF" and V_O is ramping down. The rising V_I will eventually equal to the falling V_O, and then start discharging. Then, both V_I and V_O discharge until V_I hits the trip point, V_T, again, when the driver is turned "ON", charging up V_O and subsequently V_I to complete a cycle.

This oscillator is ideal for low cost applications like the 1-package siren shown in *Figure 16*, where 1 oscillator is used as a VCO while the other is generating the voltage ramp to vary the frequency at the VCO output.

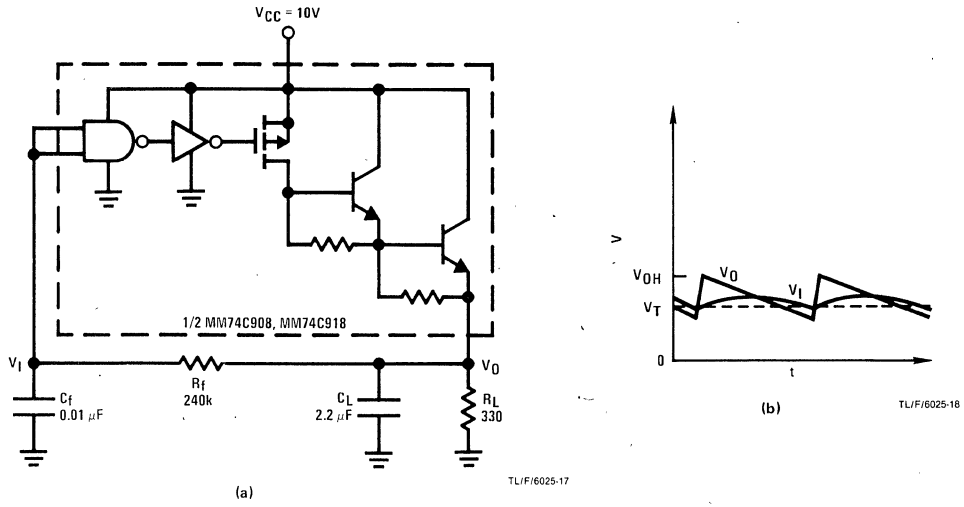


FIGURE 15. Single Driver Oscillator

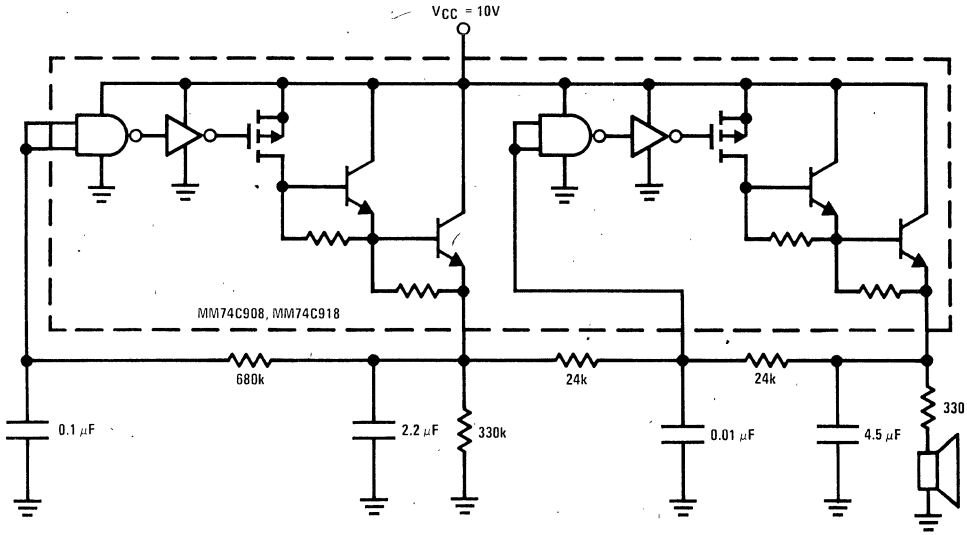


FIGURE 16. Low Cost Siren

TL/F/6025-19

The NAND functions at the input can also be used to reduce package count in applications where both high output drive and input NAND features are required. One such example is given in *Figure 17*.

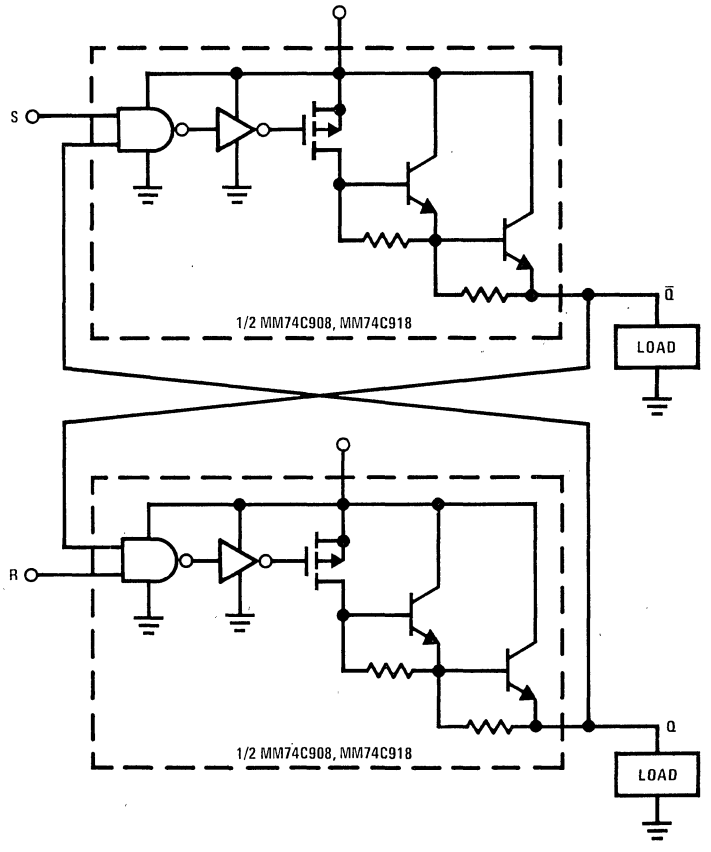


FIGURE 17. High Drive RS Latch

Electrostatic Discharge Prevention — Input Protection Circuits and Handling Guide for CMOS Devices

National Semiconductor
Application Note 248
Vivek Kulkarni
June 1980

Introduction

During the past few years, there have been significant increase in the usage of low-power CMOS devices in system designs. This has resulted in more stringent attention to handling techniques of these devices, due to their static sensitivity, than ever before.

All CMOS devices, which are composed of complementary pairs of n- and p-channel MOSFETs, are susceptible to damage by the discharge of electrostatic energy between any two pins. This sensitivity to static charge is due to the fact that gate input capacitance (5 picofarads typical) in parallel with an extremely high input resistance (10^{12} ohms typical) lends itself to a high input impedance and hence readily builds up the electrostatic charges, unless proper precautionary measures are taken. This voltage build-up on the gate can easily break down the thin (1000 Å) gate oxide insulator beneath the gate metal. Local defects such as pinholes or lattice defects of gate oxide can substantially reduce the dielectric strength from a breakdown field of $8\text{–}10 \times 10^6$V/cm to $3\text{–}4 \times 10^6$V/cm. This then becomes the limiting factor on how much voltage can be applied safely to the gates of CMOS devices.

When a higher voltage, resulting from a static discharge, is applied to the device, permanent damage like a short to substrate, V_{DD} pin, V_{SS} pin, or output can occur. Now static electricity is always present in any manufacturing environment. It is generated whenever two different materials are rubbed together. A person walking across a production floor can generate a charge of thousands of volts. A person working at a bench, sliding around on a stool or rubbing his arms on the work bench can develop a high static potential. Table I shows the results of work done by Speakman[1] on various static potentials developed in a common environment. The ambient relative humidity, of course, has a great effect on the amount of static charge developed, as moisture tends to provide a leakage path to ground and helps reduce the static charge accumulation.

TABLE I. Various Voltages Generated in 15%–30% Relative Humidity (after Speakman[1])

Condition	Most Common Reading (Volts)	Highest Reading (Volts)
Person walking across carpet	12,000	39,000
Person walking across vinyl floor	4,000	13,000
Person working at bench	500	3,000
16-lead DIPs in plastic box	3,500	12,000
16-lead DIPs in plastic shipping tube	500	3,000

Standard Input Protection Networks

In order to protect the gate oxide against moderate levels of electrostatic discharge, protective networks are provided on all National CMOS devices, as described below.

Figure 1 shows the standard protection circuit used on all A, B, and 74C series CMOS devices. The series resistance of 200 ohms using a P^+ diffusion helps limit the current when the input is subjected to a high-voltage zap. Associated with this resistance is a distributed diode network to V_{DD} which protects against positive transients. An additional diode to V_{SS} helps to shunt negative surges by forward conduction. Development work is currently being done at National on various other input protection schemes.

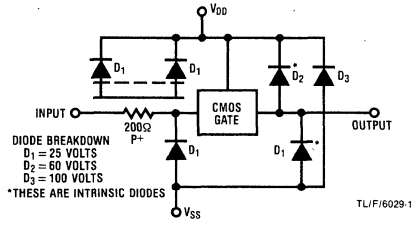


Figure 1. Standard Input Protection Network

Other Protective Networks

Figure 2 shows the modified protective network for CD4049/4050 buffer. The input diode to V_{DD} is deleted here so that level shifting can be achieved where inputs are higher than V_{DD}.

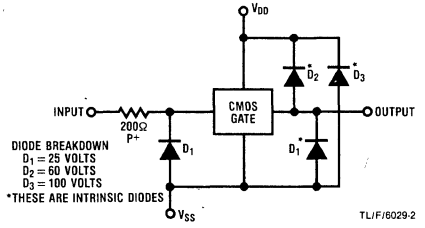


Figure 2. Protective Network for CD4049/50 and MM74C901/2

Figure 3 shows a transmission gate with the intrinsic diode protection. No additional series resistors are used so the on resistance of the transmission gate is not affected.

All CMOS circuits from National's CD4000 Series and 74C Series meet MIL-STD-38510 zap test requirements of 400 volts from a 100 pF charging capacitor and 1.5 kΩ series resistance. This human body simulated model of

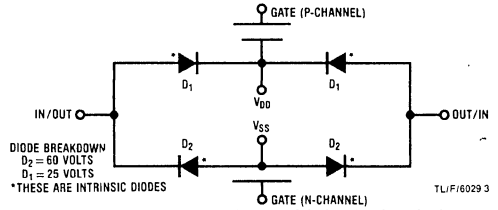


Figure 3. Transmission Gate with Intrinsic Diodes to Protect Against Static Discharge

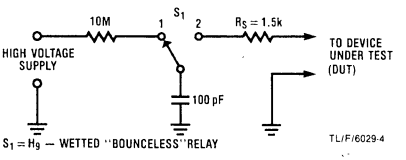


Figure 4. Equivalent RC Network to Simulate Human Body Static Discharge (After Lenzlinger[2])

100 pF capacitance in series with 1.5 kΩ series resistance was proposed by Lenzlinger[2] and has been widely accepted by the industry. The set-up used to perform the zap test is shown in Figure 4.

V_{ZAP} is applied to DUT in the following modes by charging the 100 pF capacitor to V_{ZAP} with the switch S_1 in position 1 and then switching to position 2, thus discharging the charge through 1.5 kΩ series resistance into the device under test. Table II shows the various modes used for testing.

TABLE II. Modes of High-Voltage Test

Mode	+Terminal	−Terminal
1	Input	V_{SS}
2	V_{DD}	Input
3	Input	Associated Output
4	Associated Output	Input

Pre- and post-zap performance is monitored on the input leakage parameter at $V_{DD} = 18$ Volts. It has been found that all National's CMOS devices of CD4000 and 74C families can withstand 400 volts zap testing with above mentioned conditions and still be under the pre- and post-zap input leakage conditions of ±10 nA.

Handling Guide for CMOS Devices

From Table I, it is apparent that extremely high static voltages generated in a manufacturing environment can destroy even the optimally protected devices by reaching their threshold failure energy levels. For preventing such catastrophies, simple precautions taken could save thousands of dollars for both the manufacturer and the user.

In handling unmounted chips, care should be taken to avoid differences in voltage potential between pins. Conductive carriers such as conductive foams or conductive rails should be used in transporting devices. The following simple precautions should also be observed.

1. Soldering-iron tips, metal parts of fixtures and tools, and handling facilities should be grounded.
2. Devices should not be inserted into or removed from circuits with the power on because transient voltages may cause permanent damage.
3. Table tops should be covered with grounded conductive tops. Also test areas should have conductive floor mats.

Above all, there should be static awareness amongst all personnel involved who handle CMOS devices or the sub-assembly boards. Automated feed mechanisms for testing of devices, for example, must be insulated from the device under test at the point where devices are connected to the test set. This is necessary as the transport path of devices can generate very high levels of static electricity due to continuous sliding of devices. Proper grounding of equipment or presence of ionized-air blowers can eliminate all these problems.

At National all CMOS devices are handled using all the precautions described above. The devices are also transported in anti-static rails or conductive foams. Anti-static, by definition[3] means a container which resists generation of triboelectric charge (frictionally generated) as the device is inserted into, removed from, or allowed to slide around in it. It must be emphasized here that packaging problems will not be solved merely by using anti-static rails or containers as they do not necessarily shield devices from external static fields, such as those generated by a charged person. Commercially available static shielding bags, such as 3M company's low resistivity ($\leq 10^4$ ohms/sq.) metallic coated polyester bags, will help prevent damages due to external stray fields. These bags work on the well-known Faraday cage principle. Other commercially available materials are Legge company's conductive wrist straps, conductive floor coating, and various other grounding straps which help prevent against the electrostatic damage by providing conductive paths for the generated charge and equipotential surfaces.

It can be concluded that electrostatic discharge prevention is achievable with simple awareness and careful handling of CMOS devices. This will mean wide and useful applications of CMOS in system designs.

Footnotes

1. T.S. Speakman, "A Model for the Failure of Bipolar Silicon Integrated Circuits Subjected to ESD," 12th Annual Proc. of Reliability Physics, 1974.
2. M. Lenzlinger, "Gate Protection of MIS Devices," IEEE Transac. on Electron Devices, ED-18, No. 4, April 1971.
3. J.R. Huntsman, D.M. Yenni, G. Mueller, "Fundamental Requirements for Static Protective Containers." Presented at 1980 Nepcon/West Conference, Application Note — 3M Static Control Systems.

MM54240 Asynchronous Receiver/Transmitter Remote Controller Applications

National Semiconductor
Application Note 249
J. Hong
May 1980

Introduction

The MM5420 Asynchronous Receiver/Transmitter Remote Controller is a low cost, easy-to-use circuit for serial data transmission applications. The circuit is fabricated in the N-channel metal gate process which gives it a wide supply voltage range (V_{DD} = 4.75V–11.50V) and TTL compatibility.

A typical application would consist of an information handling center and up to 128 information gathering and information supplying stations. The information handling center would be composed of one MM54240 circuit interfaced to a microprocessor I/O system. The MM54240 in this instance is called the "master" circuit. An information gathering and supplying station would be one MM54240 interfaced to a A-to-D converter/D-to-A converter system or a digital peripheral system or any information source/destination. The MM54240 in this instance is the "slave" circuit.

The simplest way to interface such a system is by means of a twisted pair or a coaxial cable. A pull-up resistor is necessary on this communication line since the circuit drivers are open drain outputs. Care should be taken to reduce capacitance and resistance on this line. With the use of pulse width modulation techniques, frequency tolerance between the circuits is broadened. This feature is extremely desirable since the need for an expensive crystal controlled oscillator or ceramic resonator is eliminated. Furthermore, critical timing schemes with start and stop bits are not used. In addition, a debounce circuit is incorporated which contributes greatly to the noise immunity feature of the circuit.

Circuit Description

A functional block diagram of the MM54240 is shown in Figure 2. The Control Logic section consists of the switching functions of the circuit. The PWM encoder/decoder encodes and decodes the pulse width modulation data format. The Shift Registers store and shift the data.

Temperature Control and Security Application

The MM54240 can be used in many different types of low to medium speed processor controlled applications. For a system with 128 "slave" circuits, the time that it takes to interrogate all "slave" circuits can range from 1 to 2.5 seconds depending on the oscillator frequency of each individual circuit.

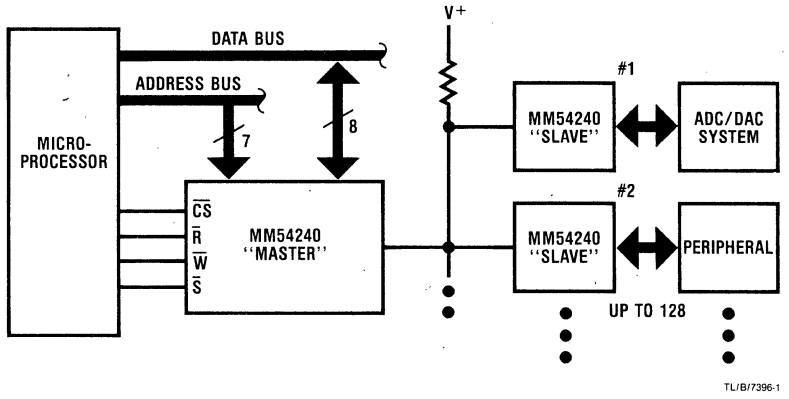


Figure 1. Typical System Block Diagram

The following example illustrates a possible in-the home use of such a system. A set of MM54240 circuits are used for controlling the temperature of the various rooms inside the house, the security of the windows and entrances, and also for turning the lights on and off when certain events take place. The processor controlling the system is a COP421L and it is directly interfaced to the MM54240 "master" circuit. Three address inputs of the "master" circuit are not used and they are tied directly to the power supply. A maximum of 16 "slave" circuits are then possible. They will start with address 112 and go up to 127. The "master" circuit has the Data I/O ports interfaced to the L I/O ports, the Address inputs interfaced to the D I/O ports, and the Control inputs interfaced to the G output ports of the COP421L. The Mode input is tied to V_{DD} to select "master" operation and the only external components are the R-C's connected to each circuit. The power supply terminals are shared between the two circuits.

The heating system of the house consists of a furnace with a multi-speed air blower. A thermocouple thermometer installed in each room supplies the temperature information to the processor. The amount of air flowing into a room is controlled by a variable ventilation grating. When the temperature of the room falls, the ventilator opens further to let in increasing amounts of warm air. When all the rooms are sufficiently heated, the furnace is turned off. The temperature in different rooms may not be the same since the processor can control and adjust them to a programmed setting.

The first "slave" circuit has hard-wired address 112 and it is used for furnace control. The control (C_1, C_2) inputs are set up for (0,1) the low impedance output port selection. D_1 of the D outputs is used for furnace ignition. The other D outputs are used for controlling the air blower's variable speed. The second "slave" circuit has hard-wired address 113 and it is used for temperature sensing and ventilation opening control. The control (C_1, C_2) inputs are set up for (0,0) 4 in/4 out selection. D_1-D_4 are low impedance output ports for controlling the ventilator opening; D_5-D_8 are high impedance input ports for receiving temperature information from the thermocouple.

The third "slave" circuit has hard-wired address 114 and it is used for security purposes. The control (C_1, C_2) inputs are set up for (1,0) the weak pull-up option. The processor will have to initialize the output latches by loading logic ones into them. The D_6 I/O port is for Arming and Disarming the alarms. This is accomplished by a locking switch shorting the I/O port to V_{SS} when armed. The D_1-D_5 I/O ports are connected to doors and windows. When they are shut, the I/O ports are shorted to V_{SS}. When a window or door is opened, the voltage level of that I/O port will increase. When the COP421L processor detects this change, it will enable the alarm at the D_8 I/O port and turn the light on at the D_7 I/O port. The processor can also be programmed to turn the light — D_7 I/O port — on when one or certain doors are open.

The second and third "slave" circuit configurations can be duplicated for other rooms. Each "slave" circuit has an optional clear switch in case the processor circuit fails and the "slave" circuit outputs have to be overridden.

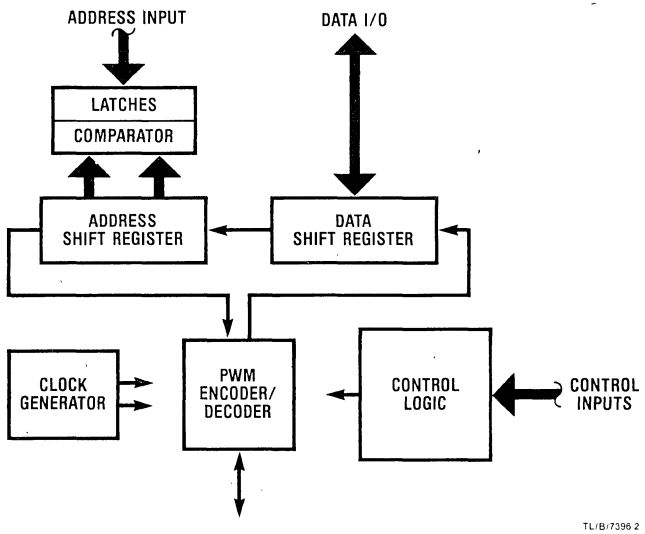


Figure 2. Circuit Functional Block Diagram

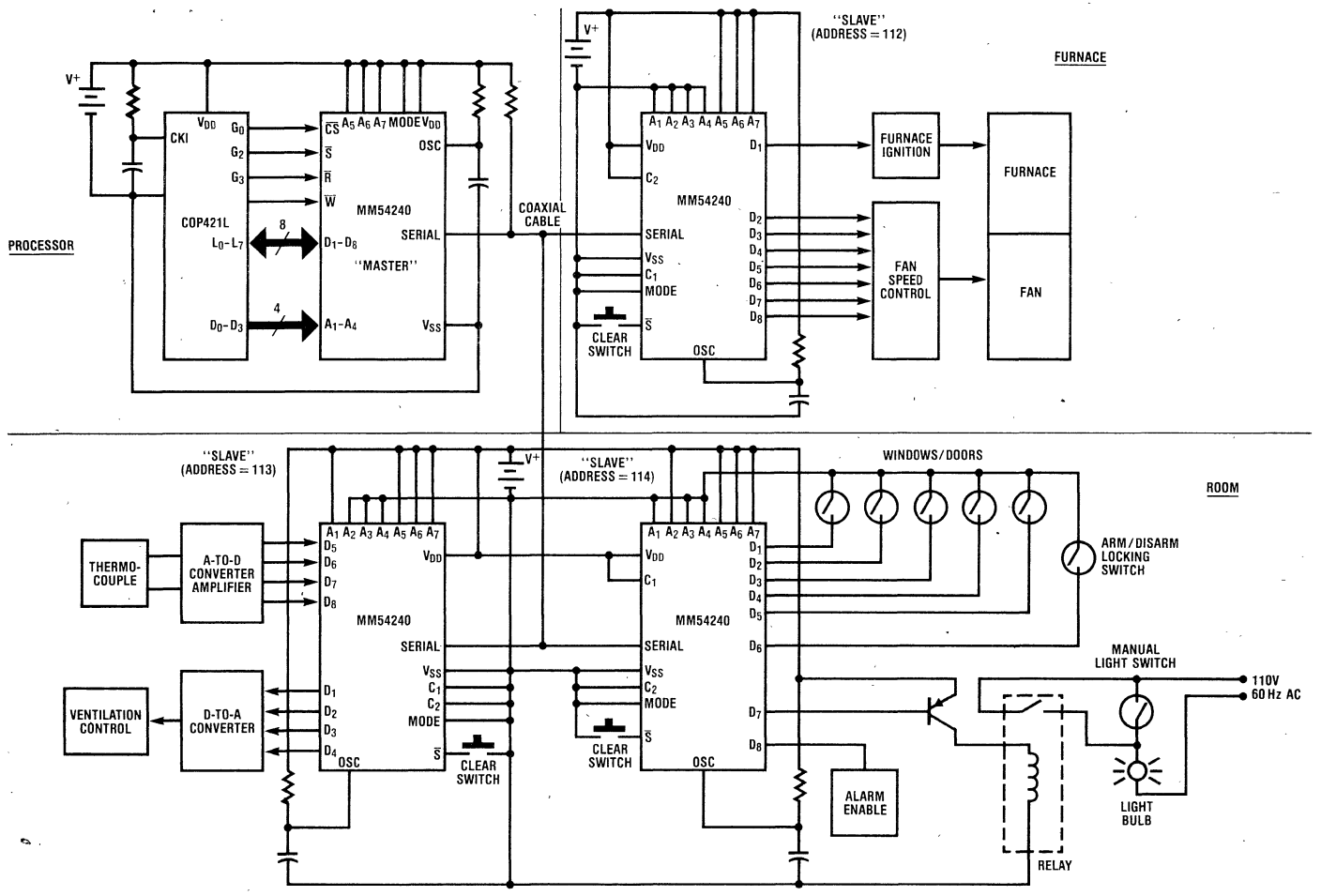


Figure 3. Temperature Control and Security Application

Power Line Transmission

A MM54240 system can be interfaced using other techniques. The pulse width modulated information can be transmitted by carriers like Radio Frequency, infra-red waves, power line transmission or any other suitable medium. For power line transmission applications, an interfacing circuit is used to modulate the information on the 60 Hz AC lines. For the "master" circuit, the processor must generate a signal to control the direction of transmission of the interface circuit. For the "slave" circuit, the chip select ($\overline{CS}$) output is designed for this purpose and can be used directly to control the direction of transmission of the interface circuit.

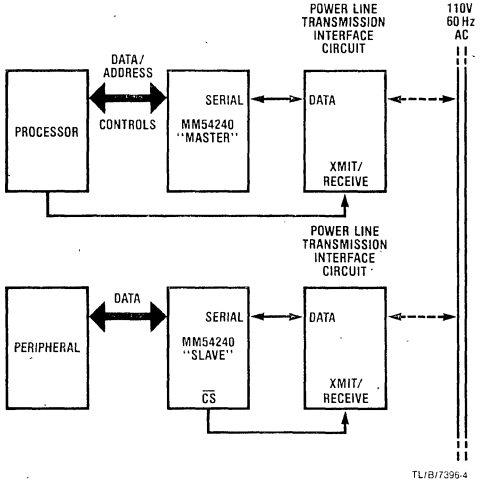


Figure 4. Power Line Transmission Application

Radio Frequency Transmission

A Radio Frequency transmission system can be built in a similar structure. An I/O multiplexing circuit has to be designed to direct the flow of the transmitted data.

Conclusion

The MM54240 is a flexible, easy-to-use, and adaptable circuit. It can be used in any application where a serial data transmission is desired. The transmitted data is pulse width modulated. This gives it desirable features such as a low cost oscillator, wide frequency tolerance, and excellent noise immunity. Up to 129 MM54240 circuits can be used for any one system. The circuit is fabricated in the N-channel metal gate process. Designed with National's Microbus™ structure in mind, the circuit is easily and directly interfaced to most microprocessor systems.

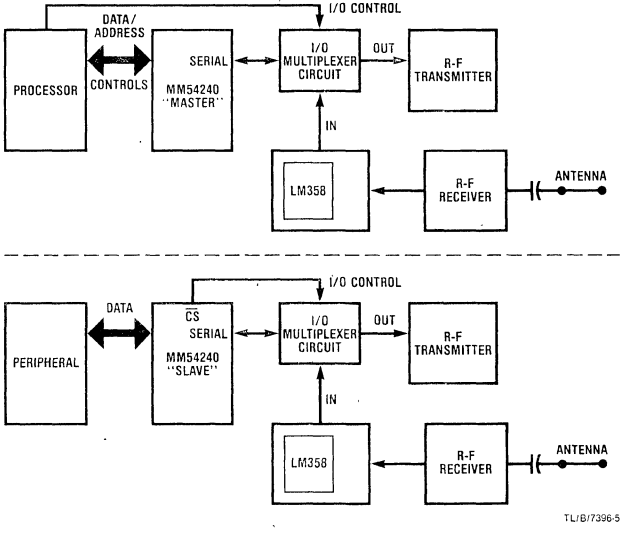


Figure 5. Radio Frequency Transmission Application

Applications and Uses of the MM5321 TV Camera Sync Generator

National Semiconductor
Application Note 250
Edwin Schoell
May 1980

1. Introduction

The MM5321 has been introduced to replace the older MM5320 and correct some difficulties associated with that part. It is a plug-in replacement in almost all applications.

Major Differences and Improvements are:

- Horizontal reset control allows resetting to beginning or center of horizontal line.
- Vertical (field) index pulse with both 1.26 and 2.045 MHz clock.
- Improved clocking characteristics.
- Vertical interval always generated after vertical reset pulse at pin 5.
- Vertical sync separator included.

Power Supplies

The MM5321 is designed to operate from a total supply voltage of 17 volts, or various combinations to supply a total of 17 volts. Interfacing to TTL or CMOS is best accomplished using +5V and −12V as shown in Figure 1. Note that no ground is needed for the MM5321, but it is used as the power return for peripheral chips.

Input Interfacing

Since the MM5321 is a P-channel device, input switching thresholds are with respect to the most positive (V_{SS}) power supply voltage. For this reason, it is important to use the same regulators, or insure the 5V supply to the driver chip is the same as the 5V supply to the MM5321. Problems with poor clocking can often be traced to drive levels not coming to within 1.5 volts of the 5V supply to the MM5321. In some cases, the addition of a 470Ω pull-up resistor from clock input to V_{SS} will solve the problem.

Input clocking problems have also been found with low duty cycle waveforms of the 2.048 MHz clock. A look at the data sheet will reveal that a 50 percent duty cycle is best, but 3 to 4 on/off (43%-57%) ratio is satisfactory. This can be obtained from a properly configured divide by seven counter from a 14.31818 MHz clock.

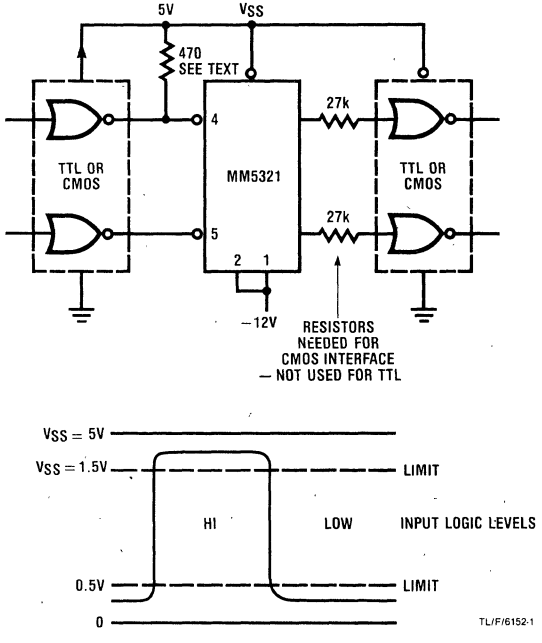


Figure 1. Input/Output Interfacing

Two schemes for driving the MM5321 are shown in Figure 2. The first shows a CMOS gate oscillator/buffer, while the second uses a transistor crystal oscillator and a TTL up-counter programmed to divide by seven and produce a 3 to 4 on/off ratio for the MM5321 clock input. In color applications the 14.32 MHz is also divided by four in a shift register type of counter to produce quadrature 3.58 MHz for the systems chroma modulators.

All other inputs should be tied high or low depending on the application of the part, with the exception of the horizontal reset, which is internally pulled down to V_{GG}.

Output Interfacing

The MM5321 will drive 1 TTL load when operated with +5V and −12V supplies as shown in Figure 1. The output structure is an active device to V_{SS} and a current source load to V_{DD}, Figure 3. When interfacing to CMOS, a 27 kΩ current limit resistor must be used to prevent damage to the CMOS inputs when the protection diode is turned "on".

2. Some Applications

The most basic application of the MM5321 is a TV camera sync generator, where it will generate all the usual drive signals as well as high quality composite sync. In this application, little interfacing is needed.

Genlocking

In some systems, it is necessary to lock the sync generator to another source of sync. This is commonly done by a process called "genlocking" in which the two generators are either fed from the same master (2.045 MHz) clock, or the crystal oscillator of one generator is phase-locked to vertical or horizontal sync of the master generator.

The vertical divider may be reset either by feeding composite sync to the vertical reset control, or by feeding differentiated (short pulses) of vertical sync to the vertical reset pin of the MM5321.

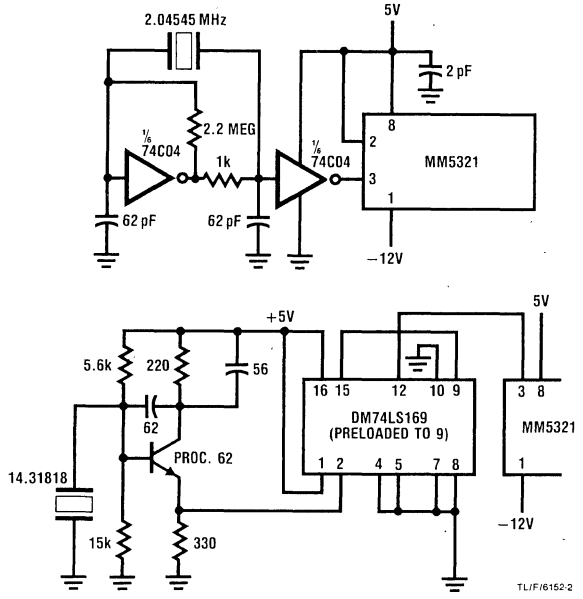


Figure 2. Input Clock Generating Schemes

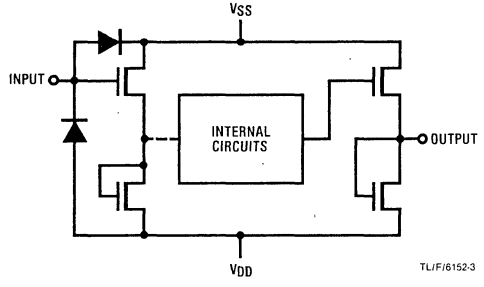


Figure 3. MM5321 Input/Output Circuits

Figure 4 shows a genlock application. External horizontal sync is used as a reference to a phase detector which compares to the horizontal sync generated by the MM5321. The error signal controls the clock to the MM5321. In order to insure exact horizontal and vertical timing, external composite sync is fed to the Vertical Reset Control of the MM5321. Circuitry inside the MM5321 decodes the vertical interval of the external sync generating a vertical sync pulse to reset the vertical counter of the MM5321. In effect then, this input acts as a vertical sync separator.

A disadvantage of this approach is that there is a one field delay between the source and the MM5321, so that serration pulses of the slave will begin one half line earlier than that of the source.

A more precise genlock application is shown in Figure 5. Phase locking is done at 3.58 MHz, vertical is reset with the leading edge of a vertical sync pulse derived from incoming video with the vertical control of the MM5321 resetting to the eleventh half line of generated sync. Composite sync resets the horizontal divider chain for clock periods before horizontal sync resulting in a μs delay between master and slave. Horizontal drive may be used to reset the horizontal counter to within one clock period or 0.5μs of master sync. In order not to produce double frequency horizontal drive during the vertical interval, horizontal sync from the master is gated with vertical drive from the slave.

It should be noted in the above application that if the phase lock were omitted, and the 2.048 MHz OSC were allowed to free run, the MM5321 would still maintain vertical and horizontal lock with the source. However, timing errors will build up with time and since the counters in the MM5321 can only be reset in 1 divided by 2.045 MHz or 500 ns intervals, the effect will be to shift the position of horizontal sync 500 ns (1% of 1 horizontal line) every few lines depending on how far apart the two clock sources are.

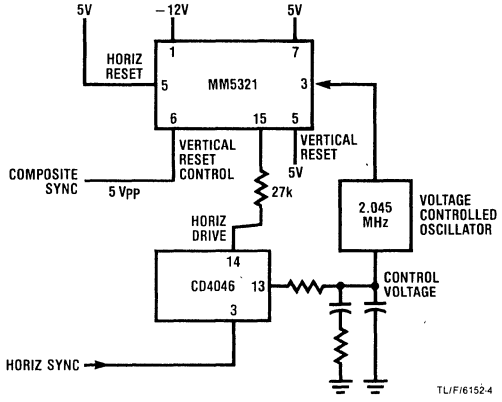


Figure 4. Genlocking

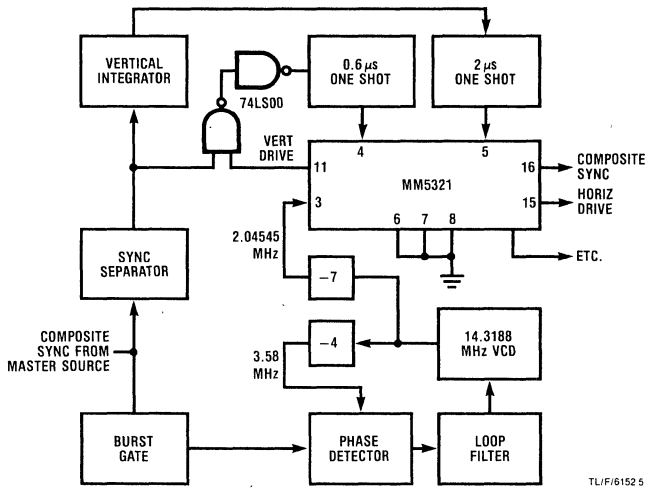


Figure 5. Genlocking with Color-Burst Phaselock

As an example, assuming a 0.1% error in clock frequency, after 1000 clock cycles, the error between clocks will be 1 clock cycle or 489 ns and the horizontal counter will reset one line earlier. 1000 clock cycles occur in 489 μs, or once every 7.7 horizontal lines.

The effect will be a sawtooth appearance on a vertical line displayed on a display.

3. PAL and Other Non-Standard Applications

The MM5321 may be used with some external circuitry to generate approximately correct PAL sync. By using the vertical control on the even line after 50 Horizontal lines are counted, the divide by 525 is reset to 5½ lines from zero. The field reference is slightly reduced to give horizontal rate of 50 Hz. It can be seen that for 819 lines, 147 and 152 extra pulses are needed.

Figure 6 shows a realizable circuit, the MM5321 provides all the necessary wave forms as in the 525 lines case. A divide by two provides odd and even field identification. A programmable counter is toggled at half field rate between the counts of 50 and 55; The MM5321 is reset at these times, the combinational logic around the 74C93 is toggled to detect alternately the 10th and 11th counts.

The ensure reliable reset of the 74C93 counter an extra delay was provided by a 74C14 inverter. The vertical drive sets an R-S flip flop at 0 time. The divide by 10/divide by 11 counter is enabled to count five, ten, or eleven pulses, the R-S flip flop is reset by the output of the divide by 5 counter.

The circuit now awaits the next vertical blanking pulse.

Specifications

Line Period	64 μs
Line Blanketing	11.2 μs
Front Porch	1.6 μs
Horizontal Pulse	4.8 μs
Back Porch	4.8 μs
Burst	2.4 μs
Field	50 Hz/312 = 313
Duration of Field Sequence	91 H
Field Blank. Int.	21 H lines
No. of Serrations	6

In conclusion it can be seen that this sync generator does not exactly conform with CCIR specs. However, there should be a few applications where these waveforms would be ample.

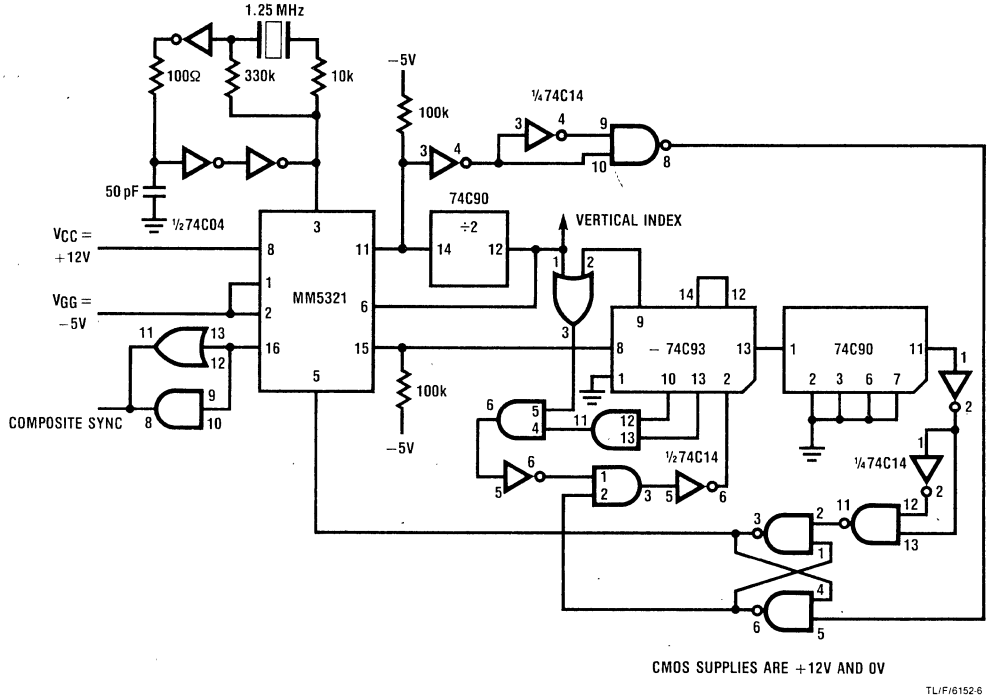


Figure 6. PAL Application

A Broadcast Quality TV Sync Generator Made Economical through LSI

National Semiconductor
Application Note 251
Robert B. Johnson and
Eugene H. Campbell
May 1980

The growing number of applications of video tape recorders and TV cameras in the consumer market have resulted in the need for a single-chip LSI integrated circuit TV camera sync generator. The National Semiconductor MM5321 TV Camera Sync Generator has been developed to economically provide the basic sync functions for color and monochrome, 525 line, 60 Hz, interlaced applications — and provide it with the reliability and accuracy of a digital IC system. A Metal-Oxide-Semiconductor (MOS) technology was chosen as the most economical method of obtaining the necessary circuit density and speed.

Figure 1 shows the simplified block diagram and Figures 2 through 5 are the timing diagrams of the generator.

All inputs and outputs of the 14-pin device are TTL compatible without the use of external components. Two supplies are required, with the nominal difference between them 17 volts. Ambient temperature may be varied between −25°C and +70°C.

The output functions provided are Horizontal Drive, Vertical Drive, Composite Blanking, Composite Sync, and Color Burst Gate. In addition, a Field Index output function identifies a particular field, and a Color Burst Sync output presents a pulse at half the horizontal rate, but otherwise identical to the Color Burst Gate, and may be used to synchronize the color burst with the generator.

All output functions are derived from the clock applied to the Master Clock input. The user may select either of two input frequencies by selecting the proper horizontal divider, which is accomplished by hard-wiring the Divider Control pin to either the V_{SS} (most positive) or V_{GG} (most negative) power supply.

In color applications, a frequency four times the color burst is usually available to generate the 0°C and 90°C color sub-carrier signals. Dividing that frequency by seven results in 2.04545 MHz, which is the input clock signal to be used when the Divider Control pin is connected to V_{SS}. With the control pin wired to V_{GG}, the horizontal divider is programmed to accept an input signal eighty times the horizontal rate, or 1.260 MHz.

The horizontal divider is essentially a 65-bit shift register which can be shortened to 40-bits with the Divider Control logic. Control logic also selects the proper set of register taps used for decoding the horizontal timing edges.

One of the outputs of the horizontal divider is a signal used to drive the ten-stage vertical counter and a 42-bit shift register, which together provide the verical division and timing edges.

Shift registers are usually very efficient logic blocks in MOS designs, which is why they were selected for many of the counters in this product. Parasitic capacitances may be used to store charge for periods of time that are

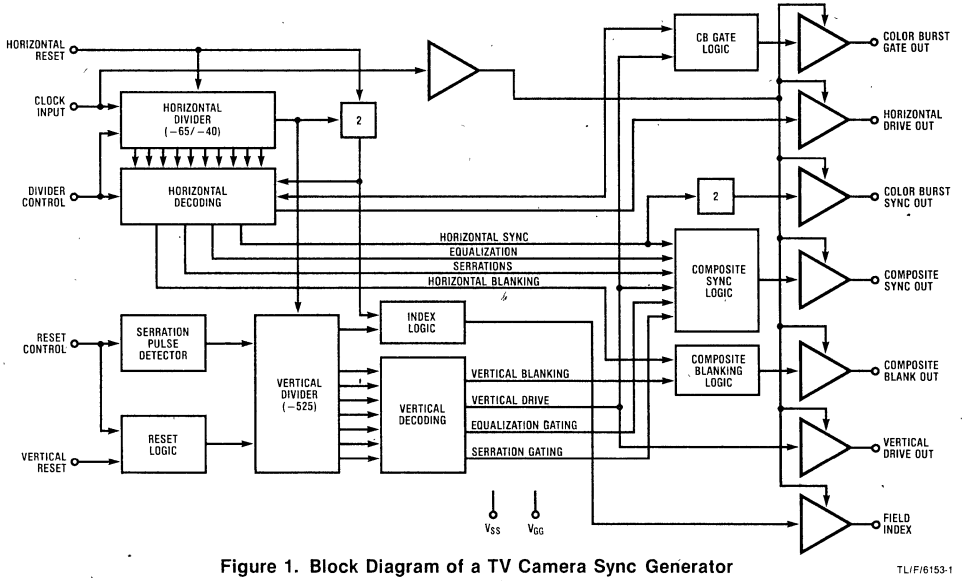


Figure 1. Block Diagram of a TV Camera Sync Generator Fabricated with MOS/LSI Techniques

essentially dependent only on semiconductor junction characteristics. Thus, in MOS it is possible to design both dynamic and static shift registers. Dynamic registers were used for both the vertical and horizontal counters because in each case the clock frequency is well above any minimum limitation due to leakage current considerations, and they offer a layout/size advantage over static type cells. The configuration selected uses ten transistors and is capable of being reset to either a "1" or "0" logic state.

The vertical divider is comprised of DC flip-flops configured as a ten-stage short-cycled, modulus 525, ripple counter. Each stage is resettable, and to accommodate additional vertical reset versatility, stages 1, 2, and 8 can be set or reset.

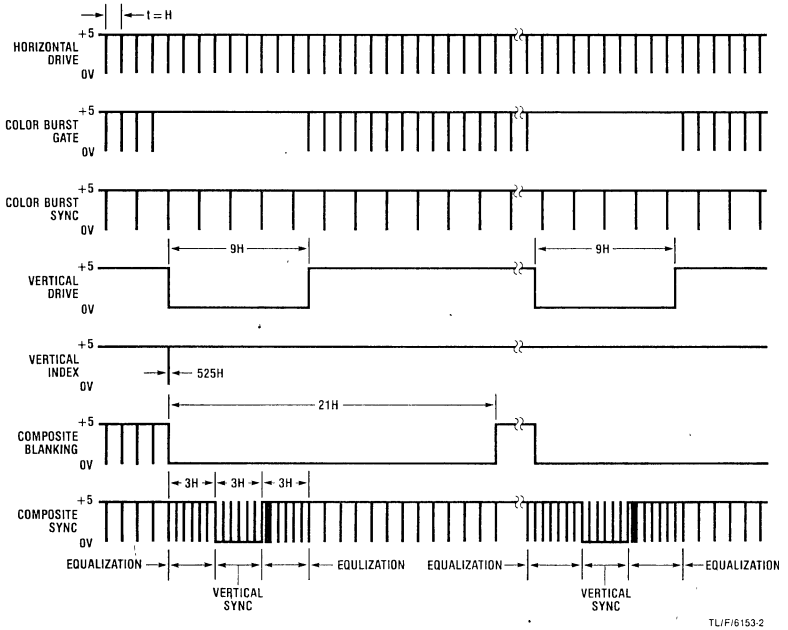


Figure 2. Sync Generator Output Waveforms

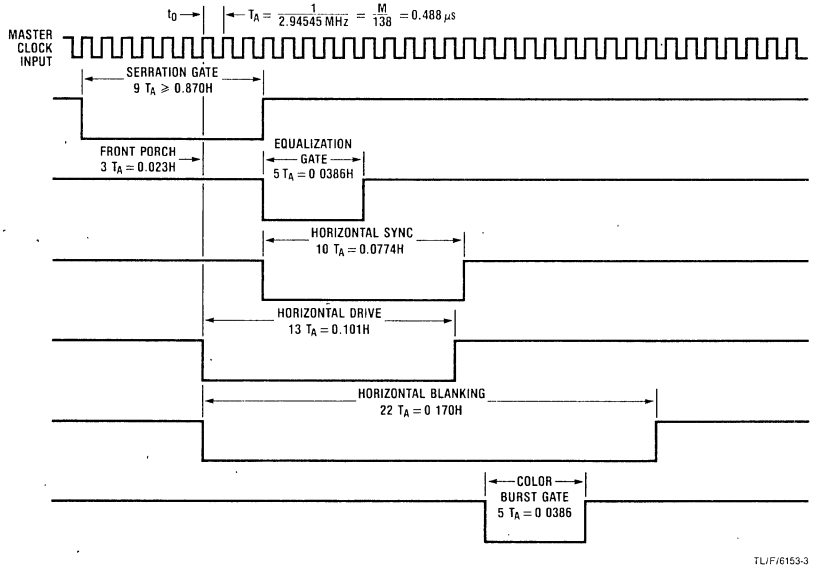


Figure 3. Horizontal Timing Diagram with the Input Clock Frequency Equal to 2.04545 MHz

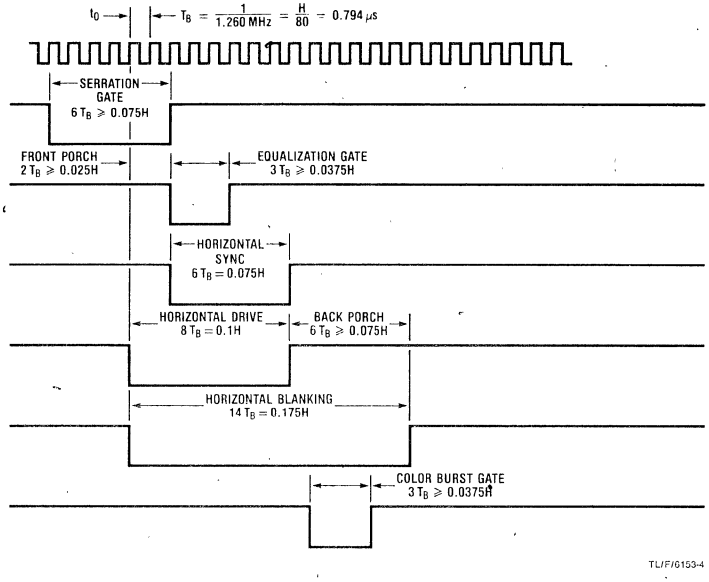


Figure 4. Horizontal Timing Diagram with the Input Clock Equal to 1.260 MHz

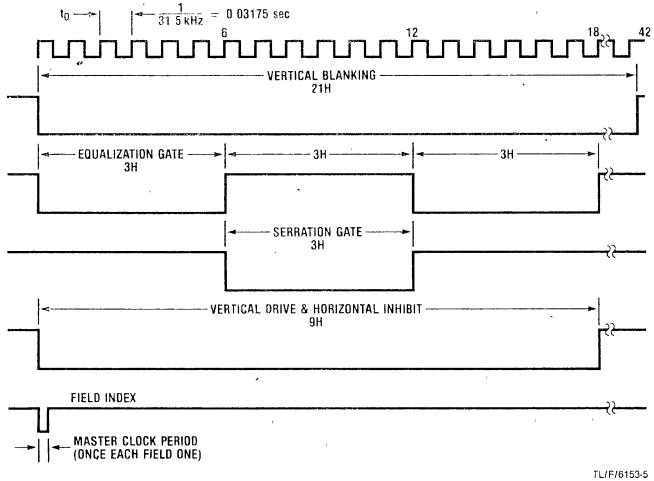


Figure 5. Vertical Timing Diagram

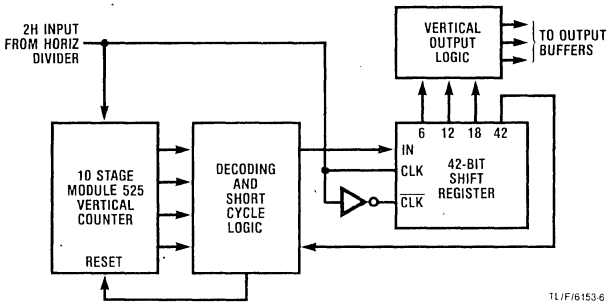


Figure 6. Simplified Vertical Timing Logic

Figure 6 indicates the method of generating the vertical output functions. Decoding logic detects the 525th state and short cycles the counter by resetting it to zero. Simultaneously, the input of the 42-bit shift register is set to zero and the vertical blanking and equalization gates are initiated. Six register clock periods later, the equalization gate is terminated and the serration pulse is initiated by the arrival of a zero state at the sixth bit of the shift register. Similarly, the serration gate is terminated and the equalization gate reinitiated when a zero is detected at the 12th tap and, finally, the equalization gate is terminated when the 18th tap changes to a zero. The vertical drive pulse is also initiated when the register input goes to a zero, and is terminated when the zero reaches the 18th bit. The vertical blanking pulse lasts until the zero propagates to the 42nd bit, at which time the register input is reset to a logical "1" level.

In some applications, particularly video recorder tape editing, it is necessary to identify which field of the vertical frame the system is in. For that purpose, the generator derives a Field Index pulse which identified field one by occurring for two input clock periods at the leading edge of the vertical blanking pulse of field one. Field one is defined as the field with a whole scanning line interval between the equalizing pulse and the last line sync pulse of the preceding field.

When designing MOS circuits, one must be aware of the effects of power supply variations, ambient temperature excursions, and process variables on circuit performance. This is the case in design of most circuits of course, but MOS tends to be more sensitive than bipolar circuits due to increased parasitic capacitance and limited current drive capabilities. The speed of any MOS product is essentially dependent upon how fast critical capacitive nodes can be charged and discharged. The charging or discharging current is in turn a function of the size, the voltages applied to, and the threshold and gain factor of the transistor(s) supplying the current. Threshold and gain factor are functions of process variables such as gate oxide thickness, the type of substrate material and its impurity concentration. They are also affected by temperature, which reduce the fermi potential (decreasing threshold), and modifies the carrier mobility in the transistor channel (which lowers the gain factor). the reduction in gain factor generally has more effect than the change in threshold, resulting in an overall reduction in speed with increasing temperature.

As far as the sync generator is concerned, this variation in performance as a function of environmental and power supply conditions could cause skewing of individual output timing edges, reducing the accuracy of the sync functions. Careful design essentially eliminates this problem in the MM5321. First, all output functions were matched for total logic delay by simulating circuit performance for all environmental and process variations, and then optimizing the delays to the output buffers. Second, all output functions are resynchronized at the outputs by an internal clock signal running at the input clock rate, with its own optimized delay characteristics with respect to the horizontal divider clock. For all worst-case conditions the output functions reach the synchronizing point before the synchronizing clock. Third, all the output buffers themselves are identical and therefore have matched delays. Thus, the design results in output functions whose timing delays are matched with respect to each other, but will have differences in delay with respect to the input clock on a part to part basis (due to variations in process variables). Even on a part to part basis, maximum differences in delay between two parts with the maximum allowed process variation should be less than 200ns, or 0.003H, at similar temperature and power supply values.

The output buffers are push-pull using the circuit configuration shown in Figure 7. The output transistors Q1 and Q2 provide the sink and source characteristics shown in Figure 8. When interfacing directly with TTL, the 800Ω resistor serves to limit the excess sink current supplied to the TTL clamp diode, by reducing the gate drive to Q2. This minimizes excessive power dissipation on the chip and protects the TTL diode. Q8 is the logic transfer device driven by the synchronizing clock.

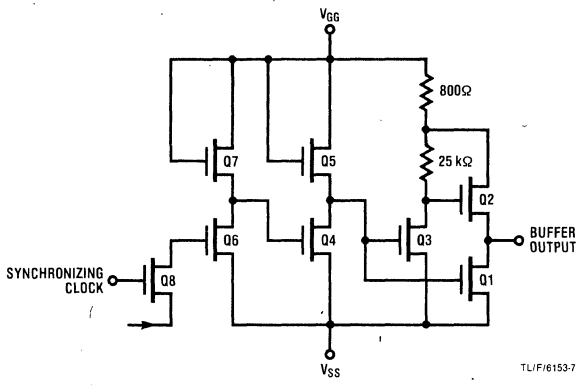


Figure 7. Schematic of TTL Compatible Push-Pull Buffer used on All Outputs of the Sync Generator

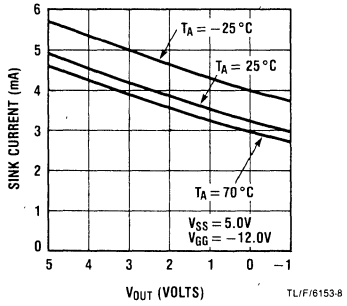


Figure 8a. Typical Output Sink Current as a Function of Output Voltage

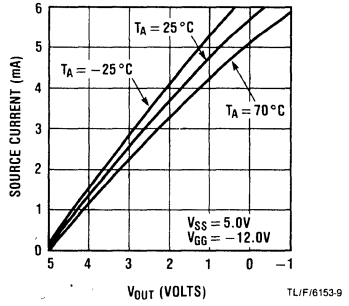


Figure 8b. Typical Output Source Current as a Function of Output Voltage

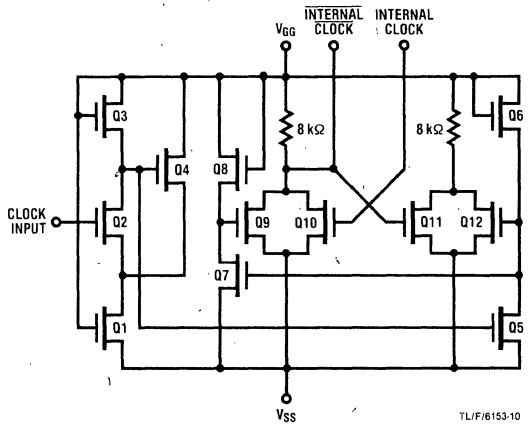


Figure 9. Schematic of Input Clock Buffer

The most critical circuitry in the generator, from the standpoint of speed, is the input clock buffer (Figure 9). The buffer is designed to generate a two-phase, full power supply amplitude clock signal from the single-phase low amplitude input signal. Q1 through Q4 constitute a Schmitt trigger type input stage that guarantees a trip-point range of $V_{SS} - 4.2V$ maximum for "0" levels, and $V_{SS} - 2.0V$ minimum for TTL "1" levels. When interfacing directly with TTL, the normal supplies will be +5 volts connected to V_{SS}, and −12V connected to the V_{GG} pin. For a tolerance of 5% on the V_{SS} supply, the guaranteed trip-points decipher to a required input level more negative than 4.75V-4.2V, or 0.55V, for the "0" level, and a required level more positive than 4.75V-2.0V, or 2.75, for the "1" level. These levels are obtainable from standard TTL without any external interface components. Q10 and Q11 are feedback latches which eliminate internal clock overlap problems.

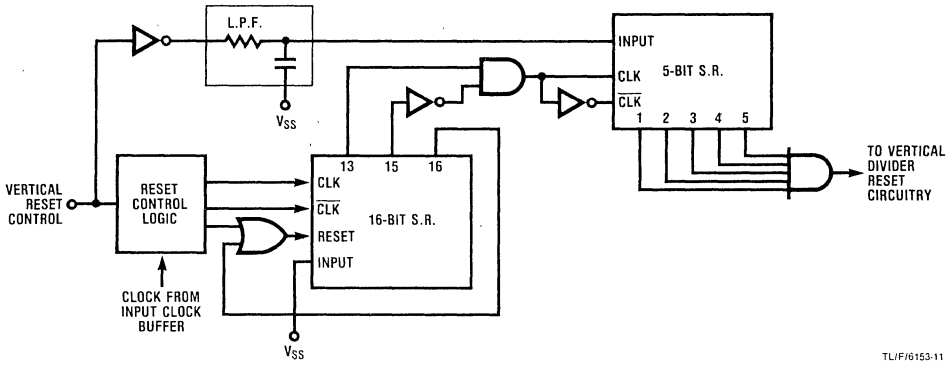


Figure 10. Basic Logic for Detecting Proper State of the Composite Sync Input Signal for Resetting the Vertical Divider in "Gen-Lock" Operation

To provide as much versatility as possible, a variety of divider reset ("gen-clock") features have been included. The horizontal and vertical dividers have individual Vertical and Horizontal Reset inputs which allow independent resetting of the appropriate divider. With the inputs tied together, both dividers may be reset simultaneously.

The vertical divider may be reset to either of two states, depending upon the DC level of the Reset Control pin. If the Reset Control is tied to V_{SS}, the most positive supply, a TTL "1" to the "0" level transition on the Vertical Reset pin will reset the vertical divider to all zeros, which is time zero as defined by the vertical timing diagram. With the Reset Control returned to V_{GG}, a Vertical Reset pulse will reset the vertical divider to the fifth serration pulse (eleven 0.5H time intervals from time zero). This allows the reset pulse to be generated by analog detection of a composite sync or video signal, and used to gen-lock the slave sync generator within the same field interval. The horizontal divider is always reset to zero, as defined by the horizontal timing diagram.

The Field Index output pulse occurs once during each field one at time zero and last for two master clock periods. It can be used to gen-lock similar sync generator chips by connecting it to their Vertical Reset inputs and wiring the Reset Control to the V_{SS} supply.

Another method of resetting the vertical divider is provided by using the Reset Control pin as an input for a composite sync signal from which gen-locking is desired. The slaved generator detects the fifth serration pulse and resets the vertical divider to the proper state (Figure 10).

The reset control logic generates a two-phase clock with a frequency equal to the input clock rate anytime the composite sync input signal is more negative than the Reset Control trip-point. A 16-bit dynamic shift register with its input connected to V_{SS} is driven by the modulated clock signal. When the composite sync input becomes more positive than the Reset Control trip-point, or if the 16th bit becomes a "1", all sixteen bits of the register are reset to zeros. If the composite sync signal remains low for fifteen master clock periods, another two-phase signal is generated which acts as the clock for a 5-bit shift register used to store the sampled state of the inverted (and filtered) composite sync signal. The sample is the average value of the filtered signal during an approximately 200ns sampling window occurring just before the fifteenth master clock time after the composite sync input signal initially went low. The input trip-point of the 5-bit register determines whether the sampled signal is stored as a "1" or "0" logic state.

Fifteen input clock periods equal a time of 7.3μs at an input clock frequency of 2.04545MHz, and 11.9μs when the input rate is 1.260MHz. The only interval of the composite sync waveform which is legitimately low during this time is the vertical sync pulse. In the present design, the first five serrated intervals must be successfully detected before the vertical divider is reset to the proper state. The limitation in this design may be the difficulty in acutally acquiring legitimate detection due to excessive noise and missing pulses in the composite sync input signal. If this proves to be the case, it is possible to eliminate the second and/or fourth bits of the 5-bit register as detection requirements. This should improve the statistical probability of getting an initial gen-lock condition within a reasonable time.

As illustrated above, the Reset Control input has a dual function. It selects the reset state of the vertical divider when hardwired to either V_{SS} or V_{GG}, and acts as a dynamic input when gen-locking is to be established using a composite sync input signal. When using the Reset Control as the input for a composite sync signal, the Vertical Reset pin should be hardwired to V_{SS}.

The MM5321 TV Sync Generator has been designed with both versatility and economy as the primary objectives. We feel it exemplifies the role of MOS/LSI standard products can play in providing useful consumer products in a manner that both large *and* small volume users will find attractive.

Simplified Multi-Digit LED Display Design Using MM74C911/MM74C912/ MM74C917 Display Controllers

National Semiconductor
Application Note 257
Larry Wakeman
May 1981

I. Introduction

The MM74C911, MM74C912 and MM74C9127 are CMOS display controllers that control multiplexing of 8-segment LED displays. These devices each have an on-chip multiplex oscillator and associated logic to easily implement multi-digit displays with minimal additional hardware. These controllers were designed to be easily interfaced to a microprocessor as a small 4-or 6-byte area of write-only memory (WOM), but they are not limited to this environment.

The MM74C911 is the simplest of these devices. It has one data input for each of its eight segment outputs, allowing direct control of any LED segment. Both the MM74C912 and MM74C917 have five data inputs which accept either BCD (MM74C912) or hexadecimal (MM74C917) data, plus decimal point. The MM74C911 can interface up to four 8-segment displays and the MM74C912/MM74C917 can control up to six 8-segment displays.

II. Functional Description — MM74C911

The functional block diagram for the MM74C911 is shown in *Figure 1*. The eight data inputs are buffered and bussed to the four dual-port latches. To write data into a particular latch, K1 and K2 address inputs are decoded and the proper latch is enabled when $\overline{CE}$ and $\overline{WE}$ are taken low.

The latch outputs are controlled by the multiplexer (MUX) logic. All four latch data outputs are commonly bussed, and are sequentially read by the MUX logic. The bussed 8-segment outputs are then buffered by bipolar segment driver transistors, which are enabled when $\overline{SOE}$ is low, and are in TRI-STATE® mode when Segment Output Enable ($\overline{SOE}$) is held high. This allows easy display blanking without loss of data.

The multiplexer logic controls all of the timing for the MM74C911 and also generates the digit output strobes. The timing diagram is shown in *Figure 2*.

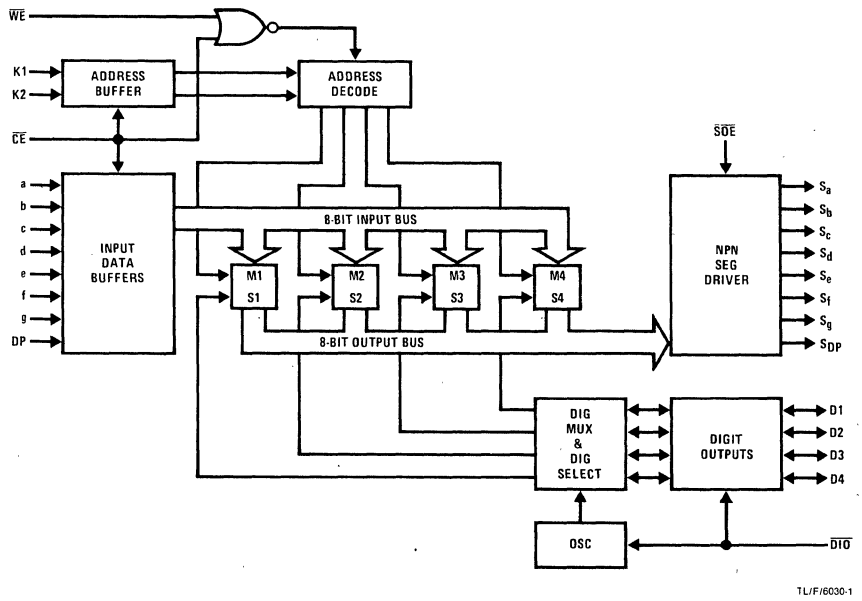


Figure 1. MM74C911 Block Diagram

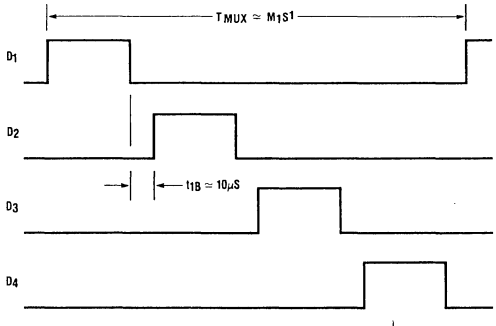


Figure 2. MUX Timing for MM74C911 TL/F/6030-2

By raising the Digit In-Out ($\overline{DIO}$) input high, the internal oscillator is disabled and the digit outputs become inputs which control reading of the 4-digit latches. This allows the MM74C911 to be slaved to other multiplex timing signals. If both $\overline{SOE}$ and $\overline{DIO}$ are held high, both the display and oscillator are disabled causing the MM74C911 to be in a low-power mode where it typically draws less than 1 μA. *Figure 3* shows the truth table for these control inputs.

$\overline{DIO}$/$\overline{OSE}$	$\overline{SOE}$	MODE
0	0	NORMAL DISPLAY MODE
0	1	DISPLAY BLANKED
1	0	WILL DISPLAY ONE DIGIT*
1	1	LOW POWER MODE

TL/F/6030-3

Figure 3. Operating Modes for the MM74C911/ MM74C912/MM74C917 (*The 74C911 Digit Outputs become inputs.)

III. Functional Description — MM74C912/MM74C917

The functional block diagram for the MM74C912 and MM74C917 is shown in *Figure 4*. These devices are very similar to the MM74C911. There are only five data inputs on the MM74C912 and MM74C917 which are buffered, then bussed to six 5-bit dual-port latches. The address present on K1, K2, and K3 will dictate which of the six latches will be loaded when both $\overline{CE}$ and $\overline{WE}$ are low. The outputs of all of the latches are commonly bussed and fed into a decoder ROM which converts BCD (MM74C912) or hexadecimal (MM74C917) code to seven segment. The fifth bit is the decimal point, which bypasses the ROM. The 8-segment bits are then buffered by eight NPN-segment drivers. Like the MM74C911, these outputs are TRI-STATE and will blank the display when $\overline{SOE}$ is held high.

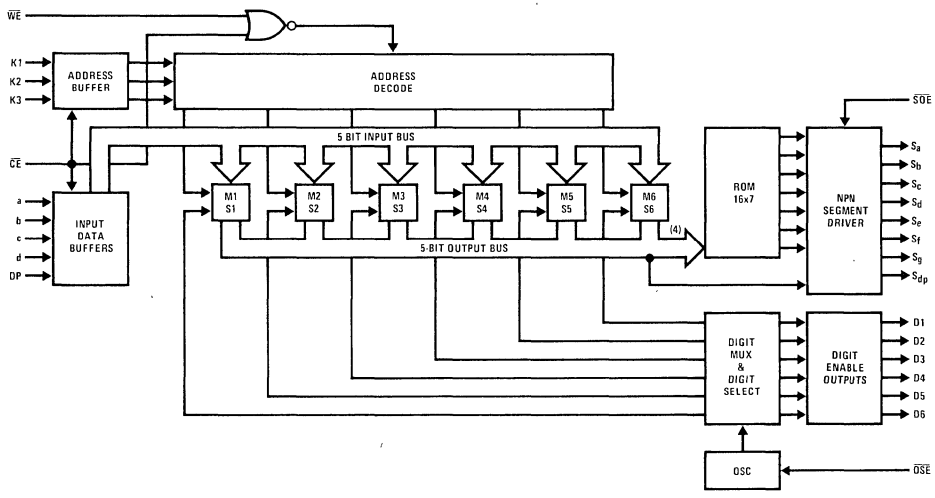
All of the multiplexing is controlled by an internal oscillator and control logic. The logic sequentially reads each latch and activates the digit outputs. The oscillator can be disabled by raising the Oscillator Enable ($\overline{OSE}$) input high, but the digit outputs do not become inputs and thus the MM74C912, and MM74C917 can not be slaved. However, by raising both $\overline{SOE}$ and $\overline{OSE}$ high, these parts can be put into a low-power mode similar to the MM74C911. *Figure 3* shows the controller operating modes.

The MM74C912 and the MM74C917 are identical except for the last seven ROM locations. The ROM outputs are shown in *Figure 5* for both parts.

IV. Display Interface Design

A. Common Cathode LED's

Since the MM74C911/MM74C912/MM74C917 contain all the multiplex circuitry necessary to operate a 4- or 6-digit display, all the designer must do is choose appropriate segment resistors and digit drivers to properly illuminate the LEDs. A typical LED connection is shown in *Figure 6*. Based on the selected display, a certain segment current will be required. This current will determine the value of the segment resistor and the type of digit driver necessary. The design for the MM74C911 is



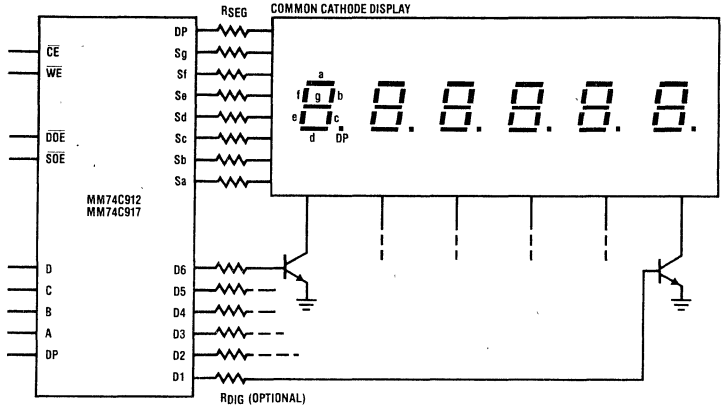
TL/F/6030-4

Figure 4. MM74C912 and MM74C917 Display Controller

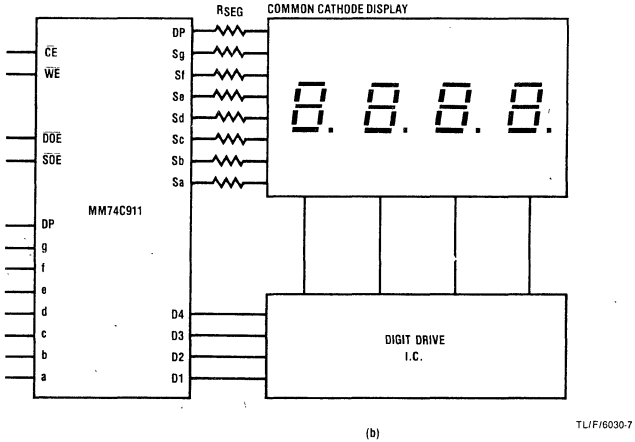
MM74C917	Hi-Z	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F	.
MM74C912	Hi-Z	0	1	2	3	4	5	6	7	8	9	°	⁻	–	_			.
Input A 2^0	X	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
Data B 2^1	X	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
C 2^2	X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
D 2^3	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DP	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Output Enable $\overline{SOE}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TL/F/6030-5

Figure 5. MM74C912/MM74C917 Character Fonts



(a)



(b)

Figure 6. Typical LED Connections for (a) MM74C912/MM74C917 (b) MM74C911

nearly the same as for the MM74C912/MM74C917 except that due to multiplexing the 6-digit controllers must be designed to a higher peak current value.

As an example, suppose the the NSN781 (2-digit, 0.7" common catholde LED display) has been selected. These displays require an average current of 8 mA per segment for good illumination. The MM74C911 multiplexes four digits; thus, any one digit is on ¼ of the time. Each digit must have a peak current four times its average current to achieve the same brightness. The MM74C911 must supply about 32 mA per segment, and the MM74C912/MM74C917 would have to supply a current six times the average current or about 48 mA.

The maximum digit driver current is the maximum number of "on" segments multiplied by the segment current. For the MM74C911 design, the digit current is ~260 mA, and is ~380 mA for the MM74C912/MM74C917. Using this digit current value, the digit driver can be selected. *Figure 7* shows possible digit driver ICs, but discrete transistors or Darlingtons may also be used, and may be desirable in some higher current applications. It is also important to keep in mind that the output voltage of the driver at the designed current, as this voltage can affect the display controllers current drive. For most designs, an output voltage of < 2V is reasonable.

Once the digit driver has been chosen and the output voltage at the desired current is known, the segment resistor, R_{SEG} can be calculated using:

$$R_{SEG} = \frac{V_{SEG} - V_{LED} - V_{DO}}{I_{SEG}}$$

where V_{LED} is the voltage across the LED, 1.8 V; V_{DO} is the digit driver output voltage at the chosen current; I_{SEG} is the peak segment current; and V_{SEG} is the MM74C911 or MM74C912 segment driver output voltage at the peak segment current, which can be determined from the curves in *Figure 8*.

In most cases, R_{SEG} can be more quickly determined from *Figure 9* which plots R_{SEG} vs. average segment current. These curves are plotted for various digit driver output voltages using current values from *Figure 8*. Thus, for the above example, if a DS75492 driver I.C. is used with the MM74C911 to interface to the NSB781 LEDs $R_{SEG} = 38\,\Omega$ assuming the drivers output voltage is 1.0 V. Note that *Figure 7* tabulates minimum output drive where the above V_{DO} is an approximation of the DS75492s typical V_{DO} at 260 mA.

Part Number	Driver Type	Number of Drivers	Minimum Output Drive
DS75492	Darlington Driver	6	250 mA@1.5 V
DS75494	Multiple Transistor Driver	6	150 mA@0.35 V
DS8646	Transistor Driver	6	84 mA@0.55 V
DS8658	Transistor Driver	4	84 mA@0.55 V
DS8870	Darlington Driver	6	350 mA@1.4 V
DS8871/2	Transistor Driver	8/9	40 mA@0.5 V
DS8877	Transistor Driver	6	35 mA@0.5 V
DS8920	Transistor Driver	9	40 mA@0.5 V
DS8963	Darlington Driver	8	500 mA@1.5 V
DS8978	Transistor Driver	9	100 mA@0.7 V
DS8692	Transistor Driver	8	350 mA@1.0 V

Figure 7. Typical LED Digit Drivers and Their Characteristics

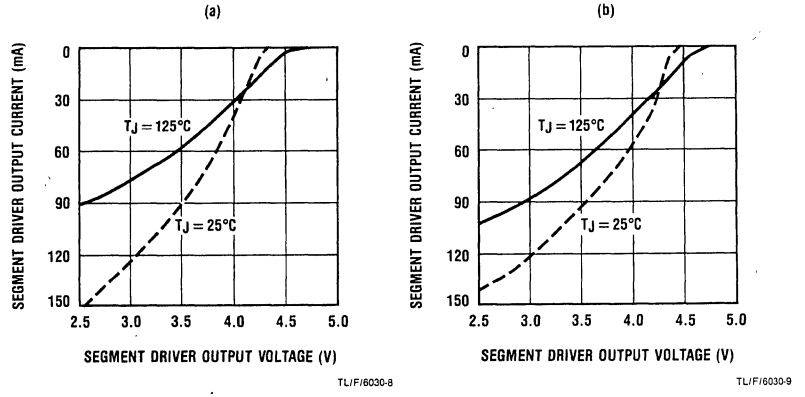


Figure 8. Typical Segment Driver Current vs. Output Voltage for (a) MM74C911 (b) MM74C912/MM74C917

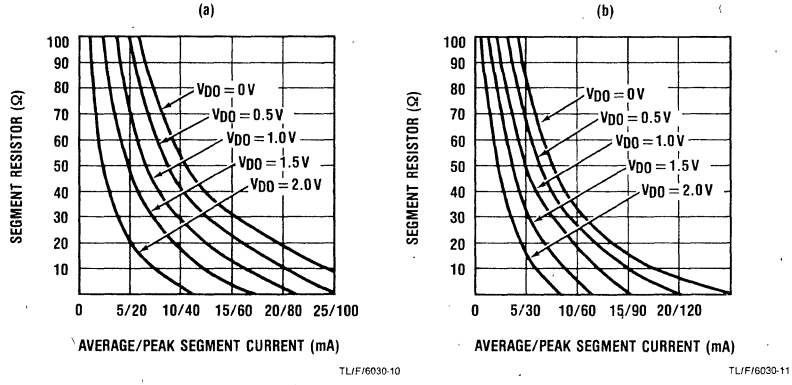


Figure 9. Average LED Segment Current vs. Segment Resistor for (a) MM74C911 (b) MM74C912/MM74C917

Figures 10 and *11* tabulate some typical segment resistor values for various National LED displays. (See Optoelectronics Databook for detailed specifications.) This table was compiled for a well lit room, but variation in ambient lighting may require some slight modification in the typical segment resistor values.

If a transistor digit driver is being used, it is sometimes desirable to use a base current limiting resistor between the controller's output and the transistor's base. This will help limit the power dissipation of the display controller in critical situations. The digit resistor, R_{DIG}, can be calculated using:

$$R_{DIG} = \frac{V_{DIG} - V_{DI}}{I_{DI}}$$

where V_{DI} is the digit driver input voltage, 0.7 V for a transistor, I_{DI} is the desired digit driver current and V_{DIG} is the controller's digit output voltage for the chosen current which can be found from *Figure 12*.

When the MM74C911 is to be used as a "master" to drive another MM74C911 or other logic, the digit outputs must have a high output voltage of 3.0 V to driver another MM74C911 or 3.5 V to drive standard CMOS logic. The digit resistor should be $> 300\,\Omega$ for $V_{OH} \geq 3.0$ V and $R_{DIG} > 350$ for $V_{OH} \geq 3.5$ V.

A final design consideration is power dissipation. When designing a low-power system where the total current is to be minimized, the total system power consumption is simply:

$$P_T \cong V_{CC}[I_{DO} + I_{DI}]$$

DISPLAY			DRIVER	TYPICAL RANGE OF SEGMENT RESISTORS
PART NO.	HEIGHT (IN.)	NO. OF DIGITS		
NSA1298	0.110	9	DS75492	300-1000 Ω 300-2000 Ω*
NSA1558	0.140	8	DS75492	200-800 Ω 200-1800Ω*
NSN381	0.3	2	DS75492 2N3904	15-80 Ω
NSB3881	0.5	4	DS75492 2N3904	15-80 Ω
NSN581	0.5	2	DS75492 2N3904	10-60 Ω
NSB5881	0.5	4	DS75492 2N3904	10-60 Ω
NSN781	0.7	2	DS75492 2N3904	10-50 Ω
NSB7881	0.7	4	DS75492 2N3904	10-50 Ω

Figure 10. MM74C911 Segment Resistor Values for Various Displays ($V_{CC} = 5$ V) (*Using Red LED Filter over Display)

DISPLAY			DRIVER ($R_D = 0$)	TYPICAL RANGE OF SEGMENT RESISTORS
PART NO.	HEIGHT (IN.)	NO. OF DIGITS		
NSA1298	0.110	9	DS75494	200-800 Ω 300-1500 Ω*
NSA1558	0.140	8	DS75494	150-700 Ω 150-1000Ω*
NSN381	0.3	2	DS75492	5-50 Ω
NSB581	0.5	2	DS75492	5-50 Ω
NS5931	0.5	6	DS75492 2N3904	5-40 Ω
NSN781	0.7	2	DS75492 2N3904	5-30 Ω

Figure 11. MM74C912/MM74C917 Segment Resistor for Average Intensity for Various Displays (*Using Red LED Filter over Display)

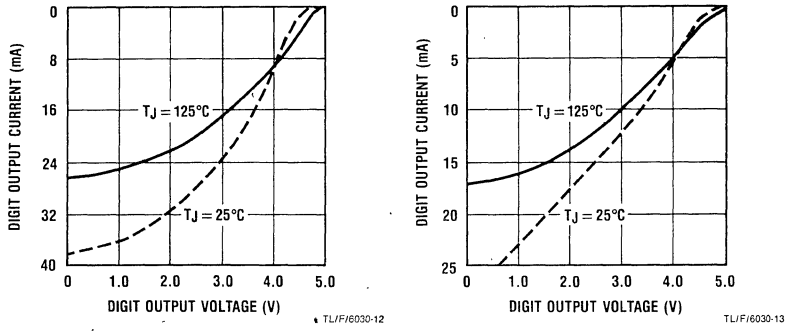


Figure 12. Typical Digit Driver Current vs. Output Voltage for (a) MM74C911 (b) MM74C912/MM74C917

where I_{DO} is the maximum digit driver output current, V_{CC} is the power supply voltage, and I_{DI} is the digit driver input current.

When a circuit design employs large segment currents, the maximum dissipation should be calculated to ensure that the power consumption of the controller or digit driver is within the maximum limits. The display controller power dissipation is:

$$P_C = S(I_{SEG})(V_{CC} - V_{SEG})$$

where I_{SEG} and V_{SEG} are the peak segment current and segment voltage, as previously determined; and S is the maximum number of segments lit per digit. The maximum package dissipation for the controllers vs. temperature is shown in *Figure 13*.

To gain an understanding of how segment current affects the controllers power dissipation, *Figure 14* plots average and peak LED segment current vs. package dissipation for both the MM74C911 and the MM74C912/MM74C917. These typical curves are plotted using the typical segment driver output currents and voltages from *Figure 8*.

As the digit driver output voltage V_{DO} becomes larger, the driver dissipates more power, thus the designer should also ensure that the driver's dissipation is not exceeded. Generally, the standard digit driver IC will dissipate around ½ watt. (See specific data sheets.) Driver power dissipation can be calculated by:

$$P_D = (V_{DO})(I_{DIG})$$

where V_{DO} and I_{DIG} are the digit driver output voltage and current. In a standard digit driver, one output will be active all the time, but if discrete transistors are used, each transistor is turned on 25% of the time. The average power dissipation for each discrete transistor digit driver is ¼ of the above equation.

B. Common Anode LED Display

Although connecting the MM74C911/MM74C912/MM74C917 to common anode displays is somewhat more difficult than to common cathode displays, it can be done. These controllers still provide all the necessary timing signals, but some extra buffering must be added to ensure the correct logic levels and drive capability.

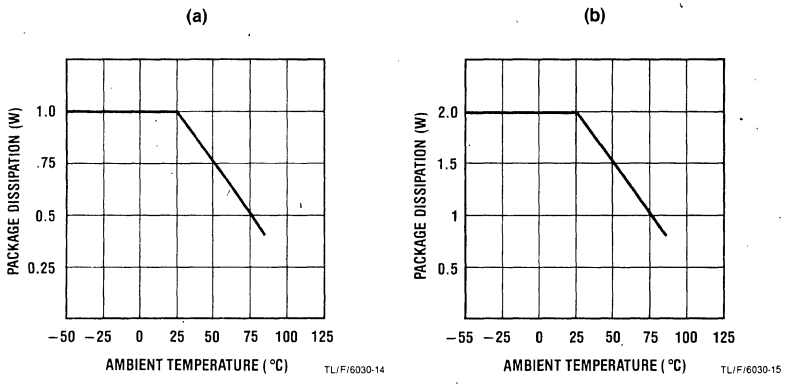


Figure 13. MM74C911/MM74C912MM74C917 Maximum Power Dissipation for (a) Plastic "N" Package (b) Ceramic "J" Package (Note $T_{J(MAX)}$ = 125°C Maximum Junction Temperature)

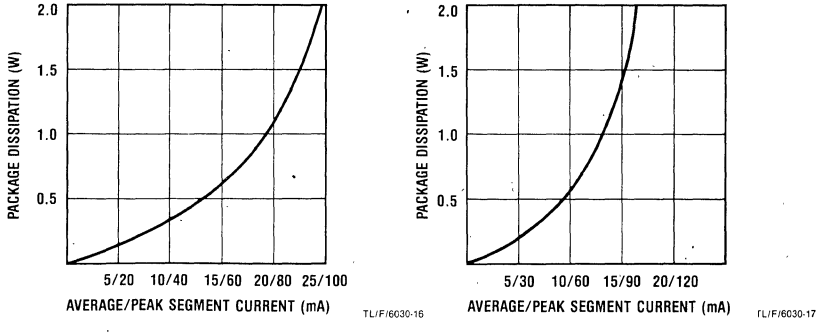


Figure 14. Typical Power Dissipation vs. Segment Current for (a) MM74C911 (b) MM74C912/MM74C917

To drive common anode displays, the display controller's segment outputs must be inverted and the digit outputs must be current buffered. *Figure 15* shows a simple circuit to interface to most common anode displays. An 8-digit calculator digit driver IC, DS8871, is used to drive the display segments. Segment resistors on the controller's segment outputs are not necessary but may be necessary on the outputs of the DS8871 driver.

For higher current displays, the choice of digit driver transistor is important as the digit current will depend on how high the digit driver output of the display controller can pull up due to the emitter follower configuration. For good display brightness, a high gain medium power transistor should be used.

C. Vacuum Fluorescent (VF) Displays

The MM74C911/MM74C912/MM74C917 are not directly capable of driving VF displays, but serve as a major functional block to ease driving 4- or 6-digit displays. The controllers provide the multiplex timing for this display, but the segment and digit outputs must be level shifted, and a filament voltage must be applied.

In *Figure 16*, a DS8654 or similar device is used to translate the segment and digit voltages to 30V to drive the segment plates and digit grids. The AC filament voltage is derived from a separate low-voltage transformer which is biased by a zener. Since there is no pull-down in the DS8654, pull-down resistors must be added. The exact anode and cathode voltages and the bias zener will depend on the display used, but the basic circuit is the same.

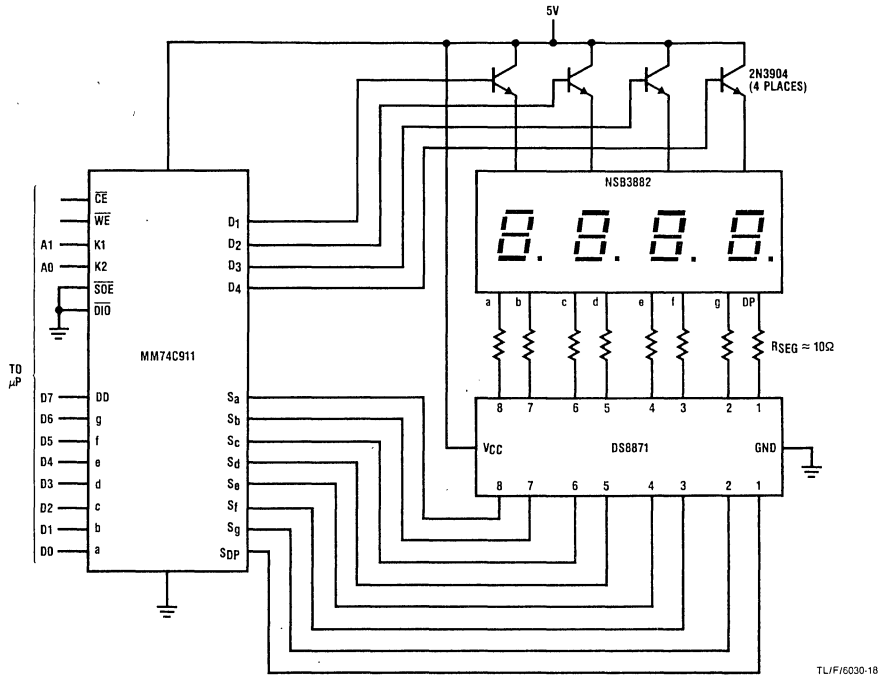


Figure 15. MM74C911 to Common Anode LED Interface Using 9 Digit Driver

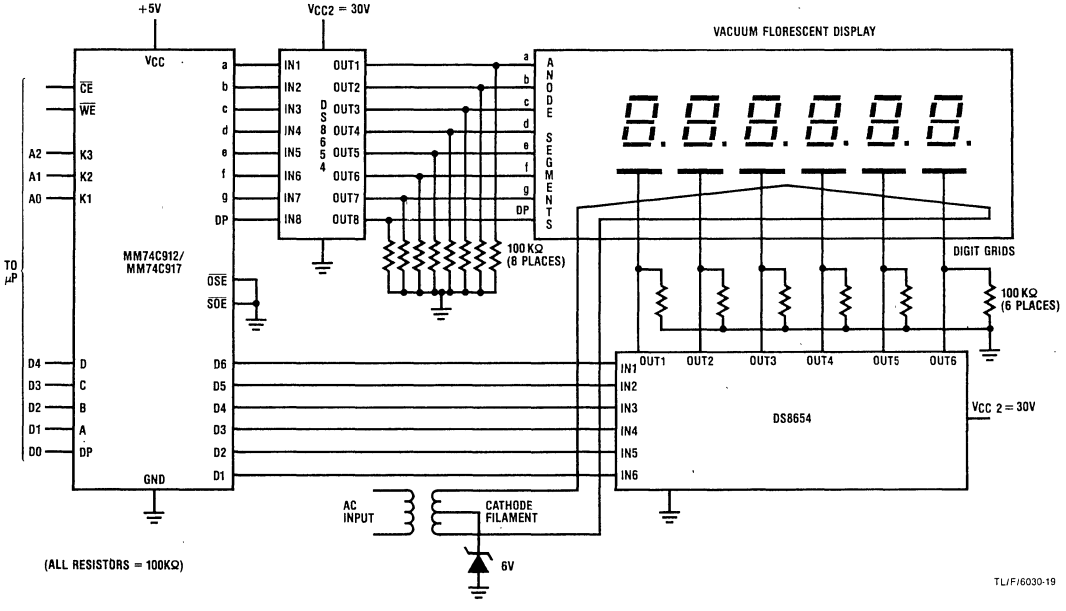


Figure 16. MM74C912/MM74C917 to Vacuum Fluorescent Display Interface

V. MM74C911 Display Applications

Of the three CMOS display controllers, the MM74C911 is the simplest, but also the most versatile. Since the character font is not predetermined, many non-numerical characters can be displayed using standard 8-segment displays. In many cases, it may be desirable to enable a small microprocessor to display prompt messages where the use of more complicated alpha-numeric displays is not justified. For these cases, the MM74C911 is ideal, because any combination of segments can be controlled. *Figure 17* shows many of the possible letters and numbers that can be displayed along with their binary and hexadecimal values on 8-segment displays.

There is no reason to restrict the MM74C911 to alpha-numeric displays, as the controller allows direct control of individual LEDs. The MM74C911 can be connected to a mixture of numerical and discrete LEDs as typified by *Figure 18*. Thus status and numerical data can be simultaneously controlled.

Taking this one step further, all the LEDs could be discrete as shown in *Figure 19*. This type of arrangement is multipurpose. The LEDs could be configured as a 4×8 matrix or possible two-bar graphs of 16 LEDs, *Figure 20*, or maybe some sort of binary data display. There are many variations possible.

VI. Slaving The MM74C911

As mentioned, the MM74C911 has the unique feature of being able to be slaved to external multiplex logic or a "master" MM74C911. This feature is useful when the controller is to be synchronized with a master. *Figure 21* shows a typical application where two MM74C911s are used to drive a 16-segment alpha-numeric display. In order to drive this display, synchronization is required to ensure that both controllers are outputting the same digit information at the same time.

A more subtle advantage to slaving MM74C911s occurs when trying to use multi-controllers to drive more digits. This case, illustrated in *Figure 22*, allows fewer, more powerful digit drivers to be used. This can be advantageous when using smaller displays that require little power to begin with.

VII. MM74C912/MM74C917 Display Applications

Both the MM74C911/MM74C912 have predetermined character fonts and this limits their versatility, but greatly simplifies their application in hex and decimal display application. Still, there are a few small "tricks" that can be used to stretch the controller's capabilities.

In many applications, the decimal point segment is not needed, particularly when the MM74C917 is used. Generally, this part is used to display hexadecimal address and data information where decimal points are rarely needed. These segments could be used for status information. *Figure 23* shows a typical implementation. The status LEDs could indicate power, run and halt status information of a host μP or could indicate the type of instruction being executed. Although the MM74C912 applications would tend to use the decimal point more often, it is equally capable of implementing *Figure 23*.

Another possibility, if all six digits are not required, is to use the unused digits for status indicators. A possible example using the MM74C917 is shown in *Figure 24*, and another possible implementation for the MM74C912 is shown in *Figure 25*. In both of these applications, four bits of data is loaded into digits 1 and/or 2. Depending on the data loaded, various combinations of discrete LEDs would be lit. The tables included in these figures illustrate numerical combinations and their results.

CHARACTER	HEX CODE FOR 74C911	DISPLAY	CHARACTER	HEX CODE FOR 74C911	DISPLAY
0	FC		J	78	
1	60		L	1C	
2	DA		N	2A	
3	F2		O	FC	
4	66		O	3A	
5	B6		P	CE	
6	BE		R	0A	
7	E0		S	B6	
8	FF		T	8C	
9	F6		U	7C	
			U	38	
A	EE		Y	76	
B	3E		Y	4E	
C	9C				
D	7A		(Blank)	00	
E	9E		.	01	
F	8E		−	02	
G	BC		=	12	
H	6E		?	CA	
H	2E		≥	D1	
I	0C		≤	9B	
I	20				

Figure 17. Segment Codes for Various Characters Using 8-Segment Displays (MSB of Hex Code is segment a, LSB is Decimal Point ie for 0 (a = 1, b = 1, c = 1, d = 1, e = 1, f = 1, g = 0, dp = 0) = FC)

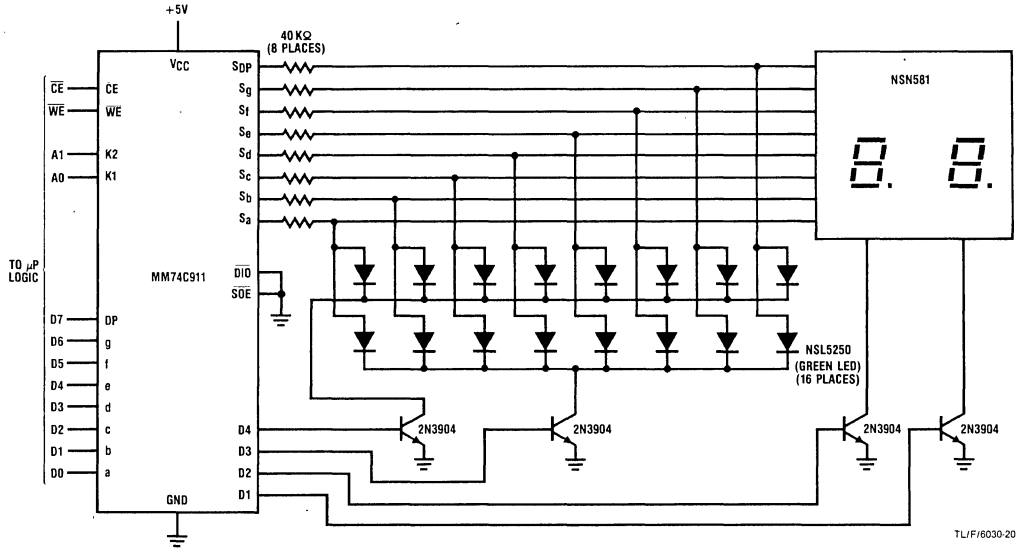


Figure 18. Discrete and Numeric Display

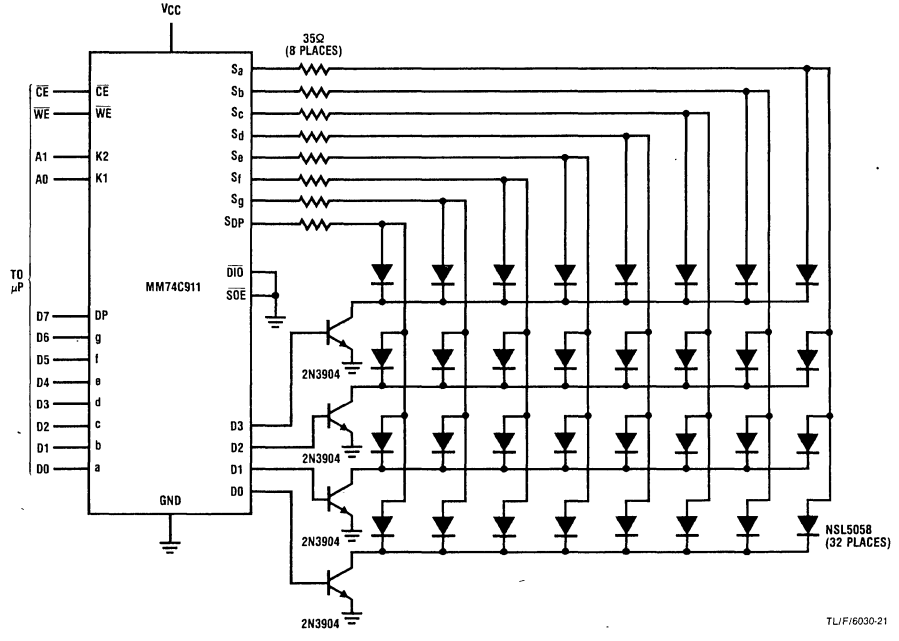


Figure 19. Discrete LED Matrix Display

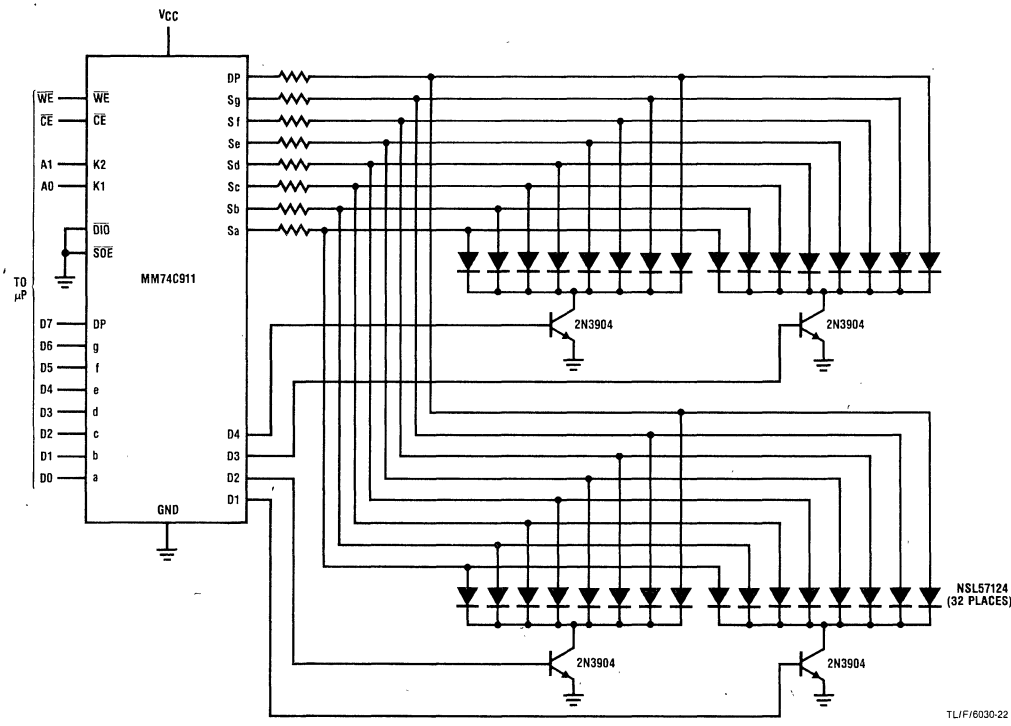


Figure 20. Dual 16 Element Bar Graph Display

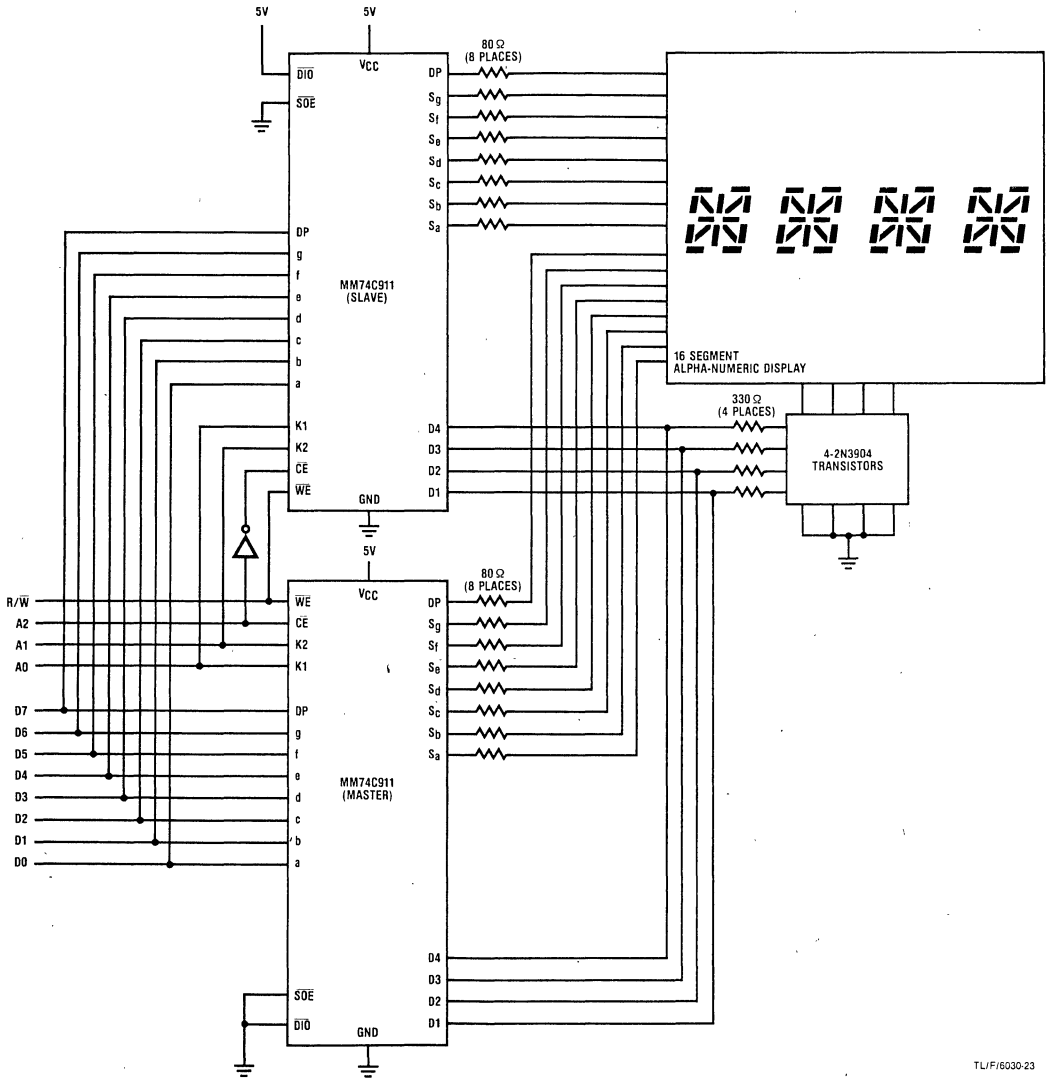


Figure 21. Interfacing to Alphanumeric Displays

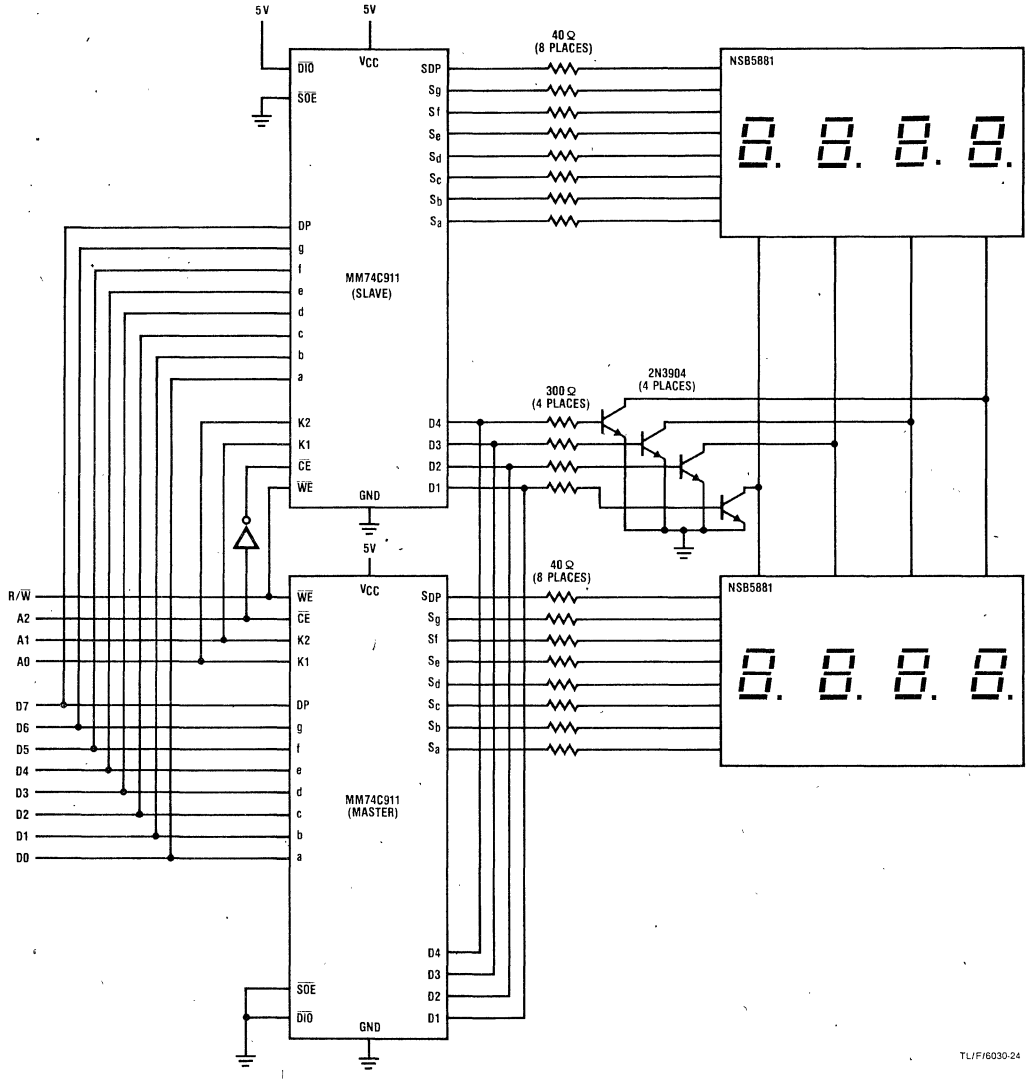


Figure 22. Multi-Digit Displays

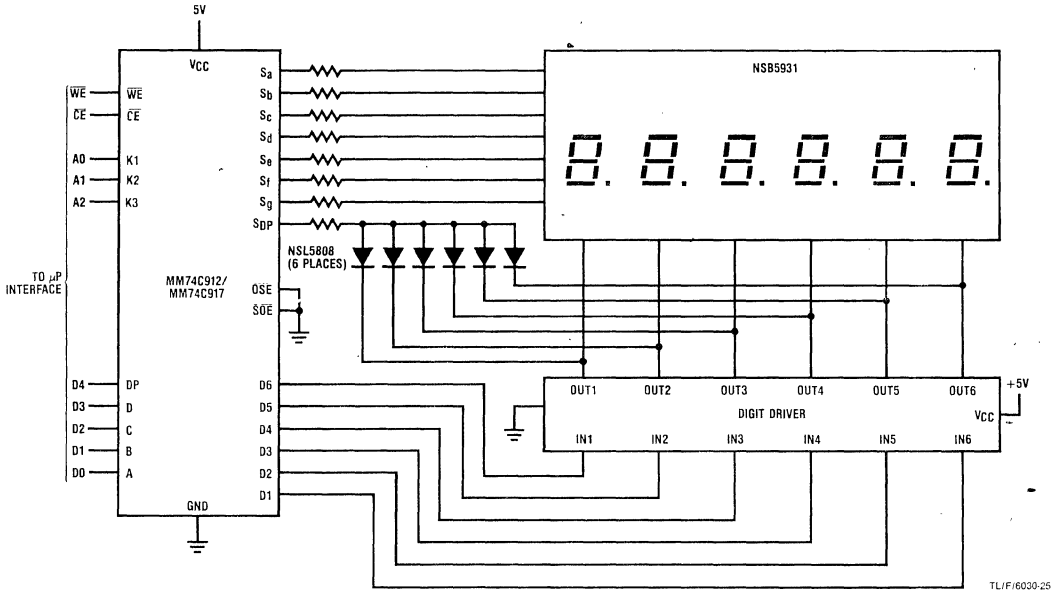
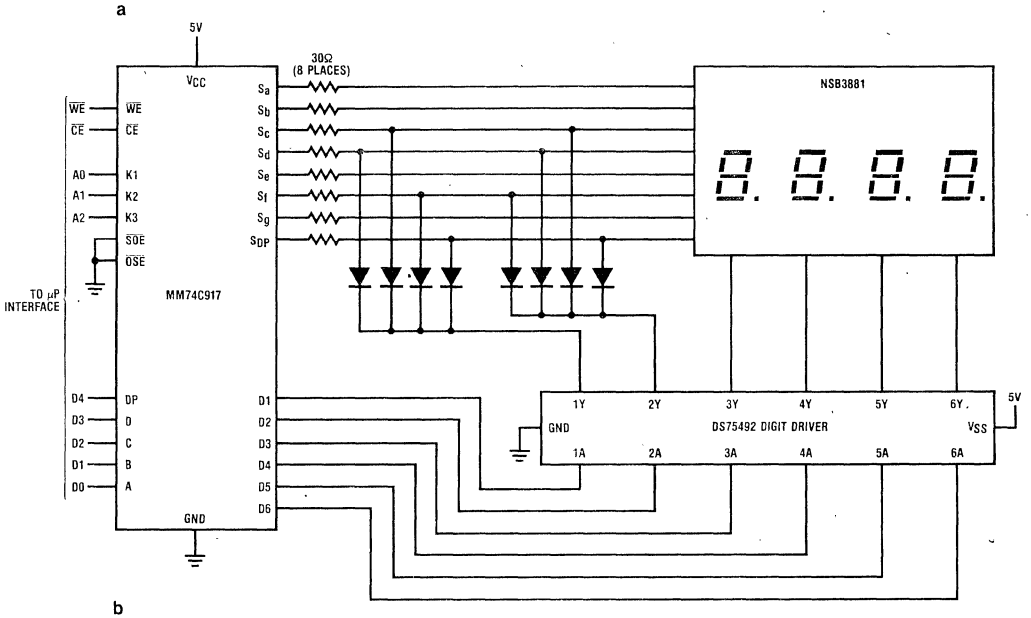


Figure 23. 7-Segment Displays with 6-Discrete LED Indicators for MM74C912/MM74C917 Using "DP" Segment

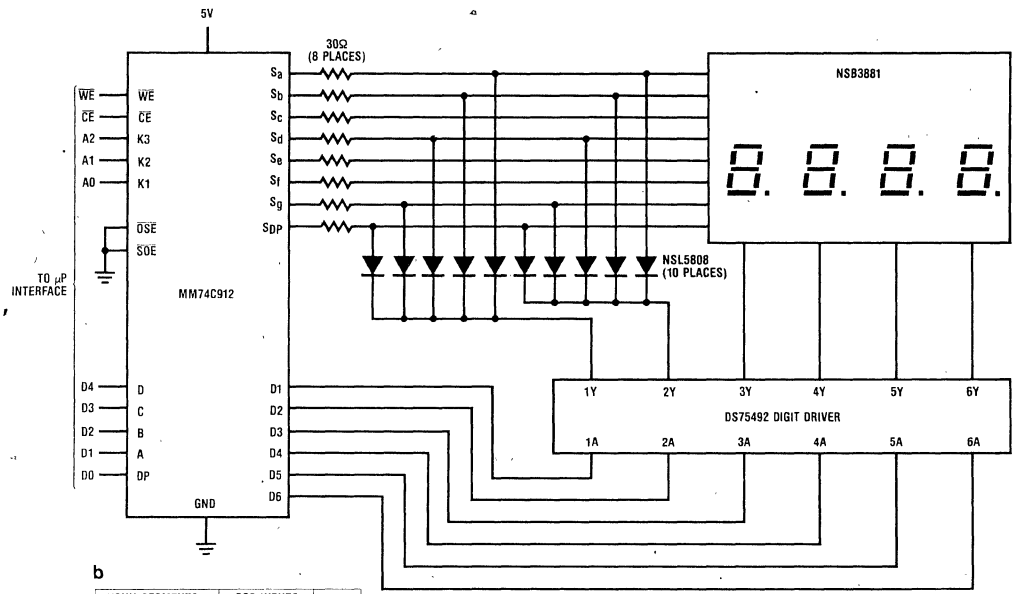


b

LED'S (1 = ON)				INPUTS				
DP	f	d	c	A	B	C	D	DP
1/0	0	0	0	—	—	—	—	1/0
1/0	0	0	1	0	0	0	1	1/0
1/0	0	1	0	0	0	1	0	1/0
1/0	0	1	1	0	0	1	1	1/0
1/0	1	0	0	1	1	1	1	1/0
1/0	1	0	1	0	1	0	0	1/0
1/0	1	1	0	1	1	0	0	1/0
1/0	1	1	1	1	0	0	0	1/0

Figure 24. MM74C917 (a) Display with 8 Discrete LED's (b) Inputs for LED Output Table

a



b

"ON" SEGMENTS					BCD INPUTS				
DP	G	D	B	A	D	C	B	A	DP
1/0	0	0	0	0	1	1	1	1	1/0
1/0	0	0	0	1	1	1	0	0	1/0
1/0	0	0	1	0	0	0	0	1	1/0
1/0	0	0	1	1	0	1	1	1	1/0
1/0	0	1	0	0	1	1	1	0	1/0
1/0	0	1	0	1	—	—	—	—	1/0
1/0	0	1	1	0	—	—	—	—	1/0
1/0	0	1	1	1	0	0	0	0	1/0
1/0	1	0	0	0	1	1	0	1	1/0
1/0	1	0	0	1	—	—	—	—	1/0
1/0	1	0	1	0	0	1	0	0	1/0
1/0	1	0	1	1	1	0	1	1	1/0
1/0	1	1	0	0	1	0	1	0	1/0
1/0	1	1	0	1	0	1	0	1	1/0
1/0	1	1	1	0	—	—	—	—	1/0
1/0	1	1	1	1	1	0	0	0	1/0

TL/F/6030-27

Figure 25. MM74C912 (a) 4 Digit Display with Discrete LEDs (b) I/O Data Table

VIII. Interfacing To Microprocessors

The CMOS LED display controllers can be easily interfaced to most of the popular microprocessors with the addition of only a few ICs. Most microprocessor data and address bus logic is specified to be TTL compatible. A standard TTL logic high, V_{OH} is supposed to be ≥ 2.4 at full load which is not compatible with a CMOS $V_{IH} \geq 3.5$ V. Although microprocessor inputs will typically pull-up above 3.5 V, this is not guaranteed over the entire temperature range. It is recommended that pull-up resistors be added to raise this level above 3.5 V. Under most conditions, a 5-10 K resistor should suffice.

The write timing of the display controllers is illustrated in *Figure 26*. The minimum write access time is 430 ns for the MM74C912/MM74C917 and 450 ns for the MM74C911. A write to the controller is accomplished by placing the desired data on the data inputs, lowering the $\overline{CE}$ and $\overline{WE}$ inputs, and then raising them to complete the write. Even though $\overline{CE}$ and $\overline{WE}$ are interchangeable, $\overline{CE}$ is usually derived from the address decoding logic and $\overline{WE}$ is connected to the CPU write strobe. Other than the slight timing differences between the MM74C911 and the MM74C912/MM74C917, the only other major microprocessor interfacing differences are that the MM74C912/MM74C917 have an additional digit address bit which must be connected to the microprocessors address bus, and the MM74C911 has eight data inputs whereas the MM74C912/MM74C917 have only five.

A. Interfacing To The INS8080

These controllers can be connected to the INS8080/INS8224/INS8238 CPU group with no external logic if no more than a minimal amount of address decoding is required. Since the INS8080 has a separate memory and I/O port address spaces, one of the I/O port address bits could be directly connected to the $\overline{CE}$ input. *Figure 27* illustrates this using an MM74C911. Whenever an OUT instruction is executed causing the $\overline{I/OW}$ (INS8080 write enable signal) to go low and the address is such that A7 is low, A0 A1 will select the digit to be written. If more decoding is required, some external gating logic may be added to the $\overline{CE}$ input.

The MM74C912/MM74C917 would be interfaced by connecting the A, B, C, D and DP to bit D0-D4 of the data bus and connecting K1-K3 to A_0-A_2. Writing data to these controllers would be the same as writing to the MM74C911.

B. Interfacing to the Z80™*

To connect these display controllers to the Z80 microprocessor, only a minor modification to the INS 8080 need be made. The Z80 control signals are slightly different from the INS8080. Instead of the INS8080 I/O write strobe, the Z80 has an I/O request line ($\overline{IOREQ}$), which goes low to indicate an I/O port is to be accessed, and a write ($\overline{WR}$) strobe which indicates that a memory or I/O write is to be done. By OR-ing, these together an equivalent $\overline{I/OW}$ signal is generated as shown in *Figure 28*.

C. Interfacing to the NSC800

The NSC800 has very different timing because the lower eight address bits and the data bus are multiplexed. But when connecting the display controllers as I/O ports, the interface is only slightly different from the INS8080 design. When an I/O instruction is executed, the port address that appears on A0-A7 is duplicated on A8-A15, and this address can be used directly. The controller $\overline{WE}$ input must be decoded from a $\overline{WR}$ (write enable) and $IO/\overline{M}$ (I/O or memory enable) as shown in *Figure 29*. Note that since the NSC800 is a CMOS microprocessor, no pull-up resistors are needed.

Figure 29 uses address bit A15 which is equivalent to bit A7 on the previous examples. As with the previous examples, if more address decoding is required, either gates or decoders could be connected to the $\overline{CE}$ input.

D. Interfacing To The 6800

When using the INS8080, Z80, or NSC800, these processors have separate I/O and memory address spaces. This usually allows simpler interfaces to be designed. The 6800 has no separate I/O addressing so I/O ports are usually mapped into a small block of memory. This requires more address decoding to ensure that memory and I/O don't overlap.

Figure 30 shows a DM8131 6-bit address bus comparator whose B_n inputs are a combination of A15-A12 address bits, the Φ_2 (6800 system clock) and the VMA (Valid Memory Access) control signal. When these inputs equal the corresponding T_n inputs, the output goes low. The 6800 R/$\overline{W}$ signal is connected to the $\overline{WE}$.

E. Interfacing To The INS8060/INS8070

Like the 6800, the INS8060/8070 series of microprocessors don't have any separate I/O addressing, so the MM74C911/MM74C912/MM74C917 must be memory addressed, but unlike the 6800 both the INS8070 series and the INS8060 have separate read/write strobes, which can simplify interfacing the display controllers. *Figure 31* illustrates a typical INS8060 interface. The $\overline{NWDS}$ (write enable) is directly connected to the MM74C912s $\overline{WE}$ input and the DM8131 provides the address decoding for the controller. The INS8060 has only 12 address bits (unless using paged addressing) so bits A_6-A_{11} are decoded by the comparator.

The INS8070 series microprocessor has the identical $\overline{NWDS}$ signal but has 16 address bits. Thus *Figure 31* would connect the A10-A15 address bits to the DM8131.

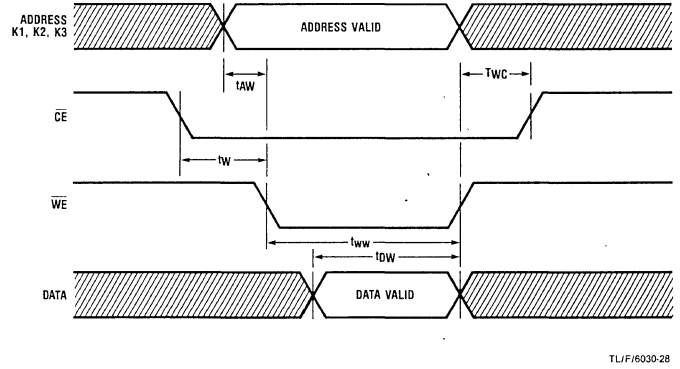


Figure 26. MM74C911/MM74C912/MM74C917 Timing Diagram (See data sheets for numbers)

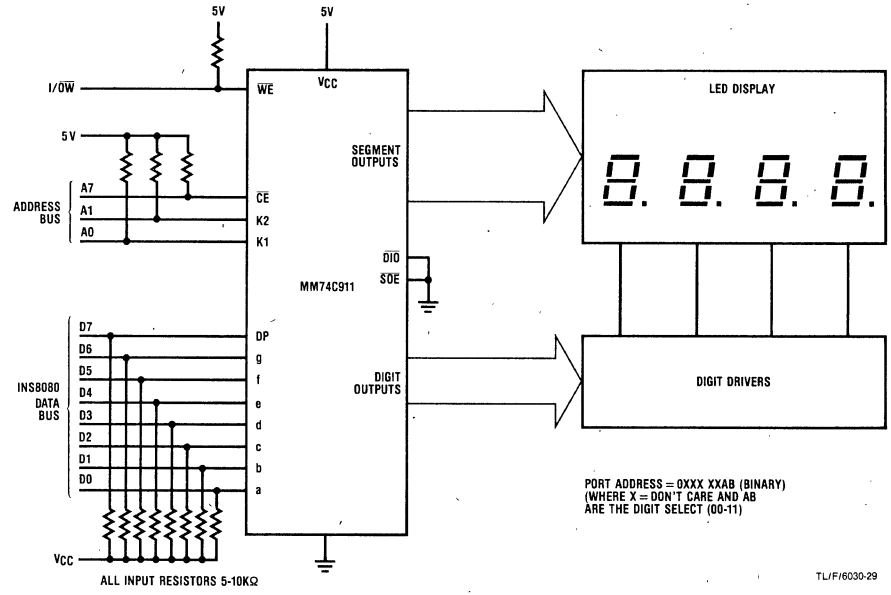


Figure 27. INS8080/INS8224/INS8238 Interface to MM74C911

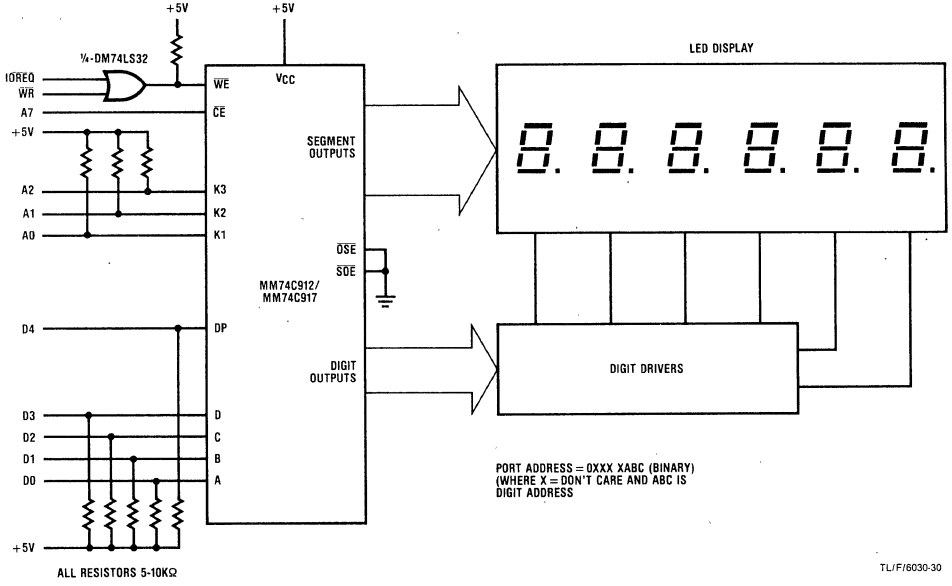


Figure 28. Z80 Interface to MM74C912/MM74C917

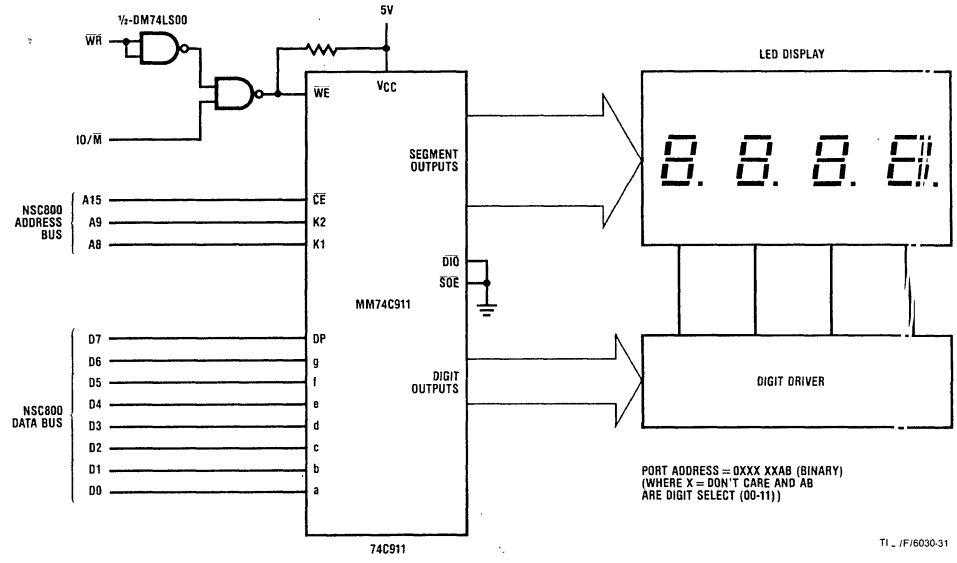


Figure 29. NSC800 Interface to MM74C911

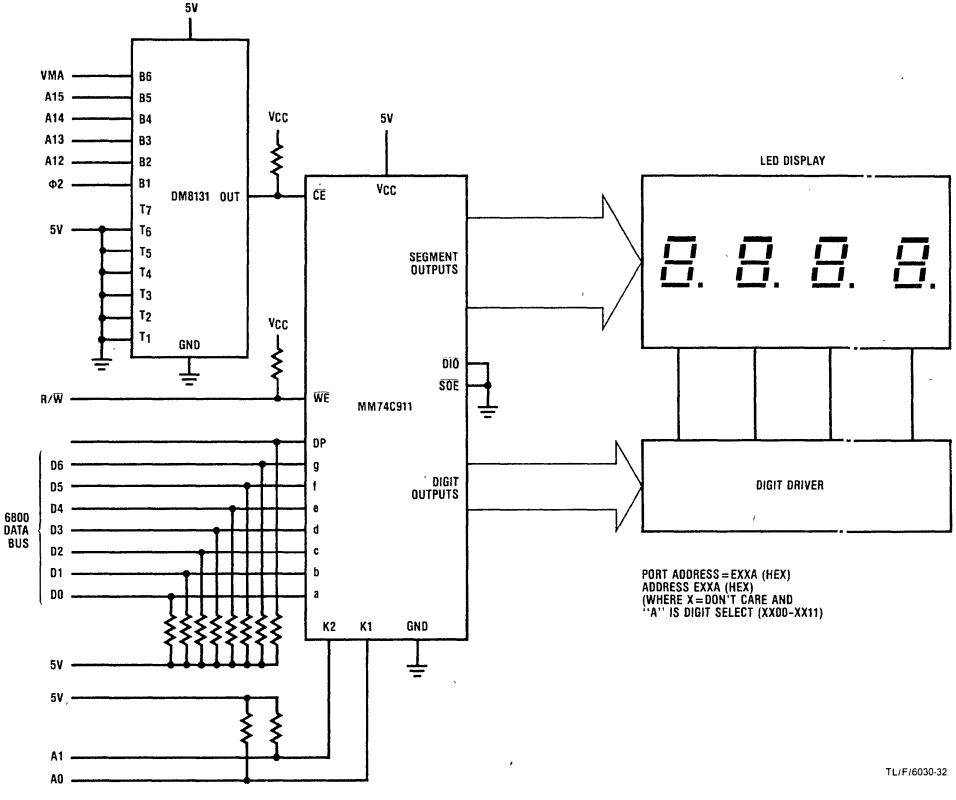


Figure 30. MM74C911 to 6800 Microprocessor Interface

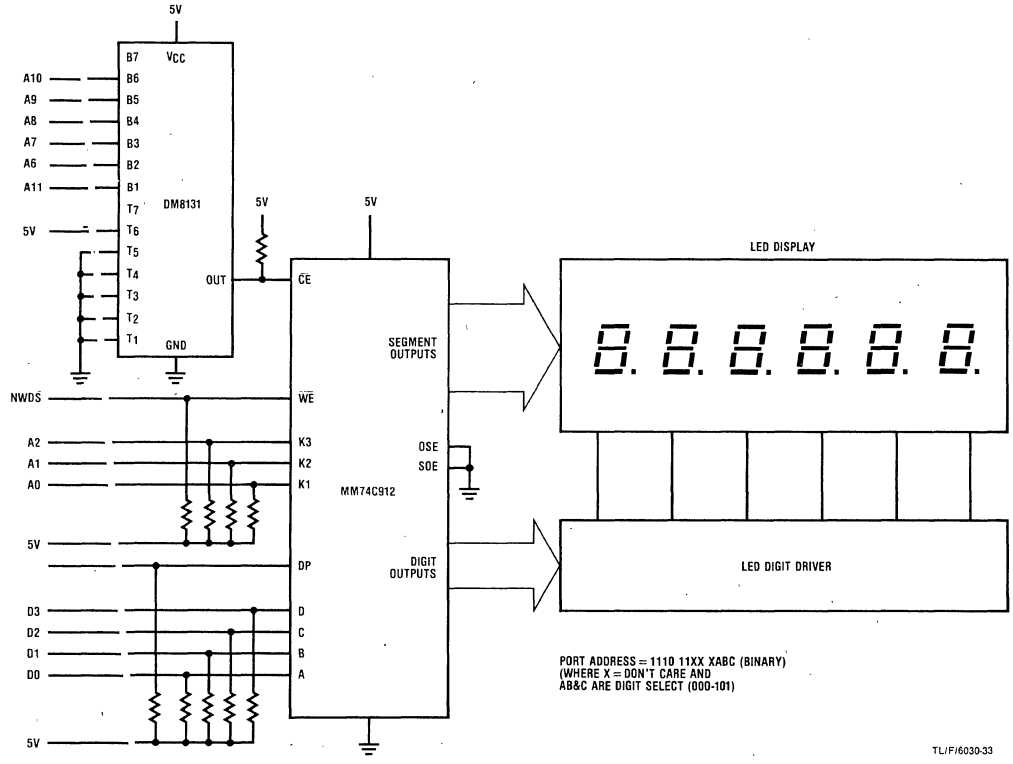


Figure 31. MM74C912/MM74C917 to INS8060 (SC/MP) Interface

F. Multiple Display Controllers

In systems where multiple display controllers are to be used, the simple addressing schemes of the previous examples may prove to be too costly in I/O capabilities, so some extra decoding is necessary to derive the $\overline{CE}$ signals. A typical method uses a 2-4 line decoder or a 3-8 line decoder. Where the total time from a stable address to the write pulse goes inactive is $\geqslant 1\mu S$, a CMOS decoder such as the MM74C42 or MM74C154 can be used, but if faster accessing is required, their LS equivalents should be employed.

Figure 32 shows a typical implementation of a 16-digit display using half of a DM74LS139 decoder to provide the $\overline{CE}$ signals for each controller.

G. Making The MM74C911/MM74C912/ MM74C917 Look Like RAM

So far, the discussion of addressing the controllers has been to separate the devices from memory, but there are certain advantages to not doing this. In many instances, microprocessor software requirements are such that data outputted to the controller also must be remembered by the microprocessor for later use. Since data cannot be read from the display controllers, the processor must also write the data in a spare register or a memory location. This extra writing and "book-keeping" software can be eliminated by addressing the MM74C911/MM74C912/MM74C917 over existing RAM. When data is written to the controller, it could also be stored in RAM simultaneously and can be read later by the CPU.

Figure 31 shows a simple example of this using an MM74C912 controller and two MM2114 1K × 4 memory chips. A DM74LS30 is used to detect when the last eight bytes of this memory is being accessed and enables the controller display. Thus, the last eight bytes of the RAM contains a duplicate copy of what the display controller is displaying.

IX. Conclusion

All three controllers provide simple and inexpensive interfaces to multiplexed multidigit displays. These devices are particularly well suited to microprocessor environments, but any type of CMOS compatible control hardware can be used. The MM74C911/MM74C912/ MM74C917 can most easily drive common anode displays. By providing most of the multiplex circuitry into one low-cost integrated circuit, the burden of designing discrete multiplexing has been eliminated.

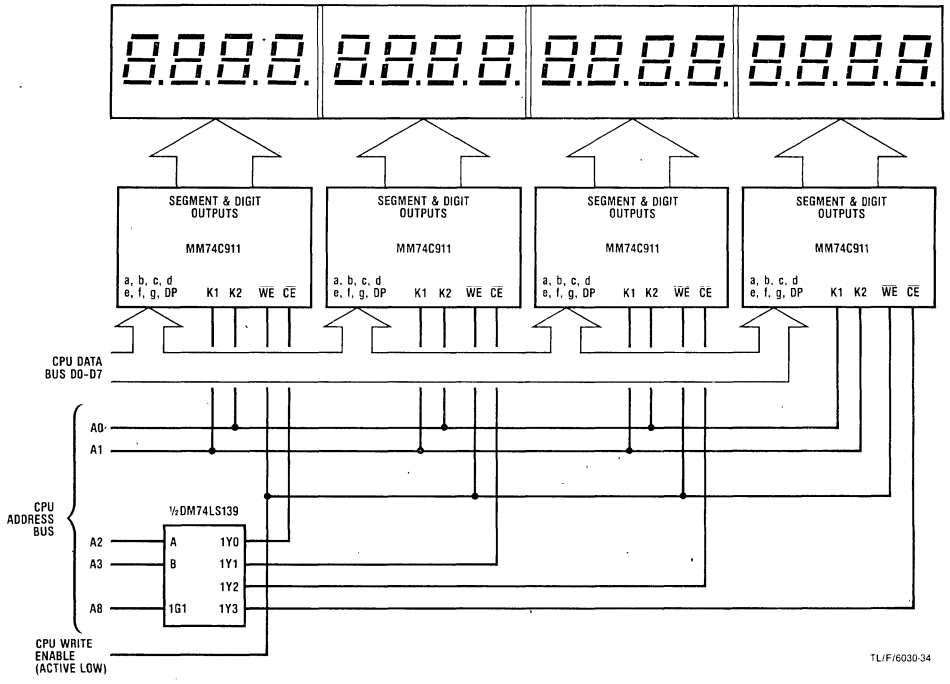


Figure 32. Multi-Digit Array

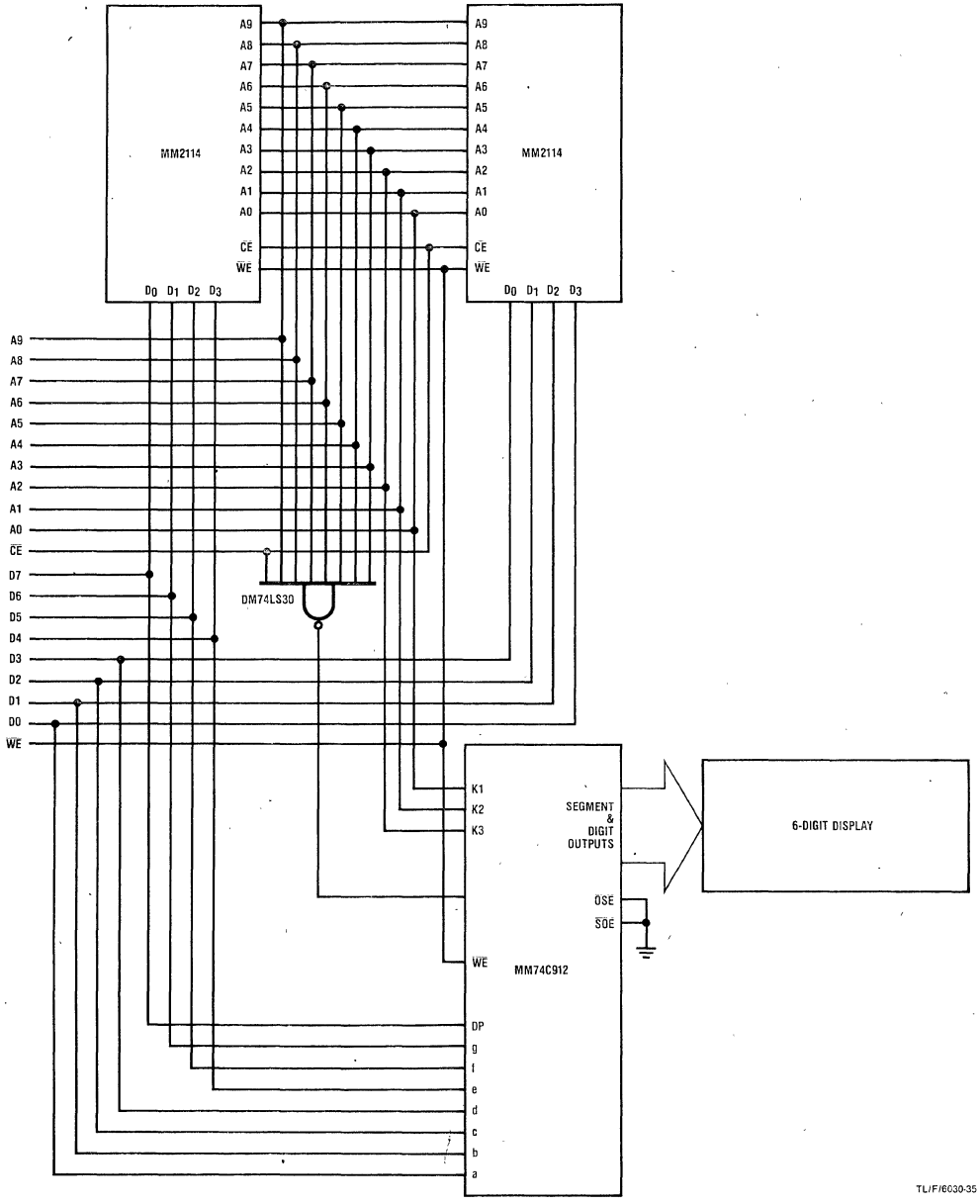


Figure 33. Display Controller Mapped Over RAM (5-10 KΩ Pull-up Resistors may be needed on MM74C912 inputs)

HC-MOS Power Dissipation

National Semiconductor
Application Note 303
Kenneth Karakotsios
February 1984

If there is one single characteristic that justifies the existence of CMOS, it is low power dissipation. In the quiescent state, high-speed CMOS draws five to seven orders of magnitude less power than the equivalent LSTTL function. When switching, the amount of power dissipated by both metal gate and high-speed silicon gate CMOS is directly proportional to the operating frequency of the device. This is because the higher the operating frequency, the more often the device is being switched. Since each transition requires power, power consumption increases with frequency.

First, one will find a description of the causes of power consumption in HC-CMOS and LSTTL applications. Next will follow a comparison of MM54HC/MM74HC to LSTTL power dissipation. Finally, the maximum ratings for power dissipation imposed by the device package will be discussed.

Quiescent Power Consumption

Ideally, when a CMOS integrated circuit is not switching, there should be no DC current paths from V_{CC} to ground, and the device should not draw any supply current at all. However, due to the inherent nature of semiconductors, a small amount of leakage current flows across all reverse-biased diode junctions on the integrated circuit. These leakages are caused by thermally-generated charge carriers in the diode area. As the temperature of the diode increases, so do the number of these unwanted charge carriers, hence leakage current increases.

Leakage current is specified for all CMOS devices as I_{CC}. This is the DC current that flows from V_{CC} to ground when all inputs are held at either V_{CC} or ground, and all outputs are open. This is known as the quiescent state.

For the MM54HC/MM74HC family, I_{CC} is specified at ambient temperatures (T_A) of 25°C, 85°C, and 125°C. There are three different specifications at each temperature, depending on the complexity of the device. The number of diode junctions grows with circuit complexity, thereby increasing the leakage current. The worst case I_{CC} specifications for the MM54HC/MM74HC family are summarized in Table I. In addition, it should be noted that the maximum I_{CC} current will decrease as the temperature goes below 25°C.

TABLE I. Supply Current (I_{CC}) for MM54HC/MM74HC Specified at $V_{CC}=6V$

T_A	Gate	Buffer	MSI	Unit
25°C	2.0	4.0	8.0	μA
85°C	20	40	80	μA
125°C	40	80	160	μA

To obtain the quiescent power consumption for any CMOS device, simply multiply I_{CC} by the supply voltage:

$$P_{DC}=I_{CC}V_{CC}$$

Sample calculations show that at room temperature the maximum power dissipation of gate, buffer, and MSI circuits at $V_{CC}=6V$ are 10 μW, 20 μW, and 40 μW, respectively.

Dynamic Power Consumption

Dynamic power consumption is basically the result of charging and discharging capacitances. It can be broken down into three fundamental components, which are:

1. Load capacitance transient dissipation
2. Internal capacitance transient dissipation
3. Current spiking during switching.

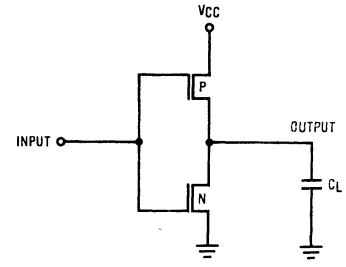
Load Capacitance Transient Dissipation

The first contributor to power consumption is the charging and discharging of external load capacitances. *Figure 1* is a schematic diagram of a simple CMOS inverter driving a capacitive load. A simple expression for power dissipation as a function of load capacitance can be derived starting with:

$$Q_L=C_LV_{CC}$$

where C_L is the load capacitance, and Q_L is the charge on the capacitor. If both sides of the equation are divided by the time required to charge and discharge the capacitor (one period, T, of the input signal), we obtain:

$$\frac{Q_L}{T}=C_LV_{CC}\left(\frac{1}{T}\right)$$



TL/L/5021–1

FIGURE 1. Simple CMOS Inverter Driving a Capacitive External Load

Since charge per unit time is current ($Q_L/T=I$) and the inverse of the period of a waveform is frequency ($1/T=f$):

$$I_L=C_LV_{CC}f$$

To find the power dissipation, both sides of the equation must be multiplied by the supply voltage ($P=VI$), yielding:

$$P_L=C_L\,V_{CC}{}^2f$$

One note of caution is in order. If all the outputs of a device are not switching at the same frequency, then the power consumption must be calculated at the proper frequency for each output:

$$P_L = V_{CC}^2(C_{L1}f_1 + C_{L2}f_2 + \ldots + C_{Ln}f_n).$$

Examples of devices for which this may apply are: counters, dual flip-flops with independent clocks, and other integrated circuits containing dual, triple, etc., independent circuits.

Internal Capacitance Transient Dissipation

Internal capacitance transient dissipation is similar to load capacitance dissipation, except that the internal parasitic "on-chip" capacitance is being charged and discharged. *Figure 2* is a diagram of the parasitic nodal capacitances associated with two CMOS inverters.

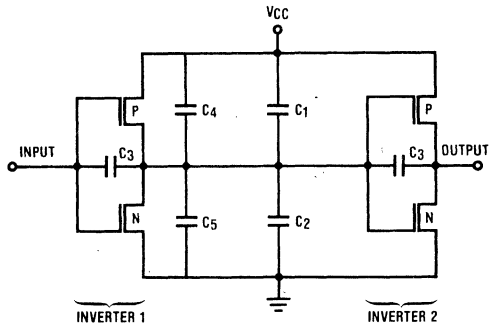


FIGURE 2. Parasitic Internal Capacitances Associated with Two Inverters

C_1 and C_2 are capacitances associated with the overlap of the gate area and the source and channel regions of the P- and N-channel transistors, respectively. C_3 is due to the overlap of the gate and source (output), and is known as the Miller capacitance. C_4 and C_5 are capacitances of the parasitic diodes from the output to V_{CC} and ground, respectively. Thus the total internal capacitance seen by inverter 1 driving inverter 2 is:

$$C_I = C_1 + C_2 + 2C_3 + C_4 + C_5$$

Since an internal capacitance may be treated identically to an external load capacitor for power consumption calculations, the same equation may be used:

$$P_I = C_I V_{CC}^2 f$$

At this point, it may be assumed that different parts of the internal circuitry are operating at different frequencies. Although this is true, each part of the circuit has a fixed frequency relationship between it and the rest of the device. Thus, one value of an effective C_I can be used to compute the internal power dissipation at any frequency. More will be said about this shortly.

Current Spiking During Switching

The final contributor to power consumption is current spiking during switching. While the input to a gate is making a transition between logic levels, both the P- and N-channel transistors are turned partially on. This creates a low impedance path for supply current to flow from V_{CC} to ground, as illustrated in *Figure 3*.

For fast input rise and fall times (shorter than 50 ns for the MM54HC/MM74HC family), the resulting power consumption is frequency dependent. This is due to the fact that the more often a device is switched, the more often the input is situated between logic levels, causing both transistors to be partially turned on. Since this power consumption is proportional to input frequency and specific to a given device in any application, as is C_I, it can be combined with C_I. The resulting term is called "C_{PD}," the no-load power dissipation capacitance. It is specified for every MM54HC/MM74HC device in the AC Electrical Characteristic section of each data sheet.

It should be noted that as input rise and fall times become longer, the switching current power dissipation becomes more dependent on the amount of time that both the P- and N-channel transistors are turned on, and less related to C_{PD} as specified in the data sheets. *Figure 4* is a representation of the effective value of C_{PD} as input rise and fall times increase for the MM54HC/MM74HC08, MM54HC/MM74HC139, and MM54HC/MM74HC390. To get a fair comparison between the three curves, each is divided by the value of C_{PD} for the particular device with fast input rise and fall times. This is represented by "C_{PD0}," the value of C_{PD} specified in the data sheets for each part. This comparison appears in *Figure 5*. C_{PD} remains constant for input rise and fall times up to about 20 ns, after which it rises, approaching a linear slope of 1. The graphs do not all reach a slope of 1 at the same time because of necessary differences in circuit design for each part. The MM54HC/MM74HC08 exhibits the greatest change in C_{PD}, while the MM54HC/MM74HC139 shows less of an increase in C_{PD} at

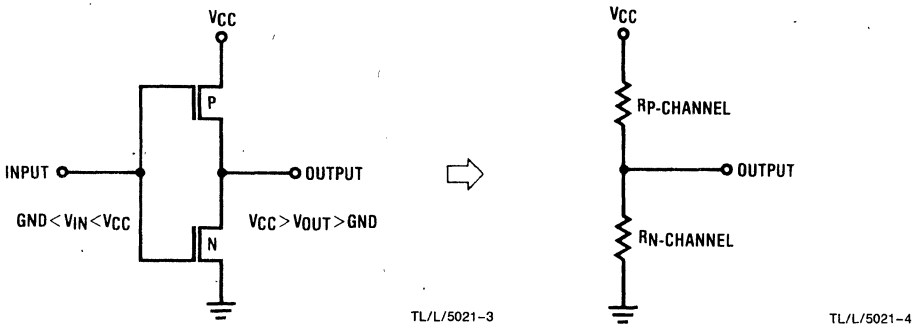
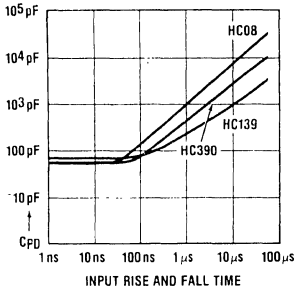


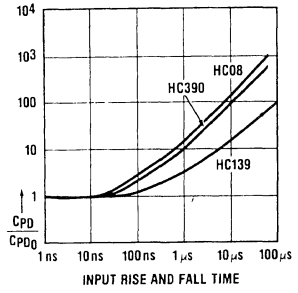
FIGURE 3. Equivalent schematic of a CMOS inverter whose input is between logic levels

any given frequency. Thus, the power dissipation for most of the parts in the MM54HC/MM74HC family will fall within these two curves. One notable exception is the MM54HC/MM74HCU04.



TL/L/5021–5

FIGURE 4. Comparison of Typical C_{PD} for MM54HC/MM74HC08, MM54HC/MM74HC139 MM54HC/MM74HC390 as a Function of Input Rise and Fall Time. $t_{rise} = t_{fall}$, $V_{CC} = 5V$, $T_A = 25°C$



TL/L/5021–6

FIGURE 5. Normalized Effective C_{PD} (Typical) for Slow Input Rise and Fall Times. $t_{rise} = t_{fall}$, $V_{CC} = 5V$, $T_A = 25°C$

Inputs that do not pull all the way to V_{CC} or ground can also cause an increase in power consumption, for the same reason given for slow rise and fall times. If the input voltage is between the minimum input high voltage and V_{CC}, then the input N-channel transistor will have a low impedance (i.e., be "turned on") as expected, but the P-channel transistor will not be completely turned off. Similarly, if the input is between ground and the maximum input low voltage, the P-channel transistor will be fully on and the N-channel transistor will be partially on. In either case, a resistive path from V_{CC} to ground will occur, resulting in an increase in power consumption.

Combining all the derived equations, we arrive at the following:

$$P_{TOTAL} = (C_L + C_{PD})V_{CC}^2 f + I_{CC}V_{CC}$$

This equation can be used to compute the total power consumption of any MM54HC/MM74HC device, as well as any other CMOS device, at any operating frequency. It includes both DC and AC contributions to power usage. C_{PD} and I_{CC} are supplied in each data sheet for the particular device, and V_{CC} and f are determined by the particular application.

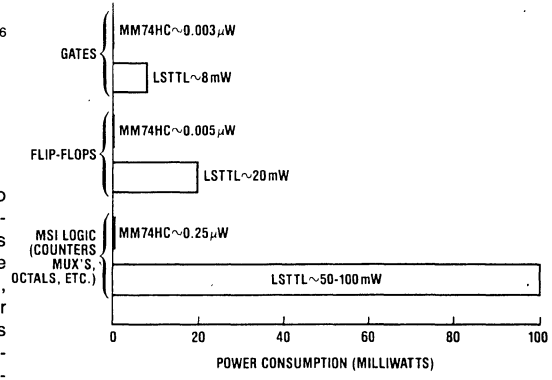
Comparing HC-CMOS to LSTTL

Although power consumption is somewhat dependent on frequency in LSTTL devices, the majority of power dissipated below 1 MHz is due to quiescent supply current. LSTTL contains many resistive paths from V_{CC} to ground, and even when it is not switching, it draws several orders of magnitude greater supply current than HC-CMOS. *Figure 6* is a bar graph comparison of quiescent power requirements $(V_{CC}) \times (I_{CC})$ between LSTTL and HC-CMOS devices.

The reduction in CMOS power consumption as compared to LSTTL devices is illustrated in *Figures 7* and *8*. These graphs are comparisons of the typical supply current (I_{CC}) required for equivalent functions in MM54HC/MM74HC, MM54HC/MM74C, CD4000, and 54LS/74LS logic families. The currents were measured at room temperature (25°C) with a supply voltage of 5V.

Figure 7 represents the supply current required for a quad NAND gate with one gate in the package switching. The MM54HC/MM74HC family draws slightly more supply current than the 54C/74C and CD4000 series. This is mainly due to the large size of the output buffers necessary to source and sink currents characteristic of the LSTTL family. Other reasons include processing differences and the larger internal circuitry required to drive the output buffers at high frequencies. The frequency at which the CMOS device draws as much power as the LSTTL device, known as the power cross-over-frequency, is about 20 MHz.

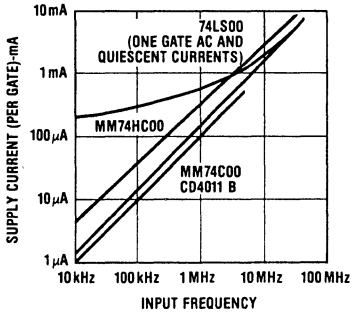
In *Figure 8*, which is a comparison of equivalent flip-flops (174) and shift registers (164) from the different logic families, the power cross-over frequency again occurs at about 20 MHz.



TL/L/5021–7

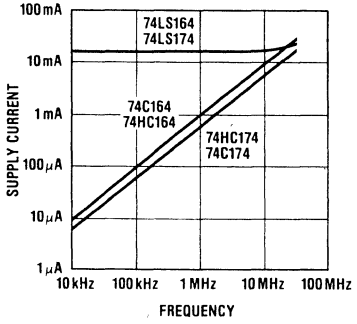
FIGURE 6. High Speed CMOS (HC-CMOS) vs. LSTTL Quiescent Power Consumption

The power cross-over frequency increases as circuit complexity increases. There are two major reasons for this. First, having more devices on an LSTTL integrated circuit means that more resistive paths between V_{CC} and ground will occur, and more quiescent current will be required. In a CMOS integrated circuit, although the supply leakage current will increase, it is of such a small magnitude (nanoAmps per device) that there will be very little increase in total power consumption.



TL/L/5021–8

FIGURE 7. Supply Current vs. Input Frequency for Equivalent NAND Gates



TL/L/5021–9

FIGURE 8. Supply Current vs. Frequency

Secondly, as system complexity increases, the precentage of the total system operating at the maximum frequency tends to decrease. *Figure 9* shows block diagrams of a CMOS and an equivalent LSTTL system. In this abstract system, there is a block of parts operating at the maximum frequency (F_{max}), a block operating at half F_{max}, a block operating at one quarter F_{max}, and so on. Let us call the power consumed in the first section P1. In a CMOS system, since power consumption is directly proportional to the operating frequency, the amount of power consumed by the second block will be (P1)/2, and the amount used in the third section will be (P1)/4. If the power consumed over a large number of blocks is summed up, we obtain:

$$P_{TOTAL} = P1 + (P1)/2 + (P1)/4 + \ldots + (P1)/(2^{n-1})$$

and $P_{TOTAL} \leq 2(P1)$

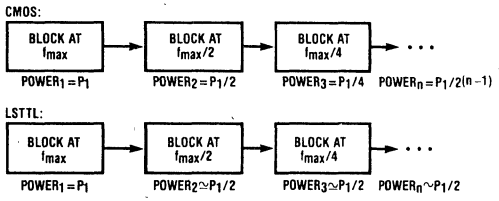
Now consider the LSTTL system. Again, the power consumed in the first block is P1. The amount of power dissipated in the second block is something less than P1, but greater than (P1)/2. For simplicity, we can assume the best case, that P2 = (P1)/2. The power consumption for all system blocks operating at frequencies $F_{max}/2$ and below will be dominated by quiescent current, which will not change with frequency. The power used by blocks 3 through n will be approximately equal to the power dissipated by block 2, (P1)/2. The total power consumed in the LSTTL system is:

$$P_{TOTAL} = (P1 + (P1)/2 + (P1)/2 + \ldots + (P1)/2$$

$$P_{TOTAL} = P1 + (N-1)(P1)/2$$

and for $n > 2$, $P_{TOTAL} > 2(P1)$

Thus, an LSTTL system will draw more power than an equivalent HC-CMOS system.



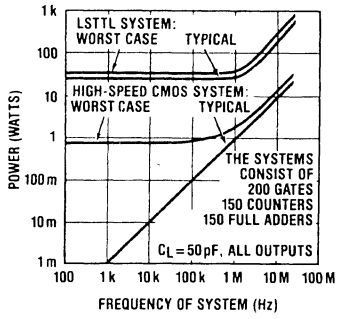
TL/L/5021–10

FIGURE 9. Comparison of Equivalent CMOS and LSTTL Systems

This effect is further illustrated in *Figure 10*. An arbitrary system is composed of 200 gates, 150 counters, and 150 full adders, with 50 pF loads on all of the outputs. The supply voltage is 5V, and the system is at room temperature. For this system, the worst case power consumption for CMOS is about an order of magnitude lower than the typical LSTTL power requirements. Thus, as system complexity increases, CMOS will save more power.

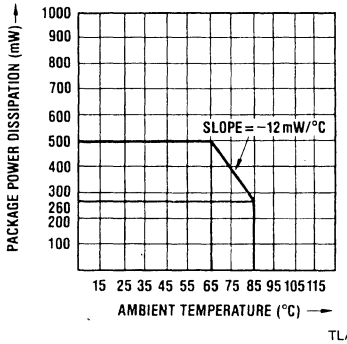
Maximum Power Dissipation Limits

It is important to take into consideration the maximum power dissipation limits imposed on a device by the package when designing with high-speed CMOS. Both the plastic and ceramic packages can dissipate up to 500 mW. Although this limit will rarely be reached in typical high-speed applications, the MM54HC/MM74HC family has such large output current source and sink capabilities that driving a resistive load could possibly take a device to the 500 mW limit. This maximum power dissipation rating should be derated by −12 mW/°C, starting at 65°C for the plastic package and 100°C for the ceramic package. This is illustrated in *Figures 11* and *12*. Thus, if a device in a plastic package is operating at 70°C, then the maximum power dissipation rating would be 500 mW — (70°C—65°C) (12 mW/°C) = 44 mW. Note that the maximum ambient temperature is 85°C for plastic packages and 125°C for ceramic packages.



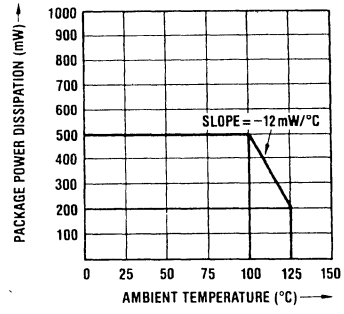
TL/L/5021–11

FIGURE 10. System Power vs. Frequency MMHC74HC vs. LSTTL



TL/L/5021–12

FIGURE 11. Plastic Package (MM74HC) High Temperature Power Derating for MM54HC/MM74HC Family



TL/L/5021–13

FIGURE 12. Ceramic Package (MM54HC) High Temperature Power Derating for MM54HC/MM74HC Family

Summary

The MM54HC/MM74HC high-speed silicon gate CMOS family has quiescent (standby) power consumption five to seven orders of magnitude lower than the equivalent LSTTL function. At high frequencies (30 MHz and above), both families consume a similar amount of power for very simple systems. However, as system complexity increases, HC-CMOS uses much less power than LSTTL. To keep power consumption low, input rise and fall times should be fast (less than 50 to 100 ns) and inputs should swing all the way to V_{CC} and ground.

There is an easy-to-use equation to compute the power consumption of any HC-CMOS device in any application:

$$P_{TOTAL} = (C_L + C_{PD})V_{CC}^2 f + I_{CC}V_{CC}$$

The maximum power dissipation rating is 500 mW per package at room temperature, and must be derated as temperature increases.

High-Speed CMOS (MM54HC/MM74HC) Processing

National Semiconductor
Application Note 310
Kenneth Karakotsios
June 1983

The MM54HC/MM74HC logic family achieves its high speed by utilizing microCMOS Technology. This is a 3.5 silicon gate P-well CMOS process single layer poly, single layer metal, P-well process with oxide-isolated transistors. Why do silicon-gate transistors (polycrystalline) switch faster than metal-gate transistors? The reason is related both to the parasitic capacitances inherent in integrated circuits and the gain of the transistors. The speed at which an MOS transistor can switch depends on how fast its internal parasitic capacitance, as well as its external load capacitance, can be charged and discharged. Capacitance takes time to be charged and discharged, and hence degrades a transistor's performance. The gain of a transistor is a measure of how well a transistor can charge and discharge a capacitor. Therefore, to increase speed, it is desirable to both decrease parasitic capacitance and increase transistor gain. These advantages are achieved with National's silicon-gate CMOS process. To understand exactly how these improvements occur in silicon-gate CMOS, it is helpful to compare the process to the metal-gate CMOS process.

Metal-Gate CMOS Processing

Figure 1 through *12* are cross sections of a metal-gate CMOS pair of P- and N-channel transistors with associated guard rings. Guard rings are necessary in metal-gate processing to prevent leakage currents between the sources and drains of separate transistors. The starting material is an N− type silicon substrate covered by a thin layer of thermally grown silicon dioxide (SiO_2) (*Figure 1*). Silicon dioxide, also called oxide acts as both a mask for certain processing steps and a dielectric insulator. *Figure 2* shows the addition of a lightly doped P− well in which the N-channel transistors and P+ guard rings will later be located. The P− well is ion implanted into the substrate. A thin layer of oxide allows ions to be implanted through it, while a thicker oxide will block ion implantation.

Next, the oxide over the P− well is stripped, and a new layer of oxide is grown. Following this, holes are etched into the oxide where the P+ source, drain, and guard ring diffusions shall occur. The P+ regions are diffused, and then additional oxide is grown to fill the holes created for diffusion (*Figures 3, 4,* and *5*). The following step is to cut holes in the oxide to diffuse the N-channel sources, drains and guard bands. Then oxide is again thermally grown (*Figures 6* and *7*).

In the following step, the composite mask is created by again cutting holes in the oxide. This defines the areas where contacts and transistor gates will occur (*Figure 8*). A thin layer of gate oxide is grown over these regions (*Figure 9*), and alignment of this to the source and drain regions is a critical step. If the gate oxide overlaps the source or drain, this will cause additional parasitic capacitance.

Contacts to transistor sources and drains are cut into the thin oxide where appropriate (*Figure 10*), and then the interconnect metal is deposited (*Figure 11*). Depositing the metal over the gate areas is also a critical step, for a misalignment will cause extra unwanted overlap capacitance. *Figure 12* illustrates the final step in processing, which is to deposit an insulating layer of silicon dioxide over the entire surface of the integrated circuit.

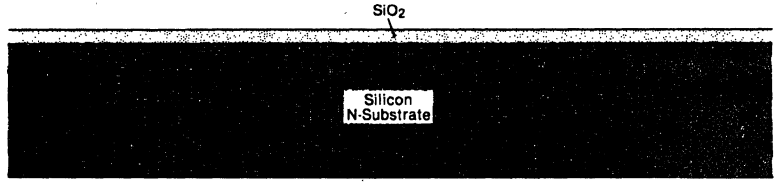
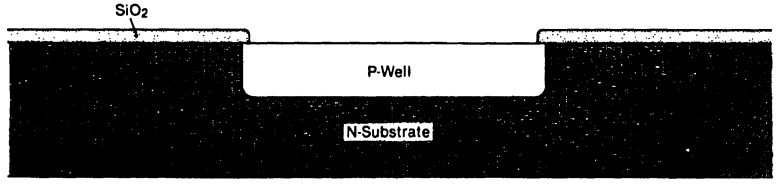


FIGURE 1. Initial Oxidation, Thermally Grown Silicon Dioxide Layer on Silicon Substrate Surface



TL/L/5044–1

FIGURE 2. P− Mask and Formation of P− Well Tub in Which N-Channel Devices Will Be Located

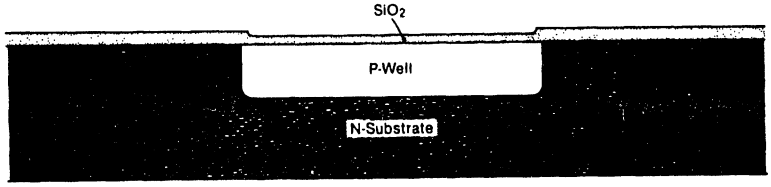


FIGURE 3. P− Well Oxidation, Thermally Grown Silicon Dioxide Layer Over P− Well Area

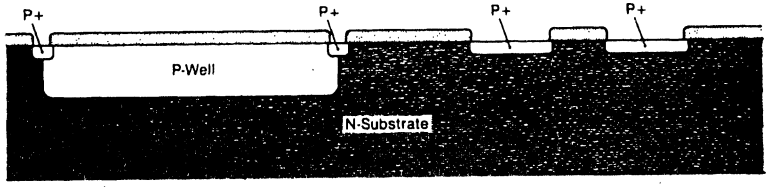
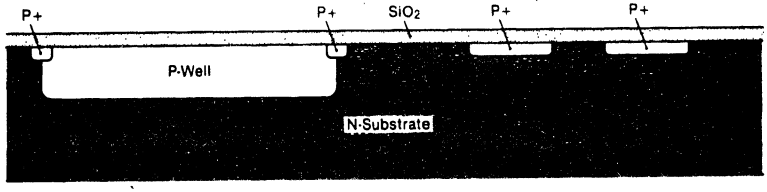


FIGURE 4. P + Mask and Formation of Low Resistance P + Type Pockets in P− Well and N-Substrate



TL/L/5044–2

FIGURE 5. P + Oxidation, Thermally Grown Silicon Dioxide Layer Over P+ Type Pockets

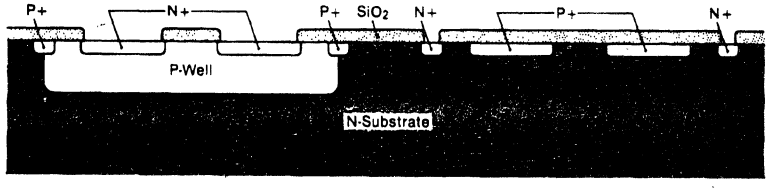
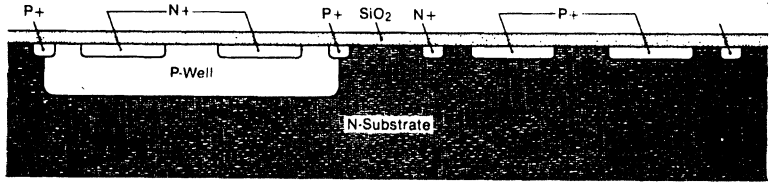


FIGURE 6. N + Mask and Formation of Low Resistance N + Type Pockets in P− Well and N-Substrate



TL/L/5044–3

FIGURE 7. N + Oxidation, Thermally Grown Silicon Dioxide Layer Over N + Type Pockets

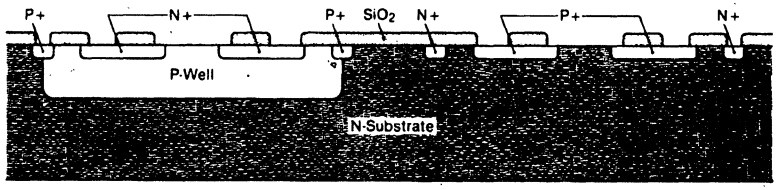


FIGURE 8. Composite Mask and Openings to N- and P-Channel Devices

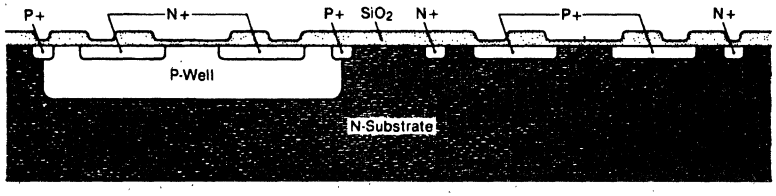
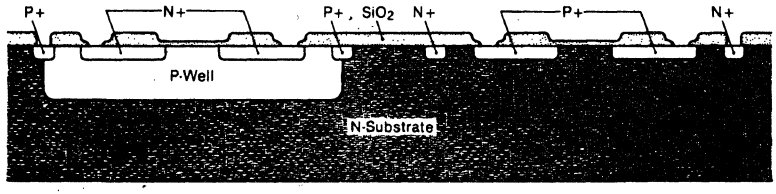


FIGURE 9. Gate Oxidation, Thermally Grown Silicon Dioxide Layer Over N- and P-Channel Devices



TL/L/5044–4

FIGURE 10. Contact Mask and Openings to N- and P-Channel Devices

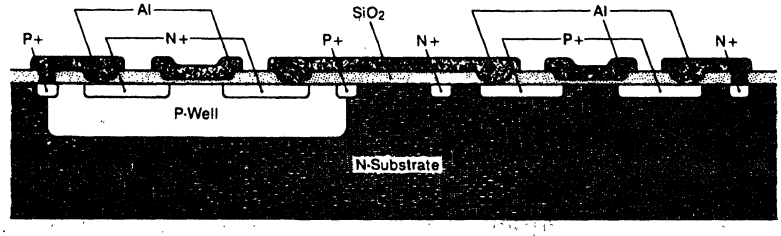
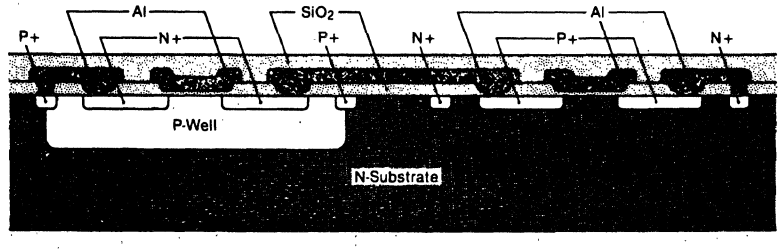


FIGURE 11. Metallization, Metal Mask, Resulting in Gate Metal and Metal Interconnects



TL/L/5044–5

FIGURE 12. Passivation Oxide, Deposited Silicon Dioxide Over Entire Die Surface

Silicon-Gate CMOS Processing

The silicon-gate CMOS process starts with the same two steps as the metal-gate process, yielding an N− substrate with an ion-implanted P− well (*Figures 13* and *14*). That, however, is where the similarity ends. Next, the initial oxide is stripped, and another layer of oxide, called pad oxide, is thermally grown. Also, a layer of silicon nitride is deposited across the surface of the wafer (*Figure 15*). The nitride prevents oxide growth on the areas it covers. Thus, in *Figure 16*, the nitride is etched away wherever field oxide is to be grown. The field oxide is a very thick layer of oxide, and it is grown everywhere except in the transistor regions (*Figure 17*). As an oxide grows in silicon, it consumes the silicon substrate beneath it and combines it with ambient oxygen to produce silicon dioxide. Growth of this very thick oxide causes the oxide to be recessed below the surface of the silicon substrate by a significant amount. A recessed field oxide eliminates the need for guard ring diffusions, because current cannot flow through the field oxide, which completely isolates each transistor from every other transistor.

The next step is to deposit a layer of polycrystalline silicon, also called poly, which will form both the gate areas and a second layer of interconnect (*Figure 18*). The poly is then etched, and any poly remaining becomes a gate if it is over gate oxide, and interconnect if it is over field oxide. A new layer of oxide is grown over the poly, which will act as an insulator between the poly and the metal interconnect (*Figure 19*). The poly over the transistor areas is not as wide as the gate oxide. This allows the source and drain diffusions to be ion implanted through the gate oxide. The poly gate itself, along with the field oxide, is used as a mask for implantation. Therefore, the source and drain implants will automatically be aligned to the gate poly, which is what makes this process a self-aligned gate process (*Figure 20*).

Figure 21 illustrates the steps of cutting contacts into the insulating layer of oxide, so the metal may be connected to gate and field poly, as well as to source and drain implants. A layer of metal is deposited across the entire wafer, and is etched to produce the desired interconnection. Finally, as in metal-gate processing, an insulating layer of oxide is deposited onto the wafer (*Figure 22*).

Advantages of Silicon-Gate Processing

There are three major ways in which silicon-gate processing reduces parasitic capacitance: recessed field oxide, lower gate overlap capacitance, and shallower junction depths. *Figures 23* and *24* are cross sections of metal gate and silicon gate CMOS circuits, respectively. These figures show the parasitic on-chip capacitances (C_1 through C_4) for each type of process.

The N+ and P+ source and drain regions, as well as guard ring regions, in the metal-gate process, have two capacitances associated with them: periphery and area capacitances (C_2 and C_1). These capacitances are associated with the diode junctions between the P+ regions and the N− substrate, as well as the N+ regions and P− well. The finer line widths of silicon-gate CMOS, coupled with the shallower junction depths, act to decrease the size of these parasitic diodes. Capacitance is proportional to diode area, hence the diode area reduction results in a significantly reduced parasitic capacitance in silicon-gate CMOS.

Another origin of unwanted capacitance is the area where the gate overlaps the source and drain regions (C_4). The overlap is much larger in metal-gate processing than in silicon-gate CMOS. This is due to the fact that the metal-gate must be made wider than the channel width to allow for alignment tolerances. In silicon-gate processing, since the gate acts as the mask for the ion implantation of the source and drain regions, there is no alignment error, which results in greatly reduced overlap.

How does the use of polysilicon gates increase the gain of a MOSFET? Polysilicon may be etched to finer line widths than metal, permitting the fabrication of transistors with shorter gate lengths. The equation that describes the gain of a MOSFET is shown below:

$$I = \frac{(\text{Beta})\ (\text{Width})}{2\ (\text{Length})}\ [(\text{Gate Voltage}) - (\text{Threshold Voltage})]^2$$

Thus, a decrease in gate length will cause an increase in current drive capability. This, in turn, will allow the transistor to charge a capacitance more rapidly, therefore increasing the gain of the transistor. Also, the gate oxide is thinner for the silicon-gate CMOS process. A thinner gate oxide increases the Beta term in the equation, which further increases gain. Finally, although it is not apparent from the processing cross sections, the transistor threshold (turn on) voltage is lower. This is accomplished by the use of ion implants to adjust the threshold.

There is one more advantage of silicon-gate processing that should be noted: the polysilicon provides for an additional layer of interconnect. This allows three levels of interconnect, which are metal, polysilicon, and the N+ and P+ ion-implanted regions. Having these three levels helps to keep the die area down, since much die area is usually taken up by interconnection.

When all these advantages are summed up, the result is a CMOS technology that produces devices as fast as the equivalent LSTTL device. *Figure 25* illustrates a comparison between the MM74HC00 buffered NAND gate and the MM74C00, CD4011B, and DM74LS00 NAND gates. The MM74HC00 is about an order of magnitude faster than the CD4011B buffered NAND gate, and about 5 times faster than the unbuffered MM74C00, at 15 pF. As load capacitance increases, the speed differential between metal-gate and silicon-gate CMOS increases, with the MM74HC00 operating as fast as the DM74S00 at any load capacitance.

Summary

Polycrystalline silicon-gate CMOS has many advantages over metal-gate CMOS. It is faster because on-chip parasitic capacitances are reduced and transistor gains are increased. This is due mainly to a recessed field oxide and a self-aligned gate process. Transistor gains are increased by decreasing transistor lengths and threshold voltages, and increasing beta. Polysilicon also allows for an extra layer of interconnect, which helps to keep die area down.

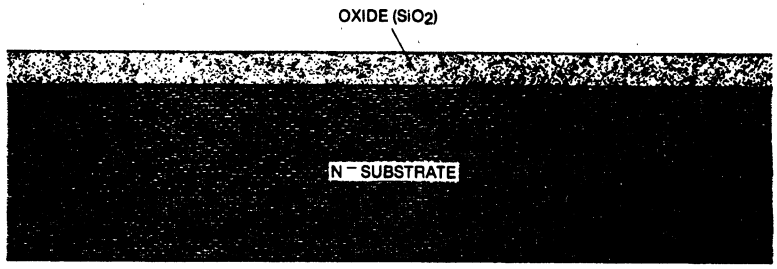
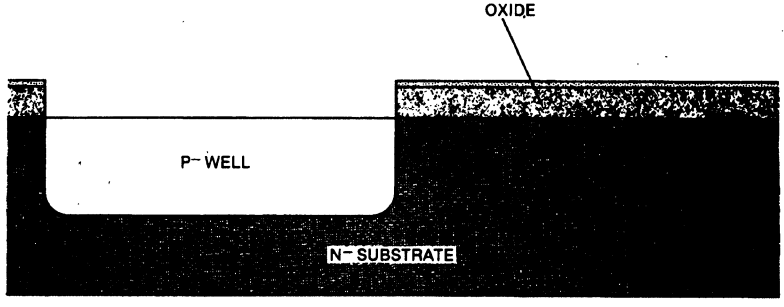
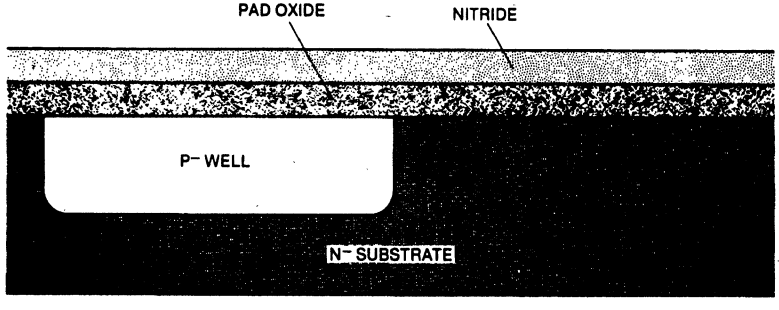


FIGURE 13. Initial Oxidation, Thermally Grown Silicon Dioxide on N− Silicon Substrate



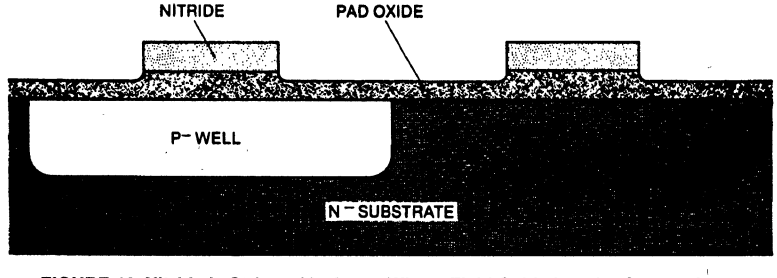
TL/L/5044–6

FIGURE 14. Ion-Implanted P− Tub in Which N-Channel Devices Will Be Located



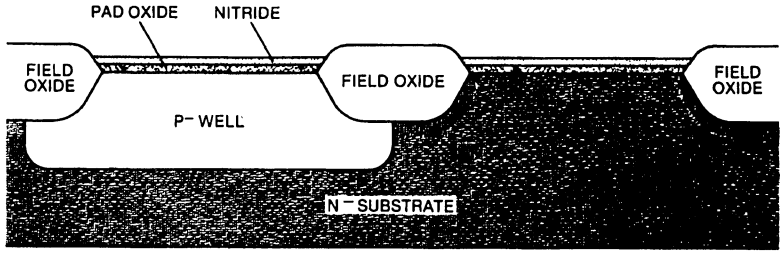
TL/L/5044–15

FIGURE 15. Initial Oxide Is Stripped, Pad Oxide Is Thermally Grown, and a Layer of Silicon Nitride Is Deposited Across the Surface of the Wafer



TL/L/5044–16

FIGURE 16. Nitride Is Stripped in Areas Where Field Oxide Is to be Grown. Areas Covered by Nitride Will Become Transistor Area



TL/L/5044–8

FIGURE 17. Field Oxide Is Thermally Grown. The Nitride Acts as a Barrier to Oxide Growth

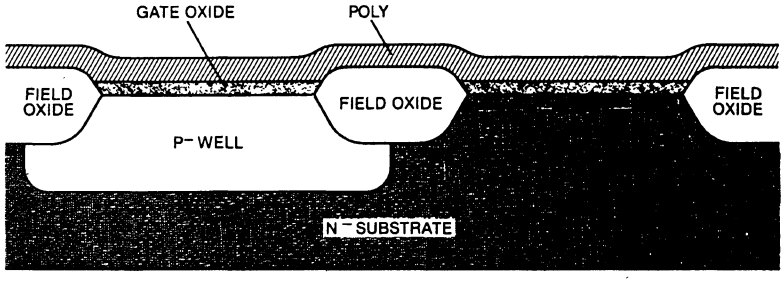
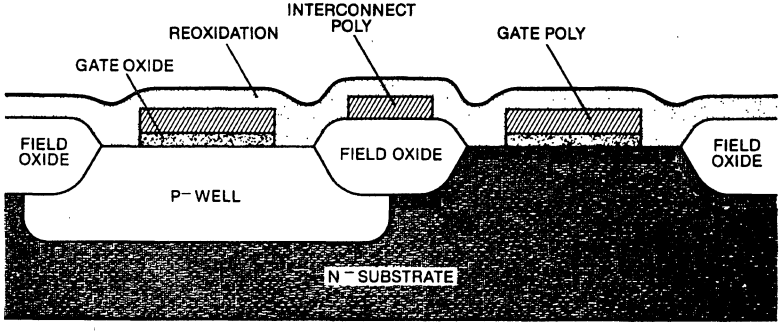


FIGURE 18. Nitride Is Stripped, Pad Oxide Is Stripped Over Transistor Areas and a Thin Gate Oxide Is Grown Polycrystalline Silicon Is Deposited



TL/L/5044–9

FIGURE 19. Polysilicon Layer Is Etched to Provide Gate and Interconnect Poly Areas. New Layer of Oxidation Is Grown

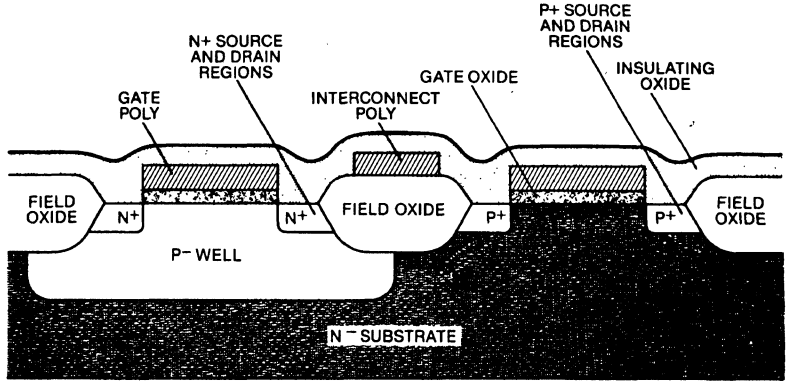
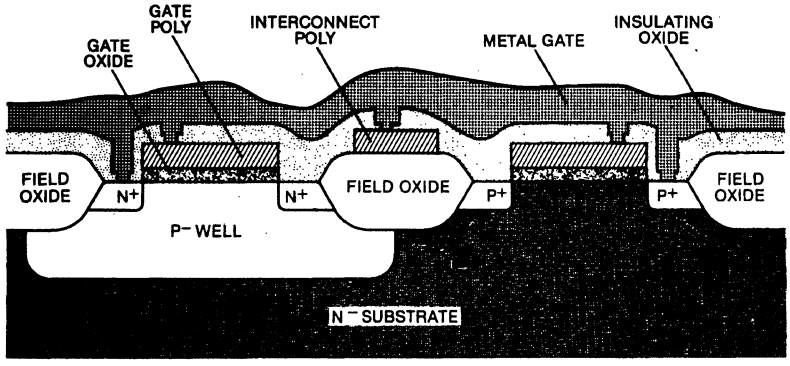
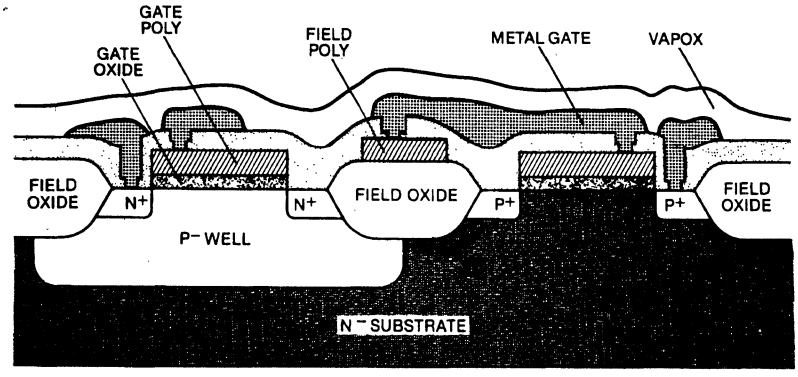


FIGURE 20. N+ and P+ Source and Drain Regions Are Ion Implanted, and the Reoxidation Is Grown Thicker to Form an Insulating Layer



TL/L/5044–10

FIGURE 21. Contact Openings Are Cut in the Insulating Oxide, and a Layer of Metalization Is Deposited Across the Entire Wafer



TL/L/5044–11

FIGURE 22. Metal Mask Is Etched to Provide Interconnect. Vapox (SiO_2) Is Deposited Over Entire Surface of Wafer

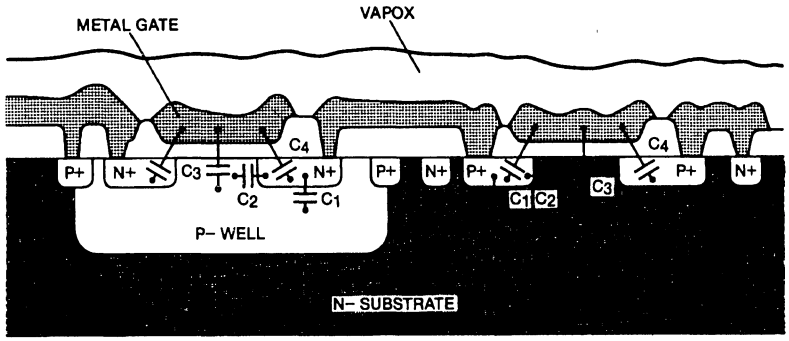
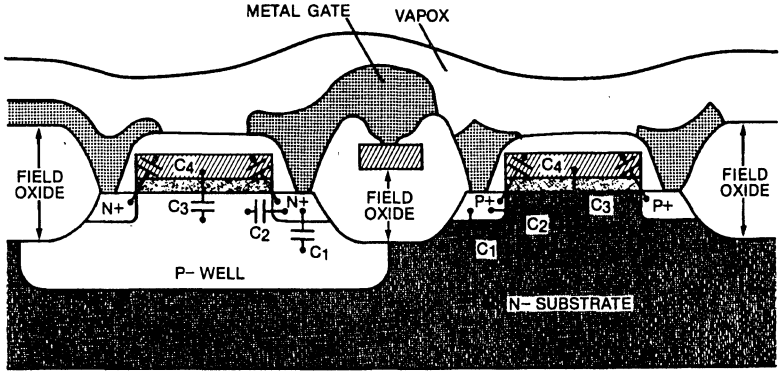
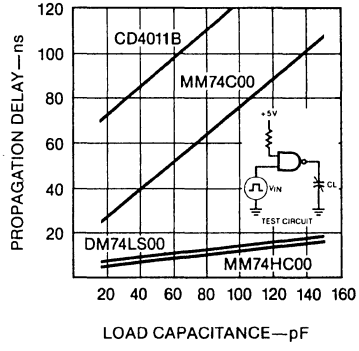


FIGURE 23. Cross Section of Metal Gate CMOS Process Showing Parasitic On-Chip Capacitances



TL/L/5044–12

FIGURE 24. Cross Section of Silicon Gate CMOS Process Showing Parasitic On-Chip Capacitances



TL/L/5044–13

FIGURE 25. Propagation Delay vs. Load Capacitance for 2-Input NAND Gate

DC Electrical Characteristics of MM54HC/MM74HC High-Speed CMOS Logic

National Semiconductor
Application Note 313
Larry Wakeman
June 1983

The input and output characteristics of the MM54HC/MM74HC high-speed CMOS logic family were conceived to meet several basic goals. These goals are to provide input current and voltage requirements, noise immunity and quiescent power dissipation similar to CD4000 and MM54C/MM74C metal-gate CMOS logic and output current drives similar to low power Schottky TTL. In addition, to enable merging of TTL and HC-CMOS designs, the MM54HCT/MM74HCT sub family differs only in their input voltage requirements, which are the same as TTL, to ease interfacing between logic families.

In order to familiarize the user with the MM54HC/MM74HC logic family, its input and output characteristics are discussed in this application note, as well as how these characteristics are affected by various parameters such as power supply voltage and temperature. Also, for those users who have been designing with metal-gate CMOS and TTL logic, notable differences and features of high-speed CMOS are compared to those logic families.

A Buffered CMOS Logic Family

The MM54HC/MM74HC is a "buffered" logic family like the CD4000B series CMOS. Buffering CMOS logic merely denotes designing the IC so that the output is taken from an inverting buffer stage. For example, the internal circuit implementation of a NAND gate would be a simple NAND followed by two inverting stages. An unbuffered gate would be implemented as a single stage. Both are shown in *Figure 1*. Most MSI logic devices are inherently buffered because they are inherently multi-stage circuits. Gates and similar small circuits yield the greatest improvement in performance by buffering.

There are several advantages to buffering this high-speed CMOS family. By using a standardized buffer, the output characteristics for all devices are more easily made identical. Multi-stage gates will have better noise immunity due to the higher gain caused by having several stages from input to output. Also, the output impedance of an unbuffered gate may change with input logic level voltage and input logic combination, whereas buffered outputs are unaffected by input conditions.

Finally, single stage gates implemented in MM54HC/MM74HC CMOS would require large transistors due to the large output drive requirements. These large devices would have a large input capacitance associated with them. This would affect the speed of circuits driving into an unbuffered gate, especially when driving large fanouts. Buffered gates have small input transistors and correspondingly small input capacitance.

One may think that a major disadvantage of buffered circuits would be speed loss. It would seem that a two or three stage gate would be two to three times slower than a buffered one. However, internal stages are much faster than the output stage and the speed lost by buffering is relatively small.

The one exception to buffering is the MM54HCU04/MM74HCU04 hex inverter which is unbuffered to enable its use in various linear and crystal oscillator applications.

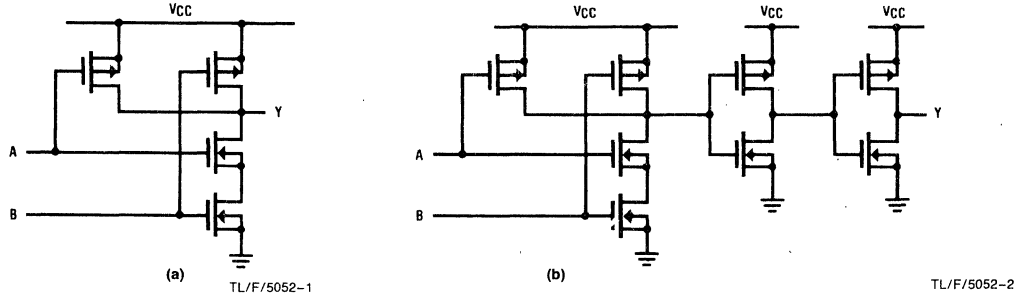


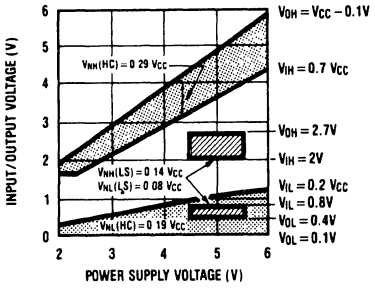
FIGURE 1. Schematic Diagrams of (a) Unbuffered and (b) Buffered NAND Gate

CMOS Input Voltage Characteristics

As mentioned before, MM54HC/MM74HC standard input levels are similar to metal-gate CMOS. This enables the high-speed logic family to enjoy the same wide noise margin of CD4000 and MM54C/MM74C logic. With $V_{CC}=5V$ these input levels are 3.5V for minimum logic "1" (V_{IH}) and 1.0V for a logic "0" (V_{IL}). The output levels when operated at $V_{CC}=5V\pm10\%$ and worst case input levels, are specified to be $V_{CC}-0.1$ or 0.1V. The output levels will actually be within a few millivolts of either V_{CC} or ground.

When operated over the entire supply voltage range, the input logic levels are: $V_{IH}=0.7V_{CC}$ and $V_{IL}=0.2V_{CC}$. *Figure 2* illustrates the input voltage levels and the noise margin of these circuits over the power supply range. The shaded area indicates the noise margin which is the difference between the input and output logic levels. The logic "1" noise margin is 29% of V_{CC} and the logic "0" noise margin is 19% of V_{CC}. Also shown for comparison are the 54LS/74LS input levels and noise margins over their supply range.

These input levels are specified on individual data sheets at $V_{CC}=2.0V$, 4.5V, 6.0V. At 2.0V the input levels are not quite $0.7(V_{CC})$ and $0.2(V_{CC})$ as at low voltages transistor turn on thresholds become significant. This is shown in *Figure 2*.



TL/F/5052-3

FIGURE 2. Worst Case Input and Output Voltages Over Operating Supply Range for "HC" and "LS" Logic

The input and output logic voltages and their behavior with temperature variation is determined by the input to output transfer function of the logic circuit. *Figure 3a* shows the transfer function of the MM54HC00/MM74HC00 NAND gate. As can be seen, the NAND gate has V_{CC} and ground output levels and a very sharp transition at about 2.25V. Thus, good noise immunity is achieved, since input noise of a volt or two will not appear on the output. The transition point is also very stable with temperature, drifting typically 50 or so millivolts over the entire temperature range. As a comparison, the transfer function for a 54LS00/74LS00 is plotted in *Figure 3b*. LSTTL output transitions at about 1.1V and the transition region varies several hundred millivolts over the temperature range. Also, since the transition region is closer to the low logic level, less ground noise can be tolerated on the input.

In typical systems, noise can be capacitively coupled to the signal lines. The amount of voltage coupled by capacitively induced currents is dependent on the impedance of the output driving the signal line. Thus, the lower the output impedance the lower the induced voltage. High-speed CMOS offers improved noise immunity over CD4000 in this respect because its output impedance is one tenth that of CD4000 and so it is about 7 times less susceptible to capacitively induced current noise.

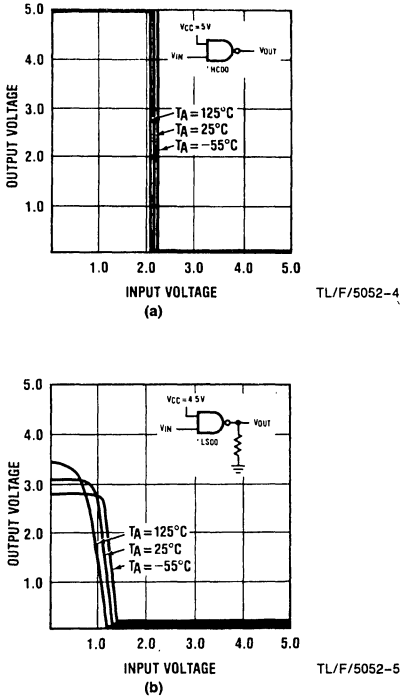


FIGURE 3. Input/Output Transfer Characteristics for (a) 'HC00 and (b) 'LS00 Nand Gate

The MM54HCT/MM74HCT sub-family of MM54HC/MM74HC logic provides TTL compatible input logic voltage levels. This will enable TTL outputs to be guaranteed to correctly drive CMOS inputs. An incompatibility results because TTL outputs are only guaranteed to pull to a 2.7V logic high level, which is not high enough to guarantee a valid CMOS logic high input. To design the entire family to be TTL compatible would compromise speed, input noise immunity and circuit size. This sub-family can be used to interface sub-systems implemented using TTL logic to CMOS sub-systems. The input level specifications of MM54HCT/MM74HCT circuits are the same as LSTTL. Minimum input high level is 2.0V and the maximum low level is 0.8V using a $5V\pm10\%$ supply.

A fairly simple alternative to interfacing from LSTTL is to tie a pull-up resistor from the TTL output to V_{CC}, usually 4–10 kΩ. This resistor will ensure that TTL will pull up to V_{CC}. (See Interfacing MM54HC/MM74HC High-Speed CMOS Logic application note.)

High-Speed CMOS Input Current and Capacitance

Both standard "HC" and TTL compatible "HCT" circuits maintain the ultra low input currents inherent in CMOS circuits when CMOS levels are applied. This current is typically less than a nanoamp and is due to reverse leakages of the input protection diodes. Input currents are so small that they can usually be neglected. Since CMOS inputs present essentially no load, their fanout is nearly infinite.

Each CMOS input has some capacitance associated with it, as do TTL inputs. This capacitance is typically 3–5 pF for MM54HC/MM74HC, and is due to package, input protection diode, and transistor gate capacitances. Capacitance information is given in the data sheets and is measured with all pins grounded except the test pin. This method is used because it yields a fairly conservative result and avoids capacitance meter and power supply ground loops and decoupling problems. *Figure 4* plots typical input capacitance versus input voltage for HC-CMOS logic with the device powered on. The small peaking at 2.2V is due to internal Miller feedback capacitance effects.

When comparing MM54HC/MM74HC input currents to TTL logic, 54LS/74LS does need significantly more input current. LSTTL requires 400 μA of current when a logic low is applied and 40 μA in the high state which is significantly more than the worst case 1 μA leakage that MM54HC/MM74HC has.

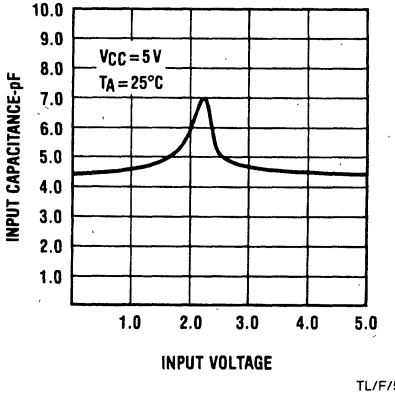


FIGURE 4. Input Capacitance vs. Input Voltage for a Typical Device

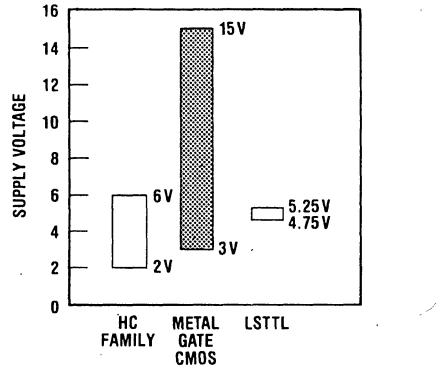


FIGURE 5. Comparison of Supply Range for "HC", "LS" and Metal-Gate

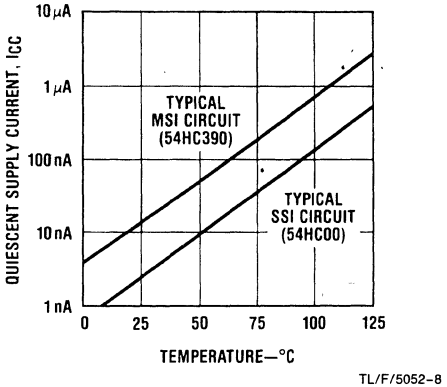


FIGURE 6. Typical Quiescent Supply Current Variation with Temperature

MM54HC/MM74HC Power Supply Voltage and Quiescent Current

Figure 5 compares the operating power supply range of high-speed CMOS to TTL and metal-gate CMOS. As can be seen, MM54HC/MM74HC can operate at power supply voltages from 2–6V. This range is narrower than the 3–15V range of CD4000 and MM54C/MM74C CMOS. The narrower range is due to the silicon-gate CMOS process employed which has been optimized to attain high operating frequencies at $V_{CC}=5V$. The 2–6V range is however much wider than the 4.5V to 5.5V range specified for TTL circuits, and guaranteeing operation down to 2V is useful when operating CMOS off batteries in portable or battery backup applications.

The quiescent power supply current of the high-speed CMOS family is very similar to CD4000 and MM54C/MM74C CMOS. When CMOS circuits are not switching there is no current path between V_{CC} and ground, except for leakage currents which are typically much less than 1 μA. These are due to diode and transistor leakages.

Figure 6 illustrates how this leakage increases with temperature by plotting typical leakage current versus temperature for an MSI and SSI device. As a result of this temperature dependence, there is a set of standardized I_{CC} specifications which specify higher current at elevated temperatures. A summary of these specifications are shown in Table I.

TABLE I. Standardized I_{CC} Specifications for MM54HC/MM74HC Logic at 25°C, 85°C and 125°C at $V_{CC}=6.0V$

Temperature	Gates	Flip-Flops	MSI
25°C	2 μA	4 μA	8 μA
85°C	20 μA	40 μA	80 μA
125°C	40 μA	80 μA	160 μA

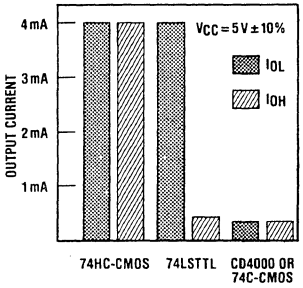
Output Characteristics

One of the prime advantages of MM54HC/MM74HC over metal-gate CMOS (besides speed) is the output drive current, which is about ten times CD4000 or MM54C/MM74C logic. The larger output current enables high-speed CMOS to directly drive large fanouts of 54LS/74LS devices, and also enables HC-CMOS to more easily drive large capacitive loads. This improvement in output drive is due to a variety of enhancements provided by the silicon-gate process used. The basic current equation for a MOSFET is:

$$I = (\text{Beta})(\text{Width}/\text{Length})((V_g - V_t)V_d - 0.5(V_d^2))$$

Where V_g is the transistor gate voltage, V_t is the transistor threshold voltage, and V_d is the transistor drain voltage which is equivalent to the circuit output voltage. This CMOS process, when compared to metal-gate CMOS, has increased transistor gains, Beta, and lower threshold voltages, V_t. Also, improved photolithography has reduced the transistor lengths, and wider transistors are also possible because of tighter geometries.

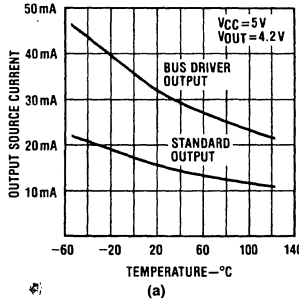
Figure 7 compares the output high and low current specifications of MM74HC, 74LS and metal-gate CMOS for standard device outputs. High-speed CMOS has worst case output low current of 4 mA which is similar to low power Schottky TTL circuits, and offers symmetrical logic high and low currents as well. In addition, CMOS circuits whose functions make them ideal for use driving large capacitive loads have a larger output current of 6 mA. For example, these bus driver outputs are used on the octal flip-flops, latches, buffers, and bidirectional circuits.



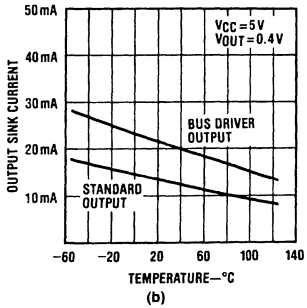
TL/F/5052–9

FIGURE 7. Comparison of 74HC, 74LS and CD4000/ 74C Output Drive Currents, I_{OH} and I_{OL}

Table II summarizes the various output current specifications for MM54HC/MM74HC CMOS along with their equivalent LSTTL fanouts. As Table II shows, the output currents of the MM54HC/MM74HC devices are derated from the MM74HC devices. The derating is caused by the decrease in current drive of the output transistors as temperature is increased. To show this, *Figure 8* plots typical output source and sink currents against temperature for both standard and bus driver circuits. This variation is similar to that found in metal-gate CMOS, and so the same −0.3% per °C derating that is used to approximate temperature derating of CD4000 and MM54C/MM74C can be applied to 54HC/74HC. As an example, the approximate worst case 25°C current drive one would expect by using the 4 mA 85°C data sheet number would be about 4 mA at $V_{OUT} = 0.26V$, and this is what is specified in the device data sheets.



TL/F/5052–10



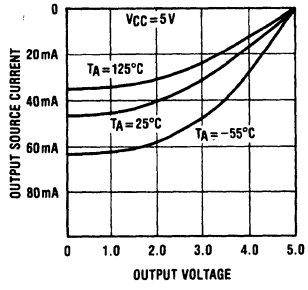
TL/F/5052–11

FIGURE 8. Typical Output (a) Source and (b) Sink Current Temperature for Standard and Bus Outputs

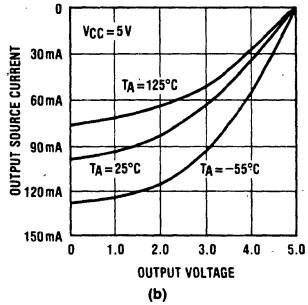
TABLE II. Data Sheet Output Current Specifications for MM54HC/MM74HC Logic

Device $V_{CC} = 4.5V$	Output High Current	Output Low Current	LSTTL Fanout
Standard 54HC	4.0 mA ($V_{OUT} = 3.7V$)	4.0 mA ($V_{OUT} = 0.4V$)	10
Bus Driver 54HC	6.0 mA ($V_{OUT} = 3.7V$)	6.0 mA ($V_{OUT} = 0.4V$)	15
Standard 74HC	4.0 mA ($V_{OUT} = 3.94$)	4.0 mA ($V_{OUT} = 0.33V$)	10
Bus 74HC	6.0 mA ($V_{OUT} = 3.94$)	6.0 mA ($V_{OUT} = 0.33V$)	15

The data sheet specifications for output current are measured at only one output voltage for either source or sink current for each of three temperature ranges, room, commercial, and military. The outputs can supply much larger currents if larger output voltages are allowed. This is shown in *Figures 9* and *10*, which plot output current versus output voltage for both N-channel sink current and P-channel source current. Both standard and bus driver outputs are shown. For example, a standard output would typically sink 20 mA with $V_{OL} = 1V$, and typically capable of a short circuit current of 50 mA.

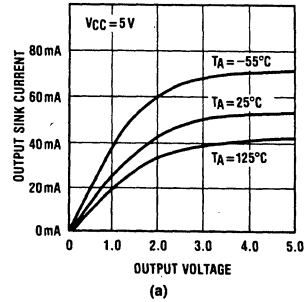


(a) TL/F/5052–12

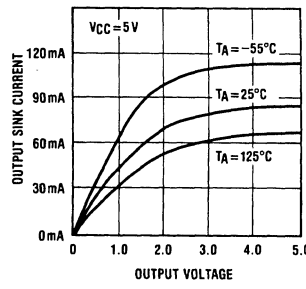


(b) TL/F/5052–13

FIGURE 9. Typical P-Channel Output Source Current vs. Output Voltage for (a) Standard and (b) Bus Outputs



(a) TL/F/5052–14



(b) TL/F/5052–15

FIGURE 10. Typical N-Channel Output Sink Current vs. Output Voltage for (a) Standard and (b) Bus Outputs

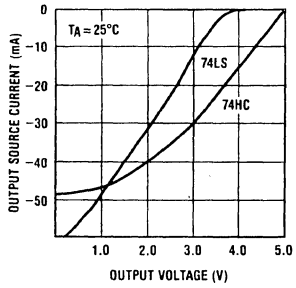
The output current and voltage characteristics of a logic circuit determine how well that circuit will switch its output when driving capacitive loads and transmission lines. The more current available, the faster the load can be switched. In order for HC-CMOS to achieve LSTTL performance, the outputs should have characteristics similar to LSTTL. This similarity is illustrated in *Figure 11* by plotted typical LSTTL and HC-CMOS output characteristics together.

As the supply voltage is decreased, the output currents will decrease. *Figure 12a* plots the output sink current versus power supply voltage with a 0.4V output voltage, and *Figure 12b* plots output source current against power supply with an output voltage of $V_{CC} - 0.8V$. It is interesting to note that MM54HC/MM74HC powered at $V_{CC} = 3V$, typically, will still drive 10 LSTTL inputs ($T = 25°C$).

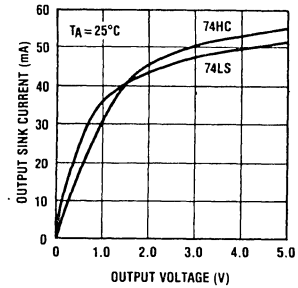
Absolute Maximum Ratings

Absolute maximum ratings are a set of guidelines that define the limits of operation for the MM54HC/MM74HC logic devices. To exceed these ratings could cause a device to malfunction and permanently damage itself. These limits are tabulated in Table III, and their reasons for existing are discussed below.

The largest power supply voltage that should be applied to a device is 7V. If larger voltages are applied, the transistors will breakdown, or "punch through". The smallest voltage that should be applied to a MM54HC/MM74HC circuit is −0.5V. If more negative voltages are applied, a substrate diode would become forward biased. In both cases large currents could flow, damaging the device.

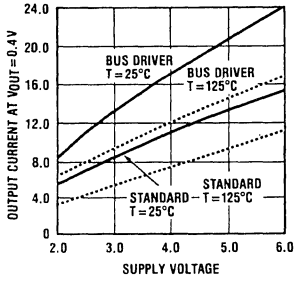


(a) TL/F/5052–16

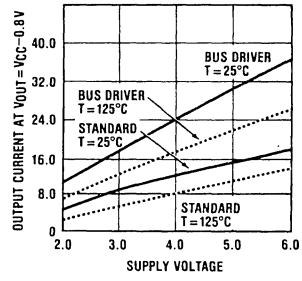


(b) TL/F/5052–17

FIGURE 11. Comparison of Standard LSTTL and HC-CMOS Output (a) Source and (b) Sink Currents



(a) TL/F/5052–18



(b) TL/F/5052–19

FIGURE 12. Output (a) Sink and (b) Source Current Variation with Power Supply

High-speed CMOS inputs should not have DC voltages applied to them that exceed V_{CC} or go below ground by more than 1.5V. To do so would forward bias input protection diodes excessive currents which may damage them. In actuality the diodes are specified to withstand 20 mA current. Thus the input voltage can exceed 1.5V if the designer limits his input current to less than 20 mA. The output voltages should be restricted to no less than −0.5V and no greater than $V_{CC}+0.5V$, or the current must be limited to 20 mA. The same limitations on the input diodes apply to the outputs as well. This includes both standard and TRI-STATE® outputs. These are DC current restrictions. In normal high speed systems, line ringing and power supply spiking unavoidably cause the inputs or outputs to glitch above these limits. This will not damage these diodes or internal circuitry. The diodes have been specifically designed to withstand momentary transient currents that would normally occur in high speed systems.

Additionally, there is a maximum rating on the DC output or supply currents as shown in Table 3. This is a restriction dictated by the current capability of the integrated circuit metal traces. Again this is a DC specification and it is expected that during switching transients the output and supply currents could exceed these specifications by several times these numbers.

For most CD4000 and MM54C/MM74C CMOS operating at $V_{CC} = 5V$, the designer does not need to worry about excessive output currents, since the output transistors usually cannot source or sink enough current to stress the metal or dissipate excessive amounts of power. The high-speed CMOS devices do have much improved output characteristics, so care should be exercised to ensure that they do not draw excessive currents for long durations, i.e., greater than 0.1 seconds. It is also important to ensure that internal dissipation of a circuit does not exceed the package power dissipation. This will usually only occur when driving large currents into small resistive loads.

TABLE III. Absolute Maximum Ratings for MM54HC/MM74HC CMOS Logic

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to 7.0	V
V_{IN}	DC Input Voltage		−1.5 to $V_{CC}+1.5$	V
V_{OUT}	DC Output Voltage		−0.5 to $V_{CC}+0.5$	V
I_{OUT}	DC Current, Per Output Pin	Standard	±25	mA
		Bus Driver	±35	mA
I_{CC}	DC V_{CC} or Ground Current	Standard	±50	mA
		Bus Driver	±70	mA
I_{IK}, I_{OK}	Input or Output Diode Current		±20	mA

MM54HC/MM74HC Input Protection

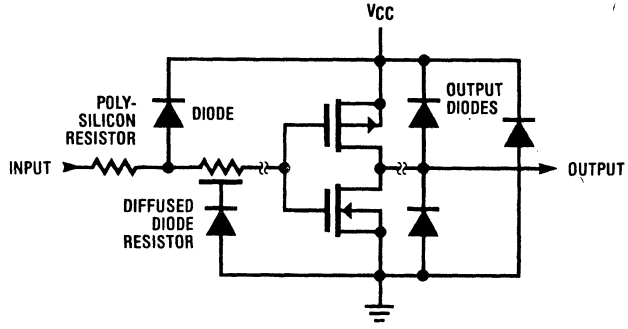
As with any circuits designed with MOS transistors "HC" logic must be protected against damage due to excessive electrostatic discharges, which can sometimes occur during handling and assembly procedures. If no protection were provided, large static voltages appearing across any two pins of a MOS IC could cause damage. However, the new input protection which takes full advantage of the "HC" silicon-gate process has been carefully designed to reduce the susceptibility of these high-speed CMOS circuits to oxide rupture due to large static voltages. In conjunction with the input protection, the output parasitic diodes also protect the circuit from large static voltages occuring between any input, output, or supply pin.

Figure 13 shows a schematic of the input protection network employed. The network consists of three elements: a poly-silicon resistor, a diode connected to V_{CC}, and a distributed diode-resistor connected to ground. This high-speed process utilizes the poly resistor to more effectively isolate the input diodes than the diode-resistor used in metal-gate CMOS. This resistor will slow down incoming transients and dissipate some of their energy. Connected to the resistor are the two diodes which clamp the input spike and prevent large voltages from appearing across the transistor. These diodes are larger than those used in metal-gate CMOS to enable greater current shunting and make them less susceptible to damage. The input network is ringed by V_{CC} and ground diffusions, which prevent substrate currents caused by these transients from affecting other circuitry.

The parasitic output diodes (*Figure 13*) that isolate the output transistor drains from the substrate are also important in preventing damage. They clamp large voltages that appear across the output pins. These diodes are also ringed by V_{CC} and ground diffusions to again shunt substrate currents, preventing damage to other parts of the circuit.

Summary

The MM54HC/MM74HC, because of many process enhancements, does provide a combination of features from 54LS/74LS and metal-gate CMOS logic families. High-speed CMOS gives the designer increased flexibility in power supply range over LSTTL, much larger output drive than CMOS has previously had, wider noise immunity than 54LS/74LS, and low CMOS power consumption.



TL/F/5052–20

FIGURE 13. Schematic Diagram of Input and Output Protection Structures

Interfacing to MM54HC/ MM74HC High-Speed CMOS Logic

National Semiconductor
Application Note 314
Larry Wakeman
June 1983

On many occasions it might be necessary to interface MM54HC/MM74HC logic to other types of logic or to some other control circuitry. HC-CMOS can easily be interfaced to any other logic family including 54LS/74LS TTL, MM54C/MM74C, CD4000 CMOS and 10,000 ECL logic. Logic interfacing can be sub-divided into two basic categories: interfacing circuitry operating at the same supply voltage and interfacing to circuitry operating on a different voltage. In the latter case, some logic level translation is usually required, but many easily available circuits simplify this task. Usually, both instances require little or no external circuitry.

Interfacing Between TTL and MM54HC/MM74HC Logic

This high-speed CMOS family can operate from 2–6V, however, in most applications which interface to TTL, both logic families will probably operate off the same 5V TTL supply. The interconnection can be broken down into two categories: TTL outputs driving CMOS inputs, and CMOS outputs driving TTL inputs. In both cases the interface is very simple.

In the first case, TTL driving HC, there are some minor differences in TTL specifications for totem-pole outputs and high-speed CMOS input specifications. The TTL output low level is completely compatible with the MM54HC/MM74HC input low, but TTL outputs are specified to have an output high level of 2.4V (2.7V for LSTTL). High-speed CMOS's logic "1" input level is 3.5V (V_{CC} = 5.0V), so TTL is not guaranteed to pull a valid CMOS logic "1" level. If the TTL circuit is only driving CMOS, its output voltage is usually about 3.5V. HC-CMOS typically recognizes levels greater than 3V as a logic high, so in most instances TTL can drive MM74HC/MM54HC.

To see why TTL does not pull up further, *Figure 1a* shows a typical standard TTL gate's output schematic. As the output pulls up, it can go no higher than two diode voltage drops below V_{CC} due to Q2 and D2. So when operating with a 5V supply, the TTL output cannot go much higher than about 3.5V. *Figure 1b* shows an LSTTL gate, which has an output structure formed by Q2 and Q4. As the LSTTL output goes high, these two transistors cannot pull higher than two base-emitter voltage drops below V_{CC}, and, as above, the output cannot go much higher than 3.5V. If the output of either the LSTTL or TTL gate is loaded or the off sink transistor has some collector leakages, the output voltage will be lower.

Many LSTTL and ALSTTL circuits take R2 of *Figure 2b* and instead of connecting it to ground, it is connected to the output. This enables the TTL output to go to 4.3V (V_{CC} = 5.0V) which is more than adequate to drive CMOS. A simple measurement of open circuit V_{OH} can verify this circuit configuration.

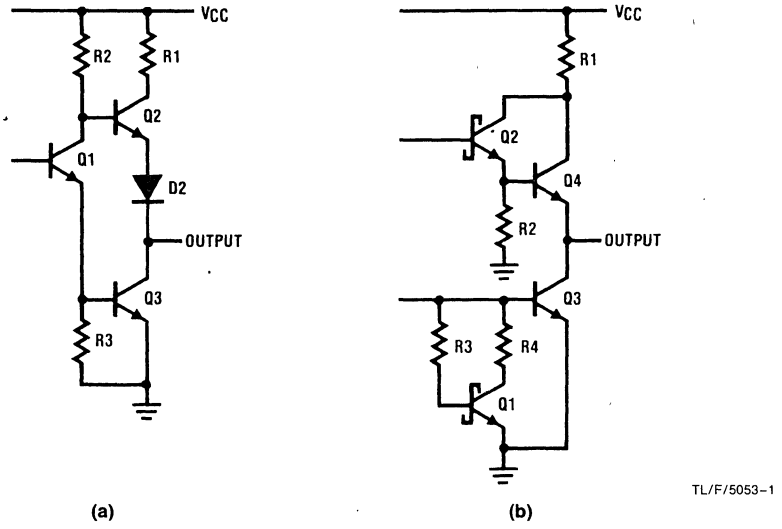
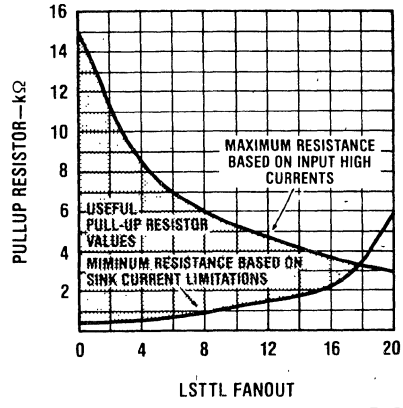


FIGURE 1. Schematic Diagrams for Typical (a) Standard and (b) Low Power Schottky TTL Outputs

Since LSTTL specifications guarantee a 2.7V output high level instead of a 3.5V output high, when designing to the worst case characteristics greater compatibility is sometimes desired. One solution to increase compatibility is to raise the output high level on the TTL output by placing a pull-up resistor from the TTL output to V_{CC}, as shown in *Figure 2*. When the output pulls up, the resistor pulls the voltage very close to V_{CC}. The value of the resistor should be chosen based on the LSTTL and CMOS fanout of the LS gate. *Figure 3* shows the range of pull-up resistors values versus LS fanout that can be used. For example, if an LSTTL device is driving only CMOS circuits, the resistor value is chosen from the left axis which corresponds to a zero LSTTL fanout.

A second solution is to use one of the many MM54HCT/MM74HCT TTL input compatible devices. These circuits have a specially designed input circuit that is compatible with TTL logic levels. Their input high level is specified at 2.0V and their input low is 0.8V with $V_{CC} = 5.0V \pm 10\%$. Thus LS can be directly connected to HC logic and the extra pull-up resistors can be eliminated. The direct interconnection of the TTL to CMOS translators is shown in *Figure 4*.

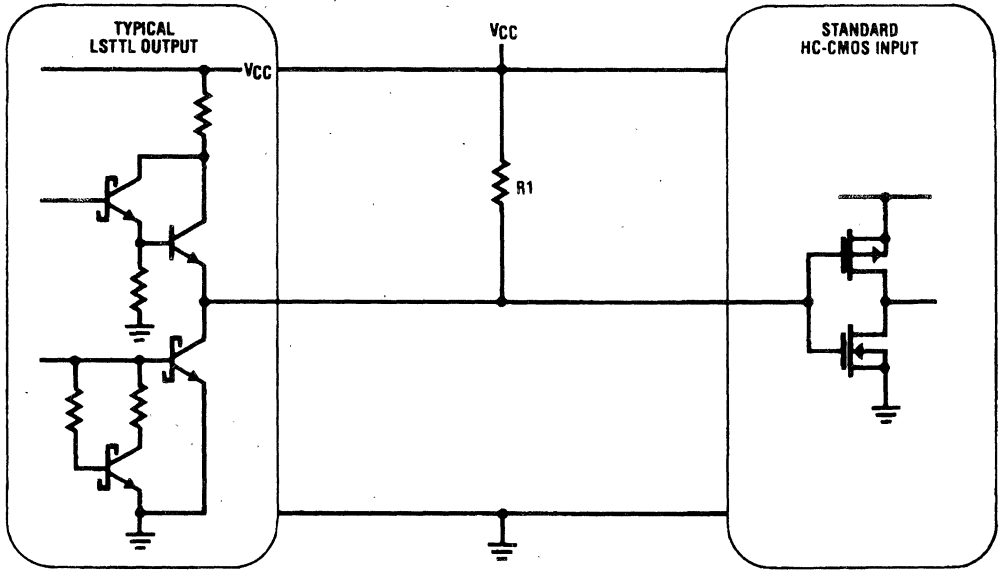
If TTL open collector outputs with a pull-up resistor are driving MM54HC/MM74HC logic, there is no interface circuitry needed as the external pull-up will pull the output to a high level very close to V_{CC}. The value of this pull-up for LS gates has the same constraints as the totem-pole outputs and its value can be chosen from *Figure 2* as well. The special TTL to CMOS buffers may also be used in this case, but they are not necessary.



TL/F/5053–2

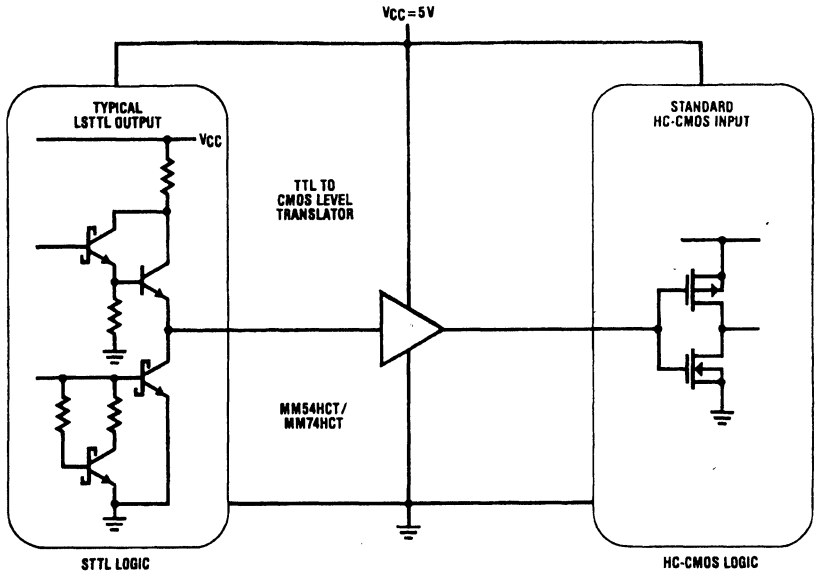
FIGURE 3. Range of Pull-Up Resistors for Low Power Schottkey TTL to CMOS Interface

When MM54HC/MM74HC outputs are driving TTL inputs, as shown in *Figure 5*, there is no incompatibility. Both the high and low output voltages are compatible with TTL. The only restriction in high-speed CMOS driving TTL is the same fanout restrictions that apply when TTL is driving TTL.



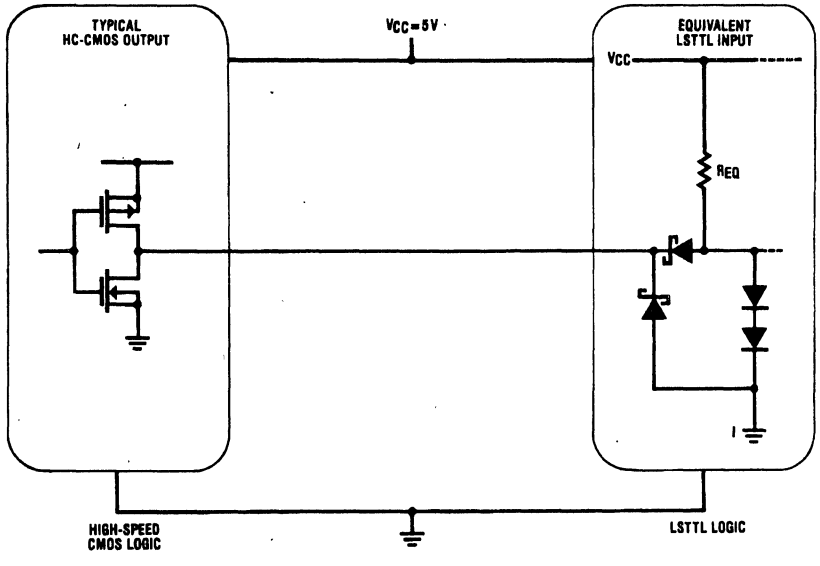
TL/F/5053–3

FIGURE 2. Interfacing LSTTL Outputs to Standard CMOS Inputs Using a Pull-Up Resistor



TL/F/5053–4

FIGURE 4. LSTTL Outputs Directly Drives MM54HCT/MM74HCT Logic Directly Which Can Interface to MM54HC/MM74HC



TL/F/5053–5

FIGURE 5. High-Speed CMOS Can Directly Connect Up to LSTTL Within its Fanout Restrictions

High-speed CMOS has much improved output drive compared to CD4000 and MM54C/MM74C metal-gate CMOS logic. *Figure 6* tabulates the fanout capabilities for this family. MM54HC/MM74HC standard outputs have a fanout capability of driving 10 LSTTL equivalent load and MM74HC bus driver outputs can drive up to 15 LSTTL inputs. It is unlikely that greater fanouts will be necessary, but several gates can be paralleled to increase output drive.

MM54HC/MM74HC and NMOS/HMOS Interconnection

With the introduction of CMOS circuits that are speed-equivalent to LSTTL, these fast CMOS devices will replace much of the bipolar support logic for many NMOS and HMOS microprocessor and LSI circuits. As a group, there is no real standard set of input and output specifications, but most NMOS circuits conform to TTL logic input and output logic level specifications.

NMOS outputs will typically pull close to V_{CC}. As with LSTTL, standard MM54HC/MM74HC CMOS inputs will typically accept NMOS outputs directly. However, to improve compatibility the MM54HCT/MM74HCT series of TTL compatible circuits may be used. These devices are particularly useful in microprocessor systems, since many of the octal devices are bus oriented and have pin-outs with inputs and outputs on opposite sides of the package. As with LSTTL, a second solution is to add a pull-up resistor between the NMOS output and V_{CC}. Both methods are shown in *Figure 7*.

MM54HC/MM74HC outputs can directly drive NMOS inputs. In fact, this situation is the same as if high-speed CMOS was driving itself. NMOS circuits have near zero input current and usually have input voltage levels that are TTL compatible. Thus MM54HC/MM74HC needs no additional circuitry to drive NMOS and there is also virtually no DC fanout restriction.

Interfacing High-Speed CMOS to MM54C/MM74C, CD4000 and CMOS-LSI

MM54HC/MM74HC CMOS and metal-gate CMOS logic interconnection is trivial. When both families are operated for the same power supply, no interface circuitry is needed. MM54HC/MM74HC, CD4000 and MM54C/MM74C logic families are completely input and output logic level compatible. Since both families have very low input currents, there is essentially no fanout limitations for either family.

The same input and output compatibility of the HC-CMOS makes it also ideal for use interfacing to CMOS-LSI circuits. For example, MM54HC/MM74HC can be directly connected to the NSC800, and 80C48 microprocessors and other microCMOS products, as well as CMOS telecommunications products.

MM54HC/MM74HC to ECL Interconnection

There may be some instances where an ECL logic system must be connected to high-speed CMOS logic. There are several possible methods to interconnect these families. *Figure 8* shows one method which uses the 10125/10525 ECL to TTL interface circuit to go from ECL to HC-CMOS logic and the 10124/10524 to connect CMOS outputs to ECL inputs. These devices allow the CMOS to operate with $V_{CC} = 5V$ while the ECL circuitry uses a $-5.2V$ supply.

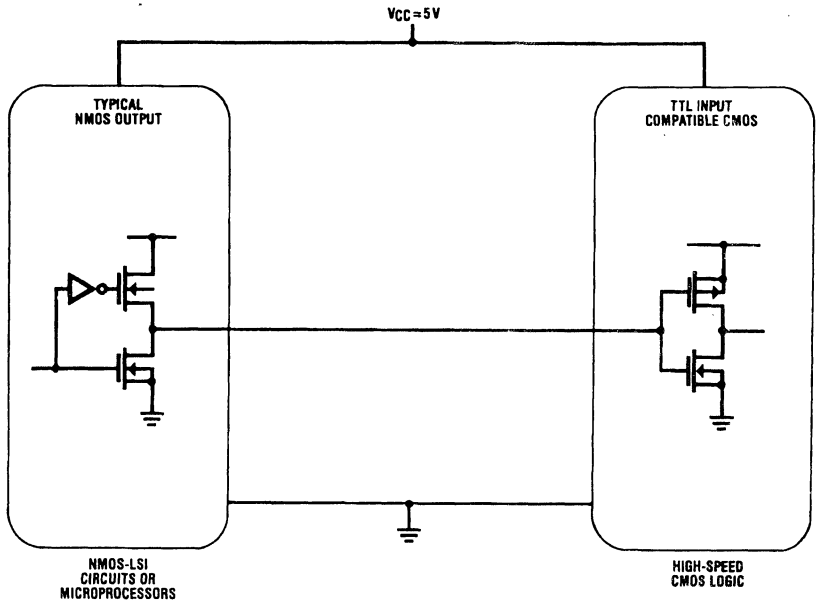
An alternate approach would be to operate the CMOS from the $-5.2V$ ECL supply as shown in *Figure 9*. Thus CMOS outputs could be directly connected to ECL inputs.

Logic Interfaces Requiring Level Translation

There are many instances when interfacing from one logic family to another that the other logic family will be operating from a different power supply voltage. If this is the case, a level translation must be accomplished. There are many different permutations of up and down level conversions that may be required. A few of the more likely ones are discussed here.

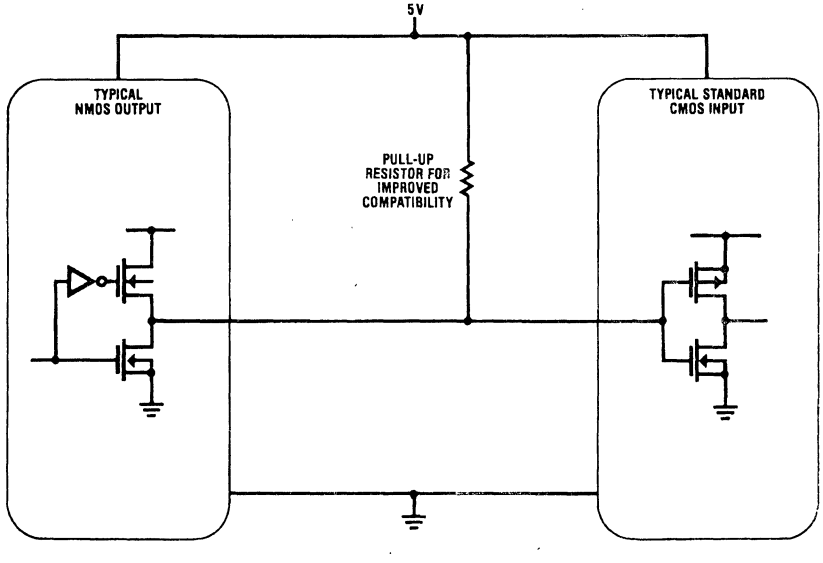
HC-CMOS Equivalent Fanouts	LSTTL		TTL		S-TTL		ALS-TTL	
	Min	Typ	Min	Typ	Min	Typ	Min	Typ
Standard Output MM54HC/MM74HC	10	20	2	4	2	4	20	40
Bus Driver Output MM54HC/MM74HC	15	30	4	8	3	6	30	60

FIGURE 6. Equivalent Fanout Capabilities of High-Speed CMOS Logic



TL/F/5053-6

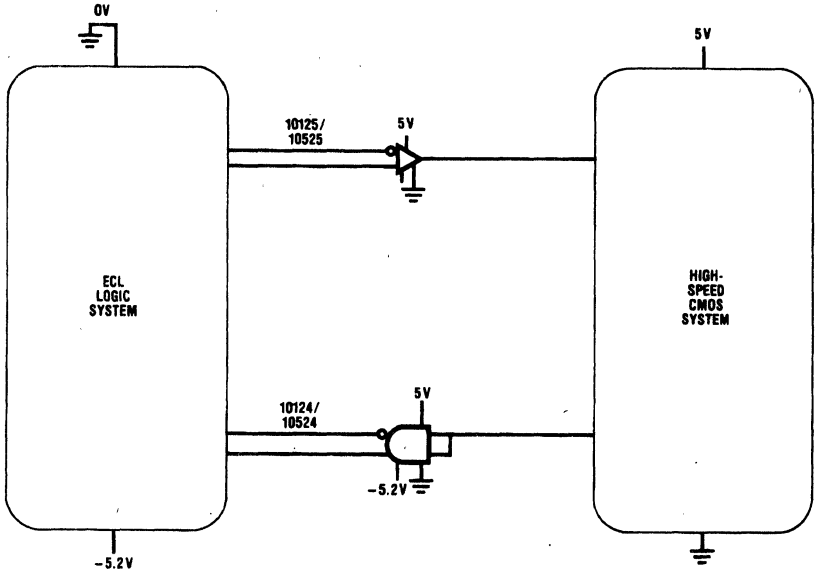
(a)



TL/F/5053-7

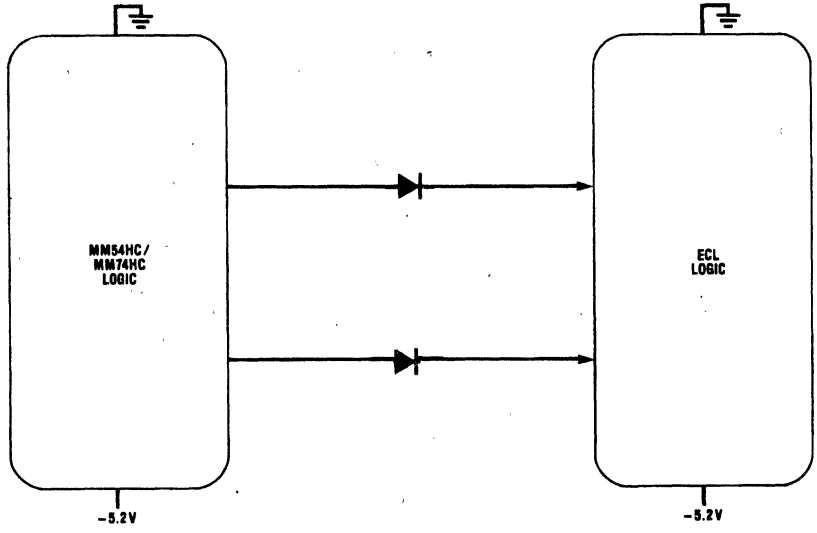
(b)

FIGURE 7. Improved Compatibility NMOS to CMOS Connection Using (a) TTL Input Compatible Devices or (b) External Pull-Up Resistors



TL/F/5053–8

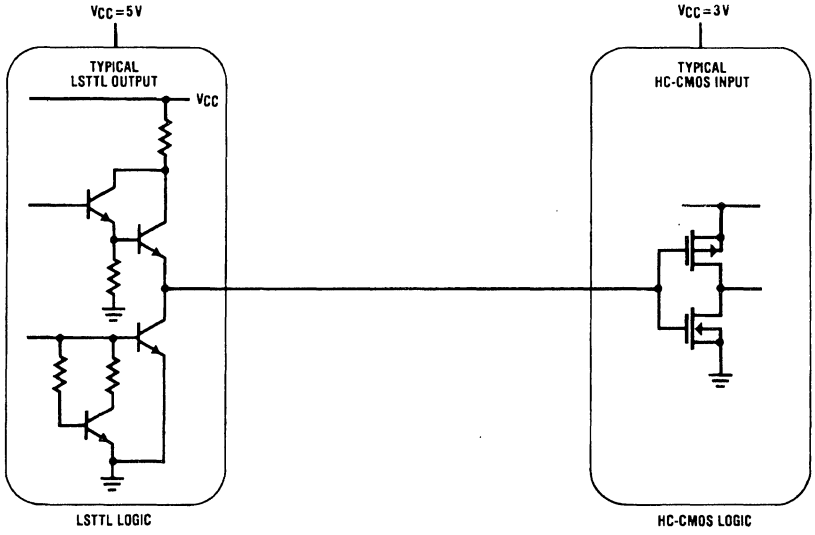
FIGURE 8. MM54HC/MM74HC to ECL and ECL to HC-CMOS Interface



TL/F/5053–9

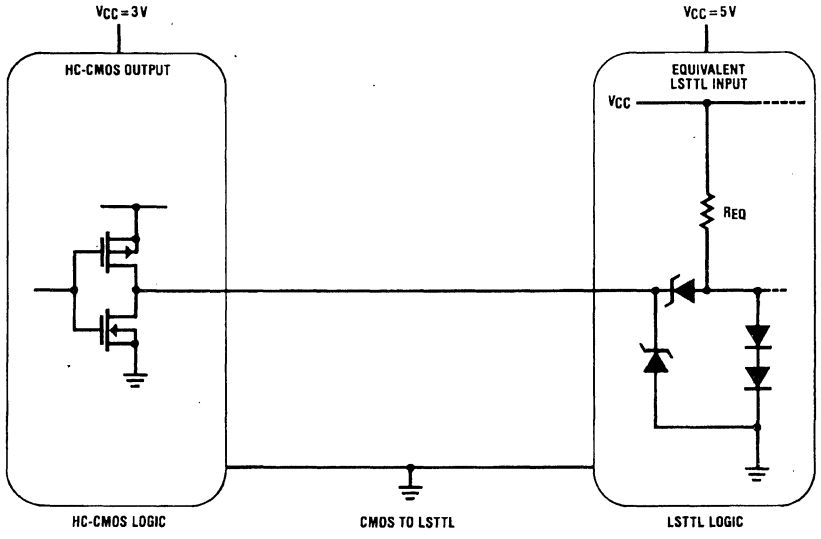
FIGURE 9. HC-CMOS Driving ECL Logic from Same Power Supply

If MM54HC/MM74HC is operated in a battery back up application for a TTL system, high-speed CMOS may be operated at $V_{CC} = 2-3V$ and can be connected to 5V TTL. CMOS operating at 3V can be directly connected to TTL since its input and output levels are compatible with TTL, and the TTL output levels are compatible with CMOS inputs, as shown in *Figure 10*. When high-speed CMOS is operated at 2V, the TTL outputs will exceed the CMOS power supply and the CMOS outputs will just barely pull high enough to drive TTL, so some level translation will be necessary.



TL/F/5053–10

(a)

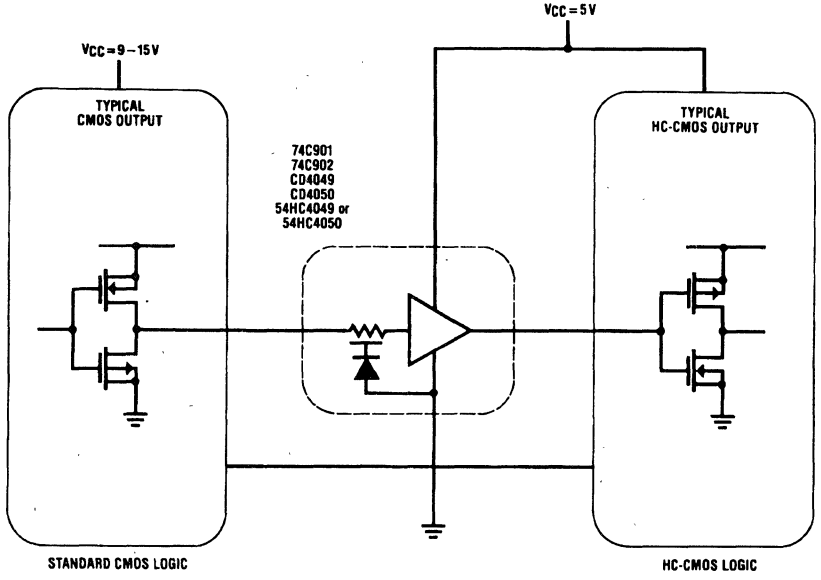


TL/F/5053–11

(b)

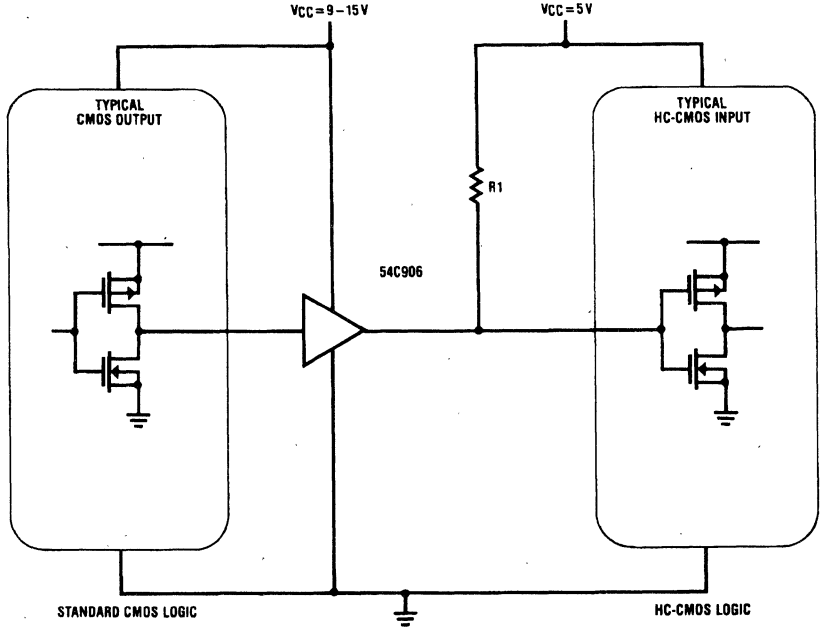
FIGURE 10. When HC-CMOS Is Operating At $V_{CC} = 3V$ No Logic Level Conversion Circuitry Is Needed

CD4000 and MM54C/MM74C metal-gate CMOS logic can be operated over a wider supply range that MM54HC/MM74HC, and because of this there will be instances when metal-gate CMOS and HC-CMOS will be operated off different supply voltages. Usually 9V to 15V CD4000 logic levels will have to be down converted to 5V high-speed CMOS levels. *Figure 11* shows several possible down conversion techniques using either a CD4049, CD4050, MM54HC4049, MM54HC4050, or MM54C906.



TL/F/5053–12

(a)



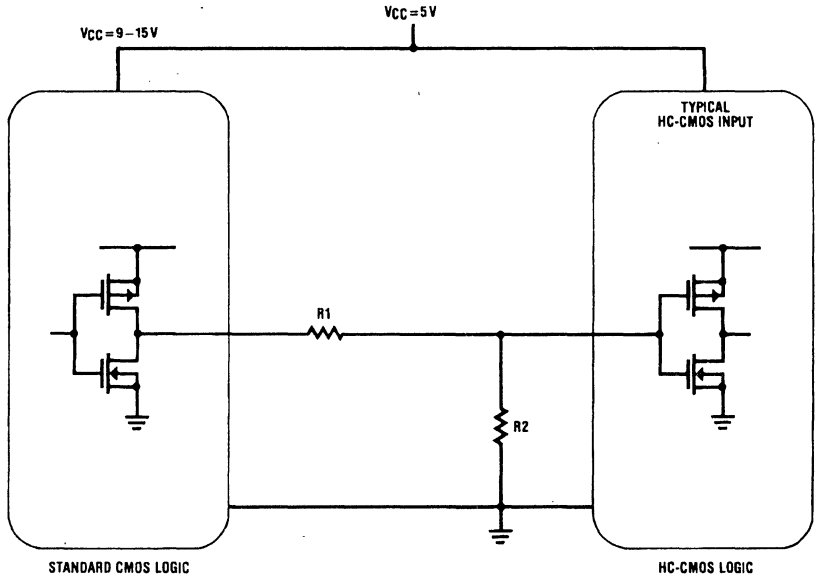
TL/F/5053–13

(b)

FIGURE 11. CD4000 or 74C Series CMOS to HC-CMOS Connection with Logic Level Conversion Using (a) Special Down Converters or (b) Open Drain CMOS

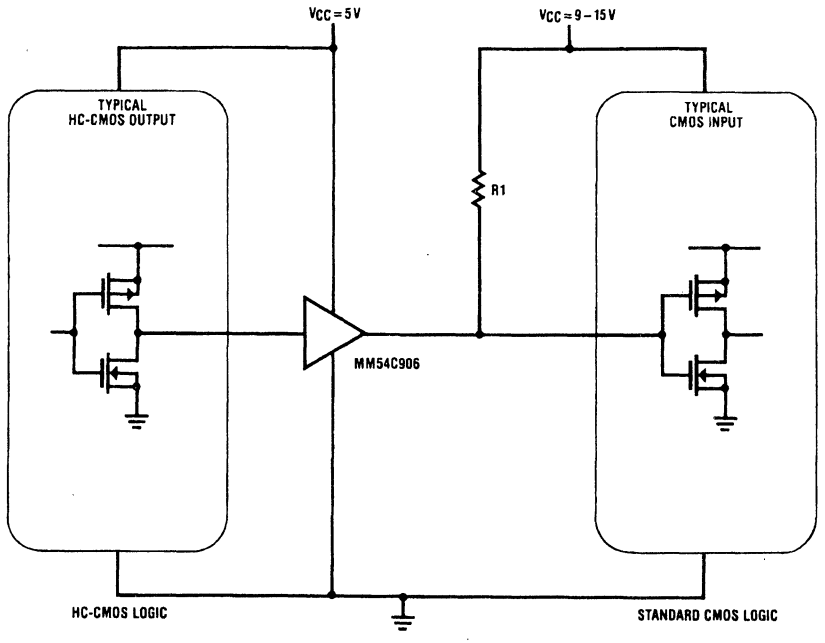
Since CMOS has a high input impedance, another possibility is to use a resistor voltage divider for down level conversion as shown in *Figure 12*. Voltage dividers will, however, dissipate some power.

Up conversion from MM54HC/MM74HC to metal-gate CMOS can be accomplished as shown in *Figure 13*. Here an MM54C906 open drain buffer with a pull-up resistor tied to the larger power supply is used.



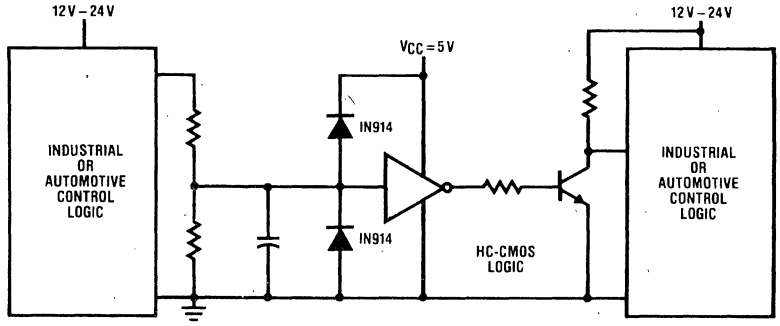
TL/F/5053–14

FIGURE 12. CMOS to "HC" CMOS Logic Level Translation Using Resistor Divider



TL/F/5053–15

FIGURE 13. HC-CMOS to CD4000 or 74C Series CMOS Connection with Logic Level Conversion Using an Open Drain CMOS Circuit



TL/F/5053–16

FIGURE 14. Interfacing Between HC-CMOS and High Voltage Control Logic

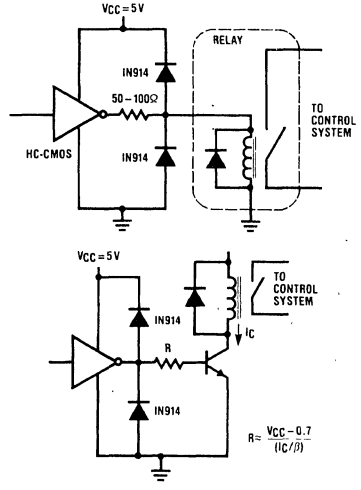
High Voltage and Industrial Control Interfaces

On occasion, interfacing to industrial and automotive control systems may be necessary. If these systems operate within the metal-gate CMOS supply range, interfacing MM54HC/MM74HC to them is similar to interfacing to CD4000 operating at a higher supply. In rugged industrial environments, care may be required to ensure that large transients do not harm the CMOS logic. *Figure 14* shows a typical connection to a high voltage system using diode clamps for input and output protection.

The higher drive of HC-CMOS can enable direct connection to relay circuits, but additional isolation is recommended. Clamp diodes should again be used to prevent spikes generated by the relay from harming the CMOS device. For higher current drive an external transistor may be used to interface to high-speed CMOS. Both of these are shown in *Figure 15*. Also, the higher drive enables easy connection to SCR's and other power control semiconductors as shown in *Figure 16*.

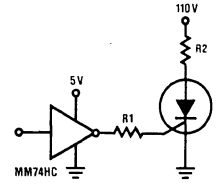
Conclusion

Interfacing between different logic families is not at all difficult. In most instances, when no logic level translation between is done, no external circuitry is needed to interconnect logic families. Even though the wide supply range of MM54C/MM74C and CD4000 creates many possible logic level conversion interface situations, most are easily handled by employing a minimum of extra circuitry. Additionally, several special interface devices also simplify logic level conversion.



TL/F/5053–17

FIGURE 15. Interfacing MM54HC/MM74HC to Relays



TL/F/5053–18

FIGURE 16. MM54HC/MM74HC Driving an SCR

AC Characteristics of MM54HC/MM74HC High-Speed CMOS

National Semiconductor
Application Note 317
Larry Wakeman
June 1983

When deciding what circuits to use for a design, speed is most often a very important criteria. MM54HC/MM74HC is intended to offer the same basic speed performance as low power Schottky TTL while giving the designer the low power and high noise immunity characteristics of CMOS. In other words, HC-CMOS is about ten times faster than CD4000 and MM54C/MM74C metal-gate CMOS logic. Even though HC-CMOS logic does have speeds similar to LSTTL, there are some differences in how this family's speeds are specified, and how various parameters affect circuit performance.

To give the designer an idea of the expected performance, this discussion will include how the AC characteristics of high-speed CMOS are specified. This logic family has been specified so that in the majority of applications, the specifications can be directly applied to the design. Since it is impossible to specify a device under all possible situations, performance variations with power supply, loading and temperature are discussed, and several easy methods for determining propagation delays in nearly any situation are also described. Finally, it is useful to compare the performance of HC-CMOS to 54LS/74LS and to CD4000.

Data Sheet Specifications

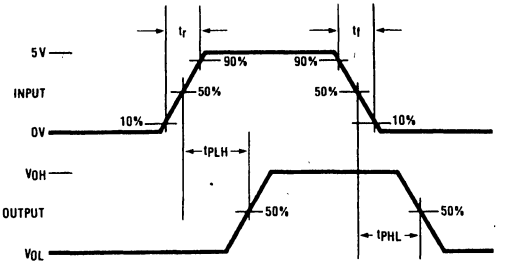
Even though the speeds achieved by this high-speed CMOS family are similar to LSTTL, the input, output and power supply characteristics are very similar to metal-gate CMOS. Because of this, the actual measurements for various timing parameters are not done the same way as TTL. The MM54HCT/MM74HCT TTL input compatible circuits are an exception.

Standard HC-CMOS AC specifications are measured at V_{CC} = 2.0V, 4.5V, 6.0V for room, military and commercial temperature ranges. Also HC is specified with LS equivalent supply (5.0V) and load conditions to enable proper comparison to low power Schottkey TTL. Input signal levels are ground to V_{CC} with rise and fall times of 6 ns (10% to 90%). Since standard CMOS logic has a logic trip point at about mid-supply, and the outputs will transition from ground to V_{CC}, timing measurements are made from the 50% points on input and output waveforms. This is shown in *Figure 1*. Using the mid-supply point gives a more accurate representation of how high-speed CMOS will perform in a CMOS system. This is different from the 1.3V measurement point and ground to 3V input waveforms that are used to measure TTL timing.

This output loading used for data sheet specifications fall into two categories, depending on the output drive capability of the specific device. The output drive categories are standard outputs (I_{OL} = 4 mA) and bus driver outputs (I_{OL} = 6 mA). Timing measurements for standard outputs are made using a 50 pF load. Bus driver circuits are measured using both a 50 pF and 150 pF load. In all AC tests, the test load capacitance includes all stray and test jig capacitances.

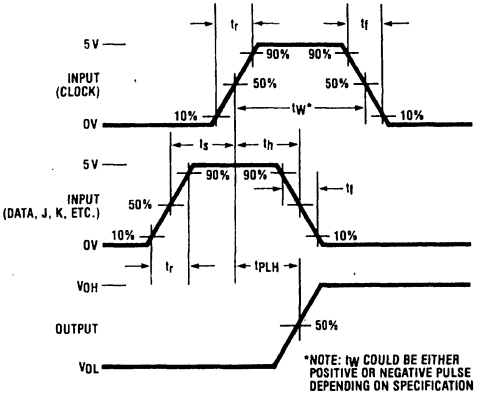
TRI-STATE® measurements where the outputs go from an active output level to a high impedance state, are made using the same input waveforms described above, but the timing is measured to the 10% or 90% points on the output waveforms. The test circuit load is composed of a 50 pF capacitor and a 1 kΩ resistor. To test t_{PHZ}, the resistor is swiched to ground, and for t_{PLZ} it is switched to V_{CC}. The TRI-STATE test circuit and typical timing waveforms are shown in *Figure 2*.

Measurements, where the output goes from the high impedance state to active output, are the same except that measurements are made to the 50% points and for bus driver devices both 50 pF and 150 pF capacitors are used.



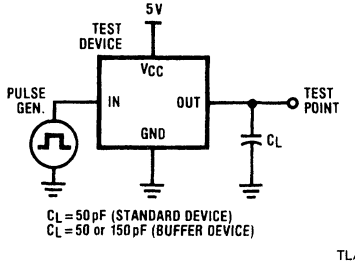
TL/F/5067–1

(a)



TL/F/5067–2

(b)



TL/F/5067–3

(c)

FIGURE 1. Typical Timing Waveform for (a) Propagation Delays, and (b) Clocked Delays. Also Test Circuit (c) for These Waveforms ($t_r = t_f$ = 6 ns)

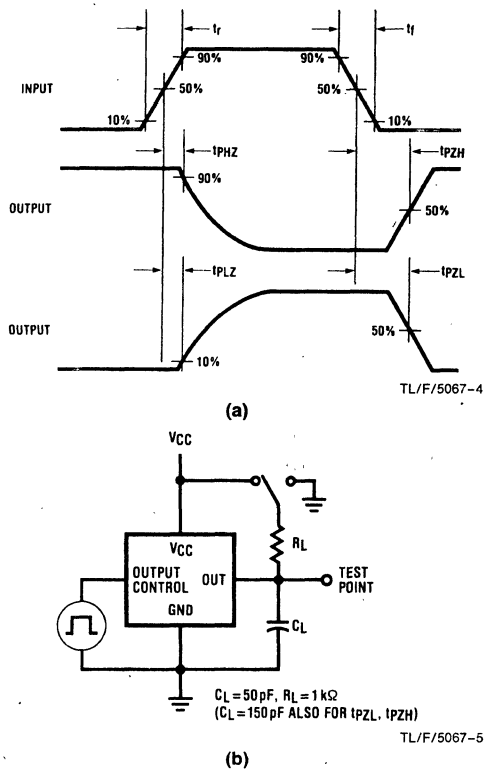


FIGURE 2. Typical TRI-STATE (a) Timing Waveforms and (b) Test Circuit

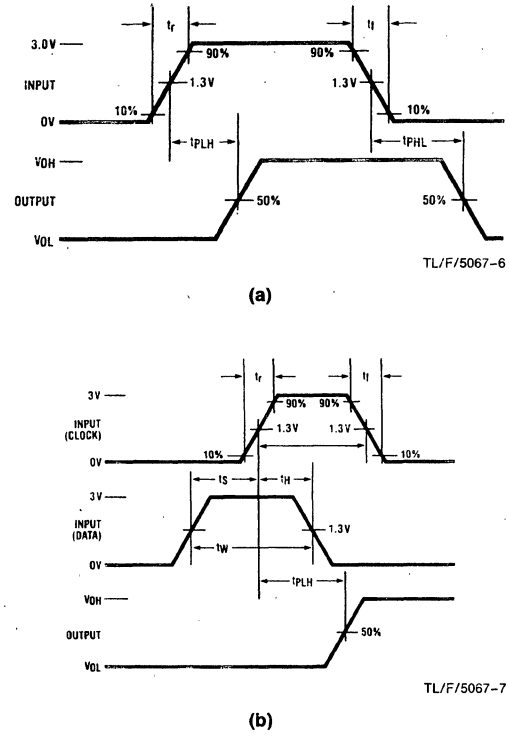


FIGURE 3. Typical Timing Waveforms for (a) Propagation Delays, and (b) Clocked Delays for 54HCT/74HCT Devices ($t_r = t_f = 6$ ns)

Note: Some early data sheets used a different test circuit. This has been changed or will be changed.

The MM54HCT/MM74HCT TTL input compatible devices are intended to operate with TTL devices, and so it makes sense to specify them the same way as TTL. Thus, as shown in *Figure 3*, typical timing input waveforms use 0–3V levels and timing measurements are made from the 1.3V levels on these signals. The test circuits used are the same as standard HC input circuits. This is shown in *Figure 3*. These measurements are compatible with TTL type specified devices.

Specifying standard MM54HC/MM74HC speeds using 2.5V input measurement levels does represent a specification incompatibility between TTL and most RAM/ROM and microprocessor speed specifications. It should not, however, present a design problem. The timing difference that results from using different measurement points is the time it takes for an output to make the extra excursion from 1.3V to 2.5V. Thus, for a standard high-speed CMOS output, the extra transition time should result, worst case, in less than a 2 ns increase in the circuit delay measurement for a 50 pF load. Thus in speed critical designs adding 1–2 ns safely enables proper design of HC into the TTL level systems.

Power Supply Affect on AC Performance

The overall power supply range of MM54HC/MM74HC logic is not as wide as CD4000 series CMOS due to performance optimization for 5V operation; however, this family can operate over a 2–6V range which does enable some versatility, especially when battery operated. Like metal-gate CMOS, lowering the power supply voltage will result in increased circuit delays. Some typical delays are shown in *Figure 4*. As the supply voltage is decreased from 5V to 2V, propagation delays increase by about two to three times, and when the voltage is increased to 6V, the delays decrease by 10–15%.

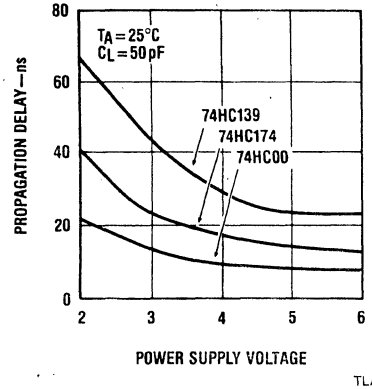


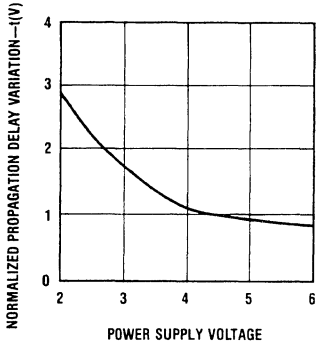
FIGURE 4. Typical Propagation Delay Variations of 74HC00, 74HC139, 74HC174 with Power Supply

In some designs it may be important to calculate the expected propagation delays for a specific situation not covered in the data sheet. This can easily be accomplished by using the normalized curve of *Figure 5* which plots propagation delay variation constant, t(V), versus power supply voltage normalized to 4.5V and 5V operation. This constant, when used with the following equation and the data sheet 5.0V specifications, yields the required delay at any power supply.

$$t_{PD}(V) = [t(V)]\,[t_{PD}(5V)] \qquad 1.0$$

Where $t_{PD}(5V)$ is the data sheet delay and $t_{PD}(V)$ is the resultant delay at the desired supply voltage. This curve can also be used for the $V_{CC} = 4.5V$ specifications.

For example, to calculate the typical delay of the 74HC00 at $V_{CC} = 6V$, the data sheet typical of 9 ns (15 pF load) is used. From *Figure 5* t(V) is 0.9, so the 6V delay would be 8 ns.



TL/F/5067–9

FIGURE 5. MM54HCMM74HC Propagation Delay Variation Vs. Power Supply Normalized to $V_{CC} = 4.5V$, and $V_{CC} = 5.0V$

Speed Variation with Capacitive Loading

When high-speed CMOS is designed into a CMOS system, the load on a given output is essentially capacitive, and is the sum of the individual input capacitances, TRI-STATE output capacitances, and parasitic wiring capacitances. As the load is increased, the propagation delay increases. The rate of increase in delay for a particular device is due to the increased charge/discharge time of the output and the load. The rate at which the delay changes is dependent on the output impedance of the MM54HC/MM74HC circuit. As mentioned, for high-speed CMOS, there are two output structures: bus driver and standard.

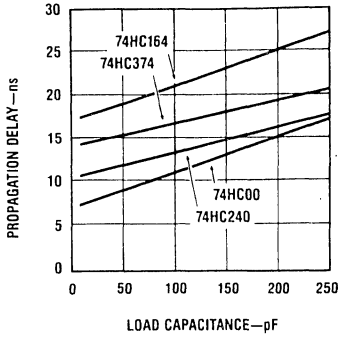
Figure 6 plots some typical propagation delay variations against load capacitance. To calculate under a particular load condition what the propagation delay of a circuit is, one need only know what the rate of change of the propagation delay with the load capacitance and use this number to extrapolate the delay from the data sheet vaue to the desired value. *Figure 7* plots this constant, t(C), against power supply voltage variation. Thus, by expanding on equation 1.0, the propagation delay at any load and power supply can be calculated using:

$$t_{PD}(C,V) = [t(C)\,(C_L - 15\text{ pF})] + [t_{PD}(5V)\,t(V)] \qquad 1.1$$

Where t(V) is the propagation delay variation with power supply constant, $t_{PD}(5V)$ is the data sheet 4.5V (use ($C_L - = 50$ pF) in equation) or 5V delay, C_L is the load capacitance and $t_{PD}(C,V)$ is the resultant propagation delay at the desired load and supply. This equation's first term is the difference in propagation delay from the desired load and the data sheet specification load. The second term is essentially equation 1.0. If the delay is to be calculated at $V_{CC} = 5V$, then $t(V) = 1$ and $t(C) = 0.042$ ns/pF (standard output), 0.028 ns/pF (bus output).

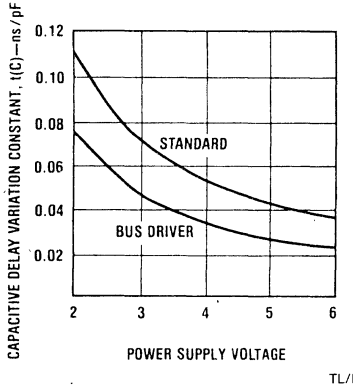
Using the previous 74HC00 example, the delay at $V_{CC} = 6V$ and a 100 pF load is:

$$t_{PD}(100\text{ pF},6V) = (0.042)(100-15) + (0.9 \times 9) = 11\text{ ns}$$



TL/F/5067–10

FIGURE 6. Typical Propagation Delay Variation With Load Capacitance for 74HC04, 74HC164, 74HC240, 74HC374



TL/F/5067–11

FIGURE 7. Propagation Delay Capacitance Variation Constant Vs. Power Supply

Speed Variations with Change in Temperature

Changes in temperature will cause some change in speed. As with CD4000 and other metal-gate CMOS logic parts, MM54HC/MM74HC operates slightly slower at elevated temperatures, and somewhat faster at lower temperatures. The mechanism which causes this variation is the same as that which causes variations in metal-gate CMOS. This

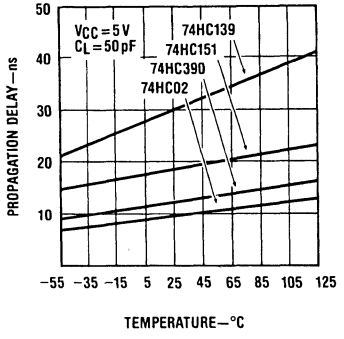
factor is carrier mobility, which decreases with increase in temperature, and this causes a decrease in overall transistor gain which has a corresponding affect on speed.

Figure 8 shows some typical temperature-delay variations for some high-speed CMOS circuits. As can be seen, speeds derate fairly linearly from 25°C at about −0.3%/C. Thus, 125°C propagation delays will be increased about 30% from 25°C. 54HC/74HC speeds are specified at room temperature, −40 to 85°C (commercial temperature range), and −55 to 125°C (military range). In virtually all cases the numbers given are for the highest temperature.

To calculate the expected device speeds at any temperature, not specified in the device data sheet, the following equation can be used:

$$t_{PD}(T) = [1 + ((T-25)(0.003))][t_{PD}(25)] \quad 1.2$$

Where $t_{PD}(T)$ is the delay at the desired temperature, and $t_{PD}(25)$ is the room temperature delay. Using the 74HC00 example from the previous section, the expected increase in propagation delay when operated at $V_{CC} = 5V$ and 85°C is $[1 + (85-25)(0.003)](10\ ns) = 12$ ns. The expected delay at some other supply can also be calculated by calculating the room temperature delay then calculating the delay at the desired temperature.



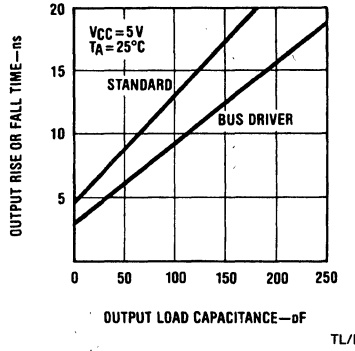
TL/F/5067–12

FIGURE 8. Typical Propagation Delay Variation With Temperature for 54HC02, 54HC390, 54HC139, 54HC151

Output Rise and Fall, Setup and Hold Times and Pulse Width Performance Variations

So far, the previous discussion has been restricted to propagation delay variations, and in most instances, this is the most important parameter to know. Output rise and fall times may also be important. Unlike TTL type logic families HC specifies these in the data sheet. High-speed CMOS outputs were designed to have typically symmetrical rise and fall times. Output rise and fall time variations track very closely the propagation delay variations over temperature and supply. *Figure 9* plots rise and fall time against output load at $V_{CC} = 5V$ and at room temperature. Load variation of the transition time is twice the delay variation because delays are measured at halfway points on the waveform transition.

Setup times and pulse width performance under different conditions may be necessary when using clocked logic circuits. These parameters are indirect measurements of internal propagation delays. Thus they exhibit the similar temperature and supply dependence as propagation delays. They are, however, independent of output load conditions.



TL/F/5067–13

FIGURE 9. Typical Output Rise or Fall Time Vs. Load For Standard and Bus Driver Outputs

Input Rise and Fall Times

Another speed consideration, though not directly related to propagation delays, is input rise and fall time. As with other high-speed logic families and also CD4000B and 54C/74C CMOS, slow input rise and fall times on input signals can cause logic problems.

Typically, small signal gains for a MM54HC/MM74HC gate is greater than 1000 and, if input signals spend appreciable time between logic states, noise on the input or power supply will cause the output to oscillate during this transition. This oscillation could cause logic errors in the user's circuit as well as dissipate extra power unnecessarily. For this reason MM54HC/MM74HC data sheets recommend that input rise and fall times be shorter than 500 ns at $V_{CC} = 4.5V$.

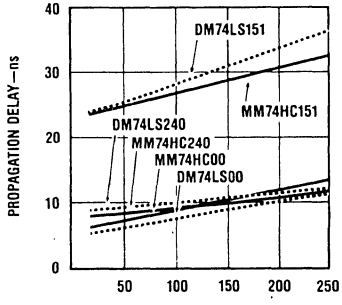
Flip-flops and other clocked circuits also should have their input rise and fall times faster than 500 ns at $V_{CC} = 4.5V$. If clock input rise and fall times become too long, system noise can generate internal oscillations, causing the internal flip-flops to toggle on the wrong external clock edge. Even if no noise were present, internal clock skew caused by slow rise times could cause the logic to malfunction.

If long rise and fall times are unavoidable, Schmitt triggers ('HC14/'HC132) or other special devices that employ Schmitt trigger circuits should be used to speed up these input signals.

Logic Family Performance Comparison

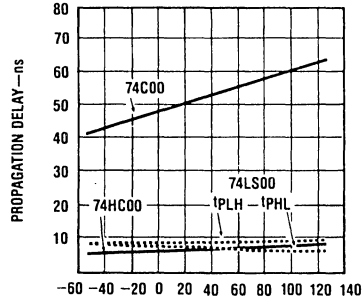
To obtain a better feeling of how high-speed CMOS compares to bipolar and other CMOS logic families, *Figure 10* plots MM54HC/MM74HC, 54LS/74LS and CD4000B logic device speeds versus output loading. HC-CMOS propagation delay and delay variation with load is nearly the same as LSTTL and about ten times faster than metal-gate CMOS. Utilizing a silicon-gate process enables achievement of LSTTL speeds, and the large output drive of this family enables the variation with loading to be nearly the same as LSTTL as well.

When comparing to CD4000 operating at 5V, HC-CMOS is typically ten times faster, and about three times faster than CD4000 logic operating at 15V. This is shown in *Figure 11*.



TL/F/5067–14

FIGURE 10. Comparison of LSTTL and High-Speed CMOS Delays



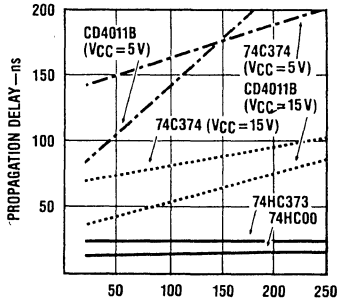
TL/F/5067–16

FIGURE 12. Comparison of HC-CMOS, Metal-Gate CMOS, and LSTTL Propagation Delay Vs. Temperature

At 5V CD4000 has about a tenth the output drive of MM54HC/MM74HC and as seen in *Figure 10*, the capacitive delay variation is much larger.

As shown in *Figure 12*, the temperature variation of HC-CMOS is similar to CD4000. This is due to the same physical phenomenon in both families. The 54LS/74LS logic family has a very different temperature variation, which is due to different circuit parameter variations. One advantage to CMOS is that its temperature variation is predictable, but with LSTTL, sometimes the speed increases and other times speed decreases with temperature.

The inherent symmetry of MM54HC/MM74HC's logic levels and rise and fall times tends to make high to low and low to high propagation delay very similar, thus making these parts easy to use.



TL/F/5067–15

FIGURE 11. Comparison of Metal-Gate CMOS and High-Speed CMOS Delays

Conclusion

High-speed CMOS circuits are speed compatible with 54LS/74LS circuits, not only on the data sheets, but even driving different loads. In general, HC-CMOS provides a large improvement in performance over older metal-gate CMOS.

By using some of the equations and curves detailed here, along with data sheet specifications, the designer can very closely estimate the performance of any MM54HC/MM74HC device. Even though the above examples illustrate typical performance calculations, a more conservative design can be implemented by more conservatively estimating various constants and using worst case data sheet limits. It is also possible to estimate the fastest propagation delays by using speeds about 0.4–0.7 times the data sheet typicals and aggressively estimating the various constants.

Comparison of MM54HC/MM74HC to 54LS/74LS, 54S/74S and 54ALS/74ALS Logic

National Semiconductor
Application Note 319
Larry Wakeman
June 1983

The MM54HC/MM74HC family of high speed logic components provides a combination of speed and power characteristics that is not duplicated by bipolar logic families or any other CMOS family. This CMOS family has operating speeds similar to low power Schottky (54LS/74LS) technology. MM54HC/MM74HC is approximately half as fast (delays are twice as long) as the 54ALS/74ALS and 54S/74S logic. Compared to CD4000 and 54C/74C, this is an order of magnitude improvement in speed, which is achieved by utilizing an advanced 3.5 micron silicon gate-recessed oxide CMOS process. The MM54HC/MM74HC components are designed to retain all the advantages of older metal gate CMOS, plus provide the speeds required by today's high speed systems.

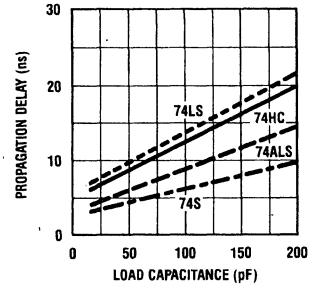
Another key advantage of the MM54HC/MM74HC family is that it provides the functions and pin outs of the popular 54LS/74LS series logic components. Many functions which are unique to the CD4000 metal gate CMOS family have also been implemented in this high speed technology. In addition, the MM54HC/MM74HC family contains several special functions not previously implemented in CD4000 or 54LS/74LS.

Although the functions and the speeds are the same as 54LS/74LS, some of the electrical characteristics are different from either LS-TTL, S-TTL or ALS-TTL. The following discusses these differences and highlights the advantages and disadvantages of high speed CMOS.

AC PERFORMANCE

As mentioned previously, the MM54HC/MM74HC logic family has been designed to have speeds equivalent to LS-TTL, and to be 8–10 times faster than CD4000B and MM54C/MM74C logic. Table I compares high speed CMOS to the bipolar logic families. HC-CMOS gate delays are typically the same as LS-TTL, and ALS-TTL is two to three times faster. S-TTL is also about twice as fast as HC-CMOS. Flip-flop and counter speeds also follow the same pattern.

Also, HC logic's propagation delay variation due to changes in capacitive loading is very similar to LS-TTL. *Figure 1* illustrates this by plotting delay versus loading for the various bipolar logic families and MM54HC/MM74HC. HC-CMOS has virtually the same speed and load-delay variation as



TL/F/5101–1

FIGURE 1. HC, LS, ALS, S Comparison of Propagation Delay vs Load for a NAND Gate

TABLE I. Comparison of Typical AC Performance of LS-TTL, S-TTL, ALS-TTL and HC-CMOS

Gates		LS-TTL	ALS-TTL	HC-CMOS	S-TTL	Units
74XX00	Propagation Delay	8	5	8	4	ns
74XX04	Propagation Delay	8	4	8	3	ns
Combinational MSI						
74XX139	Propagation Delay					
	Select	25	8	25	8	ns
	Enable	21	8	20	7	ns
74XX151	Propagation Delay					
	Address	27	8	26	12	ns
	Strobe	26	7	17	12	ns
74XX240	Propagation Delay	12	3	10	5	ns
	Enable/Disable Time	20	7	17	10	ns
Clocked MSI						
74XX174	Propagation Delay	20	7	18	13	ns
	Operating Frequency	40	50	50	100	MHz
74XX374	Propagation Delay	19	7	16	11	ns
	Enable/Disable Time	21	9	17	11	ns
	Operating Frequency	50	50	50	100	MHz

LS-TTL and, as is expected, is slower than ALS and S-TTL logic. The slopes of these lines indicate the amount of variation in speed with loading, and are dependent on the output impedance of the particular logic gate. The delay variation of LS-TTL and HC-CMOS is similar whereas ALS-TTL and S-TTL have slightly less variation.

POWER DISSIPATION

CD4000B and MM54C/MM74C CMOS devices are well known for extremely low quiescent power dissipation, and high speed CMOS retains this feature. Table II compares typical HC static power consumption with LS, ALS and S-TTL. Even CMOS MSI dissipation is well below 1 μW while LS-TTL dissipation is many milliwatts. This makes MM54HC/MM74HC ideal for battery operated or ultra-low power systems where the system may be put to "sleep" by shutting off the system clock.

TABLE II. Comparison of Typical Quiescent Supply Current for Various Logic Families

	HC-CMOS	LS-TTL	ALS-TTL	S-TTL
SSI	0.0025 μW	5.0 mW	2.0 mW	75 mW
Flip-Flop	0.005 μW	20.0 mW	10 mW	150 mW
MSI	0.25 μW	90 mW	40 mW	470 mW

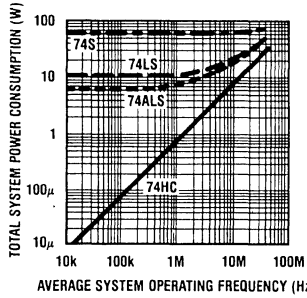
CMOS dissipation increases proportionately with operating frequency. Doubling the operating frequency doubles the current consumption. This is due to currents generated by charging internal and load capacitances. *Figure 2* shows power dissipation versus frequency for a completely unloaded NAND gate, flip-flop and counter implemented in all 4 technologies.

The LS, S and ALS curves are essentially flat because the quiescent currents mask out capacitive effects, except at very high frequencies. Capacitive effects are slightly lower for the TTL families, so that, at high frequencies, CMOS dissipation may actually be more than ALS and LS. However, the power crossover frequency is usually well above the maximum operating frequency of MM54HC/MM74HC.

The previously mentioned curves plot unloaded circuits. When considering typical system power consumption, capacitive loading should also be considered. Table III lists components to implement all the support logic for a small microprocessor based system. By assuming a typical load capacitance of 50 pF, the power dissipation for these devices can be calculated at various average system clock frequencies. *Figure 3* plots power consumption for 74HC, 74LS, 74ALS and 74S logic implementations. Above 1 MHz, capacitive currents now also tend to dominate bipolar power dissipation as well.

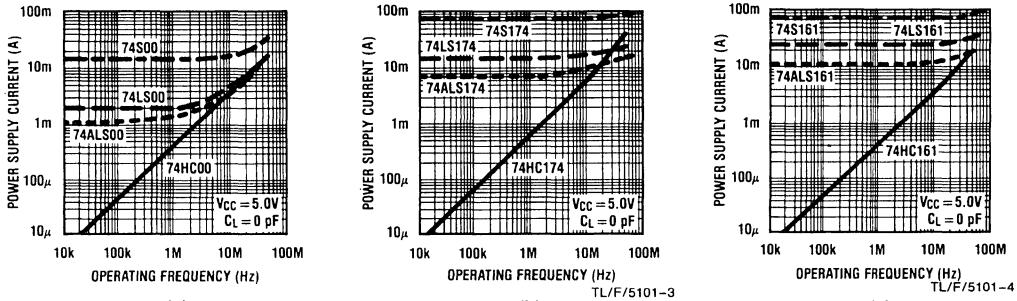
TABLE III. Hypothetical "Glue" Logic for a Typical Microprocessor System

System Components	# of ICs
Address Decoders ('138)	10
Address Comparators ('688)	5
Address/Data Buffers ('240/4)	10
Address/Data Latches ('373/4)	20
MSI Control/Gating ('00, '10)	30
Misc. Counter/Shift Reg ('161, '164)	20
Flip-Flops ('73/4)	10



TL/F/5101–2

FIGURE 3. Power Consumption for Hypothetical Microprocessor System Support Logic



TL/F/5101–3

TL/F/5101–4

FIGURE 2. Supply Current Consumption Comparison for (a) 74XX00 (b) 74XX714 (c) 74XX161 Circuits

Since, in a typical system, some sections will operate at a high frequency and other parts at lower frequencies, the average system clock frequency is a simplification. For example, a 10 MHz microprocessor will have a bus cycle frequency of 2 to 5 MHz. Most system and memory components will be accessed a small amount of the time, resulting in effective clock frequencies on the order of 100 kHz for these sections. Thus, the average system clock frequency would be around 1 to 2 MHz, and an 8 to 1 power savings would be realized by using CMOS.

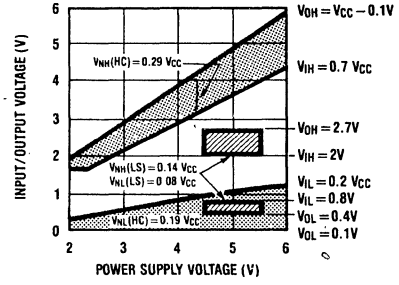
Another simplification was made to calculate system power. CMOS circuits will dissipate much less power when TRI-STATE®, which would save much power since, in a given bus cycle, only a few buffers will be enabled. LS, ALS and S, however, actually dissipate more power when their outputs are disabled.

Several interesting conclusions can be drawn from *Figure 3*. First, notice that, at higher frequencies, the bipolar logic families start to dissipate more power. This is a result of current consumption due to switching the load. As the operating frequency approaches infinity, this will be the dominant effect. So, for extremely fast low power systems, minimizing load capacitance and overall operating frequency becomes more important. As lower power TTL logic is introduced, system power will be increasingly dependent on capacitive load effects similar to CMOS.

Second, TTL logic has a slightly smaller logic voltage swing than CMOS. Thus, for a given load, TTL will actually have a lower average load current. So, similar to the unloaded example, at very high frequencies, CMOS could consume more power than TTL. As *Figure 5* indicates, these frequencies are usually far above the 30 MHz limit of HC-CMOS or LS-TTL.

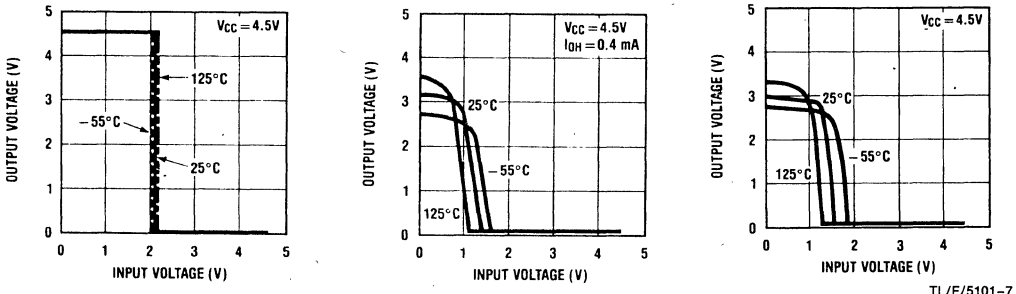
INPUT VOLTAGE CHARACTERISTICS AND NOISE IMMUNITY

To maintain the advantage CMOS has in noise immunity, the input logic levels are defined to be similar to metal gate CMOS. At $V_{CC}=5V$, MM54HC/MM74HC is designed to have input voltages of $V_{IH}=3.5V$ and $V_{IL}=1.0V$. Additionally, input voltage over the operating supply voltage range is: $V_{IH}=0.7V_{CC}$ and $V_{IL}=0.2V_{CC}$. This compares to $V_{IH}=2.0V$ and $V_{IL}=0.8V$ specified for LS-TTL over its supply range. *Figure 4* illustrates the input voltage differences, and the greater noise immunity HC logic has over its supply range. Maintaining wide noise immunity gives HC-CMOS an advantage in many industrial, automotive, and computer applications where high noise levels exist.



TL/F/5101–5

FIGURE 4. Worst-Case Input and Output Voltages Over Operating Supply Range for HC and LS Logic



(a) (b) (c)

TL/F/5101–6

TL/F/5101–7

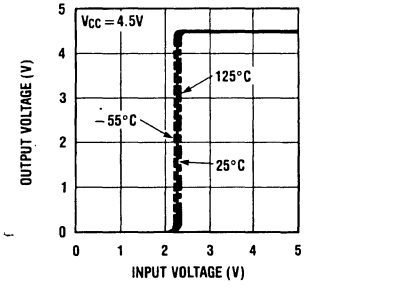
FIGURE 5. Input-Output Transfer Characteristics for 74XX00 NAND Gate Implemented in (a) HC-CMOS (b) LS-TTL (c) ALS-TTL

Another indication of DC noise immunity is the typical transfer characteristics for the logic families. *Figure 5* shows the transfer function of the 74XX00 NAND gate for HC-CMOS, LS-TTL and ALS-TTL. High speed CMOS has a very sharp transition typically at 2.25V, and this transition point is very stable over temperature. The bipolar logic transfer functions are not as sharp and vary several hundred millivolts over temperature. This sharp transition is due to the large circuit gains provided by triple buffering the HC-CMOS gate compared to the single bipolar gain stage. *Figure 6* compares the transfer function of the 'HC08 and the 'ALS08, both of which are double buffered. The 'ALS08 has a sharper transition, but the CMOS gate still has less temperature variation and a more centered trip point. However, the TTL trip point is not dependent on V_{CC} variation as CMOS is.

The high speed CMOS input levels are not totally compatible with TTL output voltage specifications. To make them compatible would compromise noise immunity, die size, and significant speed. The designer may improve compatibility by adding a pull-up resistor to the TTL output. He may also utilize a series of TTL-to-CMOS level converters which are being provided to ease design of mixed HC/LS/ALS/S systems. These buffers have 0.8V and 2.0V TTL input voltage specifications, and provide CMOS compatible outputs. When mixing logic, the noise immunity at the TTL to CMOS interface is no better than LS-TTL, but a substantial savings in power will occur when using MM54HC/MM74HC logic.

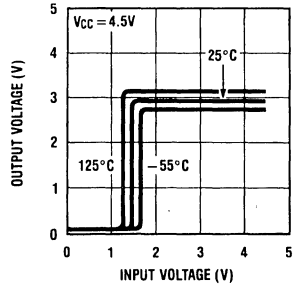
INPUT CURRENT

The HC family maintains the ultra-low input currents typical of CMOS circuits. This current is less than 1 μA and is caused by input protection diode leakages. This compares to the much larger LS-TTL input currents of 0.4 mA for a low input and 40 μA for a high input. ALS-TTL input currents are 0.2 mA and 20 μA and S-TTL input currents are 3.2 mA and 100 μA. *Figure 7* tabulates these values. The near zero input current of CMOS eases designing, since a typical input can be viewed as an open circuit. This eliminates the need for fanout restrictions which are necessary in TTL logic designs.



TL/F/5101–9

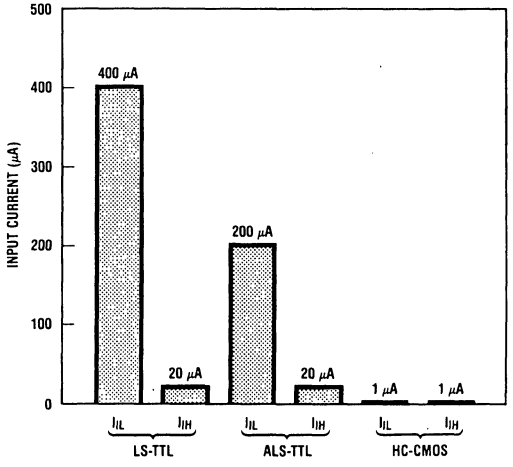
(a)



TL/F/5101–8

(b)

FIGURE 6. Input-Output Transfer Characteristics for 74XX08 AND Gate Implemented in (a) HC-CMOS (b) ALS-TTL



TL/F/5101–10

FIGURE 7. Comparison of Input Current Specifications for Various Logic Families

POWER SUPPLY RANGE

Figure 4 also compares the supply range of MM54HC/MM74HC logic and LS-TTL. The high speed CMOS family is specified to operate at voltages from 2V to 6V. 54LS, 54S and 54ALS logic is specified to operate from 4.5V to 5.5V, and 74LS and 74S will operate from 4.75V to 5.25V. 74ALS is specified over a 4.5V to 5.5V supply range. This wider operating range for the HC family eases power supply design by eliminating costly regulators and enhances battery operation capabilities.

OUTPUT DRIVE

Since there was no speed, noise immunity, or power tradeoff, standard HC-CMOS was designed to have similar high current output drive that is characteristic of LS-TTL and ALS-TTL. Schottky TTL has about 5 times the output drive of MM54HC/MM74HC. Thus HC-CMOS has an output low current specification of 4 mA at an output voltage of 0.4V. In keeping with CD4000B series and 54C/74C series logic, the source and sink currents are symmetrical. Thus HC logic can source 4 mA as well. This large increase in output current for high speed CMOS over CD4000B also has the added advantage of reducing signal line crosstalk which can be of greater concern in high speed systems. *Figure 8* compares HC, LS, and ALS specified output currents.

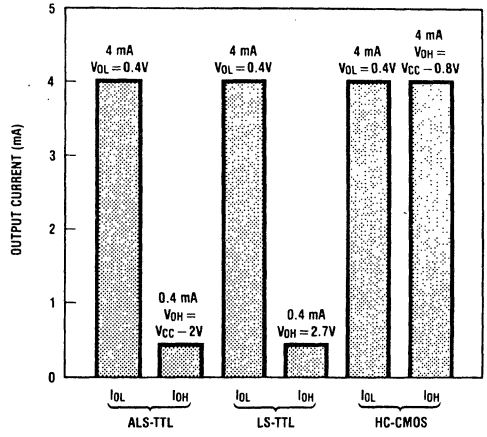
Since TTL logic families do have significant input currents they have a limited fanout capability. Table IV illustrates the limitations of these families, based on their input and output currents. High speed CMOS is also included. MM54HC/MM74HC has the same CMOS-to-CMOS fanout characteristics as CD4000B, virtually infinite.

TABLE IV. Fanout of HC-CMOS, LS-TTL, ALS-TTL, S-TTL

From, To	74HC	74LS	74ALS	74S
74HC	4000	10	20	2
74LS	*	20	40	4
74ALS	*	20	40	4
74S	*	50	100	10

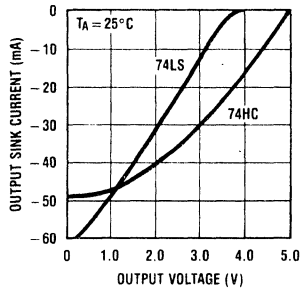
As another indication of the similarity of HC-CMOS to LS-TTL, *Figure 9* plots typical output currents versus output voltage for LS and HC. The output sink current curves are very similar, but LS source current is somewhat different, due to its emitter-follower output circuitry.

MM54HC/MM74HC bus driving circuits, namely the TRI-STATE buffers and latches, have half again as much output current drive as standard outputs. These components have a 6 mA output drive. The 6 mA was chosen based on a trade-off of die size and speed-load variations. This current is less than the 12 mA or more specified for LS and ALS bus driver circuits, because the bus fanout limitations of these families do not apply in CMOS systems. S-TTL bus output sink current is 48 mA.



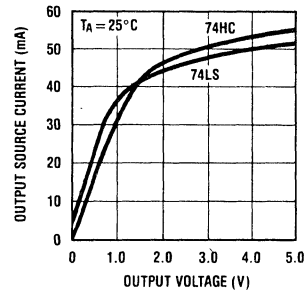
TL/F/5101-11

FIGURE 8. Output Current Specifications for ALS-TTL, S-TTL and HC-CMOS



TL/F/5101-12

(a)



TL/F/5101-13

(b)

FIGURE 9. Comparison of Standard LS-TTL and HC-CMOS Output (a) Source (b) Sink Currents

OPERATING TEMPERATURE RANGE

The operating temperature range and temperature effects on various HC-CMOS operating parameters differ from bipolar logic. The recommended temperature range for 74LS, 74S, and 74ALS is 0°C to 70°C, compared to −40°C to 85°C for the 74HC family. 54 series logic is specified from −55°C to 125°C for all four families.

Temperature variation of operating parameters for the MM54HC/MM74HC family behaves very predictably and is due to the gain decreasing of MOSFET transistors as temperature is increased. Thus the output currents decrease and propagation delays increase at about 0.3% per degree centigrade.

Figure 10 shows typical propagation delays for the 74XX00 over the −55°C to +125°C temperature range. The 'HC00's speed increases almost linearly with temperature, whereas the LS and ALS behave differently.

A WORD ABOUT PLUG-IN REPLACEMENT OF TTL

MM54HC/MM74HC logic implements TTL equivalent functions with the same pin outs as TTL. HC is not designed to be directly plug-in replaceable, but, with some care, some TTL systems can be converted to MM54HC/MM74HC with little or no modification. The replaceability of HC is determined by several factors.

One factor is the difference in input levels. In systems where all TTL is not being replaced and TTL outputs feed CMOS inputs, the input high voltages, as specified, are not totally compatible. Although TTL outputs will typically drive HC inputs correctly, an external pull-up resistor should be added to the TTL outputs, or an MM54HCT/MM74HCT TTL compatible circuit should be used. This incompatibility tends to limit the designer's ability to intermingle TTL and HC-CMOS. Note, though, that HC outputs are completely compatible with the various TTL family's input specifications; therefore, there is no problem when HC is driving TTL.

Another source of possible problems can occur when the LS design floats device inputs. This practice is not recommended when using LS-TTL, but it is sometimes done. Usually, TTL inputs float high; however, CMOS inputs may float either high or low depending on the static charge on the input. It is therefore important to always tie unused CMOS inputs to either V_{CC} or ground to avoid incorrect logic functioning.

A third factor to consider when replacing any TTL logic is AC performance. The logic functions provided by 54HC/74HC are equivalent to LS-TTL, and the propagation delay, set-up and hold times are similar to LS. However, there are some differences in the way CMOS circuits are implemented which will cause differences in speed. For the most part, these differences are minor, but it is important to verify that they do not affect the design.

CONCLUSION

The MM54HC/MM74HC family represents a major step forward in CMOS performance. It is a full line family capable of being designed into virtually any application which now uses LS-TTL with substantial improvement in power consumption. ALS and S-TTL primarily offer faster speeds than HC-CMOS, but still do not have the input and output advantages or the lower power consumption of CMOS. Because of its high input impedance and large output drive, HC logic is actually easier to use. This, coupled with continued expansion of the 54HC/74HC, will make it an increasingly popular logic family.

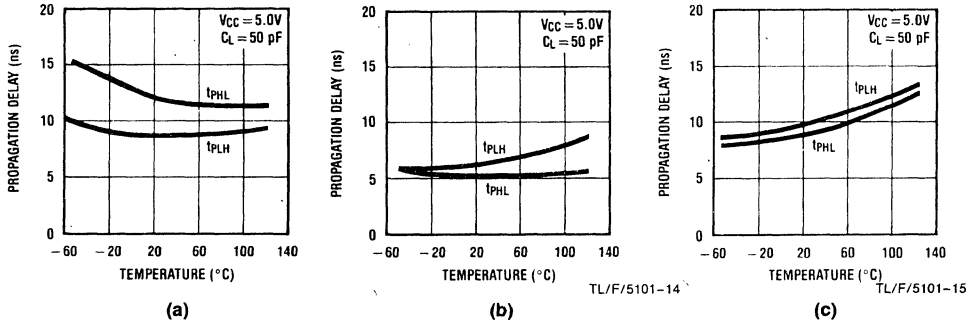


FIGURE 10. Propagation Delay Variation Across Temperature for (a) 74LS00 (b) 74ALS00 and (c) 74HC00

National's Process Enhancements Eliminate the CMOS SCR Latch-Up Problem In 54HC/74HC Logic

National Semiconductor
Application Note 339
Larry Wakeman
May 1983

INTRODUCTION

SCR latch-up is a parasitic phenomena that has existed in circuits fabricated using bulk silicon CMOS technologies. The latch-up mechanism, once triggered, turns on a parasitic SCR internal to CMOS circuits which essentially shorts V_{CC} to ground. This generally destroys the CMOS IC or at the very least causes the system to malfunction. In order to make MM54HC/MM74HC high speed CMOS logic easy to use and reliable it is very important to eliminate latch-up. This has been accomplished through several layout and process enhancements. It is primarily several proprietary innovations in CMOS processing that eliminates the SCR.

First, what is "SCR latch-up?" It is a phenomena common to most monolithic CMOS processes, which involves "turning on" a four layer thyristor structure (P-N-P-N) that appears from V_{CC} to ground. This structure is formed by the parasitic substrate interconnections of various circuit diffusions. It most commonly can be turned on by applying a voltage greater than V_{CC} or less than ground any input or output, which forward biases the input or output protection diodes. *Figure 1* schematically illustrates these diodes found in the MM54HC/MM74HC family. Standard CD4000 and MM54C/MM74C logic also has a very similar structure. These diodes can act as the gate to the parasitic SCR, and if enough current flows the SCR will trigger. A second method of turning on the SCR is to apply a very large supply voltage across the device. This will breakdown internal diodes causing enough current to flow to trigger latch-up. In HC logic the typical V_{CC} breakdown voltage is above 10V so this method is more uncommon. In either case, once the SCR is turned on a large current will flow from V_{CC} to ground, causing the CMOS circuit to malfunction and possibly damage itself.

CMOS SCR problems can be minimized by proper system design techniques or added external protection circuits, but obviously the reduction or elimination of latch-up in the IC itself would ease CMOS system design, increase system reliability and eliminate additional circuitry. For this reason it was important to eliminate this phenomena in National's high speed CMOS logic family.

Characterization of this proprietary high speed CMOS process for latch up has verified the elimination of this parasitic mechanism. In tests conducted under worst case conditions ($V_{CC}=7V$ and $T_A=125°C$) it has been impossible to latch-up these devices on the inputs or on the outputs.

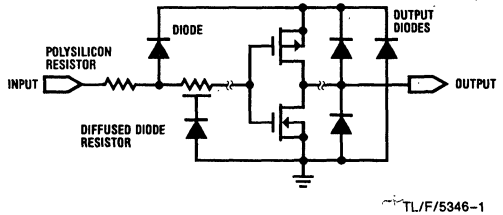
In testing for latch-up, caution must be exercised when trying to force large currents into an IC. As with any integrated circuit there are maximum limitations to the current handling capabilities of the internal metalization, and diodes, and thus they can be damaged by excessive currents. This is discussed later in the test section.

To enable the user to understand what latch-up is and how it has been eliminated, it is useful to review the operating of a simple discrete SCR, and then apply this to the CMOS SCR. Since most latch-up problems historically have been caused by extraneous noise and system transients, the AC characteristics of CMOS latch are presented. Also various methods of external and internal protection against latch-up is discussed as well as example test methods for determining the latch up susceptibility of CMOS IC's.

SIMPLE DISCRETE SCR OPERATION

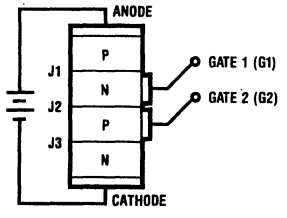
To understand the behavior of the SCR structure parasitic to CMOS IC's, it is first useful to review the basic static operation of the discrete SCR, and then apply it to the CMOS SCR. There are two basic trigger methods for this SCR. One is turning on the SCR by forcing current into its gate, and the second is by placing a large voltage across its anode and cathode. *Figure 2* shows the basic four layer structure biased into its forward blocking state. The SCR action can be more easily understood if this device is modeled as a cross coupled PNP and NPN transistor as shown in *Figure 3*.

In the case of latch-up caused by forward biasing a diode, if current is injected into the base of Q2, this transistor turns on, and a collector current beta times its base current flows into the base of Q1. Q1 in turn amplifies this current by beta and feeds it back into the base of Q2, where the current is again amplified. If the product of the two transistors' Beta becomes greater than one, B(NPN)xB(PNP)>1, this current multiplication continues until the transistors saturate, and the SCR is triggered. Once the regenerative action occurs a large anode current flows, and the SCR will remain on even after the gate current is removed, if enough anode current flows to sustain latch-up. However, if the transistor current gains are small no self sustaining positive feedback will occur, and when the base current is removed the collector current will stop. In a similar manner the SCR can be triggered by drawing current by forward biasing the base of Q1.



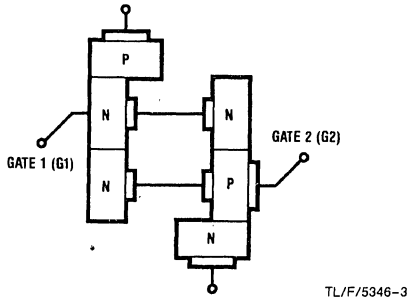
TL/F/5346–1

FIGURE 1. Schematic Diagram of Input and Output Protection Structures

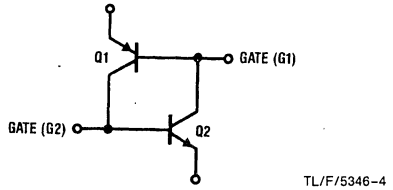


TL/F/5346–2

FIGURE 2. Simplified SCR Structure



TL/F/5346-3



TL/F/5346-4

FIGURE 3. Cross-Coupled Transistor Model of SCR

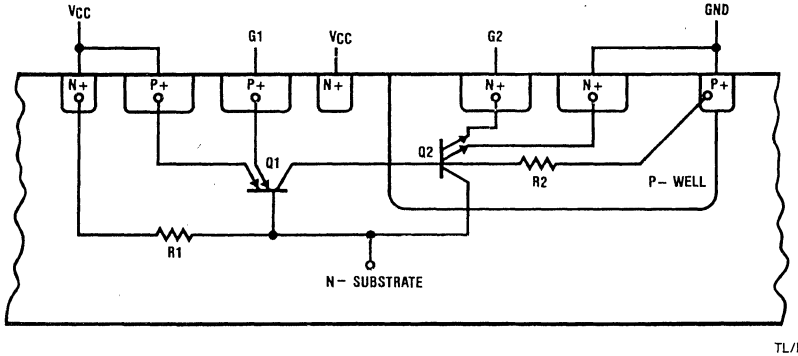
The second case, the SCR may also be triggered without injecting any gate current. In the forward blocking state the small leakage current that is present does not trigger the SCR, but if the voltage is increased to a point where significant leakage currents start conducting, these currents could also trigger the SCR, again forming a low impedance path through the device. The same requirement that the Beta product of the PNP and NPN be greater than one in order for the SCR to trigger applies here as well. This leakage current trigger is characteristic of Schottkey diode operation.

THE CMOS SCR: STATIC DC OPERATION

For discussion purposes CMOS SCR latch up characteristics can be divided into two areas. One is the basic operation of the SCR when static DC voltages are applied, and the second is the behavior when transients or pulses are applied.

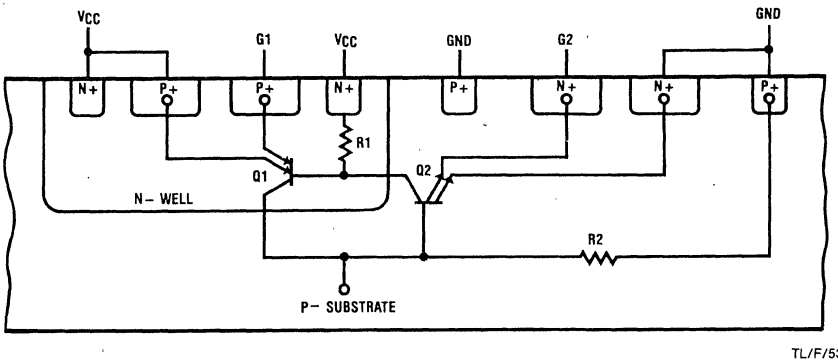
First looking at the device statically, the parasitic SCR in CMOS integrated circuits is much more complex and its triggering is somewhat different than the simple SCR already discussed. However, the regenerative feedback effect is basically the same. *Figure 4a* shows a simplified P− well CMOS structure illustrating only the diffusions and the resultant parasitic transistors. The NPN transistor is a vertical device whose emitter is formed by n+ diffusions. The P− well forms the base and the N− substrate forms the collector of the NPN. The PNP transistor is a lateral device. Its emitter is formed by p+ diffusions, its base is the N− substrate, and its collector is the P− well.

Figure 4b illustrates a cross section of a simplified N− well process and its corresponding parasitic bipolar transistors. In this process the NPN is a lateral device and the PNP is vertical. Essentially the description of the P− well SCR is the same as the N− well version except the NPN is a low gain lateral device and the PNP is a high gain vertical transistor. Thus the following discussion for the P− well also applies to the N− well with this exception.



TL/F/5346-6

(a)

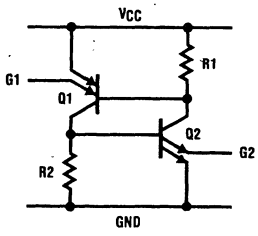


TL/F/5346-5

(b)

FIGURE 4. Simplified Cross Section of CMOS Processes a) P− well and b) N− well

The transistors for the P− well CMOS process are drawn schematically in *Figure 5*, so that their cross coupled interconnection is more easily seen. The SCR structure in *Figure 5* differs from that of *Figure 3* in two ways. First, the transistors of *Figure 5* have multiple emitters, due to the many diffusions on a typical die. One emitter of each transistor could function as the trigger input to the SCR. Secondly, R1 and R2 have been added and are due to P− and N− substrate resistances between the base of each transistor and the substrate power supply contacts.



TL/F/5346–7

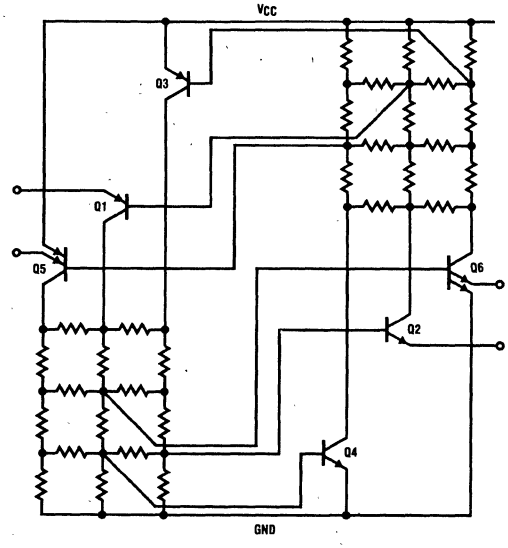
FIGURE 5. Schematic of Simple SCR Model

Like the discrete SCR there are two basic methods of turning the CMOS SCR on. The first method is however slightly different. In the CMOS parasitic SCR current cannot be directly injected into the base of one of its transistors. Instead either node G1 must be raised above V_{CC} enough to turn on Q1, or node G2 must be lowered below ground enough to turn on Q2. If G1 is brought above V_{CC}, current is injected from the emitter of Q1 and is swept to the collector of Q1. The collector of Q1 feeds the base of Q2 and also R2. R2 has the effect of stealing current from the base of Q2, but as current flows through R2 a voltage will appear at the base of Q2. Once this voltage reaches 0.6 volts Q2 will turn on and feed current from its collector back into R1 and into Q1. If 0.6 volts is generated across R1, Q1 then turns on even more.

Again, if the two transistors have enough gain and enough anode current flows to sustain the SCR, it will turn on, and remain on even after G1 is returned to V_{CC}. The actual requirements for latch up are altered by the two resistors, R1 and R2. Since the resistors shunt some current away from the base of both transistors, the resistors essentially reduce the effective gains of the transistors. Thus the transistors must actually have much higher gains in order to achieve an overall SCR loop gain greater than one, and hence enable the SCR to trigger. The actual equations to show quantitatively how the resistors effect the SCR's behavior could be derived, but it is sufficient to notice that as R1 and R2 become smaller the SCR becomes harder to turn on. IC designers utilize this to reduce latch up.

The second method of turning on the SCR mentioned earlier also applies here. If the supply voltage is raised to a large value, and internal substrate diodes start breaking down excessive leakage currents will flow possibly triggering the SCR. The resistors also affect this trigger method as well, since they steal some of the leakage currents from Q1 and Q2, and hence it takes more current to trigger the SCR. In high speed CMOS the process enhancements reduce the transistor betas and hence eliminate latch up by this mechanism as well.

While useful, the SCR model of *Figures 4 and 5* is very simplified, since in actuality the CMOS SCR is a structure with many transistors interconnected by many resistances. Although still somewhat simiplified, *Figure 6* attempts to illustrate how the parasitics on a chip connect. It is important to remember that any transistor or diode diffusion can parasitically form part of the SCR. In the figure transistor Q1 and Q2 are single emitter transistors formed by the input protection diodes. Internal P and N channel transistors have no external connection and are represented by Q3 and Q4. Q5 and Q6 represent output transistor diffusions, and the second emitter corresponds to the output. All of these transistors are connected together by the N− substrate and P− well resistances, which are illustrated by the resistor mesh.



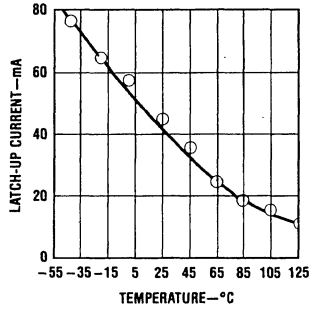
TL/F/5346–8

FIGURE 6. Distributed Model of CMOS SCR

If any of the emitters associated with the trigger inputs G1–G4 become forward biased the SCR may be triggered. Also due to the intertwined nature of this structure, part of the SCR may be initially latched up. In this case only a limited amount of current may flow, but this limited latch up may spread and cause other parts to be triggered until eventually the whole chip is involved.

In general the trigger to the SCR has been conceptualized as a current, since ideally the CMOS input looks into the base of the SCR transistors. However this may not be quite true. There may be some resistance in series with each base, due to substrate or input protection resistances. In newer silicon gate CMOS processes, MM54HC/MM74HC for example, a poly-silicon resistor is used for electrostatic protection, and this enables larger voltages to be applied to the circuit pins without causing latchup. This is because the poly resistor actually forms a current limit resistor in series with the diodes. In most applications the designer is more concerned with accidental application of a large voltage, and the use of the poly resistor internally enables good voltage resistance to latch up. CMOS outputs are directly connected to parasitic output diodes since no poly resistor can be placed on an output without degrading output current drive. Thus the output latch up mechanism is usually thought of as a current.

Temperature variations will affect the amount of current required to trigger the SCR. This is readily understandable since temperature effects the bipolar transistor's gain and the resistance of the base-emitter resistors. Generally, as the temperature is increased less current is needed to cause latch-up. This is because as temperature increases the bipolar transistor's base-emitter voltage decreases and the base-emitter resistor value increases. *Figure 7* plots trigger current versus temperature for a sensitive CMOS input. This data was taken on a CMOS device without any layout or process enhancements to eliminate latch up. Increasing temperature from room to 125°C will reduce the trigger current by about a factor of three. Once the circuit is latched up, heating of the device die caused by SCR currents will actually increase the susceptibility to repeated latch up.



TL/F/5346–9

FIGURE 7. Temperature versus SCR Trigger Current for Special CMOS Test Structure

OTHER LATCH UP TRIGGER METHODS

There are some other methods of latching up CMOS circuits, they are not as circuit design related and shall only be briefly mentioned. The first is latch up due to radiation bombardment. In hostile environments energetic atomic particals can bombard a CMOS die freeing carriers in the substrate. These carriers then can cause the SCR to trigger. This can be of concern in high radiation environments which call for some sort of radiation hardened CMOS logic.

Another latch up mechanism is the application of a fast rise or fall spike to the supply inputs of a CMOS device. Even if insufficient current is injected into the circuit the fast voltage change could trigger latch up. This occurs because the voltage change across the part changes the junction depletion capacitances, and this change in capacitance theoretically could cause a current that would trigger the SCR latch. In actual practice this is very difficult to do because the response time of the SCR (discussed shortly) is very poor. This is hardly a problem since power supplies must be adequately decoupled anyway.

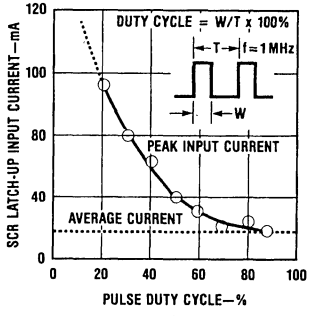
A third latch up cause which is completely internal to the IC itself and is out of the control of the system designer is internally triggered latch up. Any internal switching node connects to a diode diffusion, and as these diffusions switch the junction depletion capacitance associated with these nodes changes causing a current to be generated. This current could trigger the SCR. The poor frequency response of the SCR tends to make this difficult, but as chip geometries are shrunk packing densities will increase and the gain of the lateral PNP transistor increase. This may increase the latch up susceptibility. It is up to the IC designer to ensure that this doesn't happen, and care in the layout and circuit design of 54HC/74HC logic has ensured that this will be avoided.

THE CMOS SCR: TRANSIENT BEHAVIOR

With the introduction of fast CMOS logic the transient nature of the CMOS SCR phenomena becomes more important because signal line ringing and power supply transients are more prevalent in these systems. Older metal gate CMOS (CD4000 & 74HC) circuits have slow rise and fall times which do not cause a large amount of line ringing. Power supply spiking is also somewhat less, again due to slow switching times associated with these circuits.

The previous discussion assumed that the trigger to the CMOS SCR was essentially static and was a fixed current. Under these conditions a certain value current will cause the SCR to trigger, but if the trigger is a short pulse the peak value of the pulse current that will trigger the SCR can be much larger than the static DC trigger current. This is due to the poor frequency characteristics of the SCR.

For short noise pulses, $<5\ \mu s$, the peak current required to latch up a device is dependent on the duty cycle of the pulses. At these speeds it is the average current that causes latch-up. For example, if a 1 MHz 50% duty cycle over voltage pulse train is applied to a device that latched with 20 mA DC current, then typically the peak current required will be about 40 mA. For a 25% duty cycle the peak current would be 80 mA. An example of this is shown in *Figure 8* which plots latch up current against over-voltage pulse width at 1 MHz.

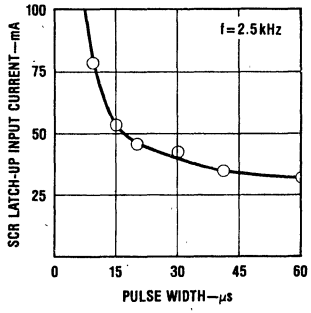


TL/F/5346–10

FIGURE 8. Trigger Current of SCR of Input Overvoltage Pulses at High Repetition Rate on Special Test Unit

If the pulse widths become long, many microseconds, the latch up current will approach the DC value even for low duty cycles. This is shown in *Figure 9* which plots peak trigger current vs pulse width for the same test device used in *Figure 8*. The repetition rate in this case is a slow 2.5 kHz (period = 400 μs). These long pulse widths approach the trigger time of the SCR, and thus pulses lasting several microseconds are long enough to appear as DC voltages to the SCR. This indirectly indicates the trigger speed of the SCR to be on the order of ten to fifteen microseconds. This is however dependent on the way the IC was designed and the processing used.

In normal high speed systems noise spikes will typically be only a few nanoseconds in duration, and the average duty cycle will be small. So even a device that is not designed to



TL/F/5346–11

FIGURE 9. Trigger Current of Pulse on Special Test Unit SCR for Single Transient Overvoltage

be latch up resistant, will probably not latch up even with significant line ringing on its inputs or outputs (Then again . . .). However, in some systems where inductive or other loads are used transients of several microseconds can be easily generated. For example, some possible applications are automotive and relay drivers. In other CMOS logic families spikes of this nature are much more likely to cause the SCR to trigger, but here again MM54HC/MM74HC high speed CMOS is immune.

PREVENTING SCR LATCH UP: USER SYSTEM DESIGN SOLUTIONS

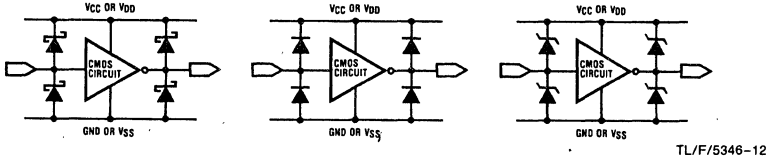
SCR latch-up can be prevented either on the system level or on the IC level. Since National's MM54HC/MM74HC series will not latch up, this eliminates the need for the system designer to worry about preventing latch up at the system level. This not only eases the design, but negates the need to add external diodes and resistors to protect the CMOS circuit, and hence additional cost. (Note however that even though the devices don't latch up, diode currents should be limited to their Absolute Maximum Ratings listed in the Data Sheets).

If one is using a CMOS device that may latch up, older CD4000 CMOS or another vendors HC for example, and its input or output voltages may forward bias the input or output diodes then some external circuitry may need to be added to eliminate possible SCR triggering. As with the previous discussions of latch-up preventing SCR latch-up falls into two categories: the static case, and the transient condition. Each is related but has some unique solutions.

In the static condition to ensure SCR latch up does not occur, the simplest solution is to design CMOS systems so that their input/output diodes don't become forward biased. To ease this requirement some special circuits that have some of their input protection diodes removed are provided, and this enables input voltages to exceed the supply range. These devices are MM54HC4049/50, CD4049/50, and MM54C901/2/3/4.

If standard logic is used and input voltages will exceed the supply range, an external network should be added that protects the device by either clamping the input voltage or by limiting the currents which flow through the internal diodes. *Figure 10* illustrates various input and output diode clamping circuits that shunt the diode currents when excessive input voltages are applied. Usually either an additional input or output diode is required, rarely both, and if the voltages only exceed one supply then only one diode is necessary. If an external silicon diode is used the current shunt is only partially effective since this diode is in parallel with the internal silicon protection diode, and both diodes clamp to about 0.7V.

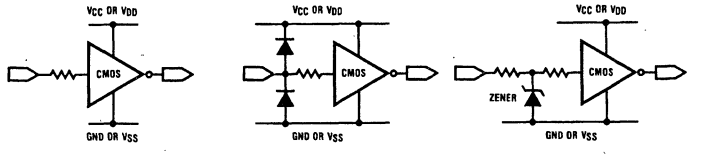
A second method, limiting input current, is very effective in preventing latch-up, and several designs are shown in *Figure 11*. The simplest approach is a series input resistor. It is recommended that this resistor should be as large as possible without causing excessive speed degradation yet ensure the input current is limited to a safe value. If speed is critical, it is better to use a combination diode-resistor network as shown in *Figures 11b* and *11c*. These input networks effectively limit input currents while using lower input resistors. The series resistor may not be an ideal solution for protecting outputs because it will reduce the effective drive of the output. In most cases this is only a problem when the output must drive a lot of current or must switch large capacitances quickly.



TL/F/5346–12

Schottky Diodes (a) **Germanium Diodes (b)** **Zener Diodes (c)**

FIGURE 10. External Input and Output Protection Diodes Circuits for Eliminating SCR Latch-up

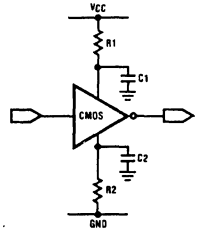


TL/F/5346–13

(a) **(b)** **(c)**

FIGURE 11. Input Resistor and Resistor-Diode Protection Circuits for Eliminating Latch-up

A third approach is instead of placing resistors in series with the inputs to place them in series with the power supply lines as shown in *Figure 12*. The resistors must be bypassed by capacitors so that momentary switching currents don't produce large voltage transients across R1 and R2. These resistors can limit input currents but primarily they should be chosen to ensure that the supply current that can flow is less than the holding current of the SCR. Thus even though the input current can cause latch up it cannot be sustained and the IC will not be damaged.



TL/F/5346–14

FIGURE 12. Supply Resistor-Capacitor Circuits for Eliminating Latch-up

This last solution has the advantage of fewer added components, but also has some disadvantages. This method may not prevent latch up unless the resistors are fairly large, but this will greatly degrade the output current drive and switching characteristics of the device. Secondly, this circuit protects the IC from damage but if diodes currents are applied causing large supply currents, the circuits will logically malfunction where as with other schemes logic malfunction can be prevented as well.

PREVENTING LATCH UP: IC DESIGN SOLUTIONS

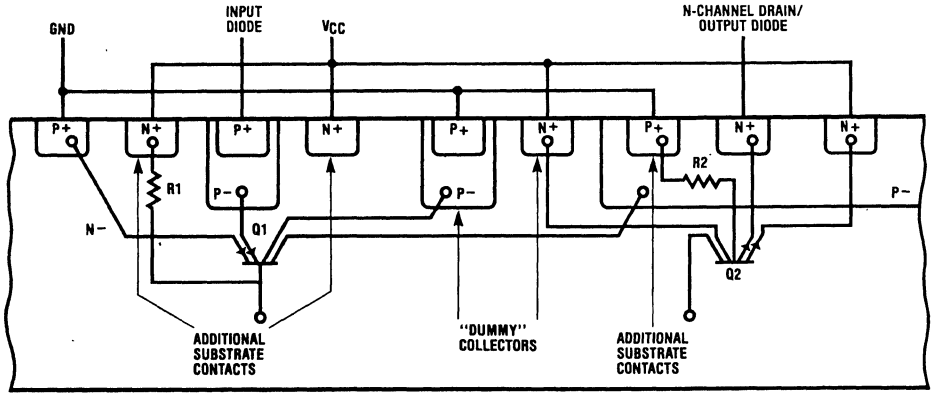
The previous latch up solutions involve adding extra components and hence extra cost and board space. One can imagine that in a microprocessor bus system if for some reason the designer had to protect each output of several CMOS devices that are driving a 16-bit address bus that up to 32 diodes and possibly 16 resistors may need to be added. Thus for the system designer the preferable solution is to use logic that won't latch up.

Most methods previously employed to eliminate latch up are either not effective, increase the die size significantly, and/or degrade MOS transistor performance. The process enhancements employed on 54HC/74HC logic circumvent these problems. Primarily it is effective without degrading MOS performance.

When designing CMOS integrated circuits, there are many ways that the SCR action of these circuits can be reduced. One of the several methods of eliminating the SCR is to reduce the effective gain of at least one of the transistors, thus eliminating the regenerative feedback. This can be accomplished either by modifying the process and/or by inserting other parasitic structures to shunt the transistor action. Also the substrate resistances modeled as R1 and R2 in *Figures 4* and *5* can be reduced. As these resistances approach zero more and more current is required to develop enough voltage across them to turn on the transistors.

As mentioned, the current gains of the NPN and PNP parasitic transistors directly affect the current required to trigger the latch. Thus some layout and process enhancements can be implemented to reduce the NPN and PNP Betas. In a P−well process the gain of the vertical NPN is determined by the specific CMOS process, and is dependent on junction depths and doping concentrations. These parameters also control the performance of the N-MOS transistors as well and so process modification must be done without degrading CMOS performance. To reduce the gain of the vertical PNP the doping levels of the P− well can be increased. This will decrease minority carrier lifetimes. It will also reduce the substrate resistance lowering the NPN base-emitter resistance. However this will increase parasitic junction capacitances, and may affect NMOS threshold voltages and carrier mobility. The depth of the well may be increased as well. This will reduce layout density due to increased lateral diffusion, and increase processing time as it will take longer to drive the well deeper into the substrate.

The lateral PNP's gain is determined by the spacing of input and output diode diffusions to active circuitry and minority carrier life times in the N− substrate. The carrier life times are a function of process doping levels as well, and care must be exercised to ensure no MOS transistor performance degradation. Again the doping levels of the substrate can be increased, but this will increase parasitic junction capacitances, and may alter the PMOS threshold characteristics. The spacing between input/output diodes and other



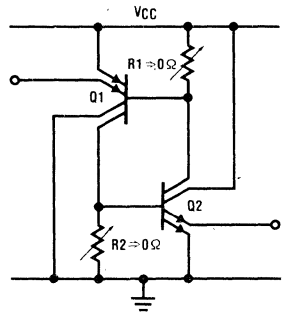
TL/F/5346–15

FIGURE 13. Simplified CMOS Cross Section Showing Added Latch-up Reduction Structures

diffusions can be increased. This will increase the PNP's base width, lowering its beta. This may be done only a limited amount without significantly impacting die size and cost.

Another method for enhancing the latch-up immunity of MM54HC/MM74HC is to short out the SCR by creating additional parasitic transistors and reducing the effective substrate resistances. These techniques employ the use of ringing structures (termed guard rings) to surround inputs and outputs with diffusions that are shorted to V_{CC} or ground. These diffusions act to lower the substrate resistances, making it harder to turn on the bipolar transistors. They also act "dummy" collectors that shunt transistor action by collecting charges directly to either V_{CC} or ground, rather than through active circuitry. *Figure 13* shows a cross section of how this might look and *Figure 14* schematically illustrates how these techniques ideally modify the SCR structure.

Ideally, in *Figure 14* if the inputs are forward biased any transistor action is immediately shunted to V_{CC} or ground through the "dummy" collectors. Any current not collected will flow through the resistors, which are now much lower in value and will not allow the opposite transistor to turn on.



TL/F/5346–16

FIGURE 14. Schematic Representation of SCR with Improvements to Reduce Turn On.

Unfortunately in order to reduce latch up these techniques add quite significantly to the die size, and still may not be completely effective.

The ineffectiveness of the ringing structures at completely eliminating latch up is for one because the collectors are only surface devices and carriers can be injected very deep into the N− substrate. Thus they can very easily go under the fairly small "dummy" collectors and be collected by the relatively large active P− well. A possible solution might be to make the collector diffusions much deeper. This suffers from the same drawbacks as making the well deeper, as well as requiring additional mask steps increasing process complexity. Secondly, the base emitter resistances can be reduced only so much, but again only the surface resistances are reduced. Some transistor action can occur under the P− well and deep in the N− bulk where these surface shorts are only partially effective.

The above discussion described modifications to a P− well process. For an N− well process the descriptions are the same except that instead of a P− well an N− well is used resulting in a vertical PNP instead of an NPN and a lateral NPN instead of a PNP.

These methods are employed in 54HC/74HC CMOS logic, but in addition processing enhancements were made that effectively eliminate the PNP transistor. The primary enhancement is a modification to the doping profile of the N− substrate (P− well process). This lowers the conductivity of the substrate material while maintaining a lightly dope surface concentration. This allows optimum performance NMOS and PMOS transistors while dramatically reducing the gain of the PNP and its base-emitter resistance. The gain of the PNP is reduced because the minority carrier lifetimes are reduced. This modification also increases the effectiveness of the "dummy" collectors by maintaining carriers closer to the surface. This then eliminates the SCR latch up mechanism.

5.0 TESTING SCR LATCH-UP

There are several methods and test circuits that can be employed to test for latch-up. The one primarily used to characterize the 54HC/74HC logic family is shown in *Figure 15*. This circuit utilizes several supplies and various meters to either force current into the V_{CC} diodes or force current out of the ground diodes. By controlling the input supply a current is forced into or out of an input or output of the test device. As the input supply voltage is increased the current into the diode increases. Internal transistor action may cause some supply current to flow, but this should not be considered latch up. When latch-up occurs the power supply current will jump, and if the input supply is reduced to zero the power supply current should remain. The input trigger current is the input current seen just prior to the supply current jumping.

Testing latch-up is a destructive test, but in order to test 54HC/74HC devices without causing immediate damage, test limits for the amount of input or output currents and supply voltages should be observed. Even though immediate damage is avoided, SCR latch-up test is a destructive test and the IC performance may be degraded when testing to these limits. Therefore parts tested to these limits should not be used for design or production purposes. In the case of National's high speed CMOS logic the definition of "latch-up proof" requires the following test limits when using the standard DC power supply test as is shown in *Figure 15*.

1. Inputs: When testing latch-up on CMOS inputs the current into these inputs should be limited to less than 70 mA. Application of currents greater than this may damage the input protection poly resistor or input metalization, and prevent further testing of the IC.
2. Outputs: When testing outputs there is a limit to the metalization's current capacity. Output test currents should be limited to 200 mA. This limitation is due again to metalization short term current capabilities, similar to inputs. Application of currents greater than this may blow out the output.
3. Supply: The power supply voltage is recommended to be 7.0V which is at the absolute maximum limit specified in 54HC/74HC and is the worst case voltage for testing latch-up. If a device latches up it will short out the power supply and self destruct. (Another Vendors HC may latch-up for example.) It is recommended that to prevent immediate destruction of other vendors parts that the power supply be current limited to less than 300 mA.

In almost all instances at high temperature, if it is going to occur, latch-up will occur at current values between 0–50 mA.

There are a few special considerations when trying to measure worst case latch-up current. Measuring input latch-up current is straight forward, just force the inputs above or below the power supply, but to measure an output it must first be set to a high level when forcing it above V_{CC}, or to a low level when forcing it below ground. When measuring Tri-State outputs, the outputs should be disabled, and when measuring analog switches they should be either left open or turned off.

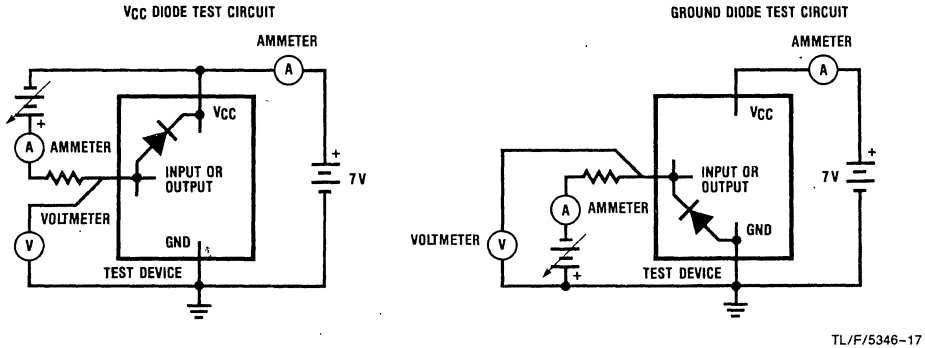
To measure the transient behavior of the test device or to reduce IC heating effects a pulse generator can be used in place of the input supply and an oscilloscope with a current probe should then replace the current meter. Care should be exercised to avoid ground loops in the test hardware as this may short out the supplies.

Although there are several methods of testing latch-up, this method is very simple and easy to understand. It also yields conservative data since manually controlling the supplies is a slow process which causes localized heating on the chip prior to latch-up, and lowers the latch-up current.

6.0 CONCLUSION

SCR latch-up in CMOS circuits is a phenomena which when understood can be effectively controlled both from the integrated circuit and system level. National's proprietary CMOS process and layout considerations have eliminated CMOS latch-up in the MM54HC/MM74HC family. This will increase the ease of use and design of this family by negating the need for extra SCR protection circuitry as well as very favorable impact system integrity and reliability.

Testing SCR Latch-Up of HCMOS



TL/F/5346–17

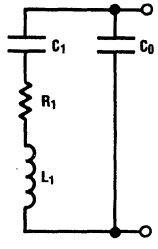
$T_A = 125°C$

FIGURE 15. Bench Test Setup for Measuring Latch-up

HCMOS Crystal Oscillators

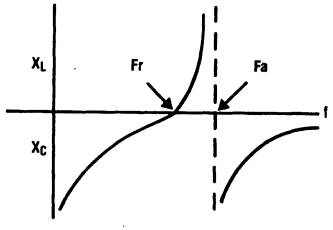
National Semiconducter
Application Note 340
Thomas B. Mills
May 1983

With the advent of high speed HCMOS circuits, it is possible to build systems with clock rates of greater than 30 MHz. The familiar gate oscillator circuits used at low frequencies work well at higher frequencies and either L–C or crystal resonators maybe used depending on the stability required. Above 20 MHz, it becomes expensive to fabricate fundamental mode crystals, so overtone modes are used.



TL/F/5347–1

Crystal Equivalent Circuit



TL/F/5347–2

Reactance of Crystal Resonator
FIGURE 1

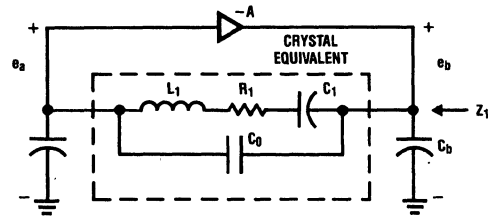
Basic Oscillator Theory

The equivalent circuit of a quartz crystal, and its reactance characteristics with frequency are shown in *Figure 1*. F_R is called the resonant frequency and is where L_1 and C_1 are in series resonance and the crystal looks like a small resistor R1. The frequency F_A is the antiresonant frequency and is the point where L_1–C_1 look inductive and resonate with C_O to form the parallel resonant frequency F_A, F_R and F_A are usually less than 0.1% apart. In specifying crystals, the frequency F_R is the oscillation frequency to the crystal in a series mode circuit, and F_R is the parallel resonant frequency. In a parallel mode circuit, the oscillation frequency will be slightly below F_A where the inductive component of the $L_1 - C_1$ arm resonates with C_O and the external circuit capacitance. The exact frequency is often corrected by the crystal manufacture to a specified load capacitance, usually 20 or 32 picofarads.

TABLE I. Typical Crystal Parameters

Parameter	32 kHz fundamental	200 kHz fundamental	2 MHz fundamental	30 MHz overtone
R_1	200 kΩ	2 kΩ	100 Ω	20 Ω
L_1	7000H	27H	529 mH	11 mH
C_1	.003 pF	0.024 pF	0.012 pF	0.0026 pF
C_0	1.7 pF	9 pF	4 pF	6 pF
Q	100k	18k	54k	100k

The Pierce oscillator is one of the more popular circuits, and is the foundation for almost all single gate oscillators in use today. In this circuit, *Figure 2*, the signal from the input to the output of the amplifier is phase shifted 180 degrees. The crystal appears as a large inductor since it is operating in the parallel mode, and in conjunction with C_A and C_B, forms a pi network that provides an additional 180 degrees of phase shift from output to the input. C_A in series with C_B



TL/F/5347–3

FIGURE 2. Pierce Oscillator

plus any additional stray capacitance form the load capacitance for the crystal. In this circuit, C_A is usually made about the same value as C_B, and the total value of both capacitors in series is the load capacitance of the crystal which is generally chosen to be 32 pF, making the value of each capacitor 64 pF. The approximation equations of the load impedance, Z_1, presented to the output of the crystal oscillator's amplifier by the crystal network is:

$$Z_L = \frac{X_C^2}{R_L}$$

Where $X_C = -j/\omega C_B$ and R_L is the series resistance of the crystal as shown in Table I. Also $\omega = 2\pi f$ where f is the frequency of oscillation.

The ratio of the crystal network's input voltage to it's output voltage is given by:

$$\frac{e_A}{e_B} = \frac{\omega C_B}{\omega C_A} = \frac{C_B}{C_A}$$

C_A and C_B are chosen such that their series combination capacitance equals the load capacitance specified by the manufacturer, ie 20 pF or 32 pF as mentioned. In order to oscillate the phase shift at the desired frequency around the oscillator loop must be 360° and the gain of the oscillator loop must be greater or equal to one, or:

$$(A_A)(A_F) \geq 1$$

Where A_A is amplifier gain and A_F is crystal network voltage gain of the crystal π network: e_A/e_B. Thus not only should the series combination of C_B and C_A be chosen. The ratio of the two can be set to adjust the loop gain of the oscillator.

For example if a 2 MHz oscillator is required. Then $R_L = 100\Omega$ (Table I). If $e_A/e_B = 1$ and the crystal requires a 32 pF load so $C_B = 64$ pF and then C_A becomes 64 pF also. The load presented by the crystal network is $Z_L = (1/2\pi\ (2\ \text{MHz})\ (64\ \text{pF})^2)/100 = 16\ \text{k}\Omega$.

The CMOS Gate Oscillator

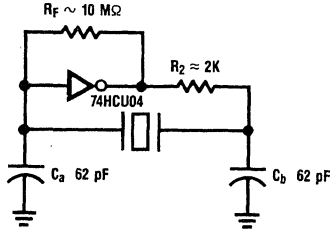
A CMOS gate sufficiently approaches the ideal amplifier shown above that it can be used in almost the same circuit. A review of manufacturers data sheets will reveal there are two types of inverting CMOS gates:

a) Unbuffered: gates composed of a single inverting stage. Voltage gain in the hundreds.

b) Buffered: gates composed of three inverting stages in series. Voltage gains are greater than ten thousand.

CMOS gates must be designed to drive relatively large loads and must supply a fairly large amount of current. In a single gate structure that is biased in its linear region so both devices are on, supply current will be high. Buffered gates are designed with the first and second gates to be much smaller than the output gate and will dissipate little power. Since the gain is so high, even a small signal will drive the output high or low and little power is dissipated. In this manner, unbuffered gates will dissipate more power than buffered gates.

Both buffered and unbuffered gates maybe used as crystal oscillators, with only slight design changes in the circuits.



TL/F/5347–4

FIGURE 3. Typical Gate Oscillator

In this circuit, R_F serves to bias the gate in its linear region, insuring oscillation, while R_2 provides an impedance to add some additional phase shift in conjunction with C_B. It also serves to prevent spurious high frequency oscillations and isolates the output of the gate from the crystal network so a clean square wave can be obtained from the output of the gate. Its value is chosen to be roughly equal to the capacitive reactance of C_B at the frequency of oscillation, or the value of load impedance Z_L calculated above. In this case, there will be a two to one loss in voltage from the output of the gate to the input of the crystal network due to the voltage divider effect of R_2 and Z_L. If C_A and C_B are chosen equal, the voltage at the input to the gate will be the same as that at the input to the crystal network or one half of the voltage at the output of the gate. In this case, the gate must have a voltage gain of 2 or greater to oscillate. Except at very high frequencies, all CMOS gates have voltage gains well in excess of 10 and satisfactory operation should result.

Theory and experiment show that unbuffered gates are more stable as oscillators by as much as 5 to 1. However, unbuffered gates draw more operating power if used in the same circuit as a buffered gate. Power consumption can be minimized by increasing feedback which forces the gate to operate for less time in its linear region.

When designing with buffered gates, the value of R_2 or C_B may be increased by a factor of 10 or more. This will increase the voltage loss around the feedback loop which is desirable since the gain of the gate is considerably higher than that of an unbuffered gate.

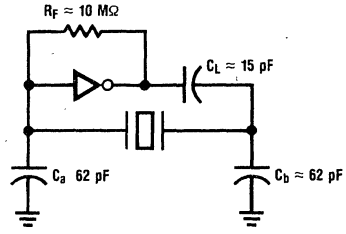
C_A and C_B form the load capacitance for the crystal. Many crystals are cut for either 20 to 32 picofarad load capacitance. This is the capacitance that will cause the crystal to oscillate at its nominal frequency. Varying this capacitance will vary the frequency of oscillation. Generally designers work with crystal manufacturers to select the best value of load capacitance for their application, unless an off the shelf crystal is selected.

High Frequency Effects

The phase shift thru the gate may be estimated by considering it's delay time:

Phase Shift = Frequency X Time delay X 360°

The "typical gate oscillator" works well at lower frequencies where phase shift thru the gate is not excessive. However, above 4 MHz, where 10 nsec of time delay represents 14.4° of excess phase shift, R_2 should be changed to a small capacitor to avoid the additional phase shift of R_2. The value of this capacitor is approximately $1/\omega C$ where $\omega = 2\pi f$, but not less than about 20 pF.

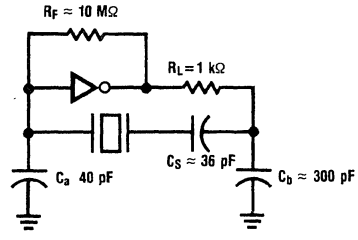


TL/F/5347–5

FIGURE 4. Gate Oscillator for Higher Frequencies

Improving Oscillator Stability

The CMOS gate makes a mediocre oscillator when compared to a transistor or FET: It draws more power and is generally less stable. However, extra gates are often available and are often pressed into service as oscillators. If improved stability is required, especially from buffered gate oscillators, an approach shown in *Figure 5* can be used.



TL/F/5347–6

FIGURE 5. Gate oscillator with improved stability

In this circuit, C_A and C_B are made large to swamp out the effects of temperature and supply voltage change on the gate input and output impedances. A small capacitor in series with the crystal acts as the crystal load and further isolates the crystal from the rest of the circuit.

Overtone Crystal Oscillators

At frequencies above 20 MHz, it becomes increasingly difficult to cut or work with crystal blanks and so generally a crystal is used in it's overtone mode. Also, fundamental mode crystals above this frequency have less stability and greater aging rates. All crystals will exhibit the same reactance vs. frequency characteristics at odd overtone frequencies that they do at the fundamental frequency. However, the overtone resonances are not exact multiples of the fundamental, so an overtone crystal must be specified as such.

In the design of an overtone crystal oscillator, it is very important to suppress the fundamental mode, or the circuit will try to oscillate there, or worse, at both the fundamental and the overtone with little predictability as to which. Basically, this requires that the crystal feedback network have more gain at the overtone frequency than the fundamental. This is usually done with a frequency selective network such as a tuned circuit.

The circuit in *Figure 6* operates in the parallel mode just as the Pierce oscillator above. The resonant circuit L_A—C_B is an effective short at the fundamental frequency, and is tuned somewhat below the deferred crystal overtone frequency. Also, C_L is chosen to suppress operation in the fundamental mode.

The coil L_A may be tuned to produce maximum output and will affect the oscillation frequency slightly. The crystal should be specified so that proper frequency is obtained at maximum output level from the gate.

Some Practical Design Tips

In the above circuits, some generalizations can be made regarding the selection of component values.

R_F: Sets the bias point, should be as large as practical.

R1: Isolates the crystal network from the gate output and provides excess phaseshift decreasing the probability of spurious oscillation at high frequencies. Value should be approximately equal to input impedance of the crystal network or reactance of C_B at the oscillator frequency. Increasing value will decrease the amount of feedback and improve stability.

C_B: Part of load for crystal network. Often chosen to be twice the value of the crystal load capacitance. Increasing value will increase feedback.

C_A: Part of crystal load network. Often chosen to be twice the value of the crystal load capacitance. Increasing value will increase feedback.

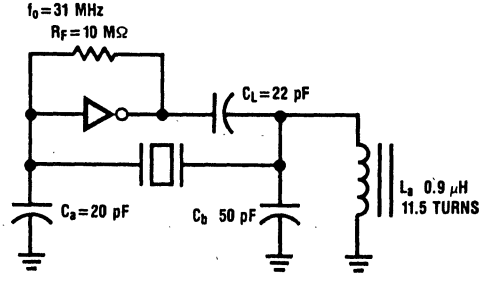
C_L: Used in place of R1 in high frequency applications. Reactance should be approximately equal to crystal network input impedance.

Oscillator design is an imperfect art at best. Combinations of theoretical and experimental design techniques should be used.

A. Do not design for an excessive amount of gain around the feedback loop. Excessive gain will lead to instability and may result in the oscillator not being crystal controlled.

B. Be sure to worst case the design. A resistor may be added in series with the crystal to simulate worst case crystals. The circuit should not oscillate on any frequency with the crystal out of the circuit.

C. A quick check of oscillator peformance is to measure the frequency stability with supply voltage variations. For HCMOS gates, a change of supply voltage from 2.5 to 6 volts should result in less than 10 PPM change in frequency. Circuit value changes should be evaluated for improvements in stability.



TL/F/5347–7

FIGURE 6. Parallel Mode Overtone Circuit

MM74HC942 and MM74HC943 Design Guide

National Semiconductor
Application Note 347
Peter Single
Steve Munich
April 1984

SECTIONS

2

1) TIMING AND CONTROL

a) Input and Output Thresholds

The MM74HC942/943 may be used in a CMOS or TTL environment. In a CMOS environment, no interfacing is required. If the MM74HC942/943 is interfaced to NMOS or bipolar logic circuits, standard interface techniques may be used. These are discussed in detail in National Semiconductor Application Note AN-314. This note is included in the National Semiconductor MM54HC/74HC High Speed microCMOS Logic Family Databook.

b) Logic States and Control Pin Function

Transmitted Data

TXD (pin 11) in conjunction with O/A selects the frequency of the transmitted tone and thus controls the transmitted data.

TXD = V_{CC} selects a "mark" and thus the high tone of the tone pair. This is discussed further in the following section.

Originate and Answer Mode

This is controlled by O/A (pin 13). O/A = V_{CC} selects originate mode. O/A = GND selects answer mode. These modes refer to the tone allocation used by the modem. When two modems are communicating with each other one will be in originate mode and one will be in answer mode. This assures that each modem is receiving the tone pair that the other modem is transmitting. The modem on the phone that originated the phone call is called the originate modem. The other modem is the answer modem.

The other pin controlling the transmitted tone is TXD (pin 11).

Bell 103 Tone Allocation

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070 Hz	2025 Hz	2025 Hz	1070 Hz
Mark	1270 Hz	2225 Hz	2225 Hz	1270 Hz

Squelch Transmitter

Transmitter squelch is achieved by putting SQT = V_{CC} (SQT is pin 14). The line driver remains active in this state (assuming ALB = GND).

This state is commonly used during the protocol of establishing a call. The originate user initiates a phone call with its transmitter squelched, and waits for a tone to be received before beginning transmission. During the wait time, the modem is active to allow tone detection, but no tone may be transmitted.

The state SQT = V_{CC} may also be used if the line driver is required but a signal other than modem tones (e.g., DTMF tones or voice) is to be transmitted. This is discussed further in Transmission of Externally Generated Tones (section 3d).

Analog Loop Back

ALB = V_{CC}, SQT = GND selects the state "analog loop back". (The state ALB = SQT = V_{CC} is discussed in the following section.)

In analog loop back mode, the modulator output (at the line driver) is connected to the demodulator input (at the hybrid), and the demodulator is tuned to the transmitted frequency tone set. Thus the data on the TXD pin will, after some delay, appear at the RXD pin. This provides a simple "self test" of the modem.

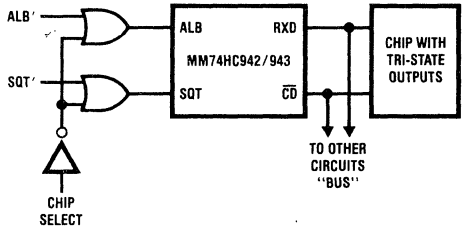
The signal applied to the demodulator during analog loop back is sufficient to cause the carrier detect output CD to go low indicating receipt of carrier.

In analog loop back mode, the modulator and transmitter are active, so the transmitted tone is not squelched.

Power-Down Mode

The state SQT = ALB = V_{CC} puts the MM74HC942/943 in power-down mode. In this state, the entire circuit except the oscillator is disabled. (The oscillator is left running in case it is required for a system clock). In power-down mode the supply current falls from 8 mA (typ) to 180 μA (typ), and all outputs, both analog and digital, TRI-STATE (become Hi-Z).

Using TRI-STATE Capability



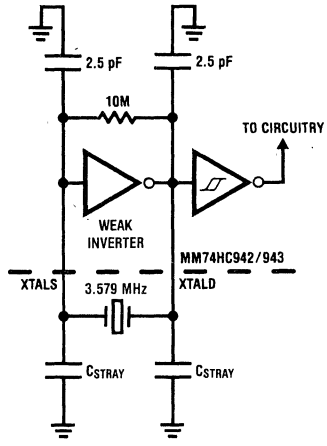
TL/F/5531-1

The ability of the outputs to TRI-STATE allows the modem to be connected to other circuitry in a bus-like configuration with the state SQT or ALB = GND being the modem chip select.

c) The Oscillator

The oscillator is a Pierce crystal oscillator. The crystal used in such an oscillator is a parallel resonant crystal.

The Oscillator



TL/F/5531-2

The capacitors used on each end of the crystal are a combination of on-chip and stray capacitances. This generally means the crystal is operating with less than the specified parallel capacitance. This causes the oscillator to run faster than the frequency of the crystal. This is not a problem as the frequency shift is small (approximately 0.1%).

The oscillator is designed to run with equal capacitive loading on each side of the crystal. This should be taken into consideration when designing PC layouts. This need not be exact.

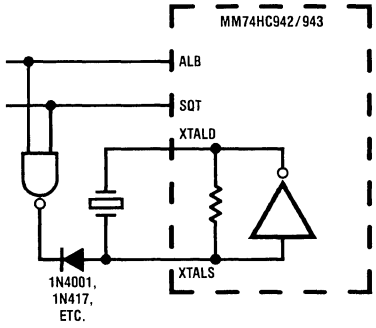
If a 3.58 MHz oscillator is available, the XTALD pin may be driven. The internal inverter driving this pin is very weak and can be overpowered by any CMOS gate output.

The Oscillator and Power-Down Mode

When the chip powers down, all circuits except the oscillator are switched off. The oscillator is left running so it may be used as a clock to drive other circuits within the system.

It is possible to shut the oscillator down by clamping the XTALS pin to V_{CC} or GND. This will cause the total chip current to fall to less than 5 μA. This may be useful in battery powered systems where minimizing supply current is important.

Powering Down the Oscillator



TL/F/5531-3

2) MODULATOR SECTION

a) Operation

The modulator receives data from the transmit data (TXD) pin and synthesizes a frequency shift keyed, phase coherent sine wave to be transmitted by the line driver through the transmit analog (TXA) pin. Four different sine wave frequencies are generated, depending on whether the modem is set to the orginate or answer mode and whether the data input to TXD is a logical high or low. See Timing and Control (section 1) for more information.

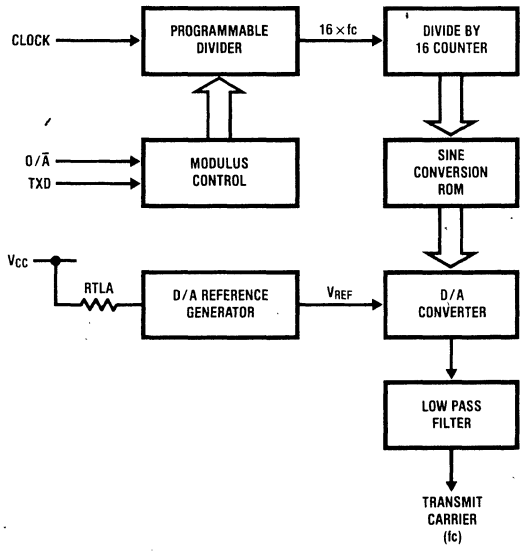
The TXD and O/A pins set the divisor of a dual modulus programmable divider. This produces a clock frequency which is sixteen times the frequency of the carrier to be transmitted. The clock signal is then fed to a four bit counter whose outputs go to the sine ROM. The ROM acts like a four-to-sixteen decoder that selects the appropriate tap on the D/A converter to synthesize a staircase-approximated sine wave. A switched capacitor filter and a low pass filter smooth the sine wave, removing high frequency components and insuring that noise levels are below FCC regulations.

b) Transmit Level Adjustment

The maximum transmit level of the MM74HC943 is −9 dBm. Since most phone lines attenuate the signal by 3 dB, the maximum level that will be received at the exchange is −12 dBm. This level is also the maximum allowed by most phone companies. The MM74HC942 has a maximum transmit level of 0 dBm, making possible adjustments for line losses up to −12 dB. The resistor values required to adjust the transmit level for both the MM74HC942 and the MM74HC943 follow the Universal Service Order Code and can be found in the data sheets. This resistor added between the TLA pin and V_{CC} serves to control the voltage reference at the top of the D/A ladder, adjusting output levels accordingly.

Note that for transmission above −9 dBm the required resistor must be chosen with the co-operation of the relevant phone company. This resistor is usually wired into the phone jack at the installation as the resistor value is specific to the particular phone line. This is called the Universal Registered Jack Arrangement. This arrangement is possible only with the MM74HC942 because of the dynamic range constraints of the MM74HC943.

The Modulator



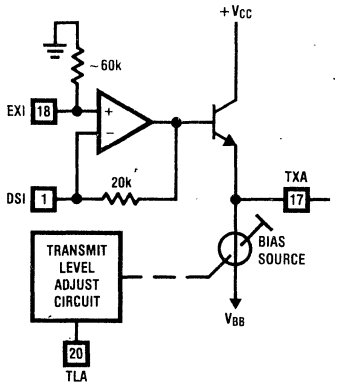
TL/F/5531-4

3) THE LINE DRIVER

a) Operation

The line driver is a class A power amplifier for transmitting the carrier signals from the modulator. It can also be used to transmit externally generated tones such as DTMF signals, as discussed in section 3d. When used for transmitting modem-produced tones, the external input (EXI) pin should be grounded to pin 19 for both the MM74HC942 and the MM74HC943. The line driver output is the transmit analog (TXA) pin.

The Line Driver Equivalent Schematic



TL/F/5531 5

b) Second Harmonic Distortion

If the modem is operating in the originate mode, the line driver output has frequencies of 1070 Hz for a space and 1270 Hz for mark. The second harmonic for a space frequency is at 2140 Hz, and this falls in the originate modem's receive frequency band from 2025 Hz to 2225 Hz. While the modulator produces very little second harmonic energy, the amplifier has been designed not to degrade the analog output any further. The result is that the second harmonic is below −56 dBm. Thus it is well below the minimum carrier amplitude recognized by the demodulator.

c) Dynamic Range

The decision to use the MM74HC942 or the MM74HC943 is a tradeoff between output dynamic range and power supply constraints. The power supply is discussed in another section. The MM74HC942 will transmit at 0 dBm while the maximum transmit level of the MM74HC943 is −9 dBm. This level applies to externally generated tones as well as the standard modem tone set.

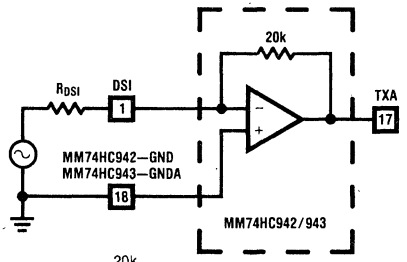
It is important to realize that the signal levels referred to above, and in the data sheet's specifications, are the levels referred to a 600Ω load resistor (representing the phone line) when driven from the external 600Ω source resistor. Also, the transmit levels discussed previously are maximum values. Typical values are 1 dB to 2 dB below these.

d) Transmission of Externally Generated Tones

Since a phone line connection is usually made on the TXA pin, it may be useful to use the line driver to transmit DTMF, voice or other externally generated tones. Both the inverting and non-inverting inputs to the line driver are available for this purpose. A DTMF tone generator with a TRI-STATE output may instead be directly connected to the same node as the TXA pin rather than the line driver. The choice of which method to use depends on whether the MM74HC942 or MM74HC943 is being used and the signal level of the transmission. Most phone companies allow DTMF tone generation at 0 dBm. This level is the maximum that the MM74HC942 can produce and is beyond the range of the MM74HC943.

If the line driver is to be used for external tone generation, the modem must be powered up and the transmission must be squelched by the SQT pin being held high. This will disable the output of the modulator section. The choice between the EXI pin and DSI pin is up to the user. The EXI pin gives a fixed gain of about 2. The DSI input allows for adjustable gain as a series resistor is necessary.

Using the DSI Input

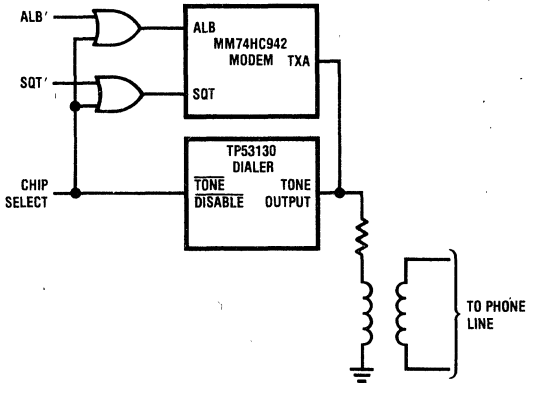


$$\text{Gain } A_V = \frac{20k}{R_{DSI}}$$

TL/F/5531-6

A better solution may be to use the power-down mode of the MM74HC942/943 with a DTMF tone generator that has a TRI-STATE output. Such a device is a TP53130 and is shown in the diagram following. When the tone generator is not in use and the modem is not squelched, the DTMF generator's output is in TRI-STATE. Rather than using the line driver, the tone generator's output is instead connected to the same node as the TXA pin. The tone generator is active when the modem is in power-down. Power-down TRI-STATEs the TXA output.

Interfacing to DTMF Generator Using TRI-STATE Feature



TL/F/5531-7

4) THE HYBRID

The MM74HC942/943 has an on-chip hybrid. (A hybrid in this context refers to a circuit which performs two-to-four wire conversion.)

Under ideal conditions the phone line and isolation network have an equivalent input impedance of 600Ω. Under these conditions the gain from the transmitter to the op amp output is zero, while the gain from the phone line to the op amp output is unity. Thus the hybrid, by subtracting the transmitted signal from the total signal on the phone line, has removed the transmitted component.

Unfortunately, these ideal conditions rarely exist and filtering is used to remove the remaining transmitted signal component. This is discussed further in the next section.

Note that the signals into the hybrid must be referred to GND in the MM74HC942 and GNDA in the case of the MM74HC943. Thus blocking capacitors are required in the latter case. This is discussed further in DC Levels and Analog Interface (section 9a).

5) THE RECEIVE FILTER

The signal from the hybrid is a mixture of transmitted and received signals. The receive filter removes the transmitted signals so only received signal goes to the discriminator.

The receive filter may be characterized by driving RXA1 or RXA2 with a signal generator. The filter response may then be observed at the FTLC pin with the capacitor removed. In this state the output impedance of the FTLC pin is 16 kΩ nominal.

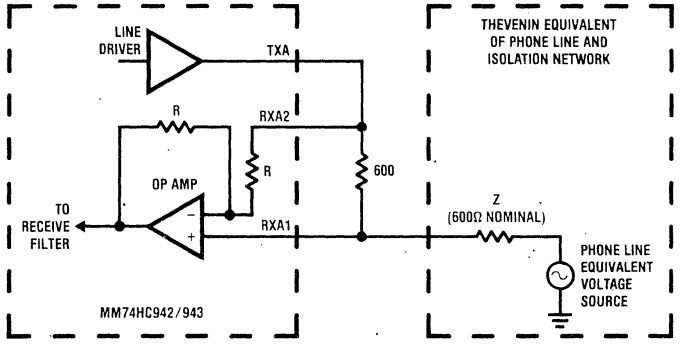
6) THE FTLC PIN

The FTLC pin is at the point of the circuit where the receive filter output goes to the hard limiter input and the carrier detect circuit input.

The signal at the output of the receive filter may be as low as 7 mVrms. It is thus important that the wiring to the FTLC pin and the associated circuit be clean. Ideally the track from the capacitor to pin 19 (GND on the MM74HC942, GNDA on the MM74HC943) should be shared by no other devices.

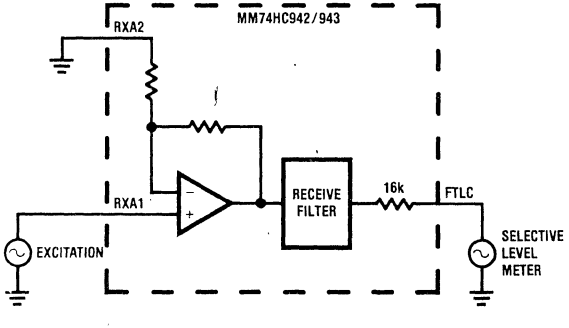
If these precautions are not observed, circuit performance may be unnecessarily degraded.

The Hybrid



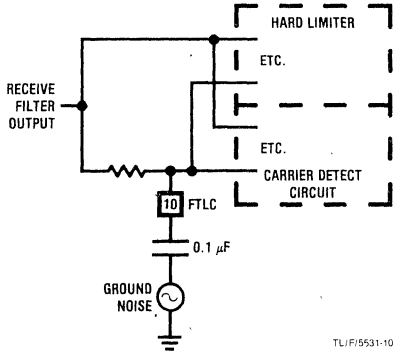
TL/F/5531-8

Characterizing the Receive Filter



TL/F/5531-9

The FTLC Pin and Associated Circuitry



TL/F/5531-10

7) THE CARRIER DETECT CIRCUIT

a) Operation

The carrier detect circuit senses if there is carrier present on the line. If carrier is not present, the data output is clamped high.

The RC circuit filters the DC from the output of the receive filter. The comparator inputs are thus the filter output, and the DC level of the receive filter minus the controlled offset. The controlled offset sets the amount that the AC signal must exceed the DC level (and thus the AC amplitude) before the comparator switches. When this happens, the comparator output sets a resettable one-shot which converts the periodic comparator output to a continuous signal. This signal then controls the time delay set by the CDT pin. After the preset time delay the CD bar output goes low. This shifts the comparator offset providing hysteresis to the overall circuit.

b) Threshold Control

The carrier detect threshold may be adjusted by adjusting the voltage on the CDA pin.

The carrier detect trip points are nominally set at −43 dBm and −46 dBm. The CDA pin sits at a nominal 1.2V. The carrier detect trip points are directly proportional to the voltage on this pin, so doubling the voltage causes a 6 dB increase in the carrier detect trip points. Similarly, halving the voltage causes a 6 dB decrease in carrier detect trip points.

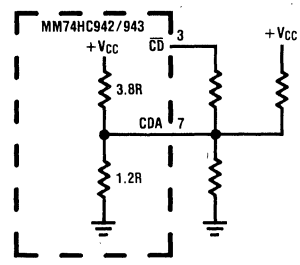
Note that as the carrier detect trip point is reduced, the system noise will approach the carrier level, and the accuracy and predictability of the carrier detect trip points will decrease.

The output impedance of the CDA pin his high. It is constant (±10%) from die to die but has a very high temperature coefficient. It is thus advisable, if the CDA pin is driven, to drive from a low source impedance.

Because the output impedance of the CDA pin is high, capacitive coupling from the adjacent XTALD pin can present a problem. For this reason a 0.1 μF capacitor is usually connected from the CDA pin to ground. If the CDA pin is driven from a low impedance source, this capacitor may be omitted.

If a resistor is connected from the CD bar pin to the CDA pin, the CDA voltage will vary depending on whether carrier is detected. This will effectively increase the carrier detect hysteresis.

Increased Carrier Detect Hysteresis



TL/F/5531-12

Similarly an inverter and a resistor from the CD bar pin to the CDA pin will reduce the hysteresis. This is not recommended as the 3 dB nominal figure chosen is close to the minimum value useable for stable operation.

c) Timing Conrol

The capacitor on the CDT pin adjusts the amount of time that carrier must be present before the carrier is recognized as valid.

This circuit is designed for a long off-to-on time compared to the on-to-off time. This means carrier must be present and stable to be acknowledged, and that if carrier is marginal it will be rejected quickly.

The equations for the capacitor value are

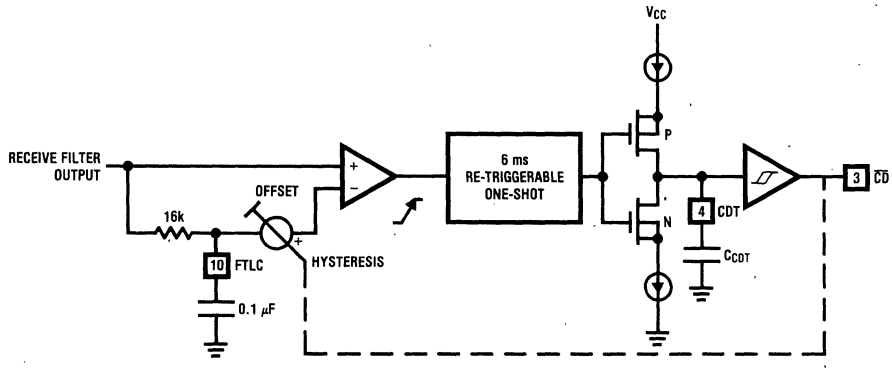
$$T_{on\text{-}to\text{-}off} = C * 0.54 \text{ seconds}$$

and

$$T_{off\text{-}to\text{-}on} = C * 6.4 \text{ seconds.}$$

The ratio of on-to-off and off-to-on times may be adjusted over a narrow range by the addition of pull-up or pull-down resistors on the CDT pin.

Carrier Detect Block Diagram

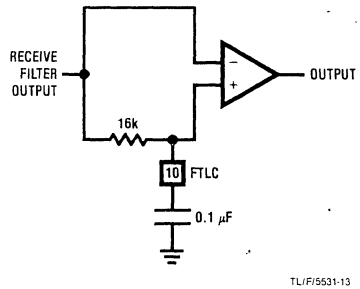


TL/F/5531-11

The repeatability of the times is high from die to die at fixed temperature, but is strongly temperature dependent. The times will shift by approximately ±30% over process and temperature.

8) THE DISCRIMINATOR

a) The Hard Limiter



The signal to the inverting input of the comparator has the same DC component as the signal to the non-inverting input. The differential input to the comparator is thus the AC component of the filter output. The comparator has very low input offset and so the limiter will operate with very low input signal levels.

The demodulator employed requires an input signal having equal amplitude for a mark and a space. It also requires a high level signal. The hard limiter converts all signals to a square wave. All amplitude information is lost but frequency information is retained.

By removing the capacitor from the FTLC pin, the hard limiter ceases to operate, but the filter output may be observed. This is useful for circuit evaluation and testing.

b) Discriminator Operation

The discriminator separates the incoming energy into mark and space energy. This occurs in the band pass filters which are tuned to the mark and space frequencies. The outputs of the mark and space band pass filters are rectified to extract the output amplitudes. The rectifier outputs are filtered to remove ripple. The low pass filter outputs are compared to determine if the mark or space path is receiving greater energy, and thus if the incoming data is a mark or a space.

The output of the discriminator is only valid if carrier is being received. If carrier is not being received (as determined in the carrier detect circuit) the RXD output is clamped high. This stops the discriminator from attempting to demodulate a signal which is too low for reliable operation.

9) POWER SUPPLIES

a) DC Levels and Analog Interface

The MM74HC942 refers all analog inputs and outputs to GND (pin 19). The analog interface thus requires no DC blocking capacitors.

The MM74HC943 refers all analog inputs and outputs to GNDA (pin 19) which requires a nominal 2.5V supply. The current requirements of GNDA are low, so the GNDA supply may be derived with a simple resistive divider. The GNDA supply can then be referenced to GND using capacitors. This GNDA supply will have poor load regulation so the high current interface must be connected to GND and a DC blocking capacitor used.

As the FTLC capacitor is connected to the input of the hard limiter, any noise on the FTLC ground return will couple directly into this circuit. The signal on FTLC may be only millivolts, so it is important that the FTLC capacitor ground be at the same potential as the chip's ground reference. Thus when using the MM74HC943 the FTLC capacitor ground return should go directly to GNDA (pin 19). For both the MM74HC942 and MM74HC943 this ground return should be shared by no other circuits. Failure to observe this precaution could result in unnecessary reduction of dynamic range and carrier detect accuracy, and an increase in error rate.

b) Power Supply Noise

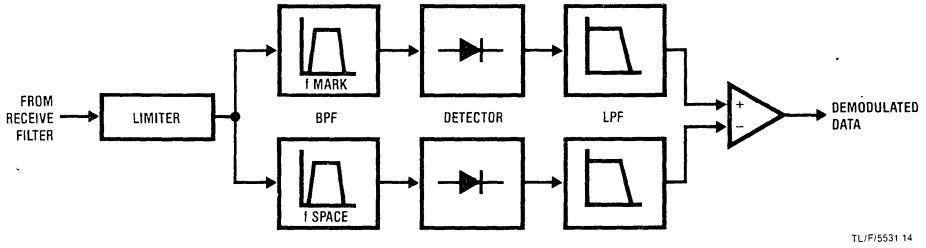
It is important that the power supplies to the MM74HC942/943 be stable supplies, having low noise, particularly in the frequency band from 50 kHz to 10 MHz.

The MM74HC942/943 use switched capacitor techniques extensively. A feature of switched capacitor circuits is their ability to translate noise from high frequency bands to low frequency bands. At the same time it is difficult to design op amps with high power supply rejection at high frequencies. (The MM74HC942/943 has 19 op amps internally.) As a result the high frequency PSSR of the MM74HC942/943 is not high, so high frequency noise on the power supply can degrade circuit operation.

This should not cause a problem if the circuits are powered from a three terminal regulator, and no other circuitry shares the regulator. Power supply noise could be a problem if:

a) One or both of the power supplies are switching regulator circuits. Switching regulators can produce a lot of supply noise.

b) The modem shares its supply with a large digital circuit. Digital circuits, particularly high speed CMOS (the HC family) can produce large spikes on the supplies. These spikes have wide spectral content.



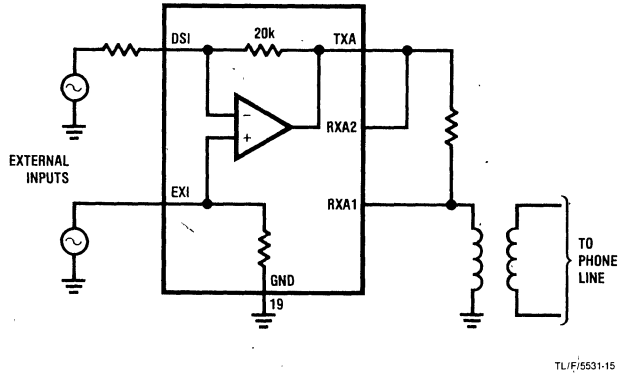
Ideally the modem could have its own supply. This may not be cost effective, so in some applications power supply filters may be necessary. These may just be RC filters but LC filters may be necessary depending on the extent of the supply noise. Miniature inductors in half watt resistor packages are cheap, lend themselves to automatic insertion, and are ideal for these filters.

It is difficult to set specifications for a "clean" supply because spectral density considerations are important. The following guidelines should be taken as "rule of thumb":

a) From 50 kHz to 20 MHz the ripple should not exceed −60 dBV.

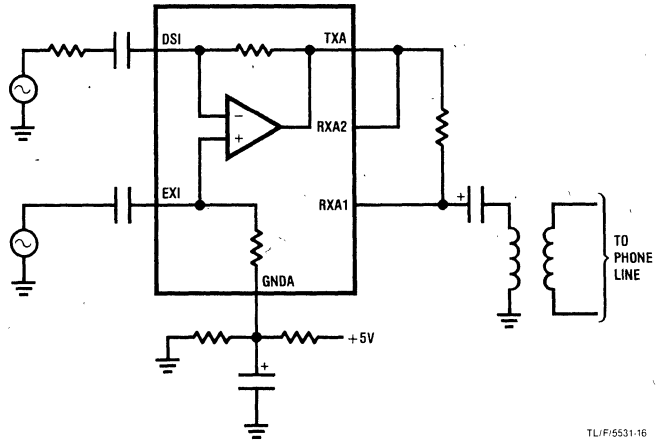
b) From DC to 50 kHz the ripple should not exceed −50 dBV.

MM74HC942 Analog Interface



TL/F/5531-15

MM74HC943 Analog Interface



TL/F/5531-16

CMOS 300 Baud Modem

National Semiconductor
Application Note 349
Anthony Chan
Peter Single
Daniel Deschene
April 1984

INTRODUCTION

The advent of low cost microprocessor based systems has created a strong demand for low cost, reliable means of data communication via the dial-up telephone network. The most widespread means for this task is the Bell 103 type modem, which has become the de facto standard of low speed modems. This type of modem uses frequency shift keying (FSK) to modulate binary data asynchronously at speeds up to 300 baud.

The success of this type of modem, despite its modest transmission speed, is largely due to its ability to provide full duplex data transmission at low error rates even with unconditioned telephone lines. It also has a significant cost advantage over the other types of modems available today. Advances in CMOS and circuit design technology have made possible the MM74HC942—a high performance, low power, Bell 103 compatible single chip modem. This chip combines both digital and linear circuitry to bring the benefits of system level integration to modem and system designers.

THE PROCESS—microCMOS

The chip was designed with National's double poly CMOS (microCMOS) process used extensively for its line of PCM CODECs and filters. This is a self-aligned, silicon gate CMOS process with two layers of polysilicon, one of which is primarily used for gates of the MOS transistors. Thus there are three layers of interconnect available (two polysilicon and one metal layer) making possible a very dense layout.

The two polysilicon layers also offer a near perfect capacitor structure which is used to advantage in the linear portions of the chip. The self-aligned silicon gate P and N-chanel MOSFETs combine high gain with minimal parasitic gate-to-drain overlap capacitance, facilitating the design of operational amplifiers with high gain-bandwidth product and excellent dynamic range.

CHIP ARCHITECTURE

The chip architecture was arrived at after critically evaluating several trial system partitionings of the Bell 103 type data set. The overriding goal was to integrate as much of the function as possible without sacrificing versatility and cost effectiveness in new applications. The resulting chip architecture reflects this philosophy. Since the majority of users of this device would probably be digital designers unfamiliar with filter design and analog signal processing, inclusion of these functions was thus mandatory. The precision filters needed for a high performance modem also make discrete implementations expensive. On the other hand, the majority of new systems will typically include a microprocessor which is quite capable of handling the channel establishment protocol. Besides, different systems may require different protocols. Circuitry for this task was therefore omitted.

A block diagram illustrating the chip architecture is shown in *Figure 1*. The on-chip line driver and line hybrid greatly simplify interfacing to the phone line by saving two external op amps. The output of the line hybrid, which is used to reduce the effect of the local transmit signal on the received signal, goes to a programmable receive bandpass filter. This filter improves the signal-to-noise ratio at the input of the frequency discriminator, which performs the actual FSK demodulation. The output of the receive filter is also monitored by a carrier detector which compares the amplitude of the received signal to an externally adjustable threshold level.

The modulator consists of a frequency synthesizer which generates a clock at a frequency determined by the TXD (transmit data) and O/$\overline{A}$ (originate/answer) inputs. This is subsequently shaped by the sine converter into the final modulated transmit carrier signal.

All internal clocks and control signals are derived from an on-chip oscillator operating from a common 3.58 MHz TV crystal. On-chip control logic allows the modem to be set to answer or originate mode operation, or to an analog loop-back mode via the O/$\overline{A}$ and ALB inputs respectively. The line driver can be squelched via the SQT input, which typically occurs during the channel establishment sequence.

Another feature of this design not obvious from the block diagram of *Figure 1* is that the chip can be powered down by asserting the ALB and SQT inputs simultaneously, a condition that does not occur during normal operation. This cuts power consumption to typically under 50 μA, making it very suitable for battery operation.

DEMODULATOR

Receive Filter

This is a nine pole, switched capacitor[1, 2] bandpass filter. It is programmable by internal logic to one of two passbands, corresponding to originate or answer mode operation. The measured frequency response of the filter is shown in *Figure 2*. It shows that better than 60 dB of adjacent channel rejection has been achieved. Note also the deep notches at the frequencies of the locally transmitted tone pair.

Reprinted from Midcon/82

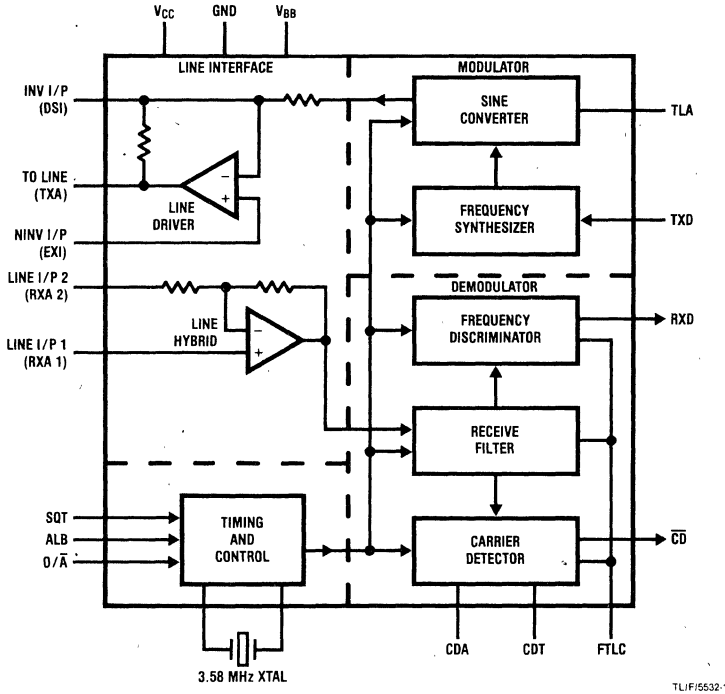


FIGURE 1. Chip Architecture of the MM74HC942

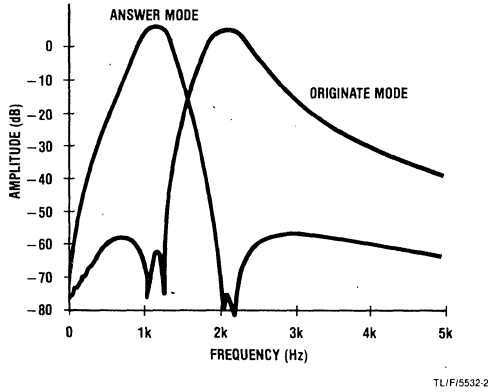


FIGURE 2. Measured Frequency Response of the Receive Filter

A key design goal was to minimize the delay distortion of the filter. This has also been met as evidenced by the delay response curves shown in *Figures 3a and 3b.* These curves have been normalized to the delays at 1170 Hz and 2125 Hz respectively. They show that the delay distortion in the 1020 Hz to 1320 Hz band is approximately 70 μs, while that in the 1975 Hz to 2275 Hz band is approximately 110 μs. These bands contain all the significant sidebands of a 300 baud FSK signal. The low delay distortion of the receive filter translates directly into low jitter in the demodulated data.

An on-chip, second order, real time anti-aliasing filter precedes the receive filter. This masks the sampled data nature of the switched capacitor design from the user, contributing to the ease of use of the chip.

Frequency Discriminator

Referring to *Figure 4*, the filtered receive carrier is first hard limited to remove any residual amplitude modulation. It is then split into two parallel, functionally identical paths, each consisting of a second order bandpass filter (BPF), a full wave detector and a post detection lowpass filter (LPF).

The bandpass filter in the upper path is tuned to the 'mark' frequency, and that in the lower path to the 'space' frequency. The detectors are full wave rectifier circuits which, together with the post detection filters, measure the energy in the mark and space frequencies. These are compared by the trailing comparator to decide whether a mark or space has been received.

Carrier Detector

The carrier detector compares the output of the receive filter against an externally adjustable threshold voltage. Referring back to *Figure 1*, if the CDA (carrier detect adjust) pin is left floating, the threshold is nominally set to ON at −44 dBm, and OFF at −47 dBm. This can be modified by forcing an external voltage at the CDA input. If the received carrier exceeds the set threshold, the $\overline{CD}$ (carrier detect) output will go low after a preset time delay. This delay is set externally by a timing capacitor connected to the CDT (carrier detect timing) pin.

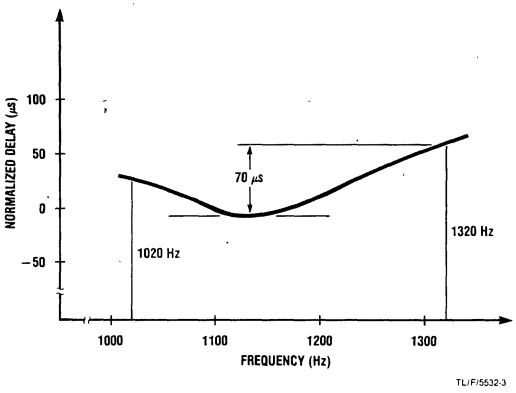


FIGURE 3a. Normalized Delay Response of the Receive Filter in Answer Mode

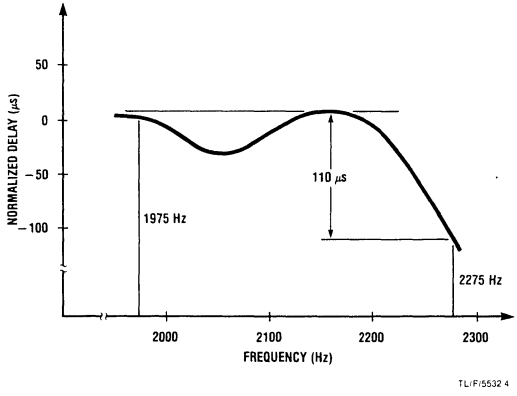


FIGURE 3b. Normalized Delay Response of the Receive Filter in Originate Mode

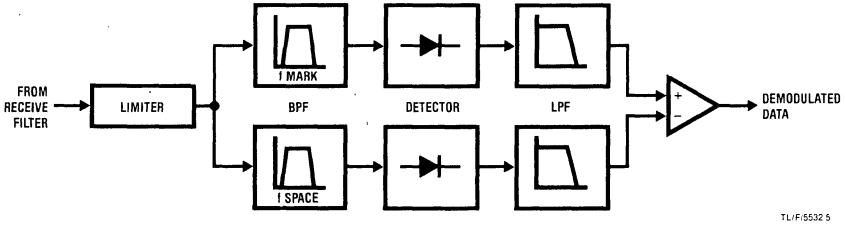


FIGURE 4. Block Diagram of the Frequency Discriminator

MODULATOR

As shown in *Figure 5*, the modulator consists of a frequency synthesizer and a sine wave converter. The transmit data (TXD) and mode (O/$\overline{A}$) inputs set the divisor of a dual modulus programmable divider. This produces a clock at sixteen times the frequency of the transmitted tone. This then clocks a four bit counter, whose states represent the voltage levels corresponding to the sixteen time slots in one cycle of a staircase approximated sine wave. The sine ROM decodes the state of the counter and drives a digital-to-analog converter to synthesize the frequency shift keyed sine wave. This modulator design also preserves phase coherence in the transmit carrier across frequency excursions.

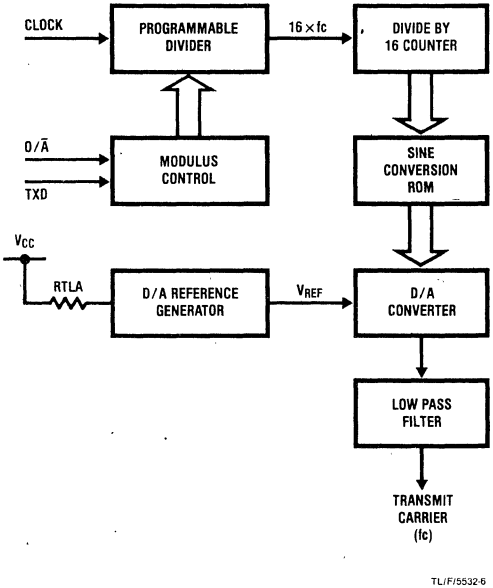


FIGURE 5. Modulator Block Diagram

The reference voltage for the digital-to-analog converter is derived from a reference generator controlled by an external resistor (RTLA). This allows the transmit signal level to be programmable in accordance with the Universal Service Order Code. This code specifies the programming resistances corresponding to various transmit levels. If no external resistor is connected, the transmit level defaults to −12 dBm.

The synthesized sine wave is filtered by a second order, real time lowpass filter to remove spurious harmonics before being fed to the line driver amplifier.

LINE INTERFACE

Line Driver

This is a class A power amplifier designed to drive a 600Ω line through an external 600Ω terminating resistor. With the proper transmit level programming resistor installed, it will drive the line at 0 dBm when operated from ±5V supplies. The quiescent current of the output stage of the driver varies with the programmed transmit level to maximize the efficiency of the amplifier. A class A design was chosen mainly because it can tolerate a wider range of reactive loads.

As shown in *Figure 6*, both inverting and non-inverting inputs of the driver amplifier are accessible externally, making it easy to accommodate an external signal source, such as a tone dialer. An external capacitor can also be connected between the inverting input and the amplifier output to give it a lowpass response.

Line Hybrid

The line hybrid is essentially a difference amplifier which, when connected as shown in *Figure 6*, causes the transmit carrier to appear as common-mode signal and be cancelled from the output. If the termination resistor (R_T) and phone line impedance are perfectly matched, the output of the line hybrid would be just the received carrier. In practice, perfect matching is impossible and 10 dB to 20 dB of transmit carrier rejection is more realistic. The residual is more than adequately rejected by the receive filter of the demodulator.

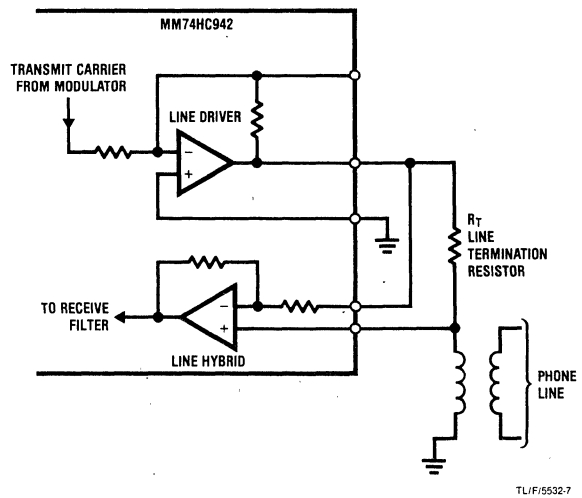


FIGURE 6. Typical Interface Between the MM74HC942 and the Phone Line

TIMING AND CONTROL

This includes an oscillator amplifier, divider chain and internal control logic. The oscillator, in conjunction with an external 3.58 MHz TV crystal and the divider chain, provides all the internal clocks for the switched capacitor circuits and the frequency synthesizer. The control logic orchestrates the various operating modes of the chip (e.g., originate, answer or analog loop-back modes).

APPLICATIONS

Figure 7 shows the MM74HC942 in an acoustically coupled modem application. It demonstrates the simplicity of the resulting design and a dramatic reduction in parts count. *Figure 8* shows two typical direct connect modem applications. The simplicity of these circuits is again evident.

The simple power supply requirement (±5V), low power (60 mW when transmitting at −9 dBm, 0.5 mW standby) and low external component count makes the MM74HC942 an efficient implementation of the 300 baud modem function.

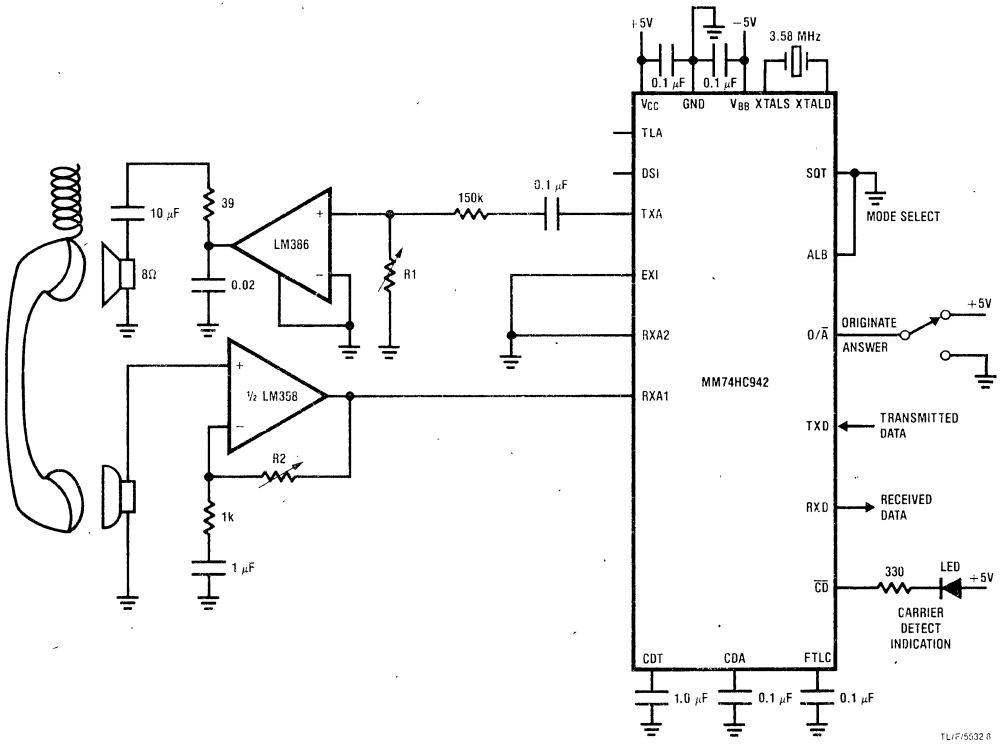


FIGURE 7. Typical Implementation of an Acoustically Coupled Modem Using the MM74HC942

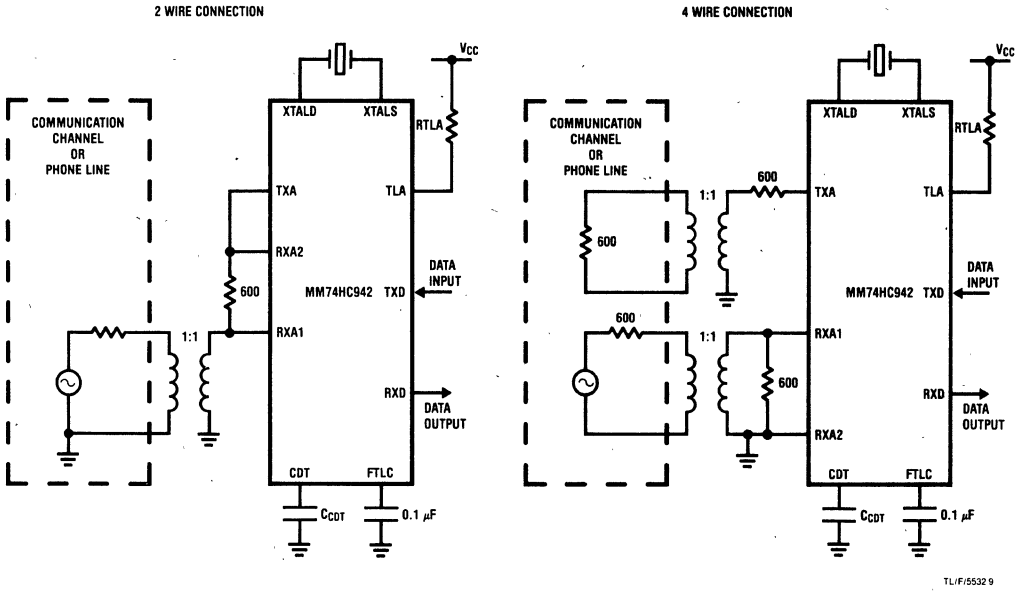


FIGURE 8. Typical Implementations of Direct Connect Modems Using the MM74HC942

SUMMARY

In conclusion, the MM74HC942 integrates the entire data path of a Bell 103 type data set into a 20-pin package with the following features:

- On-chip 9 pole receive filter
- Carrier detector with adjustable threshold
- Analog demodulator with low bit jitter and bias
- Phase coherent modulator with low spurious harmonics
- 600Ω line driver with adjustable transmit level
- On-chip line hybrid
- Full duplex originate or answer mode operation
- Low power operation, power-down mode
- Simple supply requirements (± 5V)

REFERENCES

1. J. Caves et al., *"Sampled Analog Filtering using Switched Capacitors as Resistor Equivalents"*, IEEE Journal of Solid State Circuits, Vol. SC-12, No. 6, Dec. 1977

2. W. Black et al., *"A High Performance Low Power CMOS Channel Filter"*, IEEE Journal of Solid State Circuits, Vol. SC-15, No. 6, Dec. 1980

Designing an LCD Dot Matrix Display Interface

National Semiconductor
Application Note 350
Bob Lutz
February 1984

The MM58201 is a CMOS LCD driver capable of driving a multiplexed display of up to 192 segments (24 segment columns by 8 backplanes). The number of backplanes being driven is programmable from one to eight. Data to be displayed is sent to the chip serially and stored in an internal RAM. An external resistor and capacitor control the frequency of the driving signals to the LCD. The MM58201 can also be programmed to accept the oscillator output and backplane signals of another MM58201 for cascading purposes. The displayed data may also be read serially from the on-chip RAM. A simplified functional block diagram of the MM58201 is shown in *Figure 1*.

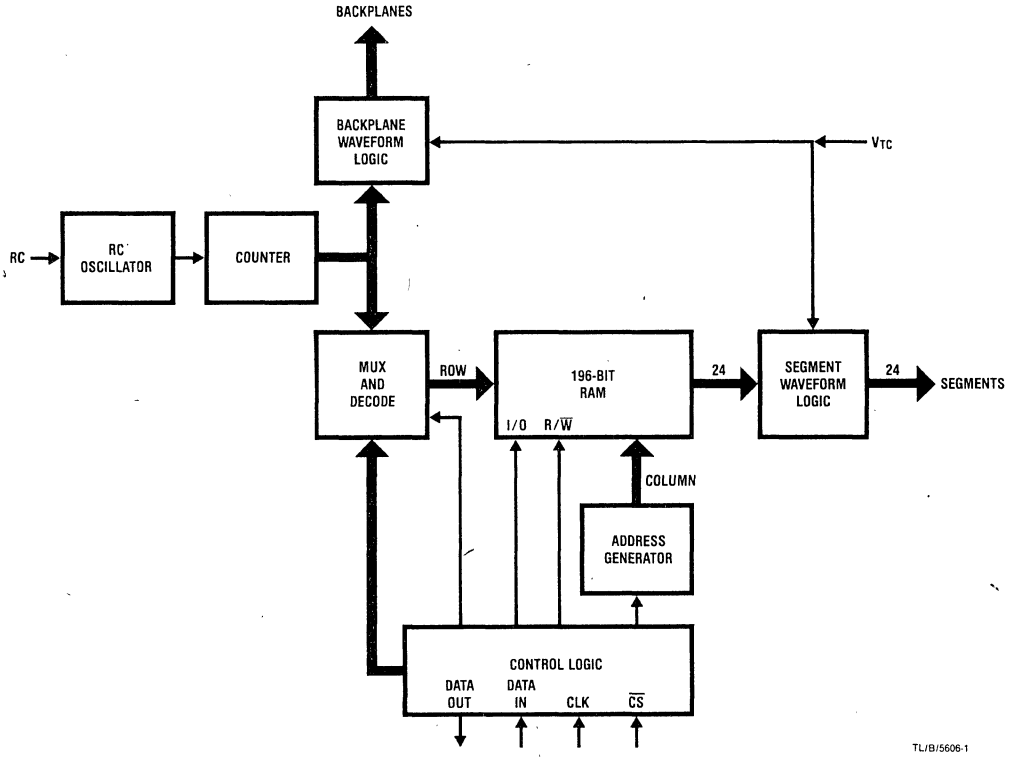


FIGURE 1. MM58201 Functional Diagram

BACKGROUND

LCD displays have become very popular because of their ultra-low power consumption and high contrast ratio under high ambient light levels. Typically an LCD has a backplane that overlaps the entire display area and multiple segment lines that each overlap just one segment or descriptor. This means that a separate external connection is needed for every segment or descriptor as shown in *Figure 2*. For a display with many segments such as a dot matrix display, the number of external connections could easily grow to be very large.

Unlike other display technologies that respond to peak or average voltage and current, LCDs are sensitive to the rms voltage between the backplane and given segment location. Also, any DC bias across this junction would cause an irreversible electrochemical action that would shorten the life of the display. A typical LCD driving signal is shown in *Figure 3*. The backplane signal is simply a symmetrical square wave. The individual segment outputs are also square waves, either in phase with the backplane for an "off" segment or out of phase for an "on" segment. This causes a Vrms of zero for an "off" segment and a Vrms of + V for an "on" segment.

One way to reduce the number of external connections is to multiplex the display. An example of this could be an LCD with its segments arranged as intersections of an X-Y grid. A driver to control a matrix like this would be fairly straightforward for an LED display. However, it is more complex for an LCD because of the DC bias restriction.

A multiplexed LCD driver must generate a complex set of output signals to insure that an "on" segment sees an rms voltage greater than the display's turn-on voltage and that an "off" segment sees an rms voltage less than the display's turn-off voltage. The driver must also insure that there is no DC bias.

One pattern that can accomplish this is shown as an example in *Figure 4*. This is the pattern that the MM58201 uses. The actual Vrms of an "on" segment and an "off" segment is shown in *Figure 5*. If there are eight backplanes, the Vrms (ON) = $0.2935 \times V_{TC}$ and the Vrms (OFF) = $0.2029 \times V_{TC}$. It can be seen in *Figure 6* that as the number of backplanes increases, the difference between Vrms (ON) and Vrms (OFF) becomes less. Refer to the specifications of the LCD to determine exactly what Vrms is required.

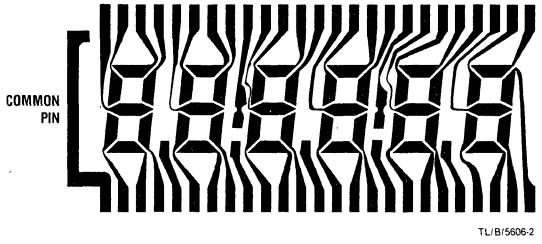


FIGURE 2. Typical LCD Pin Connections

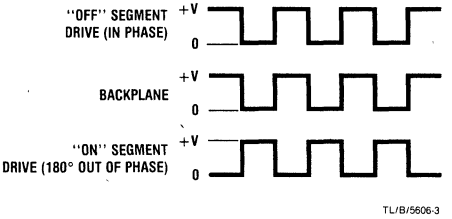


FIGURE 3. Drive Signals from a Direct Connect LCD Driver

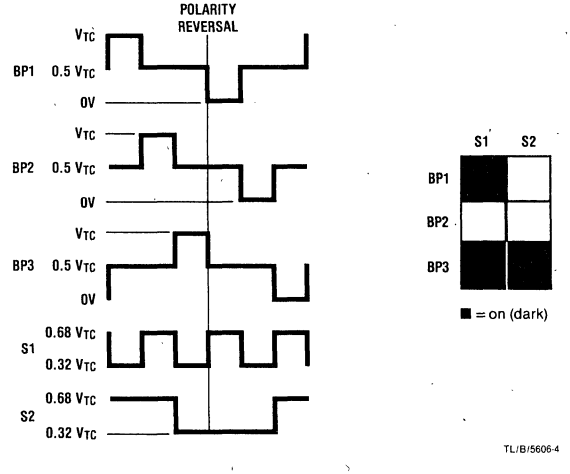
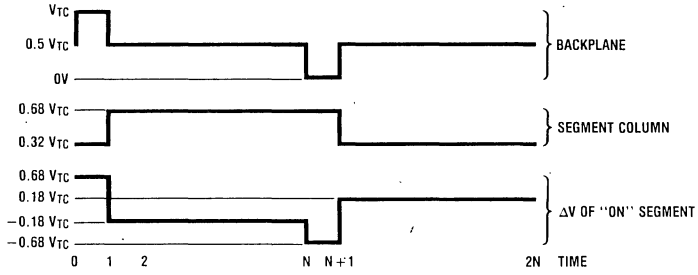


FIGURE 4. Example of Backplane and Segment Patterns



TL/B/5606 5

$$\text{Vrms (ON)} = \left(\frac{1}{T}\int_{t0}^{t0+T} V^2(t)dt\right)^{1/2}$$

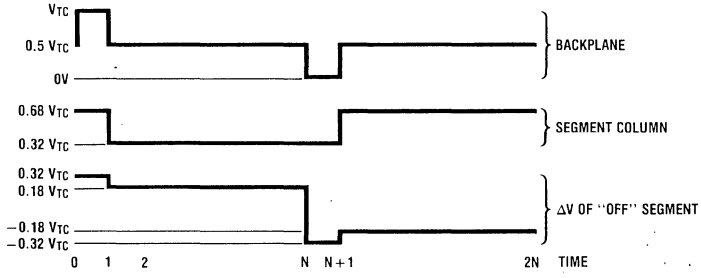
$$= \left(\frac{1}{N}\left[\int_0^1 (0.68\ V_{TC})^2 dt + \int_1^N (-0.18\ V_{TC})^2 dt\right]\right)^{1/2}$$

$$= \left(\frac{1}{N} V_{TC}^2 [0.4624 + 0.0324(N-1)]\right)^{1/2}$$

$$= V_{TC}\left[\frac{0.4624 + 0.0324(N-1)}{N}\right]^{1/2}$$

N = number of backplanes

a. Analysis of Vrms (ON)



TL/B/5606 6

$$\text{Vrms (OFF)} = \left(\frac{1}{T}\int_{t0}^{t0+T} V^2(t)dt\right)^{1/2}$$

$$= \left(\frac{1}{N}\left[\int_0^1 (0.32\ V_{TC})^2 dt + \int_1^N (-0.18\ V_{TC})^2 dt\right]\right)^{1/2}$$

$$= \left(\frac{1}{N} V_{TC}^2 [0.1024 + 0.0324(N-1)]\right)^{1/2}$$

$$= V_{TC}\left[\frac{0.1024 + 0.0324(N-1)}{N}\right]^{1/2}$$

N = number of backplanes

b. Analysis of Vrms (OFF)

$$V_{TC} = 1/2\left[\underbrace{\left(\frac{\text{Vrms (OFF)}}{\frac{0.1024 + 0.0324(N-1)}{N}}\right)}_{\text{must be greater than}} + \left(\frac{\text{Vrms (ON)}}{\frac{0.4624 + 0.0324(N-1)}{N}}\right)\right]$$

Example: If N = 8
and Vrms (OFF) = 1.8V
and Vrms (ON) = 2.2V
then V_{TC} = 7.5V

FIGURE 5

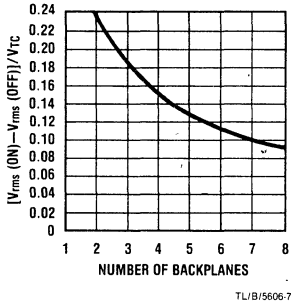


FIGURE 6. $\Delta Vrms/V_{TC}$

FUNCTIONAL DESCRIPTION

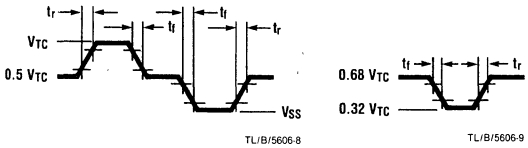
Connecting an MM58201 to an LCD

The backplane and segment outputs of the MM58201 connect directly to the backplane and segment lines of the LCD. These outputs are designed to drive a display with a total "on" capacitance of up to 2000 pF. This is especially important for the backplane outputs, as it is usually the backplanes that have the most capacitance. As the capacitance of the output lines increases, the DC offset between a backplane and segment signal may increase. Most LCD displays specify that a maximum offset of 50 mV is acceptable. For backplane capacitance under 2000 pF the MM58201 guarantees an offset of less than 10 mV.

If the LCD display to be used has 24 segments per backplane or less, then each MM58201 should be configured as a "master" so that each one will generate its own set of backplane signals. However, if the LCD display has more than 24 segments per backplane, more than one MM58201 will be needed for each backplane. To synchronize the driving signals there must be one "master" chip and then an additional "slave" chip for every 24 segments after the first 24. When a chip is configured as a "slave" it does not generate its own backplane signals. It simply synchronizes itself to the backplane signals generated by a "master" chip by sensing the BP1 signal. An example of both an all "master" configuration and a "master-slave" configuration will be shown later.

Voltage Control Pin and Circuitry

The voltage presented at the V_{TC} pin determines the actual voltage that is output on the backplane and segment lines. These voltages are shown in *Figure 7*. V_{TC} should be set with respect to Vrms (ON) and Vrms (OFF) and can be calculated as shown in *Figure 5*.



a. Backplane Output b. Segment Output

FIGURE 7. Output Voltages

Since the input impedance of V_{TC} may vary between 10 kΩ and 30 kΩ, the output impedance of the voltage reference at V_{TC} should be relatively low. One example of a V_{TC} driver is shown in *Figure 8*. To put the MM58201 in a standby mode, bring V_{TC} to V_{SS} (ground). This will blank out the display and reduce the supply current to less than 300 μA.

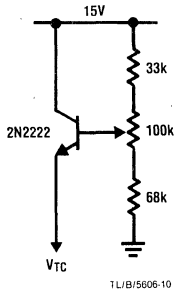


FIGURE 8. Example of V_{TC} Driver

RC Oscillator

This oscillator works with an external resistor tied to V_{DD} and an external capacitor tied to V_{SS}. The frequency of oscillation is related to the external R and C by:

$$f_{OSC} = 1/1.25\ RC \pm 30\%$$

The value of the external resistor should be in the range from 10 kΩ to 1 MΩ. The value of the external capacitor should be less than 0.005 μF.

The oscillator generates the timing required for multiplexing the LCD. The frequency of the oscillator is 4N times the refresh rate of the display, where N is the number of backplanes programmed. Since the refresh rate should be in the range from 32 Hz to 100 Hz, the oscillator frequency should be:

$$128N < f_{OSC} < 400N$$

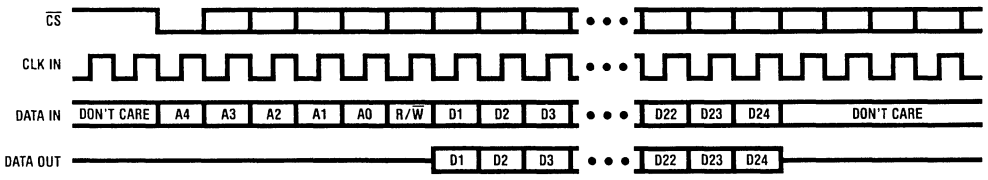
If the frequency is too slow, there will be a noticeable flicker in the display. If the frequency is too fast, there will be a loss of contrast between segments and an increase in power consumption.

Serial Input and Output

Data is sent to the MM58201 serially through the DATA IN pin. Each transmission must consist of 30 bits of information, as shown in *Figure 9*. The first five bits are the address, MSB first, of the first column of LCD segments that are to be changed. The next bit is a read or write flag. The following 24 bits are the actual data to be displayed.

The address specifies the first LCD column that is going to be affected. The columns are numbered as shown in *Figure 10*. Data is always written in three column chunks. Twenty-four bits of data must always be sent, even if some of the backplanes are not in use. The starting column can be any number between one (00000) and twenty-four (10111). If column 23 or 24 is specified the displayed data will wrap around to column 1.

If the R/$\overline{W}$ bit is a "0" then the specified columns of the LCD will be overwritten with the new data. If the bit is a "1" then the data displayed in the specified columns will be available serially at the DATA OUT pin and the display will not be changed.



TL/B/5606-11

FIGURE 9. Transmission of Data

	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	
BP1													D1	D9	D17										B2
BP2													D2	D10	D18										B1
BP3													D3	D11	D19										B0
BP4													D4	D12	D20										M/S
BP5													D5	D13	D21										
BP6													D6	D14	D22										
BP7													D7	D15	D23										
BP8													D8	D16	D24										
A4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
A2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
A1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
A0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

TL/B/5606 12

Diagram above shows where data will appear on display if starting address 01100 is specified in data format.

FIGURE 10. Address of Particular Segment Columns

The data is formatted as shown in *Figure 10*. The first bit in the data stream corresponds to backplane 1 in the first specified column. The second bit corresponds to backplane 2 in the first specified column and so on.

During initialization each MM58201 must be programmed to select how many backplanes are to be used, and whether the chip is to be a "master" or a "slave". The format of this transmission is just like a regular data transmission except for the following: the address must be 11000; the R/$\overline{W}$ must be a write (0); the first three data bits must be selected from the list in Table I. The next bit should be a "1" for the chip to be a master or a "0" for the chip to be a slave. The following 20 bits are necessary to complete the transmission but they will be ignored. The mode cannot be read back from the chip.

TABLE I. Backplane Select

Number of Backplanes	B2	B1	B0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

The timing of the CLK, $\overline{CS}$, DATA IN, and DATA OUT are illustrated in *Figure 11*. The frequency of the clock can be between DC and 100 kHz with the shortest half-period being 5.0 μs. A transmission is initiated by $\overline{CS}$ going low. $\overline{CS}$ can then be raised anytime after the rising edge of the first clock pulse and before the rising edge of the last clock pulse (the clock edge that reads in D24). 30 bits of information must always be sent.

The data at DATA IN is latched on each rising edge of the clock pulse. The data at DATA OUT is valid after each falling edge of the last 24 clock pulses.

It is important to note that during a read or write transmission the LCD will display random bits. Thus the transmissions should be kept as short as possible to avoid disrupting the pattern viewed on the display. A recommended frequency is:

$f_{OSC} = 30/(t_{LCD} - 7\,t_S)$

t_{LCD} = turn on/off time of LCD

t_S = time between each successive transmission

This should produce a flicker-free display.

The DATA OUT pin is an open drain N-channel device to V_{SS}. This output must be tied to V_{DD} through a resistor if it is to be used. It could also be tied to a lower voltage if this output is to be interfaced to logic running at a lower voltage. The value of the resistor is calculated by:

$R = (+V - 0.4)/0.0006$

$+V$ = voltage of lower voltage logic

Power Supply

V_{DD} can range between 7V and 18V. A voltage should be used that is greater than or equal to the voltage that you calculate for V_{TC} as shown in *Figure 5*.

TYPICAL APPLICATIONS

One application of the MM58201 is a general purpose display to show graphic symbols and text. This type of display could be used in an electronic toy or a small portable computer or calculator. One such display is shown in *Figure 12.* This display consists of four separate LCD displays that are built into one housing. Each separate LCD display has 8 backplanes and 24 segment lines. The entire display will require four MM58201s to control it.

The circuit diagram of this application is shown in *Figure 14.* Each separate LCD display is driven by one MM58201. The backplanes are driven by the separate MM58201s and are not paralleled together. There are three common lines: CLK, DATA IN, and DATA OUT. The CLK and DATA IN are generated from an output port such as an INS8255. Four other bits of the output port generate a linear select with a different bit going to each MM58201 chip select as shown in *Figure 13.* DATA OUT is sent to one bit of an input port.

The V_{TC} driver is as described beforehand. The MM74C906 is an open drain CMOS buffer that has near regular TTL compatible inputs. This is to provide level translation from the 5V supply of the computer system to the 12V supply of the MM58201.

If I/O ports are not available, the circuit in *Figure 15* could be used as an interface between the MM58201s and a microprocessor bus.

To reduce the number of connections between the circuit and the LCD, all of the backplanes could have been driven by one MM58201 as shown in *Figure 16.* The other MM58201s would be configured as "slaves" synchronized to the one "master" MM58201. This would save 24 connections to the LCD but would increase the capacitance of the backplanes. In this application the capacitance is not a problem with either setup.

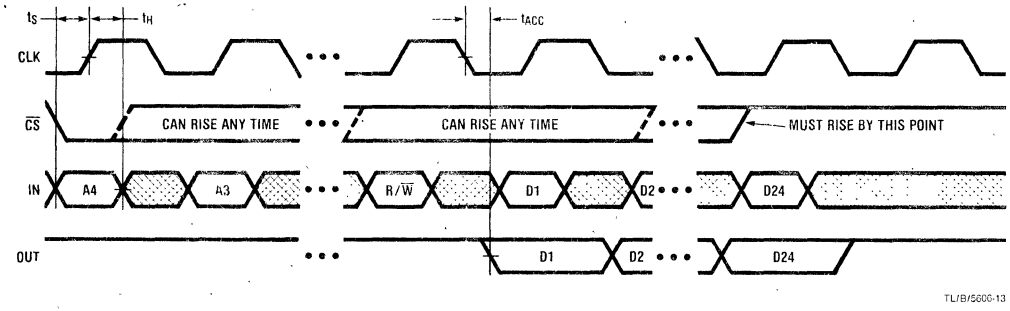


FIGURE 11. Timing of One Transmission

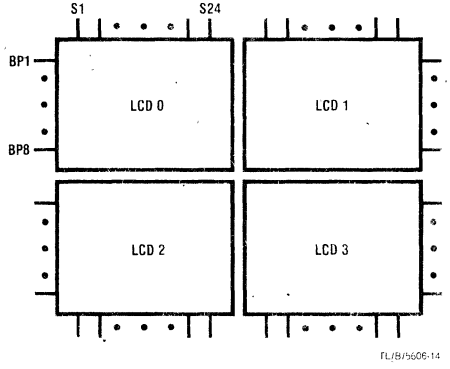
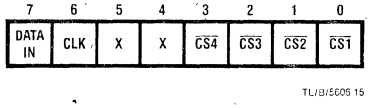


FIGURE 12. Four Separate LCD Displays Positioned to Look Like One Display



$\overline{CS4}$	$\overline{CS3}$	$\overline{CS2}$	$\overline{CS1}$	
1	1	1	0	Chip 1 selected
1	1	0	1	Chip 2 selected
1	0	1	1	Chip 3 selected
0	1	1	1	Chip 4 selected
1	1	1	1	No chip selected

FIGURE 13. Chip Select Scheme

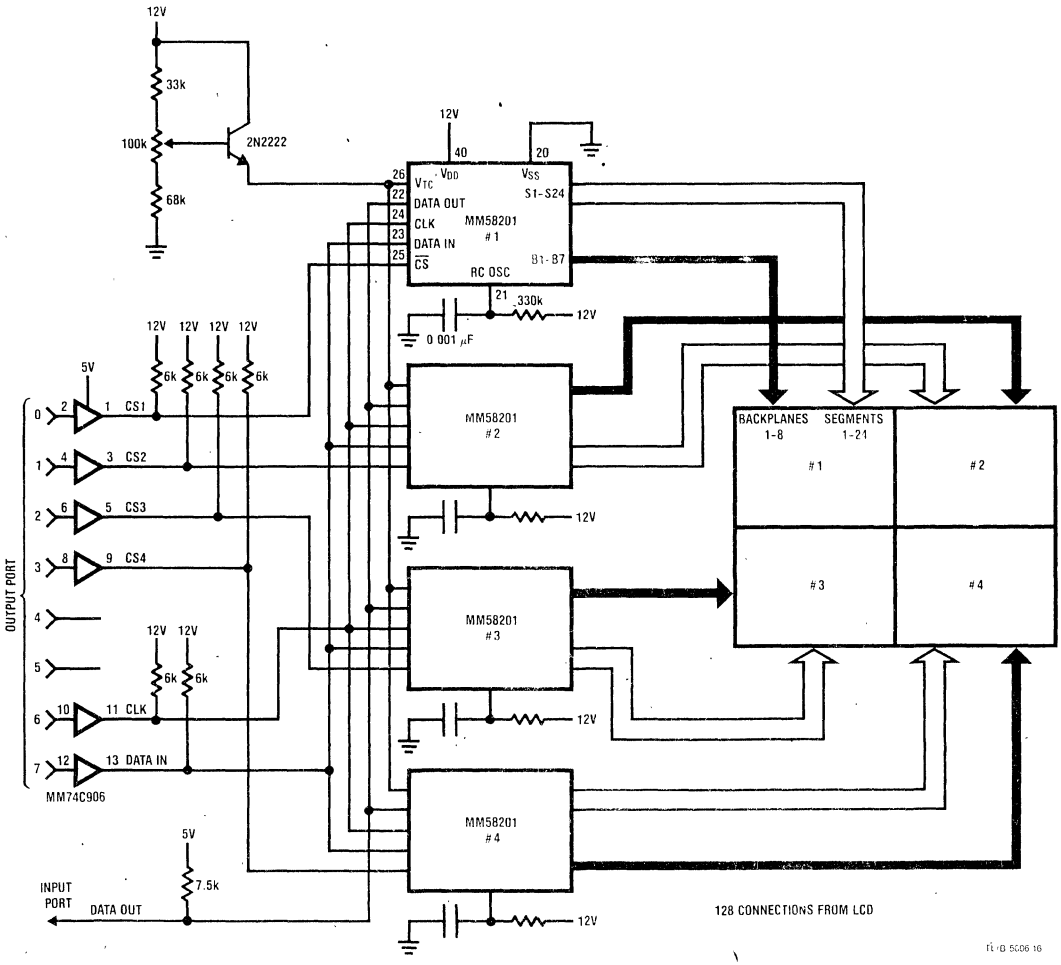
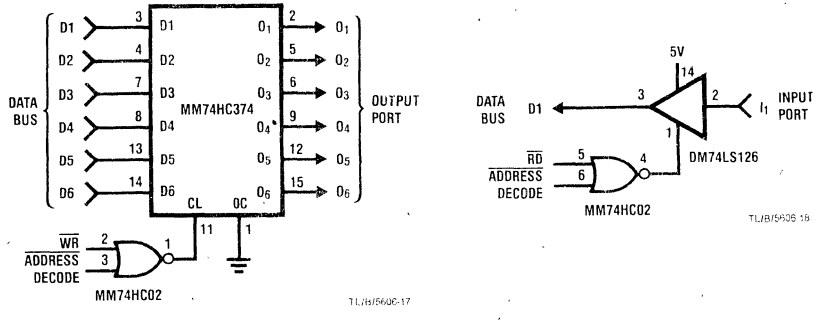


FIGURE 14. Diagram of Application



a. Output Port

b. Input Port

FIGURE 15. Input and Output Ports for Interface

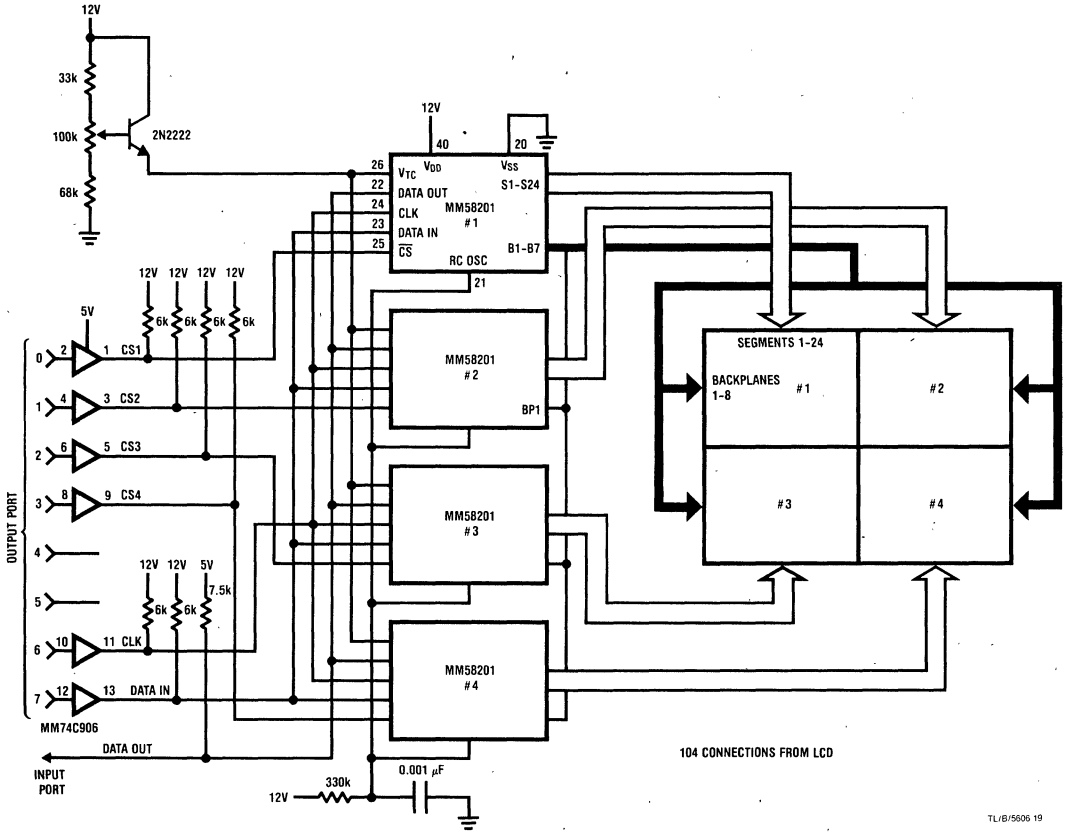


FIGURE 16. Diagram of Master-Slave Set-Up Not Used for this Application

SOFTWARE

The real heart of this system is the software which consists of four parts. Part one is the initialization portion. This sets up the MM58201s as "masters" and programs them for 8 backplanes. It then sets up the needed pointers for the other subroutines which consist of:

1) GRAPH: displays pattern on LCD.
2) TEXT: prints ASCII characters on display.
3) SCROLL: scrolls whatever pattern is displayed to the right until LCD is cleared.

This application used an NSC800™ with 8080 mnemonics. It could easily be adapted for other microprocessors.

MAIN

This progam initializes the MM58201s. It controls the sequence of display output by calling other programs.

It first sends out a "dummy" transmission to make sure that the chips are ready to respond to a valid transmission. It then programs the chips to be "masters" and to use eight backplanes.

After initialization, this program sets up the correct pointers to display a graphic symbol. First it displays the upper eight bits of it, then it displays the lower eight bits.

The words "TESTING MM58201" are then displayed. A call to scroll then causes this to scroll to the right until the screen is blank. Finally the words "END OF TEST" appear and the program ends.

The method to create a custom graphic symbol will be demonstrated in the next section.

```
        NGRAD
        EXTRN GRAPH,WRITE,MODE,TEXT,CURSOR,SCROLL

;INITIALIZE THE STACK POINTER
        LXI SP,0FFFH

;INITIALIZE THE 810
;SET MODE 0 FOR PORT A
INIT:   MVI A,00H
        OUT 27H
;SET PORT A AS OUTPUT AND PORT C AS INPUT
        MVI A,0FFH
        OUT 24H         ;PORT A DDR
        MVI A,00H
        OUT 26H         ;PORT B DDR

;INITIALIZE THE FOUR 58201'S
        MVI A,0         ;SET FOR WRITE MODE
        STA MODE
        LXI H,MASTER    ;SEND A COMPLETE TRANSMISSION TO CLEAR OUT
        MVI E,11000B    ;   ANY OLD CHIP SELECT.
        MVI D,00001110B
        CALL WRITE
        LXI H,MASTER    ;CONFIGURE CHIPS 0, 1, 2, AND 3 AS MASTERS
        MVI D,00001110B
        CALL WRITE
        LXI H,MASTER
        MVI D,00001101B
        CALL WRITE
        LXI H,MASTER
        MVI D,00001011B
        CALL WRITE
        LXI H,MASTER
        MVI D,00000111B
        CALL WRITE

;SET UP POINTER AND COUNTERS TO DISPLAY NATIONAL SEMI SYMBOL
        MVI B,21        ;B HOLDS # OF COLUMNS TO CHANGE
RESTRT: MVI D,0         ;D HOLDS THE STARTING COLUMN NUMBER FOR UPPER HALF
        MVI E,48        ;E HOLDS STARTING COLUMN NUMBER FOR LOWER HALF
DSLOOP: MOV C,D
        LXI H,NATSM1    ;DISPLAY UPPER HALF OF GRAPHIC
        CALL GRAPH
        LXI H,NATSM2    ;DISPLAY LOWER HALF OF GRAPHIC
        MOV C,E
        CALL GRAPH

        LXI H,0FFFFH    ;PAUSE
PAUSE:  DCX H
        MOV A,H
        ORA L
        JNZ PAUSE

        INR D           ;INCREMENT STARTING COLUMN NUMBERS
        INR D
        INR D
        INR E
        INR E
        INR E
        MVI A,30        ;DISPLAY IT UNTIL COLUMN COUNT IS 30
        CMP D
        JNZ DSLOOP

        LXI H,TEXT1     ;PRINT FIRST TEXT
        MVI A,0         ;ZERO THE CURSOR
        STA CURSOR
        CALL TEXT

        CALL SCROLL     ;SCROLL THE TEXT

        LXI H,TEXT2     ;PRINT SECOND TEXT
        MVI A,0         ;ZERO THE CURSOR
        STA CURSOR
        CALL TEXT

        LXI H,0FFFFH    ;PAUSE
PAUSE1: DCX H
        MVI A,2
PAUSE2: DCR A
        JNZ PAUSE2
        MOV A,H
        ORA L
        JNZ PAUSE1
```

```
        LXI H,TEXT3     ;PRINT THIRD TEXT
        MVI A,0
        STA CURSOR
        CALL TEXT

        RST 6           ;END

TEXT1:  DB 'TESTING MM58201 ', 0
TEXT2:  DB 'THIS IS THE END ', 0
TEXT3:  DB ' OF THE   TEST  ', 0

MASTER: DB 1111B        ;ADDRESS FOR MASTER
SLAVE:  DB 0111B        ;ADDRESS FOR SLAVE

NATSM1: DB 0FFH, 0FFH, 0FFH, 7FH, 3FH, 9FH, 0CFH, 67H, 33H, 01H, 7FH
        DB 3FH, 9FH, 0CFH, 67H, 33H
        DB 99H, 0FFH, 0FFH, 00H, 00H
NATSM2: DB 0FFH, 0FFH, 0FFH, 0E6H, 0F3H, 0F9H, 0FCH, 0FEH, 0FFH
        DB 0E0H, 0E6H, 0F3H, 0F9H, 0FCH
        DB 0FEH, 0FFH, 0FFH, 0FFH, 0FFH, 00H, 00H
        END
```

GRAPH

This subroutine is the center of the software. It is the interface between the calling programs and the hardware. All I/O is generated by this subroutine.

There are two entrances to this subroutine: graph and read. Graph is the entrance used to display new data. Read is the entrance used to read data from the display.

The HL register should point to the beginning of the data to be displayed. The B register should hold the number of columns to change. This must be a multiple of three. The C register should hold the column number to start with. This must also be a multiple of three. These restrictions are to simplify the software.

The first operation is the calculation of the correct chip to enable and the column number to start within that chip. The first bit of the column address is output with the correct chip select going low. The rest of the column address is then output with all the chip selects high. If the operation is a write, the data is sent to the display bit by bit. If the operation is a read, the data is read in bit by bit.

To create a custom graphic symbol, draw it on a grid as shown in *Figure 17*. Group the upper eight squares as a byte with the least significant bit at the top, counting a dark square as a one. Group the lower eight squares as a byte with the most significant bit at the bottom. Use this generated data as input lists to the graph subroutine. A good example of this is shown in the listing of main when it calls graph.

Pad the data at the end with zeros as shown to keep the number of data values a multiple of three. Remember, this is only a software restriction. A different routine could be used that would allow any number of columns to be displayed.

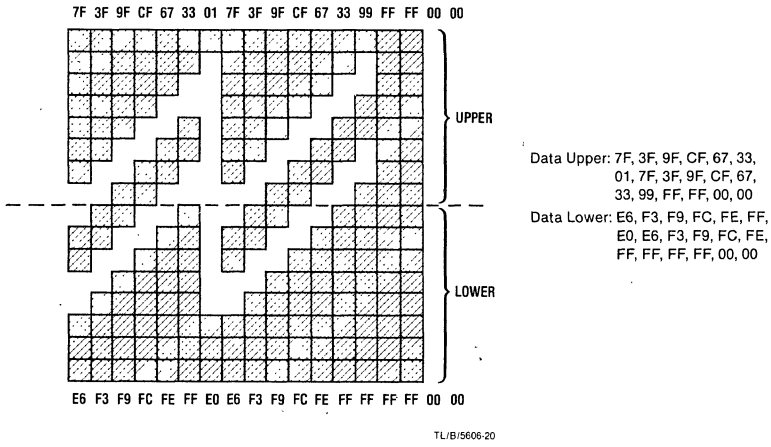


FIGURE 17. Example Graphic Symbol

```
        NOOBO
        PUBLIC GRAPH, READ, WRITE, MODE

;GRAPHIC DISPLAY DRIVER
;       INPUT:  HL - POINTS TO START OF DATA
;               B  - # OF 8 BIT COLUMNS TO CHANGE (MUST BE MULT. OF 3)
;               C  - COLUMN # TO START WITH (MUST BE MULT. OF 3)
;       OUTPUT: NO REGISTERS DISTURBED
;               DATA POINTED TO IS DISPLAYED ON LCD DISPLAY,
;               COLUMNS NOT SPECIFIED ARE NOT EFFECTED.

READ:
;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H

;FLAG FOR A READ OPERATION
        MVI A,10000000B
        STA MODE
        JMP GRAPH1

GRAPH:
;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H

;FLAG FOR A WRITE OPERATION
        MVI A,0
        STA MODE

;CALCULATE WHICH 58201 TO ACCESS
GRAPH1: MVI D,0EEH      ;START WITH CS1
ACC:    MOV A,C
        SUI 24          ;SUBTRACT 24 FROM COLUMN COUNT
        JC GO           ;IF CARRY IS SET THE CORRECT CHIP IS SELECTED
        MOV C,A         ;REG C GETS NEW COLUMN NUMBER
        MOV A,D
        RLC             ;INCREMENT THE CS TO NEXT CHIP
        MOV D,A
        JMP ACC

;MAIN LOOP
GO:     MOV E,C         ;GET COLUMN NUMBER
M.LOOP: CALL WRITE      ;DRAW 3 COLUMNS
        DCR B           ;SUBTRACT 3 FROM COLUMN COUNT
        DCR B
        DCR B
        JZ END.G        ;IF DONE, JUMP.
        MOV A,E         ;ADD 3 TO ADDRESS
        ADI 3
        CPI 11000B      ;IF ADDRESS NOT MAX THEN SKIP THIS
        JNZ SKIP1
        MOV A,D
        RLC             ;SELECT NEXT 58201 CS
        MOV D,A
        MVI A,0
SKIP1:  MOV E,A         ;SAVE NEXT ADDRESS
        JMP M.LOOP      ;LOOP UNTIL DONE

END.G:  POP H           ;RESTORE ALL STATES
        POP D
        POP B
        POP PSW
        RET

WRITE:
;       DISPLAY 3 COLUMNS OF DATA
;       INPUT:  HL- POINTS TO START OF DATA
;               E - ADDRESS
;               D - OUTPUT CS
;       OUTPUT: HL<- HL + 3

;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D

START:  MVI A,00001111B ;ISOLATE CS IN REG D
        ANA D
        MOV D,A
        MOV A,E         ;GET ADDRESS BITS AT HIGH END OF BYTE
        RLC
        RLC
        MOV E,A
```

```
;OUTPUT FIVE ADDRESS BITS WITH CHIP SELECT
        MVI C,5
W.LOOP: MOV A,E
        RLC             ;ROTATE ADDRESS
        MOV E,A
        MVI A,10000000B
        ANA E           ;GET MSB
        ORA D           ;MERGE WITH CHIP SELECT
        CALL DISPLY
        DCR C           ;DEC ADDRESS BIT COUNTER
        JNZ W.LOOP      ;LOOP UNTIL ADDRESS IS OUT

;SIGNAL FOR A READ OR WRITE
        LDA MODE
        ORI 00001111B
        CALL DISPLY
        JP DIS0         ;JUMP IF THIS IS A WRITE

;READ THE DATA
        MVI B,3         ;3 BYTES OF DATA
READ1:  MVI C,8         ;8 BITS PER BYTE
        MVI D,0         ;CLEAR DATA BYTE
READ2:  IN 22H          ;GET A BIT OF DATA
        ANI 00000001B   ;MASK OFF UNWANTED BITS
        ORA D           ;MERGE WITH DATA BYTE
        RRC             ;ROTATE DATA
        MOV D,A
        MVI A,00001111B ;SET UP 58201 TO READ NEXT BIT
        CALL DISPLY
        DCR C           ;LOOP UNTIL DONE WITH BYTE
        JNZ READ2
        MOV M,D
        INX H           ;INCREMENT BYTE POINTER
        DCR B           ;LOOP UNTIL DONE WITH ALL BYTES
        JNZ READ1

;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET


;DISPLAY THE DATA
DIS0:   MVI B,3         ;3 BYTES OF DATA
DIS1:   MVI C,8         ;8 BITS PER BYTE
        MOV D,M
DIS2:   MOV A,D         ;ROTATE DATA
        RRC
        MOV D,A
        ANI 10000000B   ;GET NEXT BIT
        ORI 00001111B   ;SET CS
        CALL DISPLY     ;OUTPUT A BIT OF DATA
        DCR C
        JNZ DIS2        ;LOOP UNTIL DONE WITH BYTE
        INX H
        DCR B
        JNZ DIS1        ;LOOP UNTIL DONE WITH 3 BYTES

;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

DISPLY:
;DISPLAY ROUTINE
;       INPUT:  A - DATA AND CHIP SELECT
;                       BIT 7 - DATA
;                       BITS 0-3 - CHIP SELECT
;       OUTPUT: NO REGISTERS DISTURBED
;               OUTPUT ONE BIT TO 58201

        PUSH PSW        ;SAVE STATES

        ANI 10001111B   ;MASK OFF UNWANTED BITS
        OUT 20H         ;SET UP DATA AND CHIP SELECT
        ORI 01000000B   ;CLOCK HIGH
        OUT 20H
        ANI 10111111B   ;CLOCK LOW
        OUT 20H

        POP PSW         ;RESTORE STATES
        RET

MODE:   DS 1
        END
```

TEXT

This subroutine will take the ASCII text pointed to by HL and display it on the LCD starting at the column pointed to by the memory location CURSOR. The data should end with a zero. CURSOR should be in the range of 0-15 as this is the extent of this LCD display. The first operation is the calculation of the offset into the ASCII table of the first character. Thirty-two is subtracted from the ASCII number because the table starts with a space character. This result is then multiplied by six because the data to be displayed is six bytes long. We now have the offset into the table. The character is displayed on the LCD. This operation is repeated until all the characters have been displayed.

A custom font can be generated using the same technique as that used to create a custom graphic symbol.

```
        N8080
        EXTRN GRAPH
        PUBLIC TEXT, LETTR, CURSOR

TEXT:
;DISPLAY A CHARACTER STRING ON LCD DISPLAY
;       INPUT:  HL - POINTS TO BEGINNING OF STRING
;               CURSOR - CURRENT CURSOR POSITION
;       OUTPUT: CURSOR <= CURSOR + LENGTH OF STRING
;               NO REGISTERS DISTURBED

        PUSH PSW        ;SAVE STATES
        PUSH H
T.LOOP: MOV A,M         ;CHECK FOR END OF STRING
        CPI 0
        JZ T.FIN
        CALL LETTR      ;PRINT LETTER
        INX H
        JMP T.LOOP      ;LOOP UNTIL DONE
T.FIN:  POP H           ;RESTORE STATES
        POP PSW
        RET


LETTR:
;DISPLAY AN ASCII CHARACTER ON LCD DISPLAY
;       INPUT:  A - CHARACTER TO DISPLAY
;               CURSOR - CURRENT CURSOR LOCATION (0 - 95)
;       OUTPUT: CURSOR <= CURSOR + 1
;               NO REGISTERS DISTURBED

;SAVE STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H

;SET UP HL TO POINT TO CORRECT DATA
        LXI H,ASCII     ;HL POINTS TO BASE ADDRESS
        MVI B,0         ;BC GETS ASCII OFFSET MINUS A CONSTANT
        SUI 20H
        MOV C,A
        CALL MULT       ;MULTIPLY OFFSET BY 6 (DOUBLE PRECISION)
        DAD B           ;HL POINTS TO CORRECT CHARACTER DATA
        LDA CURSOR      ;MULTIPLY CURSOR BY 6 TO GET COLUMN NUMBER
        MOV B,A
        ADD B
        ADD B
        ADD B
        ADD B
        ADD B
        MOV C,A
        MVI B,6         ;EACH CHARACTER IS SIX COLUMNS WIDE
        CALL GRAPH      ;DISPLAY THE CHARACTER
        LDA CURSOR      ;INCREMENT CURSOR
        INR A
        CPI 16          ;CHECK FOR END OF LCD DISPLAY
        JNZ T.END
        MVI A,0         ;IF SO, RESET TO ZERO
T.END:  STA CURSOR

;RESTORE STATES
        POP H
        POP D
        POP B
        POP PSW
        RET
```

```
MULT:
;MULTIPLY BC REG BY SIX
;       INPUT:  BC = MULTIPLICAND
;       OUTPUT: BC <= BC * 6
;               NO REGISTERS DISTURBED

        PUSH PSW
        PUSH H
        MOV H,B
        MOV L,C
        DAD B
        DAD B
        DAD B
        DAD B
        DAD B
        MOV B,H
        MOV C,L
        POP H
        POP PSW
        RET

CURSOR: DS 1
ASCII:  DB 0,0,0,0,0,0          ;SPACE
        DB 0,95,95,0,0,0        ;!
        DB 0,7,0,7,0,0          ;"
        DB 20,127,20,127,20,0   ;#
        DB 36,42,127,42,18,0    ;$
        DB 35,19,8,100,98,0     ;%
        DB 54,73,102,32,80,0    ;&
        DB 0,0,7,0,0,0          ;'
        DB 0,28,34,65,0,0       ;(
        DB 0,65,34,28,0,0       ;)
        DB 34,20,127,20,34,0    ;*
        DB 8,8,62,8,8,0         ;+
        DB 0,64,48,0,0,0        ;'
        DB 8,8,8,8,8,0          ;-
        DB 0,96,96,0,0,0        ;.
        DB 32,16,8,4,2,0        ;/

        DB 62,81,73,69,62,0     ;0
        DB 0,66,127,64,0,0      ;1
        DB 122,73,73,73,70,0    ;2
        DB 34,65,73,73,54,0     ;3
        DB 15,8,8,126,8,0       ;4
        DB 39,69,69,69,57,0     ;5
        DB 62,73,73,73,49,0     ;6
        DB 1,97,17,9,7,0        ;7
        DB 54,73,73,73,54,0     ;8
        DB 6,9,9,9,126,0        ;9
        DB 0,54,54,0,0,0        ;:
        DB 96,54,54,0,0,0       ;;
        DB 8,20,34,65,0,0       ;<
        DB 20,20,20,20,20,0     ;=
        DB 0,65,34,20,8,0       ;>
        DB 2,1,88,5,2,0         ;?
        DB 62,65,93,89,78,0     ;@

        DB 124,18,17,18,124,0   ;A
        DB 127,73,73,73,54,0    ;B
        DB 62,65,65,65,34,0     ;C
        DB 127,65,65,65,62,0    ;D
        DB 127,73,73,65,65,0    ;E
        DB 127,9,9,1,1,0        ;F
        DB 62,65,65,81,114,0    ;G
        DB 127,8,8,8,127,0      ;H
        DB 0,65,127,65,0,0      ;I
        DB 32,64,64,64,63,0     ;J
        DB 127,8,20,34,65,0     ;K
        DB 127,64,64,64,64,0    ;L
        DB 127,2,12,2,127,0     ;M
        DB 127,4,8,16,127,0     ;N
        DB 62,65,65,65,62,0     ;O
        DB 127,9,9,9,6,0        ;P
        DB 62,65,81,33,94,0     ;Q
        DB 127,9,25,41,70,0     ;R
        DB 34,69,73,81,34,0     ;S
        DB 1,1,127,1,1,0        ;T
        DB 63,64,64,64,63,0     ;U
        DB 31,32,64,32,31,0     ;V
        DB 127,32,24,32,127,0   ;W
        DB 99,20,8,20,99,0      ;X
        DB 3,4,120,4,3,0        ;Y
        DB 97,81,73,69,67,0     ;Z

        END
```

SCROLL

This subroutine will scroll whatever is displayed on the LCD to the right until the screen is clear. It first reads in three columns of data. It then writes three columns of data with the HL pointer shifted by one byte. This will shift the displayed data by one column. This is repeated until the entire LCD has been shifted by one column. Then the entire operation is repeated until all the displayed data is shifted off the screen.

This subroutine could easily be adapted to scroll the display to the left if desired.

```
        N8080
        PUBLIC SCROLL
        EXTRN READ,GRAPH

SCROLL:
;SCROLLS DISPLAY TO THE RIGHT UNTIL CLEAR
;       INPUT:  NONE
;       OUTPUT: NO REGISTERS ARE CHANGED
;               SCREEN IS SCROLLED UNTIL CLEAR

;SAVE ALL STATES
        PUSH PSW
        PUSH B
        PUSH D
        PUSH H

;SET UP ALL THE POINTERS
        MVI D,96            ;LOOP UNTIL SCREEN IS CLEAR (96 CYCLES)
REPEAT: MVI A,0             ;CLEAR FIRST BYTE IN BUFFER
        STA BUFFER
        MVI B,3             ;READ 3 COLUMNS ALWAYS
        MVI C,0             ;START WITH COLUMN ZERO

;READ THE DATA
L.READ: LXI H,BUFFER+1      ;SET HL TO POINT TO BUFFER+1
        CALL READ
        LXI H,BUFFER        ;SET HL TO SHIFT THE DATA
        CALL GRAPH          ;REDRAW THE SHIFTED DATA

;MOVE LAST COLUMN OF LAST READ INTO FIRST COLUMN OF NEXT WRITE
        LDA BUFFER+3
        STA BUFFER

;UPDATE COUNTERS
        MOV A,C             ;INCREMENT COLUMN NUMBER
        ADI 3
        MOV C,A
        CPI 96              ;CHECK IF DONE WITH ONE CYCLE
        JNZ L.READ
        DCR D               ;DECREMENT LOOP COUNT
        JNZ REPEAT          ;LOOP UNTIL DONE WITH ALL CYCLES

;RESTORE STATES
        POP H
        POP D
        POP B
        POP PSW
        RET

BUFFER: DS 4

        END
```

OTHER APPLICATIONS

There are many different types of LCDs that can be controlled by the MM58201. Some of these are shown in *Figure 18.*

Up to 24 seven-segment digits can be controlled by one MM58201. The software to control a multiplexed seven-segment display is not too much different from that of the previous application. The software is simpler because only one MM58201 is needed instead of four. A logic diagram for a six-digit multiplexed seven-segment LCD display is shown in *Figure 19* and the software to control it is in Listing 5.

Given a string of numbers to display, this subroutine simply looks up the data it needs from a look-up table and stores this data in a buffer. After every three digits, the subroutine sends this data to the MM58201 to be displayed. The digit backplanes are wired backward in groups of three to simplify the software. The subroutines that this subroutine uses are very similar to the equivalent subroutines in the LCD dot matrix application. Since there is only one MM58201, the software is simpler. There is no need to calculate which MM58201 chip select to enable.

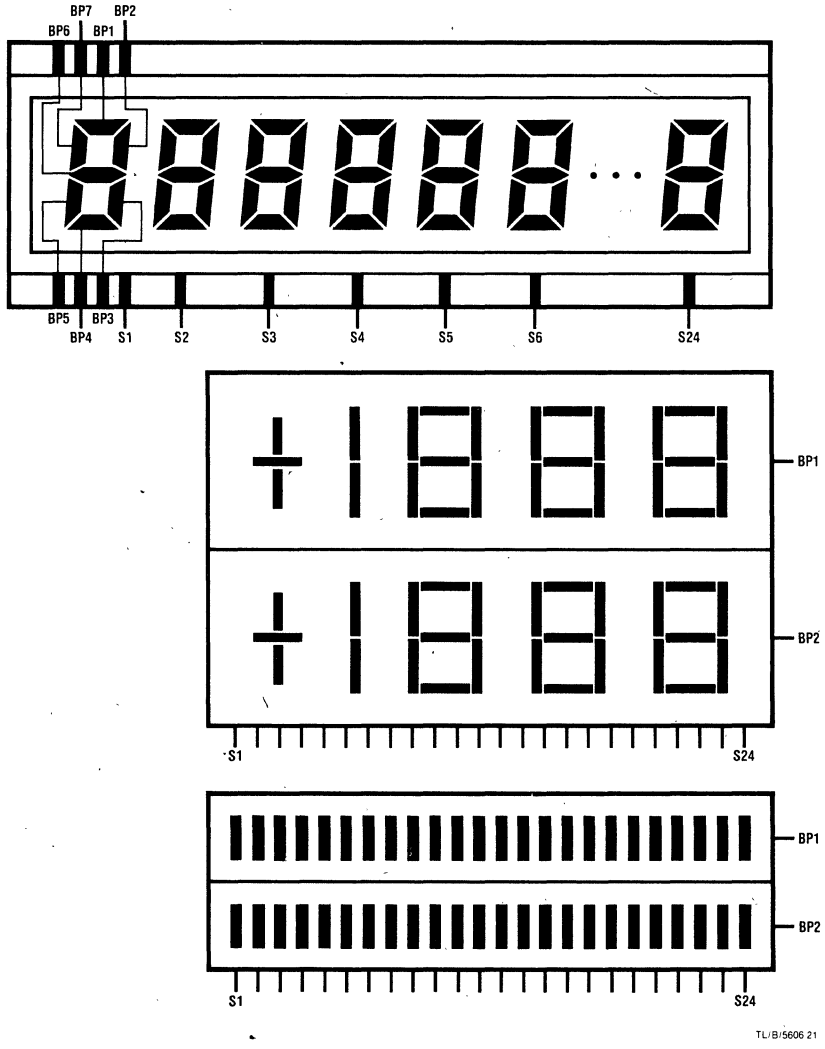


FIGURE 18. Typical LCD Connections to the MM58201

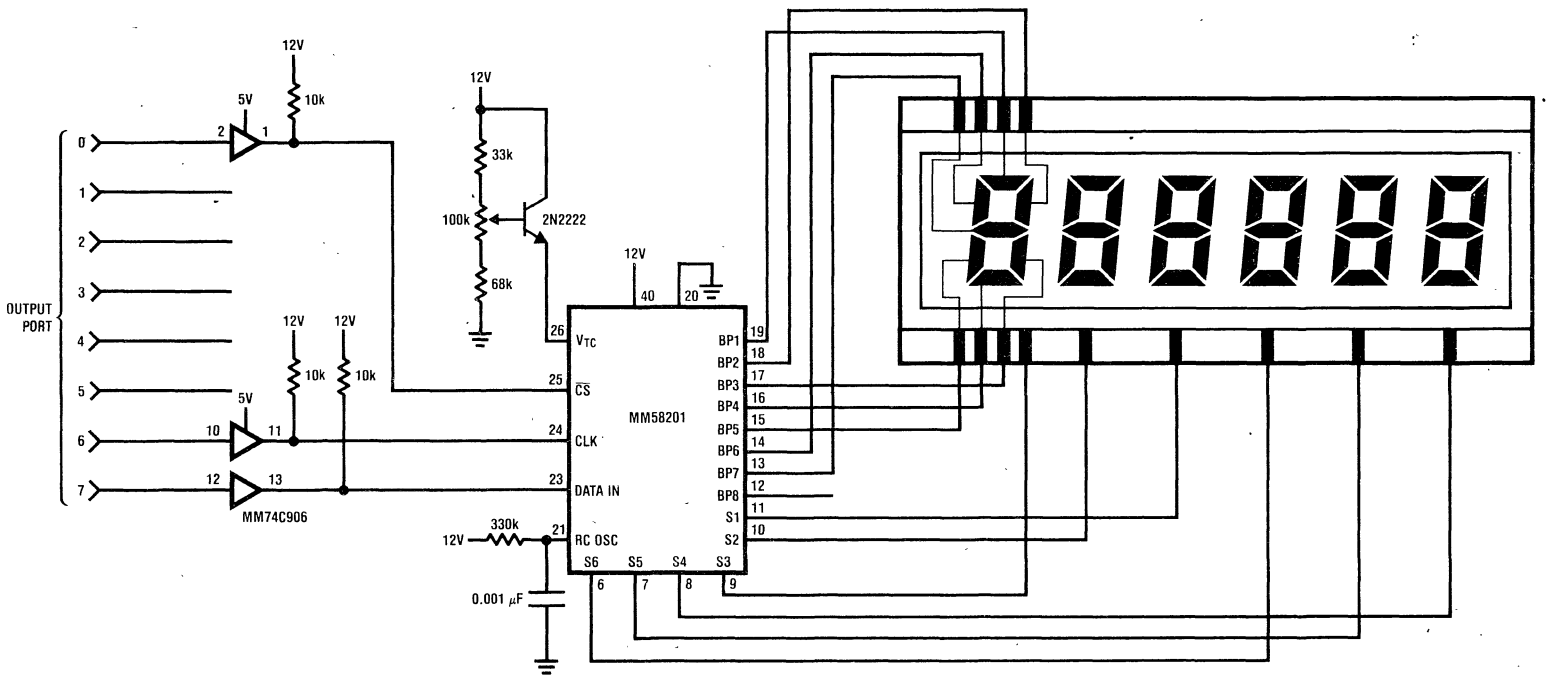


FIGURE 19. Diagram of a Six-Digit Seven-Segment LCD Multiplexed Display

```
        N8000
;INITIALIZE THE 810
        MVI A,0
        OUT 27H
        MVI A,0FFH
        OUT 24H

        LXI BC,TEST
        MVI E,6
        CALL NUMBER
        RST 6

TEST:   DB 1,2,3,4,5,6

;SUBROUTINE TO DISPLAY NUMERALS ON LCD DISPLAY
;       INPUT   BC- POINTS TO BCD DATA STRING
;               E - LENGTH OF DATA STRING (MULTIPLE OF 3)
;       OUTPUT    - NO REGISTERS DISTURBED
;                 - DATA STRING IS DISPLAYED
;
NUMBER: PUSH PSW        ;SAVE STATES
        PUSH B
        PUSH D
        PUSH H

DIG3:   MVI D,3         ;LOOP FOR 3 DIGITS
LOOP:   LDAX B
        LXI H,TABLE     ;CALCULATE ADDRESS INTO TABLE
        ADD L
        MOV L,A
        MVI A,00H
        ADC H
        MOV H,A

        MOV A,M         ;GET OUTPUT DATA FROM TABLE
        PUSH PSW

        LXI H,DATA      ;STORE INTO DATA BUFFER
        MOV A,L
        ADD D
        MOV L,A
        DCR L
        POP PSW
        MOV M,A

        INX B           ;INCREMENT POINTER TO DATA STRING
        DCR E           ;DECREMENT # OF DIGITS
        DCR D           ;DECREMENT 3 DIGIT COUNT
        JNZ LOOP        ;IF NOT THIRD DIGIT THEN LOOP BACK

        LXI H,DATA
        CALL WRITE      ;DISPLAY THESE THREE DIGITS

        MOV A,E         ;CHECK FOR LAST DIGIT OF DATA STRING
        ANA A
        JNZ DIG3

        POP H           ;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

WRITE:
; DISPLAY 3 DIGITS
;       INPUT   HL- POINTS TO START OF DATA
;               E - COLUMN ADDRESS
;       OUTPUT    - NO REGISTERS DISTURBED
;
        PUSH PSW        ;SAVE STATES
        PUSH B
        PUSH D
        PUSH H

        MOV A,E         ;GET ADDRESS BITS AT HIGH END OF BYTE
        RLC
        RLC
        MOV E,A
```

```
;OUTPUT FIVE ADDRESS BITS
        MVI C,5
W.LOOP: MOV A,E
        RLC                 ;ROTATE ADDRESS
        MOV E,A
        MVI A,10000000B ;GET MSB & ENABLE CHIP SELECT BIT
        ANA E
        CALL OUT            ;OUTPUT BIT WITH CHIP SELECT
        DCR C
        JNZ W.LOOP          ;LOOP UNTIL ADDRESS IS OUT

;SIGNAL FOR A WRITE
        MVI A,00H
        CALL OUT            ;OUTPUT A ZERO BIT

;OUTPUT THE DATA
        MVI B,3             ;3 BYTES OF DATA
DIS1:   MVI C,8             ;8 BITS PER BYTE
        MOV D,M
DIS2:   MOV A,D             ;ROTATE DATA
        RRC
        MOV D,A
        ANI 10000000B       ;GET NEXT BIT
        ORI 00000001B       ;DISABLE CHIP SELECT
        CALL OUT
        DCR C
        JNZ DIS2            ;LOOP UNTIL DONE WITH BYTE
        INX H
        DCR B
        JNZ DIS1            ;LOOP UNTIL DONE WITH 3 BYTES

        POP H               ;RESTORE STATES
        POP D
        POP B
        POP PSW
        RET

OUT:
;SUBROUTINE TO OUTPUT ONE BIT TO THE MM58201
;       INPUT    A - DATA BIT IN MSB POSITION
;       OUTPUT     - NO REGISTERS DISTURBED
;                  - OUTPUT ONE BIT TO 58201

        PUSH PSW
        OUT 20H
        ORI 01000000B       ;CLOCK HIGH
        OUT 20H
        ANI 10111111B       ;CLOCK LOW
        OUT 20H
        POP PSW
        RET

DATA:   DS 3
TABLE:  DB 00111111B, 00000110B, 01011011B, 01001111B
        DB 01100110B, 01101101B, 01111101B, 00000111B
        DB 01111111B, 01101111B

        END
```

SUMMARY

The MM58201 makes it easy to interface a multiplexed LCD display to a microprocessor. It is simply a matter of connecting the display and the microprocessor to the chip, choosing a value for V_{TC}, then interfacing your program to use the subroutines listed here or similar ones.

Multiplexed LCDs are the perfect way to cut down on display interconnections while still taking advantage of the LCD's low power consumption and high contrast ratio—and the MM58201 makes them easy to use.

MM58167A Real Time Clock Design Guide

National Semiconductor
Application Note 353
Milt Schwartz
May 1984

The MM58167A is a real-time 24-hour format clock with in-out/output structure and control lines that facilitate interfacing to microprocessors. It provides a reliable source of calendar data from milliseconds through months, as well as 6 bytes plus 2 nibbles of RAM, which are available to the user if the alarm (compare) interrupt is not used. The MM58167A features low power consumption (typically 4.5 microamperes at 3-volt supply) during battery backed mode, flexible interrupt structure (alarm and repetitive), and a fast internal update rate (1 kHz). Systems utilizing this device include, personal computers, process control, security, and data acquisition.

This application note covers hardware interface to microprocessors, clock interrupts, oscillator operation, accuracy, calibration techniques, software, and battery back-up considerations.

Hardware Description Overview

1.0 *Figure 1* is a functional block diagram of the MM58167A. It can be subdivided into the following sections:

1.1 Oscillator

The oscillator consists of an internal inverter to which the user connects a 32.768 kHz crystal, bias resistor and capacitors, to form a Pierce parallel resonant circuit.

1.2 Prescaler

The prescaler divides the 32.768 kHz oscillator down to 1 kHz using pulse swallowing techniques. The 1 kHz pulse rate is the incrementing signal for the timekeeping counters.

Block Diagram

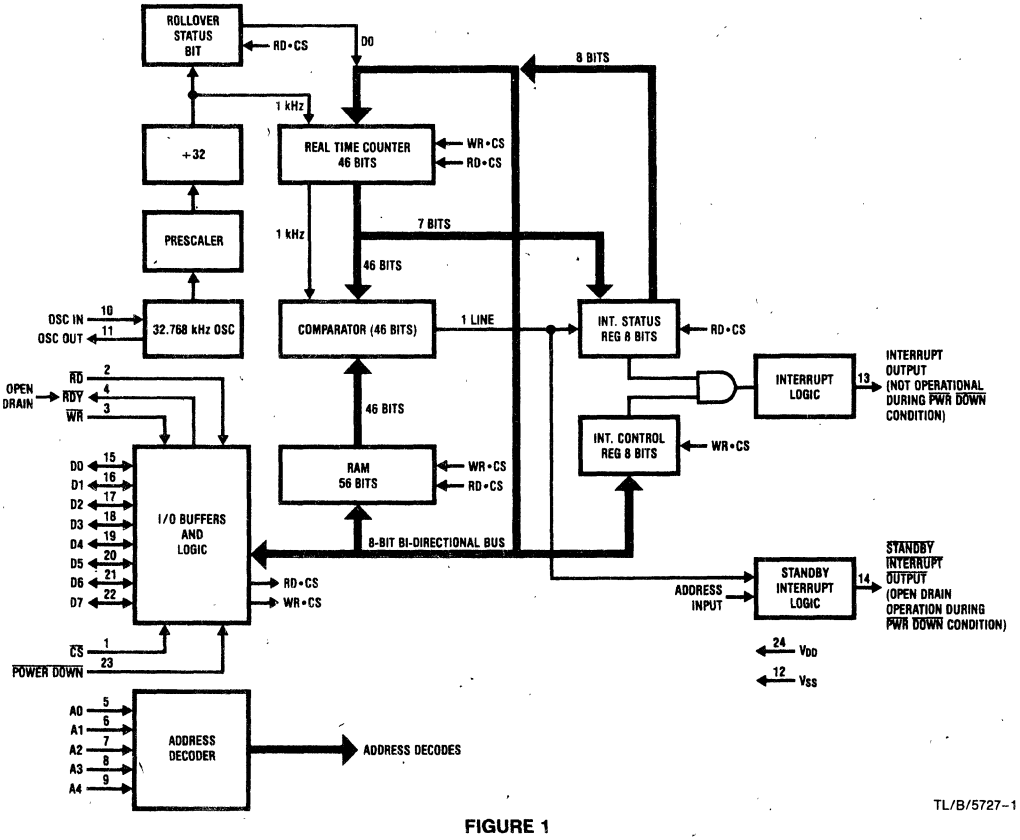


FIGURE 1

Hardware Description Overview (Continued)

1.3 Timekeeping Counters

The timekeeping section consists of a 14-stage BCD counter, each stage having read/write capability. The counters keep time in a 24-hour format. *Figure 8* shows the counter detail of calendar-date-time format.

1.4 Rollover Status

A rollover status bit (read only) informs the user that invalid data may have been read, due to the counters being incremented during a counter read or between successive counter reads. This situation occurs because the counters are clocked asynchronously with respect to the microprocessor.

1.5 RAM

14 nibbles of RAM are provided for alarm (compare) interrupt or general storage. The nibbles are packed 2 per address except for 2 locations, address 08 and 0D (HEX). The nibble at address 08 appears in the high order 4 bits, while the nibble at address 0D appears in the low order 4 bits. See memory map *Figure 2* for details.

Address In HEX	D7 D6 D5 D4	D3 D2 D1 D0
8	Milliseconds	No RAM Exists
9	Tenths of Seconds	Hundredths of Seconds
A	Tens of Seconds	Units of Seconds
B	Tens of Minutes	Units of Minutes
C	Tens of Hours	Units of Hours
D	No RAM Exists	Day of Week
E	Tens Day of Month	Units Day of Month
F	Tens of Months	Units of Months

FIGURE 2. RAM Memory Map

1.6 Comparator

A 46-bit comparator compares values in RAM against the counters to provide an alarm (compare) interrupt. When a compare occurs, the main interrupt will be activated if the D0 bit of the interrupt control register was set. The standby interrupt will be activated if a "1"was written to address 16 hex.

1.7 Interrupt Hardware

Interrupt hardware consists of two interrupt outputs. The main interrupt and the standby interrupt. The main interrupt is an active high push-pull output. The standby interrupt is an active low open drain output. For the main interrupt, an 8-bit control register allows the user to select from 1 to 7 interrupt rates, as well as an alarm. An 8-bit status register informs the user which of the 8 interrupts occurred. A one-bit control register enables/disables the standby interrupt. The standby interrupt is activated only for the alarm condition. A 46-bit comparator matches the timekeeping counters against RAM for the alarm interrupt.

1.8 Input/Output and Control Lines

The input/output structure consists of a 5-bit address bus and 8-bit bidirectional data bus. The control lines are chip select, power down, read and write. In addition, a ready output is provided for those microprocessors that have wait-state capability and meet the timing requirements of the ready signal. The power down input acts as a chip select of opposite polarity. It differs from the chip select in that it TRI-STATES the main interrupt output while the chip select does not TRI-STATE the interrupt. The power down input is intended to facilitate deselecting the chip for battery backed operation. Chip select, read and write are active low controls. The ready output is active low open drain and is caused by chip select and the negative-going-edge of read or write (it is an internal one-shot). If the ready output is not used as a control line when interfacing to a microprocessor, it may be left open circuit.

Detail Descriptions

OSCILLATOR

Figure 3 represents the internal and external circuitry that comprise the oscillator. The inverter, which is the heart of the oscillator, is designed to consume minimum power. The inverter has a typical gain of 30 at 1 kHz and 4 at 30 kHz. The oscillator input may be driven from an external source. If this is desired, the input should swing rail-to-rail and be approximately a 50% duty cycle. The oscillator output pin is open circuit for this case. The external oscillator circuit may be constructed using a CMOS inverter, N-FET, or a transistor (see *Figure 4*). Referring to *Figure 3*, the external 20 MΩ resistor biases the inverter in its active region. The internal feedback resistor may be too large in value to guarantee reliable biasing.

The external series resistor is to protect the crystal from being overdriven and possibly damaged. Manufacturers of these crystals specify maximum power that the crystal can dissipate. It is this rating which determines what value of series resistor should be used. The two external capacitors are effectively in series with each other (from an A.C. viewpoint). This total value comprises the load capacitance (typically 9 to 13 picofarad) specified by the crystal manufacturer at the crystal's oscillating frequency. The rule of thumb in choosing these capacitors is:

$$1/\text{load capacitance} = 1/C1 + 1/C2$$

C2 is greater than C1 (typically two to four times)

C1 is usually trimmed to obtain the 32768 Hertz frequency.

The start-up time of this oscillator may vary from two to seven seconds (empirical observation) and is due to the high "Q" of the crystal. Typical waveform values monitored at the oscillator output are observed to be 3 volts peak to peak riding on a 2.5 volt D.C. level (for V+ = 5 volts).

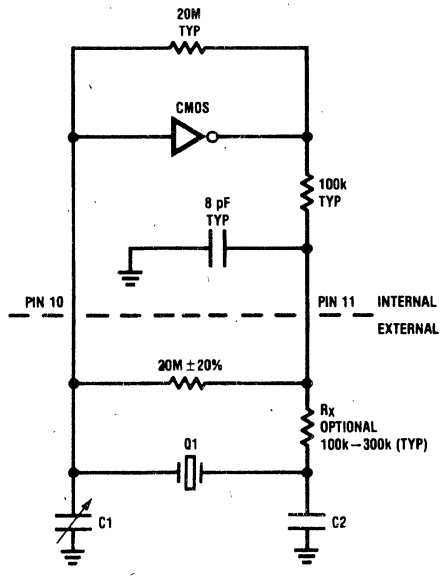
CHOOSING THE CRYSTAL

The below parameters describe the crystal to be used

Parallel Resonant, tuning fork (N cut) or XY Bar

Q> = 35,000

Load Capacitance (CL)	9 to 13 Picofarad
Power Rating	20 Microwatt Max.
Accuracy	User Choice
Temperature Coefficient	User Choice



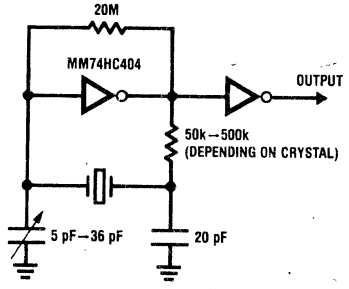
Q1 = 32,768 Hz

Mnfg.	Tel. #
RCD	800-228-8108
Saronix	415-856-6900
Reeves-Hoffman	717-243-5929

C1 = 5 → 30 pf
Circuit Specialists
Part # 275-0430-005
Tel. # 1-800-528-1417
Johanson #9613 or #9410-3 pc.
Tel. # 201-334-2676
C2 = 15 → 20 pf mica

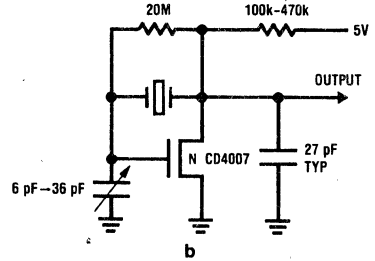
TL/B/5727–2

FIGURE 3. Oscillator Circuit and Recommended Connections



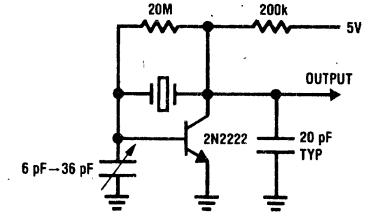
TL/B/5727–3

a



TL/B/5727–4

b



TL/B/5727–5

c

FIGURE 4. Examples of External OSC Circuits

Detail Descriptions (Continued)

When used with a crystal, the accuracy of the oscillator circuit over voltage and temperature is about +/− 10 PPM. Voltage variations cause about 50% of the inaccuracy and temperature variations account for the other half. This inaccuracy results in an error of about 5 minutes per year. Errors due to external components must be taken into account by the user. If an external oscillator is used, then it determines the accuracy of the clock. The oscillator input pin (pin 10), is a high impedance node that is susceptible to 'noise'. The usual result is the clock gains time at a high rate (on the order of seconds per hour or greater). This noise is usually the result of coupling from pin 9 which is a low order address bit if tied directly to a microprocessor bus. Suggestions to alleviate this condition are:

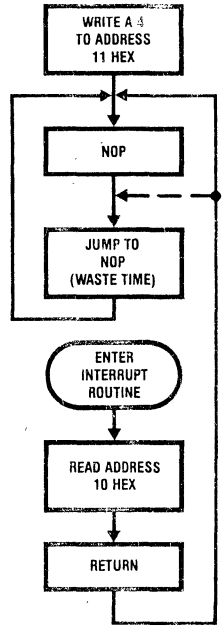
1. Gate pin 9 with chip select.
2. Use a slow rise and fall time non inverting buffer such as a CMOS to drive pin 9. If this choice is made, similar CMOS should drive the write and read strobes to avoid timing conflicts.
3. Use an external oscillator and drive pin 10 with a low impedance device (CMOS or transistor), leave pin 11 open circuit.
4. Connect all oscillator components as close as possible to pins 10 and 11.

CALIBRATION

To calibrate the oscillator three methods are suggested. The one second repetitive interrupt is activated. This is done by first connecting the interrupt (pin 13) of the clock to the interrupt of the microprocessor. Next a short program is written that sets bit D2 of the interrupt control register, and then enters a loop that wastes time while awaiting an interrupt. The interrupt service routine only needs to read the interrupt status register, which clears the interrupt, and then returns. The result is a 1 second periodic signal at pin 13.

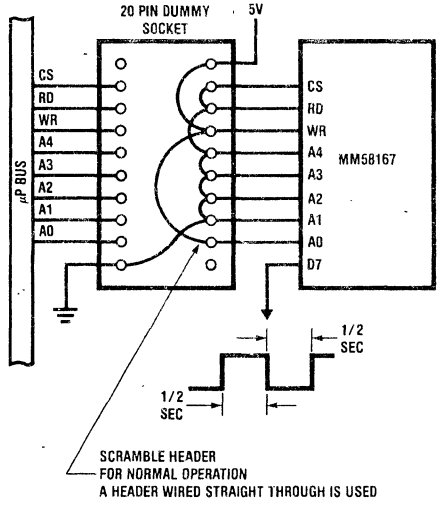
The flow chart of *Figure 5* is an example of the detail steps. A time event meter is used to measure the time interval between successive positive going edges of the interrupt output while adjusting the variable capacitor C1. This period will be 1 second when the oscillator is at 32,768 Hertz. The second method is to monitor the most significant bit (D7) of counter 1, while statically reading. A static read is performed by connecting chip select and read low, and applying the address of the selected counter. Refer to *Figure 6* for detail. The period of this output is one second if the oscillator is exact at 32,768 Hertz. The adjustment procedure is the same as for the first method.

A third method is to monitor D0 of the seconds counter (addr 2) while statically reading. The D0 output presents a



TL/B/5727-6

FIGURE 5. Flow Chart for Calibration Using the 1 Hz Repetitive Interrupt



TL/B/5727-7

FIGURE 6. Hardware to Achieve a Static Read of Address 1

Detail Descriptions (Continued)

square wave that is one second high, one second low when the oscillator is at 32,768 Hertz. Refer to *Figure 7* for static read hardware. If the 32,768 Hertz is to be measured directly, then a HI impedance LO capacitance amplifier or comparator or CMOS gate should be connected to the oscillator output pin to prevent the measuring instrument from offsetting the frequency of the oscillator. This addition is permanently a part of the oscillator circuit and must be battery backed if the clock is battery backed. The reason for battery backing this buffer is to ensure that its input impedance does not change during the power down operation which could result in the oscillator stopping or being offset in frequency.

PRESCALER OPERATION

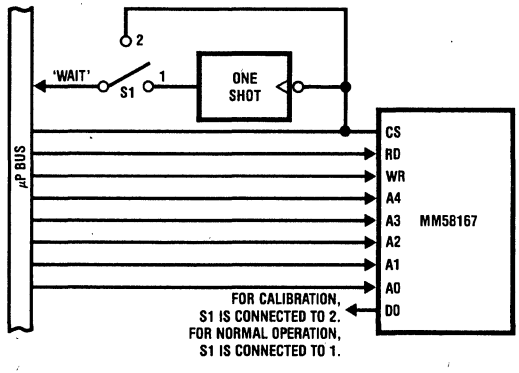
The 32,768 Hertz signal is divided to an even 32,000 Hertz using pulse swallowing techniques. This is accomplished by dropping three pulses every 128 counts of the 32,768 Hertz signal. The resulting 32 kHz is then divided to produce 1 kHz which is the internal incrementer for the rest of the timekeeper. This 1 kHz waveform is nonmonotonic with respect to individual periods. As a result, there are 750 short and 250 long periods within a one second interval.

The short period is 1/1024 seconds, and the long period is [1/1024 + 3/32768] seconds. As a result, the milliseconds, hundredths and tenths of seconds "jitter". The inaccuracy on an individual period basis is about 91 microseconds. The period and number of clock edges are correct over one second within the accuracy of the crystal oscillator. The ten thousandths of seconds counter referred to in the data sheet counts milliseconds. The 1 second and slower signals are jitter free. Refer to *Figure 8* for counter block diagram.

TIMEKEEPING COUNTERS

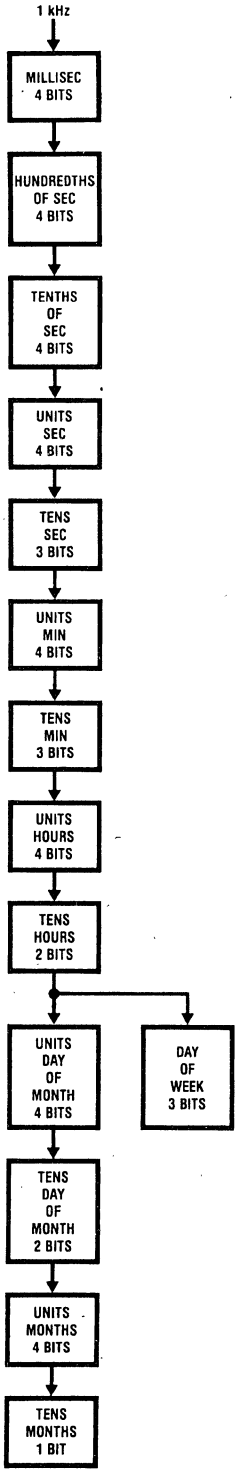
The timekeeping counters are intended to work with valid BCD values. In general, if illegal codes are entered then no guarantee is given for recovery. As shown in *Figure 8*, the timekeeping stages are arranged as a ripple counter. The month, day of month, and day of week counters count 1 through N. The milliseconds through hours counters count 0 through N. The rollover of a counter stage increments the next higher order counter. This rollover takes place when the highest allowed value plus one is decoded. For example, in a 30-day month, the day of month counter would decode the value 31, reset to one and increment the month counter. If the highest allowed value plus one is written to a counter, the counter will reset when the write is removed and "may" increment the next higher order counter.

For example, if February 29 is written to the clock, the read back will be a "1" in the day of month counter and the month may read "3". However, for leap year use, February 31 may be written. If this is done on Mar 1 at 0 (hours through milliseconds), then the clock will read March 1 after 24 hours. In this way, the value Feb 31 could be used as an indication that the date is really Feb 29. Refer to *Figures 9A 9B,* and *9C* for flowcharts of a program and alarm interrupt bit map that take leap year into account. Note that the software implemented leap year counter is accurate at least through the year 2048. For a perpetual calendar, a more sophisticated algorithm would be needed.



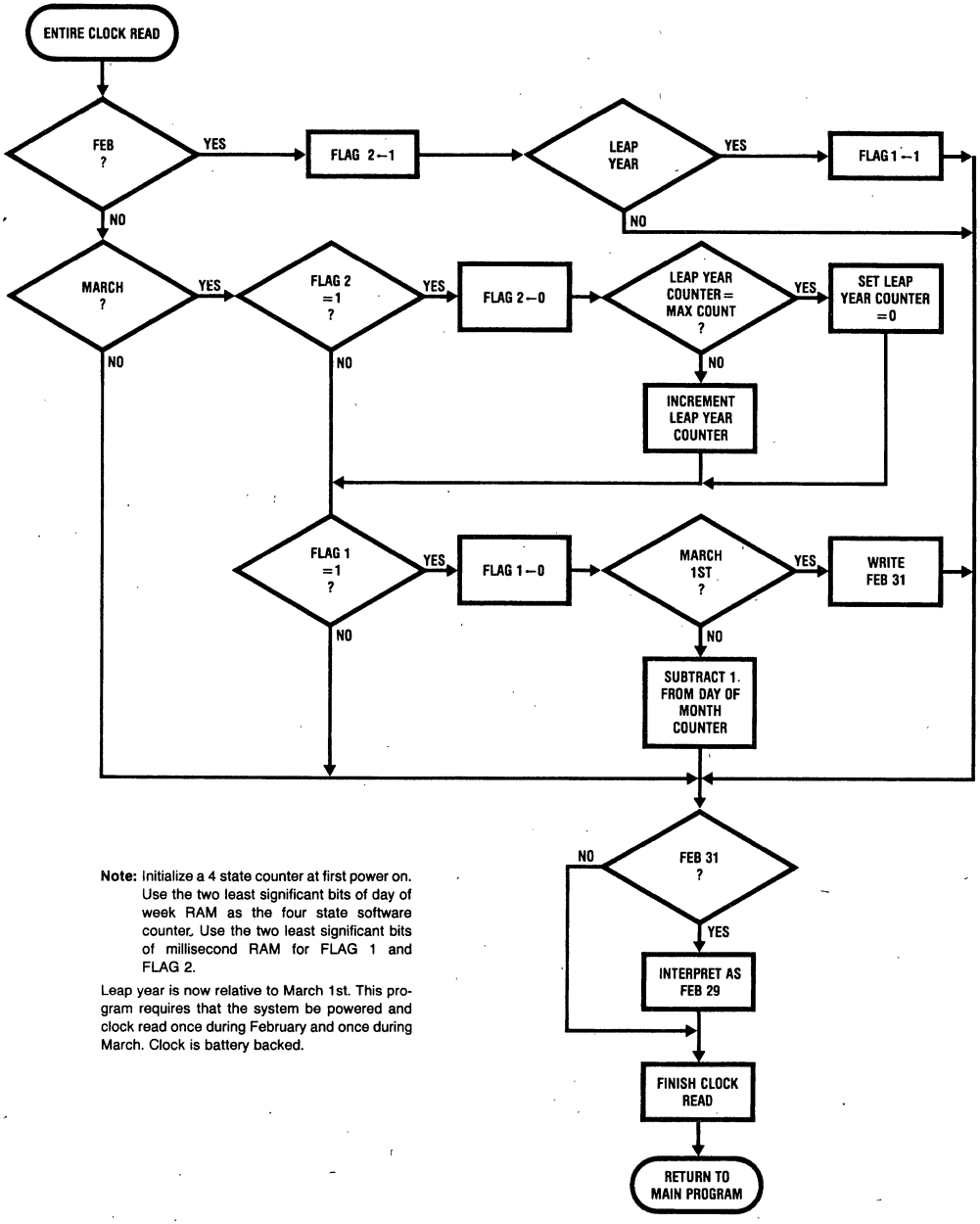
TL/B/5727–8

FIGURE 7. Static Read Hardware Where Up Has External Wait State Capability



TL/B/5727–9

FIGURE 8. BCD Timekeeping Counters

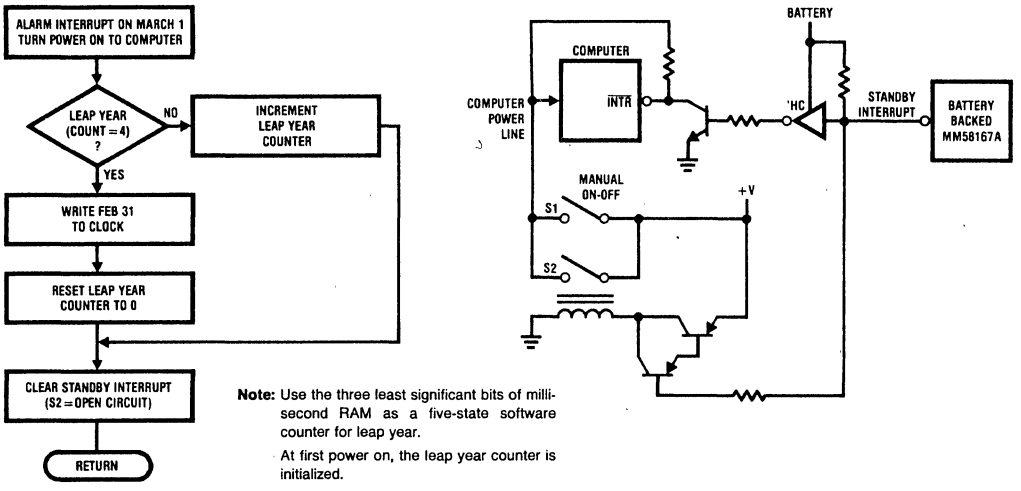


Note: Initialize a 4 state counter at first power on. Use the two least significant bits of day of week RAM as the four state software counter. Use the two least significant bits of millisecond RAM for FLAG 1 and FLAG 2.

Leap year is now relative to March 1st. This program requires that the system be powered and clock read once during February and once during March. Clock is battery backed.

TL/B/5727–10

FIGURE 9A. Leap Year Flow Chart



Note: Use the three least significant bits of milli-second RAM as a five-state software counter for leap year.

At first power on, the leap year counter is initialized.

TL/B/5727–11

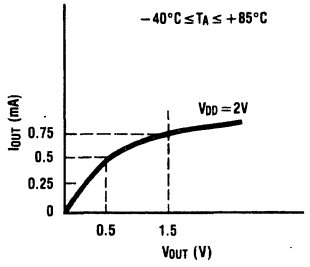
FIGURE 9B. Leap Year Flow Chart and Hardware

Function	Address					DATA							
						Hi Nibble				Lo Nibble			
	4	3	2	1	0	7	6	5	4	3	2	1	0
Milliseconds	0	1	0	0	0	0	0	0	0	No RAM Exists			
Hundredths and Tenths of Seconds	0	1	0	0	1	0	0	0	0	0	0	0	0
Seconds	0	1	0	1	0	0	0	0	0	0	0	0	0
Minutes	0	1	0	1	1	0	0	0	0	0	0	0	0
Hours	0	1	1	0	0	0	0	0	0	0	0	0	0
Day of Week	0	1	1	0	1	No RAM Exists				1	1	X	X
Day of Month	0	1	1	1	0	0	0	0	0	0	0	0	1
Months	0	1	1	1	1	0	0	0	0	0	0	1	1

FIGURE 9C. Clock RAM Bit Map For Alarm Interrupt on March 1@ 0 Hrs

INTERRUPTS

The 58167 has two interrupt output pins. The main interrupt (pin 13) is active "high", and is active when the power down pin is "high". When power down (pin 23) is low, the main interrupt output is TRI-STATED. The second interrupt is the "standby interrupt" and is an active low open drain requiring a pull up resistor to VDD. This interrupt is always powered. Refer to *Figure 10* for typical sink current versus voltage out characteristics. Separate control bits exist for the two interrupts. The main interrupt offers two modes of operation which may be combined. Mode 1 is the interactive repetitive interrupt. For this case, a logic 1 is written to one or more bits in the control register (address 11 hex) from D1 through D7, a logic 0 is written into the D0 position. Refer to *Figure 11* for bit configuration of the interrupt control and status registers.



TL/B/5727-12

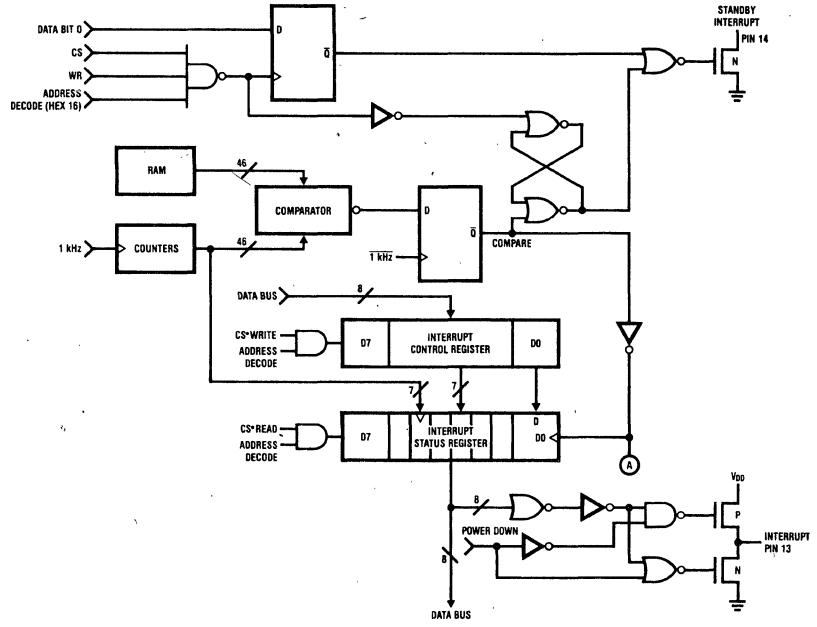
FIGURE 10. Typical Curve of I vs V of Standby Interrupt

As a result, the clock chip provides an interactive repetitive interrupt, that occurs when the selected counter rolls over. That is, the user must clear the interrupt so the next one can be recognized. This is done by reading the interrupt status register (address 10 hex). This read results in the user obtaining the interrupt status (which interrupt occurred) and the clearing of the interrupt output as well as the status register. It is the positive-going-edge of the read strobe which causes the preceding. This clearing action precludes polling the status register. For precision timing, the positive-going-edge of the repetitive interrupt should be used as a trigger. The one-per-second through one-per-month repetitive interrupts will be as accurate as the setting of the crystal oscillator. The ten-per-second interrupt will be accurate to about 91 microseconds. Refer to prescaler description for more detail.

The second mode of main interrupt is the "compare" or "alarm". In this case, a specific value is entered in the RAM of the clock. When the time keeping counter(s) match that value, the interrupt becomes active. Refer to *Figure 13* for a typical example. *Figures 11* and *12* show internal interrupt logic and waveforms. In addition to a specific one time interrupt (alarm), a repetitive interrupt can be achieved by reprogramming the selected RAM location with a future event value. The rule of thumb for an "alarm" interrupt is: All nibbles of higher order than specified are set to C hex (always compare). All nibbles lower than specified are set to "zero".

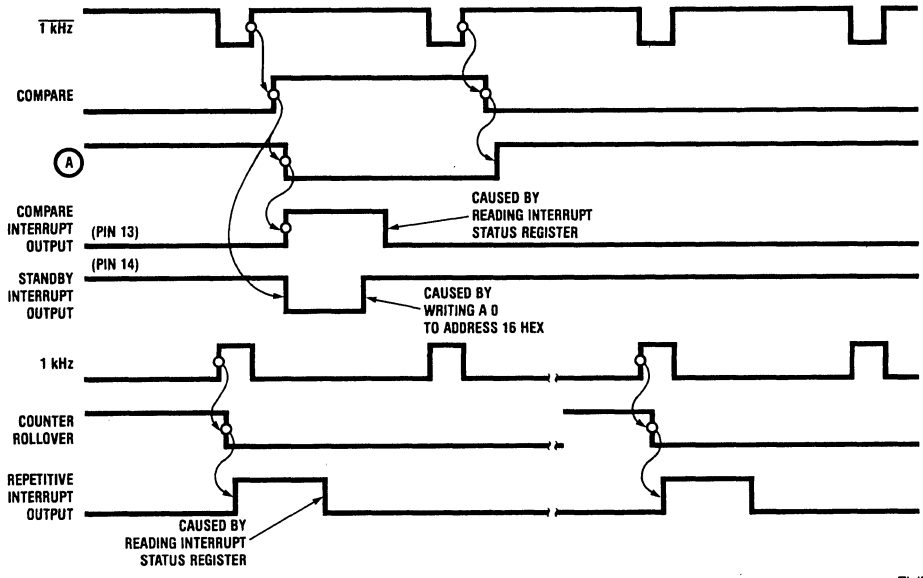
A programming example of the fastest interrupt rate obtainable (500 per second) is given in *Figure 14*. This program written in NSC800 code (Z80) sets "always compare" conditions (CC hex) in RAM locations 9 through C, E and F. RAM location D which corresponds to the day of the week counter (a single digit), is set to C. RAM location 8 is set to 0. When the first interrupt occurs, the service routine reads the status register and sets the value 2 into RAM location 8. At succeeding interrupts, the values 4, 6, 8 are set into location 8 and the sequence repeats.

If an interrupt is activated and the interrupt occurs during battery backed operation (power down), the main interrupt output will be active high when system power returns.



TL/B/5727-13

FIGURE 11. Interrupt Registers and Logic



TL/B/5727–14

FIGURE 12. Internal Interrupt Timing

Function	Address					DATA							
						Hi Nibble				Lo Nibble			
	4	3	2	1	0	7	6	5	4	3	2	1	0
Milliseconds	0	1	0	0	0	0	0	0	0	No RAM Exists			
Hundredths and Tenths of Seconds	0	1	0	0	1	0	0	0	0	0	0	0	0
Seconds	0	1	0	1	0	0	0	0	0	0	0	0	0
Minutes	0	1	0	1	1	0	0	1	0	0	0	1	0
Hours	0	1	1	0	0	0	0	0	1	0	0	0	0
Day of Week	0	1	1	0	1	No RAM Exists				1	1	X	X
Day of Month	0	1	1	1	0	1	1	X	X	1	1	X	X
Months	0	1	1	1	1	1	1	X	X	1	1	X	X

FIGURE 13. Ram Mapping for Alarm Interrupt at 10:22:00 Every Day

```
                NAME ('I500Hz')
                TITLE 58167 500HZ REPETITIVE INTERRUPT (10/13/83)

                ;THIS PROGRAM IS FOR USE WITH THE 58167 POWER DOWN BOARD
                ;INTERFACED TO THE NSC888 BOARD. CODE IS NSC800.
                ;A 500HZ SIGNAL IS GENERATED AT THE INTERRUPT PIN (13).
                ;THIS SIGNAL IS GENERATED USING THE COMPARE INTERRUPT
                ;AND UPDATING THE ''RAM'' FOR THE NEXT INTERRUPT


                                        ORG 0800H

4092                            RESET EQU 04092H
4091                            CONT  EQU 04091H
4090                            STAT  EQU 04090H
408F                            MON   EQU 0408FH
408E                            DOM   EQU 0408EH
408D                            DOW   EQU 0408DH
408C                            HRS   EQU 0408CH
408B                            MIN   EQU 0408BH
408A                            SEC   EQU 0408AH
4089                            HT    EQU 04089H
4088                            MIL   EQU 04088H
101C                            VEC1  EQU 0101CH
101D                            VEC2  EQU 0101DH


0800'  3E 00                    INIT:   LD      A,0             ;SET UP INTRPT FOR NSC888
0802'  32 101C                          LD      (VEC1),A        ;          *
0805'  3E 09                            LD      A,009H          ;          *
0807'  32 101D                          LD      (VEC2),A        ;          *
080A'  3E 08                            LD      A,8             ;          *
080C'  D3 BB                            OUT     (0BBH),A        ;          *
080E'  31 1FFF                          LD      SP,01FFFH       ;INIT STACK POINTER
0811'  3E FF                            LD      A,0FFH
0813'  32 4092                          LD      (Reset),A       ;RESET ALL CLOCK COUNTERS
0816'  3E 00                            LD      A,0
0818'  32 4091                          LD      (CONT),A        ;CLEAR INTRPT CONTROL
081B'  3A 4090                          LD      A,(STAT)        ;CLEAR ANY PENDING INTRPT
081E'  3E CC                            LD      A,0CCH          ;SET RAM FOR INTRPT
0820'  32 408F                          LD      (MON),A
0823'  32 408E                          LD      (DOM),A
0826'  32 408D                          LD      (DOW),A
0829'  32 408C                          LD      (HRS),A
082C'  32 408B                          LD      (MIN),A
082F'  32 408A                          LD      (SEC),A
0832'  32 4089                          LD      (HT),A
0835'  3E 00                            LD      A,0
0837'  32 4088                          LD      (MIL),A
083A'  3E 01                            LD      A,1
083C'  32 4091                          LD      (CONT), A       ;SET COMPARE INTRPT
083E'  FB                               EI
0840'  00                       NOP:    NOP
0841'  C3 0840                         JP      NOP             ;WASTE TIME AWAITING
                                                                ;INTERRUPT
                                ;INTERRUPT SERVICE ROUTINE GETS THE VALUE IN THE
                                ;MILLISECOND RAM, TEST FOR 8. IF YES THEN SET RAM
                                ;EQUAL TO 0, CLEAR INTERRUPT AND RETURN.
                                ;IF NO, ADD 2 TO RAM MILLISECOND,
                                ;CLEAR INTERRUPT AND RETURN.
                                ;''REMEMBER'' RAM MILLISECONDS IS ''HIGH'' ORDER NIBBLE
                                ;ONLY

                                        ORG 0900H

0900'  3A 4088                  ZERO:   LD      A,(MIL)         ;GET RAM MILLSEC
0903'  E6 F0                            AND     0F0H            ;MASK
0905'  FE 80                            CP      080H            ;? RAM=8
0907'  CA 0912'                         JP      Z,ZERO
090A'  C6 20                            ADD     A,020H
090C'  32 4088                          LD      (MIL),A
090F'  C3 0917'                         JP      RETRN
0912'  3E 00                            LD      A,0
0914'  32 4088                          LD      (MIL),A
0917'  3A 4090                  RETRN:  LD      A,(STAT)        ;CLEAR INTRPT
091A'  FB                               EI
091B'  C9                               RET

                                                END
```

FIGURE 14. NSC800 Assembly Code for 500 Hz Interrupt

STANDBY INTERRUPT

A "1" written to address 16 hex enables the standby interrupt and a "0" disables it. This interrupt also becomes active when a match exists between time keeping counter(s) and a value written into RAM. The standby interrupt can be cleared as soon as it is recognized. The user should ensure that a delay of one millisecond or greater exists prior to reenabling the standby interrupt. This delay is necessary because of the internal signal level which causes the interrupt. If this delay does not occur, then the standby interrupt becomes reactivated until the internal latched compare goes away, which occurs at the next 1 kHz clock. *Figure 12* illustrates interrupt timing.

RAM

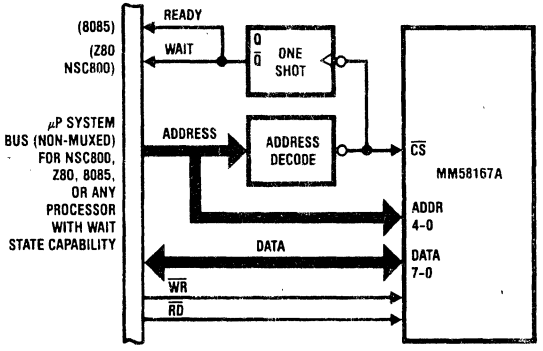
RAM is organized as shown in *Figure 2*. There are 4 bits of RAM for each BCD counter. The RAM may be used as general purpose or for an alarm interrupt. It is possible under certain conditions to perform the compare interrupt and use selected bits of the RAM for general purpose storage. Any RAM position that is set for the 'always compare' condition allows the user to manipulate the 2 LO order bits in each nibble. However, the 2 high order bits in each nibble position must be maintained as logic 1'S. For example, the user may have an alarm interrupt that does not use the day of the week as a condition for interrupt. Therefore the 2 low order bits might be used as a 4 state software counter to keep track of leap year. Reading and writing the RAM is the same as any standard RAM.

HARDWARE INTERFACE CONSIDERATIONS

There are four basic methods of interfacing the 58167A to a microprocessor. They are memory mapped, microprocessor ports (for single chip microprocessors like the 8048), peripheral adapter, and separate latches. The advantage of memory mapped interface is use of all memory reference instructions. The disadvantages are the processor may need to be "wait-stated" and the environment is noisier with respect to the crystal oscillator. Refer to *Figure 15* for typical bus interface.

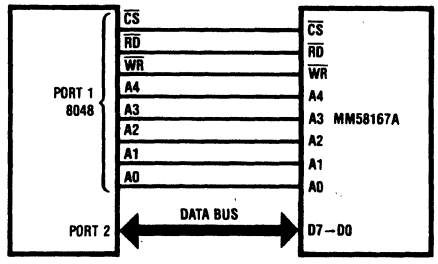
Microprocessors that have separate ports (16 are sufficient) offer the capability to interface directly without "wait-stating", or additional device count. Eight of the port bits (data) need to be bidirectional for this interface. *Figure 16* indicates port interface. Programmable peripheral interface devices such as the 8255A or NSC810 afford the user the advantage of timing control by data bit manipulation, as well as a less noisy environment with respect to the oscillator circuit. *Figure 17* depicts the 8255A and NSC810 interface.

External latches may be used in place of the programmable peripheral interface device. This results in higher package count but easier troubleshooting. Also, the latches do not have to be manipulated through a control register. *Figure 18* illustrates the external latch approach. For the peripheral approaches, address, data, chip select, read and write strobes are manipulated by controlling the data bus bits via program execution. The peripheral interface approach facilitates calibration of the oscillator because the chip select, read strobe, and address lines can be set to steady state logic levels. Refer to calibration techniques for more detail.



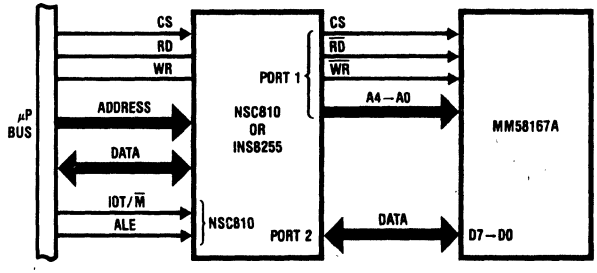
TL/B/5727–15

FIGURE 15. Typical μP Bus Interface



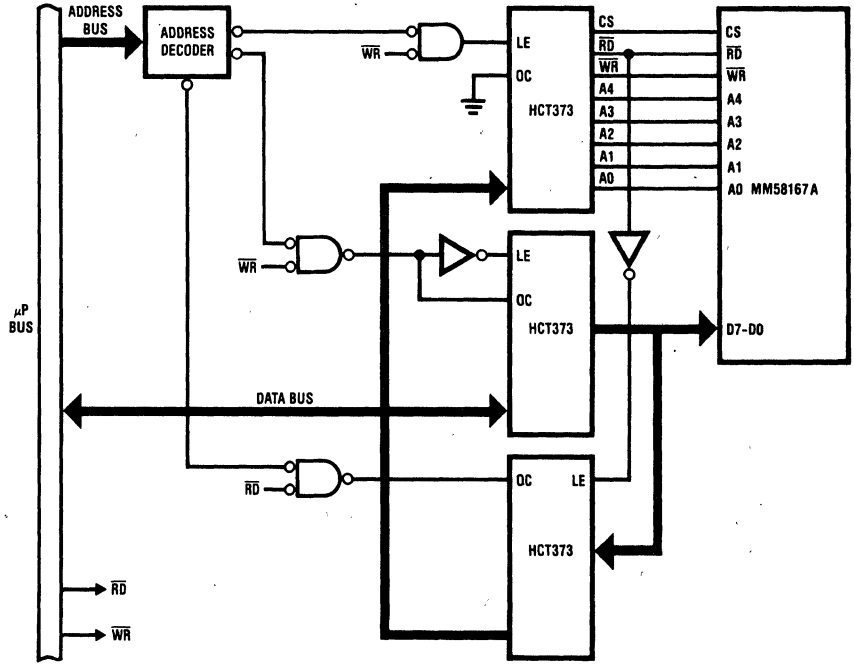
TL/B/5727–16

FIGURE 16. MM58167A Interfaced to Single Chip Microcomputer



TL/B/5727–17

FIGURE 17. MM58167A Interfaced to μP Through Peripheral Adapter



TL/B/5727–18

FIGURE 18. MM58167A Interfaced to μp Using TRI-STATE Latches

POWER DOWN/BATTERY BACKED CONSIDERATIONS

Battery back up of the clock may be considered by the user to maintain time during power failure, provide a "wake-up" alarm, save the time that power failure occurred, calculate how long power failure lasted. The first step in providing a battery backed system is to isolate the system supply from the battery. This is to ensure that the battery is not discharged by the system supply when power failure occurs. *Figure 19* shows two techniques to achieve isolation. *Figure 19A* is implemented using diodes to isolate. In one case a Schottky diode is used to guarantee minimum voltage drop loss, while in the other case an adjustable voltage regulator (LM317) is used from a higher voltage and regulated to about 5.7 volts. A 1N914 diode in series with the regulator achieves the 5 volts for the clock. The Schottky diode has a drop of about 0.3 volts. Thus the V+ of the clock is typically at 4.7 volts. The user must be cautious about input signals not exceeding the 4.7 volt V+, since the clock is a CMOS device. This situation could arise if the devices driving the inputs of the clock were CMOS and received power from the 5 volt system supply. *Figure 19B* makes use of the low saturation of a PNP transistor (0.1 volt) to take care of the above situation. The NPN transistor is used to achieve isolation. The zener diode ensures that the circuit stops conducting and appears open circuit before the battery switches in.

Some basic considerations must be adhered to in a power down situation where the real time clock is battey backed. One is to ensure no spurious write strobes accompanied by a chip select occur during power down or power up. Another is to guarantee the system is stable when selecting/deselecting the clock. Also, any legitimate write-in-progress should be completed. To accomplish this, hardware is implemented such that early power failure is detected (usually a comparator detects DC failure, a retriggerable one-shot detects AC failure) See *Figures 20* and *21*. At this point the clock chip is deselected. The worst case is the power fails faster than the detection circuit can cause deselection. When power returns, the hardware detects power on, but the system must be stable before communication is allowed with the real-time-clock.

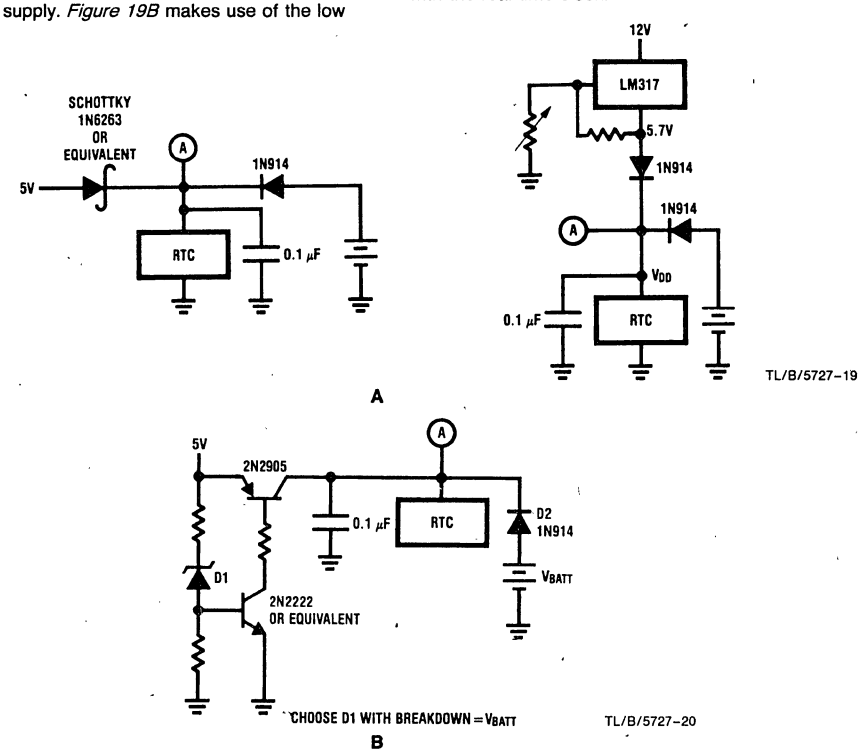


FIGURE 19. Isolating System Supply from Battery

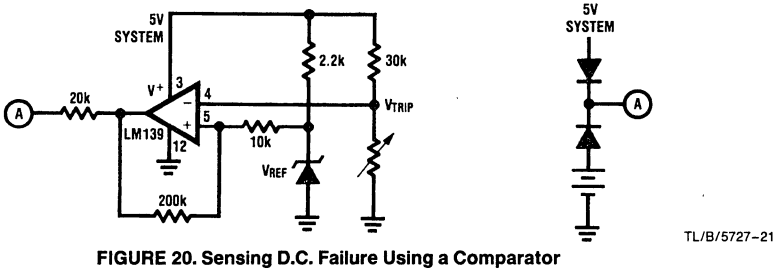


FIGURE 20. Sensing D.C. Failure Using a Comparator

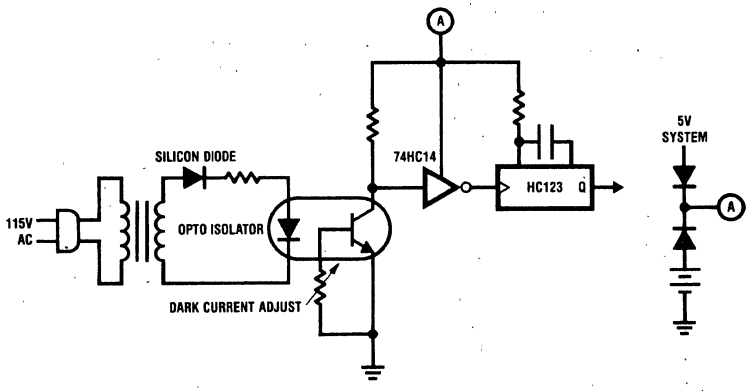


FIGURE 21. Sensing AC Line Failure Using Retriggerable One Shot

The 5-volt system supply rise and fall time characteristics during power turn on and power failure must be known. Care should be taken to allow a legitimate write in progress to be completed. This is necessary because a "short write" could cause erroneous data to be entered to the clock. If the clock is used as a "read only" device (except for initialization of calendar and time), the circuitry to allow a write in progress to be completed does not have to be considered. For this situation, a switch in series with the write strobe could be implemented such that the write line to the clock is "tied high" after initialization.

To sense system DC power failure a comparator and voltage reference may be used. *Figure 22*, detail 1, shows the comparator and voltage reference configured such that the comparator output is "low" when 5-volt system power is greater than 4.6 volts. If possible, the power fail trip point should be referenced to a lightly loaded (fast collapse) DC supply, preferably higher than the 5-volt system. This would allow early sense of power failure. When using comparators, the output may oscillate as the trip point is approached. The oscillation is caused by noise on the DC line appearing at the input to the comparator when at or near the trip voltage. The cleaner the supply, the less chance of oscillation. In all cases, hysteresis should be used to minimize oscillations. Note that the 20 kohm pull-up resistor is connected to the battery backed node, while the LM139 V+ pin is connected to the 5-volt system supply. Used this way, the comparator does not draw any current except leakage from the battery and the output remains high during power down.

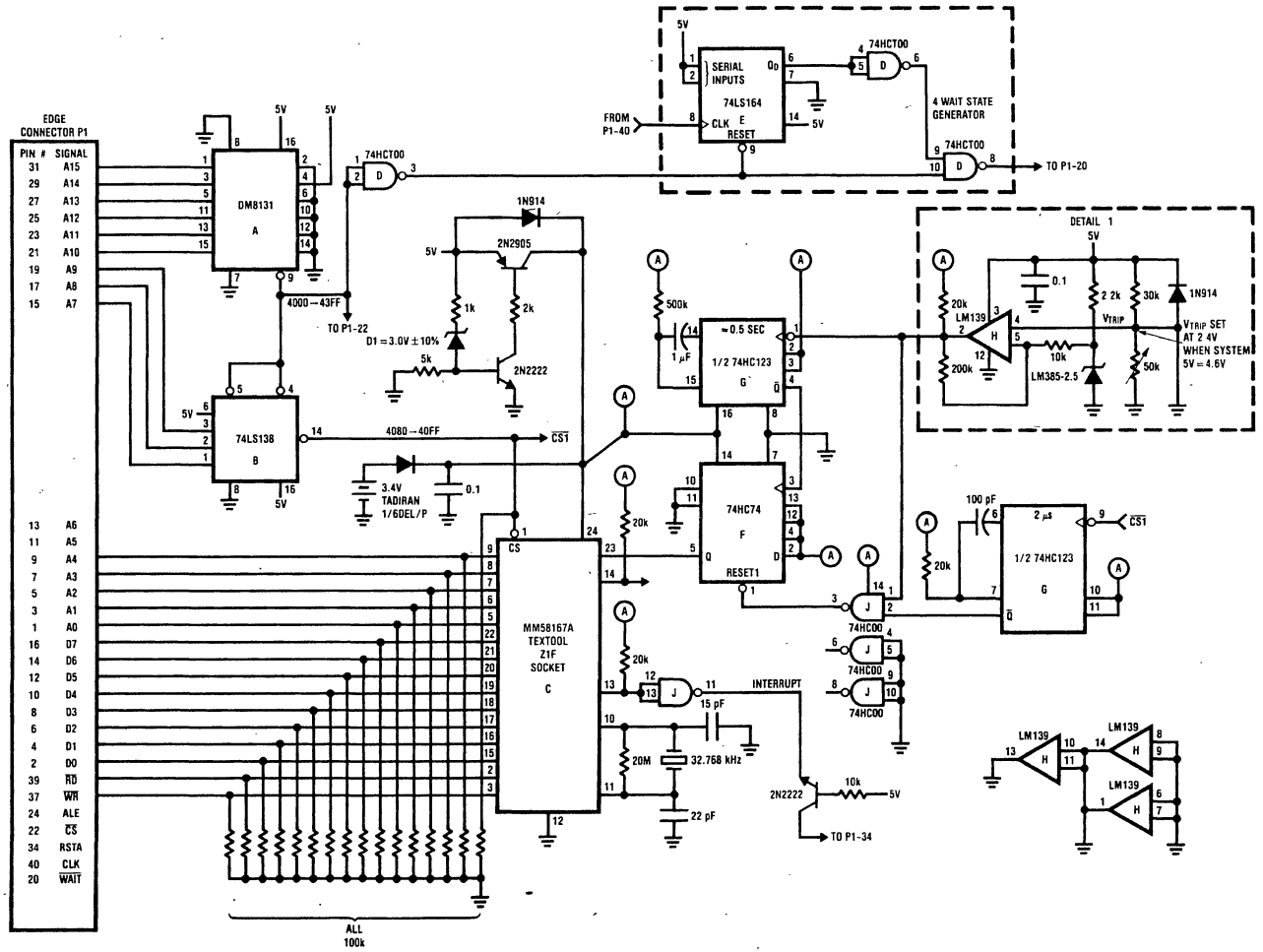
To sense AC failure, a retriggerable one-shot may be used. The RC time out may be adjusted to allow for one or more cycles of 60 Hertz to be missed. Using this approach, the Q output of the one-shot is always high while 60 Hertz is present. When a cycle is missed the one-shot times out and Q goes low. *Figure 21* shows AC sensing. This technique could cause a spurious deselect of the clock if a "glitch" occurs on the AC line resulting in a missed cycle.

For this application, the circuit shown in *Figure 22* was implemented. The MM58167A was interfaced to the NSC800 in memory mapped locations. A demo program was written to exercise the clock, and display time, date and calendar. Power was switched on and off at irregular intervals, to test the battery backed circuitry. The results were that the clock kept correct time. Battery backed current for all circuitry was 10 microamp. For general consideration, this circuitry allows a chip select in progress to be completed.

FUNCTIONAL OPERATION OF *FIGURE 22*

Power up sequencing consists of the LM139 (comparator) making a high to low transition when the 5-volt system supply exceeds 4.6 volts. This transition triggers the 0.5 second one-shot causing its output to be low and removes the low reset on the D flip-flop through nand gate J. The output of the 2 microsecond one-shot is "don't care" once the comparator switches from high to low. After 0.5 seconds, the system is assumed to be stable, and the D flip-flop output which was reset is clocked high by the low to high transition of the 0.5 second one-shot. Thus, the clock chip is enabled allowing normal communication with the microprocessor.

The power down sequence consists of the comparator making a low to high transition when the 5-volt supply is less than 4.6 volts. If no chip select is present, the D flip-flop is reset through nand gate J, causing pin 23 of the clock to be low (deselected). If a legitimate chip select was in progress, the reset action through nand gate J would be delayed by the low level of the 2-microsecond one-shot.



TL/B/5727–23

FIGURE 22. Detailed Schematic of Power Down Circuitry, and Interface to NSC888 Board

A wait state generator was implemented using the chip select as the sensing signal. This was necessary to comply with NSC800 wait state timing. The wait generator provides 2 microseconds of access time, which is more than adequate to meet clock chip timing requirements. Pull-down resistors were added to all clock input pins to guarantee no floating inputs during power down. This ensures that the CMOS clock does not draw excessive current from the battery during power down. A diode isolates 5-volt system from the battery (A 3.4-volt Tadiran nonrechargeable lithium cell was used in this application). The battery is isolated from the 5-volt supply using a circuit comprised of PNP and NPN transistors along with a zener diode. The zener diode value was selected such that the combined voltage drop of the zener and the base emitter of the NPN transistor was greater than the battery voltage. This ensures no current will be drawn from the battery by the 5-volt supply when power failure occurs.

The battery is non rechargeable, but allows up to 10 microamps of charge current without damaging the cell. An LM139 voltage comparator and LM385-2.5 voltage reference were used to sense the 5-volt system supply. The trip point was adjusted such that when the 5-volt supply dropped to 4.6 volts, the comparator switched from low to high. Observation of the comparator output showed oscillation, but caused no malfunction. The duration of the oscillation was about 100 microseconds. Burst noise on the 5-volt supply was about 0.5 volts peak to peak. For the circuitry implemented, the 5-volt supply should fall no faster than 1 volt per millisecond. This rate allows 100 microseconds for deselect to take place while the supply is falling from 4.6 volts to 4.5 volts. Thus, deselect occurs while the system is stable.

Miscellaneous

TEST MODE

The test mode applies the oscillator output to the input of the millisecond counter. This affords faster testing of the chip. This mode is intended for factory testing, where a programmable pulse generator is used. A pulse rate of 50 kHz may be used in this mode. The pulse should swing rail to rail and be a square wave. Apply the pulses to the oscillator input pin, leaving the oscillator output pin open circuit. The basic sequence would be to write values to the counters, enter test mode and apply a known number of pulses. Next, read the counters using normal read sequence.

GO COMMAND

A write to address 15 hex (data is a "don't care") will clear the seconds through milliseconds counters. If the value in the seconds counter is equal to or greater than 40 when the GO command is executed, then the minute counter will be incremented.

REST COMMAND

Writing the value FF hex to address 12 hex causes the hours through milliseconds counters to be reset to zero. The day of week, day of month, and month counters are set to 1.

Writing the value FF hex to address 13 hex causes the RAM to be cleared.

GENERAL TIMING CONSIDERATIONS:

To guarantee a valid read/write without using the ready output, the following criteria must be met.

Read Operation

1. Address setup before RD = 100 ns min
2. CS to RD = 0 min
3. Read strobe width = 950 ns min
4. Address hold after read = 50 ns min

Write Operation

1. Address setup before WR = 100 ns min
2. CS to WR = 0 ns min
3. WR and data must be coincident for 950 ns min
4. Data hold after WR = 110 ns min
5. Address hold after WR = 50 ns min

If the ready output is used to guarantee read write operation, then the following recommendations are made. Referencing the April 1982 data sheet, during a read, the ready line makes its positive transition 100 nanoseconds before data is valid. (Not shown in the data sheet). The user should not use this signal to latch data into an external latch. If this signal is used to wait state a microprocessor, then a critical examination of the microprocessor timing with respect to when it terminates its wait stated cycle must be made. This examination must also include any set-up time the processor needs prior to reading data. Also, note that the ready output (per the data sheet) negative-going-edge occurs 150 nanoseconds after the read or write strobe has gone low. Check microprocessor timing to ensure that the ready signal would be recognized as a "wait-signal".

It is not advised to perform sequential reading by connecting chip select and read low and cycling through the counters by changing address lines. The reason is that it is possible to cause an internal latch to "flip," the result being an error in timekeeping.

SOFTWARE CONSIDERATIONS

Reading the Counters

A read of one counter plus the rollover status bit or all the counters plus the rollover bit must be done within 800 microseconds. If the rollover status bit is a "1" then a complete read of counter(s) must be performed again. The 800 microsecond value is conservative. If the time between the read of any counter(s) and the rollover status bit exceeds 800 microseconds, then the status bit will always be set. The order of reading must be counter(s) first, then rollover status bit. This is because the positive going edge of the read strobe clears the status bit. Refer to *Figure 23.* The status bit is enabled for a period of 150 microsecond maximum at a rate of 1 kHz. If during this 150 microsecond period a counter(s) read occurs, the status bit will be set. This is true no matter how often the rollover status is read during that time period. Each rollover status read resets the status bit, but any counter read within the 150 microsecond period will set the rollover status bit. If the counters are read after a repetitive interrupt, then allow 150 microseconds (conservative) from the sense of the interrupt to the read of the counters (ripple delay time) and the data will be valid. If the counters are read after a compare interrupt, the read can occur immediately and will be valid.

Writing the Counters

The counters may be written to in any order, because the write overrides the internal increment. If it is desired to write all the counters without increments occurring in between writes, then the complete write operation must be performed within 800 microseconds. As long as valid BCD values (with respect to the specific counter) are written, no other counter is affected by the write. In general, writing the high order to low order counters is the conservative approach. This method is less susceptible to increments between writes for cases where the writing takes greater than 800 microseconds. For initialization of time, if the "GO" command is issued prior to any write, then 10 milliseconds are available to write from months through tenths and hundredths of seconds without any effect due to internal incrementing.

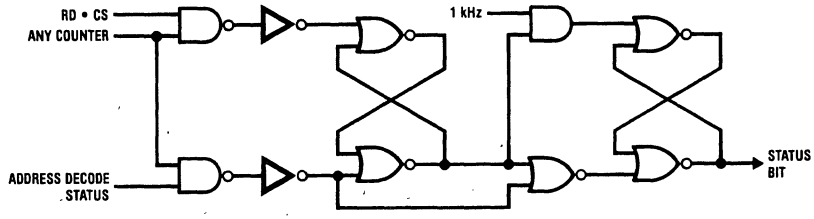
BIBLIOGRAPHY

MM58167A Microprocessor Real Time Clock Data Sheet April 1982.

"Crystal Oscillator Design And Temperature Compensation" By Marvin E. Frerking.

National Semiconductor Application Note AN-313 D.C. Electrical Characterization Of High Speed CMOS Logic.

LM-139 Quad Voltage Comparator Data Sheet.



TL/B/5727–25

FIGURE 23. Rollover Status Bit Logic

The MM58174A Real Time Clock in a Battery Backed-Up Design Provides Reliable Clock and Calendar Functions

National Semiconductor
Application Note 359
Steve Munich
February 1984

INTRODUCTION

National Semiconductor's MM58174A microprocessor real time clock is a reliable and economical solution to adding clock and calendar timekeeping to any system. This metal-gate CMOS circuit (*Figure 1*) will operate with a supply voltage as low as 2.2V, allowing easy implementation of battery back-up circuitry to maintain timekeeping year after year, even when the system's main supply fails. The MM58174A has counters for months, day of month, day of week, hours, minutes, seconds and tenths of seconds, as well as a register for automatic leap year calculations. Also included are periodic and single interrupt capabilities at 0.5, 5 and 60 second intervals.

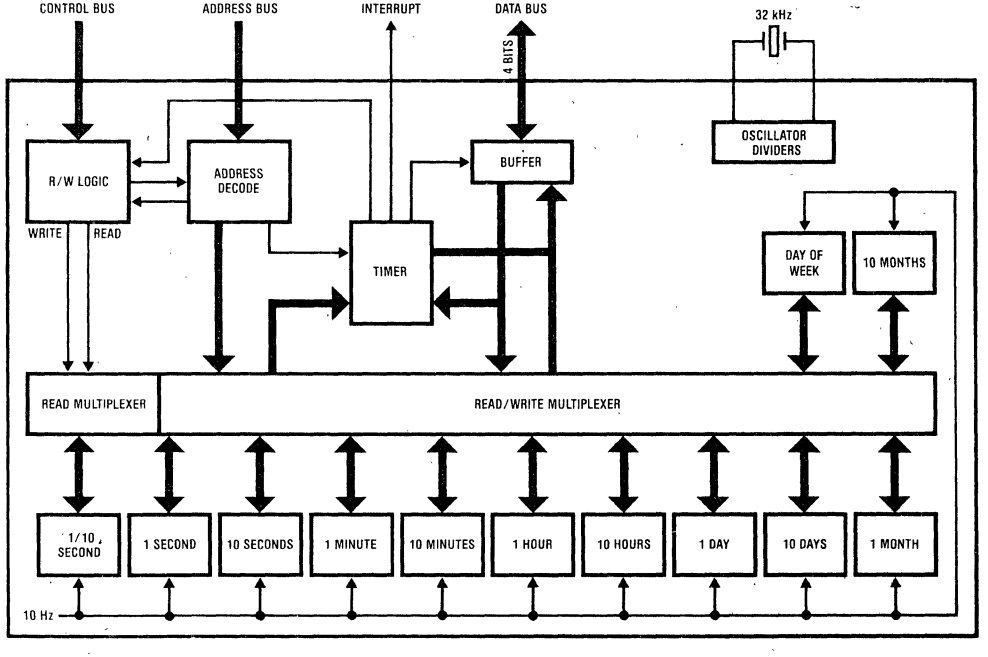
This application note will describe how to interface the MM58174A to microprocessors with battery backed-up circuitry. Included will be a functional circuit description, trouble-shooting hints, crystal oscillator adjustment and supplier information. Please refer to the data sheet for AC and DC electrical specifications and timing diagrams.

DESCRIPTION OF FEATURES

Reading and Writing the Time

The MM58174A has BCD counters for tenths of seconds through months, which are accessed by a 4-bit address as shown in Table I. Months through minutes registers can be read and written to. Tens of seconds, units of seconds and tenths of seconds registers can only be read and are reset to zero when counting is enabled by the start/stop flip-flop. When properly addressed, a nibble of data appears on the data pins DB0–DB3 when a read occurs, and data is accepted on these pins during a write. Any unused data pins will be ignored during a write operation (e.g., days of week uses only DB2 through DB0). To insure proper counter incrementation and accessing, all timing specifications must be observed. It is particularly important that the $\overline{RD}$ strobe width be less than 15 μs for the highest timekeeping accuracy, but never greater than 15 ms.

Address 13 is a write only leap year status register. Writing a "1" to DB3 at this address will cause the time 02/28 23:59 59.9 to roll over to 02/29 00:00 00.0 in one-tenth of a second. If a "1" is instead written to any other data bit, the roll-over will go to 03/01 00:00 00.0 and the leap year will occur as shown in Table II.



TL/F/6169-1

FIGURE 1. Block Diagram

TABLE I. Address Decoding for Internal Registers

Selected Counter	Address Bits AD3	AD2	AD1	AD0	Mode
0 Test Only	0	0	0	0	Write Only
1 Tenths of Seconds	0	0	0	1	Read Only
2 Units of Seconds	0	0	1	0	Read Only
3 Tens of Seconds	0	0	1	1	Read Only
4 Units of Minutes	0	1	0	0	Read or Write
5 Tens of Minutes	0	1	0	1	Read or Write
6 Units of Hours	0	1	1	0	Read or Write
7 Tens of Hours	0	1	1	1	Read or Write
8 Units of Days	1	0	0	0	Read or Write
9 Tens of Days	1	0	0	1	Read or Write
10 Day of Week	1	0	1	0	Read or Write
11 Units of Months	1	0	1	1	Read or Write
12 Tens of Months	1	1	0	0	Read or Write
13 Years	1	1	0	1	Write Only
14 Stop/Start	1	1	1	0	Write Only
15 Interrupt	1	1	1	1	Read or Write

TABLE II. Years Status Register

Mode: Address 13, Write Mode				
	DB3	DB2	DB1	DB0
Leap Year	1	0	0	0
Leap Year – 1	0	1	0	0
Leap Year – 2	0	0	1	0
Leap Year – 3	0	0	0	1

Detecting Changed Data

It is possible that during a sequential read of months through tenths of seconds a roll-over may occur. If the time at the start of the read is 23:59 59.5 and it rolls over to the time 00:00 00.0, the microprocessor could read back 23:50 00.0 or 23:00 00.0, etc. Wrong data could also be stored in the clock if the clock is running and is updated during a write (the start/stop flip-flop discussed in the next paragraph will help avoid invalid writes). The MM58174A has a data-changed flip-flop which indicates that a tenths of seconds roll-over has occurred. This flip-flop sets all the data lines high each time the tenths of seconds counter is updated. The "F" on the data lines is then cleared by the next low-to-high transition of any read strobe. In a sequential read of the counters, the tenths of seconds counter may change while the read strobe is low, but an "F" may never be seen before the read strobe comes high. Thus, the "F" may not be detected, although the experimental probability of this occurrence is approximately one in ten thousand reads, in the worst-case. It is essential to restart the whole sequence of reads, beginning from the tens of months register whenever an "F" is encountered on the data lines. A better procedure, outlined in the flowchart of *Figure 2*, would be to always begin each sequence of reads with the tenths of seconds register and end with this register. If comparing the two values read from this register shows them to be equal, the data read is valid and should be used. If the compare yields two different values, repeat the same sequence of reads until the same value is

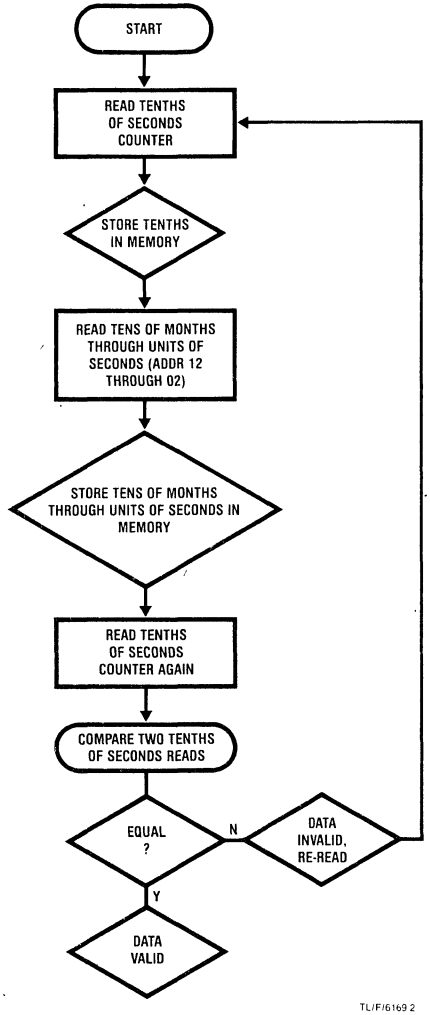


FIGURE 2. Flowchart to Detect Changed Data

read from the tenths of seconds register at the beginning and end of the sequence. It is advisable to use a machine code clock reading routine, or else the time to execute machine-interpreted code may be longer than one-tenth of a second, invalidating all sequential reads.

Clock Accuracy

Two important factors affect the accuracy of the MM58174A. Any internal counter can jitter by $-30.5\ \mu s$, meaning that the true count can be late by this amount. Also, whenever the clock is restarted (see next section), instead of holding a "0" in the tenths of seconds position for one-tenth of a second, the clock immediately jumps to a "1". So each time the clock is restarted, one-tenth of a second is lost. Accuracy would be maintained if the clock is restarted 0.1 second after the time reference's minutes change.

Starting and Stopping the Clock

Table I shows that address 14 accesses the start/stop flip-flop. A "1" on DB0 will start the clock. Writing a "0" to DB0 will stop it. This flip-flop is used for precise starting and stopping of the clock. It also prevents writing invalid data during a clock roll-over, as mentioned in the last paragraph. Before any sequence of writes, stop the clock. Restart it after the last write is completed.

Interrupts

The interrupt counter is controlled internally by three sequential flip-flops. By sending a sequence of read strobes to these flip-flops, the interrupt counter can be cleared or enabled. Initialization is necessary at power-up because these flip-flops can come up in any state. It is also necessary to re-initialize if an interrupt is not serviced within 16.6 ms. To initialize interrupts on the MM58174A, first write a "0" on the data lines at address 15, then read that address three times. The first read will clear any interrupts set. The second read insures that the counter is reset and the third read enables interrupts. Be sure to disable the microprocessor from accepting interrupts before initialization, because the act of writing "0" to address 15 may cause an interrupt.

Table III indicates which values turn on the 0.5, 5 and 60 second periodic or single interrupts. These values are written at address 15, as shown in Table I. To set a particular interrupt, a write need only occur once. Whenever an interrupt occurs, the signal at pin 13 falls from high to low.

TABLE III. Interrupt Selection and Status

Mode: Address 15, Read or Write Mode				
Function	**DB3**	**DB2**	**DB1**	**DB0**
No Interrupt	X	0	0	0
Int. at 60 Sec. Interval†	*	1	0	0
Int. at 5.0 Sec. Interval†	*	0	1	0
Int. at 0.5 Sec. Interval†	*	0	0	1

*0 for single interrupt (write), 1 for periodic interrupt (write), X don't care (read)

†Add 16.6 ms to each time interval

To service the interrupt, read address 15 three times. This causes the interrupt output on pin 13 to return high and restarts the interrupt timer if periodic interrupts have been selected. The interrupt register may be read to see which interrupts have been set, but the MM58174A has no status bit indicating that the clock has sent out an interrupt. A version prior to the MM58174A had interrupt acknowledgement capability (the MM58174), so be sure to match data sheets with the correct parts. One final note about interrupts: they are not intended to be generated when the chip is in the sleep mode (see next paragraph). The MM58174A must be running with at least a 4V supply for interrupts to function.

Powering Down and Up

When the supply to pin 16 falls below 5V, timing becomes much more critical because propagation delays increase with a lowering of the power supply voltage. Note that the data sheet has timing specifications for 5V, and although the part is fully operational down to 4V, your design may not tolerate it. When the supply falls below 4V but stays above 2.2V, the MM58174A is in the sleep mode and only microamps are drawn from the battery. In this mode, the chip is not accessible by reading or writing, but time is being maintained.

On power-up from zero volts V_{CC}, one must make sure the chip is not in the test mode. This is done by writing a "0" to DB3 at address 0. It is advisable to do this even when coming out of the sleep mode. The test mode is mainly for production testing of the circuit.

There are several things to consider when designing the power-down circuitry. The basic functional requirements are to disable the chips before full power loss or malfunction, and to wait for V_{CC} to stabilize before enabling the chip on power-up. A desirable feature would be to allow the read or write in progress to complete. *Figures 3 and 4* include a typical power-down circuit which achieves these goals. In general, avoid using TTL since it is not rated below 4.5V. The power-down circuitry's signals to the MM58174A must not be allowed to deviate more than a diode drop above the clock's supply or below ground in order to avoid triggering SCR latch-up. Finally, be sure to use a PNP switch instead of a diode to disconnect the power supply from the battery. This will allow the MM58174A to see a V_{CC} closer to 5.0V coming from the main supply rather than 4.3V, enhancing timing requirements. See *Figures 3 and 4* and the next section for more information on design of power-down circuitry.

DESIGN IDEAS

Figures 3 and 4 show two possible ways of interfacing the MM58174A to a microprocessor; the former with wait stating and the latter eliminating wait states using the NSC810A RAM/IO timer as a peripheral interface adapter.

Real Time Clock Interface with Wait States

The design of *Figure 3* uses wait states to guarantee that the set-up and hold times of the MM58174A are satisfied. If one can afford to constrict his microprocessor throughput while accessing the MM58174A, this design has the advantages of simplified software and somewhat less expensive hardware. Decreased microprocessor throughput is usually not a consideration in most applications unless the clock is continuously being accessed for a real time display, while at the same time the processor is multiplexing the execution of other tasks.

The HC688s of *Figure 3* are used to fully decode the 4 bits of address space for the real time clock and to generate chip select and wait states. Each time an address between 4080H and 408FH appears on the address lines of the bus, the second of the cascaded HC688s generates a low strobe that allows the power-down circuitry to create a chip select, and also fires an HC123 one-shot configured to drive a 2 μs wait state onto the wait line of the microprocessor bus. For wait lines of the opposite polarity, the HC123's Q output could be used. A shift register may also be configured to give the proper access time delay.

Power is supplied to the parts from a 5.0V supply which is disconnectable by a PNP switch to a battery. When the main supply is on, the PNP in saturation brings the voltage at node B to about 4.8V. The diode near node B is back-biased to keep the battery from discharging and to protect it from damage by isolating it from 5V. If the main supply were to drift far enough downward, the diode would forward-bias, bringing node B to 0.7V below the battery voltage. Since the clock is now in the sleep mode, the only

parts needed to be powered by the battery are the clock and the power-down circuitry. An NPN between the bus connection and the $\overline{WR}$ pin, as shown in *Figure 3*, will reduce power consumption without inverting the signal into this pin. This is made necessary because both $\overline{CS}$ and $\overline{WR}$ inputs on the MM58174A have pull-ups to V_{CC} which could cause an unnecessary current drain if either input were to become grounded. The NPN switch isolates the $\overline{WR}$ from ground, while the $\overline{CS}$ input is held high by the power-down circuitry.

Power-Down Circuitry Operation

The power-down circuitry of *Figures 3 and 4* consists of seven HC00 NAND gates and an LM139 low voltage comparator with an assortment of resistors, diodes and capacitors at the differential input.

With the 5.0V supply on, the assortment of diodes, resistors and capacitors at the comparator's differential input creates a low output. But when the supply is off, the battery pulls this output high through the 20 kΩ resistor. On power-up, after a short delay by the diodes and capacitors at the inverting input, the LM139's low level output enables a latch made from HC00 NAND gates to allow a chip select from the 'HC688 (*Figure 3*) or the NSC810A (*Figure 4*) to flow through to pin 1 ($\overline{CS}$) of the MM58174A.

As power from the 5.0V supply falls below 4.5V, the comparator's output immediately goes high. This threshold voltage is adjustable by the 200 kΩ potentiometer at the LM139's inverting input. A high output from the comparator to the NAND latch will disable chip selects to the MM58174A.

So as power begins to fail, this circuit will allow reads or writes to the MM58174A to go to completion if the chip is selected before the LM139's output goes high. This assumes that the MM58174A's $\overline{CS}$ pin returns high before the supply falls to 4.0V (the minimum V_{CC} to access the chip). The length of the chip select strobe determines the limit of how fast the main power supply can drop from 4.5V to 4.0V. In situations where power failure detection is more critical, it is suggested that the comparator's output be connected to the microprocessor's highest priority interrupt so that the necessary software can be accessed.

This power-down circuitry has the advantage of proper operation in the presence of noise. With a slowly falling power supply in a noisy environment, the comparator's output may oscillate momentarily. This oscillation will have no bearing on the chip select signal to the MM58174A in this circuit because the HC00 latch only allows chip selects when the LM139 output is high, and it also does not alter their length once they begin. When the supply falls low enough to stop the comparator from oscillating, chip selects are locked out. One may consider the time that the comparator bounces as a delay before chip access is completely locked out as the standby mode is entered. If the cessation of comparator oscillation is desired, hysteresis can be added. A diagram of this can be found in the LM139 data sheet.

Real Time Clock Interface without Wait States Using a PIA

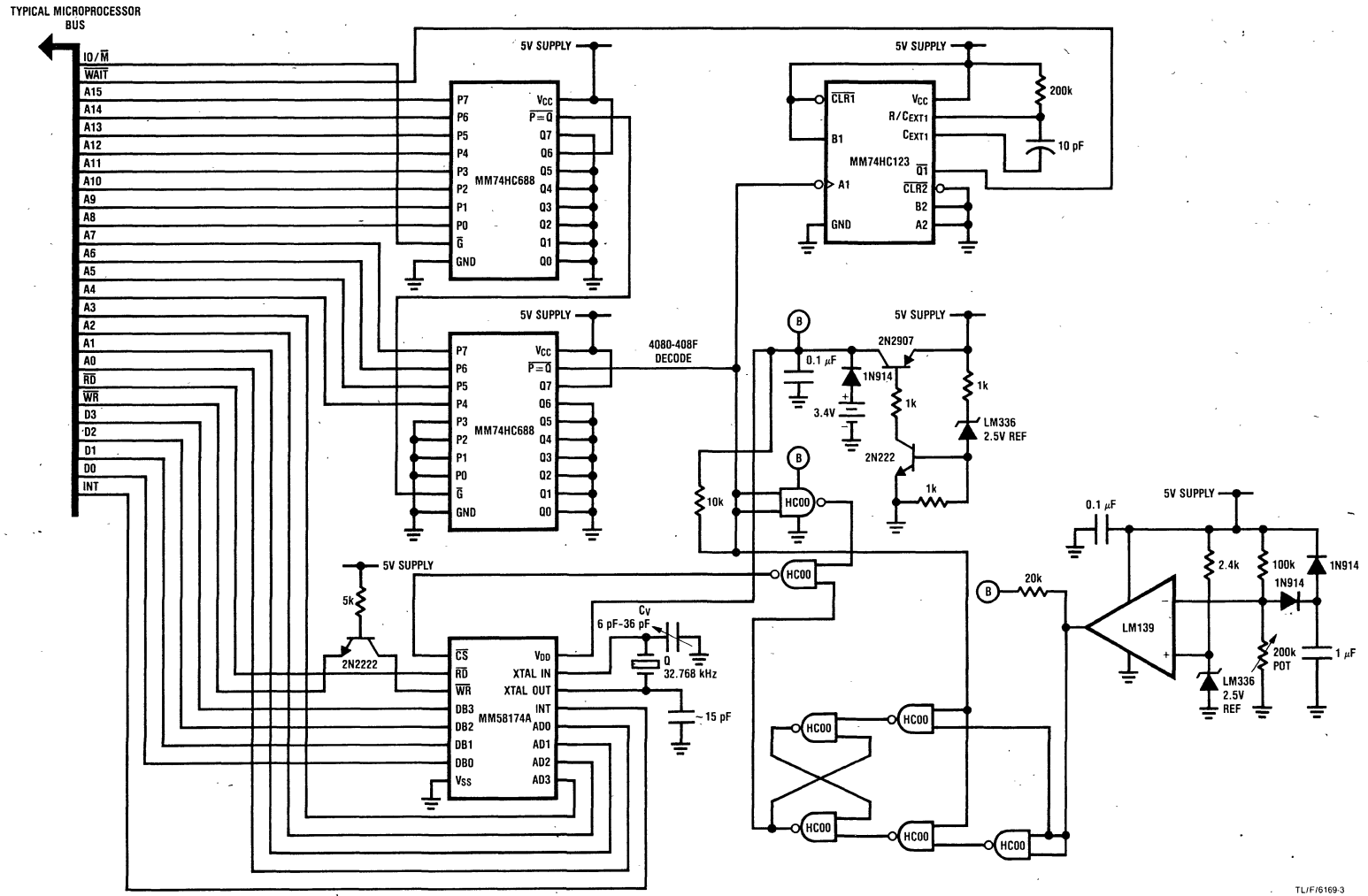
Figure 4 shows the details of a design using the NSC800™ CMOS microprocessor and the NSC810A as a peripheral interface adapter. This has the advantages of lower chip count and the absence of wait states. Similar PIAs, such as the INS8255 or the 8155, could be used with some software adaptation. The power-down circuitry is operationally equivalent to that of *Figure 3*, except that in this design the chip select is created by the PIA. Only the essential connections between the NSC800 and the NSC810A are shown in the *Figure 4*.

The NSC800 is an 8-bit CMOS microprocessor combining the features of the Intel 8085 and the Zilog Z80®. In this application 8085 code is used to manipulate the control strobes and handle interrupts as detailed in *Figures 5 through 9*. The interconnection between the NSC800 and the NSC810A is straightforward, except for the CE connection on the NSC810A. By tying CE to A13 of the NSC800, chip enabling occurs whenever an IN 2X or an OUT 2X instruction is executed, because the same port address appears on NSC800 lines AD0-AD7 as on A8-A16. Using 2X will raise A13 on the NSC800 high, where X represents a specific port address. This method of enabling is entirely optional. For more information on the NSC800 and NSC810A, refer to the NSC800 Microprocessor Family Handbook.

Software Description

The ports on the NSC810A are specially configured to control the data, address and control lines. The software allows the port signals to fulfill timing requirements. Port C is used to control the $\overline{WR}$, $\overline{RD}$ and $\overline{CS}$ lines, port B is used to control the address lines, and port A is used to read and write the data.

The NSC810A is configured into the strobed input mode in the read subroutine in order to get the shortest possible $\overline{RD}$ strobe. As stated previously, the read strobe must be under 15 μs to guarantee proper counter operation. The $\overline{RD}$ strobe is fed back to the PC2/$\overline{STB}$ input of the NSC810A in order to latch in the data from the MM58174A. The read subroutine of *Figure 5* begins by setting the port C direction. All bits are set for output, except PC2/$\overline{STB}$, which is set for input. Port B is set out and port A is set in. Next, all the control strobes from port C are set high using bit set. Before calling the read routine, the MM58174A address to be accessed was loaded into the NSC800's register B, and it is now sent out on port B. Bit clear is used to lower the $\overline{CS}$ strobe from PC5. The mode definition register is then written to for selecting the strobed mode of the NSC810A. Bit clear is used to lower the $\overline{RD}$ strobe from port C, and before it is raised again, a MOV instruction puts control values from port C into the accumulator in the shortest time possible. Using these three instructions, the read strobe is held low for about 5 μs. The rising edge of the $\overline{RD}$ strobe is fed into PC2/$\overline{STB}$ to latch the data into port A, and the IN instruction reads the data. Before exiting the read subroutine, the mode definition register of the NSC810A is again accessed to return the PIA's operation to the basic I/O mode. A wait loop may be added to the read subroutine or elsewhere in the code to limit the number of read strobes to less than 10,000 per second. This specification has been added because more than 10,000 reads per second can slightly degrade timekeeping accuracy. The write subroutine of *Figure 6* uses the NSC810A ports in the same manner as the read routine; i.e., port A for data, port B for address and port C for control strobes. However, there is no need to latch the data in port A, so the basic I/O mode is used. The write subroutine uses the control strobes from port C by beginning with all three strobes high, manipulating $\overline{CS}$ and $\overline{WR}$ low, and finally bringing these port outputs high again. Before calling the write subroutine, the desired address to be accessed is to be stored in the NSC800's register B, and data stored in register A.



Q = 32.768 kHz crystal (RCD, Saronix)

C_V = variable capacitor (Erie, Circuit.Specialists)

FIGURE 3. Real Time Clock Interface with Wait States

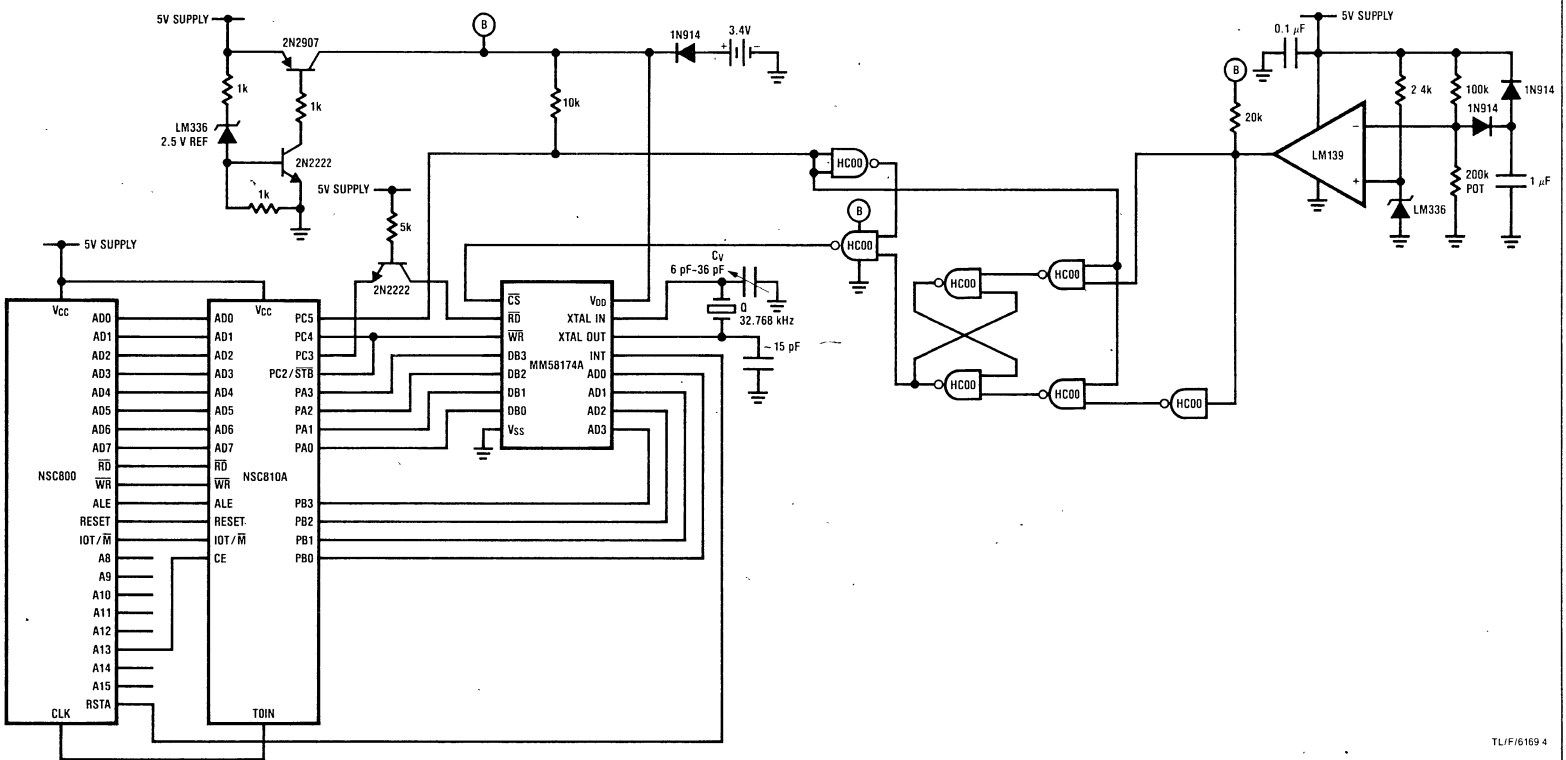


FIGURE 4. Real Time Clock Interface to NSC800 and NSC810A without Wait States

```
                    ;DATA IS RETURNED INTO REG A
READ:   MVI A, 0FBH ;SET PORT C
        OUT 026H            ;DIRECTION
        MVI A, 0FFH ;SET PORT B
        OUT 025H            ;DIRECTION OUT
        MVI A, 00H  ;SET PORT A
        OUT 024H            ;DIRECTION IN
        MVI A, 038H ;SET PC3, PC4 & PC5 HIGH
        OUT 02EH            ;USING BIT SET
        MOV A, B    ;PUT ADDRESS IN A
        OUT 021H    ;ADDRESS OUT ON PORT B
        MVI A, 020H ;BIT CLEAR - PC5
        OUT 02AH            ;CHIP SELECT
        MVI A, 01H  ;SELECT STROBED
        OUT 027H            ;MODE
        MVI C, 030H ;GET READY
        MVI A, 010H ;BIT CLEAR - PC4
        OUT 02AH            ;RD STROBE
        MOV A, C    ;LATCH DATA IN PORT A
        OUT 02EH            ;& BRING STROBES HIGH
        IN 020H     ;GET DATA FROM PORT A
        ANI 0FH     ;MASK-OUT LOWER BITS
        MOV C, A    ;SAVE DATA
        MVI A, 00H  ;RETURN TO
        OUT 027H            ;BASIC I/O MODE
        MOV A, C    ;RECOVER DATA
        RET
```

TL/F/6169-5

FIGURE 5. Read Subroutine

```
                    ;BEFORE CALLING WRITE SUBROUTINE
                          ;STORE 174A ADDRESS IN REG B
                                ;AND DATA IN REG A
WRITE:  MOV C, A    ;SAVE DATA IN REG C
        MVI A, 0FBH
        OUT 026H    ;SET PORT C DIRECTION
        MVI A, 0FFH
        OUT 022H    ;SET PORT C HIGH
        OUT 024H    ;SET PORT A DIRECTION OUT
        OUT 025H    ;SET PORT B DIRECTION OUT
        MOV A, B    ;MOVE 174A ADDRESS TO REG A
        OUT 021H    ;ADDRESS OUT FROM PORT B
        MVI A, 020H ;CHIP SELECT - BIT CLEAR
        OUT 02AH            ;ON PC5
        MVI A, 08H  ;WRITE STROBE - BIT CLEAR
        OUT 02AH            ;ON PC3
        MOV A, C    ;RECOVER DATA FROM REG C
        OUT 020H            ;DATA GOES OUT
        MVI A, 0FFH ;SET PORT C
        OUT 022H            ;HIGH
        RET
```

TL/F/6169-6

FIGURE 6. Write Subroutine

```
ORG 1200H       ;ORIGINATE @1200H
LXI SP, 01FH    ;LOAD STACK POINTER
MVI A, 00H      ;ENTER NON-TEST MODE
MVI B, 00H              ;
CALL WRITE                      ;
LXI H, VECTOR   ;"VECTOR" IS INTERRUPT SERVICE
SHLD 1016H              ;ROUTINE @1016H
MVI A, 04H      ;SET NSC800'S INTERRUPT CON-
OUT 0BBH                ;TROL REGISTER FOR RSTA
DI              ;DISABLE NSC800 INTERRUPTS
MVI A, 00H      ;ENABLE INTERRUPTS ON 174A
MVI B, 0FH              ;
CALL WRITE                      ;
CALL READ                               ;
CALL READ                                       ;
CALL READ
EI              ;ENABLE NSC800 INTERRUPTS
```

TL/F/6169-7

FIGURE 7. Initialization

Figure 7 shows the necessary initialization code for the NSC800, NSC810A, and the MM58174A, which use the read and write subroutines. Of greatest importance is the code to insure that the clock is not in the test mode. Notice that a DI instruction is used to disable interrupts before a "0" is written to address 15. Also included is the code to initialize interrupts on the MM58174A. *Figure 8* shows the interrupt service routine, while *Figure 9* shows a method of time setting by first stopping the clock, then restarting it once the setting is complete.

```
VECTOR:  MVI B, 0FH
         CALL READ
         CALL READ
         CALL READ
         EI
         RET
```

TL/F/6169-8

FIGURE 8. Interrupt Service Routine

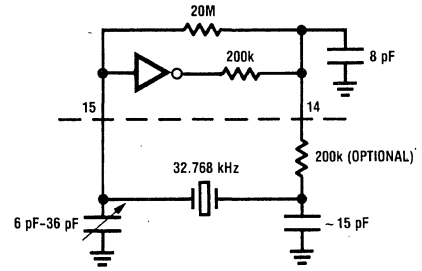
```
MVI A, 00H      ;STOP CLOCK USING
MVI B, 0EH              ;START/STOP FLIP-FLOP
CALL WRITE

(time setting code)

MVI A, 01H
MVI B, 0EH
CALL WRITE
```

TL/F/6169-9

FIGURE 9. Recommended Procedure for Setting Time

Oscillator Design

The MM58174A is driven by a standard Pierce oscillator. *Figure 10* shows both the internal and external component sizes to be used. For crystals with a power rating of less than 1 μW, a 200 kΩ resistor, in series with the oscillator output, should be used to insure that the crystal is not overdriven. The typical gain for the internal inverter and internal 200 kΩ series resistor is 20 at 1 kHz input frequency and about 5 at 30 kHz. The oscillator may take from two to seven seconds to begin oscillating due to the high Q of the crystal.



TL/F/6169-10

FIGURE 10. Crystal Oscillator

Crystal Information

Choose one of the following crystal types: parallel resonant or tuning fork (NT CUT or XY BAR) with a Q > 35,000 and a frequency of 32.768 kHz. The load capacitance required ranges from 9 pF to 13 pF. The maximum power rating is 20 μW. The choice of crystal accuracy and temperature coefficient are left to the user. Two crystals used in our lab are RCD's #RV-38 and Saronix's #NTF3238C.

Oscillator Adjustment and External Drive

A well-tuned oscillator for the MM58174A will have a frequency error of no more than ± 10 ppm. This would result in the clock being off by ± 5 minutes per year. This is a worst-case number, taking into account such factors as temperature variation (− 40°C to 85°C) and supply variation (2.2V to 5.5V). The external oscillator components can also contribute to error and this should be taken into account by the user.

Adjusting the trimmer capacitor at pin 15 will minimize the oscillator error. But simply putting a scope probe on the crystal will load the oscillator with at least 10 pF, significantly altering the frequency. There are two good ways of isolating the probe from the oscillator. One method is to put the part in the test mode by writing a "0" to DB3 at AD0, then tune the signal at DB0 to 16,384.00 Hz using an accurate frequency counter. Another method would be to isolate the oscillator from the probe by adding an inverter to the small capacitance at pin 14. This would load the oscillator, but the input capacitance of the gate would not be affected by a probe at the output. The total capacitance on pin 14 should be kept near 15 pF.

To drive the oscillator from an external clock, connect the clock to pin 14 (crystal out) and tie pin 15 (crystal in) high.

CONCLUSION

The MM58174A can easily be interfaced to a microprocessor to bring the functions of a real time clock and calendar to any system. With a power-fail/back-up circuit, the system will be able to keep accurate time for years, independent of the system power supply.

The MM58274 Adds Reliable Real-Time Keeping to Any Microprocessor System

National Semiconductor
Application Note 365
Peter K. Thomson
April 1984

INTRODUCTION

When a Real-Time Clock (RTC) is to be added into a digital system, the designer will face a number of design constraints and problems that do not usually occur in normal systems. Attention to detail in both hardware and software design is necessary to ensure that a reliable and trouble free product is implemented.

The extra circuitry required for an RTC falls into three main groups: a precise oscillator to control real-time counting; a backup power source to maintain time-keeping when the main system power is removed; power failure detection and write protection circuitry. The MM58274 in common with most RTC devices uses an on-chip oscillator circuit and an external watch crystal (frequency 32.768 kHz) as the time reference. A battery is the usual source of backup power, along with circuitry to isolate the battery-backed clock from the rest of the system. Like any CMOS component, the RTC must be protected against data corruption when the main system power fails; a problem that is very often not fully appreciated.

Rather than dealing strictly with any one particular application, this applications note discusses all of the aspects involved in adding a reliable RTC function to a microprocessor system, with descriptions of suitable circuitry to achieve this. Hardware problems, component selection, and physical board layout are examined. The software examples given in the data sheet are explained and clarified, and some other software suggestions are presented. Finally a number of otherwise unrelated topics are lumped together under 'Miscellany'; including a discussion on how the MM58274 may be used directly to upgrade an existing MM58174A installation.

CONTENTS

1.0 HARDWARE

Selecting the correct components for the job and implementing a good board layout is crucial to developing an accurate and reliable Real-Time Clock function. The range of component choices available is large and the suitability of different types depends on the demands of the system.

1.1 COMPONENT SELECTION

With reference to *Figure 1*, the oscillator components and the battery are examined and the suitability of different types is discussed.

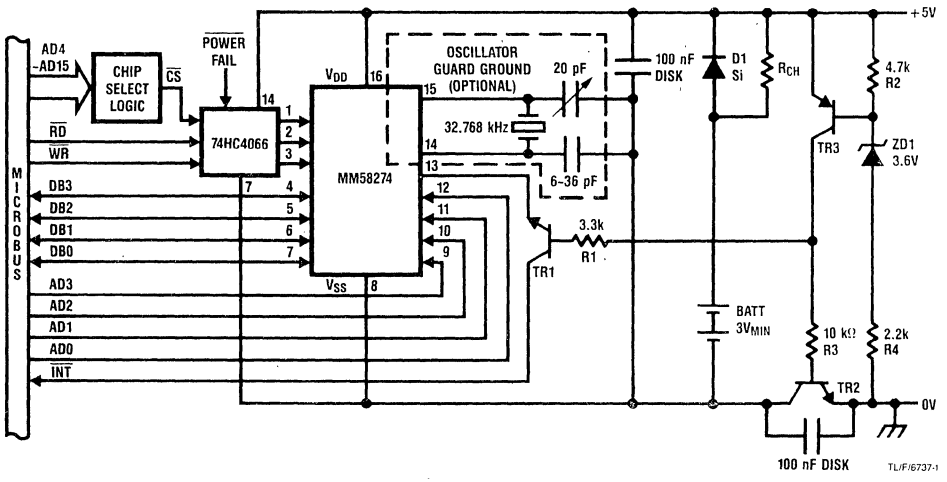


FIGURE 1. MM58274 System Installation

1.1.1 Crystal

The oscillator is designed to work with a standard low power NT cut or XY Bar clock crystal of 32.768 kHz frequency. The circuit is a Pierce oscillator and is shown complete in *Figure 2*. The 20 MΩ resistor biases the oscillator into its linear region and ensures oscillator start-up. The 200 kΩ resistor prevents the oscillator amplifier from overdriving the crystal. If very low power crystals are used (i.e., less than 1 μW) an external resistor of around 200 kΩ may have to be added to reduce the drive to the crystal.

The oscillator will drive most normal watch crystals, with up to 20 μW drive available from the on-chip oscillator.

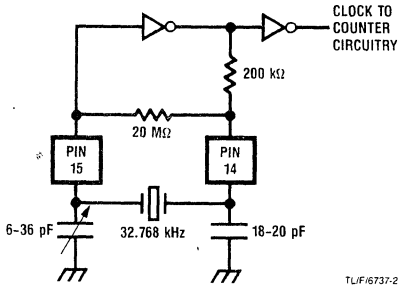


FIGURE 2. Complete Oscillator Diagram

1.1.2 Loading Capacitors

Two capacitors are used to provide the correct output loading for the crystal. One is a fixed value capacitor in the range 18 pF–20 pF and the other is a variable 6 pF–36 pF trimmer capacitor. Adjusting the trimmer allows the crystal loading (and hence the oscillator frequency) to be fine tuned for optimal results.

The capacitors are the components most likely to affect the overall accuracy of the oscillator and care must be exercised in selection. Ceramic capacitors offer good operating temperature range with close tolerance and low temperature coefficients (typically ±3 ppm/K, for good quality examples). If trimming is undesirable a pair of close tolerance (±5% or better) capacitors in the range 18 pF–20 pF may be used. The average time-keeping accuracy for this configuration is within ±20 seconds per month.

1.1.3 Backup Battery

There are a number of different cell types available that can be used for time-keeping retention. Some cells are more suitable than others, and the way in which the system is used also influences the choice of cell. Ideally the standby voltage of the RTC should be kept as low as possible, as the supply current increases with increasing voltage *(Figure 3)*. Four different power sources are discussed: capacitors, nickel-cadmium rechargeable cells, alkaline and lithium primary cells.

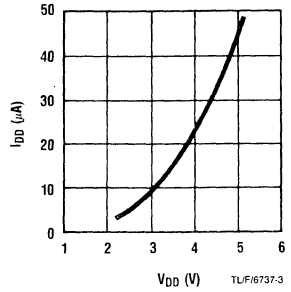


FIGURE 3. Typical I_{DD} (μA) vs. V_{DD} (V) for MM58274 in Standby Mode (T_A = 25°C)

Capacitors
When the system is permanently powered, and any long term removal of system power (i.e., more than a few hours) requires complete restarting, then a 1–2 Farad capacitor may be sufficient to run the clock during the power down. This can keep the clock running for 48–72 hours.

Nickel-Cadmium Cells
Nickel-cadmium (Ni-Cad) cells can be trickle-charged from the system power supply using a resistor as shown in *Figure 1.* The exact value of resistor used depends on the capacity and number of cells in the battery. Consult the manufacturers data for information on charging rates and times.

A 3- or 4-cell battery should be used to power the clock (the nominal battery voltages are 3.6V for 3 cells in series and 4.8V for 4 cells), with 3 cells preferable. PCB mounting batteries of 100 mAh capacity are available and these will give around 6 months data retention (at normal room temperature). For this cell type to be used the system must spend a large proportion of its time turned on to keep the battery charged (i.e., used daily).

Alkaline
Alkaline cells are among the least expensive primary cells which are suitable for use in real-time clock applications. They are available in a large range of capacities and shapes and have a very good storage (shelf) life.

Two cells in series will provide a nominal 3V, which is adequate to power the clock (via the isolating diode). The main problem with the alkaline system is that the cell terminal voltage drops slowly over the life of the cell. When the voltage at the clock supply pin drops to 2.2V, the cells must be replaced (battery voltage around 2.6V–2.7V). With present alkaline cells, this point is usually reached when the cells are only $^1/_2$ to $^2/_3$ discharged.

Provisions must be made either to check the battery voltage at regular intervals or to replace the cells regularly enough to avoid the danger of using discharged cells. Once again the manufacturers data regarding capacity and cell voltage against time must be examined to determine a suitable cell selection. A good alkaline system will supply 1–2 years continuous time-keeping.

Lithium
Lithium cells are the most suitable cell for real-time clock applications. A single cell with 3V potential is sufficient to power the system. The cell potential is very stable over use and the storage life is excellent. The energy density of lithium cells is very high, giving enough capacity in a physically small cell to power the clock continuously for at least 5 years (at room temperature using a 1,000 mAh cell).

Several cells which are recommended for RTC use are D2/3A*, D2A*, and 1/6DEL/P**. Each have 1,000 mAh capacity. These cells are available with solder pin connections for PCB mounting, giving a reliable backup supply.

Other Cells and Notes
There are many other types of cells, both primary and secondary, which may be adapted for RTC use. When selecting a cell type, attention must be paid to:

a. Cell capacity and physical size.
b. Storage (shelf) life.
c. Voltage variation over use.
d. Operating temperature range.
e. The method of battery connection and mounting.

In general soldered cells are preferable to connector mounted cells. With replaceable batteries, the battery and connector contacts must be kept thoroughly clean. Dirty or corroded contacts can cause the clock to be starved of power, giving erratic and unreliable performance. The ease of operator access for cell replacement should also be considered.

Temperature Range
The performance of any cell will be satisfactory for most office or domestic environments. When 'ruggedized' equipment is to be used (i.e., field portable equipment, automotive, etc.) the temperature specification of different cell types should be taken into account when selecting a cell. Lithium cells offer good performance over 0°C–70°C with little loss in capacity. Once again, the manufacturer's data should be examined to determine suitability, especially since different cells of the same type can have markedly different characteristics.

Few types of cells will offer any useful capacity at temperatures in or below the range 0°C–10°C, and fewer still will operate over the full military temperature range (–55°C to +125°C). Solid lithium cells and mercury-cadmium cells are two systems which can cover this range.

1.2 BOARD LAYOUT

1.2.1 Oscillator Connection

The oscillator components must be built as close to the pins of the clock chip as is physically possible. The ideal configuration is shown in *Figure 4.* From *Figure 2,* the oscillator circuit, it can be seen that both Osc In and Osc Out are high impedance nodes, susceptible to noise coupling from adjacent lines. Hence the oscillator should, as far as is practicable, be surrounded by a guard ground. The absolute maximum length of PCB tracking on either pin is 2.5 cm (1 inch). Longer tracks increase the parasitic track to track capacitances, increasing the risk of noise coupling and hence reducing the overall oscillator stability.

Where the system operates in humid or very cold environments (below 5°C), condensation or ice may form on the PCB. This has the effect of adding parasitic resistances and capacitances between pins 14 and 15, and also to ground. This variation in loading adversely affects the stability of the oscillator and in extreme cases may cause the oscillator to stop.

Keeping the PCB tracks as short as possible will help to minimize the problem, and on its own this may be sufficient. Where the operating conditions are particularly severe, the PCB and oscillator components should be coated with a suitable water repellent material, such as lacquer or silicon grease (suitability being determined by the electrical properties of the materials — high impedance and low dielectric constant).

Figures 2 and *4* show the trimmer placed on Osc Out. The placement of the trimmer capacitor on either Osc In or Osc Out is not critical. Placing the trimmer on Osc Out yields a smaller trim range, but less susceptibility to changes in trimmer capacitance. Placement of the trimmer capacitor on Osc In gives a wider trim span, but slightly greater susceptibility to capacitance changes.

*Duracell Trade Number.
**Tadiran Trade Number.

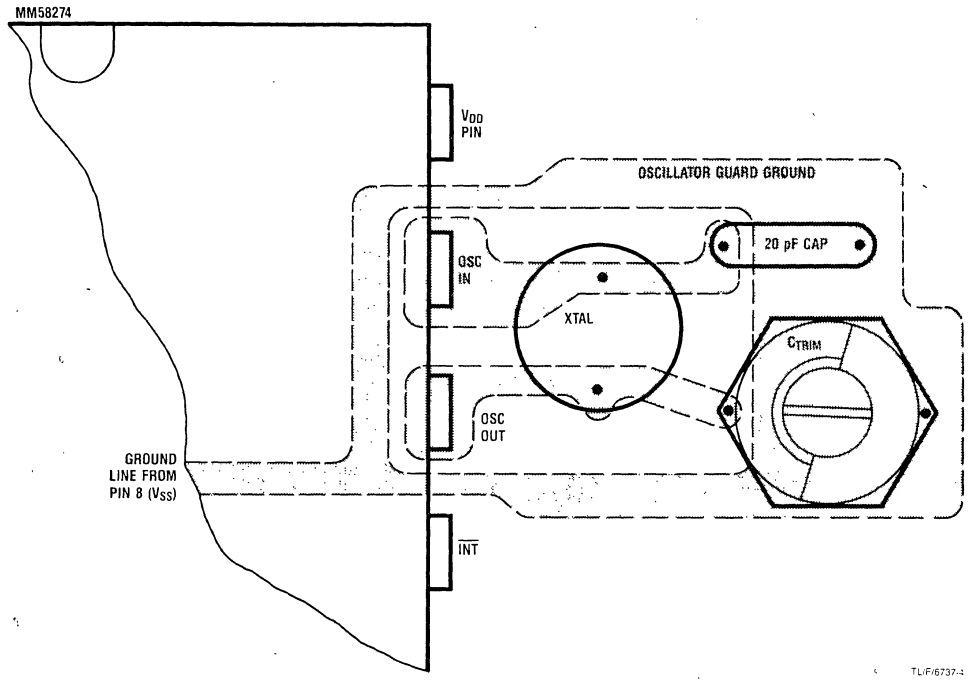


FIGURE 4. Oscillator Board Layout

1.2.2 Battery Placement

For the battery, placement is less critical than with the oscillator components. Practical considerations are of greater importance now; i.e. accessibility. The battery should be placed where it is unlikely to be accidentally shorted or disconnected during routine operation and servicing of the equipment.

When replaceable cells are used, connecting a 100 μF capacitor across the RTC supply lines will keep the clock operating for 30–40 seconds with the battery disconnected *(Figure 5)*. This allows the battery to be replaced regardless of whether or not the main supply is active.

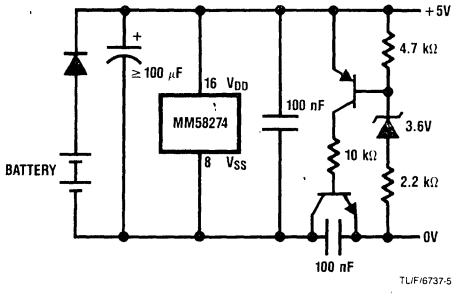


FIGURE 5. Simplified Power Supply Diagram with 100 μF Capacitor Added

1.2.3 Other Components

The placement of the other RTC dedicated components (e.g., supply disconnection and power failure protection components) is not particularly critical. However, the same guidelines as applied to the battery should be followed when the PCB layout is designed.

1.3 POWER SUPPLY ISOLATION SCHEMES

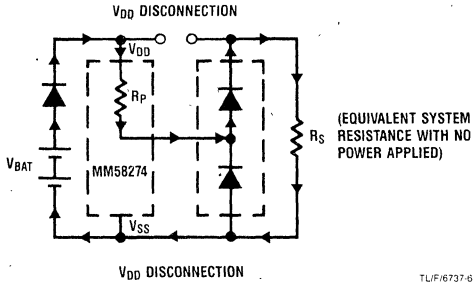
1.3.1 The Need for Isolation

There two reasons for disconnecting the clock circuit from the rest of the system:

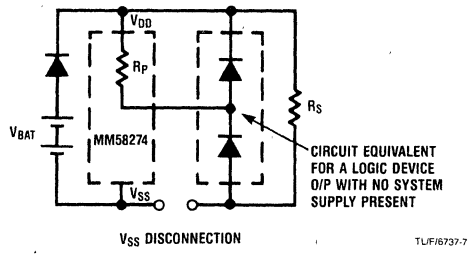
1. To prevent the backup battery from trying to power the whole system when the main power fails.
2. To minimize the battery current (and extend battery life) by preventing current leakage out of the RTC input pins.

The MM58274 inputs have internal pull-up devices which pull the inputs to V_{DD} in power down mode. This turns off the internal TTL input buffers and causes the μP interface functions of the clock to go to full CMOS logic levels, drawing no supply current (except for the unavoidable leakage current of the internal MOS transistors). For the MM58274 this is achieved by isolating the ground (V_{SS}) supply line from the rest of the system.

Figures 6a and *6b* show the two cases where first V_{DD} *(6a)* and then V_{SS} *(6b)* are open-circuited. The line out from the MM58274 represents any of the Control, Address, or Data lines on the RTC, with the internal pull-up resistor shown. The two diodes and resistor R_S represent the logic device connected to the RTC input and the resistance of the rest of the system with no power applied.



a) V_{DD} Disconnection



b) V_{SS} Disconnection

FIGURE 6. Current Leakage Prevention by Proper Supply Disconnection

When V_{DD} is open-circuit as in *Figure 6a,* there is a complete current path, shown by the arrows, out of the RTC input and through the external circuitry. This battery current is a complete waste and serves only to reduce the cell life. Depending on the value of R_S, the voltage level at the pin may fall low enough to turn on the internal TTL level buffer, wasting further current as the buffer is no longer fully CMOS.

With V_{SS} disconnected *(Figure 6b),* there is no return path to the battery and the pin is pulled completely up to V_{DD}. The TTL buffer is switched off and no power is lost.

1.3.2 Isolation Techniques I — 5V Supply Only

Figure 7 shows the isolation circuit suggested in the MM58274 data sheet. This circuit provides complete disconnection where only the system +5V is available for switching control.

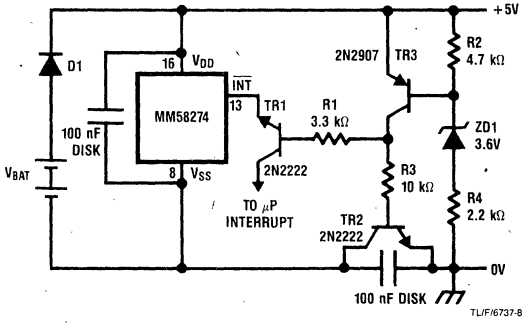


FIGURE 7. 5V Isolation Circuit

TR2 is the disconnecting device, which is controlled by TR3 and its associated circuitry. TR3 is turned on by its bias chain R2, ZD1, R4 as the system supply rises up to 4.2V. TR3 and R3 then turn on TR2 to connect the clock to the system supply. D1 isolates the backup battery when the system supply is active. The 100 nF disk capacitors decouple the supply during R/W operations and should be included in any disconnection scheme.

TR3 is necessary to prevent R3 and TR2 from leaking battery current in the power down condition. The circuit without TR3 is shown in *Figure 8* where TR2 has been replaced by equivalent diodes to clearly show the problem. The circuitry

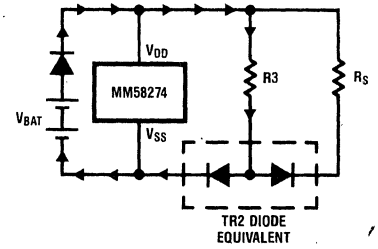


FIGURE 8. Current Leakage In Simplified Disconnection Schemes

could be simplified by replacing TR3 with a Zener diode *(Figure 9).* There will be a small loss of current down through TR2 however, as the Zener will pass a small leakage current at below its 'knee' voltage. Thus the Zener should be selected for its low current capability.

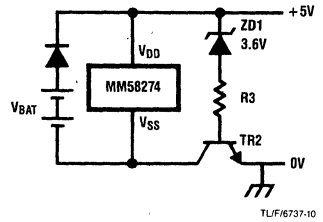


FIGURE 9. Alternative Supply Disconnection Scheme Sensing 5V (Decoupling Capacitors Omitted for Clarity)

Finally TR1 and R1 *(Figure 7)* are optional components which are only required when the interrupt output is used. If interrupts are left programmed when the power fails, the interrupt timer will still time-out setting the interrupt output. Since this is an active low pull-down transistor it effectively shorts directly across TR2, destroying the RTC isolation and discharging the battery into the rest of the system *(Figure 10).* In order to prevent this from occurring, TR1 and R1 are added.

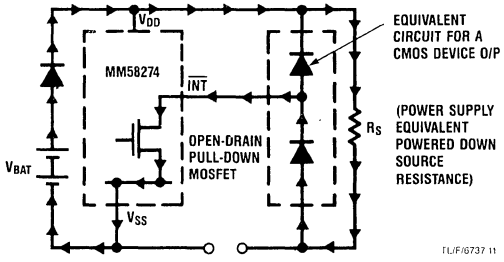


FIGURE 10. Battery Discharge Path via Unisolated Interrupt Output

None of the disconnection components are at all critical, with general purpose transistors being completely adequate for the task. D1 should be a small-signal silicon or germanium diode.

1.3.3 Isolation Techniques II — Negative Supply Switched

Where a negative voltage supply is available (either regulated or unregulated) the circuit of *Figure 11* may be used. This is similar in operation to its diode equivalent shown in *Figure 12*, where the voltage drops across the diodes provide the correct potential to the clock. *Figure 11* has the advantage, however that the clock power is supplied from the ground line by transistor action, rather than via the resistor as in *Figure 12*. Less power is dissipated in the resistor as only transistor bias current need by drawn.

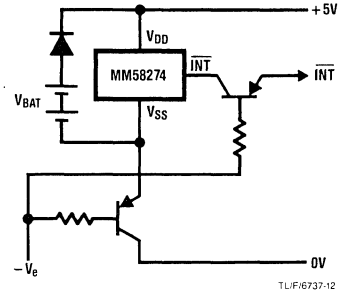


FIGURE 11. Negative Voltage Driven Supply Disconnection Scheme (Decoupling Capacitors Omitted for Clarity)

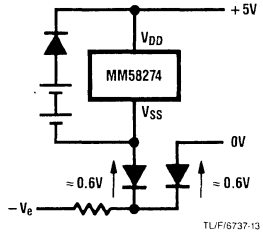


FIGURE 12. Diode Equivalent Circuit of Figure 11.

1.3.4 Other Methods

There are many other possibilities for supply disconnection schemes, i.e., relay disconnection. When designing a disconnection scheme, the performance must be analyzed both with the system power applied and with absent. Check for leakage paths and undue voltage drops and try to set up so that disconnection and reconnection will take place as near to the backup voltage as possible.

1.4 POWER FAIL PROTECTION

One of the major causes of unreliability in RTC designs is due to inadequate power failure protection. As the system is powered up and down, the μP and surrounding logic can produce numerous spurious signals, including spurious writes and illegal control signals (i.e., RD and WR both active together).

Bipolar logic devices can produce spikes and glitches as the internal biasing switches off around 3V–3.5V, and the transistors operate in their linear region for a short time. Any such spurious signals, if applied to the RTC, could cause the time data to be corrupted. Systems using 74HC logic and CMOS processors are less stringent in their power failure requirements as the devices tend to work right down to around 2V. Some form of write protection is still required, however.

In order to protect the time data, the system must be physically prevented from writing to the clock when the power supply is not stable. The ideal situation is to ban Write access to the clock before the system +5V starts to fail, and then keep the chip 'locked-out' until the power is restored and stabilized. This ideal access control signal is illustrated in *Figure 13*.

Three methods of power fail protection are discussed, although there are also many other possibilities.

1.4.1 Write Protect Switch

By far the simplest and potentially the most hazard-free method is to use a switch on the WR control line to the clock *(Figure 14)*. This is completely adequate, but requires the intervention of an operator to alter time data or program interrupts.

Some thought must be given to ensuring that the operator cannot accidentally leave the WR line switched in. This may be achieved by the physical access method used (i.e., the machine is impossible to operate or switch off when in the time setting mode, because of the placement of access hatches, etc.) or with software. The switch state could be sensed by trying to alter the data in the Tens of Years counter or Interrupt register just prior to leaving the clock setting routine, and refusing to leave the routine until the WR switch has been opened. The switch condition should similarly be checked whenever the system is initialized or reset.

The physical location of the switch should also be considered for ease of accessibility. How easy the switch is to reach will depend on the system; i.e., in some cases a 'tamper proof' clock may be required.

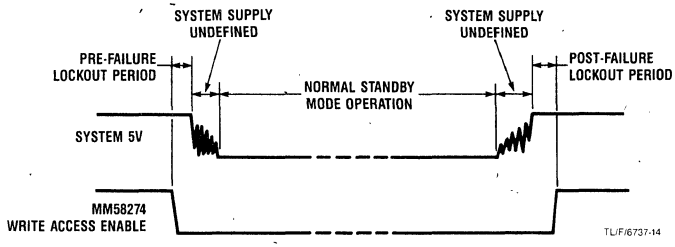


FIGURE 13. RTC Access Lockout Definition

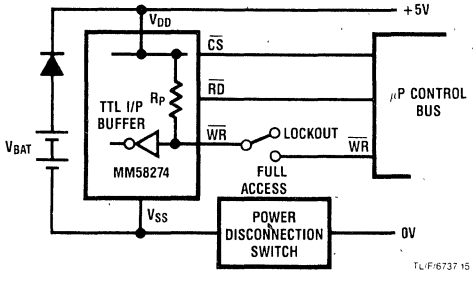


FIGURE 14. Write Protection by Manually Switching WR

1.4.2 5V Sensing

The circuit of *Figure 15* senses the system 5V supply and prevents access to the clock if the supply falls below 4.2V–4.3V. This circuit should be used where only the system 5V is available for reference. The LM139 comparator and associated components sense the 5V supply and generate the power fail signal (P. Fail). The 74HC75 and components disconnect the WR line.

R3 and ZD1 provide a reference voltage of 2V–3V for the comparator. R4 and VR1 form a potential divider chain sensing the 5V line, and VR1 is adjusted to switch the comparator output at 4.2V–4.3V. An alternative to VR1 would be to use a pair of close tolerance resistors (±2%) with values selected to suit the Zener diode reference used. The combination of R4, D3 and C2 provide an RC time constant to delay the comparator when sensing the return of 5V (to provide the post-failure delay in *Figure 13).* The LM139 has an open-collector output which is held low when 5V is present and is switched off when 5V fails. This line is pulled high by R5 to flag power failure (P. Fail). Since the comparator is a linear device drawing a bias current, it is powered by the system 5V supply to avoid consuming battery power.

One 74HC75 package contains four latches, of which two are used. These are transparent latches controlled by the 'G' input. With G high, the latch is transparent and the Q and $\overline{Q}$ outputs follow the Data input. When G is low, the state of Q and $\overline{Q}$ on the falling edge is latched. In this way, F2 prevents P. Fail from locking out the clock if there is a Write cycle in progress. F1 isolates the WR input on the clock when F2 passes the P. Fail signal. C1, R2 and D1 do not slow the advent of P. Fail, but they cause a delay in the release of the function to mask any comparator noise or oscillation as the comparator switches off or on (i.e., during the undefined supply periods).

D2, C3 and R6 smooth the comparator supply and help it to function effectively. The time constants of the RC networks should be selected to suit the power supply of the system that is used. Comparing the functioning of this circuit with the ideal case of *Figure 13* shows that most of the conditions can be satisfied, except that there is no real pre-failure lockout period. This cannot be achieved without some form of look ahead power failure.

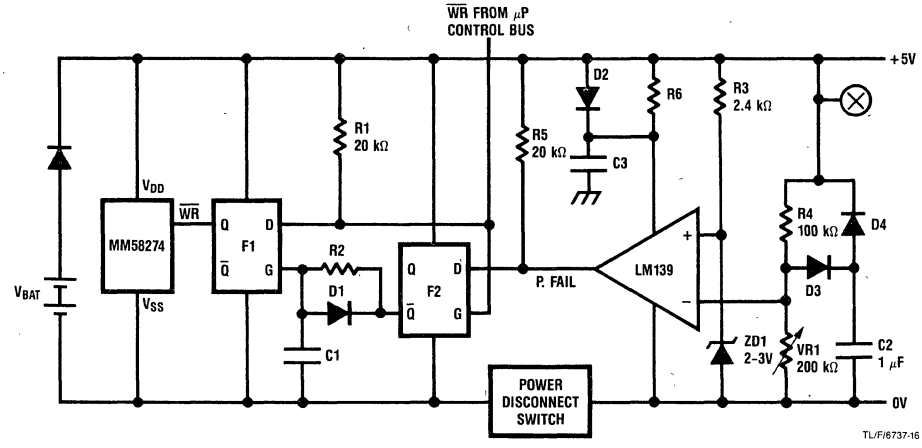


FIGURE 15. Power Supply Failure Detection and Write Protection Circuitry

As an alternative to F1 a permanently powered 74HC4066 analog switch could be used as the isolating component *(Figure 16)*. The 74HC4066 does not require pull-up resistors on its inputs as there are no internal CMOS buffers inside this device which must be controlled. The resistor on the WR line is for the benefit of the 74HC75.

Note that both of the devices mentioned must be permanently powered from the battery to be useful in this way. Unused gates in any such device must *NOT* be used in combinational logic that is not permanently powered. All unused inputs should be tied to V_{DD} or V_{SS} to render them inactive.

1.4.4 Switching Power Supplies

Switching power supplies are available which generate power failure signals. This signal may be adequate for direct use as a P. Fail line, but the manufacturer's information should be consulted to determine the suitability of a given power unit. P. Fail must still be gated with the Write signal for the clock, regardless of the actual detection method employed.

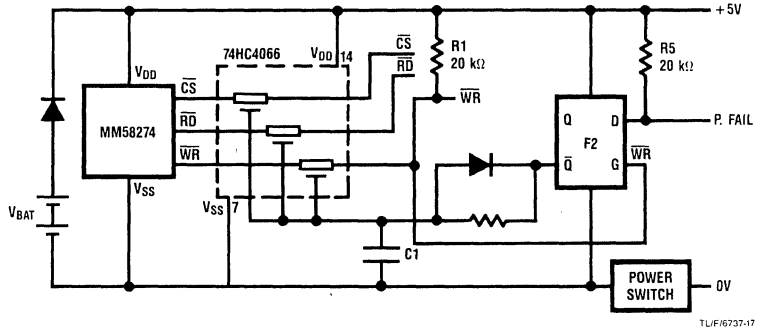


FIGURE 16. F1 Replaced by a 74HC4066 Analog Switch (Pull-Up Resistors Not Required on $\overline{CS}$ or $\overline{RD}$ Inputs)

1.4.3 Supply Pre-Sense

The same circuit of *Figure 15* can be used with unregulated supplies or other voltage lines which will fail before the 5V line. To achieve this, point X is connected to the sensed voltage instead of 5V, and the R4/VR1 ratio is adjusted to suit. The major benefit here is that advance warning of an impending 5V failure can be detected, allowing a pre-failure lockout signal to be generated.

Less precision is required to sense the unregulated supply than the system 5V supply. Consequently less complex circuitry can be used to do the detection and this is reflected in the circuit of *Figure 17*. Most 5V regulators will operate with an input voltage from 7V to 25V. Typically the input voltage is around 9V to 12V, giving some headroom. In *Figure 17* this voltage is high enough to drive a current through the Zener diode and turn on transistor TR1, holding P. FAIL low. R_{LIM} limits the Zener current. The Zener voltage is selected to switch off before the regulator fails, around 7.5V–8.5V depending on the time constant of the supply. With no current, TR1 switches off and R_P pulls P. Fail high.

When power is re-applied the 5V supply will stabilize before the Zener switches on, removing P. Fail. To provide a longer post-failure lockout period R_{LIM} could be replaced with two resistors and a diode/capacitor delay as in *Figure 15*.

Figure 18 is another extension of the same basic idea to provide an advance interrupt signal to allow μP housekeeping before the RTC (and CMOS RAM) is locked out. The extra rectifying components D1, C_t and R_t keep $\overline{NMI}$ off as long as input power is present. Time constant τ_2 is selected to be at 2–3 times faster than τ_1, the supply time constant. The interrupt signal is thus asserted before P. Fail.

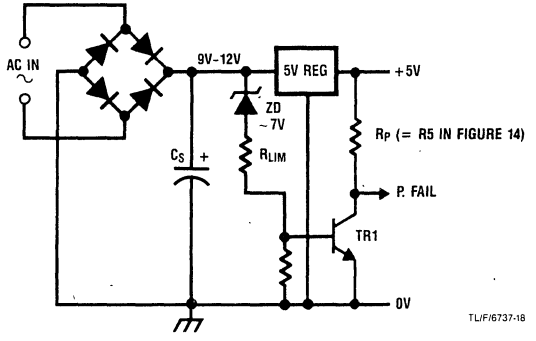


FIGURE 17. Power Fail Signal Generation from Unregulated Supplies

1.4.5 Summary

The general guidelines for power fail protection are:

1. Physically isolate the WR input to the clock. The μP cannot be relied upon to logically operate the isolation mechanism.
2. The clock should be isolated before the 5V power line starts to fail, and stay isolated until after it has re-established.
3. Consider the action of the sensing and protection circuitry if the supplies oscillate or if a momentary glitch occurs.

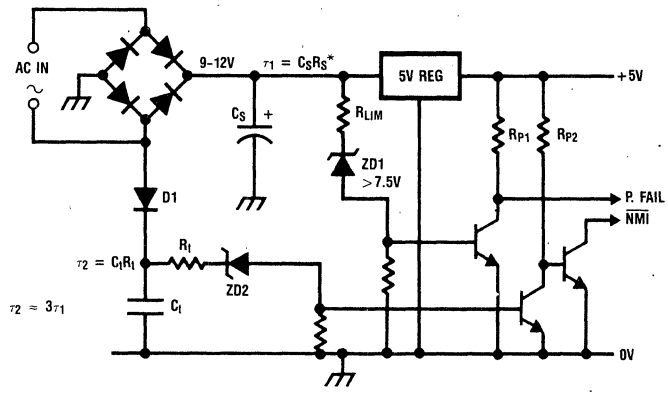


FIGURE 18. Power Fail Circuit with μP Housekeeping Interrupt

4. The Power Fail signal must be gated with Write strobes to the RTC. A foreshortened Write may also cause data corruption.
5. Logic components (and ICs in general) should be avoided when designing power failure schemes. Discrete components are far more predictable in their performance when the power supplies are not well defined. The exception to this general rule is when using permanently powered HCMOS logic devices. They will function in a reliable manner down to 2V.

System-powered logic devices cannot be relied on for power failure or Write isolation (not even CMOS).

2.0 SOFTWARE

2.1 DATA VALIDATION

The MM58274 data sheet describes in some detail three different methods of reading the clock and validating the real-time data. These techniques are reproduced in Appendix A-1. Rather than repeating the data sheet examples, this applications note examines the principles that lie behind the techniques suggested.

The basic problem is that the μP must somehow be synchronized with the changes in real-time in order to read valid data. This synchronization can either be done prior to reading the time data (pre-read), or after reading the data (post-read synchronization).

2.1.1 Post-Read Synchronization

Using the Data-Changed Flag (DCF) or the lowest order time register as outlined in the appendix: Time Reading using DCF and Time Reading with very slow Read cycles; are both examples of post-read synchronization.

What this means is that the data is read out first, and then verified. This is achieved by defining a random time-slot, started by the first DCF or low order register read, and ended by the second such read. If DCF has not been set during the time-slot or the lowest order register has not changed, then no real-time change occurred during that time-slot. All real-time reads during the time-slot are thus guaranteed.

2.1.2 Pre-Read Synchronization

The Interrupt Timer technique uses pre-read synchronization. Once it has been initialized as described, the interrupt timer times out just after the real-time data has changed. Thus the μP is guaranteed a full 100 ms period in which to read the time counters before the next change occurs.

The interrupt timer has to be synchronized with the real-time counters because it is an independent unit which may be started and stopped at any time by the μP. This software synchronization is achieved by using another pre-read technique. The timer is set up and ready to go, but then the μP waits for DCF to occur before issuing the start command. The same technique could be used to actually read the time-data, but post-read synchronization is faster.

2.2 INTERRUPT AS A 'DATA-CHANGED' FLAG

DCF is set every 100 ms when the 1/10ths of seconds counter is changed. When the time is only being read to the nearest second or minute, it would be useful to have a flag which is only set by a change in the lowest order counter being used.

If the interrupt output from the clock is not being used, the timer can be used as a programmable data-changed flag. To achieve this, the timer is set up and started in exactly the same way as described for interrupt time reading *(Appendix A-1)*. The interrupt output however, should be left unconnected. When reading the real-time data, the technique used is the same as for the normal Data-Changed Flag except that the Interrupt Flag is tested instead of DCF.

Note that the lowest order real-time register which is to be read out should be used to initially synchronize the counter. The interrupt timer is started when the real-time counter value is seen to change.

2.3 WRITING WITHOUT HALTING TIME-KEEPING

For most purposes the RTC should be halted when the time is being set, especially if large numbers of counters are

being updated. The clock can also then be re-started in synchronism with an external time reference. If only a few counters are to be altered and the clock is already synchronized, then this can be done without stopping the clock. An example of a minor change which may be undertaken in this way is daylight savings (winter/summer change of hour).

The problem to be overcome when writing in this way is that the write strobe may coincide with a time change pulse. As the time counters are synchronous, the 100 ms clock pulse is fed to each one. Writing to one counter may cause a spurious carry to be generated from that counter, causing the next one up the chain to be incremented.

Since a spurious carry will only affect the next counter if it coincides with a time update pulse, the solution is once again to synchronize clock access with the real-time change. The most suitable method for this is pre-read synchronization. In other words, the μP must wait for DCF to be set before starting to write data to the clock, giving a guaranteed 100 ms period for writing.

2.4 THE CLOCK AS A μP WATCHDOG

The interrupt timer can be used as a μP watchdog circuit, operating on a non-maskable interrupt input to the μP. The timer is set up in either single or repeat interrupt mode for the watchdog period required: 0.1s, 0.5s or 1 second are probably the most useful times for this. Synchronization with real-time is not required.

In the main program loop the μP writes to the clock, stopping and then re-starting the interrupt timer. The timer period selected will depend on how long the main loop takes to execute. As long as the μP continues to execute the loop, no time-outs occur and no interrupts are generated. If the μP fails for some reason to reset the timer, it eventually times out, generating the initializing interrupt to restore operations.

2.5 THE JAPANESE CALENDAR

Because the MM58274 has a programmable leap year counter, this allows the possibility of programming for the Japanese Showa calendar. The Japanese calendar counts years from the time that the present Japanese Emperor comes to power. Emperor Hirohito took office in 1926 (Showa year 1), hence 1984 is Showa year 59. Since the days and months of Showa follow the Gregorian pattern, Showa year 59 is also a leap year.

The normal law for the MM58274 is to program 'the number of years since last leap year.' This remains the same whether the clock is loaded with the Gregorian or Showa year. When software is used to calculate the leap year count value from the year, then the formula used must be modified.

The formula for the Gregorian year is:

Leap Year Value = [Gregorian Year/4] REMAINDER

Whereas for the Showa year the formula is:

Leap Year Value = [(Showa Year + 1)/4] REMAINDER

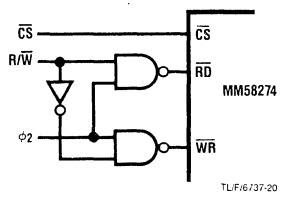
Leap Year Value is the number from 0 to 3 which is written into the leap year counter, and is the REMAINDER of the integer calculations shown above.

3.0 MISCELLANY

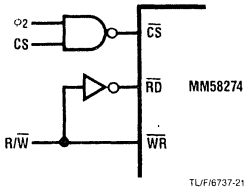
3.1 CONNECTION TO NON Microbus™ SYSTEMS

Adding the MM58274 to non Microbus processors is made fairly straightforward because of the flexibility of the control signal timing. *Figure 19* shows two examples of logic to connect the clock to a 6502/6800 microprocessor bus.

Figure 19a the $\overline{RD}$ and $\overline{WR}$ inputs are strobed, generating reasonably typical Microbus type control signals. In *Figure 19b,* CS is used as the strobe signal. There is no particular advantage to either circuit, they are just variations on the same theme. This circuit flexibility may be used to advantage to save SSI packages in the board design.



a)



b)

FIGURE 19. 6800/6502 μP Bus Interface

3.2 TEST MODE

Test Mode is used by National Semiconductor when the MM58274 is tested during manufacture. It enables the real-time counters to be clocked rapidly through their full count sequence.

The MM58274 counters are clocked synchronously to simplify μP access, with ripple carry signals from each counter to the next. In Test Mode some of these carries are intercepted and permanently asserted causing the counters to count each clock pulse. The prescaler is also bypassed so that the counters count every clock applied to the Osc In pin. The Test Mode counter connection is shown in *Figure 20.*

If Test Mode is to be used for incoming inspection or device verification, then the clock waveform of *Figure 21* should be applied to the oscillator input (Osc In, pin 15). The MM58274 uses semi-dynamic flip-flops in the counters which are only fully static when the oscillator input is high. Thus *Figure 21* shows that the oscillator waveform is normally high, pulsing low to clock the real-time counters. The time data in the counters changes on the rising edge of Osc In.

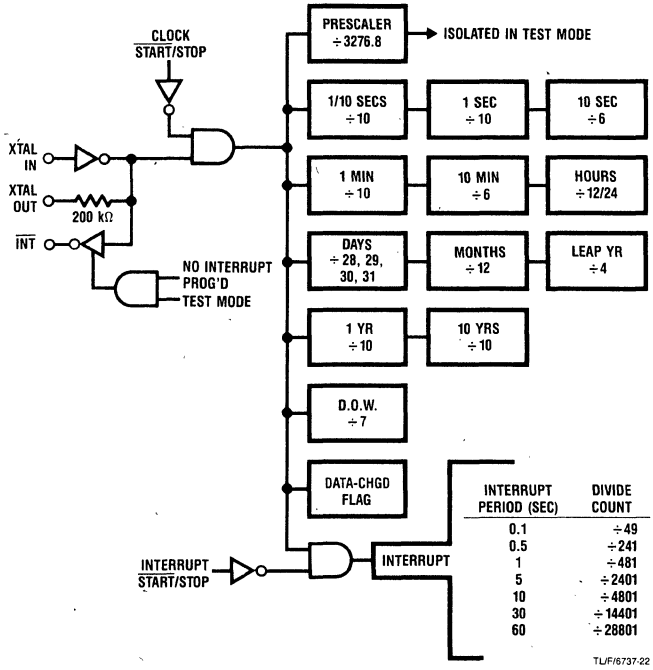


FIGURE 20. Test Mode Interconnection Diagram of Internal Counter Stages

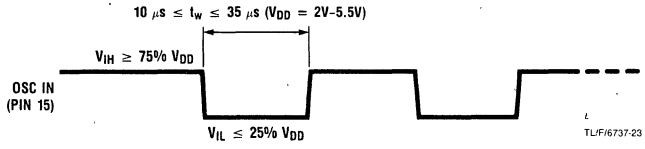


FIGURE 21. Oscillator Waveform for Counter Clocking in Test Mode

The pulse width limits for reliable clocking are shown on the diagram. When running with a 32 kHz crystal, the normal pulse width is 15.26 μs. With no forcing input, the oscillator will self bias to around 2.5V (V_{DD} = 5V). While a few hundred mV swing above and below this level is sufficient to drive the oscillator, for guaranteed test clocking the input should swing between $V_{IH} \geq 75\%\ V_{DD}$ and $V_{IL} \leq 25\%\ V_{DD}$.

3.3 TEST MODE AND OSCILLATOR SETTING

When Test Mode is used to set the oscillator frequency, the interrupt timer must be disabled (interrupt register programmed with all 0s) for the oscillator frequency to appear on the interrupt output. No test equipment should be connected directly to either oscillator pin, as the added loading will alter the characteristics of the oscillator making precise tuning impossible.

Note that oscillator frequency will vary slightly as the supply varies between operating and standby voltages. Typically this variation will be around ±6 seconds per month ($V_{STANDBY}$ = 2.4V), slowing at standby voltage. When the clock will spend the greater part of its working life in standby mode, it may prove worthwhile to correct for this in the tuning. This can be done by tuning at standby voltage (by writing the RTC into test mode, then disconnecting it from the system to tune on battery backup). Alternatively, the clock can be slightly overtuned at operational voltage, tuning to 32.7681 kHz.

In a similar way, where the RTC spends equal amounts of time in both operational and standby modes (i.e., powered by day, standby at night), the oscillator may be tuned somewhere between the two conditions. Following these tuning suggestions will not eliminate time-keeping errors, but they will help in minimizing them.

Time-keeping accuracy cannot be exactly specified. It depends on the quality of the components used in the oscillator circuit and their physical layout, also the stability of the supply voltage, the variations in ambient temperature, etc. With good components and a reasonably stable environment however, time-keeping accuracy to within 4 seconds/month can be achieved, although 8 seconds/month is somewhat more typical in practical systems.

3.4 UPGRADING AN MM58174A SYSTEM WITH THE MM58274

The MM58274 has the same pin-out as the MM58174A and can be used as a direct replacement, with certain reserva-

tions. The two devices are not quite the same in their external circuit appearances, and this is reflected in their applications circuits. In addition, the MM58274 is not software compatible with the MM58174A, requiring a change in the operating system to use the MM58274.

Figure 22 shows the circuit diagram for the MM58174A system connection. There are two major differences between this and the MM58274 diagram *(Figure 1);* a) the oscillator circuit and b) the supply disconnection scheme.

The change of pin of the tuning capacitor (from Osc Out to Osc In) is not critical.

b) The Supply Disconnection Scheme

The MM58174A uses mostly pull-down devices on its μP inputs to pull the inputs to CMOS levels, and so the 5V power line is disconnected on this device. The two exceptions to this are the $\overline{CS}$ and $\overline{WR}$ inputs which have pull-up resistors to inactivate the internal write strobe. As *Figure 5a* shows, there is a leakage path through these pins, which in most MM58174A installations are individually isolated.

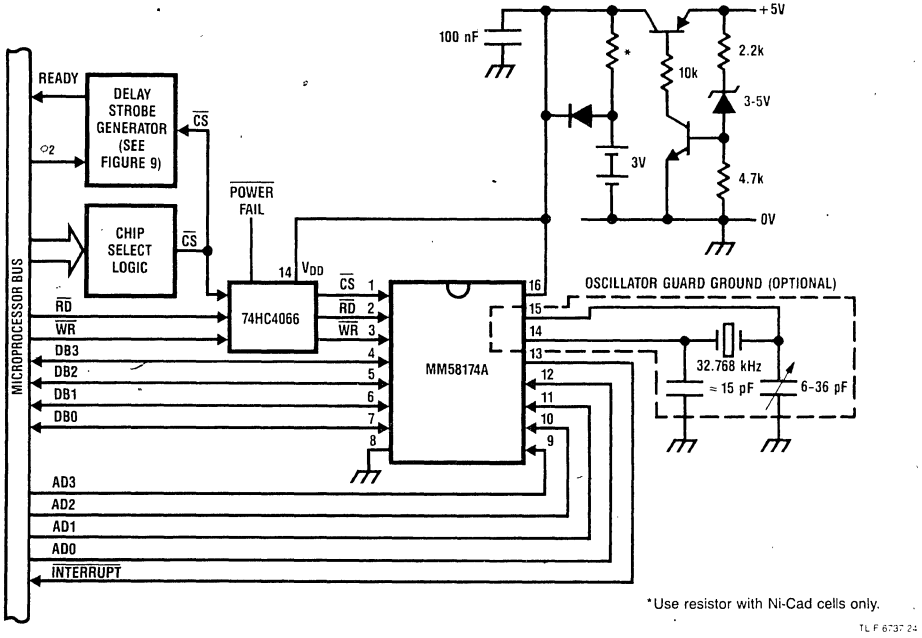


FIGURE 22. MM58174A System Installation

a) The Oscillator Circuit

The MM58274 normally operates with an 18 pF–20 pF fixed loading capacitor as opposed to the 15 pF of the MM58174A. This is a reflection of the greater internal capacitance of the MM58174A, rather than any change in the characteristics of the oscillator itself. The MM58274 will operate using a 15 pF capacitor, but the oscillator will probably need to be retrimmed.

Operating with a 15 pF capacitor will make the oscillator more sensitive to changes in the environment, i.e., temperature, voltage, moisture, etc. This will result in lower accuracy in time-keeping. The oscillator is more prone to stopping at low voltage. Oscillation would normally be maintained down to 1.8V–1.9V (although not guaranteed); with a 15 pF load it may only oscillate down to 2.0V–2.1V. It is thus important to check the battery regularly and replace it before the RTC voltage falls below 2.2V.

Where possible the 15 pF capacitor should be replaced by an 18 pF–20 pF capacitor (anywhere in the range 18 pF–20 pF is adequate), or a second 3 pF–5 pF capacitor may be added in parallel with the 15 pF.*

The largest penalty in inserting an MM58274 into an MM58174A circuit is the battery current that is lost through the pull-up devices. This will increase the typical supply current from 4 μA to 50–100 μA and it is up to the individual user to decide whether or not this drain is tolerable in a particular application.

The most important requirement is that the $\overline{WR}$ input should be electrically isolated or current leakage through pin inputs may force the inputs low enough to cause spurious writes to occur. Since it is already customary to isolate these inputs for the MM58174A, this may not be a problem. Where this has not been done, either the circuit will have to be modified or the $\overline{WR}$ PCB track can be cut and a switch or some extra circuitry added to allow isolation.

Note that power fail disconnection and input isolation may be achieved using the same components. In *Figure 22* the MM74HC4066 analog switch will do both jobs.

The current drained by the input pull-ups may be minimized with some attention to the data/address driving devices. It is

*When components have been soldered into the oscillator circuit, allow the circuit to cool to room temperature before attempting to retune the oscillator.

often possible to replace LSTTL devices with standard 7400 series devices and reduce the leakage (at the cost of some increase in operating current). Many 7400 series device outputs lack diodes in the right places to pass leakage currents. LSTTL devices will, for the main part, have these diodes. CMOS devices will always have diodes to both power rails on inputs and outputs.

There is no hard and fast rule for this. Where devices from one manufacturer work, the same part from a different one may not. Some trial and error experimentation may prove worthwhile in selecting devices.

3.5 WAIT STATE GENERATION FOR FAST μPs

Although the MM58274 has faster access times than the MM58174A, in many cases, the μP will be too fast to directly access the RTC. *Figure 23* shows a circuit which will produce wait states of any length required to enable the RTC to be accessed, using the 74HC74 dual D-type flip-flop.

The RTC $\overline{CS}$ signal clocks up a logic 1 on the Q output of the first F/F, removing the Preset from all the other F/Fs and pulling the μP WAIT line low, via the transistor. The other F/Fs 1 to n, form a shift register clocked by the ϕ_2 system clock.

After n ϕ_2 clocks (where n is the number of flip-flops in the shift register) a logic 0 shifts out from the nth F/F, resetting the main flip-flop. The main F/F then presets the shift register and clears the WAIT signal, ready for the next $\overline{CS}$ edge to repeat the cycle. On power-up the delay generator will initialize itself after a maximum of n system clocks have occurred so no reset signal is required. Some μPs demand that a $\overline{WAIT}$/READY input is synchronized with ϕ_2 of the system clock. This can readily be achieved by selecting the correct ϕ_2 edge as the clock signal for the shift register chain.

FLIP-FLOP — MM74HC74 D-TYPE LATCH

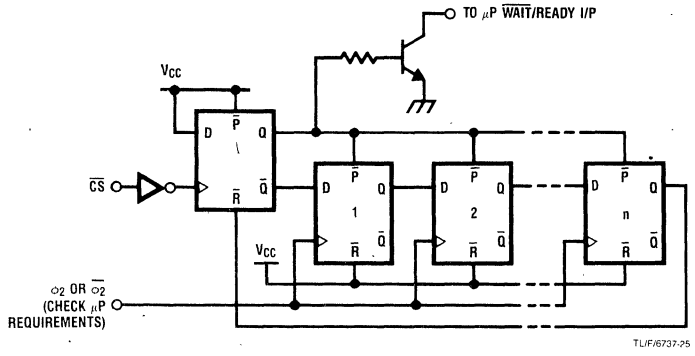


FIGURE 23. Access Delay Generator (Clocked Wait State Generator)

APPENDIX A-1. READING VALID REAL-TIME DATA

TIME READING USING DCF

Using the Data-Changed Flag (DCF) technique supports microprocessors with block move facilities, as all the necessary time data may be read sequentially and then tested for validity as shown below.

1) Read the control register, address 0: *This is a dummy read to reset the data-changed flag (DCF) prior to reading the time registers.*
2) Read time registers: *All desired time registers are read out in a block.*
3) Read the control register and test DCF: *If DCF is still clear (logic 0), then no clock setting pulses have occurred since step 1. All time data is guaranteed good and time reading is complete.*

If DCF is set (logic 1), then a time change has occurred since step 1 and time data may not be consistent. Repeat steps 2 and 3 until DCF is clear. The control read of step 3 will have reset DCF, automatically repeating the step 1 action.

TIME READING USING AN INTERRUPT

In systems such as point-of-sale terminals and data loggers, time reading is usually only required on a random demand basis. Using the data-changed flag as outlined above is ideal for this type of system. Where the μP must respond to any change in real-time (e.g., industrial timers/process controllers, TV/VCR clocks or any system where real-time is displayed) then the interrupt timer may be for time reading. Software is used to synchronize the interrupt timer with the time changing as outlined below:

1) Select the interrupt register (write 2 or 3 to ADDR0).
2) Program for repeated interrupts of the desired time interval (see Table IIB in *Appendix A-2): Do not start the timer yet.*
3) Read control register AD0: *This is a dummy read to reset the data-changed flag.*
4) Read control register AD0 repeatedly until data-changed flag is set.
5) Write 0 or 2 to control register. Interrupt timing commences.

When interrupt occurs, read out all required time data. There is no need to test DCF as the interrupt 'pre-synchronizes' the time reading already. The interrupt flag is automatically reset by reading from ADDR0 to test it. In repeat interrupt mode, the timer continues to run with no further μP intervention necessary.

TIME READING WITH VERY SLOW READ CYCLES

If a system takes longer than 100 ms to complete reading of all the necessary time registers (e.g., when CMOS processors are used or where high level interpreted language routines are used) then the data-changed flag will always be set when tested and is of no value. In this case, the time registers themselves must be tested to ensure data accuracy.

The technique below will detect both time changing *between* read strobes (i.e., between reading tens of minutes and units of hours) and also time changing *during* read, which can produce invalid data.

1) Read and store the value of the *lowest* order time register required.
2) Read out all the time registers required. The registers may be read out in any order, simplifying software requirements.
3) Re-read the lowest order register and compare it with the value stored previously in step 1. If it is still the same, then all time data is good. If it has changed, then store the new value and go back to step 2.

In general, the rule is that the first and last reads *must* both be of the lowest order time register. These two values can then be compared to ensure that no change has occurred. This technique works because for any higher order time register to change, all the lower order registers must also change. If the lowest order register does not change, then no other register has changed either.

APPENDIX A-2. FUNCTIONAL TRUTH TABLES FOR MM58274

TABLE I. Address Decoding for Internal Registers

Register Selected	Address Bits				Access
	AD3	AD2	AD1	AD0	
0 Control Register	0	0	0	0	Split Read and Write
1 Tenths of Secs	0	0	0	1	Read Only
2 Units Seconds	0	0	1	0	R/W
3 Tens Seconds	0	0	1	1	R/W
4 Units Minutes	0	1	0	0	R/W
5 Tens Minutes	0	1	0	1	R/W
6 Units Hours	0	1	1	0	R/W
7 Tens Hours	0	1	1	1	R/W
8 Units Days	1	0	0	0	R/W
9 Tens Days	1	0	0	1	R/W
10 Units Months	1	0	1	0	R/W
11 Tens Months	1	0	1	1	R/W
12 Units Years	1	1	0	0	R/W
13 Tens Years	1	1	0	1	R/W
14 Day of Week	1	1	1	0	R/W
15 Clock Setting/Interrupt Registers	1	1	1	1	R/W

TABLE IIA. Clock Setting Register Layout

Function	Data Bits Used				Comments	Access
	DB3	DB2	DB1	DB0		
Leap Year Counter	X	X			0 indicates a Leap Year	R/W
AM/PM Indicator (12 Hour Mode)			X		0 = AM 1 = PM 0 in 24 Hour Mode	R/W
12–24 Hour Select Bit				X	0 = 12 Hour Mode 1 = 24 Hour Mode	R/W

TABLE IIB. Interrupt Control Register

Function	Comments	Control Word			
		DB3	DB2	DB1	DB0
No Interrupt	Interrupt output cleared, Start/Stop bit set to 1.	X	0	0	0
0.1 Second		0/1	0	0	1
0.5 Second		0/1	0	1	0
1 Second		0/1	0	1	1
5 Seconds		0/1	1	0	0
10 Seconds		0/1	1	0	1
30 Seconds		0/1	1	1	0
60 Seconds		0/1	1	1	1

Timing Accuracy: —
Single Interrupt Mode (all time delays): ±1 ms
Repeated Mode: ±1 ms on initial timeout, thereafter synchronous with first interrupt (i.e., timing errors do not accumulate).

DB3 = 0 for Single Interrupt DB3 = 1 for Repeated Interrupt

TABLE III. The Control Register Layout

Access (ADDR0)	DB3	DB2	DB1	DB0
Read From:	Data Changed Flag	0	0	Interrupt Flag
Write To:	Test	Clock Start/Stop	Interrupt Select	Interrupt Start/Stop
	0 = Normal 1 = Test Mode	0 = Clock Run 1 = Clock Stop	0 = Clk. Set Reg. 1 = Int. Reg.	0 = Int. Run 1 = Int. Stop

An Introduction to and Comparison of 54HCT/74HCT TTL Compatible CMOS Logic

National Semiconductor
Application Note 368
Larry Wakeman
March 1984

The 54HC/74HC series of high speed CMOS logic is unique in that it has a sub-family of components, designated 54HCT/74HCT. Generally, when one encounters a 54/74 series number, the following letters designate some speed and power performance, usually determined by the technology used. Of course, the letters HC designate high speed CMOS with the same pinouts and functions as 54LS/74LS series. The sub-family of HC, called HCT, is nearly identical to HC with the exception that its input levels are compatible with TTL logic levels.

This simple difference can, however, lead to some confusion as to why HCT is needed; how HCT should be used; how it is implemented; when it should be used; and how its performance compares to HC or LS. This paper will attempt to answer these questions.

It should also be noted that not all HCTs are the same. That is, HCTs from other vendors may have some characteristics that are different. Thus, when discussing general characteristics this paper will directly address National Semiconductor's 54HCT/74HCT which is compatible with **JEDEC standard 7**. Other vendors' ICs which also meet this standard will probably have similar characteristics.

WHY DOES HCT EXIST?

Ideally, when a designer sits down to design a low power high speed system, he would like to use 54HC/74HC, and CMOS LSI components. Unfortunately, due to system requirements he may have to use NMOS microprocessors and their NMOS or bipolar peripherals or bipolar logic (54S/74S, 54F/74F, 54ALS/74ALS, or 54AS/74AS) because either the specific function does not exist in CMOS or the CMOS device may not have adequate performance. Since the system designer still desires to use HC where possible, he will mix HC with these products. If these devices are specified to be TTL compatible, incompatibilities may result at the interface between the TTL, NMOS, etc. and HC.

More specifically, in the case of where a TTL or NMOS output may drive an HC input, a specification incompatibility results. Table I lists the output drive specifications of TTL compatible outputs with the input specifications of 54HC/74HC. Notice that the output high level of a TTL specified device will not be guaranteed to have a logic high output voltage level that will be guaranteed to be recognized as a valid logic high input level by HC. A TTL output will be equal to or greater than 2.4V, but an HCMOS input needs at least 3.15V. It should be noted that in an actual application the TTL output will pull-up probably to about V_{CC} minus 2 diode voltages, and HC will accept voltages as low as 3V as a valid one level so that in almost all cases there is no problem driving HC with TTL.

Even with the specified incompatibility, it is possible to improve the TTL-CMOS interface without using HCT. *Figure 1* illustrates this solution. By merely tying a pull-up resistor from the TTL output to V_{CC}, this will force the output high voltage to go to V_{CC}. Thus, HC can be directly interfaced very easily to TTL. This works very well for systems with a few lines requiring pull-ups, but for many interfacing lines, HCT will be a better solution.

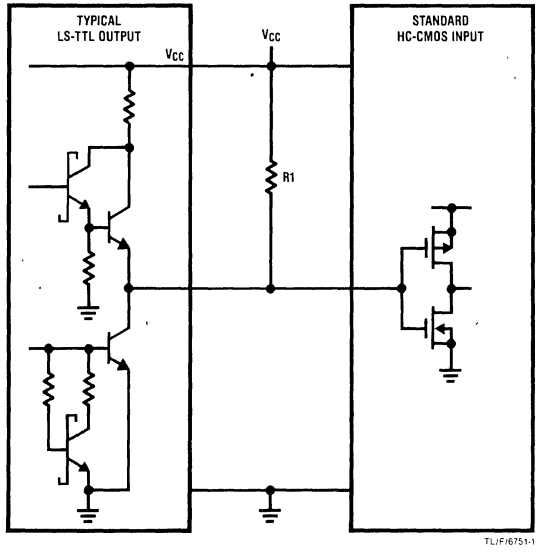


FIGURE 1. Interfacing LS-TTL Outputs to Standard CMOS Inputs Using a Pull-Up Resistor

The input high logic level of HC is the only source of incompatibility. 54HC/74HC can drive TTL easily and its input low level is TTL compatible. Again referring to Table I, the logic output of the TTL type device will be recognized to be a valid logic low (0) level, so there is no incompatibility here. Table II shows that the specified output drive of HC is capable of driving many LS-TTL inputs, so there is no incompatibility here either (although one should be aware of possible fanout restrictions similar to that encountered when designing with TTL).

The question then arises: since only the input high level must be altered, why not design CMOS logic to be TTL compatible? 54HC/74HC was designed to optimize performance in all areas, and making a completely TTL compatible logic family would sacrifice significant performance. Most importantly, there is a large loss of AC noise immunity, and there are speed and/or die size penalties when trying to design for TTL input levels.

Thus, since it is obvious that there is a need to interface with TTL and TTL compatible logic, yet optimum performance would be sacrificed, a limited sub-family of HCT devices was created. It is completely TTL input compatible, which enables guaranteed direct connection of TTL outputs to its inputs. In addition, HCT still provides many of the other advantages of 54HC/74HC.

WHEN TO USE 54HCT/74HCT LOGIC

The 54HCT/74HCT devices are primarily intended to be used to provide an easy method of interfacing between TTL compatible microprocessor and associated peripherals and bipolar TTL logic to 54HC/74HC. There are essentially two application areas where a designer will want to perform this interface.

1. The first case is illustrated in *Figure 2*. In this case the system is a TTL compatible microprocessor. This figure shows an NS16XXX (any NMOS μP may be substituted) that is in a typical system and therefore must be interfaced to 54HC/74HC. In this instance, the popular gate, buffer, decoder, and flip-flop functions provided in the 54HCT/74HCT sub-family can be used to interface the many lines that come from TTL compatible outputs. It is also easy to upgrade this configuration to an *all* CMOS system once the CMOS version of the microprocessor is available by replacing the HCT with HC.

2. A second application is, when in speed-critical situations a faster logic element than HC, probably ALS or AS, must be used in a predominantly 54HC/74HC system, or a specific logic function unique to TTL is placed into an HC design. This situation is illustrated in *Figure 3*. In this case, pull-up resistors on an HC input may be sufficient, but if not, then an HCT can be used to provide the guaranteed interface.

TABLE I. Output Specifications for LS-TTL and NMOS LSI Compared to the Input Specifications for HCT and HC

Note the specified incompatibility between the output levels HC input levels.

	LS Output		NMOS Output		HC Inputs		HCT Input		
	V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}	V_{IN}	I_{IN}	V_{IN}	I_{IN}	
Output High	2.7V	400 μA	2.4V	400 μA	3.15V	1 μA	2.0V	1 μA	Input High
Output Low	0.5V	8.0 mA	0.4V	2.0 mA	0.9V	1 μA	0.8V	1 μA	Input

$V_{CC} = 4.5V$

TABLE II. 54HC/74HC and 54HCT/74HCT Output Specifications Compared to 54LS/74LS TTL Input Specifications and Showing Fanout

Both HC and HCT output specifications are the same for the two sets of output types.

		HC Output		HCT Output		LS Inputs		
		V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}	V_{IN}	I_{IN}	Fanout
Standard Output	Output High	3.7V	4.0 mA	3.7V	4.0 mA	2.0V	40 μA	10
	Output Low	0.4V	4.0 mA	0.4V	4.0 mA	0.8V	400 μA	
Bus Output	Output High	3.7V	6.0 mA	3.7V	6.0 mA	2.0V	40 μA	15
	Output Low	0.4V	6.0 mA	0.4V	6.0 mA	0.8V	400 μA	

$V_{CC} = 4.5V$

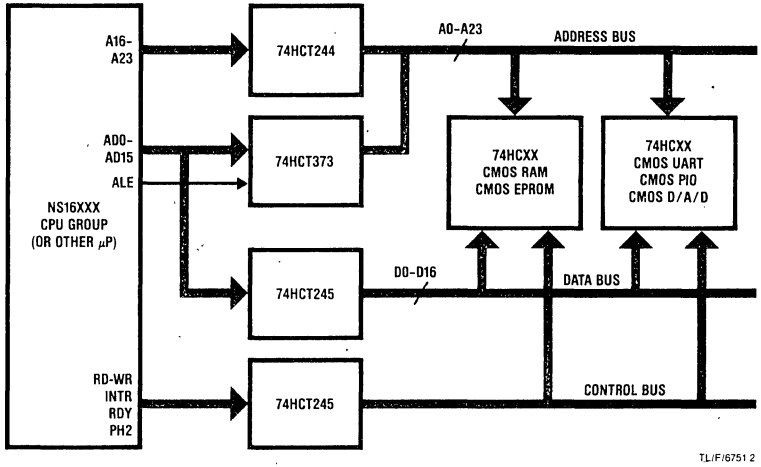


FIGURE 2. Applications Where a TTL Compatible NMOS Microprocessor is Interfaced to a CMOS System

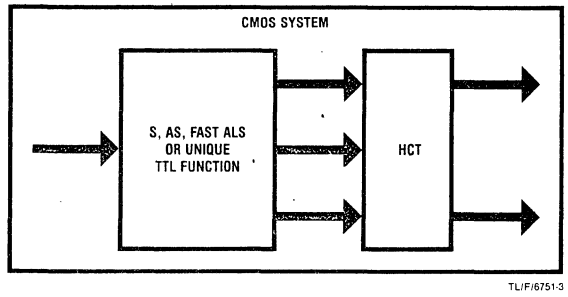


FIGURE 3. A Conceptual Diagram Showing How HCT May Be Used to Interface a Faster ALS Part or Some Unique TTL Function in a CMOS System

The functions chosen for implementation in 54HCT/74HCT were chosen to avoid the undesirable situation where the designer is forced to add in an extra gate solely for the interface. A variety of HCT functions are provided to not only interface to HC, but to perform the desired logic function at the same time.

Although not the primary intention, a third use for 54HCT/74HCT is as a direct plug-in replacement for 54LS/74LS logic in already designed systems. If HCT is used to replace LS, power consumption can be greatly reduced, usually by a factor of 5 or so. This lower power consumption, and hence less heat dissipation, has the added advantage of increasing system reliability (in addition to the greater reliability of 54HC/74HC and 54HCT/74HCT). This is extremely useful in power-critical designs and may even offer the advantage of reduced power supply costs.

One note of caution: when plug-in replacing HCT for TTL, 54HCT/74HCT (as well as 54HC/74HC) does not have identical propagation delays to LS. Minor differences will occur, as would between any two vendors' LS products. To be safe, it is recommended that the designer verify that the performance of HCT is acceptable.

PERFORMANCE COMPARISON: HCT vs HC LS-TTL

To enable intelligent use of HCT in a design, both for the interface to NMOS or TTL and for TTL replacement applications, it is useful to compare the various performance parameters of HCT to those of HC and LS-TTL.

Input/Output Voltages and Currents

Table III tabulates the input voltages for LS-TTL and LS-TTL compatible ICs, HCT, and HC. Since HCT was designed to have TTL compatible inputs, its input voltage levels are the same. However, the input currents for HCT are the same as HC. This is an advantage over LS-TTL, since there are no fanout restrictions when driving into HCT as there are when driving into LS.

Referring to Table II, the output voltage and current specifications for HC and HCT gates are shown. As can be seen, the output specifications of HCT are identical to HC. This was chosen since the primary purpose of HCT is to drive into HC as the interface from other logic.

There are some differences as to how LS-TTL, ALS-TTL and AS-TTL outputs are specified when compared to HCT (or HC), as shown in Table IV. The military parts are easy to compare. HC/HCT has the same I_{OL} as LS and much greater I_{OH}. At the commercial temperature range a direct comparison is difficult. LS has a higher output current, but also a higher output voltage and narrow operating temperature range. Taking these into account, the output drive of 74HC/HCT is roughly the same as LS.

In the HC family, there is a higher output drive specified for bus compatible devices. Again, HCT is identical. As can be seen back in Table II, the bus drive capability of both HC and HCT are identical, and both source and sink currents are symmetrical. This increased drive over standard devices provides better delay times when they are used in high load capacitance bus organized CMOS systems.

Both HC and HCT also have another voltage/current specification which is applicable to CMOS systems. This is the no load output voltage. In CMOS systems, usually the DC output drive for a device need not be greater than several μA since all CMOS inputs are very high impedance. For this reason, there is a 20 μA output voltage specification which says that 54HC/74HC and 54HCT/74HCT will pull to within 100 mV of the supplies.

NOISE MARGIN TRADEOFFS WITH HCT

The nominal trip point voltage for an HCT device has been designed to be around 1.4V, as compared to the 2.5V for a standard HC device. This will degrade the ground level noise margin for HCT by almost a volt. HC, on the other hand, has its trip point set to offer optimal noise margin for both V_{CC} and ground.

This may be a minor point since normally HCT is mixed with TTL and in this case the worst-case system noise margin is defined by the TTL circuits. If the HCT is being driven only by HC and not LS, then the worst-case V_{CC} margin is determined by the HC devices. This is not a normal usage, but may occur if, for example, some spare HCT logic can be utilized by HC to save chip count. *Figure 4* graphs input noise margin for HC, HCT in an LS application and HCT being driven by HC. As one can see, the HC has a large V_{CC} and ground noise margin, the HCT interfacing from LS has a margin equal to LS, and the HCT interfacing from HC has a skewed margin.

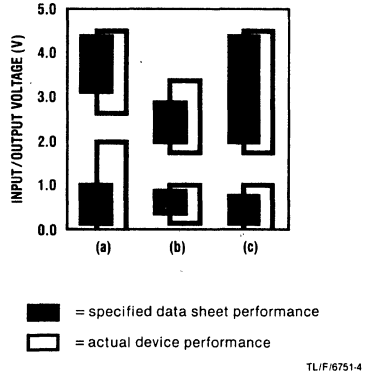


FIGURE 4. Guaranteed and Typical Noise Margins for a) HC b) HCT in TTL System c) HCT in HC System

TABLE III. A Comparison of Input Specifications for 54LS/74LS, NMOS-LSI, 54HC/74HC, and 54HCT/74HCT

The HCT specifications maintain the TTL compatible input voltage requirements and the HC input currents.

	LS Inputs		NMOS-LSI Input		HC Inputs		HCT Input	
	V_{IN}	I_{IN}	V_{OUT}	I_{OUT}	V_{IN}	I_{IN}	V_{IN}	I_{IN}
Input High	2.0V	40 μA	2.0V	10 μA	3.15V	1 μA	2.0V	1 μA
Input Low	0.8V	400 μA	0.8V	10 μA	0.9V	1 μA	0.8V	1 μA

V_{CC} = 4.5V

TABLE IV. This Compares the Output Drive of HC and HCT to LS for both the Military Temperature Range and the Commercial Temperature Range Devices at Rated Output Currents

	Military Temperature				Commercial Temperature*			
	HC/HCT Output		LS Output		HC/HCT Output		LS Output	
	V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}	V_{OUT}	I_{OUT}
Input High	3.7V	4.0 mA	2.5V	400 μA	3.84V	4.0 mA	2.7V	400 μA
Input Low	0.4V	4.0 mA	0.4V	4.0 mA	0.33V	4.0 mA	0.5V	8.0 mA

V_{CC} = 4.5V

*The commercial temperature range for HC/HCT is −40°C to +85°C, but for LS it is 0°C to 70°C.

POWER CONSUMPTION OF HCT

In normal HC applications, power consumption is essentially zero in the quiescent state but is proportional to operating frequency when operating. In LS, large quiescent currents flow which overshadow (except at very high frequencies) other dynamic components. 54HCT/74HCT is a combination of these, depending on the application. Both quiescent and frequency-dependent power can be significant.

Referring back to *Figure 1*, this figure shows an LS-TTL output driving an HCT input. To see how quiescent current is drawn, notice that it is possible to have valid TTL voltages of 2.7V and 0.4V (ignoring the pull-up resistor). With 0.4V on the HCT input, we find the input N-channel transistor OFF and the P-channel ON. Thus, the output of this stage is high. Also, since one of the P or N-channel transistors is OFF, no quiescent current flows. However, when the HCT input is high, 2.7V, the N-channel is ON and the P channel is slightly ON. This will cause some current to flow through both the transistors, even in the static state.

Thus in a TTL application, HCT has the unusual characteristic that it will draw static current only when its inputs are driven by TTL (and TTL-like) outputs, and only when those outputs are high. Thus, to calculate total power, this quiescent power must be summed with the frequency-dependent component.

When HCT is driven by HC, as it possibly might be, the HC outputs will have high and low levels of V_{CC} and ground; never statically turning on both transistors simultaneously. Thus in this application, HCT will only dissipate frequency-dependent power, and C_{PD} calculations can be made to determine power (see National Semiconductor application note, AN-303). In the latter application, HCT will dissipate the same amount of power as HC; in the first TTL application, the power dissipated will be more since there is also a DC component.

To show this, *Figure 5* plots power versus frequency for an HCT00 being driven by HC, typical LS and worst-case LS. Notice that at the lower frequencies, the DC component for the TTL input is much greater; at higher frequencies, the two converge as the dynamic component becomes dominant.

SPEED/PROPAGATION DELAY PERFORMANCE

Of primary importance is the speed at which the components operate in a system. HCT was designed to have the same basic speeds as HC. This was accomplished in spite of the fact that HCT requires the addition of a TTL input translator, which will add to internal propagation delays. A second concern in the design was to maintain the required speeds while minimizing the possible power consumption of the input stage when driven TTL high levels.

These requirements dictated designing HCT on a slightly more advanced 3μ N-well process, as well as increasing the die to help compensate for speed loss. This process is slightly faster than the standard HC process, and this enables the HCT parts to have the same delays as their HC counterparts, while minimizing possible quiescent currents. *Figure 6* shows a comparison of 74HCT240 and 74HC240 propagation delays, and they are identical.

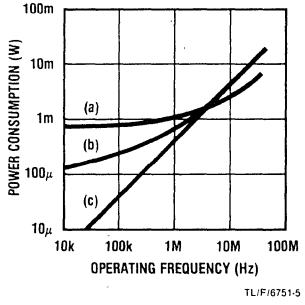


FIGURE 5. Power Consumption of 74HCT00 Being Driven by a) Worst-Case TTL Levels b) Typical TTL Levels c) CMOS Levels

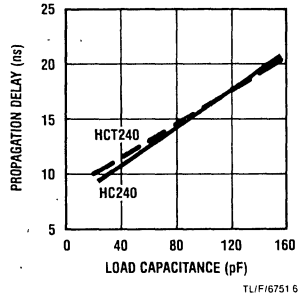


FIGURE 6. Typical Propagation Delay vs Load for 74HC240 and 74HCT240 Are Virtually the Same. Slight Differences Result from Different Design and Processing.

One interesting point is that HCT and HC speed specifications are measured differently. One can compare the AC test waveforms in the HC databook and see that HC is measured with 0V-5V input waveforms and using 2.5V points on these waveforms. HCT, on the other hand, is tested like LS-TTL. HCT's input waveforms are 0V-3V and timing is measured using the 1.3V on both the input and the output waveforms.

The different test conditions for HCT result because HCT will be primarily usd in LS-TTL applications. If HCT is used in HC systems, the actual speeds will be slightly different, but the differences will be small (<1 ns-2 ns).

HC and HCT speeds are not identical to LS-TTL. Some delays will be faster and some slightly slower. This is due to inherent differences in designing with CMOS versus bipolar logic. For an average system implemented in HC or LS-TTL, the same overall performance will result. On an individual part basis, some speeds will differ, so the designer should not blindly assume that HC or HCT will duplicate whatever a TTL IC does.

CMOS LATCH-UP AND ELECTROSTATIC DISCHARGE OF 54HCT/74HCT

These two phenomena are not strictly performance related in the same sense that speed or noise immunity are. Instead, latch-up and electrostatic discharge (ESD) immunity impact the ease of design, insusceptibility to spurious or transient signals causing a failure, and general reliability of 54HCT/74HCT.

Latch-up is a phenomenon that is a traditional problem with older CMOS families; however, as with 54HC/74HC, latch-up has been eliminated in 54HCT/74HCT circuits. In older CMOS, it is caused by forward biasing any protection diode on either an IC's input or output. If enough current flows through the diode (as low as 10 mA), then it is possible to trigger a parasitic SCR (four layer diode) within the IC that will cause the V_{CC} and ground pins to short out. Once shorted, the supply pins will remain so even after the trigger source is removed, and can only be stopped by removing power. Latch-up is described in much more detail in National Semiconductor application note AN-339, and, in particular, a set of performance criteria is discussed.

By a combination of process enhancements and some careful IC layout techniques, the latch-up condition cannot occur in 54HC/74HC or 54HCT/74HCT. If one attempts to cause latch-up by forcing current into the protection diodes, the IC will be overstressed in the same manner as overstressing a TTL circuit.

ESD has also been a concern with CMOS ICs. Primarily for historical reasons, MOS devices have always been considered to be sensitive to damage due to static discharges. However, process enhancements and careful input protection network design have actually improved 54HC/74HC and 54HCT/74HCT immunity to where it is actually better than bipolar logic. This includes 74ALS, 74LS, 74S, 74AS and 74F. ESD is measured using a standard military 38510 ESD test circuit, which zaps the test device by discharging a 100 pF capacitor through a 1.5 kΩ resistor into the test circuit. ESD test data is shown in National Semiconductor reliability report, PR-11.

CONCLUSION

HCT is a unique sub-family designation of HC. It is intended primarily for TTL level to HC interfacing, although it is far from restricted only to this application. HCT can be used as a pin-for-pin socket replacement of TTL, or can be mixed with HC logic.

54HCT/74HCT has the same speeds as HC and LS, the same noise immunity as TTL and a significantly lower power consumption than LS-TTL, although it is slightly greater than HC. Additionally, by providing latch-up immunity and low ESD sensitivity like the 54HC/74HC family, the overall system reliability and integrity is increased. All of these performance parameters enable HCT's use in a wide range of applications.

The MM58348/342/341/248/242/241 Directly Drive Vacuum Fluorescent (VF) Displays

National Semiconductor
Application Note 371
David Stewart
August 1984

1. INTRODUCTION

National has produced a family of high voltage display drivers which is specially designed for use with vacuum fluorescent (VF) displays. These circuits are fabricated using a standard metal gate CMOS process which has been extended to allow a maximum operating voltage of 60V, thus enabling the design of bright multiplexed displays. In this way, the advantages of CMOS are retained (low power), while the range of applications for this technology is increased. Many of today's high voltage MOS display drivers require the use of one external resistor per display output, and this leads to a considerable increase in component count and board area. National's display drivers, however, incorporate an on-board pull-down resistor structure which removes these disadvantages.

This application note is intended to demonstrate several ways in which these display drivers can be configured to drive and control a wide range of VF displays. Although particular attention will be given to one specific display, a 32-character alphanumeric display, the design is presented in such a way as to enable easy extrapolation to the system designer's specific application.

2. FUNCTIONAL DESCRIPTION

There are six circuits in this new family of high voltage VF drivers and they can be sub-divided according to maximum operating voltage, number of display outputs, data interfacing requirements and ability to be cascaded. Each of the three circuit configurations is available with maximum operating voltages of 35V (MM583XX) or 60V (MM582XX). Due to the nature of the output stage required to attain high voltage operation of CMOS devices, the drive capabilities of the display output decrease as maximum operating voltage increases. Therefore, to maintain the option of trading off display voltage against drive current, each circuit has a high voltage (reduced drive) version and a low voltage (high drive) version. The three circuit configurations can be identified by the number of display outputs they contain (e.g., 20, 32 or 35 outputs). In all cases, data is entered serially into a 5V internal CMOS shift register. This data is latched to the output either by an external enable control signal (MM58241/341/242/342) or automatically by a leading start bit in the data stream (MM58248/348). *Figure 1* shows how the 6 device numbers correspond to the different circuit configurations and operating voltages.

The MM58348/248 devices use a two control line data input format (data in and clock) which enables the 40-pin part to have 35 display outputs. To load data into the controller, a start bit precedes the 35 data bits. The start bit is a logical "1" clocked into the IC by the first clock pulse. Next, 35 data bits are clocked into these parts. The start and data bits are shifted in on the rising edge of the clock. As the data is clocked into the IC, the start bit is shifted down the 35-bit register. On the rising edge of the 36th clock pulse, data is transferred to the display register and the start bit is shifted into the control latch. On the negative edge of the clock, the shift register is cleared. The display register feeds the level shifters that translate 5V CMOS levels to the 35V-60V required by the display. The MM58348/248 devices are not cascadable. Typically, these devices would perform the segment refresh drive in a multiplexed multi-digit system. A functional block diagram is shown in *Figure 2*.

The MM58341/241/342/242 devices use a three control line data input format (data in, clock and enable) and have either 32 or 20 display outputs, as given by *Figure 1*. This configuration sacrifices some outputs to enable cascading, enhance control signal flexibility, and provide brightness control. Here again, data is shifted into the shift register on the rising edge of clock, but no start bit is needed. Instead, the enable signal is taken high to input data to the chip. When the enable is taken low, the contents of the shift register are loaded into the display register. Again, the display register feeds the level translator and display driver outputs.

Each of the MM58241/341 and MM58242/342 devices has a serial data output pin which is connected directly to the last stage's output of the shift register. By connecting data out from one device to the data in pin of another device, and by holding each circuit's enable constantly high, the display drivers can be cascaded. The result is a shift register with a variable number of bits, depending on the mix of circuits used.

The MM58341/241/342/242 devices also have a blanking control input. A logic high on this pin turns all outputs off, while still retaining the display data. If a logic "0" is then applied, the display data will return unchanged. Consequently, the brightness of the display is proportional to the duty cycle of this blank signal. A functional block diagram of these devices is shown in *Figure 3*.

		Operating Voltage	
		35V	60V
Number of Outputs	20	MM58342	MM58242
	32	MM58341	MM58241
	35	MM58348	MM58248

20 and 32 output drivers use envelope enable data format and may be cascaded.
35 output (5 × 7 dot matrix) drivers use start bit data format.

FIGURE 1. The Complete VF Display Driver Family

Block Diagrams

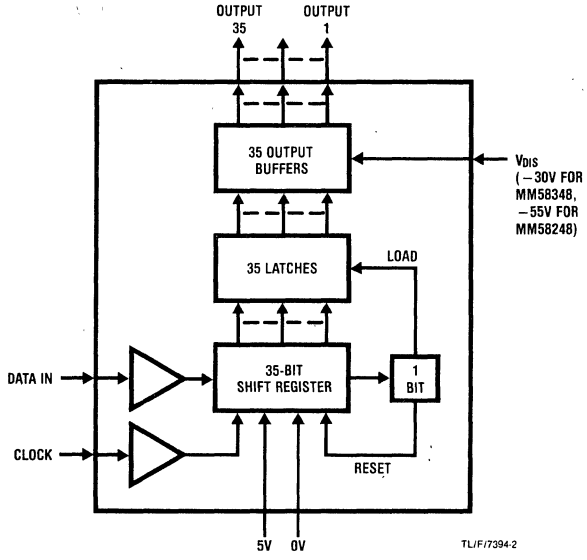


FIGURE 2. MM58348/248

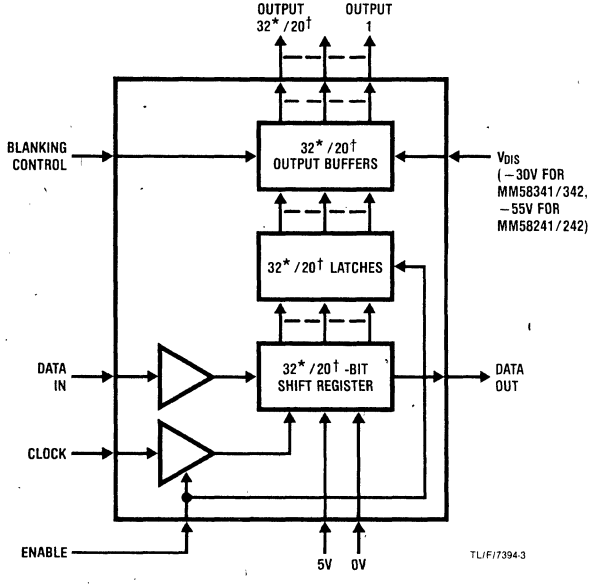


FIGURE 3. MM58341/241* and MM58342/242†

2. FUNCTIONAL DESCRIPTION (Continued)

Referring to the functional block diagrams shown in *Figures 2 and 3*, it is clear that all the internal logic is implemented in standard 5V CMOS. Such signals do not possess sufficient drive for the high voltage output stage, so the data passes through a bank of 15V level shifters to the output section. A schematic of the output stage is shown in *Figure 4*. It can be seen that all these display drivers use a two-stage high voltage structure with active pull-up transistors and passive pull-down resistors to the display voltage. Because resistor pull-downs are used, it is the output switching "off" time which is critical for the system design, and this is typically 20 μs for a rail-to-rail voltage swing.

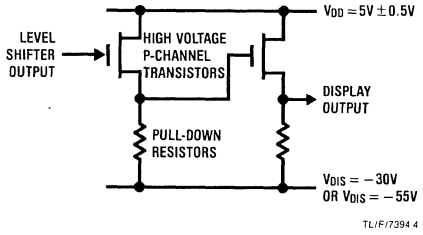


FIGURE 4. High Voltage Output Structure

3. DESIGN CONSIDERATIONS

3.1. The VF Display Configuration

The operation of a VF display is merely an extension of the valve principle, i.e., it is a voltage controlled device. An AC waveform is applied across the filament of the display, and this excitation causes electrons to be emitted. If both the grid and the anode are at a high positive voltage with respect to the cathode, the electrons reach the anode area, which is coated with a fluorescent material. When bombarded by electrons, this material emits light, hence one segment of the display is turned on.

This particular family of display drivers can drive a wide range of VF displays. The simplest case is where each display segment can be directly driven by wiring each output to the display anode. This normally occurs on displays with a small number of digits and segments (e.g., 4 characters of 7 segments) and this can be driven by cascading the drivers until sufficient data bits are available. This display configuration has the advantage of not requiring any refresh (which would be required if a multiplexed configuration were used) but has the disadvantage of needing one wire per segment.

As the size of the display increases, the number of available segments also rises, thus a multiplexing scheme which will reduce the number of display connections is desirable. This is normally achieved by hard wiring all the segments (anodes) of each digit together, then using the grids to select each digit in turn. The correct segment data can then be displayed. Using these techniques necessitates that the display be continually refreshed with each digit of data, even when that data has not changed.

To see the advantage of multiplexing, if a 32 character 5×7 dot matrix display is used, a total of 1120 segments is available. For this reason, the display is multiplexed and has 32 grid inputs and 35 segment inputs. The required refreshing task must be accomplished without the detection of flickering by the human eye, i.e., at a rate greater then 50 Hz. (Refresh timing is discussed later.)

Given the aforementioned display pinout and control logic, it is desirable in multiplexed displays to use the MM58341 to control the display grids (digits) and one MM58348 to control the display anodes (segments).

3.2. The Display-Driver Interface

When using the MM58XXX series, no buffering is required between the driver output pins and the VF display. It is necessary only that the driver charge and discharge the display in such a time that the refresh rate outlined in the previous section can be achieved. All the VF drivers have LSTTL compatible inputs, and, as the data source is generally a microprocessor, no special interface requirements exist.

3.3. The Microprocessor-Driver Interface

Typically, the system utilizing these display drivers will have some sort of microprocessor or single chip computer controlling the display. Thus, this processor will control one or more of the display drivers. The drivers have relatively little intelligence, therefore the host processor will be in charge of updating the display drivers and generating refresh timing if needed. The advantage of having minimal intelligence on the drivers themselves is flexibility. Virtually any display size or type can be used with equal ease, from small 7-segment, to British flag types, to larger 5×7, 7×9 or 5×12 displays.

The drivers can be directly interfaced to the microcontroller, COPS™4XX, or 80C48/9. This would normally be accomplished by connecting the driver's data and clock lines to control ports on the microprocessor. The MM58248/348 series is capable of accepting clock rates up to 1 MHz, and the MM58241/341 800 kHz. This is far faster than the control port bit manipulation rates for these controllers and will ensure compatibility with most low end microprocessors. 1 MHz input clock rates will also ensure that the desired display refreshing rate is attained.

In higher end systems using NSC800™ or 6800 8-bit microprocessors, the 1 MHz clock rate, coupled with a 300 ns minimum pulse width, simplifies direct interfacing of these drivers to a μP bus. In the simple case, some logic for address decoding would set aside an I/O port for communication to each driver, then several bits of the data bus could be gated to create the clock, data and enable signals.

4. TYPICAL DESIGN IMPLEMENTATION

4.1. Simple Direct Drive Application

Figure 5 illustrates a simple cascaded direct drive application where MM58241s are cascaded to drive a 7-segment (plus decimal point) display. The MM58241s were chosen because of the ease with which they can be cascaded. The MM58248s can also be used and provide a few more outputs per package, but cannot be cascaded.

In this application, the controlling μP need only update the display whenever the data changes. When updating the display, the data is assembled, enable is raised, and the data is clocked serially to the driver. Once all the data is loaded into the shift registers, the enable is taken low. This action updates the display.

4.2. A 32-Digit 5 x 7 Dot Matrix Application

In this application, the obvious choice is to implement some sort of multiplexing scheme to drive the display with fewer lines. This application usually requires that a dedicated controller be used to generate all the timing signals.

General multiplex timing of a VF display is usually similar to LED multiplexing. First, the segment data for one character is output to the display. Next, the digit strobe for that digit is raised, enabling the character. Then the digit strobe is brought low while the segment data is changed to the next character on the display. The next character is enabled by raising the digit strobe. This action continues until each character is turned on sequentially. *Figure 6* shows the basic timing for a simple display.

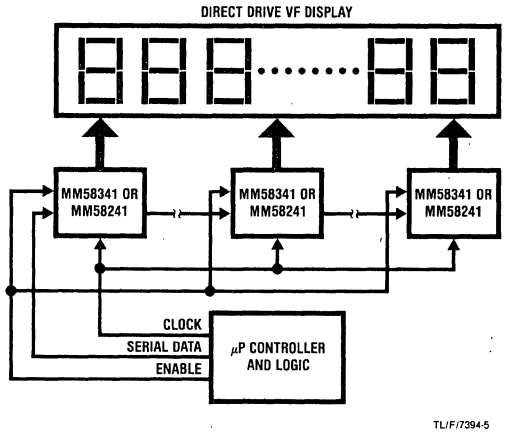


FIGURE 5. Typical Direct Drive System with μP

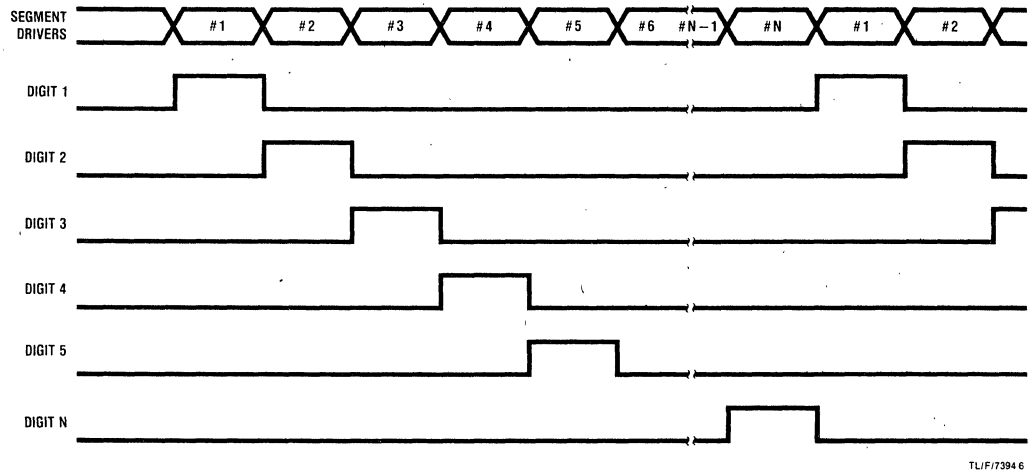


FIGURE 6. Simplified Timing for Multiplexed VF Display

4.2. A 32-Digit 5 x 7 Dot Matrix Application (Continued)

In this design, it is logical to use one MM58341 to control the display's digits. As will be seen, this driver can be easily used to shift a single high level bit which will be used to sequentially enable each character. One MM58348 can be used to drive the segments. A 5 x 7 matrix has 35 segments, which is ideal for the MM58348. Therefore, this configuration has a total of 6 connecting lines to interface the microprocessor to the display drivers. The connection diagram is shown in *Figure 7*. Because both of the drivers accept data only when the clock is active, it would be possible to couple both data lines together. However, although this saves one interface line, there is a disproportionate increase in the software burden.

The choice of which driver to use for segments and which for digits is dependent only on which configuration is the simplest to implement in hardware or software. The MM58241/242/248 devices are all equally capable of driving the digits or segments of a display.

4.3. Multiplexed Display Refresh Timing: The Controllers

Considering first the digit driver (MM58341), it is clear that the digits must be enabled sequentially and that this process must be continuous, even when the display data has not changed. To this end, the data for the MM58341 is simply a one followed by 31 zeroes, where the one is shifted along the internal register. As each digit is enabled, the corresponding segment data is displayed. To ensure that no ghosting effects are seen during the transition between digits, the blank signal is activated for a short time before and after the segment data is changed. *Figure 8* shows the microprocessor waveforms and the resultant display waveforms for the 32-character design. Thus, one can see how the blank is used to mask the display while the digit enable signal goes low and the segment data is latched.

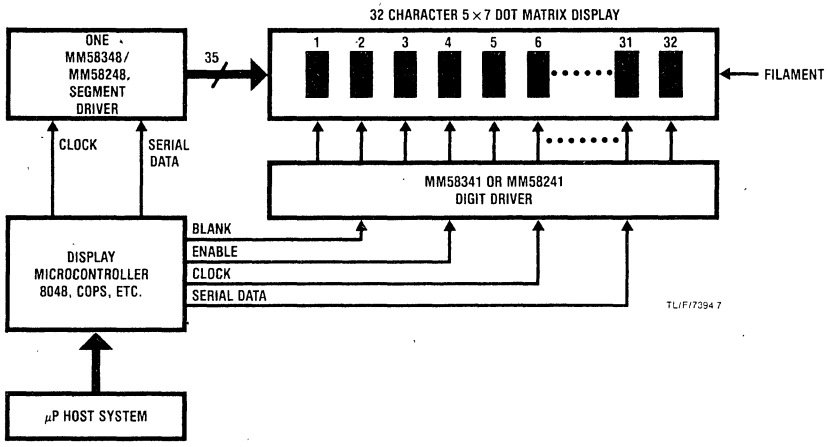


FIGURE 7a. Typical Architecture for Higher End System Utilizing Dedicated Display μP

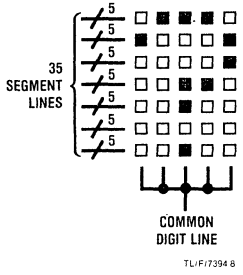
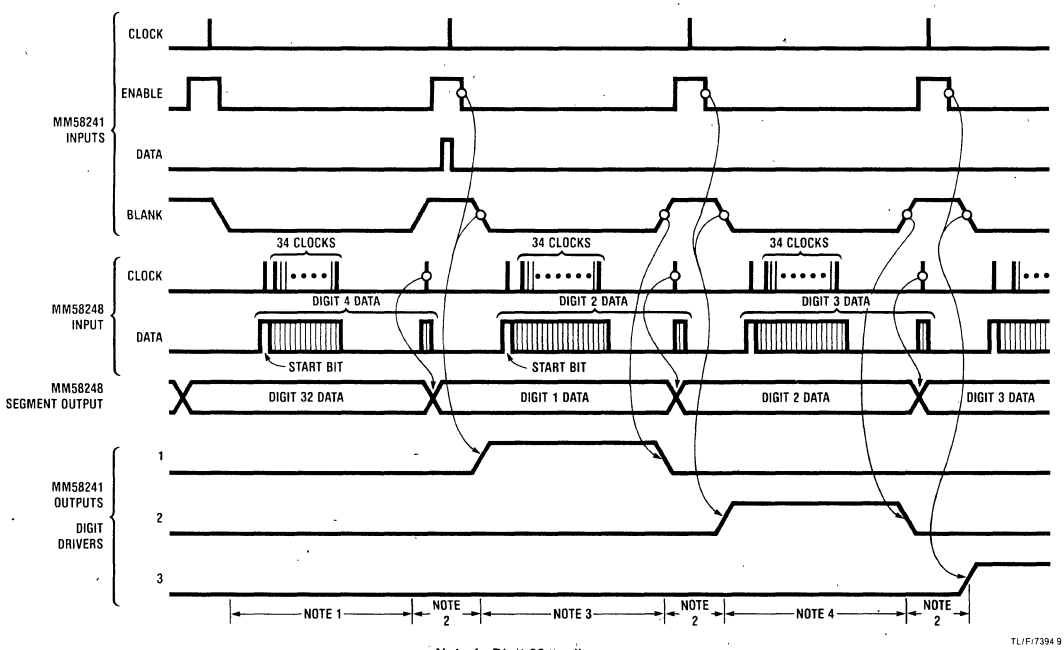


FIGURE 7b. Detail of Typical Dot Matrix Digit

4.3. Multiplexed Display Refresh Timing: Controllers (Continued)



Note 1: Digit 32 "on".
Note 2: Inter-digit blanking.
Note 3: Digit 1 "on".
Note 4: Digit 2 "on".

FIGURE 8. Microprocessor and Display Timing Waveforms

In between digit strobes, the segments are updated. The first 34 bits of segment data are set up and then the blank signal is activated to disable all 32 digits. The 35th bit is clocked in, updating the segments. Then the digit driver is clocked, shifting the digit strobe bit one position in the register. The enable is then brought low, enabling the next digit. Finally, blank is deactivated and the data displayed. Also, once the digit enable bit has been entered by the first MM58341 clock pulse, only one additional clock is required to enable each subsequent digit.

During the blank time, the order in which the segments or the digits are updated is not critical since this occurs while the display is blank. The digit driver may be clocked first, or the segments could be changed first.

The segment data must be latched to the MM58348 outputs immediately before the relevant digit is accessed, but also while the display is blanked. Because the MM58348 resets its internal shift register each time the data is latched, it can accept all but the final data bit while still displaying the previous digit, so the final clock and data bit can be loaded when the blank signal is high.

In general then, the philosophy for driving this VF display is:

a) Set up the start bit and the first 34 bits of the segment data within the internal shift register of the anode driver (MM58348).
b) Blank the display (disable all digits).
c) Clock the grid driver (MM58341) to enable the correct digit.
d) Load the final segment data bit into the anode driver, thus latching all 35 data bits onto the outputs. [c) and d) may be reversed.]
e) Remove blank signal (enables correct digit).
f) Load first 34 segment bits of next digit while displaying this data.
g) Repeat steps a) to f) for every digit in the display.

Note that items a through g must be executed continuously, even when the data has not changed.

4.4. Multiplexed Display Refresh Timing: Display Brightness

The obvious goal of a multiplexed design is to reduce the driver/display interface while maintaining proper display brightness and legibility. Thus, the limits of multiplexed operation are partly defined by the display's ability to appear bright, even as the number of multiplexed digits increases. As the number of characters is increased, the "on" time of each character is reduced, hence its perceived brightness is diminished. Also, the refresh rate needed by the display to prevent eye fatigue and flicker and the speed at which the controllers can update the display determine the limits of multiplexing.

4.4. Multiplexed Display Refresh Timing: Display Brightness (Continued)

The refresh rate of the display is defined as the frequency at which each digit is enabled (i.e., the reciprocal of the time taken to display all digits). It is generally accepted that in order to avoid visible flickering, a refresh rate in excess of 50 Hz is required. Typically, VF manufacturers recommend 100 Hz–200 Hz. Some sample calculations follow and assume a refresh rate of 100 Hz. Therefore, the time given to display all digits is 1/(100 Hz) = 10 ms, and is 10 ms/(number of digits) for any one digit. For this example, 10 ms/32 = 312.5 μs. This is defined as the total digit multiplex time and will be made up of a digit "on" time and an inter-digit blanking time. The inter-digit blanking is required to prevent display ghosting when digit information changes.

In general, then, the total digit time (t_D) is the inverse of the refresh rate (fr) divided by the number of digits in the display (nd), i.e.,

$$t_D = 1/(fr \times nd) \text{ seconds.}$$

Since each digit time is composed of the "on" time, t_{DON}, and the blanking time, t_{DOFF}, the total digit time is:

$$t_D = t_{DON} + t_{DOFF} \text{ (seconds).}$$

A useful measure of the brightness of a multiplexed display can be obtained by comparing it to the direct drive (100% brightness) case. In the direct drive application each digit is "on" permanently, while in the multiplexed mode each digit is "on" only for a portion of the time taken to refresh the display. Therefore, the measure of multiplexed brightness is given by the ratio of an individual digit "on" time to the total refresh time. Noting that the refresh time is a function of the total digit time (t_D) and the number of display digits (nd), a percentage figure for the brightness compared to the direct drive case can easily be calculated.

$$\text{percent muxed brightness} = \frac{t_{DON}}{t_D \times nd} \times 100$$

$$\text{percent muxed brightness} = \frac{t_{DON}}{(t_{DON} + t_{DOFF})nd} \times 100$$

Thus, regardless of the display logic's refresh speed, the display brightness will obviously depend on the amount of multiplexing and the amount of inter-digit blanking time. This is one constraint limiting the multiplexing scheme, and display manufacturers' data sheets should be consulted to determine a display's limits. This will, to a large degree, determine whether a design should use 32-digit multiplexing or perhaps two separate 16-digit multiplexed displays.

There are also limitations on the refresh rate based on the speeds of the hardware. In this design, the "on" time has a minimum value given by the time required to load the start bit and the first 34 data bits of the MM58348/248, i.e., the time required for 35 clock pulses of the MM58348. The MM58348 has a maximum clock frequency of 1 MHz, so the minimum time for 35 clock pulses is 35/(1 MHz) = 35 μs.

The digit "off" time is constrained by the time required to clock the digit driver and to load the final segment data bit, or the time for the display outputs to switch off then on, whichever is greater. The MM58341 has a maximum clock frequency of 800 kHz, so the minimum digit "off" time due to driver limitations is related to 1/(800 kHz) + 1/(1 MHz) = 2.25 μs. The blanking signal must be active during this time. Also, though the display outputs take typically 20 μs to switch, the display itself limits the minimum digit "off" time and is actually 20 μs.

Thus, the minimum total digit time per digit is:

$$t_D = 35\ \mu s + 20\ \mu s = 55\ \mu s.$$

At a refresh rate of 10 ms, 10 ms/55 μs equals the theoretical maximum number of digits that can be multiplexed, or about 180 35-segment characters. This is unrealizable since current display "on" times must be greater than 35 μs, and total digit duty cycles (or percent brightness) must be much higher.

$$\text{percent brightness} = \frac{25\ \mu s}{55\ \mu s \times 180} \times 100 = 0.25\%.$$

For the 32-digit case, the percent brightness is more realistic:

$$\text{percent brightness} = \frac{0.29\ ms}{0.31\ ms \times 32} \times 100 = 2.9\%$$

These times are the limits of the drivers. If the time required to load them is limited by the speed of the controlling processor, the update times are calculated from the clock rates of the controlling μP. However, as one can see, the limitations are more likely due to the display.

4.5. VF Display Brightness Control

Generally, to control or vary the brightness of a display, one can either vary the display drive voltage or vary the "on" time duty cycle by applying a signal to the blanking control. The duty cycle of the blanking signal will determine the brightness. This latter technique is preferred since more predictable behavior results.

In the simple direct drive case the MM58241/341/242/342 must be used. A periodic waveform is applied to the blanking pin. Its frequency should be greater than 100 Hz–200 Hz. As the duty cycle is varied, the percentage of time that the digits are "on" is changed and the perceived brightness changes.

In a multiplexed application, the brightness can be altered by merely modifying the relative length of the inter-digit blanking signal. This is easily accomplished in the software of the controlling μP by adding a delay while the blanking signal is active and subtracting the same delay from the time the blanking signal is inactive.

The relative brightness is the percentage of time that any one character is "on" divided by the sum of the character's "on" and "off" times. The latter term was previously defined as the total digit time. Thus:

$$\text{relative brightness} = t_{DON}/t_D.$$

Due to hardware refresh update speed limitations, 100% and 0% brightness cannot be achieved and also maintain proper refreshing, although 0% can be achieved just by stopping refresh and blanking continuously. (Note that this percentage is relative to the theoretical minimum and maximum brightness for a given multiplexed display, not the brightness relative to a direct drive display as was done previously.)

In the above 32-digit example, the maximum brightness is (assuming 10 ms refresh rate and 20 μs minimum inter-digit blanking):

$$\text{max percent brightness} = (0.29\ ms/0.31\ ms) \times 100 = 93.6\%.$$

The minimum brightness, assuming 35 μs minimum "on" time is:

$$\text{min percent brightness} = (0.035\ ms/0.31\ ms) \times 100 = 11.2\%.$$

Clearly there is a large range of available display brightness levels which are easily software controllable by altering the duty cycle of the blanking signal.

Again, the above analysis assumes that the microprocessor unit is interfacing with the display drivers at their maximum data rates. If this is not the case, some part of the brightness range will be lost.

Refer to Appendix for general system considerations.

5. THE SOFTWARE

Having outlined the general method by which the data can be displayed, it now remains to demonstrate how this can be achieved at the microprocessor level. It was thought best to use a familiar microprocessor for this task, so the implementation will use a 6502 and 6522 VIA circuit. The procedure which will be described is merely one example of how these display drivers can be applied, and it is hoped that by concentrating on the arranging and loading of the data, a more general benefit will be gained.

The application to be described here is that of an alphanumeric display where characters are entered from a keyboard onto a VF display, feeding in from the left. The program will also accept control codes such as line feed, delete, etc. The general flowchart for this routine is shown in *Figure 9*. When the character is collected from the keyboard buffer it must first be established that it is a valid ASCII code; if not, it is ignored and the present data will continue to be displayed. The next thing to check is whether it is a control code. If it is a control code, the function represented must be executed on the existing data and the resulting data displayed. Assuming the ASCII code is not identified as a control code, it must correspond to a display character, and hence will be entered at the start of the display data buffer. Following this, the 32 characters denoted by the contents of the display data buffer are displayed, and after the last digit is enabled the keyboard buffer is checked for new data. As the display refresh rate far exceeds the speed of the human typist, each set of data is displayed several times before it changes.

Looking at the routine for displaying the 32 digits in more detail, a flowchart can be drawn up, as shown in *Figure 10*.

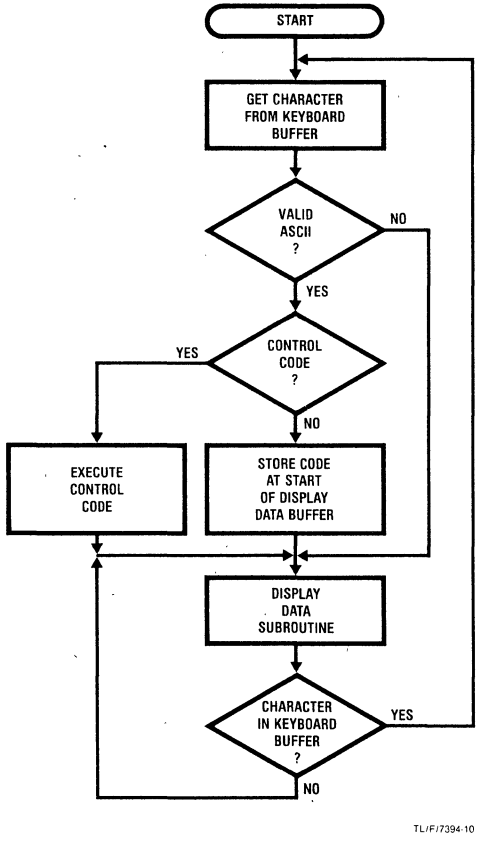


FIGURE 9. General IC Flowchart

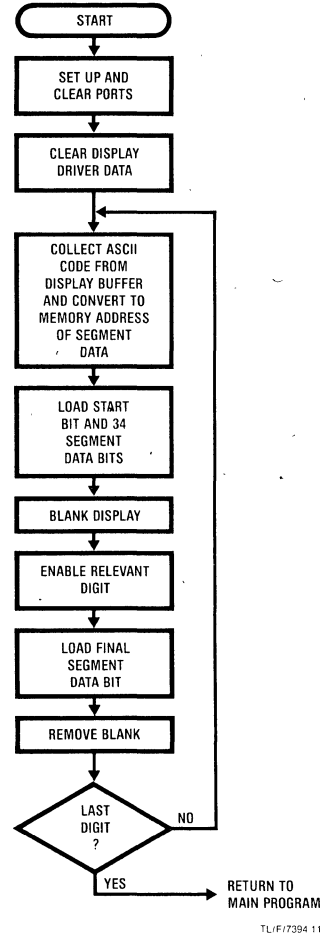


FIGURE 10. Display Data Subroutine Flowchart

5. **THE SOFTWARE** (Continued)

After first setting up and clearing the port lines and both the display drivers, a routine is performed for each of the 32 display characters. The ASCII code is collected and decoded to reveal memory locations where the corresponding 35 segment bits are stored. The start bit and first 34 data bits are loaded into the MM58348. Then the MM58341 blank signal is activated while the relevant digit is enabled and the final segment bit is loaded. After blank is removed, the next ASCII code is collected and decoded, etc. When the last digit has been loaded, control returns to the main program for the updating of the display data.

The machine code routine for the setting up of each digit of display data is shown in *Figure 11.* The relevant addresses of ports and digit codes are included in *Figure 12* to make the program comprehensible. The address of the segment data is stored in locations 00E2 and 00E3, and it is assumed that this is updated outside the display subroutine. The ports can be addressed as 8-bit memory locations or as individual lines. When considered as individual bits, the fifth address bit either sets or clears that bit, i.e., STA 0915 sets PA5 and 090B clears PB3.

The segment data for each character is stored as 7 consecutive memory locations, each containing 5 data bits.

The contents of each location are loaded into port A via the accumulator, starting with the highest memory address. This is achieved by indexing the lowest memory address by the contents of the Y register (starting as 06) and decrementing this register as every 5 bits are loaded. The least significant bit of port A is used for the segment data (PA0) and the 5 data bits are loaded by storing the code to port A, logically shifting it to the right, and storing it to port A again. This procedure is repeated 5 times for each memory location. The code given in *Figure 11* is for the brightest case, i.e., where the blank signal is disabled, as soon as the data has been latched to the display outputs. Clearly, the brightness can be altered by delaying this action.

The data is held in memory in the form of 7 locations of 5 bits each. This format was chosen because each location can be equated to one row of the 5 × 7 dot matrix, where the lowest memory location corresponds to the bottom row. For example, if it is desired that a "5" be displayed in the form shown in *Figure 12*, then the 36-bit data stream is as demonstrated. Assuming that the data is stored at the 7 locations starting at address 2120, then the location contents are as denoted in *Figure 13.*

```
DISPLAY  STA 0910
         STA 0918
         STA 0908
         STA 0900      \ Load start bit.
         LDY #06       \ Load 30 segment
         JSR LOAD5     \ bits, 5 at a time.
         LDA (I) E2    \ Load lowest addr.
         LDX #04
LOOP1    STA 0920
         STA 0918
         STA 0908
         LSRA
         DEX
         BNE LOOP1     \ Load 4 seg. bits.
         STA 091B      \ Enable high.
         STA 0919
         STA 0909      \ Digit select clock.
         STA 091C      \ Blank high.
         STA 090B      \ Enable low.
         STA 0920
         STA 0918      \ Load 35th segment
         STA 0908      \ bit.
         STA 090C      \ Blank low.
         RTS           \ Ret. to main prog.
LOAD5    LDA (I),Y E2  \ Load mem. contents.
         LDX #05       \ Count for 5 bits.
LOOP2    STA 0920      \ Push data to port A.
         STA 0918      \ Segment clock high.
         STA 0908      \ Segment clock low.
         LSRA          \ Shift seg. data
         DEX           \ and dec. bit count.
         BNE LOOP2
         DEY           \ Set up address of
         BNE LOAD5     \ next 5 seg. bits.
         RTS           \ Return to display
                       \ subroutine.
```

TL/F/7394 12

FIGURE 11. Display Data Load Subroutine

Port A—Address 0920

Port Bit	Function	Address
PA0	Data 8	09-0
PA1	Not Used	09-1
PA2	Not Used	09-2
PA3	Not Used	09-3
PA4	Not Used	09-4
PA5	Not Used	09-5
PA6	Not Used	09-6
PA7	Not Used	09-7

Port B—Address 0921

Port Bit	Function	Address
PB0	Clock 8	09-8
PB1	Clock 1	09-9
PB2	Data 1	09-A
PB3	Enable	09-B
PB4	Blank	09-C
PB5	Not Used	09-D
PB6	Not Used	09-E
PB7	Not Used	09-F

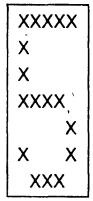
TL/F/7394-13

Lowest memory address giving location of segment display data: stored in locations 00E2 and 00E3.

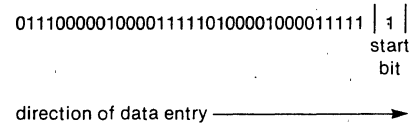
FIGURE 12. Port and Relevant Memory Addresses

5. **THE SOFTWARE** (Continued)

Desired Display Character (Numeric 5)



Desired Data Stream



Memory Contents (Assuming Lowest Address = 2120)

Address	Contents	
2120	0E	row 7
2121	11	row 6
2122	01	row 5
2123	1E	row 4
2124	10	row 3
2125	10	row 2
2126	1F	row 1

TL/F/7394 14

FIGURE 13. Example of Segment Data Arrangement

6. CONCLUSIONS

This design example is merely one of the many possible applications for the MM58348/341/248/241 family of high voltage display drivers. For other applications it should be noted that the other 2 circuits in this series, namely the MM58342 and the MM58242, can provide a much wider range of possible connections. For example, larger displays such as the 2-line by 40-digit 5 × 7 dot matrix formats can be driven with two MM58348s and two MM58342s cascaded to form a 40-bit shift register.

The method by which the segment data is shown to be stored and accessed in memory is convenient in the above example, although again it is only one of the many methods. An alternative using 5 locations of 7-segment data bits is possible, where the software would be faster but the data formatting more difficult. There are many trade-offs to be found with so versatile a series of circuits.

The code used to demonstrate this example is that of the 6502 microprocessor, and it would be a simple task to convert the instructions for another device (e.g., National's CMOS NSC800). The versatility of display formats available is a major feature, and the fact that these display drivers are CMOS devices guarantees their low power consumption. In addition, the outputs incorporate internal pull-down resistors which greatly reduce the external component count. This cuts the required board area; consequently a considerable saving in system cost can be made.

APPENDIX: SYSTEM CONSIDERATIONS FOR VF DISPLAY DRIVING

The purpose of the following text is to show how a designer can make decisions on displays he can drive or ranges of brightness he can achieve with a given system. Alternatively, it can be used as a method of designing a system to meet a desired display specification.

THE THEORY

1. System Decisions

System Constraints:

a) Refresh rate (f_r)
b) Number of display digits (nd)
c) Rate at which drivers are clocked by system (f_{CLK})

Associated Parameters:

a) Total time available to display all digits (t_r)
b) Total time allocated to each digit (t_D)
c) Total time each digit is on (t_{DON})
d) Total time each digit is off (t_{DOFF})
e) Number of display segments (ns)
f) Number of system clocks required to display one digit (nc_{ON})
g) Number of system clocks required to load segment bits (nc)
h) Number of system clocks required to latch both segment and digit data (nc_{OFF})

From the above definitions, the following equations can be stated:

$t_r = 1/f_r$ (seconds)

$t_D = t_r/nd = 1/(f_r \times nd)$ (seconds)

t_{DON} = time to load segment bits for next digit
= ns system clocks
= nc_{ON} system clocks
= nc_{ON}/f_{CLK} (seconds)

t_{DOFF} = time to latch segment bits and to enable relevant digit
= nc_{OFF} system clocks
= nc_{OFF}/f_{CLK} (seconds)

Hence:

$t_D = t_{DON} + t_{DOFF}$
$= (nc_{ON}/f_{CLK}) + (nc_{OFF}/f_{CLK})$
$= (nc_{ON} + nc_{OFF})/f_{CLK}$
$= nc/f_{CLK}$ (seconds)

And:

$f_{CLK} = nc/t_D$
$= nc \times f_r \times nd$ (Hertz)

2. Brightness Variation Considerations

The brightness of the display is proportional to the duty cycle of the blank signal, and the range of intensities available depends on the size of t_{DON} and ultimately the refresh rate, fr.

Bd = brightness of the display
= duty cycle of blank signal
= t_{DON}/t_D

In the above example, the least bright case is where the blank signal is low for only one system clock per digit.

Bd (min) = 1/nc

And the brightest case is where blank is low only for the time required to latch the segment data and enable the digit.

Bd (max) = $(nc - nc_{OFF})/nc$
$= 1 - (nc_{OFF}/nc)$

The range of available brightness level, Br, is:

Br = Bd (max)/Bd (min)
$= [(nc - nc_{OFF})/nc]/(1/nc)$
$= nc - nc_{OFF}$

It should be noted that this is the minimum range of available brightness levels because t_D was minimized to maximize fr. If the system clock were fast enough to allow the maximum refresh rate to be in excess of the desired fr, then t_D could be increased from its minimum value. This would, in turn, produce a wider range of brightness levels.

It should also be noted that most manufacturers quote a minimum duty cycle for each digit. The system designer should ensure that neither end of the brightness specification exceeds this value.

THE APPLICATION

For the purposes of doing some sample calculations using the above theory, we will assume use of the system previously described, i.e., the driving of a 32-digit 5 × 7 dot matrix display by one MM58341/241 and one MM58348/248.

1. System Decisions

The number of display digits is fixed, i.e., nd = 32 (nc_{ON} = 35 and nc_{OFF} = 2, so nc = 37 system clocks). Assume system has a 125 kHz clock rate.

Therefore, the resulting refresh rate is:

$f_r = f_{CLK}/(nc \times nd)$
$= 125000/(37 \times 32)$
$= 105$ Hz

Also, the system clock rate needed for a given refresh rate can be calculated, e.g., f_r = 200 Hz.

$f_{CLK} = nc \times f_r \times nd$
$= 37 \times 32 \times 200$
$= 237$ kHz
= approximately 250 kHz

There are many other examples of how this theory can be used to evaluate the possibilities for VF systems.

2. Brightness Variation Considerations

We can now calculate the range of brightness intensities available with the above system, i.e., where f_{CLK} = 125 kHz, f_r = 105 Hz.

Bd (min) = 1/nc
= 1/37

Bd (max) = $1 - (nc_{OFF}/nc)$
= 1 − (2/37)
= 35/37

Br = Bd (max)/Bd (min)
= 35

So the brightness can vary from its lowest value to its maximum value, which is 35 times the minimum level.

Also note that the minimum duty cycle for this display is given as 1/40 (manufacturer's specification), so there is no problem in this application.

Let us now take the example of driving the same display with a system where $f_{CLK} = 500$ kHz, at a desired refresh rate of 200 Hz.

$nc = f_{CLK}/(f_r \times nd)$
$= 500000/(200 \times 32)$
$= 78$ system clocks

nc_{OFF} is 2 as before, and although we require only 35 clocks to load the segment data,

$nc_{ON} = nc - nc_{OFF}$
$= 78 - 2$
$= 76$ system clocks

In general, the higher the system clock rate, the wider the brightness control range.

Therefore,

Bd (min) $= 1/nc$
$= 1/78$

But, remembering that Bd (min) must be less than the stated duty cycle (1/40):

Bd(min) $= 2/78$
$= 1/39$

Bd(max) $= 1 - (nc_{OFF}/nc)$
$= 1 - (2/78)$
$= 76/78$
$= 38/39$

Br $=$ Bd (max)/Bd (min)
$= (38/39)/(1/39)$
$= 38$

So, we can see that by manipulation of the system constraints, a wider range of brightness levels can be attained, although this is ultimately limited by the stated duty cycle of the display.

High-Speed-CMOS designs address noise and I/O levels

National Semiconductor
Application Note 375
Larry Wakeman
September 1984

To maximize the benefits of high-speed CMOS, you must cope with environmental interactions and component limitations. Especially important are system noise decoupling and both transient and steady-state level control.

Designs using high-speed-CMOS logic, such as the MM54HC/74HC Series, can attain characteristics that mark improvements over LS-TTL designs. To optimize these characteristics, however, you must adopt proper design procedures. This article deals with the ICs' input-output and noise-immunity considerations.

High-speed CMOS logic is essentially a digital-IC family that combines TTL (bipolar) and CD4000 (CMOS) characteristics. Because of the family's high speed, you must be more aware of the requirements of fast systems than in the case of CD4000B logic. Although the 54HC/74HC IC's CMOS construction results in noise immunity comparable to the CD4000 family, its high speed necessitates system-grounding and supply-decoding techniques normally used in LS-TTL system design.

The following sections discuss general usage guidelines, system noise susceptibility and immunity, and the 54HC/74HC logic's power-supply-noise characteristics. Note that, unless specific exceptions are stated, the considerations discussed apply also to 54HCT/74HCT, HC's TTL-compatible subset.

FOLLOW BASIC GUIDELINES

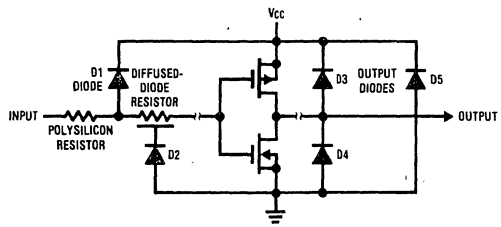
The basic rules for designing with 54HC/74HC circuits are similar to those that apply to 74LS, CD4000B and 54C/74C devices. First, under normal static operating conditions, the input should not exceed V_{CC} or go below ground. In normal high-speed systems, transients and line ringing can cause inputs to violate this rule momentarily, forcing the ICs to enter an SCR-latch-up mode.

Latch-up results if either the input- or output-protection diodes are forward biased because of voltages above V_{CC} or below ground. As a result, the IC's internal parasitic SCR shorts V_{CC} to ground *Figure 1* shows the diodes in a CMOS IC, schematically **(a)** and in a simplified die cross section **(b)**.

Thanks to some processing refinements, SCR latch-up isn't a problem with the MM54HC/74HC Series. There are, however, limitations on the currents that the internal metallization and protection diodes can handle, so for high-level transients (pulse widths less than 20 ms and inputs above V_{CC} or below ground), you must limit the current of the IC's internal diode to 20 mA rms, 100 mA peak. Usually, a simple resistor configured in series with the input suffices.

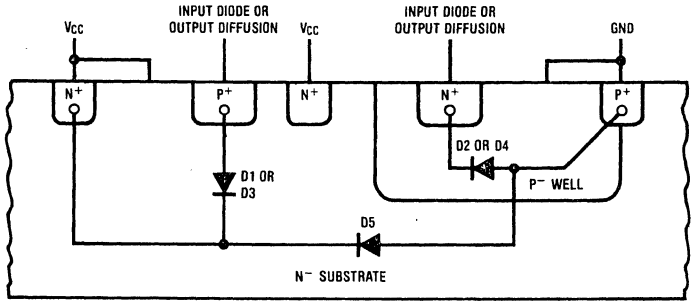
Powering the device is another important design concern. Don't power up inputs before both V_{CC} and ground are con-

(a)



TL/F/8127–1

(b)



TL/F/8127–2

FIGURE 1. Essential but sometimes evil, the diodes in CMOS-logic ICs can be easily damaged by excessive currents. Reversed supplies or large input or output currents can cause diode burnout.

Published in EDN Magazine

nected, and don't plug or unplug pc boards into or from powered connectors unless input currents are short lived or limited in the manner already described. Both conditions can forward bias input diodes, resulting in excessive diode currents. Again, *Figure 1* shows these diodes and the possible current paths. If these conditions are unavoidable, add external current limiting to prevent damage to 54HC/74HC circuits, or use special connectors that apply power before signals. Some family members (notably the HC4049/50) have modified input structures and can survive the application of power to the input before the supply.

Floating inputs are a frequently overlooked problem. CMOS inputs have extremely high impedance and, if left open, can float to any voltage. This situation can result in logic-function mishaps and unnecessary power consumption. Moreover, open inputs are susceptible to electrostatic damage. You should thus tie unused inputs to V_{CC} or ground, either through a resistor or directly.

Finally, for correct logic results you should use inputs with rise and fall times faster then 500 ns. Slower transition times can result in logic errors and oscillation.

OBSERVE OUTPUT RULES

You must observe certain usage rules for 54HC/74HC outputs as well as for inputs. Output voltages shouldn't exceed the supply voltage, and currents in the output diodes shouldn't exceed 20 mA. Moreover, output rms drive currents shouldn't exceed 25 mA for 4 mA standard-output devices or 35 mA for 6-mA devices. The die's metal lines dictate this limitation. Violations can result in long-term deterioration. Much larger currents (greater than 100 mA peak) arising from capacitive-load charging and line driving are normal and pose no real problem. As a rule of thumb, don't allow the output current's rms value to exceed the device's current rating. Unlike the inputs, unused outputs should be left floating to allow the output to switch without drawing any dc current.

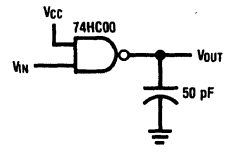
When testing a pc board, its often necessary to short the output of one CMOS device to overdrive and force a given level on the input of the IC driven by this output. In other instances, you might need to short the outputs on a one-time basis. You can do so without degrading the IC's life if you follow a few rules. When bench testing 54HC/74HC devices, for example, you can short one output for several minutes without harm. In automatic testing, you can short as many as eight outputs for a 1-sec duration. Here again, the limitation is imposed by the metallization.

POWER-SUPPLY CAVEATS

Now that you've looked at input and output signals, give some extra attention to power-supply considerations. For instance, supply levels affect the device's logical operation. You should, for example, keep the supplies within the 2 to 6V range for HC devices and the 4.5 to 5.5V range for HCT devices. Voltages as high as 7V or as low as 0V won't harm the ICs, but their performance isn't guaranteed at these levels. However, HCs and HCTs (with the exception of one-shots and Schmitt triggers) can typically function with supplies as low as about 1.4V.

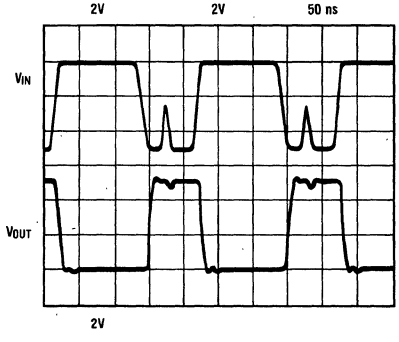
As with any IC, it's crucial that you *not* reverse the supply voltages. Doing so will forward bias a substrate diode between V_{CC} and ground (*Figure 1*), resulting in excessive currents and damage to the IC. As with inputs and outputs, don't let V_{CC} or ground rms currents exceed 50 mA for

(a)

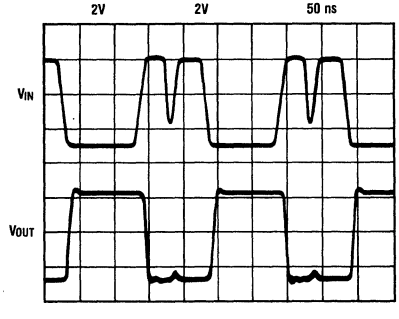


TL/F/8127–3

(b)



TL/F/8127–4



TL/F/8127–5

FIGURE 2. The reaction of 74HC00 gates (a) to noise spikes is clearly seen in these scope photos. The gate exhibits noise immunity of 2V or more (b). Furthermore, the immunity is equally good for positive- and negative-going noise spikes.

4 mA devices or 70 mA for 6 mA units. Again, transients pose no real problem as long as their rms values stay within the devices' ratings.

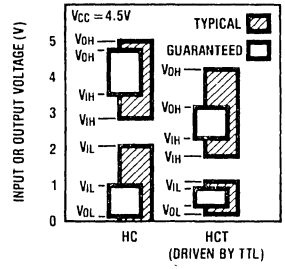
UNDERSTANDING NOISE

What happens if the signals just discussed aren't clean? In digital-logic systems, "noise" is defined as extraneous voltage in the signal or supply paths. For CMOS, ECL or TTL devices, system noise that's great enough can affect the logic's integrity. CMOS-logic families such as the CD4000 and 74C are highly immune to certain types of system noise. This immunity is due mainly to the nature of CMOS, but also to the fact that the devices' slowness reduces self-induced supply noise and crosstalk and prevents the logic from responding to short externally induced or radiated transients.

However, in high-speed CMOS (which is about 10 times faster than CD4000 logic), crosstalk, induced supply noise and noise transients become factors. Higher speeds allow the device to respond more quickly to externally induced noise transients and accentuate the parasitic interconnection inductances and capacitances that increase self-induced noise and crosstalk.

Because HC-CMOS specifies input levels similar to those of CD4000 logic, its dc noise rejection is also superior to LS-TTL. And because high-speed CMOS has an output impedance one-tenth that of CD4000 devices, it's less susceptible to noise currents coupled to its outputs. As a result, lower stray voltages are induced for a given amount of current coupling.

To quantify these noise parameters, first define "noise immunity": a device's ability to prevent noise on its input from being transferred to its output. More specifically, it's the amount of voltage that can be applied to an input without causing the output to change state. For HC-CMOS, this immunity is approximately 2V; in the worst case, it's the maximum input Low or High logic levels specified in the data sheet.



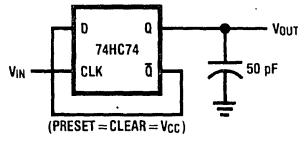
TL/F/8127–6

FIGURE 4. Noise margins for HC-CMOS and an HCT-CMOS-TTL combination are illustrated by this graph. You can see that the all-CMOS system exhibits the higher noise immunity.

Noise immunity is an important attribute, but noise margin proves more useful because it defines the amount of noise that a system can tolerate and still maintain correct logic operation. It's defined as the difference between the output logic Low (or High) of one gate and the input logic Low (or High) of the gate the given device is driving.

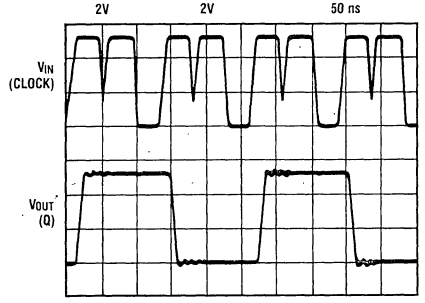
For example, in HC-CMOS using a 4.5V V_{CC}, typical output levels are ground and V_{CC}, and input thresholds are $V_{IH}=3.15V$ and $V_{IL}=0.9V$. These figures yield noise margins of approximately 1300 mV (logic One) and 850 mV (logic Zero). LS's noise immunity is 700 and 400 mV, respectively. Note that 54HC/74HC input levels are skewed slightly toward ground, so the ICs tolerate slightly more V_{CC} noise than ground noise.

(a)



TL/F/8127–7

(b)



TL/F/8127–8

FIGURE 3. Exhibiting high clock-noise immunity, this 74HC74 flip flop (a) shows no change in output for noise spikes greater than 2V (b)

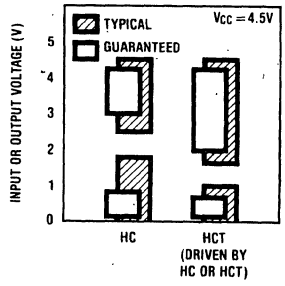
To illustrate noise margin and immunity, *Figure 2* shows the output that results when you apply several types of simulated noise to a 74HC00's input. Typically, even 2V or more input noise produces little change in the output. *Figure 3* shows how noise affects a 74HC74's clock input. Again, no logic errors occur with 2V or more clock noise.

54HCT/74HCT ICs have an input buffer specially designed to yield TTL input levels of 0.8 and 2V. Their noise-immunity characteristics are therefore substantially different from those of 54HC/74HC devices. In evaluating these differences, note two general applications for HCT logic: in a TTL or NMOS (eg, XMOS, HOMS) system; or in an all-CMOS, HC or HCT system.

In the first case, the HCT inputs get driven by outputs that are essentially TTL and specify output levels of 0.4 and 2.4V (or 0.5 and 2.7V). In this situation, the specified noise margin is similar to the TTL margin: 400 mV for a logic Zero and either 400 or 700 mV for a logic One. These values, shown in *Figure 4*, are significantly less than those of an all-HC system.

Now examine the second case. When using HCT with HC, output logic levels are almost equal to power-supply levels. Therefore, HCT's specified noise margin is approximately 700 mV for a logic Zero and 2.4V for a logic One. At first glance, the high noise margin for Ones might seem strange, but this situation presents a tradeoff against the Zero-level margin. Compare the two gate-transfer functions in *Figure 5*; the HCT device has a logic trip point at 1.4V, while the HC gate trips at 2.4V. Thus, HC's typical performance is twice that of HCT for ground noise; for V_{CC} noise, HCT is about 50% better.

The conclusion? In a normal system (including all-CMOS systems), HC provides better noise immunity than HCT. The one case where HCT could prove more helpful is in systems that are designed with noiseless ground and dirty V_{CC}. Naturally, this design approach isn't good. A second fact highlighted by these transfer functions, HC is conservatively specified for its input and output logic levels, whereas HCT is specified more tightly. So even though data-sheet limits for HCT seem better, actual system performance indicates that HC provides better overall noise margins.



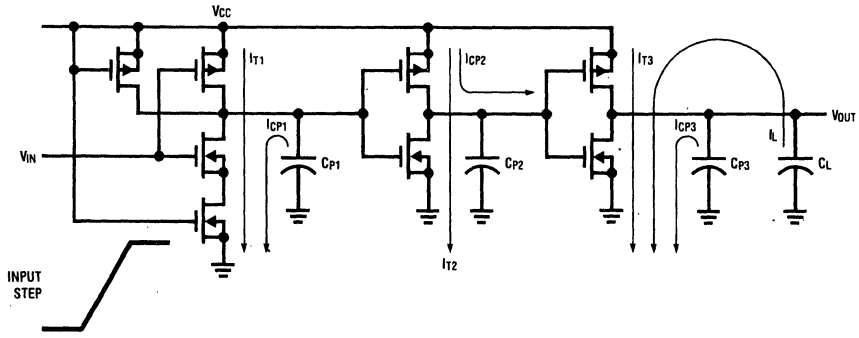
TL/F/8127–9

FIGURE 5. Comparing HC and HCT logic, this graph shows noise immunity of the respective families. HC wins for ground noise, HCT for V_{CC} noise.

CONSIDER SYSTEM NOISE

Now take a closer look at system noise, which you can group into several categories, depending on the source. The type of noise dictates the appropriate noise-supression technique.

- Power-supply I_{CC} noise, generated in the power-supply line, comes from logic switching in CMOS circuits.
- Transmission-line reflections, unwanted ringing and overshoot phenomena arise from signals propagating down improperly terminated transmission and signal lines.
- Signal crosstalk is caused by capacitive or inductive coupling of extraneous voltages from one signal line to another or to the power-supply line.
- Radiated noise, an RF phenomenon that originates within a high-speed-logic system, emits to other systems. It arises from the high-frequency energy emitted when logic toggles. This noise, not a major problem with regard to logic integrity, can interfere with other systems.



TL/F/8127–10

FIGURE 6. This schematic shows the currents in a 74HC00 gate that result when applying a positive input step. Also shown are the internal parasitic and external load capacitances.

Power-supply spiking is perhaps the most important contributor to system noise. When any element switches logic states, it generates a current spike that produces a voltage transient. If these transients become too large, they can cause logic errors because the supply-voltage drop upsets internal logic, or because a supply spike on one circuit's output feeds an extraneous noise voltage into the next device's input.

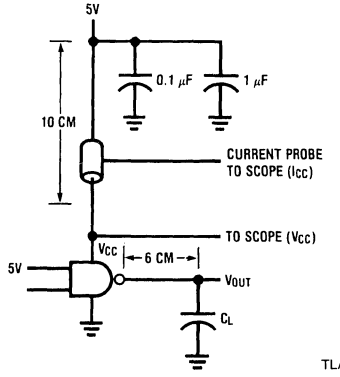
With CMOS logic in its quiescent state, essentially no current flows between V_{CC} and ground. But when an internal gate or an output buffer switches state, a momentary current flows from V_{CC} to ground. This current has two components: the current required to charge and discharge any stray or load capacitance, and the current that flows directly from V_{CC} to ground when the p- and n-channel transistors turn on momentarily during an input transition.

Figure 6 shows the paths for these current components within a 74HC00 upon application of a positive step to the device's input. C_{P1}, C_{P2}, and C_{P3} represent the internal parasitic capacitances; C_L is the external load capacitance. I_{T1}, I_{T2} and I_{T3} correspond to the currents that flow through both the n- and p-channel transistors during switching. I_{CP1}, I_{CP2} and I_{CP3} are the charging currents for the capacitances.

The switching transient caused by an unloaded output changing state typically equals 20 mA peak. *Figure 7b* shows the current and voltage spikes resulting from switching a single unloaded NAND gate. *Figures 7c* through *(e)* show the current spike's increase due to the addition of 15-, 50- and 100-pF loads. The large amount of ringing results from the test circuit's transmission-line effects.

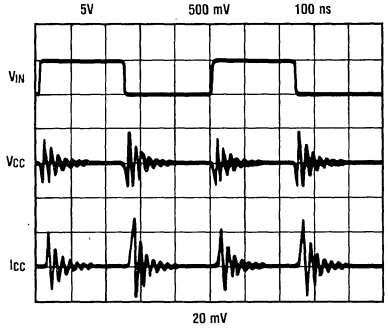
This ringing occurs partly because the CMOS gate switches from a very high impedance to a very low one and back

(a)



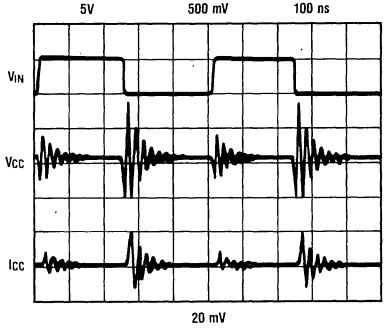
TL/F/8127–11

(b)



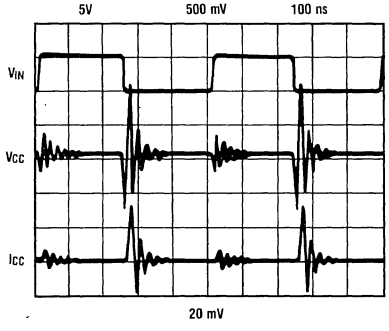
TL/F/8127–12

(c)



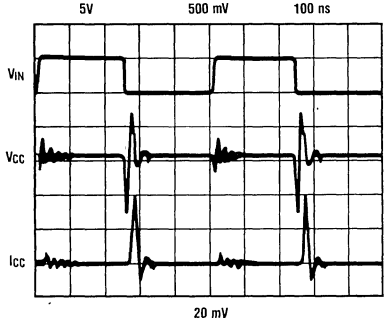
TL/F/8127–13

(d)



TL/F/8127–14

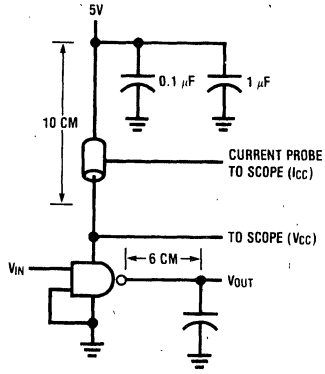
(e)



TL/F/8127–15

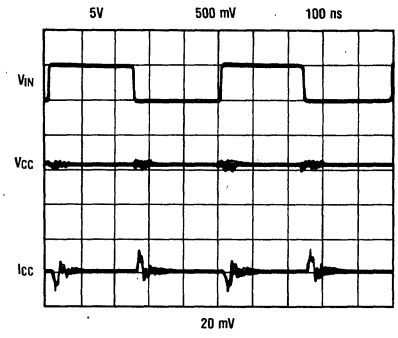
FIGURE 7. The effects of capacitive loads are seen in these photos; (b) through (e) show the spikes resulting with no load and with 15-, 50- and 100-pF loads, respectively. The ringing arises from the test circuit's transmission-line effects.

(a)



TL/F/8127–16

(b)



TL/F/8127–18

FIGURE 8. On-chip circuitry before a 74HC00's output stage (a) generates little current spiking, as shown in the photo (b). In the test circuit, one input is switching (but not the output). Note the very small power-supply glitches provoked by the input-circuit transitions

again. Note that, even for medium-size loads, load-capacitance current becomes a major current contributor, verified by the dramatic increase in current from the unloaded to the 100-pF-load case.

Although internal logic generates current spikes when switching, the bulk of a spike's current comes from output-circuit transitions. Why? Because the outputs have the largest p- and n-channel currents and the greatest parasitic and load capacitances. *Figure 8* shows the I_{CC} current for a 74HC00 gate with one input switching, the other at ground (thus, with no output transitions).

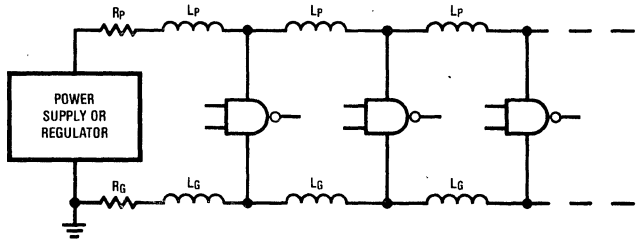
The best way to reduce noise-voltage transients is to implement good power-supply busing. You should maintain a low ac impedance from each circuit's V_{CC} to ground. In one model for a supply bus (*Figure 9*), both V_{CC} and ground traces exhibit inductances, resistances and capacitances.

To reduce voltage transients, keep the supply line's parasitic inductances as low as possible by reducing trace lengths, using wide traces, ground planes, strip-line or microstrip transmission-line techniques and by decoupling the supply with bypass capacitors.

For effective supply decoupling, bypass capacitors must supply the charge required by the current spike for its duration with minimal voltage change. You can determine a bypass capacitor's approximate value from the expression:

$$C_{BYPASS} = \frac{\int dt}{dV} = \frac{\text{(SPIKE CURRENT) (SPIKE DURATION)}}{\text{(ALLOWABLE DROOP VOLTAGE)}}$$

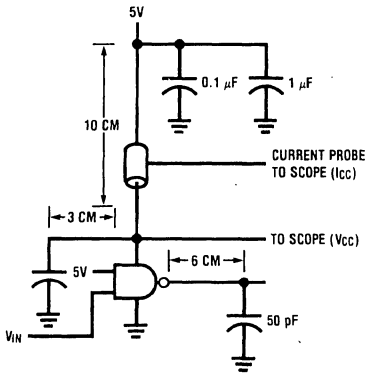
Consider this example: A typical MM54HC/74HC has an I_{CC} transient of about 20 mA, lasting approximately 20 ns (excluding ringing). If you allow 400-mV peak noise, the required bypass capacitance is about (20 mA)(20 ns)/0.4V = 1 nF per output.



TL/F/8127–17

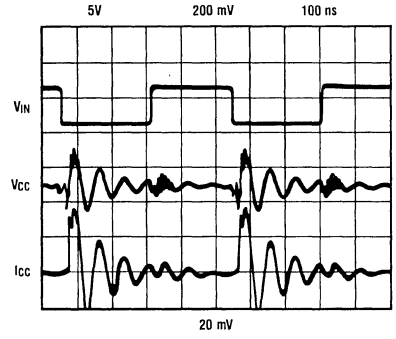
FIGURE 9. This equivalent circuit for a power-supply bus emphasizes both the V_{CC}'s and the ground's series inductances. Try to minimize these inductances through careful circuit layout

(a)



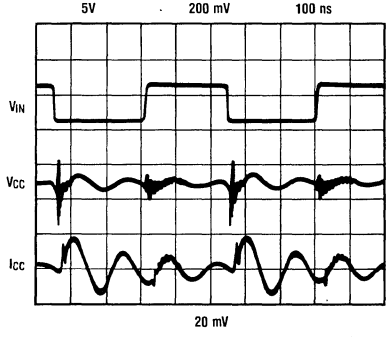
TL/F/8127–19

(b)



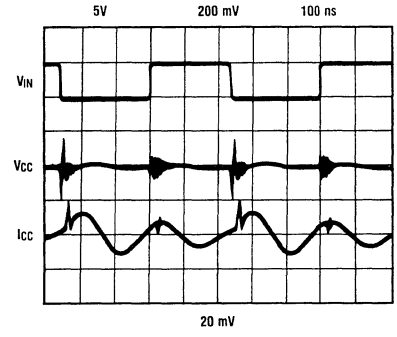
TL/F/8127–20

(c)



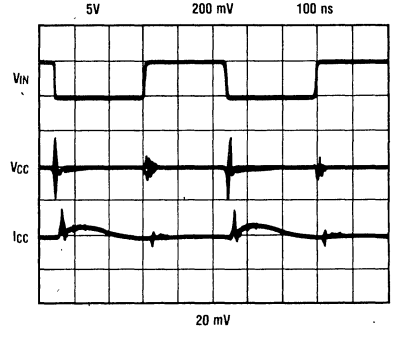
TL/F/8127–21

(d)



TL/F/8127–22

(e)



TL/F/8127–23

FIGURE 10. Demonstrating the importance of bypassing, photos (b) through (e) show power-supply transients that occur when a 74HC00 is decoupled with 1-, 4.7-, 10- and 100-nF capacitors, respectively

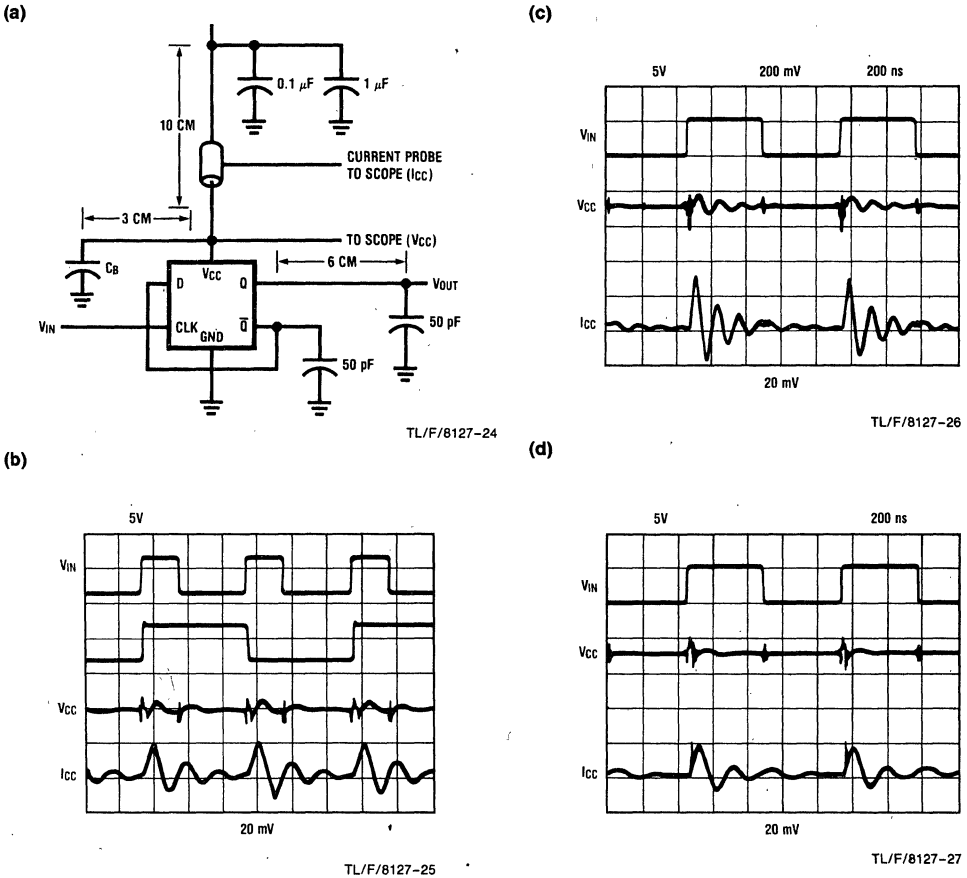


FIGURE 11. Showing results similar to those depicted in Figure 10, these photos show the effects of bypassing a 74HC74 flip flop with capacitors of 1 (b) to 10 nF (d). You can see that the 10 nF bypass yields supply spiking approximately 40% lower than that of the 1-nF capacitor.

In order to prevent additional voltage spiking, this local bypass capacitor must exhibit low inductive reactance. You should therefore use high-frequency ceramic capacitors and place them very near the IC to minimize wiring inductance. The approximate amount of tolerable inductance is given by:

$$L_{SUPPLY} = \frac{Vdt}{di} =$$

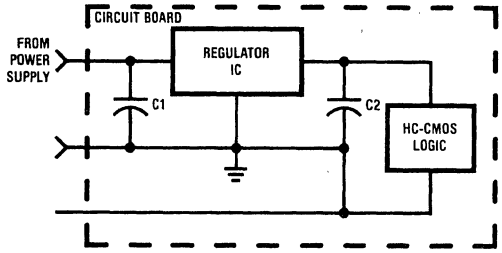
$$\frac{\text{(SPIKE VOLTAGE) (SPIKE RISE OR FALL TIME)}}{\text{(SPIKE CURRENT)}}$$

For example, restricting the inductive noise spike to 100 mV peak with 20 mA current and 4 ns rise time yields (0.4V)(4 ns)/20 mA = 80 nH max. Note that, in addition to localized decoupling of very fast transients, you also need bulk decoupling of spikes generated by the board's ICs. To decouple, provide a high-value capacitor for smoothing long time periods.

To show how decoupling affects supply noise in real-world situations, *Figure 10* depicts the power-supply transients that result when you choose different values of decoupling capacitors. In this example, one gate of a 74HC00 toggles, and 1-, 4.7-, 10- and 100-nF capacitors have approximately 10 cm of wiring between them and the supply. *Figure 11* presents similar results, obtained with the 74HC74 circuit. Note in both cases (although the unbypassed situation isn't depicted) that a 1 nF capacitor greatly reduces the voltage transient.

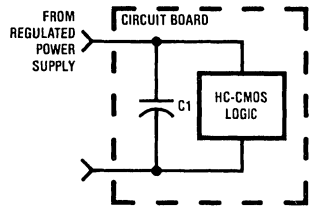
Based on empirical and theoretical considerations, you can determine a set of guidelines. These practical maxims serve only as a foundation for a system that should yield good results. Consequently, there's some leeway in following them for particular designs. As a rule of thumb, it's generally good design practice to restrict both V_{CC} and ground noise to less than 250 mV.

(a)



TL/F/8127-28

(b)



TL/F/8127-29

FIGURE 12. Tailor bypassing to the system's supply scheme. Circuit diagram (a) shows the method to use with local regulators; (b) shows the scheme to adopt with a centralized regulated supply. Use tantalum- or aluminum-electrolytic capacitors.

Before presenting the guidelines, examine some comparative attributes of earlier CMOS, HC, HCT and LS-TTL devices. First, because of higher speeds and larger output currents, the supply-bypassing requirements of HC devices are more rigorous than those of earlier metal-gate-CMOS ICs. Compared with those of LS-TTL, the requirements for HC/HCT are similar or a little more stringent, depending on the application.

Furthermore, for random logic, 54HC/74HC and 54LS/74LS are similar, but in bus-driving applications HC devices can produce larger spikes. Finally, HCT logic needs better grounding than HC logic. In fact, its design considerations closely follow those of LS-TTL. However, as with HC, HCT exhibits greater V_{CC} spiking in bus-driving applications.

Now you're ready for the guidelines:

- Keep V_{CC}-bus routing short. When using double-sided or multilayer circuit boards, use strip-line, transmission-line or ground-plane techniques.
- Keep ground lines short, and on pc boards make them as wide as possible, even if trace width varies. Use separate ground traces to supply high-current devices such as relay and transmission-line drivers.
- In systems mixing linear and logic functions and where supply noise is critical to the analog components' performance, provide separate supply buses or even separate supplies.
- If you use local regulators, bypass their inputs with a tantalum capacitor of at least 1 μF (*Figure 12a*), and bypass their outputs with a 10- to 50-μF tantalum- or alumium-electrolytic capacitor *(b)*.
- If the system uses a centralized regulated power supply, use a 10- to 20-μF tantalum-electrolytic capacitor or a 50- to 100-μF aluminum-electrolytic capacitor to decouple the V_{CC} bus connected to the circuit board (*Figure 12b*).
- Provide localized decoupling. For random logic, a rule of thumb dictates approximately 10 nF (spaced within 12 cm) per every two to five packages, and 100 nF for every 10 packages. You can group these capacitances, but it's more effective to distribute them among the ICs. If the design has a fair amount of synchronous logic with outputs that tend to switch simultaneously, additional decoupling might be advisable. Octal flip flops and buffers in bus-oriented circuits might also require more decoupling. Note that wire-wrapped circuits can require more decoupling than ground-plane or multilayer pc boards.
- For circuits that drive transmission lines or large capacitive loads (μP buses, for example), use a 10 nF ceramic capacitor close to the devices' supply pins.
- Finally, terminate transmission-line grounds near the drivers.

Logic-System Design Techniques Reduce Switching-CMOS Power

National Semiconductor
Application Note 376
Larry Wakeman
October 1984

By adopting certain techniques in the design of your CMOS-based logic system, you can effect dramatic reductions in the transitional power these zero-quiescent-current devices consume when switching.

This article describes ways to reduce the power consumption in logic designs using high-speed CMOS ICs. The MM54HC/74HC logic family has near-zero power dissipation when in the quiescent mode. Its only substantial power drain arises from dynamic switching currents. Traditional TTL and NMOS systems do not share this low-power feature, requiring instead that you reduce power by selecting low-power ICs and external components.

The CMOS device is inherently efficient, but you can greatly enhance system efficiency by designing around the following guidelines:

- minimizing effective system operating frequency;
- minimizing static dc-current paths (eg, in pull-up or -down resistors);
- putting the logic to sleep (by removing the clock);
- capitalizing on power-down situations.

Total system power dissipation is the sum of two components: static (or quiescent) and dynamic power. LS TTL systems consume such a great amount of quiescent power that the dynamic component pales into insignificance. When using 54HC/74HC logic in power-critical applications, however, you must consider both components. The following sections describe how to determine system power by using HC devices' power-dissipation-capacitance (C_{PD}) specs. The text also discusses a few power-reduction philosophies and some of the differences in consumption for 54HCT/74HCT TTL-compatible CMOS logic. Because system power is simply total I_{CC} times the supply voltage, the calculations treat power and current interchangeably.

Calculating the quiescent power is just as easy—the sum of the dc currents times the supply voltage. Thus, total system quiescent power is

$$P_{SYSTEM} = (I_{CC1} + I_{CC2} + \ldots I_{CCn})\, V_{CC}. \qquad (1)$$

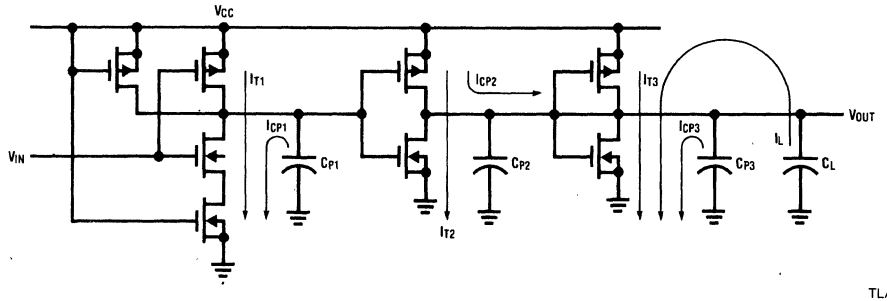
The currents in this expression are caused by pull-up and load resistors and TTL, NMOS and linear circuits in the system. If it's appreciable—although unlikely—you can include the very small quiescent I_{CC} of MM54HC/74HC devices. Generally, the worst-case I_{CC} values in the CMOS ICs' data sheets are very conservative. Typical values range from ten to 100 times less than the limits; moreover, it's almost statistically impossible for a system to contain all worst-case devices.

As pointed out earlier, the major contributors to CMOS ICs' power dissipation are dynamic switching currents. *Figure 1* is a schematic diagram of one 74HC00 NAND gate, and it shows the dynamic currents that result from switching one input Low to High. When the IC is not switching, there's no dc-current path from V_{CC} to ground except for leakage. This is because whenever an n-channel device is On, its complementary p-channel partner is Off.

CMOS power consumption is caused by the transient currents that charge and discharge internal and external capacitances during logic transitions. As frequency increases, these currents naturally increase. You can't measure these currents or their associated capacitances individually, but you can measure the total current. You can equate this total current to a power-dissipation capacitance (C_{PD}) as follows:

$$I_{CC} = (C_{PD} + C_L)(V_{CC})(f_{IC}), \qquad (2)$$

where I_{CC} is the supply current, V_{CC} is the supply voltage, f_{IC} is the input toggle rate and C_L is the toggled load capacitance. Referring again to *Figure 1*, the load current I_L results from switching the load capacitance. To obtain the internal equivalent capacitance, you must subtract the load current from I_{CC}.



TL/F/8128–1

FIGURE 1. Principal contributors to CMOS power consumption, these transient currents are the result of transitional charging and discharging of internal and load capacitances. The average currents are naturally a function of the operating frequency.

Using the C_{PD} figure spec'd in data sheets, you can estimate the current consumption of each device in your system if you know the toggling frequency. By multiplying both sides of **Equation 2** by V_{CC}, you can determine the dynamic power consumption.

$$P_{DYNAMIC} = (C_{PD} + C_L)(V_{CC}^2)(f). \quad (3)$$

As mentioned, C_{PD} is an indirect measure of the amount of switching current a circuit consumes. It depends on how much of the circuit's internal logic is switching and how many outputs are toggling. For example, a 74HC374 octal 3-state flip flop clocked at 1 MHz dissipates much more power if its data inputs change every clock period than it would if its outputs are disabled and its inputs are tied High or Low during clocking.

Figure 3 shows that when the flip flop's outputs are enabled and the data inputs are changing, virtually all internal nodes are toggling and all internal parasitic capacitances are charging. On the other hand, if the data is held High and the outputs are disabled, only the clock logic dissipates power (and very little at that). All other sections are static.

As you'll see, the method of testing C_{PD} (see "Test C_{PD} in realistic situations") can yield various values that might or might not be applicable to the particular way the part is being used. Fortunately, several generalizations allow reasonable approximations to C_{PD}'s value, as discussed in the following section.

TEST C_{PD} IN REALISTIC SITUATIONS

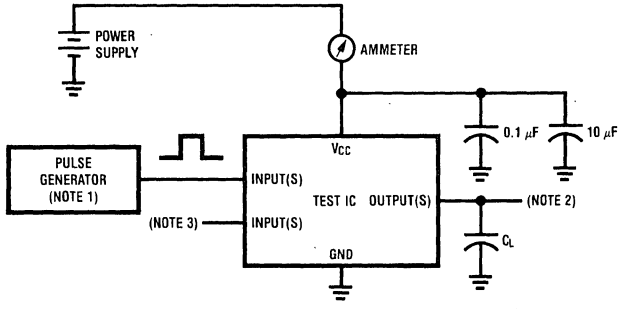
In 54HC/74HC data sheets, one or two C_{PD} values are specified. At best, the parameter is a simplification of the worst-case operating mode of a device under typical operating conditions. However, because most devices have several possible toggling modes (each having a different power consumption), you might do well to characterize C_{PD} for your particular application.

The nearby *Figure 2* shows a circuit for measuring C_{PD}. Normally, the IC is set up in a given toggling mode, with its output pins pulled out of the test socket to reduce stray-induced errors. For automated testing, you could use a standard load (eg, 50 pF) and subtract its I_{CC} contribution from the total. The ammeter in series with the V_{CC} line is bypassed with 0.1- and 1-μF capacitors.

For simple measurements, you can set the input's toggle frequency at 200 kHz, with $V_{CC} = 5V$. This yields an ammeter reading in microamps that's equal to C_{PD} in picofarads. You could use other voltages and frequencies, but little variation should result. For example, JEDEC's high-speed-CMOS committee recommends 1 MHz.

To better understand what datasheet C_{PD} means, the following listing describes by part type how each IC is toggled. In measuring C_{PD}, the worst path is always chosen. Moreover, within the constraints listed, as much of the internal circuitry and as many of the outputs as possible are toggled simultaneously.

- **Gates:** All inputs except one are held at either V_{CC} or ground, depending on which state causes the output to toggle. The one remaining input is toggled at a given frequency. C_{PD} is given on a per-gate basis.
- **Decoders:** One input is toggled, thereby causing the outputs to toggle at the same rate. Normally, one of the address-select pins is switched while the decoder is enabled. All other inputs are tied to V_{CC} or ground, whichever enables operation. C_{PD} is expressed on a per - independent - decoder basis.



TL/F/8128–2

Notes: 1. OUTPUT = square wave with ≤ 6-nsec rise and fall times; levels = GND and V_{CC}.

2. Bend all output pins from test socket, or use known load and deduct its current from measured I_{CC}.

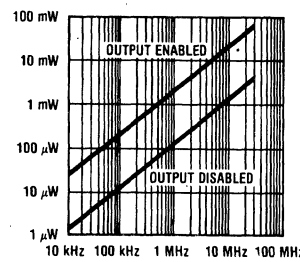
3. Terminate all unused inputs to GND or V_{CC}.

FIGURE 2. Measure equivalent CMOS-system capacitance with this simple test circuit. The text describes how to toggle the various CMOS logic functions (excepting one-shots, of course, which draw dc power).

- **Multiplexers:** One data input is tied high, and a second is tied low. The address-select lines and enable inputs are configured such that by toggling one address line the two data inputs are alternately selected, causing the outputs to toggle. If it's a 3-state MUX, C_{PD} is given for outputs both enabled and disabled. C_{PD} is measured per multiplexer function.
- **3-state buffers and transceivers:** When the outputs are enabled, C_{PD} is measured as for simple gates; ie, on a per-buffer basis. The same holds true for the 3-state condition. Transceivers are measured per buffer as well, both enabled and disabled.
- **Latches:** The device is clocked and data is toggled every other clock pulse. Other preset or clear inputs are held to enable output toggling. If the device has commonly clocked latches, the clock is toggled and one latch is exercised. 3-state latches are measured with their outputs both enabled and disabled. C_{PC} is given on a per-latch basis.
- **Flip flops:** The same as for latches. The device's inputs are configured to toggle, and any preset or clear inputs are held inactive.
- **Shift registers:** The register is clocked and the serial data input is toggled every other clock pulse, as for latches and flip flops. Other clear or load pins are held inactive, and parallel data inputs are held at V_{CC} or ground. 3-state devices are measured with outputs both enabled and disabled. If the device takes parallel loads only, it's loaded with 10101010... and clocked to shift the data out, then reloaded.
- **Counters:** A signal is applied to its clock input; other clear or load inputs are held inactive. C_{PD} is given for each counter within a package.
- **Arithmetic circuits:** adders, magnitude comparators, encoders, parity generators, ALUs and other miscellaneous circuits. The general rule is to exercise these parts to obtain the maximum number of outputs toggling simultaneously while toggling only one or two inputs.
- **Display drivers:** C_{PD} is generally not required for LED drivers, because the LEDs use so much more power they overshadow the drivers' C_{PD}; moreover, when blanked the drivers are rarely driven at any significant speed. If needed, however, C_{PD} is measured with outputs enabled and disabled, while toggling between a lamp test and blank (if provided), or between a display of numbers 6 and 7. LCD drivers are tested by toggling their phase inputs, which control the segment and backplane waveforms. If either of these driver types has latched inputs, the latches are set to a flow-through mode.
- **One-shots:** In some cases, when a device's I_{CC} is significant, C_{PD} might not be specified. When it is, C_{PD} is tested by toggling one trigger input such that the output is a square wave. The timing resistor is tied to a separate V_{CC} line, to eliminate its power contribution.

FIGURING DYNAMIC SYSTEM POWER

How do you calculate a system's dynamic power? You can do it on several levels, depending on the accuracy needed. The simplest approach is to use a C_{PD} model that's the sum of the CMOS ICs' C_{PD}s and the load capacitances. Then, assuming an average frequency, plug these numbers into **Equation 2** or **Equation 3.**



TL/F/8128–3

FIGURE 3. Output status determines dynamic dissipation in this 3-state-output flip flop. The IC dissipates an order-of-magnitude higher power with its outputs enabled.

The most accurate approach, however, is to determine each component's operating frequency and its capacitive load. This method is used in critical battery powered applications. The following section describes this approach and proposes simplifications. In this approach, system dynamic power is the sum of the individual circuits' power dissipation:

$$P_T = P_1 + P_2 + P_3 + P_4 + \text{... etc,} \quad (4)$$

where P_T is the total power and P_n is the power for each component. By substituting **Equation 3** into **Equation 4,** the total system power is

$$P_T = (C_{P1} + C_{L1})(V_{CC}^2)(f) + (C_{P2} + C_{L2})(V_{CC}^2)(f) + \text{...etc.} \quad (5)$$

In **Equation 5,** load capacitances C_{L1}, C_{L2}, etc are not simply the sum of all individual output loads. C_L is actually dependent on device type. Why? Different devices switch a different number of outputs simultaneously. What's more, these outputs can toggle at a different rate from that of the IC's clock or input. Thus, for an individual IC and its load, the actual power is

$$P_{IC} = V_{CC}^2\,[(C_{PD}f) + (C_{L1}f_{L1}) + (C_{L2}f_{L2}) + \text{...}], \quad (6)$$

where C_L is the load on each of the simultaneously toggling outputs, and f_L is the toggle rate seen by the load. A good example is the power dissipation of a 4-bit CMOS counter. Here there are four output terms—each output switches at a different frequency. Accordingly, there are four (each) distinct C_L and f_L terms. To simplify **Equation 6,** define an effective load capacitance C_{LE} which is the actual load multiplied by the ratio of the load toggle rate to the IC's toggle frequency:

$$C_{LE} = (C_L)(f_L/f). \quad (7)$$

Substituting **Equation 7** into **Equation 6** and grouping terms,

$$P_{IC} = V_{CC}^2\, f(C_{PD} + C_{LE1} + C_{LE2} + \text{...}). \quad (8)$$

This procedure simplifies the process because output toggle rates are almost exclusively a binary division of the input clock. Thus, for an accurate calculation of system power, you must calculate it for each IC using **Equation 8** and take the total. The counter is a prime candidate for using **Equation 8.** Here, the first stage's effective output capacitance is half the actual; the second, one-quarter, and so on.

TAILOR f, C TO DEVICE TYPE

To make practical use of the foregoing methods, the following list describes most of the CMOS-logic categories in terms of effective load and operating frequency:

- **Gates and buffers:** Power calculations for these are straightforward. C_{PD}, given for each gate, sums directly with its output load. Operating frequency is the rate at which the output toggles. For disabled 3-state buffers, the power calculation uses the 3-state-output C_{PD} multiplied by the input frequency (no load capacitance included.)
- **Decoders:** Each independent decoder can toggle no more than two outputs at a time. To calculate power consumption, sum C_{PD} with the load on two outputs. The frequency is the rate at which the outputs switch.
- **Multiplexers:** For non-3-state devices, sum the loads on all used outputs and add the sum to C_{PD}. The frequency is that at which the outputs switch. For 3-state devices, use only C_{PD}; the frequency is the inputs' toggle rate.
- **Counters:** The operating frequency for each of a counter's outputs is that of the previous stage divided by two. The loads on lower order stages contribute less current. So to calculate power, sum C_{PD} with one-half the first stage's load plus one-quarter the second stage's, and so on. For decade and other modulo counters, this procedure is slightly different. In general, you can neglect outputs more than four stages removed from the clock. A simple approximation is to sum C_{PD} with the average output load and use the input clock frequency.
- **Latches, flip flops and shift registers:** For these devices, the frequency is the ICs' clock rate. The outputs typically change state at half the clock rate, so when calculating power dissipation, add C_{PD} to half the output load. If the data inputs change more slowly, you can modify the effective load downward by the ratio of the data rate to the clock rate. Again, if the outputs are disabled, no load dissipation exits and you should use the 3-state C_{PD}.

These rules notwithstanding, it's rarely necessary to go through a detailed analysis of each IC. In most instances, a simpler analysis can yield good results. In noncritical applications where power consumption is used to determine the system's power-supply needs, the simpler analysis suffices. Using this method, you estimate the average operating frequency for major sections of the system. Next, sum all the C_{PD}s and effective loads in each section:

$$P_{BLOCK} = V_{CC}^2 f_{AVG} [(C_{P1} + C_{LE1}) + (C_{P2} + C_{LE2}) + \ldots + (C_{Pn} + C_{LEn})]. \quad (9)$$

Thus, to approximate the total system's power consumption, you must approximate the effective loads for each group of devices (or the entire system) and add them together.

Consider a microprocessor-based system using an 8 MHz clock frequency. In this example, you might determine that the bus operates at approximately 2 MHz, random control logic at 4 MHz, and the RAM and I/O devices at 100 kHz. You could estimate an overall system clock to be 1 to 2 MHz, depending on the actual size of each block. Next, you'd sum the C_{PD} and the effective load capacitances—say 2000 and 1000 pF, respectively. The ballpark estimate for system power is

$$P = (5)^2 (1 \text{ MHz})(2000 \text{ pF} + 1000 \text{ pF}) = 75 \text{ mW}. \quad (10)$$

Exceptions to the above rules are one-shot ICs and gates configured as oscillators, which use CMOS in an essentially linear manner. Their power consumption is not strictly attributable to negligible quiescent currents or dynamic switching currents.

Consider one-shots, some of which draw dc current continuously, some only when the output pulse is triggered (check data sheets for the device type you're using). The culprits are the ICs' internal linear CMOS comparators that use dc bias circuits. HC one-shots use several design approaches. One (the 'HC123A/221A/423A) uses a comparator that shuts off after a pulse times out; the second (the 'HC4538) leaves the comparators on at all times.

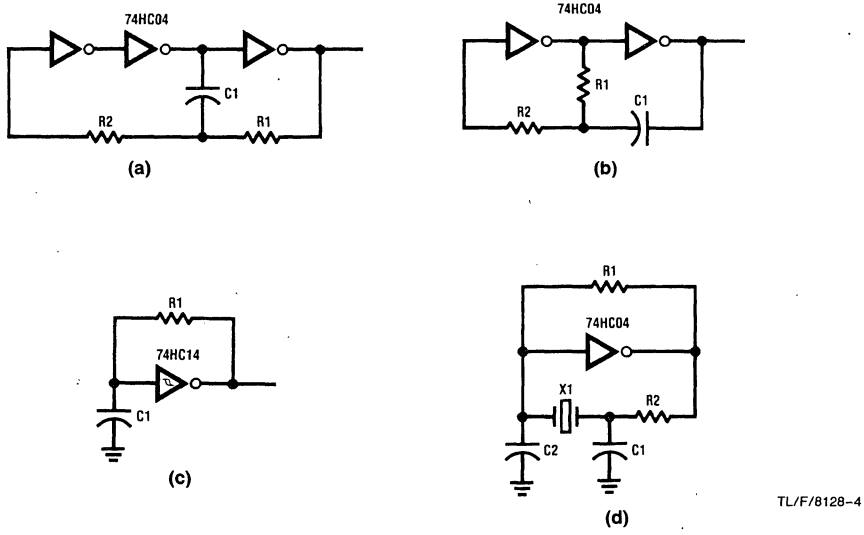


FIGURE 4. Drawing higher-than-calculated power, these CMOS oscillator configurations suffer from "soft" logic levels at their gates' inputs. Circuits (a) through (d) are 3-inverter, 2-inverter, Schmitt-trigger and crystal oscillators, respectively.

A one-shot's overall power consumption is its quiescent power plus the power consumed by its timing elements and C_{PD}. If the comparators turn off, you multiply the quiescent current by the duty cycle of the output pulse. Thus, the overall expression for one-shot power consumption is

$$P_{OS} = (I_{CC})(V_{CC})(D) + (C_{EXT} + C_L + C_{PD})(V_{CC}^2)(f), \quad (11)$$

where P_{OS} is the total power, D the one-shot's duty cycle, C_{EXT} the timing capacitor, C_L the load on both outputs, and f the operating frequency. In general, the C_{PD} term is small at lower frequencies; you can safely set it to zero to simplify the equation.

What about oscillators? The circuits shown in *Figure 4* draw more current at a given operating frequency than you'd calculate using only C_{PD}. This is because in these applications, the inputs to some of the gates are at "soft" logic levels for significant amounts of time. This causes both p- and n-channel transistors to conduct simultaneously and hence draw dc current.

Figure 5a plots current vs input voltage for the 74HC00 gate and gives an idea of the amount of current typically drawn when soft logic levels are applied. The large spike at 2.3V is the result of the output's switching. At low frequencies, the oscillator's supply current can be several milliamps higher than you might expect because of the amount of dc current drawn.

The same is true of a 74HC14 used as an oscillator. *Figure 5b* shows the supply current vs input voltage for the 74HC14 and the 74C14 (or CD40106). Because the actual power consumed vaires with frequency and component values, it's best to determine it empirically. As with the one-shots, the oscillator timing capacitor's contribution to power dissipation can be expressed by $P = V_{CC}(C_t)f$.

MM54HC/74HC logic uses bigger devices and lower transistor thresholds than metal-gate CMOS, so it might be more desirable to use either CD4000 or MM54C/74C logic for lower power oscillators (if operating frequency and output-drive requirements permit.)

MORE SPECIAL CASES: HCT

Because of their unique applications in TTL and NMOS systems, 54HCT/74HCT devices have some additional traits that you should consider in designing systems. In TTL systems, the HCT ICs' inputs are driven under worst-case conditions by TTL levels of 0.5 and 2.4V. With these input levels applied, HCT consumes significant quiescent current: about 200 to 500 μA per input. You must consider this dc current when calculating power.

To see the origins of this quiescent current, refer to *Figure 6,* which shows a typical HCT's input. With a 2.4V input level, the n-channel transistor turns fully on; the p-channel device turns slightly on. This scenario results in a quiescent current dependent on the number of logic-One inputs applied. The 0.5V level is close enough to ground to cause the n-channel transistor to turn off, so HCT ICs draw quiescent current only when its inputs are at a high state.

The I_{CC} values with these logic levels are specified in the HCT data sheets. It's specified on a per-input basis—this allows you some flexibility in determining quiescent power when an IC is driven by both CMOS and TTL. The specified quiescent-current value results in calculated I_{CC} values of several milliamps per IC, significantly less than that of LS TTL circuits.

Note, however, that using this data-sheet approach yields current values roughly five times higher than that actually seen in system designs. The reason for this is that the I_{CC} test is spec'd at $V_{CC} = 5.5V$ and $V_{IN} = 2.4V$, but even worst-case TTL output-High levels are at least 3.4V under these conditions. Output levels can only attain a low 2.4V with $V_{CC} = 4.5V$. Moreover, both TTL and NMOS outputs typically assume levels closer to 3V (at $V_{CC} = 4.5V$), lowering quiescent current more. The point is, don't let I_{CC} specs scare you into thinking CMOS is a power hog.

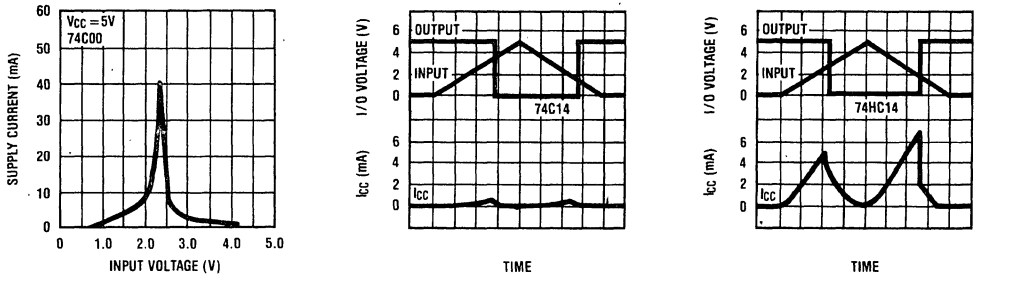


FIGURE 5. "Soft" logic levels cause high currents in a 74HC00 inverter (a) and a 74HC14 connected as an oscillator (b,c). Because the power varies with frequency and component values, it's best to determine its value empirically.

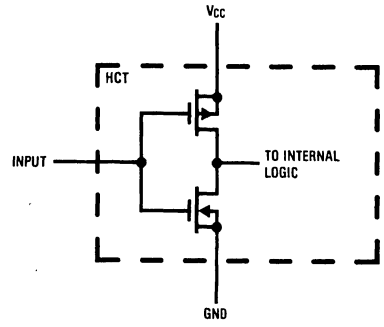
In mixed TTL-CMOS applications, the calculation of power consumed by the HCT logic must take into account both the dynamic and the quiescent currents.The dynamic portion is the same as that for HC logic—in fact, C_{PD} is measured with 0 and 5V input levels to exclude any quiescent current. The static portion is the sum of the number of TTL logic-One inputs times their High-period duty cycle times the current per input. For a single IC, the power consumption is

$$P_{IC} = (V_{CC})(I_{CC})(N)(D) + V_{CC}^2 f(C_{PD} + C_{LE}), \quad (12)$$

where C_{LE} is defined as before, N is the number of TTL-driven inputs and D is the logic-High duty cycle.

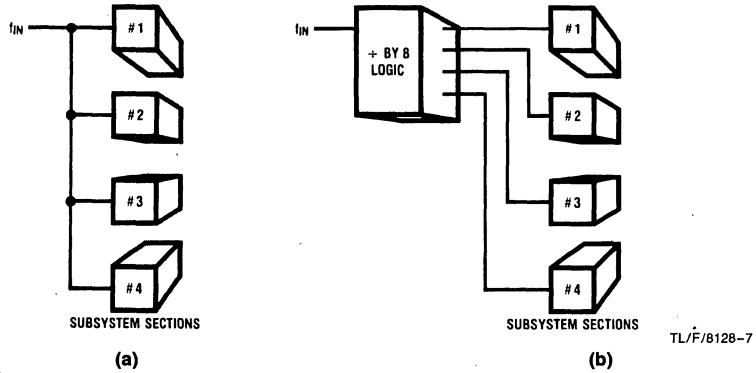
I_{CC} is the data sheet's per-input spec. This expression can then be one term in **Equation 4.** If you're using the package-level quiescent current, the terms N and D drop out.

What about a situation in which HC drives HCT? In this scenario, ground and V_{CC} levels are applied, thereby ensuring that the p- and n-channel transistors don't turn on simultaneously. You can thus determine HCT power dissipation just as for HC by using C_{PD}.



TL/F/8128–6

FIGURE 6. TTL-compatible CMOS is a special case. This schematic shows the 54HCT/74HCT family's input buffer. With a 2.4V input applied, the n-channel transistor is fully On; the p-channel, slightly On.



TL/F/8128–7

FIGURE 7. Reducing clock rate—but not throughput—this scheme allows you to reduce power by clocking a system's n subsections only as fast as needed, instead of clocking all system blocks at the full clock frequency

NOW LET'S REDUCE POWER

When designing low-power CMOS systems, there are several ways to minimize power. These methods involve reducing operating frequencies, cutting system load capacitances, using fast input transition times and minimizing any dc-current paths.

First, for low-power system implementations, it's important not to overdesign the operating frequency. Very simply put, it makes no sense to clock a counter at 20 MHz when 5 MHz will suffice.

Note that a reduction in overall system clock frequency doesn't necessarily entail a reduction in throughput. For example, consider a system consisting of four subsections, clocked at 8 MHz *(Figure 7a)*. Rather than clocking all sections in parallel, you can reduce power by clocking each section only as fast as need be *(Figure 7b)*. A second example of reducing the overall system clock rate is shown in *Figure 8*.

In (*a*), a CMOS memory array is driven directly from the CPU's address bus. Here, every memory is driven at the bus frequency. If, however, the address is latched by each memory block only when that block is being accessed (*b*), then only the block currently being accessed is clocked. This is why some CMOS RAMs incorporate on-chip address latches.

Another way to operate a system at the minimum possible frequency is to switch the system clock. The system is thus made to operate at the highest frequency only when needed. *Figure 9* shows the logic used to implement this scheme for a CMOS μP system. In this method, there are two oscillators, either of which can feed a divide-by-two circuit that provides a square-wave output. The flip flop's output is the system clock. The system's μP can set or reset the flip flop so that it can operate at either frequency.

Besides frequency reduction, there are several other methods to save power, including reducing load capacitances. You can accomplish this by reducing wiring capacitance (especially in high-frequency sections) through good layout practices, and by maintaining close proximity between interrelated high-frequency sections. In some instances where you might instinctively parallel several unused inputs, you can achieve lower load capacitance by tying the unused inputs to a supply. In another example, when using RC oscillators, it's best to use the smallest capacitor and the largest resistor possible.

Slow input transitions can cause extra dissipation. If an input signal rises slowly, it causes both input transistors to conduct for a longer time, thereby causing more current to flow. One rule of thumb is if rise and fall times are shorter than 25 nsec, minimal current will flow. But don't go overboard. Be aware that slow transitions are more tolerable in slower operating sections because the transitions occur less often. Therefore, weigh the importance of the extra dissipation against the cost of speeding signals up.

It's important to point out that floating inputs can result in unnecessary power dissipation. If inputs are open, the input

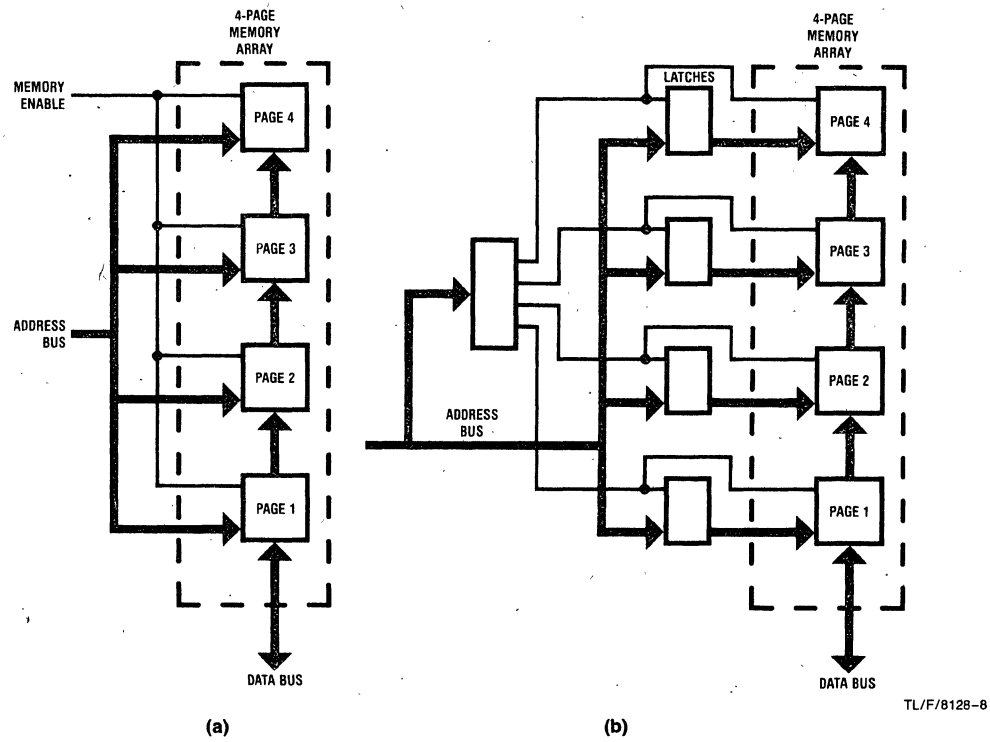
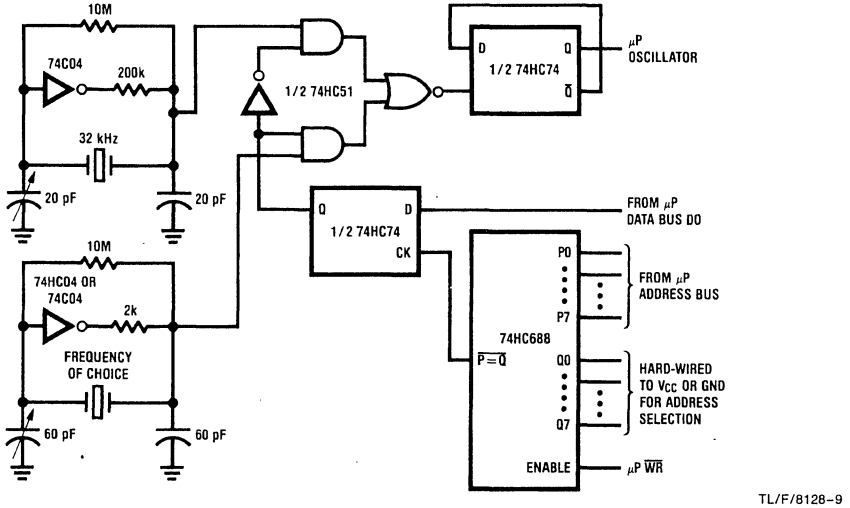


FIGURE 8. Latching memories' addresses (b) can reduce system power. In (a), every memory is driven at the bus frequency. By contrast, in (b)'s configuration, only the memory block being addresed is clocked.



TL/F/8128–9

FIGURE 9. Switch your system's clock frequency for reduced power consumption. The circuit shown is a software-selectable oscillator for a microprocessor system.

voltage can float to an indeterminate and intermediate level; thus, don't float CMOS Inputs. This action can turn on both p- and n-channel transistors, resulting in supply-current drain. In bus-oriented systems, don't allow the bus to become completely 3-stated or float for extended periods because this will have the same effect as leaving inputs open.

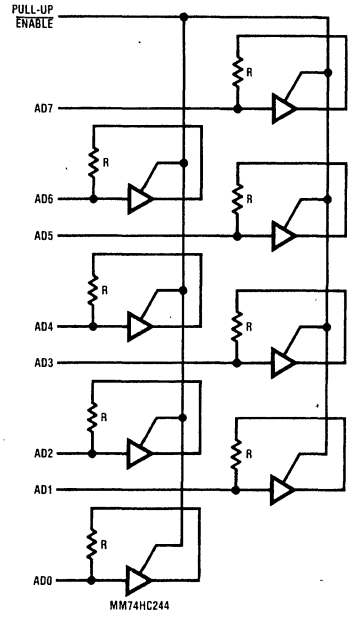
Bus structures subject to prolonged 3-state conditions should be terminated to ensure that the bus lines pull to either V_{CC} or ground. For short durations, the bus capacitance can maintain valid logic levels, so for short-time floating, pull-up or -down resistors might not be necessary.

Finally, make sure your design ensures solid V_{CC} and ground logic levels at 54HC/74HC inputs. If the logic Low is greater than 0.5V or the logic High is lower than $V_{CC}-0.5V$, then the normally Off p- or n-channel transistor can actually conduct slightly, causing additional I_{CC} to flow (similarly to the previously discussed HCT "soft" levels).

BE WARY OF STATIC LOADS

Previous sections discussed the effects of capacitive loads on system power dissipation. What about resistive loads? In ultra-low-power systems, their contribution can be significant, so it's important to find ways to eliminate or minimize their detrimental effects. The loads could be pull-up resistors, bus terminators, displays, relays or peripheral drivers. Of course, the most obvious way to reduce power is to select low-power relays or displays, for example, and to make resistor values as high as possible. In addition, you can switch these loads out of the circuit when not needed.

Figure 10 shows a circuit that dissipates no static power; you can use it to terminate a 3-state bus to the last active logic level seen on the bus. This technique is useful to ensure the bus doesn't float when 3-stated. The circuit uses a 74HC244 whose input is tied to its output. If the terminating resistors must be completely turned off, use the 3-state Enable.

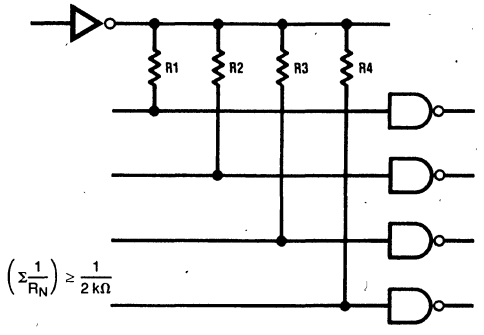


TL/F/8128–10

100 Ω < R < 200k

FIGURE 10. Dissipating zero static power, this scheme can serve to terminate a 3-state bus to the last active logic level seen on the bus. To disconnect the terminating resistors, use the 3-state Enable command.

Figure 11 illustrates a method of controlling a series of pull-up resistors using the output of an HC gate or 3-state buffer. Because HC outputs can pull up to V_{CC}, you can use them as an enable for many pull-ups, as long as the parallel combination of the pull-up resistors exceeds 2 kΩ. You can also use the method for pull-down resistors.



TL/F/8128–11

FIGURE 11. Enable or disable pull-up resistors with this configuration. You can use an HC device's outputs to enable several pull-ups. The scheme is also applicable to pull-down resistors.

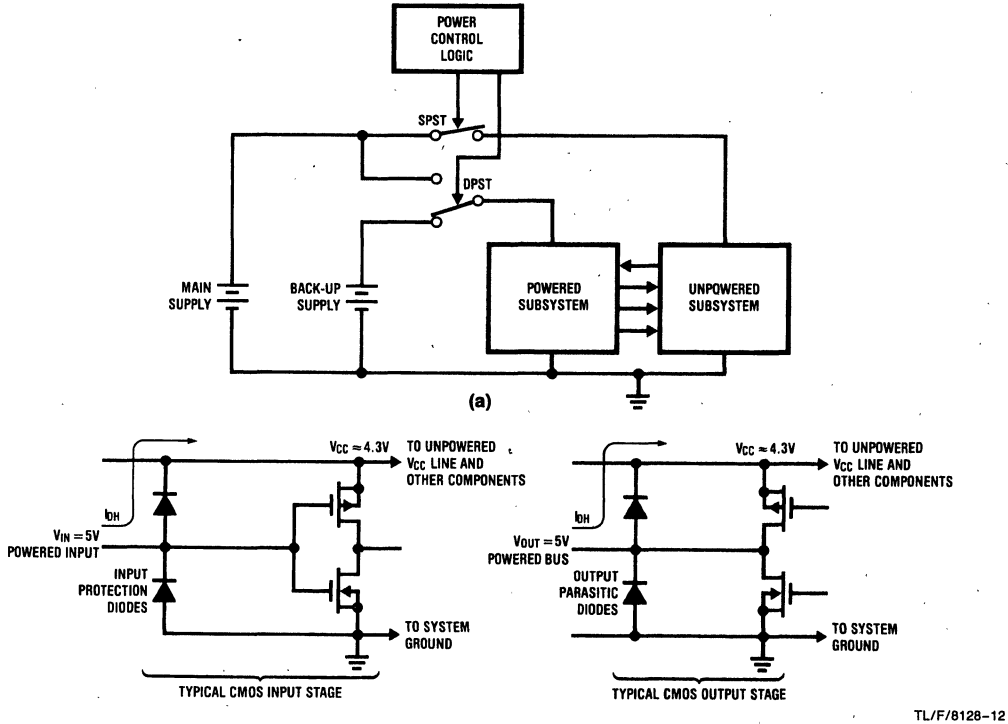
When considering whether you should add circuitry to disable pull-up resistors, remember that in CMOS systems, the pull-ups only dissipate power when the driving output is low. No power is consumed when the driving output is high or at the 3-state level (disabled).

THE FINAL SOLUTION: POWER DOWN

When all else fails, the best way to reduce system power is to shut off the system or unnecessary parts. Before you do this, keep in mind that turning off the clock to a section of the system is almost tantamount to turning the section off (thanks to the ICs' low leakage currents). The advantage of the clock-killing approach? It avoids the complications of the power-down methods that follow.

Still, there are occasions in which parts of a system are powered down. When all or part of a system is shut off, or when one of several interconnected systems is powered down, you should respect several criteria to avoid spurious signals during the power-down period, and to eliminate possibly fatal conditions.

One condition that requires very careful consideration is the application of high-level signals to unpowered HC devices. *Figure 12a* shows in block form the basic concepts of powering down part of a system. In this scenario, it's possible to apply a logic One to the unpowered CMOS logic. If this happens to either an input *(b)* or a 3-state output *(c)*, the device will still be powered.



TL/F/8128–12

FIGURE 12. This basic power-up and -down system (a) presents dangers to CMOS-logic ICs. As the input (b) and output (c) schematics show, a logic One can actually power up the "unpowered" system, thereby causing damage to input and output diodes.

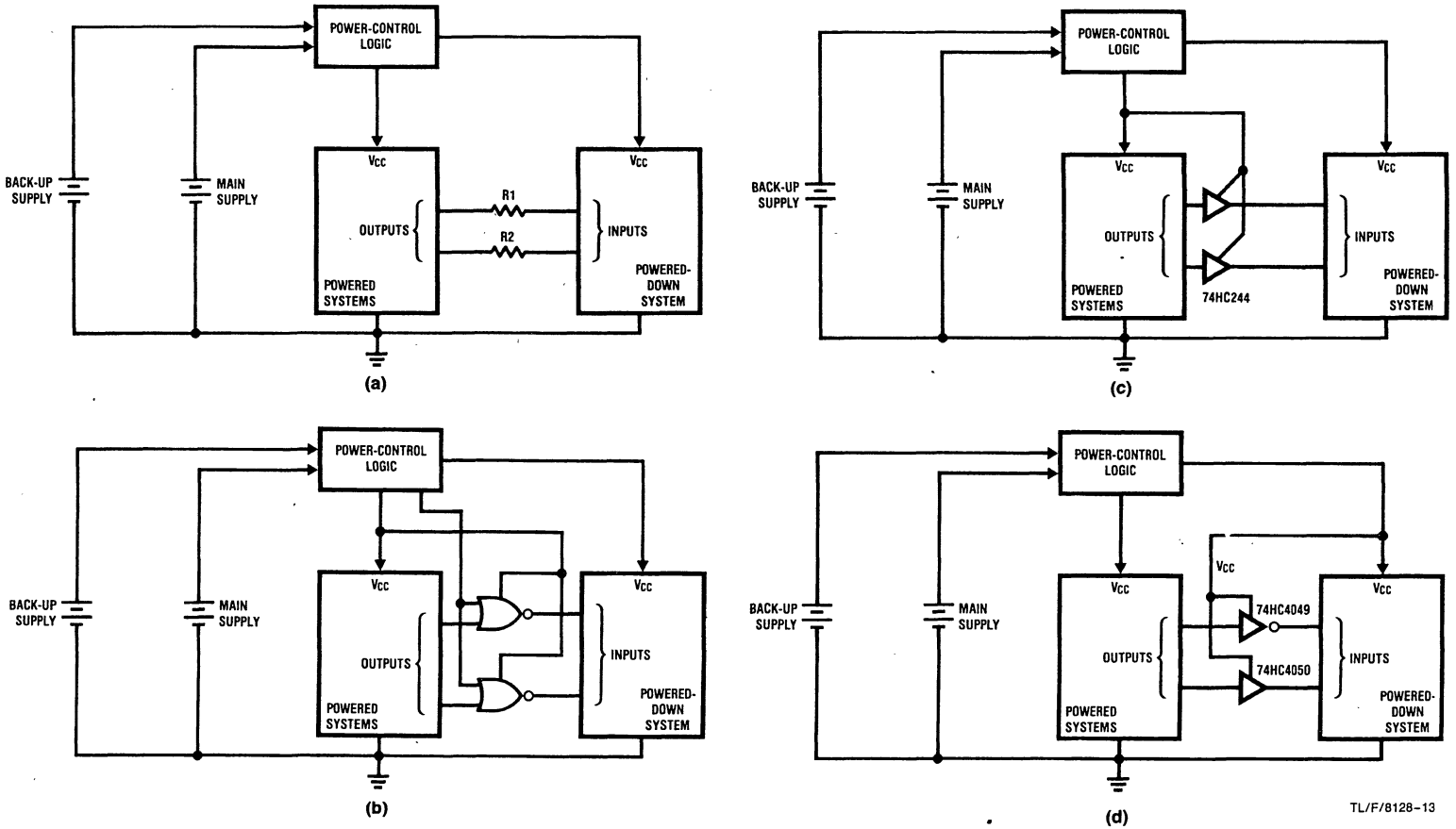


FIGURE 13. Solutions to the problems in *Figure 12*, these configurations protect CMOS circuits' inputs and outputs in power-down situations. The brute-force solution in (a) limits input currents; (b)'s scheme forces inputs to ground; in (c), 3-state gates disable the inputs. In (d), 74HC4049 or -4050 level translators isolate inputs from the power supply.

Referring again to *Figures 12b* and *12c,* the input protection diodes and the output parasitic diodes form a path to the V_{CC} pin. The voltage at this pin will be $V_{IN}-0.7V$. The "unpowered" system is really powered up by the logic signal through these diodes. If the "unpowered" V_{CC} line accepts appreciable current, diode damage can (and usually does) result.

Figure 13 shows several solutions to the signal-powered "unpowered" problem. A resistor in series with each input (*a*) limits the current to 20 mA max. This low-cost, brute-force solution has the undesirable tendency, however, to dissipate power from the supply.

To avoid extra power consumption, you can use the methods in *Figures 13b* to *13d.* Upon removal of power, additional logic can force all inputs to ground *(b).* Alternatively, 3-state logic can disable the signals by presenting an open circuit *(c).* The third possible solution *(d)* is to use a 74HC4049 or 74HC4050—circuits that lack a V_{CC} diode. In this case, even when power is removed the inputs are isolated from the power supply.

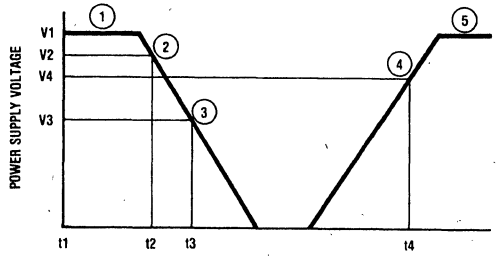
A situation analogous to the previous section's might occur on bidirectional buses or in "party-line" media, where 3-state output devices are powered down on the bus. In this case, power down all but the 3-state buffer, as shown in *Figure 14.* Because the buffers inputs are shut off, the IC draws negligible extra power.

In addition to ensuring that power-down proceeds smoothly, it's important to guarantee that spurious signals from the subsystem that's shutting down do not cause logic errors in the powered section. For example, battery-backed memory must be controlled to prevent spurious writes by the host processor that's shutting off.

Figure 15 illustrates a method for eliminating spurious operation upon loss of power. First, the system detects the loss of system power prior to the system's malfunction by comparing the system voltage to an arbitrary minimum voltage (V_2), or by directly monitoring the ac line for loss of 50 or 60 Hz. Having detected this loss, the system should perform all bookkeeping operations to prepare for power-down before the minimum correct operating voltage (V_3) is attained.

At V_3, the system cannot be guaranteed to function correctly—therefore, powered logic should disable all signals that might affect the powered or battery-backed subsystem. Once stable power is restored to the minimum operating voltage (V_4), the signals should be re-enabled.

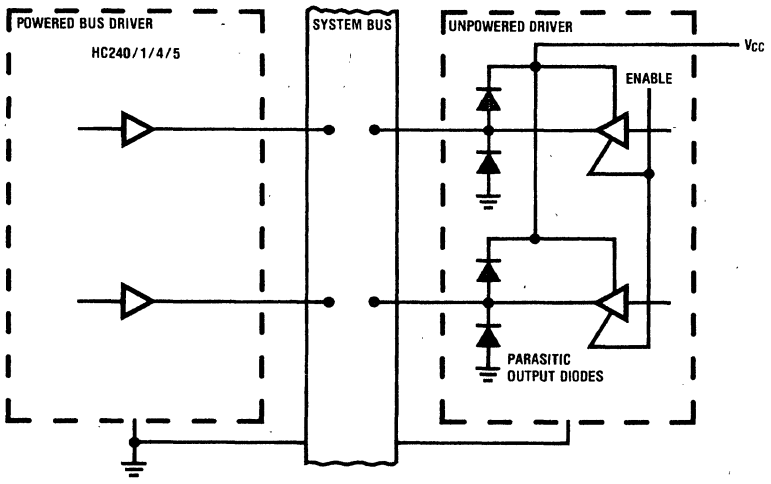
Clearly, there is more to shutting off a system (while leaving part of it powered by a backup battery) than just switching the power supplies. The primordial design consideration when powering down a system is to ensure that spurious signals do not destroy valuable data or logic conditions in the battery-operated subsystem.



TL/F/8128–15

①NORMAL SYSTEM OPERATION
②LOW-VOLTAGE POWER-FAIL DETECT
③MINIMUM OPERATING VOLTAGE
④MINIMUM RESTORED OPERATING VOLTAGE
⑤NORMAL SYSTEM OPERATION

FIGURE 15. Prevent spurious host-processor write operations in battery-backup systems by using this graph's concepts. To sum up, the system should prepare itself for power-down before minimum-operating voltage V_3 is reached, and re-enable signals when V_4 is attained upon power-up.



TL/F/8128–14

FIGURE 14. Powering down all but the 3-state buffer, this method protects CMOS ICs' output-protection diodes. The buffers draw negligible system power.

DC Noise Immunity of CMOS Logic Gates

National Semiconductor
Application Note 377
Vivek Kulkarni
July 1984

Introduction

The immunity of a CMOS logic gate to noise signals is a function of many variables, such as individual chip differences, fan-in and fan-out, stray inductance and capacitance, supply voltage, location of the noise, shape of the noise signal, and temperature. Moreover, the immunity of a system of gates usually differs from that of any individual gate; thus a generalized analysis of the noise immunity of a logic circuit becomes a very complex process when one takes all the above parameters into consideration.

The complementary structure of the inverter results in a near-ideal input-output characteristic with switching point midway (45%–55%) between the "0" and "1" output logic levels. The result is a high noise immunity (defined as the maximum noise voltage which can appear on the input without switching an inverter from one state to another). National's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 45% of the power supply voltage typically will not propagate through the circuit. However, the standard guaranteed value through the industry is 30%.

This note describes the variation of the transfer region (or DC noise immunity) of a multiple-input gate in conjunction with the gate configuration—a consideration important in the system design.

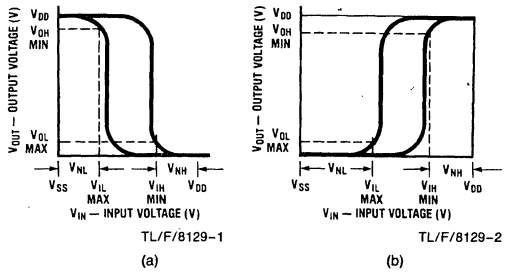


FIGURE 1. Minimum and Maximum Transfer Characteristics for (a) Inverting Logic Function and (b) Noninverting Logic Function

Transfer Characteristics

FIGURE 1 illustrates minimum and maximum transfer characteristics useful for defining noise immunity for an inverter and a non-inverter. Some definitions are as follows:

$V_{IH\ min}$ = the minimum input voltage high-level input for which the output logic level does not change state.

Then:

$V_{NL} = V_{ILmax}$ = "low level" noise immunity

$V_{NH} = V_{DD} - V_{IH}$ = "high level" noise immunity

V_{OHmin} = minimum high level output voltage for rated V_{NL} [for inverting function as in *Figure 1(a)*]

Table 1 shows the UB and B series noise immunity and noise margin ratings determined by the Joint Electron Devices Engineering Council (JEDEC). B series ratings are slightly higher than the UB series because of the buffered nature of these gates.

TABLE I. UB and B Series DC Noise Immunity and Noise Margin ($T_A = 25°C$)

Characteristics	Test Conditions		Input Voltage
	V_O (V)	V_{DD} (V)	(V)
Input Low Voltage			
V_{IL} max			
B types	0.5/4.5	5	1.5
	1/9	10	3
	1.5/13.5	15	4
UB types	0.5/4.5	5	1
	1/9	10	2
	1.5/13.5	15	2.5
Input High Voltage			
V_{IH} min			
B types	0.5/4.5	5	3.5
	1/9	10	7
	1.5/13.5	15	11
UB types	0.5/4.5	5	4
	1/9	10	8
	1.5/13.5	15	12.5

Since the MOS transistors are voltage-controlled resistors, the transfer characteristics and consequently the DC noise immunity are determined by the parallel series combination of the transistor impedances in conjunction with the input voltages, the number of inputs, and the gate circuit configuration. This consideration becomes more important for a system designer who has harsh-noise-prone applications.

The value of the standard transistor ON resistance may vary from 10 MΩ down to almost 30Ω (depending on the dimensions of the MOS-FET and applied voltages). For different input conditions, different combinations of the impedances of the N-channel transistors connected in parallel and the P-channel transistors connected in series will come into play for a NOR gate. This is illustrated in *Figure 2*. For a NAND gate, similar considerations hold good and give rise to varying transfer characteristics as shown in *Figure 3*.

Example of CD4001

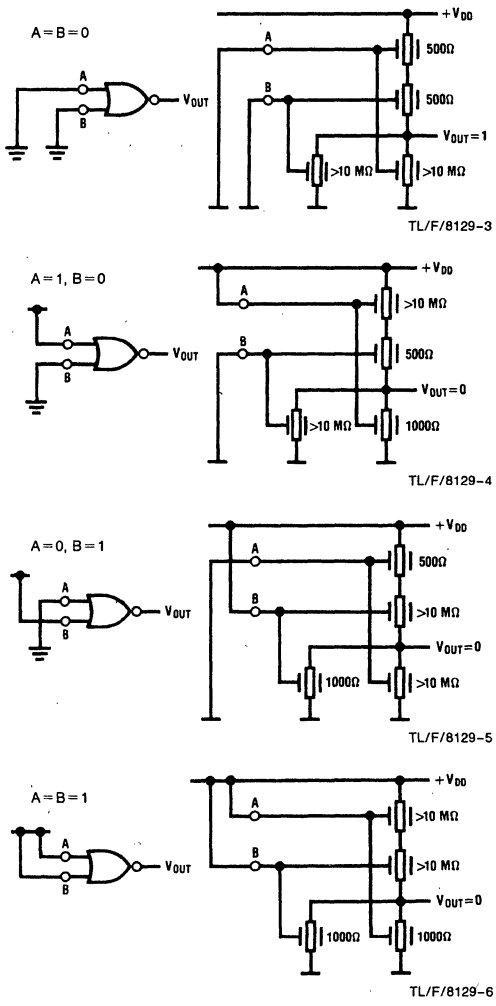


FIGURE 2. Typical Transfer ON/OFF Resistances for Various Input Combinations for CD4001

Analysis

The DC transfer characteristics of the CMOS inverter can be calculated from the simplified DC current-voltage characteristics of the N- and P-channel MOS devices.

In the transfer region, where both transistors are in saturation, the following relationships can be used for an inverter.

N-channel drain current will be:

$$I_{dsn} = \frac{K_n}{2}(V_{IN} - V_{TN})^2 \quad (1)$$

P-channel drain current will be:

$$-I_{dsp} = \frac{K_p}{2}(V_{IN} - V_{DD} - V_{TP})^2 \quad (2)$$

where:

$$K_n = \frac{\mu n\, C_{ox}\, W_n}{L_n},\ K_p = \frac{\mu p\, C_{ox}\, W_p}{L_p}$$

Taking the ratio of (2) and (1):

$$\frac{|I_{dsp}|}{I_{dsn}} = \frac{K_p}{K_n} \cdot \frac{(V_{IN} - V_{DD} - V_{TP})^2}{(V_{IN} - V_{TN})^2}$$

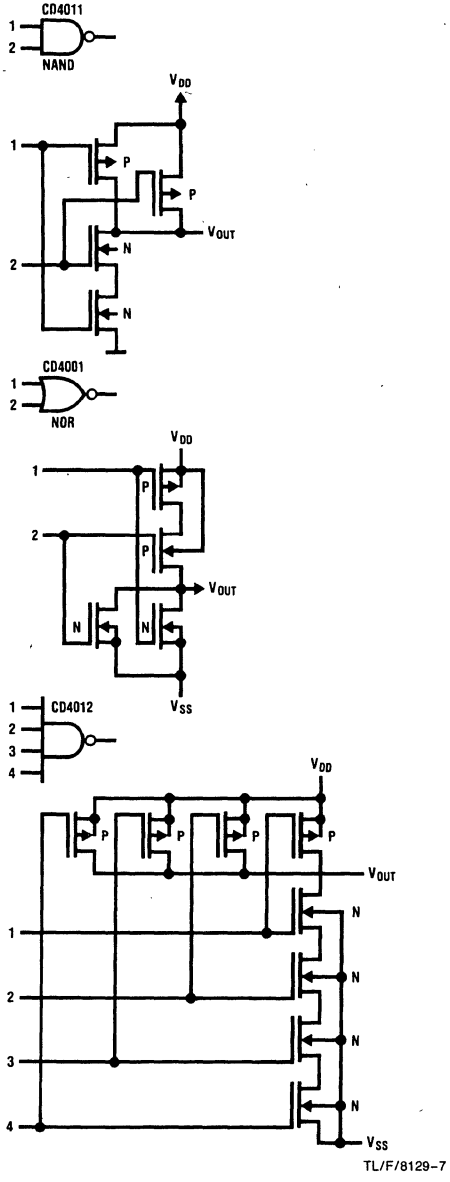
$$\frac{K_p}{K_n} = \frac{|Idsp|}{I_{dsn}} \cdot \frac{(V_{IN} - V_{TN})^2}{(V_{IN} - V_{DD} - V_{TP})^2} \quad (3)$$

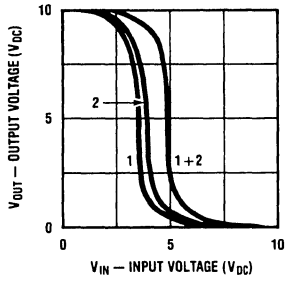
Studies made at National show good correlations between the process monitor pattern and actual device on a wafer for drive currents. Thus the ratio K_p/K_n can be calculated for the actual device if one knows drive currents for the test pattern, widths of N- and P-channel devices and threshold voltages from a given process.

The transition voltage is calculated from basic current equations and from the fact that some current has to flow through P- and N-channel devices. Equating saturation currents and rearranging terms, one can obtain[1]:

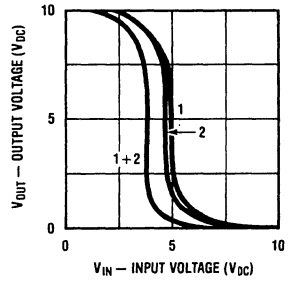
Transition Voltage $= V_{IN}^*$

$$= \frac{V_{TN} + \sqrt{\frac{K_p}{K_n}}(V_{DD} - |V_{TP}|)}{\sqrt{1 + K_p/K_n}} \quad (4)$$

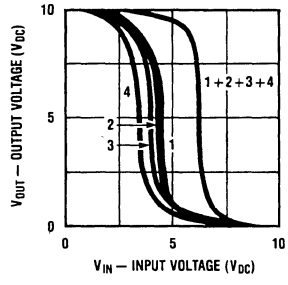




TL/F/8129-8



TL/F/8129-9



TL/F/8129-10

FIGURE 3. Allowed Voltage Transfer Curve Shifts which Result Due to Various Input Combinations of Multiple Input Gates

By selecting $|V_{TP}| = V_{TN}$ and $K_p = K_n$, transition voltage can be designed to fall midway between 0V and V_{DD}—an ideal situation for obtaining excellent noise immunity. However, it is not always possible to obtain equal threshold voltages because of process variations. Also, W/L ratio for a P-channel device must be made 2 or 3 times larger than W/L ratio for an N-channel device to take into account mobility variations. The designer should consider these factors when designing for the best noise immunity characteristics.

In equation (4), the value of K_p/K_n substituted is obtained from equation (3). With different gate configurations, effective W_p and W_n values change; also, K_p/K_n ratio changes and a shift in transfer characteristics results.

For the 4-input NOR gate like CD4002, an empirical relation for the low noise margin V_{NL} has been obtained, which is as follows:

$$V_{NL} \approx V_{DD}\left[\frac{1}{1.5 + \frac{N_i}{N_m}} - 0.1\right] \quad (5)$$

where:

N_i = number of used inputs/gate

N_m = total number of inputs/gate

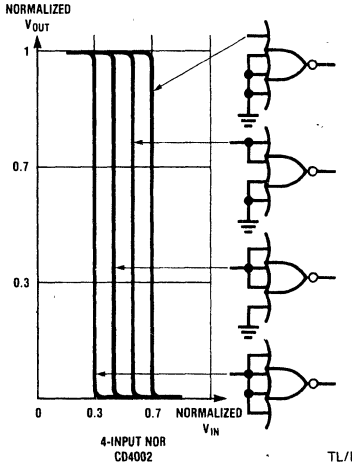
The input voltage high noise margin V_{NH} can be calculated by:

$$V_{NH} \approx V_{DD}\left[0.9 - \frac{1}{1.5 + \frac{N_i}{N_m}}\right] \quad (6)$$

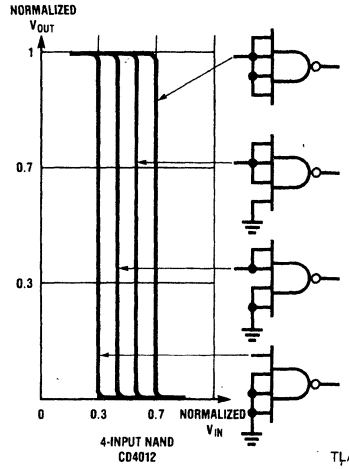
Similar equations can be derived for a NAND gate.

From equations (5) and (6), one can see that the low noise margin V_{NL} will *decrease* as a function of the number of controlled inputs, while it will increase for a NAND gate. The input HIGH noise margin will *increase* as a function of the number of controlled inputs for the NOR gate; for the NAND gate it will decrease.

Figure 4 depicts $V_{OUT} = f(V_{IN})$ for different configurations for NOR and NAND gates. The system designer can thus use these facts effectively in his design and obtain the best possible configuration for the desired noise immunity with National's logic family.



TL/F/8129–11



TL/F/8129–12

FIGURE 4. Example of Transfer Voltage Variation for NOR and NAND Gates for Various Input Combinations

1. Carr, W.N., and Mize, J.P., *MOS/LSI Design and Application*, Texas Instruments Electronic Series, 1972

MM54C/MM74C Voltage Translation/Buffering

National Semiconductor
Memory Brief 18
John Jorgensen
Thomas P. Redfern

INTRODUCTION

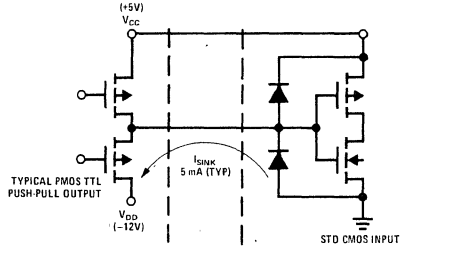
A new series of MM54C/MM74C buffers has been designed to interface systems operating at different voltage levels. In addition to performing voltage translation, the MM54C901/MM74C901 through MM54C904/MM74C904 hex buffers can drive two standard TTL loads at V_{CC} = 5V. This is an increase of ten times over the two LpTTL loads that the standard MM54C/MM74C gate can drive. These new devices greatly increase the flexibility of the MM54C/MM74C family when interfacing to other logic systems.

PMOS TO CMOS INTERFACE

Since most PMOS outputs normally can pull more negative than ground, the conventional CMOS input diode clamp from input to ground poses problems. The least of these is increased power consumption. Even though the output would be clamped at one diode drop (−0.6V), all the current that flows comes from the PMOS negative supply. For TTL compatible PMOS this is −12V. A PMOS output designed to drive one TTL load will typically sink 5 mA. The total power per TTL output is then 5 mA x 12V = 60 mW. The second problem is more serious. Currents of 5 mA or greater from a CMOS input clamp diode can cause four-layer diode action on the CMOS device. This, at best, will totally disrupt normal circuit operation and, at worst, will cause catastrophic failure.

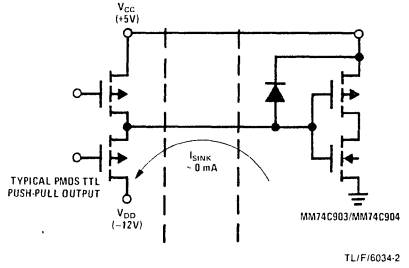
To overcome this problem the MM74C903 and MM74C904 have been designed with a clamp diode from inputs to V_{CC} only. This single diode provides adequate static discharge protection and, at the same time, allows voltages of up to −17V on any input. Since there is essentially no current without the diode, both the high power dissipation and latch up problems are eliminated.

To demonstrate the above characteristics, *Figures 1, 2, and 3* show typical TTL compatible PMOS circuits driving standard CMOS with two clamp diodes, TTL compatible PMOS driving MM74C903/MM74C904, and the TTL compatible PMOS to CMOS system interface, respectively.



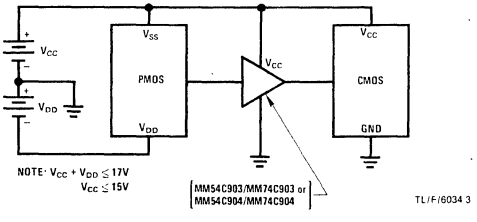
TL/F/6034-1

FIGURE 1



TL/F/6034-2

FIGURE 2



TL/F/6034 3

FIGURE 3. PMOS to CMOS or TTL Interface

CMOS TO CMOS OR TTL INTERFACE

When a CMOS system which is operating at V_{CC} = 10V must provide signals to a CMOS system whose V_{CC} = 5V, a problem similar to that found in PMOS-to-CMOS interface occurs. That is, current would flow through the upper input diode of the device operating at the lower V_{CC}. This current could be in excess of 10 mA on a typical 74C device, as shown in *Figure 4.* Again, this will cause increased power as well as possible four layer diode action.

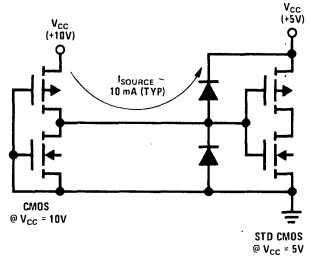
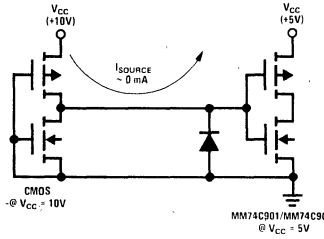


FIGURE 4

TL/F/6034-4



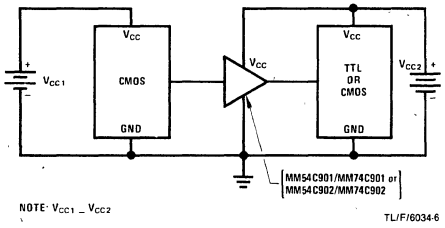
TL/F/6034-5

FIGURE 5

Using the MM74C901 or MM74C902 will eliminate this problem. This occurs simply because these parts are designed with the upper diode removed, as shown in *Figure 5.* With this diode removed the current being sourced goes from about 10 mA to the leakage current of the reverse biased input diode.

Since the MM74C901 and MM74C902 are capable of driving two standard TTL loads with only normal input levels, the output can be used to directly drive TTL. With the example shown, the inputs of the MM74C901 are in excess of 5V. Therefore, they can drive more than two TTL loads. In this case the device would drive four loads with V_{IN} = 10V. If the MM74C902 were used, the output drive would not increase with increased input voltage. This is because the gate of the output n-channel device is always being driven by an internal inverter whose output equals that of V_{CC} of the device.

The example used was for systems of V_{CC} = 10V on one system and V_{CC} = 5V on the second, but the MM74C901 and MM74C902 are capable of using any combination of supplies up to 15V and greater than 3V, as long as V_{CC1} is greater than or equal to V_{CC2} and grounds are common. *Figure 6* diagrams this configuration.



TL/F/6034-6

FIGURE 6. CMOS to TTL or CMOS at a Lower V_{CC}

The inputs on these devices are adequately protected with the single diode, but, as with all MOS devices, normal care in handling should be observed.

Section 3

MM54HC/MM74HC

3

Section Contents

Section Contents (Continued)

Section Contents (Continued)

Section Contents (Continued)

National Semiconductor

microCMOS

MM54HC00/MM74HC00
Quad 2-Input NAND Gate

General Description

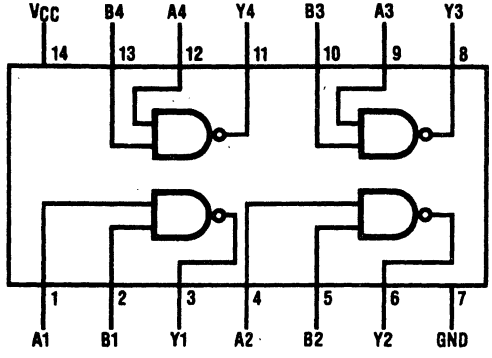
These NAND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

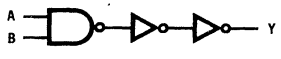


TL/F/5292–1

Top View

Order Number MM54HC00J or MM74HC00J, N

See NS Package J14A or N14A



TL/F/5292–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC02/MM74HC02 Quad 2-Input NOR Gate

General Description

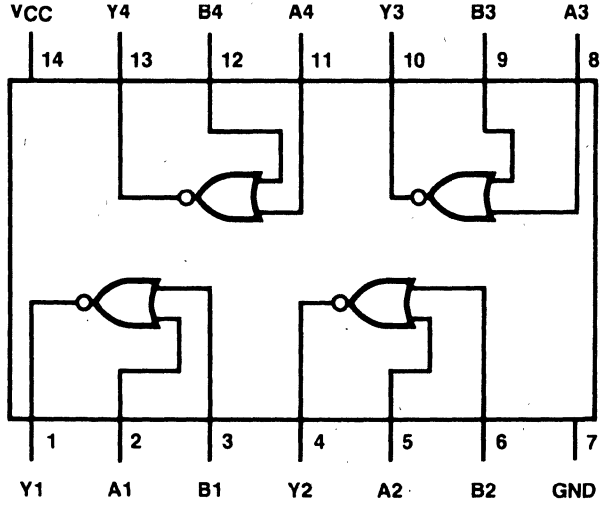
These NOR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent supply current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- High output current: 4 mA minimum

Connection and Logic Diagrams

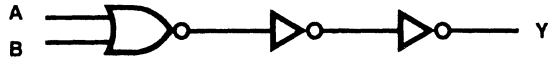
Dual-In-Line Package



TL/F/5294–1

Top View

Order Number MM54HC02J or MM74HC02J, N
See NS Package J14A or N14A



TL/F/5294–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IL}$ $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IL}$ $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC03/MM74HC03 Quad 2-Input Open Drain NAND Gate

General Description

These NAND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

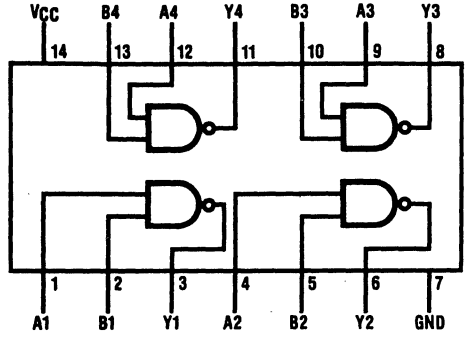
As with standard 54HC/74HC push-pull outputs there are diodes to both V_{CC} and ground. Therefore the output should not be pulled above V_{CC} as it would be clamped to one diode voltage above V_{CC}. This diode is added to enhance electrostatic protection.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

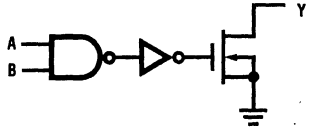
Dual-In-Line Package



TL/F/5295–1

Top View

Order Number MM54HC03J or MM74HC03J,N
See NS Package J14A or N14A



TL/F/5295–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
		R_L=1 kΩ	4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
V_{OL}	Minimum Low Level Output Voltage	V_{IN}=V_{IH}						
		$\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
		R_L=∞	4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH}						
		$\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{LKG}	Maximum High Level Output Leakage Current	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}	6.0V		0.5	5	10	μA
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$R_L=1$ KΩ	10	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C		54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$R_L=1$ KΩ	2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{THL}	Maximum Output Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$. The power dissipated by R_L is not included.

3

National Semiconductor

microCMOS

MM54HC04/MM74HC04 Hex Inverter

General Description

These inverters utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

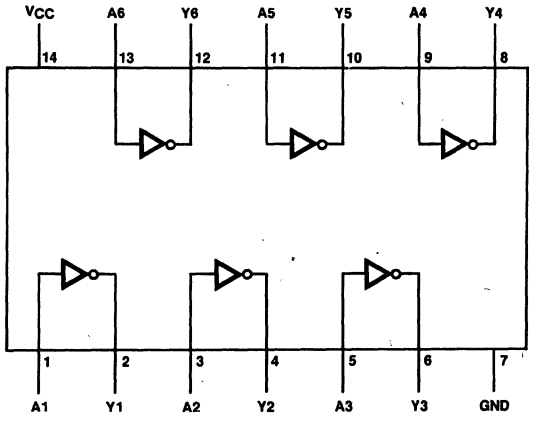
The MM54HC04/MM74HC04 is a triple buffered inverter. It has high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Fan out of 10 LS-TTL loads
- Quiescent power consumption: 10 μW maximum at room temperature
- Typical input current: 10^{-5} μA

Connection and Logic Diagrams

Dual-In-Line Package

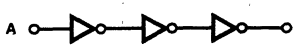


TL/F/5069–1

Top View

Order Number MM54HC04J or MM74HC04J, N
See NS Package J14A or N14A

1 of 6 Inverters



TL/F/5069–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	55	95	120	145	ns
			4.5V	11	19	24	29	ns
			6.0V	9	16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HCU04/MM74HCU04 Hex Inverter

General Description

These inverters utilize microCMOS Technology, 3.5 micro silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits.

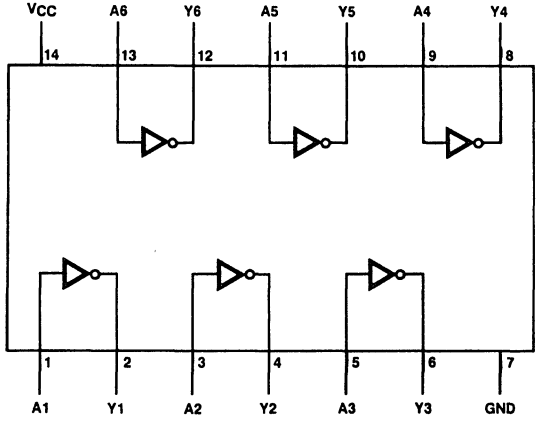
The MM54HCU04/MM74HCU04 is an unbuffered inverter. It has high noise immunity and the ability to drive 15 LS-TTL loads. The 54HCU/74HCU logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns
- Fanout of 15 LS-TTL loads
- Quiescent power consumption: 10 μA maximum at room temperature
- Typical input current: 10^{-5} μA

Connection and Schematic Diagrams

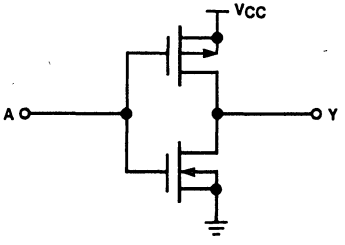
Dual-In-Line Package



TL/F/5296–1

Top View

Order Number MM54HCU04J or MM74HCU04J, N
See NS Package J14A or N14A



TL/F/5296–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCU	−40	+85	°C
MM54HCU	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HCU T_A = −40 to 85°C	54HCU T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.7	1.7	1.7	V
			4.5V		3.6	3.6	3.6	V
			6.0V		4.8	4.8	4.8	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.8	0.8	0.8	V
			6.0V		1.1	1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.8	1.8	1.8	V
			4.5V	4.5	4.0	4.0	4.0	V
			6.0V	6.0	5.5	5.5	5.5	V
		V_{IN} = GND $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.2	0.2	0.2	V
			4.5V	0	0.5	0.5	0.5	V
			6.0V	0	0.5	0.5	0.5	V
		V_{IN} = V_{CC} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

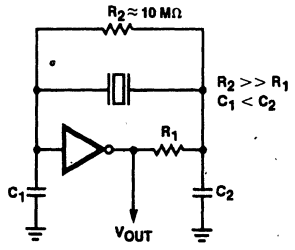
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		7	13	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HCU $T_A=-40$ to $85°C$	54HCU $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	49	82	103	120	ns
			4.5V	9.9	16	21	24	ns
			6.0V	8.4	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		90				pF
C_{IN}	Maximum Input Capacitance			8	15	15	15	pF

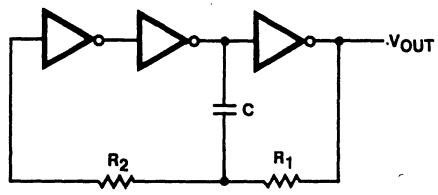
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

Typical Applications



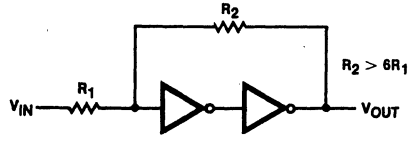
TL/F/5296–3

FIGURE 1. Crystal Oscillator



TL/F/5296–4

FIGURE 2. Stable RC Oscillator



TL/F/5296–5

FIGURE 3. Schmitt Trigger

National Semiconductor

microCMOS

MM54HC08/MM74HC08 Quad 2-Input AND Gate

General Description

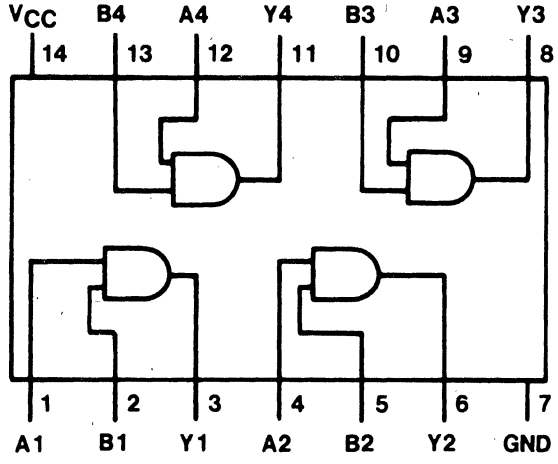
These AND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. The HC08 has buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 7 ns (t_{PHL}), 12 ns (t_{PLH})
- Fanout of 10 LS-TTL loads
- Quiescent power consumption: 2 μA maximum at room temperature
- Typical input current: 10^{-5} μA

Connection Diagram

Dual-In-Line Package



TL/F/5297–1

Top View

Order Number MM54HC08J or MM74HC08J, N
See NS Package J14A or N14A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, Output High to Low		12	20	ns
t_{PLH}	Maximum Propagation Delay, Output Low to High		7	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay, Output High to Low		2.0V	77	121	151	175	ns
			4.5V	15	24	30	35	ns
			6.0V	13	20	25	30	ns
t_{PLH}	Maximum Propagation Delay, Output Low to High		2.0V	30	90	113	134	ns
			4.5V	10	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		38				pF
C_{IN}	Maximum Input Capacitance			4	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC10/MM74HC10
Triple 3-Input NAND Gate

General Description

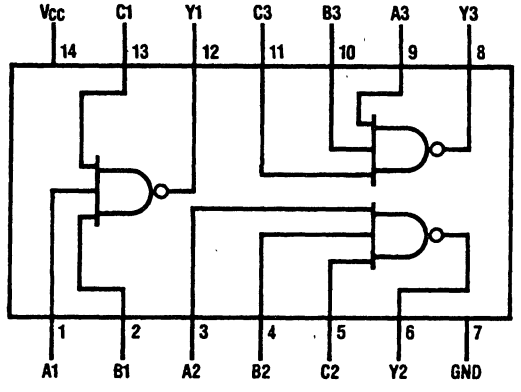
These NAND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

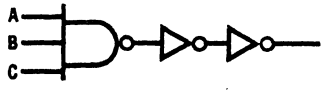
Dual-In-Line Package



TL/F/5153–1

Top View

Order Number MM54HC10J or MM74HC10J,N
See NS Package J14A or N14A



$Y = \overline{ABC}$

TL/F/5153–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	48	90	113	134	ns
			4.5V	10	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC11/MM74HC11 Triple 3-Input AND Gate

General Description

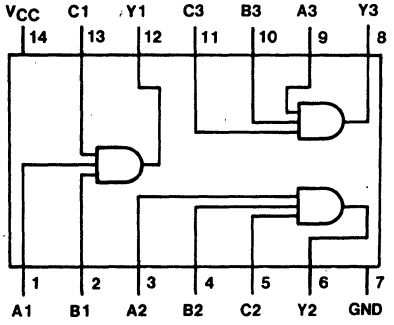
These AND gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

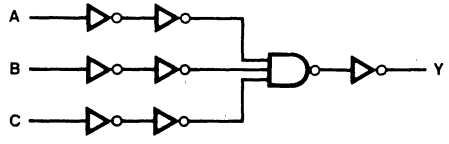
Dual-In-Line Package



TL/F/5298–1

Top View

Order Number MM54HC11J or MM74HC11J, N
See NS Package J14A or N14A



TL/F/5298–2

(1 OF 3 GATES)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	48	125	156	190	ns
			4.5V	18	25	31	38	ns
			6.0V	15	21	27	31	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		35				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC14/MM74HC14
Hex Inverting Schmitt Trigger

General Description

The MM54HC14/MM74HC14 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

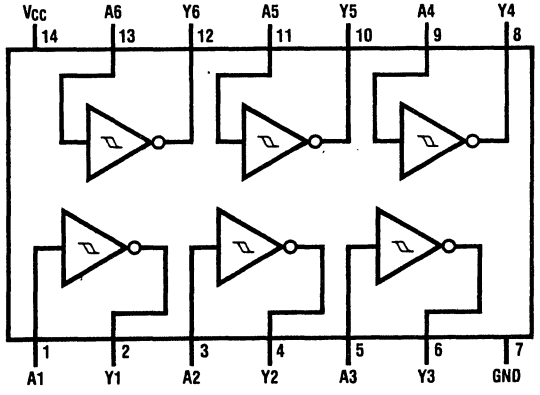
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC}=4.5V

Connection and Schematic Diagrams

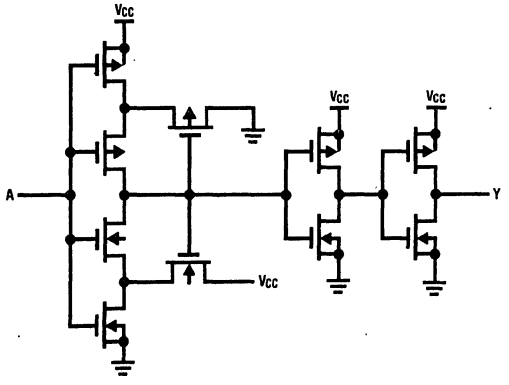
Dual-In-Line Package



TL/F/5105–1

Top View

Order Number MM54HC14J or MM74HC14J,N
See NS Package J14A or N14A



TL/F/5105–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{T+}	Positive Going Threshold Voltage	Minimum	2.0V	1.2	1.0	1.0	1.0	V
			4.5V	2.7	2.3	2.3	2.3	V
			6.0V	3.2	2.7	2.7	2.7	V
		Maximum	2.0V	1.2	1.5	1.5	1.5	V
			4.5V	2.7	3.15	3.15	3.15	V
			6.0V	3.2	4.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage	Minimum	2.0V	0.7	0.3	0.3	0.3	V
			4.5V	1.8	0.9	0.9	0.9	V
			6.0V	2.2	1.2	1.2	1.2	V
		Maximum	2.0V	0.7	1.0	1.0	1.0	V
			4.5V	1.8	2.2	2.2	2.2	V
			6.0V	2.2	2.7	2.7	2.7	V
V_H	Hysteresis Voltage	Minimum	2.0V	0.5	0.2	0.2	0.2	V
			4.5V	0.9	0.4	0.4	0.4	V
			6.0V	1.0	0.6	0.6	0.6	V
		Maximum	2.0V	0.5	1.2	1.2	1.2	V
			4.5V	0.9	2.25	2.25	2.25	V
			6.0V	1.0	3.0	3.0	3.0	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL} $\lvert I_{OUT}\rvert$ = 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IL} $\lvert I_{OUT}\rvert$ = 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$ = 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} $\lvert I_{OUT}\rvert$ = 20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} $\lvert I_{OUT}\rvert$ = 4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$ = 5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	22	ns

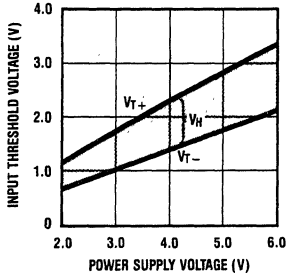
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	11	21	26	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		27				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

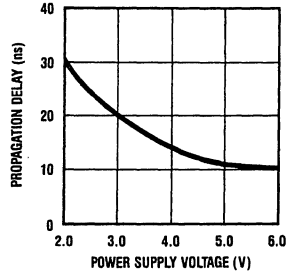
Typical Performance Characteristics

Input Threshold, V_{T+}, V_{T-}, vs Power Supply Voltage



TL/F/5105–3

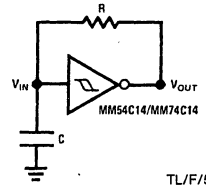
Propagation Delay vs Power Supply



TL/F/5105–4

Typical Applications

Low Power Oscillator



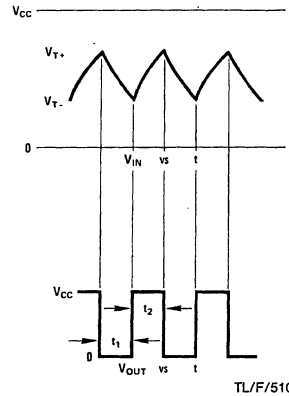
TL/F/5105–5

$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC \ln \frac{V_{CC}-V_{T-}}{V_{CC}-V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC}-V_{T-})}{V_{T-}(V_{CC}-V_{T+})}}$$

Note: The equations assume $t_1 + t_2 \gg t_{pd0} + t_{pd1}$



TL/F/5105–6

National Semiconductor

microCMOS

MM54HC20/MM74HC20 Dual 4-Input NAND Gate

General Description

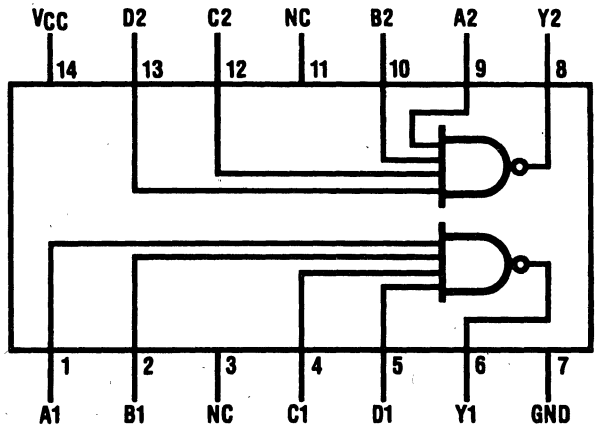
These NAND gates utilize microCMOS Technology, 3.5 micron silicon gate P-Well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

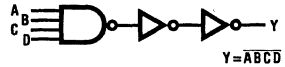
Dual-In-Line Package



TL/F/5299–1

Top View

Order Number MM54HC20J or MM74HC20J, N
See NS Package J14A or N14A



TL/F/5299–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2 f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC27/MM74HC27 Triple 3-Input NOR Gate

General Description

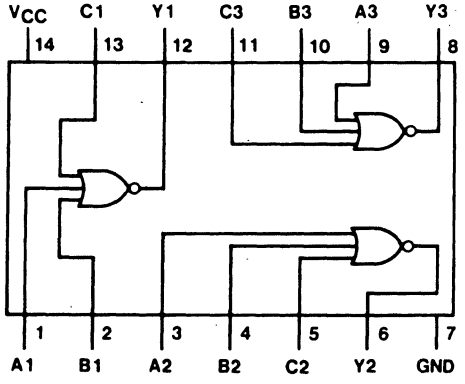
These NOR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide operating supply voltage range: 2–6V
- Low input current: < 1 μA
- Low quiescent supply current: 20 μA maximum (74HC Series)
- Fanout of 10 LS-TTL Loads

Connection and Logic Diagrams

Dual-In-Line Package

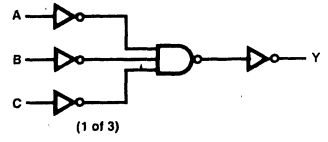


TL/F/5300–1

Top View

Order Number MM54HC27J or MM74HC27J,N
See NS Package J14A or N14A

$$Y = \overline{A + B + C}$$



TL/F/5300–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	90	113	134	ns
			4.5V	9	18	23	27	ns
			6.0V	8	15	19	23	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		36				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC30/MM74HC30 8-Input NAND Gate

General Description

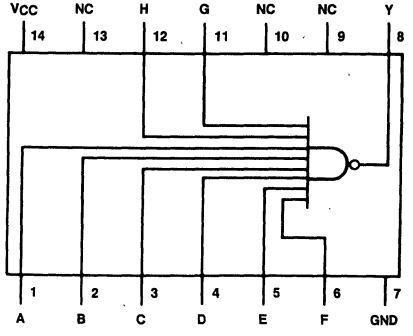
This NAND gate utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. This device has high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

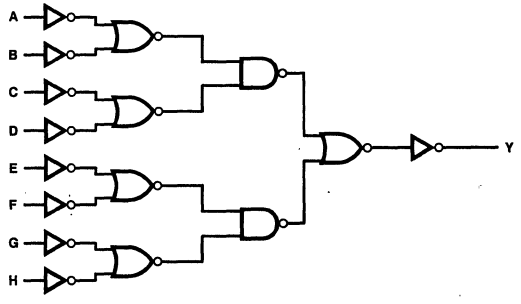
Dual-In-Line Package



TL/F/5133–1

Top View

Order Number MM54HC30J or MM74HC30J, N
See NS Package J14A or N14A



Y = ABCDEFGH

TL/F/5133–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
DC Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} $\|I_{OUT}\|$≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		20	30	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$tns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	66	160	190	220	ns
			4.5V	23	35	42	49	ns
			6.0V	18	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			34				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC32/MM74HC32 Quad 2-Input OR Gate

General Description

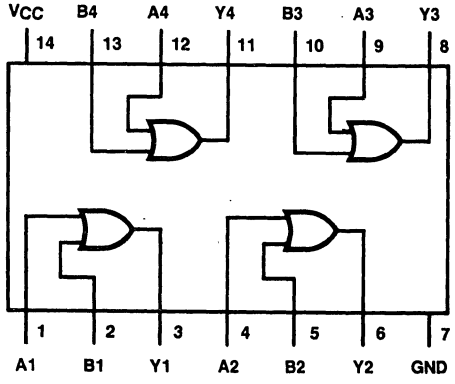
These OR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

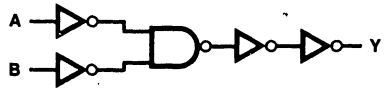
Dual-In-Line Package



TL/F/5132–1

Top View

Order Number MM54HC32J or MM74HC32J,N
See NS Package J14A or N14A



$Y = A + B$

TL/F/5132–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.7	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	30	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	9	17	21	25	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC42/MM74HC42 BCD-to-Decimal Decoder

General Description

This decoder utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Data on the four input pins select one of the 10 outputs corresponding to the value of the BCD number on the inputs. An output will go low when selected, otherwise it remains high. If the input data is not a valid BCD number all outputs will remain high. The circuit has high noise immunity and low power consumption usually associated with CMOS circuitry, yet also has speeds comparable to low power Schottky TTL (LS-TTL) circuits, and is capable of driving 10 LS-TTL equivalent loads.

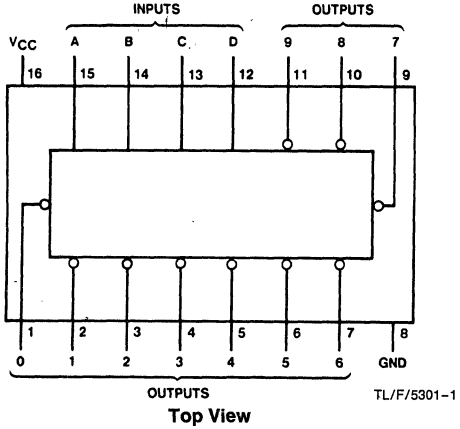
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide supply range: 2V–6V
- Low quiescent current: 80 μA (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-in-line Package



Top View

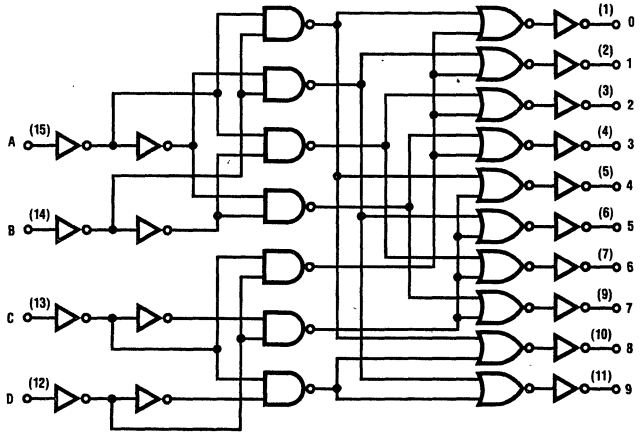
Order Number MM54HC42J or MM74HC42J, N
See NS Package J16A or N16E

Truth Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level

Logic Diagram



TL/F/5301–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Minimum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		15	25	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	75	150	189	224	ns
			4.5V	17	30	38	45	ns
			6.0V	15	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)						pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC51/MM74HC51 Dual AND-OR-Invert Gate MM54HC58/MM74HC58 Dual AND-OR Gate

General Description

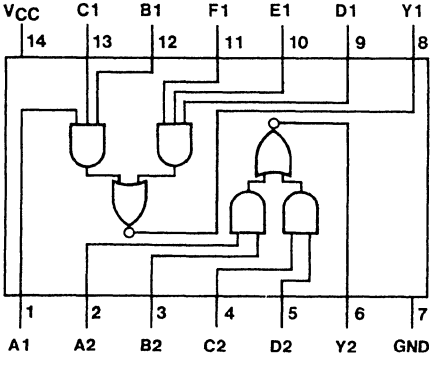
These gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 10 ns
- Wide power supply range: 2–6V
- Low quiescent supply current: 20 μA maximum (74 Series)
- Low input current: 1 μA maximum
- High output current: 4 mA minimum

Connection Diagrams

Dual-In-Line Package

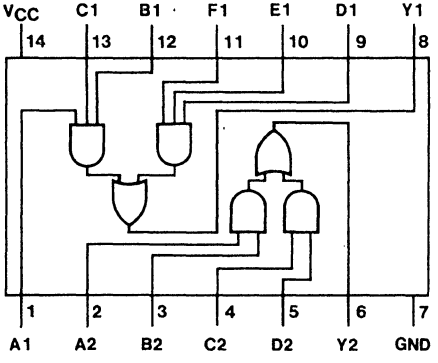


TL/F/5302–1

Top View

Order Number MM54HC51J or MM74HC51J, N
See NS Packages J14A or N14A

Dual-In-Line Package



TL/F/5302–2

Top View

Order Number MM54HC58J or MM74HC58J, N
See NS Packages J14A or N14A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		10	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per AND-OR-Gate)		20				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC73/MM74HC73
Dual J-K Flip-Flops with Clear

General Description

These J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent, J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family.

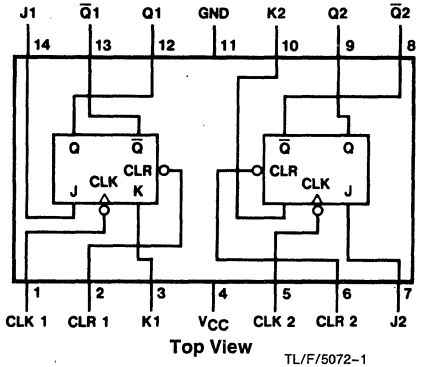
All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC Series)
- High output drive: 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



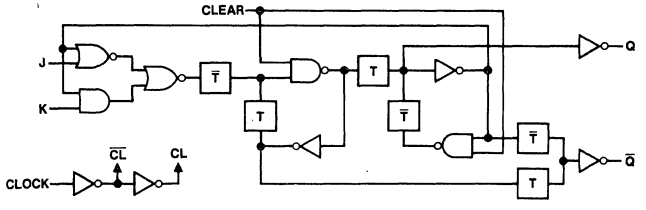
Top View

TL/F/5072–1

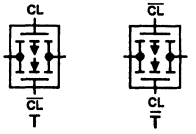
Order Number MM54HC73J or MM74HC73J, N
See NS Package J14A or N14A

Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0



TL/F/5072–2



TL/F/5072–3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage		0	V_{CC}	V
(V_{IN}, V_{OUT})				
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Setup Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K to Clock		−3	0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

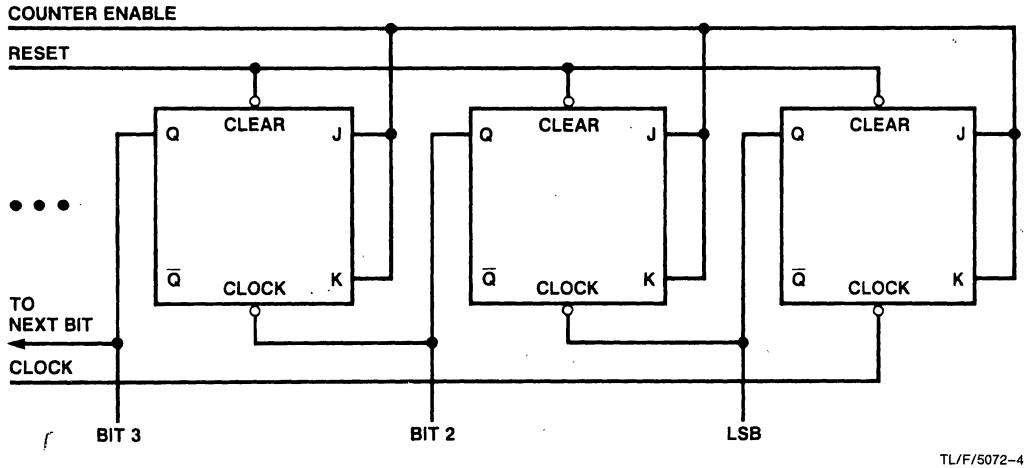
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	70	126	160	185	ns
			4.5V	18	25	32	37	ns
			6.0V	15	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V	126	155	194	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	32	40	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15.4	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

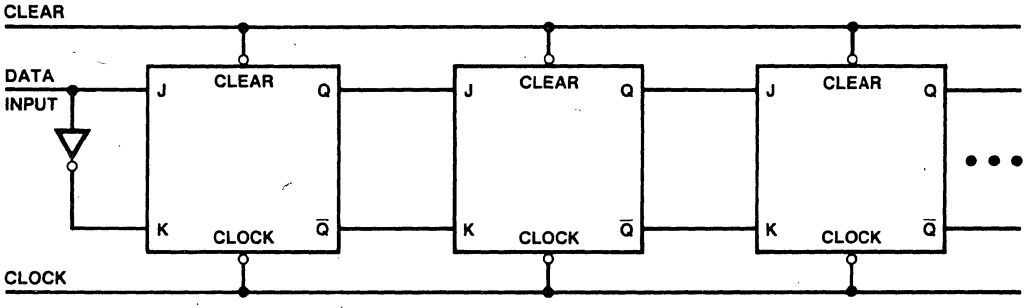
Typical Applications

N Bit Binary Ripple Counter with Enable and Reset



TL/F/5072–4

N Bit Shift Register with Clear



TL/F/5072–5

National Semiconductor

microCMOS

MM54HC74/MM74HC74
Dual D Flip-Flop with Preset and Clear

General Description

The MM54HC74/MM74HC74 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

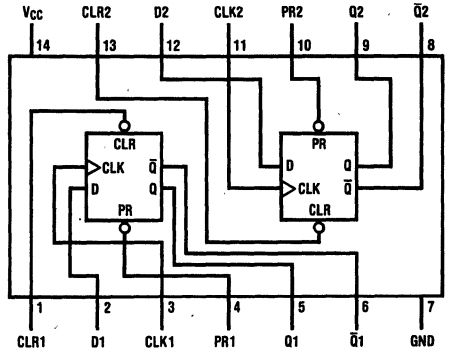
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 40 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



TOP VIEW TL/F/5106–1

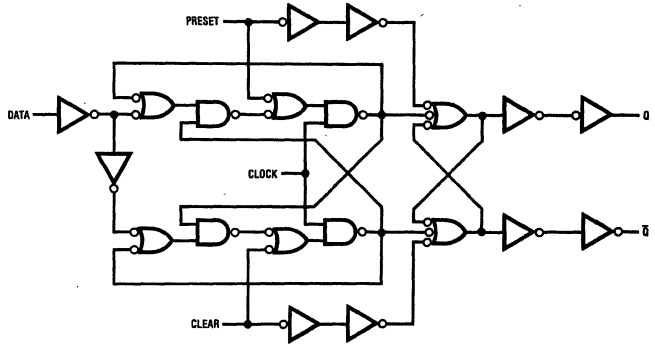
Order Number MM54HC74J or MM74HC74J, N
See NS Package J14A or N14A

Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



TL/F/5106–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.3	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear to Q or $\overline{Q}$		25	40	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			5	ns
t_S	Minimum Setup Time Data to Clock			20	ns
t_H	Minimum Hold Time Clock to Data			0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	4	MHz
			4.5V		27	21	18	MHz
			6.0V		32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	88	175	221	261	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset or Clear To Q or $\overline{Q}$		2.0V	98	230	290	343	ns
			4.5V	30	46	58	69	ns
			6.0V	28	39	49	58	ns
t_{REM}	Minimum Removal Time Preset or Clear To Clock		2.0V		25	32	37	ns
			4.5V		5	6	7	ns
			6.0V		4	5	6	ns
t_S	Minimum Setup Time Data to Clock		2.0V		100	126	149	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum, Pulse Width Clock, Preset or Clear		2.0V	30	80	101	119	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC75/MM74HC75
4-Bit Bistable Latch with Q and $\overline{Q}$ Output

General Description

This 4-bit latch utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. To achieve the high noise immunity and low power consumption normally associated with standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

This latch is ideally suited for use as temporary storage for binary information processing, input/output, and indicator units. Information present at the data (D) input is transferred to the Q output when the enable (G) is high. The Q output will follow the data input as long as the enable remains high. When the enable goes low, the information that was present at the data input at the time the transition occurred is retained at the Q output until the enable is permitted to go high again.

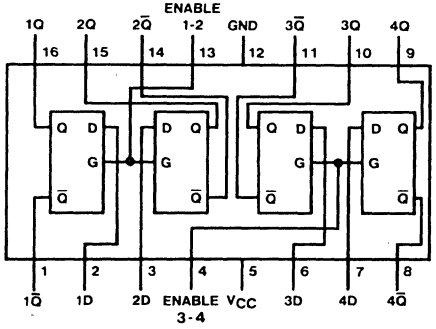
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 12 ns
- Wide operating supply voltage range: 2–6V
- Low input current: < 1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



TOP VIEW

TL/F/5303–1

Order Number MM54HC75J or MM74HC75J, N
See NS Package J16A or N16E

Truth Table

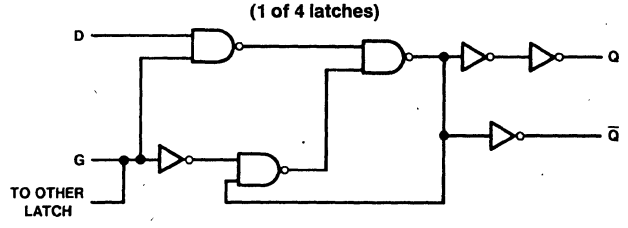
Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level; L = Low Level

X = Don't Care

Q_0 = The level of Q before the transition of G

(1 of 4 latches)



TL/F/5303–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q		14	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$		10	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Q		16	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$		11	23	ns
t_S	Minimum Set Up Time			20	ns
t_H	Minimum Hold Time		−2	0	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q		2.0V	37	125	156	188	ns
			4.5V	15	25	32	38	ns
			6.0V	14	24	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$		2.0V	29	110	138	165	ns
			4.5V	12	22	28	33	ns
			6.0V	11	19	24	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Q		2.0V	40	145	181	218	ns
			4.5V	18	29	36	44	ns
			6.0V	16	25	31	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$		2.0V	36	125	156	188	ns
			4.5V	15	25	31	38	ns
			6.0V	14	22	28	33	ns
t_S	Minimum Set Up Time Data to Enable		2.0V	40	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	25	ns
t_H	Minimum Hold Time Enable to Data		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_W	Minimum Enable Pulse Width		2.0V	40	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per commonly clocked latched pair)		40				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC76/MM74HC76 Dual J-K Flip-Flops with Preset and Clear

General Description

These high speed (30 MHz minimum) J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon P-well CMOS, to achieve, the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

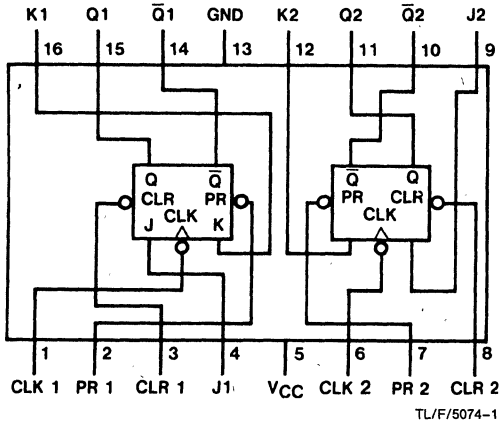
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HC Series)
- High output drive: 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5074–1

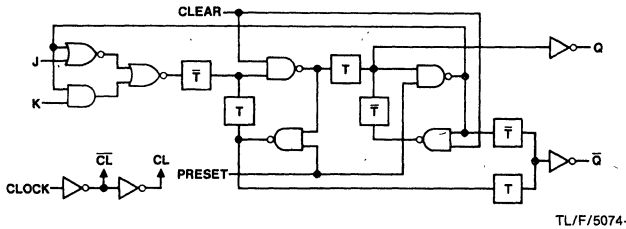
Top View

Order Number MM54HC76J or MM74HC76J, N
See NS Package J16A or N16E

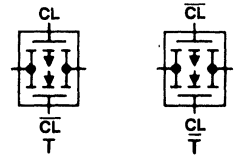
Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed



TL/F/5074–2



TL/F/5074–3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		4	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time		10	20	ns
t_S	Minimum Setup Time J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K to Clock		−3	0	ns
t_W	Minimum Pulse Width Preset, Clear or Clock		10	16	ns

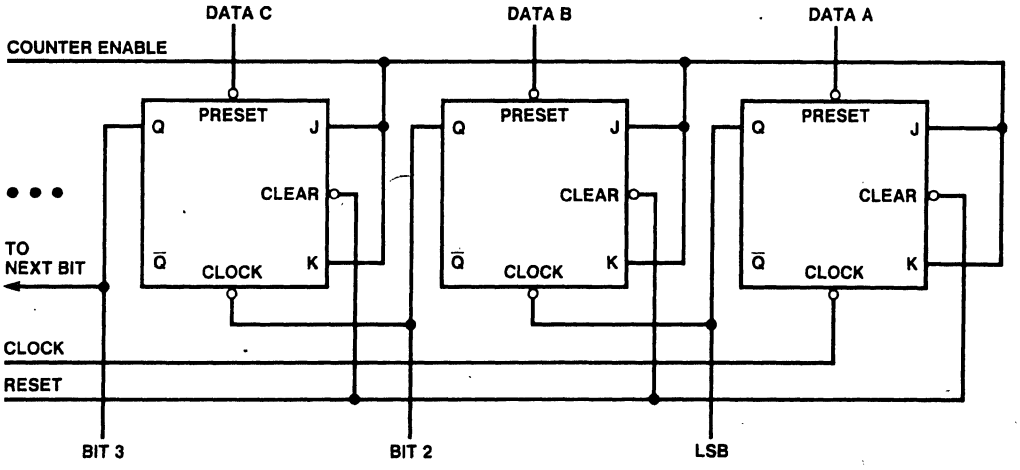
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	100	126	160	183	ns
			4.5V	20	25	31	37	ns
			6.0V	17	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V	126	155	191	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	33	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V	137	165	210	240	ns
			4.5V	27	33	41	50	ns
			6.0V	23	28	35	40	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum, Pulse Width, Preset, Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

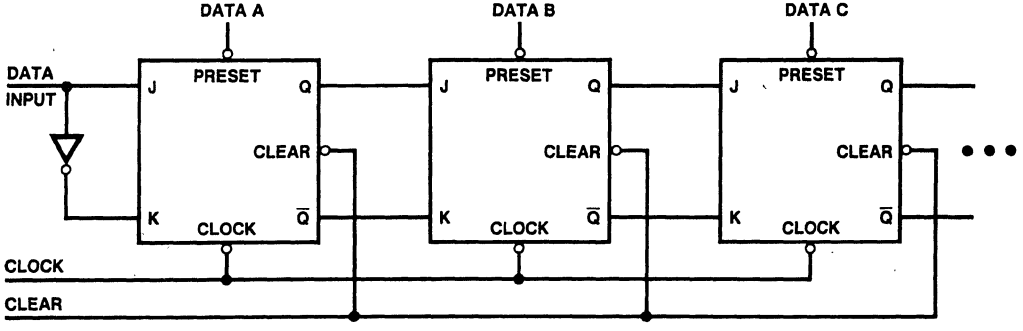
Typical Applications

N Bit Presettable Ripple Counter with Enable and Reset



TL/F/5074–4

N Bit Parallel Load/Serial Load Shift Register with Clear



TL/F/5074–5

National Semiconductor

MM54HC85/MM74HC85
4-Bit Magnitude Comparator

microCMOS

General Description

The MM54HC85/MM74HC85 is a 4-bit magnitude comparator that utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It is designed for high speed comparison of two four bit words. This circuit has eight comparison inputs, 4 for each word; three cascade inputs (A<B, A>B, A=B); and three decision outputs (A<B, A>B, A=B). The result of a comparison is indicated by a high level on one of the decision outputs. Thus it may be determined whether one word is "greater than," "less than," or "equal to" the other word. By connecting the outputs of the least significant stage to the cascade inputs of the next stage, words of greater than four bits can be compared. In addition the least significant stage must have a high level applied to the A=B input, and a low level to the A<B, and A>B inputs.

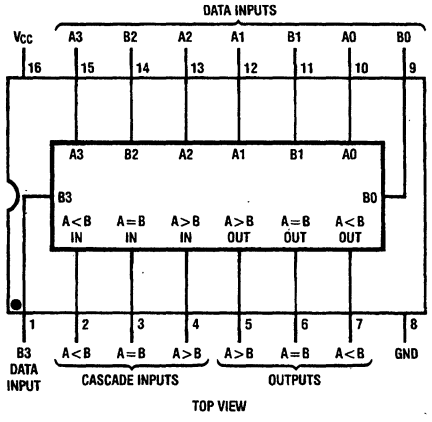
The comparator's outputs can drive 10 low power Schottky TTL (LS-TTL) equivalent loads, and is functionally, and pin equivalent to the 54LS85/74LS85. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 27 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5205–1

Order Number MM54HC85J or MM74HC85J, N
See NS Package J16A or N16E

Truth Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V	1.5	1.5	1.5	V
			4.5V	3.15	3.15	3.15	V
			6.0V	4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V	0.3	0.3	0.3	V
			4.5V	0.9	0.9	0.9	V
			6.0V	1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A<B or A>B		20	36	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A=B Input to A=B Output		12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cascade Input to Output		13	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A=B		20	30	ns

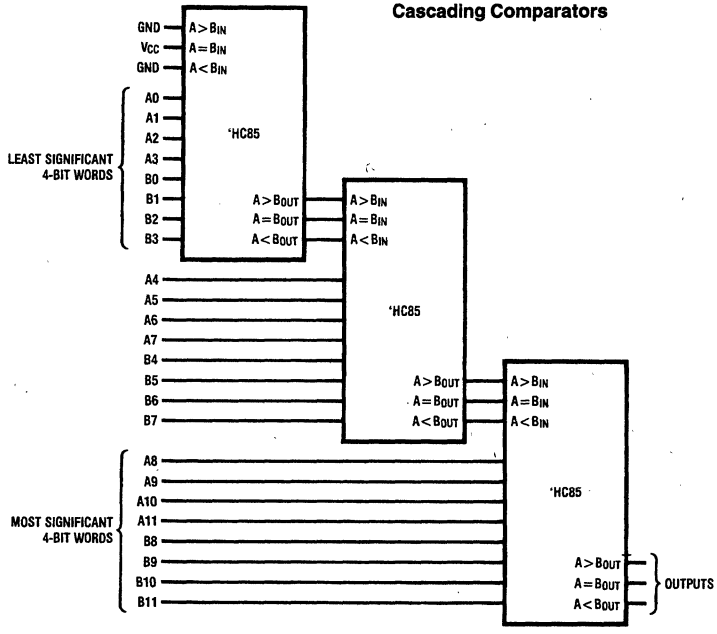
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to Output		2.0V	100	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data Input to A=B Output		2.0V	88	175	221	261	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A=B Input to A=B Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cascade Input to Output (except A=B)		2.0V	70	155	195	231	ns
			4.5V	16	31	39	46	ns
			6.0V	13	26	33	39	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

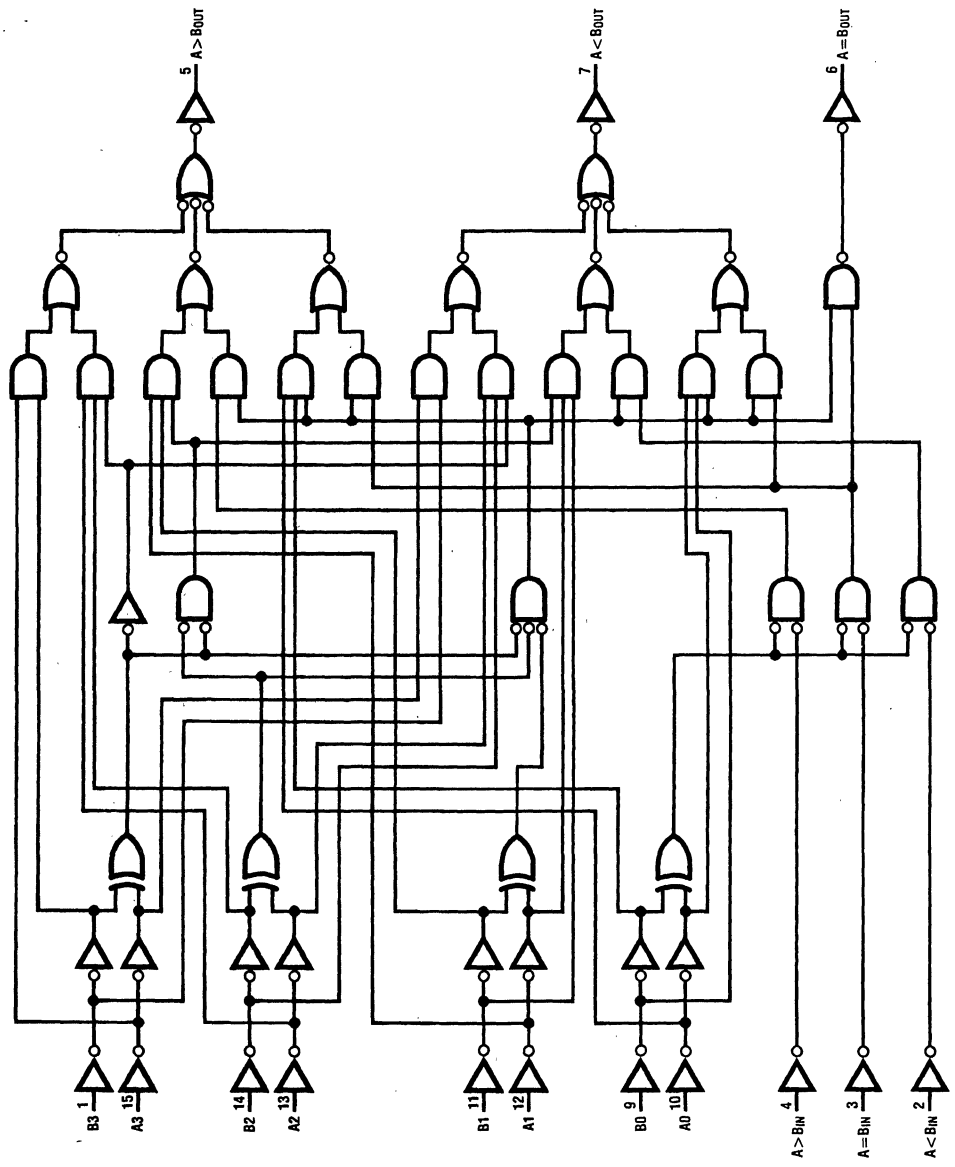
Typical Application

Cascading Comparators



TL/F/5205–4

Logic Diagram



National Semiconductor

microCMOS

MM54HC86/MM74HC86 Quad 2-Input Exclusive OR Gate

General Description

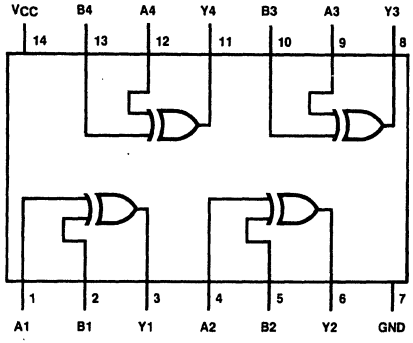
This EXCLUSIVE OR gate utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The MM54HC/74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 9 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 20 μA maximum (74 Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5305–1

Top View

Order Number MM54HC86J or MM74HC86J, N

See NS Package J14A or N14A

Truth Table

Inputs		Outputs
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

$Y = A \oplus B = \overline{A}B + A\overline{B}$

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC107/MM74HC107 Dual J-K Flip-Flops with Clear

General Description

These J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and CLEAR inputs and Q and $\overline{Q}$ outputs. CLEAR is independent of the clock and accomplished by a low level on the input.

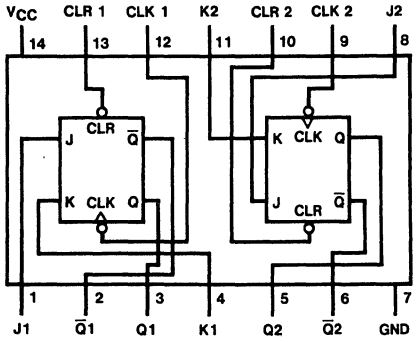
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC series)
- High output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



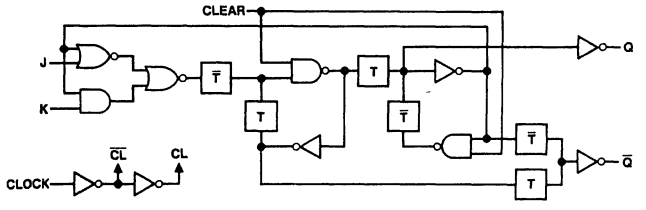
TL/F/5304–1

Order Number MM54HC107J or MM74HC107J, N
See NS Package J14A or N14A

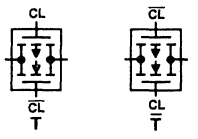
Truth Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

Logic Diagram



TL/F/5304–2



TL/F/5304–3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		21	26	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Setup Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

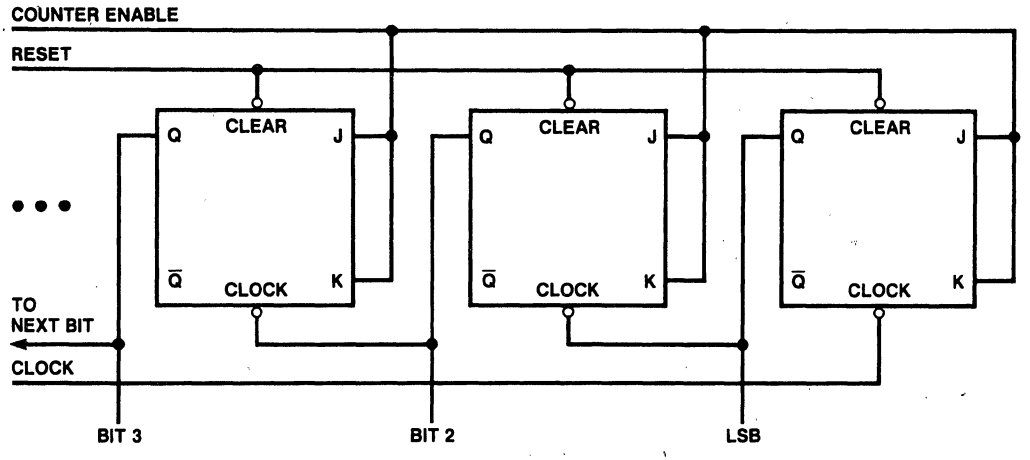
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	70	126	160	185	ns
			4.5V	18	25	32	37	ns
			6.0V	16	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clear to Q or $\overline{Q}$		2.0V	126	155	194	250	ns
			4.5V	25	31	39	47	ns
			6.0V	21	26	32	40	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K to Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	10	14	18	21	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

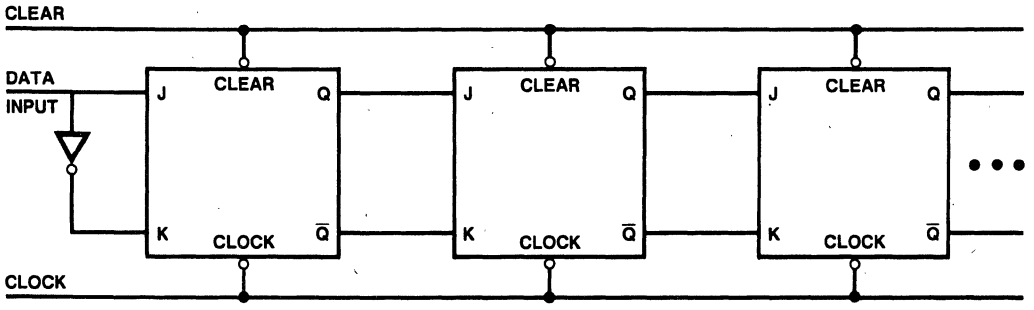
Typical Applications

N Bit Binary Ripple Counter with Enable and Reset



TL/F/5304–4

N Bit Shift Register with Clear



TL/F/5304–5

National Semiconductor

microCMOS

MM54HC109/MM74HC109
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear

General Description

These J-$\overline{K}$ FLIP-FLOPS utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip flop has independent J, $\overline{K}$ PRESET, CLEAR and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

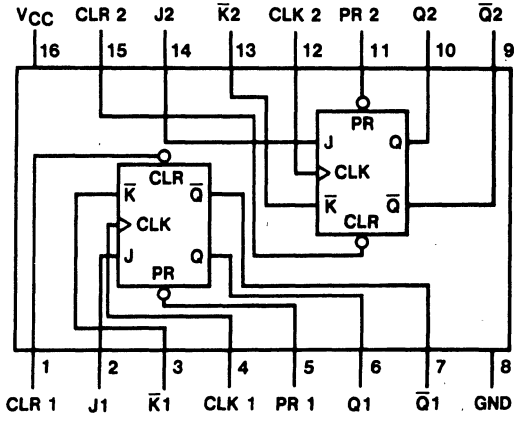
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5306–1

Top View

Order Number MM54HC109J or MM74HC109J, N
See NS Package J16A or N16E

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$		21	42	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			5	ns
t_S	Minimum Setup Time, J or $\overline{K}$ to Clock			20	ns
t_H	Minimum Hold Time, J or $\overline{K}$ to Clock			0	ns
t_W	Minimum Pulse Width: Preset, Clear or Clock		9	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 31	4 21 24	4 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	88 18 15	175 35 30	221 44 37	261 52 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset or Clear to Q or $\overline{Q}$		2.0V 4.5V 6.0V	115 23 20	230 46 39	290 58 49	343 69 58	ns ns ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V 4.5V 6.0V		25 5 4	32 6 5	37 7 6	ns ns ns
t_S	Minimum Setup Time J or $\overline{K}$ to Clock		2.0V 4.5V 6.0V		100 20 17	126 25 21	119 30 20	ns ns ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Clock, Preset or Clear		2.0V 4.5V 6.0V	30 9 8	80 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V 4.5V 6.0V	25 7 6	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC112/MM74HC112
Dual J-K Flip-Flops with Preset and Clear

General Description

These high speed (30 MHz minimum) J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip-flop has independent J, K, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

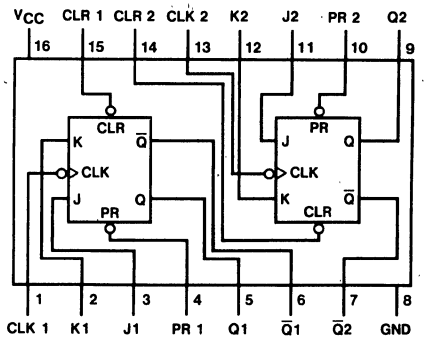
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC Series)
- High output drive: 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5307–1

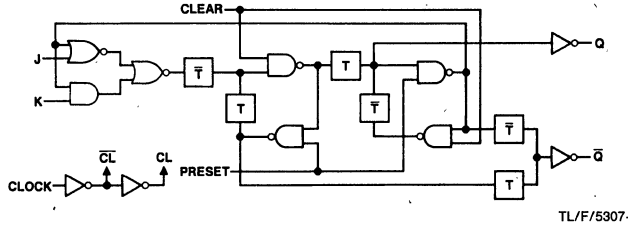
Top View

Order Number MM54HC112J or MM74HC112J, N
See NS Package J16A or N16E

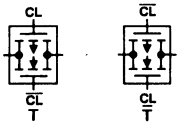
Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	L	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	L*	L*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q0	$\overline{Q}$0

*This is an unstable condition, and is not guaranteed



TL/F/5307–2



TL/F/5307–3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Q or $\overline{Q}$		21	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock		10	20	ns
t_S	Minimum Setup Time J or K to Clock		14	20	ns
t_H	Minimum Hold Time J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width Clock Preset or Clear		10	16	ns

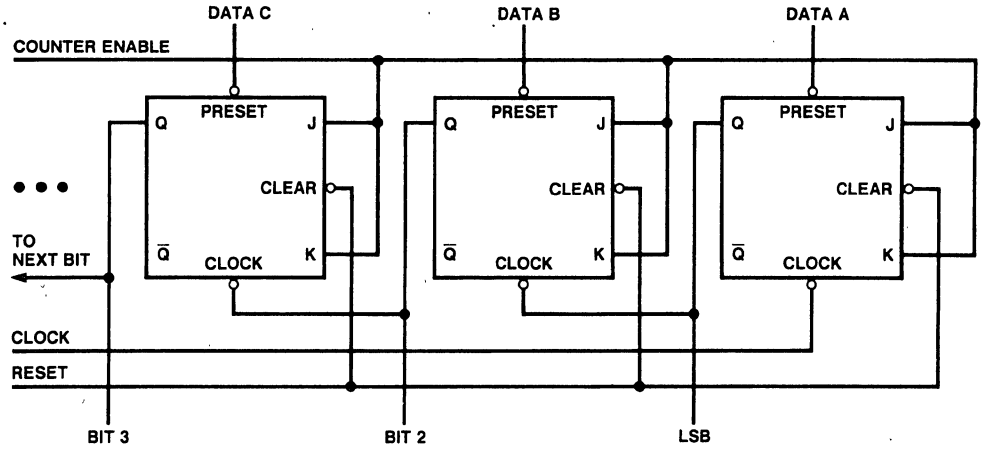
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	9 45 53	5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V 4.5V 6.0V	100 20 17	126 25 21	160 32 27	183 37 32	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Q or $\overline{Q}$		2.0V 4.5V 6.0V	126 25 21	155 31 26	191 39 33	250 47 40	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V 4.5V 6.0V	137 27 23	165 33 28	210 41 35	240 50 40	ns ns ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock		2.0V 4.5V 6.0V	55 11 9.4	100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Setup Time J or K to Clock		2.0V 4.5V 6.0V	77 15 13	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time J or K from Clock		2.0V 4.5V 6.0V	−3 −3 −3	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width Preset, Clear or Clock		2.0V 4.5V 6.0V	55 11 9	80 16 14	100 20 18	120 24 20	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

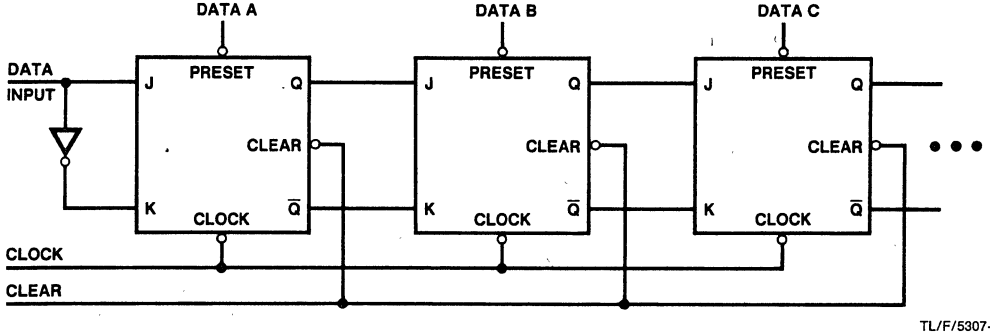
Typical Applications

N Bit Presettable Ripple Counter with Enable and Reset



TL/F/5307–4

N Bit Parallel Load/Serial Load Shift Register with Clear



TL/F/5307–5

National Semiconductor

microCMOS

MM54HC113/MM74HC113 Dual J-K Flip-Flops with Preset

General Description

These high speed J-K Flip-Flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power dissipation of standard CMOS integrated circuits. These devices can drive 10 LS-TTL loads.

These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulse. Each one has independent J, K, CLOCK, and PRESET inputs and Q and $\overline{Q}$ inputs. PRESET is independent of the clock and accomplished by a low level on the input.

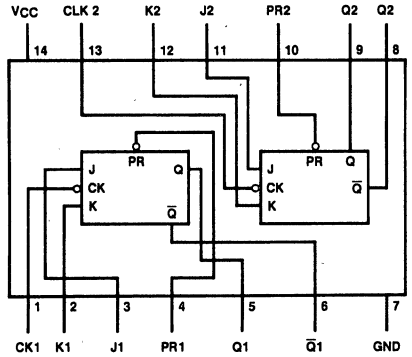
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA (74HC Series)
- High output drive: 10 LS-TTL loads

Connection Diagram and Truth Table

Dual-In-Line Package



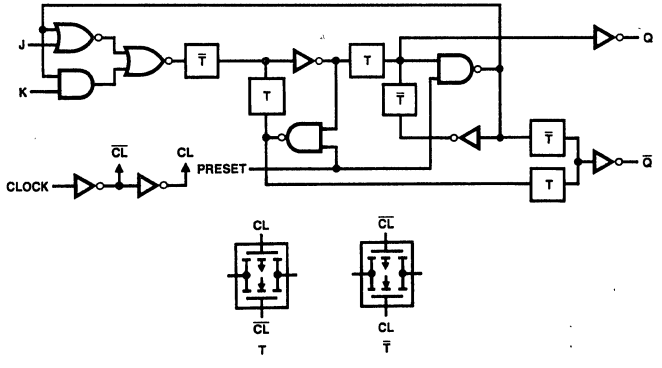
TL/F/5073–1

Top View

Order Number MM54HC113J or MM74HC113J, N
See NS Package J14A or N14A

Inputs				Outputs	
PR	CLK	J	K	O	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q0	$\overline{Q}$0
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	
H	H	X	X	Q0	$\overline{Q}$0

Logic Diagram



TL/F/5073–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		4.0	40	80	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		16	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		23	28	ns
t_{REM}	Minimum Removal Time, Preset to Clock		10	20	ns
t_s	Minimum Setup Time, J or K to Clock		14	20	ns
t_H	Minimum Hold Time, J or K from Clock		−3	0	ns
t_W	Minimum Pulse Width, Preset, Clear or Clock		10	16	ns

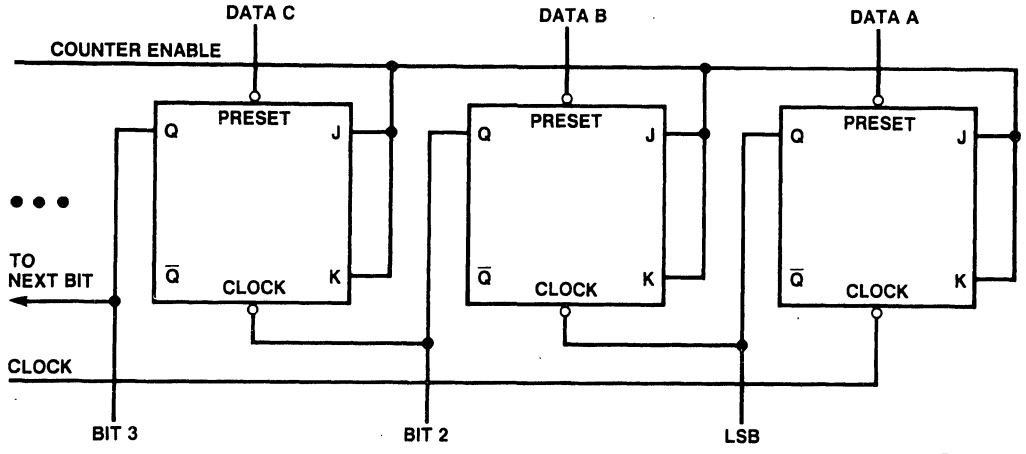
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	9	5	4	3	MHz
			4.5V	45	27	21	18	MHz
			6.0V	53	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	100	125	160	183	ns
			4.5V	20	25	32	37	ns
			6.0V	17	33	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Preset to Q or $\overline{Q}$		2.0V	137	165	206	239	ns
			4.5V	27	33	41	47	ns
			6.0V	23	28	35	40	ns
t_{REM}	Minimum Removal Time Preset to Clock		2.0V	55	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_s	Minimum Setup Time J or K to Clock		2.0V	77	100	125	150	ns
			4.5V	15	20	25	30	ns
			6.0V	13	17	21	25	ns
t_H	Minimum Hold Time J or K from Clock		2.0V	−3	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width, Preset, Clear or Clock		2.0V	55	80	100	120	ns
			4.5V	11	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

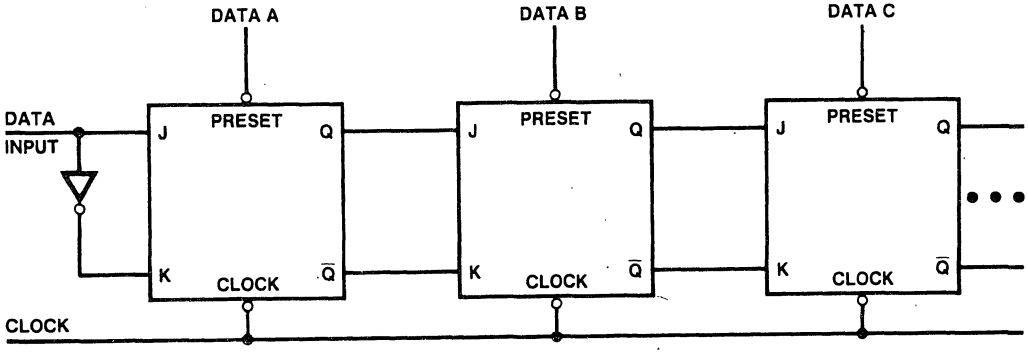
Typical Applications

N Bit Presettable Binary Ripple Counter with Enable



TL/F/5073–3

N Bit Parallel Load/Serial Load Shift Register



TL/F/5073–4

National Semiconductor

microCMOS

MM54HC123A/MM74HC123A
Dual Retriggerable Monostable Multivibrator

General Description

The MM54/74HC123A high speed monostable multivibrators (one shots) utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC123 can be triggered on the positive transition of the clear while A is held low and B is held high.

The 'HC123A is retriggerable. That is it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

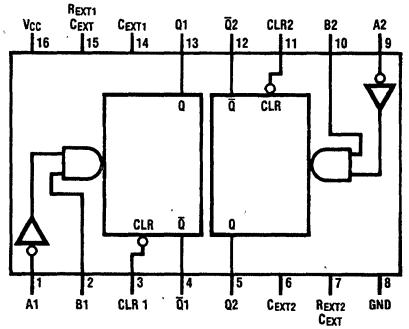
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})(C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs enable infinite signal input rise and fall times.

Connection Diagram

Dual-In-Line Package



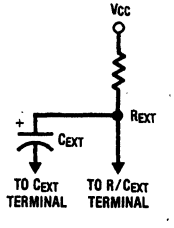
Top View

TL/F/5206–1

Order Number MM54HC123AJ or MM74HC123AJ, N

See NS Package J16A or N16E

Timing Component



TL/F/5206–2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎴
H	↓	H	⎍	⎴
↑	L	H	⎍	⎴

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎴ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (Clear Input)			
(t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤ 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤ 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN}=V_{CC} or GND	6.0V		±0.5	±5.0	±5.0	μA
I_{IN}	Maximum Input Current (all other pins)	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (standby)	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable)	V_{IN}=V_{CC} or GND R/C_{EXT}=0.5V_{CC}	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating:

Plastic "N" Package: −12mW/°C from 65°C to 85°C

Ceramic "J" Package: −12mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

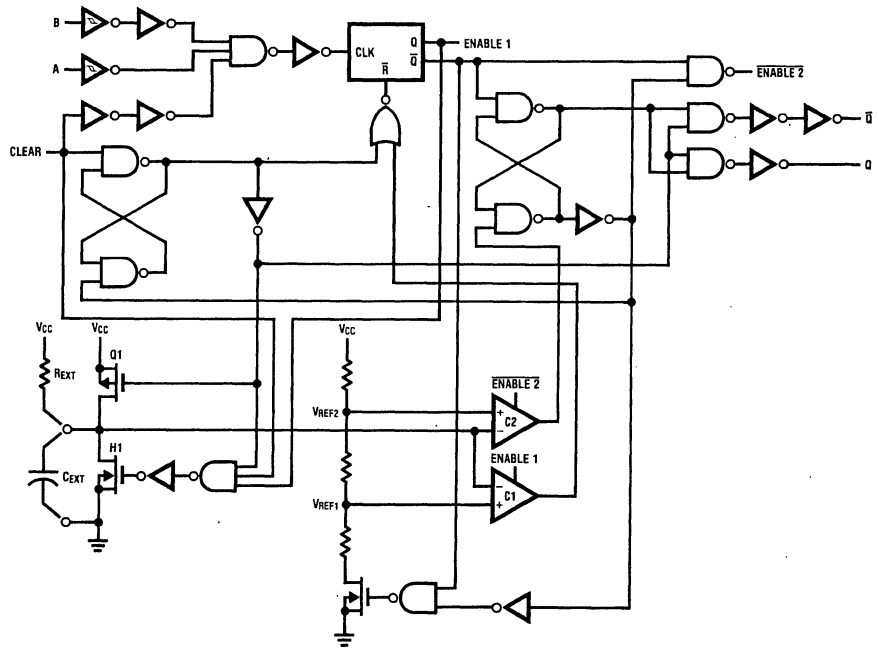
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		22	33	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns (unless otherwise specified)

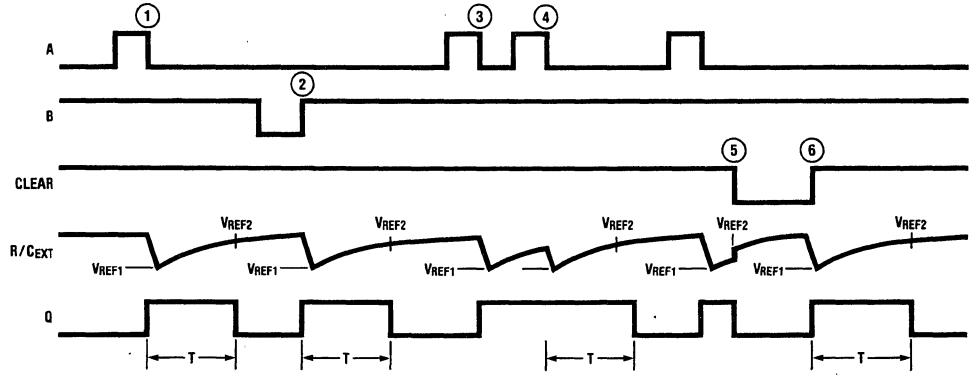
Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ	Guaranteed Limits		
t_{PLH}	Maximum Trigger Propagation Delay, A, B or Clear to Q			2.0V	77	169	194	210	ns
				4.5V	26	42	51	57	ns
				6.0V	21	32	39	44	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B or Clear to $\overline{Q}$			2.0V	88	197	229	250	ns
				4.5V	29	48	60	67	ns
				6.0V	24	38	46	51	ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V	54	114	132	143	ns
				4.5V	23	34	41	45	ns
				6.0V	19	28	33	36	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V	56	116	135	147	ns
				4.5V	25	36	42	46	ns
				6.0V	20	29	34	37	ns
t_W	Minimum Pulse Width A, B, Clear			2.0V	57	123	144	157	ns
				4.5V	17	30	37	42	ns
				6.0V	12	21	27	30	ns
t_{REM}	Minimum Clear Removal Time			2.0V		0	0	0	ns
				4.5V		0	0	0	ns
				6.0V		0	0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF		2.0V	1.5				μs
		$R_{EXT}=2$ kΩ		4.5V	450				ns
		$R_{EXT}=6$ kΩ ($V_{CC}=2V$)		6.0V	380				ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	4.5V	1	0.9			ms
			Max	4.5V	1	1.1			ms
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (other inputs)				6	10	10	10	pF

Logic Diagram



TL/F/5206–5

Theory of Operation



TL/F/5206–6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
⑤ RESET PULSE SHORTENING
⑥ CLEAR TRIGGER

FIGURE 1

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the one shot is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC} ②). The 'HC123A can also be triggered when clear goes from GND to V_{CC} (while A is at GND and B is at V_{CC} ⑥).

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC123A is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

RETRIGGER OPERATION

The 'HC123A is retriggered if a valid trigger occurs ③ followed by another trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin or has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC}. The Q output will remain high until time T, after the last valid retrigger.

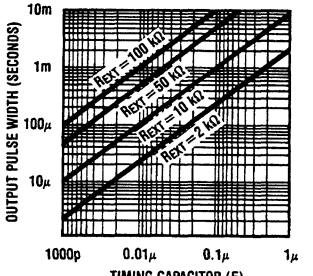
Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit, the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

$$t_{rr} \approx 20 + \frac{187}{V_{CC} - 0.7} + \frac{565 + (0.256\ V_{CC})C_X}{[V_{CC} - 0.7]^2}$$

RESET OPERATION

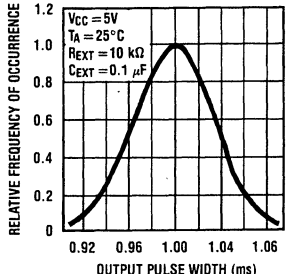
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



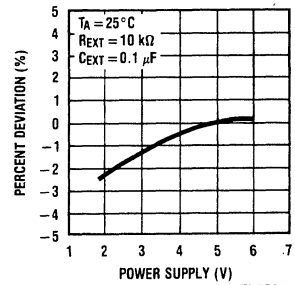
TL/F/5206–7

Typical Distribution of Output Pulse Width, Part to Part



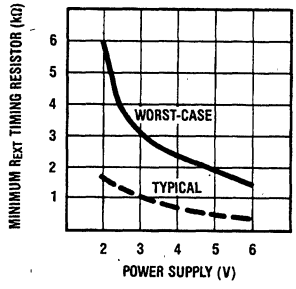
TL/F/5206–8

Typical 1ms Pulse Width Variation vs. Supply



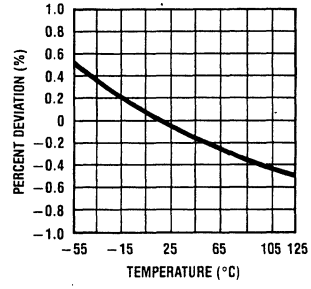
TL/F/5206–9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5206–10

Typical 1ms Pulse Width Variation vs. Temperature



TL/F/5206–11

Note: R and C are not subjected to temperature. The C is polypropylene.

National Semiconductor

microCMOS

MM54HC125/MM74HC125
MM54HC126/MM74HC126
TRI-STATE® Quad Buffers

General Description

These are general purpose TRI-STATE high speed non-inverting buffers utilizing microCMOS technology, 3.5 micron silicon gate P-well CMOS. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. Both circuits are capable of driving up to 15 low power Schottky inputs.

The MM54HC125/MM74HC125 require the TRI-STATE control input C to be taken high to put the output into the high impedance condition, whereas the MM54HC126/MM74HC126 require the control input to be low to put the output into high impedance.

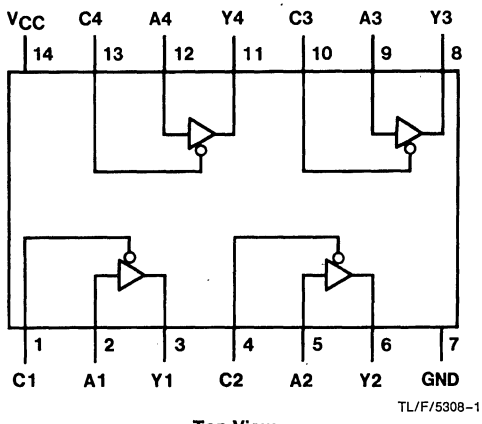
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC)
- Fanout of 15 LS-TTL loads

Connection Diagrams

Dual-In-Line Package

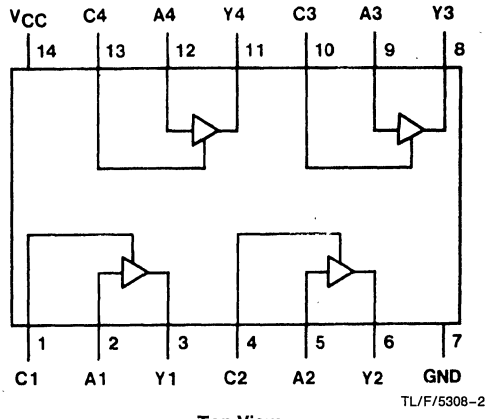


TL/F/5308–1

Top View

Order Number MM54HC125J or MM74HC125J, N
See NS Package J14A or N14A

Dual-In-Line Package



TL/F/5308–2

Top View

Order Number MM54HC126J or MM74HC126J, N
See NS Package J14A or N14A

Truth Tables

Inputs		Output
A	C	Y
H	L	H
L	L	L
X	H	Z

Inputs		Output
A	C	Y
H	H	H
L	H	L
X	L	Z

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND C_n=Disabled	6.0V		±0.5	±5	±10	μA
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		13	18	ns
t_{PZH}	Maximum Output Enable Time to High Level	$R_L=1$ kΩ	13	25	ns
t_{PHZ}	Maximum Output Disable Time from High Level	$R_L=1$ kΩ $C_L=5$ pF	17	25	ns
t_{PZL}	Maximum Output Enable Time to Low Level	$R_L=1$ kΩ	18	25	ns
t_{PLZ}	Maximum Output Disable Time from Low Level	$R_L=1$ kΩ $C_L=5$ pF	13	25	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	Temperature °C				Units
				54HC/74HC $T_A=25°C$		74HC −40 to 85°C	54HC −55 to 125°C	
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time		2.0V	40	100	125	150	ns
			4.5V	14	20	25	30	ns
			6.0V	12	17	21	25	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	$C_L=150$ pF	2.0V	35	130	163	195	ns
			4.5V	14	26	33	39	ns
			6.0V	12	22	28	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	25	125	156	188	ns
			4.5V	14	25	31	38	ns
			6.0V	12	21	26	31	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$C_L=150$ pF $R_L=1$ kΩ	2.0V	35	140	175	210	ns
			4.5V	15	28	35	42	ns
			6.0V	13	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	30	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{OUT}	Output Capacitance Outputs			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)						
		Enabled		45				pF
		Disabled		6				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC132/MM74HC132 Quad 2-Input NAND Schmitt Trigger

General Description

The MM54HC132/MM74HC132 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

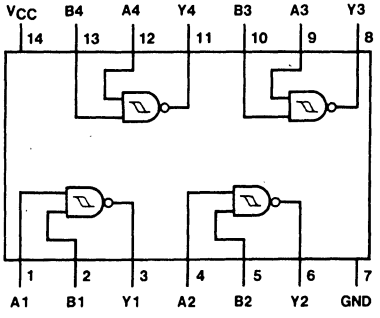
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at $V_{CC}=4.5V$

Connection and Logic Diagrams

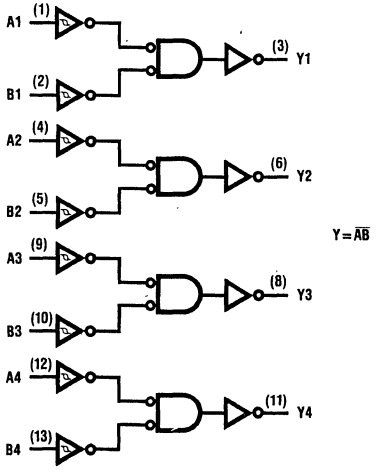
Dual-In-Line Package



TL/F/5309–1

Top View

Order Number MM54HC132J or MM74HC132J,N
See NS Package J14A or N14A



TL/F/5309–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions		V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
					Typ	Guaranteed Limits		
V_{T+}	Positive Going Threshold Voltage		Min	2.0V		1.0	0.95	0.95	V
			Max			1.5	1.5	1.5	V
			Min	4.5V		2.30	2.25	2.25	V
			Max			3.15	3.15	3.15	V
			Min	6.0V		3.0	2.95	2.95	V
			Max			4.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage		Min	2.0V		0.3	0.3	0.3	V
			Max			0.8	0.85	0.85	V
			Min	4.5V		0.9	0.9	0.9	V
			Max			2.0	2.05	2.05	V
			Min	6.0V		1.2	1.2	1.2	V
			Max			2.3	2.35	2.35	V
V_H	Hysteresis Voltage		Min	2.0V		0.2	0.2	0.2	V
			Max	2.0V		1.2	1.2	1.2	V
			Min	4.5V		0.4	0.4	0.4	V
			Max	4.5V		2.25	2.25	2.25	V
			Min	6.0V		0.6	0.6	0.6	V
			Max	6.0V		3.0	3.0	3.0	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$		2.0V	2.0	1.9	1.9	1.9	V
				4.5V	4.5	4.4	4.4	4.4	V
				6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA		4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA		6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$		2.0V	0	0.1	0.1	0.1	V
				4.5V	0	0.1	0.1	0.1	V
				6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA		4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA		6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)						pF
C_{IN}	Maximum Input Capacitance				5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2 f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC133/MM74HC133
13-Input NAND Gate

General Description

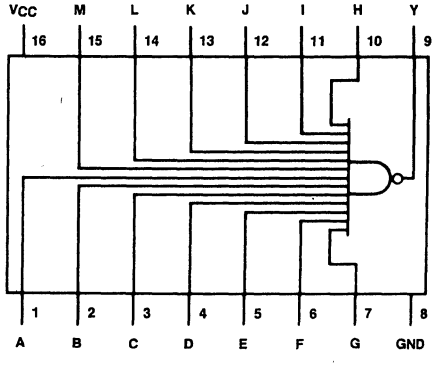
This NAND gate utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs. All devices have high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

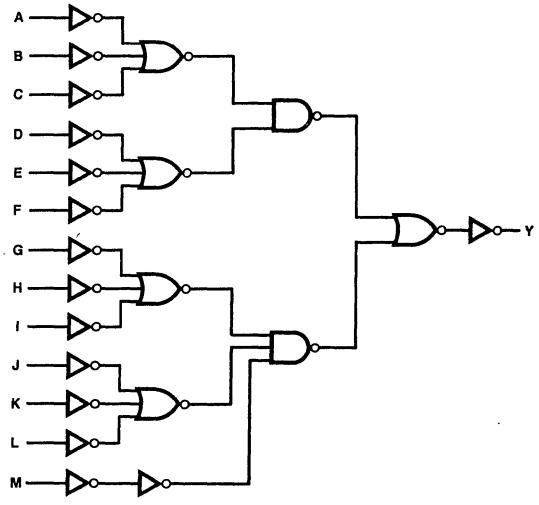
Dual-In-Line Package



TL/F/5134–1

Top View

Order Number MM54HC133J or MM74HC133J, N
See NS Package J16A or N16E



TL/F/5134–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		20	30	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	66	160	190	220	ns
			4.5V	23	35	42	49	ns
			6.0V	18	30	36	42	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			34				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC137/MM74HC137 3-to-8 Line Decoder With Address Latches (Inverted Output)

General Description

This device utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to implement a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and $\overline{G2}$ is low. The HC137 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

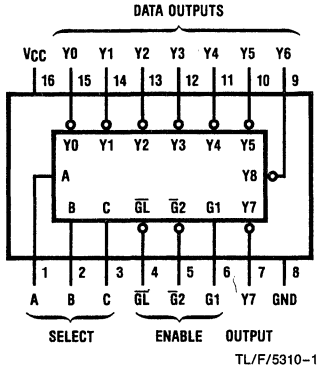
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing.
- Fanout of 10 LS-TTL loads.

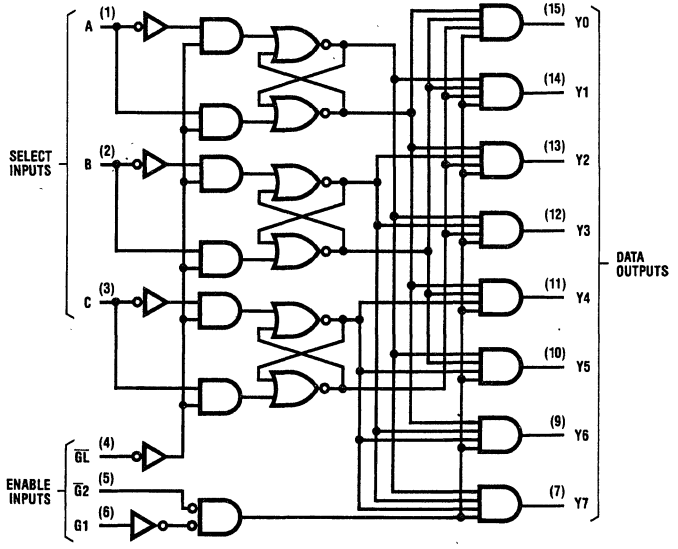
Connection and Functional Block Diagrams

Dual-In-Line Package



TL/F/5310–1

Order Number MM54HC137J or MM74HC137J,N
See NS Package J16A or N16E



TL/F/5310–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

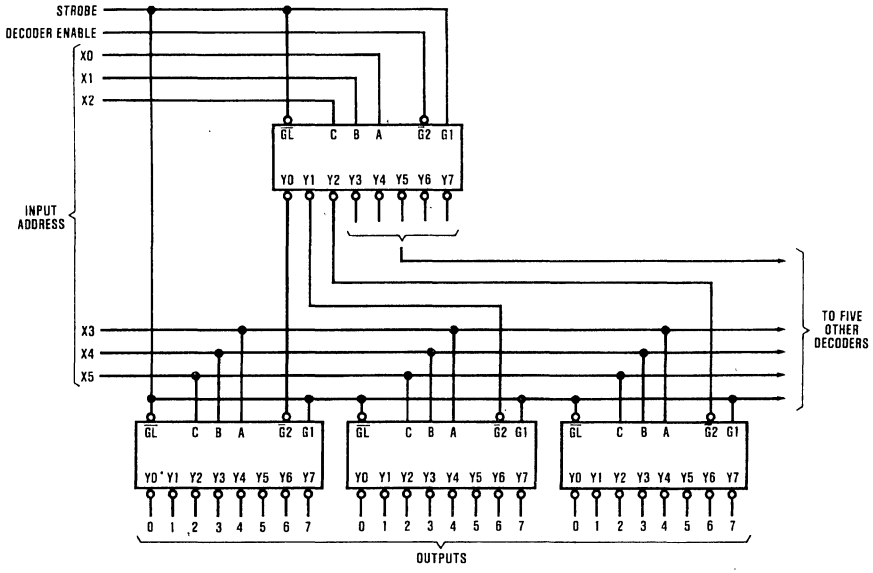
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		14	29	ns
t_{PHL}	Maximum Propagation Delay, A, B or C to any Y Output		20	42	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		12	22	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		15	34	ns
t_{PLH}	Maximum Propagation Delay G1 to any Output		13	25	ns
t_{PHL}	Maximum Propagation Delay GL to any Output		17	34	ns
t_{PLH}	Maximum Propagation GL to Output		15	30	ns
t_{PHL}	Maximum Propagation Delay GL to Output		22	34	ns
t_S	Minimum Setup Time at A, B and C Inputs			20	ns
t_H	Minimum Hold Time at A, B and C Inputs			0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		2.0V	85	170	214	253	ns
			4.5V	17	34	43	51	ns
			6.0V	14	29	36	43	ns
t_{PHL}	Maximum Propagation Delay A, B or C to any Y Output		2.0V	120	240	302	358	ns
			4.5V	24	48	60	72	ns
			6.0V	20	41	51	61	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2}$ to any Y Output		2.0V	65	130	164	194	ns
			4.5V	13	26	33	39	ns
			6.0V	11	22	28	33	ns
t_{PLH}	Maximum Propagation Delay G1 to Output		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}	Maximum Propagation Delay G1 to Output		2.0V	98	195	246	291	ns
			4.5V	20	39	49	58	ns
			6.0V	17	33	42	49	ns
t_{PLH}	Maximum Propagation Delay GL to Output		2.0V	88	175	221	261	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}	Maximum Propagation Delay GL to Output		2.0V	125	250	315	373	ns
			4.5V	25	50	63	75	ns
			6.0V	21	43	54	63	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2}$, to any Y Output		2.0V	98	195	246	291	ns
			4.5V	20	39	49	58	ns
			6.0V	17	33	42	49	ns
t_S	Minimum Setup Time at A, B and C inputs		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time at A, B and C inputs		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		8	11	13	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			75				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Typical Application



TL/F/5310–3

6-Line to 64-Line Decoder with Input Address Storage

Truth Table

Inputs						Outputs							
Enable			Select										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output corresponding to stored address L; all others, H							

H = high level, L = low level, X = irrelevant

National Semiconductor

microCMOS

MM54HC138/MM74HC138 3-to-8 Line Decoder

General Description

This decoder utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and is well suited to memory address decoding or data routing applications. The circuit features high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM54HC138/MM74HC138 has 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, $\overline{G2A}$ and $\overline{G2B}$) are provided to ease the cascading of decoders.

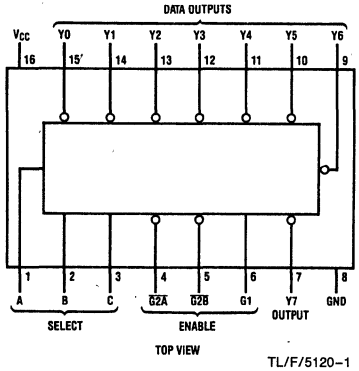
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

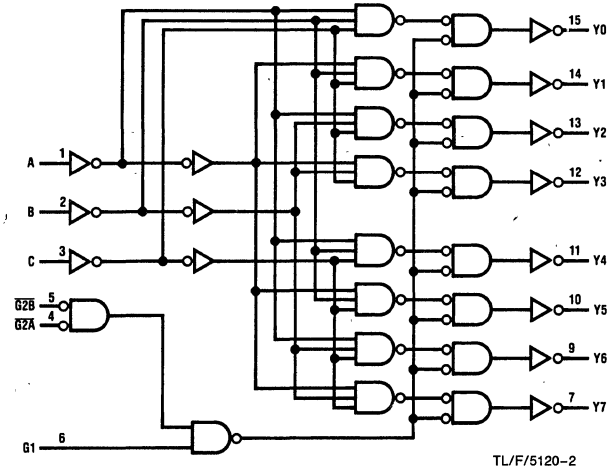
Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5120–1

Order Number MM54HC138J or MM74HC138J, N
See NS Package J16A or N16E



TL/F/5120–2

Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* $\overline{G2} = G2A + G2B$

H = high level, L = low level, X = don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay, Binary Select to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay, Binary Select to any Output		28	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, G1 to any Output		18	25	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		23	30	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		18	25	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PLH}	Maximum Propagation Delay Binary Select to any Output Low to High		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}	Maximum Propagation Delay Binary Select to any Output High to Low		2.0V	100	200	252	298	ns
			4.5V	20	40	40	60	ns
			6.0V	17	34	43	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay G1 to any Output		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	82	175	221	261	ns
			4.5V	28	35	44	52	ns
			6.0V	22	30	37	44	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Output		2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			3	10	10	10	μF
C_{PD}	Power Dissipation Capacitance	(Note 5)		75				μF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC139/MM74HC139 Dual 2-To-4 Line Decoder

General Description

This decoder utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and is well suited to memory address decoding or data routing applications. It possesses the high noise immunity and low power consumption usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL logic.

The MM54HC139/MM74HC139 contain two independent one-of-four decoders each with a single active low enable input (G1, or G2). Data on the select inputs (A1, and B1 or A2, and B2) cause one of the four normally high outputs to go low.

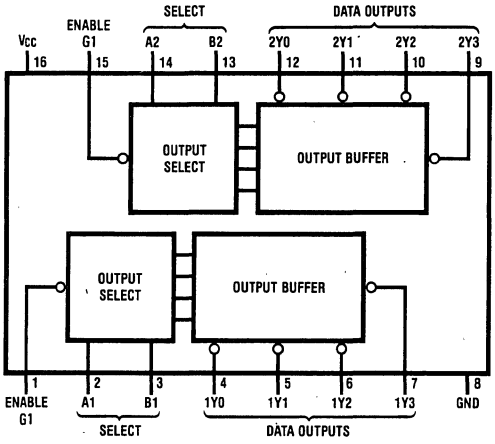
The decoder's outputs can drive 10 low power Schottky TTL equivalent loads, and are functionally as well as pin equivalent to the 54LS139/74LS139. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delays —
  Select to outputs (4 delays): 18 ns
  Select to output (5 delays): 28 ns
  Enable to output: 20 ns
- Low power: 40 μW quiescent supply power
- Fanout of 10 LS-TTL devices
- Input current maximum 1 μA, typical 10 pA

Connection Diagram

Dual-In-Line Package



TL/F/5311–1

Order Number MM54HC139J or MM74HC139J, N
See NS Package J16A or N16E

Truth Table

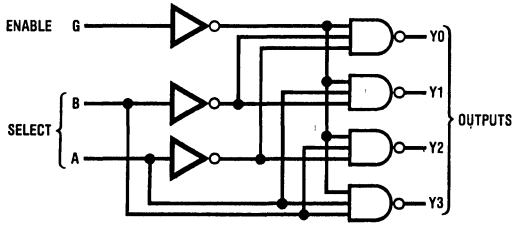
'HC139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

½ MM54HC139/MM74HC139



TL/F/5311–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 4 levels of delay		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Binary Select to any Output 5 levels of delay		28	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to any Output		19	30	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 4 levels of delay		2.0V	110	175	219	254	ns
			4.5V	22	35	44	51	ns
			6.0V	18	30	38	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Binary Select to any Output 5 levels of delay		2.0V	165	220	275	320	ns
			4.5V	33	44	55	64	ns
			6.0V	28	38	47	54	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to any Output		2.0V	115	175	219	254	ns
			4.5V	23	35	44	51	ns
			6.0V	19	30	38	44	ns
t_{TLH}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			3	10	10	10	μF
C_{PD}	Power Dissipation Capacitance (Note 5)	(Note 5)		75				μF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC147/MM74HC147 10-to-4 Line Priority Encoder

General Description

This high speed 10-to-4 Line Priority Encoder utilizes micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits. This device is fully buffered, giving it a fanout of 10 LS-TTL loads.

The MM54HC147/MM74HC147 features priority encoding of the inputs to ensure that only the highest order data line is encoded. Nine input lines are encoded to a four line BCD output. The implied decimal zero condition requires no input condition as zero is encoded when all nine data lines are at a high logic level. All data inputs and outputs are active at the low logic level.

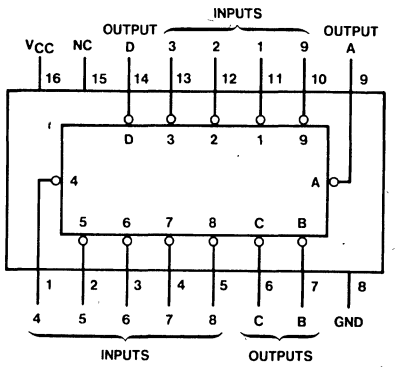
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent power consumption: 40 μW maximum at 25°C
- High speed: 31 ns propagation delay (typical)
- Very low input current: 10^{-5} μA typical
- Wide supply range: 2V to 6V

Connection and Logic Diagrams

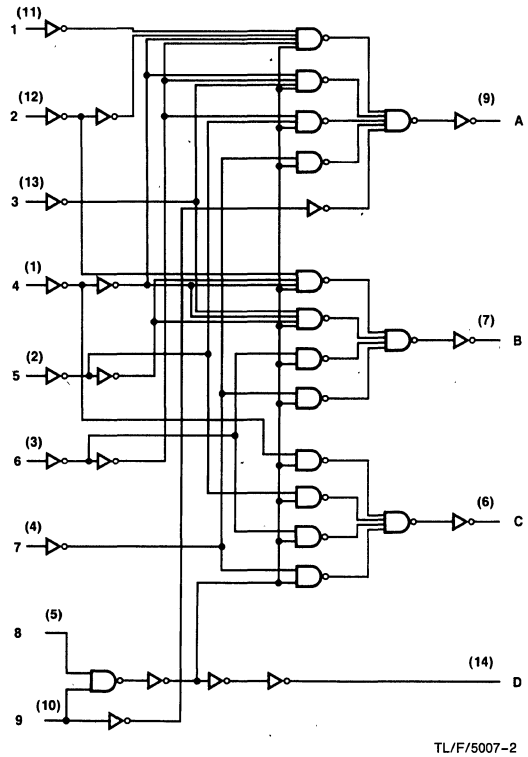
Dual-In-Line Package



TL/F/5007–1

Top View

Order Number MM54HC147J or MM74HC147J, N
See NS Package J16A or N16E



TL/F/5007–2

Truth Table

Inputs									Outputs			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	X	L	H	H	H	L	L	L
X	X	X	X	X	L	H	H	H	H	L	L	H
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Logic Level, L = Low Logic Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.7	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		31	38	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	181	220	275	319	ns
			4.5V	36	44	55	64	ns
			6.0V	31	37	47	54	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		180				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC149/MM74HC149
8 Line to 8 Line Priority Encoder

General Description

This priority encoder utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority encoder accepts 8 input request lines, $\overline{RI7}$–$\overline{RI0}$, and outputs 8 lines, $\overline{RO7}$–$\overline{RO0}$. Only one request output can be low at a time. The output that is low is dependent on the highest priority request that is low. The order of priority is $\overline{RI7}$ highest and $\overline{RI0}$ lowest. Also provided is and enable input, $\overline{RQE}$, which when high forces all outputs high. A request output is also provided, $\overline{RQP}$, which goes low when any $\overline{RIn}$ is active.

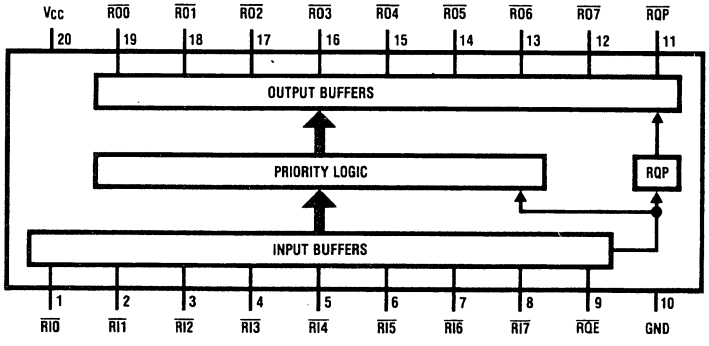
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- Propagation delay: 15 ns typical
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA max (74HC Series)
- Wide input noise immunity

Connection Diagram

Dual-In-Line Package



TL/F/5312–1

Top View

Order Number MM54HC149J or MM74HC149J,N
See NS Package J20A or N20A

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns (Note 6)

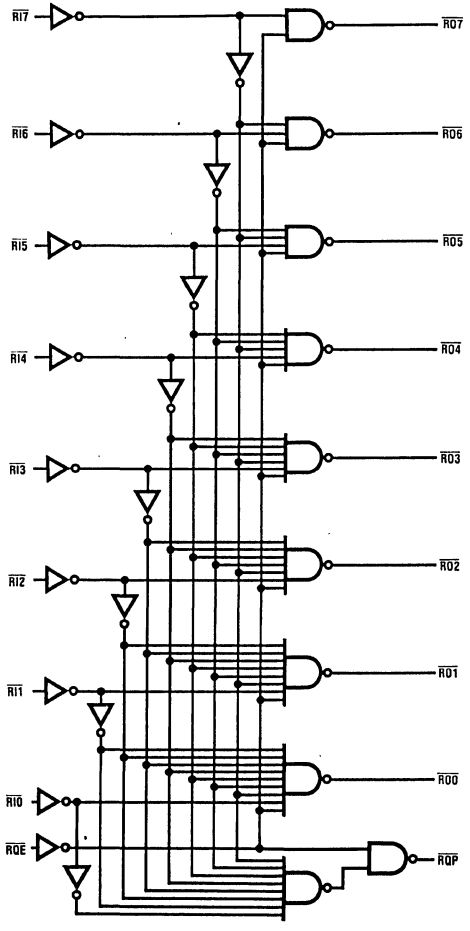
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any Input To Any Output		20	33	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any Input To Any Output		2.0V 4.5V 6.0V	73 25 21	205 41 35	255 51 43	310 62 53	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)			70				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Simplified Logic Diagram



TL/F/5312–2

National Semiconductor

MM54HC151/MM74HC151 8-Channel Digital Multiplexer

microCMOS

General Description

This high speed Digital multiplexer utilizes micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM54HC151/MM74HC151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output high and the Y output low.

The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family.

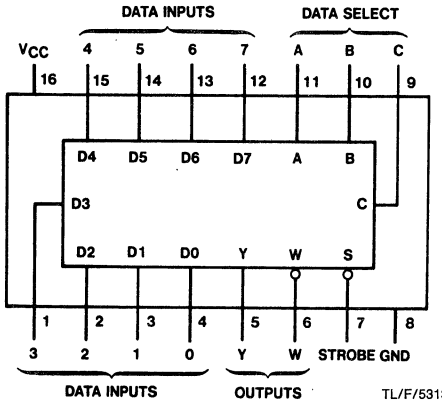
All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay data select to output Y: 26 ns
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 4 mA minimum

Connection and Logic Diagrams

Dual-In-Line Package



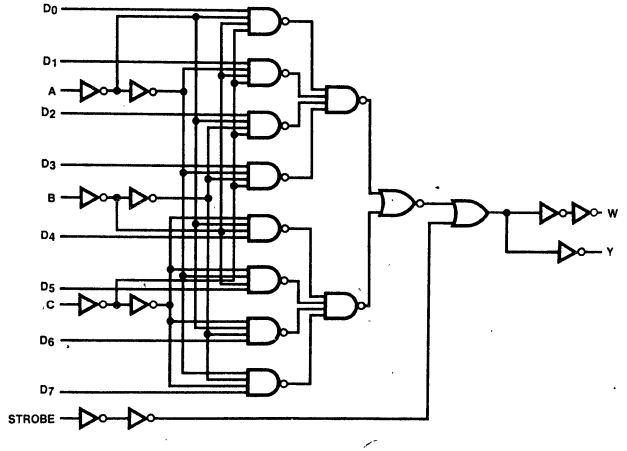
Top View

Order Number MM54HC151J or MM74HC151J, N
See NS Package J16A or N16E

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0, D1...D7 = the level of the respective D input



Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		24	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		17	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		16	21	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V	90	205	256	300	ns
			4.5V	31	41	51	60	ns
			6.0V	26	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to W		2.0V	95	205	256	300	ns
			4.5V	32	41	51	60	ns
			6.0V	27	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to Y		2.0V	70	195	244	283	ns
			4.5V	27	39	49	57	ns
			6.0V	23	33	41	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay any D to W		2.0V	75	185	231	268	ns
			4.5V	29	37	46	54	ns
			6.0V	25	32	40	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to Y		2.0V	50	140	175	203	ns
			4.5V	21	28	35	41	ns
			6.0V	18	24	30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Strobe to W		2.0V	45	127	159	185	ns
			4.5V	20	25	32	37	ns
			6.0V	17	22	28	32	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC153/MM74HC153 Dual 4-Input Multiplexer

General Description

This 4-to-1 line multiplexer utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the low power consumption and high noise immunity of standard CMOS integrated circuits. This device is fully buffered, allowing it to drive 10 LS-TTL loads. Information on the data inputs of each multiplexer is selected by the address on the A and B inputs, and is presented on the Y outputs. Each multiplexer possesses a strobe input which enables it when taken to a low logic level. When a high logic level is applied to a strobe input, the output of its associated multiplexer is taken low.

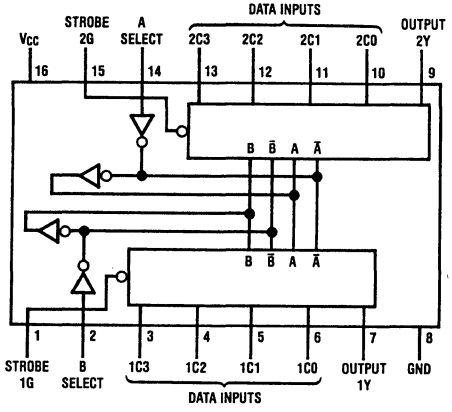
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5107–1

Top View

Order Number MM54HC153J or MM74HC153J,N
See NS Package J16A or N16E

Truth Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = don't care.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.3	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

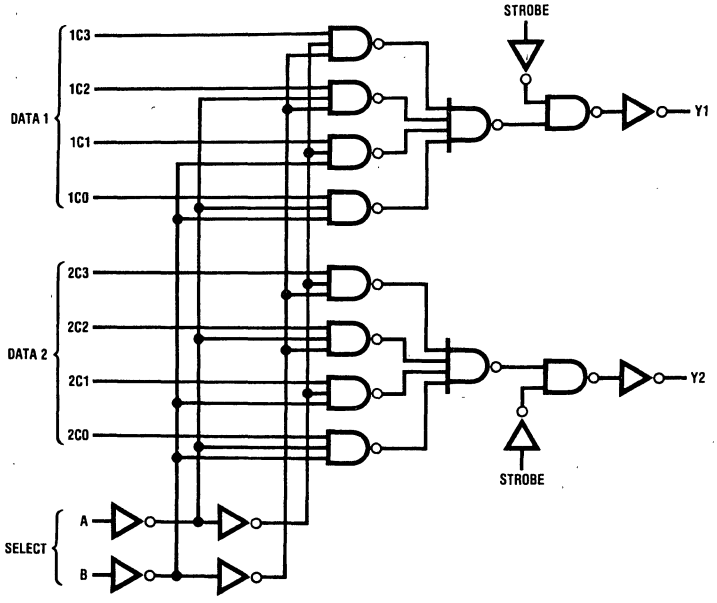
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		26	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		20	23	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y		8	15	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		2.0V	131	158	198	237	ns
			4.5V	29	35	44	52	ns
			6.0V	25	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		2.0V	99	126	158	189	ns
			4.5V	22	28	35	42	ns
			6.0V	19	23	29	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Y		2.0V	50	86	108	129	ns
			4.5V	12	19	24	29	ns
			6.0V	10	16	20	24	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)(per package)						
		Outputs Enabled		90				pF
		Outputs Disabled		25				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5107–2

National Semiconductor

microCMOS

MM54HC154/MM74HC154
4-to-16 Line Decoder

General Description

This decoder utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and is well suited to memory address decoding or data routing applications. It possesses high noise immunity, and low power consumption of CMOS with speeds similar to low power Schottky TTL circuits.

The MM54HC154/MM74HC154 have 4 binary select inputs (A, B, C, and D). If the device is enabled these inputs determine which one of the 16 normally high outputs will go low. Two active low enables ($\overline{G1}$ and $\overline{G2}$) are provided to ease cascading of decoders with little or no external logic.

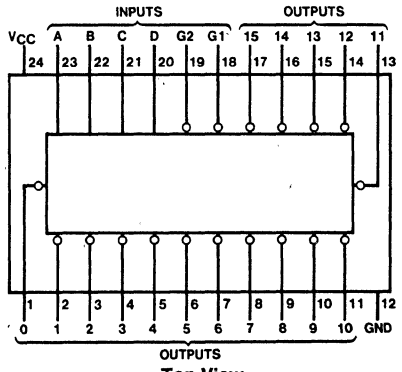
Each output can drive 10 low power Schottky TTL equivalent loads, and is functionally and pin equivalent to the 54LS154/74LS154. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 21 ns
- Power supply quiescent current: 80 μA (74HC)
- Wide power supply voltage range: 2–6V
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5122–1

Top View

Order Number MM54HC154J or MM74HC154J, N

See NS Package J24A or N24C

Truth Table

Inputs						Low Output*
$\overline{G1}$	$\overline{G2}$	D	C	B	A	
L	L	L	L	L	L	0
L	L	L	L	L	H	1
L	L	L	L	H	L	2
L	L	L	L	H	H	3
L	L	L	H	L	L	4
L	L	L	H	L	H	5
L	L	L	H	H	L	6
L	L	L	H	H	H	7
L	L	H	L	L	L	8
L	L	H	L	L	H	9
L	L	H	L	H	L	10
L	L	H	L	H	H	11
L	L	H	H	L	L	12
L	L	H	H	L	H	13
L	L	H	H	H	L	14
L	L	H	H	H	H	15
L	H	X	X	X	X	—
H	L	X	X	X	X	—
H	H	X	X	X	X	—

*All others high

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

3

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

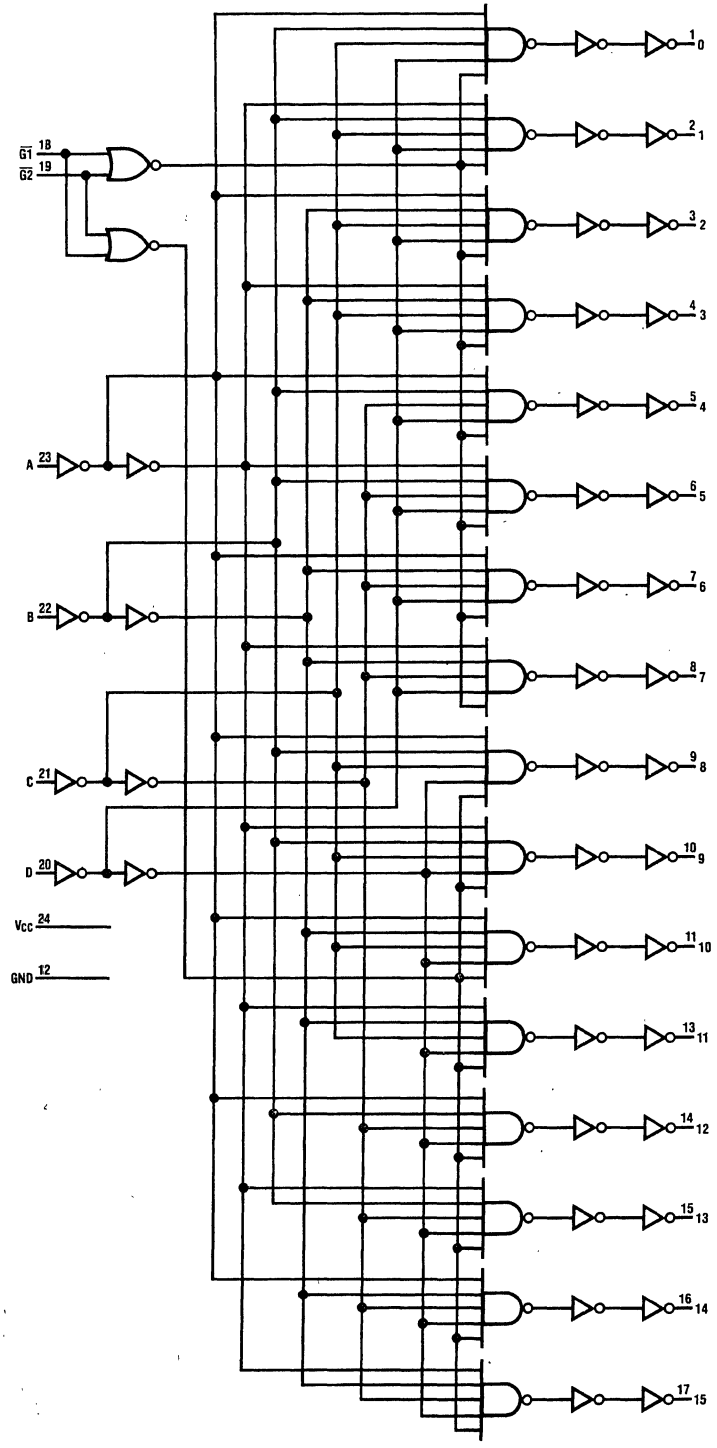
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, $\overline{G1}$, $\overline{G2}$ or A, B, C, D		21	32	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, $\overline{G1}$ or $\overline{G2}$ or A, B, C, D		2.0V	63	160	190	220	ns
			4.5V	24	36	42	46	ns
			6.0V	20	30	35	39	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5122–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC155/MM74HC155 Dual 2-To-4 Line Decoder/Demultiplexers

General Description

The MM54HC155/MM74HC155 is a high speed silicon-gate CMOS decoder/demultiplexer. It utilizes microCMOS Technology, 3μ silicon gate N well CMOS and features dual 1-line-to-4-line demultiplexers with independent strobes and common binary-address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without gating.

All inputs to the decoder are protected from damage due to electrostatic discharge by diodes to V_{CC} and Ground.

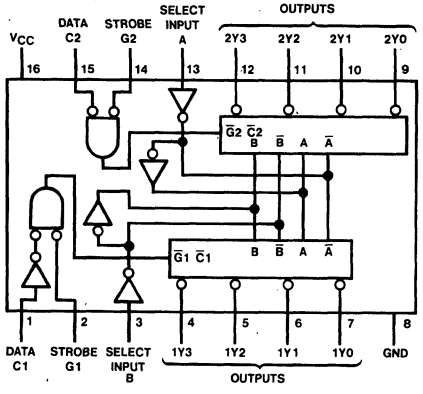
The device is capable of driving 10 low power Schottky TTL equivalent loads.

The MM54HC155/MM74HC155 is functionally and pin equivalent to the 54LS155/74LS155 with the advantage of reduced power consumption.

Features

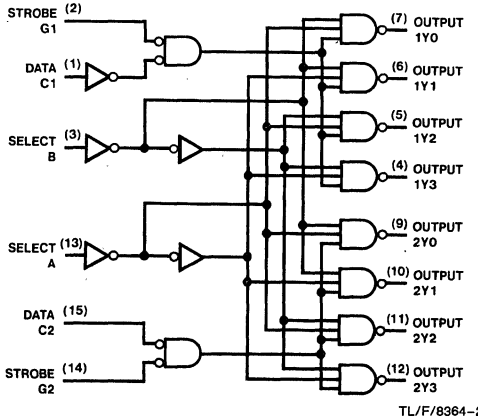
- Applications
  - Dual 2-to-4-line decoder
  - Dual 1-to-4-line demultiplexer
  - 3-to-8-line decoder
  - 1-to-8-line demultiplexer
- Typical propagation delay: 22 nS
- Low quiescent current: 40 μA maximum (74HC series)
- Wide operating range: 2–6V

Connect and Logic Diagrams



TL/F/8364–1

Order Number MM54HC155J or MM74HC155J, N
See NS Package J16A or N16E



TL/F/8364–2

Truth Tables

2-to-4-Line Decoder or 1-Line to 4-line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C1	B	A	G1	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

C = inputs C1 and C2 connected together
G = inputs G1 and G2 connected together
H = high level L = low level X = don't care

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	20 mA
DC Output Current, per pin (I_{OUT})	25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_d) (Note 3)	500 mW
Lead Temp. (T_l) (Soldering 10 sec)	260°C

Operating Conditions

	Min	Max	Unit
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HC	−40	+85	C
MM54HC	−55	+125	C
Input Rise/Fall Time V_{CC} = 2.0V		1000	ns
(t_r, t_f) V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40° to 85°C	54HC T_A = −55° to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\|$ = 20 μA	2.0V	2.0	1.9	1.9	1.9	V
		$\|I_{OUT}\|$ = 20 μA	4.5V	4.5	4.4	4.4	4.4	V
		$\|I_{OUT}\|$ = 20 μA	6.0V	6.0	5.9	5.9	5.9	V
		$\|I_{OUT}\|$ = 4.0 mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 5.2 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\|$ = 20 μA	2.0V	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 20 μA	4.5V	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 20 μA	6.0V	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 5.2 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.
ceramic "J" package: −12 mW/°C from 100°C to 125°.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC} and I_{OZ}) occur at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics (Note 6) V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

Symbol	Parameters	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs A, B, or C2 to any Output				ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs G1 or G2 to any Output				ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Input C1 to any Output				ns

AC Electrical Characteristics (Note 6) C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	V_{CC}	Typ	Guaranteed Limits			Units
			T = 25°C	T = 25°C	74HC T = −40° to 85°C	54HC T = −55° to 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs A, B, or C2 to any Output	2.0V					
		4.5V					
		6.0V					
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs G1 or G2 to any Output	2.0V					
		4.5V					
		6.0V					
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Input C1 to any Output	2.0V					
		4.5V					
		6.0V					
t_{TLH}, t_{THL}	Rise and Fall Time	2.0V					
		4.5V					
		6.0V					
C_{PD}	Power Dissipation Capacitance	2.0V					
		4.5V					
		6.0V					
C_{IN}	Minimum Input Capacitance		5	10	10	10	pF

Note 5: CPC determines the no load dynamic power consumption, P_d = (CPD*V_{CC}**2)*f + I_{CC} + V_{CC}, and the no load dynamic current composition, I_S = CPD*V_{CC}f + I_{CC}.

Note 6: Typical MM5474HC AC Switching Waveforms and Test Circuits.

National Semiconductor

microCMOS

MM54HC157/MM74HC157 Quad 2-Input Multiplexer
MM54HC158/MM74HC158 Quad 2-Input Multiplexer (Inverted Output)

General Description

These high speed Quad 2-to-1 Line data selector/Multiplexers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These devices each consist of four 2-input digital multiplexers with common select and STROBE inputs. On the MM54HC157/MM74HC157, when the STROBE input is at logical "0" the four outputs assume the values as selected from the inputs. When the STROBE input is at a logical "1" the outputs assume logical "0". The MM54HC158/MM74HC158 operates in the same manner, except that its outputs are inverted. Select decoding is done internally resulting in a single select input only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

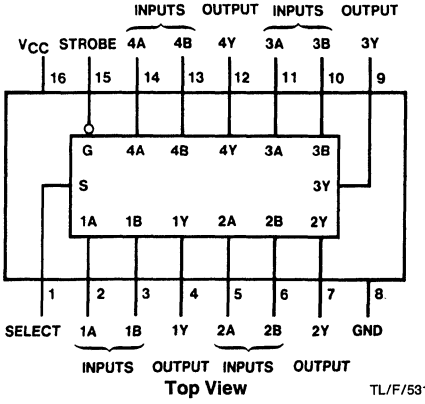
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

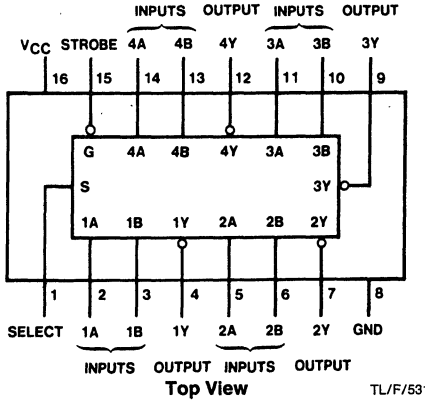
- Typical propagation delay: 14 ns data to any output
- Wide power supply range: 2–6V
- Low power supply quiescent current: 80 μA maximum (74HC Series)
- Fan-out of 10 LS-TTL loads
- Low input current: 1 μA maximum

Connection Diagrams

Dual-In-Line Packages



Top View TL/F/5314–1



Top View TL/F/5314–2

Order Number MM54HC157J, MM54HC158J, MM74HC157J,N or MM74HC158J,N
See NS Package J16A or N16E

Function Table

Inputs				Output Y	
Strobe	Select	A	B	HC157	HC158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		12	18	ns

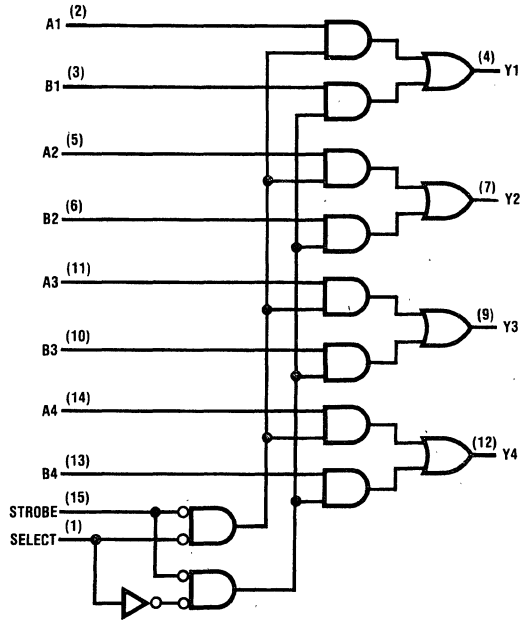
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		2.0V	63	125	158	186	ns
			4.5V	13	25	32	37	ns
			6.0V	11	21	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		2.0V	58	115	145	171	ns
			4.5V	12	23	29	34	ns
			6.0V	10	20	25	29	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per Multiplexer)						pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

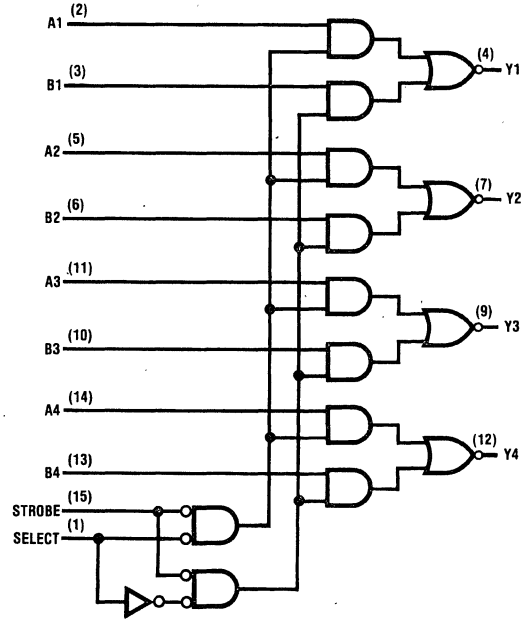
Logic Diagrams

'HC157



TL/F/5314–3

'HC158



TL/F/5314–4

National Semiconductor

PRELIMINARY

microCMOS

MM54HC160/MM74HC160 Synchronous Decade Counter with Asynchronous Clear MM54HC161/MM74HC161 Synchronous Binary Counter with Asynchronous Clear MM54HC162/MM74HC162 Synchronous Decade Counter with Synchronous Clear MM54HC163/MM74HC163 Synchronous Binary Counter with Synchronous Clear

General Description

The MM54HC160/MM74HC160, MM54HC161/MM74HC161, MM54HC162/MM74HC162, and MM54HC163/MM74HC163 synchronous presettable counters utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and internal look-ahead carry logic for use in high speed counting applications. They offer the high noise immunity and low power consumption inherent to CMOS with speeds similar to low power Schottky TTL. The 'HC160 and the 'HC162 are 4 bit decade counters, and the 'HC161 and the 'HC163 are 4 bit binary counters. All flip-flops are clocked simultaneously on the low to high to transition (positive edge) of the CLOCK input waveform.

These counters may be preset using the LOAD input. Presetting of all four flip-flops is synchronous to the rising edge of CLOCK. When LOAD is held low counting is disabled and the data on the A, B, C, and D inputs is loaded into the counter on the rising edge of CLOCK. If the load input is taken high before the positive edge of CLOCK the count operation will be unaffected.

All of these counters may be cleared by utilizing the CLEAR input. The clear function on the MM54HC162/MM74HC162 and MM54HC163/MM74HC163 counters are synchronous to the clock. That is, the counters are cleared on the positive edge of CLOCK while the clear input is held low.

The MM54HC160/MM74HC160 and MM54HC161/MM74HC161 counters are cleared asynchronously. When the CLEAR is taken low the counter is cleared immediately regardless of the CLOCK.

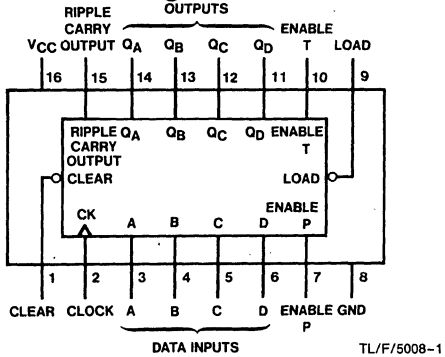
Two active high enable inputs (ENP and ENT) and a RIPPLE CARRY (RC) output are provided to enable easy cascading of counters. Both ENABLE inputs must be high to count. The ENT input also enables the RC output. When enabled, the RC outputs a positive pulse when the counter overflows. This pulse is approximately equal in duration to the high level portion of the Q_A output. The RC output is fed to successive cascaded stages to facilitate easy implementation of N-bit counters.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 40 MHz
- Typical propagation delay; clock to Q: 18 ns
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Wide power supply range: 2–6V

Connection Diagram



TL/F/5008–1

Order Number MM54HC160J, MM54HC161J, MM54HC162J, MM54HC163J, MM74HC160J, N, MM74HC161J, N, MM74HC162J, N or MM74HC163J, N
See NS Package J16A or N16E

Truth Tables

'HC160/HC161

CLK	CLR	ENP	ENT	Load	Function
X	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

H = high level, L = low level
X = don't care, ↑ = low to high transition

'HC162/HC163

CLK	CLR	ENP	ENT	Load	Function
↑	L	X	X	X	Clear
X	H	H	L	H	Count & RC disabled
X	H	L	H	H	Count disabled
X	H	L	L	H	Count & RC disabled
↑	H	X	X	L	Load
↑	H	H	H	H	Increment Counter

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		43	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to RC		30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		29	34	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, ENT to RC		18	32	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		27	38	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Set Up Time Clear, Load, Enable or Data to Clock			30	ns
t_H	Minimum Hold Time, Data from Clock			5	ns
t_W	Minimum Pulse Width Clock, Clear, or Load			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency		2.0V	10	5	4	4	MHz
			4.5V	40	27	21	18	MHz
			6.0V	45	32	25	21	MHz
t_{PHL}	Maximum Propagation Delay, Clock to RC		2.0V	100	215	271	320	ns
			4.5V	32	43	54	64	ns
			6.0V	28	37	46	54	ns
t_{PLH}	Maximum Propagation Delay, Clock to RC		2.0V	88	175	220	260	ns
			4.5V	18	35	44	52	ns
			6.0V	15	30	37	44	ns
t_{PHL}	Maximum Propagation Delay, Clock to Q		2.0V	95	205	258	305	ns
			4.5V	30	41	52	61	ns
			6.0V	26	35	44	52	ns
t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V	85	170	214	253	ns
			4.5V	17	34	43	51	ns
			6.0V	14	29	36	43	ns
t_{PHL}	Maximum Propagation Delay, ENT to RC		2.0V	90	195	246	291	ns
			4.5V	28	39	49	58	ns
			6.0V	24	33	42	49	ns
t_{PLH}	Maximum Propagation Delay, ENT to RC		2.0V	80	160	202	238	ns
			4.5V	16	32	40	48	ns
			6.0V	14	27	34	41	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q or RC		2.0V	100	220	277	328	ns
			4.5V	32	44	55	66	ns
			6.0V	28	37	47	55	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		125	158	186	ns
			4.5V		25	32	37	ns
			6.0V		21	27	32	ns
t_S	Minimum Set Up Time Clear, Load, or Data to Clock		2.0V		150	190	225	ns
			4.5V		30	38	45	ns
			6.0V		26	32	38	ns
t_S	Minimum Set Up Time Enable To Clock		2.0V		175	220	260	ns
			4.5V		35	44	52	ns
			6.0V		30	37	44	ns
t_H	Minimum Hold Time Data from Clock		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_H	Minimum Hold Time Enable, Load or Clear to Clock		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width Clock, Clear, or Load		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns

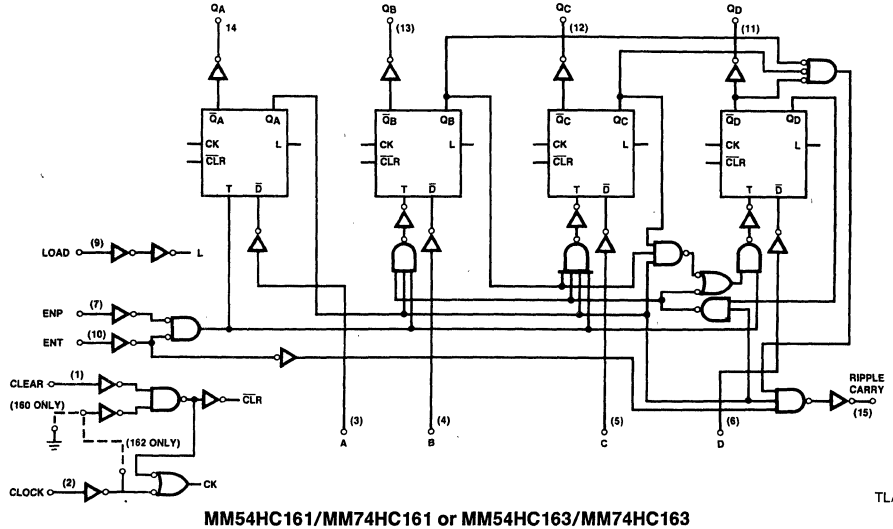
AC Electrical Characteristics (Continued) $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	40	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		90				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

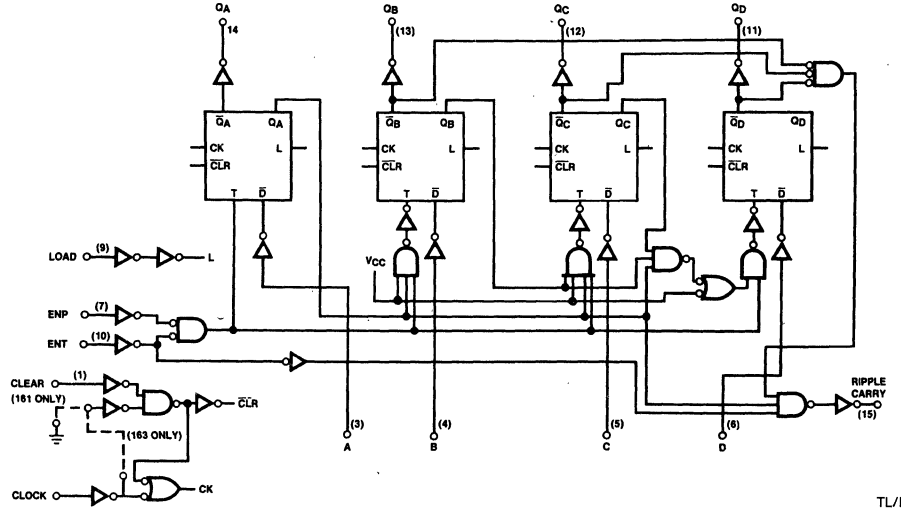
Logic Diagrams

MM54HC160/MM74HC160 or MM54HC162/MM74HC162



TL/F/5008–2

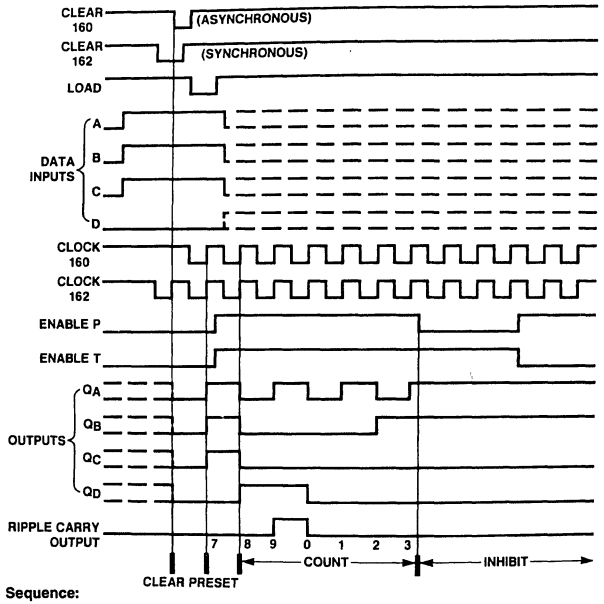
MM54HC161/MM74HC161 or MM54HC163/MM74HC163



TL/F/5008–3

Logic Waveforms

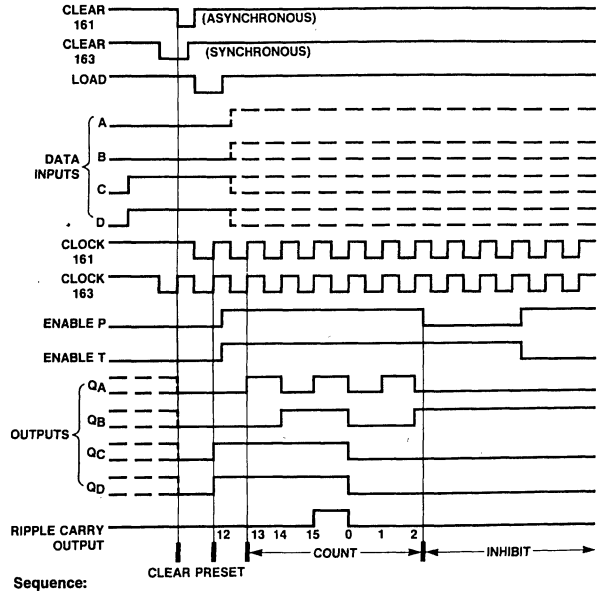
160, 162 Synchronous Decade Counters Typical Clear, Preset, Count and Inhibit Sequences



TL/F/5008–4

Sequence:
(1) Clear outputs to zero
(2) Preset to BCD seven
(3) Count to eight, nine, zero, one, two, and three
(4) Inhibit

161, 163 Synchronous Binary Counters Typical Clear, Preset, Count and Inhibit Sequences



TL/F/5008–5

Sequence:
(1) Clear outputs to zero
(2) Preset to binary twelve
(3) Count to thirteen, fourteen, fifteen, zero, one and two
(4) Inhibit

National Semiconductor

microCMOS

MM54HC164/MM74HC164
8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM54HC164/MM74HC164 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-Bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-Bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

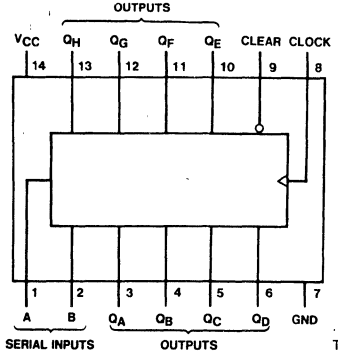
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 19 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

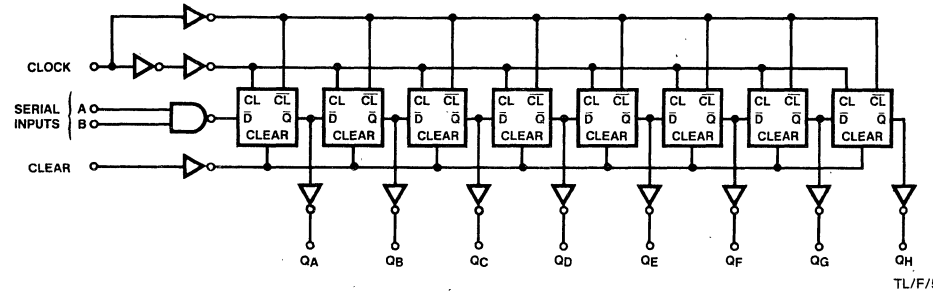
Dual-In-Line Package



TL/F/5315–1

Top View

Order Number MM54HC164J or MM74HC164J,N
See NS Package J14A or N14A



TL/F/5315–2

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		19	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Output		23	35	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	0	ns
t_S	Minimum Setup Time Data to Clock		12	20	ns
t_H	Minimum Hold Time Clock to Data		1	5	ns
t_W	Minimum Pulse Width Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V		5 27 31	4 21 24	3 18 20	MHz MHz MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V 4.5V 6.0V	115 13 20	175 35 30	218 44 38	254 51 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clear to Output		2.0V 4.5V 6.0V	140 28 24	205 41 35	256 51 44	297 59 51	ns ns ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V 4.5V 6.0V	−7 −3 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_S	Minimum Setup Time Data to Clock		2.0V 4.5V 6.0V	25 14 12	100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time Clock to Data		2.0V 4.5V 6.0V	−2 0 1	5 5 5	5 5 5	5 5 5	ns ns ns
t_W	Minimum Pulse Width Clear or Clock		2.0V 4.5V 6.0V	22 11 10	80 16 14	100 20 18	120 24 20	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V		75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)	5.0V	150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2 f+I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD} V_{CC} f+I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC165/MM74HC165
Parallel-in/Serial-out 8-Bit Shift Register

General Description

The MM54HC165/MM74HC165 high speed PARALLEL-IN/SERIAL-OUT SHIFT REGISTER utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the SHIFT/LOAD input. Also included is a gated CLOCK input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a CLOCK INHIBIT function. Holding either of the CLOCK inputs high inhibits clocking, and holding either CLOCK input low with the SHIFT/LOAD input high enables the other CLOCK input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the SHIFT/LOAD input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

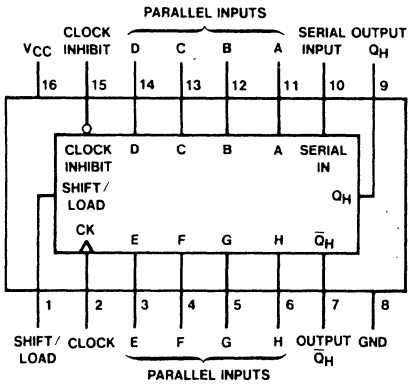
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5316–1

Top View

Order Number MM54HC165J or MM74HC165J,N
See NS Package J16A or N16E

Function Table

Inputs					Internal Outputs		Output Q_H
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A . . . H	Q_A	Q_B	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{AN}	Q_{GN}
H	L	↑	L	X	L	Q_{AN}	Q_{GN}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{AN}, Q_{GN} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND V_{CC} = 2–6V	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA V_{CC} = 2–6V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/Parallel Load to Q_H		13	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		15	25	ns
t_S	Minimum Setup Time Serial Input to Clock, Parallel or Data to Shift/Load		10	20	ns
t_S	Minimum Setup Time Shift/Load to Clock		11	20	ns
t_S	Minimum Setup Time Clock Inhibit to Clock		10	20	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load			0	ns
t_W	Minimum Pulse Width Clock			16	ns

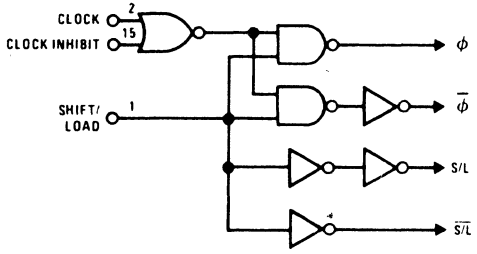
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	50	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay H to Q_H or $\overline{Q}_H$		2.0V	70	150	189	225	ns
			4.5V	21	30	38	45	ns
			6.0V	18	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Serial Shift/ Parallel Load to Q_H		2.0V	70	175	220	260	ns
			4.5V	21	35	44	52	ns
			6.0V	18	30	37	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Output		2.0V	70	150	189	225	ns
			4.5V	21	30	38	45	ns
			6.0V	18	26	33	39	ns
t_S	Minimum Setup Time Serial Input to Clock, or Parallel Data to Shift/Load		2.0V	35	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time Shift/Load to Clock		2.0V	38	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time Clock Inhibit to Clock		2.0V	35	100	125	150	ns
			4.5V	11	20	25	30	ns
			6.0V	9	17	21	25	ns
t_H	Minimum Hold Time Serial Input to Clock or Parallel Data to Shift/Load		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width, Clock		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	9	15	19	22	ns
			6.0V	8	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

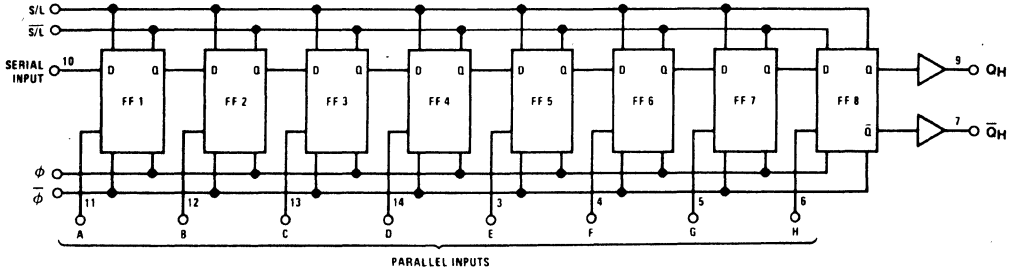
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

Logic Diagrams



TL/F/5316–2



TL/F/5316–3

National Semiconductor

microCMOS

MM54HC173/MM74HC173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54HC173/MM74HC173 is a high speed TRI-STATE QUAD D TYPE FLIP-FLOP that utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It possesses the low power consumption and high noise immunity of standard CMOS integrated circuits, and can operate at speeds comparable to the equivalent low power Schottky device. The outputs are buffered, allowing this circuit to drive 15 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

The four D TYPE FLIP-FLOPS operate synchronously from a common clock. The TRI-STATE outputs allow the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip-flops to remain in their present states without having to disrupt the clock. If either of the 2 input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs, forcing the flip flops to remain in the same state. Clearing is enabled by taking the CLEAR input to a logic "1" level. The data outputs change state on the positive going edge of the clock.

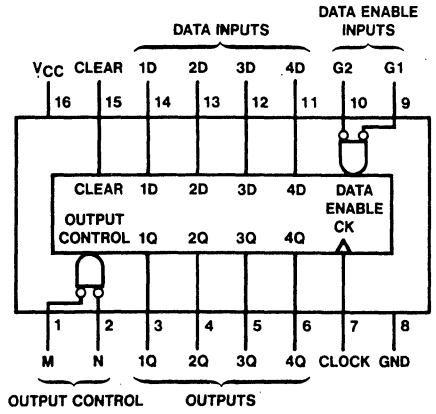
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating supply voltage range: 2–6V
- TRI-STATE outputs
- Low input current: <1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 6 mA minimum

Connection Diagram

Dual-In-Line Package



TL/F/5317–1

Top View

Order Number MM54HC173J or MM74HC173J,N
See NS Package J16A or N16E

Truth Table

Inputs					Output Q
Clear	Clock	Data Enable G1	Data Enable G2	Data D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state: however, sequential operation of the flip-flops is not affected.

H = high level (steady state)

L = low level (steady state)

↑ = low-to-high level transition

X = don't care (any input including transitions)

Q_0 = the level of Q before the indicated steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V		3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V		0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT}=V_{CC} or GND Enable=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay: Clock to Q			31	ns
t_{PHL}	Maximum Propagation Delay: Clear to Q		18	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	16	25	ns
t_S	Minimum Data Setup Time			20	ns
t_S	Minimum Data Enable Setup Time			20	ns
t_H	Minimum Data Hold Time			0	ns
t_H	Minimum Data Enable Hold Time			0	ns
t_W	Minimum Clock Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	55	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q	$C_L=50$ pF	2.0V	80	175	220	262	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	23	35	44	53	ns
		$C_L=150$ pF	4.5V	28	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	38	45	ns
		$C_L=150$ pF	6.0V	26	38	48	57	ns
t_{PHL}	Maximum Propagation Delay from Clear to Q	$C_L=50$ pF	2.0V	70	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	20	30	38	45	ns
		$C_L=150$ pF	4.5V	25	40	50	60	ns
		$C_L=50$ pF	6.0V	17	26	32	38	ns
		$C_L=150$ pF	6.0V	22	34	43	51	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	70	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	20	30	38	45	ns
		$C_L=150$ pF	4.5V	25	40	50	60	ns
		$C_L=50$ pF	6.0V	17	26	32	38	ns
		$C_L=150$ pF	6.0V	22	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	70	150	189	224	ns
			4.5V	20	30	38	45	ns
			6.0V	17	26	32	38	ns
t_S	Minimum Data or Data Enable Setup Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_{REM}	Minimum Removal Time		2.0V		90	112	135	ns
			4.5V		18	22	26	ns
			6.0V		15	19	22	ns
t_H	Minimum Data or Data Enable Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Clear or Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns

3

AC Electrical Characteristics (Continued)

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	5	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance	(per flop)		80				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

microCMOS

MM54HC174/MM74HC174
Hex D Flip-Flops With Clear

General Description

These edge triggered flip-flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 6 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The CLEAR input when low, sets all outputs to a low state.

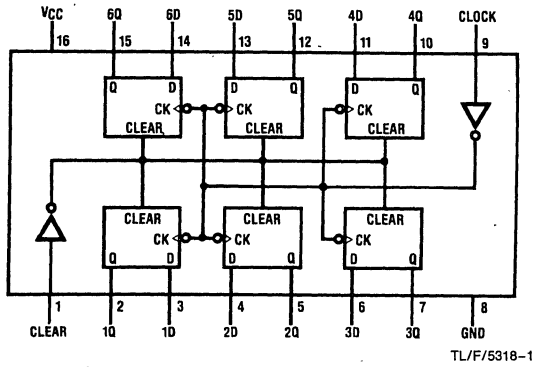
Each output can drive 10 low power Schottky TTL equivalent loads. The MM54HC174/MM74HC174 is functionally as well as pin compatible to the 54LS174/74LS174. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA (74HC Series)
- Output drive: 10 LSTTL loads

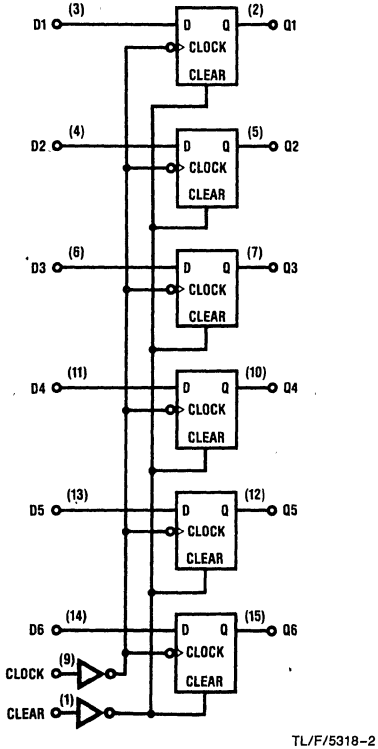
Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5318–1

Order Number MM54HC174J or MM74HC174J, N
See NS Package J16A or N16E



TL/F/5318–2

Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = High level (steady state)
L = Low level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady state input conditions were established.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock or Clear to Output		16	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	5	ns
t_S	Minimum Setup Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		0	5	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock or Clear to Output		2.0V	55	165	206	248	ns
			4.5V	18	33	41	49	ns
			6.0V	16	28	35	42	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t_S	Minimum Setup Time Data to Clock		2.0V	42	100	125	150	ns
			4.5V	12	20	25	30	ns
			6.0V	10	17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V	1	5	5	5	ns
			4.5V	1	5	5	5	ns
			6.0V	1	5	5	5	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	35	80	106	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		136				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC175/MM74HC175
Quad D-Type Flip-Flop With Clear

General Description

This high speed D-TYPE FLIP-FLOP with complementary outputs utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Information at the D inputs of the MM54HC175/MM74HC175 is transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip flop are externally available. All four flip flops are controlled by a common clock and a common CLEAR. Clearing is accomplished by a negative pulse at the CLEAR input. All four Q outputs are cleared to a logical "0" and all four $\overline{Q}$ outputs to a logical "1."

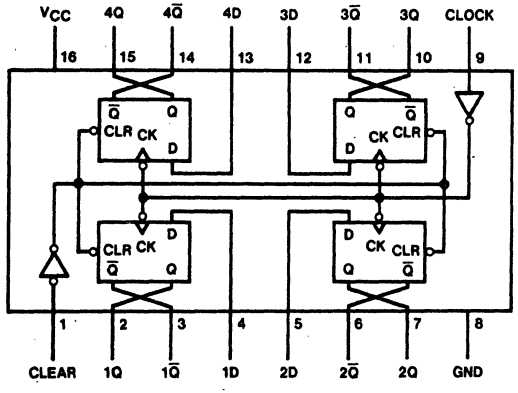
The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA maximum
- Low quiescent supply current: 80 μA maximum (74HC)
- High output drive current: 4 mA minimum (74HC)

Connection Diagram

Dual-In-Line Package



TL/F/5319–1

Top View

Order Number MM54HC175J or MM74HC175J,N
See NS Package J16A or N16E

Truth Table

(Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

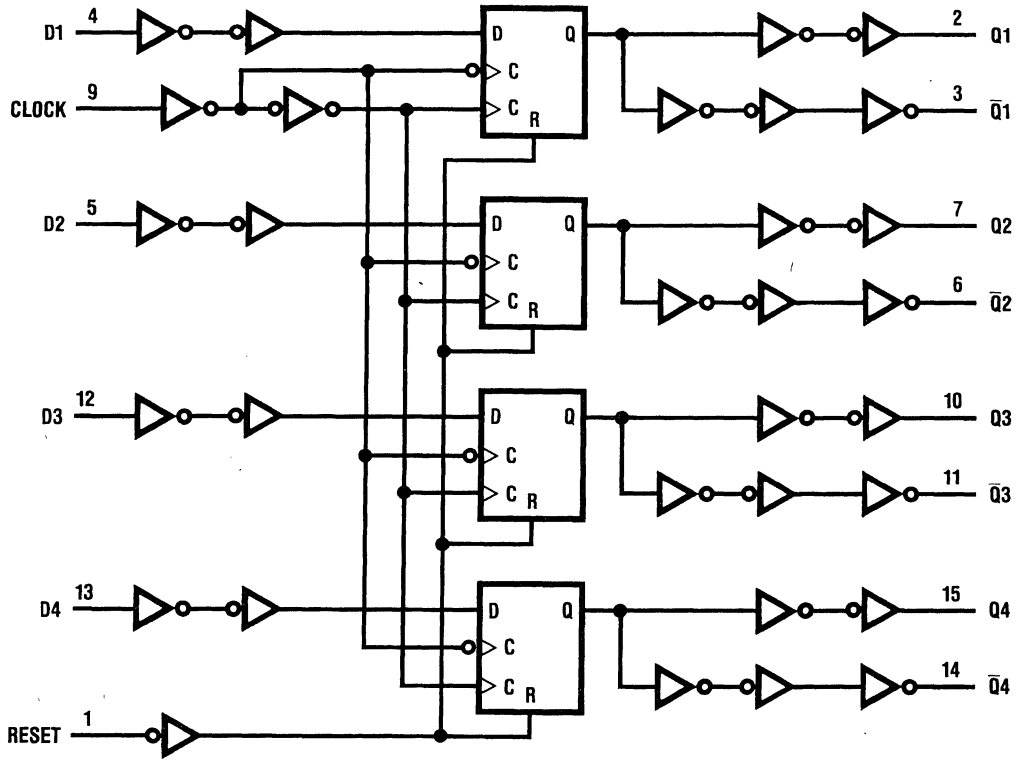
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		60	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		15	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		13	21	ns
t_{REC}	Minimum Removal Time, Clear to Clock			20	ns
t_S	Minimum Setup Time, Data to Clock			20	ns
t_H	Minimum Hold Time, Data from Clock			0	ns
t_W	Minimum Pulse Width, Clock or Clear		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	12	6	5	4	MHz
			4.5V	60	30	24	20	MHz
			6.0V	70	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$		2.0V	80	150	190	225	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset to Q or $\overline{Q}$		2.0V	64	125	158	186	ns
			4.5V	14	25	32	37	ns
			6.0V	12	21	27	32	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Setup Time Data to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Data from Clock		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	9	15	19	22	ns
			6.0V	8	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5319–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC181/MM74HC181 Arithmetic Logic Units/Function Generators

General Description

These arithmetic logic units (ALU)/function generators utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The MM54HC181/MM74HC181 are arithmetic logic unit (ALU)/function generators that have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the MM54HC182 or MM74HC182, full carry look-ahead circuits, high-speed arithmetic operations can be performed. The method of cascading HC182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the MM54HC182/MM74HC182.

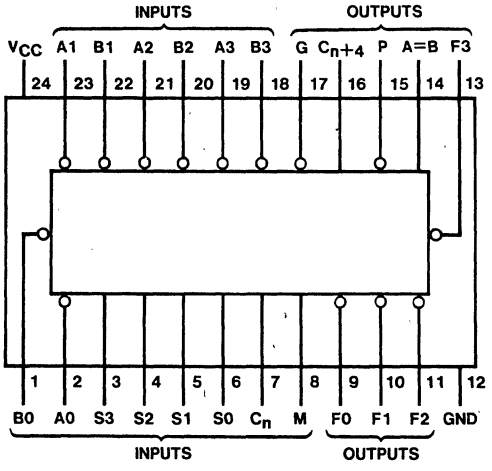
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

Features

- Full look-ahead for high-speed operations on long words
- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand a one position magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5320–1

Top View

Order Number MM54HC181J or MM74HC181J, N
See NS Package J24F or N24C

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Outputs
P	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

General Description (Continued)

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to produce A—B.

The 181 can also be utilized as a comparator. The A=B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A=B). The ALU should be in the subtract mode with C_n=H when performing this comparison. The A=B output is open-drain so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The MM54HC181/MM74HC181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table 1; those obtained with the signal designations of *Figure 2* are given in Table 2.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table 1)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-Low Data (Table 1)	$\overline{A0}$	$\overline{B0}$	$\overline{A1}$	$\overline{B1}$	$\overline{A2}$	$\overline{B2}$	$\overline{A3}$	$\overline{B3}$	$\overline{F0}$	$\overline{F1}$	$\overline{F2}$	$\overline{F3}$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Input C_n	Output C_n+4	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

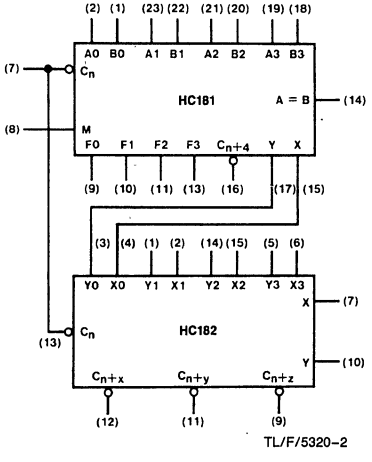


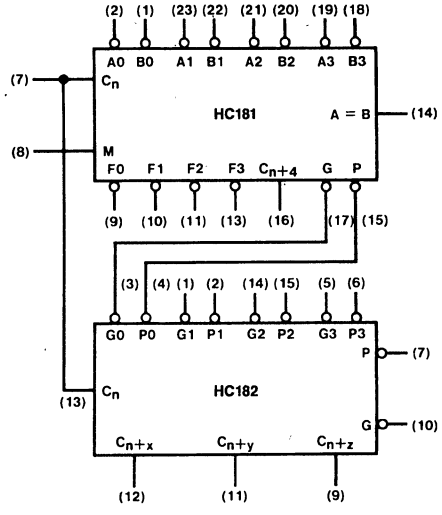
FIGURE 1

Table I

Selection				Active High Data		
				M=H	M=L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n=H (no carry)	C_n=L (with carry)
L	L	L	L	F=$\overline{A}$	F=A	F=A Plus 1
L	L	L	H	F=$\overline{A+B}$	F=A + B	F=(A + B) Plus 1
L	L	H	L	F=$\overline{A}B$	F=A + $\overline{B}$	F=(A + $\overline{B}$) Plus 1
L	L	H	H	F=0	F=Minus 1 (2's Compl)	F=Zero
L	H	L	L	F=$\overline{AB}$	F=A Plus A$\overline{B}$	F=A Plus A$\overline{B}$ Plus 1
L	H	L	H	F=$\overline{B}$	F=(A + B) Plus A$\overline{B}$	F=(A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F=A ⊕ B	F=A Minus B Minus 1	F=A Minus B
L	H	H	H	F=A$\overline{B}$	F=A$\overline{B}$ Minus 1	F=A$\overline{B}$
H	L	L	L	F=$\overline{A}$ + B	F=A Plus AB	F=A Plus AB Plus 1
H	L	L	H	F=$\overline{A \oplus B}$	F=A Plus B	F=A Plus B Plus 1
H	L	H	L	F=B	F=(A + $\overline{B}$) Plus AB	F=(A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F=AB	F=AB Minus 1	F=AB
H	H	L	L	F=1	F=A Plus A*	F=A Plus A Plus 1
H	H	L	H	F=A + $\overline{B}$	F=(A + B) Plus A	F=(A + B) Plus A Plus 1
H	H	H	L	F=A + B	F=(A + $\overline{B}$) Plus A	F=(A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F=A	F=A Minus 1	F=A

*Each bit is shifted to the next more significant position.

General Description (Continued)



TL/F/5320–3

FIGURE 2

Table II

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = (A$\overline{B}$)
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A + B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$ Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A + B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage (any output except A=B)	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
I_{LKG}	Maximum Leakage Open Drain Output Current (A=B Output)	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC}	6.0V		0.5	5.0	10	μA
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC} = 5V, T_A = 25°C, C_L = 15\ pF, t_r = t_f = 6\ ns$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to C_n+4		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_N+4	M = 0V, S0 = S3 = V_{CC} S1 = S0 = 0V ($\overline{\text{Sum}}$ mode)	30	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_N+4	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff.}}$ mode)	30	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to any F	M = 0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff.}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	27	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	24	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	19	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = V_{CC} (Logic mode)	25	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to A = B	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	25	37	ns

AC Electrical Characteristics C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to C_n+4		2.0V 4.5V 6.0V	 	125 25 22	155 31 28	190 38 33	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_n+4	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V 4.5V 6.0V	110 35 30	250 50 43	325 63 53	375 75 65	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to C_n+4	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	 	250 50 43	325 63 53	375 75 65	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from C_n to any F	M = 0V ($\overline{\text{Sum}}$ or $\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	65 22 14	150 32 28	190 40 35	225 48 42	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = V_{CC}, S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V 4.5V 6.0V	70 20 12	175 35 30	220 44 38	263 53 45	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to G	M = 0V, S0 = S3 = 0V S1 = S2 ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	65 23 16	165 33 29	210 42 37	250 50 44	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V 4.5V 6.0V	80 30 25	220 44 37	275 55 47	330 66 56	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to P	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	75 27 24	195 39 34	244 49 43	293 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = V_{CC} S1 = S2 = 0V ($\overline{\text{Sum}}$ mode)	2.0V 4.5V 6.0V	70 26 21	180 36 31	225 45 39	270 54 47	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	 	160 32 27	200 40 34	290 48 41	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from A_I or B_I to F_I	M = V_{CC} (Logic mode)	2.0V 4.5V 6.0V	180 30 23	200 40 34	250 50 43	300 60 51	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from any A or B to A = B	M = 0V, S0 = S3 = 0V S1 = S2 = V_{CC} ($\overline{\text{Diff}}$ mode)	2.0V 4.5V 6.0V	180 30 23	200 40 34	250 50 43	300 60 51	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	15	15	15	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

Parameter Measurement Information

Logic Mode Test Table **Function Inputs: S1 = S2 = M = V_{CC}, S0 = S3 = 0 V**

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	F_I	Out-of-Phase

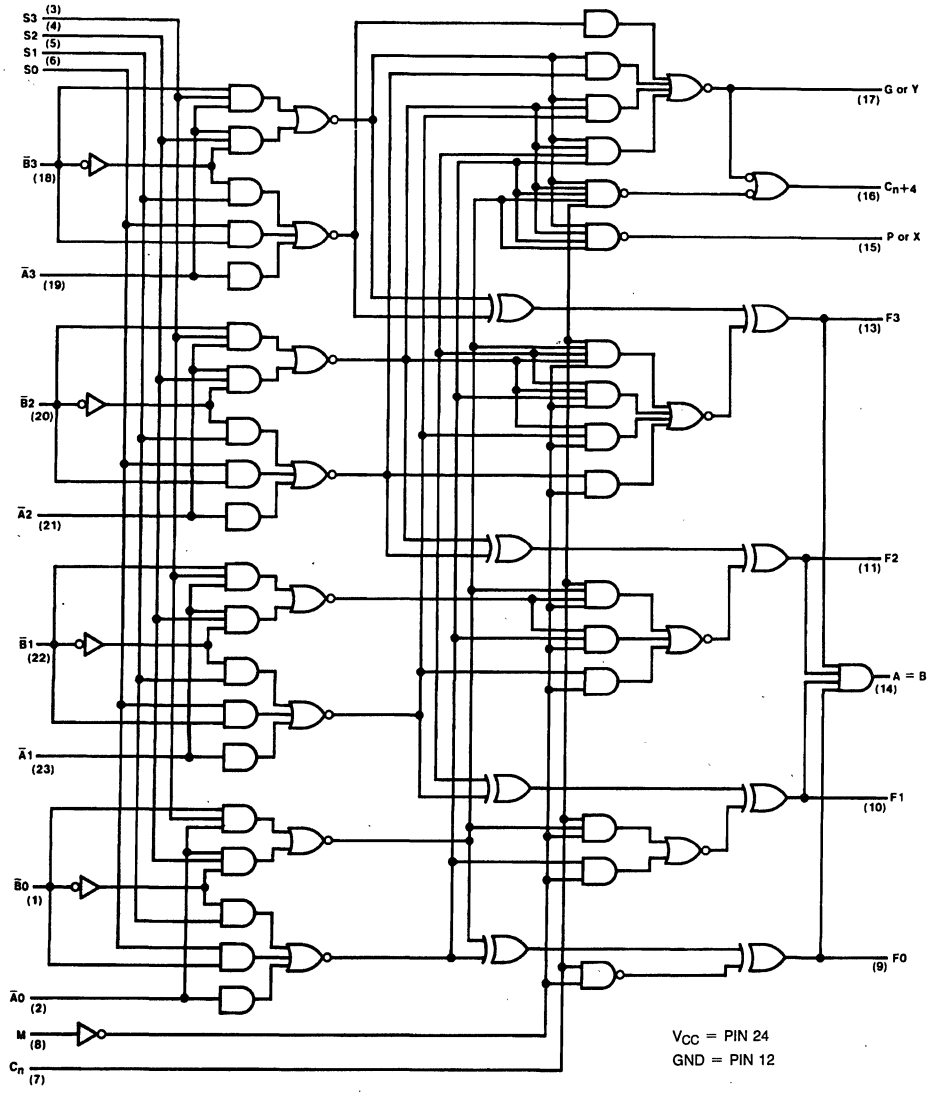
$\overline{SUM}$ Mode Test Table **Function Inputs: S0 = S3 = V_{CC} S1 = S2 = M = 0 V**

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	B_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A and B	C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	G	In-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

$\overline{Diff}$ Mode Test Table **Function Inputs: S1 = S2 = V_{CC}, S0 = S3 = M = 0 V**

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply V_{CC}	Apply GND	Apply V_{CC}	Apply GND		
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	F_I	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	F_I	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	None	Remaining A and B, C_n	P	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A and B, C_n	G	In-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PHL}, t_{PLH}	A_I	None	B_I	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PHL}, t_{PLH}	B_I	A_I	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PHL}, t_{PLH}	C_n	None	None	All A and B	None	C_n+4 or any F	In-Phase
t_{PHL}, t_{PLH}	A_I	B_I	None	None	Remaining A, B, C_n	C_n+4	Out-of-Phase
t_{PHL}, t_{PLH}	B_I	None	A_I	None	Remaining A, B, C_n	C_n+4	In-Phase

Logic Diagram



TL/F/5320–4

National Semiconductor

PRELIMINARY

microCMOS

MM54HC182/MM74HC182 Look-Ahead Carry Generator

General Description

The MM54HC182/MM74HC182 is a high speed LOOK-AHEAD CARRY GENERATOR utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

These circuits are capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the HC181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each HC182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

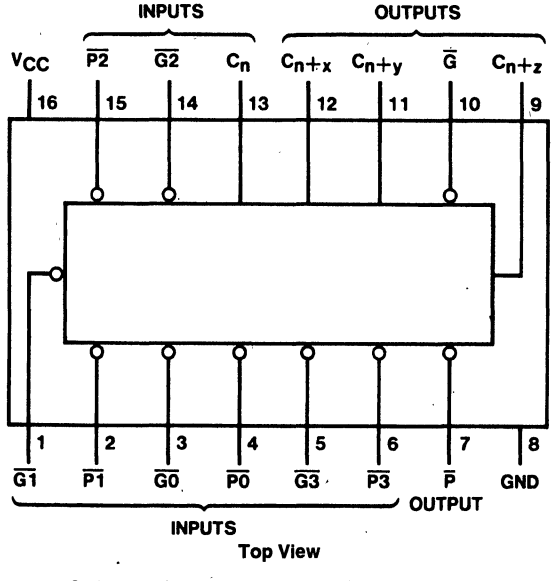
Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions as explained on the HC181 data sheet are also applicable to and compatible with the look-ahead generator.

Features

- TTL pinout compatible
- Typical propagation delay: 18 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: $< 1\ \mu A$
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5321–1

Top View

Order Number MM54HC182J or MM74HC182J, N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Pn to P		16	24	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Cn to any output		18	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay - Pn or Gn to any output		23	35	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Pn to P		2.0V	45	140	162	ns
			4.5V	18	35	40	ns
			6.0V	15	27	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Cn to any output		2.0V	50	156	182	ns
			4.5V	20	37	44	ns
			6.0V	16	30	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Pn or Gn to any output		2.0V	62	194	225	ns
			4.5V	25	46	54	ns
			6.0V	22	42	48	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	25	95	110	ns
			4.5V	7	19	22	ns
			6.0V	6	16	19	ns
C_{PD}	Power Dissipation Capacitance			150			pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Equations

$$C_{n+x} = G0 + P0\ C_n$$

$$C_{n+y} = G1 + P1\ G0 + P1\ P0\ C_n$$

$$C_{n+z} = G2 + P2\ G1 + P2\ P1\ P0\ C_n$$

$$\overline{G} = \overline{G3 + P3\ G2 + P3\ P2\ G1 + P3\ P2\ P1\ G0}$$

$$\overline{P} = \overline{P3\ P2\ P1\ P0}$$

or

$$\overline{C}_{n+x} = \overline{Y0\ (X0 + C_n)}$$

$$\overline{C}_{n+y} = \overline{Y1\ [X1 + Y0\ (X0 + C_n)]}$$

$$\overline{C}_{n+z} = \overline{Y2\ \{X2 + Y1\ [X1 + Y0\ (X0 + C_n)]\}}$$

$$Y = Y3\ (X3 + Y2)\ (X3 + X2 + Y1)\ (X3 + X2 + X1 + Y0)$$

$$X = X3 + X2 + X1 + X0$$

FUNCTION TABLE FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FUNCTION TABLE FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FUNCTION TABLE FOR C_{n+x} OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

FUNCTION TABLE FOR C_{n+z} OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

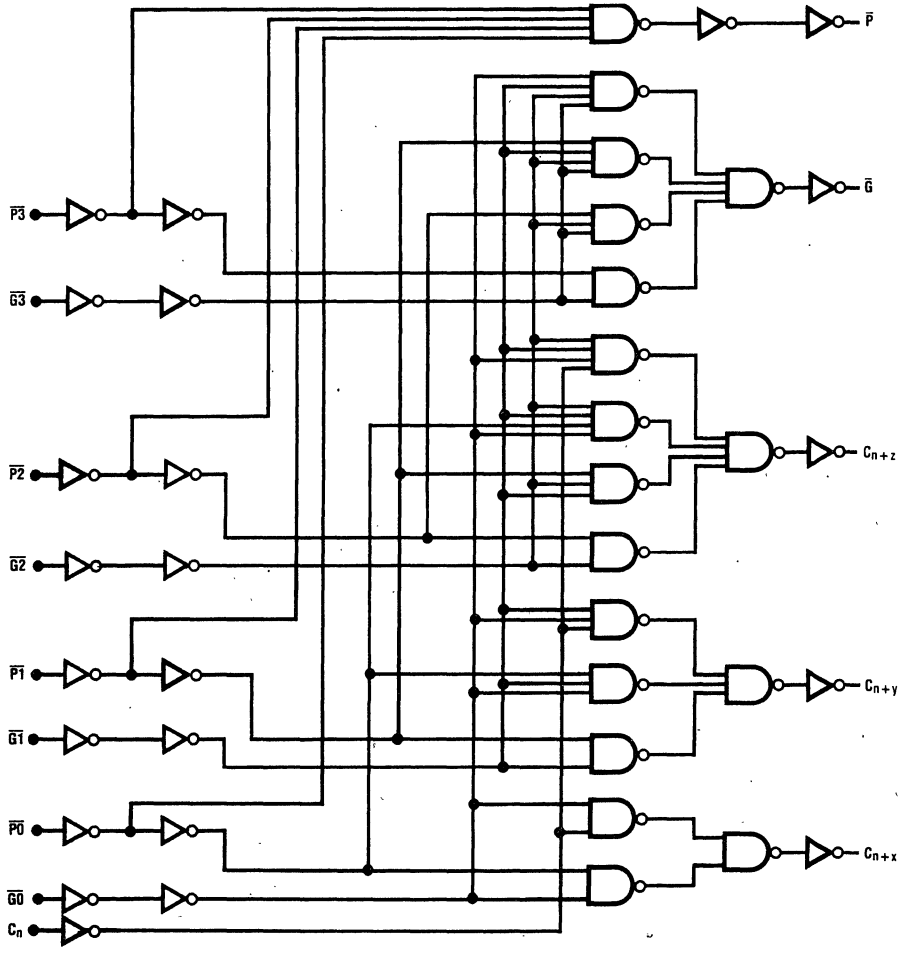
FUNCTION TABLE FOR C_{n+y} OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	C_n	C_{n+y}
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

H = high level L = low level X = irrelevant

Any inputs not shown in a given table are irrelevant with respect to that output.

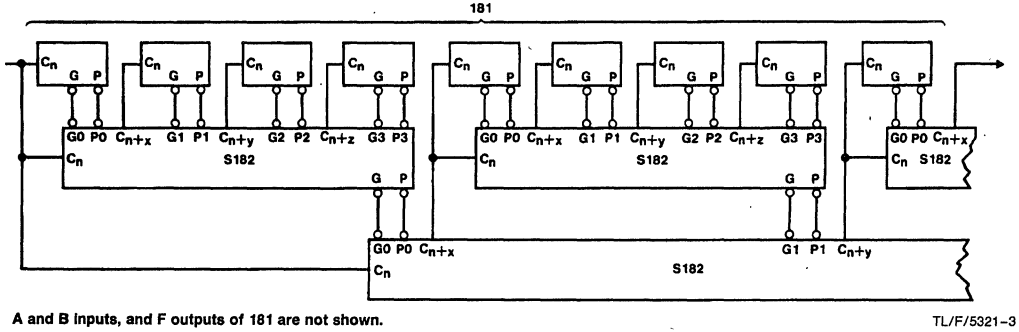
Logic Diagram



TL/F/5321–2

Typical Application

64-BIT ALU, FULL-CARRY LOOK AHEAD IN THREE LEVELS



A and B inputs, and F outputs of 181 are not shown.

TL/F/5321–3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC190/MM74HC190 Synchronous Decade Up/Down Counters with Mode Control MM54HC191/MM74HC191 Synchronous Binary Up/Down Counters with Mode Control

General Description

These high speed synchronous counters utilize micro-CMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL.

These circuits are synchronous, reversible, up/down counters. The MM54HC191/MM74HC191 are 4-bit binary counters and the MM54HC190/MM74HC190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

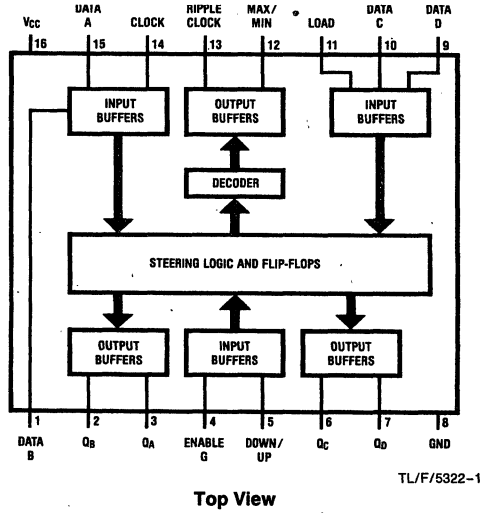
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Level changes on Enable or Down/Up can be made regardless of the level of the clock input
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5322–1

Top View

Load	Enable G	Down/ Up	Clock	Function
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Asynchronous inputs Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

Order Number MM54HC190J, MM54HC191J, MM74HC190J, N or MM74HC191J, N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency				40		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		30		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		27		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock		16		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		24		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		30		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		29		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		22		ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	Enable	Ripple Clock		22		ns
t_W	Minimum Clock, Clear or Load Input Pulse Width				10		ns
t_S	Minimum Setup Time	Data	Clock				ns
t_H	Minimum Hold Time	Clock	Data				ns
t_S	Minimum Setup Time	Down/Up	Clock				ns
t_H	Minimum Hold Time	Clock	Down/Up				ns
t_S	Minimum Setup Time	Enable	Clock				ns
t_H	Minimum Hold Time	Clock	Enable				ns
t_S	Minimum Setup Time Load Inactive to Clock						ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
						Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency				2.0V 4.5V 6.0V	10 38 40			MHz MHz MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		2.0V 4.5V 6.0V	106 32 29			ns ns ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		2.0V 4.5V 6.0V	93 28 25			ns ns ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock		2.0V 4.5V 6.0V	62 18 16			ns ns ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		2.0V 4.5V 6.0V	90 27 24			ns ns ns

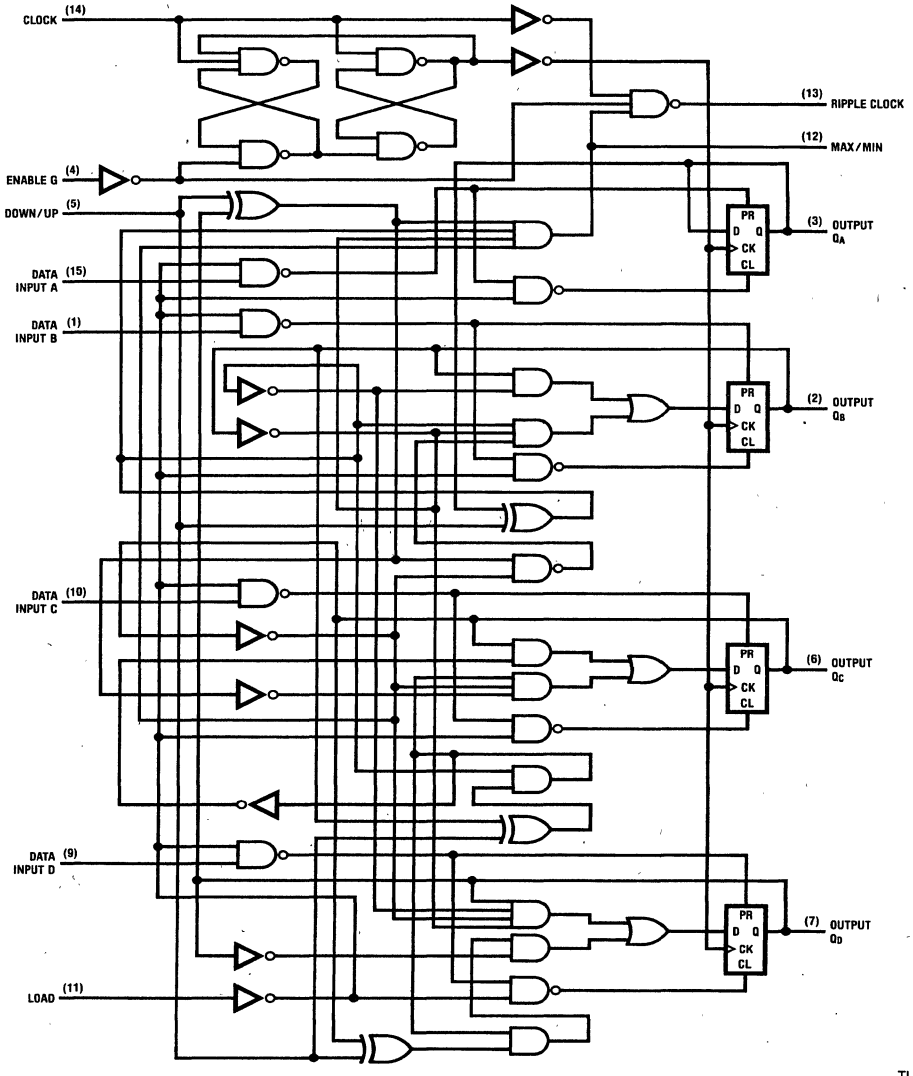
AC Electrical Characteristics (Continued)

Symbol	Parameter	From (Input)	To (Output)	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$		54HC $T_A = -55$ to $125°C$		Units
						Typ	Guaranteed Limits				
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		2.0V	108					ns
					4.5V	33					ns
					6.0V	30					ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		2.0V	98					ns
					4.5V	30					ns
					6.0V	28					ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		2.0V	85					ns
					4.5V	25					ns
					6.0V	23					ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	Enable	Ripple Clock		2.0V	85					ns
					4.5V	25					ns
					6.0V	23					ns
t_W	Minimum Clock, Load or Clear Input Pulse Width				2.0V						ns
					4.5V						ns
					6.0V						ns
t_S	Minimum Setup Time	Data	Clock		2.0V	20					ns
					4.5V	10					ns
					6.0V	8					ns
t_H	Data Hold Time				2.0V						ns
					4.5V						ns
					6.0V						ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time				2.0V						s
					4.5V						ns
					6.0V						ns
t_r, t_f	Maximum Input Rise and Fall Time				2.0V						ns
					4.5V						ns
					6.0V						ns
C_{IN}	Input Capacitance					5	10	10			pF
C_{PD}	Power Dissipation Capacitance (Note 5)					100					pF
	Minimum Setup Time	Down/Up	Clock		2.0V						ns
					4.5V						ns
					6.0V						ns
	Minimum Hold Time	Clock	Down/Up		2.0V						ns
					4.5V						ns
					6.0V						ns
	Minimum Setup Time	Enable	Clock		2.0V						ns
					4.5V						ns
					6.0V						ns
	Minimum Hold Time	Clock	Enable		2.0V						ns
					4.5V						ns
					6.0V						ns
	Minimum Setup Time (Inactive)	Load	Clock		2.0V						ns
					4.5V						ns
					6.0V						ns

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagrams

'HC190 Decade Counters

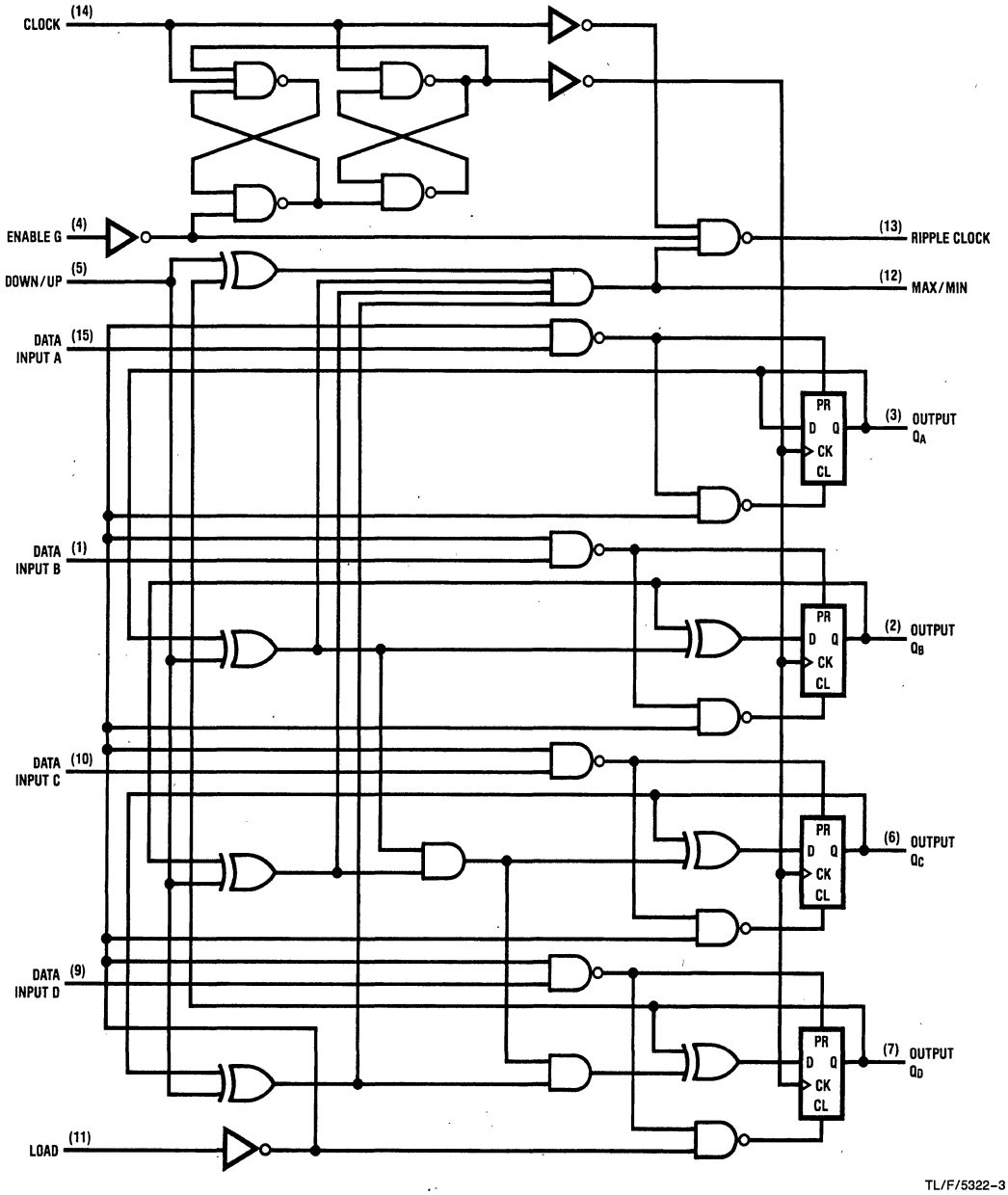


Pin (16) = V_{CC}, Pin (8) = GND

TL/F/5322–2

Logic Diagrams (Continued)

'HC191 Binary Counters

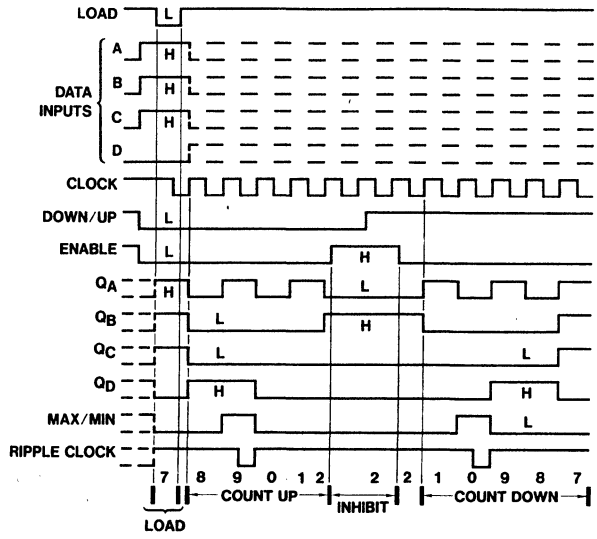


TL/F/5322–3

Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

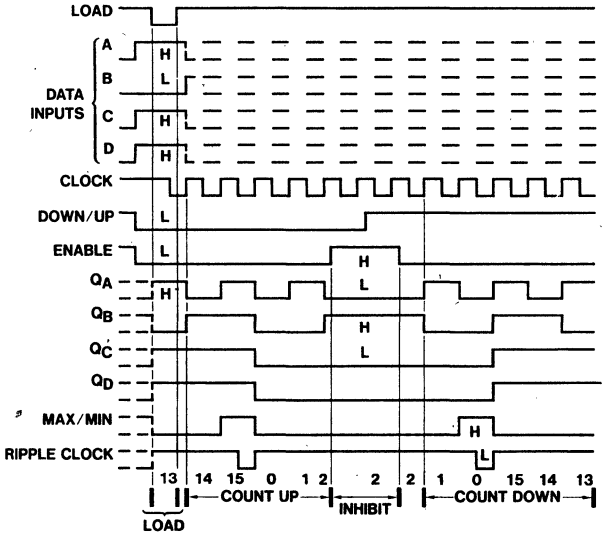
'HC190 Synchronous Decade Counters
Typical Load, Count, and Inhibit Sequences



TL/F/5322–4

Sequence:
(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one and two
(3) Inhibit
(4) Count down to one, zero, nine, eight, and seven

'HC191 Synchronous Binary Counters
Typical Load, Count, and Inhibit Sequence



TL/F/5322–5

Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

National Semiconductor

microCMOS

MM54HC192/MM74HC192 Synchronous Decade Up/Down Counters MM54HC193/MM74HC193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters utilize micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HC192/MM74HC192 is a decade counter, and the MM54HC193/MM74HC193 is a binary counter. Both counters have two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low to high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

These counters may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low the data is loaded independently of either clock input. This feature allows the counters to be used as divide-by-n counters by modifying the count length with the preset inputs.

In addition both counters can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counters can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

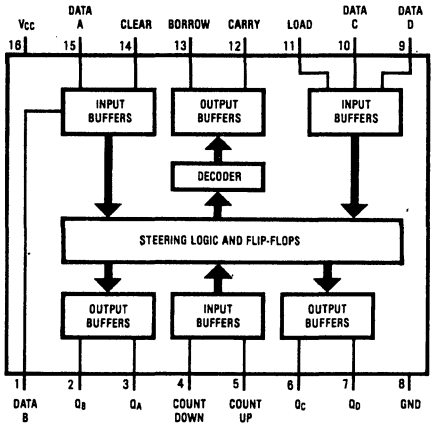
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, Count up to Q: 28 ns
- Typical operating frequency: 27 MHz
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 4 mA output drive

Connection Diagram

Dual-In-Line Package



TL/F/5011–1

Order Number MM54HC192J, MM54HC193J, MM74HC192J, N, or MM74HC193J, N
See NS Package J16A or N16E

Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = high level
L = low level
↑ = transition from low-to-high
X = don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	Conditions		Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency	Count Up		27	20	MHz
		Count Down		31	24	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry		17	26	ns
t_{PHL}	Maximum Propagation Delay High to Low			18	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Down to Borrow		16	24	ns
t_{PHL}	Maximum Propagation Delay High to Low			15	24	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q		28	40	ns
t_{PHL}	Maximum Propagation Delay High to Low			36	52	ns
t_{PLH}	Maximum Propagation Delay Low to High	Data or Load to Q		30	42	ns
t_{PHL}	Maximum Propagation Delay High to Low			40	55	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q		35	47	ns
t_W	Minimum Pulse Width	Clear	'HC192	40	52	ns
			'HC193	20	26	ns
		Load	'HC192	40	52	ns
			'HC193	10	20	ns
		Count Up/Down		15	22	ns
t_{SD}	Minimum Setup time	Data to Load		10	20	ns
t_{HD}	Minimum Hold Time			−3	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock			10	ns

AC Electrical Characteristics $V_{CC} = 2.0V$ to $6.0V$, $C_L = 50$ pF, $t_r = t_f = 6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency	Count Up	2.0V	5	3	2.5	2	MHz
			4.5V	25	18	14	12	MHz
			6.0V	29	20	16	13	MHz
		Count Down	2.0V	5	4	3	2	MHz
			4.5V	27	20	16	11	MHz
			6.0V	31	23	18	12	MHz
t_{PLH}	Maximum Propagation Delay Low to High	Count Up to Carry	2.0V	30	140	175	210	ns
			4.5V	13	28	35	42	ns
			6.0V	11	24	30	36	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	39	130	163	195	ns
			4.5V	16	26	33	39	ns
			6.0V	14	22	28	33	ns

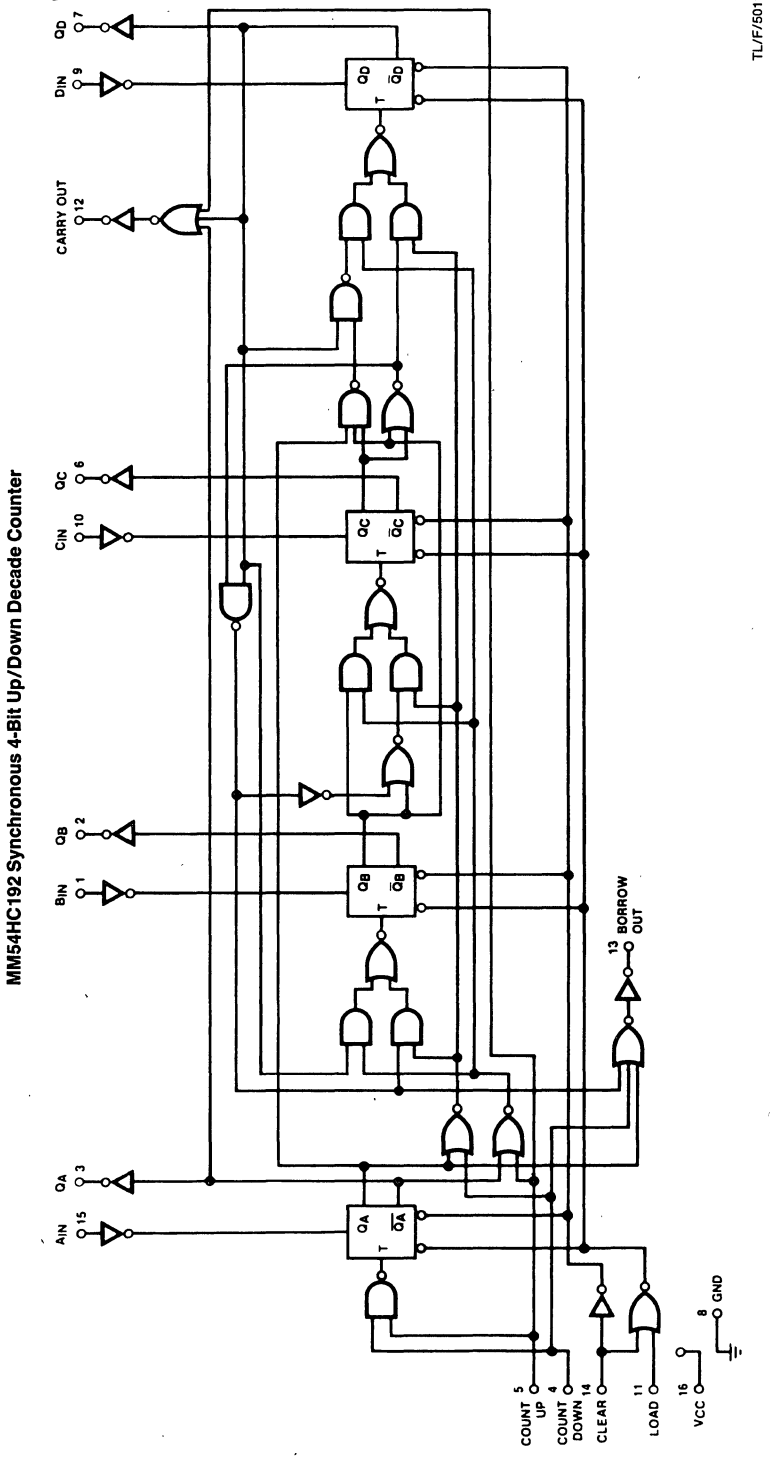
AC Electrical Characteristics (Continued) V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay	Count Down to Borrow	2.0V	39	130	163	195	ns
			4.5V	16	26	33	39	ns
			6.0V	14	22	28	33	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{PLH}	Maximum Propagation Delay Low to High	Count Up Or Down to Q	2.0V	77	215	269	323	ns
			4.5V	35	43	54	65	ns
			6.0V	30	37	46	55	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	95	275	344	413	ns
			4.5V	45	55	69	83	ns
			6.0V	38	47	59	71	ns
t_{PLH}	Maximum Propagation Delay Low to High	Data or Load to Q	2.0V	85	230	288	345	ns
			4.5V	37	46	58	69	ns
			6.0V	30	39	49	59	ns
t_{PHL}	Maximum Propagation Delay High to Low		2.0V	102	290	363	435	ns
			4.5V	47	58	73	87	ns
			6.0V	39	49	61	74	ns
t_{PHL}	Maximum Propagation Delay High to Low	Clear to Q	2.0V	85	265	331	398	ns
			4.5V	42	53	66	80	ns
			6.0V	38	45	56	68	ns
t_W	Minimum Pulse Width	Clear or Load 'HC192	2.0V	119	260	325	390	ns
			4.5V	42	52	65	78	ns
			6.0V	38	45	56	68	ns
		Load 'HC193	2.0V	31	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	26	ns
		Count Up/Down	2.0V	43	110	138	165	ns
			4.5V	17	22	28	33	ns
			6.0V	15	19	24	29	ns
		Clear 'HC193	2.0V	70	130	163	195	ns
			4.5V	21	26	33	39	ns
			6.0V	19	22	28	33	ns
t_{SD}	Minimum Setup Time	Data To Load	2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	22	25	ns
t_{HD}	Minimum Hold Time		2.0V	−30	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_{REM}	Minimum Removal Time	Clear Inactive to Clock	2.0V	−20	10	10	10	ns
			4.5V	−3	10	10	10	ns
			6.0V	−2	10	10	10	ns
t_r, t_f	Maximum Count Up or Down Input Rise & Fall Time		2.0V		500	500	500	ns
			4.5V		300	300	300	ns
			6.0V		200	200	200	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagrams

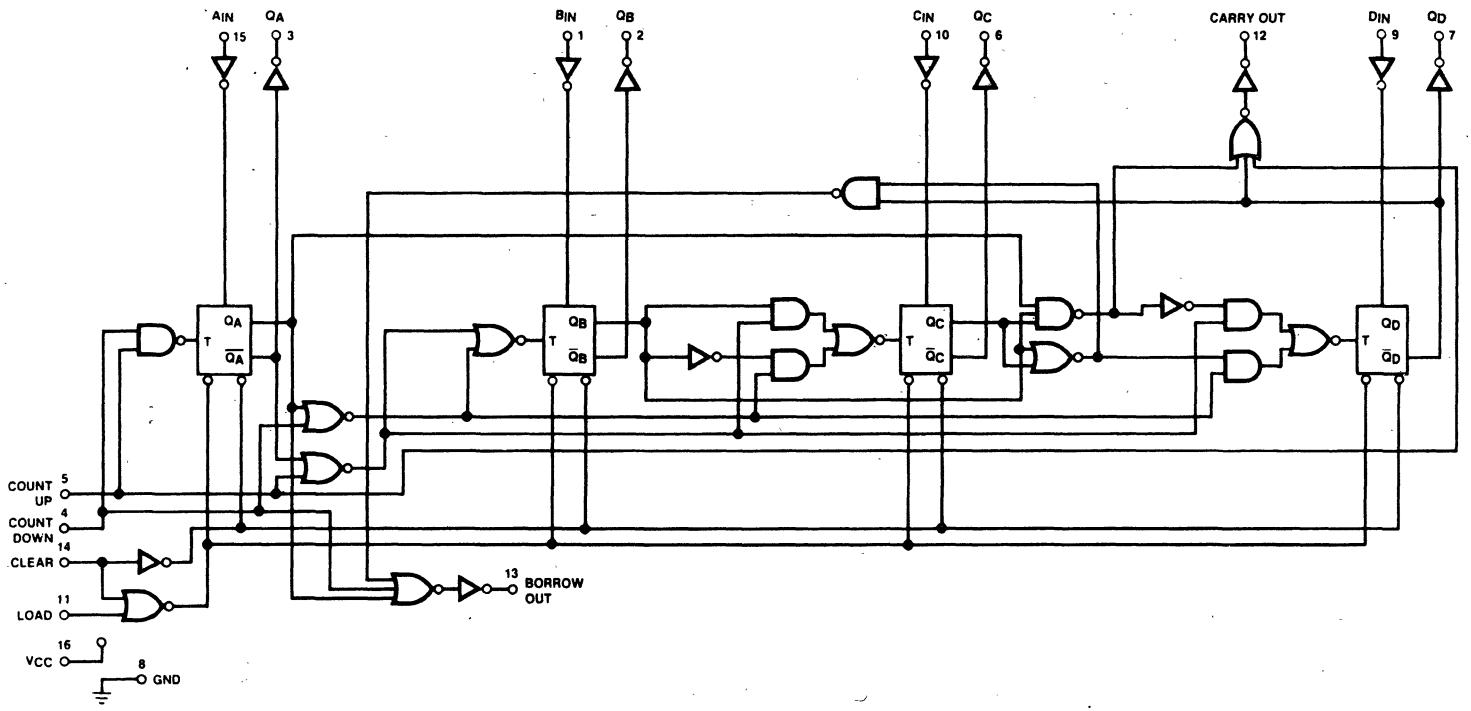
MM54HC192 Synchronous 4-Bit Up/Down Decade Counter



TL/F/5011–2

Logic Diagrams (Continued)

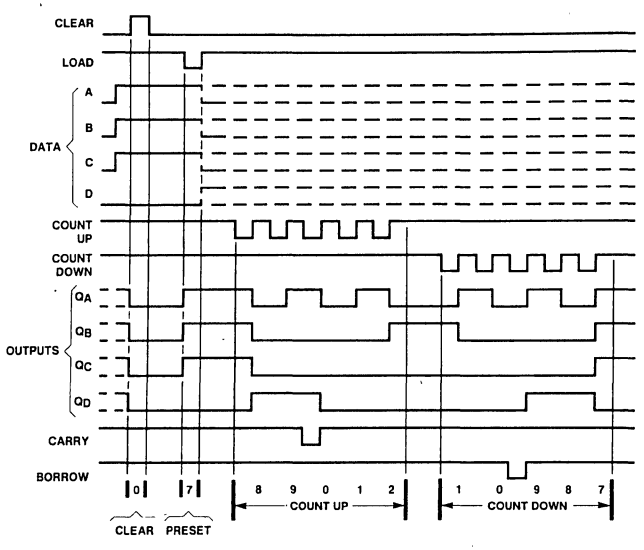
MM54HC193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/5011–3

Logic Waveforms

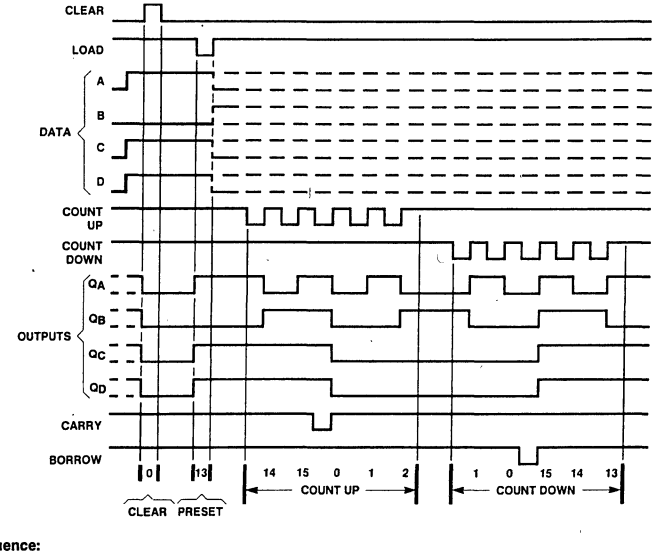
'HC192 Synchronous Decade Counters
Typical Clear, Load, and Count Sequences



TL/F/5011–4

Sequences:
(1) Clear outputs to zero
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

'HC193 Synchronous Binary Counters
Typical Clear, Load, and Count Sequences



TL/F/5011–5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.
Note A: Clear overrides load data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor

microCMOS

MM54HC194/MM74HC194
4-Bit Bidirectional Universal Shift Register

General Description

This 4-bit high speed bidirectional shift register utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads. This device operates at speeds similar to the equivalent low power Schottky part.

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register. It features parallel inputs, parallel outputs, right shift and left shift serial inputs, operating mode control inputs, and a direct overriding clear line. The register has four distinct modes of operation: PARALLEL (broadside) LOAD; SHIFT RIGHT (in the direction Q_A toward Q_D); SHIFT LEFT; INHIBIT CLOCK (do nothing).

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into their respective flip flops and appear at the outputs after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the SHIFT RIGHT data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the SHIFT LEFT serial input. Clocking of the flip flops is inhibited when both mode control inputs are low. The mode control inputs should be changed only when the CLOCK input is high.

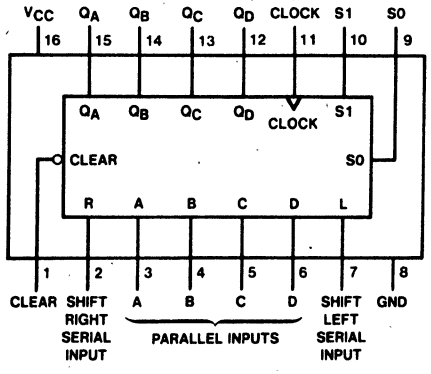
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent supply current: 160 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In Line Package



TL/F/5323–1

Order Number MM54HC194J or MM74HC194J, N
See NS Package J16A or N16E

Function Table

Inputs									Outputs			
Clear	Mode		Clock	Serial		Parallel						
	S1	S2		Left	Right	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

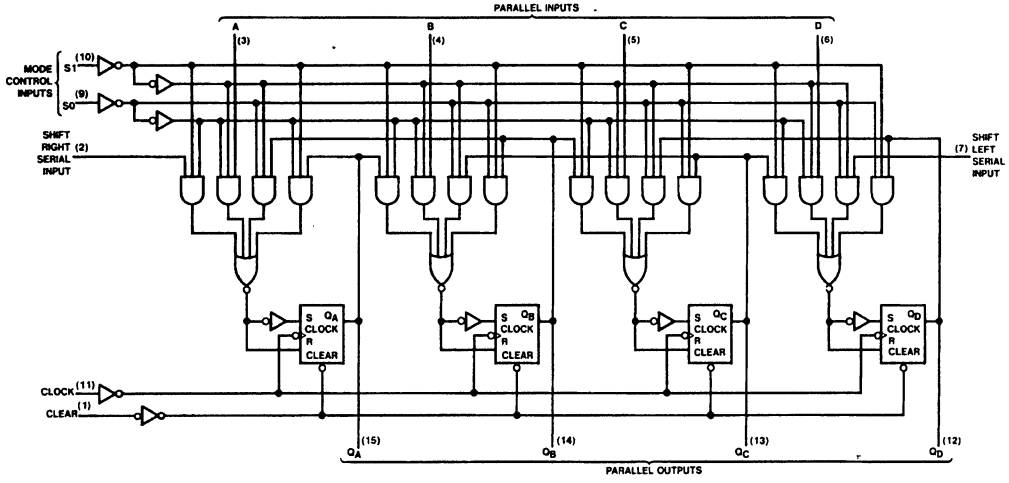
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		17	24	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		19	25	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock			5	ns
t_S	Minimum Setup Time (A, B, C, D to Clock)			20	ns
t_S	Minimum Setup Time Mode Controls to Clock			20	ns
t_W	Minimum Pulse Width Clock or Reset		9	16	ns
t_H	Minimum Hold Time any Input		−3	0	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

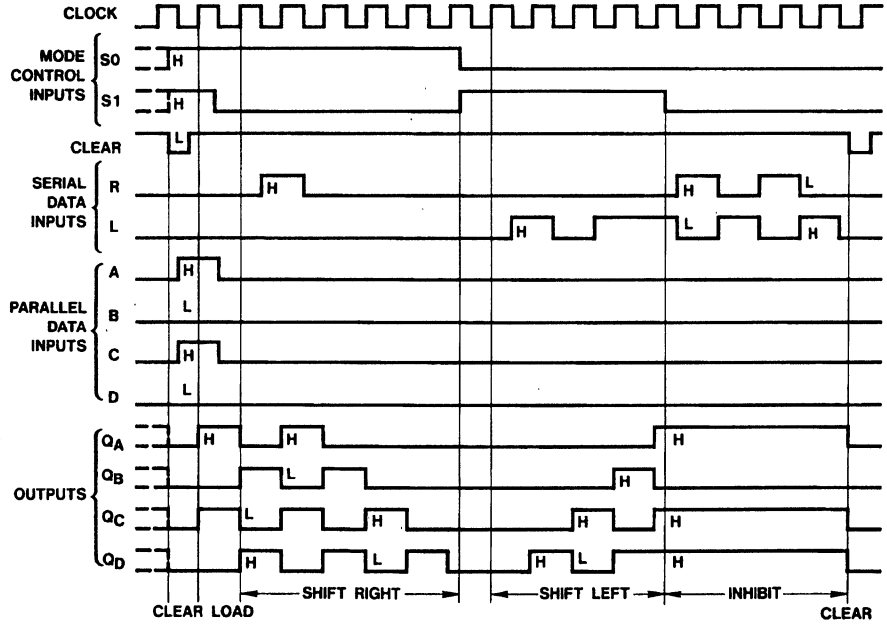
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V	70	145	183	216	ns
			4.5V	15	29	37	45	ns
			6.0V	12	25	31	37	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		2.0V	80	150	189	216	ns
			4.5V	15	30	37	45	ns
			6.0V	12	26	31	37	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_{REM}	Minimum Removal Time Reset Inactive to Clock		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_S	Minimum Set Up Time (A, B, C, or D to Clock)		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Set Time Mode Controls to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time any Input		2.0V	−10	0	0	0	ns
			4.5V	−3	0	0	0	ns
			6.0V	−3	0	0	0	ns
t_W	Minimum Pulse Width Clock or Reset		2.0V	30	80	100	120	ns
			4.5V	89	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic and Timing Diagrams



TL/F/5323–2



TL/F/5323–3

National Semiconductor

microCMOS

MM54HC195/MM74HC195 4-Bit Parallel Shift Register

General Description

The MM54HC195/MM74HC195 is a high speed 4-bit SHIFT REGISTER utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads at LS type speeds.

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, SHIFT/LOAD control input, and a direct overriding CLEAR. This shift register can operate in two modes: PARALLEL LOAD; SHIFT from Q_A towards Q_D.

Parallel loading is accomplished by applying the four bits of data, and taking the SHIFT/LOAD control input low. The data is loaded into the associated flip flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the SHIFT/LOAD control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or TOGGLE flip flop as shown in the truth table.

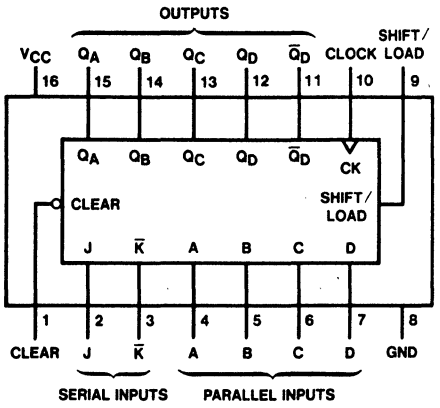
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency: 45 MHz
- Typical propagation delay: 16 ns (clock to Q)
- Wide operating supply voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5324–1

Top View

Order Number MM54HC195J or MM74HC195J,N
See NS Package J16A or N16E

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, Q_C, respectively, before the most-recent transition of the clock.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

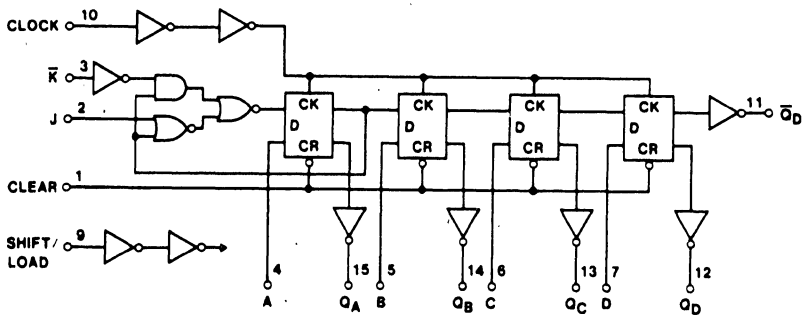
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		14	24	ns
t_{PHL}	Maximum Propagation Delay, Reset to Q		16	25	ns
t_{REM}	Minimum Removal Time, Shift/Load to Clock			0	ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock			5	ns
t_S	Minimum Setup Time, (A, B, C, D, J, $\overline{K}$ to Clock)			20	ns
t_S	Minimum Setup Time, Shift/Load to Clock			20	ns
t_W	Minimum Pulse Width Clock or Reset			16	ns
t_H	Minimum Hold Time, any Input except Shift/Load			0	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

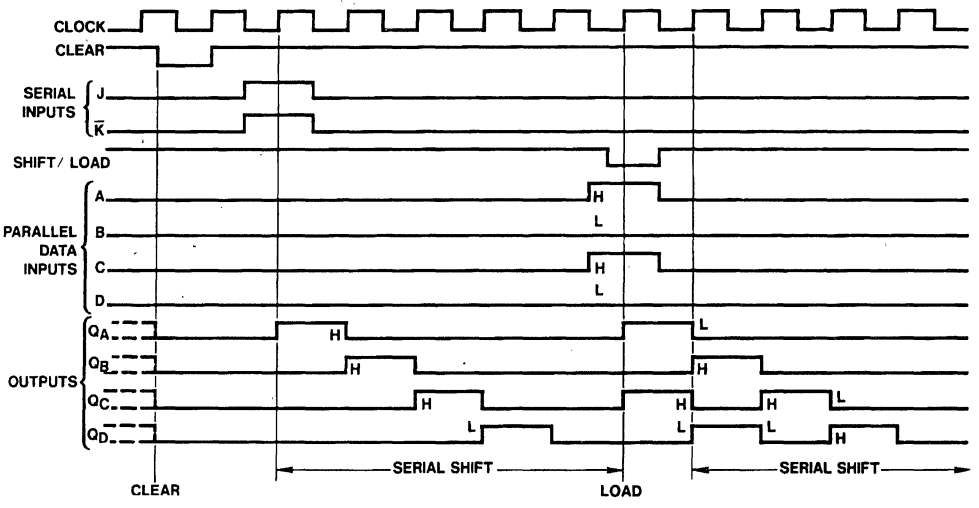
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V 4.5V 6.0V	10 45 50	6 30 35	5 24 28	4 20 24	MHz MHz MHz
t_{PHL}	Maximum Propagation Delay, Reset to Q		2.0V 4.5V 6.0V	70 15 12	150 30 26	189 38 32	224 45 38	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q		2.0V 4.5V 6.0V	70 15 12	145 29 25	183 37 31	216 43 37	ns ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
t_{REM}	Minimum Removal Time, Shift Load to Clock		2.0V 4.5V 6.0V	−2 −2 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_{REM}	Minimum Removal Time, Reset Inactive to Clock		2.0V 4.5V 6.0V		5 5 5	5 5 5	5 5 5	ns ns ns
t_S	Minimum Setup Time, (A, B, C, D, J, $\overline{K}$ to Clock)		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_S	Minimum Setup Time, Shift/Load to Clock		2.0V 4.5V 6.0V		100 20 17	125 25 21	150 30 25	ns ns ns
t_H	Minimum Hold Time any Input except Shift/Load		2.0V 4.5V 6.0V	−10 −2 −2	0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width, Clock or Reset		2.0V 4.5V 6.0V	30 10 9	80 16 14	100 20 18	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)			100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic and Timing Diagrams



TL/F/5324–2



TL/F/5324–3

National Semiconductor

microCMOS

MM54HC221A/MM74HC221A
Dual Non-Retriggerable Monostable Multivibrator

General Description

The MM54/74HC221A high speed monostable multivibrators (one shots) utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC221A can be triggered on the positive transition of the clear while A is held low and B is held high.

The 'HC221A is a non-retriggerable, and therefore cannot be retriggered until the output pulse times out.

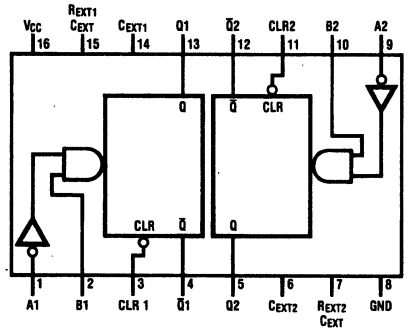
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})(C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: ±5% (typ)
- Schmitt Trigger A & B inputs enable infinite signal input rise or fall times

Connection Diagram

Dual-In-Line Package

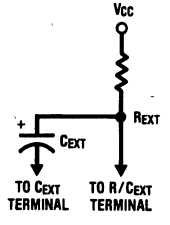


TL/F/5325–1

Top View

Order Number MM54HC221AJ or MM74HC221AJ, N
See NS Package J16A or N16E

Timing Component



TL/F/5325–2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎏
H	↓	H	⎍	⎏
↑	L	H	⎍	⎏

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎏ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Maximum Input Rise and Fall Time (Clear Input)			
V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN} = V_{CC} or GND	6.0V		±0.5	±5.0	±5.0	μA
I_{IN}	Maximum Input Current (all other pins)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (standby)	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable)	V_{IN} = V_{CC} or GND R/C_{EXT} = 0.5V_{CC}	2.0V	36	80	110	130	μA
			4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

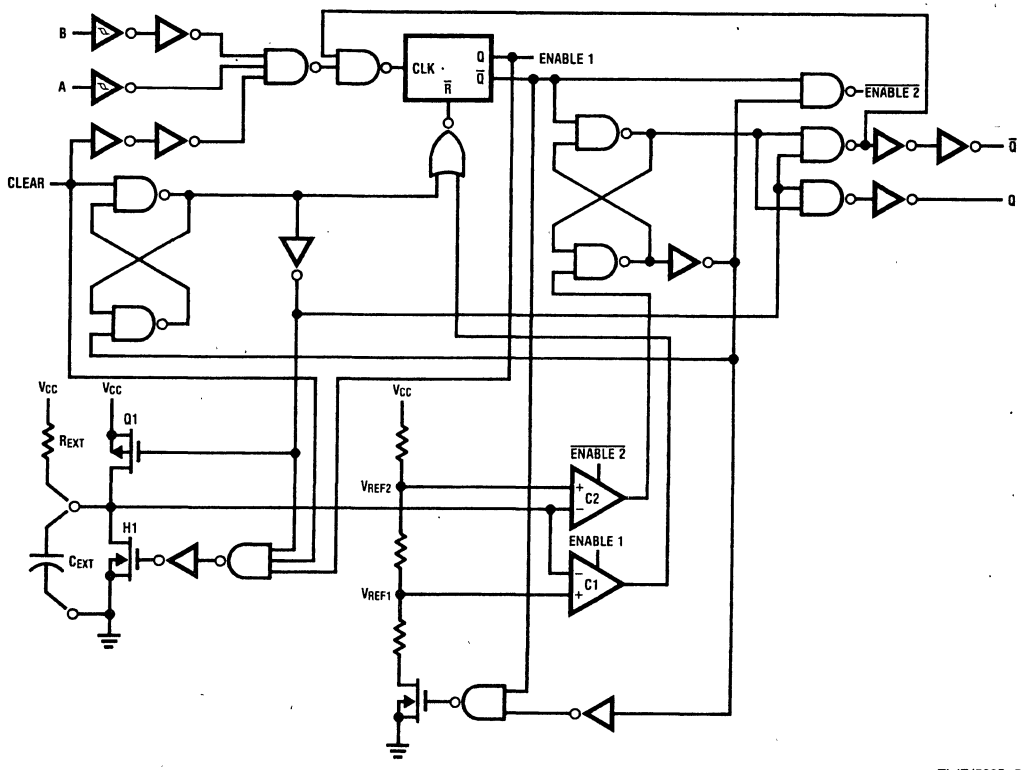
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q		22	36	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay Clear to Q		20	31	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns(unless otherwise specified)

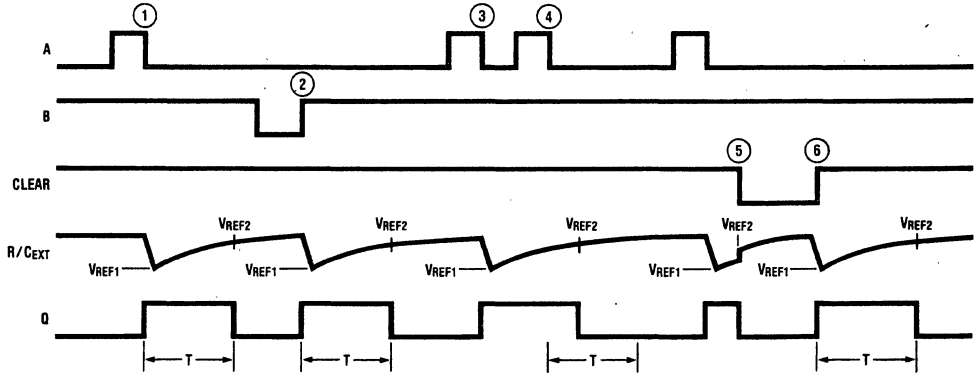
Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ	Guaranteed Limits		
t_{PLH}	Maximum Trigger Propagation Delay A, B or Clear to Q			2.0V	77	169	194	210	ns
				4.5V	26	42	51	57	ns
				6.0V	21	32	39	44	ns
t_{PHL}	Maximum Trigger Propagation Delay A, B or Clear to $\overline{Q}$			2.0V	88	197	229	250	ns
				4.5V	29	48	60	67	ns
				6.0V	24	38	46	51	ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V	54	114	132	143	ns
				4.5V	23	34	41	45	ns
				6.0V	19	28	33	36	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V	56	116	135	147	ns
				4.5V	25	36	42	46	ns
				6.0V	20	29	34	37	ns
t_W	Minimum Pulse Width A, B, Clear			2.0V	57	123	144	157	ns
				4.5V	17	30	37	42	ns
				6.0V	12	21	27	30	ns
t_{REM}	Minimum Clear Removal Time			2.0V		0	0	0	ns
				4.5V		0	0	0	ns
				6.0V		0	0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V	30	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ $R_{EXT}=6$ kΩ ($V_{CC}=2V$)		2.0V	1.5				μs
				4.5V	450				ns
				6.0V	380				ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	4.5V	1	0.9			ms
			Max	4.5	1	1.1			ms
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (other inputs)				6	10	10	10	pF

Logic Diagram



TL/F/5325–5

Theory of Operation



TL/F/5325–6

① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ NO RETRIGGERING
⑤ RESET PULSE SHORTENING
⑥ CLEAR TRIGGER

FIGURE 1

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC} ②). The 'HC221 can also be triggered when clear goes from GND to V_{CC} (while A is at Gnd and B is at V_{CC} ⑥).

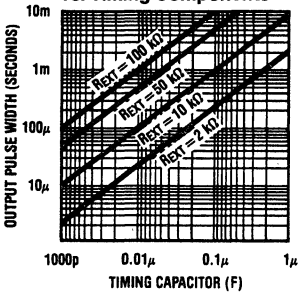
It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC221 is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

The 'HC221 is non-retriggerable and will ignore input transitions on A and B until it has timed out ③ and ④.

RESET OPERATION

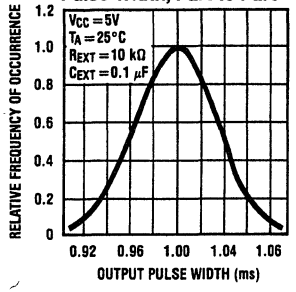
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



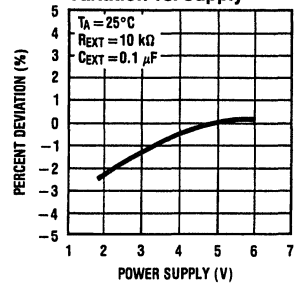
TL/F/5325–7

Typical Distribution of Output Pulse Width, Part to Part



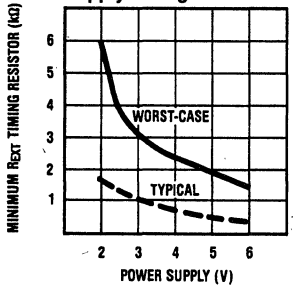
TL/F/5325–8

Typical 1ms Pulse Width Variation vs. Supply



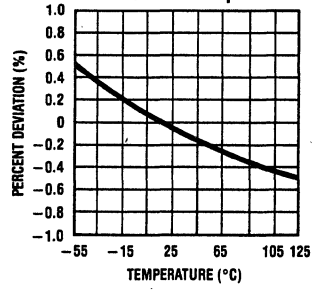
TL/F/5325–9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5325–10

Typical 1 ms Pulse Width Variation vs. Temperature



TL/F/5325–11

Note: R and C are not subjected to temperature. The C is polypropylene.

National Semiconductor

microCMOS

MM54HC237/MM74HC237
3-to-8 Line Decoder With Address Latches

General Description

These devices utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to implement a three-to-eight line decoder with latches on the three address inputs. When $\overline{GL}$ goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as $\overline{GL}$ remains high no address changes will be recognized. Output enable controls, G1 and $\overline{G2}$, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are low unless G1 is high and $\overline{G2}$ is low. The 'HC237 is ideally suited for the implementation of glitch-free decoders in stored-address applications in bus oriented systems.

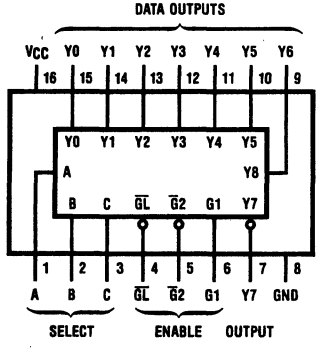
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide supply range: 2–6V
- Latched inputs for easy interfacing
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5326–1

Top View

Order Number MM54HC237J or MM74HC237J,N

See NS Package J16A or N16E

Truth Table

INPUTS						OUTPUTS							
ENABLE			SELECT										
$\overline{GL}$	G1	$\overline{G2}$	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	H	L	L	L	L
L	H	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	H	L	H	L	L	L	L	L	H	L	L
L	H	L	H	H	L	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Output corresponding to stored address, L; all others, H							

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		20	41	ns
t_{PLH}	Maximum Propagation Delay A, B or C to any Y Output		16	32	ns
t_{PLH}	Maximum Propagation $\overline{GL}$ to any Y Output		22	44	ns
t_{PHL}	Maximum Propagation Delay GL to any Y Output		17	33	ns
t_{PLH}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		16	35	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		14	25	ns
t_S	Minimum Set Up Time at A, B and C Inputs		10	20	ns
t_H	Minimum Hold Time at A, B and C Inputs		−3	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		9	16	ns

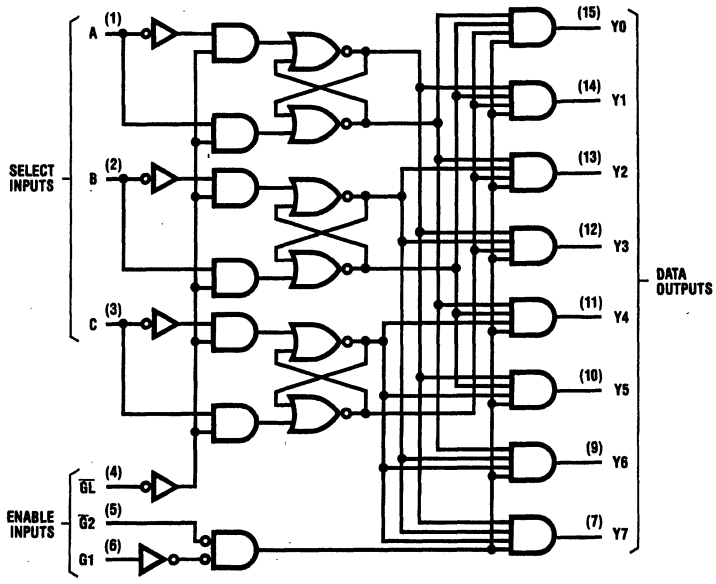
AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	100	235	296	350	ns
			4.5V	24	47	59	70	ns
			6.0V	20	40	50	60	ns
t_{PLH}	Maximum Propagation Delay, A, B or C to any Y Output		2.0V	80	185	233	276	ns
			4.5V	19	37	47	55	ns
			6.0V	17	31	40	47	ns
t_{PLH}	Maximum Propagation $\overline{GL}$ to any Y Output		2.0V	125	250	315	373	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	63	ns
t_{PHL}	Maximum Propagation Delay $\overline{GL}$ to any Y Output		2.0V	95	190	239	283	ns
			4.5V	19	38	48	75	ns
			6.0V	16	32	41	48	ns
t_{PLH}	Maximum Propagation Delay, G1 or $\overline{G2}$ to Output		2.0V	100	200	252	298	ns
			4.5V	20	40	50	60	ns
			6.0V	17	34	43	51	ns
t_{PHL}	Maximum Propagation Delay G1 or $\overline{G2}$ to Output		2.0V	73	145	183	216	ns
			4.5V	15	29	37	43	ns
			6.0V	12	25	31	37	ns
t_S	Minimum Set Up Time at A, B and C Inputs		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time at A, B and C Inputs		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Enabling Pulse at $\overline{GL}$		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			75				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

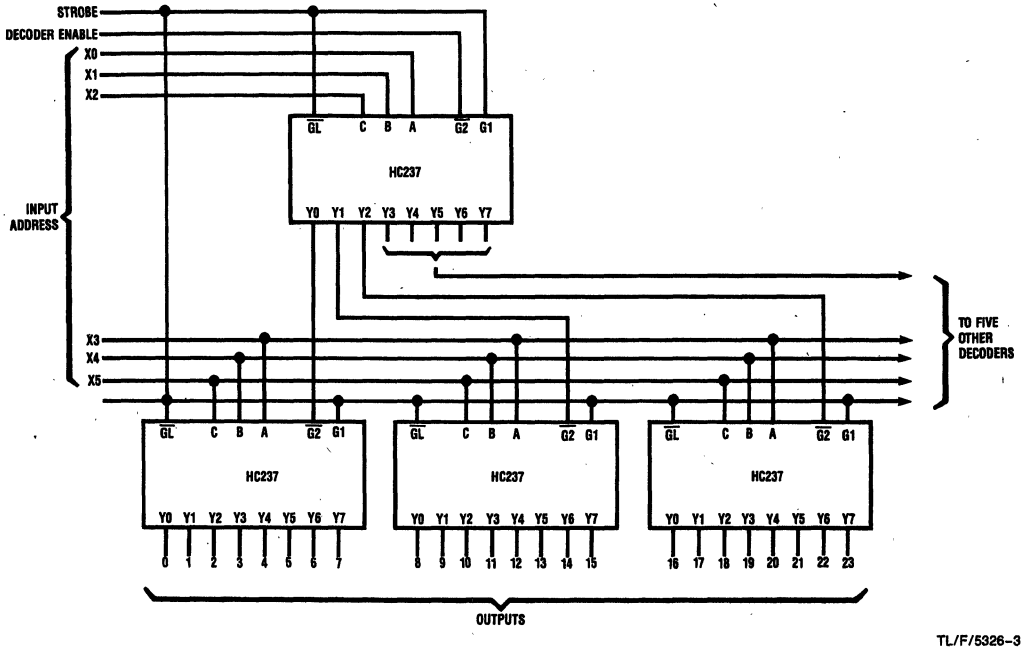
3

Functional Block Diagram



TL/F/5326–2

Typical Application



TL/F/5326–3

6-Line to 64-Line Decoder with Input Address Storage

National Semiconductor

PRELIMINARY

microCMOS

MM54HC240/MM74HC240 Inverting Octal TRI-STATE® Buffer MM54HC241/MM74HC241 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity and low power consumption. Each has a fanout of 15 LS-TTL equivalent inputs.

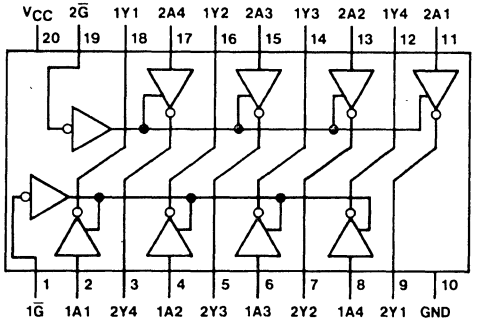
The MM54HC240/MM74HC240 is an inverting buffer and has two active low enables ($1\overline{G}$ and $2\overline{G}$). Each enable independently controls 4 buffers. MM54HC241/MM74HC241 is a non-inverting buffer that has one active low enable and one active high enable, each again controlling 4 buffers. Neither device has Schmitt trigger inputs.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

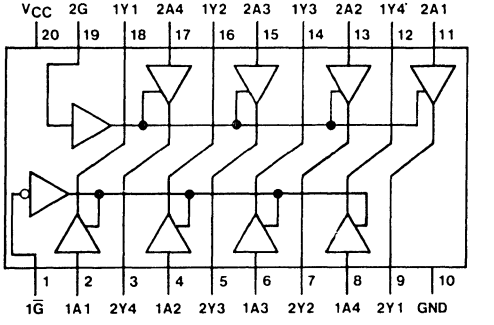
- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74 Series)
- Output current: 6 mA

Connection Diagrams Dual-In-Line Packages



TL/L/5020–1

Top View
Order Number MM54HC240J, MM74HC240J, N
See NS Package J20A or N20A



TL/L/5020–2

Top View
Order Number MM54HC241J, MM74HC241J, N
See NS Package J20A or N20A

Truth Tables

('HC240)

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

('HC241)

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL} V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}, G=V_{IL}	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC240/MM74HC240 $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ $C_L=45$ pF	14	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	$R_L=1$ kΩ $C_L=5$ pF	13	25	ns

AC Electrical Characteristics MM54HC240/MM74HC240

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	80	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	28	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable TIme	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	75	150	189	224	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$\overline{G}=V_{IH}$		12				pF
		$\overline{G}=V_{IL}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

AC Electrical Characteristics MM54HC241/MM74HC241 $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions		Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF		13	20	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	$R_L=1$ kΩ	$1\overline{G}$	17	28	ns
		$C_L=45$ pF	$2\overline{G}$	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Input	$R_L=1$ kΩ	$1\overline{G}$	15	25	ns
		$C_L=5$ pF	$2\overline{G}$	13	25	ns

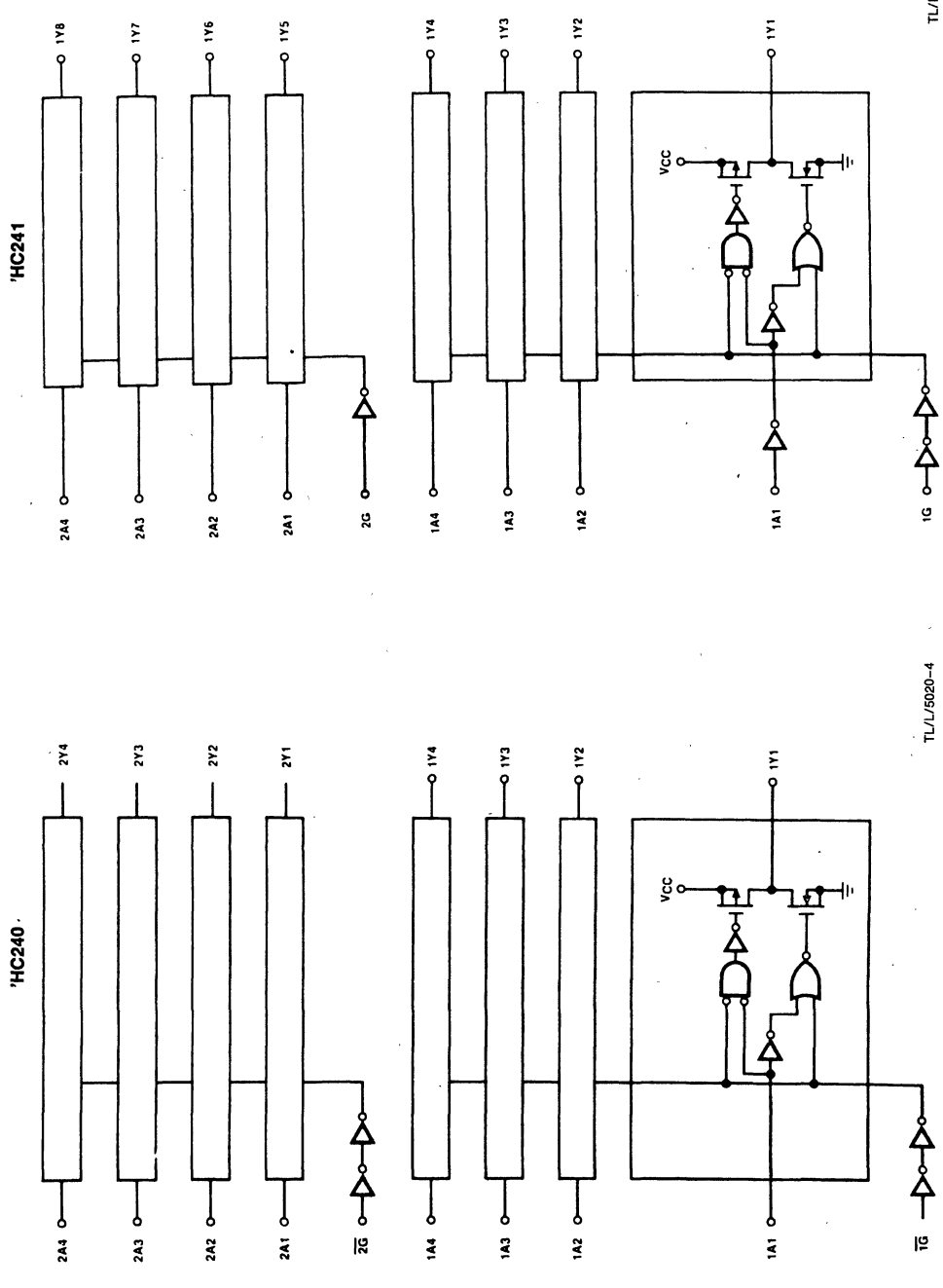
AC Electrical Characteristics MM54HC241/MM74HC241

$V_{CC}=2.0V$ to 6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	83	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	10	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	75	150	189	224	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer)						
		$G=V_{IL}$, $\overline{G}=V_{IH}$		12				pF
		$G=V_{IH}$, $\overline{G}=V_{IL}$		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Logic Diagrams



National Semiconductor

microCMOS

MM54HC242/MM74HC242 Inverting Quad TRI-STATE® Transceiver MM54HC243/MM74HC243 Quad TRI-STATE Transceiver

General Description

These TRI-STATE bidirectional inverting and non-inverting buffers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation when driving large bus capacitances. These circuits possess the low power dissipation and high noise immunity associated with CMOS circuits, but speeds comparable to low power Schottky TTL circuits. They can also drive 15 LS-TTL loads.

The MM54HC242/MM74HC242 is a non-inverting buffer and the MM54HC243/MM74HC243 is an inverting buffer. Each device has one active high enable (GBA), and one active low enable (GAB). GBA enables the A outputs and GAB enables the B outputs. This device does not have Schmitt trigger inputs.

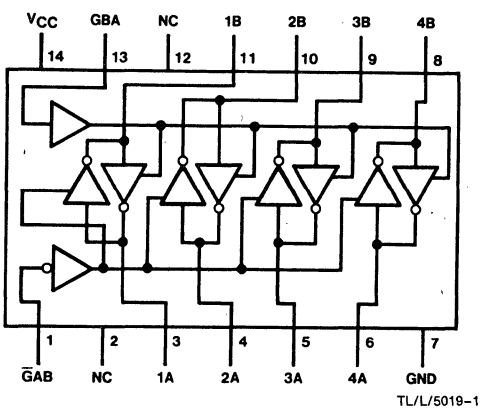
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs
- Two way asynchronous communication
- High output current: 6 mA (74HC)
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74HC)

Connection Diagrams

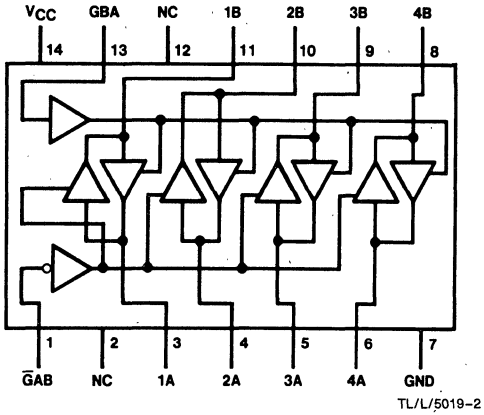
Dual-In-Line Package



TL/L/5019–1

Top View
Order Number MM54HC242J, MM74HC242J, N
See NS Package J14A or N14A

Dual-In-Line Package



TL/L/5019–2

Top View
Order Number MM54HC243J, MM74HC243J, N
See NS Package J14A or N14A

Truth Tables

'HC242

Control Inputs		Data Port Status	
$\overline{GAB}$	GBA	A	B
H	H	$\overline{OUTPUT}$	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	$\overline{OUTPUT}$

'HC243

Control Inputs		Data Port Status	
$\overline{GAB}$	GBA	A	B
H	H	OUTPUT	Input
L	H	Isolated	Isolated
H	L	Isolated	Isolated
L	L	Input	OUTPUT

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND $\overline{G}AB$=V_{IH}, GBA=V_{IL}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics (MM54HC242/MM74HC242)

V_{CC} = 5V, T_A = 25°C, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	12	18	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	R_L = 1kΩ C_L = 45 pF	17	28	ns
t_{PHZ}, t_{PHL}	Maximum Output Disable Time from Active Output	R_L = 1 kΩ C_L = 5 pF	15	25	ns

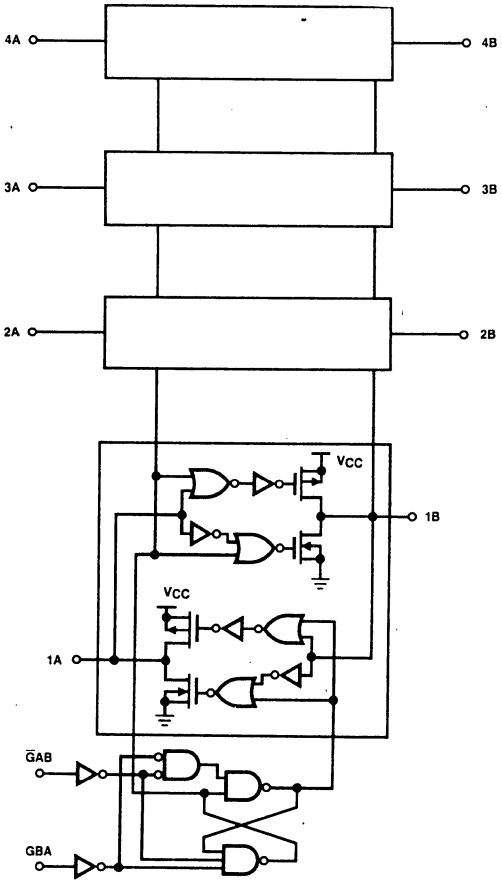
AC Electrical Characteristics (MM54HC242/MM74HC242, MM54HC243/MM74HC243)

V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	2.0V	55	100	126	149	ns
		C_L = 150 pF	2.0V	80	150	190	224	ns
		C_L = 50 pF	4.5V	12	20	25	30	ns
		C_L = 150 pF	4.5V	22	30	38	45	ns
		C_L = 50 pF	6.0V	11	17	21	25	ns
		C_L = 150 pF	6.0V	18	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time to Active Output	R_L = 1 kΩ C_L = 50 pF	2.0V	75	150	189	224	ns
		C_L = 150 pF	2.0V	100	200	252	298	ns
		C_L = 50 pF	4.5V	15	30	38	45	ns
		C_L = 150 pF	4.5V	30	40	50	60	ns
		C_L = 50 pF	6.0V	13	26	32	38	ns
		C_L = 150 pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from Active Output	R_L = 1 kΩ C_L = 50 pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer) $\overline{G} = V_{IH}$, $G = V_{IL}$ $\overline{G} = V_{IL}$, $G = V_{IH}$		12 50				pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

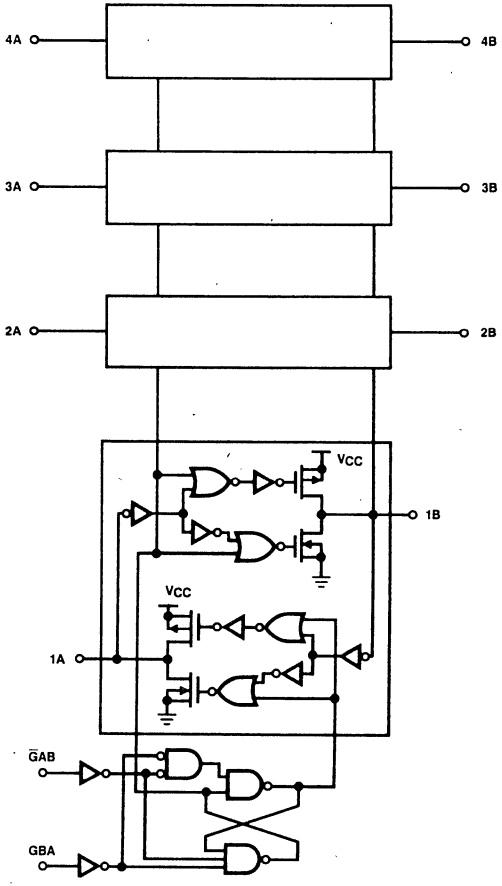
Logic Diagrams

MM54HC242/MM74HC242



TL/L/5019–3

MM54HC243/MM74HC243



TL/L/5019–4

National Semiconductor

microCMOS

MM54HC244/MM74HC244 Octal TRI-STATE® Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and are general purpose high speed non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. All three devices have a fanout of 15 LS-TTL equivalent inputs.

The MM54HC244/MM74HC244 is a non-inverting buffer and has two active low enables (1G and 2G). Each enable independently controls 4 buffers. This device does not have Schmitt trigger inputs.

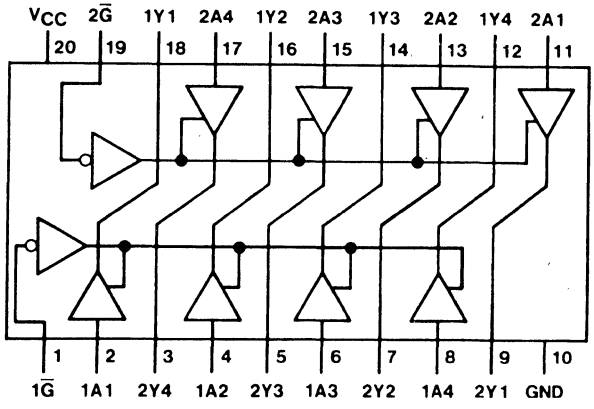
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent supply current: 80 μA (74 Series)
- Output current: 6 mA

Connection Diagram

Dual-In-Line Package



TL/F/5327–1

Top View

Order Number MM54HC244J or MM74HC244J,N
See NS Package J20A or N20A

Truth Table

'HC244

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\|$≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\|$≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH}, or V_{IL} V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC244/MM74HC244

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Enable Delay to Active Output	R_L = 1 kΩ C_L = 45 pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Delay from Active Output	R_L = 1 kΩ C_L = 5 pF	15	25	ns

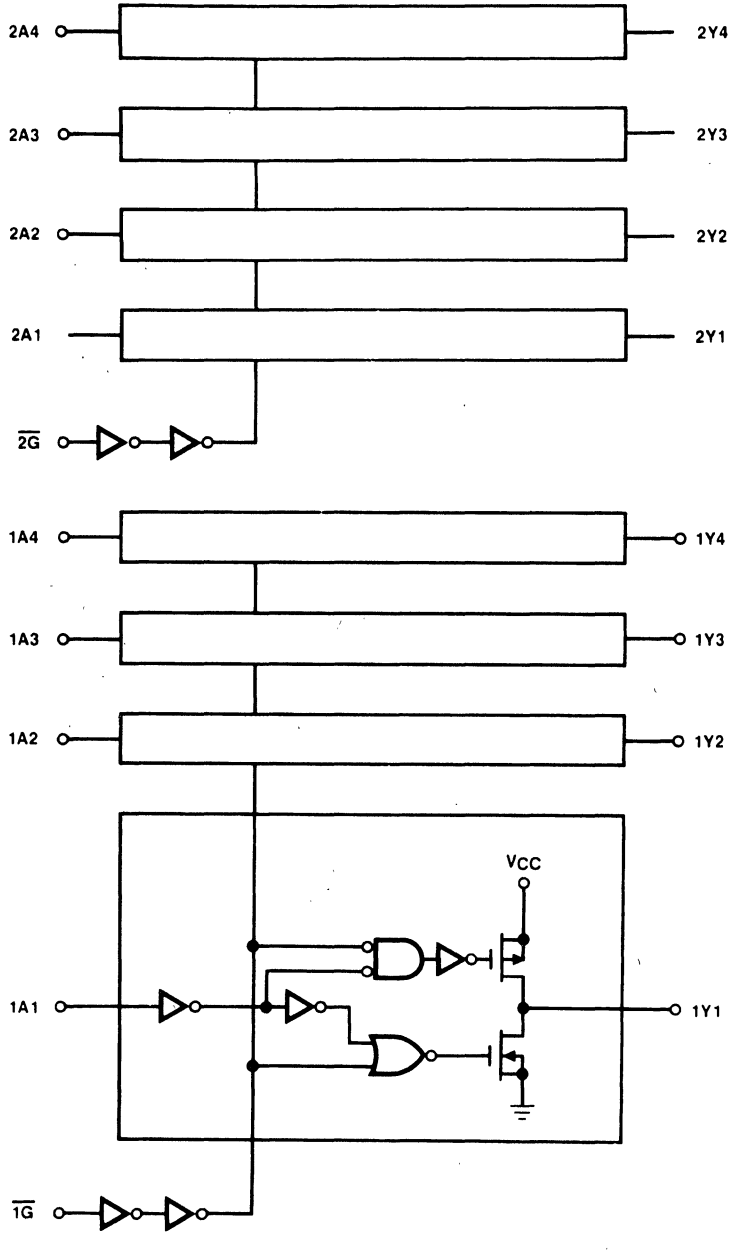
AC Electrical Characteristics $V_{CC}=2.0V$-$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	83	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	10	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	750	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer) $\overline{G}=V_{IH}$ $\overline{G}=V_{IL}$		12 50				pF pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram

'HC244



TL/F/5327–2

National Semiconductor

microCMOS

MM54HC245/MM74HC245 Octal TRI-STATE® Transceiver

General Description

This TRI-STATE bidirectional buffer utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and is intended for two-way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption and high noise immunity usually associated with CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device has an active low enable input $\overline{G}$ and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC245/MM74HC245 transfers true data from one bus to the other.

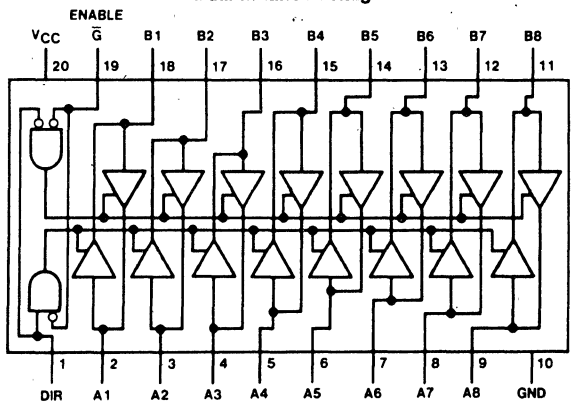
This device can drive up to 15 LS-TTL Loads, and does not have Schmitt trigger inputs. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74 HC)
- TRI-STATE outputs for connection to bus oriented systems
- High output drive: 6 mA (minimum)
- Same as the '645

Connection Diagram

Dual-In-Line Package



TL/F/5165–1

Top View

Order Number MM54HC245J or MM74HC245J, N
See NS Package J20A or N20A

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5 to V_{CC}+1.5V
DC Input/Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	V_{IN}=V_{CC} to GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable $\overline{G}$=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

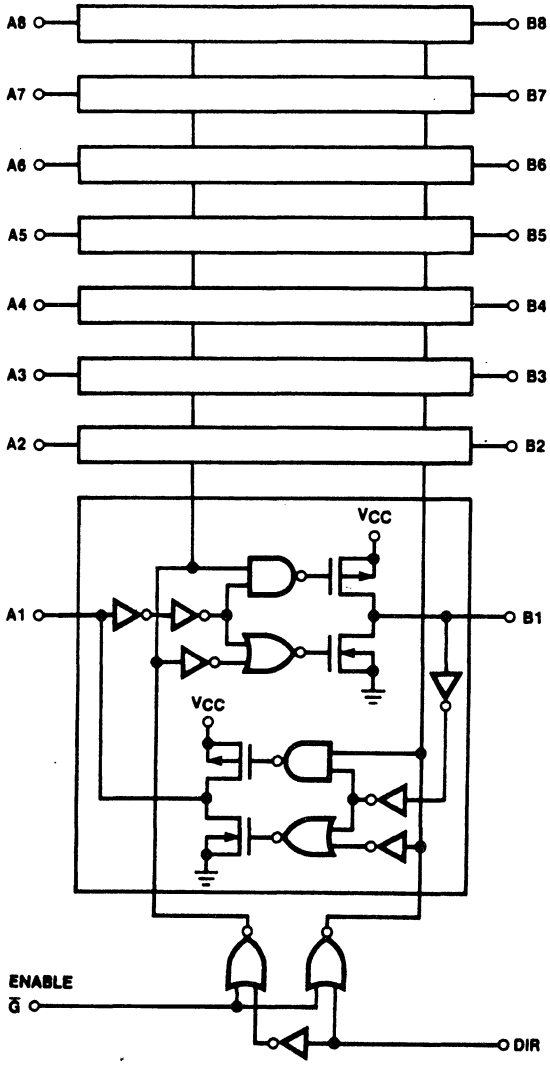
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	13	17	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 45 pF	33	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 5 pF	32	42	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	2.0V	29	72	88	96	ns
		C_L = 150 pF	2.0V	38	96	116	128	ns
		C_L = 50 pF	4.5V	14	18	22	24	ns
		C_L = 150 pF	4.5V	18	24	29	32	ns
		C_L = 50 pF	6.0V	14	18	22	24	ns
		C_L = 150 pF	6.0V	18	24	29	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	70	184	224	240	ns
		C_L = 150 pF	2.0V	80	216	260	284	ns
		C_L = 50 pF	4.5V	35	46	56	60	ns
		C_L = 150 pF	4.5V	41	54	65	71	ns
		C_L = 50 pF	6.0V	31	41	50	54	ns
		C_L = 150 pF	6.0V	36	47	57	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0V	47	172	208	224	ns
			4.5V	33	43	52	56	ns
			6.0V	31	41	50	54	ns
t_{TLH}, t_{THL}	Output Rise and Fall Time	C_L = 50 pF	2.0V	20	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G}=V_{IL}$		100				pF
		$\overline{G}=V_{IH}$		12				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5165–2

National Semiconductor

microCMOS

MM54HC251/MM74HC251
8-Channel TRI-STATE® Multiplexer

General Description

This 8-channel digital multiplexer with TRI-STATE outputs utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Along with the high noise immunity and low power consumption of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The large output drive capability and TRI-STATE feature make this part ideally suited for interfacing with bus lines in a bus oriented system.

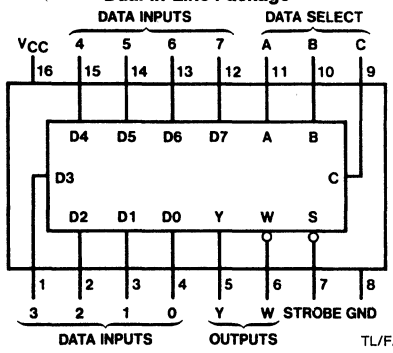
This multiplexer features both true (Y) and complement (W) outputs as well as a STROBE input. The STROBE must be at a low logic level to enable this device. When the STROBE input is high, both outputs are in the high impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and W outputs. The 54HC/74HC logic family is speed, function, as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay
  Data select to Y: 26 ns
- Wide supply range: 2–6V
- Low power supply quiescent current: 80 μA maximum (74HC)
- TRI-STATE outputs for interface to bus oriented systems

Connection and Logic Diagrams

Dual-In-Line Package



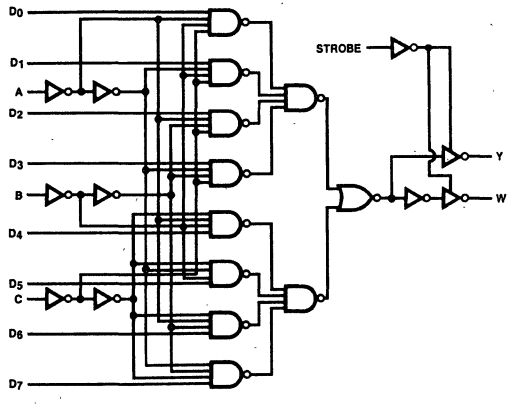
Top View

Order Number MM54HC251J or MM74HC251J, N
See NS Package J16A or N16E

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high logic level, L = logic level
X = irrelevant, Z = high impedance (off)
D0, D1 . . . D7 = the level of the respective D input



Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Leakage Current	Strobe=V_{CC} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		27	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to Y		22	29	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Any D to W		24	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, W Output	$R_L=1k$ $C_L=50$ pF	19	27	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, Y Output	$R_L=1k$ $C_L=50$ pF	19	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1k$ $C_L=5$ pF	26	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1k$ $C_L=5$ pF	27	35	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay A, B or C to Y		2.0V	90	205	256	300	ns
			4.5V	31	41	51	60	ns
			6.0V	26	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A, B or C to W		2.0V	95	205	256	300	ns
			4.5V	32	41	51	60	ns
			6.0V	27	35	44	51	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to Y		2.0V	70	195	244	283	ns
			4.5V	27	39	49	57	ns
			6.0V	23	33	41	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any D to W		2.0V	75	185	231	268	ns
			4.5V	29	37	46	54	ns
			6.0V	25	32	40	46	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time W Output	$R_L=1k$	2.0V	45	150	188	218	ns
			4.5V	21	30	38	44	ns
			6.0V	18	26	33	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output	$R_L=1k$	2.0V	45	145	181	210	ns
			4.5V	21	29	36	42	ns
			6.0V	18	25	31	36	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time W Output	$R_L=1k$	2.0V	60	220	275	319	ns
			4.5V	29	44	55	64	ns
			6.0V	25	37	46	54	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output	$R_L=1k$	2.0V	60	195	244	283	ns
			4.5V	30	39	49	57	ns
			6.0V	26	33	41	48	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		110				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC253/MM74HC253
Dual 4-Channel TRI-STATE® Multiplexer

General Description

The MM54HC253/MM74HC253 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the capability to drive 10 LS-TTL loads. The large output drive and TRI-STATE features of this device make it ideally suited for interfacing with bus lines in bus organized systems. When the output control input is taken high, the multiplexer outputs are sent into a high impedance state.

When the output control is held low, the associated multiplexer chooses the correct output channel for the given input signals determined by the select A and B inputs.

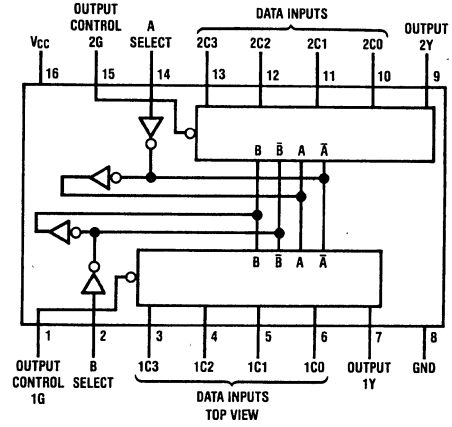
The 54HC/74HC logic family is functionally and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 24 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5108–1

Order Number MM54HC253J or MM74HC253J, N
See NS Package J16A or N16E

Truth Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = high level, L = low level, X = irrelevant, Z = high impedance (off).

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	Strobe=V_{CC} $V_{OUT}=V_{CC}$ or GND	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns, $C_L=15$ pF

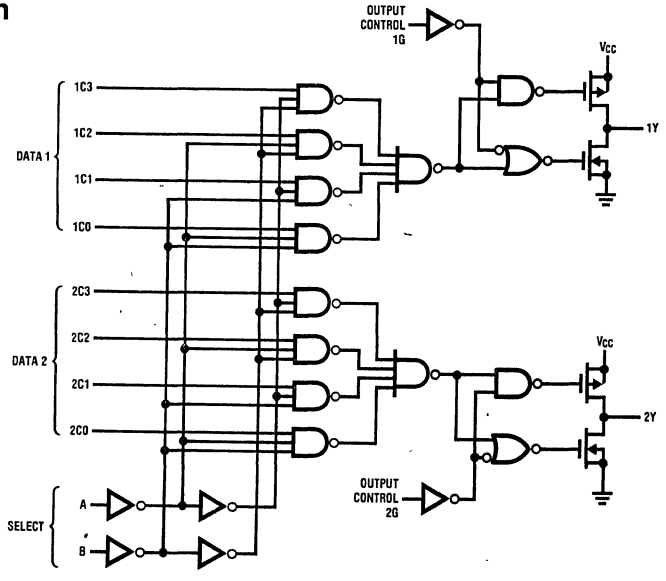
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		24	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		18	23	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time Y Output to a Logic Level	$R_L=1k$	13	18	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time Y Output to High Impedance State	$R_L=1k$	18	27	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select A or B to Y		2.0V	131	198	237	ns
			4.5V	29	44	53	ns
			6.0V	24	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any Data to Y		2.0V	99	158	189	ns
			4.5V	22	35	42	ns
			6.0V	19	29	35	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ	2.0V	63	113	135	ns
			4.5V	14	25	30	ns
			6.0V	12	21	26	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	90	169	203	ns
			4.5V	20	38	45	ns
			6.0V	17	31	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	95	110	ns
			4.5V	8	19	22	ns
			6.0V	7	13	16	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Outputs Enabled		90			pF
		Outputs Disabled		25			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5108–2

National Semiconductor

microCMOS

MM54HC257/MM74HC257
Quad 2-Channel TRI-STATE® Multiplexer

General Description

This QUAD 2-TO-1 line data selector/multiplexer utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive LS-TTL loads. The large output drive capability coupled with the TRI-STATE feature make this device ideal for interfacing with bus lines in a bus organized system. When the OUTPUT CONTROL input line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the OUTPUT CONTROL line is low, the SELECT input chooses whether the A or B input is used.

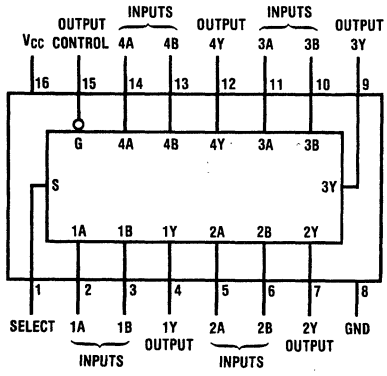
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- TRI-STATE outputs for connection to system buses.

Connection and Logic Diagrams

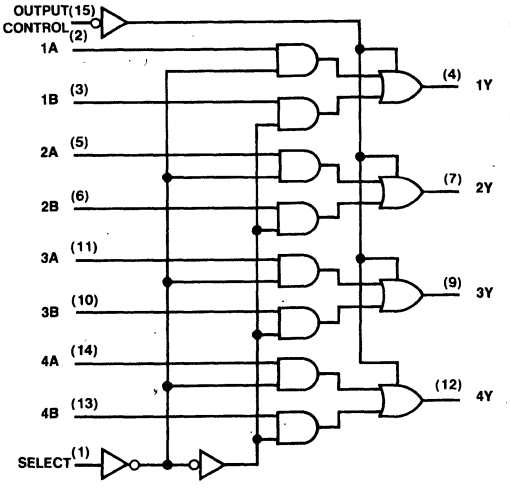
Dual-In-Line Package



TL/F/5329–1

Top View

Order Number MM54HC257J or MM74HC257J, N
See NS Package J16A or N16E



TL/F/5329–2

Truth Table

Inputs				
Output Control	Select	A	B	Output Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT}=V_{CC} or GND OC=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Y Output	$C_L=45$ pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L=50$ pF	13	21	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L=1$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L=1$ kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Y Output	$C_L=50$ pF	2.0V	50	100	125	150	ns
		$C_L=150$ pF	2.0V	70	150	189	224	ns
		$C_L=50$ pF	4.5V	10	20	25	30	ns
		$C_L=150$ pF	4.5V	15	30	38	45	ns
		$C_L=50$ pF	6.0V	9	17	21	25	ns
		$C_L=150$ pF	6.0V	13	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Y Output	$C_L=50$ pF	2.0V	50	100	125	150	ns
		$C_L=150$ pF	2.0V	70	150	190	221	ns
		$C_L=50$ pF	4.5V	10	20	29	30	ns
		$C_L=150$ pF	4.5V	15	30	38	45	ns
		$C_L=50$ pF	6.0V	10	17	21	25	ns
		$C_L=150$ pF	6.0V	17	26	32	38	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time, any Y Output to a Logic Level	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, any Y Output to a High Impedance State	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per mux)						
		Enable		30				pF
		Disabled		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC259/MM74HC259
8-Bit Addressable Latch/3-to-8 Line Decoder

General Description

This device utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to implement an 8-bit addressable latch, designed for general purpose storage applications in digital systems.

The MM54HC259/MM74HC259 has a single data input (D), 8 latch outputs (Q1–Q8), 3 address inputs (A, B, and C), a common enable input (E), and a common CLEAR input. To operate this device as an addressable latch, data is held on the D input, and the address of the latch into which the data is to be entered is held on the A, B, and C inputs. When ENABLE is taken low the data flows through to the addressed output. The data is stored when ENABLE transitions from low to high. All unaddressed latches will remain unaffected. With enable in the high state the device is deselected, and all latches remain in their previous state, unaffected by changes on the data or address inputs. To eliminate the possibility of entering erroneous data into the latches, the enable should be held high (inactive) while the address lines are changing.

If enable is held high and CLEAR is taken low all eight latches are cleared to a low state. If enable is low all latches except the addressed latch will be cleared. The addressed latch will instead follow the D input, effectively implementing a 3-to-8 line decoder.

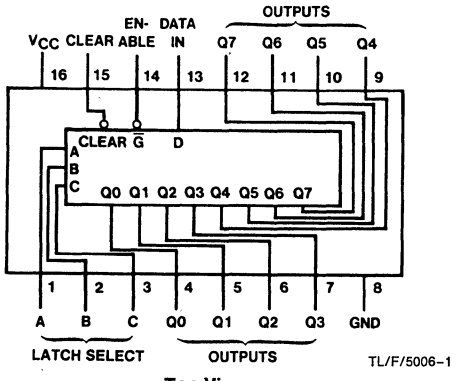
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide supply range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)

Connection Diagram

Dual-In-Line Package



Top View

Order Number MM54HC259J or MM74HC259J,N
See NS Package J16A or N16E

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = high level, L = low level

D = the level at the data input

Q_{i0} the level of Q_i (i = 0, 1 . . . 7, as appropriate) before the indicated steady-state input conditions were established.

Truth Table

Inputs		Outputs of Addressed Latch	Each Other Output	Function
Clear	$\overline{G}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Decoder
L	H	L	L	Clear

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics (V_{CC} = 5.0V, T_A = 25°C, $t_r = t_f$ = 6 ns, C_L = 15 pF unless otherwise specified.)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		18	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		20	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		20	35	ns
t_{PHL}	Maximum Propagation Delay Clear to Output		17	27	ns
t_W	Minimum Enable Pulse Width		10	16	ns
t_W	Minimum Clear Pulse Width		10	16	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	ns
t_S	Minimum Setup Time Select or Data to Enable		15	20	ns
t_H	Minimum Hold Time Data or Address to Enable		−2	0	ns

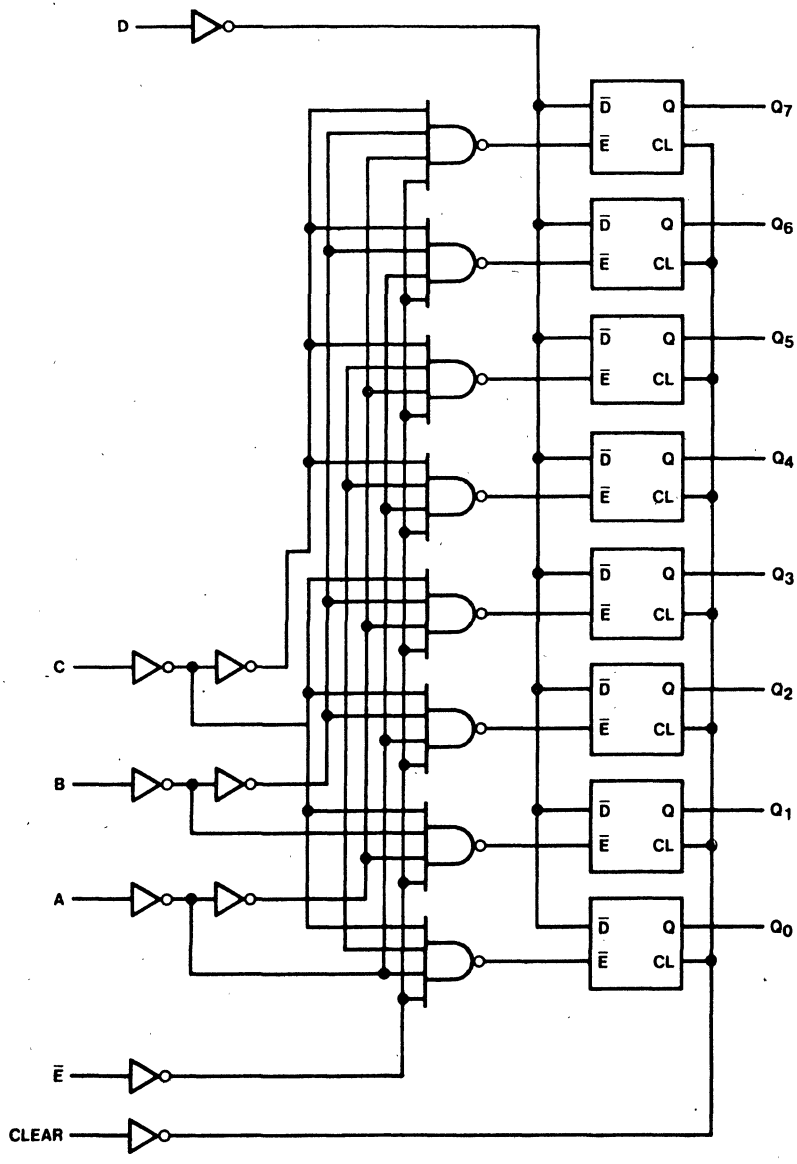
AC Electrical Characteristics $t_r = t_f$ = 6 ns, C_L = 50 pF, V_{CC} = 2.0V–6.0V

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		2.0V	60	180	225	250	ns
			4.5V	19	37	46	52	ns
			6.0V	17	32	40	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Select to Output		2.0V	72	220	275	310	ns
			4.5V	21	43	54	60	ns
			6.0V	18	37	46	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable to Output		2.0V	65	200	250	280	ns
			4.5V	27	40	50	58	ns
			6.0V	23	35	44	50	ns
t_{PHL}	Maximum Propagation Delay Clear to Output		2.0V	50	150	190	210	ns
			4.5V	18	31	39	44	ns
			6.0V	16	26	32	37	ns
t_W	Minimum Pulse Width Clear or Enable		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_S	Minimum Setup Time Address or Data to Enable		2.0V		100	125	150	ns
			4.5V		20	25	28	ns
			6.0V		15	19	25	ns
t_H	Minimum Hold Time Address or Data to Enable		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		80				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

Logic Diagram



TL/F/5006–2

National Semiconductor

microCMOS

MM54HC266/MM74HC266 Quad 2-Input Exclusive NOR Gate

General Description

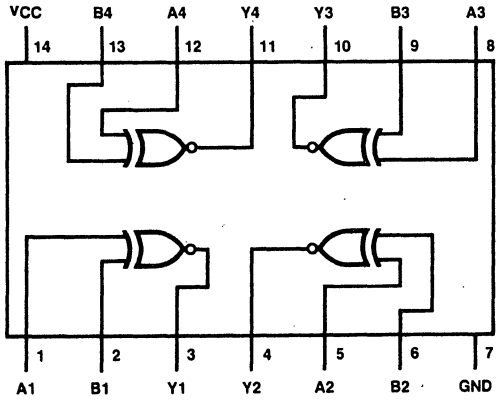
This exclusive NOR gate utilizies microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to equivalent LS-TTL gates while maintaining the low power consumption and high noise immunity characteristic of standard CMOS integrated circuits. These gates are fully buffered and have a fanout of 10 LS-TTL loads. The MM54HC/MM74HC logic family is functionally as well as pin out compatible with the standard 54LS/74LS logic family. However, unlike the 'LS266, which is an open collector gate, the 'HC266 has standard CMOS push-pull outputs. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 9 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 20 μA maximum (74 Series)
- Output drive capability: 10 LS-TTL loads
- Push-pull output

Connection Diagram

Dual-In-Line Package



TL/F/5330–1

Top View

Order Number MM54HC266J or MM74HC266J, N
See NS Package J14A or N14A

Truth Table

Inputs		Outputs
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

$Y = \overline{A \oplus B} = AB + \overline{A}\,\overline{B}$

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics V_{CC} = 2.0V to 6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC273/MM74HC273 Octal D Flip-Flops With Clear

General Description

These edge triggered flip-flops utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, to implement D-type flip-flops. They possess high noise immunity, low power, and speeds comparable to low power Schottky TTL circuits. This device contains 8 master-slave flip-flops with a common clock and common clear. Data on the D input having the specified setup and hold times is transferred to the Q output on the low to high transition of the CLOCK input. The CLEAR input when low, sets all outputs to a low state.

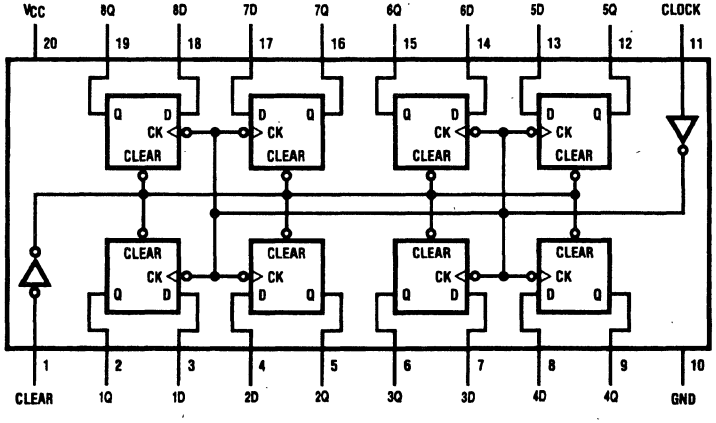
Each output can drive 10 low power Schottky TTL equivalent loads. The MM54HC273/MM74HC273 is functionally as well as pin compatible to the 54LS273/74LS273. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA (74 Series)
- Output drive: 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5331–1

Top View

Order Number MM54HC273J or MM74HC273J, N
See NS Package J20A or N20A

Truth Table

(Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

H = high level (steady state)
L = low level (steady state)
X = don't care
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

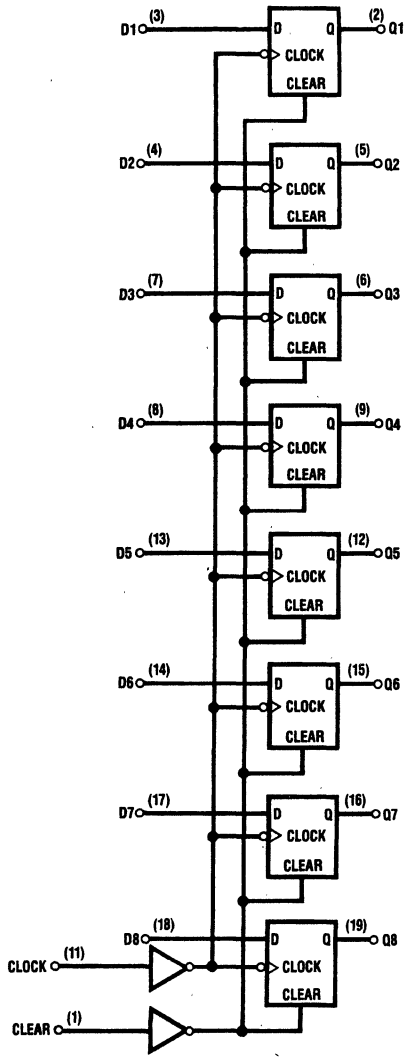
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		18	27	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		18	27	ns
t_{REM}	Minimum Removal Time, Clear to Clock		10	20	ns
t_S	Minimum Setup Time Data to Clock		10	20	ns
t_H	Minimum Hold Time Clock to Data		−2	0	ns
t_W	Minimum Pulse Width Clock or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Output		2.0V	50	160	200	240	ns
			4.5V	21	32	40	48	ns
			6.0V	19	27	33	40	ns
t_{PHL}	Maximum Propagation Delay, Clear to Output		2.0V	50	160	200	240	ns
			4.5V	21	32	40	48	ns
			6.0V	19	27	33	40	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	25	ns
t_S	Minimum Setup Time Data to Clock		2.0V	30	100	125	150	ns
			4.5V	10	20	25	30	ns
			6.0V	9	17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V	−10	0	0	0	ns
			4.5V	−2	0	0	0	ns
			6.0V	−2	0	0	0	ns
t_W	Minimum Pulse Width Clock or Clear		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		175				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5331–2

National Semiconductor

microCMOS

MM54HC280/MM74HC280
9-Bit Odd/Even Parity Generator/Checker

General Description

The MM54HC280/MM74HC280 utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits. It possesses the ability to drive 10 LS-TTL loads.

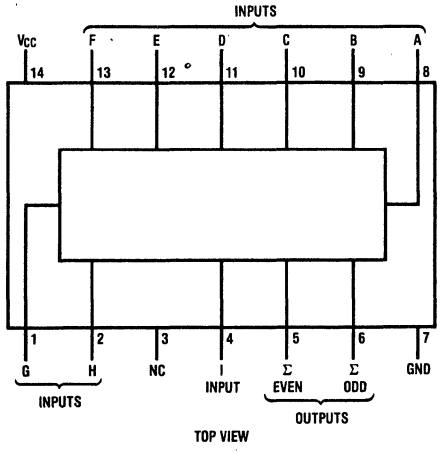
This parity generator/checker features odd/even outputs to facilitate operation of either odd or even parity applications. The word length capability is easily expanded by cascading devices. The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 28 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5121–1

Order Number MM54HC280J or MM74HC280J, N
See NS Package J14A or N14A

Function Table

Numbers of Inputs A thru 1 that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L= low level

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

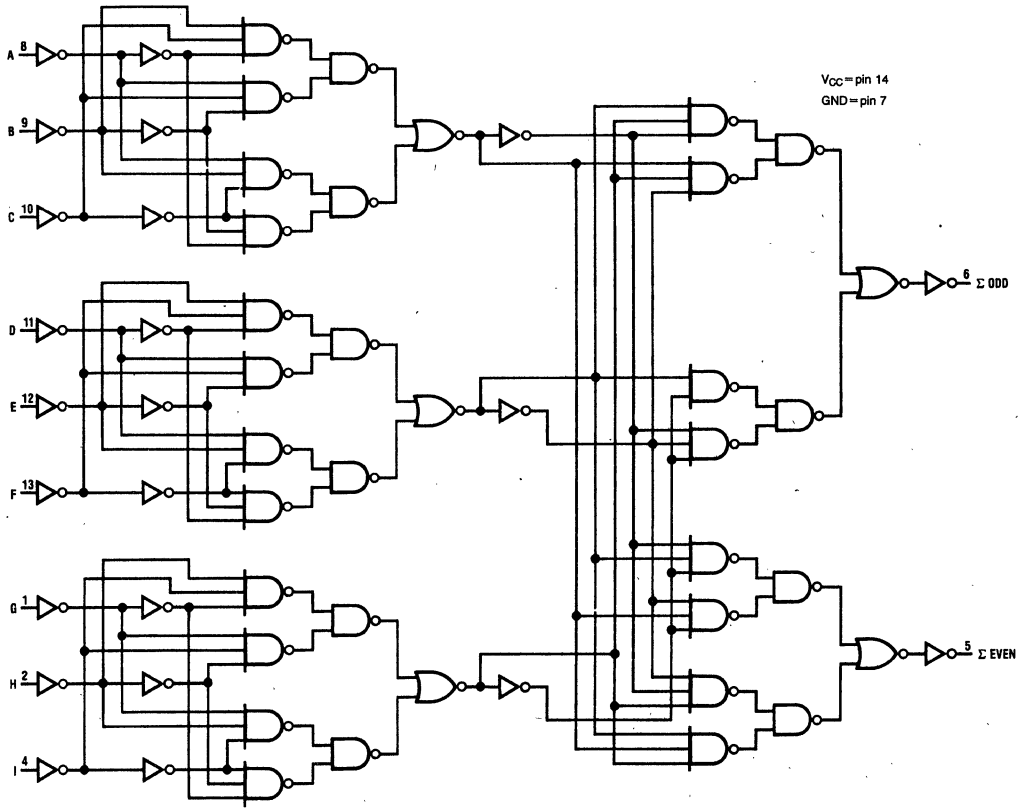
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Even		28	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Odd		28	35	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Even		2.0V	103	205	258	305	ns
			4.5V	21	41	52	61	ns
			6.0V	17	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Σ Odd		2.0V	103	205	258	305	ns
			4.5V	21	41	52	61	ns
			6.0V	17	35	44	52	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



'HC280

TL/F/5121–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC283/MM74HC283
4-Bit Binary Adder with Fast Carry

General Description

This full adder performs the addition of two 4-bit binary numbers utilizing microCMOS Technology, 3.5 micron silicon gate P-well CMOS. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

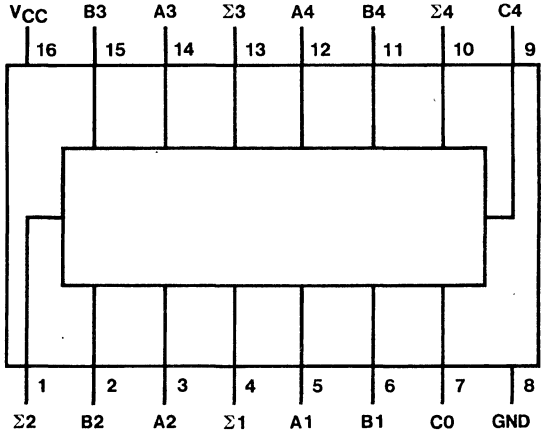
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Wide supply range: 2V to 6V
- Low quiescent power consumption: 8 μA at 25°C
- Low input current: <1 μA

Connection Diagram

Dual-In-Line Package



TL/F/5332–1

Top View

Order Number MM54HC283J or MM74HC283J, N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +1.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ1 or Σ2		18	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ3		18	27	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ4		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A1 or B1 to Σ1		17	26	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to C4		22	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A1 or B1 to C4		22	32	ns

AC Electrical Characteristics C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ1 or Σ2		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ3		2.0V	60	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	18	26	32	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to Σ4		2.0V	65	162	202	243	ns
			4.5V	24	34	43	51	ns
			6.0V	19	28	35	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A1 or B1 to Σ1		2.0V	60	150	188	225	ns
			4.5V	22	33	41	50	ns
			6.0V	18	27	34	41	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From C0 to C4		2.0V	70	175	219	263	ns
			4.5V	26	39	49	59	ns
			6.0V	21	32	40	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay From A1 or B1 to C4		2.0V	70	175	219	263	ns
			4.5V	26	39	49	59	ns
			6.0V	21	32	40	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	28	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{IN}	Maximum Input Capacitance			6	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)		5.0V	150				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

Truth Table

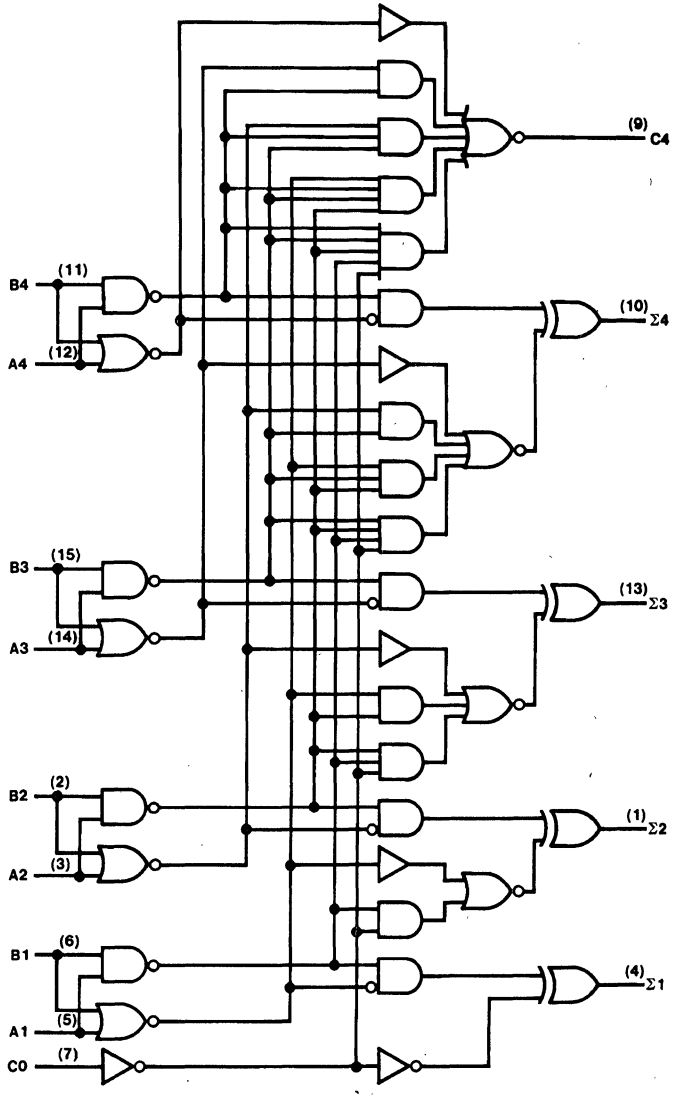
Input								Output									
								When C0 = L						When C0 = H			
												When C2 = L					When C2 = H
A1	A3	B1	B3	A2	A4	B2	B4	Σ1	Σ3	Σ2	Σ4	C2	C4	Σ1	Σ3	Σ2	Σ4	C2	C4
L		L		L		L		L		L		L		H		L		L	
H		L		L		L		H		L		L		L		H		L	
L		H		L		L		H		L		L		L		H		L	
H		H		L		L		L		H		L		H		H		L	
L		L		H		L		L		H		L		H		H		L	
H		L		H		L		H		H		L		L		L		H	
L		H		H		L		H		H		L		L		L		H	
H		H		H		L		L		L		H		H		L		H	
L		L		L		H		L		H		L		H		H		L	
H		L		L		H		H		H		L		L		L		H	
L		H		L		H		H		H		L		L		L		H	
H		H		L		H		L		L		H		H		L		H	
L		L		H		H		L		L		H		H		L		H	
H		L		H		H		H		L		H		L		H		H	
L		H		H		H		H		L		H		L		H		H	
H		H		H		H		L		H		H		H		H		H	

H = high level, L = low level

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4

Logic Diagram

'HC283



TL/F/5332–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC298/MM74HC298
Quad 2-Input Multiplexers With Storage

General Description

These high speed quad two input multiplexers with storage utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Both circuits feature high noise immunity and low power consumption associated with CMOS circuitry, along with speeds comparable to low power Schottky TTL logic.

These circuits are controlled by the signals WORD SELECT and CLOCK. When the WORD SELECT input is taken low Word 1 (A1, B1, C1 and D1) is presented to the inputs of the flip-flops, and when WORD SELECT is high Word 2 (A2, B2, C2 and D2) is presented to the inputs of the flip-flops. The selected word is clocked to the output terminals on the negative edge of the clock pulse.

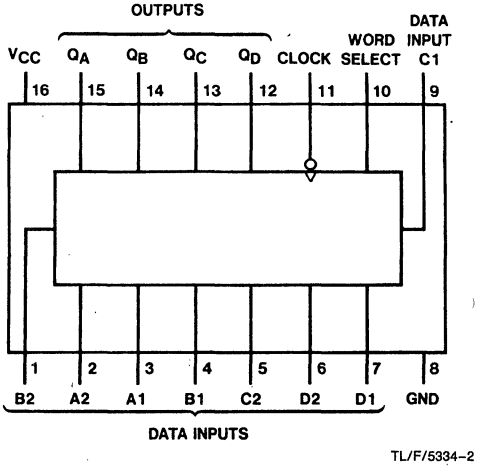
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay, clock to output: 20 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum

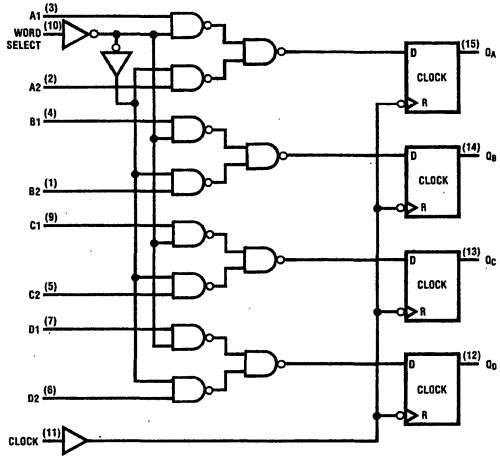
Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5334–2

Top View



TL/F/5334–1

Order Number MM54HC298J or MM74HC298J, N
See NS Package J16A or N16E

Truth Table

Inputs		Outputs			
Word Select	Clock	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care (any input, including transitions)
↓ = Transition from high to low level
a1, a2, etc. = The level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = The level of Q_A, Q_B, etc. entered on the most recent ↓ transition of the clock input.

Absolute Maximum Ratings

(Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter		Conditions	Typ	Guaranteed Limit	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output			21	32	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output			15	32	ns
t_W	Width of Clock Pulse, High or Low Level			10	16	ns
t_{SETUP}	Setup Time	Data		5	20	ns
		Word Select		10	20	
t_{HOLD}	Hold Time	Data		−2	0	ns
		Word Select		−2	0	

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns

Symbol	Parameter		Conditions	V_{CC}	54HC/74HC $T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ	Guaranteed Limits		
t_{PLH}	Propagation Delay Time Low-to-High Level Output			2.0V	75	185	231	278	ns
				4.5V	25	37	46	56	ns
				6.0V	20	31	39	47	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output			2.0V	75	185	231	278	ns
				4.5V	25	37	46	56	ns
				6.0V	20	31	39	47	ns
t_W	Width of Clock Pulse High or Low Level			2.0V	35	80	100	120	ns
				4.5V	10	16	20	24	ns
				6.0V	9	14	18	21	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			2.0V	90	75	95	110	ns
				4.5V	8	15	19	22	ns
				6.0V	7	13	16	19	ns
t_{SETUP}	Setup Time	Data		2.0V	35	100	125	150	ns
				4.5V	5	20	25	30	ns
				6.0V	4	17	21	25	ns
		Word Select		2.0V	40	100	125	150	ns
				4.5V	10	20	25	30	ns
				6.0V	9	17	21	25	ns
t_{HOLD}	Hold Time	Data		2.0V	−10	0	0	0	ns
				4.5V	−3	0	0	0	ns
				6.0V	−2	0	0	0	ns
		Word Select		2.0V	−10	0	0	0	ns
				4.5V	−3	0	0	0	ns
				6.0V	−2	0	0	0	ns
C_{PD}	Power Dissipation Capacitance (Note 5)								pF
C_{IN}	Maximum Input Capacitance				5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

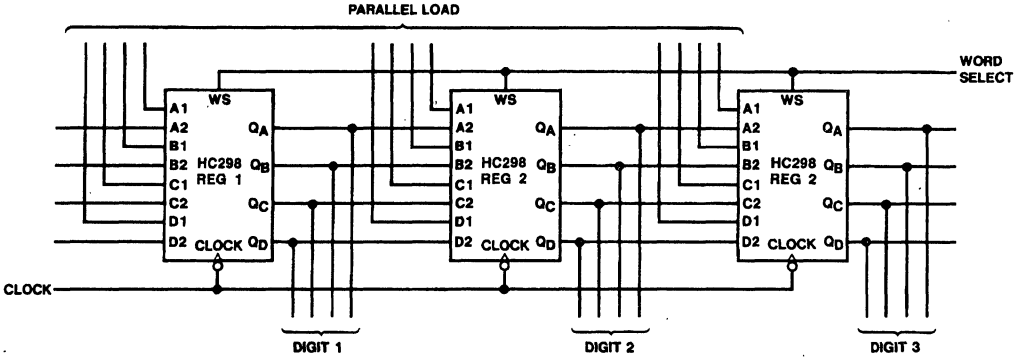
Typical Applications

Figure 1 illustrates a BCD shift register that will shift an entire 4-bit BCD digit in one clock pulse.

When the word select input is high and the registers are clocked, the contents of Register 1 is transferred (shifted) to Register 2, etc. In effect, the BCD digits are shifted one position. In addition, this application retains a parallel-load capability which means that new BCD data can be entered into the entire register with one clock pulse. This arrangement can be modified to perform the shifting of binary data for any number of bit locations.

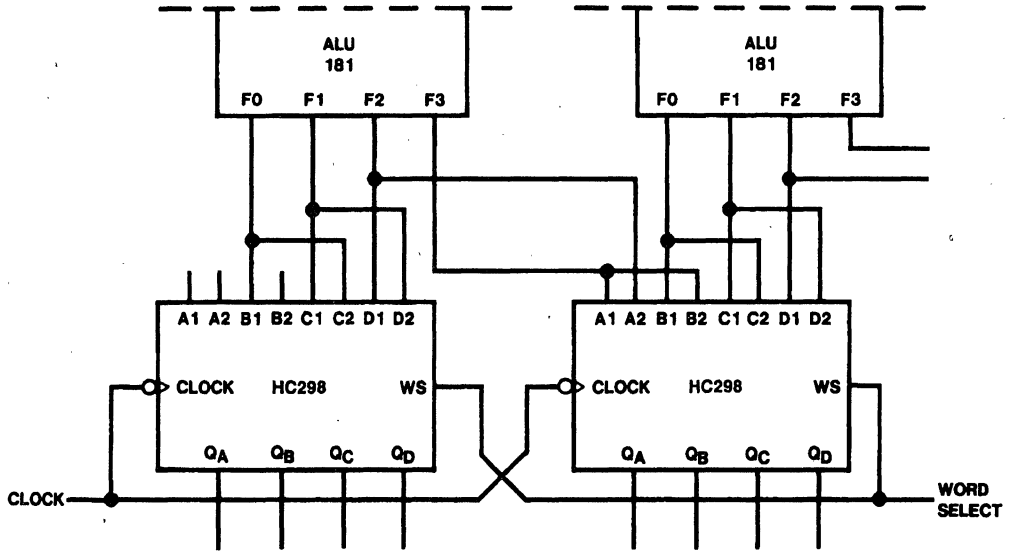
Another function that can be implemented with the MM54HC298/MM74HC298 is a register that can be designed specifically for supporting multiplier or division operations. *Figure 2* is an example of a one place/two place shift register.

When word select is low and the register is clocked, the outputs of the arithmetic/logic units (ALU's) are shifted one place. When word select is high and the registers are clocked, the data is shifted two places.



TL/F/5334–3

FIGURE 1



TL/F/5334–4

FIGURE 2

National Semiconductor

microCMOS

MM54HC299/MM74HC299
8-Bit TRI-STATE® Universal Shift Register

General Description

This 8-bit TRI-STATE shift/storage register utilizes micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. Along with the low power consumption and high noise immunity of standard CMOS integrated circuits, it has the ability to drive 15 LS-TTL loads. This circuit also features operating speeds comparable to the equivalent low power Schottky device.

The MM54HC299/MM74HC299 features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus oriented system.

Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines S0 and S1 high. This places the TRI-STATE outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding CLEAR input is provided to clear the register whether the outputs are enabled or disabled.

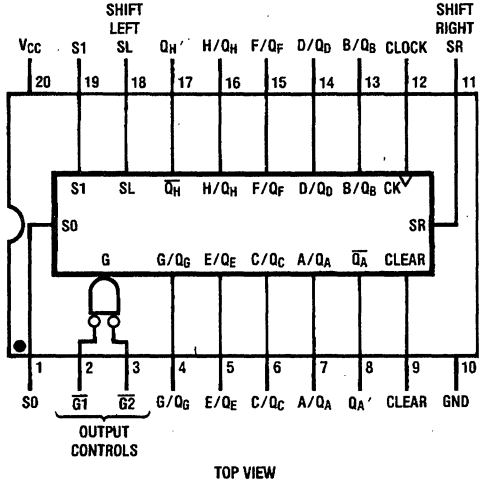
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical operating frequency 40 MHz
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HC)
- High output drive for bus applications
- Low quiescent current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5207–1

Order Number MM54HC299J or MM74HC299J,N
See NS Package J20A or N20A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA ($Q_{A'}$, $Q_{H'}$)
	±35 mA (others)
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	$Q_{A'}$ & $Q_{H'}$ Outputs	V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\|$≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
	A/Q_A thru H/Q_H Outputs	V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\|$≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	$Q_{A'}$ and $Q_{H'}$ Outputs	V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\|$≤4 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
	A/Q_A thru H/Q_H Outputs	V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\|$≤6 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Currrent	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}	6.0V		±0.5	±0.5	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns, $C_L=45$ pF

Symbol	Parameter		Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			40	25	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $Q_{A'}$ or $Q_{H'}$			25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to $Q_{A'}$ or $Q_{H'}$			39	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q_A–Q_H		$C_L=45$ pF	25	35	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A–Q_H		$C_L=45$ pF	28	40	ns
t_{PZL}, t_{PZH}	Maximum Enable Time		$C_L=45$ pF $R_L=1$ kΩ	10	35	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time		$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_S	Minimum Setup Time	Select			20	ns
		Data			20	
t_H	Minimum Hold Time	Select			0	ns
		Data			0	
t_W	Minimum Pulse Width			12	20	ns
t_{REM}	Clear Removal Time				10	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3.5	MHz
			4.5V		25	20	18	MHz
			6.0V		29	23	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $Q_{A'}$ or $Q_{H'}$		2.0V	15	170	210	240	ns
			4.5V	27	38	48	54	ns
			6.0V	25	35	44	49	ns
t_{PHL}	Maximum Propagation Delay, Clear to $Q_{A'}$ or $Q_{H'}$		2.0V	70	200	250	280	ns
			4.5V	30	44	55	62	ns
			6.0V	26	38	46	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q_A–Q_H	$C_L=50$ pF	2.0V	65	170	210	240	ns
		$C_L=150$ pF	2.0V	100	206	260	295	ns
		$C_L=50$ pF	4.5V	27	38	48	54	ns
		$C_L=150$ pF	4.5V	34	46	57	66	ns
		$C_L=50$ pF	6.0V	25	35	44	49	ns
		$C_L=150$ pF	6.0V	31	39	49	55	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q_A–Q_H	$C_L=50$ pF	2.0V	70	200	250	280	ns
		$C_L=150$ pF	2.0V	110	236	295	325	ns
		$C_L=50$ pF	4.5V	30	44	55	62	ns
		$C_L=150$ pF	4.5V	37	52	65	75	ns
		$C_L=50$ pF	6.0V	26	38	46	52	ns
		$C_L=150$ pF	6.0V	32	46	57	64	ns

AC Electrical Characteristic (Continued) $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L = 1$ kΩ					
		$C_L = 50$ pF	2.0V	70	160	200	225	ns
		$C_L = 150$ pF	2.0V	90	220	275	310	ns
		$C_L = 50$ pF	4.5V	22	32	40	45	ns
		$C_L = 150$ pF	4.5V	30	44	55	62	ns
		$C_L = 50$ pF	6.0V	19	28	34	38	ns
		$C_L = 150$ pF	6.0V	24	47	47	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L = 1$ kΩ, $C_L = 50$ pF	2.0V	70	160	200	225	ns
			4.5V	22	32	40	45	ns
			6.0V	19	28	34	38	ns
t_S	Minimum Setup Time, Data Select S_L or S_R		2.0V		100	125	140	ns
			4.5V		20	25	28	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time, Data Select S_L or S_R		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{REM}	Minimum Clear Removal Time		2.0V		10	10	10	ns
			4.5V		10	10	10	ns
			6.0V		10	10	10	ns
t_W	Minimum Pulse Width, Clock and Clear		2.0V		100	125	140	ns
			4.5V		20	25	28	ns
			6.0V		17	21	25	ns
t_r, t_f	Maximum Input Rise and Fall Time				500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time, Clock		2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
C_{PD}	Power Dissipation Capacitance	Outputs Enabled		240				pF
		Outputs Disabled		110				pF
C_{IN}	Maximum Input Capacitance Capacitance			5	10	10	10	pF
C_{OUT}	Maximum TRI-STATE Output Capacitance			15	20	20	20	pF

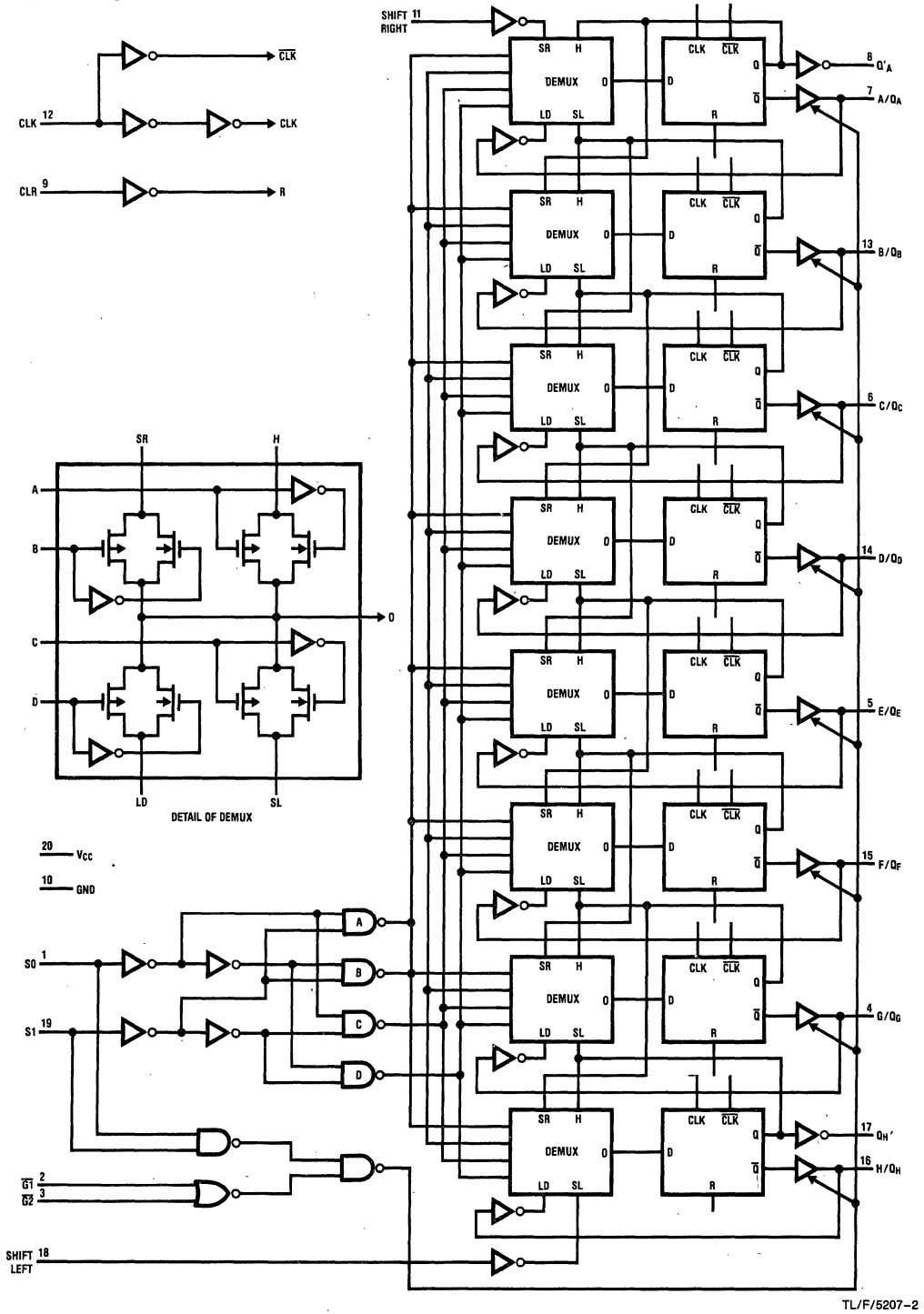
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L or H	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{GN}
	H	L	H	L	L	↑	X	H	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{GN}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

Logic Diagram



TL/F/5207–2

National Semiconductor

microCMOS

MM54HC354/MM74HC354/ MM54HC356/MM74HC356 8-Channel TRI-STATE® Multiplexers with Latches

General Description

The MM54HC354/MM74HC354 and MM54HC356/MM74HC356 utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They exhibit the high noise immunity and low power dissipation of standard CMOS integrated circuits, along with the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data select address is stored in transparent latches that are enabled by a low level address on pin 11, $\overline{SC}$. Data on the 8 input lines is stored in a parallel input/output register which in the MM54HC354/MM74HC354 is composed of 8 transparent latches enabled by a low level on pin 9, $\overline{DC}$, and in the MM54HC356/MM74HC356 is composed of 8 edge-triggered flip-flops, clocked by a low to high transition on pin 9, CLK. Both true (Y) and complementary (W) TRI-STATE outputs are available on both devices.

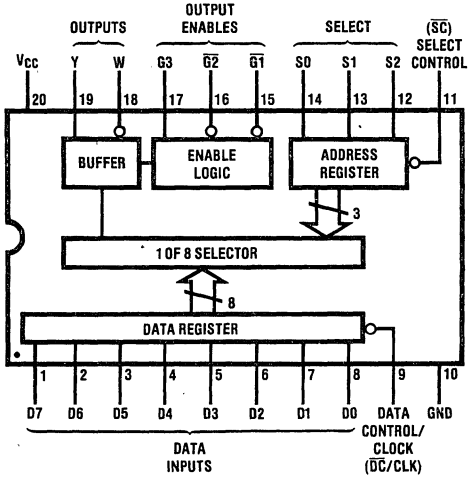
The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS-TTL logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Transparent latches on data select inputs
- Choice of data registers:
  - Transparent ('354)
  - Edge-triggered ('356)
- TRI-STATE complementary outputs with fanout of 15 LS-TTL loads
- Typical propagation delay:
  - Data to output ('354): 32 ns
  - Clock to output ('346): 35 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 80 μA maximum
- Low input current: 1 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5208–1

Top View

Order Number MM54HC354J, MM54HC356J, MM74HC354J,N or MM74HC356J,N
See NS Package J20A or N20A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|<20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{OUT}=V_{CC}$ or GND $\overline{G1}=V_{IH}$	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

MM54HC354/MM74HC354

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0–D7 to either Output	$C_L=45$ pF	32	46	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{DC}$ to either Output	$C_L=45$ pF	38	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	$C_L=45$ pF	40	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	$C_L=45$ pF	42	58	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	17	24	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	23	32	ns
t_S	Minimum Setup Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		3	10	ns
t_H	Minimum Hold Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		0	5	ns
t_W	Minimum Pulse Width, $\overline{SC}$ or $\overline{DC}$		10	15	ns

MM54HC356/MM74HC356

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay CLK to either Output	$C_L=45$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	$C_L=45$ pF	40	56	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	$C_L=45$ pF	42	58	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	17	24	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	23	32	ns
t_S	Minimum Setup Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		3	10	ns
t_H	Minimum Hold Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		0	5	ns
t_W	Minimum Pulse Width, $\overline{SC}$ or CLK		10	15	ns

AC Electrical Characteristics MM54HC354/MM74HC354 (Continued)

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay D0–D7 to either Output	C_L = 50 pF	2.0V	90	235	294	352	ns
		C_L = 150 pF	2.0V	100	275	344	412	ns
		C_L = 50 pF	4.5V	35	47	59	70	ns
		C_L = 150 pF	4.5V	40	55	68	83	ns
		C_L = 50 pF	6.0V	26	40	50	60	ns
		C_L = 150 pF	6.0V	32	46	58	69	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{DC}$ to either Output	C_L = 50 pF	2.0V	115	270	337	405	ns
		C_L = 150 pF	2.0V	125	310	387	465	ns
		C_L = 50 pF	4.5V	40	54	68	82	ns
		C_L = 150 pF	4.5V	46	62	78	93	ns
		C_L = 50 pF	6.0V	32	46	58	69	ns
		C_L = 150 pF	6.0V	38	52	66	78	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	C_L = 50 pF	2.0V	120	285	356	427	ns
		C_L = 150 pF	2.0V	130	325	406	488	ns
		C_L = 50 pF	4.5V	42	57	71	86	ns
		C_L = 150 pF	4.5V	50	65	81	97	ns
		C_L = 50 pF	6.0V	34	48	60	72	ns
		C_L = 150 pF	6.0V	40	55	69	82	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	C_L = 50 pF	2.0V	120	300	375	450	ns
		C_L = 150 pF	2.0V	110	340	425	510	ns
		C_L = 50 pF	4.5V	45	60	75	90	ns
		C_L = 150 pF	4.5V	52	68	85	102	ns
		C_L = 50 pF	6.0V	36	51	64	77	ns
		C_L = 150 pF	6.0V	42	58	72	87	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	50	125	156	188	ns
		C_L = 150 pF	2.0V	60	165	206	248	ns
		C_L = 50 pF	4.5V	18	25	31	38	ns
		C_L = 150 pF	4.5V	25	33	41	49	ns
		C_L = 50 pF	6.0V	15	21	26	32	ns
		C_L = 150 pF	6.0V	21	28	35	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ	2.0V	68	165	206	248	ns
		C_L = 50 pF	4.5V	24	33	40	46	ns
			6.0V	20	28	35	42	ns
t_S	Minimum Setup Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		2.0V	6	50	60	75	ns
			4.5V	3	10	13	15	ns
			6.0V	3	10	13	15	ns
t_H	Minimum Hold Time D0–D7 to $\overline{DC}$, S0–S2 to $\overline{SC}$		2.0V	0	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	0	5	5	5	ns
t_W	Minimum Pulse Width $\overline{SC}$ or $\overline{DC}$		2.0V	30	80	100	120	ns
			4.5V	10	16	20	27	ns
			6.0V	10	15	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Active		150				pF
		TRI-STATE		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

AC Electrical Characteristics MM54HC356/MM74HC356 (Continued)

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$		74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay CLK to either Output	C_L = 50 pF	2.0V	100	225	318	338	ns
		C_L = 150 pF	2.0V	110	295	369	442	ns
		C_L = 50 pF	4.5V	36	51	63	76	ns
		C_L = 150 pF	4.5V	42	59	73	90	ns
		C_L = 50 pF	6.0V	28	43	53	64	ns
		C_L = 150 pF	6.0V	34	50	63	75	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay S0–S2 to either Output	C_L = 50 pF	2.0V	120	285	356	427	ns
		C_L = 150 pF	2.0V	130	325	406	488	ns
		C_L = 50 pF	4.5V	42	57	71	86	ns
		C_L = 150 pF	4.5V	50	65	81	97	ns
		C_L = 50 pF	6.0V	34	48	60	72	ns
		C_L = 150 pF	6.0V	40	55	69	82	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{SC}$ to either Output	C_L = 50 pF	2.0V	120	300	375	450	ns
		C_L = 150 pF	2.0V	110	340	425	510	ns
		C_L = 50 pF	4.5V	45	60	75	90	ns
		C_L = 150 pF	4.5V	52	68	85	102	ns
		C_L = 50 pF	6.0V	36	51	64	77	ns
		C_L = 150 pF	6.0V	42	58	72	87	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	50	125	156	188	ns
		C_L = 150 pF	2.0V	60	165	206	248	ns
		C_L = 50 pF	4.5V	18	25	31	38	ns
		C_L = 150 pF	4.5V	25	33	41	49	ns
		C_L = 50 pF	6.0V	15	21	26	32	ns
		C_L = 150 pF	6.0V	21	28	35	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ	2.0V	68	165	206	248	ns
		C_L = 50 pF	4.5V	24	33	41	49	ns
			6.0V	20	28	35	42	ns
t_S	Minimum Setup Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		2.0V	6	50	50	50	ns
			4.5V	3	10	10	10	ns
			6.0V	3	10	10	10	ns
t_H	Minimum Hold Time D0–D7 to CLK, S0–S2 to $\overline{SC}$		2.0V	0	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	0	5	5	5	ns
t_W	Minimum Pulse Width $\overline{SC}$ to CLK		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	10	15	18	20	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package) Active		150				pF
		TRI-STATE		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

Function Table

Inputs								Outputs	
Select†			Data Control 'HC354	Clock 'HC356	Output Enables				
S1	S2	S0	$\overline{DC}$	CLK	$\overline{G1}$	$\overline{G2}$	G3	W	Y
X	X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	X	L	Z	Z
L	L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	H	H or L	L	L	H	$\overline{D0}_n$	$D0_n$
L	L	H	L	↑	L	L	H	$\overline{D1}$	D1
L	L	H	H	H or L	L	L	H	$\overline{D1}_n$	$D1_n$
L	H	L	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	H	H or L	L	L	H	$\overline{D2}_n$	$D2_n$
L	H	H	L	↑	L	L	H	$\overline{D3}$	D3
L	H	H	H	H or L	L	L	H	$\overline{D3}_n$	$D3_n$
H	L	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	H	H or L	L	L	H	$\overline{D4}_n$	$D4_n$
H	L	H	L	↑	L	L	H	$\overline{D5}$	D5
H	L	H	H	H or L	L	L	H	$\overline{D5}_n$	$D5_n$
H	H	L	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	H	H or L	L	L	H	$\overline{D6}_n$	$D6_n$
H	H	H	L	↑	L	L	H	$\overline{D7}$	D7
H	H	H	H	H or L	L	L	H	$\overline{D7}_n$	$D7_n$

H = high level (steady state)

L = low level (steady state)

X = irrelevant (any input, including transitions)

Z = high-impedance state (off state)

↑ = transition from low to high level

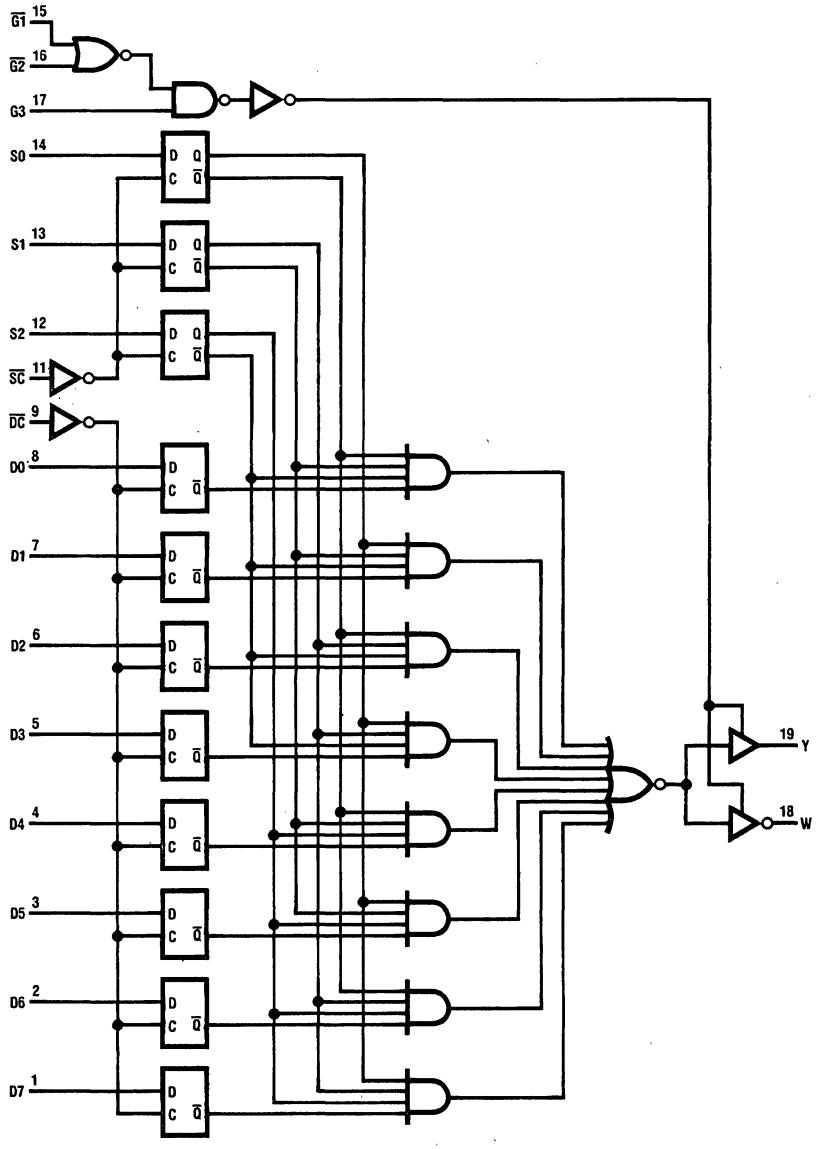
D0 . . . D7 = the level steady-state inputs at inputs D0 through D7, respectively, at the time of the low-to-high clock transition in the case of 'HC356

$D0_n$ . . . $D7_n$ = the level of steady state inputs at inputs D0 through D7, respectively, before the most recent low-to-high transition of data control or clock.

†This column shows the input address set-up with $\overline{SC}$ low.

Logic Diagram

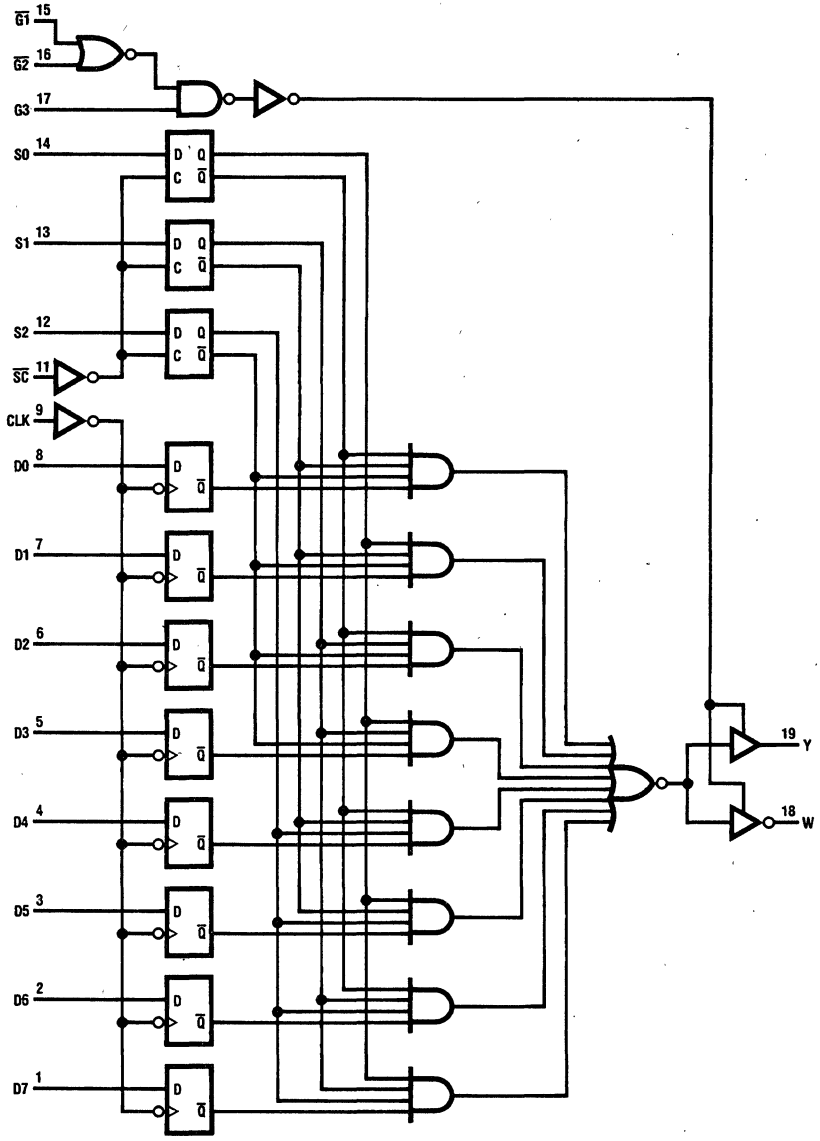
'HC354



TL/F/5208–2

Logic Diagram

'HC356



TL/F/5208–3

National Semiconductor

microCMOS

MM54HC365/MM74HC365 Hex TRI-STATE® Buffer
MM54HC366/MM74HC366 Inverting Hex TRI-STATE Buffer
MM54HC367/MM74HC367 Hex TRI-STATE Buffer
MM54HC368/MM74HC368 Inverting Hex TRI-STATE Buffer

General Description

These TRI-STATE buffers are general purpose high speed inverting and non-inverting buffers that utilize micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power dissipation of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits. All 4 circuits are capable of driving up to 15 low power Schottky inputs.

The MM54/74HC366 and the MM54/74HC368 are inverting buffers, where as the MM54/74HC365 and the MM54/74HC367 are non-inverting buffers. The MM54/74HC365 and the MM54/74HC366 have two TRI-STATE control inputs ($\overline{G1}$ and $\overline{G2}$) which are NORed together to control all six gates. The MM54/74HC367 and the MM54/74HC368 also have two output enables, but one enable ($\overline{G1}$) controls 4 gates and the other ($\overline{G2}$) controls the remaining 2 gates.

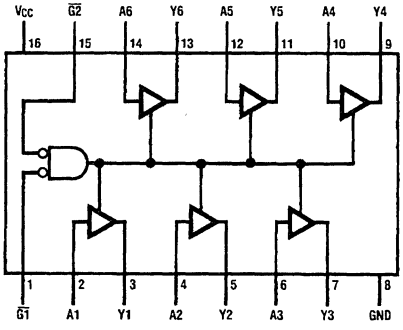
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Output drive capability: 15 LS-TTL loads

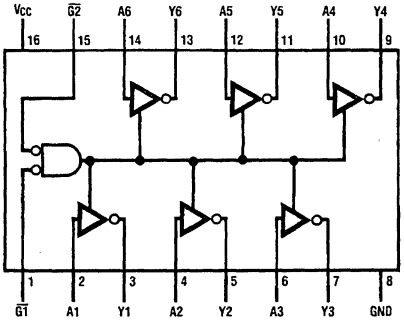
Connection Diagrams

Dual-In-Line Packages/Top Views



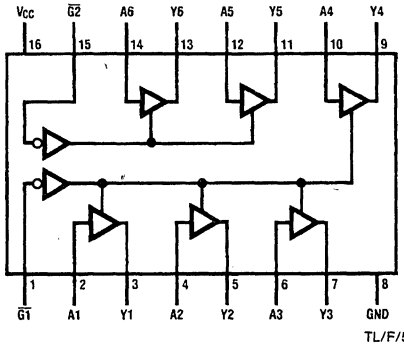
TL/F/5209–1

Order Number MM54HC365J, MM74HC365J, N
See NS Package J16A or N16E



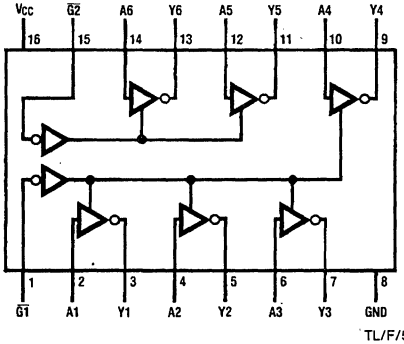
TL/F/5209–2

Order Number MM54HC366J, MM74HC366J, N
See NS Package J16A or N16E



TL/F/5209–3

Order Number MM54HC367J, MM74HC367J, N
See NS Package J16A or N16E



TL/F/5209–4

Order Number MM54HC368J, MM74HC368J, N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC365/MM74HC365

V_{CC} = 5V, T_A = 25°C, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 45 pF	15	22	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 45 pF	29	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 5 pF	25	36	ns

AC Electrical Characteristics MM54HC365/MM74HC365

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	C_L = 50 pF	2.0V	35	105	130	150	ns
		C_L = 150 pF	2.0V	45	135	168	205	ns
		C_L = 50 pF	4.5V	14	24	30	36	ns
		C_L = 150 pF	4.5V	17	29	36	45	ns
		C_L = 50 pF	6.0V	11	19	24	28	ns
		C_L = 150 pF	6.0V	15	24	30	36	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ C_L = 50 pF	2.0V	90	230	287	345	ns
		C_L = 150 pF	2.0V	98	245	306	367	ns
		C_L = 50 pF	4.5V	31	44	55	66	ns
		C_L = 150 pF	4.5V	38	53	66	80	ns
		C_L = 50 pF	6.0V	25	35	43	52	ns
		C_L = 150 pF	6.0V	29	41	51	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF	2.0V	58	175	218	260	ns
			4.5V	26	44	55	66	ns
			6.0V	22	37	46	55	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Truth Table

'HC365

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	H
L	L	L	L

AC Electrical Characteristics (Continued) MM54HC366/MM74HC366

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	29	40	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	25	36	ns

AC Electrical Characteristics MM54HC366/MM74HC366

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	33	82	102	125	ns
		$C_L=150$ pF	2.0V	43	107	134	160	ns
		$C_L=50$ pF	4.5V	12	19	24	30	ns
		$C_L=150$ pF	4.5V	16	26	32	39	ns
		$C_L=50$ pF	6.0V	10	16	20	24	ns
		$C_L=150$ pF	6.0V	14	22	27	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						ns
		$C_L=50$ pF	2.0V	90	230	287	345	ns
		$C_L=150$ pF	2.0V	98	245	306	367	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	38	53	66	80	ns
		$C_L=50$ pF	6.0V	25	35	43	52	ns
		$C_L=150$ pF	6.0V	29	41	51	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	58	175	218	260	ns
		$C_L=50$ pF	4.5V	26	44	55	66	ns
			6.0V	22	37	46	55	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Truth Table

'HC366

Inputs			Output
$\overline{G1}$	$\overline{G2}$	A	Y
H	X	X	Z
X	H	X	Z
L	L	H	L
L	L	L	H

AC Electrical Characteristics (Continued) MM54HC367/MM74HC367

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	13	22	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	23	37	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	25	33	ns

AC Electrical Characteristics MM54HC367/MM74HC367

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	35	105	130	150	ns
		$C_L=150$ pF	2.0V	45	135	168	205	ns
		$C_L=50$ pF	4.5V	14	24	30	36	ns
		$C_L=150$ pF	4.5V	17	29	36	45	ns
		$C_L=50$ pF	6.0V	11	19	24	28	ns
		$C_L=150$ pF	6.0V	15	24	30	36	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						ns
		$C_L=50$ pF	2.0V	69	172	216	250	ns
		$C_L=150$ pF	2.0V	75	187	233	280	ns
		$C_L=50$ pF	4.5V	24	38	47	57	ns
		$C_L=150$ pF	4.5V	29	46	57	69	ns
		$C_L=50$ pF	6.0V	22	35	43	52	ns
		$C_L=150$ pF	6.0V	26	42	52	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	47	117	146	220	ns
			4.5V	22	35	44	52	ns
			6.0V	19	31	39	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		8				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

Truth Table

'HC367

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

AC Electrical Characteristics (Continued) MM54HC368/MM74HC368

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	11	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	23	37	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	33	ns

AC Electrical Characteristics MM54HC368/MM74HC368

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	33	82	102	125	ns
		$C_L=150$ pF	2.0V	43	107	134	160	ns
		$C_L=50$ pF	4.5V	12	19	24	30	ns
		$C_L=150$ pF	4.5V	16	26	32	39	ns
		$C_L=50$ pF	6.0V	10	16	20	24	ns
		$C_L=150$ pF	6.0V	14	22	27	33	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						ns
		$C_L=50$ pF	2.0V	69	172	216	250	ns
		$C_L=150$ pF	2.0V	75	187	233	280	ns
		$C_L=50$ pF	4.5V	24	38	47	57	ns
		$C_L=150$ pF	4.5V	29	46	57	69	ns
		$C_L=50$ pF	6.0V	22	35	43	52	ns
		$C_L=150$ pF	6.0V	26	42	52	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	47	117	146	220	ns
		$C_L=50$ pF	4.5V	22	35	44	52	ns
			6.0V	19	31	39	46	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	Any Enabled A Input		45				pF
		Any Disabled A Input		6				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Input Capacitance			10	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

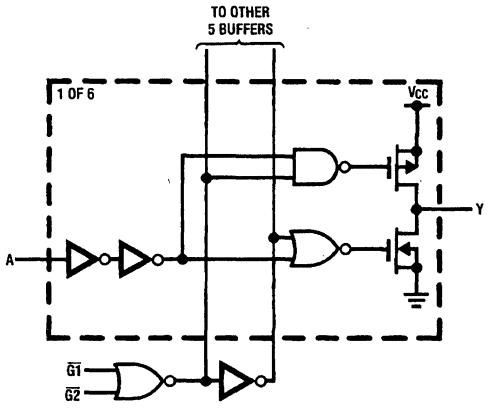
Truth Table

'HC368

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

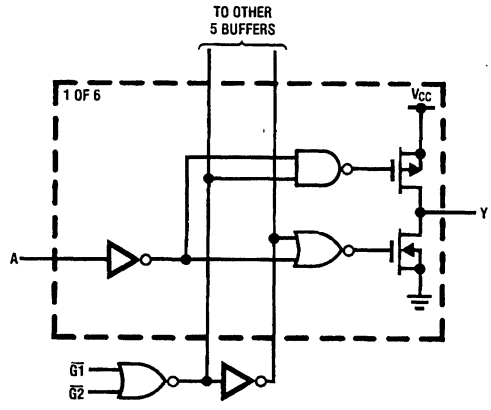
Logic Diagrams

MM54HC365/MM74HC365



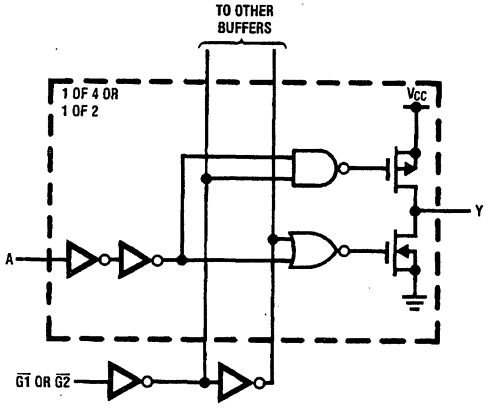
TL/F/5209–5

MM54HC366/MM74HC366



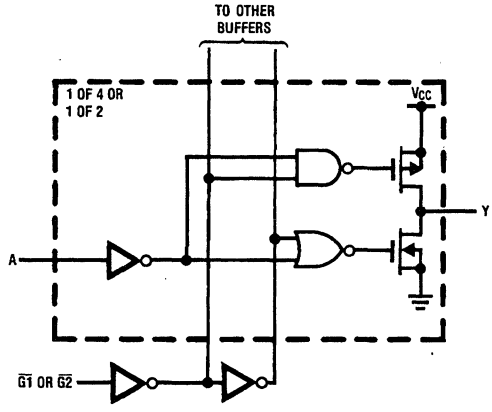
TL/F/5209–6

MM54HC367/MM74HC367



TL/F/5209–7

MM54HC368/MM74HC368



TL/F/5209–8

National Semiconductor

microCMOS

MM54HC373/MM74HC373 TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

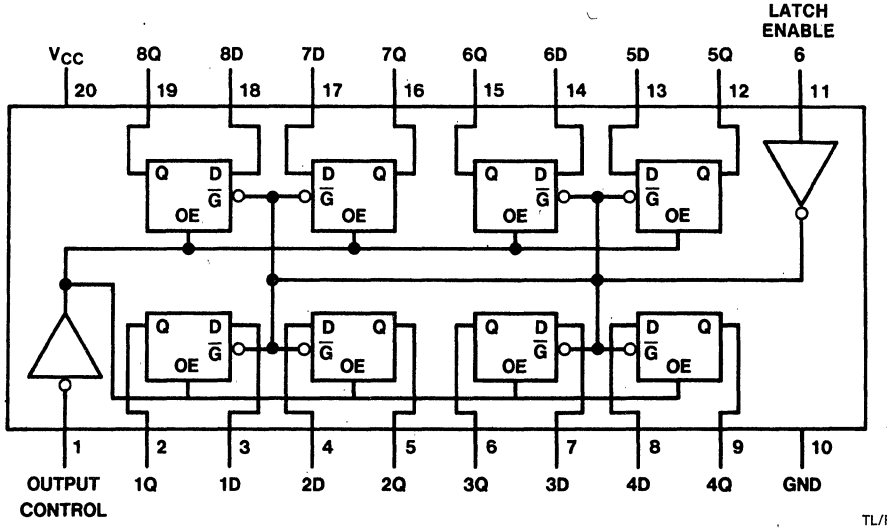
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5335–1

Top View

Order Number MM54HC373J or MM74HC373J,N
See NS Package J20A or N20A

Truth Table

Output Control	Latch Enable	Data	373 Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL}, OC=V_{IH} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	22	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	63	175	220	263	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	25	35	44	52	ns
		$C_L=150$ pF	4.5V	35	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	28	39	49	59	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	188	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V	5	25	31	38	ns
			4.5V	2	5	6	8	ns
			6.0V	2	5	6	8	ns
t_H	Minimum Hold Time		2.0V	20	50	60	75	ns
			4.5V	6	10	13	20	ns
			6.0V	6	10	13	20	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time, Clock	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch)						
		OC=V_{CC}		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC374/MM74HC374
TRI-STATE® Octal D-Type Flip-Flop

General Description

These high speed Octal D-Type Flip-Flops utilize micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

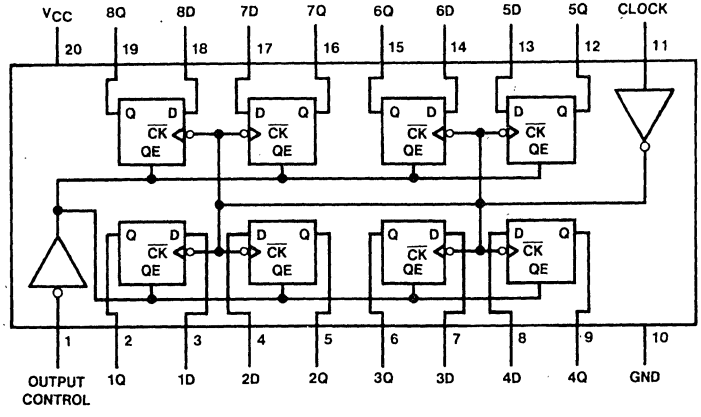
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5336–1

Top View

Order Number MM54HC374J or MM74HC374J, N
See NS Package J20A or N20A

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high Level, L = Low Level
X = don't Care
↑ = transition from low-to-high
Z = high impedance state
Q_0 = the level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{IN}=V_{IH}$, OC=V_{IH} $V_{OUT}=V_{CC}$ or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=$ kΩ $C_L=45$ pF	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=$ kΩ $C_L=5$ pF	17	25	ns
t_S	Minimum Setup Time			20	ns
t_H	Minimum Hold Time			5	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–6.0V, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V	6	5	4	MHz
			4.5V	30	24	20	MHz
			6.0V	35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	68	180	225	270	ns
		$C_L=150$ pF	2.0V	110	230	288	345	ns
		$C_L=50$ pF	4.5V	22	36	45	48	ns
		$C_L=150$ pF	4.5V	30	46	57	69	ns
		$C_L=50$ pF	6.0V	20	31	39	46	ns
		$C_L=150$ pF	6.0V	28	40	50	60	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	189	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Setup Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		25	31	38	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop) OC=V_{CC}		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC390/MM74HC390 Dual 4-Bit Decade Counter
MM54HC393/MM74HC393 Dual 4-Bit Binary Counter

General Description

These counter circuits contain independent ripple carry counters and utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. The MM54HC390/MM74HC390 incorporate dual decade counters, each composed of a divide-by-two and a divide-by-five counter. The divide-by-two and divide-by-five counters can be cascaded to form dual decade, dual bi-quinary, or various combinations up to a single divide-by-100 counter. The MM54HC393/MM74HC393 contain two 4-bit ripple carry binary counters, which can be cascaded to create a single divide-by-256 counter.

Each of the two 4-bit counters is incremented on the high to low transition (negative edge) of the clock input, and each has an independent clear input. When clear is set high all four bits of each counter are set to a low level. This enables count truncation and allows the implementation of divide-by-N counter configurations.

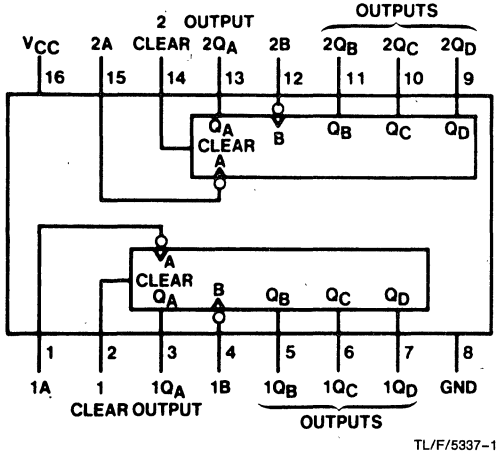
Each of the counters outputs can drive 10 low power Schottky TTL equivalent loads. These counters are functionally as well as pin equivalent to the 54LS390/74LS390 and the 54LS393/74LS393, respectively. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical operating frequency: 50 MHz
- Typical propagation delay: 13 ns (Ck to Q_A)
- Wide operating supply voltage range: 2–6V
- Low input current: <1 μA
- Low quiescent supply current: 80 μA maximum (74HC Series)
- Fanout of 10 LS-TTL loads

Connection Diagrams

Dual-In-Line Package

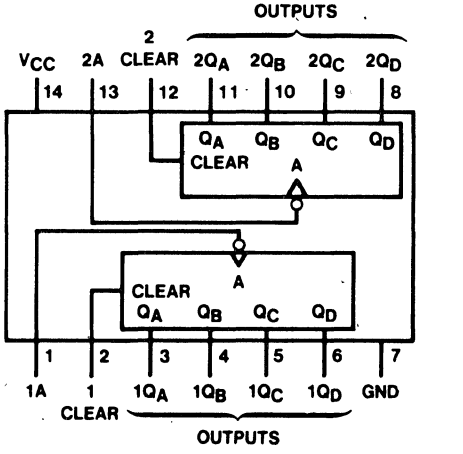


TL/F/5337–1

Top View

Order Number MM54HC390J or MM74HC390J, N
See NS Package J16A or N16E

Dual-In-Line Package



TL/F/5337–2

Top View

Order Number MM54HC393J or MM74HC393J, N
See NS Package J14A or N14A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC390/MM74HC390

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency, Clock A or B		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A Output		12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A Connected to Clock B)		32	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_B or Q_D		15	21	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_C		20	32	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Output		15	28	ns
t_{REM}	Minimum Removal Time, Clear to Clock		−2	5	ns
t_W	Minimum Pulse Width, Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A		2.0V	45	120	150	180	ns
			4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C (Q_A Connected to Clock B)		2.0V	100	290	360	430	ns
			4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_B or Q_D		2.0V	50	130	160	195	ns
			4.5V	16	26	33	39	ns
			6.0V	13	22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock B to Q_C		2.0V	60	185	230	280	ns
			4.5V	20	37	46	55	ns
			6.0V	17	32	40	48	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Q		2.0V	55	165	210	250	ns
			4.5V	17	33	41	49	ns
			6.0V	15	28	35	42	ns
t_{REM}	Minimum Removal Time Clear to Clock		2.0V		25	25	25	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per counter)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

AC Electrical Characteristics MM54HC393/MM74HC393

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

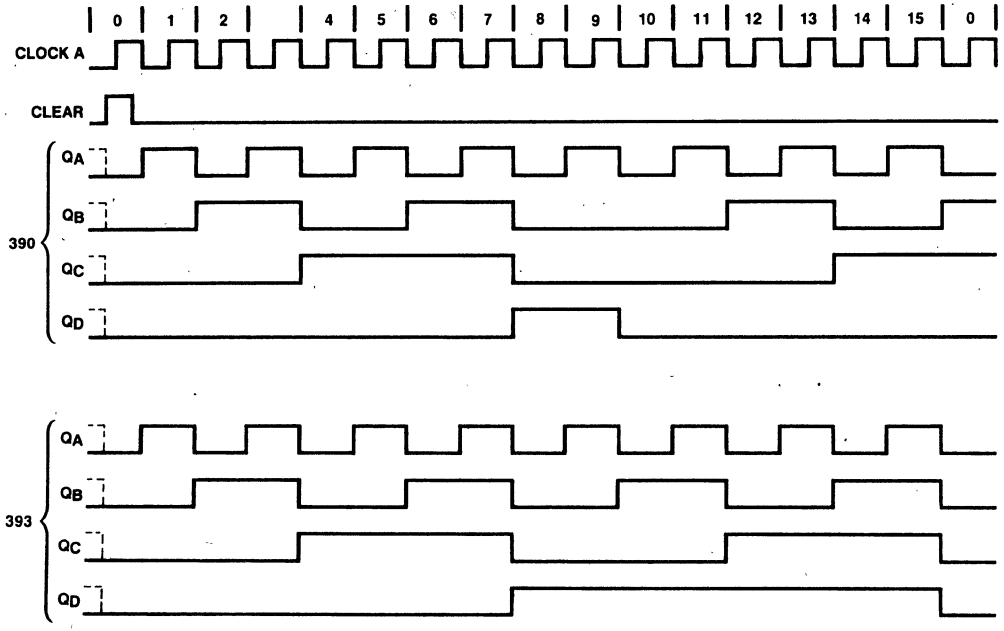
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_A		13	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_B		19	35	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_C		23	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock A to Q_D		27	50	ns
t_{PHL}	Maximum Propagation Delay, Clear to any Q		15	28	ns
t_{REM}	Minimum Removal Time		−2	5	ns
t_W	Minimum Pulse Width Clear or Clock		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	5	4	3	
			4.5V	27	21	18	MHz
			6.0V	31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_A		2.0V	45	120	150	180	ns
			4.5V	15	24	30	35	ns
			6.0V	13	21	26	31	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_B		2.0V	68	190	240	285	ns
			4.5V	23	38	47	57	ns
			6.0V	20	32	40	48	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock A to Q_C		2.0V	90	240	300	360	ns
			4.5V	30	48	60	72	ns
			6.0V	26	41	51	61	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_D		2.0V	100	290	360	430	ns
			4.5V	35	58	72	87	ns
			6.0V	30	50	62	75	ns
t_{PHL}	Maximum Propagation Delay Clear to any Q		2.0V	54	165	210	250	ns
			4.5V	18	33	41	49	ns
			6.0V	15	28	35	42	ns
t_{REM}	Minimum Clear Removal Time		2.0V		25	25	25	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width Clear or Clock		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per counter)		42				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Timing Waveforms



TL/F/5337–3

National Semiconductor

microCMOS

MM54HC423A/MM74HC423A
Dual Retriggerable Monostable Multivibrator

General Description

The MM54/74HC423A high speed monostable multivibrators (one shots) utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC423A cannot be triggered from clear.

The 'HC423A is retriggerable. That is, it may be triggered repeatedly while its outputs are generating a pulse and the pulse will be extended.

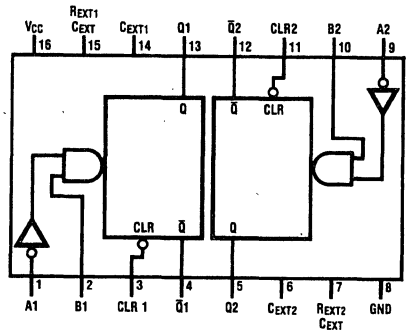
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: $PW = (R_{EXT})(C_{EXT})$; where PW is in seconds, R is in ohms, and C is in farads. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 40 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Simple pulse width formula T = RC
- Wide pulse range: 400 ns to ∞ (typ)
- Part to part variation: $\pm$5% (typ)
- Schmitt Trigger A & B inputs allow infinite rise and fall times on these inputs

Connection Diagram

Dual-In-Line Package

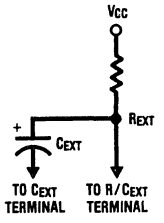


TL/F/5338–1

Top View

Order Number MM54HC423AJ or MM74HC423AJ, N
See NS Package J16A or N16E

Timing Component



TL/F/5338–2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎏
H	↓	H	⎍	⎏

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎏ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Maximum Input Rise and Fall Time (Clear Input)			
V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤ 20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\|$≤ 4.0 mA	4.5V		3.96	3.84	3.7	V
		$\|I_{OUT}\|$≤ 5.2 mA	6.0V		5.46	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL}						V
		$\|I_{OUT}\|$≤4 mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤5.2 mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 7, 15)	V_{IN}=V_{CC} or GND	5.0V		0.5	5.0	5.0	μA
I_{IN}	Maximum Input Current (all other pins)	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (standby)	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA
I_{CC}	Maximum Active Supply Current (per monostable)	V_{IN}=V_{CC} or GND	2.0V	36	80	110	130	μA
		R/C_{EXT}=0.5V_{CC}	4.5V	0.33	1.0	1.3	1.6	mA
			6.0V	0.7	2.0	2.6	3.2	mA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C Ceramic "J" Package: −12mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

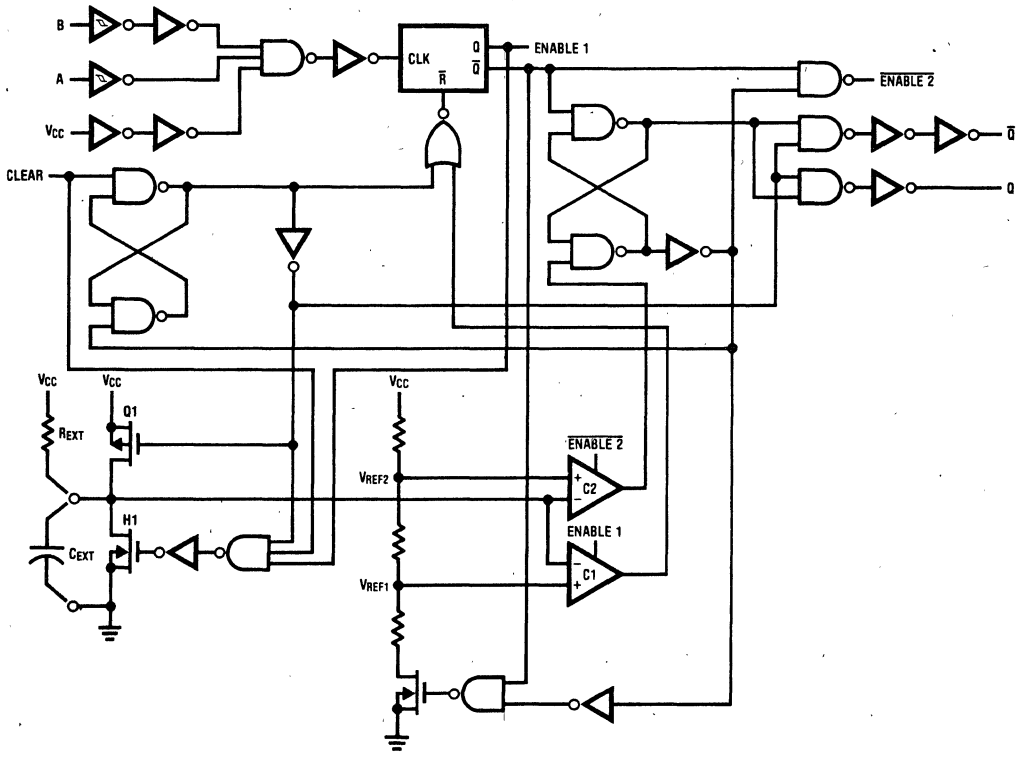
AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Trigger Propagation Delay, A, B to Q		22	33	ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B to $\overline{Q}$		25	42	ns
t_{PHL}	Maximum Propagation Delay, Clear to Q		20	27	ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$		22	33	ns
t_W	Minimum Pulse Width, A, B or Clear		14	26	ns
t_{REM}	Minimum Clear Removal Time			0	ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ	400		ns
t_{WQ}	Output Pulse Width	$C_{EXT}=1000$ pF $R_{EXT}=10$ kΩ	10		μs

AC Electrical Characteristics $C_L=50$ pF $t_r=t_f=6$ ns (Unless otherwise specified)

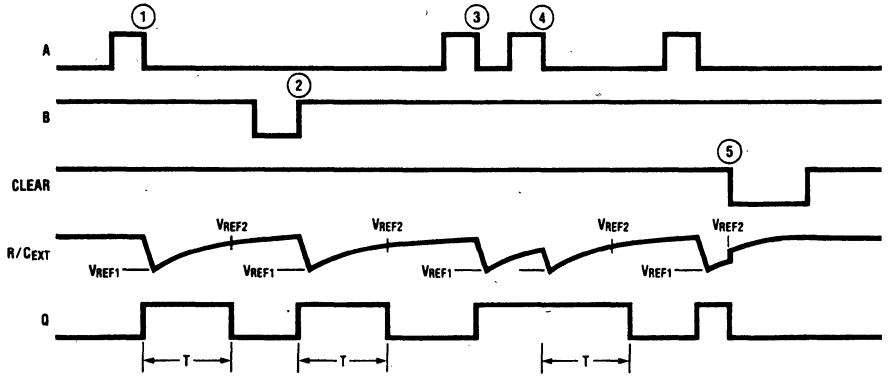
Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$ Typ	74HC $T_A=-40$ to 85°C Guaranteed Limits	54HC $T_A=-55$ to 125°C Guaranteed Limits	Units
t_{PLH}	Maximum Trigger Propagation Delay, A, B or Clear to Q			2.0V 4.5V 6.0V	77 26 21	169 42 32	194 51 39	210 57 44	ns ns ns
t_{PHL}	Maximum Trigger Propagation Delay, A, B or Clear to $\overline{Q}$			2.0V 4.5V 6.0V	88 29 24	197 48 38	229 60 46	250 67 51	ns ns ns
t_{PHL}	Maximum Propagation Delay, Clear to Q			2.0V 4.5V 6.0V	54 23 19	114 34 28	132 41 33	143 45 36	ns ns ns
t_{PLH}	Maximum Propagation Delay, Clear to $\overline{Q}$			2.0V 4.5V 6.0V	56 25 20	116 36 29	135 42 34	147 46 37	ns ns ns
t_W	Minimum Pulse Width A, B, Clear			2.0V 4.5V 6.0V	57 17 12	123 30 21	144 37 27	157 42 30	ns ns ns
t_{REM}	Minimum Clear Removal Time			2.0V 4.5V 6.0V	0 0 0	0 0 0	0 0 0	0 0 0	ns ns ns
$t_{WQ(MIN)}$	Minimum Output Pulse Width	$C_{EXT}=28$ pF $R_{EXT}=2$ kΩ $R_{EXT}=6$ kΩ ($V_{CC}=2V$)		2.0V 4.5V 6.0V	1.5 450 380				μs ns ns
t_{WQ}	Output Pulse Width	$C_{EXT}=0.1$ μF $R_{EXT}=10$ kΩ	Min	4.5V	1	0.9			ms
			Max	4.5V	1	1.1			ms
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V 4.5V 6.0V	30 8 7	75 15 13	95 19 16	110 22 19	ns ns ns
C_{IN}	Maximum Input Capacitance (Pins 7 & 15)				12	20	20	20	pF
C_{IN}	Maximum Input Capacitance (other inputs)				6	10	10	10	pF

Logic Diagram



TL/F/5338–5

Theory of Operation



① POSITIVE EDGE TRIGGER
② NEGATIVE EDGE TRIGGER
③ POSITIVE EDGE TRIGGER
④ POSITIVE EDGE RE-TRIGGER (PULSE LENGTHENING)
⑤ RESET PULSE SHORTENING

TL/F/5338–6

FIGURE 1

Theory of Operation

TRIGGER OPERATION

As shown in *Figure 1* and the logic diagram before an input trigger occurs, the one-shot is in the quiescent state with the Q output low, and the timing capacitor C_{EXT} completely charged to V_{CC}. When the trigger input A goes from V_{CC} to GND (while inputs B and clear are held to V_{CC}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1 ①. At the same time the output latch is set. With transistor N1 on, the capacitor C_{EXT} rapidly discharges toward GND until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_{EXT} begins to charge through the timing resistor, R_{EXT}, toward V_{CC}. When the voltage across C_{EXT} equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the one-shot in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from GND to V_{CC} (while input A is at GND and input clear is at V_{CC} ②.)

It should be noted that in the quiescent state C_{EXT} is fully charged to V_{CC} causing the current through resistor R_{EXT} to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the 'HC423A is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_{EXT}, R_{EXT}, or the duty cycle of the input waveform.

RETRIGGER OPERATION

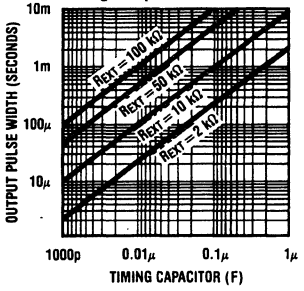
The 'HC423A is retriggered if a valid trigger occurs ③ followed by another trigger ④ before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin or has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated ④, the voltage at the R/C_{EXT} pin will again drop to V_{REF1} before progressing along the RC charging curve toward V_{CC}. The Q output will remain high until time T, after the last valid retrigger.

Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit, the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

RESET OPERATION

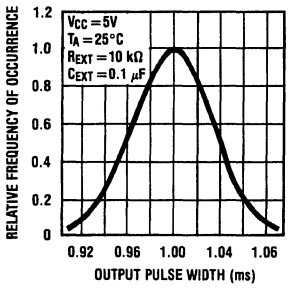
These one shots may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on clear sets the reset latch and causes the capacitor to be fast charged to V_{CC} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the clear input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the Clear input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Output Pulse Width vs. Timing Components



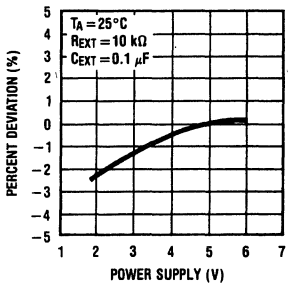
TL/F/5338–7

Typical Distribution of Output Pulse Width, Part to Part



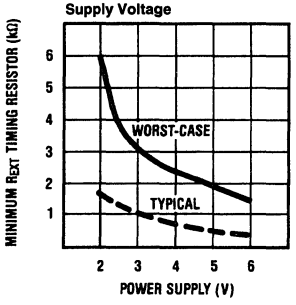
TL/F/5338–8

Typical 1ms Pulse Width Variation vs. Supply



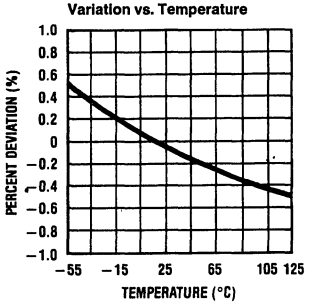
TL/F/5338–9

Minimum R_{EXT} vs. Supply Voltage



TL/F/5338–10

Typical 1ms Pulse Width Variation vs. Temperature



TL/F/5338–11

Note: R and C are not subjected to temperature. The C is polypropylene.

National Semiconductor

microCMOS

MM54HC521/MM74HC521
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to compare bit for bit two 8-bit words and indicates whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

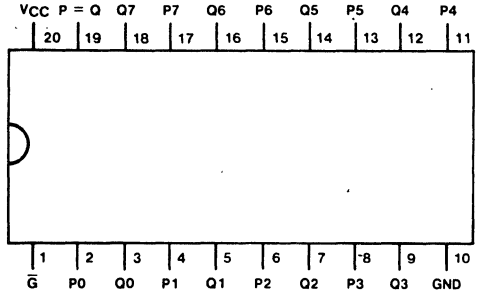
The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 54LS688/74LS688. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA (74 Series)
- Large output current: 4 mA (74 Series)

Connection and Logic Diagrams

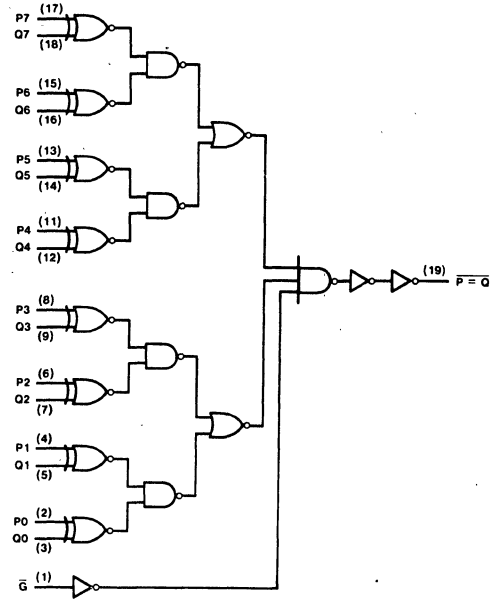
Dual-In-Line Package



TL/F/6128–1

Top View

Order Number MM54HC521J or MM74HC521J,N
See NS Package J20A or N20A



TL/F/6128–2

Truth Table

Inputs		
Data P,Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

3

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any P or Q to Output		21	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to any Output		14	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	175	220	263	ns
			4.5V	22	35	44	53	ns
			6.0V	19	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	120	150	180	ns
			4.5V	15	24	30	36	ns
			6.0V	13	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			45				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC533/MM74HC533 TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed OCTAL D-TYPE LATCHES utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the inversion of the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

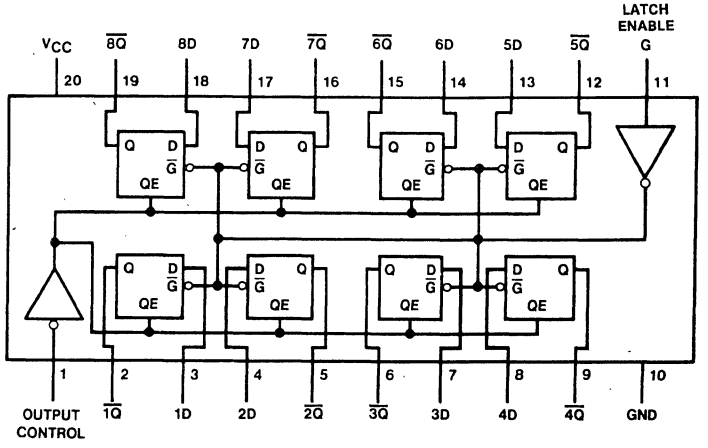
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA, maximum (74HC Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5339–1

Top View

Order Number MM54HC533J or MM74HC533J, N
See NS Package J20A or N20A

Truth Table

Output Control	Latch Enable G	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN}=V_{IH} or V_{IL}, OC=V_{IH} V_{OUT}=V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	18	25	ns
t_S	Minimum Set Up Time			5	ns
t_H	Minimum Hold Time			10	ns
t_W	Minimum Pulse Width			16	ns

AC Electrical Characteristics $V_{CC}=2.0V$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	22	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to $\overline{Q}$	$C_L=50$ pF	2.0V	63	175	220	263	ns
		$C_L=150$ pF	2.0V	110	225	280	338	ns
		$C_L=50$ pF	4.5V	25	35	44	52	ns
		$C_L=150$ pF	4.5V	35	45	56	68	ns
		$C_L=50$ pF	6.0V	21	30	37	45	ns
		$C_L=150$ pF	6.0V	28	39	49	59	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	188	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	26	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ	2.0V	50	150	188	225	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Set Up Time		2.0V	5	25	31	38	ns
			4.5V	2	5	6	8	ns
			6.0V	2	5	6	8	ns
t_H	Minimum Hold Time		2.0V	20	50	60	75	ns
			4.5V	6	10	13	20	ns
			6.0V	6	10	13	20	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	9	14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time, Clock	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per latch)						
		OC = V_{CC}		30				pF
		OC = Gnd		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC534/MM74HC534 TRI-STATE® Octal D-Type Flip-Flop with Inverted Outputs

General Description

These high speed Octal D-Type Flip-Flops utilize micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

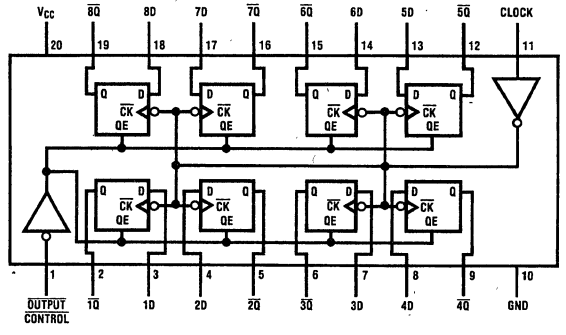
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5340–1

Top View

Order Number MM54HC534J or MM74HC534J,N
See NS Package J20A or N20A

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
$\overline{Q}_0$ = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{IN} = V_{IH} or V_{IL}, OC = V_{IH} V_{OUT} = V_{CC} or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency			35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to $\overline{Q}$	$C_L=45$ pF	23	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	21	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	19	25	ns
t_S	Minimum Setup Time		10	20	ns
t_H	Minimum Hold Time		0	5	ns
t_W	Minimum Pulse Width		9	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF	2.0V	68	180	225	270	ns
		$C_L=150$ pF	2.0V	110	230	288	345	ns
		$C_L=50$ pF	4.5V	22	36	45	48	ns
		$C_L=150$ pF	4.5V	30	46	57	69	ns
		$C_L=50$ pF	6.0V	20	31	39	46	ns
		$C_L=150$ pF	6.0V	28	40	50	60	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	50	150	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	29	40	50	60	ns
		$C_L=50$ pF	6.0V	19	26	31	39	ns
		$C_L=150$ pF	6.0V	25	35	44	53	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	50	150	189	225	ns
			4.5V	21	30	37	45	ns
			6.0V	19	26	31	39	ns
t_S	Minimum Setup Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_r, t_f	Maximum Input Rise and Fall Time Clock				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)						
		OC=V_{CC}		30				pF
		OC=Gnd		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HC540/MM74HC540 Inverting Octal TRI-STATE® Buffer
MM54HC541/MM74HC541 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity, and low power consumption. Both devices have a fanout of 15 LS-TTL equivalent inputs.

The MM54HC540/MM74HC540 is an inverting buffer and the MM54HC541/MM74HC541 is a non-inverting buffer. The TRI-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

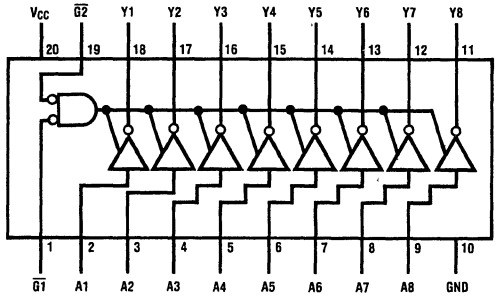
In order to enhance PC board layout, the 'HC540 and 'HC541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74HC Series)
- Output current: 6 mA

Connection Diagrams

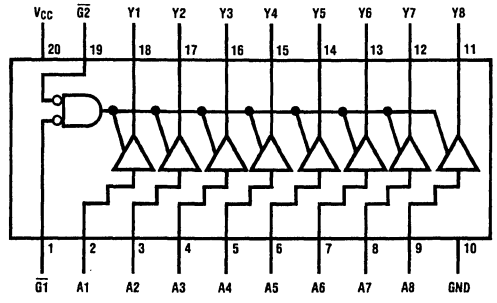
Dual-In-Line Package



TL/F/5341–1

Top View
Order Number MM54HC540J or MM74HC540J, N
See NS Package J20A or N20A

Dual-In-Line Package



TL/F/5341–2

Top View
Order Number MM54HC541J or MM74HC541J, N
See NS Package J20A or N20A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	$V_{IN}=V_{IH}$ or V_{IL}, $\overline{G}=V_{IH}$ $V_{OUT}=V_{CC}$ or GND	6.0V		±0.5	±5	±10	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	$C_L=45$ pF	12	18	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	$C_L=45$ pF	14	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=$ kΩ $C_L=5$ pF	15	25	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay (540)	$C_L=50$ pF	2.0V	55	100	126	149	ns
		$C_L=150$ pF	2.0V	83	150	190	224	ns
		$C_L=50$ pF	4.5V	12	20	25	30	ns
		$C_L=150$ pF	4.5V	22	30	38	45	ns
		$C_L=50$ pF	6.0V	11	17	21	25	ns
		$C_L=150$ pF	6.0V	18	26	32	38	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay (541)	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	83	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	11	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	75	150	189	224	ns
			4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	OC=V_{CC}		10				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC563/MM74HC563
TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed octal D-type latches utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE (LE) input is high, the $\overline{Q}$ outputs will follow the inversion of the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

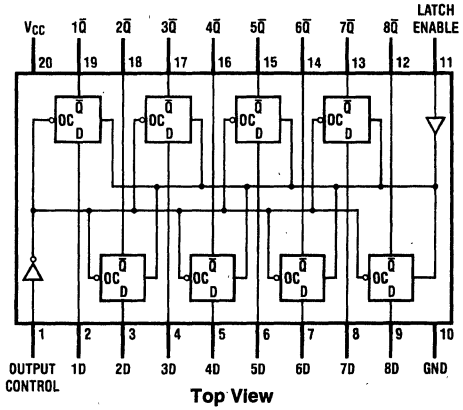
The 54HC/74HC logic family is speed, function and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- Functionally compatible with '580

Connection Diagram

Dual-In-Line Package



Top View

TL/F/5210–1

Order Number MM54HC563J or MM74HC563J, N
See NS Package J20A or N20A

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	L
L	H	L	H
L	L	X	Q0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established

Z = high impedance

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CC})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND OC = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA			8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=45$ pF	12	19	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to $\overline{Q}$	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set Up Time		10	15	ns
t_H	Minimum Hold Time		2	5	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to $\overline{Q}$	$C_L=50$ pF	2.0V	45	110	138	165	ns
		$C_L=150$ pF	2.0V	58	150	188	225	ns
		$C_L=50$ pF	4.5V	14	22	28	33	ns
		$C_L=150$ pF	4.5V	21	30	38	40	ns
		$C_L=50$ pF	6.0V	12	19	24	29	ns
		$C_L=150$ pF	6.0V	19	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to $\overline{Q}$	$C_L=50$ pF	2.0V	46	115	143	173	ns
		$C_L=150$ pF	2.0V	60	155	194	233	ns
		$C_L=50$ pF	4.5V	14	23	29	35	ns
		$C_L=150$ pF	4.5V	21	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	19	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	55	140	175	210	ns
		$C_L=150$ pF	2.0V	67	180	225	270	ns
		$C_L=50$ pF	4.5V	15	28	35	42	ns
		$C_L=150$ pF	4.5V	24	36	45	54	ns
		$C_L=50$ pF	6.0V	14	24	30	36	ns
		$C_L=150$ pF	6.0V	22	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	40	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	12	21	27	32	ns
t_S	Minimum Set Up Time Data to LE		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_H	Minimum Hold Time LE to Data		2.0V		25	31	38	ns
			4.5V		5	6	7	ns
			6.0V		4	5	6	ns
t_W	Minimum Pulse Width, LE or Data		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC=V_{CC}		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC564/MM74HC564 TRI-STATE® Octal D-Type Edge-Triggered Flip-Flop with Inverted Outputs

General Description

These octal D-type flip-flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

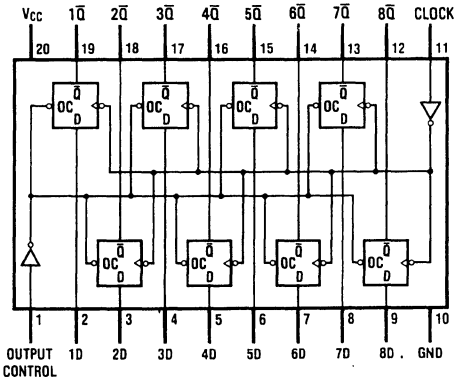
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- Functionally compatible with 54/74LS576

Connection Diagram

Dual-In-Line Package



TL/F/5211–1

Order Number MM54HC564J or MM74HC564J, N
See NS Package J20A or N20A

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High Impedance State
Q_0 = The level of the output before steady state Input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND OC = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Setup Time, Data to Clock			20	ns
t_H	Minimum Hold Time, Clock to Data			0	ns
t_W	Minimum Clock Pulse Width			16	ns

AC Electrical Characteristics

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to $\overline{Q}$	$C_L=50$ pF	2.0V	40	115	143	173	ns
		$C_L=150$ pF	2.0V	51	155	194	233	ns
		$C_L=50$ pF	4.5V	13	23	29	35	ns
		$C_L=150$ pF	4.5V	19	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	18	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	45	140	175	210	ns
		$C_L=150$ pF	2.0V	59	180	225	270	ns
		$C_L=50$ pF	4.5V	14	28	35	42	ns
		$C_L=150$ pF	4.5V	20	36	45	54	ns
		$C_L=50$ pF	6.0V	12	24	30	36	ns
		$C_L=150$ pF	6.0V	18	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	35	125	156	188	ns
			4.5V	12	25	31	38	ns
			6.0V	10	21	27	32	ns
t_S	Minimum Setup Time Data to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_W	Minimum Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	8	16	20	24	ns
			6.0V	7	14	18	20	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC=VCC		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC573/MM74HC573 TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE(LE) input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL OC input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

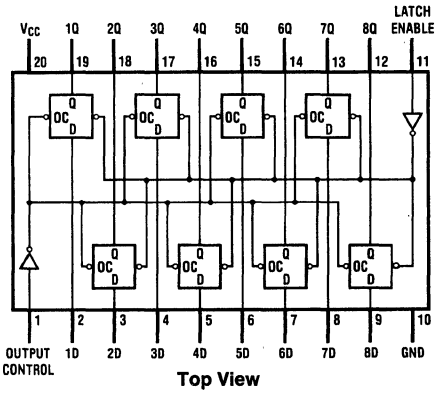
The 54HC/74HC logic family is speed, function and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



Top View

TL/F/5212-1

Order Number MM54HC573J or MM74HC573J, N

See NS Package J20A or N20A

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

X = Don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND OC=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	12	19	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Set Up Time, Data to LE		10	15	ns
t_H	Minimum Hold Time, LE to Data		2	5	ns
t_W	Minimum Pulse Width, LE or Data		10	16	ns

AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Q	$C_L=50$ pF	2.0V	45	110	138	165	ns
		$C_L=150$ pF	2.0V	58	150	188	225	ns
		$C_L=50$ pF	4.5V	14	22	28	33	ns
		$C_L=150$ pF	4.5V	21	30	38	40	ns
		$C_L=50$ pF	6.0V	12	19	24	29	ns
		$C_L=150$ pF	6.0V	19	26	33	39	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Latch Enable to Q	$C_L=50$ pF	2.0V	46	115	143	173	ns
		$C_L=150$ pF	2.0V	60	155	194	233	ns
		$C_L=50$ pF	4.5V	14	23	29	35	ns
		$C_L=150$ pF	4.5V	21	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	19	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	55	140	175	210	ns
		$C_L=150$ pF	2.0V	67	180	225	270	ns
		$C_L=50$ pF	4.5V	15	28	35	42	ns
		$C_L=150$ pF	4.5V	24	36	45	54	ns
		$C_L=50$ pF	6.0V	14	24	30	36	ns
		$C_L=150$ pF	6.0V	22	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	40	125	156	188	ns
			4.5V	13	25	31	38	ns
			6.0V	12	21	27	32	ns
t_S	Minimum Set Up Time Data to LE		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_H	Minimum Hold Time LE to Data		2.0V		25	31	38	ns
			4.5V		5	6	7	ns
			6.0V		4	5	6	ns
t_W	Minimum Pulse Width LE, or Data		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time, Clock	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC=V_{CC}		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC574/MM74HC574
TRI-STATE® Octal D-Type Edge-Triggered Flip-Flop

General Description

These high speed octal D-type flip-flops utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

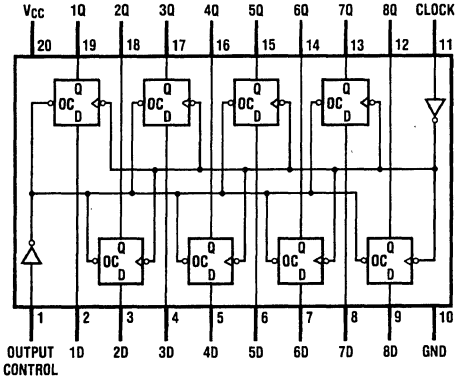
The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide operating voltage range: 2V–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5213–1

Top View

Order Number MM54HC574J or MM74HC574J, N

See NS Package J20A or N20A

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
X = don't care
↑ = transition from low-to-high
Z = high impedance state
Q_0 = the level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND OC = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst-case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst-case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst-case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	35	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12	20	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13	25	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11	20	ns
t_S	Minimum Setup Time, Data to Clock			20	ns
t_H	Minimum Hold Time, Clock to Data			0	ns
t_W	Minimum Pulse Clock Width		8	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		6	5	4	MHz
			4.5V		30	24	20	MHz
			6.0V		35	28	23	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF	2.0V	40	115	143	173	ns
		$C_L=150$ pF	2.0V	51	155	194	233	ns
		$C_L=50$ pF	4.5V	13	23	29	35	ns
		$C_L=150$ pF	4.5V	19	31	47	47	ns
		$C_L=50$ pF	6.0V	12	20	25	30	ns
		$C_L=150$ pF	6.0V	18	27	34	41	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	45	140	175	210	ns
		$C_L=150$ pF	2.0V	59	180	225	270	ns
		$C_L=50$ pF	4.5V	14	28	35	42	ns
		$C_L=150$ pF	4.5V	20	36	45	54	ns
		$C_L=50$ pF	6.0V	12	24	30	36	ns
		$C_L=150$ pF	6.0V	18	31	39	47	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	35	125	156	188	ns
			4.5V	12	25	31	38	ns
			6.0V	10	21	27	32	ns
t_S	Minimum Setup Time Data to Clock		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
t_W	Minimum Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5) (per latch)	OC=VCC		30				pF
		OC=GND		50				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC589/MM74HC589 8-Bit Shift Registers with Input Latches and TRI-STATE® Serial Output

General Description

This high speed shift register utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

The 'HC589 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Data can also be entered serially the shift register through the SER pin. Both the storage register and shift register have positive-edge triggered clocks, RCK and SCK, respectively. $\overline{SLOAD}$ pin controls parallel LOAD or serial shift operations for the shift register. The shift register has a TRI-STATE output to enable the wire-ORing of multiple devices on a serial bus.

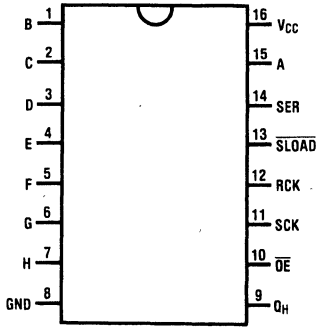
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- 8-bit parallel storage register inputs
- Wide operating voltage range: 2V–6V
- Shift register has direct overriding load
- Guaranteed shift frequency . . . DC to 30 MHz
- Low quiescent current: 80 μA maximum (74HC Series)
- TRI-STATE output for 'Wire-OR'

Connection Diagram

Dual-In-Line Package



TL/F/5368–1

Top View

Order Number MM54HC589J or MM74HC589J,N
See NS Package J16A or N16E

Truth Table

RCK	SCK	$\overline{SLOAD}$	$\overline{OE}$	Function
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	X	L	Serial output in high impedance state
X	↑	H	H	Shift register clocked $Q_N = Q_{n-1}$, Q_O = SER

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency for SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q_H'			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SLOAD}$ to Q_H'			30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from LCK to Q_H'	$\overline{SLOAD}$ = logic '0'	25	45	ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L=1$ kΩ	18	28	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$R_L=1$ kΩ, $C_L=5$ pF	19	25	ns
t_S	Minimum Setup Time from RCK to SCK		10	20	ns
t_S	Minimum Setup Time from SER to SCK		10	20	ns
t_S	Minimum Setup Time from Inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		0	5	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SLOAD}$		8	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency for SCK		2.0V		5	4	4	MHz
			4.5V		27	21	18	MHz
			6.0V		32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK or $\overline{SLOAD}$ to Q_H		2.0V	62	175	220	266	ns
			4.5V	20	35	43	52	ns
			6.0V	18	30	37	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK or $\overline{SLOAD}$ to Q_H	$C_L=150$ pF	2.0V	120	225	284	335	ns
			4.5V	31	45	57	67	ns
			6.0V	28	38	48	57	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_H		2.0V	80	210	265	313	ns
			4.5V	25	42	53	63	ns
			6.0V	21	36	45	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay RCK to Q_H	$C_L=150$ pF	2.0V	80	210	265	313	ns
			4.5V	25	52	66	77	ns
			6.0V	21	44	56	66	ns
t_{PZH}, t_{PZL}	Output Enable Time	$R_L=1$ kΩ	2.0V	70	150	189	224	ns
			4.5V	22	30	38	45	ns
			6.0V	20	26	32	38	ns
t_{PHZ}, t_{PLZ}	Output Disable Time	$R_L=1$ kΩ	2.0V	70	150	189	224	ns
			4.5V	22	30	38	45	ns
			6.0V	20	26	32	38	ns
t_S	Minimum Setup Time from RCK to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_S	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_S	Minimum Setup Time from Inputs A thru H to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	22	25	ns
t_H	Minimum Hold Time		2.0V	−5	5	5	5	ns
			4.5V	0	5	5	5	ns
			6.0V	1	5	5	5	ns

AC Electrical Characteristics (Continued)

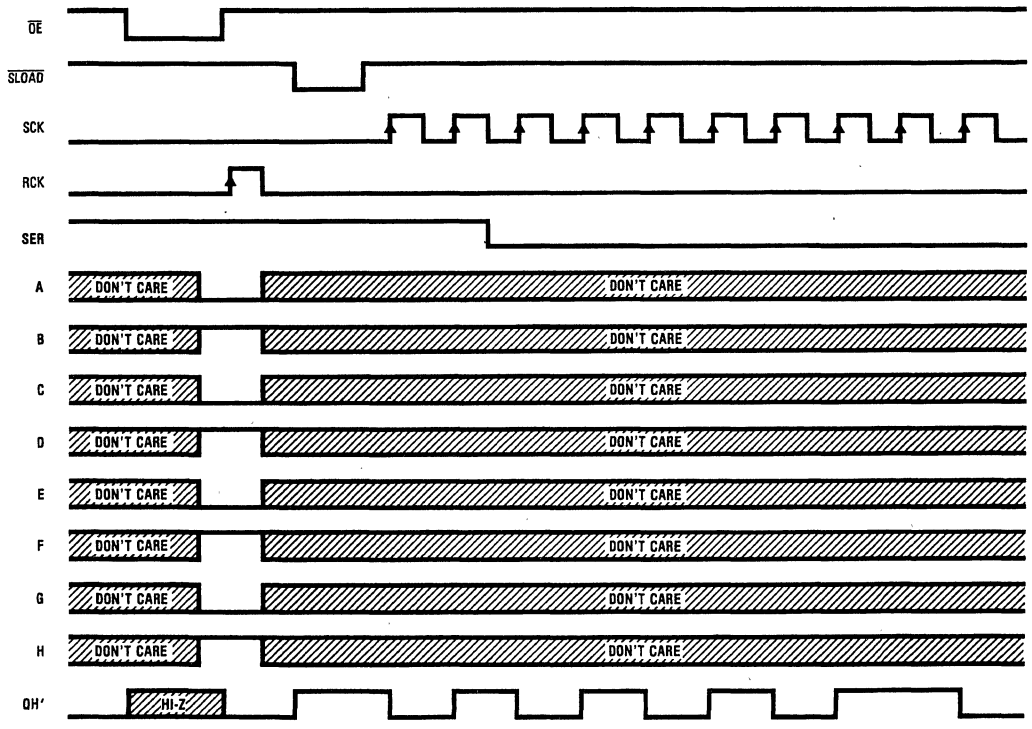
V_{CC} = 2.0–6V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to 85°C	54HC $T_A = -55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_W	Minimum Pulse Width SCK, RCK, $\overline{SLOAD}$, $\overline{SLOAD}$		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1500	1500	1500	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	12	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ sf + I_{CC}$.

Logic Timing Diagram

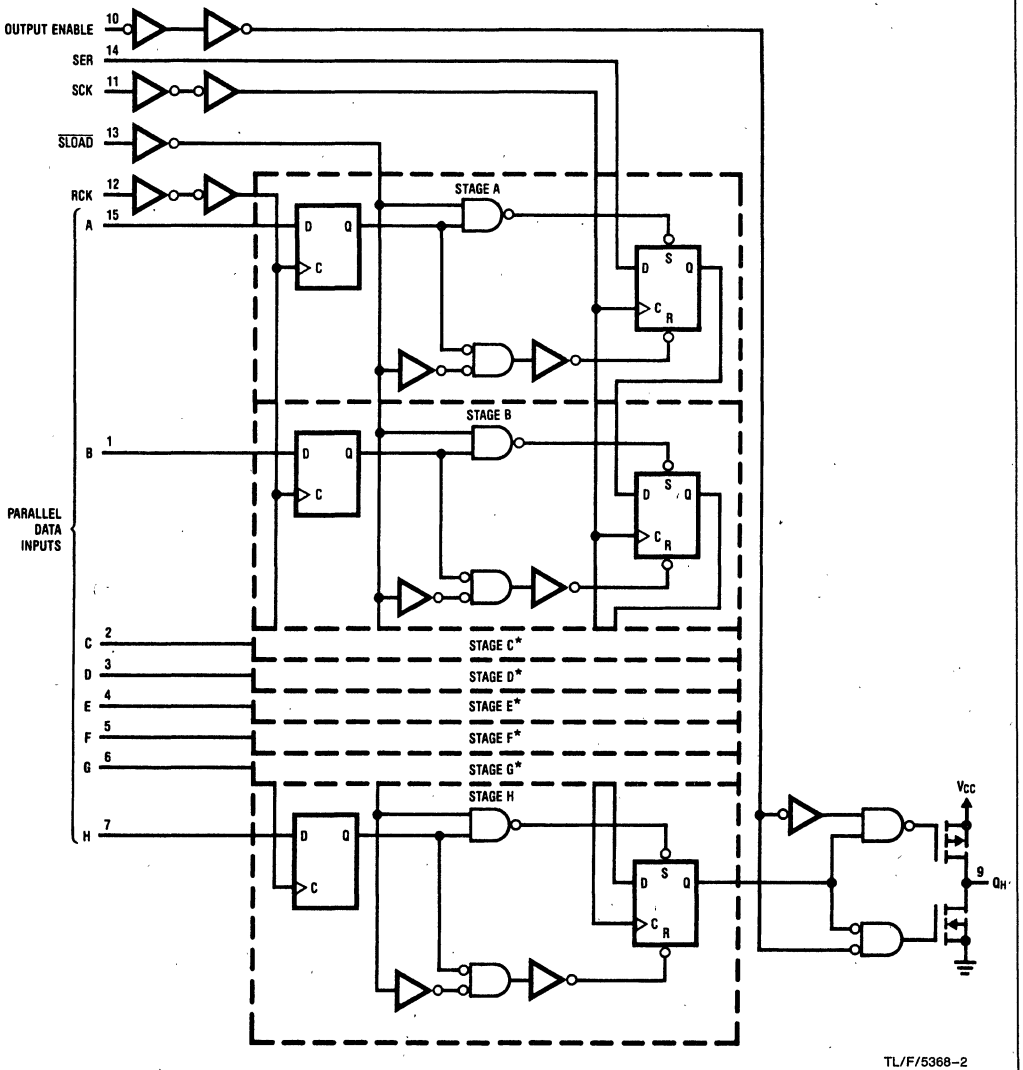
MM54HC589/MM74HC589



TL/F/5368–3

Functional Block Diagram (positive logic)

MM54HC589/MM74HC589



TL/F/5368–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC590/MM74HC590 8-Bit Binary Counter with TRI-STATE® Output Register

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high performance. These devices retain the low power and high noise immunity of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits.

The MM54HC590/MM74HC590 contain an 8-bit binary counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{\text{CCKEN}}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{\text{RCO}}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{\text{RCO}}$ of the first stage to the $\overline{\text{CCKEN}}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{\text{RCO}}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed TRI-STATE outputs which are enabled when the enable input, G, is taken low. This enables connection of this part to a system bus.

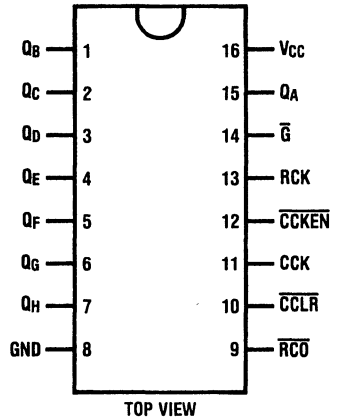
The MM54HC590/MM74HC590 are functional, speed and pin equivalent to the equivalent LS-TTL circuit. Its inputs are protected from damage due to the electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 2.0V to 6.0V
- High input noise immunity
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HC)

Connection Diagram

Dual-In-Line Package

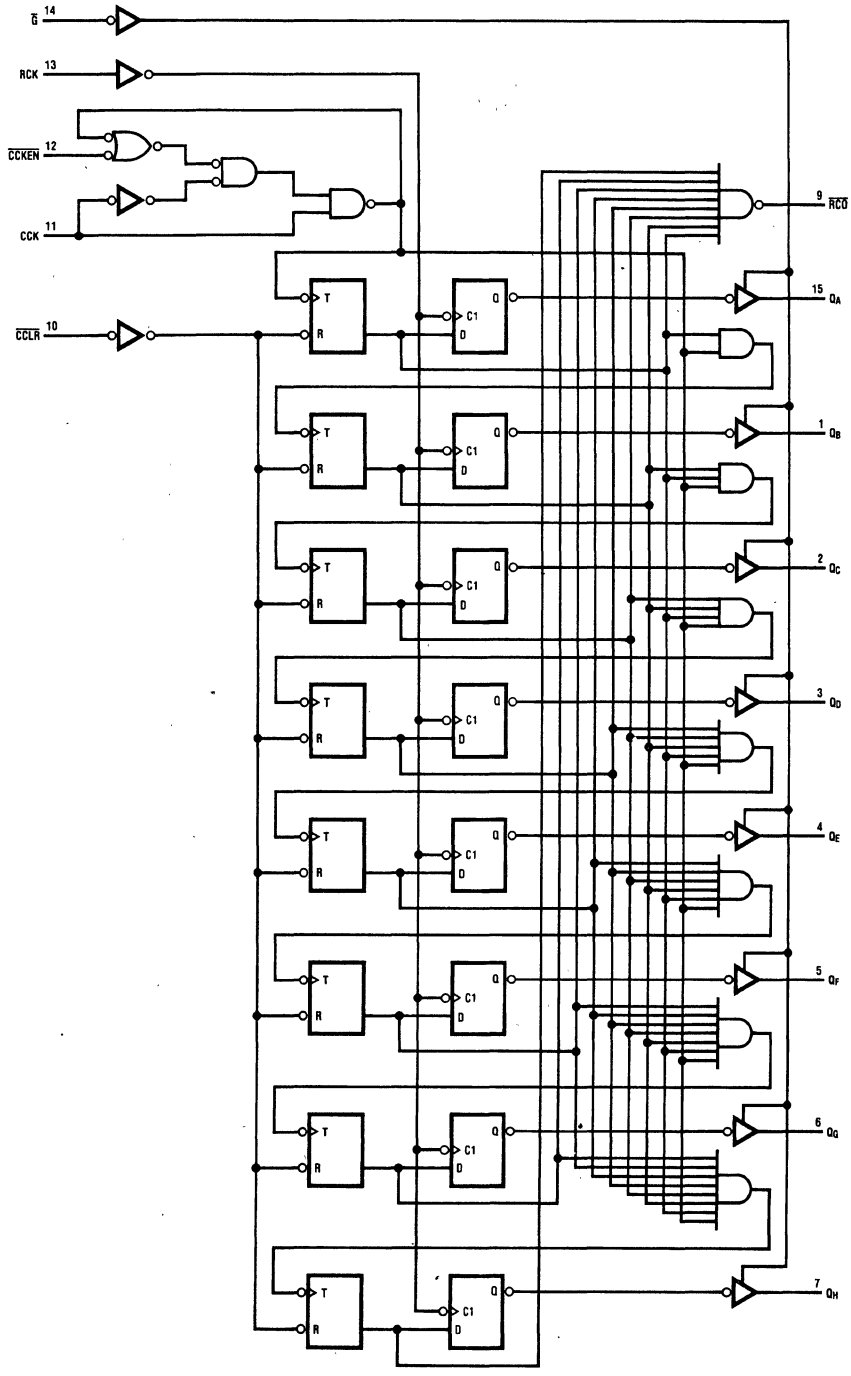


TOP VIEW

TL/F/5772–1

Order Number MM54HC590J or MM74HC590J, N
See NS Package J16A or N16E

Logic Diagram



TL/F/5772–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HC592/MM74HC592 8-Bit Binary Counter with Input Register MM54HC593/MM74HC593 8-Bit Binary Counter with Bidirectional Input Register/Counter Outputs

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high performance. These devices retain the low power and high noise immunity of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits.

The MM54HC592/MM74HC592 and the MM54HC593/MM74HC593 contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{CCKEN}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{RCO}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{RCO}$ of the first stage to the $\overline{CCKEN}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{RCO}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, $\overline{CLOAD}$, input is taken low.

The 'HC592 differs from the 'HC593 in that the latter device has bidirectional input/output pins. The TRI-STATE® outputs of the counter can be enabled and are active when enable input, $\overline{G}$, is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The 'HC593 also has a second clock enable pin, $\overline{CCKEN}$, which is active high and it also has an active low register clock enable, $\overline{RCKEN}$.

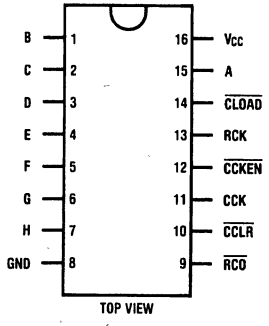
The MM54HC592/MM74HC592 and the MM54HC593/MM74HC593 are functional, speed and pin equivalent to the equivalent LS-TTL circuit. Their inputs are protected from damage due to electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 2.0V to 6.0V
- High input noise immunity
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HC)

Connection Diagrams

Dual-In-Line Package
MM54HC592/MM74HC592

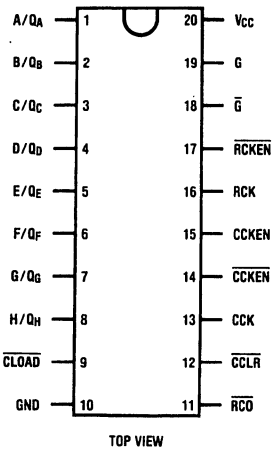


TOP VIEW

TL/F/5773–1

Order Number MM54HC592J, MM54HC593J, MM74HC592J, N or MM74HC593J, N
See NS Package J16A, J20A, N16E or N20A

Dual-In-Line Package
MM54HC593/MM74HC593

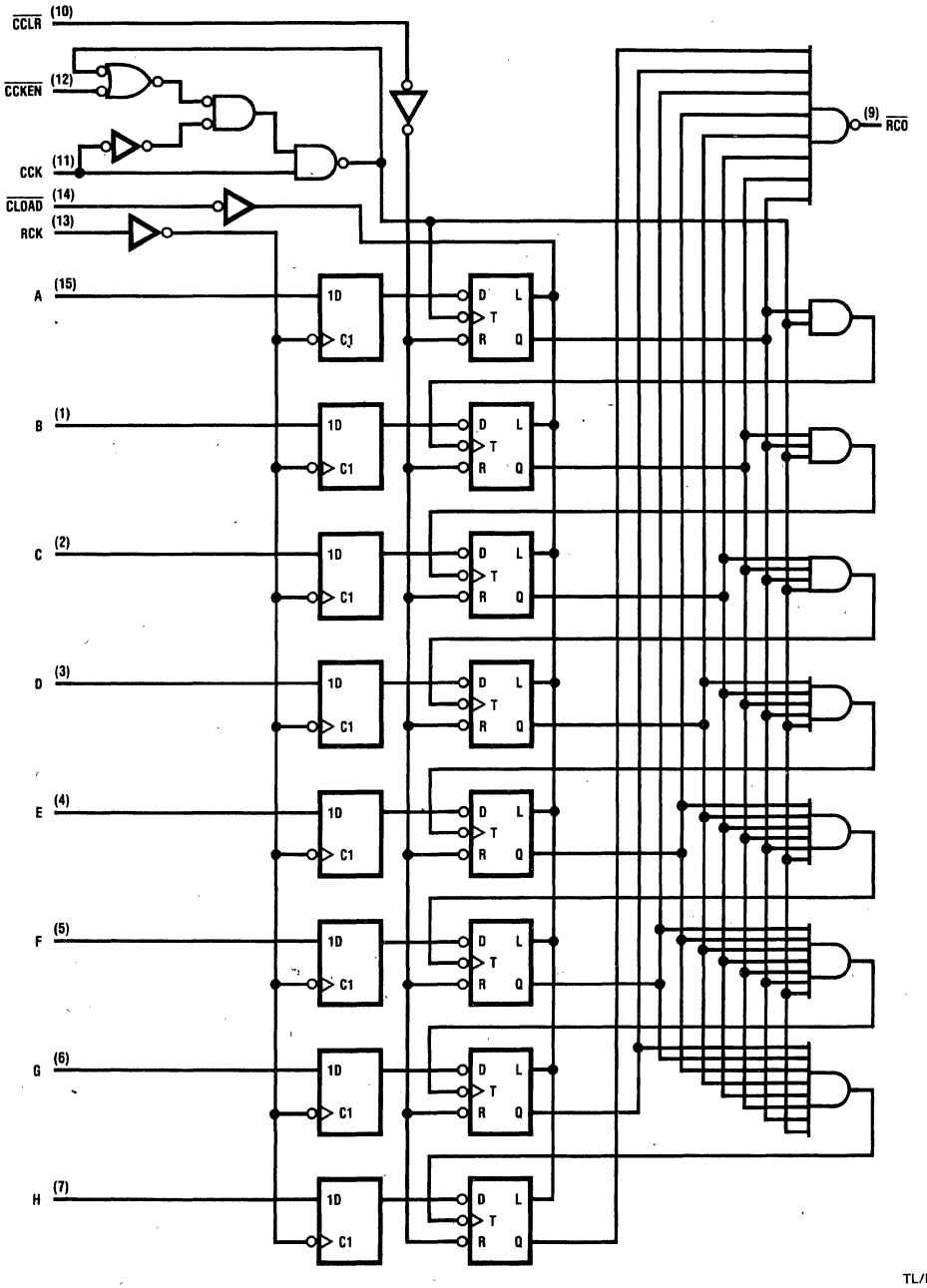


TOP VIEW

TL/F/5773–2

Logic Diagrams

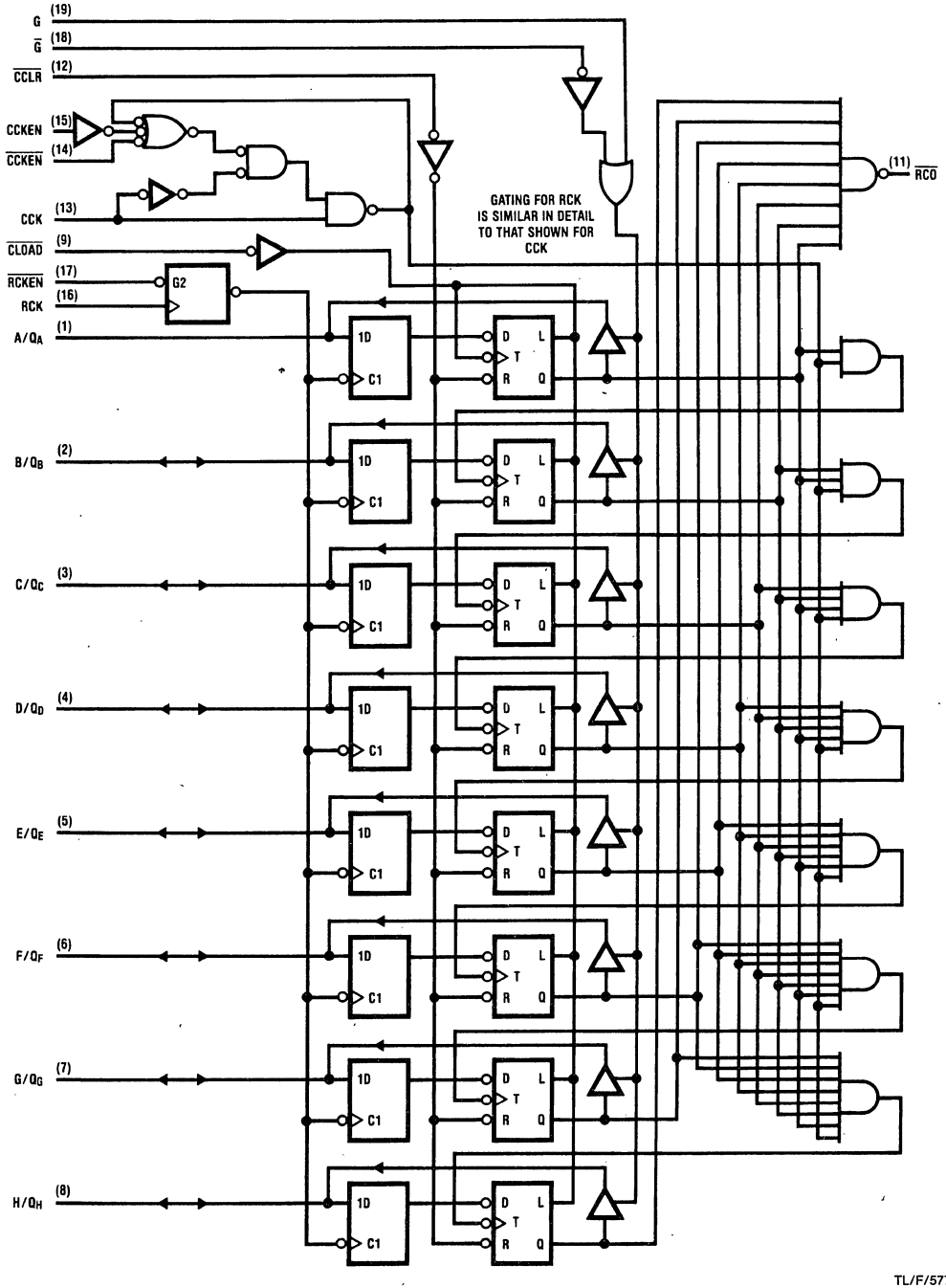
MM54/74HC592



TL/F/5773–4

Logic Diagrams (Continued)

MM54/74HC593



TL/F/5773–3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC595/MM74HC595
8-Bit Shift Registers with Output Latches

General Description

This high speed shift register utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 TRI-STATE® outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

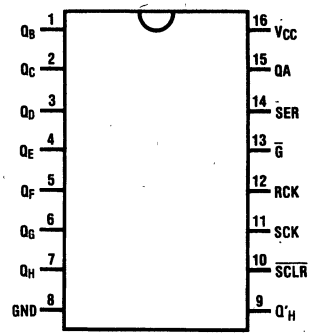
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz

Connection Diagram

Dual-In-Line Package



TL/F/5342–1

Top View

Order Number MM54HC595J or MM74HC595J, N
See NS Package J16A or N16E

Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{G}$	Function
X	X	X	1	Q_A thru Q_H = TRI-STATE
X	X	L	X	Shift Register cleared $Q'_H = 0$
X	↑	H	X	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER
↑	X	H	X	Contents of Shift Register transferred to output latches

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	$Q_{H'}$	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
	Q_A thru Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	$Q_{H'}$	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
	Q_A thru Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to $Q_{H'}$	$C_L=45$ pF	12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, RCK to Q_A thru Q_H	$C_L=45$ pF	18	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time from $\overline{G}$ to Q_A thru Q_H	$R_L=1$ kΩ $C_L=45$ pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to Q_A thru Q_H	$R_L=$ kΩ $C_L=5$ pF	15	25	ns
t_S	Minimum Setup Time from SER to SCK			20	ns
t_S	Minimum Setup Time from $\overline{SCLR}$ to SCK			20	ns
t_S	Minimum Setup Time from SCK to RCK (See Note 5)			40	ns
t_H	Minimum Hold Time from SER to SCK			0	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

Note 5: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

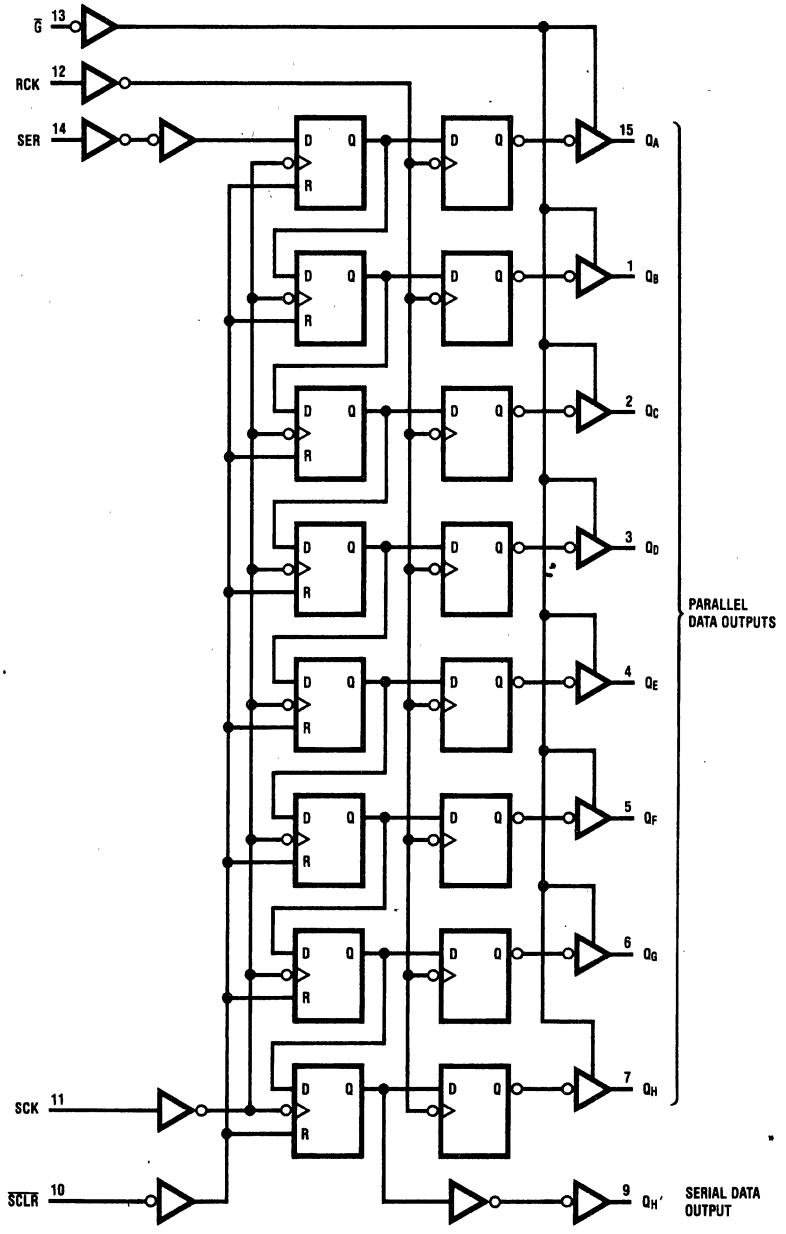
AC Electrical Characteristics $V_{CC}=2.0-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	50	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to $Q_{H'}$	$C_L=50$ pF	2.0V	58	115	145	171	ns
		$C_L=150$ pF	2.0V	83	165	208	246	ns
		$C_L=50$ pF	4.5V	14	23	29	34	ns
		$C_L=150$ pF	4.5V	17	33	42	49	ns
		$C_L=50$ pF	6.0V	10	20	25	29	ns
		$C_L=150$ pF	6.0V	14	28	35	42	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_A thru Q_H	$C_L=50$ pF	2.0V	70	150	188	225	ns
		$C_L=150$ pF	2.0V	105	200	225	250	ns
		$C_L=50$ pF	4.5V	21	30	38	45	ns
		$C_L=150$ pF	4.5V	28	40	50	60	ns
		$C_L=50$ pF	6.0V	18	26	33	39	ns
		$C_L=150$ pF	6.0V	26	34	43	51	ns
t_{PZH}, t_{PZL}	Maximum Output Enable from $\overline{G}$ to Q_A thru Q_H	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	75	150	189	224	ns
		$C_L=150$ pF	2.0V	100	200	252	298	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
		$C_L=150$ pF	4.5V	20	40	50	60	ns
		$C_L=50$ pF	6.0V	13	26	32	38	ns
		$C_L=150$ pF	6.0V	17	34	43	51	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to Q_A thru Q_H	$R_L=1$ kΩ	2.0V	75	150	189	224	ns
		$C_L=50$ pF	4.5V	15	30	38	45	ns
			6.0V	13	26	32	38	ns
t_S	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Setup Time from $\overline{SCLR}$ to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Setup Time from SCK to RCK		2.0V		200	250	300	ns
			4.5V		40	50	60	ns
			6.0V		34	42	50	ns
t_H	Minimum Hold Time SER to SCK		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of SCK or RCLK		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	22	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	60	75	90	ns
			4.5V	7	12	15	18	ns
			6.0V	6	10	13	15	ns
C_{PD}	Power Dissipation Capacitance, Outputs Enabled (Note 6)	$\overline{G}=V_{CC}$		90				pF
		$\overline{G}=GND$		150				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

3

Logic Diagram (positive logic)



TL/F/5342–3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC597/MM74HC597
8-Bit Shift Registers with Input Latches

General Description

This high speed shift register utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

The 'HC597 comes in a 16-pin package and consists of an 8-bit storage latch feeding a parallel-in, serial-out 8-bit shift register. Both the storage register and shift register have positive-edge triggered clocks. The shift register also has direct load (from storage) and clear inputs.

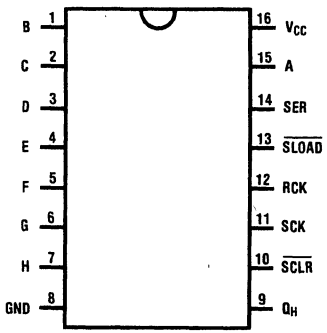
The 54HC/74HC logic family is speed, function, and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- 8-bit parallel storage register inputs
- Wide operating voltage range: 2V–6V
- Shift register has direct overriding load and clear
- Guaranteed shift frequency . . . DC to 30 MHz
- Low quiescent current: 80 μA maximum

Connection Diagram

Dual-In-Line Package



TL/F/5343–1

Top View

Order Number MM54HC597J or MM74HC597J, N
See NS Package J16A or N16E

Truth Table

RCK	SCK	$\overline{SLOAD}$	$\overline{SCLR}$	Function
↑	X	X	X	Data loaded to input latches
↑	X	L	H	Data loaded from inputs to shift register
No clock edge	X	L	H	Data transferred from input latches to shift register
X	X	L	L	Invalid logic, state of shift register indeterminate when signals removed
X	X	H	L	Shift register cleared
X	↑	H	H	Shift register clocked $Q_n = Q_n\text{-}1$, $Q_0 = SER$

3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		|I_{OUT}|≤5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} |I_{OUT}|≤4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		|I_{OUT}|≤5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency for SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q_H		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SLOAD}$ to Q_H		20	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_H	$\overline{SLOAD}$ = logic'0'	25	45	ns
t_{PHL}	Maximum Propagation Delay from $\overline{SCLR}$ to Q_H		20	30	ns
t_{REM}	Minimum Removal Time, $\overline{SCLR}$ to SCK		10	20	ns
t_S	Minimum Setup Time from RCK to SCK		30	40	ns
t_S	Minimum Setup Time from SER to SCK		10	20	ns
t_S	Minimum Setup Time from Inputs A thru H to RCK		10	20	ns
t_H	Minimum Hold Time		−2	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$ $\overline{SLOAD}$		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

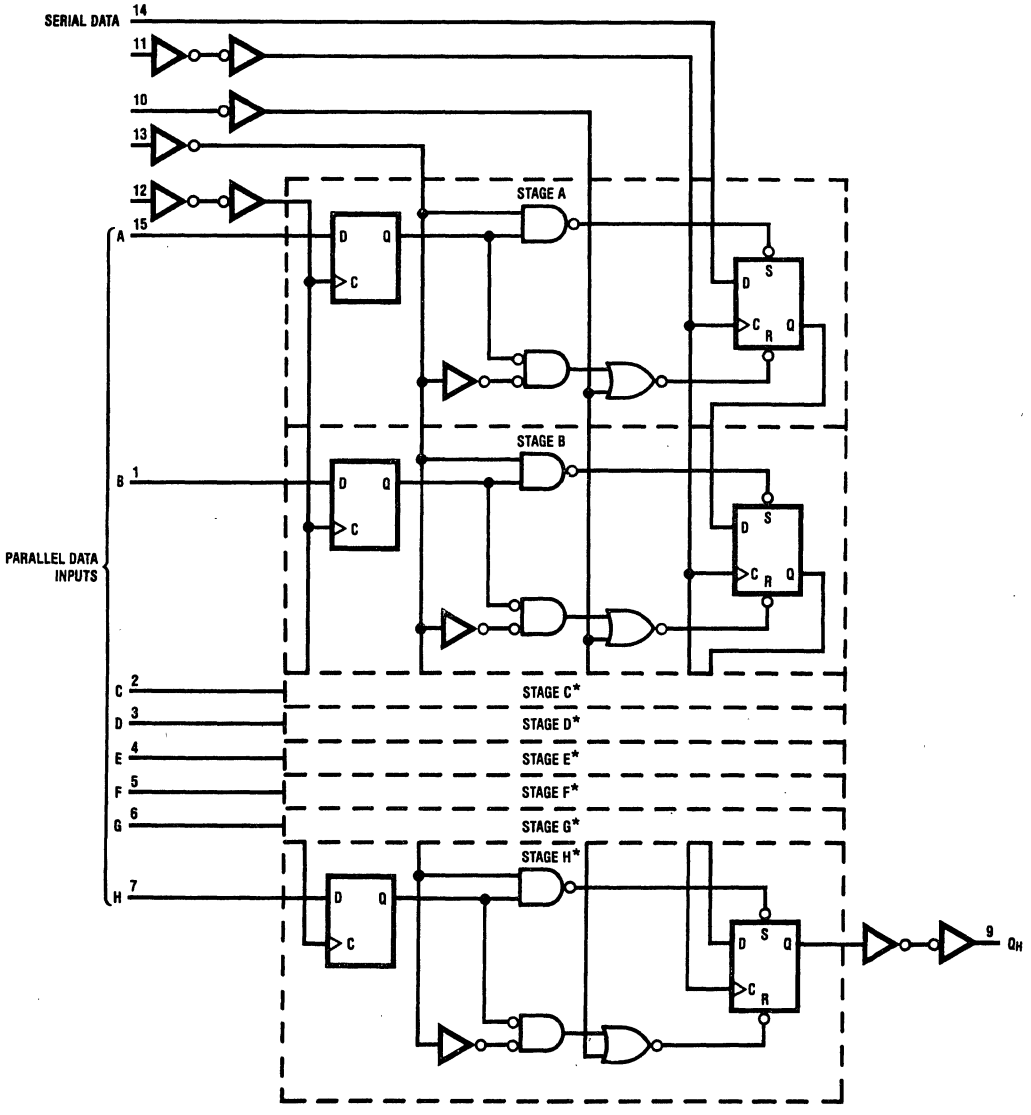
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency for SCK		2.0V	10	5	4	4	MHz
			4.5V	45	27	21	18	MHz
			6.0V	50	32	25	21	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q_H		2.0V	62	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SLOAD}$ to Q_H		2.0V	65	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_H	$\overline{SLOAD}$ = Logic '0'	2.0V	120	250	312	375	ns
			4.5V	30	50	65	75	ns
			6.0V	28	43	53	65	ns
t_{PHL}	Maximum Propagation Delay from $\overline{SCLR}$ to Q_H		2.0V	66	175	220	263	ns
			4.5V	20	35	44	53	ns
			6.0V	18	30	38	45	ns
t_{REM}	Minimum Removal Time $\overline{SCLR}$ to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Setup Time from RCK to SCK		2.0V		200	250	300	ns
			4.5V		40	50	60	ns
			6.0V		34	42	50	ns
t_S	Minimum Setup Time from SER to SCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns

AC Electrical Characteristics (Continued) $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_S	Minimum Setup Time from Inputs A thru H to RCK		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width SCK, RCK, $\overline{SCLR}$, $\overline{SLOAD}$		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	8	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2\ f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Functional Block Diagram (Positive Logic)



TL/F/5343–3

* **NOTE:** Stages C thru G (not shown in detail) are identical to stages A and B above.

National Semiconductor

microCMOS

MM54HC640/MM74HC640 Inverting Octal TRI-STATE® Transceiver MM54HC643/MM74HC643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional buffers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption and high noise immunity usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

Each device has an active enable $\overline{G}$ and a direction control input, DIR. When DIR is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from the B inputs to the A outputs. The MM54HC640/MM74HC640 transfers inverted data from one bus to other and the MM54HC643/MM74HC643 transfers inverted data from the A bus to the B bus and true data from the B bus to the A bus.

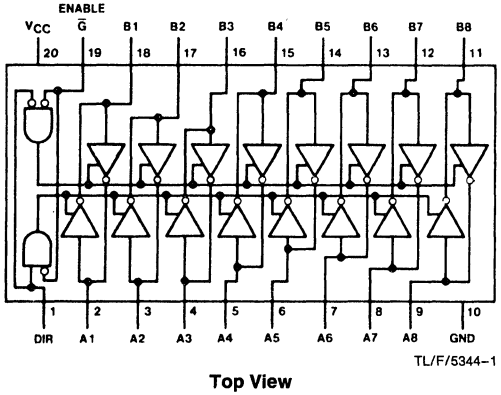
These devices can drive up to 15 LS-TTL Loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA maximum (74 HC)
- TRI-STATE outputs for connection to bus oriented systems
- High output drive: 6 mA (min)

Connection Diagrams

Dual-In-Line Package

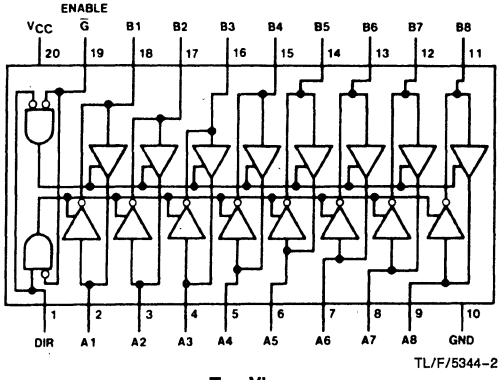


TL/F/5344–1

Top View

Order Number MM54HC640J or MM74HC640J,N
See NS Package J20A or N20A

Dual-In-Line Package



TL/F/5344–2

Top View

Order Number MM54HC643J or MM74HC643J,N
See NS Package J20A or N20A

Truth Table

Control Inputs		Operation	
$\overline{G}$	DIR	640	643
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage DIR and $\overline{G}$ pins (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{IN}, V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise/Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Input Leakage Current ($\overline{G}$ and DIR)	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable $\overline{G}$=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=45$ pF	13	17	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	33	42	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	32	42	ns

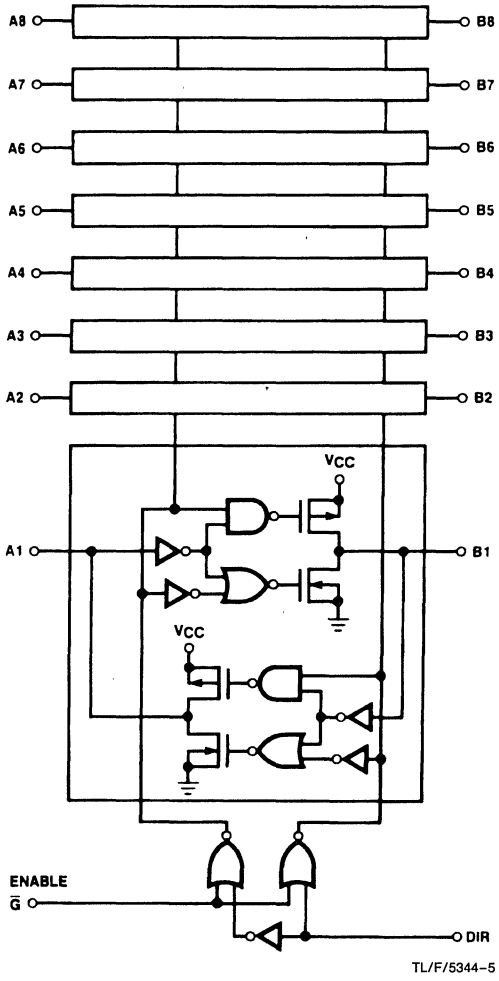
AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay	$C_L=50$ pF	2.0V	29	72	88	96	ns
		$C_L=150$ pF	2.0V	38	96	116	128	ns
		$C_L=50$ pF	4.5V	14	18	22	24	ns
		$C_L=150$ pF	4.5V	18	24	29	32	ns
		$C_L=50$ pF	6.0V	14	18	22	24	ns
		$C_L=150$ pF	6.0V	18	24	29	32	ns
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L=1$ kΩ						
		$C_L=50$ pF	2.0V	70	184	224	240	ns
		$C_L=150$ pF	2.0V	80	216	260	284	ns
		$C_L=50$ pF	4.5V	35	46	56	60	ns
		$C_L=150$ pF	4.5V	41	54	65	71	ns
		$C_L=50$ pF	6.0V	31	41	50	54	ns
		$C_L=150$ pF	6.0V	36	47	57	62	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	2.0V	47	172	208	224	ns
			4.5V	33	43	52	56	ns
			6.0V	31	41	50	54	ns
t_{THL}, t_{TLH}	Output Rise and Fall Time	$C_L=50$ pF	2.0V	20	60	75	90	ns
			4.5V	6	12	15	18	ns
			6.0V	5	10	13	15	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	$\overline{G}=V_{IL}$		120				pF
		$\overline{G}=V_{IH}$		12				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
$C_{IN/OUT}$	Maximum Input/Output Capacitance, A or B			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

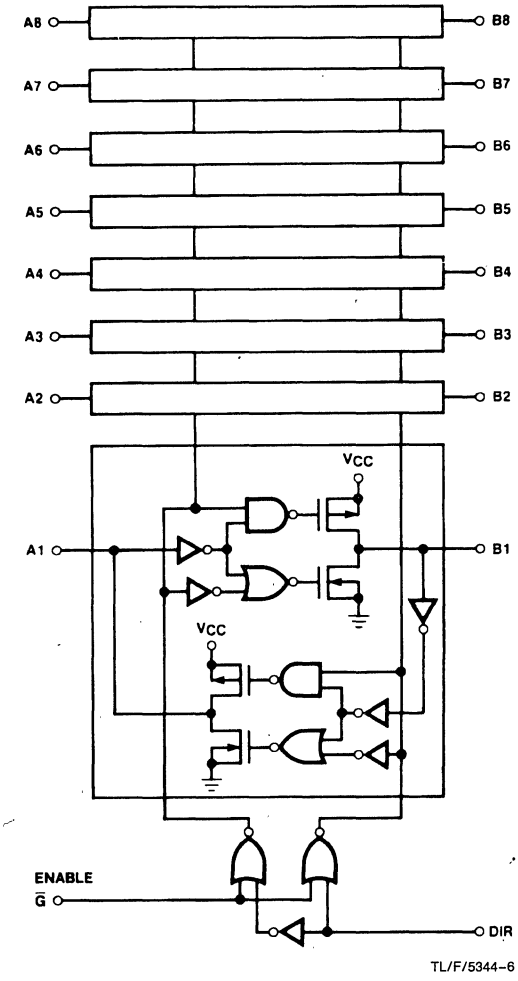
Logic Diagrams

'HC640



TL/F/5344–5

'HC643



TL/F/5344–6

National Semiconductor

microCMOS

MM54HC646/MM74HC646 Non-Inverting Octal Bus Transceiver/Registers
MM54HC648/MM74HC648 Inverting Octal Bus Transceiver/Registers

General Description

These transceivers utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and contain two sets of TRI-STATE® outputs, two sets of D-type flip-flops, and control circuitry designed for high speed multiplexed transmission of data.

Six control inputs enable this device to be used as a latched transceiver, unlatched transceiver, or a combination of both. As a latched transceiver, data from one bus is stored for later retrieval by the other bus. Alternately real time bus data (unlatched) may be directly transferred from one bus to another.

Circuit operation is determined by the G, DIR, CAB, CBA, SAB, SBA control inputs. The enable input, G, controls whether any bus outputs are enabled. The direction control, DIR, determines which bus is enabled, and hence the direction data flows: The SAB, SBA inputs control whether the latched data (stored in D type flip flops), or the bus data (from other bus input pins) is transferred. Each set of flip-flops has its own clock CAB, and CBA, for storing data. Data is latched on the rising edge of the clock.

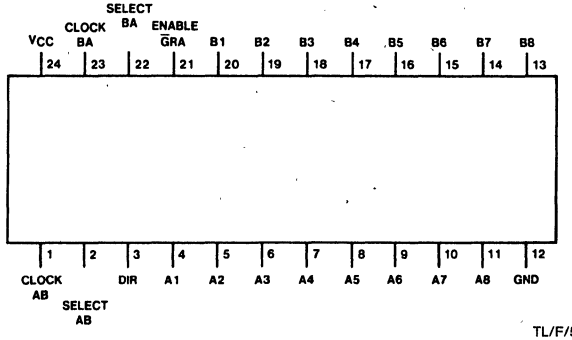
Each output can drive up to 15 low power Schottky TTL loads. These devices are functionally and pin compatible to their LS-TTL counterparts. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns
- TRI-STATE outputs
- Bidirectional communication
- Wide power supply range: 2–6V
- Low quiescent supply current: 160 μA maximum (74HC)
- High output current: 6 mA (74HC)

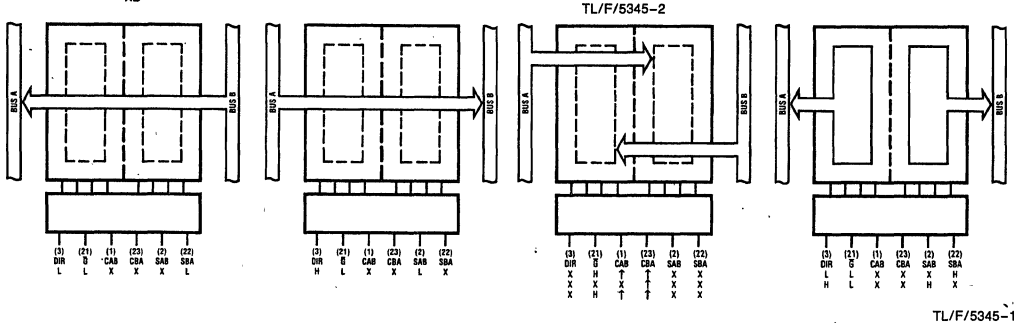
Connection Diagram

Dual-In-Line Package



Order Number MM54HC646J, MM54HC648J, MM74HC646J, N or MM74HC648J, N
See NS Package J24F or N24C

TL/F/5345–2



Real-Time Transfer Bus B to Bus A | **Real-Time Transfer Bus A to Bus B** | **Storage from A, B, or A and B** | **Transfer Stored Data to A or B**

TL/F/5345–1

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	4.2	3.96	3.84	3.7	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	5.7	5.46	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$≤6.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$≤7.8 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.
Note 2: Unless otherwise specified all voltages are referenced to ground.
Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.
Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

Truth Table

Inputs						Data I/O		Operation or Function	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 Thru A8	B1 Thru B8	'ALS646, 'ALS647 'AS646	'ALS648, 'ALS649 'AS648
X	X	↑	X	X	X	Input	Not Specified	Store A, B Unspecified	Store A, B Unspecified
X	X	X	↑	X	X	Not Specified	Input	Store B, A Unspecified	Store B, A Unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	X	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	X	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

H = High Level L = Low Level X = Irrelevant ↑ = low-to-high level transition
The data output functions i.e., data at the bus pins may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled.
The data output functions i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

AC Electrical Characteristics MM54HC646/MM74HC646

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		45	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=45$ pF	14	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=45$ pF	31	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=45$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	$C_L=45$ pF	35	50	ns
t_{PZH}, t_{PZL}	Maximum Enable Time $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=45$ pF	18	33	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time, $\overline{G}$ or DIR Input to A or B Output	$R_L=1$ kΩ $C_L=5$ pF	17	30	ns

AC Electrical Characteristics MM54HC646/MM74HC646

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=50$ pF	2.0V	60	180	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	18	26	31	39	ns
		$C_L=150$ pF	6.0V	22	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=50$ pF	2.0V	110	220	275	330	ns
		$C_L=150$ pF	2.0V	150	270	338	405	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	40	54	68	81	ns
		$C_L=50$ pF	6.0V	28	38	47	57	ns
		$C_L=150$ pF	6.0V	34	47	59	71	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=50$ pF	2.0V	180	290	363	435	ns
		$C_L=150$ pF	2.0V	210	340	425	510	ns
		$C_L=50$ pF	4.5V	39	58	72	87	ns
		$C_L=150$ pF	4.5V	47	68	85	102	ns
		$C_L=50$ pF	6.0V	34	50	63	75	ns
		$C_L=150$ pF	6.0V	39	58	72	87	ns

AC Electrical Characteristics (Continued) MM54HC646/MM74HC646

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B Low	C_L = 50 pF	2.0V	180	290	363	435	ns
		C_L = 150 pF	2.0V	210	340	425	510	ns
		C_L = 50 pF	4.5V	39	58	72	87	ns
		C_L = 150 pF	4.5V	47	68	85	102	ns
		C_L = 50 pF	6.0V	34	50	63	75	ns
		C_L = 150 pF	6.0V	39	58	72	87	ns
t_{PZH}, t_{PZH}	Maximum Output Enable Time, $\overline{G}$ Input or DIR to A or B Output	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	80	175	219	263	ns
		C_L = 150 pF	2.0V	120	225	281	338	ns
		C_L = 50 pF	4.5V	23	35	44	53	ns
		C_L = 150 pF	4.5V	31	45	56	68	ns
		C_L = 50 pF	6.0V	21	30	37	45	ns
		C_L = 150 pF	6.0V	27	38	48	57	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, $\overline{G}$ Input to A or B Output	R_L = 1 kΩ, C_L = 50 pF	2.0V	85	175	219	263	ns
			4.5V	23	35	44	53	ns
			6.0V	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
t_S	Minimum Setup Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Clock		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Input Capacitance			15	20	20	20	pF

3

AC Electrical Characteristics MM54HC648/MM74HC648

$V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		44	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=50$ pF	14	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=50$ pF	31	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=50$ pF	35	50	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	$C_L=50$ pF	35	50	ns
t_{PZH}, t_{PZL}	Maximum Enable Time $\overline{G}$ Input to A or B Output	$R_L=1$ kΩ $C_L=45$ pF	18	33	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time, $\overline{G}$ Input to A or B Output	$R_L=1$ kΩ $C_L=5$ pF	17	30	ns

AC Electrical Characteristics MM54HC648/MM74HC648

$V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency	$C_L=50$ pF	2.0V		5	4	3	MHz
			4.5V		27	21	18	MHz
			6.0V		31	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B Input to B or A Output	$C_L=50$ pF	2.0V	60	180	189	225	ns
		$C_L=150$ pF	2.0V	80	200	250	300	ns
		$C_L=50$ pF	4.5V	21	30	37	45	ns
		$C_L=150$ pF	4.5V	30	40	50	60	ns
		$C_L=50$ pF	6.0V	18	26	31	39	ns
		$C_L=150$ pF	6.0V	22	35	44	53	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, CBA or CAB Input to A or B Output	$C_L=50$ pF	2.0V	110	220	275	330	ns
		$C_L=150$ pF	2.0V	150	270	338	405	ns
		$C_L=50$ pF	4.5V	31	44	55	66	ns
		$C_L=150$ pF	4.5V	40	54	68	81	ns
		$C_L=50$ pF	6.0V	28	38	47	57	ns
		$C_L=150$ pF	6.0V	34	47	59	71	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B high	$C_L=50$ pF	2.0V	180	290	363	435	ns
		$C_L=150$ pF	2.0V	210	340	425	510	ns
		$C_L=50$ pF	4.5V	39	58	72	87	ns
		$C_L=150$ pF	4.5V	47	68	85	102	ns
		$C_L=50$ pF	6.0V	34	50	63	75	ns
		$C_L=150$ pF	6.0V	39	58	72	87	ns

AC Electrical Characteristics MM54HC648/MM74HC648 (Continued)

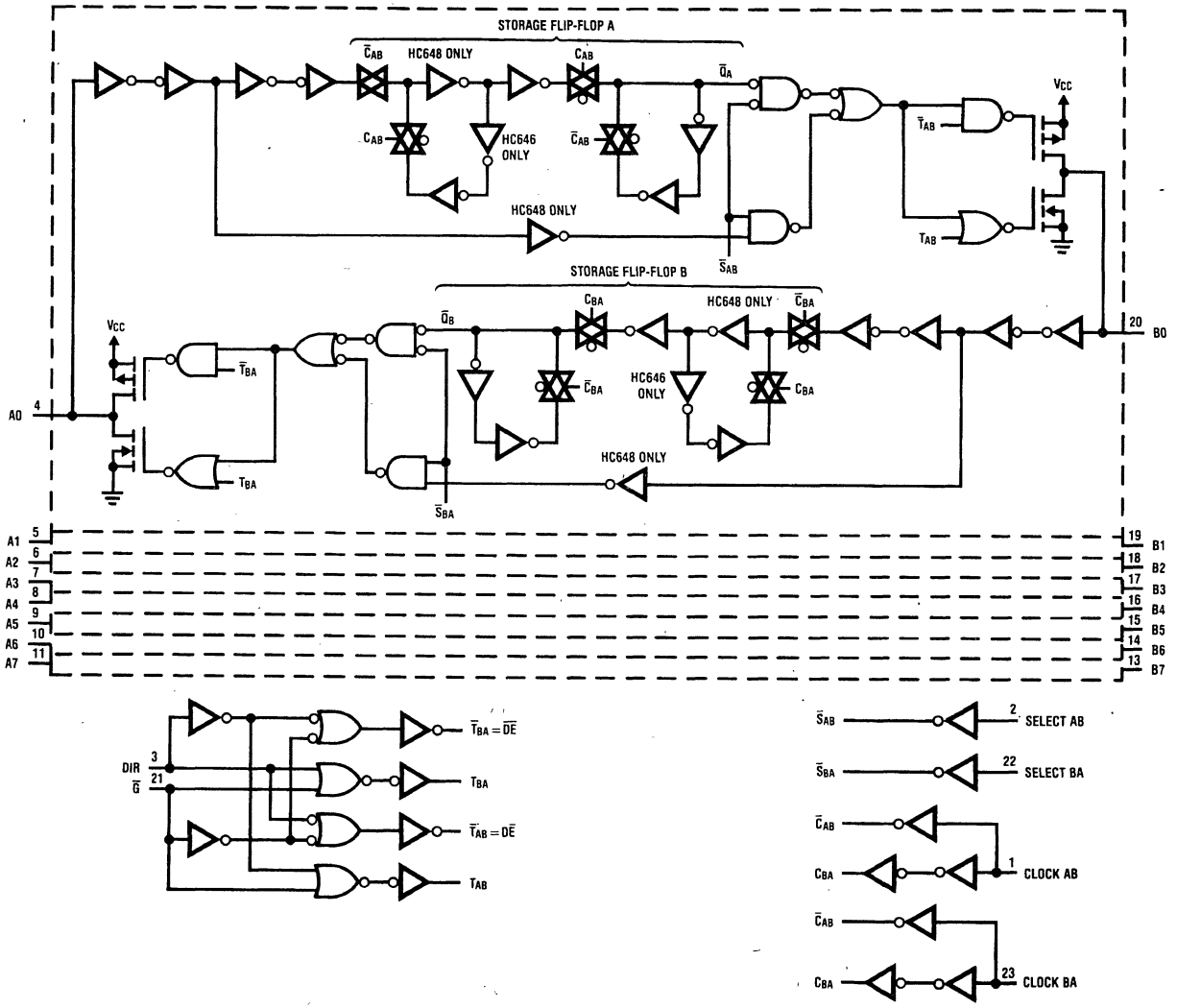
V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SBA or SAB Input to A or B Output, with A or B low	C_L = 50 pF	2.0V	180	290	363	435	ns
		C_L = 150 pF	2.0V	210	340	425	510	ns
		C_L = 50 pF	4.5V	39	58	72	87	ns
		C_L = 150 pF	4.5V	47	68	85	102	ns
		C_L = 50 pF	6.0V	34	50	63	75	ns
		C_L = 150 pF	6.0V	39	58	72	87	ns
t_{PZL}, t_{PZL}	Maximum Output Enable Time, $\overline{G}$ Input or DIR to A or B Output	R_L = 1 kΩ						
		C_L = 50 pF	2.0V	80	175	219	263	ns
		C_L = 150 pF	2.0V	120	225	281	338	ns
		C_L = 50 pF	4.5V	23	35	44	53	ns
		C_L = 150 pF	4.5V	31	45	56	68	ns
		C_L = 50 pF	6.0V	21	30	37	45	ns
		C_L = 150 pF	6.0V	27	38	48	57	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time, $\overline{G}$ Input to A or B Output	R_L = 1 kΩ, C_L = 50 pF	2.0V	85	175	219	263	ns
			4.5V	23	35	44	53	ns
			6.0V	21	30	37	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF	2.0V		60	75	90	ns
			4.5V		12	15	18	ns
			6.0V		10	13	15	ns
t_S	Minimum Set Up Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t_W	Minimum Pulse Width of Clock		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	21	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Note 6: Refer to back of this section for Typical MM54/74HC AC Switching Waveforms and Test Circuits.

Logic Diagram



TL/F/5345–3

National Semiconductor

microCMOS

MM54HC688/MM74HC688
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to compare bit for bit two 8-bit words and indicates whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

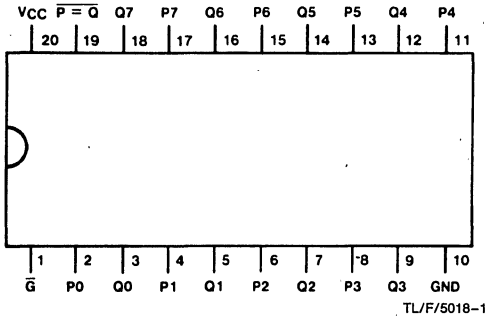
The comparator's output can drive 10 low power Schottky equivalent loads. This comparator is functionally and pin compatible to the 54LS688/74LS688. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 80 μA (74 Series)
- Large output current: 4 mA (74 Series)
- Same as 'HC521

Connection and Logic Diagrams

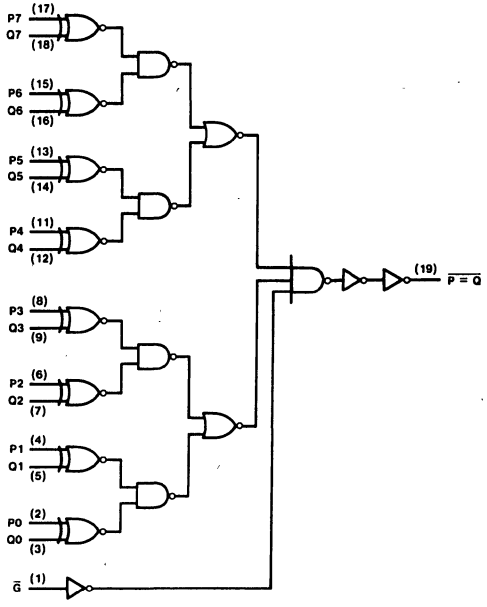
Dual-In-Line Package



TL/F/5018–1

Top View

Order Number MM54HC688J or MM74HC688J, N
See NS Package J20A or N20A



TL/F/5018–2

Truth Table

Inputs		
Data P,Q	Enable $\overline{G}$	$\overline{P=Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, any P or Q to Output		21	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Enable to any Output		14	20	ns

AC Electrical Characteristics

$V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	60	175	220	263	ns
			4.5V	22	35	44	53	ns
			6.0V	19	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	45	120	150	180	ns
			4.5V	15	24	30	36	ns
			6.0V	13	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			45				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

PRELIMINARY

microCMOS

MM74HC942 300 Baud Modem

General Description

The MM74HC942 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC942 utilizes microCMOS Technology, 2 layers of polysilicon and 1 layer of metal P-well CMOS. Switched capacitor techniques are used to perform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600Ω phone line. They can perform two-to-four-wire conversion and drive the line at a maximum of 0 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

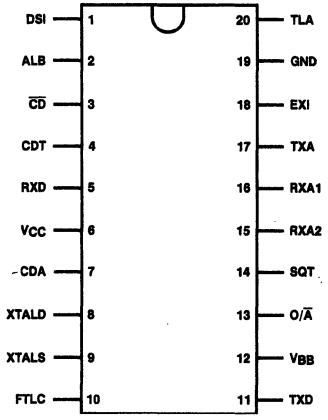
- Drives 600Ω at 0 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- ±5V supplies
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signalling systems
- Remote process control

Connection and Block Diagrams

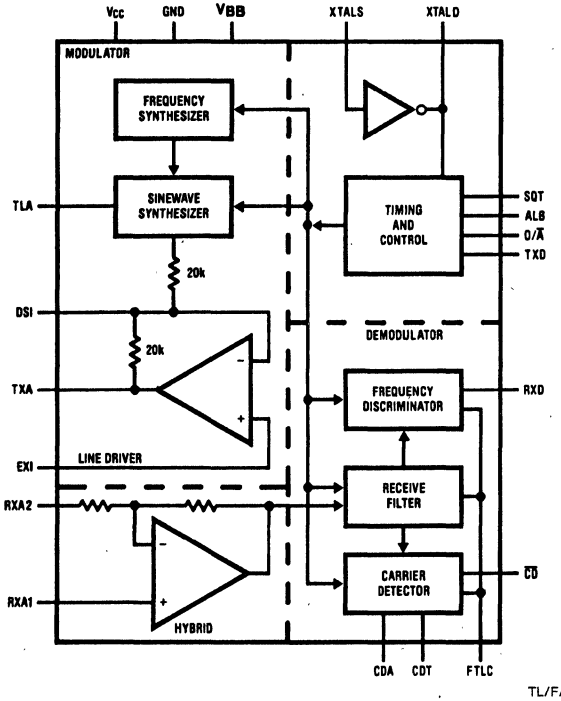
Dual-In-Line Package



TL/F/5348–1

Top View

Order Number MM74HC942J, N
See NS Package J20A or N20A



TL/F/5348–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
Supply Voltage (V_{BB})	+0.5 to −7.0V
DC Input Voltage (V_{IN})	V_{BB} −1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	V_{BB} −0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
Supply Voltage (V_{BB})	−4.5	−5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A) MM74HC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics

Symbol	Parameter	Conditions	T = 25°C	74HC T = −40 to 85°C		Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	V_{CC}	V_{CC} −0.1 3.98	V_{CC} −0.1 3.7	V V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V		0.1 0.26	0.1 0.4	V V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	μA
I_{OZ}	Output TRI-STATE® Leakage Current RXD and $\overline{CD}$ Outputs	ALB = SQT = V_{CC}			±5	μA
I_{CC}, I_{BB}	Maximum Quiescent Supply Current	V_{IN} = V_{CC}, V_{IL} = GND ALB or SQT = GND Transmit Level = −9 dBm	8.0	12.0	12.0	mA
I_{CC}, I_{BB}	Power Down Supply Current	ALB = SQT = V_{CC} V_{IH} = V_{CC}, V_{IL} = GND			300	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

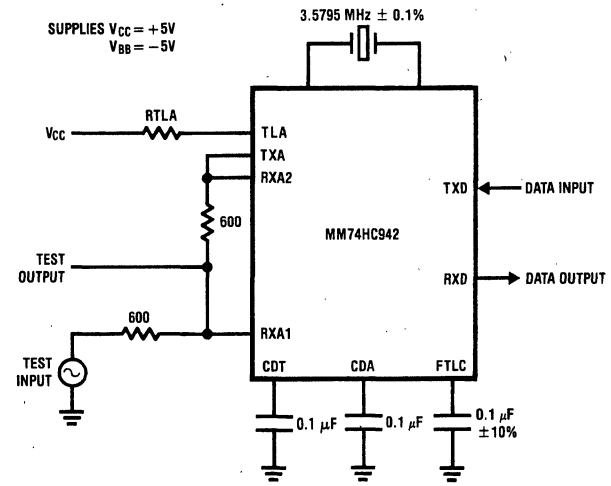
*The demodulator specifications apply to the MM74HC942 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC942 modulator.

AC Electrical Characteristics

Unless otherwise specified, all specifications apply to the MM74HC942 over the range −40°C to +85°C using a V_{CC} = +5V ±10%, a V_{BB} = −5V ±10% and a 3.579MHz ±0.1% crystal.*

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER							
F_{CE}	Carrier Frequency Error					4	Hz
	Power Output	V_{CC}=5.0V	R_{TLA} = 0	−3	−1.5	0	dBm
		R_L=1.2 kΩ	R_{TLA} = 5.49 kΩ	−12	−10.5	−9	dBm
	2nd Harmonic Energy				−62	−56	dBm
RECEIVE FILTER AND HYBRID							
	Hybrid Input Impedance (Pins 15 and 16)			50			kΩ
	FTLC Output Impedance			5	10	50	kΩ
	Adjacent Channel Rejection	RXA2=GND TXA=GND or V_{CC} Input to RXA1		60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)							
	Carrier Amplitude			−48		−9	dBm
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud			100	200	μS
	Bit Bias	Alternating 1-0 Pattern			5	10	%
	Carrier Detect Trip Points	CDA=1.2V	Off to On	−45	−42	−40	dBm
		V_{CC}=5.0V	On to Off	−47	−45	−42	dBm
	Carrier Detect Hysteresis	V_{CC}=5V		2	3	4	dB

AC Specification Circuit



TL/F/5348–3

Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data output pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system, XTALD can be driven.
9	XTALS	Crystal Sense: Refer to Pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receive filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	V_{BB}	Negative Supply: The recommended supply is −5V.
13	O/$\overline{A}$	Originate/$\overline{Answer}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded.
19	GND	Ground: This defines the chip 0V.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC942 uses frequency shift keying (FSK) of an audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC942 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC942 is capable of transmitting and receiving data simultaneously.

The tone allocation by the MM74HC942 and other Bell 103 compatible modems is shown in Table I. The terms "originate" and "answer" which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

TABLE I. BELL 103 Allocation

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switched capacitor nine-pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60 Hz, a common noise component.

The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques. The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency produces one of four tones depending on the O/A and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter. The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

TRANSMIT LEVEL ADJUSTMENT

The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source impedances.

The transmit level is programmable by placing a resistor from TLA to VCC. With a 5.5k resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the MM74HC942 will interface to most telephones. This arrangement is called the "permissive arrangement." The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

SNR can be maximized by adjusting the transmit level until the level at the exchange reaches −12 dBm. This must be done with the cooperation of the telephone company. The programming resistor used is specific for a given installation and is often included in the telephone jack at the installation. The modem is thus programmable and can be used with any jack correctly wired. This arrangement is called the universal registered jack arrangement and is possible with the MM74HC942. The values of resistors required to program the MM74HC942 follow the most common code in use; the universal service order code. The required resistors are given in Table II.

TABLE II. Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ohms)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490
4	−8	3,610
5	−7	2,520
6	−6	1,780
7	−5	1,240
8	−4	866
9	−3	562
10	−2	336
11	−1	150
12	0	0

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used;

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on Pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$T_{\overline{CDL}} \cong 6.4 \times C_{CDT}$ for $\overline{CD}$ going low

$T_{\overline{CDH}} \cong 0.54 \times C_{CDT}$ for $\overline{CD}$ going high

Where $T_{\overline{CDL}}$ & $T_{\overline{CDH}}$ are in seconds, and C_{CDT} is in μF.

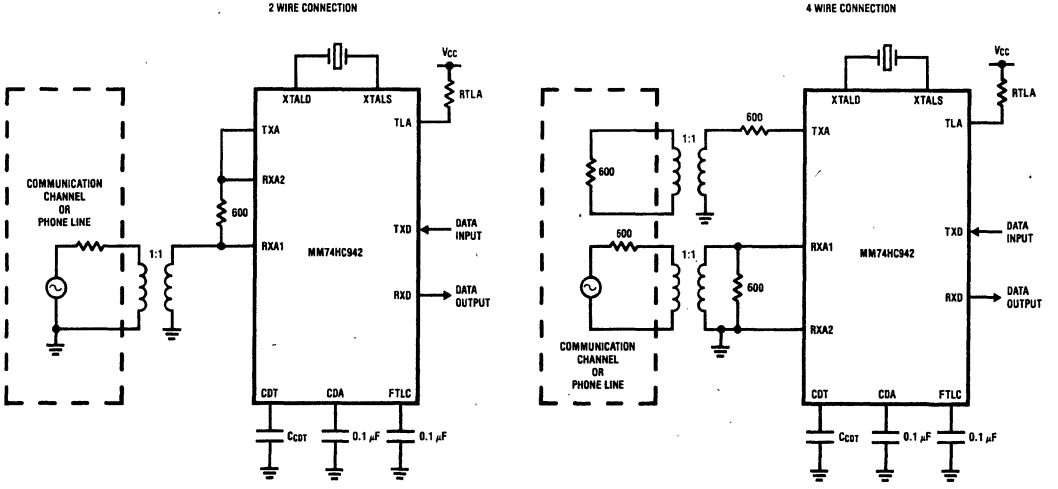
Applications Information (Continued)

DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC942 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout.

Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

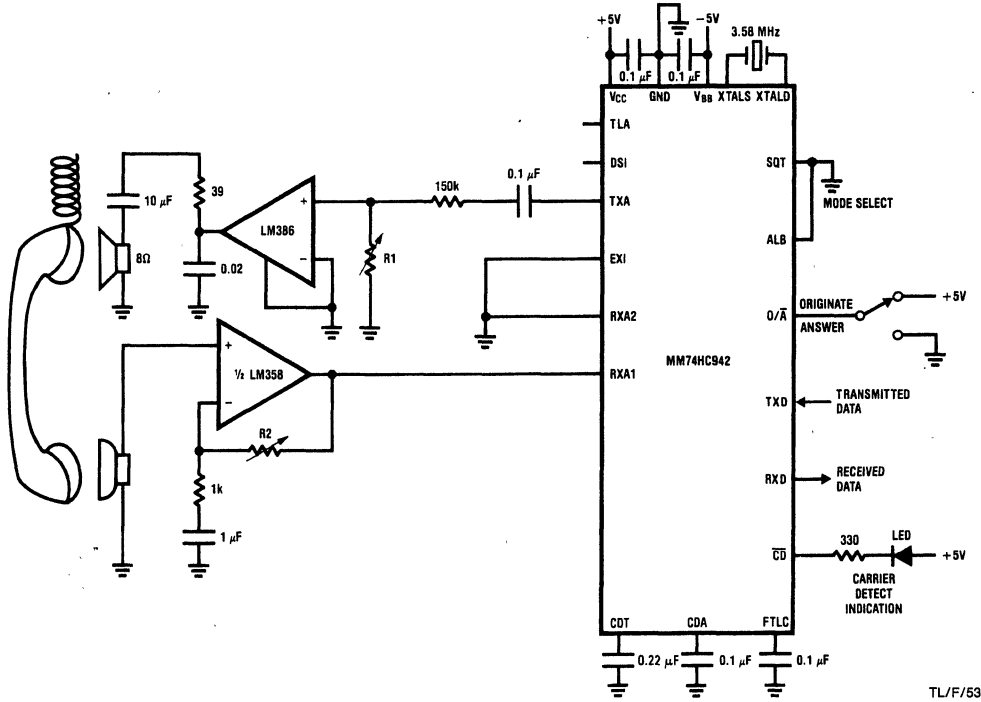
Interface Circuits for MM74HC942 300 Baud Modem



TL/F/5348–4

C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.

Complete Acoustically Coupled 300 Baud Modem



TL/F/5348–5

Note: The efficiency of the acoustic coupling will set the valves of R1 and R2.

National Semiconductor

PRELIMINARY

microCMOS

MM74HC943 300 Baud Modem

General Description

The MM74HC943 is a full duplex low speed modem. It provides a 300 baud bidirectional serial interface for data communication over telephone lines and other narrow bandwidth channels. It is Bell 103 compatible.

The MM74HC943 utilizes microCMOS Technology, 2 layers of polysilicon and 1 layer metal P-well CMOS. Switched capacitor techniques are used to peform analog signal processing.

MODULATOR SECTION

The modulator contains a frequency synthesizer and a sine wave synthesizer. It produces a phase coherent frequency shift keyed (FSK) output.

LINE DRIVER AND HYBRID SECTION

The line driver and hybrid are designed to facilitate connection to a 600Ω phone line. They can perform two to four wire conversion and drive the line at a maximum of −9 dBm.

DEMODULATOR SECTION

The demodulator incorporates anti-aliasing filters, a receive filter, limiter, discriminator, and carrier detect circuit. The nine-pole receive filter provides 60 dB of transmitted tone rejection. The discriminator is fully balanced for stable operation.

Features

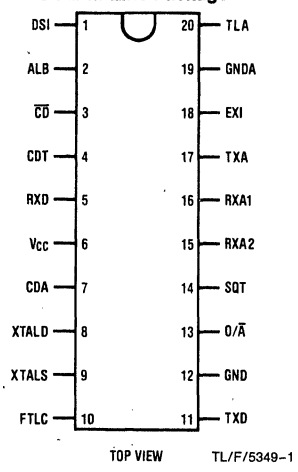
- 5V supply
- Drives 600Ω at −9 dBm
- All filters on chip
- Transmit level adjustment compatible with universal service order code
- TTL and CMOS compatible logic
- All inputs protected against static damage
- Low power consumption
- Full duplex answer or originate operation
- Analog loopback for self test
- Power down mode

Applications

- Built-in low speed modems
- Remote data collection
- Radio telemetry
- Credit verification
- Stand-alone modems
- Point-of-sale terminals
- Tone signaling systems
- Remote process control

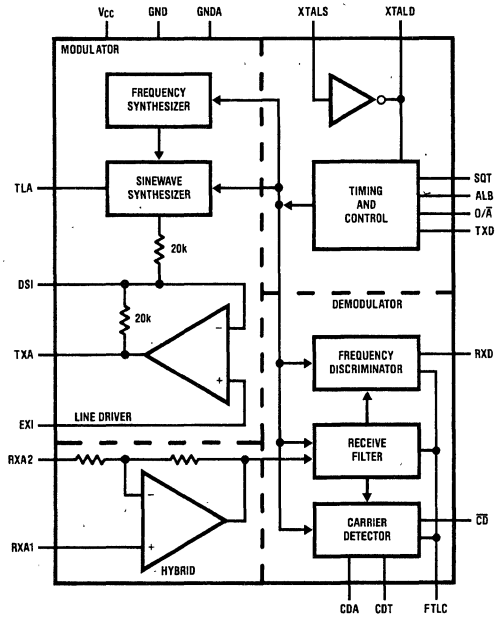
Connection and Block Diagrams

Dual-In-Line Package



TOP VIEW TL/F/5349-1

Order Number MM74HC943J or MM74HC943N
See NS Package J20A or N20A



TL/F/5349-2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A) MM74HC	−40	+85	°C
Input Rise or Fall Times (t_r, t_f)		500	ns
Crystal frequency		3.579	MHz

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C		74HC T_A=−40 to 85°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			1.1	1.1	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	V_{CC-EE}	V_{CC}−0.1 3.84	V_{CC}−0.1 3.7	V V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V		0.1 0.33	0.1 0.4	V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	μA
I_{OZ}	Output TRI-STATE® Leakage Current, RXD and $\overline{CD}$ Outputs	ALB=SQT=V_{CC}			±5	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IH}=V_{CC}, V_{IL}=GND ALB or SQT=GND Transmit Level=−9 dBm	8.0		10.0	mA
I_{GNDA}	Analog Ground Current		1.0		2.0	mA
I_{CC}	Power Down Supply Current	ALB=SQT=V_{CC} V_{IH}=V_{CC}, V_{IL}=GND			300	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

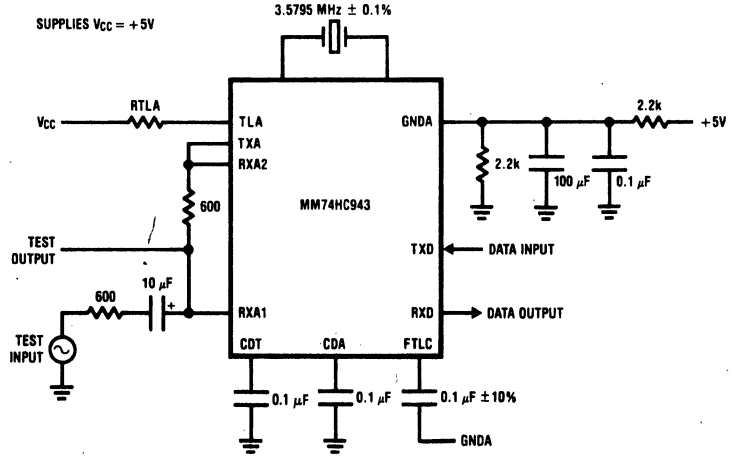
*The demodulator specifications apply to the MM74HC943 operating with a modulator having frequency accuracy, phase jitter and harmonic content equal to or better than the MM74HC943 modulator.

AC Electrical Characteristics

Unless otherwise specified, all specifications apply to the MM74HC943 over the range −40°C to +85°C using a V_{CC} of +5V ±10%, and a 3.579 MHz ±0.1% crystal.*

Symbol	Parameter	Conditions		Min	Typ	Max	Units
TRANSMITTER							
F_{CE}	Carrier Frequency Error					4	Hz
	Power Output	V_{CC} = 5.0V R_L = 1.2 kΩ	R_{TLA} = 5490Ω	−12	−10.5	−9	dBm
	2nd Harmonic Energy				−62	−56	dBm
RECEIVE FILTER AND HYBRID							
	Hybrid Input Impedance (Pins 15 and 16)			50			kΩ
	FTLC Output Impedance			5	10	50	kΩ
	Adjacent Channel Rejection	RXA2 = GNDA, TXD = GND or V_{CC} Input to RXA1		60			dB
DEMODULATOR (INCORPORATING HYBRID, RECEIVE FILTER AND DISCRIMINATOR)							
	Carrier Amplitude			−48		−12	dBm
	Bit Jitter	SNR = 30 dB Input = −38 dBm Baud Rate = 300 Baud			100	200	μS
	Bit Bias	Alternating 1−0 Pattern			5	10	%
	Carrier Detect Trip Points	CDA = 1.2V	Off to On	−45	−42	−40	dBm
		V_{CC} = 5.0V	On to Off	−47	−45	−42	dBm
	Carrier Detect Hystereisis	V_{CC} = 5.0V		2	3	4	dB

AC Specification Circuit



TL/F/5349–3

Description of Pin Functions

Pin No.	Name	Function
1	DSI	Driver Summing Input: This input may be used to transmit externally generated tones such as dual tone multifrequency (DTMF) dialing signals.
2	ALB	Analog Loop Back: A logic high on this pin causes the modulator output to be connected to the demodulator input so that data is looped back through the entire chip. This is used as a chip self test. If ALB and SQT are simultaneously held high the chip powers down.
3	$\overline{CD}$	Carrier Detect: This pin goes to a logic low when carrier is sensed by the carrier detect circuit.
4	CDT	Carrier Detect Timing: A capacitor on this pin sets the time interval that the carrier must be present before the $\overline{CD}$ goes low.
5	RXD	Received Data: This is the data output pin.
6	V_{CC}	Positive Supply Pin: A +5V supply is recommended.
7	CDA	Carrier Detect Adjust: This is used for adjustment of the carrier detect threshold. Carrier detect hysteresis is set at 3 dB.
8	XTALD	Crystal Drive: XTALD and XTALS connect to a 3.5795 MHz crystal to generate a crystal locked clock for the chip. If an external circuit requires this clock XTALD should be sensed. If a suitable clock is already available in the system. XTALD can be driven.
9	XTALS	Crystal Sense: Refer to pin 8 for details.
10	FTLC	Filter Test/Limiter Capacitor: This is connected to a high impedance output of the receiver filter. It may thus be used to evaluate filter performance. This pin may also be driven to evaluate the demodulator. RXA1 and RXA2 must be grounded during this test. For normal modem operation FTLC is AC grounded via a 0.1 μF bypass capacitor.
11	TXD	Transmitted Data: This is the data input.
12	GND	Ground: This defines the chip 0V.
13	O/$\overline{A}$	Originate/$\overline{Answer}$ mode select: When logic high this pin selects the originate mode of operation.
14	SQT	Squelch Transmitter: This disables the modulator when held high. The EXI input remains active. If SQT and ALB are simultaneously held high the chip powers down.
15	RXA2	Receive Analog #2: RXA2 and RXA1 are analog inputs. When connected as recommended they produce a 600Ω hybrid.
16	RXA1	Receive Analog #1: See RXA2 for details.
17	TXA	Transmit Analog: This is the output of the line driver.
18	EXI	External Input: This is a high impedance input to the line driver. This input may be used to transmit externally generated tones. When not used for this purpose it should be grounded to GNDA.
19	GNDA	Analog Ground: Analog signals within the chip are referred to this pin.
20	TLA	Transmit Level Adjust: A resistor from this pin to V_{CC} sets the transmit level.

Functional Description

INTRODUCTION

A modem is a device for transmitting and receiving serial data over a narrow bandwidth communication channel. The MM74HC943 uses frequency shift keying (FSK) of audio frequency tone. The tone may be transmitted over the switched telephone network and other voice grade channels. The MM74HC943 is also capable of demodulating FSK signals. By suitable tone allocation and considerable signal processing the MM74HC943 is capable of transmitting and receiving data simultaneously.

The tone allocation used by the MM74HC943 and other Bell 103 compatible modems is shown in Table I. The terms "originate" and "answer" which define the frequency allocation come from use with telephones. The modem on the end of the line which initiates the call is called the originate modem. The other modem is the answer modem.

TABLE I. Bell 103 Tone Allocation

Data	Originate Modem		Answer Modem	
	Transmit	Receive	Transmit	Receive
Space	1070Hz	2025Hz	2025Hz	1070Hz
Mark	1270Hz	2225Hz	2225Hz	1270Hz

THE LINE INTERFACE

The line interface section performs two to four wire conversion and provides impedance matching between the modem and the phone line.

THE LINE DRIVER

The line driver is a power amplifier for driving the line. If the modem is operating as an originate modem, the second harmonics of the transmitted tones fall close to the frequencies of the received tones and degrade the received signal to noise ratio (SNR). The line driver must thus produce low second harmonic distortion.

THE HYBRID

The voltage on the telephone line is the sum of the transmitted and received signals. The hybrid subtracts the transmitted voltage from the voltage on the telephone line. If the telephone line was matched to the hybrid impedance, the output of the hybrid would be only the received signal. This rarely happens because telephone line characteristic impedances vary considerably. The hybrid output is thus a mixture of transmitted and received signals.

Functional Description (Continued)

THE DEMODULATOR SECTION

The Receive Filter

The demodulator recovers the data from the received signals. The signal from the hybrid is a mixture of transmitted signal, received signals and noise. The first stage of the receive filter is an anti-alias filter which attenuates high frequency noise before sampling occurs. The signal then goes to the second stage of the receive filter where the transmitted tones and other noise are filtered from the received signal. This is a switch capacitor nine pole filter providing at least 60 dB of transmitted tone rejection. This also provides high attenuation at 60Hz, a common noise component.

The Discriminator

The first stage of the discriminator is a hard limiter. The hard limiter removes from the received signal any amplitude modulation which may bias the demodulator toward a mark or a space. It compares the output of the receive filter to the voltage on the 0.1 μF capacitor on the FTLC pin.

The hard limiter output connects to two parallel bandpass filters in the discriminator. One filter is tuned to the mark frequency and the other to the space frequency. The outputs of these filters are rectified, filtered and compared. If the output of the mark path exceeds the output of the space path the RXD output goes high. The opposite case sends RXD low.

The demodulator is implemented using precision switched capacitor techniques The highly critical comparators in the limiter and discriminator are auto-zeroed for low offset.

Carrier Detector

The output of the discriminator is meaningful only if there is sufficient carrier being received. This is established in the carrier detection circuit which measures the signal on the line. If this exceeds a certain level for a preset period (adjustable by the CDT pin) the $\overline{CD}$ output goes low indicating that carrier is present. Then the carrier detect threshold is lowered by 3 dB. This provides hysteresis ensuring the $\overline{CD}$ output remains stable. If carrier is lost $\overline{CD}$ goes high after the preset delay and the threshold is increased by 3 dB.

MODULATOR SECTION

The modulator consists of a frequency synthesizer and a sine wave synthesizer. The frequency synthesizer produces one of four tones depending on the O/$\overline{A}$ and TXD pins. The frequencies are synthesized to high precision using a crystal oscillator and variable dual modulus counter.

The counters used respond quickly to data changes, introducing negligible bit jitter while maintaining phase coherence.

The sine wave synthesizer uses switched capacitors to "look up" the voltages of the sine wave. This sampled signal is then further processed by switched capacitor and continuous filters to ensure the high spectral purity required by FCC regulations.

Applications Information

TRANSMIT LEVEL ADJUSTMENT

The transmitted power levels of Table II refer to the power delivered to a 600Ω load from the external 600Ω source impedance. The voltage on the load is half the TXA voltage. This should be kept in mind when designing interface circuits which do not match the load and source inpedances.

The transmit level is programmable by placing a resistor from TLA to V_{CC}. With a 5.5k resistor the line driver transmits a maximum of −9 dBm. Since most lines from a phone installation to the exchange provide 3 dB of attenuation the maximum level reaching the exchange will be −12 dBm. This is the maximum level permitted by most telephone companies. Thus with this programming the MM74HC943 will interface to most telephones. This arrangement is called the "permissive arrangement." The disadvantage with the permissive arrangement is that when the loss from a phone to the exchange exceeds 3 dB, no compensation is made and SNR may be unnecessarily degraded.

TABLE II. Universal Service Order Code Resistor Values

Line Loss (dB)	Transmit Level (dBm)	Programming Resistor (R_{TLA}) (Ω)
0	−12	Open
1	−11	19,800
2	−10	9,200
3	−9	5,490

CARRIER DETECT THRESHOLD ADJUSTMENT

The carrier detect threshold is directly proportional to the voltage on CDA. This pin is connected internally to a high impedance source. This source has a nominal Thevenin equivalent voltage of 1.2V and output impedance of 100 kΩ.

By forcing the voltage on CDA the carrier detect threshold may be adjusted. To find the voltage required for a given threshold the following equation may be used:

$$V_{CDA} = 244 \times V_{ON}$$

$$V_{CDA} = 345 \times V_{OFF}$$

CARRIER DETECT TIMING ADJUSTMENT

CDT: A capacitor on Pin 4 sets the time interval that the carrier must be present before $\overline{CD}$ goes low. It also sets the time interval that carrier must be removed before $\overline{CD}$ returns high. The relevant timing equations are:

$$T_{\overline{CDL}} \cong 6.4 \times C_{CDT} \quad \text{for } \overline{CD} \text{ going low}$$

$$T_{\overline{CDH}} \cong 0.54 \times C_{CDT} \quad \text{for } \overline{CD} \text{ going high}$$

Where $T_{\overline{CDL}}$ & $T_{\overline{CDH}}$ are in seconds, and C_{CDT} is in μF.

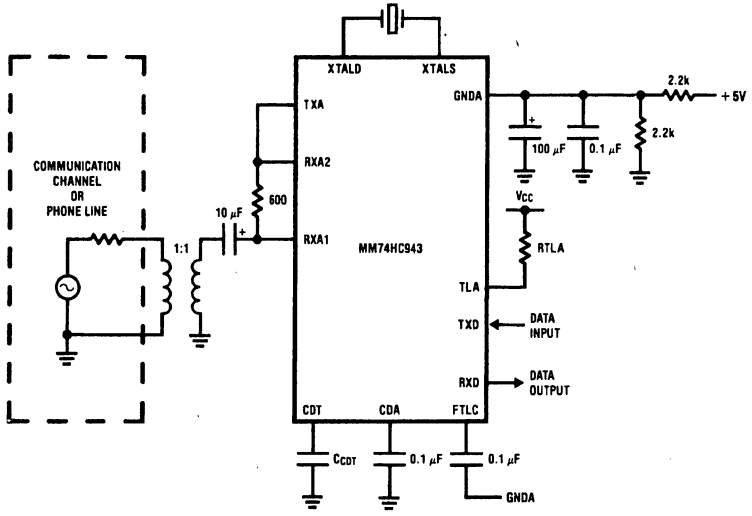
DESIGN PRECAUTIONS

Power supplies to digital systems may contain high amplitude spikes and other noise. To optimize performance of the MM74HC943 operating in close proximity to digital systems, supply and ground noise should be minimized. This involves attention to power supply design and circuit board layout. Power supply decoupling close to the device is recommended. Ground loops should be avoided. For further discussion of these subjects see the Audio/Radio Handbook published by National Semiconductor Corporation.

Applications Information (Continued)

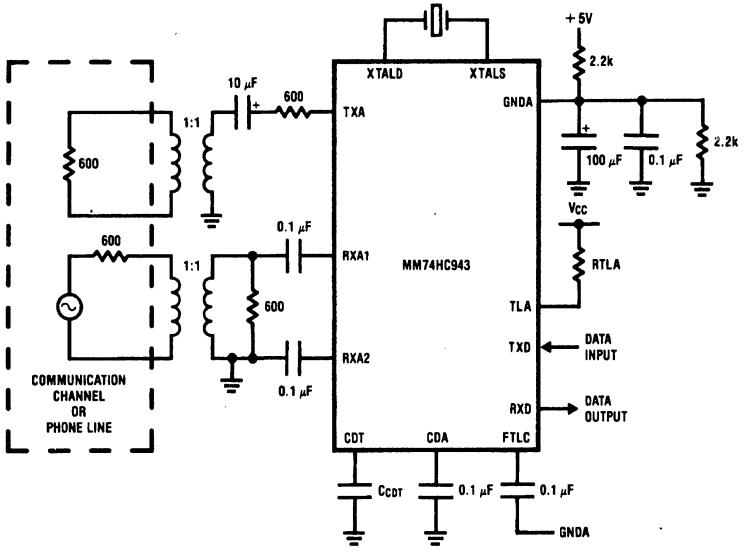
Interface Circuits for MM74HC943 300 Baud Modem

2 Wire Connection



TL/F/5349–4

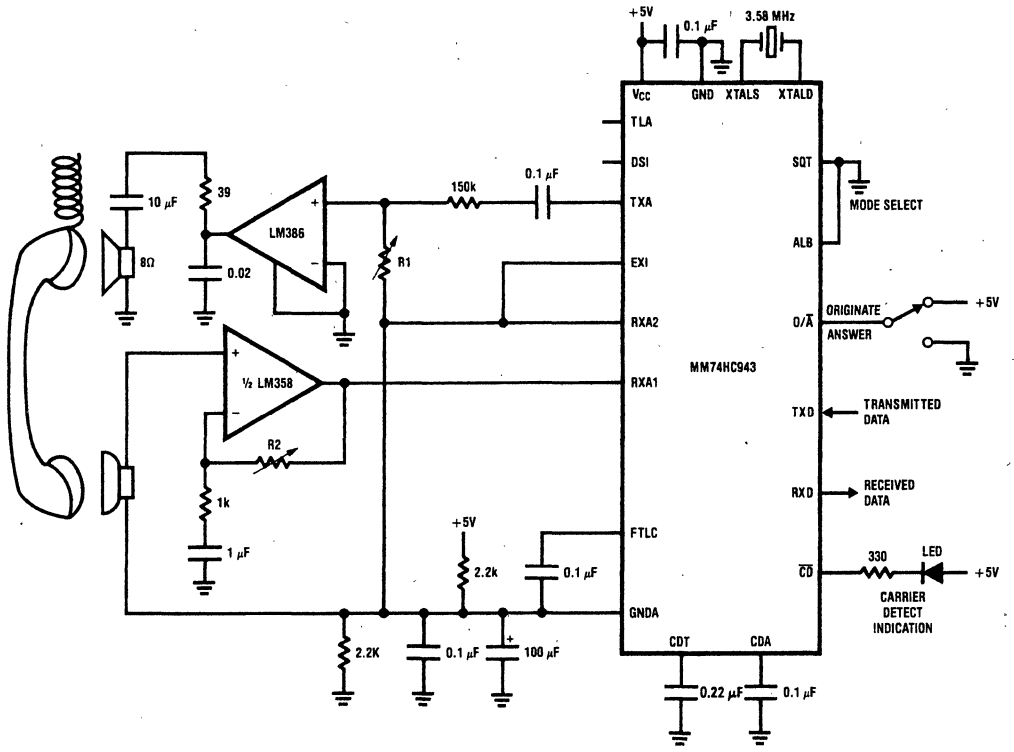
4 Wire Connection



TL/F/5349–5

C_{CDT} and R_{TLA} should be chosen to suit the application. See the Applications Information for more details.

Complete Acoustically Coupled 300 Baud Modem



TL/F/5349–6

Note: The efficiency of the acoustic coupling will set the values of R1 and R2.

National Semiconductor

microCMOS

MM54HC4002/MM74HC4002
Dual 4-Input NOR Gate

General Description

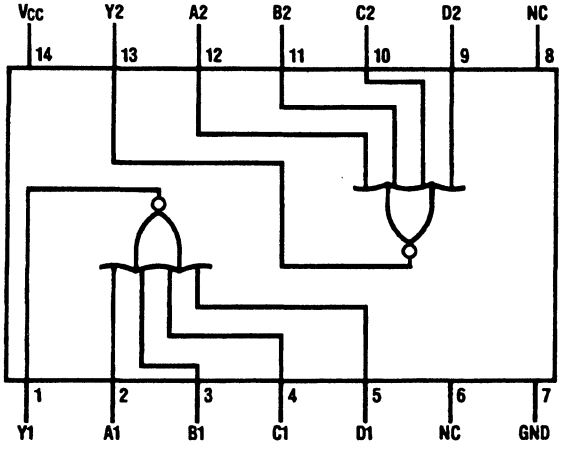
These NOR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4002/74HC4002 is functionally equivalent and pin-out compatible with the CD4002B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5154–1

$Y = \overline{A + B + C + D}$

Order Number MM54HC4002J or MM74HC4002J, N
See NS Package J14A or N14A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		11	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$		54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	40	120	151	179	ns
			4.5V	12	24	30	36	ns
			6.0V	10	20	26	30	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

microCMOS

MM54HC4016/MM74HC4016 Quad Analog Switch

General Description

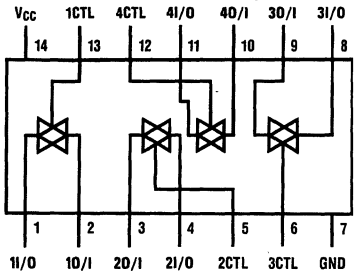
These devices are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. The '4016 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 50Ω typ.
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram

Dual-In-Line Package



TL/F/5350–1

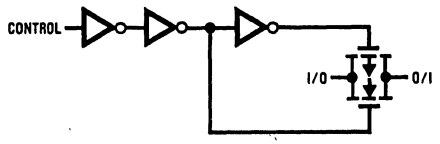
Top View

Order Number MM54HC4016J or MM74HC4016J, N
See NS Package J14A or N14A

Truth Table

Input	Switch
CTL	I/O-O/I
L	"OFF"
H	"ON"

Schematic Diagram



TL/F/5350–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	6.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			9.0V		1.8	1.8	1.8	V
			12.0V		2.4	2.4	2.4	V
R_{ON}	Maximum 'ON' Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} to GND (Figure 1)	4.5V	100	170	200	220	Ω
			9.0V	50	85	105	120	Ω
			12.0V	30	70	85	100	Ω
		V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} or GND (Figure 1)	2.0V	100	180	215	240	Ω
			4.5V	40	80	100	120	Ω
			9.0V	35	60	75	80	Ω
			12.0V	20	40	60	70	Ω
R_{ON}	Maximum 'ON' Resistance Matching	V_{CTL}=V_{IH} V_{IS}=V_{CC} to GND	4.5V	10	15	20	20	Ω
			9.0V	5	10	15	15	Ω
			12.V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND V_{CC}=2–6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch 'OFF' Leakage Current	V_{OS}=V_{CC} or GND V_{IS}=GND or V_{CC} V_{CTL}=V_{IL} (Figure 2)	5.5V		±60	±600	±600	nA
			9.0V		±80	±800	±800	nA
			12.0V		±100	±1000	±1000	nA
I_{IZ}	Maximum Switch 'ON' Leakage Current	V_{OS}=V_{CC} or GND V_{CTL}=V_{IH} (Figure 3)	5.5V		±40	±150	±150	nA
			9.0V		±50	±200	±200	nA
			12.0V		±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	5.5V		2.0	20	40	μA
			9.0V		8.0	80	160	μA
			12.0V		16.0	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so these values should be used.

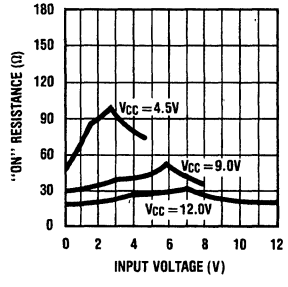
Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics V_{CC} = 2.0V–6.0V, C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C		74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ		Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V	25	50	62	75	ns
			4.5V	5	10	13	15	ns
			9.0V	4	8	12	14	ns
			12.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L = 1 kΩ	2.0V	32	100	125	150	ns
			4.5V	8	20	25	30	ns
			9.0V	6	12	15	18	ns
			12.0V	5	10	13	15	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	R_L = 1 kΩ	2.0V	45	168	210	252	ns
			4.5V	15	36	45	54	ns
			9.0V	10	32	40	48	ns
			12.0V	8	30	38	45	ns
f_{MAX}	Maximum Switch Frequency Response 20 log(V_I/V_O) = −3 dB		4.5V	35				MHz
			9.0V	40				MHz
	Cross Talk Control to Switch	(Figure 7)	4.5V	80				mV_{P-P}
	Cross Talk Between any Two Switches (Frequency at −50 dB)	(Figure 8)	4.5V					MHz
	Switch Feedthrough Input to Output	F = 5 MHz	4.5V					dB
		F = 10 MHz	4.5V					dB
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL} = GND		5				pF
C_{PD}	Power Dissipation Capacitance	(per switch)		15				pF

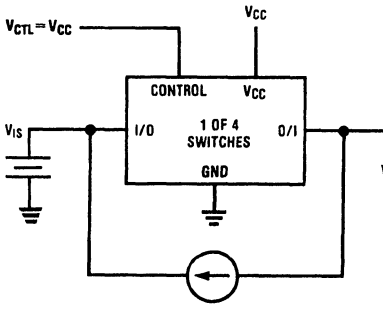
Typical Performance Characteristics

Typical "On" Resistance Versus Input Voltages ('4016)



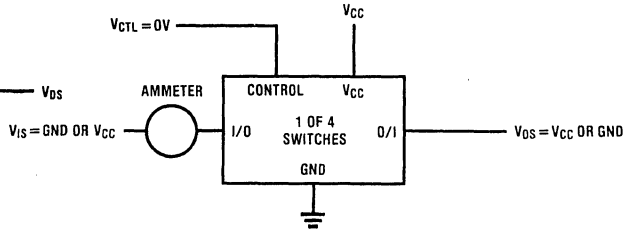
TL/F/5350–17

AC Test Circuits and Switching Time Waveforms



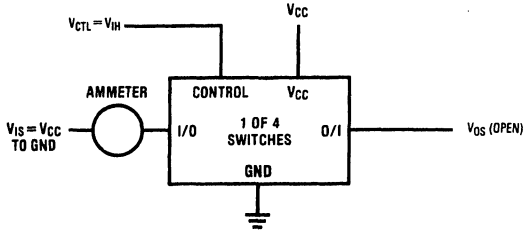
TL/F/5350-3

FIGURE 1. "ON" Resistance



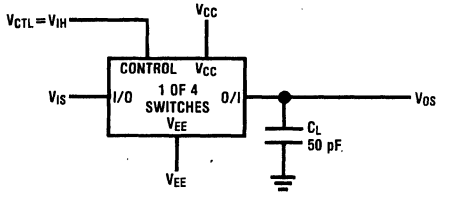
TL/F/5350-4

FIGURE 2. "OFF" Channel Leakage Current

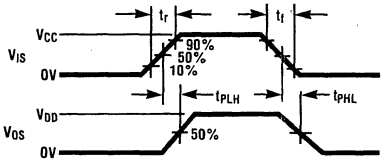


TL/F/5350-5

FIGURE 3. "ON" Channel Leakage Current

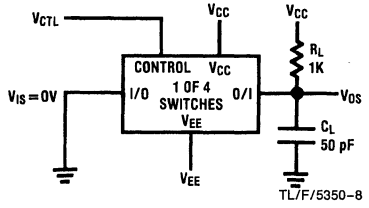


TL/F/5350-6

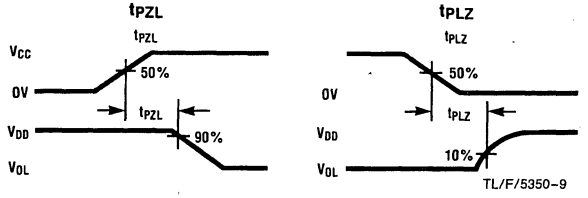


TL/F/5350-7

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



TL/F/5350-8



TL/F/5350-9

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

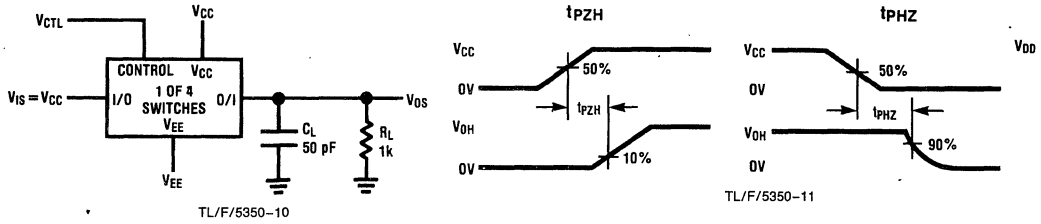


FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

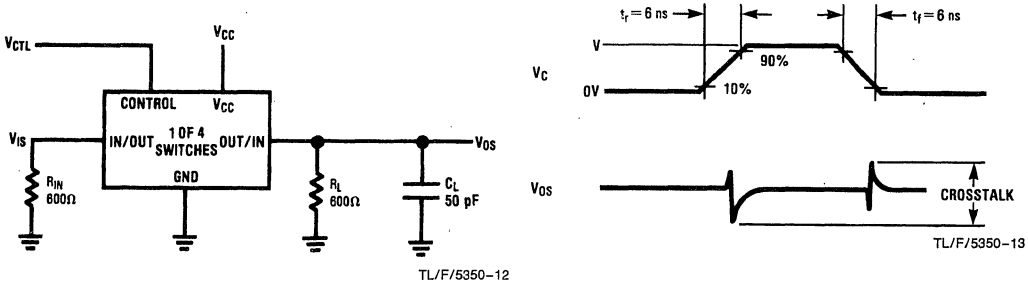


FIGURE 7. Crosstalk: Control Input to Signal Output

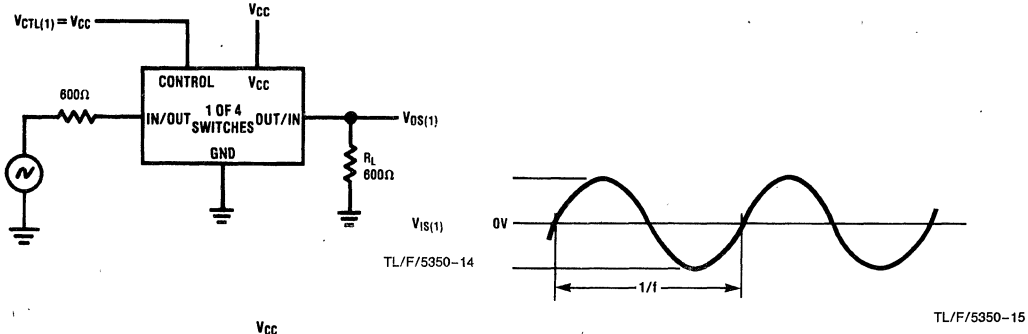


FIGURE 8: Crosstalk Between Any Two Switches

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4017/MM74HC4017
Decade Counter/Divider with 10 Decoded Outputs

General Description

The MM54HC4017/MM74HC4017 is a 5-stage Johnson counter with 10 decoded outputs that utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. Each of the decoded outputs is normally low and sequentially goes high on the low to high transition of the clock input. Each output stays high for one clock period of the 10 clock period cycle. The CARRY output transitions low to high after OUTPUT 10 goes low, and can be used in conjunction with the CLOCK ENABLE to cascade several stages. The CLOCK ENABLE input disables counting when in the high state. A RESET input is also provided which when taken high sets all the decoded outputs low except output 0.

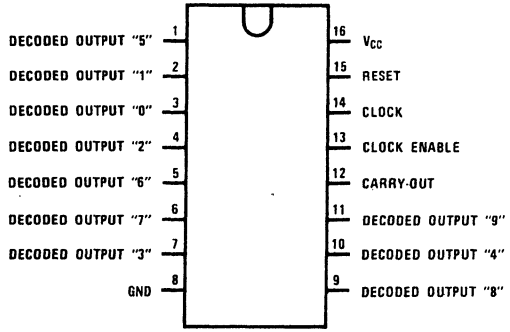
The MM54HC4017/MM74HC4017 is functionally and pinout equivalent to the CD4017BM/CD4017BC. It can drive up to 10 low power Schottky equivalent loads. All inputs are protected from damage due to static discharge by diodes from V_{CC} and ground.

Features

- Wide power supply range: 2–6V
- Typical operating frequency: 30 MHz
- Fanout of 10 LS-TTL loads
- Low quiescent current: 80 μA (74HC Series)
- Low input current: 1.0 μA

Connection Diagram

Dual-In-Line and Flat Package



TL/F/5351–1

Order Number MM54HC4017J or MM74HC4017J,N
See NS Package J16A or N16E

3

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency	Measured with respect to carry line	50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Carry-Out Line		26	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Enable Decode-Out Lines		27	44	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Decode Out		23	40	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Carry Out		23	40	ns
t_S	Minimum Clock Inhibit to Clock Set-Up Time		12	20	ns
t_W	Minimum Clock or Reset Pulse Width		8	16	ns
t_{REM}	Minimum Reset Removal Time		20	10	ns

AC Electrical Characteristics $V_{CC}=2.0$–$6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

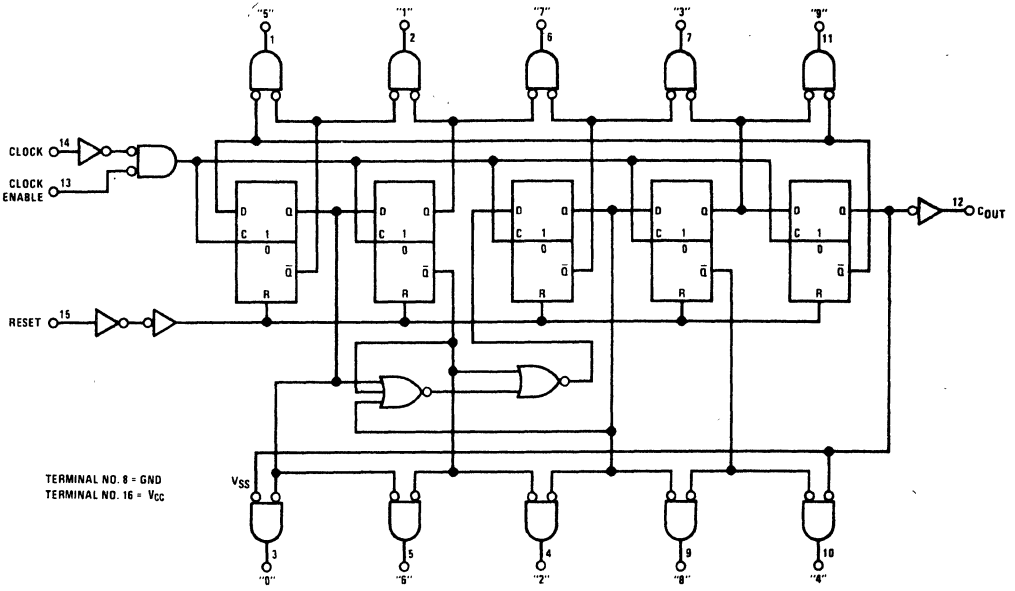
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency	Measured with respect to carry line	2.0V		4	3	3	MHz
			4.5V		20	16	13	MHz
			6.0V		23	18	15	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Carry-Out Line		2.0V	89	250	312	375	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Enable to Decode Out Line		2.0V	90	250	312	375	ns
			4.5V	25	50	63	75	ns
			6.0V	20	43	54	65	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Decode Out		2.0V	82	230	288	345	ns
			4.5V	22	46	58	69	ns
			6.0V	18	39	49	59	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Reset or Clock to Carry Out		2.0V	82	230	288	345	ns
			4.5V	22	46	58	69	ns
			6.0V	18	39	49	59	ns
t_W	Minimum Reset or Clock Pulse Width		2.0V	30	80	100	120	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	18	21	ns
t_{REM}	Minimum Reset Removal Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_S	Minimum Clock Inhibit to Clock Set-Up Time		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	8	15	19	22	ns
			6.0V	7	13	16	19	ns
t_r, t_f	Minimum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)						pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

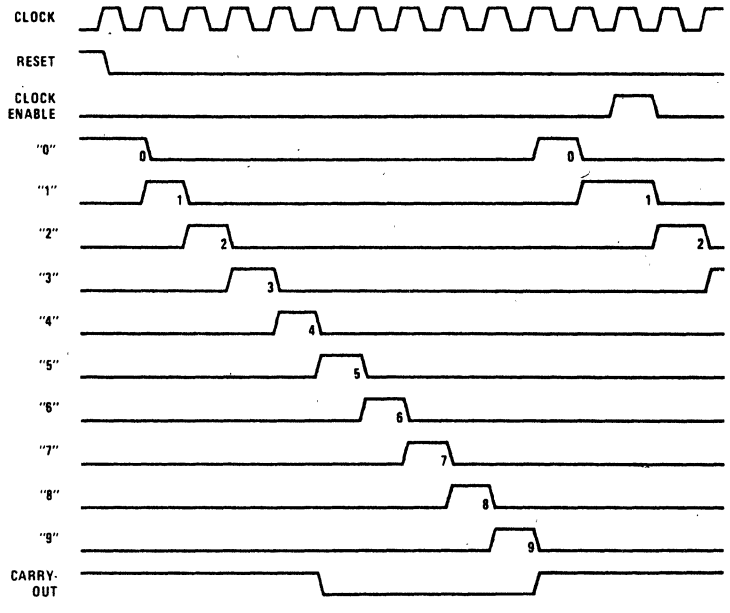
3

Logic and Timing Diagrams

MM54HC4017/MM74HC4017



TL/F/5351–2



TL/F/5351–3

National Semiconductor

microCMOS

MM54HC4020/MM74HC4020 14-Stage Binary Counter
MM54HC4024/MM74HC4024 7-Stage Binary Counter
MM54HC4040/MM74HC4040 12-Stage Binary Counter

General Description

The MM54HC4020/MM74HC4020, MM54HC4024/MM74HC4024, MM54HC4040/MM74HC4040, are high speed binary ripple carry counters. These counters are implemented utilizing microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4020 is a 14 stage counter, the 'HC4040 is a 12-stage counter, and the 'HC4024 is a 7-stage counter. All these devices are incremented on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input.

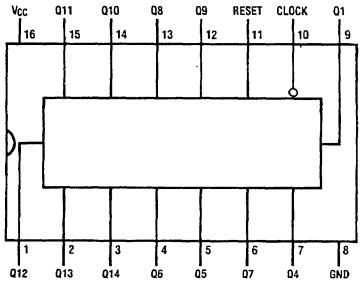
These devices are pin equivalent to the CD4020, CD4024 and CD4040 respectively. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

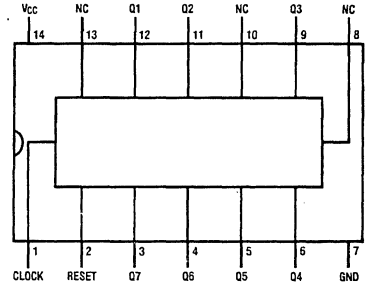
- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74HC Series)
- Output drive capability: 10 LS-TTL loads

Connection Diagrams

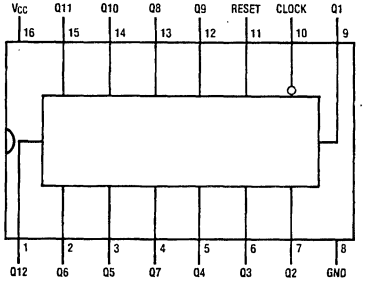
Dual-In-Line Packages



TOP VIEW TL/F/5216–1



TOP VIEW TL/F/5216–2



TOP VIEW TL/F/5216–3

Order Number MM54HC4020J, MM54HC4024J, MM54HC4040J, MM74HC4020J, N, MM74HC4024J, N or MM74HC4040J, N
See NS Package J14A, J16A, N14A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q	(Note 5)	17	35	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

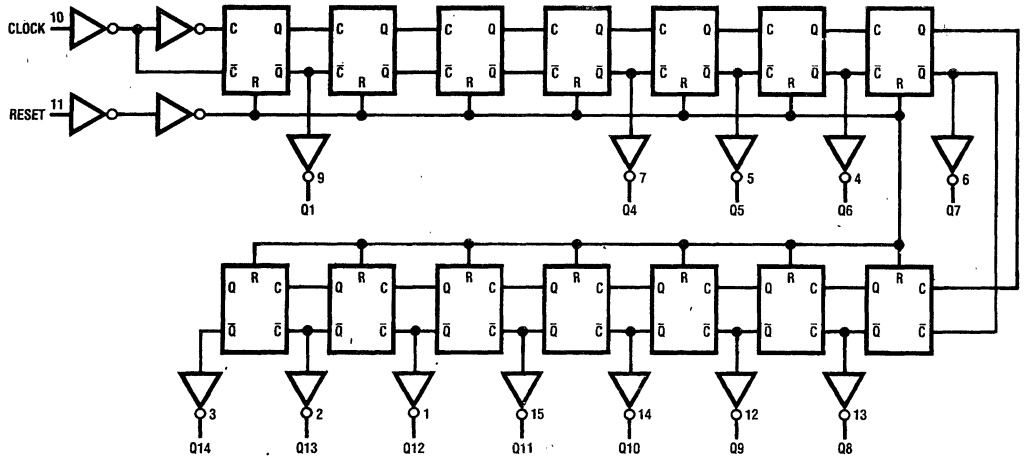
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V	10	6	5	4	MHz
			4.5V	40	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_1		2.0V	80	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
T_{PHL}, t_{PLH}	Maximum Propagation Delay Between Stages from Q_n to Q_{n+1}		2.0V	80	125	156	188	ns
			4.5V	18	25	31	38	ns
			6.0V	15	21	26	31	ns
t_{PHL}	Maximum Propagation Delay Reset to Q ('4024 only)		2.0V	80	210	265	313	ns
			4.5V	21	42	53	63	ns
			6.0V	18	36	45	53	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q ('4020 and '4040)		2.0V	72	240	302	358	ns
			4.5V	24	48	60	72	ns
			6.0V	20	41	51	61	ns
t_{REM}	Minimum Reset Removal Time		2.0V		100	126	149	ns
			4.5V		20	25	50	ns
			6.0V		16	21	25	ns
t_W	Minimum Pulse Width		2.0V		90	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	18	20	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
t_r, t_f	Maximum Input Rise and Fall Time				1000	1000	1000	ns
					500	500	500	ns
					400	400	400	ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: Typical Propagation delay time to any output can be calculated using: $t_P=17+12(N-1)$ ns; where N is the number of the output, Q_W, at $V_{CC}=5V$.

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

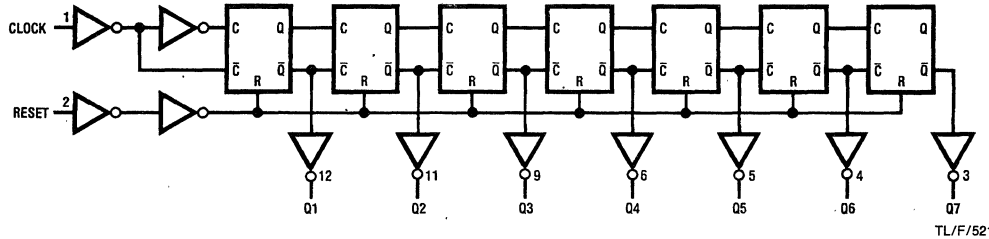
Logic Diagrams

MM54HC4020/MM74HC4020



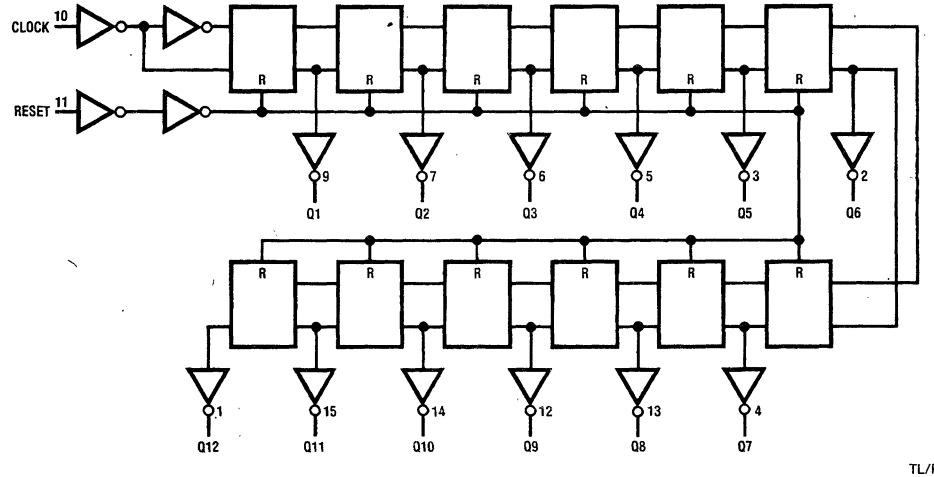
TL/F/5216–5

MM54HC4024/MM74HC4024



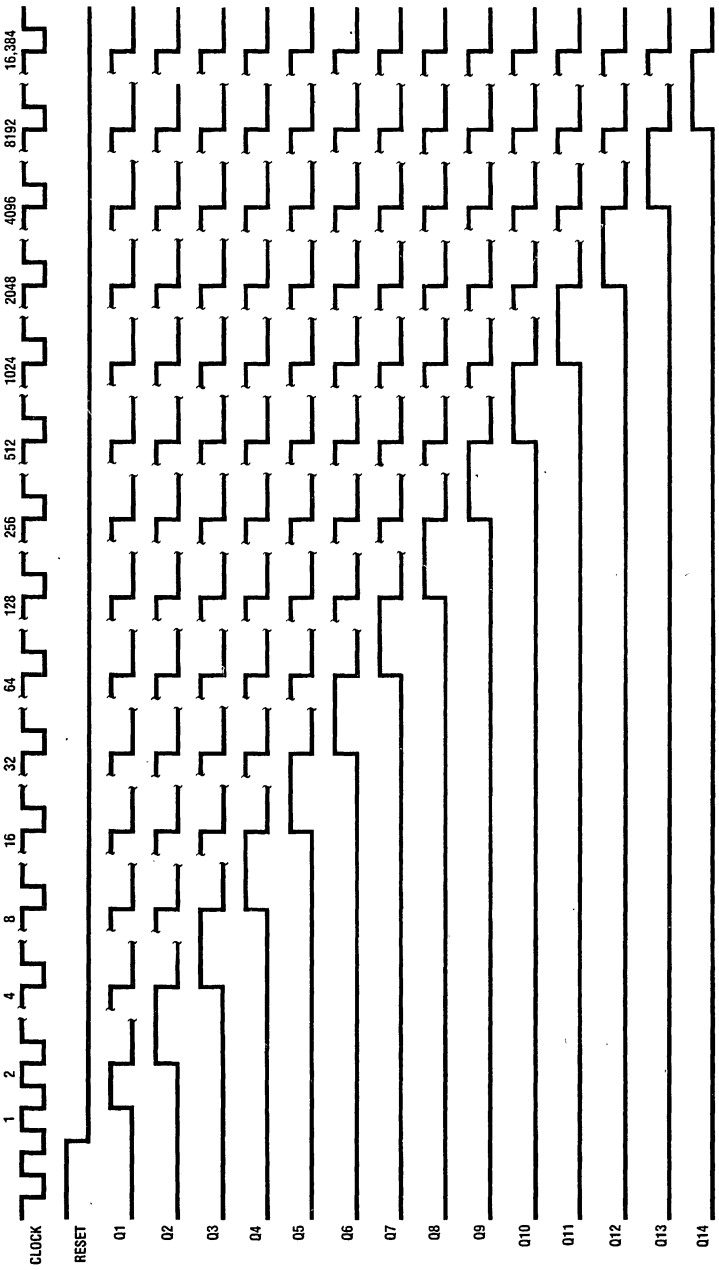
TL/F/5216–6

MM54HC4040/MM74HC4040



TL/F/5216–7

Timing Diagram



National Semiconductor

PRELIMINARY

microCMOS

MM54HC4046/MM74HC4046 CMOS Phase Lock Loop

General Description

The MM54HC4046/MM74HC4046 is a low power phase lock loop utilizing 3.5μ silicon-gate p-well microCMOS technology to obtain high frequency operation both in the phase comparator and VCO sections. This device contains a low power linear voltage controlled oscillator (VCO), a source follower, and three phase comparators. The three phase comparators have a common signal input and a common comparator input. The signal input has a self biasing amplifier allowing signals to be either capacitively coupled to the phase comparators with a small signal or directly coupled with standard input logic levels. This device is similar to the CD4046 except that the Zener diode of the metal gate CMOS device has been replaced with a third phase comparator.

Phase Comparator I is an exclusive OR (XOR) gate. It provides a digital error signal that maintains a 90 phase shift between the VCO's center frequency and the input signal (50% duty cycle input waveforms. This phase detector is more susceptible to locking onto harmonics of the input frequency than phase comparator I, but provides better noise rejection.

Phase comparator III is an SR flip-flop gate. It can be used to provide the phase comparator functions and is similar to the first comparator in performance.

Phase comparator II is an edge sensitive digital sequential network. Two signal outputs are provided, a comparator output and a phase pulse output. The comparator output is a TRI-STATE® output that provides a signal that locks the VCO output signal to the input signal with 0 phase shift between them. This comparator is more susceptible to noise throwing the loop out of lock, but is less likely to lock onto harmonics than the other two comparators.

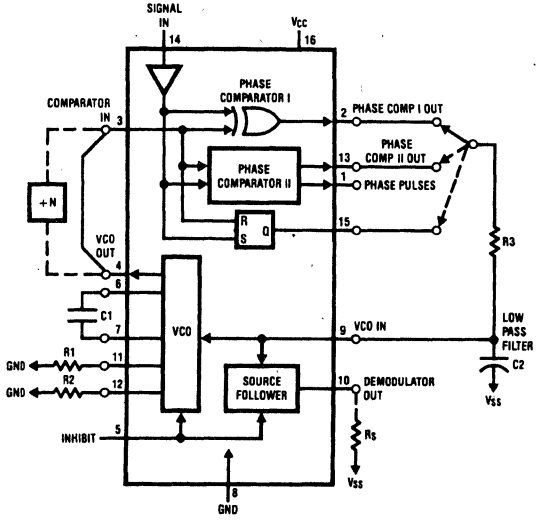
In a typical application all three comparators feed an external filter network which in turn feeds the VCO input. This input is a very high impedance CMOS input which also drives the source follower. The VCO's operating frequency is set by three external components connected to the C1A, C1B, R1 and R2 pins. An inhibit pin is provided to disable the VCO and the source follower, providing a method of putting the IC in a low power state.

The source follower is a MOS transistor whose gate is connected to the VCO input and whose drain connects the Demodulator output. This output normally is used by tying a resistor from pin 10 to ground, and provides a means of looking at the VCO input without loading down modifying the characteristics of the PLL filter.

Features

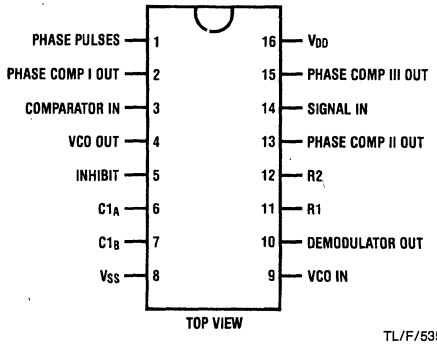
- Low dynamic power consumption: (V_{CC} = 4.5V)
- Maximum VCO operating frequency: 20 MHz (V_{CC} = 4.5V)
- Fast comparator response time (V_{CC} = 4.5V)
  - Comparator I: 20 ns
  - Comparator II: 25 ns
  - Comparator III: 20 ns
- VCO has high linearity and high temperature stability

Block and Connection Diagrams



TL/F/5352–1

Dual-In-Line Package



TL/F/5352–2

Order Number MM54HC4046J or MM74HC4046J,N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to + 7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 8.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 3,5,9)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{IN}	Maximum Input Current (Pin 14)	V_{IN} = V_{CC} or GND	6.0V		2	3	4	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 2.0 to 6.0V, CL = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified.)

Symbol	Parameters	Conditions	V_{CC}	T = 25C		74HC	54HC	Units
				Typ	Guaranteed Limits			
	AC Coupled Input Sensitivity, Signal In	C (series) = 100 pF f_{IN} = 500 kHz	2.0V 4.5V 6.0V	100 200 300	200 400 600	225 450 650	250 500 700	mV mV mV
t_r, t_f	Maximum Output Rise and Fall Time		2.0V 4.5V 6.0V	30 9 8	75 15 12	95 19 15	110 22 19	ns ns ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
Phase Comparator I								
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5 6.0V	58 20 18				ns ns ns
C_{PD}	Maximum Power Dissipation Capacitance							pF
Phase Comparator II								
t_{PHL}, t_{PLH}	Maximum Propagation Delay Comp. Output		2.0V 4.5V 6.0V	100 45 40				ns ns ns
t_{PZL}	Maximum TRI-STATE Enable Time		2.0V 4.5V 6.0V	110 50 45				ns ns ns
t_{PZH}	Maximum TRI-STATE Enable Time		2.0V 4.5V 6.0V	100 40 35				ns ns ns
t_{PLZ}	Maximum TRI-STATE Disable Time		2.0V 4.5V 6.0V	110 50 45				ns ns ns
t_{PHZ}	Maximum TRI-STATE Disable Time		2.0V 4.5V 6.0V	110 45 40				ns ns ns
t_{PHL}	Maximum Propagation Delay High to Low to Phase Pulses		2.0V 4.5V 6.0V	100 40 35				ns ns ns
t_{PLH}	Maximum Propagation Delay Low to High to Phase Pulses		2.0V 4.5V 6.0V	110 50 45				ns ns ns
C_{PD}	Maximum Power Dissipation Capacitance							pF
Phase Comparator III								
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V 4.5V 6.0V	120 50 45				ns ns ns
C_{PD}	Maximum Power Dissipation Capacitance							pF

AC Electrical Characteristics (Continued)

V_{CC} = 2.0 to 6.0V, CL = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified.)

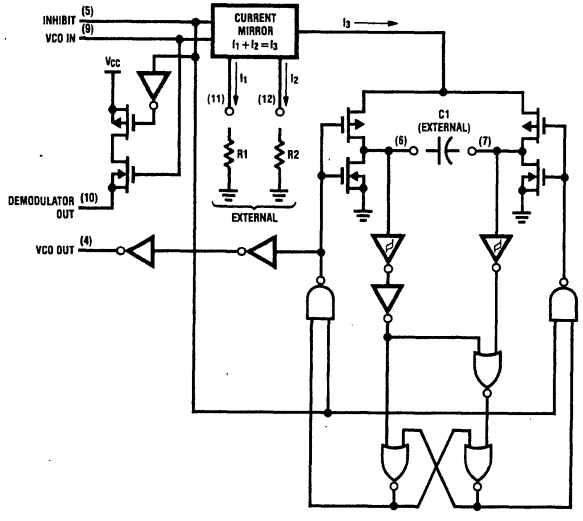
Symbol	Parameters	Conditions	V_{CC}	T = 25C		74HC	54HC	Units
				Typ	Guaranteed Limits			
Voltage Controlled Oscillator (Specified to operate from V_{CC} = 3.0V to 6.0V								
f_{MAX}	Maximum Operating Frequency	C1 = 10pF, R1 = 100, R2 = ∞ $VCO_{in} = V_{CC}$	4.5V 6.0V	15 18				MHz MHz
	Linearity	$VCO_{in} = 2.25 \pm 1V$ $VCO_{in} = 3 \pm 1.5V$	4.5V 6.0V	1.0 1.0				% %
	Temperature-Frequency Stability	No Frequency Offset	4.5V 6.0V					%/ C %/ C
	Temperature-Frequency Stability	Frequency Offset	4.5V 6.0V					%/ C %/ C
	Duty Cycle			50				%
Demodulator Output								
	Offset Voltage VCO_{in}-V_{dem}	R_S = 1k Ohm		1.5	2.2	2.7	3.2	V
	Linearity	R_S = 5k Ohm $VCO_{in} = 2.25V \pm 1.0V$			0.1	0.2	0.3	%

Detailed Circuit Description

VOLTAGE CONTROLLED OSCILLATOR/SOURCE FOLLOWER

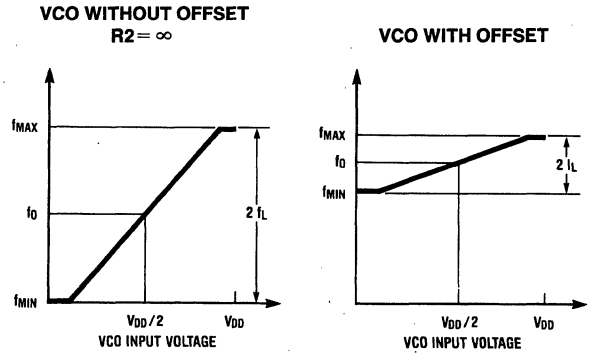
The VCO requires two or three external components to operate. These are R1, R2, C1. Resistor R1 and capacitor C1 are selected to determine the center frequency of the VCO. (See typical performance curves) R2 can be used to set the offset frequency with 0V at VCO input. If R2 is omitted the VCO range is from 0Hz; as R2 is decreased the offset frequency is increased. The effect of R2 is shown in the design information table and typical performance curves. By increasing the value of R2 the lock range of the PLL is decreased and the gain (Volts/Hz) is increased. Thus, for a narrow lock range large swings on the VCO input will cause less frequency variation.

Internally the resistors set a current in a current mirror as shown in *Figure 1*. The mirrored current drives one side of



TL/F/5352–3

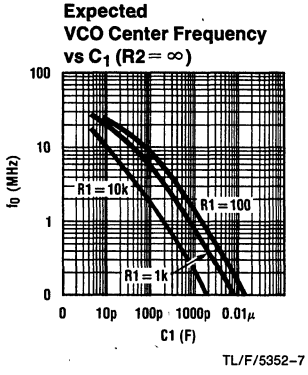
FIGURE 1. Logic Diagram for VCO



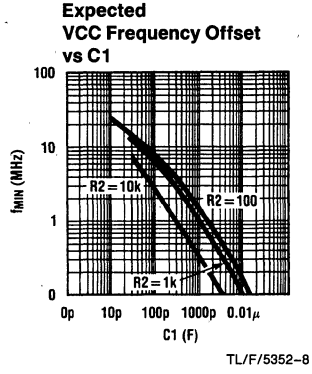
(a)

Comparator I		Comparator II		Comparator III	
$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$	$R_2 = \infty$	$R_2 \neq \infty$
–Given: f_0 –Use f_0 with *Figure 2c* to determine R1 and C1	–Given: f_0 and f_L –Calculate f_{min} from the equation $f_{min} = f_0 - f_L$ –Use f_{min} with *Figure 2d* to determine R2 and C1 –Calculate f_{max}/f_{min} from the equation $f_{max}/f_{min} = f_0 + f_L/f_0 - f_L$ –Use f_{max}/f_{min} with *Figure 2e* to determine ratio R2/R1 to obtain R1	–Given: f_{max} –Calculate f_0 from the equation $f_0 = f_{max}/2$ –Use f_0 with *Figure 2c* to determine R1 and C1	–Given: f_{min} and f_{max} –Use f_{min} with *Figure 2d* to determine R2 and C1 –Calculate f_{max}/f_{min} –Use f_{max}/f_{min} with *Figure 2e* to determine ratio R2/R1 to obtain R1		

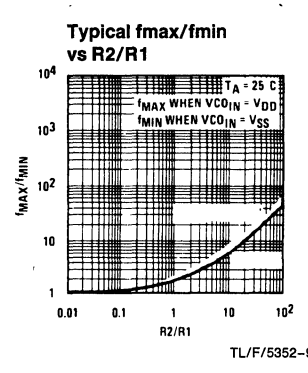
(b)



(c)



(d)



(e)

FIGURE 2. VCO Characteristics: a) Idealized Transfer Function b) Determining External Components c), d), e) Typical frequency characteristics versus component values

Detailed Circuit Description (Continued)

the capacitor once the capacitor charges up to the threshold of the schmitt trigger the oscillator logic flips the capacitor over and causes the mirror to charge the opposite side of the capacitor. The output from the internal logic is then taken to pin 4.

The input to the VCO is a very high impedance CMOS input and so it will not load down the loop filter, easing the filters design. In order to make signals at the VCO input accessible without degrading the loop performance a source follower transistor is provided. This transistor can be used by connecting a resistor to ground and its drain output will follow the VCO input signal.

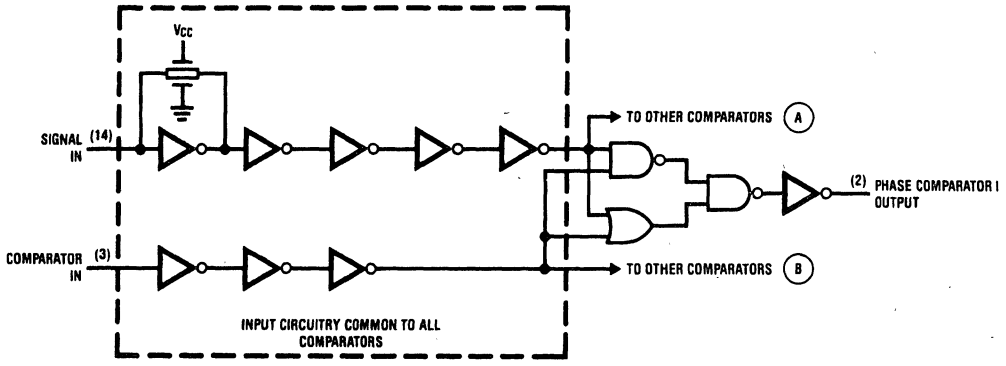
An inhibit signal is provided to allow disabling of the VCO and the source follower. This is useful if the internal VCO is not being used, but an external one is. A logic high on inhibit disables the VCO and source follower.

The output of the VCO is a standard high speed CMOS output with an equivalent LSTTL fanout of 10. The VCO output is approximately a square wave. This output can either directly feed the comparator input of the phase comparators or feed external prescalers (counters) to enable frequency synthesis.

PHASE COMPARATORS

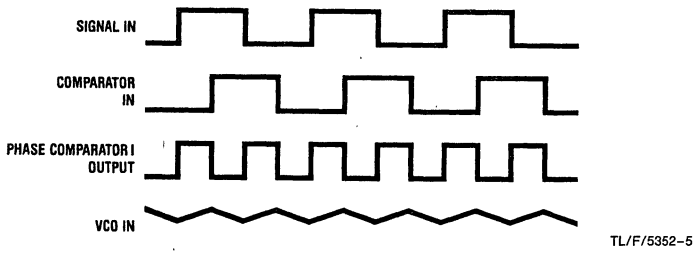
All three phase comparators have two inputs, Signal In and Comparator In. The Signal In has a special DC bias network that enables AC coupling of input signals. If the signals are not AC coupled then this input requires logic levels the same as standard 54HC/74HC. The Comparator input is a standard digital input. Both input structures are shown in *Figure 3.*

The outputs of these comparators are essentially standard 54HC/74HC voltage outputs. (Comparator II is TRI-STATE).



TL/F/5352–4

FIGURE 3. Logic Diagram for Phase Comparator I and the common input circuit for all three comparators



TL/F/5352–5

FIGURE 4. Typical Phase Comparator I. Waveforms

Detailed Circuit Description (Continued)

Thus in normal operation V_{CC} and ground voltage levels are fed to the loop filter. This differs from some phase detectors which supply a current output to the loop filter and this should be considered in the design. (The CD4046 also provides a voltage.)

Figure 5 shows the state tables for all three comparators.

PHASE COMPARATOR I

This comparator is a simple XOR gate similar to the 54/74HC86, and its operation is similar to an overdriven balanced modulator. To maximize lock range the input frequencies must have a 50% duty cycle. Typical input and output waveforms are shown in *Figure 4*. The output of the phase detector feeds the loop filter which averages the output voltage. The frequency range upon which the PLL will lock onto if initially out of lock is defined as the capture range. The capture range for phase detector I is dependent on the loop filter employed. The capture range can be as large as the lock range which is equal to the VCO frequency range.

To see how the detector operates refer to *Figure 4*. When two square wave inputs are applied to this comparator, an output waveform whose duty cycle is dependent on the phase difference between the two signals results. As the phase difference increases the output duty cycle increases and the voltage after the loop filter increases. Thus in order to achieve lock, when the PLL input frequency increases the VCO input voltage must increase and the phase difference between comparator in and signal in will increase. At an input frequency equal f_{min}, the VCO input is at 0V and this requires the phase detector output to be ground hence the two input signals must be in phase. When the input frequency is f_{max} then the VCO input must be V_{CC} and the phase detector inputs must be 180° out of phase.

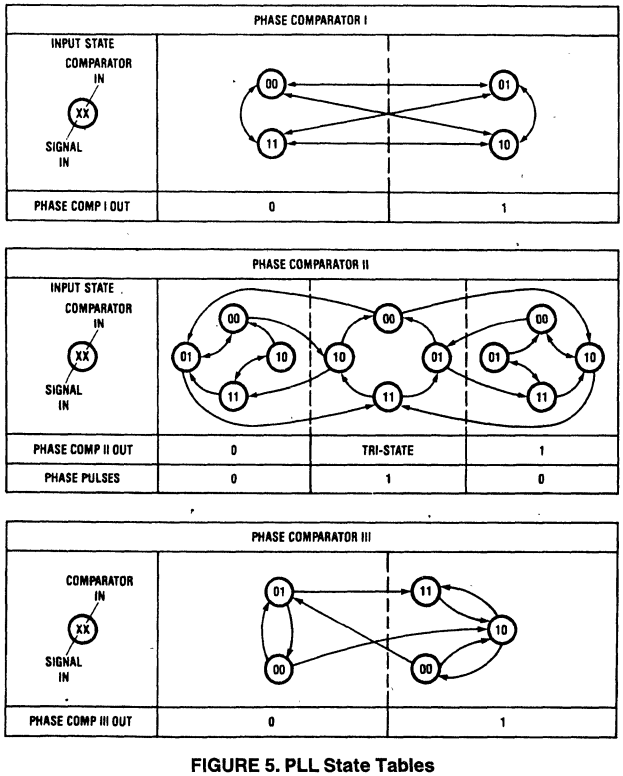
The XOR is more susceptible to locking onto harmonics of the signal input than the digital phase detector II. This can be seen by noticing that a signal 2 times the VCO frequency results in the same output duty cycle as a signal equal the VCO frequency. The difference is that the output frequency of the 2f example is twice that of the other example. The loop filter and the VCO range should be designed to prevent locking on to harmonics.

PHASE COMPARATOR II

This detector is a digital memory network. It consists of four flip-flops and some gating logic, a three state output and a phase pulse output as shown in *Figure 6*. This comparator acts only on the positive edges of the input signals and is thus independent of signal duty cycle.

Phase comparator II operates in such a way as to force the PLL into lock with 0 phase difference between the VCO output and the signal input positive waveform edges. *Figure 7* shows some typical loop waveforms. First assume that the signal input phase is leading the comparator input. This

Phase Comparator State Diagrams



TL/F/5352–10

FIGURE 5. PLL State Tables

Detailed Circuit Description (Continued)

means that the VCO's frequency must be increased to bring its leading edge into proper phase alignment. Thus the phase detector II output is set high. This will cause the loop filter to charge up the VCO input increasing the VCO frequency. Once the leading edge of the comparator input is detected the output goes tri-state holding the VCO input at the loop filter voltage. If the VCO still lags the signal then the phase detector will again charge up to VCO input for the time between the leading edges of both waveforms.

If the VCO leads the signal then when the leading edge of the VCO is seen the output of the phase comparator goes low. This discharges the loop filter until the leading edge of the signal is detected at which time the output tri-states itself again. This has the effect of slowing down the VCO to again make the rising edges of both waveform coincident.

When the PLL is out of lock the VCO will be running either slower or faster than the signal input. If it is running slower the phase detector will see more signal rising edges and so the output of the phase comparator will be high a majority of the time, raising the VCO's frequency. Conversely, if the VCO is running faster than the signal the output of the detector will be low most of the time and the VCO's output frequency will be decreased.

As one can see when the PLL is locked the output of phase comparator II will be almost always tri-stated except for minor corrections at the leading edge of the waveforms. When the detector is tri-state the phase pulse output is high. This output can be used to determine when the PLL is in the locked condition.

This detector has several interesting characteristics. Over the entire VCO frequency range there is no phase difference between the comparator input and the signal input. The lock range of the PLL is the same as the capture range.

Minimal power is consumed in the loop filter since in lock the detector output is a high impedance. Also when no signal is present the detector will see only VCO leading edges, and so the comparator output will stay low forcing the VCO to f_{min} operating frequency.

Phase comparator II is more susceptible to noise causing the phase lock loop to unlock. If a noise pulse is seen on the signal input, the comparator treats it as another positive edge of the signal and will cause the output to go high until the VCO leading edge is seen, potentially for a whole signal input period. This would cause the VCO to speed up during that time. When using the phase comparator I the output of that phase detector would be disturbed for only the short duration of the noise spike and would cause less upset.

PHASE COMPARATOR III

This comparator is a simple S-R Flip-Flop which can function as a phase comparator *Figure 8*. It has some similar characteristics to the edge sensitive comparator. To see how this detector works assume input pulses are applied to the signal and comparator inputs as shown in *Figure 9*. When the signal input leads the comparator input the flop is set. This will charge up the loop filter and cause the VCO to speed up, bringing the comparator into phase with the signal input. When using short pulses as input this comparator behaves very similar to the second comparator. But one can see that if the signal input is a long pulse, the output of the comparator will be forced to a one no matter how many comparator input pulses are received. Also if the VCO input is a square wave (as it is) and the signal input is pulse then the VCO will force the comparator output low much of the time. Therefore it is ideal to condition the signal and comparator input to short pulses. This is most easily done by using a series capacitor.

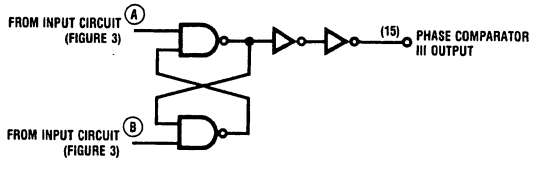


FIGURE 8. Phase Comparator III Logic Diagram

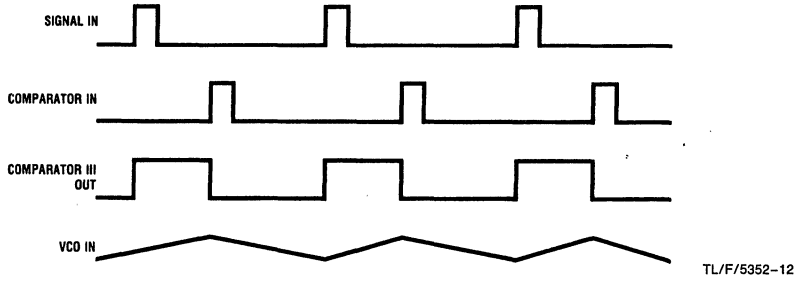
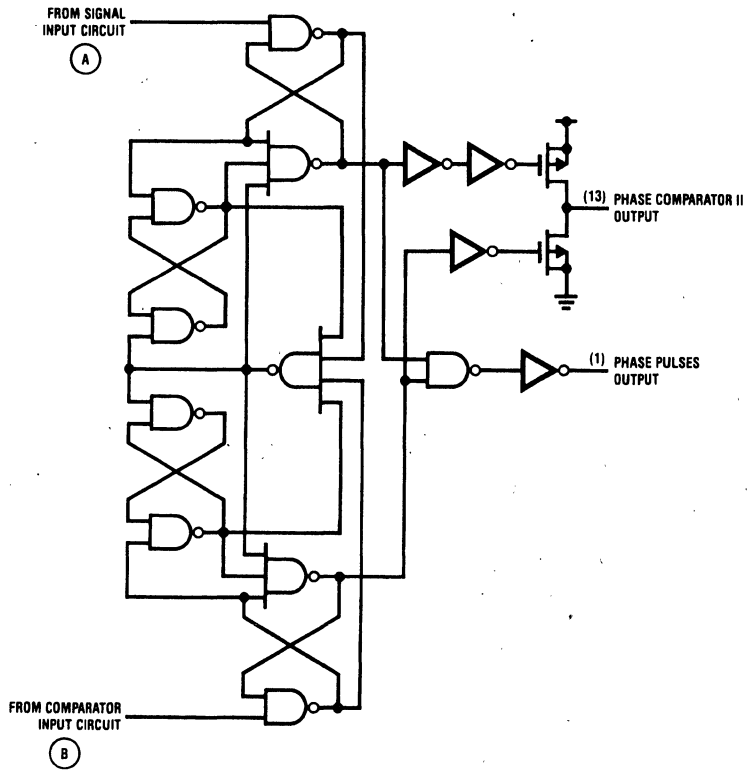
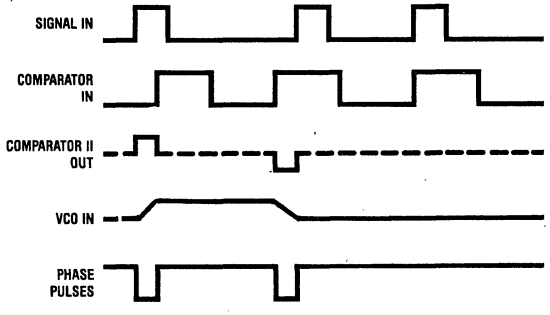


FIGURE 9. Typical Waveforms for Phase Comparator III



TL/F/5352–14

FIGURE 6. Logic Diagram for Phase Comparator II



TL/F/5352–13

FIGURE 7. Typical Phase Comparator II Output Waveforms

National Semiconductor

microCMOS

MM54HC4049/MM74HC4049 Hex Inverting Logic Level Down Converter MM54HC4050/MM74HC4050 Hex Logic Level Down Converter

General Description

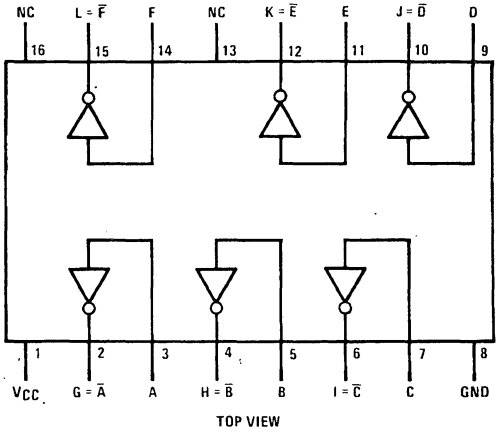
The MM54HC4049/MM74HC4049 and the MM54HC4050/MM74HC4050 utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and have a modified input protection structure that enables these parts to be used as logic level translators which will convert high level logic to a low level logic while operating from the low logic supply. For example, 0–15V CMOS logic can be converted to 0–5V logic when using a 5V supply. The modified input protection has no diode connected to V_{CC}, thus allowing the input voltage to exceed the supply. The lower zener diode protects the input from both positive and negative static voltages. In addition each part can be used as a simple buffer or inverter without level translation. The MM54HC4049/MM74HC4049 is pin and functionally compatible to the CD4049BM/CD4049BC and the MM54HC4050/MM74HC4050 is compatible to the CD4050BM/CD4050BC

Features

- Typical propagation delay: 8 ns
- Wide power supply range: 2V–6V
- Low quiescent supply current: 20 μA maximum (74HC)
- Fanout of 10 LS-TTL loads

Connection Diagrams

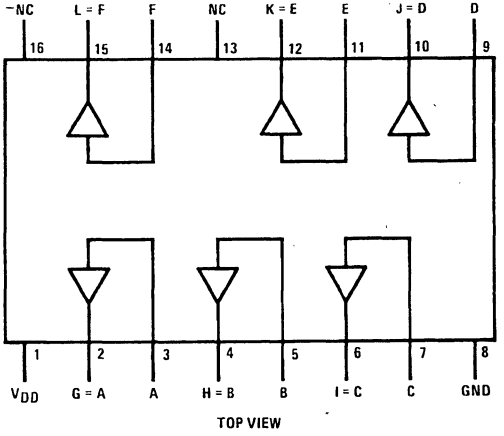
Dual-In-Line Package



TOP VIEW

TL/F/5214–1

Dual-In-Line Package



TOP VIEW

TL/F/5214–2

Order Number MM54HC4049J, MM54HC4050J, MM74HC4049J,N or MM74HC4050J,N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to +18V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{ZK}, I_{OK})	−20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temp. Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input Voltage (V_{IN})	0	15	V
DC Output Voltage (V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40°C to 85°C	54HC T_A=−55°C to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	60V		±0.1	±1.0	±1.0	μA
		V_{IN}=15V	6.0V		±0.5	±5	±5	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		8	15	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40°$ to $85°C$	54HC $T_A=-55°$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	30	85	100	130	ns
			4.5V	10	17	20	26	ns
			6.0V	9	15	18	22	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		25				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4051/MM74HC4051 8-Channel Analog Multiplexer
MM54HC4052/MM74HC4052 Dual 4-Channel Analog Multiplexer
MM54HC4053/MM74HC4053 Triple 2-Channel Analog Multiplexer

General Description

These multiplexers are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Also these switches contain linearization circuitry which lowers the on resistance and increases switch linearity. These devices allow control of up to ±6V (peak) analog signals with digital control signals of 0 to 6V. Three supply pins are provided for V_{CC}, ground, and V_{EE}. This enables the connection of 0–5V logic signals when $V_{CC}=5V$ and an analog input range of ±5V when $V_{EE}=5V$. All three devices also have an inhibit control which when high will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

MM54HC4051/MM74HC4051: This device connects together the outputs of 8 switches, thus achieving an 8 channel Multiplexer. The binary code placed on the A, B, and C select lines determines which one of the eight switches is "on", and connects one of the eight inputs to the common output.

MM54HC4052/MM74HC4052: This device connects together the outputs of 4 switches in two sets, thus achieving a pair of 4-channel multiplexers. The binary code placed on the A, and B select lines determine which switch in each 4 channel section is "on", connecting one of the four inputs in each section to its common output. This enables the implementation of a 4-channel differential multiplexer.

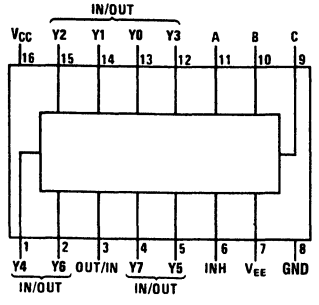
MM54HC4053/MM74HC4053: This device contains 6 switches whose outputs are connected together in pairs, thus implementing a triple 2 channel multiplexer, or the equivalent of 3 single-pole-double throw configurations. Each of the A, B, or C select lines independently controls one pair of switches, selecting one of the two switches to be "on".

Features

- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Logic level translation to enable 5V logic with ±5V analog signals
- Low quiescent current: 80 μA maximum (74HC)
- Matched Switch characteristic

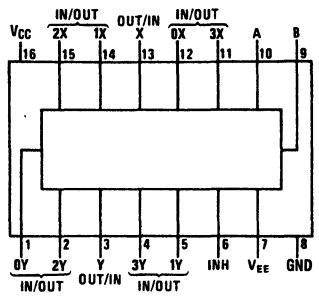
Connection Diagrams

Dual-In-Line Packages



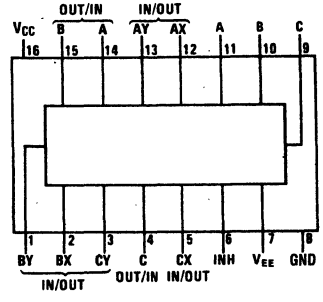
TL/F/5353–1

Top View



TL/F/5353–2

Top View



TL/F/5353–3

Top View

Order Number MM54HC4051J, MM54HC4052J, MM54HC4053J, MM74HC4051J, N, MM74HC4052J, N or MM74HC4053J, N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
Output Current, per pin (I_{OUT})	±25 mA
V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
Supply Voltage (V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)			
V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter		Conditions	V_{EE}	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
						Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage				2.0V		1.5	1.5	1.5	V
					4.5V		3.15	3.15	3.15	V
					6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage				2.0V		0.3	0.3	0.3	V
					4.5V		0.9	0.9	0.9	V
					6.0V		1.2	1.2	1.2	V
R_{ON}	Maximum "ON" Resistance (See Note 5)		V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} to V_{EE} (Figure 1)	GND	4.5V	40	200	250	300	Ω
				−4.5V	4.5V	30	100	125	150	Ω
				−6.0V	6.0V	20	90	112	135	Ω
			V_{CTL}=V_{IH}, I_S=1.0 mA V_{IS}=V_{CC} or V_{EE} (Figure 1)	GND	2.0V	100	230	290	350	Ω
				GND	4.5V	40	110	138	165	Ω
				−4.5V	4.5V	20	90	110	135	Ω
				−6.0V	6.0V	15	80	100	120	Ω
R_{ON}	Maximum "ON" Resistance Matching		V_{CTL}=V_{IH} V_{IS}=V_{CC} to GND	GND	4.5V	10	15	20	20	Ω
				−4.5V	4.5V	5	10	15	15	Ω
				−6.0V	6.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current		V_{IN}=V_{CC} or GND V_{CC}=2−6V				±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current (Switch Input)		V_{OS}=V_{CC} or GND V_{IS}=GND or V_{CC} V_{INH}=V_{IH} (Figure 2)	GND	6.0V		±60	±600	±600	nA
				−6.0V	6.0V		±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	HC4051	V_{OS}=V_{CC} or GND V_{INH}=V_{IL} (Figure 3)	GND	6.0V					μA
				−6.0V	6.0V					μA
		HC4052	V_{OS}=V_{CC} or GND V_{INH}=V_{IL} (Figure 3)	GND	6.0V					μA
				−6.0V	6.0V					μA
		HC4053	V_{OS}=V_{CC} or GND V_{INH}=V_{IL} (Figure 3)	GND	6.0V					μA
				−6.0V	6.0V					μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occur for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}−V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

DC Electrical Characteristics (Note 4) (Continued)

Symbol	Parameter		Conditions	V_{EE}	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
						Typ	Guaranteed Limits		
I_{IZ}	Maximum Switch "OFF" Leakage Current (Common Pin)	HC4051	$V_{OS} = V_{CC}$ or GND $V_{IS} = GND$ or V_{CC} $V_{INH} = V_{IH}$	GND −6.0V	6.0V 6.0V				μA μA
		HC4052	$V_{OS} = V_{CC}$ or GND $V_{IS} = GND$ or V_{CC} $V_{INH} = V_{IH}$	GND −6.0V	6.0V 6.0V				μA μA
		HC4053	$V_{OS} = V_{CC}$ or GND $V_{IS} = GND$ or V_{CC} $V_{INH} = V_{IH}$	GND −6.0V	6.0V 6.0V				μA μA
I_{CC}	Maximum Quiescent Supply Current		$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$ μA	GND −6.0V	6.0V 6.0V		8 16	80 160	160 320	μA μA

AC Electrical Characteristics $V_{CC} = 2.0V-6.0V$ $V_{EE} = 0V-6V$, $C_L = 50$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	$T_A = 25°C$	74HC $T_A = -40$ to $85°C$	54HC $T_A = -55$ to $125°C$	Units
					Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	25 5 4 3	50 10 8 7	62 13 12 11	75 15 14 13	ns ns ns ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	$R_L = 1$ kΩ	GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	92 18 16 15				ns ns ns ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay		GND GND −4.5V −6.0V	2.0V 4.5V 4.5V 6.0V	65 28 18 16				ns ns ns
f_{MAX}	Minimum Switch Frequency Response 20 log $(V_I/V_O) = 3$ dB		GND −4.5V	4.5V 4.5V	30 35				MHz MHz
	Cross Talk Control to Switch	(Figure 7)	−4.5V	4.5V	180				mV_{P-P}
	Cross Talk Between any Two Switches (Frequency at −50 dB)	(Figure 8)	−4.5V	4.5V					MHz
	Feed Through, Switch Input to Output	F = 5 MHz F = 10 MHz							dB dB
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input 4051 Common 4052 Common 4053 Common			15 90 45 30				pF
C_{IN}	Maximum Feedthrough Capacitance				5				pF

Truth Tables

'4051

Input				"ON" Channel
Inh	C	B	A	
H	X	X	X	None
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7

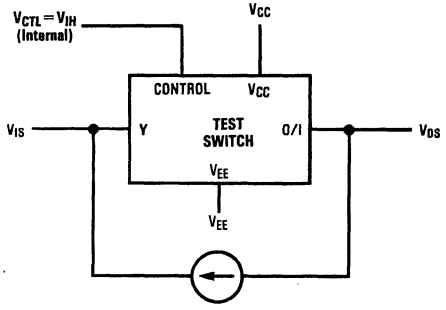
'4052

Inputs			"ON" Channels	
Inh	B	A	X	Y
H	X	X	None	None
L	L	L	0X	0Y
L	L	H	1X	1Y
L	H	L	2X	2Y
L	H	H	3X	3Y

'4053

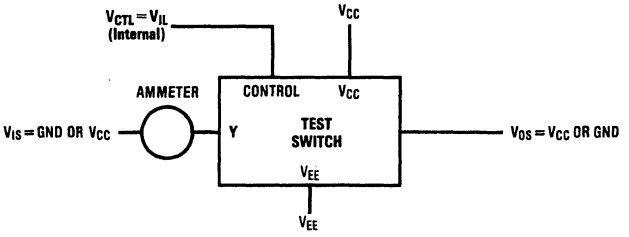
Input				"ON" Channels		
Inh	C	B	A	C	b	a
H	X	X	X	None	None	None
L	L	L	L	CX	BX	AX
L	L	L	H	CX	BX	AY
L	L	H	L	CX	BY	AY
L	L	H	H	CX	BY	AY
L	H	L	L	CY	BX	AY
L	H	L	H	CY	BX	AY
L	H	H	L	CY	BY	AY
L	H	H	H	CY	BY	AY

AC Test Circuits and Switching Time Waveforms



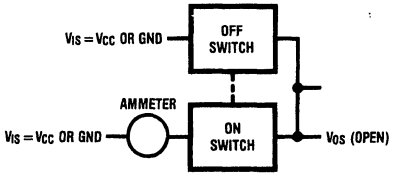
TL/F/5353–4

FIGURE 1. "ON" Resistance



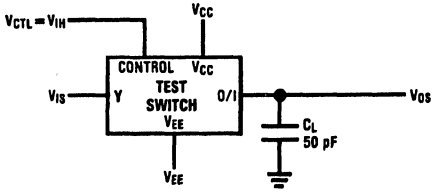
TL/F/5353–5

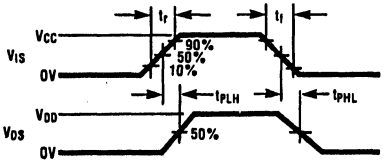
FIGURE 2. "OFF" Channel Leakage Current



TL/F/5353–6

FIGURE 3. "ON" Channel Leakage Current

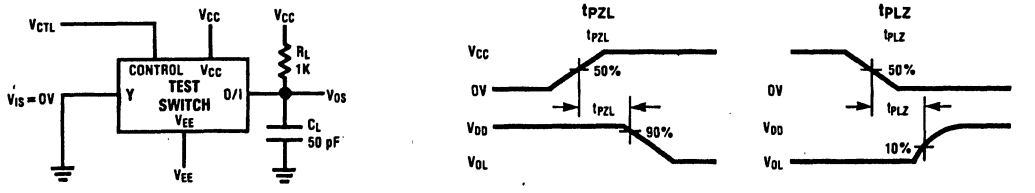




TL/F/5353–7

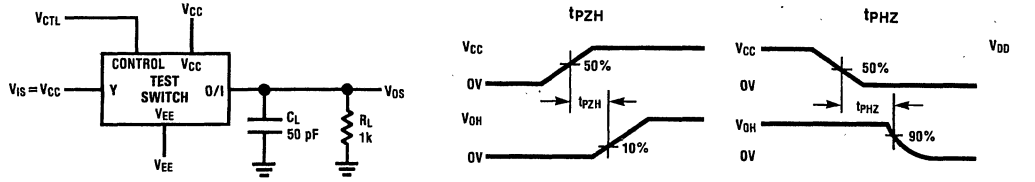
FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



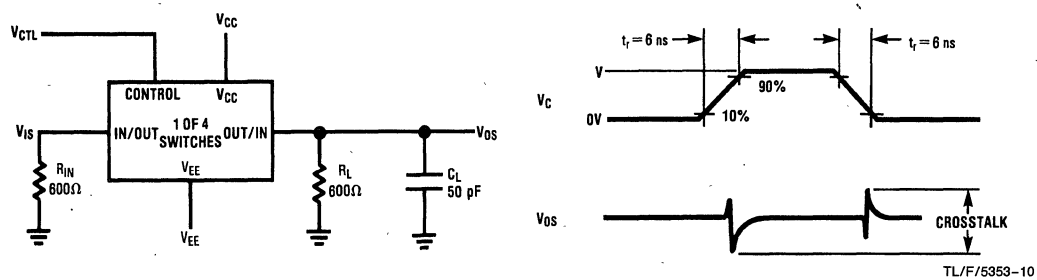
TL/F/5353–8

FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output



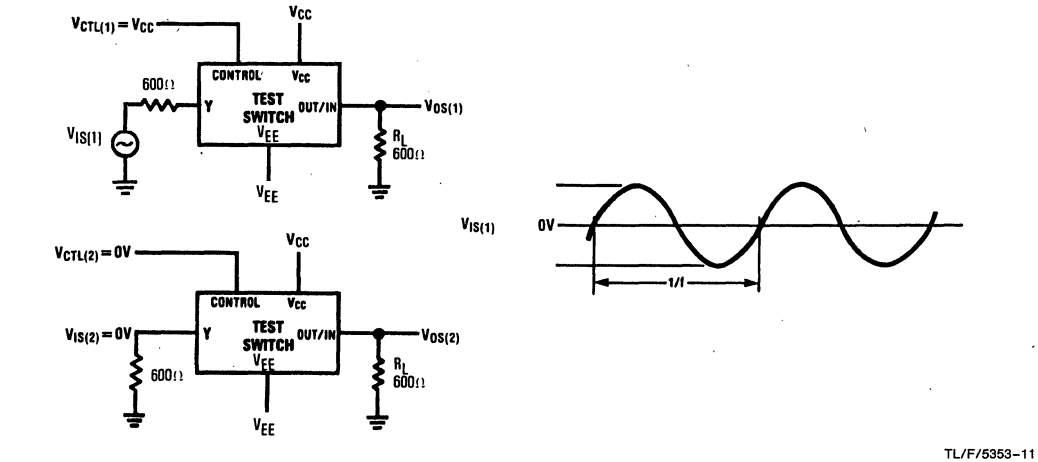
TL/F/5353–9

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



TL/F/5353–10

FIGURE 7. Crosstalk: Control Input to Signal Output

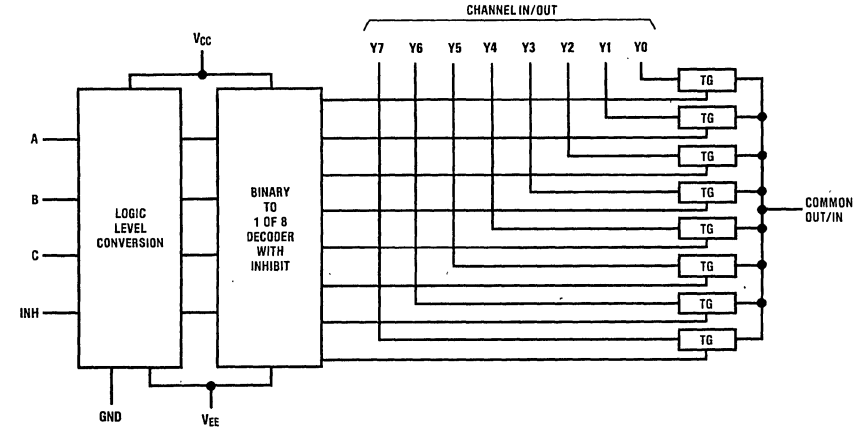


TL/F/5353–11

FIGURE 8. Crosstalk Between Any Two Switches

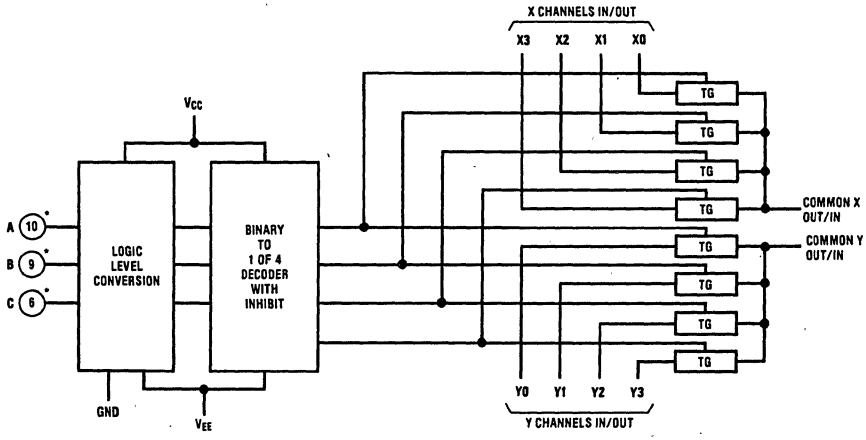
Logic Diagrams

MM54HC4051/MM74HC4051



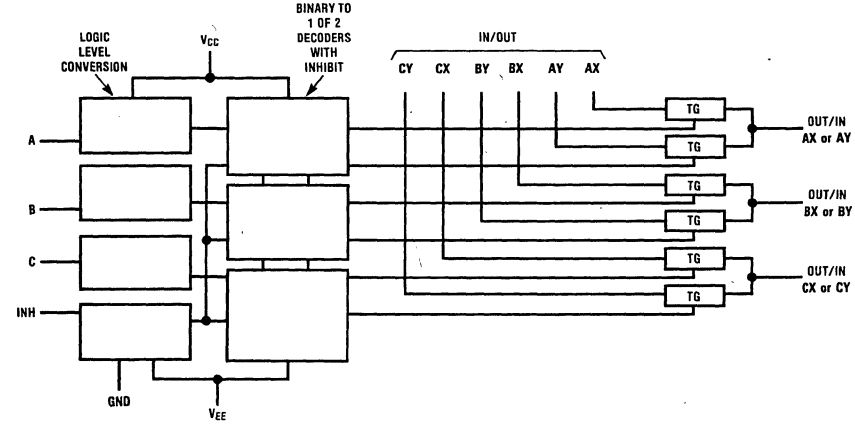
TL/F/5353–19

MM54HC4052/MM74HC4052



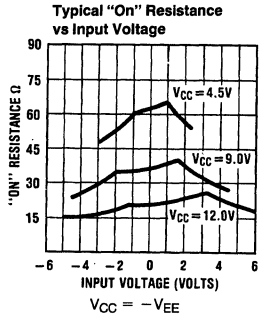
TL/F/5353–20

MM54HC4053/MM74HC4053



TL/F/5353–21

Typical Performance Characteristics



$V_{CC} = -V_{EE}$

TL/F/5353–18

National Semiconductor

microCMOS

MM54HC4060/MM74HC4060
14 Stage Binary Counter

General Description

The MM54HC4060/MM74HC4060 is a high speed binary ripple carry counter. These counters are implemented utilizing microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve speed performance similar to LS-TTL logic while retaining the low power and high noise immunity of CMOS.

The 'HC4060 is a 14-stage counter, which device increments on the falling edge (negative transition) of the input clock, and all their outputs are reset to a low level by applying a logical high on their reset input. The 'HC4060 also has two additional inputs to enable easy connection of either an RC or crystal oscillator.

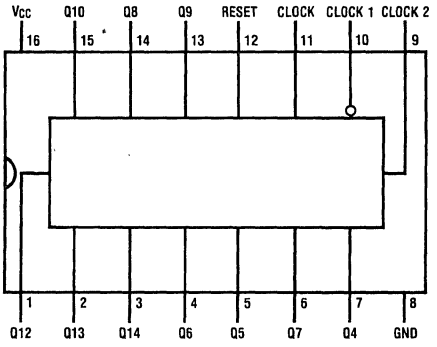
This device is pin equivalent to the CD4060. All inputs are protected from damage due to static discharge by protection diodes to V_{CC} and ground.

Features

- Typical propagation delay: 16 ns
- Wide operating voltage range: 2–6V
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Output drive capability: 10 LS-TTL loads

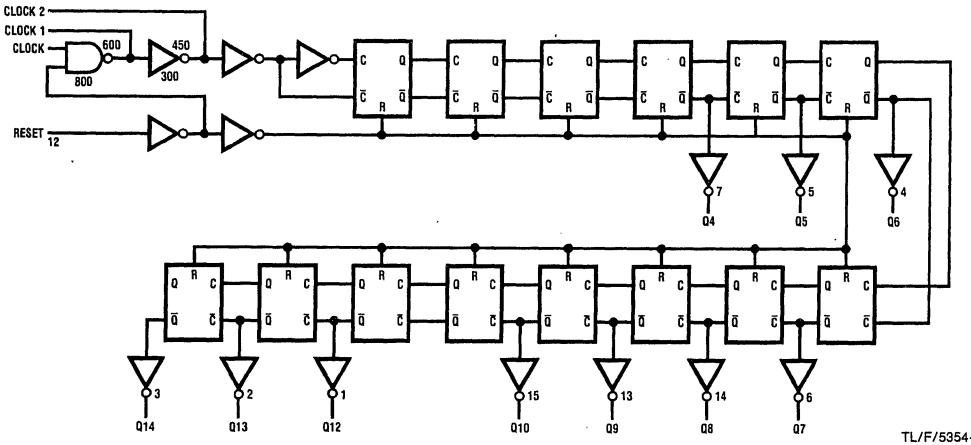
Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5354–1

Top View
Order Number MM54HC4060J or MM74HC4060J, N
See NS Package J16A or N16E



TL/F/5354–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{CD})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC Vcc or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	Except Pins 11 & 12	V_{IN}=V_{IH} orV_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
	Pins 11 & 12	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\|$=0.4 mA			3.98	3.84	3.7	V
		$\|I_{OUT}\|$=0.52 mA			5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	Except Pins 11 & 12	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
	Pins 11 & 12	V_{IN}=V_{IH} or V_{IL}						
		$\|I_{OUT}\|$=0.4 mA			0.26	0.33	0.4	V
		$\|I_{OUT}\|$=0.52 mA			0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND						
		I_{OUT}=0 μA	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating: plastic "N" package: −12 mW/°C from 65°C to 85°C ceramic "J" package: −12 mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency			30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Q_4	(Note 5)	40	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay to any Q		16	40	ns
t_{REM}	Minimum Reset Removal Time		10	20	ns
t_W	Minimum Pulse Width		10	16	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

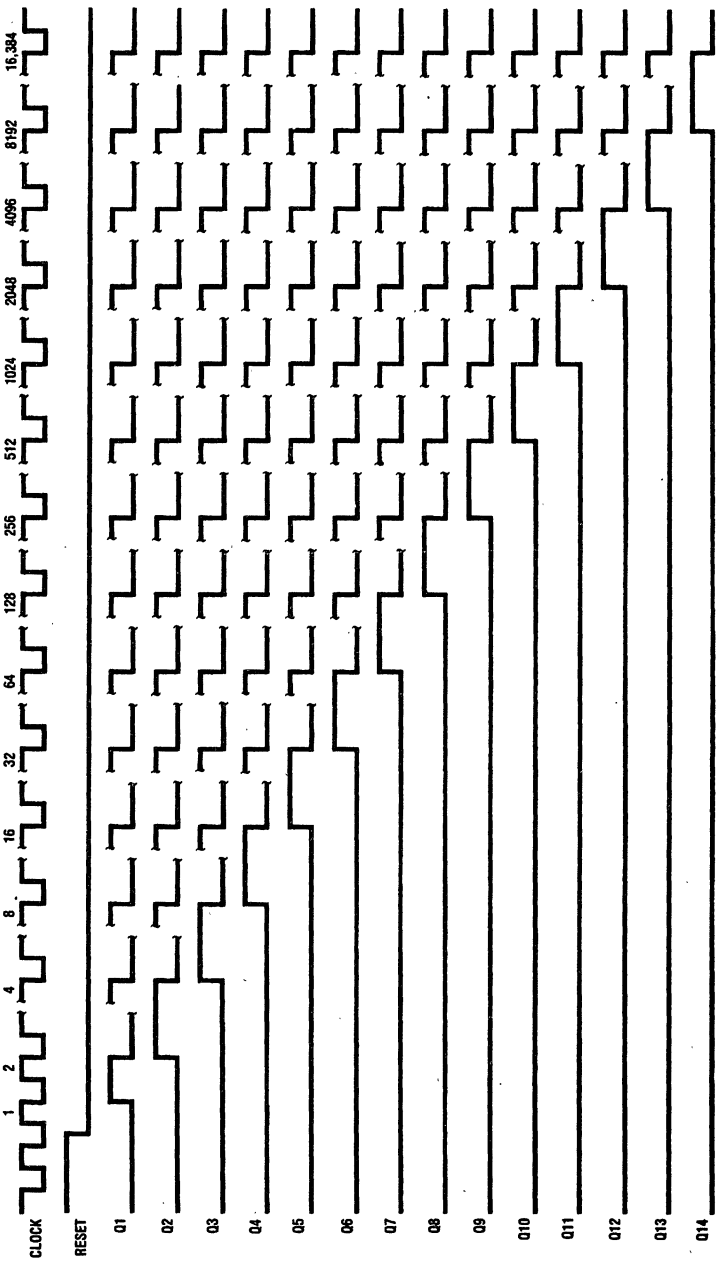
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	T_A74HC $T_A=-40$ to $85°C$	T_A54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency		2.0V		6	5	4	MHz
			4.5V0		30	24	20	MHz
			6.0V		35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q_4		2.0V	120	300	375	450	ns
			4.5V	42	60	75	90	ns
			6.0V	35	47	59	62	ns
t_{PHL}	Maximum Propagation Delay Reset to any Q		2.0V	72	240	302	358	ns
			4.5V	24	48	60	72	ns
			6.0V	20	41	51	61	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Between Stages Q_n to Q_{n+1}		2.0V		125	156	188	ns
			4.5V		25	31	38	ns
			6.0V		21	26	31	ns
t_{REM}	Mimimum Reset Removal Time		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_W	Mimimum Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 6)	(per package)		55				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: Typical Propagation delay time to any output can be calculated using: t_P 17+12(N−1) ns; where N is the number of the output, Q_W, at $V_{CC}=5V$.

Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

3

Timing Diagram



TL/F/5354–3

National Semiconductor

microCMOS

MM54HC4066/MM74HC4066 Quad Analog Switch

General Description

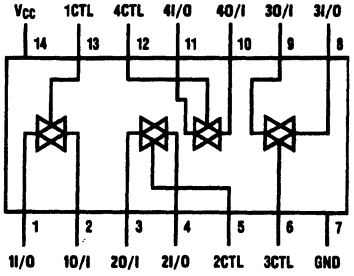
These devices are digitally controlled analog switches utilizing microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and visa-versa. Also the '4066 switches contain linearization circuitry which lowers the "on" resistance and increases switch linearity. The '4066 devices allow control of up to 12V (peak) analog signals with digital control signals of the same range. Each switch has its own control input which disables each switch when low. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 15 ns
- Wide analog input voltage range: 0–12V
- Low "on" resistance: 30 typ. ('4066)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls

Connection Diagram

Dual-In-Line Package



TL/F/5355–1

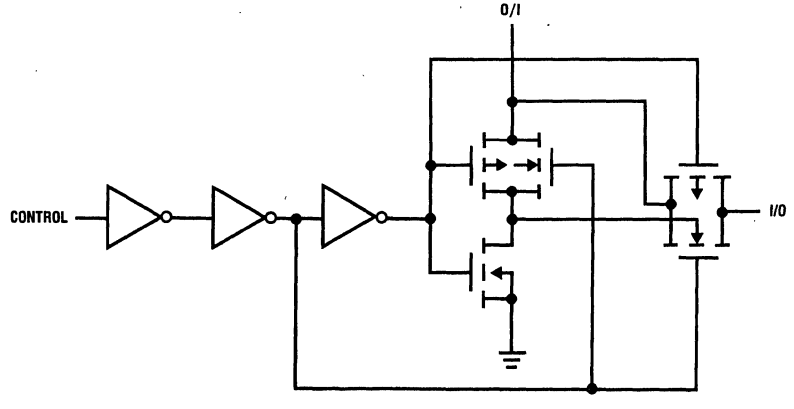
Top View

Order Number MM54HC4066J or MM74HC4066J, N
See NS Package J14A or N14A

Truth Table

Input	Switch
CTL	I/O–O/I
L	"OFF"
H	"ON"

Schematic Diagram



TL/F/5355–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +15V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE} −0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	12	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 9.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			9.0V		6.3	5.3	6.3	V
			12.0V		8.4	8.4	8.4	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			9.0V		1.8	1.8	1.8	V
			12.0V		2.4	2.4	2.4	V
R_{ON}	Maximum "ON" Resistance (See Note 5)	V_{CTL} = V_{IH}, I_S = 1.0 mA V_{IS} = V_{CC} to GND (Figure 1)	4.5V	100	170	200	220	Ω
			9.0V	50	85	105	110	Ω
			12.0	30	70	85	90	Ω
		V_{CTL} = V_{IH}, I_S = 1.0 mA V_{IS} = V_{CC} or GND (Figure 1)	2.0V	120	180	215	240	Ω
			4.5V	50	80	100	120	Ω
			9.0V	35	60	75	80	Ω
			12.0V	20	40	60	70	Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL} = V_{IH} V_{IS} = V_{CC} to GND	4.5V	10	15	20	20	Ω
			9.0V	5	10	15	15	Ω
			12.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	V_{IN} = V_{CC} or GND V_{CC} = 2–6V			±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS} = V_{CC} or GND V_{IS} = GND or V_{CC} V_{CTL} = V_{IL} (Figure 2)	5.5V	10	±60	±600	±600	nA
			9.0V	15	±80	±800	±800	nA
			12.0V	20	±100	±1000	±1000	nA
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS} = V_{CC} or GND V_{CTL} = V_{IH} (Figure 3)	5.5V	10	±40	±150	±150	nA
			9.0V	15	±50	±200	±200	nA
			12.0V	20	±60	±300	±300	nA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	5.5V		2.0	20	40	μA
			9.0V		8.0	80	160	μA
			12.0V		16.0	160	320	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistance (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

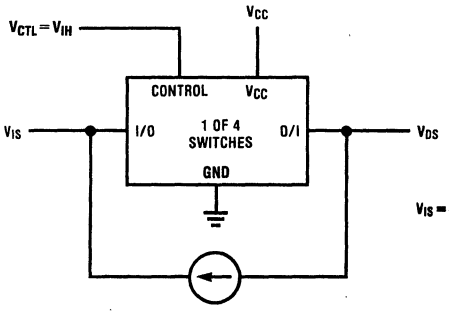
Note 5: At supply voltages (V_{CC}–V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics V_{CC}=2.0V–6.0V V_{EE}=0V–6V, C_L=50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		2.0V	25	50	30	75	ns
			4.5V	5	10	13	15	ns
			9.0V	4	8	10	12	ns
			12.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay	R_L=1 kΩ	2.0V	30	100	125	150	ns
			4.5V	12	20	25	30	ns
			9.0V	6	12	15	18	ns
			12.0V	5	10	13	15	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay	R_L=1 kΩ	2.0V	60	168	210	252	ns
			4.5V	25	36	45	54	ns
			9.0V	20	32	40	48	ns
			12.0V	15	30	38	45	
f_{MAX}	Minimum Switch Frequency Response 20 log(V_I/V_O)=3 dB		4.5V	−30				MHz
			9.0V	−35				MHz
	Cross Talk Control to Switch	(Figure 7)	4.5V	180				mV_{P-P}
	Cross Talk Between any Two Switches (Frequency at −50 dB)	(Figure 8)	4.5V					MHz
	Feedthrough Switch Input to Switch Output	F=5 MHz	4.5V					dB
		F=10 MHz	4.5V					dB
C_{IN}	Maximum Control Input Capacitance			5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance			15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL}=GND		5				pF
C_{PD}	Power Dissipation Capacitance			15				pF

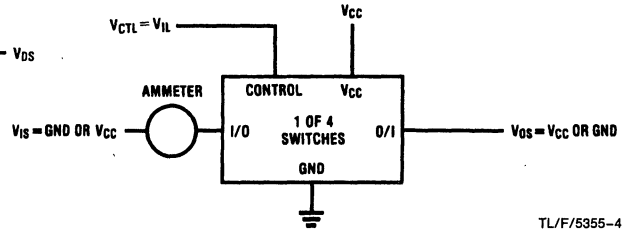
3

AC Test Circuits and Switching Time Waveforms



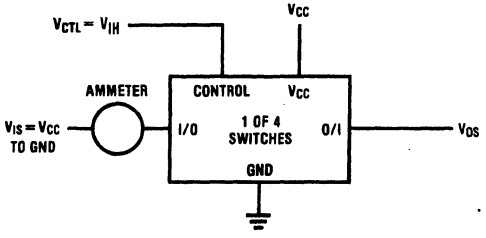
TL/F/5355-3

FIGURE 1. "ON" Resistance



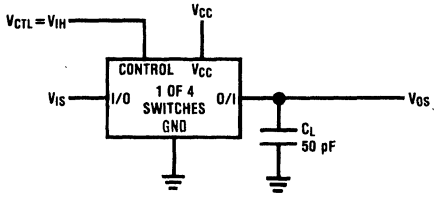
TL/F/5355-4

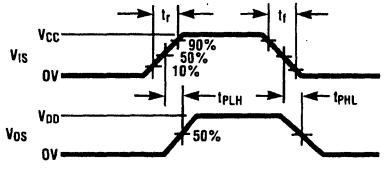
FIGURE 2. "OFF" Channel Leakage Current



TL/F/5355-5

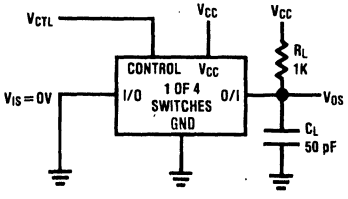
FIGURE 3. "ON" Channel Leakage Current

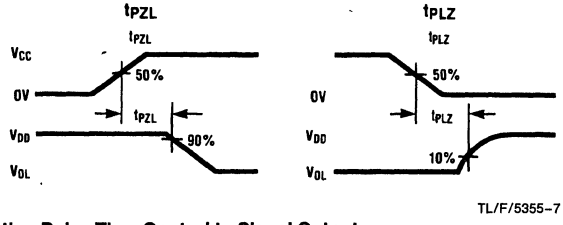




TL/F/5355-6

FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

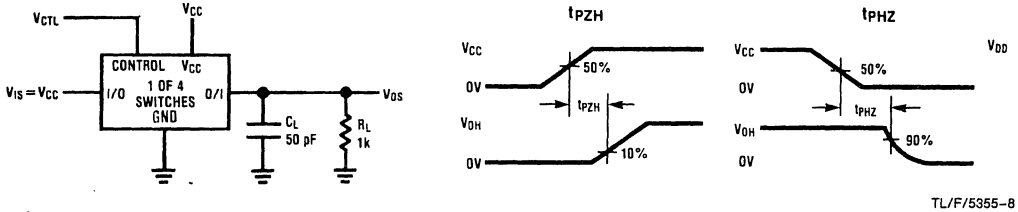




TL/F/5355-7

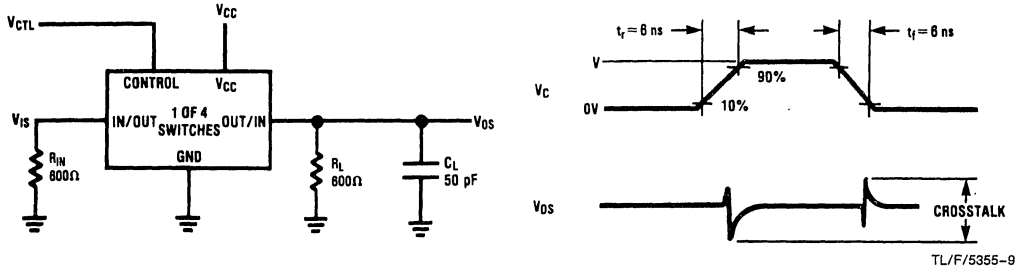
FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



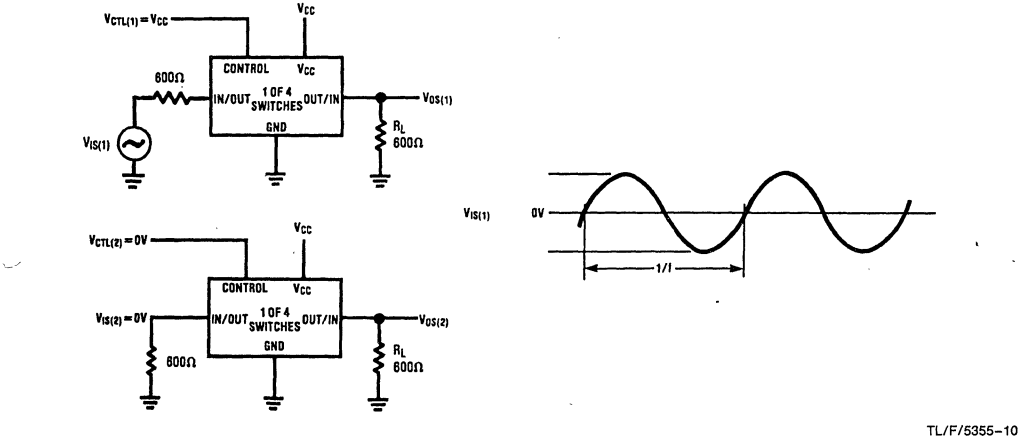
TL/F/5355–8

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



TL/F/5355–9

FIGURE 7. Crosstalk: Control Input to Signal Output

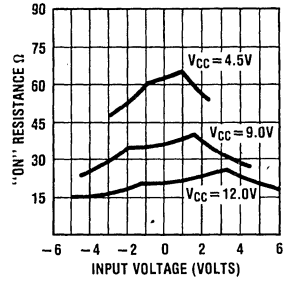


TL/F/5355–10

FIGURE 8. Crosstalk Between Any Two Switches

Typical Performance Characteristics

Typical "On" Resistance vs. Input Voltage ('4066)



TL/F/5355–18

National Semiconductor

microCMOS

MM54HC4075/MM74HC4075 Triple 3-Input OR Gate

General Description

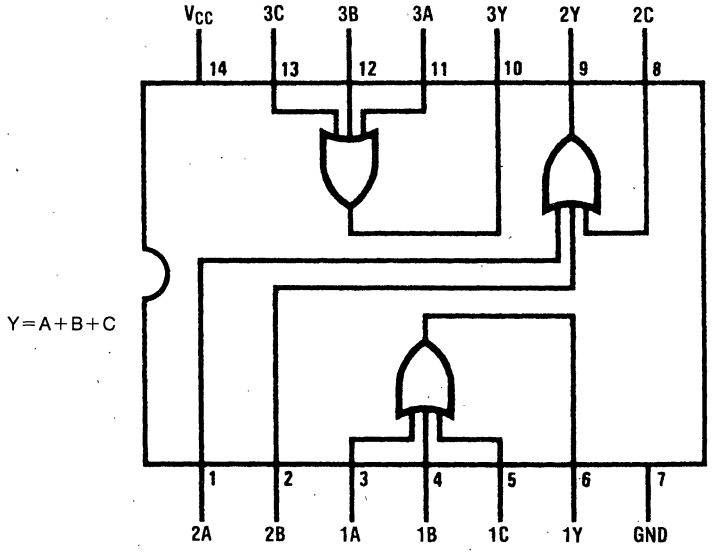
These OR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. All gates have buffered outputs, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC/74HC logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. The 54HC4075/74HC4075 is functionally equivalent and pin-out compatible with the CD4075B and MC14075B metal gate CMOS devices. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 11 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5155–1

Top View

Order Number MM54HC4075J or MM74HC4075J, N
See NS Package J14A or N14A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN},V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	V
			4.5V		3.15	3.15	V
			6.0V		4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	V
			4.5V		0.9	0.9	V
			6.0V		1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	2.0	1.9	1.9	V
			4.5V	4.5	4.4	4.4	V
			6.0V	6.0	5.9	5.9	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	4.2	3.98	3.84	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	5.7	5.48	5.34	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	2.0V	0	0.1	0.1	V
			4.5V	0	0.1	0.1	V
			6.0V	0	0.1	0.1	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$|I_{OUT}|\leq$5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay		11	20	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay		2.0V	40	115	145	171	ns
			4.5V	12	23	29	34	ns
			6.0V	10	20	25	29	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate)		30				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HC4078/MM74HC4078 8-Input NOR/OR Gate

General Description

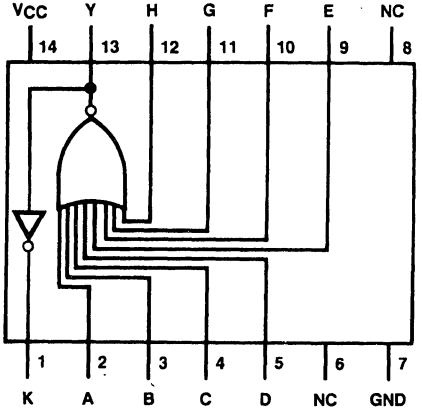
These NOR gates utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, to achieve operating speeds similar to LS-TTL gates with the low power consumption of standard CMOS integrated circuits. Both outputs are buffered, providing high noise immunity and the ability to drive 10 LS-TTL loads. The 54HC4078/74HC4078 is functionally equivalent and pin-out compatible with the CD4078B. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 15 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

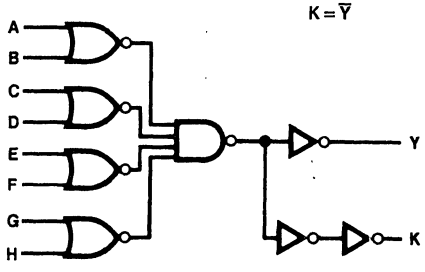


TL/F/5135–1

Top View

Order Number MM54HC4078J or MM74HC4078J, N
See NS Package J14A or N14A

$$Y = \overline{A + B + C + D + E + F + G + H}$$
$$K = \overline{Y}$$



TL/F/5135–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20$ μA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20$ μA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		2.0	20	40	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics MM54HC4078/74HC4078

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Y to Output		14	22	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, K to Output		16	24	ns

AC Electrical Characteristics $V_{CC}=2.0V$ to $6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$		74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Y to Output		2.0V	47	130	160	195	ns
			4.5V	17	26	33	39	ns
			6.0V	14	22	28	33	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, K to Output		2.0V	50	140	175	210	ns
			4.5V	20	28	35	42	ns
			6.0V	17	24	30	36	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time		2.0V	30	75	95	110	ns
			4.5V	10	15	19	22	ns
			6.0V	9	13	16	19	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per package)		100				pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4316/MM74HC4316
Quad Analog Switch with Level Translator

General Description

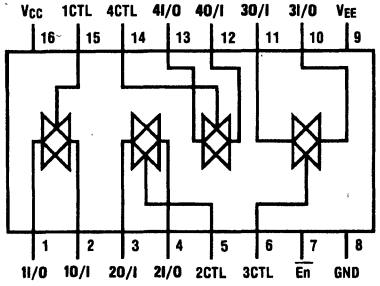
These devices are digitally controlled analog switches implemented in microCMOS Technology, 3.5 micron silicon gate P-well CMOS. These switches have low "on" resistance and low "off" leakages. They are bidirectional switches, thus any analog input may be used as an output and vice-versa. Three supply pins are provided on the '4316 to implement a level translator which enables this circuit to operate with 0–6V logic levels and up to ±6V analog switch levels. The '4316 also has a common enable input in addition to each switch's control which when low will disable all switches to their off state. All analog inputs and outputs and digital inputs are protected from electrostatic damage by diodes to V_{CC} and ground.

Features

- Typical switch enable time: 20 ns
- Wide analog input voltage range: ±6V
- Low "on" resistance: 50 typ. ($V_{CC}-V_{EE}=4.5V$)
  30 typ. ($V_{CC}-V_{EE}=9V$)
- Low quiescent current: 80 μA maximum (74HC)
- Matched switch characteristics
- Individual switch controls plus a common enable

Connection and Logic Diagrams

Dual-In-Line Package



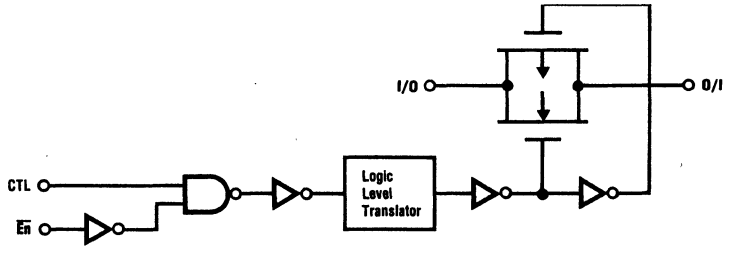
TL/F/5369–1

Top View

Order Number MM54HC4316J or MM74HC4316J,N
See NS Package J16A or N16E

Truth Table

Inputs		Switch
$\overline{En}$	CTL	I/O–O/I
H	X	"OFF"
L	L	"OFF"
L	H	"ON"



TL/F/5369–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.5V
Supply Voltage (V_{EE})	+0.5 to −7.5V
DC Control Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Switch I/O Voltage (V_{IO})	V_{EE}−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
Supply Voltage (V_{EE})	0	−6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC}=2.0V		1000	ns
V_{CC}=4.5V		500	ns
V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0V		1.5	1.5	1.5	V
				4.5V		3.15	3.15	3.15	V
				6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage			2.0V		0.3	0.3	0.3	V
				4.5V		0.9	0.9	0.9	V
				6.0V		1.2	1.2	1.2	V
R_{ON}	Minimum "ON" Resistance (See Note 5)	V_{CTL}=V_{IH}, I_S=1.0 mA	GND	4.5V	100	170	200	220	Ω
		V_{IS}=V_{CC} to V_{EE}	−4.5V	4.5V	40	85	105	110	Ω
		(Figure 1)	−6.0V	6.0V	30	70	85	90	Ω
			GND	2.0V	100	180	215	240	Ω
		V_{CTL}=V_{IH}, I_S=1.0 mA	GND	4.5V	40	80	100	120	Ω
		V_{IS}=V_{CC} or V_{EE}	−4.5V	4.5V	50	60	75	80	Ω
		(Figure 1)	−6.0V	6.0V	20	40	60	70	Ω
R_{ON}	Maximum "ON" Resistance Matching	V_{CTL}=V_{IH}	GND	4.5V	10	15	20	20	Ω
		V_{IS}=V_{CC} to GND	−4.5V	4.5V	5	10	15	15	Ω
			−6.0V	6.0V	5	10	15	15	Ω
I_{IN}	Maximum Control Input Current	V_{IN}=V_{CC} or GND			6.0V	±0.1	±1.0	±1.0	μA
I_{IZ}	Maximum Switch "OFF" Leakage Current	V_{OS}=V_{CC} or GND	GND	5.5V		±60	±600	±600	nA
		V_{IS}=GND or V_{CC}	−6.0V	6.0V		±100	±1000	±1000	nA
		V_{CTL}=V_{IL} (Fig 2)							
I_{IZ}	Maximum Switch "ON" Leakage Current	V_{OS}=V_{CC} or GND	GND	5.5V		±40	±150	±150	nA
		V_{CTL}=V_{IH}	−6.0V	6.0V		±60	±300	±300	nA
		(Figure 3)							
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND	GND	6.0V		2.0	20	40	μA
		I_{OUT}=0 μA	−6.0V	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case on resistances (R_{ON}) occurs for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current occurs for CMOS at the higher voltage and so the 5.5V values should be used.

Note 5: At supply voltages (V_{CC}−V_{EE}) approaching 2V the analog switch on resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital only when using these supply voltages.

AC Electrical Characteristics V_{CC}=2.0V–6.0V, V_{EE}=0V–6V, C_L=50 pF (unless otherwise specified)

Symbol	Parameter	Conditions	V_{EE}	V_{CC}	T_A=25°C		74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
					Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Switch In to Out		GND	2.0V	25	50	63	75	ns
			GND	4.5V	5	10	13	15	ns
			−4.5V	4.5V	4	8	12	14	ns
			−6.0V	6.0V	3	7	11	13	ns
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Control)	R_L=1 kΩ	GND	2.0V		65	206	250	ns
			GND	4.5V		35	43	53	ns
			−4.5V	4.5V		32	39	48	ns
			−6.0V	6.0V		30	37	45	ns
t_{PHZ}, t_{PLZ}	Maximum Switch Turn "OFF" Delay (Control)	R_L=1 kΩ	GND	2.0V	45	250	312	375	ns
			GND	4.5V	15	50	63	75	ns
			−4.5V	4.5V	10	44	55	66	ns
			−6.0V	6.0V	8	44	55	66	
t_{PZL}, t_{PZH}	Maximum Switch Turn "ON" Delay (Enable)		GND	2.0V	35	205	256	308	ns
			GND	4.5V	20	41	52	62	ns
			−4.5V	4.5V	19	38	48	57	ns
			−6.0V	6.0V	18	36	45	54	ns
t_{PLZ}, t_{PHZ}	Maximum Switch Turn "OFF" Delay (Enable)		GND	2.0V	48	265	330	400	ns
			GND	4.5V	18	53	67	79	ns
			−4.5V	4.5V	13	47	59	70	ns
			−6.0V	6.0V	11	47	59	70	ns
f_{MAX}	Minimum Switch Frequency Response 20 log(V_I/V_O)=3 dB		GND	4.5V	30				MHz
			−4.5V	4.5V	35				MHz
	Cross Talk Control to Switch	(Figure 7)	−4.5V	4.5V	100				mV_{P-P}
	Cross Talk Between any Two Switches (Frequency at −50 dB)	(Figure 8)	−4.5V	4.5V					MHz
	Feedthrough, Switch Input to Switch Output		GND	4.5V					dB
			GND	4.5V					dB
C_{IN}	Maximum Control Input Capacitance				5	10	10	10	pF
C_{IN}	Maximum Switch Input Capacitance	Input			15				pF
C_{IN}	Maximum Feedthrough Capacitance	V_{CTL}=GND			5				pF
C_{PD}	Power Dissipation Capacitance				15				pF

AC Test Circuits and Switching Time Waveforms

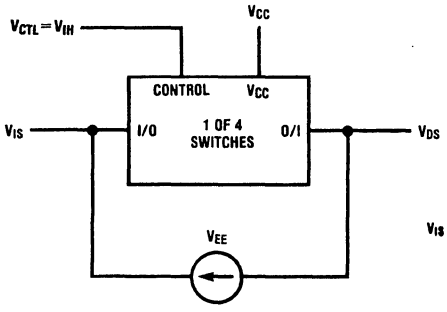


FIGURE 1. "ON" Resistance

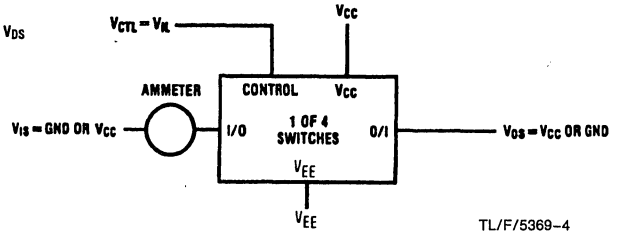


FIGURE 2. "OFF" Channel Leakage Current

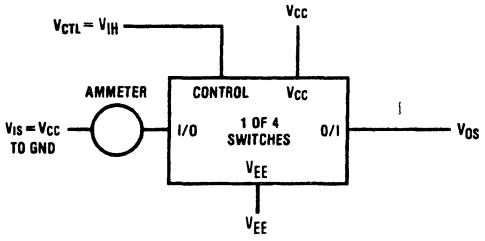


FIGURE 3. "ON" Channel Leakage Current

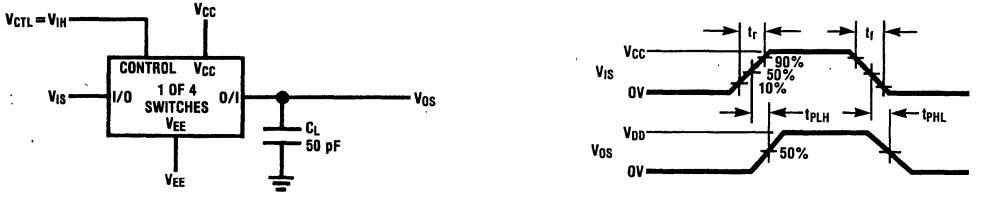


FIGURE 4. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

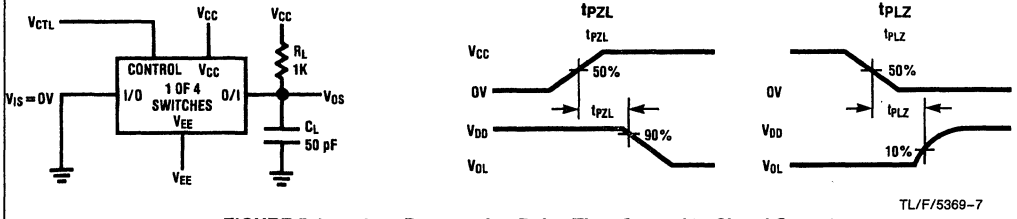
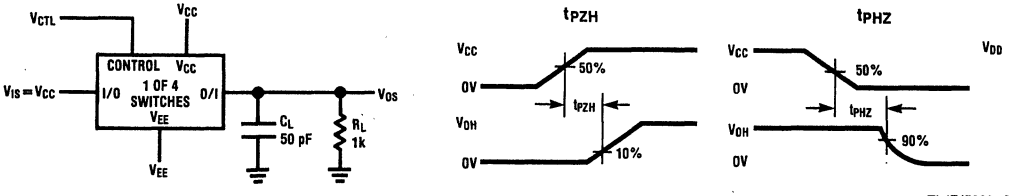


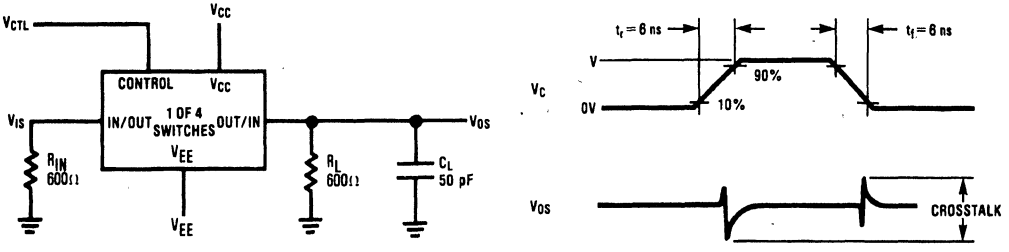
FIGURE 5. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



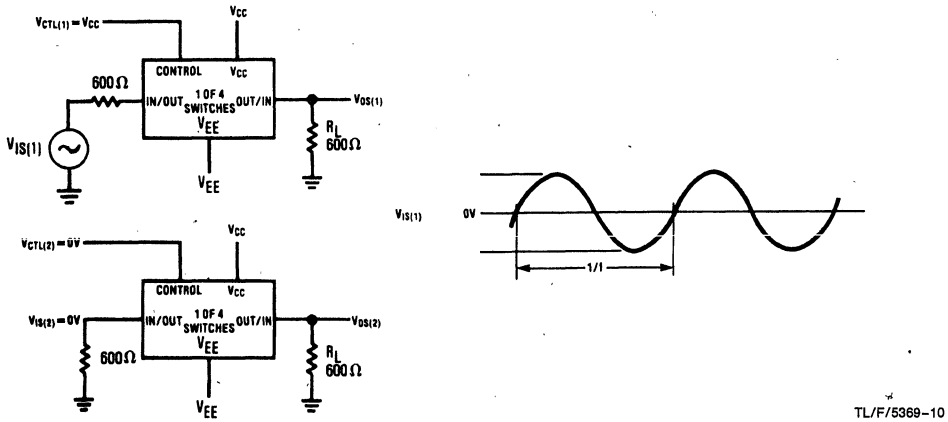
TL/F/5369–8

FIGURE 6. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output



TL/F/5369–9

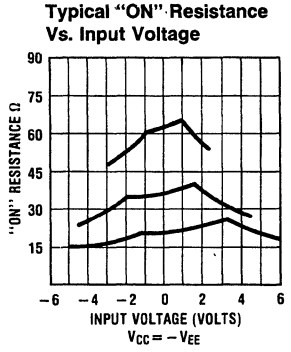
FIGURE 7. Crosstalk: Control Input to Signal Output



TL/F/5369–10

FIGURE 8: Crosstalk Between Any Two Switches

Typical Performance Characteristics



TL/F/5369–17

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4511/MM74HC4511
BCD-to-7 Segment Latch/Decoder/Driver

General Description

This high speed latch/decoder/driver utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS. It has the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

The 54HC/74HC logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

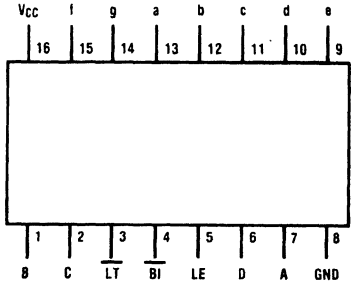
Features

- Latch storage of input data
- Blanking input
- Lamp test input
- Low power consumption characteristics of CMOS devices
- Wide operating voltage range: 2 to 6 volts
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum over full temperature range (74 Series)

3

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5373–1

Order Number MM54HC4511J or MM74HC4511J, N
See NS Package J16A or N16E

Truth Table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
x	x	L	x	x	x	x	H	H	H	H	H	H	H	8
x	L	H	x	x	x	x	L	L	L	L	L	L	L	
L	H	H	L	L	L	L	H	H	H	H	H	H	L	0
L	H	H	L	L	L	H	L	H	H	L	L	L	L	1
L	H	H	L	L	H	L	H	H	L	H	H	L	H	2
L	H	H	L	L	H	H	H	H	H	H	L	L	H	3
L	H	H	L	H	L	L	L	H	H	L	L	H	H	4
L	H	H	L	H	L	H	H	L	H	H	L	H	H	5
L	H	H	L	H	H	L	L	L	H	H	H	H	H	6
L	H	H	L	H	H	H	H	H	H	L	L	L	L	7
L	H	H	H	L	L	L	H	H	H	H	H	H	H	8
L	H	H	H	L	L	H	H	H	H	L	L	H	H	9
L	H	H	H	L	H	L	L	L	L	L	L	L	L	
L	H	H	H	L	H	H	L	L	L	L	L	L	L	
L	H	H	H	H	L	L	L	L	L	L	L	L	L	
L	H	H	H	H	L	H	L	L	L	L	L	L	L	
L	H	H	H	H	H	L	L	L	L	L	L	L	L	
L	H	H	H	H	H	H	L	L	L	L	L	L	L	
H	H	H	x	x	x	x				*				*

x = Don't care

* = Depends upon the BCD code applied during the 0 to 1 transition of LE.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times				
(t_r, t_f)	V_{CC} = 2.0V		1000	ns
	V_{CC} = 4.5V		500	ns
	V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 7.5$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 9.75$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Inputs A thru D to any Output		60	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{BI}$ to any Output		60	120	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{LT}$ to any Output		60	120	ns
t_S	Minimum Setup Time Inputs A thru D to LE		10	20	ns
t_H	Minimum Hold Time Inputs A thru D to LE		−3	0	ns
t_W	Minimum Pulse Width for LE			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Inputs A thru D to any Output	LE = 0V $\overline{LT}=V_{CC}$ $\overline{BI}=V_{CC}$	2.0V 4.5V 6.0V	300 60 51	600 120 102	756 151 129	894 179 152	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{BI}$ to any Output	$\overline{LT}=V_{CC}$	2.0V 4.5V 6.0V	300 60 51	600 120 102	756 151 129	894 179 152	ns ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{LT}$ to any Output	$\overline{BI}=0V$	2.0V 4.5V 6.0V	300 60 51	600 120 102	756 151 129	894 179 152	ns ns ns
t_S	Minimum Setup Time Inputs A thru D to LE		2.0V 4.5V 6.0V		100 20 17	126 25 21	149 30 25	ns ns ns
t_H	Minimum Hold Time Inputs A thru D to LE		2.0V 4.5V 6.0V		0 0 0	0 0 0	0 0 0	ns ns ns
t_W	Minimum Pulse Width for LE		2.0V 4.5V 6.0V		80 16 14	100 20 17	120 24 20	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time		2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

3

INPUTS

A, B, C, D (Pins 7, 1, 2, 6)—BCD data inputs. A (pin 7) is the least-significant data bit and D (pin 6) is the most significant bit. Hexadecimal data A–F at these inputs will cause the outputs to assume a logic low, offering an alternate method of blanking the display.

OUTPUTS

a–g—Decoded, buffered outputs. These outputs, unlike the 4511, have CMOS drivers, which will produce typical CMOS output voltage levels.

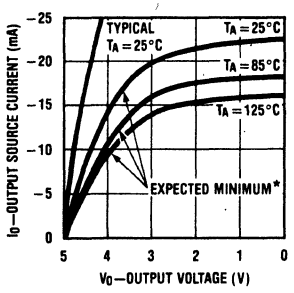
CONTROLS

$\overline{BI}$ (Pin 4)—Active-low display blanking input. A logic low on this input will cause all outputs to be held at a logic low, thereby blanking the display. LT is the only input that will override the BI input.

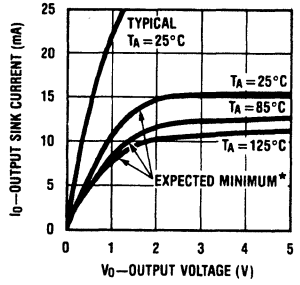
$\overline{LT}$ (Pin 3)—Active-low lamp test. A low logic level on this input causes all outputs to assume a logic high. This input allows the user to test all segments of a display, with a single control input. This input is independent of all other inputs.

LE (Pin 5)—Latch enable input. This input controls the 4-bit transparent latch. A logic high on this input latches the data present at the A, B, C and D inputs; a logic low allows the data to be transmitted through the latch to the decoder.

Output Characteristics (V_{CC} = 5V)



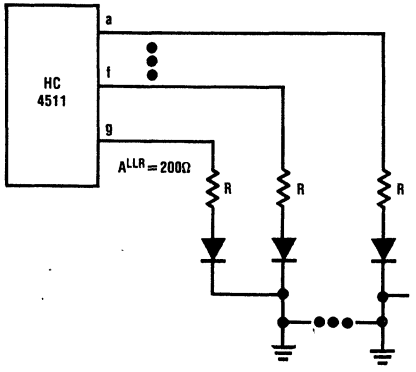
TL/F/5373–2



TL/F/5373–3

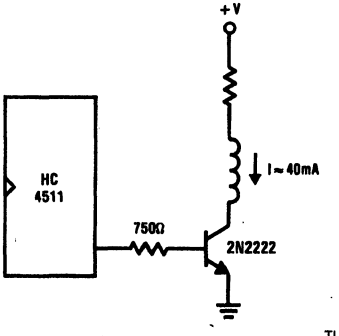
*The expected minimum curves are not guarantees, but are design aids.

Typical Applications



TL/F/5373–4

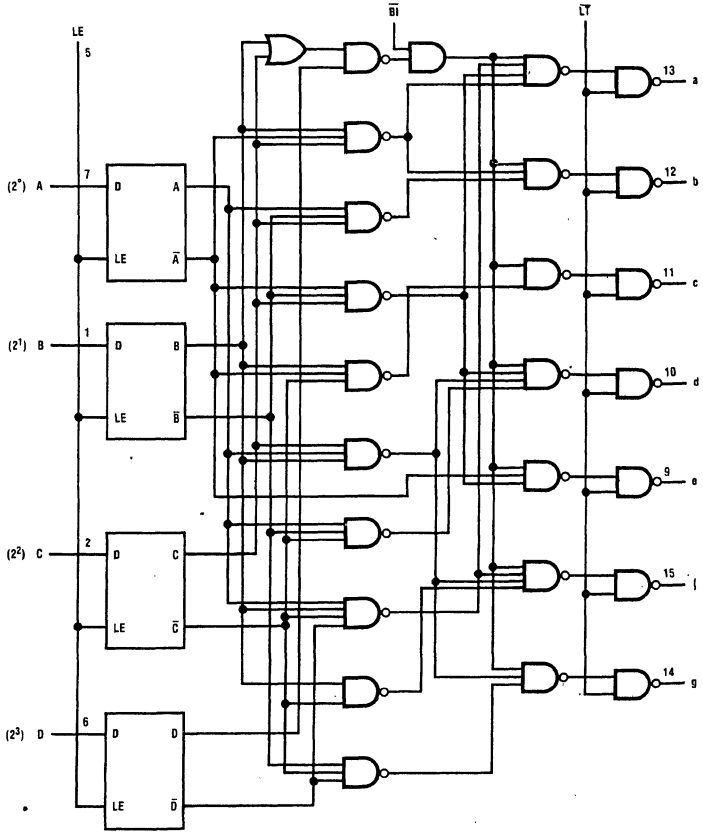
Typical Common Cathode LED Connection



TL/F/5373–5

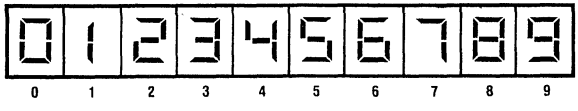
Incandescent Bulb Driving Circuit

Logic Diagram



TL/F/5373–6

Display



TL/F/5373–7

Segment Identification

TL/F/5373–8

National Semiconductor

PRELIMINARY

microCMOS

MM54HC4514/MM74HC4514
4-to-16 Line Decoder with Latch

General Description

This utilizes microCMOS Technology, 3.5 micron silicon gate P-well CMOS decoder, which is well suited to memory address decoding or data routing application. It possesses high noise immunity and low power dissipation usually associated with CMOS circuitry, yet speeds comparable to low power Schottky TTL circuits. It can drive up to 10 LS-TTL loads.

The MM54HC4514/MM74HC4514 contain a 4-to-16 line decoder and a 4-bit latch. The latch can store the data on the select inputs, thus allowing a selected output to remain high even though the select data has changed. When the LATCH ENABLE input to the latches is high the outputs will change with the inputs. When LATCH ENABLE goes low the data on the select inputs is stored in the latches. The four select inputs determine which output will go high provided the INHIBIT input is low. If the INHIBIT input is high all outputs are held low thus disabling the decoder.

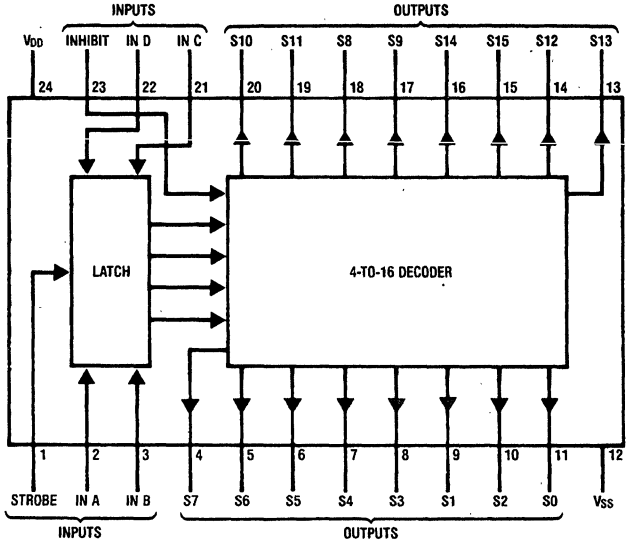
The MM54HC4514/MM74HC4514 is functionally and pinout equivalent to the CD4514BM/CD4514BC and the MC1451BA/MC1451BC. All inputs are protected against damage due to static discharge diodes from V_{CC} and ground.

Features

- Typical propagation delay: 18 ns
- Low quiescent power: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads (74HC Series)

Connection Diagram

Dual-In-Line Package



Top View

Order Number MM54HC4514J or MM74HC4514J,N
See NS Package J24A or N24A

Truth Table

		Data Inputs				
LE	Inhibit	D	C	B	A	Selected Output High
H	L	L	L	L	L	S0
H	L	L	L	L	H	S1
H	L	L	L	H	L	S2
H	L	L	L	H	H	S3
H	L	L	H	L	L	S4
H	L	L	H	L	H	S5
H	L	L	H	H	L	S6
H	L	L	H	H	H	S7
H	L	H	L	L	L	S8
H	L	H	L	L	H	S9
H	L	H	L	H	L	S10
H	L	H	L	H	H	S11
H	L	H	H	L	L	S12
H	L	H	H	L	H	S13
H	L	H	H	H	L	S14
H	L	H	H	H	H	S15
X	H	X	X	X	X	All Outputs = 0
L	L	X	X	X	X	Latched Data

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\| \le 4.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\| \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

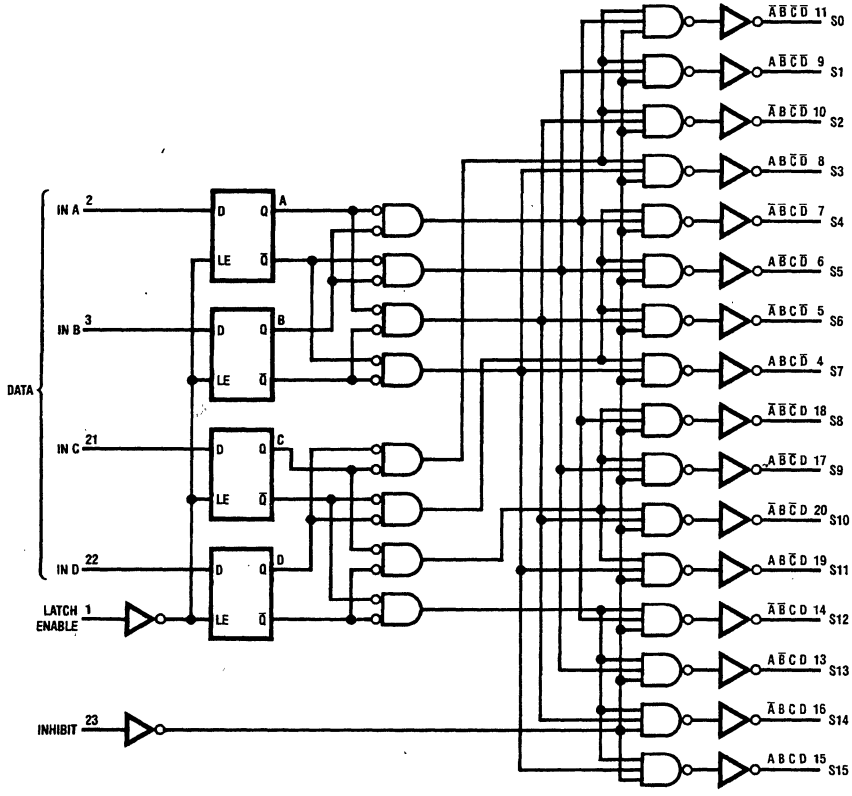
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		18	30	ns
t_{PHL}	Maximum Propagation Delay LE to Output		18	30	ns
t_{PLH}	Maximum Propagation Delay LE to Output		24	40	ns
t_{PHL}	Maximum Propagation Delay Inhibit to Output		16	30	ns
t_{PLH}	Maximum Propagation Delay Inhibit to Output		24	40	ns
t_s	Minimum Setup Time, Date to LE			20	ns
t_H	Minimum Hold Time, LE to Data			5	ns
t_W	Minimum Pulse Width, Latch Enable			16	ns

AC Electrical Characteristics $V_{CC}=2.0V-6.0V$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output		2.0V	80	175	220	263	ns
			4.5V	18	35	44	53	ns
			6.0V	16	30	38	45	ns
t_{PHL}	Maximum Propagation Delay LE to Output		2.0V	80	175	220	263	ns
			4.5V	19	35	44	53	ns
			6.0V	17	30	38	45	ns
t_{PLH}	Maximum Propagation Delay LE to Output		2.0V	120	230	290	343	ns
			4.5V	27	46	58	69	ns
			6.0V	22	39	49	58	ns
t_{PHL}	Maximum Propagation Delay Inhibit to Output		2.0V	70	175	220	263	ns
			4.5V	18	35	44	53	ns
			6.0V	16	30	38	45	ns
t_{PLH}	Maximum Propagation Delay Inhibit to Output		2.0V	120	230	290	343	ns
			4.5V	27	46	58	69	ns
			6.0V	22	39	49	58	ns
t_s	Minimum Setup Time, Data to LE		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time, LE to Data		2.0V		5	5	5	ns
			4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width, Latch Enable		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
C_{PD}	Power Dissipation Capacitance							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

Logic Diagram



TL/F/5215–2

3

National Semiconductor

microCMOS

MM54HC4538/MM74HC4538 Dual Retriggerable Monostable Multivibrator

General Description

The MM54HC4538/MM74HC4538 high speed monostable multivibrators (one shots) are implemented in micro-CMOS Technology, 3.5 micron silicon gate P-well CMOS. They feature speeds comparable to low power Schottky TTL circuitry while retaining the low power and high noise immunity characteristic of CMOS circuits.

Each multivibrator features both a negative, A, and a positive, B, transition triggered input, either of which can be used as an inhibit input. Also included is a clear input that when taken low resets the one shot. The 'HC4538 is retriggerable. That is, it may be triggered repeatedly while their outputs are generating a pulse and the pulse will be extended.

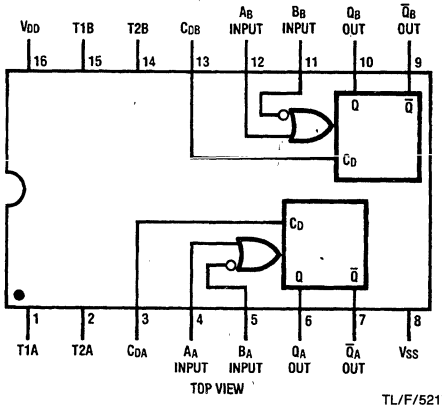
Pulse width stability over a wide range of temperature and supply is achieved using linear CMOS techniques. The output pulse equation is simply: PW = 0.7(R) (C) where PW is in seconds, R is in ohms, and C is in farads. This device is pin compatible with the CD4528, and the CD4538 one shots. All inputs are protected from damage due to static discharge by diodes to Vcc and ground.

Features

- Schmitt trigger on A and B inputs
- Wide power supply range: 2–6V
- Typical trigger propagation delay: 32 ns
- Fanout of 10 LS-TTL loads (74HC)
- Low input current: 1 μA max

Connection and Block Diagrams

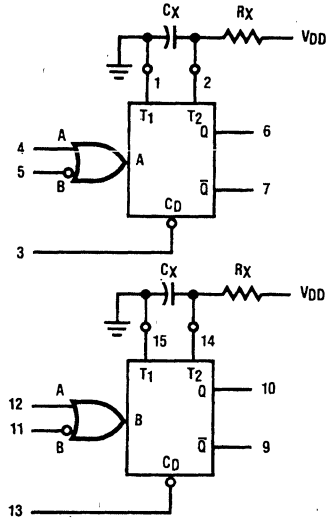
Dual-In-Line Package



TOP VIEW

TL/F/5217–1

Order Number MM54HC4538J or MM74HC4538J,N
See NS Package J16A or N16E



RX AND CX ARE EXTERNAL COMPONENTS

TL/F/5217–2

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to Vcc+1.5V
DC Output Voltage (V_{OUT})	−0.5 to Vcc+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HC	−40	+85	°C
MM54HC	−55	+125	°C
Input Rise or Fall Times (Reset only)			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	74HC T_A = −40 to 85°C	54HC T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		3.98	3.84	3.7	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \leq 4.0$ mA	4.5V		0.26	0.33	0.4	V
		$\|I_{OUT}\| \leq 5.2$ mA	6.0V		0.26	0.33	0.4	V
I_{IN}	Maximum Input Current (Pins 2, 14)	V_{IN} = V_{CC} or GND	6.0V		±0.5	±5.0	±10	μA
I_{IN}	Maximum Input Current (all other pins)	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA Pins 2 and 14 = 0.5V_{CC}	6.0V	100	150	250	400	μA

Note 1: Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation Temperature Derating: Plastic "N" Package: −12mW/°C from 65°C to 85°C Ceramic "J" Package: −12mW/°C from 100°C to 125°C

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

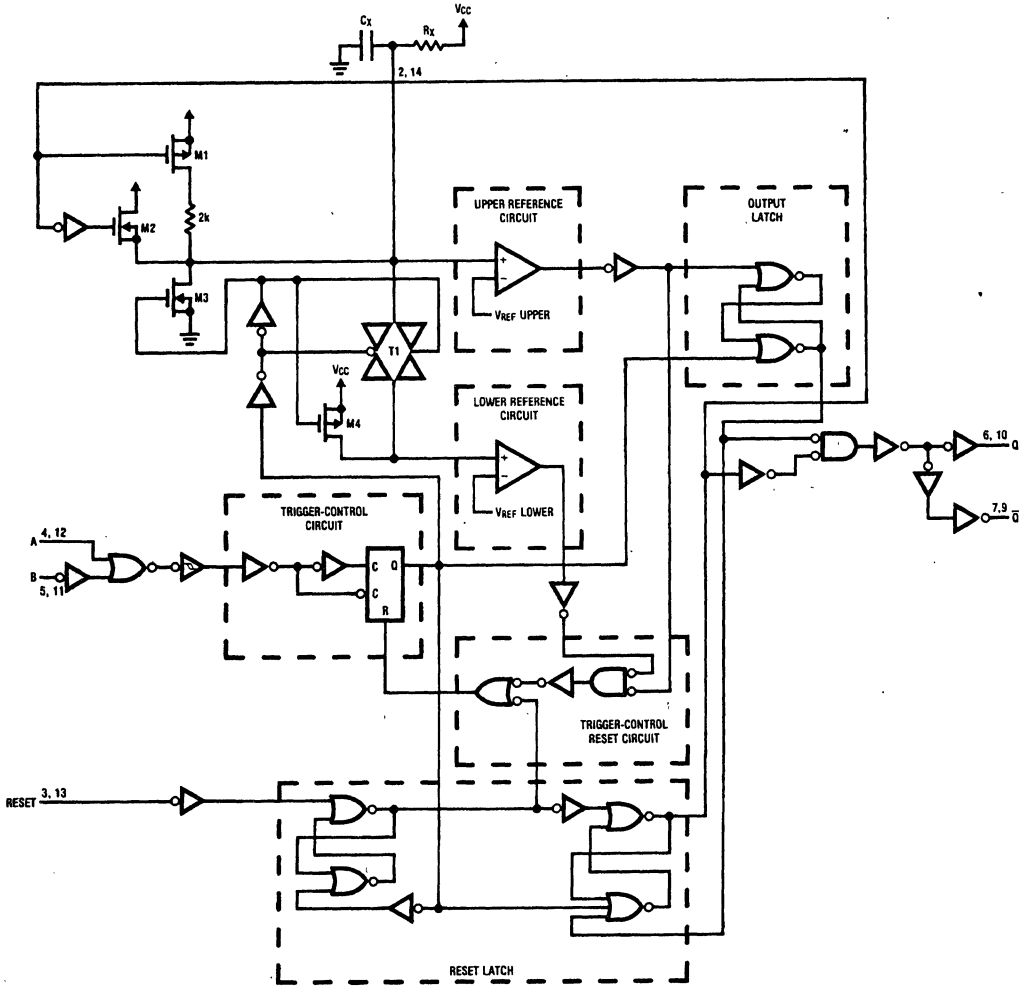
Symbol	Parameter	Conditions	Typ	Limit	Units
t_{PLH}	Maximum Propagation Delay A, or B to Q		23	45	ns
t_{PHL}	Maximum Propagation Delay A, or B to $\overline{Q}$		26	50	ns
t_{PHL}	Maximum Propagation Delay Clear to Q		23	45	ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$		26	50	ns
t_W	Minimum Pulse Width A, B or Clear		10	16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions		V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to 85°C	54HC $T_A=-55$ to 125°C	Units
					Typ	Guaranteed Limits		
t_{PLH}	Maximum Propagation Delay A, or B to Q			2.0V 4.5V 6.0V	100 25 21	250 50 43	315 63 54	373 75 63	ns ns ns
t_{PHL}	Maximum Propagation Delay A, or B to $\overline{Q}$			2.0V 4.5V 6.0V	110 28 23	275 55 47	347 69 59	410 82 70	ns ns ns
t_{PHL}	Maximum Propagation Delay Clear to Q			2.0V 4.5V 6.0V	100 25 21	250 50 43	315 63 54	373 75 63	ns ns ns
t_{PLH}	Maximum Propagation Delay Clear to $\overline{Q}$			2.0V 4.5V 6.0V	110 28 23	275 55 47	347 69 59	410 82 70	ns ns ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			2.0V 4.5V 6.0V	30 10 8	75 15 13	95 19 16	110 22 19	ns ns ns
t_r, t_f	Maximum Input Rise and Fall Time (Reset only)			2.0V 4.5V 6.0V		1000 500 400	1000 500 400	1000 500 400	ns ns ns
t_W	Minimum Pulse Width A, B, Clear			2.0V 4.5V 6.0V		80 16 14	101 20 17	119 24 20	ns ns ns
t_{WQ}	Output Pulse Width	$C_X=12$ pF $R_X=1$ kΩ	Min	3.0V 5.0V	283 147	190 120			ns ns
			Max	3.0V 5.0V	283 147	400 185			ns ns
t_{WQ}	Output Pulse Width	$C_X=100$ pF $R_X=10$ kΩ	Min	3.0V 5.0V	1.2 1.0				μs μs
			Max	3.0V 5.0V	1.2 1.0				μs μs
t_{WQ}	Output Pulse Width	$C_X=1000$ pF $R_X=10$ kΩ	Min	3.0V 5.0V	10.5 10.0	9.4 9.3			μs μs
			Max	3.0V 5.0V	10.5 10.0	11.6 11.7			μs μs
C_{IN}	Maximum Input Capacitance (Pins 2 & 14)				25				pF
C_{IN}	Maximum Input Capacitance (other inputs)				5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per one shot)			150				pF
Δt_{WQ}	Pulse Width Match Between Circuits in Same Package				±1				%

Note 5: C_{PD} determines the no load dynamic consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = V_{CC} f + I_{CC}$.

Logic Diagram



TL/F/5217–3

Circuit Operation

The 'HC4538 operates as follows (refer to logic diagram). In the quiescent state, the external timing capacitor, C_X, is charged to V_{CC}. When a trigger occurs, the Q output goes high and C_X discharges quickly to the lower reference voltage (V_{REF} Lower = ⅓ V_{CC}). C_X then charges, through R_X, back up to the upper reference voltage (V_{REF} Upper = ⅔ V_{CC}), at which point the one-shot has timed out and the Q output goes low.

The following, more detailed description of the circuit operation refers to both the logic diagram and the timing diagram.

QUIESCENT STATE

In the quiescent state, before an input trigger appears, the output latch is high and the reset latch is high (#1 in logic diagram).

Thus the Q output (pin 6 or 10) of the monostable multivibrator is low (#2, timing diagram).

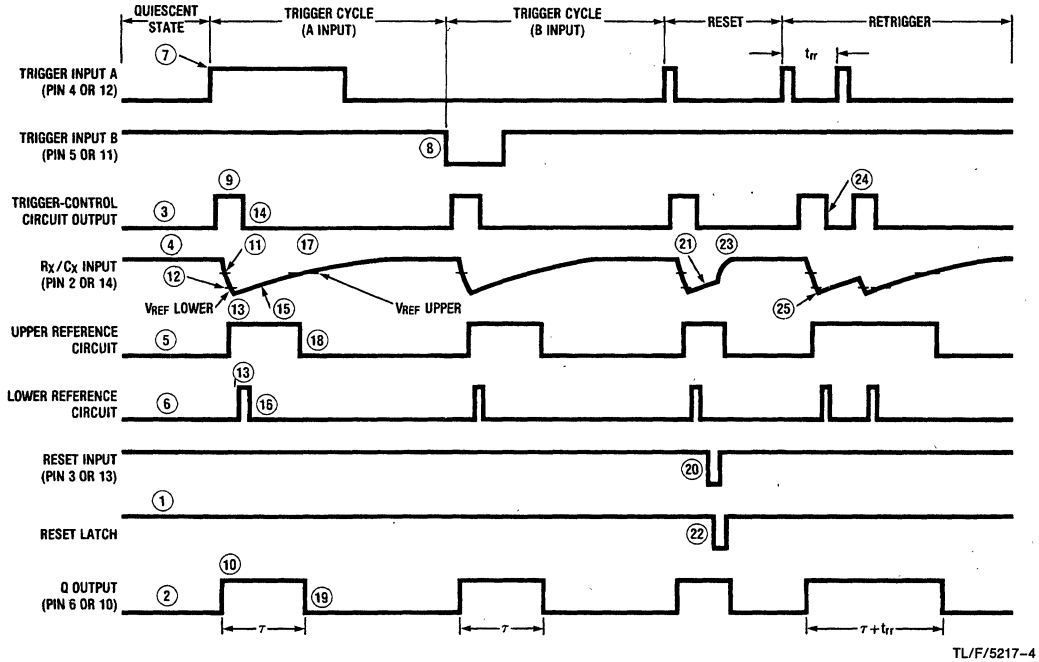
The output of the trigger-control circuit is low (#3), and transistors M1, M2, and M3 are turned off. The external timing capacitor, C_X, is charged to V_{CC} (#4), and the upper reference circuit has a low output (#5). Transistor M4 is turned on and transmission gate T1 is turned off. Thus the lower reference circuit has V_{CC} at the noninverting input and a resulting low output (#6).

In addition, the output of the trigger-control reset circuit is low.

TRIGGER OPERATION

The 'HC4538 is triggered by either a rising-edge signal at input A (#7) or a falling-edge signal at input B (#8), with the unused trigger input and the Reset input held at the voltage levels shown in the Truth Table. Either trigger signal will cause the output of the trigger-control circuit to go high (#9).

Timing Diagram



TL/F/5217–4

Circuit Operation (Continued)

The trigger-control circuit going high simultaneously initiates three events. First, the output latch goes low, thus taking the Q output of the 'HC4538 to a high state (#10). Second, transistor M3 is turned on, which allows the external timing capacitor, C_X, to rapidly discharge toward ground (#11). (Note that the voltage across C_X appears at the input of the upper reference circuit comparator.) Third, transistor M4 is turned off and transmission gate T1 is turned on, thus allowing the voltage across C_X to also appear at the input of the lower reference circuit comparator.

When C_X discharges to the reference voltage of the lower reference circuit (#12), the outputs of both reference circuits will be high (#13). The trigger-control reset circuit goes high, resetting the trigger-control circuit flip-flop to a low state (#14). This turns transistor M3 off again, allowing C_X to begin to charge back up toward V_{CC}, with a time constant $t = R_X C_X$ (#15). In addition, transistor M4 is turned on and transmission gate T1 is turned off. Thus a high voltage level is applied to the input of the lower reference circuit comparator, causing its output to go low (#16). The monostable multivibrator may be retriggered at any time after the trigger-control circuit goes low.

When C_X charges up to the reference voltage of the upper reference circuit (#17), the output of the upper reference circuit goes low (#18). This causes the output latch to toggle, taking the Q output of the 'HC4538 to a low state (#19), and completing the time-out cycle.

RESET OPERATION

A low voltage applied to the Reset pin always forces the Q output of the 'HC4538 to a low state.

The timing diagram illustrates the case in which reset occurs (#20) while C_X is charging up toward the reference voltage of the upper reference circuit (#21). When a reset occurs, the output of the reset latch goes low (#22), turning on transistor M1. Thus C_X is allowed to quickly charge up to V_{CC} (#23) to await the next trigger signal.

RETRIGGER OPERATION

In the retriggerable mode, the 'HC4538 may be retriggered during timing out of the output pulse at any time after the trigger-control circuit flip-flop has been reset (#24). Because the trigger-control circuit flip-flop resets shortly after C_X has discharged to the reference voltage of the lower reference circuit (#25), the minimum retrigger time, t_{rr} is a function of internal propagation delays and the discharge time of C_X:

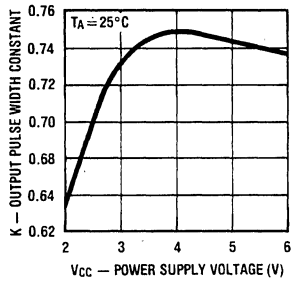
$$t_{rr}(\text{ns}) \cong 72 + \frac{V_{CC}(\text{volts}) \bullet C_X(\text{pF})}{30.5}, \text{ at room temperature}$$

Circuit Operation (Continued)

POWER-DOWN CONSIDERATIONS

Large values of C_X may cause problems when powering down the HC4538 because of the amount of energy stored in the capacitor. When a system containing this device is powered down, the capacitor may discharge from V_{CC} through the input protection diodes at pin 2 or pin 14. Current through the protection diodes must be limited to 30 mA; therefore, the turn-off time of the V_{CC} power supply must not be faster than $t = V_{CC} \bullet C_X/(30\ mA)$. For example, if $V_{CC} = 5V$ and $C_X = 15\ \mu F$, the V_{CC} supply must turn off no faster than $t = (15V) \bullet (15\ \mu F)/30\ mA = 2.5$ ms. This is usually not a problem because power supplies are heavily filtered and cannot discharge at this rate.

When a more rapid decrease of V_{CC} to zero volts occurs, the HC4538 may sustain damage. To avoid this possibility, use an external clamping diode, D_X, connected from V_{CC} to the C_X pin.



TL/F/5217–5

3

National Semiconductor

microCMOS

MM54HC4543/MM74HC4543 BCD-to-7 Segment Latch/Decoder/Driver for Liquid Crystal Displays

General Description

The MM54HC4543/MM74HC4543 BCD-to-7 segment latch/decoder/driver utilize microCMOS Technology, 3.5 micron silicon gate P-well CMOS, and can be used either as a high speed decoder or as a display driver. This circuit contains a 4-bit latch, BCD-to-7 segment decoder, and 7 output drivers. Data on the input pins flow through to the output when the LATCH ENABLE (LE) is high and is latched on the high to low transition of the LE input. The PHASE input (PH) controls the polarity of the 7 segment outputs. When PH is low the outputs are true 7 segment, and when PH is high the outputs are inverted 7 segment. When the PHASE input is driven by a liquid crystal display (LCD) backplane waveform the segment pins output the correct segment waveform for proper LCD AC drive voltages.

In addition a BLANKING INPUT (BI) is provided, which will blank the display.

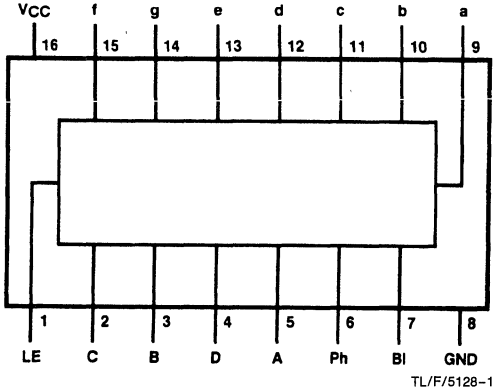
The MM54HC4543/MM74HC4543 are functionally and pinout equivalent to the CD4543BC/CD4543BM and the MC14543BA/MC14543BC. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical propagation delay: 60 ns
- Supply voltage range: 2–6V
- Maximum input current: 1 μA
- Maximum quiescent supply current: 80 μA (74HC)
- Display blanking
- Low dynamic power consumption

Connection Diagram

Dual-In-Line Package

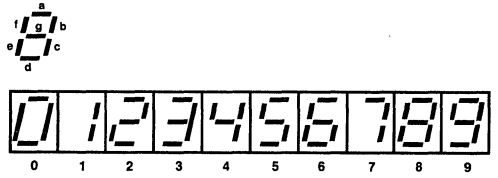


TL/F/5128–1

Top View

Order Number MM54HC4543J or MM74HC4543J, N
See NS Package J16A or N16E

Display Format



TL/F/5128–2

Truth Table

Inputs							Outputs							
LE	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	L	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	H	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	L	H	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	H	L	L	L	L	L	L	L	Blank
L	L	L	X	X	X	X	**							**
†	†	H	†				Inverse of Output Combinations Above							Display as above

X — don't care

† = same as above combinations

* = for liquid crystal readouts, apply a square wave to Ph.

** = depends upon the BCD code previously applied when LE—H

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

		Min	Max	Units
Supply Voltage (V_{CC})		2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})		0	V_{CC}	V
Operating Temp. Range (T_A)				
MM74HC		−40	+85	°C
MM54HC		−55	+125	°C
Input Rise or Fall Times (t_r, t_f)	V_{CC}=2.0V		1000	ns
	V_{CC}=4.5V		500	ns
	V_{CC}=6.0V		400	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HC T_A=−40 to 85°C	54HC T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum Low Level Input Voltage		2.0V		0.3	0.3	0.3	V
			4.5V		0.9	0.9	0.9	V
			6.0V		1.2	1.2	1.2	V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 0.4$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|\leq 0.52$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		$V_{IN}=V_{IH}$ or V_{IL} $\|I_{OUT}\|\leq 0.4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|\leq 0.52$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$	6.0V		8.0	80	160	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

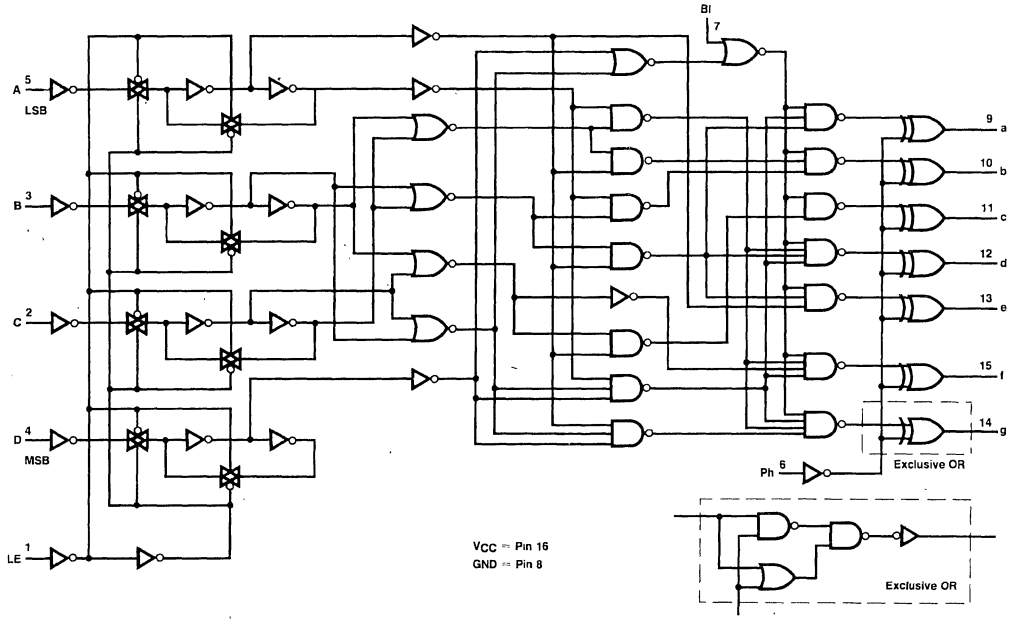
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, BI, Ph to Output		60	100	ns
t_s	Minimum Setup Time LE to Data			20	ns
t_H	Minimum Hold Time Data to LE			10	ns
t_W	Minimum LE Pulse Width			16	ns

AC Electrical Characteristics $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HC $T_A=-40$ to $85°C$	54HC $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data LE, Ph, BI to Output		2.0V	300	600	760	895	ns
			4.5V	60	120	151	179	ns
			6.0V	51	102	129	152	ns
t_s	Minimum Setup Time LE to Data		2.0V		100	125	150	ns
			4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_H	Minimum Hold Time Data to LE		2.0V		50	63	75	ns
			4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_W	Minimum LE Pulse Width		2.0V		80	100	120	ns
			4.5V		16	20	24	ns
			6.0V		14	17	20	ns
C_{PD}	Power Dissipation Capacitance (Note 5)							pF
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF

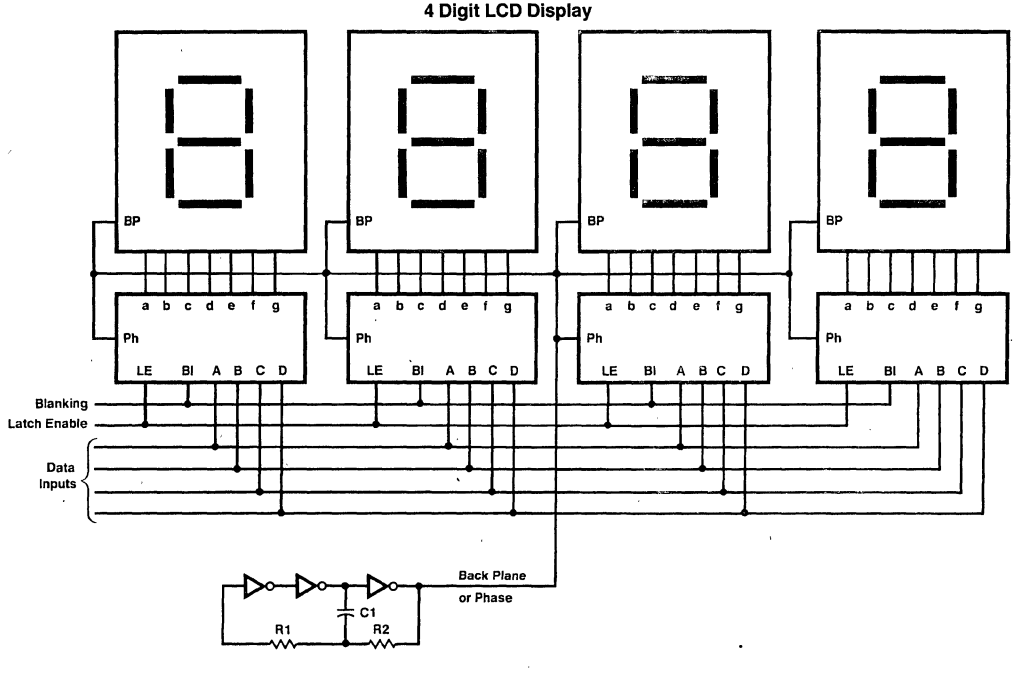
Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

Logic Diagram



TL/F/5128–3

Typical Applications



TL/F/5128–4

Section 4
MM54HCT/
MM74HCT

4

Section Contents

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT00/MM74HCT00 Quad 2 Input NAND Gate

General Description

The MM54HCT00/MM74HCT00 are NAND gates fabricated using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pin-out compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

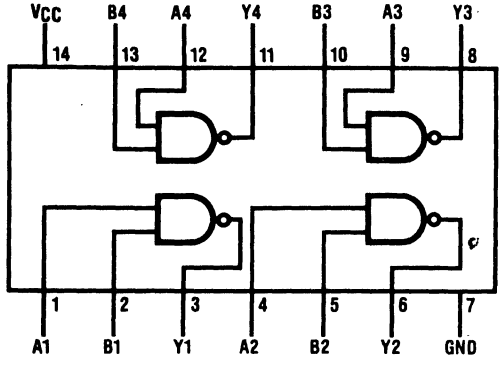
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 14 ns (typ)
- Low power: 10 μW at DC
- High fan out, 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

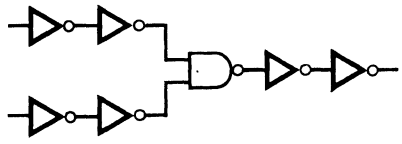


TL/F/5356–1

Top View

Order Number MM54HCT00J or MM74HCT00J, N
See NS Package J14A or N14A

(1 of 4 gates)



TL/F/5356–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND, I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

AC Electrical Characteristics V_{CC}=5.0V, t_r=t_f=6 ns, C_L=15 pF, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		12	18	ns

AC Electrical Characteristics V_{CC}=5.0V±10%, t_r=t_f=6 ns, C_L=50 pF (unless otherwise noted)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay		14	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

Note 5: C_{PD} determines the no load dynamic power consumption, P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}, and the no load dynamic current consumption, I_S=C_{PD} V_{CC} f+I_{CC}.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT04/MM74HCT04 Hex Inverter

General Description

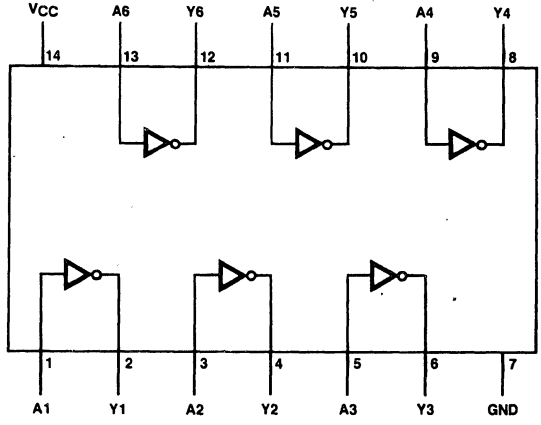
The MM54HCT04/MM74HCT04 are logic functions fabricated by using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS - low quiescent power and wide power supply range, but are input and output characteristic as well as pin-out compatible with standard DM54LS/74LS devices. The MM54HCT04/MM74HCT04, triple buffered, inverting hex inverters, feature low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 12 ns (typ)
- Low power: 10 μW at DC, 2.5 mW at 5 MHz
- High fanout: ≥ 10 LS loads
- Inverting, triple buffered

Connection Diagram



TL/F/5357–1

Top View

Order Number MM54HCT04J or MM74HCT04J,N
See NS Package J14A or N14A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		2.0	20	40	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

AC Electrical Characteristics V_{CC}=5.0V, t_r=t_f=6 ns C_L=15 pF, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	18	ns

AC Electrical Characteristics V_{CC}=5.0V ±10%, t_r=t_f=6 ns, C_L=50 pF (unless otherwise noted)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
t_{PLH}, t_{PHL}	Maximum Propagation Delay		14	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

Note 5: C_{PD} determines the no load dynamic power consumption, P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}, and the no load dynamic current consumption, I_S=C_{PD} V_{CC} f +I_{CC}.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT05/MM74HCT05 Hex Inverter (Open Drain)

General Description

The MM54HCT05/MM74HCT05 are logic functions fabricated by using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are also input-output characteristically and pin-out compatible with standard DM54LS/DM74LS logic families. The MM54HCT05/MM74HCT05 open drain Hex Inverter requires the addition of an external resistor to perform a wire-NOR function.

All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

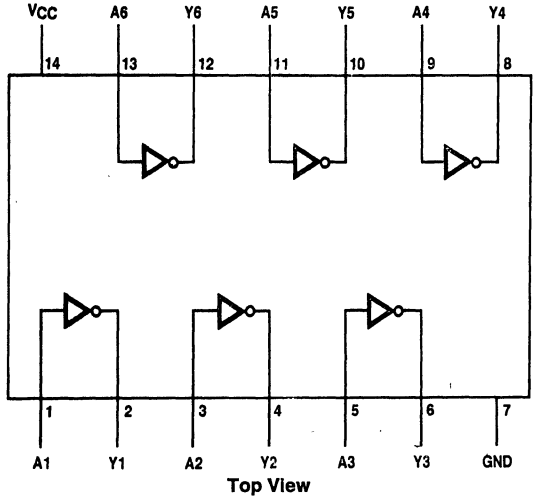
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Open drain for wire-NOR function
- LS-TTL pinout and threshold compatible
- Fanout of 10 LS-TTL loads
- Typical propagation delays:
  t_{PLH} (with 1 kΩ resistor) 10 ns
  t_{PHL} (with 1 kΩ resistor) 8 ns

Connection Diagram

Dual-In-Line Package

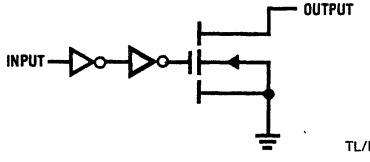


TL/F/5358–1

Top View

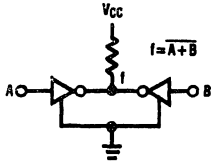
Order Number MM54HCT05J or MM74HCT05J, N
See NS Package J14A or N14A

Logic Diagram



TL/F/5358–2

Typical Application



TL/F/5358–3

Note: Can be extended to more than 2 inputs.

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC} = 5V ±10%, unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}, R_L = 1 kΩ $\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} $\|I_{OUT}\|$ = 20 μA $\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V $\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V V V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{LKG}	Minimum High Level Output Leakage Current	V_{IN} = V_{IH} or VIL, V_{OUT} = V_{CC}		0.5	5.0	10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns unless otherwise noted.

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay	$R_L=1$ kΩ	8	15	ns
t_{PLH}	Maximum Propagation Delay	$R_L=1$ kΩ	9	16	ns

AC Electrical Characteristics $V_{CC}=5V \pm 10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay	$R_L=1$ kΩ	10	22	28	33	ns
t_{PLH}	Maximum Propagation Delay	$R_L=1$ kΩ	12	20	25	30	ns
t_{THL}	Maximum Output Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per gate) $R_L=\infty$		20			pF
C_{IN}	Maximum Input Capacitance			5	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT08/MM74HCT08 Quad 2-Input AND Gate

General Description

The MM54HCT08/MM74HCT08 are logic functions fabricated by using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. These devices are input and output characteristic and pinout compatible with standard DM54LS/74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

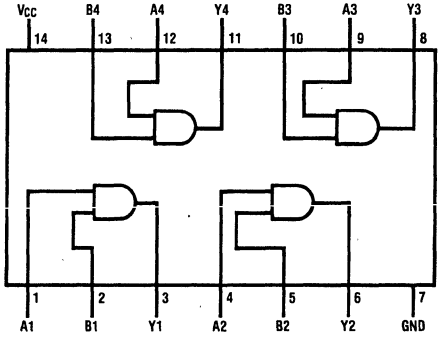
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 12 ns (typ)
- Low power: 10 μW at DC
- High fan-out, 10 LS-TTL loads

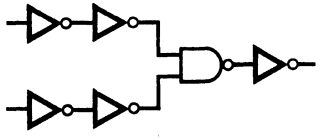
Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5754–1

Order Number MM54HCT08J or MM74HCT08J,N
See NS Package J14A or N14A



TL/F/5754–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package −12 mW/°C from 65°C to 85°C: ceramic "J" package 12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		12	20	ns

AC Electrical Characteristics $V_{CC}=5.0V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		15	24	30	35	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	38				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption. $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$ and the no load dynamic current consumption. $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT34/MM74HCT34 Non-Inverter

General Description

The MM54HCT34/74HCT34 are logic functions fabricated by using microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of CMOS - low quiescent power and wide power supply range, but are input and output characteristic as well as pin-out compatible with standard DM54LS/74LS devices. The MM54HCT34/MM74HCT34 feature low power dissipation and fast switching times. All inputs are protected from static discharge by internal diodes to V_{CC} and ground.

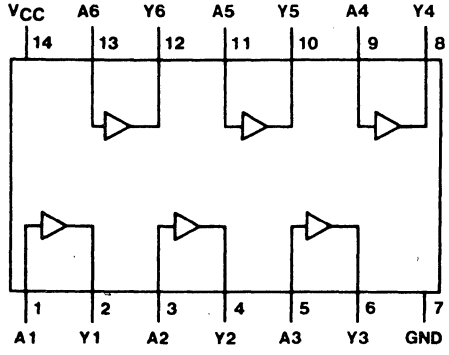
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL, LS pin-out and threshold compatible
- Fast switching: t_{PLH}, t_{PHL} = 8 ns (typ)
- Low power: 10 μW at DC, 2.5 mW at 5 MHz
- High fanout: ≥ 10 LS loads

Connection Diagram

Dual-In-Line Package



TL/F/5359–1

Top View

Order Number MM54HCT34J or MM74HCT34J, N
See NS Package J14A or N14A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		2.0	20	40	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input with all other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5.0V$, $t_r=t_f=6$ ns, $C_L=15$ pF, $T_A=25°C$ (unless otherwise noted)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	20	ns

AC Electrical Characteristics $V_{CC}=5.0V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF (unless otherwise noted)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PLH}, t_{PHL}	Maximum Propagation Delay		10	22	29	33	ns
t_{THL}, t_{TLH}	Maximum Output Rise & Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)	20				pF
C_{IN}	Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

4

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT74/MM74HCT74
Dual D Flip-Flop with Preset and Clear

General Description

The MM54HCT74/MM74HCT74 utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS, to achieve operation speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 54HCT/74HCT logic family is functionally and pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

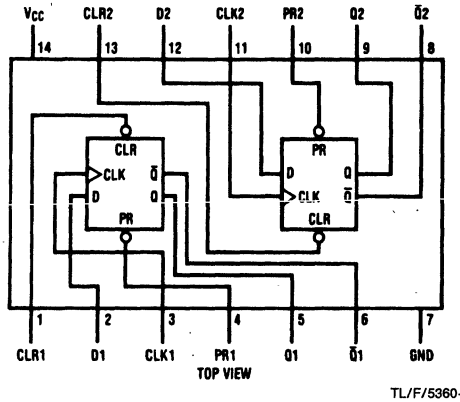
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Meta-stable hardened

Connection and Logic Diagrams

Dual-In-Line Package



TL/F/5360–1

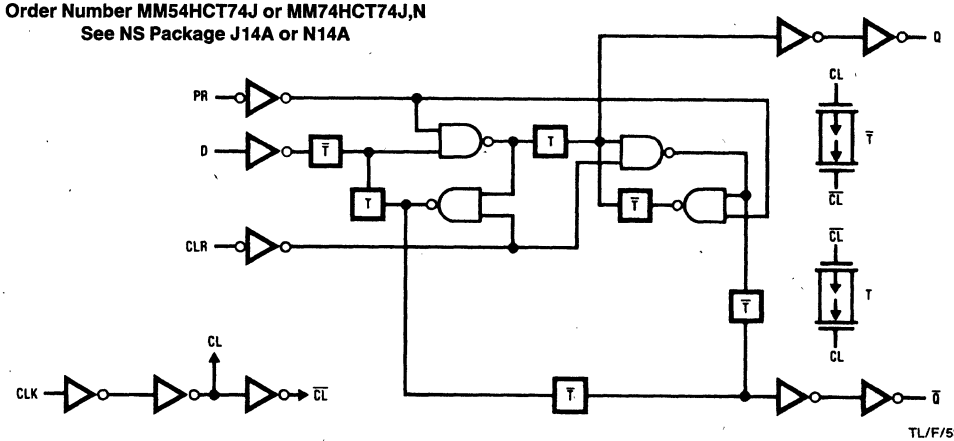
Order Number MM54HCT74J or MM74HCT74J,N
See NS Package J14A or N14A

Truth Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.



TL/F/5360–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		4.0	40	80	μA
		V_{IN}=2.4V or 0.5V (Note 4)		0.3	0.4	0.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per pin. All other inputs are held at V_{CC} Ground.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency from Clock to Q or $\overline{Q}$		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Setup Time Data to Clock			20	ns
t_H	Minimum Hold Time Clock to Data		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics $V_{CC}=5.0V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		21	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		21	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		9	16	20	24	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)	30				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT76/MM74HCT76/ MM54HCT112/MM74HCT112 Dual J-K Flip-Flops with Preset and Clear

General Description

These flip-flops utilize silicon gate microCMOS technology. They have input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These flip-flops have independent J, K, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The flip-flops are edge-triggered and change state on the negative-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low logic level on the corresponding input.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

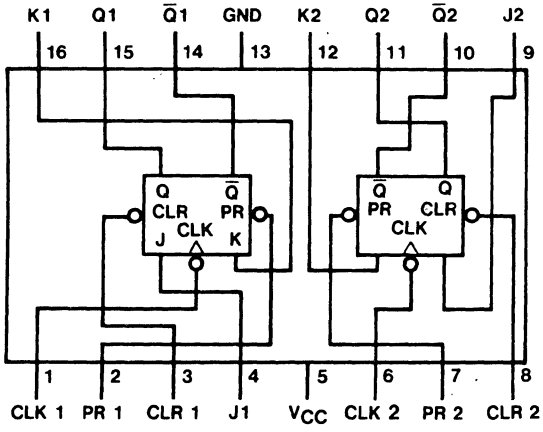
MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. When there is a LS-TTL equivalent, these parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5762–1

Order Number MM54HCT76J, MM74HCT76J,N, MM54HCT112J or MM74HCT112J,N
See NS Package J16A or N16E

Truth Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q0	$\overline{Q}$0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q0	$\overline{Q}$0

Note: Q0 = the level of Q before the indicated input conditions were established.

*This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		4.0	40	80	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, t_r = t_f = 6 ns

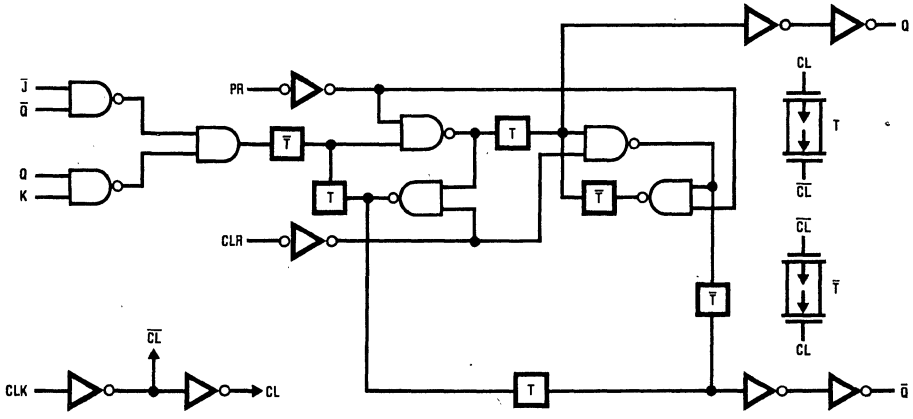
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set-Up Time J or K Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or K		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns unless otherwise specified

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40°C$ to $85°C$	54HCT $T_A=-55°C$ to $125°C$	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		22	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Setup Time J or K to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to J or K		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	20	24	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynaamic power consumption , $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Logic Diagram



TL/F/5762–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT109/MM74HCT109
Dual J-$\overline{K}$ Flip-Flops with Preset and Clear

General Description

These high speed J-$\overline{K}$ FLIP-FLOPS utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the low power consumption and high noise immunity of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

Each flip flop has independent J, $\overline{K}$, PRESET, CLEAR, and CLOCK inputs and Q and $\overline{Q}$ outputs. These devices are edge sensitive to the clock input and change state on the positive going transition of the clock pulse. Clear and preset are independent of the clock and accomplished by a low logic level on the corresponding input.

The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

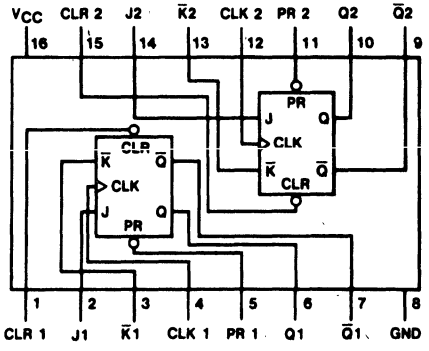
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low input current: 1 μA maximum
- Low quiescent current: 40 μA maximum (74HCT Series)
- Output drive capability: 10 LS-TTL loads

Connection and Logic Diagrams

Dual-In-Line Package

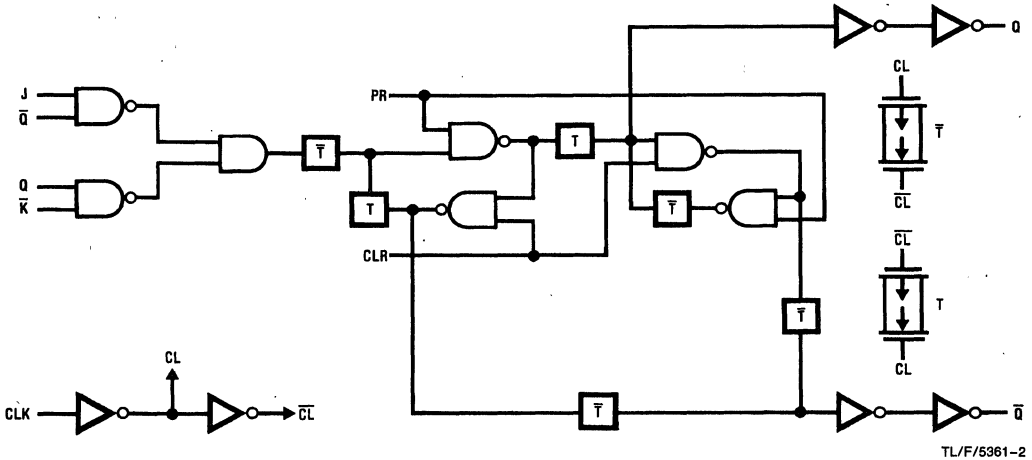


TL/F/5361–1

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q0	$\overline{Q}$0
H	H	↑	H	H	H	L
H	H	L	X	X	Q0	$\overline{Q}$0

Order Number MM54HCT109J or MM74HCT109J,N
See NS Package J16A or N16E



TL/F/5361–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		4.0	40	80	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		18	30	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Setup Time J or $\overline{K}$ Clock		10	20	ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		−3	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		8	16	ns

AC Electrical Characteristics $V_{CC}=5.0V \pm 10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40°$ to $85°C$	54HCT $T_A=-55°$ to $125°C$	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q or $\overline{Q}$		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Preset or Clear to Q or $\overline{Q}$		22	35	44	52	ns
t_{REM}	Minimum Removal Time Preset or Clear to Clock			20	25	30	ns
t_S	Minimum Setup Time J or $\overline{K}$ to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to J or $\overline{K}$		−3	0	0	0	ns
t_W	Minimum Pulse Width Clock, Preset or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD} V_{CC} f+I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT138/MM74HCT138 3-to-8 Line Decoder

General Description

This decoder utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and are well suited to memory address decoding or data routing applications. Both circuits feature high noise immunity and low power consumption usually associated with CMOS circuitry, yet have speeds comparable to low power Schottky TTL logic.

The MM54HCT138/MM74HCT138 have 3 binary select inputs (A, B, and C). If the device is enabled these inputs determine which one of the eight normally high outputs will go low. Two active low and one active high enables (G1, G2A and G2B) are provided to ease the cascading decoders.

The decoders' output can drive 10 low power Schottky TTL equivalent loads and are functionally and pin equivalent to the 54LS138/74LS138. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

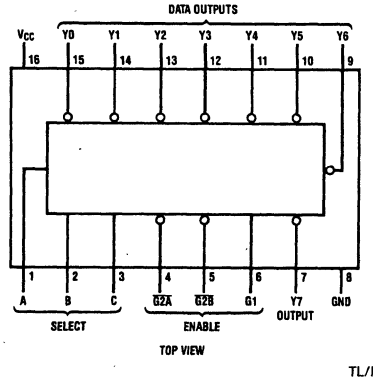
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads

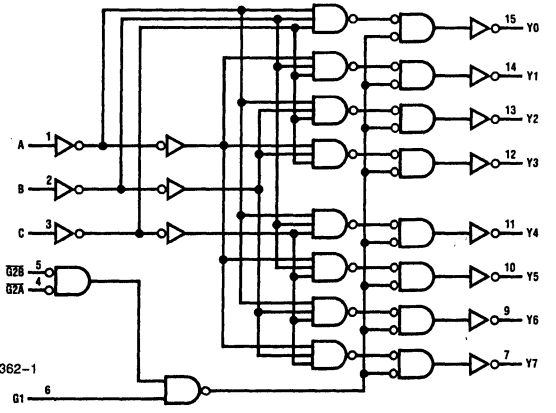
Connection Diagram

Dual-In-Line Package



Order Number MM54HCT138J or MM74HCT138J, N
See NS Package J16A, N16E

Logic Diagram



TL/F/5362-2

Truth Table

Inputs					Outputs							
Enable		Select										
G1	$\overline{G2}$*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*$\overline{G2} = \overline{G2A} + \overline{G2B}$

H = high level L = low level X = don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per input pin. All other inputs are held at V_{CC} or ground.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay, A, B, or C to Output		20	35	ns
t_{PLH}	Maximum Propagation Delay, A, B, or C to Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, G1 to Y Output		14	25	ns
t_{PLH}	Maximum Propagation Delay, G1 to Y Output		13	25	ns
t_{PHL}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		17	30	ns
t_{PLH}	Maximum Propagation Delay, $\overline{G2A}$ or $\overline{G2B}$ to Y Output		13	25	ns

AC Electrical Characteristics $V_{CC} = 5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A = 25°C$	74HCT $T_A = -40$ to $85°C$		54HCT $T = -55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay A, B, or C to Output		24	40	50	60	ns
t_{PLH}	Maximum Propagation Delay A, B, or C to Output		18	30	38	45	ns
t_{PHL}	Maximum Propagation Delay G1 to Y Output		17	30	38	45	ns
t_{PLH}	Maximum Propagation Delay G1 to Y Output		20	30	38	45	ns
t_{PHL}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		23	35	43	52	ns
t_{PLH}	Maximum Propagation Delay $\overline{G2A}$ or $\overline{G2B}$ to Y Output		18	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{IN}	Input Capacitance			5	10	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)					pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

4

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT139/MM74HCT139 Dual 2-To-4 Line Decoder

General Description

The MM54HCT139/MM74HCT139 is a high speed silicon-gate CMOS decoder that is well suited to memory address decoding or data routing applications. It possesses an input threshold and output drive similar to LS-TTL and the low standby of CMOS logic.

The device is comprised of two independent one-of-four decoders each with a single active low enable input (G1 or G2). Data on the select inputs (A1, B1 or A2, B2) cause one of the four normally high outputs to go low.

All inputs to the decoder are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground. The device is capable of driving 10 low power Schottky TTL equivalent loads.

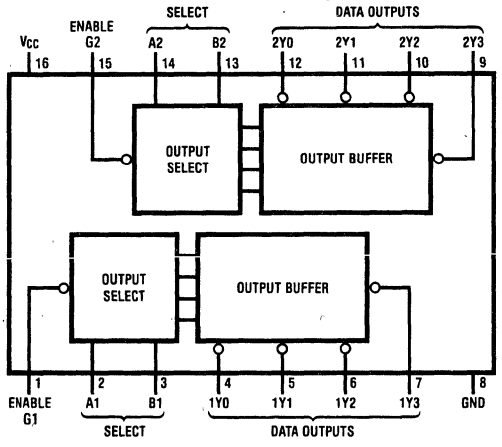
The MM54HCT139/MM74HCT139 is functionally and pin equivalent to the 54LS139/74LS139 and can be used as a plug-in replacement to reduce system power consumption in existing systems.

Features

- Typical propagation delays: 20 ns
- Low quiescent current: 40 μA maximum (74HCT Series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/5363–1

Top View
Order Number MM54HCT139J or MM74HCT139J, N
See NS Package J16A or N16E

Truth Table

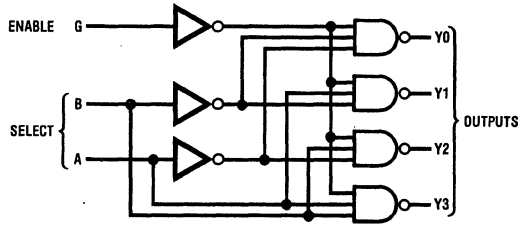
'HCT139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care

Logic Diagram

½ MM54HCT139/MM74HCT139



TL/F/5363–2

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	20 mA
DC Output Current, per Pin (I_{OUT})	25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	C
MM54HCT	−55	+125	C
Input Rise/Fall Time (t_r, t_f)		500	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	Typ	Guaranteed Limits			Units
				T=25°C	T=25°C	74HCT T=−40 to 85°C	54HCT T=−55 to 125°C	
V_{IH}	Minimum High Level Input Voltage							V
					2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8	0.8	0.8	V
								V
V_{OH}	Minimum High Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}						
		$\|I_{OUT}\|=20\ \mu A$		V_{CC}	$V_{CC}-.1$	$V_{CC}-.1$	$V_{CC}-.1$	V
		$\|I_{OUT}\|=4.0$ mA, $V_{CC}=4.5V$			3.98	3.84	3.7	V
		$\|I_{OUT}\|=4.8$ mA, $V_{CC}=5.5V$			4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Output Voltage	$V_{IN}=V_{IH}$ or V_{IL}						
		$\|I_{OUT}\|=20\ \mu A$			0.10	0.10	0.1	V
		$\|I_{OUT}\|=4.0$ mA, $V_{CC}=4.5V$			0.26	0.33	0.4	V
		$\|I_{OUT}\|=4.8$ mA, $V_{CC}=5.5V$			0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	$V_{IN}=V_{CC}$ or GND $V_{IN}=V_{IH}$ or V_{IL}			±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\ \mu A$ (Note 4)			4	40	80	μA
		$V_{IN}=2.4V$ or 0.5V $I_{OUT}=0\ \mu A$ (Note 4)			300	400	440	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating: plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs at V_{CC} or GND.

AC Electrical Characteristics (V_{CC}, temperature and loading of LS-TTL)

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
$t_{PLH,\ PHL}$	Maximum Propagation Delay, Binary Select to any Output		18	30	ns
$t_{PLH,\ PHL}$	Maximum Propagation Delay, Enable to any Output		18	30	ns

AC Electrical Characteristics

(Full range of V_{CC} and temperature) $V_{CC}=5V\ \pm 10\%$, $C_L=50$ pF (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits			Units
			$T_A=25°C$	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	
$t_{PLH,\ PHL}$	Maximum Propagation Delay, Binary Select to any Output		20	35	44	51	ns
$t_{PLH,\ PHL}$	Maximum Propagation Delay, Enable to any Output		21	35	44	51	ns
$t_{TLH,\ THL}$	Maximum Output Rise and Fall Time		9	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	Note 5					pF
C_{IN}	Minimum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=(C_{PD}\ V_{CC}^{\ 2})\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

National Semiconductor

microCMOS

MM54HCT149/MM74HCT149
8 Line to 8 Line Priority Encoder

General Description

This priority encoder is implemented in microCMOS Technology, 3.0 micron silicon gate N-well CMOS. It has the high noise immunity and low power consumption typical of CMOS circuits, as well as the speeds and output drive similar to LS-TTL.

This priority, encoder accepts 8 input request lines, $\overline{RI7}$–$\overline{RI0}$, and outputs 8 lines, $\overline{RO7}$–$\overline{RO0}$. Only one request output can be low at a time. The output that is low is dependent on the highest priority request input that is low. The order of priority is $\overline{RI7}$ highest and $\overline{RI0}$ lowest. Also provided is an enable input, $\overline{RQE}$, which, when high, forces all outputs high. A request output is also provided, $\overline{RQP}$, which goes low when any $\overline{RI}$ is active.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

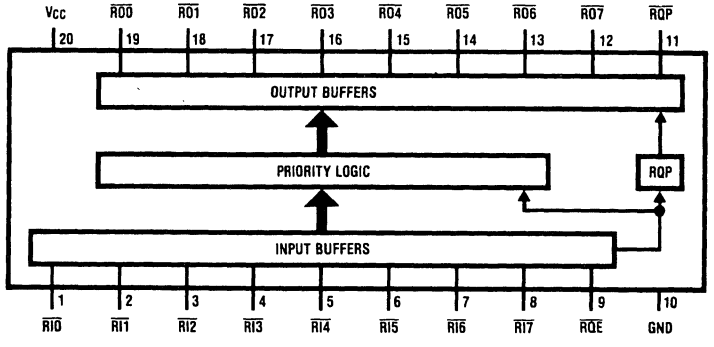
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- Internal switched pull up resistors provided to reduce power consumption

Connection Diagram

Dual-In-Line Package



TL/F/5364–1

Top View

Order Number MM54HCT149J or MM74HCT149J,N
See NS Package J20A or N20A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs held at V_{CC} or GND.

Truth Table

Inputs									Outputs								
0	1	2	3	4	5	6	7	$\overline{RQE}$	0	1	2	3	4	5	6	7	$\overline{RQP}$
X	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	L	L	H	H	H	H	H	H	H	L	L
X	X	X	X	X	X	L	H	L	H	H	H	H	H	H	L	H	L
X	X	X	X	X	L	H	H	L	H	H	H	H	H	L	H	H	L
X	X	X	X	L	H	H	H	L	H	H	H	H	L	H	H	H	L
X	X	X	L	H	H	H	H	L	H	H	H	L	H	H	H	H	L
X	X	L	H	H	H	H	H	L	H	H	L	H	H	H	H	H	L
X	L	H	H	H	H	H	H	L	H	L	H	H	H	H	H	H	L
L	H	H	H	H	H	H	H	L	L	H	H	H	H	H	H	H	L

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

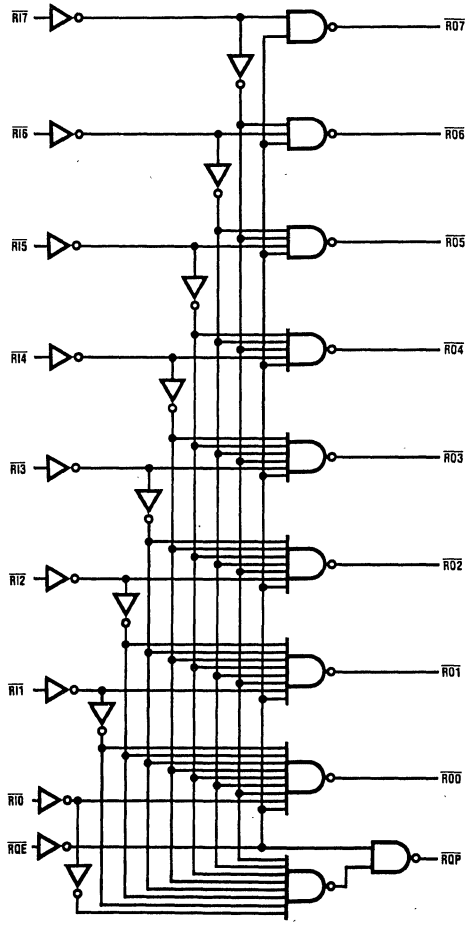
Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Any Input to $\overline{RQP}$		20	38	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Any Input to Any Other Output		20	34	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pf $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$		54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay $\overline{RQE}$ to any Output		17	42	52	63	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay $\overline{RIn}$ to $\overline{ROn}$ (same Output)		18	40	50	60	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		10	15	19	22	ns
C_{PD}	Power Dissipation Capacitance	(Note 5)		50			pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

Simplified Logic Diagram



TL/F/5364–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT155/MM74HCT155
Dual 2-to-4 Line Decoder/Demultiplexers

General Description

The MM54HCT155/MM74HCT155 is a high speed silicon gate CMOS decoder/demultiplexer. It features dual 1-to-4 line demultiplexers with independent strobes and common binary address inputs. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied to C2 is "non-inverted" at its outputs. The inverter following the C1 data input permits use as a 3-to-8 line decoder, or 1-to-8 line demultiplexer, without gating.

All inputs to the decoder are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground. The device is capable of driving 10 low power Schottky TTL equivalent loads.

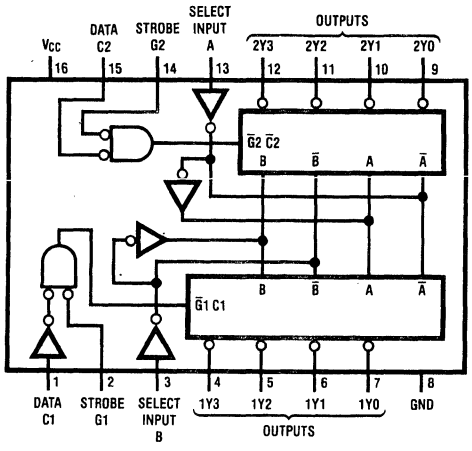
The MM54HCT155/MM74HCT155 is functionally and pin equivalent to the 54LS155/74LS155 and can be used as a plug-in replacement to reduce system power consumption in existing systems.

Features

- Applications:
  - Dual 2-to-4 line decoder
  - Dual 1-to-4 line demultiplexer
  - 3-to-8 line decoder
  - 1-to-8 line demultiplexer
- Typical propagation delay: 22 ns
- Low quiescent current: 80 μA maximum (74HCT Series)

Connection Diagram

Dual-In-Line Package



TL/F/5759-1

Order Number MM54HCT155J or MM74HCT155J, N
See NS Package J16A or N16E

IC = inputs C1 and C2 connected together
IG = inputs G1 and G2 connected together
H = high level
L = low level
X = don't care

Truth Tables

2-TO-4 LINE DECODER OR 1-TO-4 LINE DEMULTIPLEXER

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-TO-8 LINE DECODER OR 1-TO-8 LINE DEMULTIPLEXER

Inputs				Outputs							
Select			Strobe or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
IC	B	A	IG	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise/Fall Time (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	V_{CC}	Typ	Guaranteed Limits			Units
				T_A = 25°C	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	
V_{IH}	Minimum High Level Input Voltage				2.0	2.0	2.0	V
V_{IL}	Maximum High Level Input Voltage				0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\|$ = 20 μA		V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V			3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V			4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL}						
		$\|I_{OUT}\|$ = 20 μA			0.10	0.10	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V			0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V			0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND V_{IN} = V_{IH} or V_{IL}			±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0.0 μA (Note 4)			8	80	160	μA
		V_{IN} = 2.4V or 0.5V I_{OUT} = 0.0 μA (Note 4)						mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified, all voltages are referenced to ground.

Note 3: Power dissipation temperature deratings: plastic N package: −12 mW/°C from 65°C to 85°C; ceramic J package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input, other inputs at V_{CC} or GND.

4

AC Electrical Characteristics

V_{CC}, temperature and loading of LS-TTL; $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs A, B, or C2 to any Output		19	30	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs G1 or G2 to any Output		24	35	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Input C1 to any Output		25	35	ns

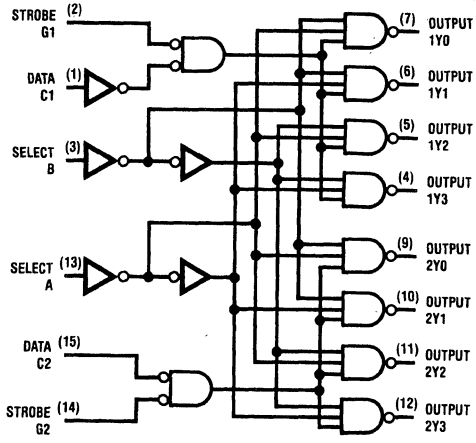
AC Electrical Characteristics

Full range of V_{CC} and temperature; $V_{CC}=5V\pm10\%$, $C_L=50$ pF unless otherwise specified

Symbol	Parameter	Conditions	Typ	Guaranteed Limits			Units
			T = 25°C	T = 25°C	74HCT T = −40°C to 85°C	54HCT T = −55°C to 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs A, B, or C2 to any Output		21	35	44	51	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Inputs G1 or G2 to any Output		26	40	50	60	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay from Input C1 to any Output		27	40	50	60	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance	Note 5					pF
C_{IN}	Minimum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

Logic Diagram



TL/F/5759–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT157/MM74HCT157 Quad 2-Input Multiplexer
MM54HCT158/MM74HCT158 Quad 2-Input Multiplexer (Inverted Output)

General Description

These high speed QUAD 2-to-1 line data selector/multiplexers utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 10 LS-TTL loads.

These devices each consist of four 2-input digital multiplexers with common select and STROBE inputs. On the MM54HCT157/MM74HCT157, when the STROBE input is at logical "0" the four outputs assume the values as selected from the inputs. When the STROBE input is at a logical "1" the outputs assume logical "0". The MM54HCT158/MM74HCT158 operates in the same manner, except that its outputs are inverted. Select decoding is done internally resulting in a single select input only. If enabled, the select input determines whether the A or B inputs get routed to their corresponding Y outputs.

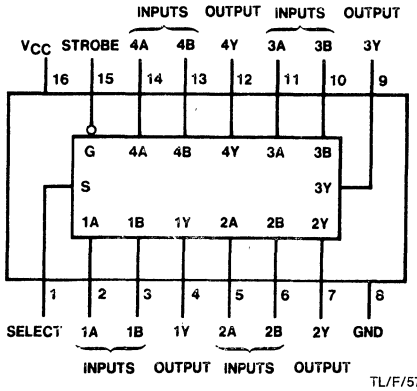
The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 14 ns data to any output
- Power supply range: 5V ± 10%
- Low power supply quiescent current: 80 μA maximum (74HCT Series)
- Fanout of 10 LS-TTL loads
- Low input current: 1 μA maximum
- Completely TTL compatible

Connection Diagrams

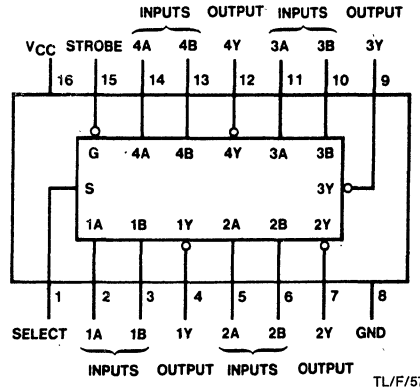
Dual-In-Line Package



TL/F/5741–1

Top View

Dual-In-Line Package



TL/F/5741–2

Top View

Order Number MM54HCT157J, MM54HCT158J, MM74HCT157J, N or MM74HCT158J, N
See NS Package J16A or N16E

Function Table

Inputs				Output Y	
Strobe	Select	A	B	HCT157	HCT158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage				2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage				0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$20 μA	4.5V		4.4	4.4	4.4	V
		V_{IN}=V_{IH} or V_{IL} $|I_{OUT}|\leq$4.0 mA $|I_{OUT}|\leq$4.8 mA	4.5V 5.5V	4.2 5.2	3.98 4.98	3.84 4.84	3.7 4.7	V V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL} $\|I_{OUT}\|$=20 μA $\|I_{OUT}\|$=4.0 mA $\|I_{OUT}\|$=4.8 mA	 4.5V 5.5V	0 0.2 0.2	0.1 0.26 0.26	0.1 0.33 0.33	0.1 0.4 0.4	V V V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA			8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)						mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HCT at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC}=5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output		14	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output		12	18	ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

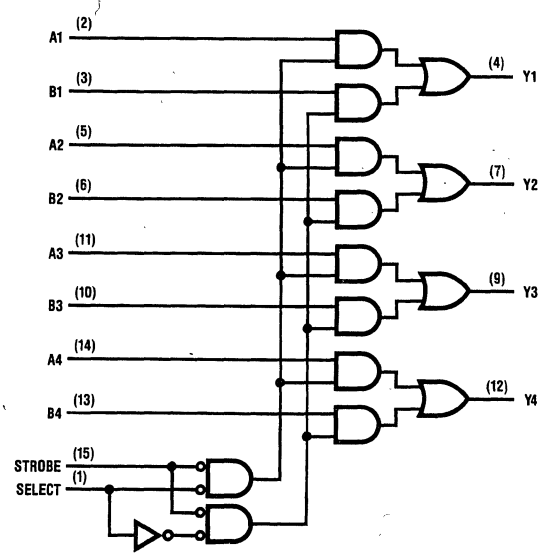
Symbol	Parameter	Conditions	V_{CC}	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$		54HCT $T_A=-55$ to $125°C$	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Output			13	25	32	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to Output			13	25	32	37	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Strobe to Output			12	23	29	34	ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time			8	15	19	22	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{PD}	Power Dissipation Capacitance (Note 5)							pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

4

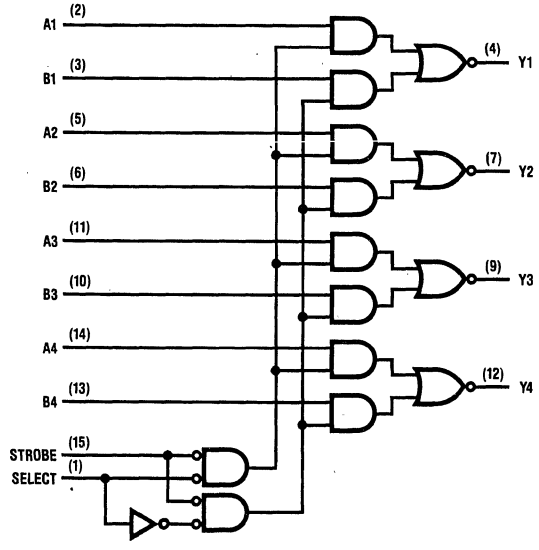
Logic Diagrams

'HCT157



TL/F/5741–3

'HCT158



TL/F/5741–4

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT164/MM74HCT164
8-Bit Serial-in/Parallel-out Shift Register

General Description

The MM54HCT164/MM74HCT164 utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS. It has the high noise immunity and low consumption of standard CMOS integrated circuits. It also offers speeds comparable to low power Schottky devices.

This 8-bit shift register has gated serial inputs and CLEAR. Each register bit is a D-type master/slave flip flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip flop to the low level at the next clock pulse. A high level on one input enables the other input which will then determine the state of the first flip flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the CLEAR input.

The 54HCT/74HCT logic family is functionally as well as pin-out compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

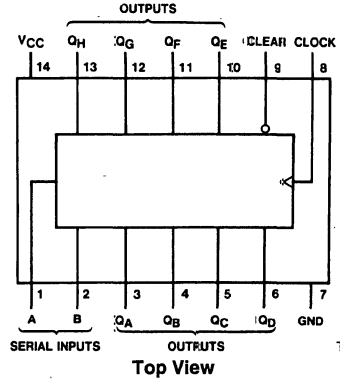
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 40 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- Fanout of 10 LS-TTL loads
- TTL input compatible

Connection Diagram

Dual-In-Line Package



Top View

Order Number MM54HCT164J or MM74HCT164J, N
See NS Package J14A or N14A

Truth Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L		L
H	L	X	X	Q_{AO}	Q_{BO}		Q_{HO}
H	↑	H	H	H	Q_{An}		Q_{Gn}
H	↑	L	X	L	Q_{An}		Q_{Gn}
H	↑	X	L	L	Q_{An}		Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

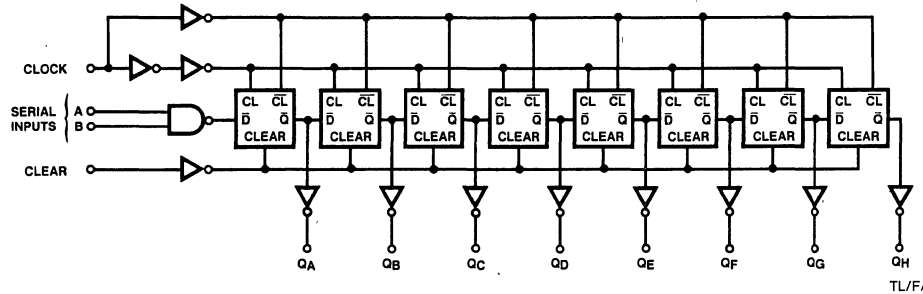
X = Irrelevant (any input, including transitions)

↑ = Transition from low to high level.

Q_{AO}, Q_{BO}, Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicated a one-bit shift.

Logic Diagram



Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=4.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=4.8 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND					
		I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: This is measured per pin. All other inputs are held at V_{CC} ground.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency from Clock to Q or $\overline{Q}$		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		20	32	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		24	36	ns
t_{REM}	Minimum Removal Time, Preset or Clear to Clock			20	ns
t_S	Minimum Set Up Time Data to Clock			20	ns
t_H	Minimum Hold Time Clock to Data		0	5	ns
t_W	Minimum Pulse Width Clock, Preset or Clear		10	18	ns

AC Electrical Characteristics V_{CC} = 5.0V ± 10%, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	21	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		23	37	46	54	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		27	41	51	61	ns
t_{REM}	Minimum Removal Time Clear to Clock			20	25	30	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data		0	5	0	0	ns
t_W	Minimum Pulse Width Clock, or Clear		10	18	22	27	ns
t_r, t_f	Maximum Input Rise and Fall Time			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(per flip-flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

4

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT191/MM74HCT191 Synchronous Binary Up/Down Counters with Mode Control

General Description

These high speed synchronous counters utilize microCMOS technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. These circuits are synchronous, reversible, up/down counters. The MM54HCT191/MM74HCT191 are 4-bit binary counters.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as divide by N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high speed operation.

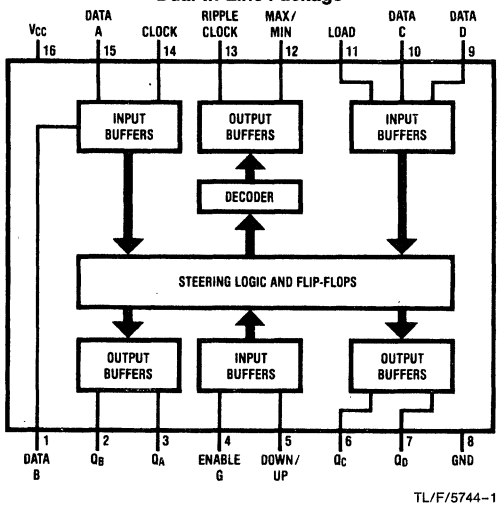
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices can be used to reduce power consumption in existing designs.

Features

- Level changes on Enable or Down/Up can be made regardless of the level of the clock.
- Low quiescent supply current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TL/F/5744–1

Truth Table

Load	Enable G	Down/ Up	Clock	Function
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Order Number MM54HCT191J or MM74HCT191J, N
See NS Package J16A or N16E

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to + 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to + 150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF unless otherwise specified

Symbol	Parameter	From Input	To Output	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Clock Frequency				40		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		30		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		27		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock		16		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		24		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		30		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		29		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		22		ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	Enable	Ripple Clock		22		ns
t_W	Minimum Clock or Load Input Pulse Width				10		ns
t_S	Minimum Set-Up Time	Data	Clock				ns
t_H	Minimum Hold Time	Clock	Data				ns
t_S	Minimum Set-Up Time	Down/Up	Clock				ns
t_H	Minimum Hold Time	Clock	Down/Up				ns
t_S	Minimum Set-Up Time	Enable	Clock				ns
t_H	Minimum Hold Time	Clock	Enable				ns
t_S	Minimum Set-Up Load Inactive to Clock						ns

AC Electrical Characteristics $V_{CC}=5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

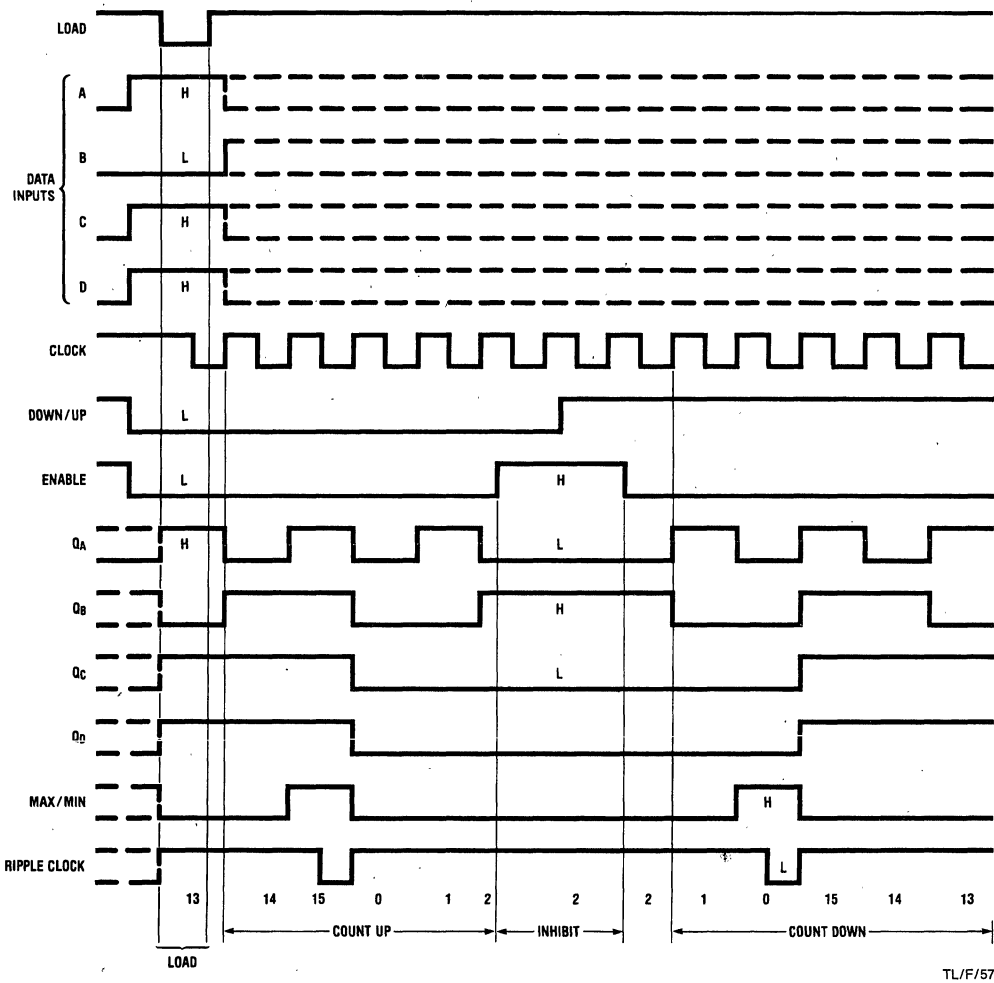
Symbol	Parameter	From Input	To Output	Conditions	$T_A=25°C$	74HCT $T_A=-40°C$ to $85°C$		54HCT $T_A=-55°C$ to $125°C$	Units
					Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency				38				MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		32				ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		28				ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock		18				ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		27				ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		33				ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		30				ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		25				ns
t_{PHL}, t_{PLH}	Propagation Delay Time	Enable	Ripple Clock		25				ns
t_W	Minimum Clock, or Load Input Pulse								ns
t_S	Minimum Set-Up Time	Data	Clock		10				ns
t_H	Minimum Hold Time	Clock	Data						ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time								ns
t_S	Minimum Set-Up Time	Down/Up	Clock						ns
t_H	Minimum Hold Time	Clock	Down/Up						ns
t_S	Minimum Set-Up Time	Enable	Clock						ns
t_H	Minimum Hold Time	Clock	Enable						ns
t_S	Minimum Set-Up Load Inactive to Clock								ns
t_r, t_f	Maximum Clock Input Rise and Fall Time								ns
C_{IN}	Input Capacitance				5				pF
C_{PD}	Power Dissipation Capacitance (Note 5)				100				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

4

Timing Diagram

HCT191 Synchronous Binary Counter Typical Load, Count, and Inhibit Sequence



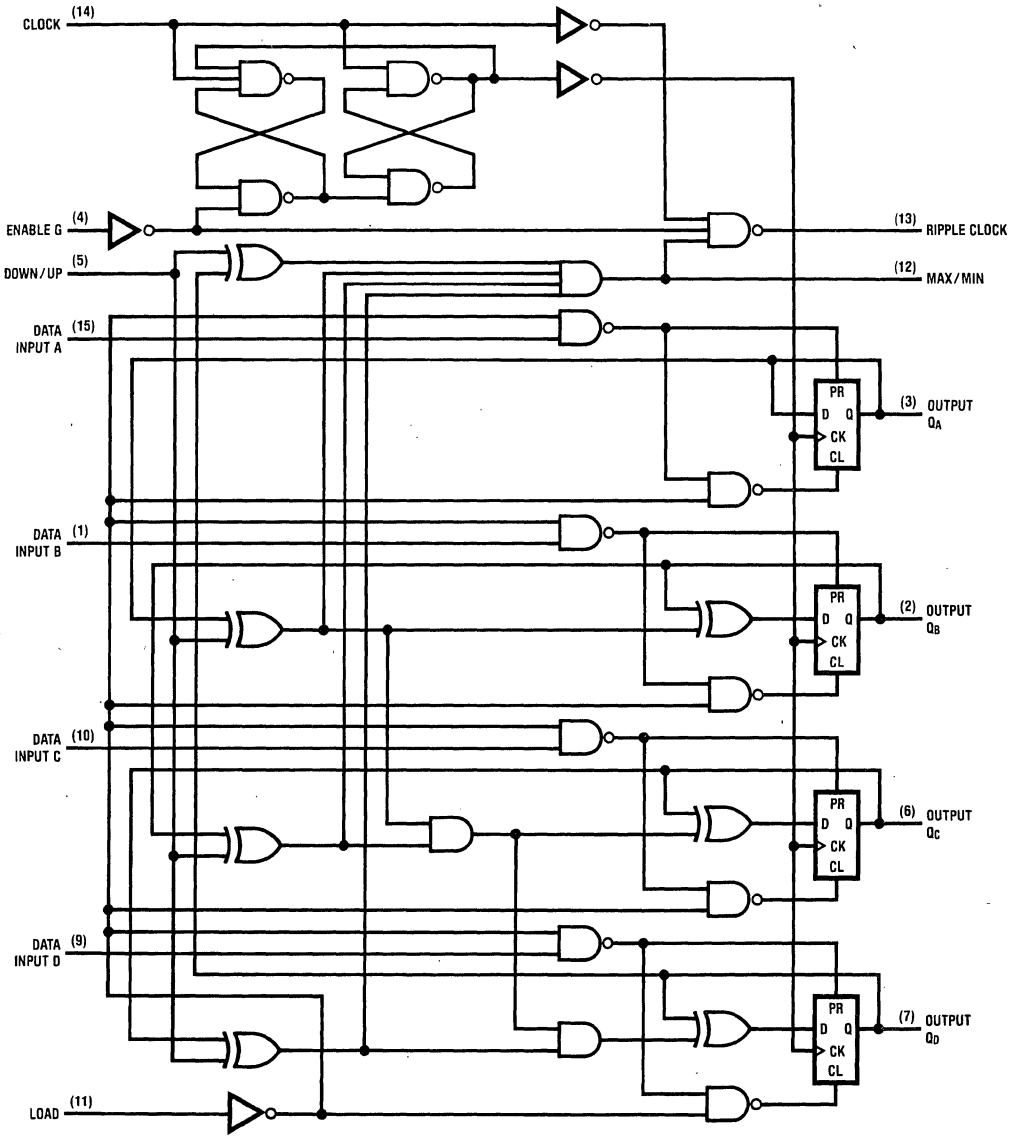
TL/F/5744–2

Sequence:

(1) Load (preset) to binary thirteen.
(2) Count up to fourteen, fifteen, zero, one, and two.
(3) Inhibit.
(4) Count down to one, zero, fifteen, fourteen, and thirteen.

Logic Diagram

HCT191



TL/F/5744–3

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT193/MM74HCT193 Synchronous Binary Up/Down Counters

General Description

These high speed synchronous counters utilize microCMOS technology, 3.0 micron silicon gate N-well CMOS to achieve the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. The MM54HCT193/MM74HCT193 is a binary counter having two separate clock inputs, an UP COUNT input and a DOWN COUNT input. All outputs of the flip-flops are simultaneously triggered on the low-to-high transition of either clock while the other input is held high. The direction of counting is determined by which input is clocked.

This device has TTL compatible inputs. It can drive 15 LS-TTL loads.

This counter may be preset by entering the desired data on the DATA A, DATA B, DATA C, and DATA D inputs. When the LOAD input is taken low, the data is loaded independently of either clock input. This feature allows the counter to be used as a divide-by-n counter by modifying the count length with the preset inputs.

In addition, the HCT191 can also be cleared. This is accomplished by inputting a high on the CLEAR input. All 4 internal stages are set to a low level independently of either COUNT input.

Both a BORROW and CARRY output are provided to enable cascading of both up and down counting functions. The BORROW output produces a negative-going pulse when the counter underflows and the CARRY outputs a pulse when the counter overflows. The counter can be cascaded by connecting the CARRY and BORROW outputs of one device to the COUNT UP and COUNT DOWN inputs, respectively, of the next device.

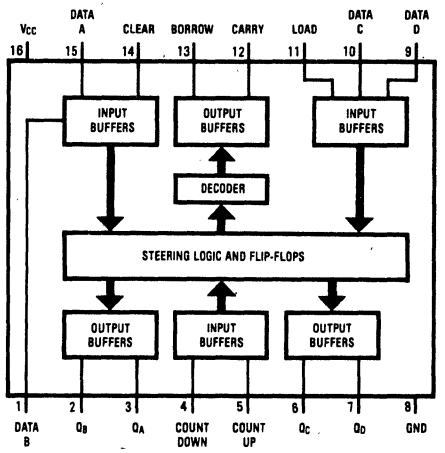
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Low quiescent supply current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TL/F/5742–1

Order Number MM54HCT193J or MM74HCT193J,N
See NS Package J16A or N16E

Truth Table

Count		Clear	Load	Function
Up	Down			
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Clear
X	X	L	L	Load

H = high level
L = low level
↑ = transition from low-to-high
X = don't care

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin(I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		4.0	40	80	μA
		V_{IN} = 2.4V or 0.5V (Note 4)	100				μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: − 12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics

(Note 6) V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency						MHz
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Load	QA, QB, QC, QD				ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Data A, B, C, D,	QA, QB, QC, QD				ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up or -Down	QA, QB, QC, QD				ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up	Carry				ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Dn	Borrow				ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Clear	QA, QB, QC, QD				ns
t_W	Width of Count, Clr, or Load Input Pulse						ns
t_S	Minimum Setup Time Data to Load-LH						ns
t_H	Minimum Hold Time Data after Load-LH						ns
t_S	Minimum Setup Time Load Inactive before Count LH transition						ns
t_S	Minimum Setup Time Clr Inactive before Count LH transition						ns
t_H	Minimum Hold Time Count-Up High after Count-Dn LH trans.						ns
t_H	Minimum Hold Time Count-Dn High after Count-Up LH trans.						ns
t_S	Minimum Setup Time Enable to Clock-LH						ns

AC Electrical Characteristics (Note 6)

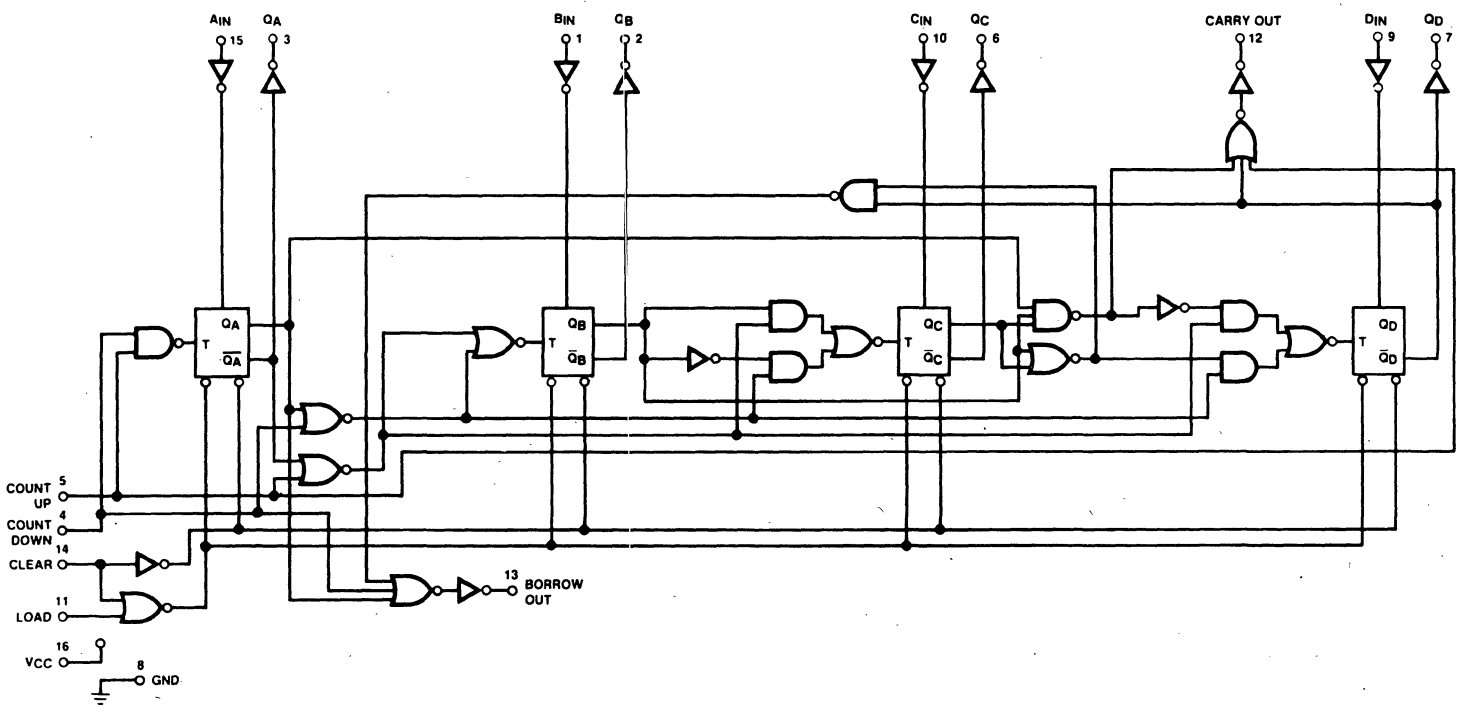
V_{CC} = 5V, ±10%, C_L = 50 pF (unless otherwise specified)

Symbol	Parameter	From (Input)	To (Output)	T = 25°C	T = 25°C	74HC T = −40° to 85°C	54HC T = −55° to 125°C	Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency							MHz
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Load	QA, QB, QC, QD					ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Data A	QA, QB, QC, QD					ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up or -Down	QA, QB QC, QD					ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Up	Carry					ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Count-Down	Borrow					ns
$t_{PLH, PHL}$	Maximum Propagation Delay Time	Clear	QA, QB QC, QD					ns
t_W	Width of Count, Clear, or Load Input Pulse							ns
t_S	Minimum Setup Time Data before Load-LH							ns
t_H	Minimum Hold Time Data after Load-LH							ns
t_S	Minimum Setup Time Load Inactive before Count LH transition							ns
t_S	Minimum Setup Time Clear Inactive before Count LH transition							ns
t_H	Minimum Hold Time Count-Up high after Count-Down LH transition							ns
t_H	Minimum Hold Time Count-Dn high after Count-Up LH transition							ns
$t_{TLH, THL}$	Output Rise or Fall Time							ns
$t_{r, f}$	Maximum Input Rise or Fall Time							ns
C_{PD}	Power Dissipation Capacitance							pF
C_{IN}	Minimum Input Capacitance							pF

Note 5: C_{PD} determines the no load dynamic power consumption, $C_{PD} * V_{CC}**2)*f + I_{CC}*V_{CC}$, and the no load dynamic current consumption, $I_s = C_{PD} * V_{CC}*f +$.

Note 6: Refer to Section 1 for Typical MM54/74HCT AC Switchforms and Test Circuits.

MM54HCT193/MM74HCT193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/5742–2

National Semiconductor

microCMOS

MM54HCT240/MM74HCT240 Inverting Octal TRI-STATE® Buffer
MM54HCT241/MM74HCT241 Octal TRI-STATE Buffer
MM54HCT244/MM74HCT244 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. All three devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM54HCT240/MM74HCT240 is an inverting buffer and the MM54HCT244/MM74HCT244 is a non-inverting buffer. Each device has two active low enables (1G and 2G), and each enable independently controls 4 buffers. MM54HCT241/MM74HCT241 is also a non-inverting buffer similar to the 244 except that the 241 has one active high enable, each again controlling 4 buffers.

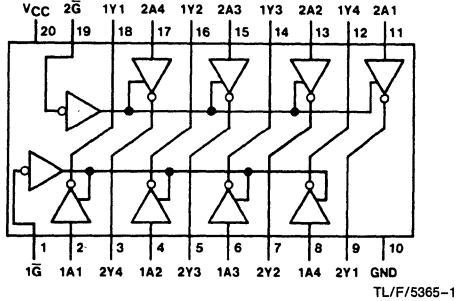
All inputs are protected from damage due to static discharge by diodes to V_{CC} and Ground.

Features

- TTL input compatible
- Typical propagation delay: 14 ns
- TRI-STATE outputs for connection to system buses
- Low quiescent current: 80 μA
- Output current: 6 mA

Connection Diagrams

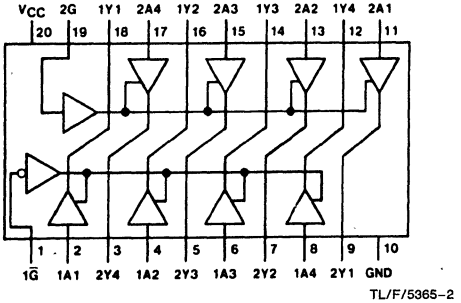
Dual-In-Line Packages



TL/F/5365–1

Top View

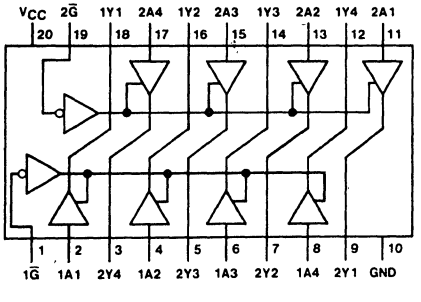
Order Number MM54HCT240J or MM74HCT240J, N



TL/F/5365–2

Top View

Order Number MM54HCT241J or MM74HCT241J, N



TL/F/5365–3

Top View

Order Number MM54HCT244J or MM74HCT244J, N
See NS Package J20A or N20A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN-EE} = VIH or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} −0.1	V_{CC} −0.1	V_{CC} −0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{iH} or V_{iL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, $\overline{G}$ = V_{IH}, G = V_{IL}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or GND.

Truth Tables

'HCT240

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Z	H	L	Z
H	H	Z	H	H	Z

'HCT241

$1\overline{G}$	1A	1Y	2G	2A	2Y
L	L	L	L	L	Z
L	H	H	L	H	Z
H	L	Z	H	L	L
H	H	Z	H	H	H

'HCT244

$1\overline{G}$	1A	1Y	$2\overline{G}$	2A	2Y
L	L	L	L	L	L
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = high level, L = low level, Z = high impedance

AC Electrical Characteristics MM54HCT240/MM74HCT240, MM54HCT241/MM74HCT241, MM54HCT244/MM74HCT244 V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	14	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kΩ	20	30	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	16	25	ns

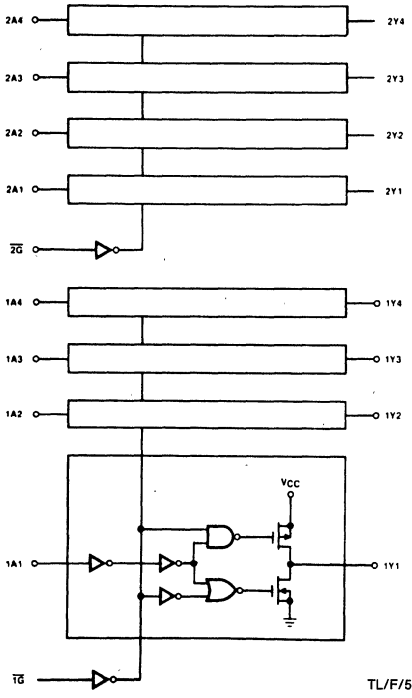
AC Electrical Characteristics MM54HCT240/MM74HCT240, MM54HCT241/MM74HCT241, MM54HCT244/MM74HCT244 V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C		54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		14	20	25	30	ns
		C_L = 150 pF		20	28	35	42	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ	C_L = 50 pF	21	30	38	45	ns
			C_L = 150 pF	26	42	53	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF		16	25	32	38	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per buffer) $\overline{G}$ = V_{CC}, G = GND $\overline{G}$ = GND, G = V_{CC}		5 90				pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

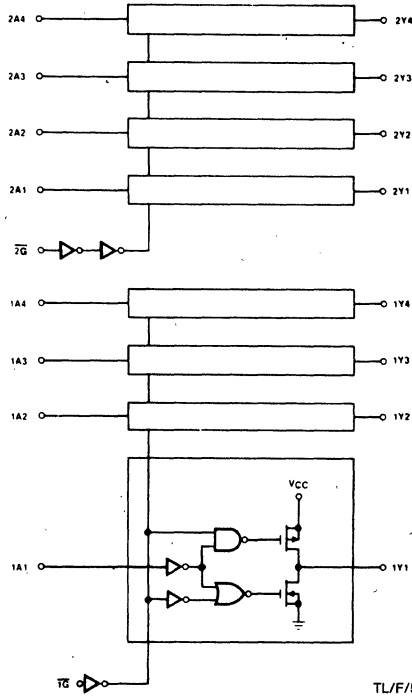
Logic Diagrams

'HCT240



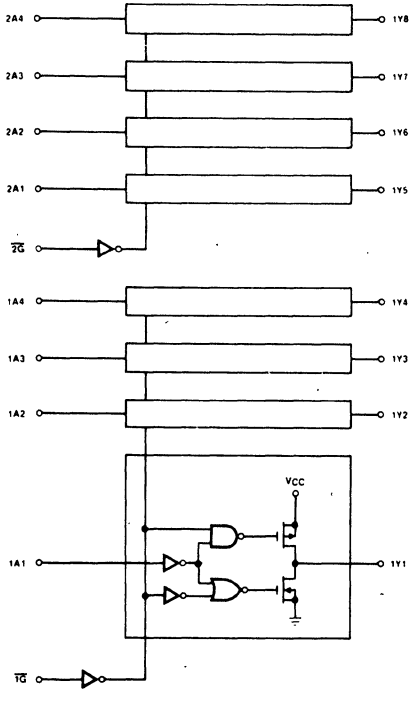
TL/F/5365-4

'HCT241



TL/F/5365-5

'HCT244



TL/F/5365-6

National Semiconductor

microCMOS

MM54HCT245/MM74HCT245 Octal TRI-STATE® Transceiver

General Description

This TRI-STATE bi-directional buffer utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and is intended for two-way asynchronous communication between data buses. It has high drive current outputs which enable high speed operation even when driving large bus capacitances. This circuit possesses the low power consumption of CMOS circuitry, yet has speeds comparable to low power Schottky TTL circuits.

This device is TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

MM54HCT245/MM74HCT245 has one active low enable input ($\overline{G}$), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A.

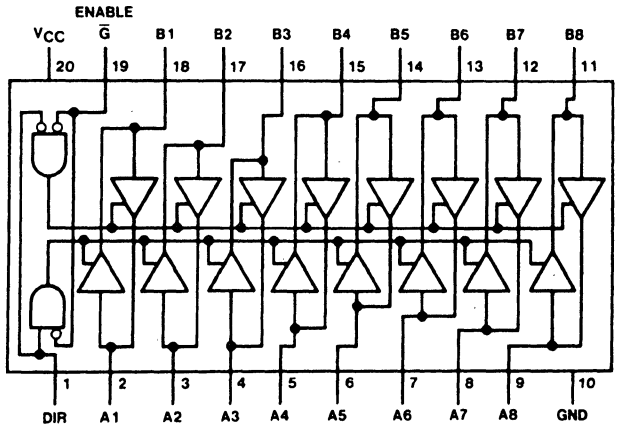
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input compatible
- Octal TRI-STATE outputs for μP bus applications: 6 mA, typ.
- High speed: 16 ns typical propagation delay
- Low power: 80 μA (74HCT Series)

Connection Diagram

Dual-In-Line Package



TL/F/5366–1

Top View

Order Number MM54HCT245J or MM74HCT245J, N
See NS Package J20A or N20A

Truth Table

Control Inputs		Operation
$\overline{G}$	DIR	245
L	L	B data to A bus
L	H	A data to B bus
H	X	isolation

H = high level L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC}=5V±10%, unless otherwise specified.)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or ground.

AC Electrical Characteristics MM54HCT245/MM74HCT245

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	20	25	ns

AC Electrical Characteristics MM54HCT245/MM74HCT245

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

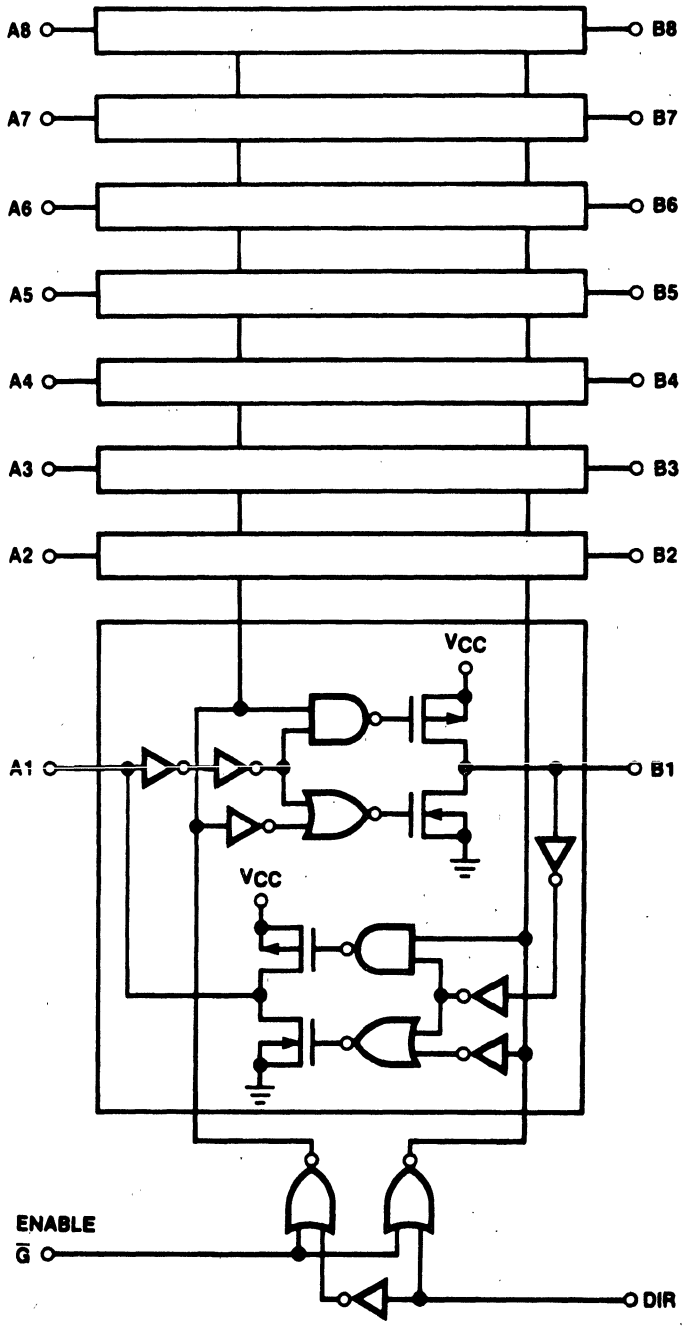
Symbol	Parameter	Conditions		T_A = 25°C		74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		17	23	29	34	ns
		C_L = 150 pF		24	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ	C_L = 50 pF	31	42	53	63	ns
			C_L = 150 pF	35	49	62	74	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF		21	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		8	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output/Input Capacitance			20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance	(Note 5) $\overline{G}$ = V_{CC} $\overline{G}$ = GND		7 100				pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

4

Logic Diagram

'HCT245



TL/F/5366–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT257/MM74HCT257
Quad 2-Channel TRI-STATE® Multiplexer

General Description

This quad 2-to-1 line date selector/multiplexer utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive LS-TTL loads. The large output drive capability coupled with the TRI-STATE feature make this device ideal for interfacing with bus lines in a bus organized system. When the OUTPUT CONTROL input line is taken high, the outputs of all four multiplexers are sent into a high impedance state. When the OUTPUT CONTROL line is low, the SELECT input chooses whether the A or B input is used.

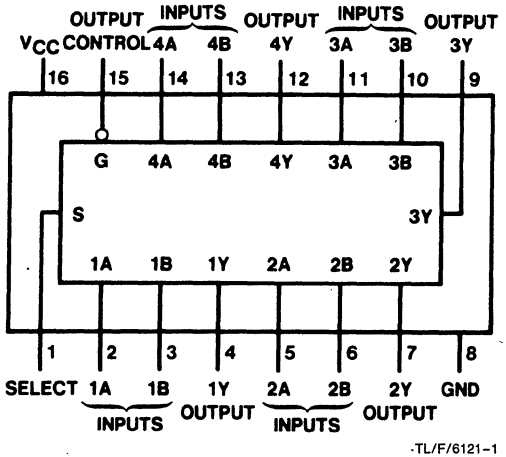
The 54HCT/74HCT logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 12 ns
- Wide power supply range: 2V–6V
- Low quiescent current: 80 μA maximum (74HCT Series)
- TRI-STATE outputs for connection to system buses
- Completely TTL compatible

Connection and Logic Diagrams

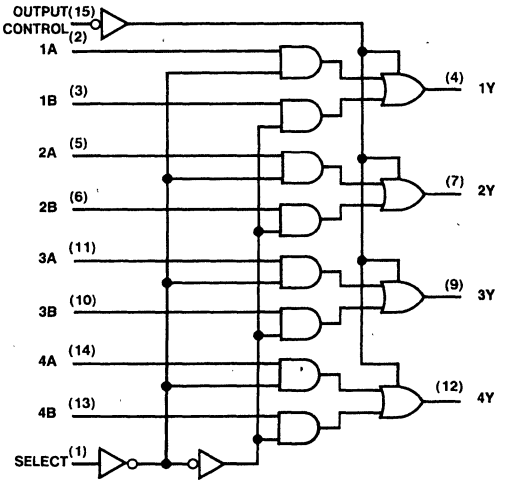
Dual-In-Line Package



TL/F/6121–1

Top View

Order Number MM54HCT257J or MM74HCT257J, N
See NS Package J16A or N16E



TL/F/6121–2

Truth Table

Inputs				
Output Control	Select	A	B	Output Y
H	X	X	X	Z
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant, Z = high impedance, (off)

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f) V_{CC} = 4.5V		500	ns

DC Electrical Characteristics (Note 4) V_{CC} = 5V ±10%

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			3.15	3.15	3.15	V
V_{IL}	Maximum Low Level Input Voltage			0.9	0.9	0.9	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	4.5	4.4	4.4	4.4	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA, V_{CC} = 4.5V $\|I_{OUT}\| \le 7.8$ mA, V_{CC} = 5.5V	4.2 5.2	3.98 4.98	3.84 4.84	3.7 4.7	V
V_{OL}	Maximum Low Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 20\ \mu A$	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH} or V_{IL} $\|I_{OUT}\| \le 6.0$ mA, V_{CC} = 4.5V $\|I_{OUT}\| \le 7.8$ mA, V_{CC} = 5.5V	0.2 0.2	0.26 0.26	0.33 0.33	0.4 0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage	V_{OUT} = V_{CC} or GND OC = V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=45$ pF, $t_r=t_f=6$ ns (unless otherwise noted.)

Symbol	Parameter	Condition	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Select to any Output		19	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay A or B to any Output		24	38	ns
t_{PZH}, t_{PZL}	Maximum Enable Time	$R_L = 1\ k\Omega$	20	30	ns
t_{PHZ}, t_{PLZ}	Maximum 1	$R_L = 1\ k\Omega$ $C_L = 5$ pF	15	25	

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF (unless otherwise noted.)

Symbol	Parameter	Condition	$T_A=25°C$	74HCT $T_A=-40°C$ to $85°C$		54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Select to any Output		12	20	25	30	ns
		$C_L = 150$ pF	12	30	38	45	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, A or B to any Output		12	20	25	30	ns
		$C_L = 150$ pF	12	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Enable to any Output		21	30	38	35	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Time		15	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		9	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)						pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

4

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT273/MM74HCT273 Octal D Flip-Flop with Clear

General Description

The MM54HCT273/MM74HCT273 utilizes 3.0 micron N-well microCMOS technology. It has an input threshold and output drive similar to LS-TTL with the low standby power of CMOS.

These positive edge-triggered flip-flops have a common clock and clear-independent Q outputs. Data on a D input, having the specified set-up and hold time, is transferred to the corresponding Q output on the positive-going transition of the clock pulse. The asynchronous clear forces all outputs low when it is low.

All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

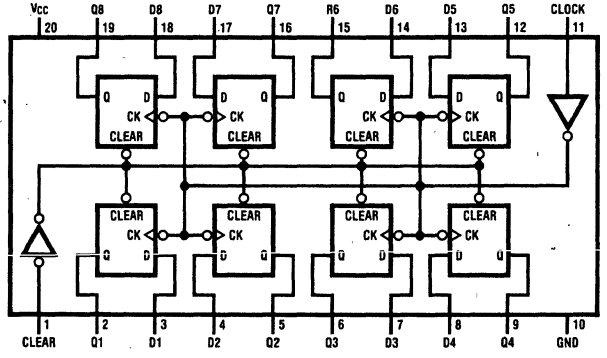
MM54HCT/MM74HCT devices are intended to interface TTL and NMOS components to CMOS components. These parts can be used as plug-in replacements to reduce system power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT series)
- Fanout of 10 LS-TTL loads

Connection Diagram

Dual-In-Line Package

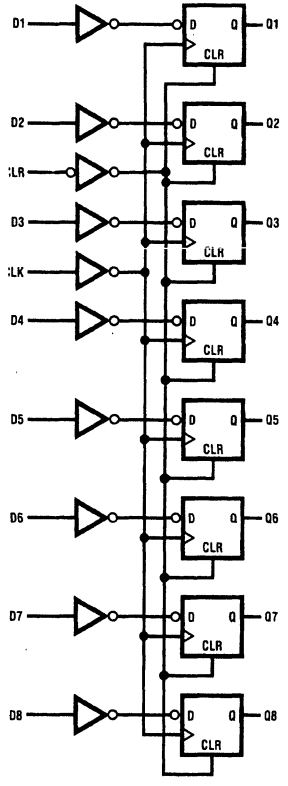


TL/F/5760–1

Top View

Order Number MM54HCT273J or MM74HCT273J, N
See NS Package J20A or N20A

Logic Diagram



TL/F/5760–2

Truth Table (Each Flip-Flop)

Inputs			Outputs
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q0

H = high level (steady-state)
L = low level (steady-state)
X = don't care
↑ = transition from low to high level
Q0 = the level of Q before the indicated steady-state input conditions were established.

Absolute Maximum Ratings (Notes 1 and 2)

Supply Voltage (V_{CC})	−0.5V to + 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to + 150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40°C to 85°C	54HCT T_A=−55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Minimum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics V_{CC} = 5V, T_A = 25°C, C_L = 15 pF, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Operating Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		18	30	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		18	30	ns
t_{REM}	Minimum Removal Time, Clear to Clock			20	ns
t_S	Minimum Set-Up Time D to Clock		10	20	ns
t_H	Minimum Hold Time Clock to D		−3	5	ns
t_W	Minimum Pulse Width Clock or Clear		8	16	ns

AC Electrical Characteristics V_{CC} = 5.0V ± 10%, C_L = 50 pF, $t_r = t_f$ = 6 ns unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Operating Frequency			27	22	18	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clock to Q		22	35	44	52	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from Clear to Q		22	35	44	52	ns
t_{REM}	Minimum Removal Time Clear to Clock			20	25	30	ns
t_S	Minimum Set-Up Time D to Clock		10	20	25	30	ns
t_H	Minimum Hold Time Clock to D		−3	5	5	5	ns
t_W	Minimum Pulse Width Clock or Clear			16	20	24	ns
t_r, t_f	Maximum Input Rise and Fall Time, Clock			500	500	500	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time			15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)	(Per Flip-Flop)					pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC}^2 f + I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT299/MM74HCT299
8-Bit TRI-STATE® Universal Shift Register

General Description

This 8-bit TRI-STATE shift/storage register utilizes micro-CMOS technology, 3.0 micron silicon gate N-well CMOS. Along with the low power consumption and high noise immunity of standard CMOS integrated circuits, it has the ability to drive 15 LS-TTL loads. This circuit also features operating speeds comparable to the equivalent low power Schottky device.

The MM54HCT299/MM74HCT299 is TTL input compatible. It features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus oriented system.

Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines, S0 and S1, high. This places the TRI-STATE outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A direct overriding CLEAR input is provided to clear the register whether the outputs are enabled or disabled.

The MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These devices are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

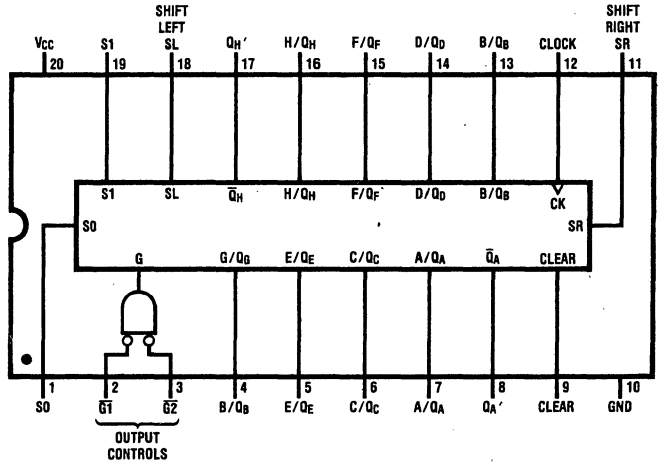
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TRI-STATE I/O
- Output drive capability: 15 LS-TTL loads
- Cascadable for n-bit word lengths
- Clock-independent clear

Connection Diagram

Dual-In-Line Package



TL/F/5746–1

Order Number MM54HCT299J or MM74HCT299J, N
See NS Package J20A or N20A

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{EO}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{EO}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both controls are high, the eight input/output terminals are disabled to the high impedance state; however, sequential operation or clearing of the register is not affected.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT323/MM74HCT323
8-Bit TRI-STATE® Universal Shift Register

General Description

This 8-bit TRI-STATE shift/storage register utilizes micro-CMOS technology, 3.0 micron silicon gate N-well CMOS. Along with the low power consumption and high noise immunity of standard CMOS integrated circuits, it has the ability to drive 15 LS-TTL loads. This circuit also features operating speeds comparable to the equivalent low power Schottky device.

The MM54HCT323/MM74HCT323 is TTL input compatible. It features multiplexed inputs/outputs to achieve full 8-bit data handling in a single 20-pin package. Due to the large output drive capability and TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus oriented system.

Two function select inputs and two output control inputs are used to choose the mode of operation as listed in the function table. Synchronous parallel loading is accomplished by taking both function select lines, S0 and S1, high. This places the TRI-STATE outputs in a high impedance state, which permits data applied to the input/output lines to be clocked into the register. Reading out of the register can be done while the outputs are enabled in any mode. A synchronous CLEAR input is provided to clear the register whether the outputs are enabled or disabled.

The MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These devices are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

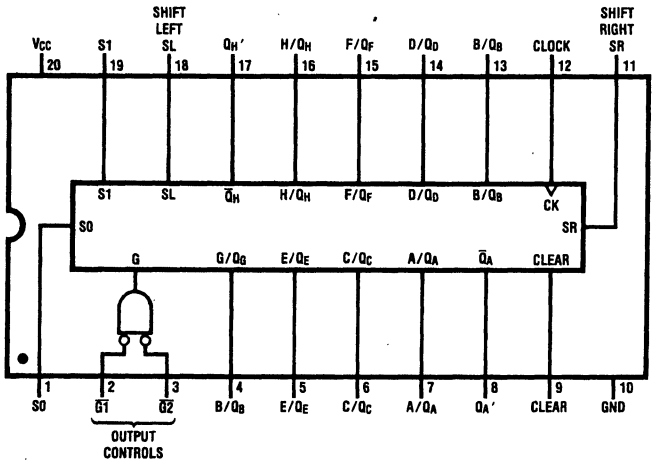
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TRI-STATE I/O
- Output drive capability: 15 LS-TTL loads
- Cascadable for n-bit word lengths
- Synchronous clear

Connection Diagram

Dual-In-Line Package



TL/F/5745–1

Order Number MM54HCT323J or MM74HCT323J,N
See NS Package J20A or N20A

Function Table

Mode	Inputs							Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial	A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL SR										
Clear	L	X	L	L	L	↑	X X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	↑	X X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{EO}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{EO}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{GN}
	H	L	H	L	L	↑	X L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{GN}
Shift Left	H	H	L	L	L	↑	H X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X X	a	b	c	d	e	f	g	h	a	h

† When one or both controls are high, the eight input/output terminals are disabled to the high impedance state; however, sequential operation or clearing of the register is not affected.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT373/MM74HCT373 TRI-STATE® Octal D-Type Latch MM54HCT374/MM74HCT374 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54HCT373/MM74HCT373 octal D-type latches and MM54HCT374/MM74HCT374 Octal D-type flip flops utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pin-out compatible. The TRI-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM54HCT373/MM74HCT373 LATCH ENABLE input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54HCT374/MM74HCT374 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

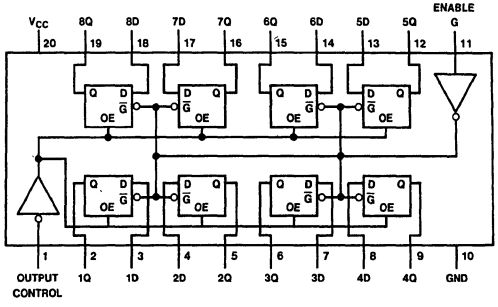
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 20 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

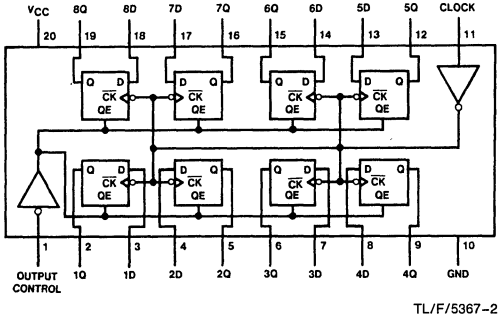
Connection Diagram

Dual-In-Line Package



TL/F/5367–1

Top View



TL/F/5367–2

Top View

Order Number MM54HCT373J, MM54HCT374J, MM74HCT373J, N, or MM74HCT374J, N
See NS Package J20A or N20A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable=V_{IH} or VIL		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)		1.0	1.3	1.5	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT373/MM74HCT373

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical Characteristics MM54HCT373/MM74HCT373

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$		74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=50$ pF $C_L=150$ pF	22 30	30 40	37 50	45 60	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=50$ pF $C_L=150$ pF	25 32	35 45	44 56	53 68	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			5	6	8	ns
t_H	Minimum Hold Time Clock to Data			10	13	20	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	$G=V_{CC}$ $G=GND$					pF pF

Truth Table

'373

Output Control	LE	Data	373 Output	573 Output
L	H	H	H	L
L	H	L	L	H
L	L	X	Q_0	$\overline{Q0}$
H	X	X	Z	Z

H = high level, L = low level

Q_0 = level of output before steady-state input conditions were established.

Z = high impedance

'374

Output Control	Clock	Data	Output (374)	Output (534)
L	↑	H	H	L
L	↑	L	L	H
L	L	X	Q_0	$\overline{Q_0}$
H	X	X	Z	Z

H = High Level, L = Low Level

X = Don't Care

↑ = Transition from low-to-high

Z = High impedance state

Q_0 = The level of the output before steady state input conditions were established.

AC Electrical Characteristics MM54HCT374/MM74HCT374

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=45$ pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

AC Electrical Characteristics MM54HCT374/MM74HCT374

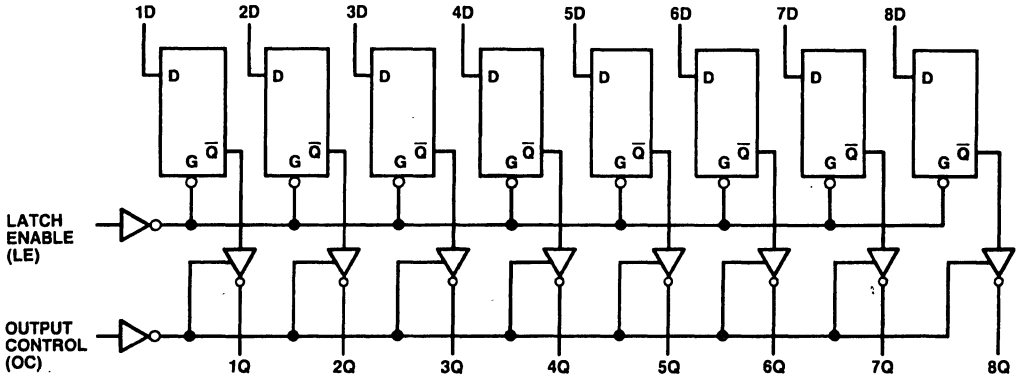
$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency			30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	$C_L=50$ pF	22	36	45	48	ns
		$C_L=150$ pF	30	46	57	69	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF	21	30	37	45	ns
		$C_L=150$ pF $R_L=1$ kΩ	30	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data			5	5	5	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	G = V_{CC}					pF
		G = GND					pF

Note 5: C_{PD} determines the no load power consumption, $P_D=C_{PD}\ V_{CC}^2\ f+I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\ V_{CC}\ f+I_{CC}$.

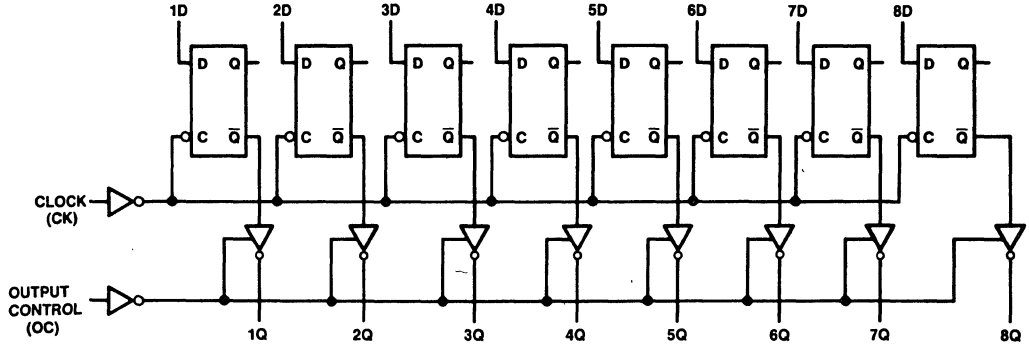
Logic Diagrams

MM54HCT373/MM74HCT373



TL/F/5367–4

MM54HCT374/MM74HCT374



TL/F/5367–5

National Semiconductor

microCMOS

MM54HCT521/MM74HCT521 8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS to compare bit for bit two 8-bit words and indicate whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

The comparator combines the low power consumption of CMOS, but inputs are compatible with TTL logic levels, and the output can drive 10 low power Schottky equivalent loads.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

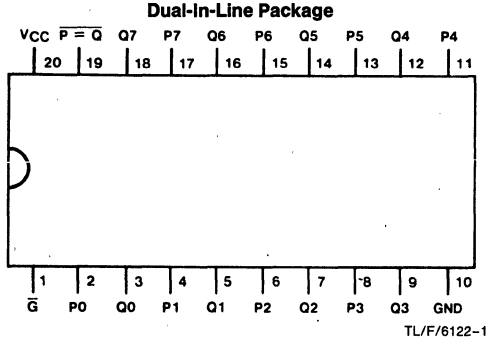
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Large output current: 4 mA

Connection and Logic Diagrams

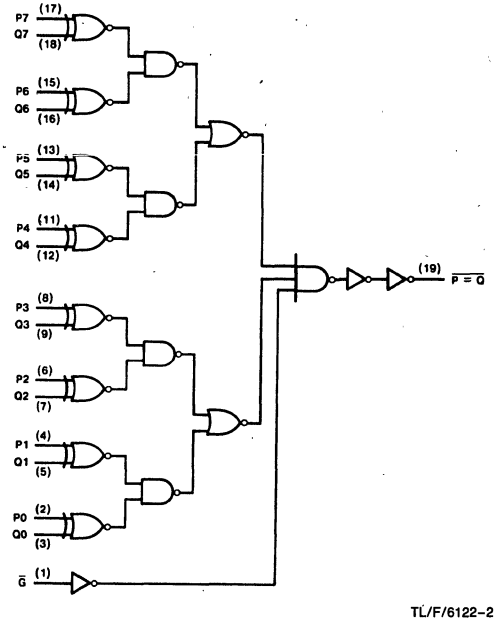
Dual-In-Line Package



TL/F/6122–1

Top View

Order Number MM54HCT521J or MM74HCT521J, N
See NS Package J20A or N20A



TL/F/6122–2

Truth Table

Inputs		$\overline{P=Q}$
Data P, Q	Enable $\overline{G}$	
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT688	−40	+85	°C
MM54HCT688	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = 0.8V or 2.0V					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V0.8V or 2.0V					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.4V (Note 4)	0.5				mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay - P or Q to Output		19	30	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		13	22	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		13	20	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		10	18	ns

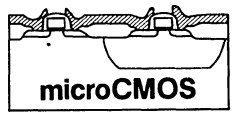
AC Electrical Characteristics $V_{CC}=5V \pm 10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$	54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits		
t_{PHL}	Maximum Propagation Delay - P or Q to Output		23	35	44	53	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		16	24	30	36	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		16	24	30	36	ns
t_{PLH}	Maximum Propagation Delay - Enable to Output		11	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)		45				pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}+I_{CC}$.

National Semiconductor

PRELIMINARY



MM54HCT533/MM74HCT533 TRI-STATE® Octal D-Type Latch MM54HCT534/MM74HCT534 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54HCT533/MM74HCT533 octal D-type latches and MM54HCT534/MM74HCT534 Octal D-type flip-flops utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, which provides the inherent benefits of low power consumption and wide power supply range, but are LS-TTL input and output characteristic & pin-out compatible. The TRI-STATE outputs are capable of driving 15 LS-TTL loads. All inputs are protected from damage due to static discharge by internal diodes to V_{CC} and ground.

When the MM54HCT533/MM74HCT533 LATCH ENABLE input is high, the $\overline{Q}$ outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54HCT534/MM74HCT534 are positive edge triggered flip-flops. Data at the D inputs, meeting the setup and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input characteristic compatible
- Typical propagation delay: 18 ns
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

4

Truth Tables

'HCT533

Output Control	Latch Enable G	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

'HCT534

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level

X = Don't Care

↑ = Transition from low-to-high

Z = High impedance state

$\overline{Q}_0$ = The level of the output before steady state Input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{iH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND Enable = V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT533/MM74HCT533

$V_{CC}=5.0V$, $t_r=t_f=6$ ns, $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=45$ pF	18	25	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=45$ pF	21	30	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=45$ pF $R_L=1$ kΩ	20	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=5$ pF $R_L=1$ kΩ	18	25	ns
t_W	Minimum Clock Pulse Width			16	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			10	ns

AC Electrical Characteristics MM54HCT533/MM74HCT533

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Output	$C_L=50$ pF $C_L=150$ pF	22 30	30 40	37 50	45 60	ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to Output	$C_L=50$ pF $C_L=150$ pF	25 32	35 45	44 56	53 68	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	$C_L=50$ pF $R_L=1$ kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			5	6	8	ns
t_H	Minimum Hold Time Clock to Data			10	13	20	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	$G=V_{CC}$ $G=GND$					pF pF

4

AC Electrical Characteristics MM54HCT534/MM74HCT534

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	C_L = 45 pF	20	32	ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 45 pF R_L = 1 kΩ	19	28	ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 5 pF R_L = 1 kΩ	17	25	ns
t_W	Minimum Clock Pulse Width			20	ns
t_S	Minimum Setup Time Data to Clock			5	ns
t_H	Minimum Hold Time Clock to Data			16	ns

AC Electrical Characteristics MM54HCT534/MM74HCT534

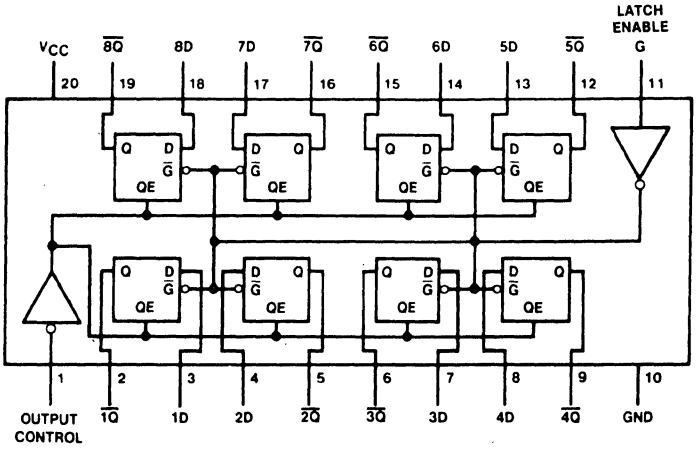
V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency			30	24	20	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay to Output	C_L = 50 pF C_L = 150 pF	22 30	36 46	45 57	48 69	ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Control to Output	C_L = 50 pF C_L = 150 pF R_L = 1 kΩ	21 30	30 40	37 50	45 60	ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Control to Output	C_L = 50 pF R_L = 1 kΩ	21	30	37	45	ns
t_W	Minimum Clock Pulse Width			16	20	24	ns
t_S	Minimum Setup Time Data to Clock			20	25	30	ns
t_H	Minimum Hold Time Clock to Data			5	5	5	ns
C_{IN}	Maximum Input Capacitance			10	10	10	pF
C_{OUT}	Maximum Output Capacitance			20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	G = V_{CC} G = GND					pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Connection Diagram

Dual-In-Line Package

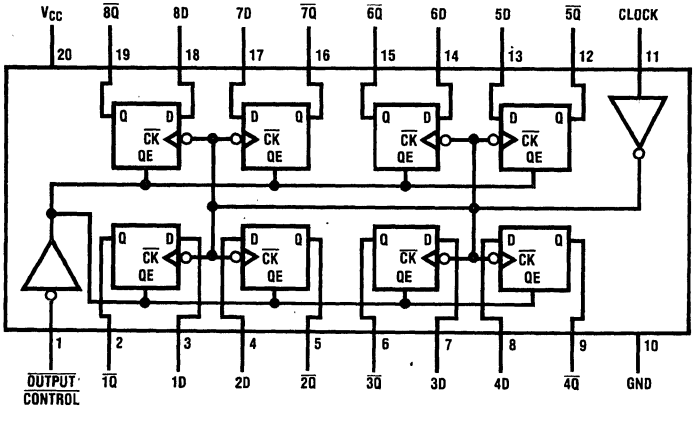


TL/F/6123–1

Top View

Order Number MM54HCT533J or MM74HCT533J, N
See NS Package J20A or N20A

Dual-In-Line Package



TL/F/6123–2

Top View

Order Number MM54HCT534J or MM74HCT534J, N
See NS Package J20A or N20A

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT540/MM74HCT540 Inverting Octal TRI-STATE® Buffer MM54HCT541/MM74HCT541 Octal TRI-STATE Buffer

General Description

These TRI-STATE buffers utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and are general purpose high speed inverting and non-inverting buffers. They possess high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the low power consumption of CMOS. Both devices are TTL input compatible and have a fanout of 15 LS-TTL equivalent inputs.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

The MM54HCT540/MM74HCT540 is an inverting buffer and the MM54HCT541/MM74HCT541 is a non-inverting buffer. The TRI-STATE control gate operates as a two-input NOR such that if either $\overline{G1}$ or $\overline{G2}$ are high, all eight outputs are in the high-impedance state.

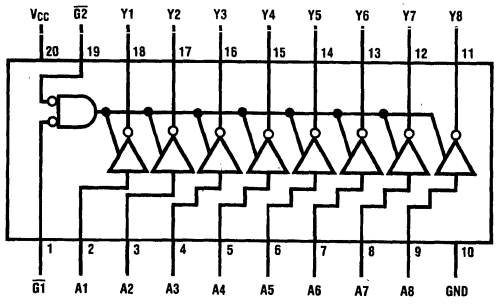
In order to enhance PC board layout, the 'HCT540 and 'HCT541 offers a pinout having inputs and outputs on opposite sides of the package. All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delay: 12 ns
- TRI-STATE outputs for connection to system buses
- Low quiescent current: 80 μA
- Output current: 6 mA

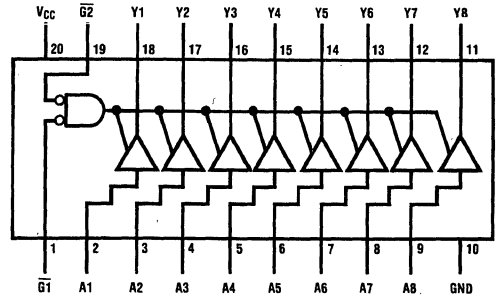
Connection Diagrams

Dual-In-Line Package



TL/F/6040–1

Top View



TL/F/6040–2

Top View

Order Number MM54HCT540J, MM54HCT541J, MM74HCT540J, N or MM74HCT541J, N
See NS Package J20A or N20A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND $\overline{G}$=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.4V (Note 4)	0.6	1.0	1.3	1.5	nA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs at V_{CC} or GND.

AC Electrical Characteristics MM54HCT540/MM74HCT540

V_{CC}=5.0V, t_r=t_f=6 ns, T_A=25°C, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L=45 pF	12	18	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L=45 pF R_L=1 kΩ	14	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L=5 pF R_L=1 kΩ	13	25	ns

AC Electrical Characteristics MM54HCT540/MM74HCT540

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		12	20	25	30	ns
		C_L = 150 pF		22	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ	C_L = 50 pF	15	30	38	45	ns
			C_L = 150 pF	20	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF		15	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}$ = V_{CC} $\overline{G}$ = GND	12 50				pF pF

AC Electrical Characteristics MM54HCT541/MM74HCT541

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C, (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	13	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kΩ	17	28	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	15	25	ns

AC Electrical Characteristics MM54HCT541/MM74HCT541

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		14	23	29	34	ns
		C_L = 150 pF		17	33	42	49	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ	C_L = 50 pF	17	30	38	45	ns
			C_L = 150 pF	22	40	50	60	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF		17	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		6	12	15	18	ns
C_{IN}	Maximum Input Capacitance			5	10	10	10	pF
C_{OUT}	Maximum Output Capacitance			15	20	20	20	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G}$ = V_{CC} $\overline{G}$ = GND	12 45				pF pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT563/MM74HCT563 TRI-STATE® Octal D-Type Latch with Inverted Outputs

General Description

These high speed octal D-type latches utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE (LE) input is high, the $\overline{Q}$ outputs will follow the inversion of the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

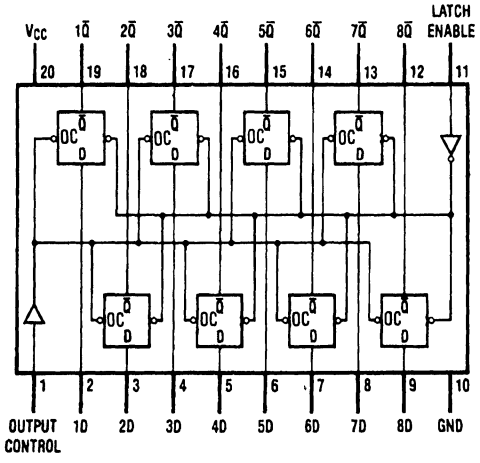
The 54HCT/74HCT logic family is speed, function and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- TTL input characteristic compatible
- Functionally compatible with 54/74LS580

Connection Diagram

Dual-In-Line Package



TL/F/6041–1

Order Number MM54HCT563J or MM74HCT563J,N
See NS Package J20A or N20A

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established
Z = high impedance
X = don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND OC = V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.4V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT563/MM74HCT563

$V_{CC}=5.0V$, $t_r=t_f=6$ ns $T_A=25°C$ (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to $\overline{Q}$	$C_L=45$ pF			ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to $\overline{Q}$	$C_L=45$ pF			ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$C_L=45$ pF $R_L=1$ kΩ			ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$C_L=5$ pF $R_L=1$ kΩ			ns
t_W	Minimum Pulse Width LE or Data				ns
t_S	Minimum Setup Time Data to LE				ns
t_H	Minimum Hold Time LE to Data				ns

AC Electrical Characteristics MM54HCT563/MM74HCT563

$V_{CC}=5.0V \pm 10\%$, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C		Units
			Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to $\overline{Q}$	$C_L=50$ pF $C_L=150$ pF	22 30				ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Latch Enable to $\overline{Q}$	$C_L=50$ pF $C_L=150$ pF	25 32				ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$C_L=50$ pF $C_L=150$ pF $R_L=1$ kΩ	21 30				ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$C_L=50$ pF $R_L=1$ kΩ	21				ns
t_W	Minimum Pulse Width LE or Data						ns
t_S	Minimum Setup Time Data to LE						ns
t_H	Minimum Hold Time LE to Data						ns
C_{IN}	Maximum Input Capacitance						pF
C_{OUT}	Maximum Output Capacitance						pF
C_{PD}	Power Dissipation Capacitance (Note 5)	OC=V_{CC} OC=GND					pF pF

4

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT564/MM74HCT564 TRI-STATE® Octal D-Type Flip-Flop with Inverted Outputs

General Description

These octal D-type flip-flops utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the $\overline{Q}$ outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

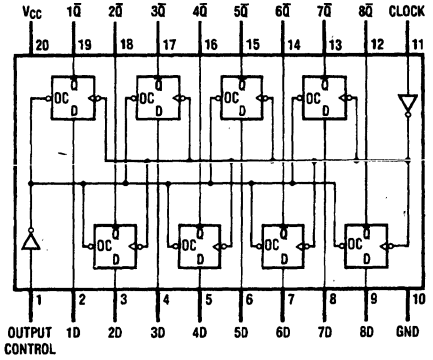
The 54HCT/74HCT logic family is speed, function, and pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum (74 Series)
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads
- TTL input characteristic compatible
- Functionally compatible with 54LS576/74LS576

Connection Diagram

Dual-In-Line Package



TL/F/6042–1

Top View

Order Number MM54HCT564J or MM74HCT564J, N
See NS Package J20A or N20A

Truth Table

Output Control	Clock	Data	Output
L	↑	H	L
L	↑	L	H
L	L	X	$\overline{Q}_0$
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High Impedance State
Q_0 = The level of the output before steady state Input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IA} or V_{IH}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND OC=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics MM54HCT564/MM74HCT564

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Clock Frequency		50		MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to $\overline{Q}$	C_L = 45 pF	20		ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Delay Output Enable Time	C_L = 45 pF R_L = 1 kΩ	19		ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Delay Output Disable Time	C_L = 5 pF R_L = 1 kΩ	17		ns
t_W	Minimum Clock Pulse Width				ns
t_S	Minimum Setup Time Data to Clock				ns
t_H	Minimum Hold Time Clock to Data				ns

AC Electrical Characteristics MM54HCT564/MM74HCT564

V_{CC} = 5.0V ±10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
f_{MAX}	Maximum Clock Frequency					MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay Clock to $\overline{Q}$	C_L = 50 pF C_L = 150 pF	22 30			ns ns
t_{PZH}, t_{PZL}	Maximum Enable Propagation Output Enable Time	C_L = 50 pF C_L = 150 pF R_L = 1 kΩ	21 30			ns ns
t_{PHZ}, t_{PLZ}	Maximum Disable Propagation Output Disable Time	C_L = 50 pF R_L = 1 kΩ	21			ns
t_W	Minimum Clock Pulse Width					ns
t_S	Minimum Setup Time Data to Clock					ns
t_H	Minimum Hold Time Clock to Data					ns
t_r, t_f	Maximum Clock Input Rise and Fall Time					ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF				ns
C_{IN}	Maximum Input Capacitance					pF
C_{OUT}	Maximum Output Capacitance					pF
C_{PD}	Power Dissipation Capacitance (Note 5)	OC = V_{CC} OC = GND				pF pF

Note 5: C_{PD} determines the no load power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT573/MM74HCT573 TRI-STATE® Octal D-Type Latch

General Description

These high speed octal D-type latches utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE(LE) input is high, the Q outputs will follow the D inputs. When the LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

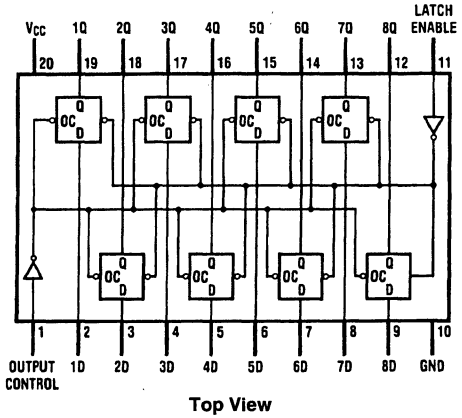
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input characteristic compatible
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/6126–1

Top View
Order Number MM54HCT573J or MM74HCT573J, N
See NS Package J20A or N20A

Truth Table

Output Control	Latch Enable	Data	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = high level, L = low level
Q_0 = level of output before steady-state input conditions were established.
Z = high impedance
X = Don't care

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temp. (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics

V_{CC} = 5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 6.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 7.2 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT} = V_{CC} or GND, OC = V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Data to Q	$C_L=45$ pF	12		ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, LE to Q	$C_L=45$ pF	12		ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13		ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11		ns
t_S	Minimum Setup Time Data to LE		10		ns
t_H	Minimum Hold Time LE to Data		2		ns
t_W	Minimum LE Pulse Width		10		ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $t_r=t_f=6$ ns, $C_L=50$ pF (unless otherwise noted.)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C	54HCT $T_A=-55$ to 125°C	Units
			Typ	Guaranteed Limits		
t_{PHL}, t_{PLH}	Maximum Propagation Delay Data to Q	$C_L=50$ pF $C_L=150$ pF	14 21			ns ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay,LE to Q	$C_L=50$ pF $C_L=150$ pF	14 21			ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=50$ pF $C_L=150$ pF	 15 24			 ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	 13			 ns
t_S	Minimum Setup Time, Data to LE		10			ns
t_H	Minimum Hold Time, LE to Data					ns
t_W	Minimum LE Pulse Width		9			ns
t_{TLH}, t_{THL}	Maximum Output Rise and Fall Time	$C_L=50$ pF	7			ns
C_{PD}	Power Dissipation Capacitance (Note 5)	OC=V_{CC} OC=GND	30 50			pF pF
C_{IN}	Maximum Input Capacitance		5			pF
C_{OUT}	Maximum Output Capacitance		15			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}V_{CC}^2f+I_{CC}V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}V_{CC}f+I_{CC}$.

4

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT574/MM74HCT574 TRI-STATE® Octal D-Type Flip-Flop

General Description

These high speed octal D-type flip-flops utilize micro-CMOS Technology, 3.0 micron silicon gate N-well CMOS. They possess the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads. Due to the large output drive capability and the TRI-STATE feature, these devices are ideally suited for interfacing with bus lines in a bus organized system.

These devices are positive edge triggered flip-flops. Data at the D inputs, meeting the set-up and hold time requirements, are transferred to the Q outputs on positive going transitions of the CLOCK (CK) input. When a high logic level is applied to the OUTPUT CONTROL (OC) input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

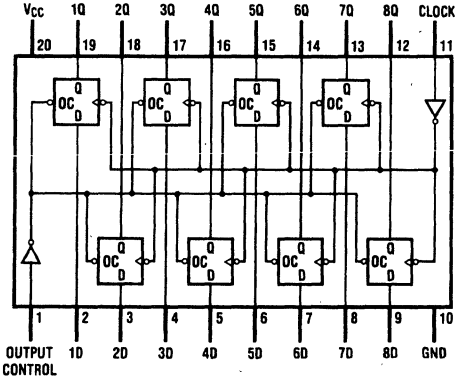
All inputs to this device are protected from damage due to electrostatic discharge by diodes to V_{CC} and ground.

Features

- TTL input characteristic compatible
- Low input current: 1 μA maximum
- Low quiescent current: 80 μA maximum
- Compatible with bus-oriented systems
- Output drive capability: 15 LS-TTL loads

Connection Diagram

Dual-In-Line Package



TL/F/6127–1

Top View

Order Number MM54HCT574J or MM74HCT574J,N
See NS Package J20A or N20A

Truth Table

Output Control	Clock	Data	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level, L = Low Level
X = Don't Care
↑ = Transition from low-to-high
Z = High impedance state
Q_0 = The level of the output before steady state input conditions were established

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}−0.1	V_{CC}−0.1	V_{CC}−0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0 mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2 mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND OC=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0 μA		8.0	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All others tied to V_{CC} or ground.

AC Electrical Characteristics $V_{CC}=5V$, $T_A=25°C$, $t_r=t_f=6$ ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency		50		MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=45$ pF	12		ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ $C_L=45$ pF	13		ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=5$ pF	11		ns
t_S	Minimum Setup Time				ns
t_H	Minimum Hold Time				ns
t_W	Minimum Pulse Width				ns

AC Electrical Characteristics $V_{CC}=5V\pm10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to 85°C		54HCT $T_A=-55$ to 125°C		Units
			Typ	Guaranteed Limits				
f_{MAX}	Maximum Operating Frequency							MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, Clock to Q	$C_L=50$ pF $C_L=150$ pF	13 19					ns ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	$R_L=1$ kΩ						
		$C_L=50$ pF $C_L=150$ pF	14 20					ns ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	$R_L=1$ kΩ $C_L=50$ pF	12					ns
t_S	Minimum Setup Time Data to Clock							ns
t_H	Minimum Hold Time Clock to Data							ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	$C_L=50$ pF	7					ns
t_W	Minimum Clock Pulse Width		9					ns
t_r, t_f	Maximum Clock Input Rise and Fall Time							ns
C_{PD}	Power Dissipation Capacitance (Note 5)	OC=V_{CC} OC=GND	30 50					pF pF
C_{IN}	Maximum Input Capacitance		5					pF
C_{OUT}	Maximum Output Capacitance		15					pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD}\,V_{CC}^2\,f+I_{CC}\,V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD}\,V_{CC}\,f+I_{CC}$.

National Semiconductor

microCMOS

MM54HCT590/MM74HCT590
8-Bit Binary Counter with TRI-STATE® Output Register

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to acheive high performance. These devices retain the low power of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits. This device is input compatible with 54LS/74LS and other TTL output compatible circuits, and may be used as a lower power direct replacement for the LS equivalent device.

The MM54HCT590/MM74HCT590 contain an 8-bit binary counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{\text{CCKEN}}$, is low. When the counter increments to the all ones condition ripple carry out, $\overline{\text{RCO}}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{\text{RCO}}$ of the first stage to the $\overline{\text{CCKEN}}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{\text{RCO}}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed TRI-STATE outputs which are enabled when the enable input, $\overline{\text{G}}$, is taken low. This enables connection of this part of a system bus.

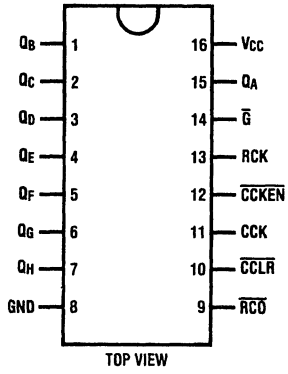
The MM54HCT590/MM74HCT590 are functional, speed and pin equivalent to the equivalent LS-TTL circuit, and may be used as a direct replacement for the equivalent LS-TTL IC. Its inputs are protected from damage due to electrostatic discharge by diodes from V_{CC} to ground.

Features

- Wide power supply range: 4.5V to 5.5V
- Guaranteed TTL compatible input logic levels: 2.0V and 0.8V
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HCT)

Connection Diagram

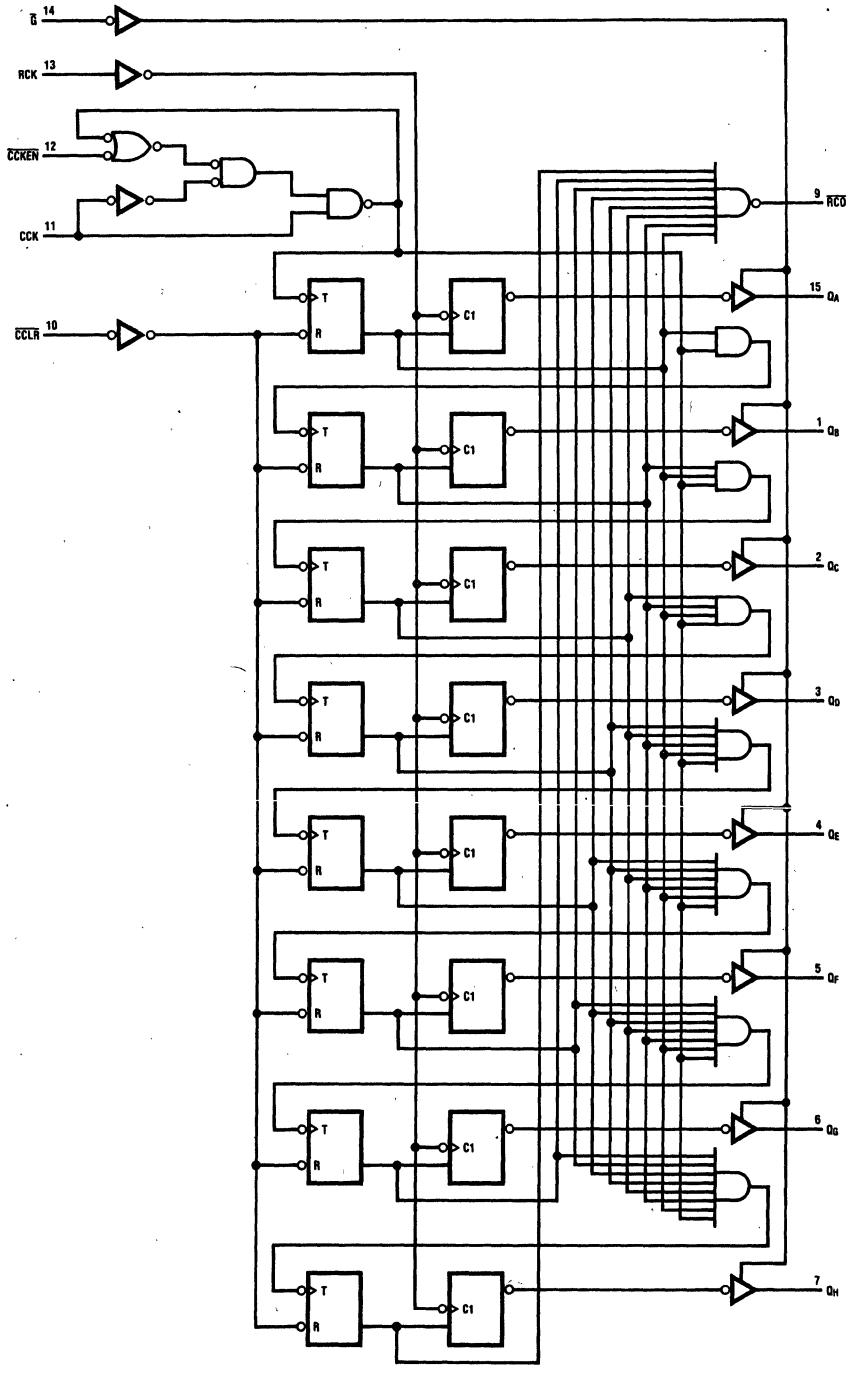
Dual-In-Line Package



TL/F/5768–1

Order Number MM54HCT590J or MM74HCT590J, N
See NS Package J16A or N16E

Logic Diagram



TL/F/5768–2

National Semiconductor

PRELIMINARY

microCMOS

MM54HCT592/MM74HCT592 8-Bit Binary Counter with Input Register MM54HCT593/MM74HCT593 8-Bit Counter with Bidirectional Input Register/Counter Outputs

General Description

These counters are implemented using an advanced 3.0 micron silicon gate N-well microCMOS process to achieve high peformance. These devices retain the low power of CMOS logic, while offering the high speed operation and large output drive typically associated with bipolar circuits. This device is input compatible with 54LS/74LS and other TTL output compatible circuits, and may be used as a lower power direct replacement for the LS equivalent device.

The MM54HCT592/MM74HCT592 and the MM54HCT593/MM74HCT593 contain an 8-bit register which feeds an 8-bit binary counter. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{CCKEN}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{RCO}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{RCO}$ of the first stage to the $\overline{CCKEN}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the RCO of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The input register is loaded on the rising edge of the register clock, RCK. The outputs of this register feed the counter. The counter is loaded with the register's contents when the clock load, $\overline{CLOAD}$, input is taken low.

The 'HCT592 differs from the 'HCT593 in that the latter device has bidirectional input/output pins. The TRI-STATE® outputs of the counter can be enabled and are active when enable input, $\overline{G}$, is taken low and input G is taken high. The outputs of the counter then appear on the register inputs. This enables connection of this part to a system bus. The 'HCT593 also has a second clock enable pin, CCKEN, which is active high and it also has an active low register clock enable, $\overline{RCKEN}$.

The MM54HCT592/MM74HCT592 and the MM54HCT593/MM74HCT593 are functional, speed and pin equivalent to the equivalent LS-TTL circuit and may be used as a direct replacement for the equivalent LS-TTL IC. Their inputs are protected from damage due to electrostatic discharge by diodes from V_{CC} to ground.

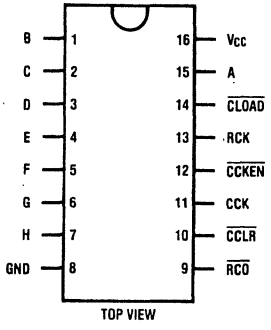
Features

- Wide power supply range: 4.5V to 5.5V
- Guaranteed TTL compatible input logic levels: 2.0V and 0.8V
- High output current drive: 6.0 mA min
- Low quiescent power consumption: 80 μA (74HCT)

4

Connection Diagrams

Dual-In-Line Package

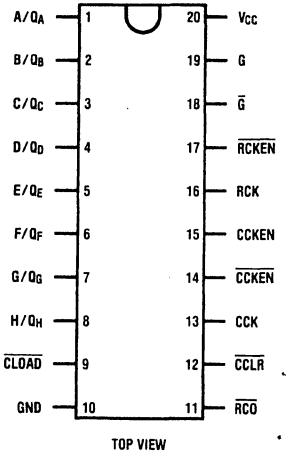


TL/F/5769–1

MM54HCT592/MM74HCT592

Order Number MM54HCT592J, MM54HCT593J, MM74HCT592J, N or MM74HCT593J, N
See NS Package J16A, J20A, N16E or N20A

Dual-In-Line Package

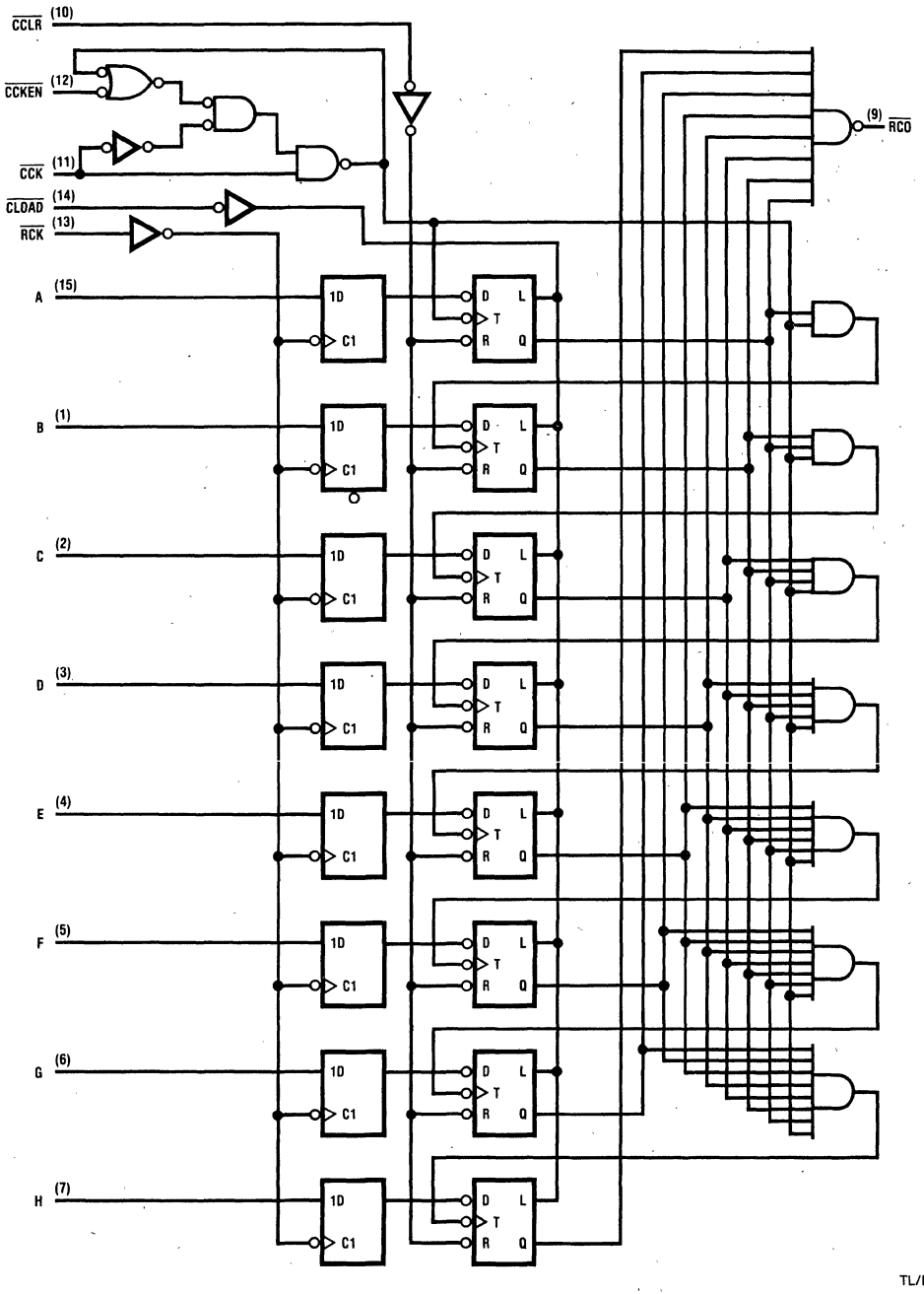


TL/F/5769–2

MM54HCT593/MM74HCT593

Logic Diagrams

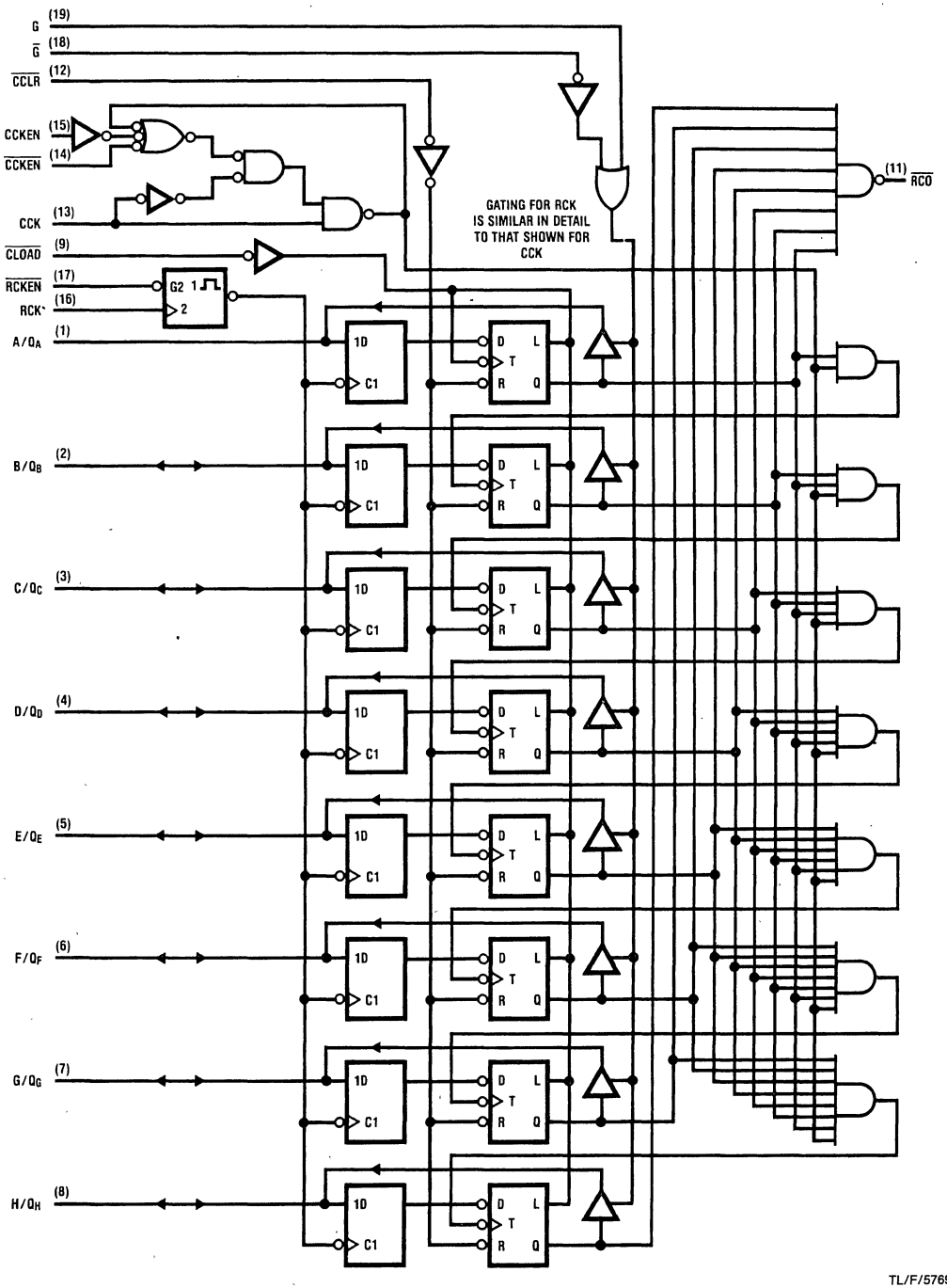
HCT592



TL/F/5769–3

Logic Diagrams (Continued)

HCT593



TL/F/5769–4

National Semiconductor

microCMOS

MM54HCT640/MM74HCT640 Inverting Octal TRI-STATE® Transceiver MM54HCT643/MM74HCT643 True-Inverting Octal TRI-STATE Transceiver

General Description

These TRI-STATE bi-directional transceivers utilize microCMOS Technology, 3.0 micron silicon gate N-well CMOS, and are intended for two-way asynchronous communication between data buses. They have high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits possess the low power consumption of CMOS circuitry, yet have speeds comparable to low power Schottky TTL circuits.

All devices are TTL input compatible and can drive up to 15 LS-TTL loads, and all inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Both the MM54HCT640/MM74HCT640 and the MM54HCT643/ MM74HCT643 have one active low enable input ($\overline{G}$), and a direction control (DIR). When the DIR input is high, data flows from the A inputs to the B outputs. When DIR is low, data flows from B to A. The MM54HCT640/MM74HCT640 transfers inverted data from one bus to the other. The MM54HCT643/MM74HCT643 transfers inverted data from the A bus to the B bus and non-inverted data from the B bus to the A bus.

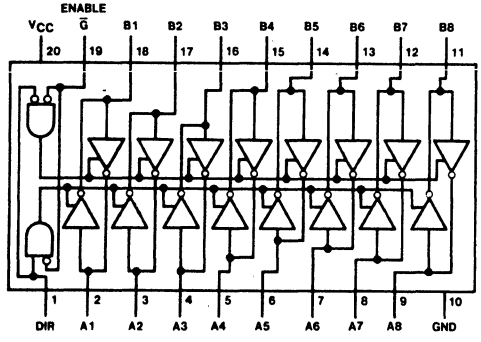
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- TTL input compatible
- Octal TRI-STATE outputs for μP bus applications: 6 mA, typical
- High speed: 16 ns typical propagation delay
- Low power: 80 μA maximum (74HCT)

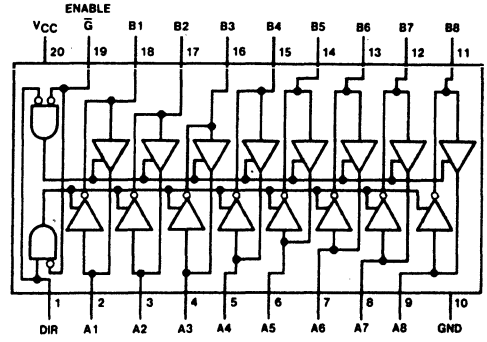
Connection Diagram

Dual-In-Line Packages



TL/F/5370–1

Top View
Order Number MM54HCT640J or MM74HCT640J, N
See NS Package J20A or N20A



TL/F/5370–2

Top View
Order Number MM54HCT643J or MM74HCT643J, N
See NS Package J20A or N20A

Truth Table

Control Inputs		Operation	
$\overline{G}$	DIR	640	643
L	L	$\overline{B}$ data to A bus	B data to A bus
L	H	$\overline{A}$ data to B bus	$\overline{A}$ data to B bus
H	X	Isolation	Isolation

H = high level, L = low level, X = irrelevant

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC}+1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC}+0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC}=5V ±10% (unless otherwise specified)

Symbol	Parameter	Conditions	T_A=25°C	74HCT T_A=−40 to 85°C	54HCT T_A=−55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	V_{CC}	V_{CC}-0.1	V_{CC}-0.1	V_{CC}-0.1	V
		$\|I_{OUT}\|$=6.0mA, V_{CC}=4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$=7.2mA, V_{CC}=5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN}=V_{IH} or V_{IL}					
		$\|I_{OUT}\|$=20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$=6.0mA, V_{CC}=4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$=7.2mA, V_{CC}=5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN}=V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum TRI-STATE Output Leakage Current	V_{OUT}=V_{CC} or GND Enable $\overline{G}$=V_{IH}		±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN}=V_{CC} or GND I_{OUT}=0μA		8	80	160	μA
		V_{IN}=2.4V or 0.5V (Note 4)	0.6	1.0	1.3	1.5	μA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per input. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics MM54HCT640/MM74HCT640

V_{CC}=5.0V, t_r=t_f=6 ns, T_A=25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L=45 pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L=45 pF R_L=1 kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L=5 pF R_L=1 kΩ	20	25	ns

AC Electrical Characteristics MM54HCT640/MM74HCT640

V_{CC} = 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C		Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		17	23	29	34	ns
		C_L = 150 pF		24	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1kΩ	C_L = 50 pF	31	42	53	63	ns
			C_L = 150 pF	35	49	62	74	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1kΩ C_L = 50 pF		21	30	38	45	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		8	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output/ Input Capacitance			20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G} = V_{CC}$ $\overline{G}$ = GND	7 100				pF pF

AC Electrical Characteristics MM54HCT643/MM74HCT643

V_{CC} = 5.0V, $t_r = t_f$ = 6 ns, T_A = 25°C (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limits	Units
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 45 pF	16	20	ns
t_{PZL}, t_{PZH}	Maximum Output Enable Time	C_L = 45 pF R_L = 1 kΩ	29	40	ns
t_{PLZ}, t_{PHZ}	Maximum Output Disable Time	C_L = 5 pF R_L = 1 kΩ	20	25	ns

AC Electrical Characteristics MM54HCT643/MM74HCT643

V_{CC} = 5.0V ± 10%, $t_r = t_f$ = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions		T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C		Units
				Typ	Guaranteed Limits			
t_{PHL}, t_{PLH}	Maximum Output Propagation Delay	C_L = 50 pF		17	23	29	34	ns
		C_L = 150 pF		24	30	38	45	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time	R_L = 1 kΩ	C_L = 50 pF	31	42	53	63	ns
			C_L = 150 pF	35	49	62	74	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time	R_L = 1 kΩ C_L = 50 pF		21	30	38	45	ns ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time	C_L = 50 pF		8	12	15	18	ns
C_{IN}	Maximum Input Capacitance			10	15	15	15	pF
C_{OUT}	Maximum Output/ Input Capacitance			20	25	25	25	pF
C_{PD}	Power Dissipation Capacitance (Note 5)	(per output)	$\overline{G} = V_{CC}$ $\overline{G}$ = GND	7 100				pF pF

Note 5: C_{PD} determines the no load power consumption. $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. The no load dynamic current consumption, $I_S = C_{PD} V_{CC} + I_{CC}$.

National Semiconductor

microCMOS

MM54HCT688/MM74HCT688
8-Bit Magnitude Comparator (Equality Detector)

General Description

This equality detector utilizes microCMOS Technology, 3.0 micron silicon gate N-well CMOS to compare bit for bit two 8-bit words and indicate whether or not they are equal. The $\overline{P=Q}$ output indicates equality when it is low. A single active low enable is provided to facilitate cascading of several packages and enable comparison of words greater than 8 bits.

This device is useful in memory block decoding applications, where memory block enable signals must be generated from computer address information.

The comparator combines the low power consumption of CMOS, but inputs are compatible with TTL logic levels, and the output can drive 10 low power Schottky equivalent loads.

MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

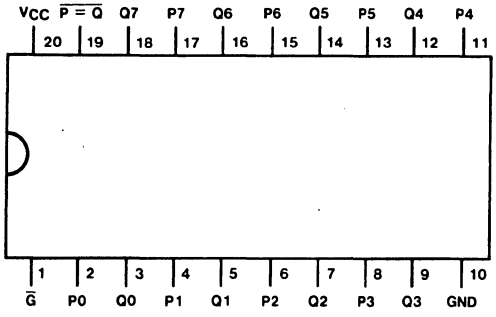
All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- TTL input compatible
- Typical propagation delay: 20 ns
- Low quiescent current: 80 μA maximum (74HCT Series)
- Large output current: 4 mA
- Same as HCT521

Connection and Logic Diagrams

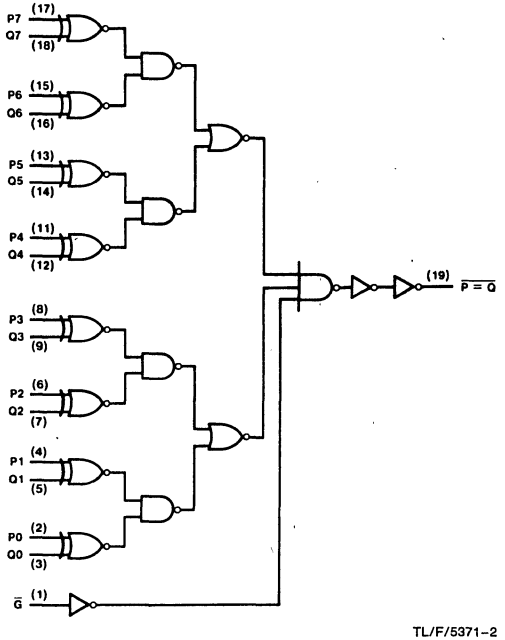
Dual-In-Line Package



TL/F/5371–1

Top View

Order Number MM54HCT688J or MM74HCT688J, N
See NS Package J20A or N20A



TL/F/5371–2

Truth Table

Inputs		
Data P, Q	Enable $\overline{G}$	$\overline{P=Q}$
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D) (Note 3)	500 mW
Lead Temperature (T_L) (Soldering 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT688	−40	+85	°C
MM54HCT688	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (V_{CC} = 5V ±10% unless otherwise specified)

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40 to 85°C	54HCT T_A = −55 to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = 0.8V or 2.0V					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.7	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V0.8V or 2.0V					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0 μA		8.0	80	160	μA
		V_{IN} = 2.4V or 0.4V (Note 4)					mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin. All other inputs held at V_{CC} or ground.

AC Electrical Characteristics

$V_{CC}=5V$, $T_A=25°C$, $C_L=15$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL}	Maximum Propagation Delay - P or Q to Output		19	30	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		13	22	
t_{PHL}	Maximum Propagation Delay - Enable to Output		13	20	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		10	18	ns

AC Electrical Characteristics

$V_{CC}=5V \pm 10\%$, $C_L=50$ pF, $t_r=t_f=6$ ns (unless otherwise specified)

Symbol	Parameter	Conditions	$T_A=25°C$	74HCT $T_A=-40$ to $85°C$		54HCT $T_A=-55$ to $125°C$	Units
			Typ	Guaranteed Limits			
t_{PHL}	Maximum Propagation Delay - P or Q to Output		23	35	44	53	ns
t_{PLH}	Maximum Propagation Delay - P or Q to Output		16	24	30	36	ns
t_{PHL}	Maximum Propagation Delay - Enable to Output		16	24	30	36	ns
t_{PLH}	Maximum Propagation Delay - Enable to Output		11	20	25	30	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C_{PD}	Power Dissipation Capacitance (Note 5)			45			pF
C_{IN}	Maximum Input Capacitance		5	10	10	10	pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D=C_{PD} V_{CC}^2 f+I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S=C_{PD} V_{CC}+I_{CC}$.

4

Section 5

CD4XXX

5

Section Contents

Section Contents (Continued)

Section Contents (Continued)

National Semiconductor

CD4000M/CD4000C Dual 3-Input NOR Gate Plus Inverter

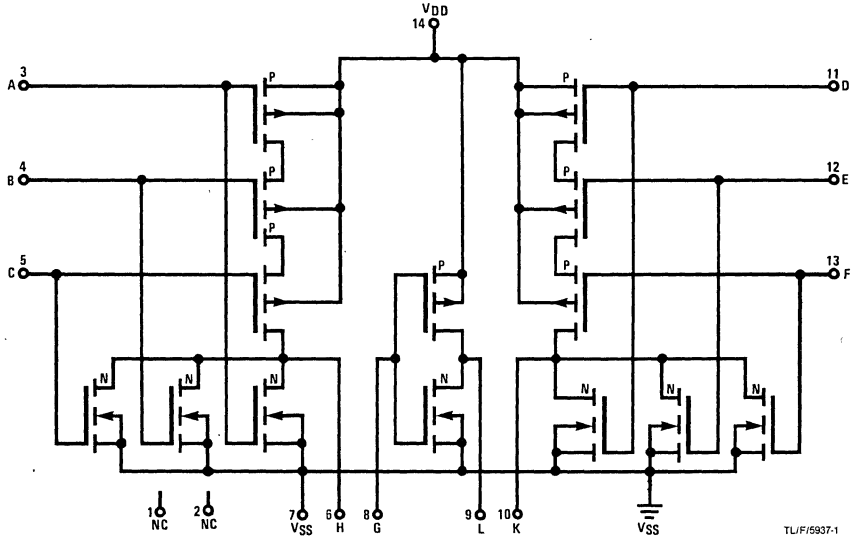
General Description

The CD4000M/CD4000C is a monolithic complementary MOS (CMOS) dual 2-input NOR gate plus an inverter. N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

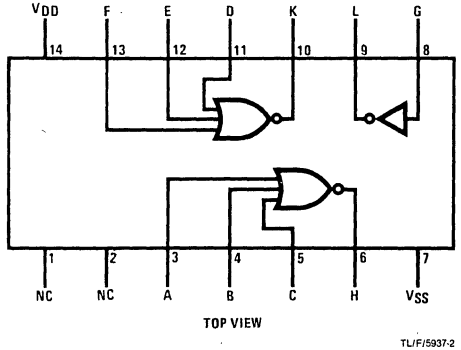
■ Wide supply voltage range	3.0 V to 15 V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Schematic and Connection Diagrams



TL/F/5937-1

Dual-In-Line Package



TOP VIEW

TL/F/5937-2

Order Number CD4000MJ or CD4000CJ
See NS Package J14A

Order Number CD4000MN or CD4000CN
See NS Package N14A

5

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin V_{SS} −0.3 V to V_{DD} + 0.3 V

Operating Temperature Range

CD4000M −55°C to +125°C

CD4000C −40°C to +85°C

Storage Temperature Range −65°C to +150°C

Package Dissipation 500 mW

Operating V_{DD} Range V_{SS} + 3 V to V_{SS} + 15 V

Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics CD4000M (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		0.05			0.05		3	μA
		V_{DD} = 10 V		0.1			0.1		6	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
		V_{DD} = 10 V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
		V_{DD} = 10 V	9.95		9.95			9.95		V
V_{NL}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.5		1.5			1.4		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	3.0		3.0			2.9		V
V_{NH}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.4		1.5			1.5		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	2.9		3.0			3.0		V
I_{DN}	Low Level Output Current (Note 4)	V_{DD} = 5 V, V_O = 0.4 V	0.5		0.4			0.28		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.1		0.9			0.65		mA
I_{DP}	High Level Output Current (Note 4)	V_{DD} = 5 V, V_O = 2.5 V	−0.62		−0.5			−0.35		mA
		V_{DD} = 10 V, V_O = 9.5 V	−0.62		−0.5			−0.35		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−1.0		−0.1	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_{IN} = 15 V		1.0		10^{-5}	0.1		1.0	μA

AC Electrical Characteristics CD4000M T_A = 25°C, C_L = 50 pF, unless otherwise noted

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High to Low Level	V_{DD} = 5 V		40	50	ns
		V_{DD} = 10 V		20	40	ns
t_{PLH}	Propagation Delay Time, Low to High Level	V_{DD} = 5 V		50	95	ns
		V_{DD} = 10 V		25	45	ns
t_{THL}	Transition Time, High to Low Level	V_{DD} = 5 V		50	125	ns
		V_{DD} = 10 V		20	70	ns
t_{TLH}	Transition Time, Low to High Level	V_{DD} = 5 V		70	175	ns
		V_{DD} = 10 V		35	75	ns
C_I	Input Capacitance	Any Input		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		35		pF

DC Electrical Characteristics C4000C (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		0.5			0.5		15	μA
		V_{DD} = 10 V		5			5		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
		V_{DD} = 10 V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
		V_{DD} = 10 V	9.95		9.95			9.95		V
V_{NL}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.5		1.5			1.4		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	3.0		3.0			2.9		V
V_{NH}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.4		1.5			1.5		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	2.9		3.0			3.0		V
I_{DN}	Low Level Output Current (Note 4)	V_{DD} = 5 V, V_O = 0.4 V	0.35		0.3			0.24		mA
		V_{DD} = 10 V, V_O = 0.5 V	0.72		0.6			0.48		mA
I_{DP}	High Level Output Current (Note 4)	V_{DD} = 5 V, V_O = 2.5 V	−0.35		−0.3			−0.24		mA
		V_{DD} = 10 V, V_O = 9.5 V	−0.3		−0.25			−0.2		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.1		1.0	μA

AC Electrical Characteristics CD4000C T_A = 25°C, C_L = 50 pF, unless otherwise noted

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High to Low Level	V_{DD} = 5 V		40	80	ns
		V_{DD} = 10 V		20	55	ns
t_{PLH}	Propagation Delay Time, Low to High Level	V_{DD} = 5 V		50	120	ns
		V_{DD} = 10 V		25	65	ns
t_{THL}	Transition Time, High to Low Level	V_{DD} = 5 V		50	200	ns
		V_{DD} = 10 V		20	115	ns
t_{TLH}	Transition Time, Low to High Level	V_{DD} = 5 V		70	300	ns
		V_{DD} = 10 V		35	125	ns
C_I	Input Capacitance	Any Input		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 5)		35		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Note 3: For the NOR gates V_{NH} and V_{NL} are tested at each input while all other inputs are at V_{SS}.

Note 4: I_{DN} and I_{DP} are tested one output at a time.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For explanation see 54C/74C Family Characteristics application note, AN-90.

National Semiconductor

CD4001M/CD4001C Quadruple 2-Input NOR Gate
CD4011M/CD4011C Quadruple 2-Input NAND Gate

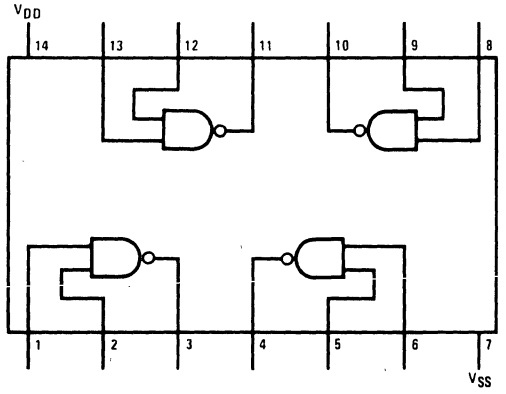
General Description

The CD4001M/CD4001C, CD4011M/CD4011C are monolithic complementary MOS (CMOS) quadruple two-input NOR and NAND gate integrated circuits. N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Connection Diagrams Dual-In-Line Packages

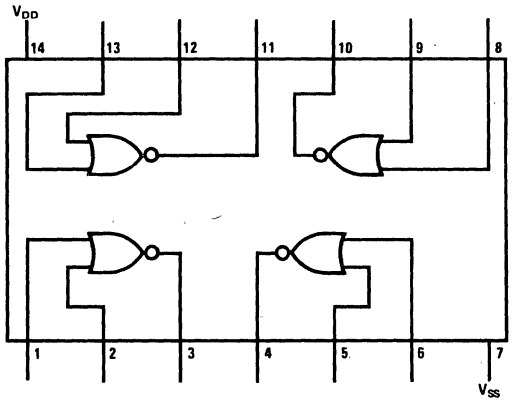


TOP VIEW

TL/F/5938-1

Order Number CD4001MJ, CD4001CJ, CD4011MJ or CD4011CJ
See NS Package J14A

Order Number CD4001MN, CD4001CN, CD4011MN or CD4011CN
See NS Package N14A



TOP VIEW

TL/F/5938-2

Absolute Maximum Ratings (Note 1)

Voltage an Any Pin $V_{SS} - 0.3\,V$ to $V_{DD} + 0.3\,V$
Operating Temperature Range
CD4001M, CD4011M −55°C to +125°C
CD4001C, CD4011C −40°C to +85°C

Storage Temperature Range −65°C to +150°C
Package Dissipation 500 mW
Operating V_{DD} Range $V_{SS} + 3.0\,V$ to $V_{SS} + 15\,V$
Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics — CD4001M, CD4011M

Sym	Parameter	Conditions	Limits							Units
			−55°C		25°C			125°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$		0.05		0.001	0.05		3.0	μA
		$V_{DD} = 10V$		0.1		0.001	0.1		6.0	μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$		0.25		0.005	0.25		15	μW
		$V_{DD} = 10V$		1.0		0.01	1.0		60	μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05		0	0.05		0.05	V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$	4.95		4.95	5.0		4.95		V
		$V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	9.95		9.95	10		9.95		V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$	1.5		1.5	2.25		1.4		V
		$V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	3.0		3.0	4.5		2.9		V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$	1.4		1.5	2.25		1.5		V
		$V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	2.9		3.0	4.5		3.0		V
I_DN	Output Drive Current N-Channel (4001) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.5		0.40	1.0		0.28		mA
		$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	1.1		0.9	2.5		0.65		mA
I_DP	Output Drive Current P-Channel (4001) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.62		−0.5	−2.0		−0.35		mA
		$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.62		−0.5	−1.0		−0.35		mA
I_DN	Output Drive Current N-Channel (4011) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$	0.31		0.25	0.5		0.175		mA
		$V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.63		0.5	0.6		0.35		mA
I_DP	Output Drive Current P-Channel (4011) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$	−0.31		−0.25	−0.5		−0.175		mA
		$V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.75		−0.6	−1.2		−0.4		mA
I_I	Input Current					10				pA

5

DC Electrical Characteristics — CD4001C, CD4011C

Sym	Parameter	Conditions	Limits							Units
			−40°C		25°C			80°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.5 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4001) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I_DP	Output Drive Current P-Channel (4001) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I_DN	Output Drive Current N-Channel (4011) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.145 0.3		0.12 0.25	0.5 0.6		0.095 0.2		mA mA
I_DP	Output Drive Current P-Channel (4011) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4001M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	65 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	125 70	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	175 75	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4001C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	80 55	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	120 65	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	200 115	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	300 125	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4011M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	100 60	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4011C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	125 75	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

National Semiconductor

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

General Description

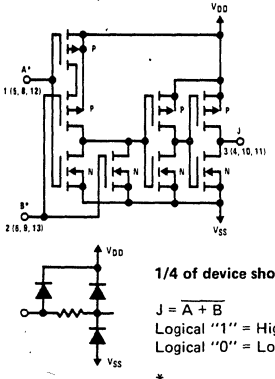
These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V—10V—15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1μA at 15V over full temperature range

Schematic and Connection Diagrams



1/4 of device shown

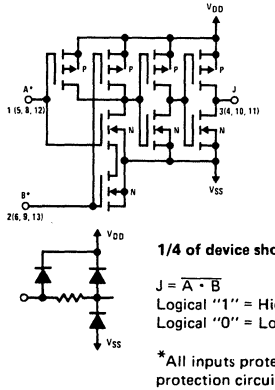
$J = \overline{A + B}$

Logical "1" = High

Logical "0" = Low

TL/F/5939-1

*All inputs protected by standard CMOS protection circuit.



1/4 of device shown

$J = \overline{A \cdot B}$

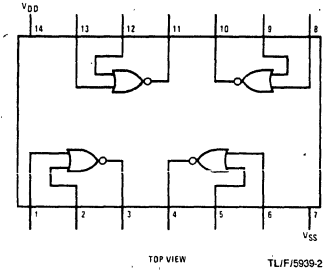
Logical "1" = High

Logical "0" = Low

TL/F/5939-3

*All inputs protected by standard CMOS protection circuit.

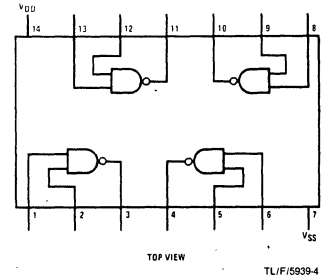
CD4001BC/CD4001BM
Dual-In-Line Package



TOP VIEW

TL/F/5939-2

CD4011BC/CD4011BM
Dual-In-Line Package



TOP VIEW

TL/F/5939-4

Order Number CD4001BMJ, CD4001BCJ, CD4011BMJ or CD4011BCJ
See NS Package J14A

Order Number CD4001BMN, CD4001BCN, CD4011BMN or CD4011BCN
See NS Package N14A

Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin	−0.5V to V_{DD} + 0.5V
Package Dissipation	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

Operating V_{DD} Range	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4001BM, CD4011BM	−55°C to +125°C
CD4001BC, CD4011BC	−40°C to +85°C

DC Electrical Characteristics CD4001BM, CD4011BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.50		0.005	0.50		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD4001BC, CD4011BC (Note 2)

SYM	PARAMETER	CONDITIONS	-40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1		0.004	1		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2		0.005	2		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics CD4001BC, CD4001BM

T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	110	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics CD4011BC, CD4011BM

$T_A = 25°C$, Input t_r; $t_f = 20$ ns. $C_L = 50$ pF, $R_L = 200$k. Typical Temperature Coefficient is 0.3%/°C.

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay, High-to-Low Level	$V_{DD} = 5V$	120	250	ns
		$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	35	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	$V_{DD} = 5V$	85	250	ns
		$V_{DD} = 10V$	40	100	ns
		$V_{DD} = 15V$	30	70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$	90	200	ns
		$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

Typical Performance Characteristics

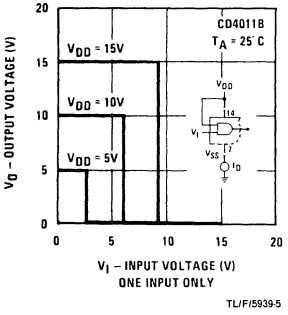


FIGURE 1. Typical Transfer Characteristics

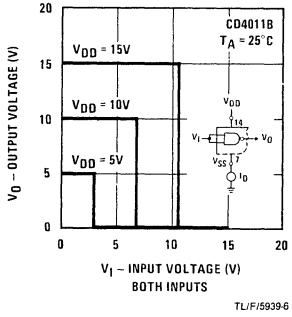


FIGURE 2. Typical Transfer Characteristics

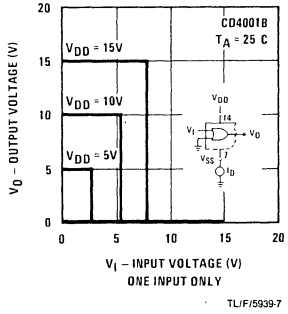


FIGURE 3. Typical Transfer Characteristics

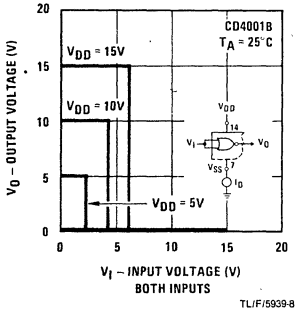


FIGURE 4. Typical Transfer Characteristics

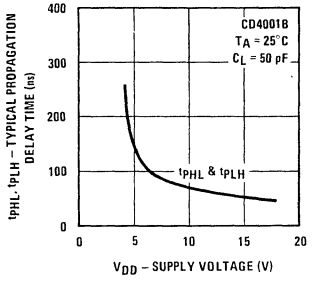


FIGURE 5

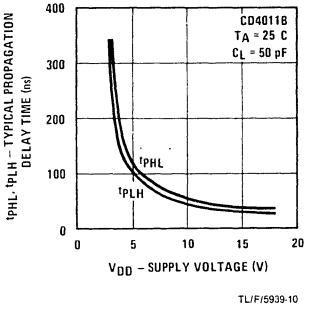


FIGURE 6

Typical Performance Characteristics (Cont'd.)

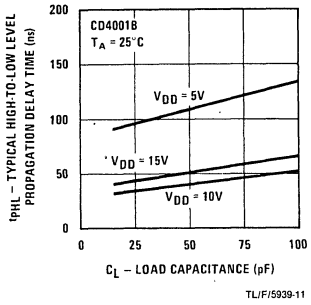


FIGURE 7

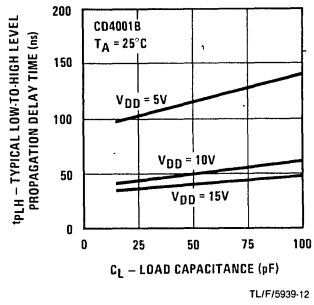


FIGURE 8

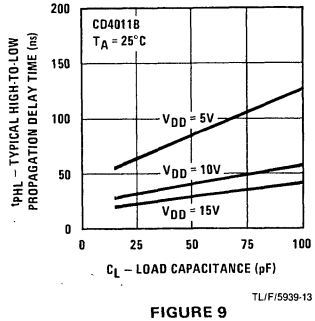


FIGURE 9

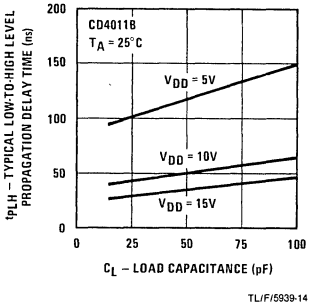


FIGURE 10

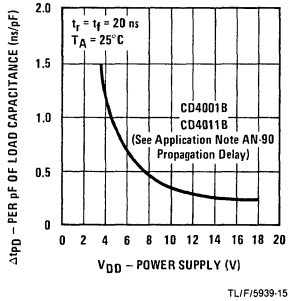


FIGURE 11

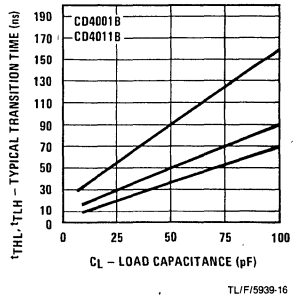


FIGURE 12

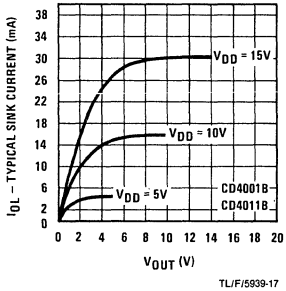


FIGURE 13

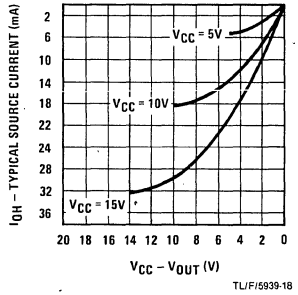


FIGURE 14

National Semiconductor

CD4002M/CD4002C Dual 4-Input NOR Gate
CD4012M/CD4012C Dual 4-Input NAND Gate

General Description

These NOR and NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

Features

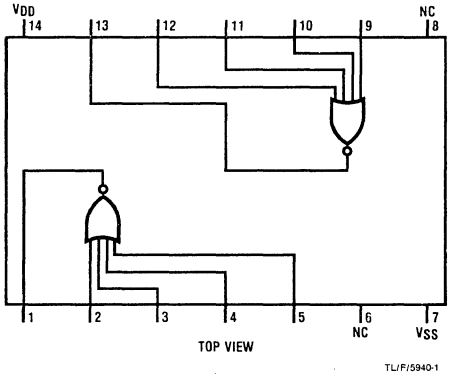
■ Wide supply voltage range	3.0 V to 15 V
■ Low power	10 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)

Applications

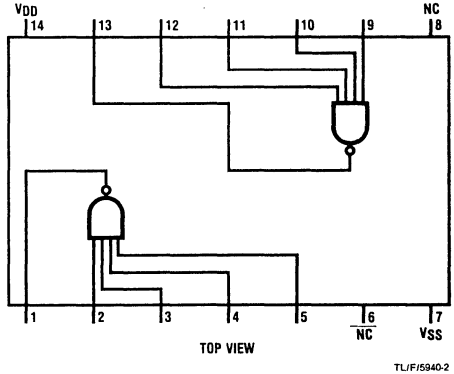
- Automotive
- Data terminals
- Instrumentation
- Medical Electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

Connection Diagrams Dual-In-Line Packages

CD4002



CD4012



Order Number CD4002MJ, CD4002CJ, CD4012MJ or CD4012CJ
See NS Package J14A

Order Number CD4002MN, CD4002CN, CD4012MN or CD4012CN
See NS Package N14A

5

Absolute Maximum Ratings (Note 1)

Voltage an Any Pin $V_{SS} - 0.3\,V$ to $V_{DD} + 0.3\,V$
Operating Temperature Range
CD4002M, CD4012M −55°C to +125°C
CD4002C, CD4012C −40°C to +85°C
Storage Temperature Range −65°C to +150°C
Package Dissipation 500 mW
Operating V_{DD} Range $V_{SS} + 3.0\,V$ to $V_{SS} + 15\,V$
Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics — CD4002M, CD4012M

Sym	Parameter	Conditions	Limits							Units
			−55°C		25°C			125°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.05 0.1		0.001 0.001	0.05 0.1		3.0 6.0	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.25 1.0		0.005 0.01	0.25 1.0		15 60	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O = 7.2V$, $I_O = 0A$	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O = 2.9V$, $I_O = 0A$	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4002) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.5 1.1		0.40 0.9	1.0 2.5		0.28 0.65		mA mA
I_DP	Output Drive Current P-Channel (4002) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.62 −0.62		−0.5 −0.5	−2.0 −1.0		−0.35 −0.35		mA mA
I_DN	Output Drive Current N-Channel (4012) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.31 0.63		0.25 0.5	0.5 0.6		0.175 0.35		mA mA
I_DP	Output Drive Current P-Channel (4012) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.31 −0.75		−0.25 −0.6	−0.5 −1.2		−0.175 −0.4		mA mA
I_I	Input Current					10				pA

DC Electrical Characteristics — CD4002C, CD4012C

Sym	Parameter	Conditions	Limits							Units
			−40°C		25°C			85°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$		0.5 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$, $V_I = V_{DD}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{DD}$, $I_O = 0A$		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$, $V_I = V_{SS}$, $I_O = 0A$ $V_{DD} = 10V$, $V_I = V_{SS}$, $I_O = 0A$	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O \geq 3.5V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O \geq 7.2V$, $I_O = 0A$	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$, $V_O \leq 1.5V$, $I_O = 0A$ $V_{DD} = 10V$, $V_O \leq 3.5V$, $I_O = 0A$	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4002) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I_DN	Output Drive Current N-Channel (4012) (Note 2)	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.145 0.3		0.12 0.25	0.5 0.6		0.095 0.2		mA mA
I_DP	Output Drive Current P-Channel (4002) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I_DP	Output Drive Current P-Channel (4012) (Note 2)	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I_I	Input Current					10				pA

5

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15pF$, and input rise and fall times = 20ns.

Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4002M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	175 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	125 70	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4002C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	120 65	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	80 55	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	300 125	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	200 115	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15pF$, and input rise and fall times = 20ns.

Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4012M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	100 60	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
CD4012C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	125 75	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

National Semiconductor

CD4002BM/CD4002BC Dual 4-Input NOR Gate
CD4012BM/CD4012BC Dual 4-Input NAND Gate

General Description

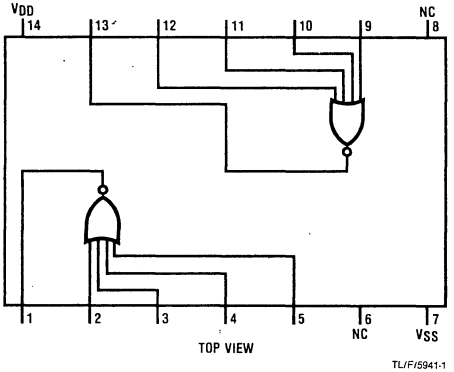
These dual gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

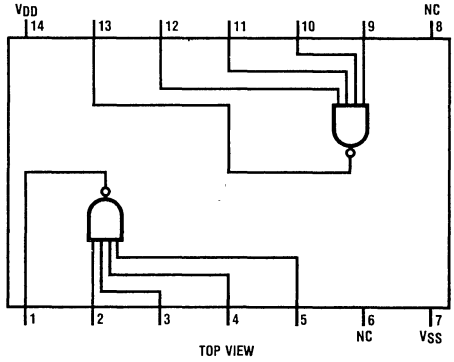
- Wide supply voltage range 3.0V to 15V
- High noise immunity $0.45\,V_{DD}$ (typ.)
- Low power TTL compatibility fanout of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagrams Dual-In-Line Packages

CD4002BM/CD4002BC



CD4012BM/CD4012BC



Order Number CD4002BMJ, CD4002BCJ, CD4012BMJ or CD4012BCJ
See NS Package J14A

Order Number CD4002BMN, CD4002BCN, CD4012BMN or CD4012BCN
See NS Package N14A

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5 V to +18 V
V_{IN}	Input Voltage	−0.5 to V_{DD}0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD}	Supply Voltage	3.0 to 15 V
V_{IN}	Input Voltage	0 V to V_{DD} V
T_A	Operating Temperature Range	
	CD4002BM, CD4012BM	−55°C to +125°C
	CD4002BC, CD4012BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4002BM, CD4012BM

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0 V, V_{IN} = V_{DD} or V_{SS}		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10 V, V_{IN} = V_{DD} or V_{SS}		0.5		0.005	0.5		15	μA
		V_{DD} = 15 V, V_{IN} = V_{DD} or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.2		0.90		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−2.2		−0.90		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.10		10^5	0.10		1.0	μA

DC Electrical Characteristics (Note 2) — CD4002BC, CD4012BC

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5.0\,V$, $V_{IN}=V_{DD}$ or V_{SS}		1.0		0.004	1.0		7.5	μA
		$V_{DD}=10\,V$, $V_{IN}=V_{DD}$ or V_{SS}		2.0		0.005	2.0		15	μA
		$V_{DD}=15\,V$, $V_{IN}=V_{DD}$ or V_{SS}		4.0		0.006	4.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5.0\,V$		0.05		0	0.05		0.05	V
		$V_{DD}=10\,V$		0.05		0	0.05		0.05	V
		$V_{DD}=15\,V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5.0\,V$	4.95		4.95	5.0		4.95		V
		$V_{DD}=10\,V$	9.95		9.95	10		9.95		V
		$V_{DD}=15\,V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5\,V$ or $4.5\,V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10\,V$, $V_O=1.0\,V$ or $9.0\,V$		3.0		4.50	3.0		3.0	V
		$V_{DD}=15\,V$, $V_O=1.5\,V$ or $13.5\,V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5.0\,V$, $V_O=0.5\,V$ or $4.5\,V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10\,V$, $V_O=1.0\,V$ or $9.0\,V$	7.0		7.0	5.50		7.0		V
		$V_{DD}=15\,V$, $V_O=1.5\,V$ or $13.5\,V$	11		11	8.25		11		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5.0\,V$, $V_O=0.4\,V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10\,V$, $V_O=0.5\,V$	1.3		1.1	2.2		0.90		mA
		$V_{DD}=15\,V$, $V_O=1.5\,V$	3.6		3.0	8.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5.0\,V$, $V_O=4.6\,V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10\,V$, $V_O=9.5\,V$	−1.3		−1.1	−2.2		−0.90		mA
		$V_{DD}=15\,V$, $V_O=13.5\,V$	−3.6		−3.0	−8.0		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15\,V$, $V_{IN}=0\,V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15\,V$, $V_{IN}=15\,V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A=25°C$, $C_L=50\,pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay, High to Low Level	$V_{DD}=5.0\,V$		125	250	ns
		$V_{DD}=10\,V$		60	100	ns
		$V_{DD}=15\,V$		45	70	ns
t_{PLH}	Propagation Delay, Low to High Level	$V_{DD}=5.0\,V$		125	250	ns
		$V_{DD}=10\,V$		60	100	ns
		$V_{DD}=15\,V$		45	70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD}=5.0\,V$		100	200	ns
		$V_{DD}=10\,V$		50	100	ns
		$V_{DD}=15\,V$		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity (Note 4)	Any Gate		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics, Application Note AN-90.

National Semiconductor

CD4006BM/CD4006BC 18-Stage Static Shift Register

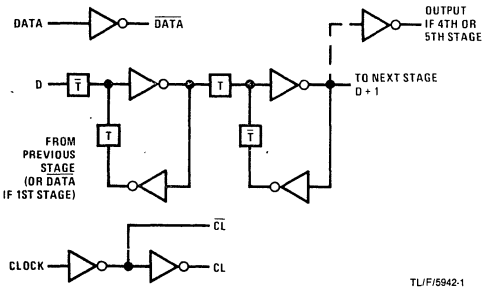
General Description

The CD4006BM/CD4006BC 18-stage static shift register is comprised of four separate shift register sections, two sections of four stages and two sections of five stages. Each section has an independent data input. Outputs are available at the fourth stage and the fifth stage of each section. A common clock signal is used for all stages. Data is shifted to the next stage on the negative-going transition of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages, or single register sections of 10, 12, 13, 14, 16, 17, and 18 stages can be implemented using one package.

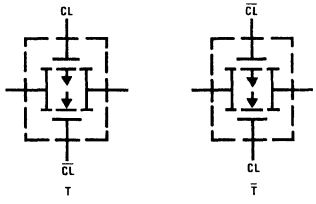
Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 drving 74L or 1 driving 74LS
- Low clock input capacitance — 6pF (typ.)
- Medium speed — 10MHz (typ.) (with V_{DD} = 10V)
- Low power
- Fully static operation

Logic Diagrams



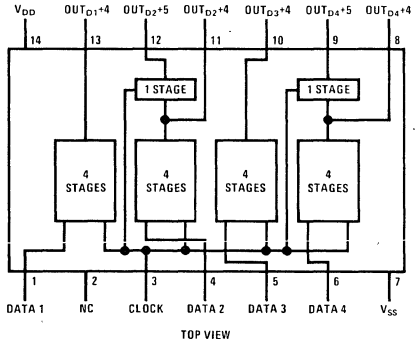
TL/F/5942-1



TL/F/5942-2

Connection Diagram

Dual-In-Line Package



TL/F/5942-3

Order Number CD4006BMJ or CD4006BCJ
See NS Package J14A

Order Number CD4006BMN or CD4006BCN
See NS Package N14A

Truth Table

D	CL$^{\Delta}$	D+1
0	↓	0
1	↓	1
X	↓	NC

X = Don't care
Δ = Level change
NC = No change

TL/F/5942-4

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD}	DC Supply Voltage	-0.5 to $+18$ V_{DC}
V_{IN}	Input Voltage	-0.5 to $V_{DD}+0.5$ V_{DC}
T_S	Storage Temperature Range	$-65°C$ to $+150°C$
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD}	DC Supply Voltage	+3.0 to +15 V
V_{IN}	Input Voltage	0 to V_{DD} V_{DC}
T_A	Operating Temperature Range	
	CD4006BM	$-55°C$ to $+125°C$
	CD4006BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4006BM (Note 2)

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5.0$ V, $V_{IN}=V_{DD}$ or V_{SS}		5.0		0.005	5.0		150	μA
		$V_{DD}=10$ V, $V_{IN}=V_{DD}$ or V_{SS}		10		0.010	10		300	μA
		$V_{DD}=15$ V, $V_{IN}=V_{DD}$ or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5.0$ V		0.05		0	0.05		0.05	V
		$V_{DD}=10$ V		0.05		0	0.05		0.05	V
		$V_{DD}=15$ V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5.0$ V	4.95		4.95	5.0		4.95		V
		$V_{DD}=10$ V	9.95		9.95	10		9.95		V
		$V_{DD}=15$ V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5.0$ V, $V_O=0.5$ V or 4.5 V		1.5		2.25	1.5		1.5	V
		$V_{DD}=10$ V, $V_O=1.0$ V or 9.0 V		3.0		4.50	3.0		3.0	V
		$V_{DD}=15$ V, $V_O=1.5$ V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5.0$ V, $V_O=0.5$ V or 4.5 V	3.5		3.5	2.75		3.5		V
		$V_{DD}=10$ V, $V_O=1.0$ V or 9.0 V	7.0		7.0	5.50		7.0		V
		$V_{DD}=15$ V, $V_O=1.5$ V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5.0$ V, $V_O=0.4$ V	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10$ V, $V_O=0.5$ V	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15$ V, $V_O=1.5$ V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5.0$ V, $V_O=4.6$ V	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10$ V, $V_O=9.5$ V	−1.6		−1.3	−2.25		−0.9		mA
		$V_{DD}=15$ V, $V_O=13.5$ V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15$ V, $V_{IN}=0$ V	−0.1		−0.1	-10^{-5}		−1.0		μA
		$V_{DD}=15$ V, $V_{IN}=15$ V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4006BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5.0$ V, $V_{IN}=V_{DD}$ or V_{SS}		20		0.005	20		150	μA
		$V_{DD}=10$ V, $V_{IN}=V_{DD}$ or V_{SS}		40		0.010	40		300	μA
		$V_{DD}=15$ V, $V_{IN}=V_{DD}$ or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5.0$ V		0.05		0	0.05		0.05	V
		$V_{DD}=10$ V		0.05		0	0.05		0.05	V
		$V_{DD}=15$ V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5.0$ V	4.95		4.95	5.0		4.95		V
		$V_{DD}=10$ V	9.95		9.95	10		9.95		V
		$V_{DD}=15$ V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5.0$ V, $V_O=0.5$ V or 4.5 V		1.5		2.25	1.5		1.5	V
		$V_{DD}=10$ V, $V_O=1.0$ V or 9.0 V		3.0		4.5	3.0		3.0	V
		$V_{DD}=15$ V, $V_O=1.5$ V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5.0$ V, $V_O=0.5$ V or 4.5 V	3.5		3.5	2.75		3.5		V
		$V_{DD}=5.0$ V, $V_O=1.0$ V or 9.0 V	7.0		7.0	5.5		7.0		V
		$V_{DD}=15$ V, $V_O=1.5$ V or 13.5 V	11		11	8.25		11		V

DC Electrical Characteristics (cont'd) CD4006BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5.0V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IL}=0V$, $V_{IH}=V_{DD}$								
		$V_{DD}=5.0V$, $V_O=4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−0.3	−8.8	−8.8	−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics CD4006BM/CD4006BC $T_A=25°C$, $C_L=50pF$, unless otherwise noted

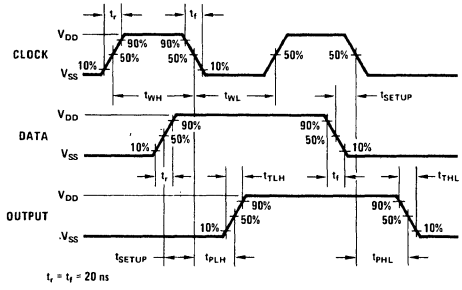
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Time ($t_{PLH}=t_{PHL}$)	$V_{DD}=5.0V$		200	400	ns
		$V_{DD}=10V$		100	200	ns
		$V_{DD}=15V$		80	150	ns
t_{TLH}, t_{THL}	Transition Time ($t_{TLH}=t_{THL}$)	$V_{DD}=5.0V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width ($t_{WL}=t_{WH}$)	$V_{DD}=5.0V$		100	200	ns
		$V_{DD}=10V$		45	100	ns
		$V_{DD}=15V$		35	70	ns
t_{RCL}, t_{FCL}	Clock Rise and Fall Time ($t_{RCL}=t_{FCL}$)	$V_{DD}=5.0V$			15	μs
		$V_{DD}=10V$			15	μs
		$V_{DD}=15V$			15	μs
t_{SU}	Minimum Set-up Time	$V_{DD}=5.0V$		50	100	ns
		$V_{DD}=10V$		25	50	ns
		$V_{DD}=15V$		20	40	ns
t_H	Minimum Hold Time	$V_{DD}=5.0V$		55	110	ns
		$V_{DD}=10V$		35	70	ns
		$V_{DD}=15V$		30	60	ns
f_{CL}	Maximum Clock Frequency	$V_{DD}=5.0V$	2.5	5.0		MHz
		$V_{DD}=10V$	5.0	12		MHz
		$V_{DD}=15V$	7.0	16		MHz
C_L	Input Capacitance	Data Input		5.0		pF
		CLK Input		7.5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Switching Time Waveforms



TL/F/5942-5

National Semiconductor

CD4007M/CD4007C Dual Complementary Pair Plus Inverter

General Description

The CD4007M/CD4007C consists of three complementary pairs of N- and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

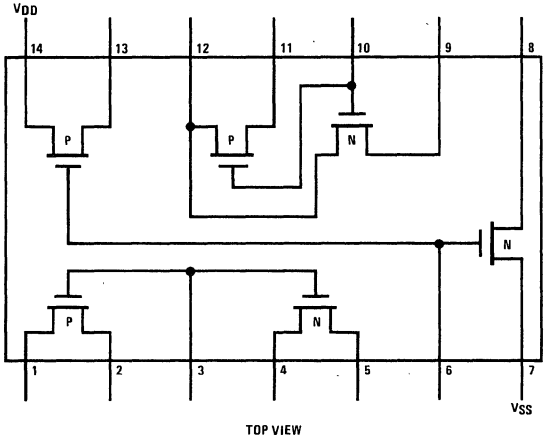
For proper operation the voltages at all pins must be constrained to be between $V_{SS} - 0.3\,V$ and $V_{DD} + 0.3\,V$ at all times.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{CC} (typ.)

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5943-1

Note: All P-channel substrates are connected to V_{DD} and all N-channel substrates are connected to V_{SS}.

Order Number CD4007MJ or CD4007CJ
See NS Package J14A

Order Number CD4007MN or CD4007CN
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin $V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature Range
CD4007M $-55°C$ to $+125°C$
CD4007C $-40°C$ to $+85°C$
Storage Tempeature Range $-65°C$ to $+150°C$
Package Dissipation 500 mW
Operating V_{DD} Range $V_{SS} + 3.0V$ to $V_{SS} + 15V$
Lead Temperature (Soldering, 10 seconds) $260°C$

DC Electrical Characteristics — CD4007M

Sym	Parameter	Conditions	Limits									Units
			−55°C			25°C			125°C			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.05 0.1		0.001 0.001	0.05 0.1			3.0 6.0	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.25 1.0		0.005 0.001	0.25 1.0			15 60	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.05 0.05		0 0	0.05 0.05			0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$	4.95 9.95			4.95 9.95	5.0 10		4.95 9.95			V V
V_{NL}	Noise Immunity (All inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$ $V_{DD} = 10V$, $V_O = 7.2V$	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V
V_{NH}	Noise Immunity (All inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$ $V_{DD} = 10V$, $V_O = 2.9V$	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V
I_DN	Output Drive Current N-Channel	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.75 1.6			0.6 1.3	1.0 2.5		0.4 0.95			mA mA
I_DP	Output Drive Current P-Channel	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−1.75 −1.35			−1.4 −1.1	−4.0 −2.5		−1.0 −0.75			mA mA
I_I	Input Current						10					pA

DC Electrical Characteristics — CD4007C

Sym	Parameter	Conditions	Limits									Units
			−40°C			25°C			85°C			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.5 1.0		0.005 0.005	0.5 1.0			15 30	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$			2.5 10		0.025 0.05	2.5 10			75 300	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.05 0.05		0 0	0.01 0.01			0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$	4.95 9.95			4.95 9.95	5.0 10		4.95 9.95			V V
V_{NL}	Noise Immunity (All inputs)	$V_{DD} = 5.0V$, $V_O = 3.6V$ $V_{DD} = 10V$, $V_O = 7.2V$	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V
V_{NH}	Noise Immunity (All inputs)	$V_{DD} = 5.0V$, $V_O = 0.95V$ $V_{DD} = 10V$, $V_O = 2.9V$	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V
I_DN	Output Drive Current N-Channel	$V_{DD} = 5.0V$, $V_O = 0.4V$, $V_I = V_{DD}$ $V_{DD} = 10V$, $V_O = 0.5V$, $V_I = V_{DD}$	0.35 1.2			0.3 1.0	1.0 2.5		0.24 0.8			mA mA
I_DP	Output Drive Current P-Channel	$V_{DD} = 5.0V$, $V_O = 2.5V$, $V_I = V_{SS}$ $V_{DD} = 10V$, $V_O = 9.5V$, $V_I = V_{SS}$	−1.3 −0.65			−1.1 −0.55	−4.0 −2.5		−0.9 −0.45			mA mA
I_I	Input Current						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

AC Electrical Characteristics — CD4007M $T_A = 25°C$ and $C_L = 15\,pF$ and rise and fall times = 20 ns.

Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

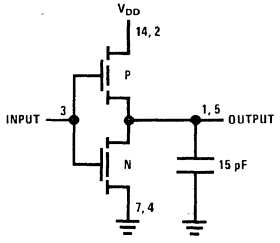
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH} = t_{PHL}$	Propagation Delay Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 20	60 40	ns ns
$t_{TLH} = t_{THL}$	Transition Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 30	75 40	ns ns
C_I	Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics CD4007C $T_A = 25°C$ and $C_L = 15\,pF$ and rise and fall times = 20 ns.

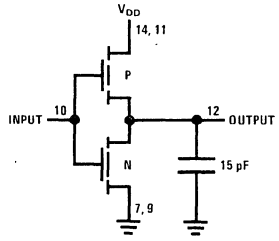
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH} = t_{PHL}$	Propagation Delay Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 20	75 50	ns ns
$t_{TLH} = t_{THL}$	Transition Time	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 30	100 50	ns ns
C_I	Input Capacitance	Any Input		5		pF

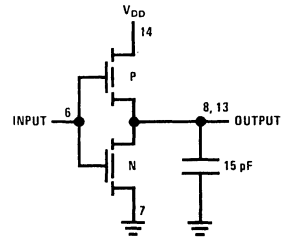
AC Test Circuits



TL/F/5943-2

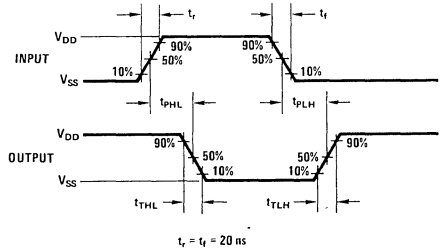


TL/F/5943-3



TL/F/5943-4

Switching Time Waveforms



$t_r = t_f = 20$ ns

TL/F/5943-5

National Semiconductor

CD4008BM/CD4008BC 4-Bit Full Adder

General Description

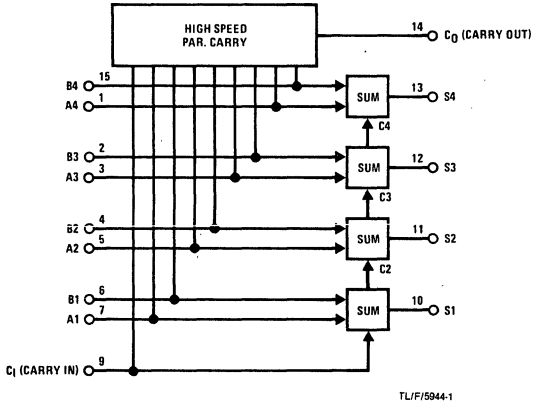
The CD4008B types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008B's. CD4008B inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the "Carry in" bit from a previous section. CD4008B outputs include the four sum bits, S1 and S4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008B section.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and GND.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 4 sum outputs plus parallel look-ahead carry-output
- Quiescent current specified to 15V
- Maximum input leakage of 1μA at 15V (full package temperature range)

Block Diagram



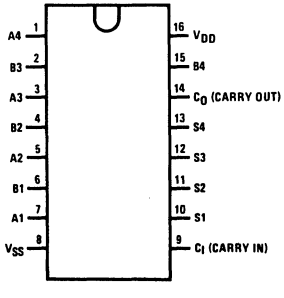
TL/F/5944-1

Truth Table

A_i	B_i	C_i	C0	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5944-2

Order Number CD4008BMJ or CD4008BCJ
See NS Package J16A

Order Number CD4008BMN or CD4008BCN
See NS Package N16E

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4008BM	−55°C to +125°C
CD4008BC	−40°C to +85°C

DC Electrical Characteristics CD4008BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.3	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.5	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.35		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−0.8		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4008BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.5	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		1	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		5	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V

5

DC Electrical Characteristics (Cont'd) CD4008BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.35		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.8		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3			−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3			0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 2000 k, input t_r, t_f = 20 ns, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time					
	Sum In to Sum Out	V_{DD} = 5V		425	750	ns
		V_{DD} = 10V		170	250	ns
		V_{DD} = 15V		125	190	ns
	Carry In to Sum Out	V_{DD} = 5V		320	650	ns
		V_{DD} = 10V		125	225	ns
		V_{DD} = 15V		95	175	ns
	Sum In to Carry Out	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		115	200	ns
		V_{DD} = 15V		90	160	ns
	Carry In to Carry Out	V_{DD} = 5V		130	245	ns
		V_{DD} = 10V		60	105	ns
		V_{DD} = 15V		45	80	ns
	Carry In to Carry Out	C_L = 15 pF				
		V_{DD} = 5V		100	175	ns
		V_{DD} = 10V		45	75	ns
		V_{DD} = 15V		35	60	ns
t_{THL}	High-to-Low Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{TLH}	Low-to-High Transition Time	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
C_{IN}	Average Input Capacitance			5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Note 4		100		pF

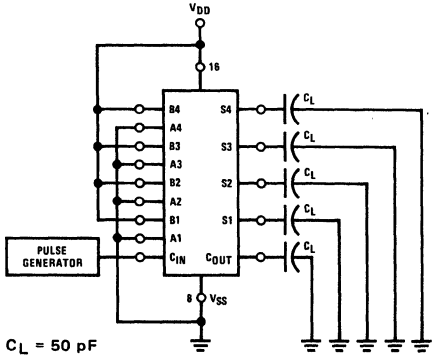
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

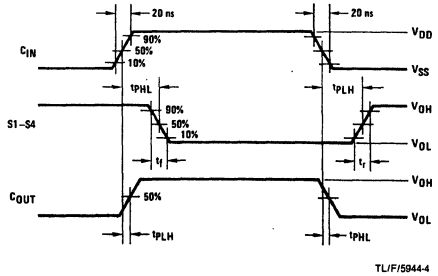
Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

AC Test Circuit and Switching Time Waveforms



C_L = 50 pF

TL/F/5944-3



TL/F/5944-4

National Semiconductor

CD4009M/CD4009C Hex Buffers (Inverting)
CD4010M/CD4010C Hex Buffers (Non-Inverting)

General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3 to 15 volts providing $V_{CC} \leq V_{DD}$.

Features

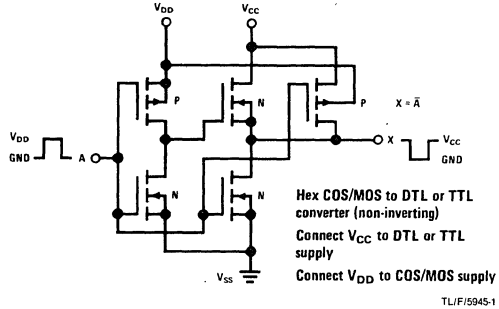
■ Wide supply voltage range	3.0 V to 15 V
■ Low power	100 nW (typ.)
■ High noise immunity	0.45 V_{DD} (typ.)
■ High current sinking capability	8 mA (min.) at $V_O = 0.5$ V and $V_{DD} = 10$ V

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

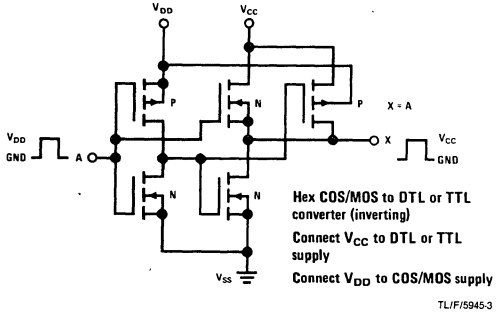
Schematic Diagrams

CD4009M/CD4009C



TL/F/5945-1

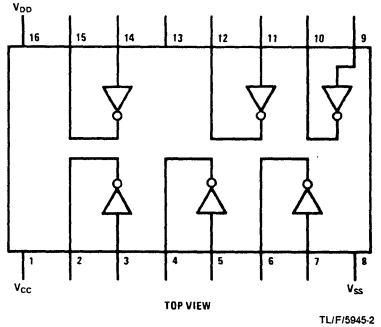
CD4010M/CD4010C



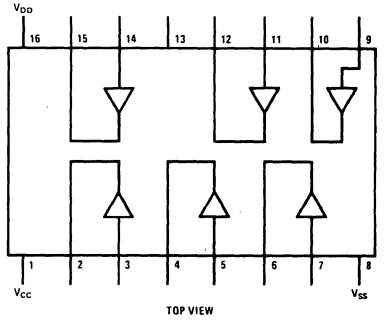
TL/F/5945-3

Connection Diagrams

Dual-In-Line Packages



TL/F/5945-2



TL/F/5945-4

Order Number CD4009MJ, CD4009CJ, CD4010MJ or CD4010CJ
See NS Package J16A

Order Number CD4009MN, CD4009CN, CD4010MN or CD4010CN
See NS Package N16E

5

Absolute Maximum Ratings

Voltage at Any Pin (Note 1) V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range CD40XXM −55°C to +125°C
CD40XXC −40°C to +85°C
Storage Temperature Range −65°C to +150°C
Package Dissipation 500mW
Lead Temperature (Soldering, 10 seconds) 260°C
Operating V_{DD} Range V_{SS} + 3V to V_{SS} + 15V

DC Electrical Characteristics

SYM	CHARACTERISTICS	TEST CONDITIONS VOLTS		LIMITS													UNITS
				CD40XXM							CD40XXC						
				−55°C		+25°C			+125°C		−40°C		+25°C			+85°C	
		V_O	V_{DD}	MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{CC}	Quiescent Device Current		5		0.3		0.01	0.3		20		3		0.03	3		42	μA
			10		0.5		0.01	0.5		30		5		0.05	5		70	μA
P_D	Quiescent Device		5		1.5		0.05	1.5		100		15		0.15	15		210	μW
	Dissipation/Package		10		5		0.1	5		300		50		0.5	50		700	μW
	Output Voltage		5		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
V_{OL}	Low Level		10		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
V_{OH}	High Level		5	4.99		4.99	5		4.95		4.99		4.99	5		4.95		V
			10	9.99		9.99	10		9.95		9.99		9.99	10		9.95		V
	Noise Immunity (All Inputs)																	
V_{NL}	CD4009M	$V_O \geq 4.0$	5	1		1	2.25		0.9		1		1	2.25		0.9		V
		$V_O \geq 8.0$	10	2		2	4.5		1.9		2		2	4.5		1.9		V
V_{NL}	CD4010M	$V_O \geq 1.5$	5	1.6		1.5	2.25		1.4		1.6		1.5	2.25		1.4		V
		$V_O \geq 3.0$	10	3.2		3	4.5		2.9		3.2		3	4.5		2.9		V
V_{NH}		$V_O \geq 3.5$	5	1.4		1.5	2.25		1.5		1.4		1.5	2.25		1.5		V
		$V_O \geq 7.0$	10	2.9		3	4.5		3		2.9		3	4.5		3		V
	Output Drive Current	0.4	5	3.75		3	4		2.1		3.6		3			2.4		mA
I_DN	N-Channel (Note 2)	0.5	10	10		8	10		5.6		9.6		8			6.4		mA
I_DP	P-Channel (Note 2)	2.5	5	−1.85		−1.25	−1.75		−0.9		−1.5		−1.25			−1		mA
		9.5	10	−0.9		−0.6	−0.8		−0.4		−0.72		−0.6			−0.48		mA
I_{IN}	Input Current						10							10				pA

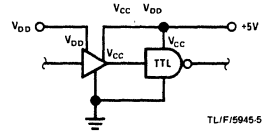
Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.
Note 2: I_DN and I_DP are tested one output at a time.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 15pF$, unless otherwise noted

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			CD40XXM			CD40XXC			
		V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time	$V_{CC} = V_{DD}$	5	—	15	55	—	15	70	
High to Low Level (t_{PHL})		10	—	10	30	—	10	40	ns
	V_{DD} = 10V		—	10	25	—	10	35	
	V_{CC} = 5V								
Low to High Level (t_{PLH})	$V_{CC} = V_{DD}$	5	—	50	80	—	50	100	
		10	—	25	55	—	25	70	ns
	V_{DD} = 10V		—	15	30	—	15	40	
	V_{CC} = 5V								
Transition Time	$V_{CC} = V_{DD}$	5	—	20	45	—	20	60	ns
High-to-Low Level (t_{THL})		10	—	16	40	—	16	50	
Low-to-High Level (t_{TLH})	$V_{CC} = V_{DD}$	5	—	80	125	—	80	160	ns
		10	—	50	100	—	50	120	
Input Capacitance (C_I)	Any Input		—	5	—	—	5	—	pF

Typical Applications



TL/F/5945-5

National Semiconductor

CD4013BM/CD4013BC Dual D Flip-Flop

General Description

The CD4013B dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

Features

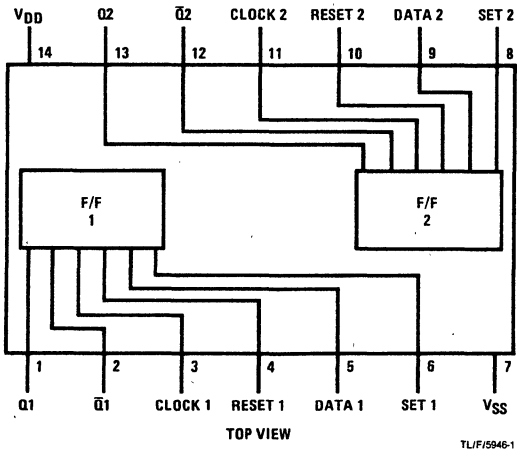
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5946-1

Order Number CD4013BMJ or CD4013BCJ
See NS Package J14A

Order Number CD4013BMN or CD4013BCN
See NS Package N14A

Truth Table

CL†	D	R	S	Q	$\overline{Q}$
↑	0	0	0	0	1
↑	1	0	0	1	0
↓	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No change
† = Level change
x = Don't care case

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4013BM	−55°C to +125°C
CD4013BC	−40°C to +85°C

DC Electrical Characteristics CD4013BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4013BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8.0			8.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD4013BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

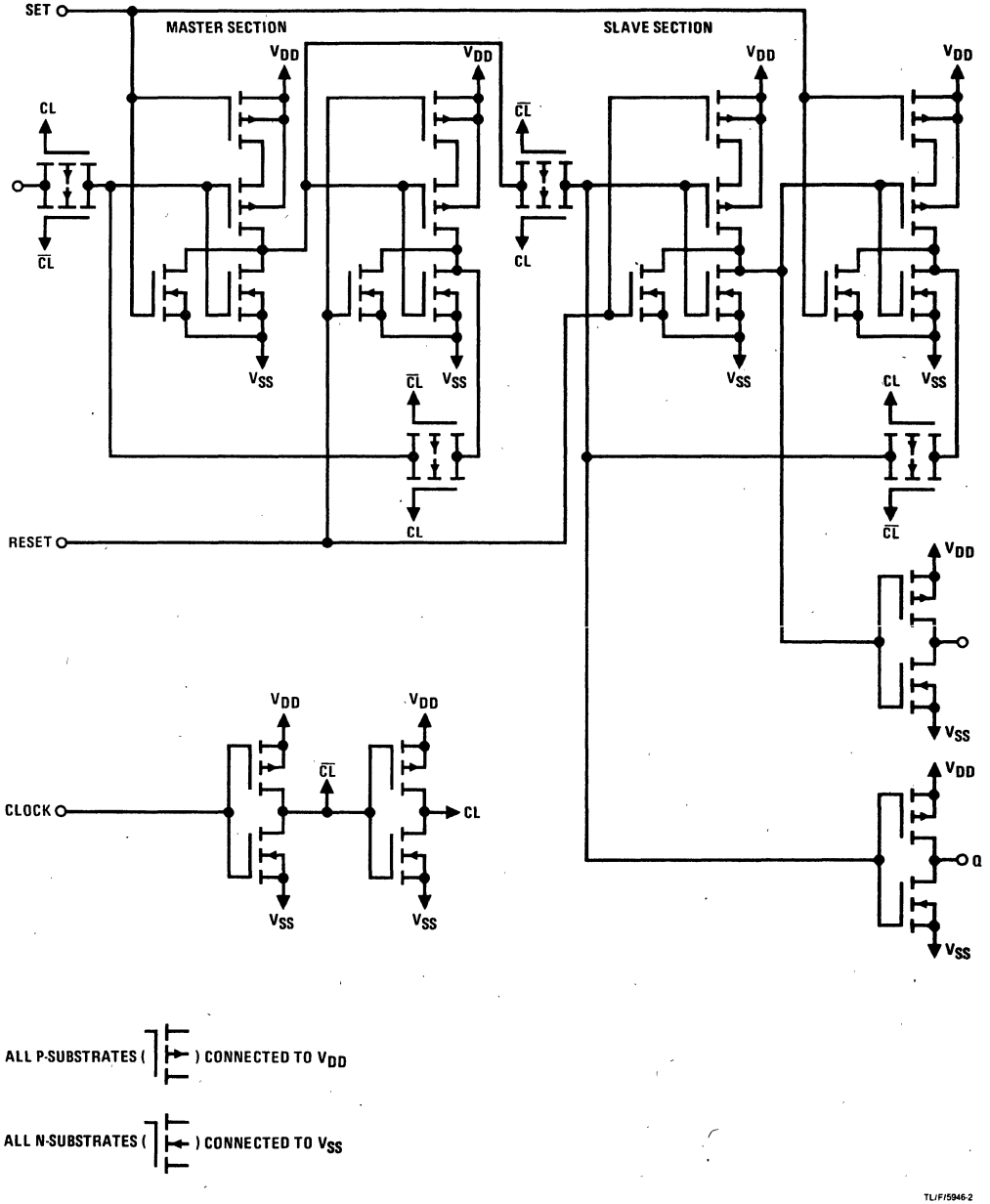
Note 3: I_{OH} and I_{OL} are measured one output at a time.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, unless otherwise noted

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OPERATION						
t_{PHL}, or t_{PLH}	Propagation Delay Time	V_{DD} = 5V		200	350	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	120	ns
t_{THL}, or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, or t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			5	μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		20	40	ns
		V_{DD} = 10V		15	30	ns
		V_{DD} = 15V		12	25	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2.5	5		MHz
		V_{DD} = 10V	6.2	12.5		MHz
		V_{DD} = 15V	7.6	15.5		MHz
SET AND RESET OPERATION						
$t_{PHL(R)}$, $t_{PLH(S)}$	Propagation Delay Time	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		45	90	ns
$t_{WH(R)}$, $t_{WH(S)}$	Minimum Set and Reset Pulse Width	V_{DD} = 5V		90	180	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

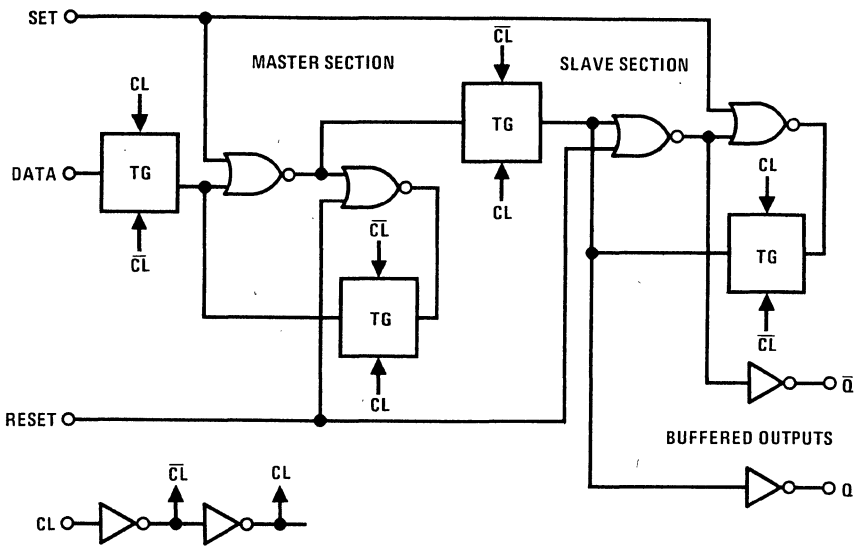
5

Schematic Diagram



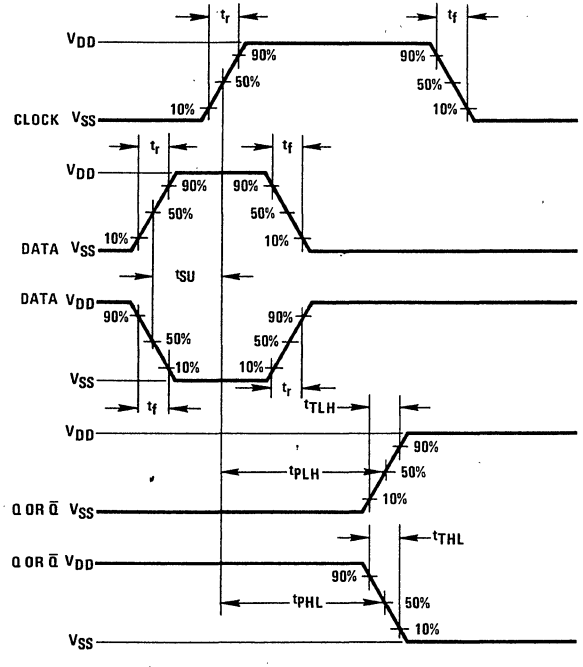
TL/F/5946-2

Logic Diagram



TL/F/5946-3

Switching Time Waveforms



TL/F/5946-4

National Semiconductor

CD4014BM/CD4014BC 8-Stage Static Shift Register

General Description

The CD4014BM/CD4014BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q outputs are available from the sixth, seventh and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control input is in the logical "1" state, data is jammed into each stage of the register synchronously with the positive transition of the clock.

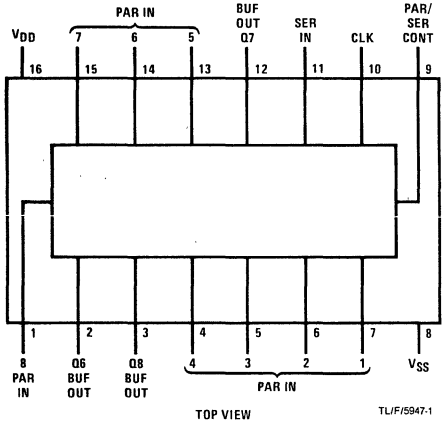
All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range—3.0V to 15V
- High noise immunity—0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5947-1

Truth Table

CL*	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q_n
⌐⌐	X	1	0	0	0	0
⌐⌐	X	1	1	0	1	0
⌐⌐	X	1	0	1	0	1
⌐⌐	X	1	1	1	1	1
⌐⌐	0	0	X	X	0	Q_{n-1}
⌐⌐	1	0	X	X	1	Q_{n-1}
⌐_	X	X	X	X	Q1	Q_n

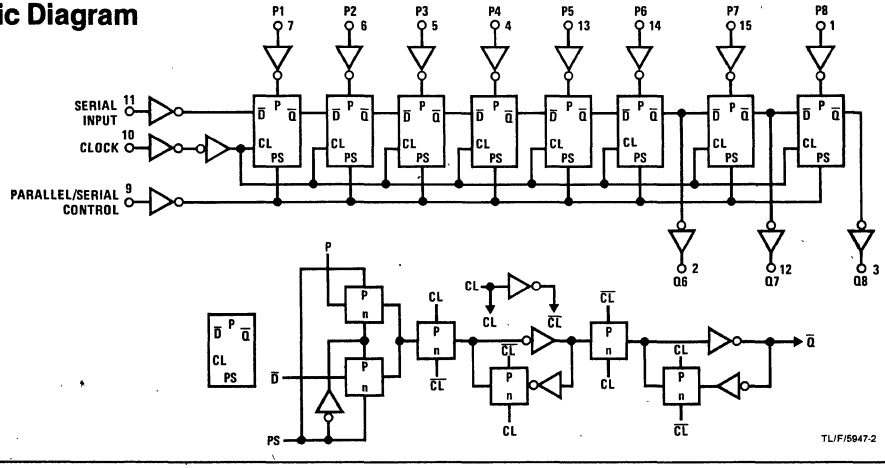
No Change

*Level change
X = Don't care case

Order Number CD4014BMJ or CD4014BCJ
See NS Package J16A

Order Number CD4014BMN or CD4014BCN
See NS Package N16E

Logic Diagram



TL/F/5947-2

Absolute Maximum Ratings
(Notes 1 & 2)

V_{DD}	Supply Voltage	−0.5 to +18 V
V_{IN}	Input Voltage	−0.5 to V_{DD} + 0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 sec.)	260°C

Recommended Operating Conditions
(Note 2)

V_{DD}	Supply Voltage	3.0 to 15 V
V_{IN}	Input Voltage	0 to V_{DD}
T_A	Operating Temperature Range	
	CD4014BM	−55°C to +125°C
	CD4014BC	40°C to 85°C

DC Electrical Characteristics (Note 2) — CD4014BM

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		5		0.1	5		150	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		10		0.2	10		300	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		20		0.3	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$ | $\|I_O\|<1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$ | $\|I_O\|<1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.6		1.3	2.2		0.90		mA
		$V_{DD}=15V$, $V_O=1.5V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD}=15V$, $V_O=13.5V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics (Note 2) — CD4014BC

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		20		0.1	20		150	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		40		0.2	40		300	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		80		0.3	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$ | $\|I_O\|<1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$ | $\|I_O\|<1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.2		0.90		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−2.2		−0.90		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		200	320	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		60	120	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Input Frequency	$V_{DD} = 5V$	2.8	4		MHz
		$V_{DD} = 10V$	6	12		MHz
		$V_{DD} = 15V$	8	16		MHz
t_W	Minimum Clock Pulse Width	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		25	50	ns
t_rCL, t_fCL	Clock Rise and Fall Time (Note 4)	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			15	μs
		$V_{DD} = 15V$			15	μs
t_s	Minimum Set-up Time (Note 6)					
	Serial Input	$V_{DD} = 5V$		60	120	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	60	ns
	Parallel Inputs	$V_{DD} = 5V$		80	160	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	60	ns
	Parallel/Serial Control	$V_{DD} = 5V$		100	200	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_H	Minimum Hold Time	$V_{DD} = 5V$			0	ns
	Serial In, Parallel In, $t_s \geq 400$ ns	$V_{DD} = 10V$			10	ns
	Parallel/Serial Control	$V_{DD} = 15V$			15	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			110		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

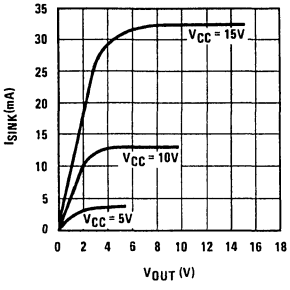
Note 3: I_{OL} and I_{OH} are tested one output at a time.

Note 4: If more than one unit is cascaded t_rCL should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

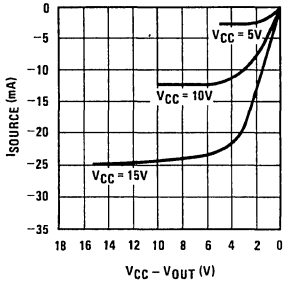
Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

Note 6: Set-up times are measured with reference to clock and a fixed hold time (t_H) as specified.

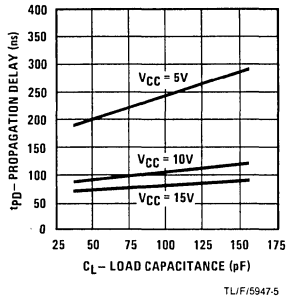
Typical Performance Characteristics



TL/F/5947-3



TL/F/5947-4



TL/F/5947-5

5

National Semiconductor

CD4015BM/CD4015BC Dual 4-Bit Static Shift Register

General Description

The CD4015BM/CD4015BC contains two identical, 4-stage, serial-input/parallel-output registers with independent "Data," "Clock," and "Reset" inputs. The logic level present at the input of each stage is transferred to the output of that stage at each positive-going clock transition. A logic high on the "Reset" input resets all four stages covered by that input. All inputs are protected from static discharge by a series resistor and diode clamps to V_{DD} and V_{SS}.

Features

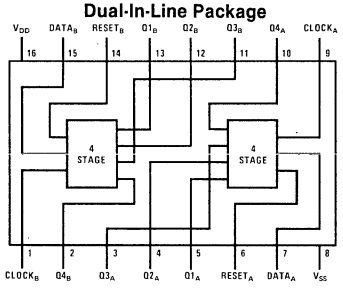
- Wide supply voltage range — 3.0V to 18V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Medium speed operation — 8MHz (typ) clock rate
- Fully static design — @ $V_{DD} - V_{SS} = 10$ Volts

Applications

- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General purpose register

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5948-1

CL▲	D	R	Q_1	Q_n	
⌐	0	0	0	Q_{n-1}	
⌐	1	0	1	Q_{n-1}	
⌐	X	0	Q_1	Q_n	(No change)
X	X	1	0	0	

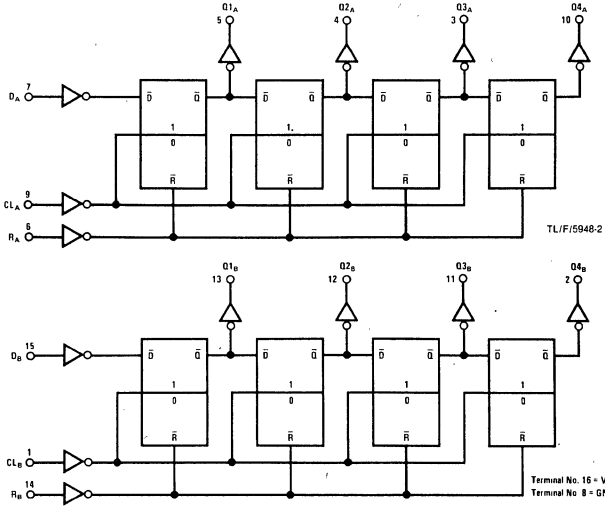
▲ Level change

X Don't care case.

Order Number CD4015BMJ or CD4015BCJ
See NS Package J16A

Order Number CD4015BMN or CD4015BCN
See NS Package N16E

Logic Diagrams



TL/F/5948-2

TL/F/5948-3

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD}	DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN}	Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S	Storage Temperature Range	−65 to +150 °C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

V_{DD}	DC Supply Voltage	+3 to +15 V_{DC}
V_{IN}	Input Voltage	0 to V_{DD} V_{DC}
T_A	Operating Temperature Range	
	CD4015BM	−55 °C to +125 °C
	CD4015BC	−40 °C to +85 °C

DC Electrical Characteristics (Note 2) — CD4015BM

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.005	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.010	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\|I_{OL}\|$ = 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\|I_{OL}\|$ = 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\|I_{OL}\|$ = 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\|I_{OL}\|$ = 1 μA	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\|I_{OL}\|$ = 1 μA	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\|I_{OL}\|$ = 1 μA	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V; or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

5

DC Electrical Characteristics (Note 2) — CD4015BC

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		20		0.005	20		150	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		40		0.010	40		300	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$ or 4.5V		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V		3.0		4.50	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_O=0.5V$; or 4.5V	3.5		3.5	2.75		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or 9.0V	7.0		7.0	5.50		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 50pF$, $R_L = 200K$, $t_r = t_f = 20ns$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Clocked Operation						
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		230	350	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		60	120	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WM}	Minimum Clock Pulse-Width	$V_{DD} = 5V$		160	250	ns
		$V_{DD} = 10V$		60	110	ns
		$V_{DD} = 15V$		50	85	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	$V_{DD} = 5V$			15	μS
		$V_{DD} = 10V$			15	μS
		$V_{DD} = 15V$			15	μS
t_{SU}	Minimum Data Set-Up Time	$V_{DD} = 5V$		50	100	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2	3.5		MHz
		$V_{DD} = 10V$	4.5	8		MHz
		$V_{DD} = 15V$	6	11		MHz
C_{IN}	Input Capacitance	Clock Input		7.5	10	pF
		Other Inputs		5	7.5	pF
Reset Operation						
$t_{PHL(R)}$	Propagation Delay Time	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	160	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		135	250	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		30	60	ns

National Semiconductor

CD4016BM/CD4016BC Quad Bilateral Switch

General Description

The CD4016BM/CD4016BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4066BM/CD4066BC.

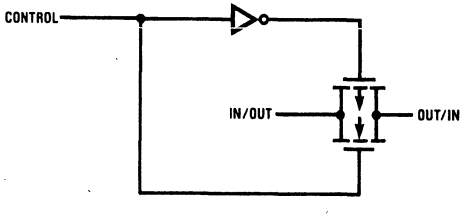
Features

- Wide supply voltage range — 3V to 15V
- Wide range of digital and analog switching — $\pm 7.5\ V_{PEAK}$
- "ON" resistance for 15V operation — 400Ω (typ.)
- Matched "ON" resistance over 15V signal input — $\Delta R_{ON} = 10\Omega$ (typ.)
- High degree of linearity — 0.4% distortion (typ.) @ f_{IS} = 1 kHz, $V_{IS} = 5\ V_{p-p}$, $V_{DD} - V_{SS} = 10V$, $R_L = 10\ k\Omega$
- Extremely low "OFF" switch leakage — 0.1 nA (typ.) @ $V_{DD} - V_{SS} = 10V$, $T_A = 25°C$
- Extremely high control input impedance — $10^{12}\Omega$ (typ.)
- Low crosstalk between switches — −50 dB (typ.) @ $f_{IS} = 0.9$ MHz, $R_L = 1\ k\Omega$
- Frequency response, switch "ON" — 40 MHz (typ.)

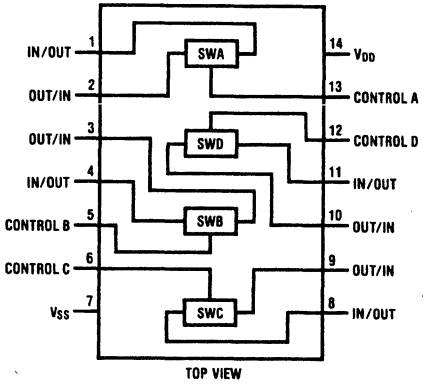
Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

Schematic and Connection Diagrams



Dual-In-Line Package



TL/F/5661–1

Order Number CD4016BMJ or CD4016BCJ
NS Package J14A

Order Number CD4016BMN or CD4016BCN
NS Package N14A

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to + 150°C
P_D Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4016BM	−55°C to +125°C
CD4016BC	−40°C to +85°C

DC Electrical Characteristics CD4016BM (Note 2)

Symbol	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		0.25		0.01	0.25		7.5	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		0.5		0.01	0.5		15	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		1.0		0.01	1.0		30	μA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ or V_{DD}								
		$V_{DD}=10V$		600		250	660		960	Ω
		$V_{DD}=15V$		360		200	400		600	Ω
		$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$								
		$V_{DD}=10V$, $V_{IS}=4.75$ to $5.25V$		1870		850	2000		2600	Ω
		$V_{DD}=15V$, $V_{IS}=7.25$ to $7.75V$		775		400	850		1230	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches (In Same Package)	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=10V$				15				Ω
		$V_{DD}=15V$				10				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C=0$, $V_{DD}=15V$		±50		±0.1	±50		±500	nA
		$V_{IS}=15V$ and 0V,								
		$V_{OS}=0V$ and 15V								
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS}=V_{SS}$ and V_{DD}								
		$V_{OS}=V_{DD}$ and V_{SS}								
		$I_{IS}=\pm 10\ \mu A$								
		$V_{DD}=5V$		0.9			0.7		0.5	V
		$V_{DD}=10V$		0.9			0.7		0.5	V
		$V_{DD}=15V$		0.9			0.7		0.5	V
V_{IHC}	High Level Input Voltage	$V_{DD}=5V$	3.5		3.5			3.5		V
		$V_{DD}=10V$ (see Note 6 and	7.0		7.0			7.0		V
		$V_{DD}=15V$ *Figure 8*)	11.0		11.0			11.0		V
I_{IN}	Input Current	$V_{DD}-V_{SS}=15V$		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA
		$V_{DD}\geq V_{IS}\geq V_{SS}$								
		$V_{DD}\geq V_C\geq V_{SS}$								

DC Electrical Characteristics CD4016BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		1.0		0.01	1.0		7.5	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		2.0		0.01	2.0		15	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		4.0		0.01	4.0		30	μA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ or V_{DD}								
		$V_{DD}=10V$		610		275	660		840	Ω
		$V_{DD}=15V$		370		200	400		520	Ω
		$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$								
		$V_{DD}=10V$, $V_{IS}=4.75$ to $5.25V$		1900		850	2000		2380	Ω
		$V_{DD}=15V$, $V_{IS}=7.25$ to $7.75V$		790		400	850		1080	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches (In Same Package)	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$								
		$V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=10V$				15				Ω
		$V_{DD}=15V$				10				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C=0$, $V_{DD}=15V$		±50		±0.1	±50		±200	nA
		$V_{IS}=0V$ or $15V$,								
		$V_{OS}=15V$ or $0V$								
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS}=V_{SS}$ and V_{DD}								
		$V_{OS}=V_{DD}$ and V_{SS}								
		$I_{IS}=\pm 10\ \mu A$								
		$V_{DD}=5V$		0.9			0.7		0.4	V
		$V_{DD}=10V$		0.9			0.7		0.4	V
		$V_{DD}=15V$		0.9			0.7		0.4	V
V_{IHC}	High Level Input Voltage	$V_{DD}=5V$	3.5		3.5			3.5		V
		$V_{DD}=10V$ (see Note 6 and	7.0		7.0			7.0		V
		$V_{DD}=15V$ *Figure 8*)	11.0		11.0			11.0		V
I_{IN}	Input Current	$V_{CC}-V_{SS}=15V$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA
		$V_{DD}\geq V_{IS}\geq V_{SS}$								
		$V_{DD}\geq V_C\geq V_{SS}$								

AC Electrical Characteristics $T_A=25°C$, $t_r=t_f=20$ ns and $V_{SS}=0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C=V_{DD}$, $C_L=50$ pF, (*Figure 1*)				
		$R_L=200k$				
		$V_{DD}=5V$		58	100	ns
		$V_{DD}=10V$		27	50	ns
		$V_{DD}=15V$		20	40	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal	$R_L=1.0\ k\Omega$, $C_L=50$ pF, (*Figures 2* and *3*)				
	Output High Impedance to Logical Level	$V_{DD}=5V$		20	50	ns
		$V_{DD}=10V$		18	40	ns
		$V_{DD}=15V$		17	35	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time *Control Input to Signal*	$R_L=1.0\ k\Omega$, $C_L=50$ pF, (*Figures 2* and *3*)				
	Output Logical Level to High Impedance	$V_{DD}=5V$		15	40	ns
		$V_{DD}=10V$		11	25	ns
		$V_{DD}=15V$		10	22	ns
	Sine Wave Distortion	$V_C=V_{DD}=5V$, $V_{SS}=-5$		0.4		%
		$R_L=10\ k\Omega$, $V_{IS}=5\ V_{P-P}$, $f=1$ kHz, (*Figure 4*)				

AC Electrical Characteristics (Continued)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Frequency Response — Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5\ V_{P-P}$, $20\ \text{Log}_{10}\ V_{OS}/V_{OS}$ (1 kHz) −dB, (*Figure 4*)		40		MHz
	Feedthrough — Switch "OFF" (Frequency at −50 dB)	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5\ V_{P-P}$, $20\ \text{Log}_{10}\ (V_{OS}/V_{IS}) = -50$ dB, (*Figure 4*)		1.25		MHz
	Crosstalk Between Any Two Switches (Frequency at −50 dB)	$V_{DD} = V_{C(A)} = 5V$; $V_{SS} = V_{C(B)} = -5V$, $R_L = 1\ k\Omega V_{IS(A)} = 5\ V_{P-P}$, $20\ \text{Log}_{10}\ (V_{OS(B)}/V_{OS(A)}) = -50$ dB, (*Figure 5*)		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$ $R_{IN} = 1\ k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$ pF (*Figure 6*)		150		mV_{P-P}
	Maximum Control Input	$R_L = 1\ k\Omega$, $C_L = 50$ pF, (*Figure 7*) $V_{OS(f)} = \frac{1}{2} V_{OS}$(1 kHz)				
		$V_{DD} = 5V$		6.5		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		9.0		MHz
C_{IS}	Signal Input Capacitance			4		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		4		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0V$		0.2		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: If the switch input is held at V_{DD}, V_{IHC} is the control input level that will cause the switch output to meet the standard "B" series V_{OH} and I_{OH} output levels. If the analog switch input is connected to V_{SS}, V_{IHC} is the control input level — which allows the switch to *sink* standard "B" series $|I_{OH}|$, high level current, and still maintain a $V_{OL} \leq$ "B" series. These currents are shown in *Figure 8*.

AC Test Circuits and Switching Time Waveforms

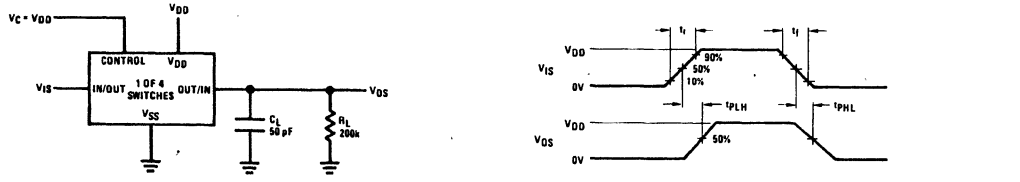
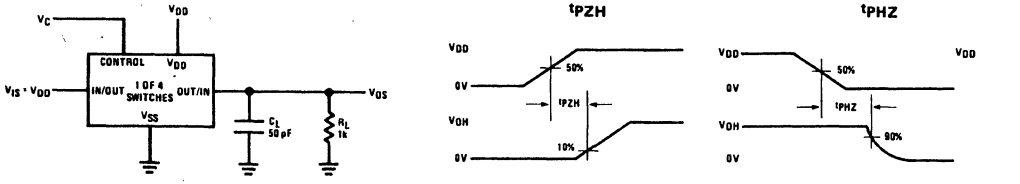


Figure 1. t_{PLH}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



TL/H/5661–2

FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

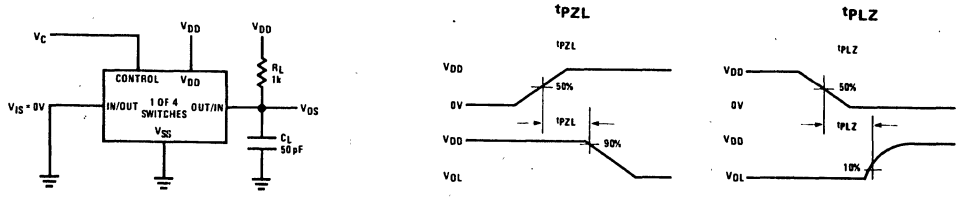


FIGURE 3. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

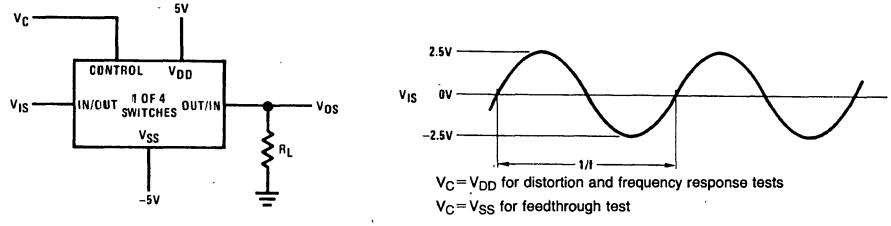


FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

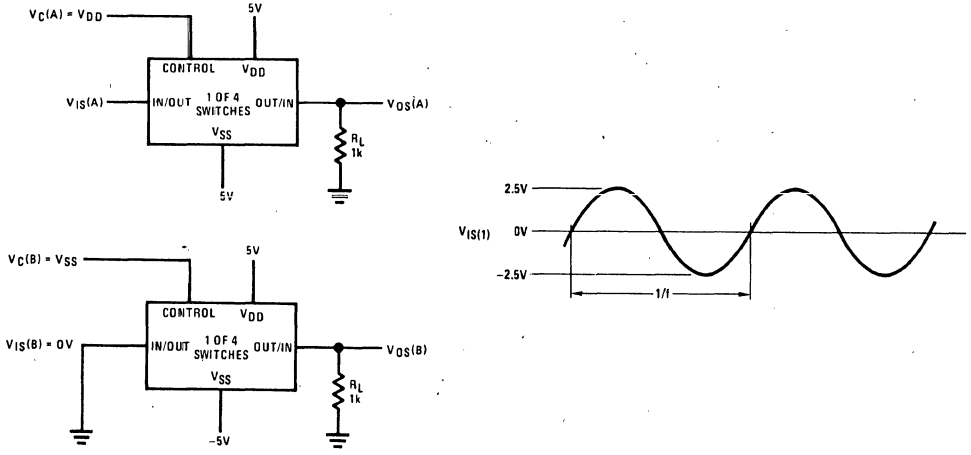
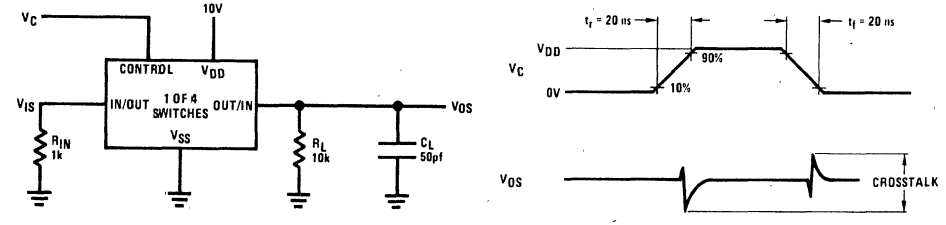


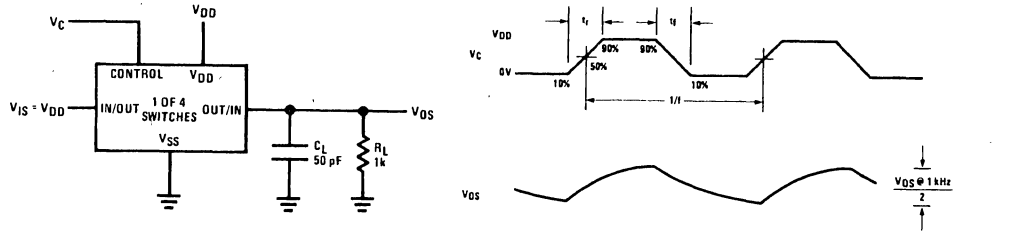
FIGURE 5. Crosstalk Between Any Two Switches



TL/H/5661–3

FIGURE 6. Crosstalk — Control to Input Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)



TL/H/5661–4

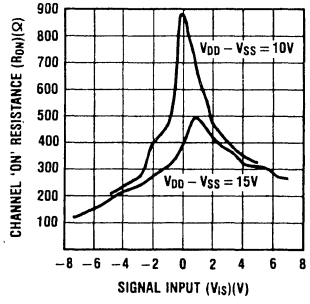
FIGURE 7. Maximum Control Input Frequency

Temperature Range	V_{DD}	Switch Input				Switch Output $V_{OS(V)}$	
		V_{IS}	I_{IS} (mA)				
			T_{LOW}	25°C	T_{HIGH}	Min	Max
MILITARY	5	0	0.25	0.2	0.14		0.4
	5	5	−0.25	−0.2	−0.14	4.6	
	10	0	0.62	0.5	0.35		0.5
	10	10	−0.62	−0.5	−0.35	9.5	
	15	0	1.8	1.5	1.1		1.5
	15	15	−1.8	−1.5	−1.1	13.5	
COMMERCIAL	5	0	0.2	0.16	0.12		0.4
	5	5	−0.2	−0.16	−0.12	4.6	
	10	0	0.5	0.4	0.3		0.5
	10	10	−0.5	−0.4	−0.3	9.5	
	15	0	1.4	1.2	1.0		1.5
	15	15	−1.4	−1.2	−1.0	13.5	

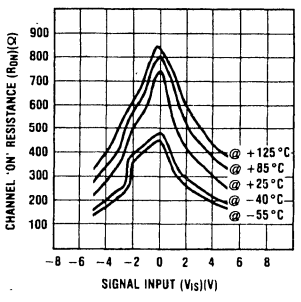
FIGURE 8. CD4016B Switch Test Conditions for V_{IHC}

Typical Performance Characteristics

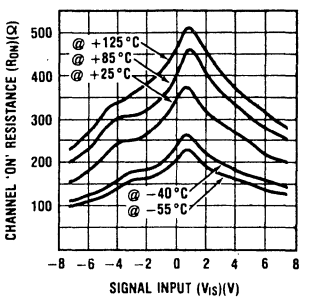
'ON' Resistance vs. Signal Voltage $T_A = 25°C$



'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 10V$



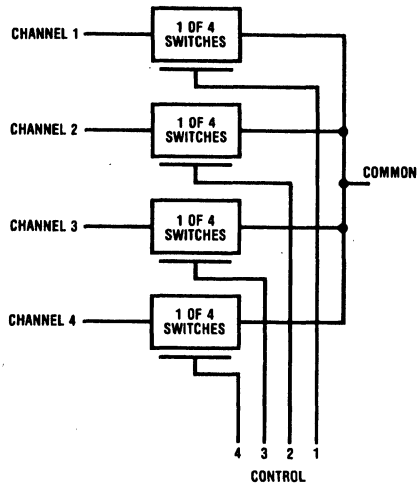
'ON' Resistance Temperature Variation for $V_{DD} - V_{SS} = 15V$



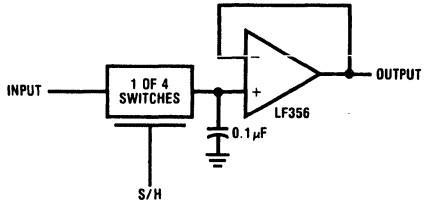
TL/H/5661–5

Typical Applications

4 Input Multiplexer



Sample/Hold Amplifier



TL/H/5661–6

Special Considerations

The CD4016B is composed of 4, two-transistor analog switches. These switches do not have any linearization or compensation circuitry for "R_{ON}" as do the CD4066B's. Because of this, the special operating considerations for the CD4066B do not apply to the CD4016B, but at low supply voltages, ≤5V, the CD4016B's on resistance becomes non-linear. It is recommended that at 5V, voltages on the in/out pins be maintained within about 1V of either V_{DD} or V_{SS}; and that at 3V the voltages on the in/out pins should be at V_{DD} or V_{SS} for reliable operation.

National Semiconductor

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs
CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BM/CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BM/CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BM/CD4017BC and CD4022BM/CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

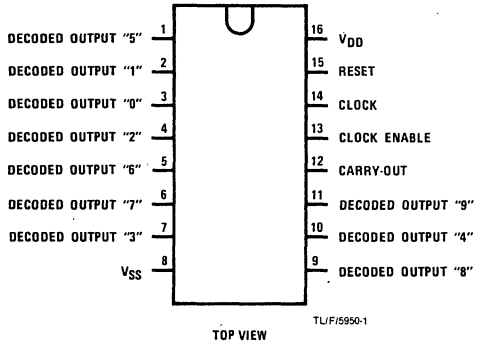
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	5.0 MHz (typ.) with 10V V_{DD}
■ Low power	10 μW (typ.)
■ Fully static operation	

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

Connection Diagrams

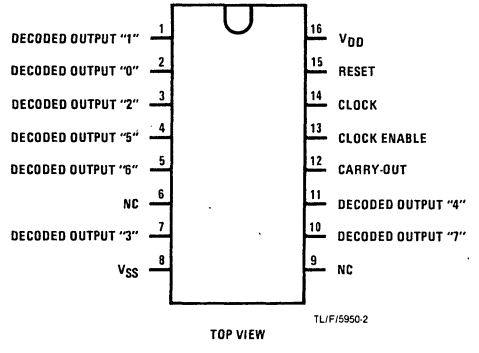
CD4017B
Dual-In-Line Package



TOP VIEW

Order Number CD4017BMJ, CD4017BCJ, CD4022BMJ or CD4022BCJ
See NS Package J16A

CD4022B
Dual-In-Line Package



TOP VIEW

Order Number CD4017BMN, CD4017BCN, CD4022BMN or CD4022BCN
See NS Package N16E

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4017BM, CD4022BM	−55°C to +125°C
CD4017BC, CD4022BC	−40°C to +85°C

DC Electrical Characteristics CD4017BM, CD4022BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.3	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.5	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.36		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−0.9		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4017BC, CD4022BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.5	20		150	μA
		V_{DD} = 10V		40		1.0	40		300	μA
		V_{DD} = 15V		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4017BC, CD4022BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.36		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.9		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200 k, t_{rCL} and t_{fCL} = 20 ns, unless otherwise specified

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time:					
	Carry Out Line	V_{DD} = 5V		415	800	ns
		V_{DD} = 10V		160	320	ns
		V_{DD} = 15V		130	250	ns
	Carry Out Line	V_{DD} = 5V, C_L = 15 pF		240	480	ns
		V_{DD} = 10V, C_L = 15 pF		85	170	ns
		V_{DD} = 15V, C_L = 15 pF		70	140	ns
	Decode Out Lines	V_{DD} = 5V		500	1000	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		160	320	ns
t_{TLH}, t_{THL}	Transition Time Carry Out and Decode Out Lines					
	t_{TLH}	V_{DD} = 5V		200	360	ns
		V_{DD} = 10V		100	180	ns
		V_{DD} = 15V		80	130	ns
	t_{THL}	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V, Measured with Respect to Carry Output Line	1.0	2		MHz
		V_{DD} = 10V, Measured with Respect to Carry Output Line	2.5	5		MHz
		V_{DD} = 15V, Measured with Respect to Carry Output Line	3.0	6		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		45	90	ns
		V_{DD} = 15V		35	70	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	V_{DD} = 5V			20	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			5	μs
t_{SU}	Minimum Clock Inhibit Data Set-Up Time	V_{DD} = 5V		120	240	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
C_{IN}	Average Input Capacitance			5	7.5	pF

5

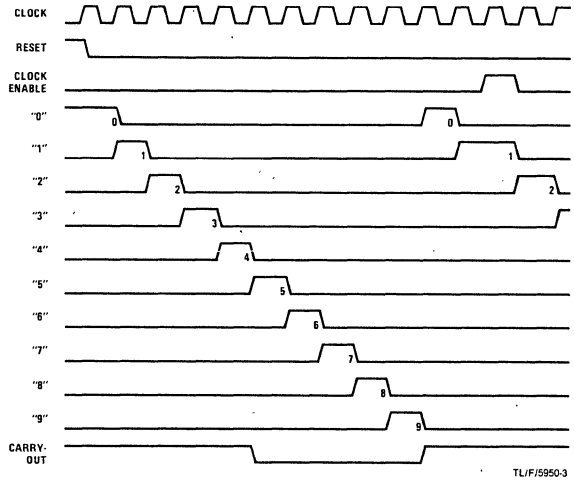
AC Electrical Characteristics (Cont'd.)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, t_{rCL} and $t_{fCL} = 20$ ns, unless otherwise specified.

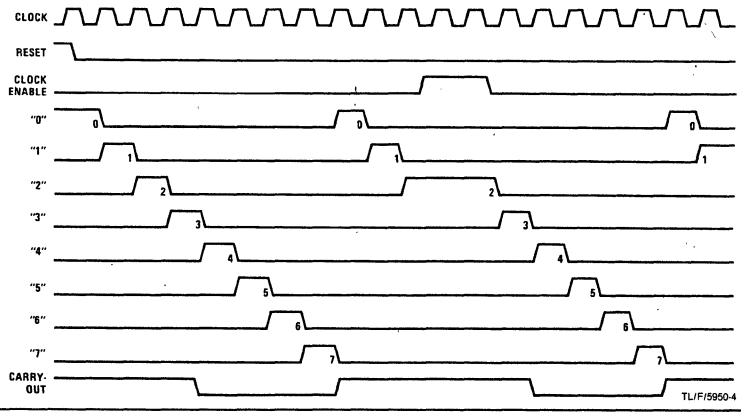
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
RESET OPERATION						
t_{PHL}	Propagation Delay Time: Carry Out Line	$V_{DD} = 5V$		415	800	ns
		$V_{DD} = 10V$		160	320	ns
		$V_{DD} = 15V$		130	250	ns
	Carry Out Line	$V_{DD} = 5V$, $C_L = 15$ pF		240	480	ns
		$V_{DD} = 10V$, $C_L = 15$ pF		85	170	ns
		$V_{DD} = 15V$, $C_L = 15$ pF		70	140	ns
	Decode Out Lines	$V_{DD} = 5V$		500	1000	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{WH}	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		55	110	ns
t_{REM}	Minimum Reset Removal Time	$V_{DD} = 5V$		75	150	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns

Timing Diagrams

CD4017B

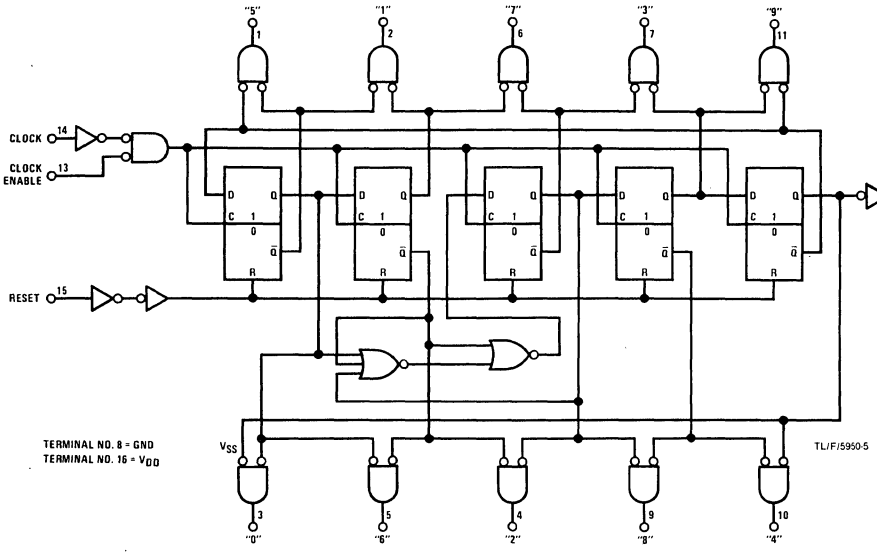


CD4022B

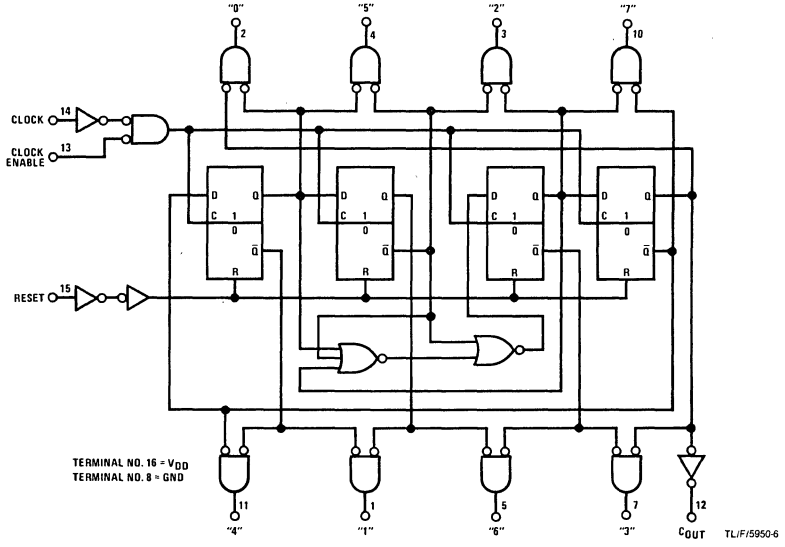


Logic Diagrams

CD4017B



CD4022B



5

National Semiconductor

CD4018BM/CD4018BC Presettable Divide-by-N Counter

General Description

The CD4018B consists of 5 Johnson counter stages. A buffered $\overline{Q}$ output from each stage, "CLOCK", "RESET", "DATA", "PRESET ENABLE", and 5 individual "JAM" inputs are provided. The counter is advanced one count at the positive clock signal transition. A high "RESET" signal clears the counters to an "ALL ZERO" condition. A high "PRESET ENABLE" signal allows information on the "JAM" inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

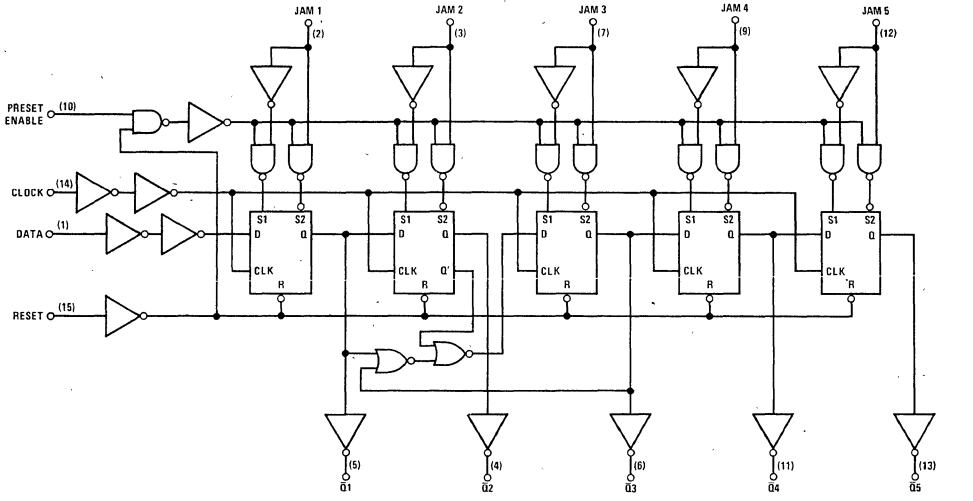
Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Fully static operation

Applications

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counter
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide by "N" counters/frequency synthesizers

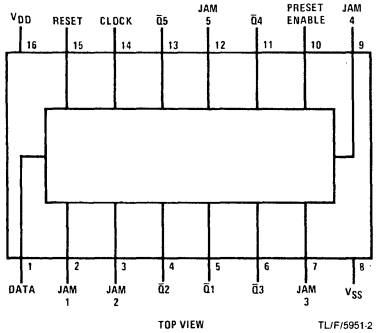
Logic Diagram



TL/F/5951-1

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5951-2

Order Number CD4018BMJ or CD4018BCJ
See NS Package J16A

Order Number CD4018BMN or CD4018BCN
See NS Package N16E

Absolute Maximum Ratings (Note 1)

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4018BM	−55°C to +125°C
CD4018BC	−40°C to +85°C

DC Electrical Characteristics CD4018BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.3	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.5	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4018BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.5	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		1.0	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics (Continued) CD4018BC

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input $t_r = t_f$ = 20 ns, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time to $\overline{Q}$	V_{DD} = 5V		235	700	ns
		V_{DD} = 10V		95	250	ns
		V_{DD} = 15V		70	200	ns
t_{THL}, t_{TLH}	Transition Time $\overline{Q}$ Outputs	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		50	100	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	500	ns
		V_{DD} = 10V		50	200	ns
		V_{DD} = 15V		40	160	ns
t_{RCL}, t_{FCL}	Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
t_{SU}	Minimum Data Input Set-Up Time	V_{DD} = 5V		40	200	ns
		V_{DD} = 10V		20	100	ns
		V_{DD} = 15V		16	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1	4		MHz
		V_{DD} = 10V	3	9		MHz
		V_{DD} = 15V	5	14		MHz
PRESET OR RESET OPERATION						
$t_{PLH(R)}$ $t_{PHL(PR)}$ $t_{PLH(PR)}$	Propagation Delay Time to $\overline{Q}$	V_{DD} = 5V		235	750	ns
		V_{DD} = 10V		95	250	ns
		V_{DD} = 15V		70	200	ns
$t_{WH(R)}$ $t_{WH(PR)}$	Minimum Preset or Reset Pulse Width	V_{DD} = 5V		100	400	ns
		V_{DD} = 10V		40	160	ns
		V_{DD} = 15V		30	120	ns
t_{REM}	Minimum Preset or Reset Removal Time	V_{DD} = 5V		100	400	ns
		V_{DD} = 10V		40	160	ns
		V_{DD} = 15V		30	120	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		63		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

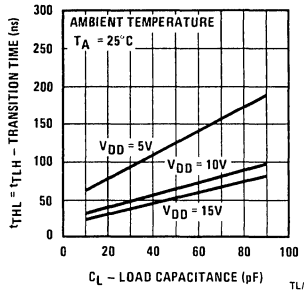
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note, AN-90.

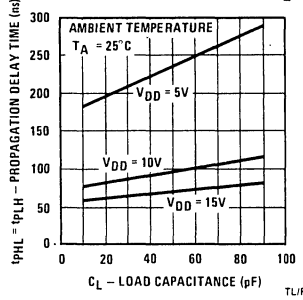
Typical Performance Characteristics

Typical Transition Time vs C_L



TL/F/5951-3

Typical Propagation Delay vs. C_L



TL/F/5951-4

External Connections

External Connections for Divide by 10, 9, 8, 7, 6, 5, 4, 3, 2, Operation

Divide By 10 — $\overline{Q}5$
Divide By 8 — $\overline{Q}4$
Divide By 6 — $\overline{Q}3$
Divide By 4 — $\overline{Q}2$
Divide By 2 — $\overline{Q}1$

} Connected Back To "DATA" Input

Divide By 9

TL/F/5951-5

Divide By 7

TL/F/5951-6

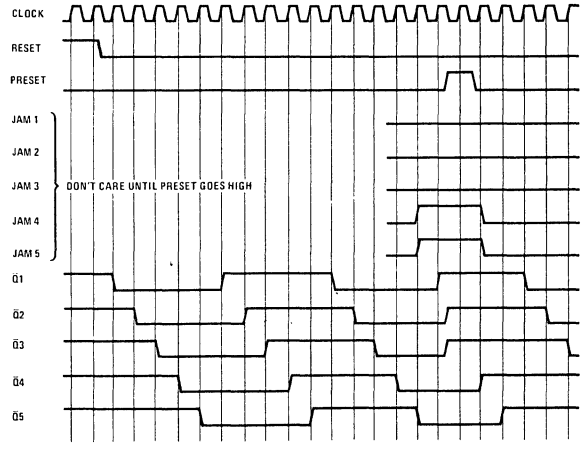
Divide By 5

TL/F/5951-7

Divide By 3

TL/F/5951-8

Timing Diagram



TL/F/5951-9

Note. "Data" input tied to $\overline{Q}5$ for decade counter configuration.

5

National Semiconductor

CD4019BM/CD4019BC Quad AND-OR Select Gate

General Description

The CD4019BM/CD4019BC is a complementary MOS quad AND-OR select gate. Low power and high noise margin over a wide voltage range is possible through implementation of N and P-channel enhancement mode transistors. These complementary MOS (CMOS) transistors provide the building blocks for the 4 "AND-OR select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B. All inputs are protected against static discharge damage.

Features

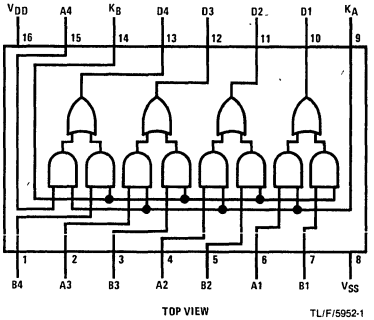
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

Applications

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/EXCLUSIVE-OR selection

Connection Diagram

Dual-In-Line Package

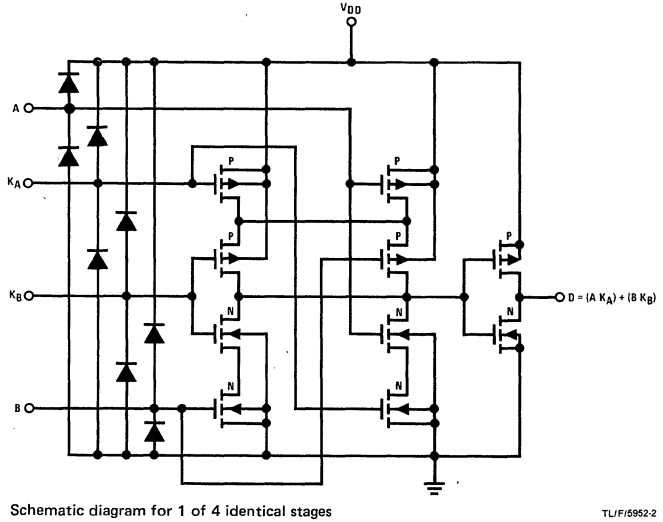


TOP VIEW TL/F/5952-1

Order Number CD4019BMJ or CD4019BCJ
See NS Package J16A

Order Number CD4019BMN or CD4019BCN
See NS Package N16E

Schematic Diagram



Schematic diagram for 1 of 4 identical stages TL/F/5952-2

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD} V
T_A Operating Temperature Range	
CD4019BM	−55°C to +125°C
CD4019BC	−40°C to +85°C

DC Electrical Characteristics CD4019BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.03	0.25		7.5	μA
		V_{DD} = 10V		0.5		0.05	0.5		15	μA
		V_{DD} = 15V		1.0		0.07	1.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	1		0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.5		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	10		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.4		−0.14		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−1.0		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.0		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD4019BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.03	1		7.5	μA
		V_{DD} = 10V		2		0.05	2		15	μA
		V_{DD} = 15V		4		0.07	4		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	1		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.5		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	10		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.4		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−1.0		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.0		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200 k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Input to Output	V_{DD} = 5V		100	300	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		45	100	ns
t_{THL}	High-to-Low Level Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{TLH}	Low-to-High Level Transition Time	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		50	100	ns
C_{IN}	Input Capacitance	All A and B Inputs		5	7.5	pF
		K_A and K_B Inputs		10	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

National Semiconductor

CD4020BM/CD4020BC 14-Stage Ripple Carry Binary Counters
CD4040BM/CD4040BC 12-Stage Ripple Carry Binary Counters
CD4060BM/CD4060BC 14-Stage Ripple Carry Binary Counters

General Description

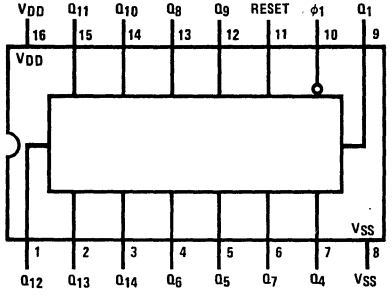
The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

Features

■ Wide supply voltage range	1.0V to 15V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	8MHz typ. at V_{DD} = 10V
■ Schmitt trigger clock input	

Connection Diagrams Dual-In-Line Packages/Top Views

CD4020BM/CD4020BC

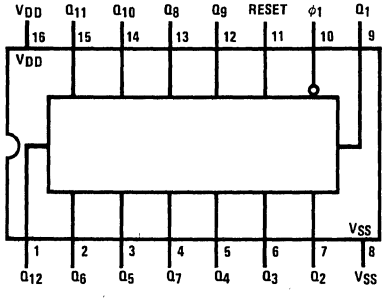


TL/F/5953-1

Order Number CD4020BMJ, CD4020BCJ, CD4040BMJ, CD4040BCJ, CD4060BMJ or CD4060BCJ
See NS Package J16A

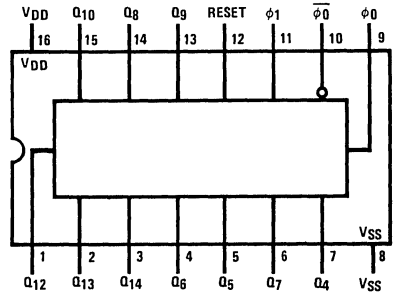
Order Number CD4020BMN, CD4020BCN, CD4040BMN, CD4040BCN, CD4060BMN or CD4060BCN
See NS Package N16E

CD4040BM/CD4040BC



TL/F/5953-2

CD4060BM/CD4060BC



TL/F/5953-3

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5V to +18V
V_{IN}	Input Voltage	−0.5V to V_{DD} + 0.5V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500mW
T_L	Lead Temperature (soldering, 10 seconds)	260°C

Recommended Operating Conditions

V_{DD}	Supply Voltage	+3V to +15V
V_{IN}	Input Voltage	0V to V_{DD}
T_A	Operating Temperature Range	
	CD40XXBM	−55°C to +125°C
	CD40XXBC	−40°C to +85°C

DC Electrical Characteristics CD40XXBM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Data does not apply to oscillator points ϕ_0 and $\overline{\phi_0}$ of CD4060BM/CD4060BC. I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics 40XXBC (Note 2)

SYMBOL	PARAMETER	CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	3.0		3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics CD4020BM/CD4020BC, CD4040BM/CD4040BC

T_A = 25°C, C_L = 50pF, R_L = 200k, t_r = t_f = 20ns, unless otherwise noted.

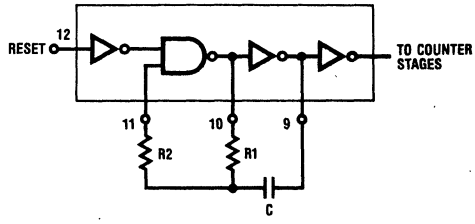
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL1}, t_{PLH1}	Propagation Delay Time to Q_1	V_{DD} = 5V		250	550	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		75	150	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	V_{DD} = 5V		150	330	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		45	90	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	335	ns
		V_{DD} = 10V		50	125	ns
		V_{DD} = 15V		40	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			no limit	ns
		V_{DD} = 10V			no limit	ns
		V_{DD} = 15V			no limit	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	4		MHz
		V_{DD} = 10V	4	10		MHz
		V_{DD} = 15V	5	12		MHz
$t_{PHL(R)}$	Reset Propagation Delay	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
C_{in}	Average Input Capacitance	Any Input		5	7.5	pF
C_{pd}	Power Dissipation Capacitance			50		pF

AC Electrical Characteristics CD4060BM/CD4060BC $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, $t_r = t_f = 20\,ns$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL4}, t_{PLH4}	Propagation Delay Time to Q_4	$V_{DD} = 5V$		550	1300	ns
		$V_{DD} = 10V$		250	525	ns
		$V_{DD} = 15V$		200	400	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		170	500	ns
		$V_{DD} = 10V$		65	170	ns
		$V_{DD} = 15V$		50	125	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$			no limit	ns
		$V_{DD} = 10V$			no limit	ns
		$V_{DD} = 15V$			no limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1	3		MHz
		$V_{DD} = 10V$	3	8		MHz
		$V_{DD} = 15V$	4	10		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
C_{in}	Average Input Capacitance	Any Input		5	7.5	pF
C_{pd}	Power Dissipation Capacitance			50		pF

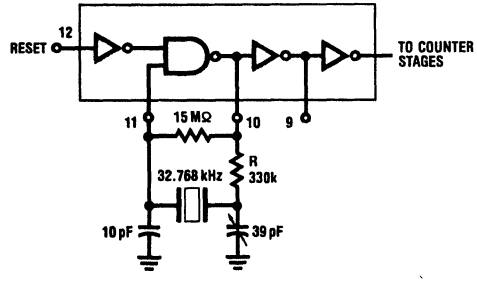
CD4060B Typical Oscillator Connections

RC Oscillator



TL/F/5953-4

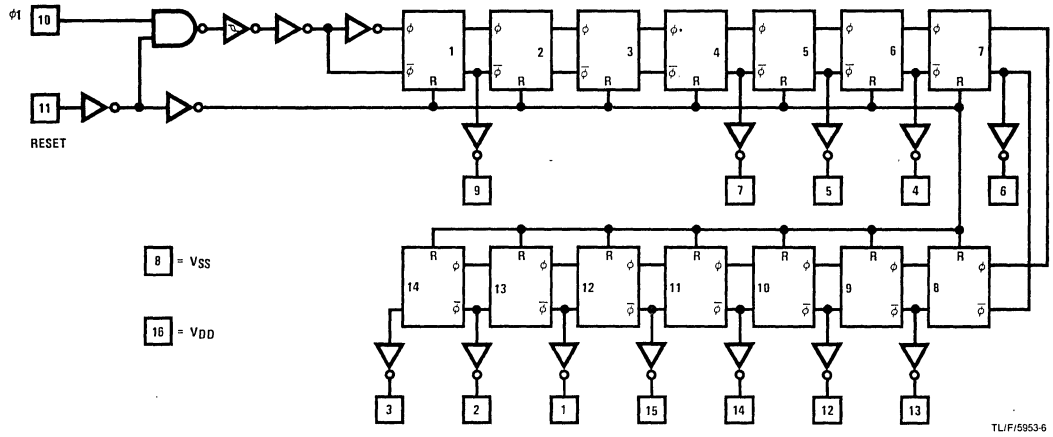
Crystal Oscillator



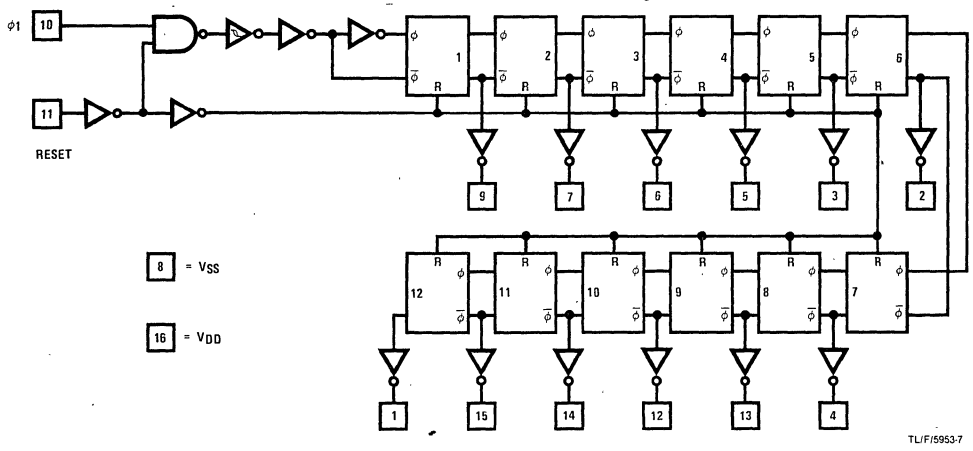
TL/F/5953-5

Schematic Diagrams

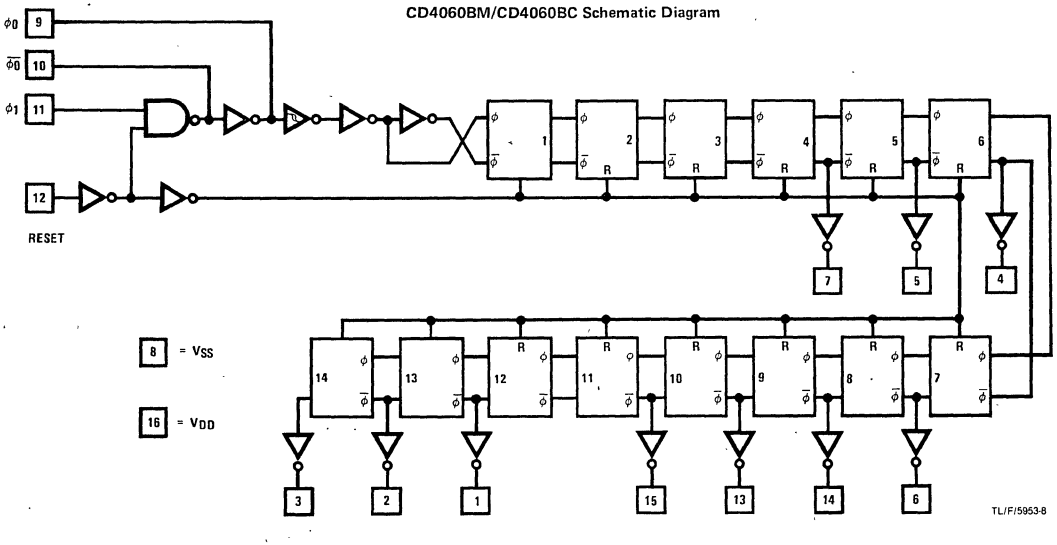
CD4020BM/CD4020BC Schematic Diagram



CD4040BM/CD4040BC Schematic Diagram



CD4060BM/CD4060BC Schematic Diagram



National Semiconductor

CD4021BM/CD4021BC 8-Stage Static Shift Register

General Description

The CD4021BM/CD4021BC is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual JAM inputs to each of 8 stages. Q output are available from the sixth, seventh, and eighth stages. All outputs have equal source and sink current capabilities and conform to standard "B" series output drive.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical "1" state, data is jammed into each stage of the register asynchronously with the clock.

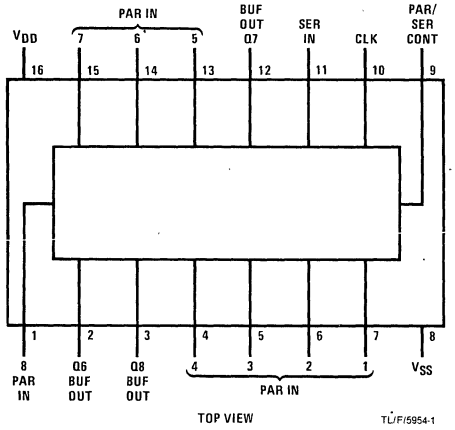
All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5954-1

Truth Table

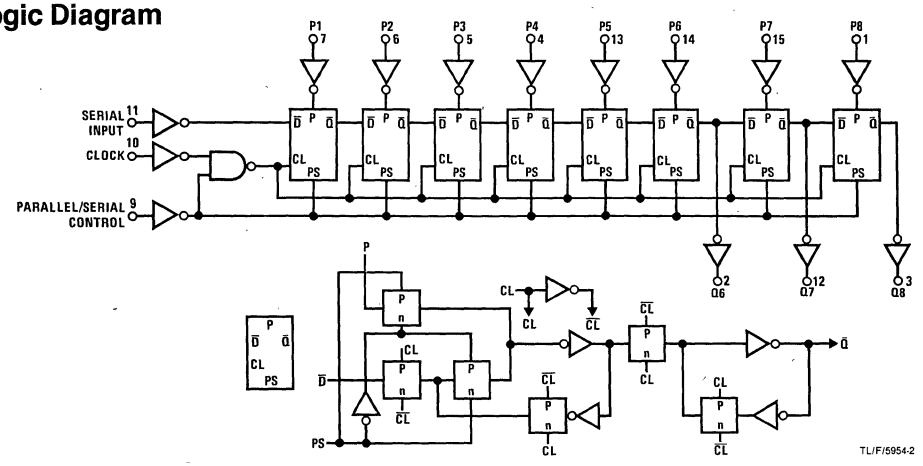
CL*	Serial Input	Parallel/ Serial Control	PI 1	PI n	Q1 (Internal)	Q_n	
X	X	1	0	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⌒	0	0	X	X	0	Q_{n-1}	
⌒	1	0	X	X	1	Q_{n-1}	
⌒	X	0	X	X	Q1	Q_n	No Change

*Level change
X = Don't care case

Order Number CD4021BMJ or CD4021BCJ
See NS Package J16A

Order Number CD4021BMN or CD4021BCN
See NS Package N16E

Logic Diagram



TL/F/5954-2

Absolute Maximum Ratings (Notes 1 & 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD} Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4021BM	−55°C to +125°C
CD4021BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4021BM

SYM	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		5		0.1	5		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		10		0.2	10		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		20		0.3	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$ | $\|I_O\|<1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$ | $\|I_O\|<1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or 4.5V		1.5		2	1.5		1.5	V
		$V_{DD}=10V, V_O=1.0V$ or 9.0V		3.0		4	3.0		3.0	V
		$V_{DD}=15V, V_O=1.5V$ or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or 4.5V	3.5		3.5	3		3.5		V
		$V_{DD}=10V, V_O=1.0V$ or 9.0V	7.0		7.0	6		7.0		V
		$V_{DD}=15V, V_O=1.5V$ or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V, V_O=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V, V_O=0.5V$	1.6		1.3	2.2		0.90		mA
		$V_{DD}=15V, V_O=1.5V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V, V_O=4.6V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD}=10V, V_O=9.5V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD}=15V, V_O=13.5V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V, V_{IN}=0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD}=15V, V_{IN}=15V$		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics (Note 2) — CD4021BC

SYM	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V, V_{IN}=V_{DD}$ or V_{SS}		20		0.1	20		150	μA
		$V_{DD}=10V, V_{IN}=V_{DD}$ or V_{SS}		40		0.2	40		300	μA
		$V_{DD}=15V, V_{IN}=V_{DD}$ or V_{SS}		80		0.3	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$ | $\|I_O\|<1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$ | $\|I_O\|<1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$ | $\|I_O\|<1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$ | $\|I_O\|<1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or 4.5V		1.5		2	1.5		1.5	V
		$V_{DD}=10V, V_O=1.0V$ or 9.0V		3.0		4	3.0		3.0	V
		$V_{DD}=15V, V_O=1.5V$ or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V, V_O=0.5V$ or 4.5V	3.5		3.5	3		3.5		V
		$V_{DD}=10V, V_O=1.0V$ or 9.0V	7.0		7.0	6		7.0		V
		$V_{DD}=15V, V_O=1.5V$ or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V, V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V, V_O=0.5V$	1.3		1.1	2.2		0.90		mA
		$V_{DD}=15V, V_O=1.5V$	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V, V_O=4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V, V_O=9.5V$	−1.3		−1.1	−2.2		−0.90		mA
		$V_{DD}=15V, V_O=13.5V$	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V, V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15V, V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, input t_r, $t_f = 20$ ns, $C_L = 50$ pF, $R_L = 200$ kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay Time	$V_{DD} = 5V$		240	350	ns
		$V_{DD} = 10V$		100	175	ns
		$V_{DD} = 15V$		70	140	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Input Frequency	$V_{DD} = 5V$	2.5	3.5		MHz
		$V_{DD} = 10V$	5	10		MHz
		$V_{DD} = 15V$	8	16		MHz
t_W	Minimum Clock Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_rCL, t_fCL	Clock Rise and Fall Time (Note 4)	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			15	μs
		$V_{DD} = 15V$			15	μs
t_s	Minimum Set-up Time					
	Serial Input	$V_{DD} = 5V$		60	120	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		40	80	ns
	(Ref. to CL)	$V_{DD} = 15V$		30	60	ns
	Parallel Inputs	$V_{DD} = 5V$		25	50	ns
	$t_H \geq 200$ ns	$V_{DD} = 10V$		15	30	ns
	(Ref. to P/S)	$V_{DD} = 15V$		10	20	ns
t_H	Minimum Hold Time	$V_{DD} = 5V$			0	ns
	Serial In, Parallel In, $t_s \geq 400$ ns	$V_{DD} = 10V$			10	ns
	Parallel/Serial Control	$V_{DD} = 15V$			15	ns
t_{WH}	Minimum P/S Pulse Width	$V_{DD} = 5V$		150	250	ns
		$V_{DD} = 10V$		75	125	ns
		$V_{DD} = 15V$		50	100	ns
t_{REM}	Minimum P/S Removal Time	$V_{DD} = 5V$		100	200	ns
	(Ref. to CL)	$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 5)			100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

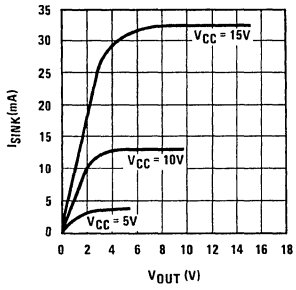
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

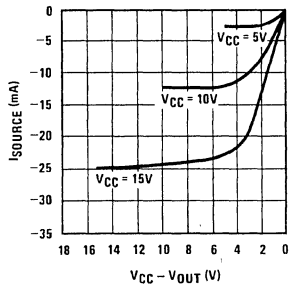
Note 4: If more than one unit is cascaded t_rCL should be made less than or equal to the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

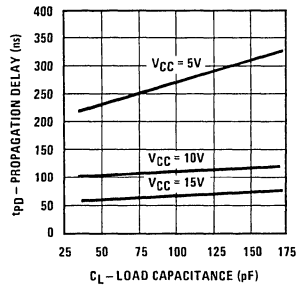
Typical Performance Characteristics



TL/F/5954-3



TL/F/5954-4



TL/F/5954-5

5

National Semiconductor

CD4023M/CD4023C Triple 3-Input NAND Gate
CD4025M/CD4025C Triple 3-Input NOR Gate

General Description

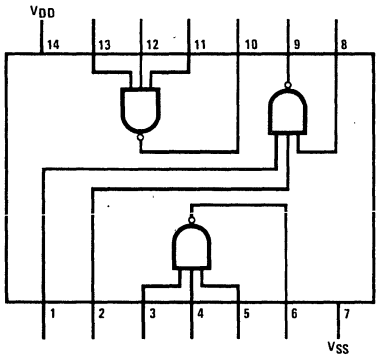
These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ 5-10 V parametric ratings	
■ Low Power	

Connection Diagrams Dual-In-Line Packages

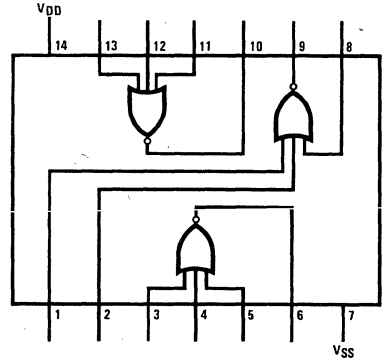
CD4023M/CD4023C



TOP VIEW

TL/F/5955-1

CD4025M/CD4025C



TOP VIEW

TL/F/5955-2

Order Number CD4023MJ, CD4023CJ, CD4025MJ or CD4025CJ
See NS Package J14A

Order Number CD4023MN, CD4023CN, CD4025MN or CD4025CN
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	V_{SS} − to V_{DD} + 0.3 V	Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C	Package Dissipation	500 mW
CD4023M, CD4025M	−55°C to +125°C	Operating V_{DD} Range	V_{SS} + 3.0 V to V_{SS} + 15 V
CD4023C, CD4025C	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	260°C

DC Electrical Characteristics — CD4023M, CD4025M

Sym	Parameter	Conditions	Limits							Units
			−55°C		25°C			125°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	V_{DD} = 5.0 V V_{DD} = 10 V		0.05 0.1		0.001 0.001	0.05 0.1		3.0 6.0	μA μA
P_D	Quiescent Device Dissipation/Package	V_{DD} = 5.0 V V_{DD} = 10 V		0.25 1.0		0.005 0.01	0.25 1.0		15 60	μW μW
V_{OL}	Output Voltage Low Level	V_{DD} = 5.0 V, V_I = V_{DD}, I_O = 0 A V_{DD} = 10 V, V_I = V_{DD}, I_O = 0 A		0.05 0.05		0 0	0.05 0.05		0.05 0.05	V V
V_{OH}	Output Voltage High Level	V_{DD} = 5.0 V, V_I = V_{SS}, I_O = 0 A V_{DD} = 10 V, V_I = V_{SS}, I_O = 0 A	4.95 9.95		4.95 9.95	5.0 10		4.95 9.95		V V
V_{NL}	Noise Immunity (All Inputs)	V_{DD} = 5.0 V, V_O = 3.6V, I_O = 0 A V_{DD} = 10 V, V_O = 7.2V, I_O = 0 A	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	V_{DD} = 5.0 V, V_0 = 0.95 V, I_O = 0 A V_{DD} = 10 V, V_O = 2.9 V, I_O = 0 A	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4025) (Note 2)	V_{DD} = 5.0 V, V_O = 0.4 V, V_I = V_{DD} V_{DD} = 10 V, V_O = 0.5 V, V_I = V_{DD}	0.5 1.1		0.40 0.9	1.0 2.5		0.28 0.65		mA mA
I_DP	Output Drive Current P-Channel (4025) (Note 2)	V_{DD} = 5.0 V, V_O = 2.5V, V_I = V_{SS} V_{DD} = 10 V, V_O = 9.5 V, V_I = V_{SS}	−0.62 −0.62		−0.5 −0.5	−2.0 −1.0		−0.35 −0.35		mA mA
I_DN	Output Drive Current N-Channel (4023) (Note 2)	V_{DD} = 5.0 V, V_O = 0.4 V, V_I = V_{DD} V_{DD} = 10 V, V_O = 0.5 V, V_I = V_{DD}	0.31 0.63		0.25 0.5	0.5 0.6		0.175 0.35		mA mA
I_DP	Output Drive Current P-Channel (4023) (Note 2)	V_{DD} = 5.0 V, V_O = 2.5 V, V_I = V_{SS} V_{DD} = 10 V, V_O = 9.5 V, V_I = V_{SS}	−0.31 −0.75		−0.25 −0.6	−0.5 −1.2		−0.175 −0.4		mA mA
I_I	Input Current					10				pA

DC Electrical Characteristics — CD4023C, CD4025C

Sym	Parameter	Conditions	Limits							Units
			−40°C		25°C			85°C		
			Min	Max	Min	Typ	Max	Min	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0\,V$ $V_{DD} = 10\,V$		0.5 5.0		0.005 0.005	0.5 5.0		15 30	μA μA
P_D	Quiescent Device Dissipation/Package	$V_{DD} = 5.0\,V$ $V_{DD} = 10\,V$		2.5 50		0.025 0.05	2.5 50		75 300	μW μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0\,V$, $V_I = V_{DD}$, $_O = 0\,A$ $V_{DD} = 10\,V$, $V_I = V_{DD}$, $I_O = 0\,A$		0.01 0.01		0 0	0.01 0.01		0.05 0.05	V V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0\,V$, $V_I = V_{SS}$, $I_O = 0\,A$ $V_{DD} = 10\,V$, $V_I = V_{SS}$, $I_O = 0\,A$	4.99 9.99		4.99 9.99	5.0 10		4.95 9.95		V V
I_I	Input Current					10				pA
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0\,V$, $V_O = 3.6\,V$, $I_O = 0\,A$ $V_{DD} = 10\,V$, $V_O = 7.2\,V$, $I_O = 0\,A$	1.5 3.0		1.5 3.0	2.25 4.5		1.4 2.9		V V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0\,V$, $V_O = 0.95\,V$, $I_O = 0\,A$ $V_{DD} = 10\,V$, $V_O = 2.9\,V$, $I_O = 0\,A$	1.4 2.9		1.5 3.0	2.25 4.5		1.5 3.0		V V
I_DN	Output Drive Current N-Channel (4025) (Note 2)	$V_{DD} = 5.0\,V$, $V_O = 0.4\,V$, $V_I = V_{DD}$ $V_{DD} = 10\,V$, $V_O = 0.5\,V$, $V_I = V_{DD}$	0.35 0.72		0.3 0.6	1.0 2.5		0.24 0.48		mA mA
I_DP	Output Drive Current P-Channel (4025) (Note 2)	$V_{DD} = 5.0\,V$, $V_O = 2.5\,V$, $V_I = V_{SS}$ $V_{DD} = 10\,V$, $V_O = 9.5\,V$, $V_I = V_{SS}$	−0.35 −0.3		−0.3 −0.25	−2.0 −1.0		−0.24 −0.2		mA mA
I_DN	Output Drive Current N-Channel (4023) (Note 2)	$V_{DD} = 5.0\,V$, $V_O = 0.4\,V$, $V_I = V_{DD}$ $V_{DD} = 10\,V$, $V_O = 0.5\,V$, $V_I = V_{DD}$	0.145 0.3		0.12 0.25	0.5 0.6		0.095 0.2		mA mA
I_DP	Output Drive Current P-Channel (4023) (Note 2)	$V_{DD} = 5.0\,V$, $V_O = 2.5\,V$, $V_I = V_{SS}$ $V_{DD} = 10\,V$, $V_O = 9.5\,V$, $V_I = V_{SS}$	−0.145 −0.35		−0.12 −0.3	−0.5 −1.2		−0.095 −0.24		mA mA
I_I	Input Current					10				pA

Note 1: "Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: I_DN and I_DP are tested one output at a time.

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4025M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	50 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	40 70	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	125 70	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	175 75	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4025C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	80 55	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		35 25	120 65	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	200 115	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		65 35	300 125	ns ns
C_I	Input Capacitance	Any Input		5.0		pF

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 15\,pF$, and input rise and fall times = 20 ns.
Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$

Sym	Parameter	Conditions	Min	Typ	Max	Units
CD4023M						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	75 40	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	125 75	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	100 60	ns ns
C_I	Input Capacitance	Any Input		5.0		pF
CD4023C						
t_{PHL}	Propagation Delay Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{PLH}	Propagation Delay Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		50 25	100 50	ns ns
t_{THL}	Transition Time High to Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 50	150 100	ns ns
t_{TLH}	Transition Time Low to High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$		75 40	125 75	ns ns
C_I	Input Capacitance	Any Input		5.0		pF

National Semiconductor

CD4023BM/CD4023BC Buffered Triple 3-Input NAND Gate
CD4025BM/CD4025BC Buffered Triple 3-Input NOR Gate

General Description

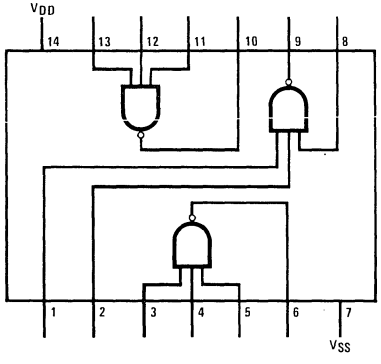
These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5 V–10 V–15 V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15 V over full temperature range

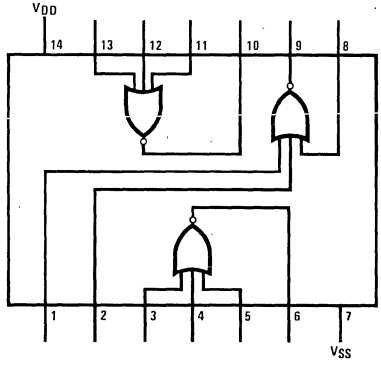
Connection Diagrams Dual-In-Line Packages

CD4023BM/CD4023BC



TOP VIEW

CD4025BM/CD4025BC



TOP VIEW

Order Number CD4023BMJ, CD4023BCJ, CD4025BMJ or CD4025BCJ
See NS Package J14A

Order Number CD4023BMN, CD4023BCN, CD4025BMN or CD4025BCN
See NS Package N14A

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
V_{IN}	Input Voltage	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
T_S	Storage Temperature Range	$-65°C$ to $+150°C$
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	260°C

Recommended Operating Conditions

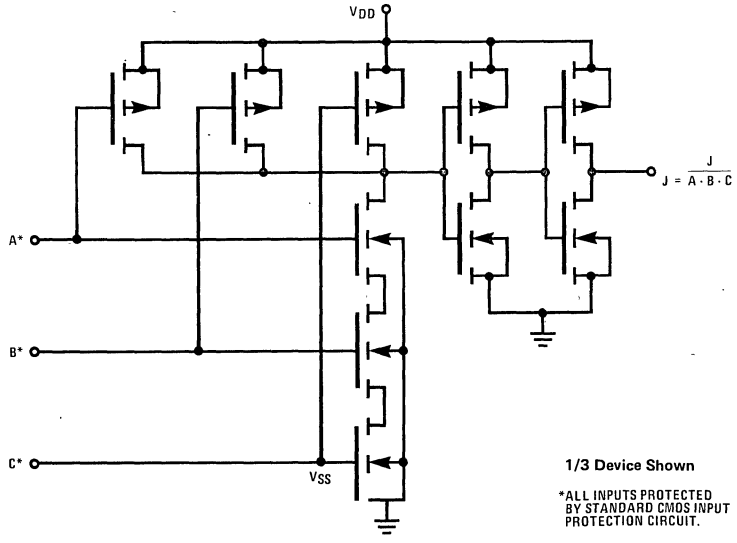
V_{DD}	DC Supply Voltage	$+5\ V_{DC}$ to $+15\ V_{DC}$
V_{IN}	Input Voltage	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
T_A	Operating Temperature Range	
	CD4023BM, CD4025BM	$-55°C$ to $+125°C$
	CD4023BC, CD4025BC	$-40°C$ to $+85°C$

DC Electrical Characteristics - CD4023BM, CD4025BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5\ V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10\ V$		0.5		0.005	0.5		15	μA
		$V_{DD} = 15\ V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5\ V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10\ V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15\ V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5\ V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10\ V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15\ V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5\ V,\ V_O = 4.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		1.5		2	1.5		1.5	V
		$V_{DD} = 10\ V,\ V_O = 9.0\ V$ | $\lvert I_O \rvert < 1\ \mu A$		3.0		4	3.0		3.0	V
		$V_{DD} = 15\ V,\ V_O = 13.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5\ V,\ V_O = 0.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	3.5		3.5	3		3.5		V
		$V_{DD} = 10\ V,\ V_O = 1.0\ V$ | $\lvert I_O \rvert < 1\ \mu A$	7.0		7.0	6		7.0		V
		$V_{DD} = 15\ V,\ V_O = 1.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5\ V,\ V_O = 0.4\ V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10\ V,\ V_O = 0.5\ V$	1.6		1.3	2.2		0.90		mA
		$V_{DD} = 15\ V,\ V_O = 1.5\ V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5\ V,\ V_O = 4.6\ V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10\ V,\ V_O = 9.5\ V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD} = 15\ V,\ V_O = 13.5\ V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15\ V,\ V_{IN} = 0\ V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15\ V,\ V_{IN} = 15\ V$		0.10		10^{-5}	0.10		1.0	μA

Schematic Diagram

CD4023BC/CD4023BM



1/3 Device Shown

*ALL INPUTS PROTECTED BY STANDARD CMOS INPUT PROTECTION CIRCUIT.

5

DC Electrical Characteristics CD4023BC, CD4025BC (Note 2)

SYM	PARAMETER	CONDITIONS	-40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		1.0		0.004	1.0		7.5	μA
		V_{DD} = 10 V		2.0		0.005	2.0		15	μA
		V_{DD} = 15 V		4.0		0.006	4.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95	5		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 4.5 V, $\lvert I_O \rvert < 1\,\mu A$		1.5		2	1.5		1.5	V
		V_{DD} = 10 V, V_O = 9.0 V, $\lvert I_O \rvert < 1\,\mu A$		3.0		4	3.0		3.0	V
		V_{DD} = 15 V, V_O = 13.5 V, $\lvert I_O \rvert < 1\,\mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V, $\lvert I_O \rvert < 1\,\mu A$	3.5		3.5	3		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V, $\lvert I_O \rvert < 1\,\mu A$	7.0		7.0	6		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V, $\lvert I_O \rvert < 1\,\mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 4.6 V	-0.52		-0.44	-0.88		-0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	-1.3		-1.1	-2.2		-0.90		mA
		V_{DD} = 15 V, V_O = 13.5 V	-3.6		-3.0	-8		-2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		-0.3		-10^{-5}	-0.3		-1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA

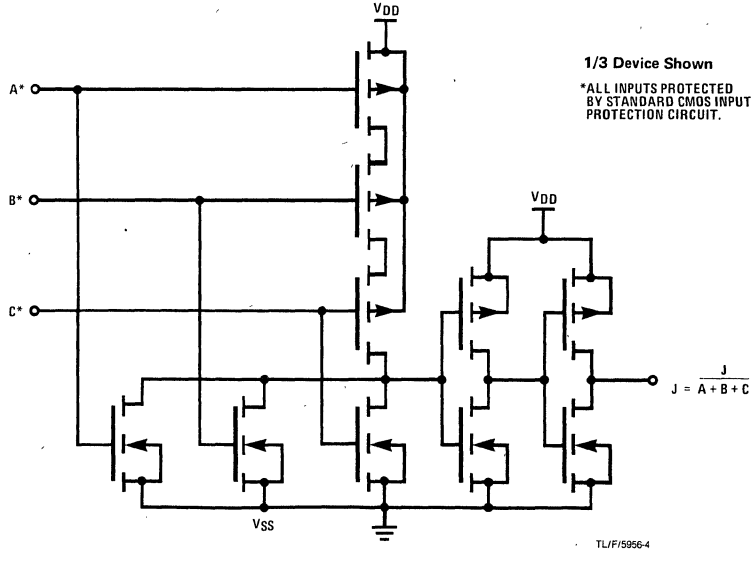
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Schematic Diagram

CD4025BM/CD4025BC



AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, unless otherwise specified.

SYM	PARAMETER	CONDITIONS	CD4023BC CD4023BM			CD4025BC CD4025BM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay, High to Low Level	$V_{DD} = 5\,V$		130	250		130	250	ns
		$V_{DD} = 10\,V$		60	100		60	100	ns
		$V_{DD} = 15\,V$		40	70		40	70	ns
t_{PLH}	Propagation Delay, Low to High Level	$V_{DD} = 5\,V$		110	250		120	250	ns
		$V_{DD} = 10\,V$		50	100		60	100	ns
		$V_{DD} = 15\,V$		35	70		40	70	ns
t_{THL} t_{TLH}	Transition Time	$V_{DD} = 5\,V$		90	200		90	200	ns
		$V_{DD} = 10\,V$		50	100		50	100	ns
		$V_{DD} = 15\,V$		40	80		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (See Note 4)	Any Gate		17			17		pF

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family characteristics Application Note AN-90.

National Semiconductor

CD4024BM/CD4024BC 7-Stage Ripple Carry Binary Counter

General Description

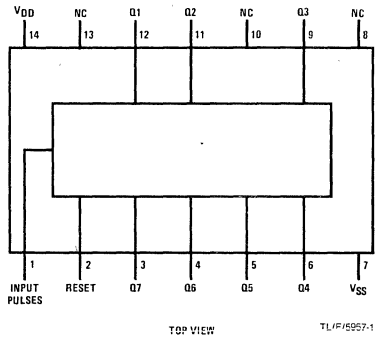
The CD4024BM/CD4024BC is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The couter is reset to its logical "0" stage by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- High speed — 12 MHz (typ.) input pulse rate $V_{DD} - V_{SS} = 10$ V
- Fully static operation

Connection Diagram

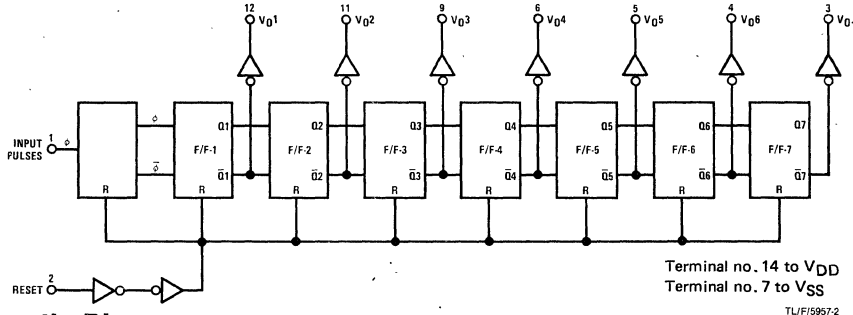
Dual-In-Line Package



Order Number CD4024BMJ or CD4024BCJ
See NS Package J14A

Order Number CD4024BMN or CD4024BCN
See NS Package N14A

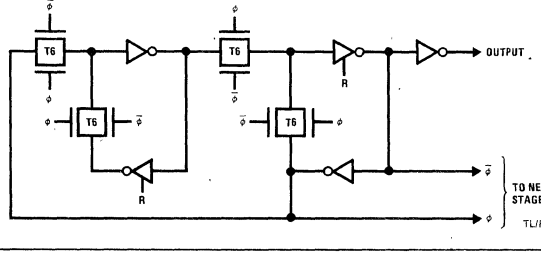
Logic Diagram

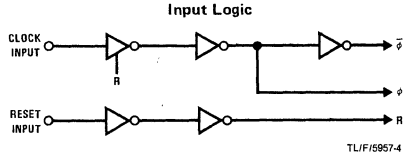


Terminal no. 14 to V_{DD}
Terminal no. 7 to V_{SS}

TL/F/5957-2

Schematic Diagram





Flip-flop logic (1 of 7 identical stages).

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4024BM	−55°C to +125°C
CD4024BC	−40°C to +85°C

DC Electrical Characteristics CD4024BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		0.7	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD4024BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.3	20		150	μA
		V_{DD} = 10V		40		0.5	40		300	μA
		V_{DD} = 15V		60		0.7	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4024BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, t_r and $t_f = 20\,ns$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time to Q1 Output	V_{DD} = 5V		185	350	ns
		V_{DD} = 10V		85	125	ns
		V_{DD} = 15V		70	100	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width	V_{DD} = 5V		75	200	ns
		V_{DD} = 10V		40	110	ns
		V_{DD} = 15V		35	90	ns
t_{RCL}, t_{FCL}	Input Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			8	μs
f_{CL}	Maximum Input Pulse Frequency	V_{DD} = 5V	1.5	5		MHz
		V_{DD} = 10V	4	12		MHz
		V_{DD} = 15V	5	15		MHz
t_{PHL}	Reset Propagation Delay Time	V_{DD} = 5V		185	350	ns
		V_{DD} = 10V		85	125	ns
		V_{DD} = 15V		70	100	ns
t_{WH}	Reset Minimum Pulse Width	V_{DD} = 5V		185	350	ns
		V_{DD} = 10V		85	125	ns
		V_{DD} = 15V		70	100	ns
C_{IN}	Input Capacitance (Note 4)	Any Input		5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Capacitance is guaranteed by periodic testing.

National Semiconductor

CD4027BM/CD4027BC Dual J-K Master/Slave Flip-Flop with Set and Reset

General Description

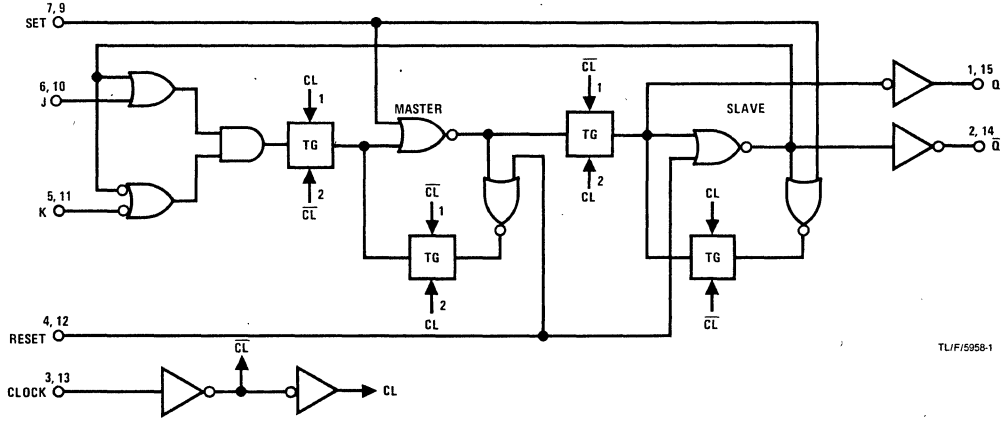
These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset, and clock inputs and buffered Q and "$\overline{Q}$" outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

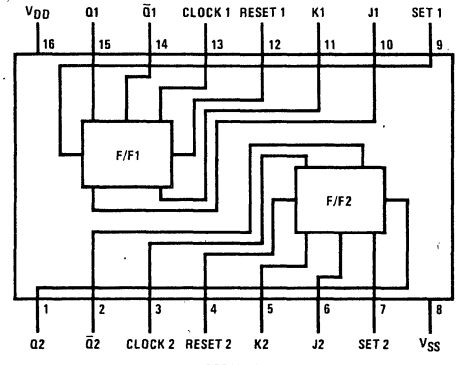
■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Low power	50 nW (typ.)
■ Medium speed operation	12 MHz (typ.) with 10 V supply

Schematic and Connection Diagrams



TL/F/5958-1

Dual-In-Line Package



TOP VIEW

TL/F/5958-2

Order Number CD4027BMJ or CD4027BCJ
See NS Package J16A

Order Number CD4027BMN or CD4027BCN
See NS Package N16E

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4027BM	−55°C to +125°C
CD4027BC	−40°C to +85°C

DC Electrical Characteristics CD4027BM (Note 2)

SYMBOL	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1			1		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2			2		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4			4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics (Cont'd.) CD4027BC (Note 2)

SYMBOL	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4			4		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8			8		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16			16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics CD4027BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $t_{rCL} = t_{fCL} = 20\,ns$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Q or $\overline{Q}$	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From Set to $\overline{Q}$ or Reset to Q	V_{DD} = 5V		170	340	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From Set to Q or Reset to $\overline{Q}$	V_{DD} = 5V		110	220	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_S	Minimum Data Set-Up Time	V_{DD} = 5V		135	270	ns
		V_{DD} = 10V		55	110	ns
		V_{DD} = 15V		45	90	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Frequency (Toggle Mode)	V_{DD} = 5V	2.5	5		MHz
		V_{DD} = 10V	6.2	12.5		MHz
		V_{DD} = 15V	7.6	15.5		MHz
t_{rCL} or t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	10			μs
		V_{DD} = 15V	5			μs
t_W	Minimum Clock Pulse Width ($t_{WH} = t_{WL}$)	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
t_{WH}	Minimum Set and Reset Pulse Width	V_{DD} = 5V		80	160	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Per Flip-Flop (Note 4)		35		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

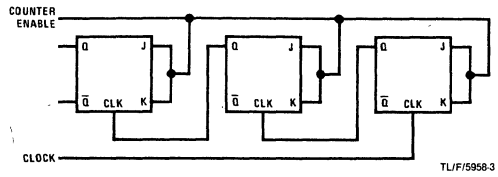
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

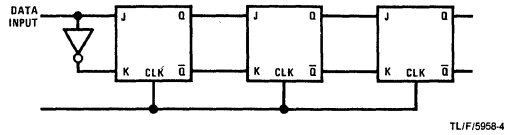
Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Typical Applications

Ripple Binary Counters



Shift Registers



Truth Table

•t_{n-1} INPUTS						♦t_n OUTPUTS		
CL▲	J	K	S	R	Q	Q	$\bar{Q}$	
⌐⌐	I	X	O	O	O	I	O	
⌐⌐	X	O	O	O	I	I	O	
⌐⌐	O	X	O	O	O	O	I	
⌐⌐	X	I	O	O	I	O	I	
⌐⌐	X	X	O	O	X			(No change)
X	X	X	I	O	X	I	O	
X	X	X	O	I	X	O	I	
X	X	X	I	I	X	I	I	

Where: I = High Level
O = Low Level
▲ = Level Change
X = Don't Care
• = t_{n-1} refers to the time interval prior to the positive clock pulse transition
♦ = t_n refers to the time intervals after the positive clock pulse transition

National Semiconductor

CD4028BM/CD4028BC BCD-to-Decimal Decoder

General Description

The CD4028BM/CD4028BC is a BCD-to-decimal or binary-to-octal decoder consisting of 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the 4 inputs, A, B, C, and D, results in a high level at the selected 1-of-10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A, B, and C is decoded in octal at outputs 0–7. A high level signal at the D input inhibits octal decoding and causes outputs 0–7 to go low.

All inputs are protected against static discharge damage by diode clamps to V_{DD} and V_{SS}.

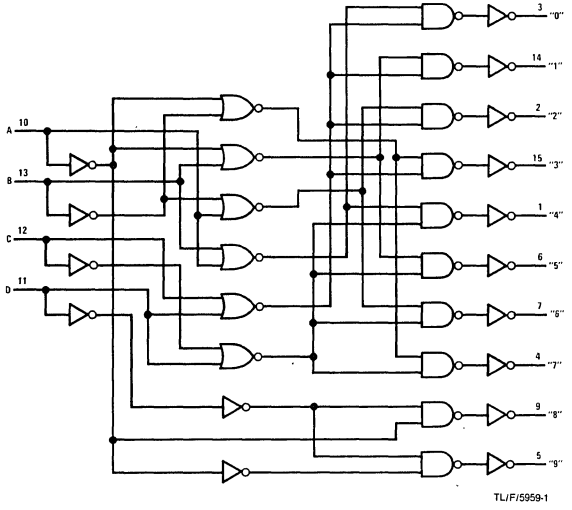
Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Low power
- Glitch free outputs
- "Positive logic" on inputs and outputs

Applications

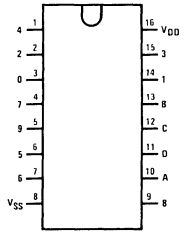
- Code conversion
- Address decoding
- Indicator-tube decoder

Logic and Connection Diagrams



TL/F/5959-1

Dual-In-Line Package



TOP VIEW

TL/F/5959-2

Order Number CD4028BMJ or CD4028BCJ
See NS Package J16A

Order Number CD4028BMN or CD4028BCN
See NS Package N16E

Truth Table

D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	BCD States
0	0	0	1	0	1	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	
0	0	1	1	0	0	0	1	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	1	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	1	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	1	
1	0	1	0	0	0	0	0	0	0	0	0	1	0	Extraordinary States
1	0	1	1	0	0	0	0	0	0	0	0	0	1	
1	1	0	0	0	0	0	0	0	0	0	0	1	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	
1	1	1	1	0	0	0	0	0	0	0	0	0	1	

1 = High level
0 = Low level

Absolute Maximum Ratings (Note 1)

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4028BM	−55°C to +125°C
CD4028BC	−40°C to +85°C

DC Electrical Characteristics CD4028BC (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.01	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.01	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{IL} = 0V, V_{IH} = V_{DD}								
	(Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	1.0		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.6		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	6.8		2.4		mA
I_{OH}	High Level Output Current	V_{IL} = 0V, V_{IH} = V_{DD}								
	(Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.4		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−1.0		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.0		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4028BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.01	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.01	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD4028BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	6.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.32		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.8		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−2.4		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3			−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3			0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

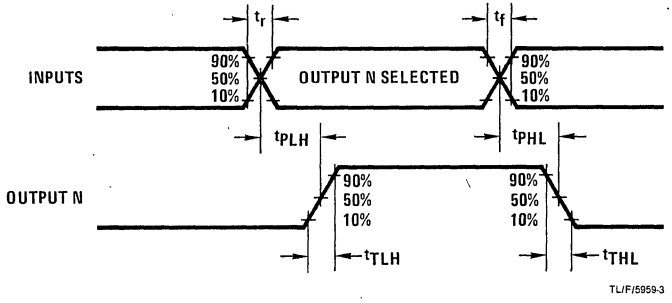
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay	V_{CC} = 5V		240	480	ns
		V_{CC} = 10V		100	200	ns
		V_{CC} = 15V		70	140	ns
t_{THL} or t_{TLH}	Transition Time	V_{CC} = 5V		175	350	ns
		V_{CC} = 10V		75	150	ns
		V_{CC} = 15V		60	110	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

Switching Time Waveforms



TL/F/5959-3

National Semiconductor

CD4029BM/CD4029BC Presettable Binary/Decade Up/Down Counter

General Description

The CD4029BM/CD4029BC is a presettable up/down counter which counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical "1," the counter counts in binary, otherwise it counts in decade. Similarly, the counter counts up when the up/down input is at logical "1" and vice versa.

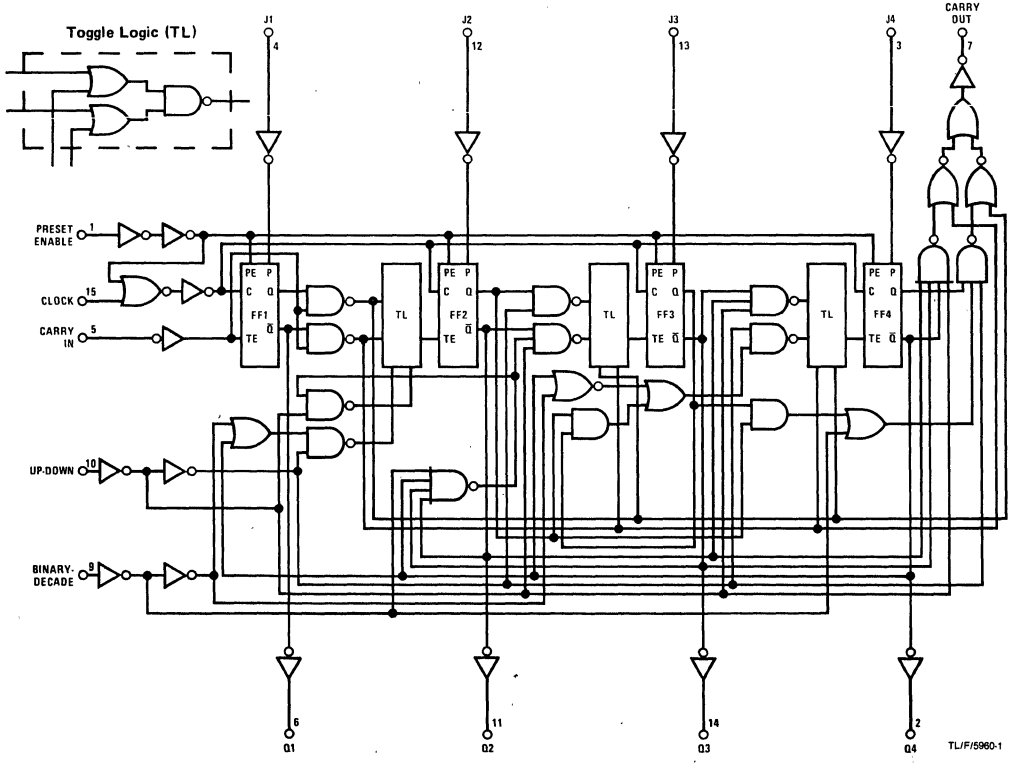
A logical "1" preset enable signal allows information at the "jam" inputs to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the positive-going edge of the clock if the carry in and preset enable inputs are at logical "0." Advancement is inhibited when either or both of these two inputs is at logical "1." The carry out signal is normally at logical "1" state and goes to logical "0" state when the counter reaches its maximum count in the "up" mode or the minimum count in the "down" mode provided the carry input is at logical "0" state.

All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Parallel jam inputs
- Binary or BCD decade up/down counting

Logic Diagram



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4029BM	−55°C to +125°C
CD4029BC	−40°C to +85°C

DC Electrical Characteristics CD4029BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5	5	150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	(Note 3)	V_{DD} = 10V V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4029BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

5

DC Electrical Characteristics (Cont'd.) CD4029BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5 or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200 k, Input $t_{rCL} = t_{fCL}$ = 20 ns, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Q Outputs	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		70	140	ns
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	V_{DD} = 5V		320	640	ns
		V_{DD} = 10V		135	270	ns
		V_{DD} = 15V		110	220	ns
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	V_{DD} = 5V, C_L = 15 pF		285	570	ns
		V_{DD} = 10V, C_L = 15 pF		120	240	ns
		V_{DD} = 15V, C_L = 15 pF		95	190	ns
t_{THL} or t_{TLH}	Transition Time/Q or Carry Output	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WH} or t_{WL}	Minimum Clock Pulse Width	V_{DD} = 5V		160	320	ns
		V_{DD} = 10V		70	135	ns
		V_{DD} = 15V		55	110	ns
t_{rCL} or t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	10			μs
		V_{DD} = 15V	5			μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		180	360	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	3.1		MHz
		V_{DD} = 10V	3.7	7.4		MHz
		V_{DD} = 15V	4.5	9		MHz
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 4)		65		pF
PRESET ENABLE OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Q Output	V_{DD} = 5V		285	570	ns
		V_{DD} = 10V		115	230	ns
		V_{DD} = 15V		95	195	ns

AC Electrical Characteristics (Cont'd.) $T_A = 25°C$, $C_L = 50$ pF, $t_{rCL} = t_{fCL} = 20$ ns, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
PRESET ENABLE OPERATION (con't)						
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	$V_{DD} = 5V$		400	800	ns
		$V_{DD} = 10V$		165	330	ns
		$V_{DD} = 15V$		135	260	ns
t_{WH}	Minimum Preset Enable Pulse Width	$V_{DD} = 5V$		80	160	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
t_{REM}	Minimum Preset Enable Removal Time	$V_{DD} = 5V$		150	300	ns
		$V_{DD} = 10V$		60	120	ns
		$V_{DD} = 15V$		50	100	ns
CARRY INPUT OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	$V_{DD} = 5V$		265	530	ns
		$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		90	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time to Carry Output	$V_{DD} = 5V$, $C_L = 15$ pF		200	400	ns
		$V_{DD} = 10V$, $C_L = 15$ pF		85	170	ns
		$V_{DD} = 15V$, $C_L = 15$ pF		70	140	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

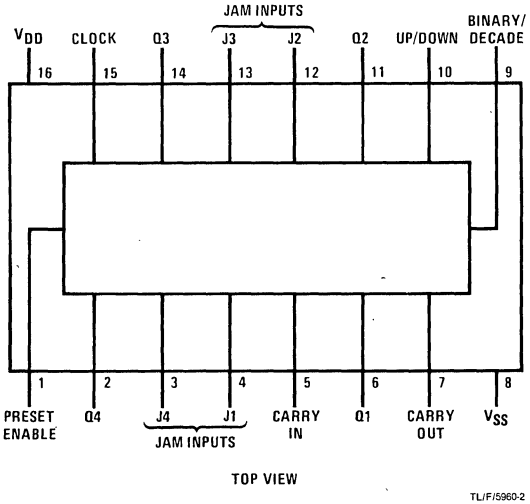
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Connection Diagram

Dual-In-Line Package



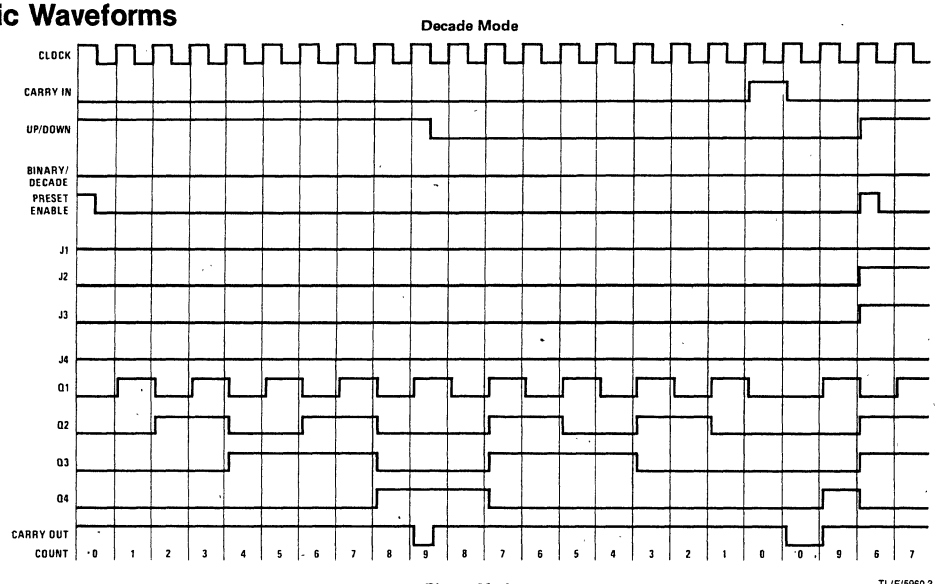
TOP VIEW

TL/F/5960-2

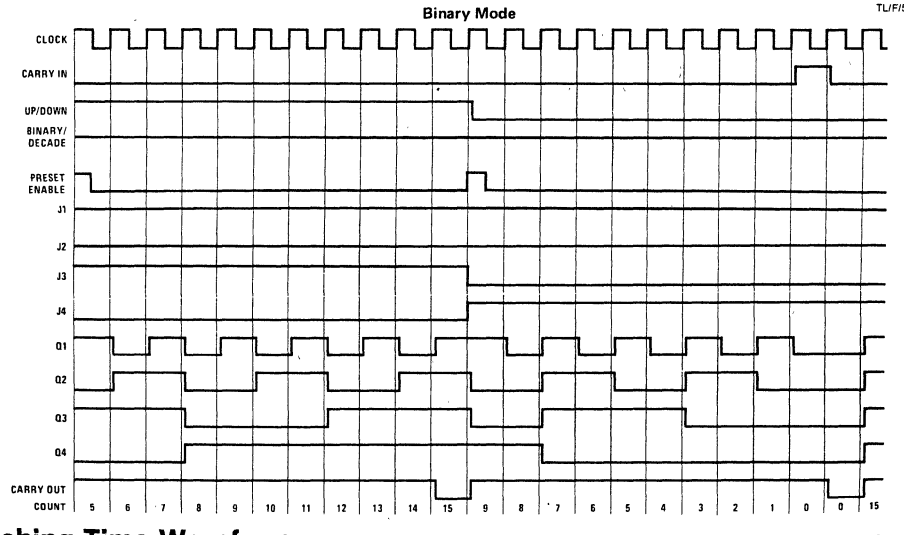
Order Number CD4029BMJ or CD4029BCJ
See NS Package J16A

Order Number CD4029BMN or CD4029BCN
See NS Package N16E

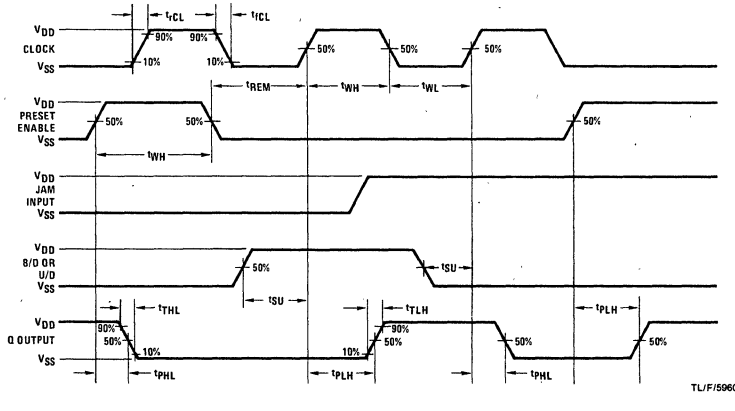
Logic Waveforms



TL/F/5960-3



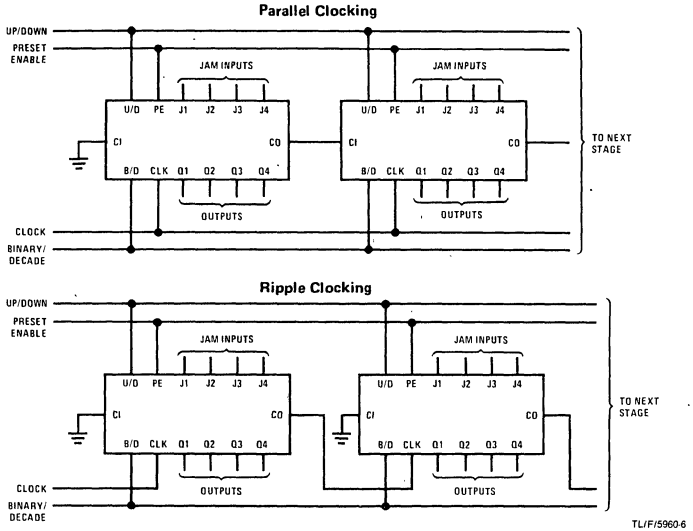
Switching Time Waveforms



TL/F/5960-4

TL/F/5960-5

Cascading Packages



Carry out lines at the 2nd or later stages may have a negative-going spike due to differential internal delays. These spikes do not affect counter operation, but if the carry out is used to trigger external circuitry the carry out should be gated with the clock.

5

National Semiconductor

CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

General Description

The EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

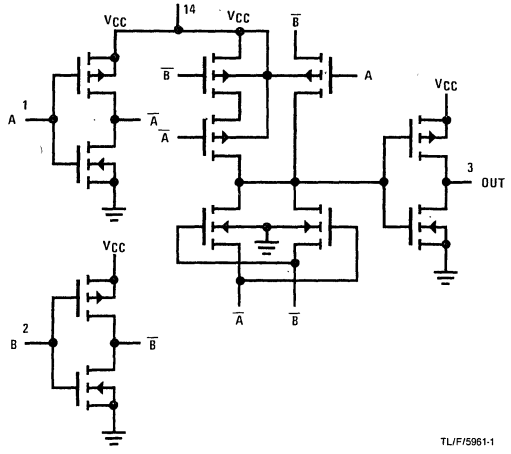
Features

■ Wide supply voltage range	3.0 V to 15 V
■ Low power	100 nW (typ.)
■ Medium speed operation	$t_{PHL} = t_{PLH} = 40$ ns (typ.) at $C_L = 15$ pF, 10 V supply
■ High noise immunity	0.45 V_{CC} (typ.)

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

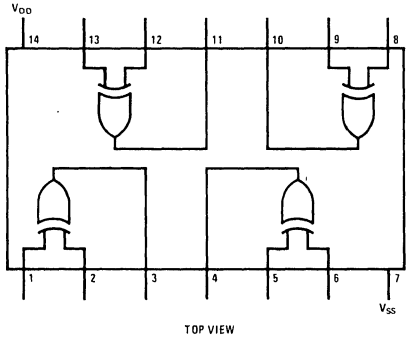
Schematic Diagram



TL/F/5961-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5961-2

Order Number CD4030MJ or CD4030CJ
See NS Package J14A

Order Number CD4030MN or CD4030CN
See NS Package N14A

Absolute Maximum Ratings

Voltage at Any Pin (Note 1) V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range
CD4030M −55°C to +125°C
CD4030C −40°C to +85°C

Storage Temperature Range −65°C to +150°C
Package Dissipation 500 mW
Operating V_{DD} Range V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds) 260°C

DC Electrical Characteristics CD4030M

PARAMETER	CONDITIONS	LIMITS									UNITS
		-55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V V_{DD} = 10V			0.5 1.0		0.005 0.01	0.5 1.0			30 60	μA μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V V_{DD} = 10V			2.5 10		0.025 0.1	2.5 10			150 600	μW μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V V_{DD} = 10V			0.05 0.05		0 0	0.05 0.05			0.05 0.05	V V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V V_{DD} = 10V	4.95 9.95			4.95 9.95	5.0 10		4.95 9.95			V V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5.0V V_{DD} = 10V	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V V_{DD} = 10V	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V
Output Drive Current N-Channel (I_DN) (Note 2)	V_{DD} = 5.0V V_{DD} = 10V	0.75 1.5			0.6 1.2	1.2 2.4		0.45 0.9			mA mA
Output Drive Current P-Channel (I_DP) (Note 2)	V_{DD} = 5.0V V_{DD} = 10V	−0.45 −0.95			−0.3 −0.65	−0.6 −1.3		−0.21 −0.45			mA mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

DC Electrical Characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS									UNITS
		-40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V V_{DD} = 10V			5.0 10		0.05 0.1	5.0 10			70 140	μA μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V V_{DD} = 10V			25 100		0.25 1.0	25 100			350 1,400	μW μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V V_{DD} = 10V			0.05 0.05		0 0	0.05 0.05			0.05 0.05	V V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V V_{DD} = 10V	4.95 9.95			4.95 9.95	5.0 10		4.95 9.95			V V
Noise Immunity (All Inputs)(V_{NL})	V_{DD} = 5.0V V_{DD} = 10V	1.5 3.0			1.5 3.0	2.25 4.5		1.4 2.9			V V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V V_{DD} = 10V	1.4 2.9			1.5 3.0	2.25 4.5		1.5 3.0			V V
Output Drive Current N-Channel (I_DN) (Note 2)	V_{DD} = 5.0 V_{DD} = 10V	0.35 0.7			0.3 0.6	1.2 2.4		0.25 0.5			mA mA
Output Drive Current P-Channel (I_DP) (Note 2)	V_{DD} = 5.0V V_{DD} = 10V	−0.21 −0.45			−0.15 −0.32	−0.6 −1.3		−0.12 −0.25			mA mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

AC Electrical Characteristics CD4030M

SYM	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
(t_{PHL})	Propagation Delay Time	V_{DD} = 5.0V V_{DD} = 10V		100 40	200 100	ns ns
(t_{PLH})	Propagation Delay Time	V_{DD} = 5.0V V_{DD} = 10V		100 40	200 100	ns ns
(t_{THL})	Transition Time High to Low Level	V_{DD} = 5.0V V_{DD} = 10V		70 25	150 75	ns ns
(t_{TLH})	Transition Time Low to High Level	V_{DD} = 5.0V V_{DD} = 10V		80 30	150 75	ns ns
(C_I)	Input Capacitance	V_I = 0V or V_I = V_{DD}		5.0		pF

AC Electrical Characteristics CD4030C

SYM	PARAMETER	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
(t_{PHL})	Propagation Delay Time	V_{DD} = 5.0V V_{DD} = 10V		100 40	300 150	ns ns
(t_{PLH})	Propagation Delay Time	V_{DD} = 5.0V V_{DD} = 10V		100 40	300 150	ns ns
(t_{THL})	Transition Time High to Low Level	V_{DD} = 5.0V V_{DD} = 10V		70 25	300 150	ns ns
(t_{TLH})	Transition Time Low to High Level	V_{DD} = 5.0V V_{DD} = 10V		80 30	300 150	ns ns
(C_I)	Input Capacitance	V_I = 0V or V_I = V_{DD}		5.0		pF

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

Note 2: I_DN and I_DP are tested one output at a time.

Truth Table (For One of Four Identical Gates)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level
"0" = Low Level

National Semiconductor

CD4031BM/CD4031BC 64-Stage Static Shift Register

General Description

The CD4031BM/CD4031BC is an integrated, complementary MOS (CMOS), 64-stage, fully static shift register. Two data inputs, DATA IN and RECIRCULATE IN, and a MODE CONTROL input are provided. Data at the DATA input (when MODE CONTROL is low) or data at the RECIRCULATE input (when MODE CONTROL is high), which meets the setup and hold time requirements, is entered into the first stage of the register and is shifted one stage at each positive transition of the CLOCK.

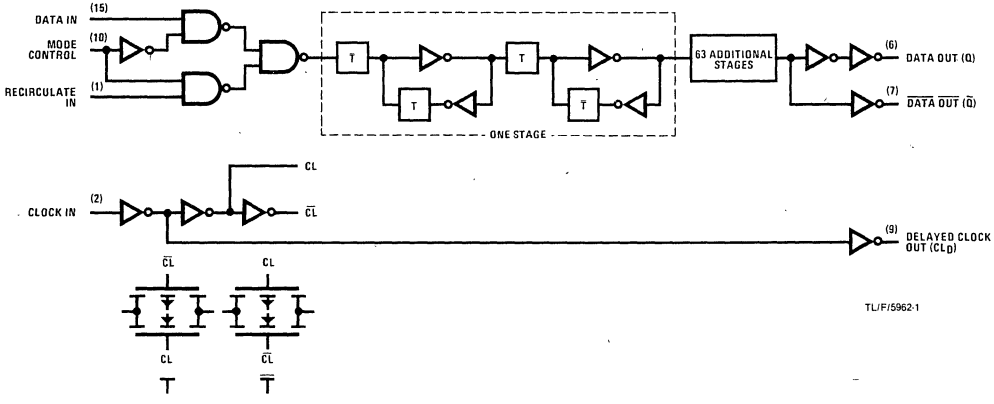
Data output is available in both true and complement forms from the 64th stage. Both the DATA OUT (Q) and $\overline{\text{DATA OUT}}$ ($\overline{Q}$) outputs are fully buffered.

The CLOCK input of the CD4031BM/CD4031BC is fully buffered, and present only a standard input load capacitance. However, a DELAYED CLOCK OUTPUT (CL_D) has been provided to allow reduced clock drive fan-out and transition time requirements when cascading packages.

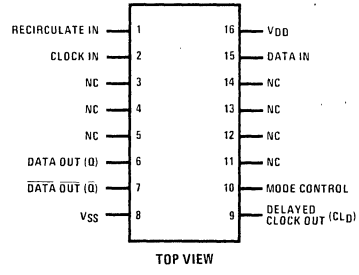
Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Fully static operation	DC to 8 MHz V_{DD} = 10 V (typ.)
■ Fully buffered clock input	5 pF (typ.) input capacitance
■ Single phase clocking requirements	
■ Delayed clock output for reduced clock drive requirements	
■ Fully buffered outputs	
■ High current sinking capability Q output	1.6 mA @ V_{DD} = 5 V and 25°C

Logic and Connection Diagrams



Dual-In-Line Package



Order Number CD4031BMJ or CD4031BCJ
See NS Package J16A

Order Number CD4031BMN or CD4031BCN
See NS Package N16E

5

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5 V to +18 V
V_{IN}	Input Voltage	−0.5 V to V_{DD} + 0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD}	Supply Voltage	+3 V to +15 V
V_{IN}	Input Voltage	0 V to V_{DD}
T_A	Operating Temperature Range	
	CD4031BM	−55°C to +125°C
	CD4031BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) CD4031BM

SYM	PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.01	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.01	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, V_{IN} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95	5		4.95		V
		V_{DD} = 10 V, V_{IN} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\,\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\|I_O\| < 1\,\mu A$		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\|I_O\| < 1\,\mu A$	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output (Note 3)	V_{DD} = 5 V, V_O = 0.4 V, V_{IH} = V_{DD}, V_{IL} = 0 V	2.3		1.9	3.8		1.3		mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	5.1		4.2	8.4		2.8		mA
		V_{DD} = 15 V, V_O = 1.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	10.5		8.8	17		6.1		mA
I_{OL}	Low Level Output Current, $\overline{Q}$ and CL_D Outputs (Note 3)	V_{DD} = 5 V, V_O = 0.4 V, V_{IH} = V_{DD}, V_{IL} = 0 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs (Note 3)	V_{DD} = 5 V, V_O = 4.6 V, V_{IH} = V_{DD}, V_{IL} = 0 V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA

Truth Tables

MODE CONTROL (data selection)

MODE CONTROL	DATA IN	RECIRCULATE IN	DATA INTO FIRST STAGE
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

EACH STAGE

D_n	CL	Q_n
0	⌐	0
1	⌐	1
X	¬	NC

X = irrelevant
NC = no change
⌐ = Low to High level transition
¬ = High to Low level transition

DC Electrical Characteristics (Note 2) CD4031BC

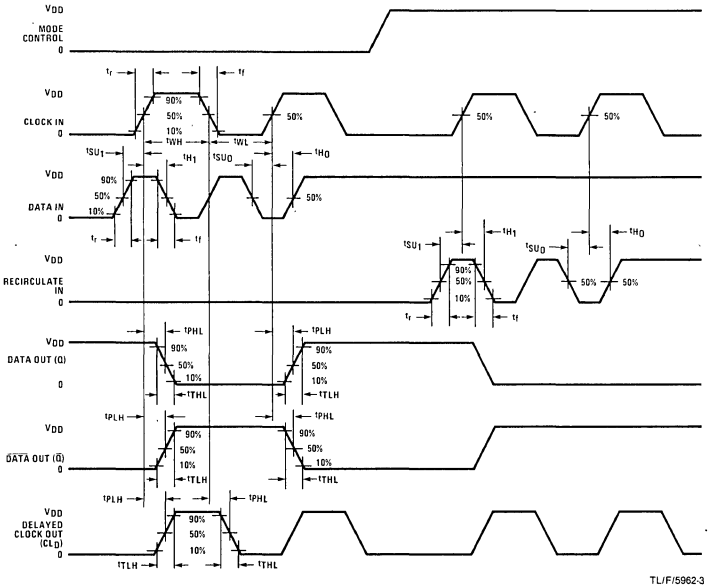
SYM	PARAMETER	CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.01	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.01	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, V_{IH} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95	5		4.95		V
		V_{DD} = 10 V, V_{IH} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\,\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V, $\|I_O\| < 1\,\mu A$		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\|I_O\| < 1\,\mu A$		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V, $\|I_O\| < 1\,\mu A$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V, $\|I_O\| < 1\,\mu A$	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\|I_O\| < 1\,\mu A$	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V, $\|I_O\| < 1\,\mu A$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output (Note 3)	V_{DD} = 5 V, V_O = 0.4 V, V_{IH} = V_{DD}, V_{IL} = 0 V	1.8		1.6	3.8		1.3		mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	4.0		3.5	8.4		2.8		mA
		V_{DD} = 15 V, V_O = 1.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	8.7		7.5	17		6.1		mA
I_{OL}	Low Level Output Current, $\overline{Q}$ and CL_D Outputs (Note 3)	V_{DD} = 5 V, V_O = 0.4 V, V_{IH} = V_{DD}, V_{IL} = 0 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs (Note 3)	V_{DD} = 5 V, V_O = 4.6 V, V_{IH} = V_{DD}, V_{IL} = 0 V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Switching Time Waveforms



TL/F/5962-3

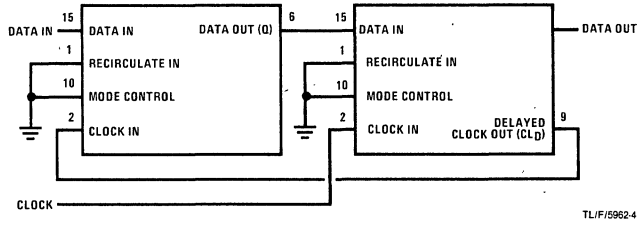
AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to Q and $\overline{Q}$	$V_{CC} = 5\,V$		300	600	ns
		$V_{CC} = 10\,V$		125	250	ns
		$V_{CC} = 15\,V$		100	200	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to CL_D	$V_{CC} = 5\,V$		125	250	ns
		$V_{CC} = 10\,V$		60	125	ns
		$V_{CC} = 15\,V$		50	100	ns
t_{THL}, t_{TLH}	Output Transition Time, All Outputs	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{SU_0} t_{SU_1}	Minimum Data Setup Time, DATA IN or RECIRCULATE IN to Clock	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{H_0} t_{H_1}	Minimum Data Hold Time, Clock to DATA IN or RECIRCULATE IN	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{CC} = 5\,V$		150	300	ns
		$V_{CC} = 10\,V$		60	125	ns
		$V_{CC} = 15\,V$		50	100	ns
f_{CL}	Maximum Clock Frequency	$V_{CC} = 5\,V$	1.6	3.2		MHz
		$V_{CC} = 10\,V$	4.0	8.0		MHz
		$V_{CC} = 15\,V$	5.0	10		MHz
t_{RCL}, t_{FCL}	Maximum Clock Input Rise and Fall Times (Note 4)	$V_{CC} = 5\,V$	15			μs
		$V_{CC} = 10\,V$	10			μs
		$V_{CC} = 15\,V$	5			μs
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Note 4: When clocking cascaded packages in parallel, one should insure that: $t_{r\,CL} \leq 2(t_{PD} - t_H)$ where: t_{PD} = the propagation delay of the driving stage and t_H = the hold time of the driven stage.

Block Diagram

cascading packages using DELAYED CLOCK (CL_D) output



National Semiconductor

CD4034BM/CD4034BC 8-Stage TRI-STATE® Bidirectional Parallel/Serial Input/Output Bus Register

General Description

The CD4034BM/CD4034BC is an 8-bit CMOS static shift register with two parallel bidirectional data ports (A and B) which, when combined with serial shifting operations, can be used to (1) bidirectionally transfer parallel data between two buses, (2) convert serial data to parallel form and direct them to either of two buses, (3) store (recirculate) parallel data, or (4) accept parallel data from either of two buses and convert them to serial form. These operations are controlled by five control inputs:

A ENABLE (AE): "A" data port is enabled only when AE is at logical "1". This allows the use of a common bus for multiple packages.

A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B): This input controls the direction of data flow. When at logical "1", data flows from port A to B (A is input, B is output). When at logical "0", the data flow direction is reversed.

ASYNCHRONOUS/SYNCHRONOUS (A/S): When A/S is at logical "0", data transfer occurs at positive transition of the CLOCK. When A/S is at logical "1", data transfer is independent of the CLOCK for parallel operation. In serial mode, A/S input is internally disabled such that operation is always synchronous. (Asynchronous serial operation is not possible.)

PARALLEL/SERIAL (P/S): A logical "1" P/S input allows data transfer into the registers via A or B port (synchronous if A/S = logical "0", asynchronous if A/S = logical "1"). A logical "0" P/S allows serial data to transfer into the register synchronously with the positive transition of the CLOCK, independent of the A/S input.

CLOCK: Single phase, enabled only in synchronous mode. (Either P/S = logical "1" and A/S = logical "0" or P/S = logical "0".

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

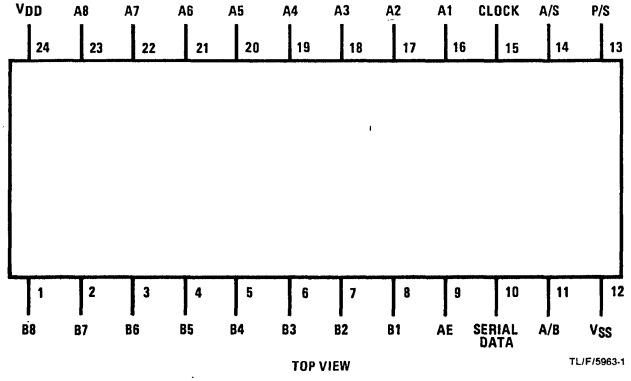
Features

- Wide supply voltage range — 3.0 to 18 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- RCA CD4034B second source

Applications

- Parallel Input/Parallel Output
  Parallel Input/Serial Output
  Serial Input/Parallel Output
  Serial Input/Serial Output register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storge, counting, display)
- Frequency and phase comparator

Connection Diagram Dual-In-Line Package



Order Number CD4034BMJ or CD4034BCJ
See NS Package J24A

Order Number CD4034BMN or CD4034BCN
See NS Package N24A

Absolute Maximum Ratings
(Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
V_{IN}	Input Voltage	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
T_S	Storage Temperature Range	$-65°C$ to $+150°C$
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions
(Note 2)

V_{DD}	DC Supply Voltage	$+3\ V_{DC}$ to $+15\ V_{DC}$
V_{IN}	Input Voltage	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
T_A	Operating Temperature Range	
	CD4034BM	$-55°C$ to $+125°C$
	CD4034BC	$-40°C$ to $+85°C$

DC Electrical Characteristics CD4034BM (Note 2)

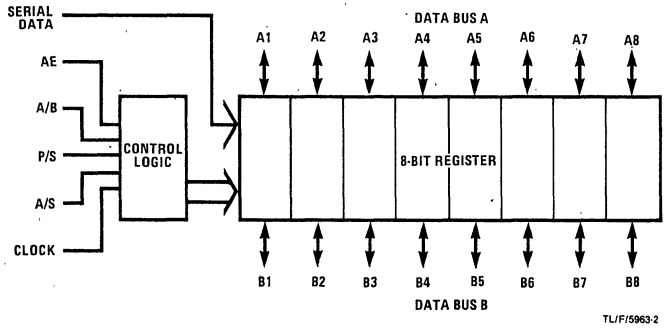
SYM	PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
		V_{DD} = 10 V		0.05			0.05		0.05	V
		V_{DD} = 15 V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
		V_{DD} = 10 V	9.95		9.95			9.95		V
		V_{DD} = 15 V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
		V_{DD} = 15 V, VO = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 0.4 V	0.64		0.51			0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3			0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4			2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 4.6 V	−0.64		−0.51			−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3			−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−0.1		−0.1	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15 V, V_O = 0 V	−0.1		−0.1	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_O = 15 V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Logic Diagram



TL/F/5963-2

DC Electrical Characteristics CD4034BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
		V_{DD} = 10 V		0.05			0.05		0.05	V
		V_{DD} = 15 V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
		V_{DD} = 10 V	9.95		9.95			9.95		V
		V_{DD} = 15 V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44			0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1			0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0			2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 4.6 V	−0.52		−0.44			−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.3		−1.1			−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V	−3.6		−3.0			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15 V, V_O = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_O = 15 V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_r = t_f = 20 ns, unless otherwise specified

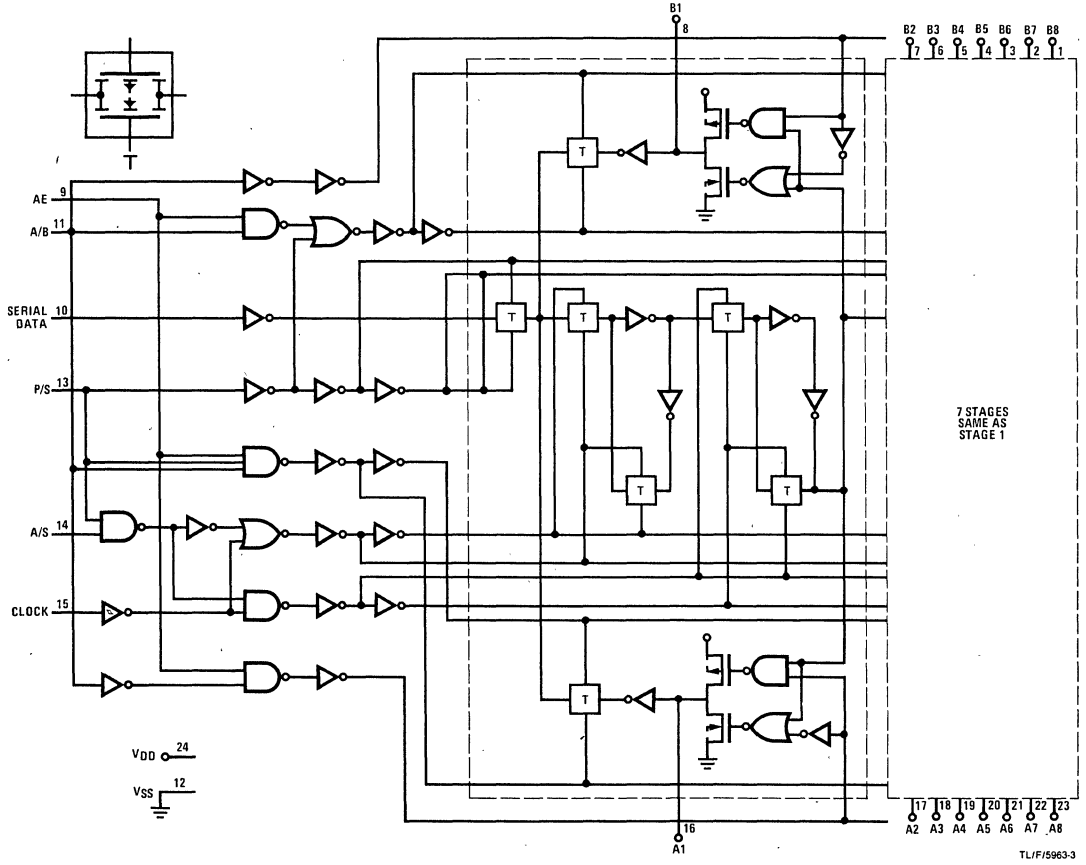
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) Synchronous Parallel Data or Serial Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) A(B) Asynchronous Parallel Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time from A/B or AE to High Impedance State at A Outputs or from A/B to High Impedance State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		95	220	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		60	130	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		45	100	ns
t_{PZH}, t_{PZL}	Propagation Delay Time from A/B or AE to Logical "1" or Logical "0" State at A Outputs or from A/B to Logical "1" or Logical "0" State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		180	480	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		75	190	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		55	140	ns
t_{THL}, t_{TLH}	Output Transition Time	V_{DD} = 5 V		100	200	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5 V	2	4		MHz
		V_{DD} = 10 V	5	10		MHz
		V_{DD} = 15 V	7	14		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5 V		125	250	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		35	70	ns

AC Electrical Characteristics (Cont'd.)

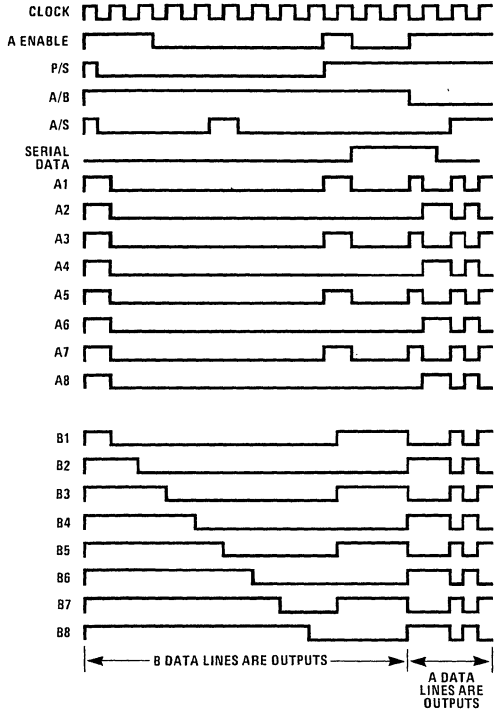
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{RCL}, t_{FCL}	Maximum Clock Rise & Fall Time	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V	15 15 15			μs μs μs
t_{SU}	Parallel (A or B) and Serial Data Setup Time	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		25 10 7	70 30 20	ns ns ns
t_{SU}	Control Inputs AE, A/B, P/S, A/S Setup Time	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		110 35 20	280 100 60	ns ns ns
t_{WH}	Minimum High Level AE, A/B, P/S, A/S Pulse Width	V_{DD} = 5 V V_{DD} = 10 V V_{DD} = 15 V		160 70 40	400 160 90	ns ns ns
C_{IN}	Average Input Capacitance	A and B Data I/O and A/B Control Input Any Other Input		7 5	15 7.5	pF pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		155		pF

Note 4: C_{PD} determines the no-load power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Schematic Diagram

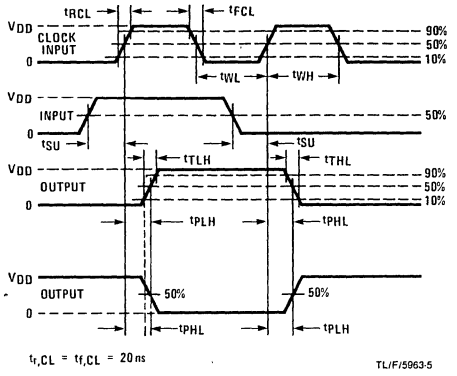


Switching Time Waveforms and Test Circuits



TL/F/5963-4

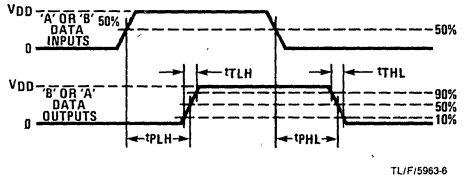
Synchronous Operation



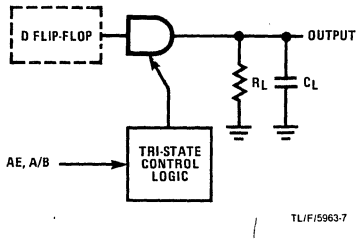
$t_{r,CL} = t_{f,CL} = 20\,ns$

TL/F/5963-5

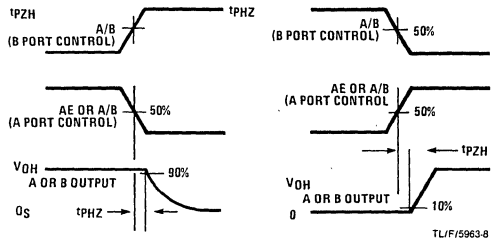
Asynchronous Operation



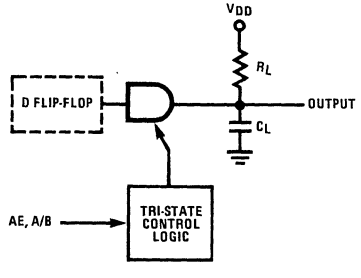
TL/F/5963-6



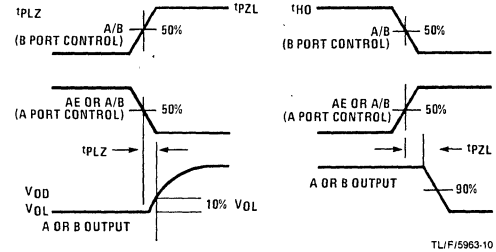
TL/F/5963-7



TL/F/5963-8



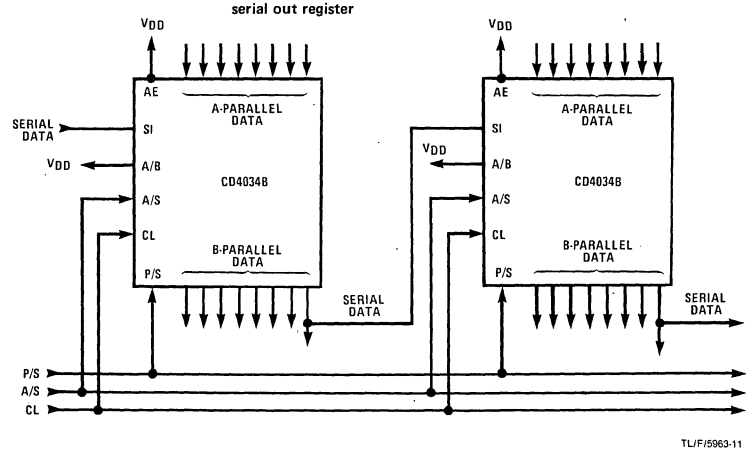
TL/F/5963-9



TL/F/5963-10

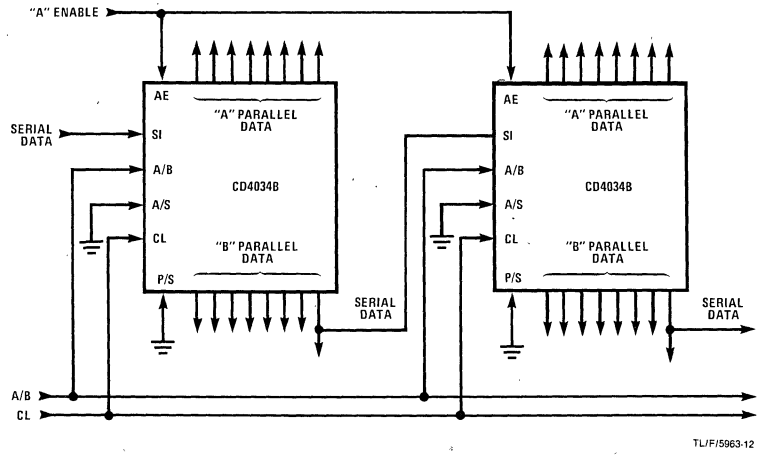
Applications

16-Bit parallel in/parallel out, parallel in/ serial out, serial in/parallel out, serial in/ serial out register



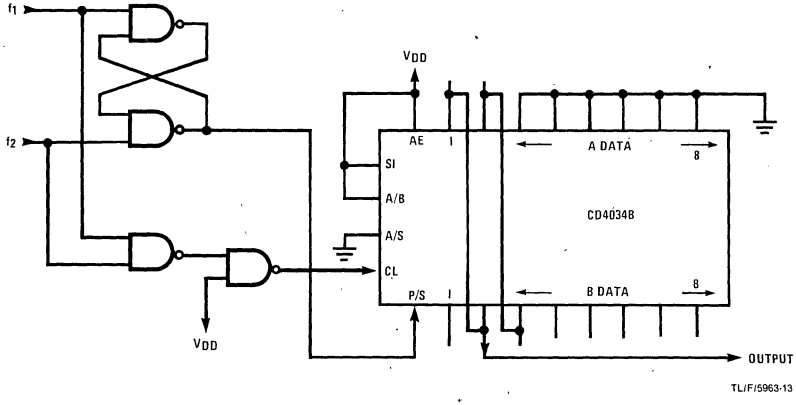
TL/F/5963-11

16-Bit serial in/gated parallel out register



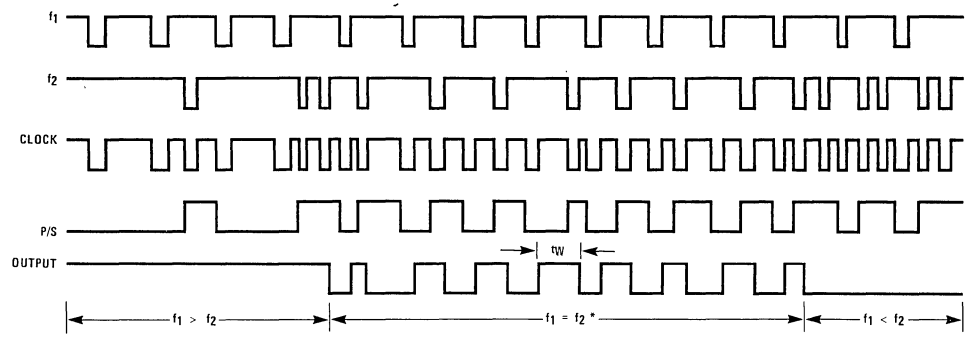
TL/F/5963-12

Frequency and Phase Comparator



TL/F/5963-13

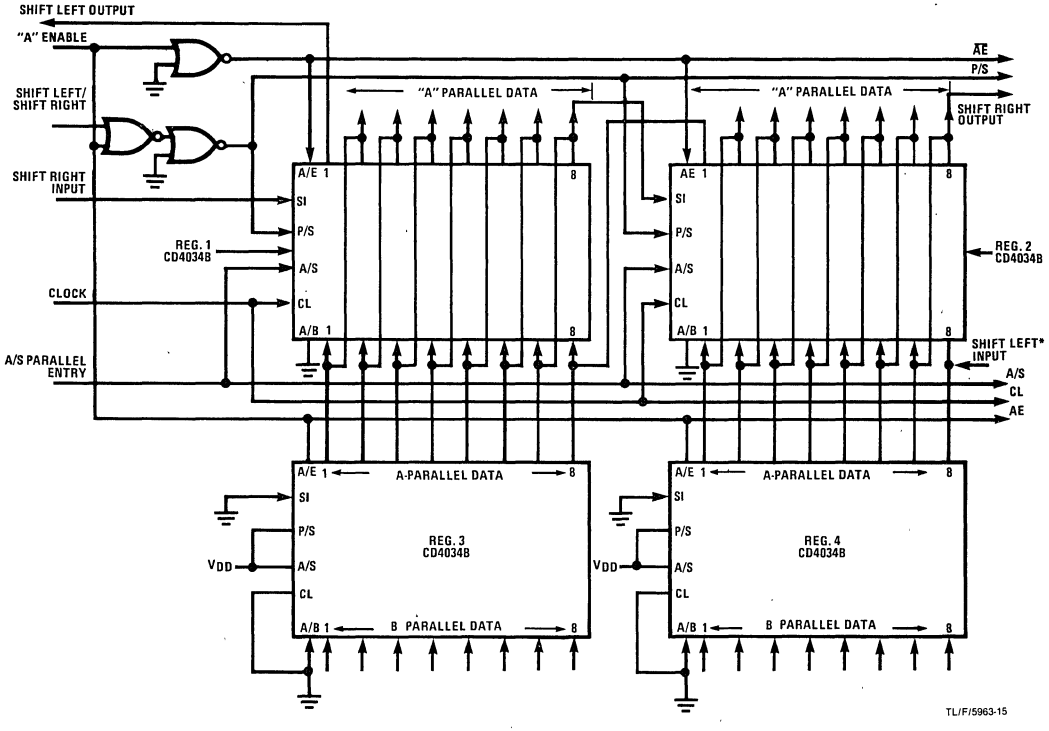
Applications (Cont'd.)



*WHEN $f_1=f_2$, t_W IS PROPORTIONAL TO THE PHASE OF f_1 WITH RESPECT TO f_2

TL/F/5963-14

Shift Right/Shift Left with Parallel Inputs



TL/F/5963-15

A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Registers 1 and 2 and enables the "A" data lines on Registers 3 and 4 and allows parallel data into Registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Registers 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

Truth Table

"A" ENABLE	P/S	A/B	A/S	MODE	OPERATION*
0	0	0	X	Serial	Synchronous Serial data input, A- and B-Parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous Serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
1	1	0	0	Parallel	B Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

*For synchronous operation (serial mode or when A/S = 0 in parallel mode), outputs change state at positive transition of the clock.

National Semiconductor

CD4035BM/CD4035BC 4-Bit Parallel-In/Parallel-Out Shift Register

General Description

The CD4035B 4-bit parallel-in/parallel-out shift register is a monlithic complementary MOS (CMOS) integrated circuit constructed with P- and N-channel enhancement mode transistors. This shift register is a 4-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via $J\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (parallel/serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the parallel/serial control is "high".

In the parallel or serial mode, information is transferred on positive clock transitions.

When the true/complement control is "high", the true contents of the register are available at the output terminals. When the true/complement control is "low", the outputs are the complements of the data in the register. The true/complement control functions asynchronously with respect to the clock signal.

$J\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With $J\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

Features

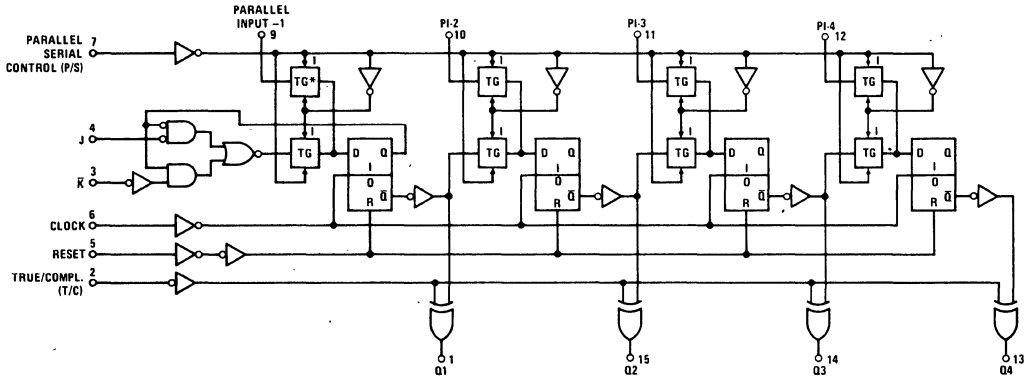
- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 4-stage clocked operation
- Synchronous parallel entry on all 4 stages
- $J\overline{K}$ inputs on first stage
- Asynchronous true/complement control on all outputs
- Reset Control
- Static flip-flop operation; master/slave configuration
- Buffered outputs
- Low power dissipation — 5 μW (typ.) (ceramic)
- High speed — to 5 MHz

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial controls
- Remote metering
- Computers

5

Logic Diagram



P/S = 0 = serial mode
T/C = 1 = true outputs
*TG = transmission gate

Input to output is:

a) A bidirectional low impedance when control input 1 is low and control input 2 is high.

b) An open circuit when control input 1 is high and control input 2 is low.

TL/F/5964-1

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions (Note 2)

V_{DD} dc Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4035BM	−55°C to +125°C
CD4035BC	−40°C to +85°C

DC Electrical Characteristics CD4035BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.3	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.5	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	0.36		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	0.9		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4035BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.5	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		1.0	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V

DC Electrical Characteristics (Cont'd.) CD4035BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.36		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.9		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics

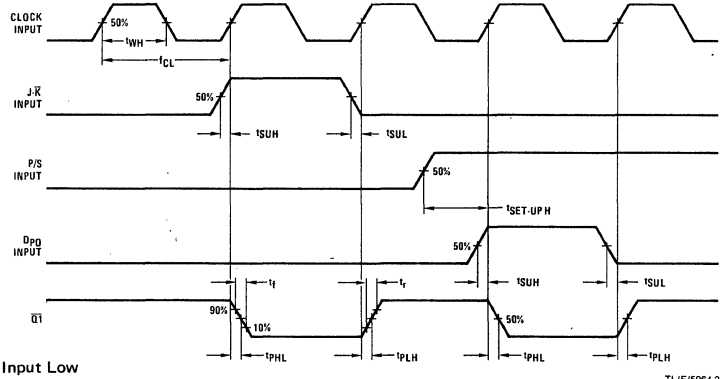
T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and t_f = 20 ns, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		75	150	ns
t_{THL}	Transition Time High Low to High	V_{DD} = 5V		90	175	ns
		V_{DD} = 10V		50	75	ns
		V_{DD} = 15V		40	60	ns
t_{TLH}	Transition Time Low to High	V_{DD} = 5V		135	270	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		60	120	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V	335	135		ns
		V_{DD} = 10V	165	50		ns
		V_{DD} = 15V	100	40		ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			5	μs
t_S	Minimum Set-up Time J/$\overline{K}$ Lines	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_S	Parallel-In Lines	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_S	P/S Control	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		35	60	ns
f_{MAX}	Maximum Clock Frequency	V_{DD} = 5V	1.5	2.5		MHz
		V_{DD} = 10V	3	6		MHz
		V_{DD} = 15V	5	9		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
RESET OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	500	ns
		V_{DD} = 10V		150	200	ns
		V_{DD} = 15V		85	150	ns
t_{WH}	Minimum Reset Pulse Width	V_{DD} = 5V		75	250	ns
		V_{DD} = 10V		30	110	ns
		V_{DD} = 15V		25	80	ns

Truth Table

C_L	$t_n - 1$ (INPUTS)				t_n (OUTPUTS)
	J	$\overline{K}$	R	$Q_n - 1$	Q_n
⎍	0	X	0	0	0
⎍	1	X	0	0	1
⎍	X	0	0	1	0
⎍	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⎍	X	1	0	1	1
⎎	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

Switching Time Waveforms

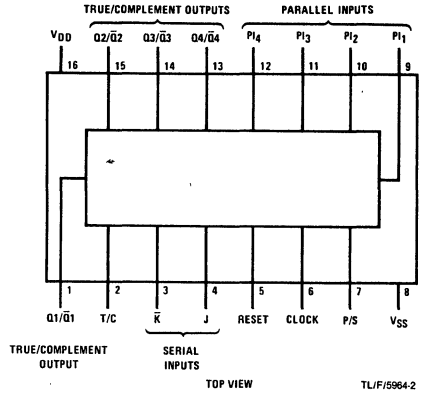


T/C Input Low
Reset Input Low

TL/F/5964-3

Connection Diagram

Dual-In-Line Package



TL/F/5964-2

Order Number CD4035BMJ or CD4035BCJ
See NS Package J16A

Order Number CD4035BMN or CD4035BCN
See NS Package N16E

National Semiconductor

CD4041M/CD4041C Quad True/Complement Buffer

General Description

The CD4041M/CD4041C is a quad true/complement buffer consisting of N- and P-channel enhancement mode transistors having low-channel resistance and high current (sourcing and sinking) capability. The CD4041 is intended for use as a buffer, line driver, or CMOS-to-TTL driver.

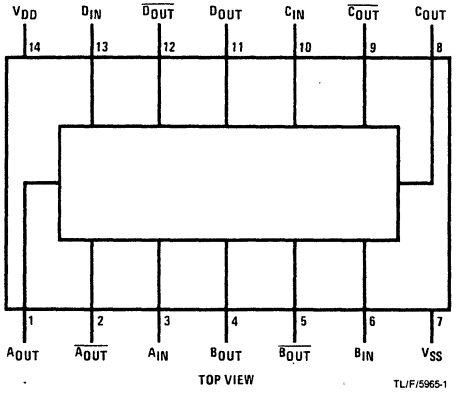
All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0 V to 15 V
- High noise immunity 40% V_{DD} (typ.)
- True output
  High current source and sink capability
  8 mA (typ.) @ $V_O = 9.5$ V, $V_{DD} = 10$ V
  3.2 mA (typ.) @ $V_O = 0.4$ V, $V_{DD} = 5$ V (two TTL loads)
- Complement output
  Medium current source and sink capability
  3.6 mA (typ.) @ $V_O = 9.5$ V, $V_{DD} = 10$ V
  1.6 mA (typ.) @ $V_O = 0.4$ V, $V_{DD} = 5$ V

Connection and Schematic Diagrams

Dual-In-Line Package



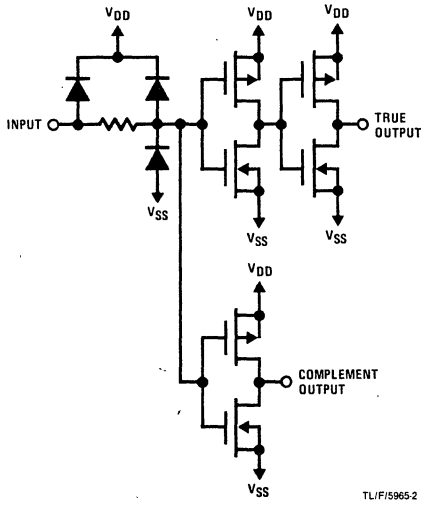
TOP VIEW

TL/F/5965-1

Order Number CD4041MJ or CD4041CJ
See NS Package J14A

Order Number CD4041MN or CD4041CN
See NS Package N14A

1 of 4 Identical Units



TL/F/5965-2

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4041M	−55°C to +125°C
CD4041C	−40°C to +85°C

DC Electrical Characteristics CD4041M (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.01	1		30	μA
		V_{DD} = 10V		2		0.01	2		60	μA
		V_{DD} = 15V		4		0.01	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.0		2	1.0		1.0	V
		V_{DD} = 10V, V_O = 1V or 9V		2.0		4	2.0		2.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		3.0		6	3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	4.0		4.0	3		4.0		V
		V_{DD} = 10V, V_O = 1V or 9V	8.0		8.0	6		8.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	12.0		12.0	9		12.0		V
I_{OL}	Low Level Output Current	V_{IL} = 0V								
	True Output	V_{DD} = 5V, V_O = 0.4V	2.1		1.6	3.2		1.2		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	6.25		5.0	10		3.5		mA
		V_{DD} = 15V, V_O = 1.5V	14		12	24		8		mA
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$								
	Complement Output	V_{DD} = 5V, V_O = 0.4V	1.0		0.8	1.6		0.55		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	2.5		2	4.0		1.4		mA
		V_{DD} = 15V, V_O = 1.5V	5.5		4.5	9.0		3.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$								
	True Output	V_{DD} = 5V, V_O = 4.6V	−1.75		−1.4	−2.8		−1.0		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−5.0		−4.0	−8.0		−2.8		mA
		V_{DD} = 15V, V_O = 13.5V	−11		−9	−18		−6		mA
I_{OH}	High Level Output Current	V_{IL} = 0V								
	Complement Output	V_{DD} = 5V, V_O = 4.6V	−0.75		−0.6	−1.2		−0.4		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−2.25		−1.8	−3.6		−1.25		mA
		V_{DD} = 15V, V_O = 13.5V	−4.8		−4	−8		−2.7		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

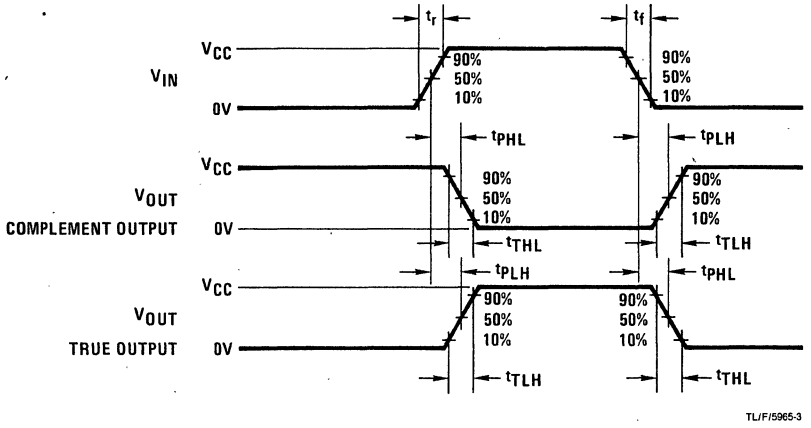
DC Electrical Characteristics CD4041C (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.01	4		30	μA
		V_{DD} = 10V		8		0.01	8		60	μA
		V_{DD} = 15V		16		0.01	16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.0		2	1.0		1.0	V
		V_{DD} = 10V, V_O = 1V or 9V		2.0		4	2.0		2.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		3.0		6	3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	4.0		4.0	3		4.0		V
		V_{DD} = 10V, V_O = 1V or 9V	8.0		8.0	6		8.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	12.0		12.0	9		12.0		V
I_{OL}	Low Level Output Current	V_{IL} = 0V								
	True Output	V_{DD} = 5V, V_O = 0.4V	1.7		1.5	3.2		1.2		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	4.9		4.3	10		3.5		mA
		V_{DD} = 15V, V_O = 1.5V	11		10	24		8		mA
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$								
	Complement Output	V_{DD} = 5V, V_O = 0.4V	0.75		0.68	1.6		0.55		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	2.0		1.8	4.0		1.4		mA
		V_{DD} = 15V, V_O = 1.5V	4.4		3.8	9.0		3.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$								
	True Output	V_{DD} = 5V, V_O = 4.6V	−1.5		−1.3	−2.8		−1.0		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−4.0		−3.5	−8.0		−2.8		mA
		V_{DD} = 15V, V_O = 13.5V	−8.7		−7.5	−18		−6		mA
I_{OH}	High Level Output Current	V_{IL} = 0V								
	Complement Output	V_{DD} = 5V, V_O = 4.6V	−0.57		−0.50	−1.2		−0.4		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.8		−1.6	−3.6		−1.25		mA
		V_{DD} = 15V, V_O = 13.5V	−3.9		−3.4	−8.0		−2.7		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time	V_{DD} = 5V		60	120	ns
	True Output	V_{DD} = 10V		35	70	ns
		V_{DD} = 15V		25	50	ns
t_{PHL} or t_{PLH}	Propagation Delay Time	V_{DD} = 5V		75	150	ns
	Complement Output	V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		30	65	ns
t_{THL} or t_{TLH}	Output Transition Time	V_{DD} = 5V		55	110	ns
	True Output	V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{THL} or t_{TLH}	Output Transition Time	V_{DD} = 5V		90	180	ns
	Complement Output	V_{DD} = 10V		45	90	ns
		V_{DD} = 15V		35	75	ns
C_{IN}	Input Capacitance	Any Input		10	15	pF

Switching Time Waveforms



TL/F/5965-3

National Semiconductor

CD4042BM/CD4042BC Quad Clocked D Latch

General Description

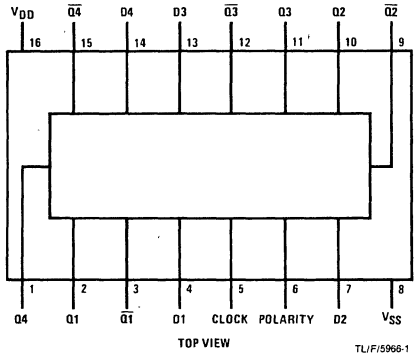
The CD4042BM/CD4042BC quad clocked "D" latch is a monolithic complementary MOS (CMOS) integrated circuit constructed with P- and N-channel enhancement mode transistors. The outputs Q and $\overline{Q}$ either latch or follow the data input depending on the clock level which is programmed by the polarity input. For polarity = 0; the information present at the data input is transferred to Q and $\overline{Q}$ during 0 clock level; and for polarity = 1, the transfer occurs during the 1 clock level. When a clock transition occurs (positive for polarity = 0 and negative for polarity = 1), the information present at the input during the clock transition is retained at the outputs until an opposite clock transition occurs.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Clock polarity control	
■ Fully buffered data inputs	
■ Q and $\overline{Q}$ outputs	

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5966-1

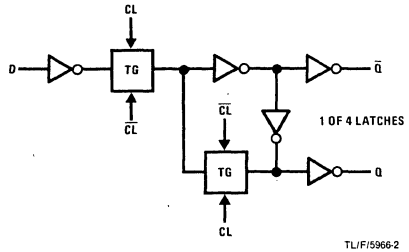
Truth Table

CLOCK	POLARITY	Q
0	0	D
⌐	0	Latch
1	1	D
⌙	1	Latch

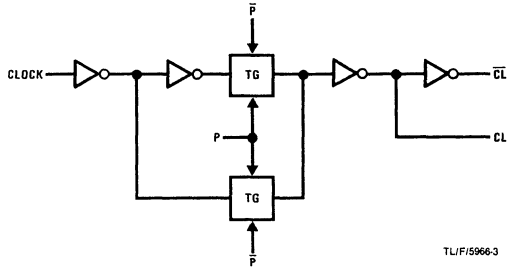
Order Number CD4042BMJ or CD4042BCJ
See NS Package J16A

Order Number CD4042BMN or CD4042BCN
See NS Package N16E

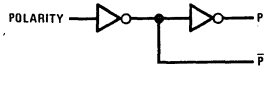
Logic Diagrams



TL/F/5966-2



TL/F/5966-3



TL/F/5966-4

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4042BM	−55°C to +125°C
CD4042BC	−40°C to +85°C

DC Electrical Characteristics CD4042BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.02	1		30	μA
		V_{DD} = 10V		2		0.02	2		60	μA
		V_{DD} = 15V		4		0.02	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 4)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 4)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4042BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.02	4		30	μA
		V_{DD} = 10V		8		0.02	8		60	μA
		V_{DD} = 15V		16		0.02	16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD4042BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 4)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 4)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time Data In to Q	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		60	120	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Data In to $\overline{Q}$	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		50	100	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to $\overline{Q}$	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		115	230	ns
		V_{DD} = 15V		90	180	ns
t_H	Minimum Hold Time	V_{DD} = 5V		60	120	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		0	50	ns
		V_{DD} = 10V		0	30	ns
		V_{DD} = 15V		0	25	ns
t_W	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		30	60	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		50	100	ns
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

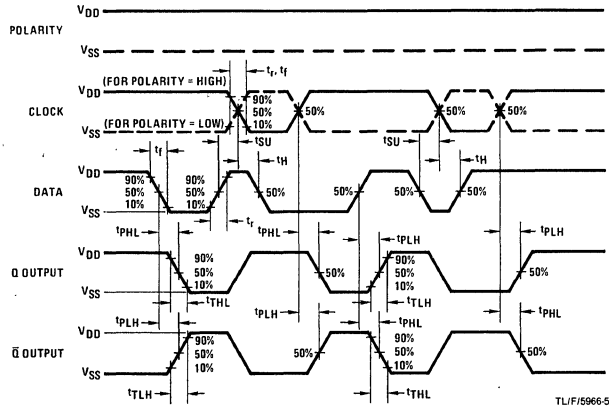
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Being a latch, the CD4042BM/CD4042BC is not clock rise and fall time sensitive.

Note 4: I_{OL} and I_{OH} are tested one output at a time.

Switching Time Waveforms



National Semiconductor

CD4043BM/CD4043BC Quad TRI-STATE® NOR R/S Latches
CD4044BM/CD4044BC Quad TRI-STATE NAND R/S Latches

General Description

CD4043BM/CD4043BC are quad cross-couple TRI-STATE CMOS NOR latches, and CD4044BM/CD4044BC are quad cross-couple TRI-STATE CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. There is a common TRI-STATE ENABLE input for all four latches. A logic "1" on the ENABLE input connects the latch states to the Q outputs. A logic "0" on the ENABLE input disconnects the latch states from the Q outputs resulting in an open circuit condition on the Q output. The TRI-STATE feature allows common bussing of the outputs.

Features

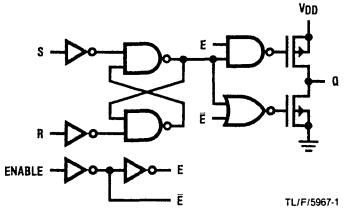
- Wide supply voltage range 3 V to 15 V
- Low power 100 nW (typ.)
- High noise immunity 0.45 V_{DD} (typ.)
- Separate SET and RESET inputs for each latch
- NOR and NAND configuration
- TRI-STATE output with common output enable

Applications

- Multiple bus storage
- Stobed register
- Four bits of independent storage with output enable
- General digital logic

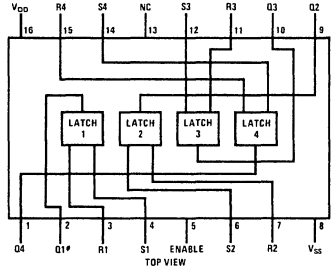
Schematic and Connection Diagrams

CD4043BM/CD4043BC



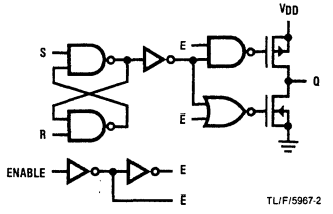
TL/F/5967-1

CD4043BM/CD4043BC
Dual-In-Line and Flat Packages



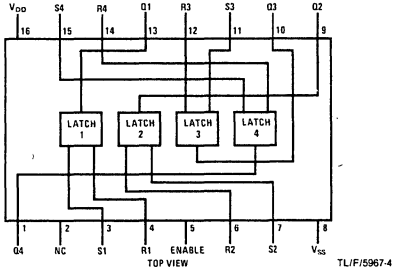
TL/F/5967-3

CD4044BM/CD4044BC



TL/F/5967-2

CD4044BM/CD4044BC
Dual-In-Line and Flat Packages



TL/F/5967-4

Order Number CD4043BMJ, CD4043BCJ, CD4044BMJ or CD4044BCJ
See NS Package J16A

Order Number CD4043BMN, CD4043BCN, CD4044BMN or CD4044BCN
See NS Package N16E

Truth Table

CD4043BM/CD4043BC

S	R	E	Q
X	X	0	OC
0	0	1	NC
1	0	1	1
0	1	1	0
1	1	1	Δ

CD4044BM/CD4044BC

S	R	E	Q
X	X	0	OC
1	1	1	NC
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

OC – TRI-STATE
NC – No change
X – Don't care
Δ – Dominated by S=1 input
ΔΔ – Dominated by R=0 input

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18 V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3.0 to 15 V
V_{IN} Input Voltage	0 to V_{DD} V
T_A Operating Temperature Range	
CD4043BM, CD4044BM	−55°C to +125°C
CD4043BC, CD4044BC	−40°C to +85°C

DC Electrical Characteristics CD4043BM/CD4044BM (Note 2)

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5.0		0.01	5.0		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.01	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 5.0 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11		11	8.25		11		V
I_{OL}	Low Level Output Current	V_{IL} = 0 V, V_{IH} = V_{DD}								
		V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	1.0		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.6		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	6.8		2.4		mA
I_{OH}	High Level Output Current	V_{IL} = 0 V, V_{IH} = V_{DD}								
		V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−0.4		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−1.0		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−3.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4043BC/CD4044BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.01	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.01	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\mu A$, V_{IL} = 0V, V_{IH} = V_{DD}								
		V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V

DC Electrical Characteristics CD4043BC/CD4044BC (cont'd)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
V_{IL}	Low Level Input Voltage	$\|I_O\| \leq 1\,\mu A$								
		$V_{DD} = 5.0\,V$, $V_O = 0.5\,V$ or $4.5\,V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10\,V$, $V_O = 1.0\,V$ or $9.0\,V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| \leq 1\,\mu A$								
		$V_{DD} = 5.0\,V$, $V_O = 0.5\,V$ or $4.5\,V$	3.5		3.5			3.5		V
		$V_{DD} = 5.0\,V$, $V_O = 1.0\,V$ or $9.0\,V$	7.0		7.0			7.0		V
		$V_{DD} = 15\,V$, $V_O = 1.5\,V$ or $13.5\,V$	11		11			11		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IL} = 0\,V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5.0\,V$, $V_O = 0.4\,V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10\,V$, $V_O = 0.5\,V$	1.3		1.1	2.2		0.9		mA
		$V_{DD} = 15\,V$, $V_O = 1.5\,V$	3.6		3.0	6.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IL} = 0\,V$, $V_{IH} = V_{DD}$								
		$V_{DD} = 5.0\,V$, $V_O = 4.6\,V$	−0.52		−0.44	−0.32		−0.36		mA
		$V_{DD} = 10\,V$, $V_O = 9.5\,V$	−1.3		−1.1	−0.8		−0.9		mA
		$V_{DD} = 15\,V$, $V_O = 13.5\,V$	−3.6		−3.0	−2.4		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15\,V$, $V_{IN} = 0\,V$	−0.3			−0.3			−1.0	μA
		$V_{DD} = 15\,V$, $V_{IN} = 15\,V$	0.3			0.3			1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, Input $t_r = t_f = 20\,ns$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	Propagation Delay S or R to Q	$V_{DD} = 5.0\,V$		175	350	ns
		$V_{DD} = 10\,V$		75	175	ns
		$V_{DD} = 15\,V$		60	120	ns
t_{PZH}, t_{PHZ}	Propagation Delay Enable to Q (High)	$V_{DD} = 5.0\,V$		115	230	ns
		$V_{DD} = 10\,V$		55	110	ns
		$V_{DD} = 15\,V$		40	80	ns
t_{PZL}, t_{PLZ}	Propagation Delay Enable to Q (Low)	$V_{DD} = 5.0\,V$		100	200	ns
		$V_{DD} = 10\,V$		50	100	ns
		$V_{DD} = 15\,V$		40	80	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5.0\,V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15\,V$		40	80	ns
t_{WO}	Minimum SET or RESET Pulse Width	$V_{DD} = 5.0\,V$		80	160	ns
		$V_{DD} = 10\,V$		40	80	ns
		$V_{DD} = 15\,V$		20	40	ns
C_{IN}	Input Capacitance			5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

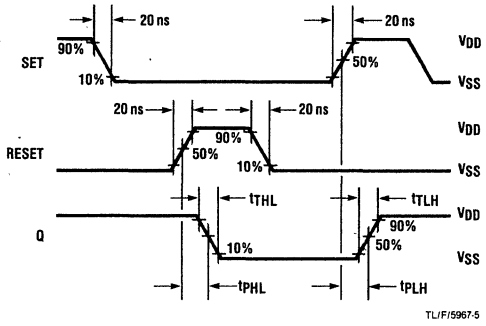
Note 2: $V_{SS} = 0\,V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

5

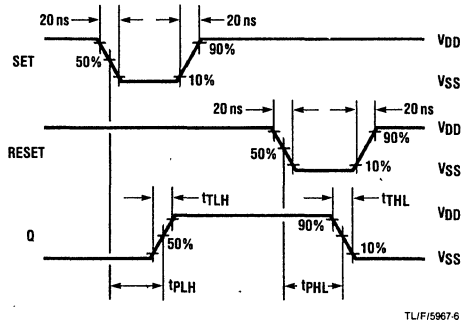
Timing Waveforms

CD4043B



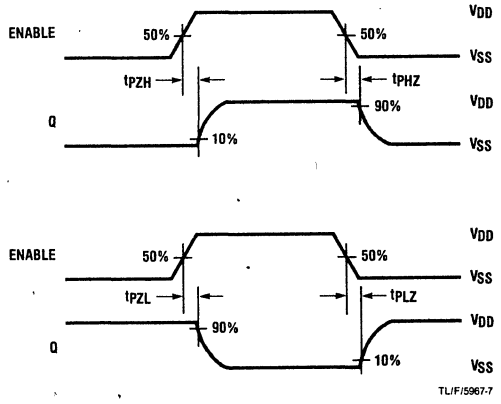
TL/F/5967-5

CD4044B



TL/F/5967-6

Enable Timing



TL/F/5967-7

National Semiconductor

CD4046BM/CD4046BC Micropower Phase-Locked Loop

General Description

The CD4046B micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more.

The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation, if necessary.

Features

■ Wide supply voltage range	3.0 V to 18 V
■ Low dynamic power consumption	70 μW (typ.) at f_o = 10 kHz, V_{DD} = 5 V
■ VCO frequency	1.3 MHz (typ.) at V_{DD} = 10 V
■ Low frequency drift with temperature	0.06%/°C at V_{DD} = 10 V
■ High VCO linearity	1% (typ.)

Applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

5

Block and Connection Diagrams

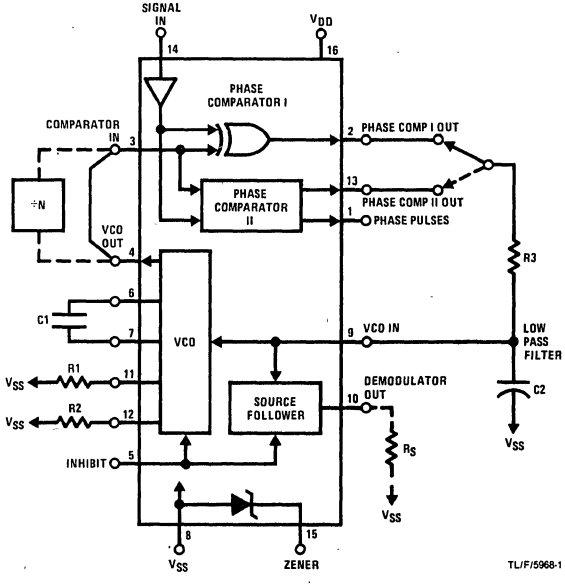
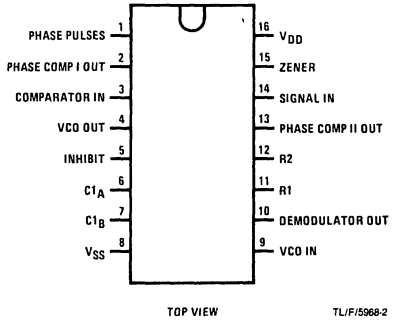


FIGURE 1

Dual-In-Line Package



Order Number CD4046BMJ or CD4046BCJ
See NS Package J16A

Order Number CD4046BMN or CD4046BCN
See NS Package N16E

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4046BM	−55°C to +125°C
CD4046BC	−40°C to +85°C

DC Electrical Characteristics CD4046BM (Note 2)

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	PIN 5 = V_{DD}, PIN 14 = V_{DD}, PIN 3, 9 = V_{SS}								
		V_{DD} = 5V		5		0.005	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.015	20		600	μA
		PIN 5 = V_{DD}, PIN 14 = Open PIN 3,2 = V_{SS}								
		V_{DD} = 5V		45		5	35		185	μA
		V_{DD} = 10V		450		20	350		650	μA
		V_{DD} = 15V		1200		50	900		1500	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	All Inputs Except Signal Input								
		V_{DD} = 14V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
C_{IN}	Input Capacitance	Any Input, (Note 3)							7.5	pF
P_T	Total Power Dissipation	f_o = 10kHz, R1 = 1MΩ R2 = ∞, VCO_{IN} = V_{DD}/2								
		V_{DD} = 5V				0.07				mW
		V_{DD} = 10V				0.6				mW
		V_{DD} = 15V				2.4				mW

DC Electrical Characteristics CD4046BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	PIN 5 = V_{DD}, PIN 14 = V_{DD}, PIN 3,9 = V_{SS}								
		V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
		PIN 5 = V_{DD}, PIN 14 = Open, PIN 3,9 = V_{SS}								
		V_{DD} = 5V		70		5	55		205	μA
		V_{DD} = 10V		530		20	410		710	μA
		V_{DD} = 15V		1500		50	1200		1800	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		1..0	8.25		1..0		V
I_{OL}	Low Level Output Current (Note 4)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 4)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	All Inputs Except Signal Input								
		V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
C_{IN}	Input Capacitance	Any Input, (Note 3)					7.5			pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ R2 = ∞, VCO_{IN} = $V_{DD}/2$								
		V_{DD} = 5V				0.07				mW
		V_{DD} = 10V				0.6				mW
		V_{DD} = 15V				2.4				mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

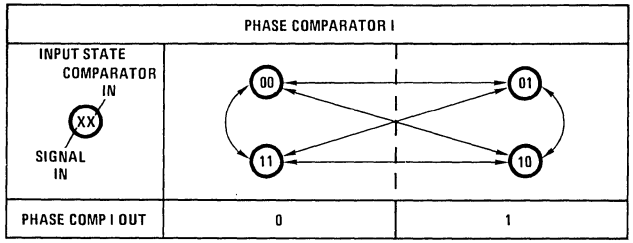
Note 4: I_{OH} and I_{OL} are tested one output at a time.

5

AC Electrical Characteristics CD4046BM/CD4046BC $T_A = 25°C$, $C_L = 50\,pF$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	VCO Section					
I_{DD}	Operating Current	f_o = 10kHz, R1 = 1MΩ, R2 = ∞, $VCO_{IN} = V_{DD}/2$				
		V_{DD} = 5V		20		μA
		V_{DD} = 10V		90		μA
		V_{DD} = 15V		200		μA
f_{MAX}	Maximum Operating Frequency	C1 = 50 pF, R1 = 10kΩ, R2 = ∞, $VCO_{IN} = V_{DD}$				
		V_{DD} = 5V	0.4	0.8		MHz
		V_{DD} = 10V	0.6	1.2		MHz
		V_{DD} = 15V	1.0	1.6		MHz
	Linearity	VCO_{IN} = 2.5V ∓0.3V, R1 ⩾ 10kΩ, V_{DD} = 5V		1		%
		VCO_{IN} = 5V ±2.5V, R1⩾400kΩ, V_{DD} = 10V		1		%
		VCO_{IN} = 7.5V ±5V, R1 ⩾ 1 MΩ, V_{DD} = 15V		1		%
	Temperature-Frequency Stability No Frequency Offset, $f_{MIN} = 0$	%/°C∝1/f. V_{DD} R2 = ∞				
		V_{DD} = 5V		0.12–0.24		%/°C
		V_{DD} = 10V		0.04–0.08		%/°C
		V_{DD} = 15V		0.015–0.03		%/°C
	Frequency Offset, $f_{MIN} \neq 0$	V_{DD} = 5V		0.06–0.12		%/°C
		V_{DD} = 10V		0.05–0.1		%/°C
		V_{DD} = 15V		0.03–0.06		%/°C
VCO_{IN}	Input Resistance	V_{DD} = 5V		10^6		MΩ
		V_{DD} = 10V		10^6		MΩ
		V_{DD} = 15V		10^6		MΩ
VCO	Output Duty Cycle	V_{DD} = 5V		50		%
		V_{DD} = 10V		50		%
		V_{DD} = 15V		50		%
t_{THL}	VCO Output Transition Time	V_{DD} = 5V		90	200	ns
t_{THL}		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		45	80	ns
	Phase Comparators Section					
R_{IN}	Input Resistance					
	Signal Input	V_{DD} = 5V	1	3		MΩ
		V_{DD} = 10V	0.2	0.7		MΩ
		V_{DD} = 15V	0.1	0.3		MΩ
	Comparator Input	V_{DD} = 5V		10^6		MΩ
		V_{DD} = 10V		10^6		MΩ
		V_{DD} = 15V		10^6		MΩ
	AC-Coupled Signal Input Voltage Sensitivity	C_{SERIES} = 1000 pF f = 50 kHz				
		V_{DD} = 5V		200	400	mV
		V_{DD} = 10V		400	800	mV
		V_{DD} = 15V		700	1400	mV
	Demodulator Output					
VCO_{IN} – V_{DEM}	Offset Voltage	RS ⩾ 10 kΩ, V_{DD} = 5V		1.50	2.2	V
		RS ⩾ 10 kΩ, V_{DD} = 10V		1.50	2.2	V
		RS ⩾ 50 kΩ, V_{DD} = 15V		1.50	2.2	V
	Linearity	RS ⩾ 50 kΩ				
		VCO_{IN} = 2.5 ±0.3V, V_{DD} = 5V		0.1		%
		VCO_{IN} = 5 ±2.5V, V_{DD} = 10V		0.6		%
		VCO_{IN} = 7.5 ±5V, V_{DD} = 15V		0.8		%
	Zener Diode					
V_Z	Zener Diode Voltage					
	CD4046BM	I_Z = 50μA	6.7	7.0	7.3	V
	CD4046BC		6.3	7.0	7.7	V
R_Z	Zener Dynamic Resistance	I_Z = 1mA		100		Ω

Phase Comparator State Diagrams



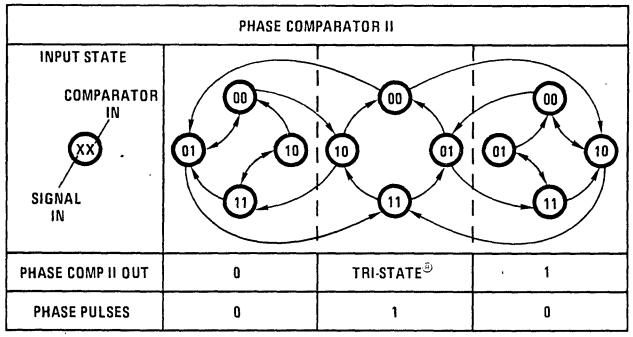


FIGURE 2 TL/F/5968-3

Typical Waveforms

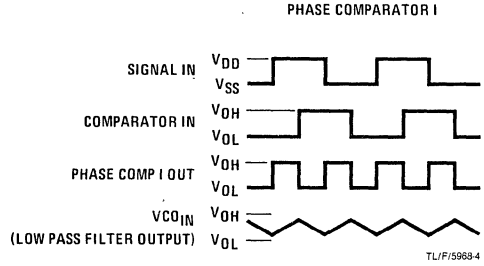


FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition

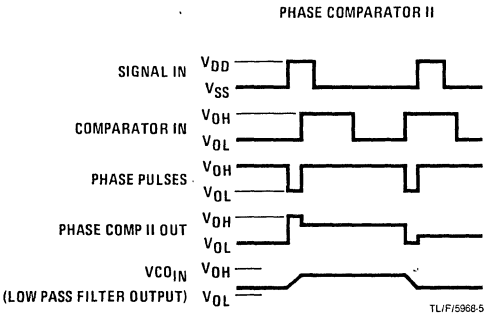


FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Performance Characteristics

Typical Center Frequency vs C1 for R1 = 10 kΩ, 100 kΩ and 1 MΩ

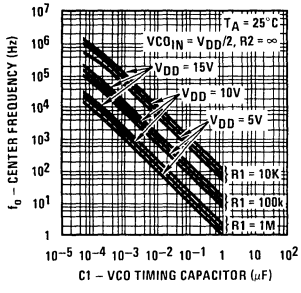


FIGURE 5a TL/F/5968-6

Typical Frequency Offset vs C1 for R2 = 10 kΩ, 100 kΩ and 1 MΩ

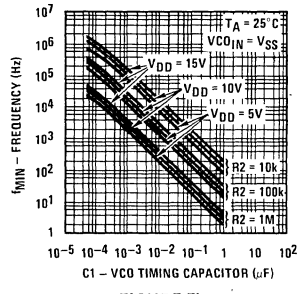


FIGURE 5b TL/F/5968-7

Typical f_{MAX}/f_{MIN} vs R2/R1

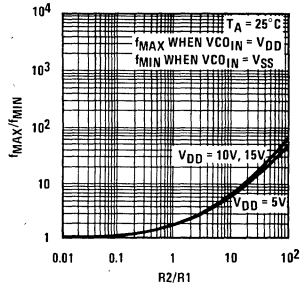


FIGURE 5c TL/F/5968-8

Typical VCO Power Dissipation at Center Frequency vs R1

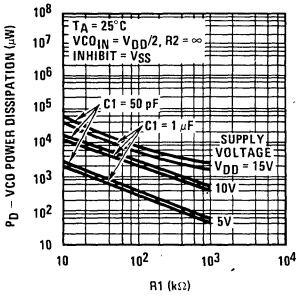


FIGURE 6a TL/F/5968-9

Typical VCO Power Dissipation at f_{MIN} vs R2

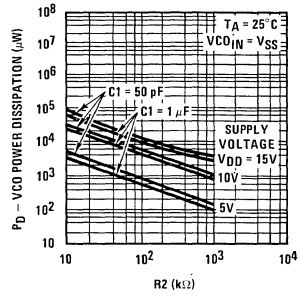


FIGURE 6b TL/F/5968-10

Typical Source Follower Power Dissipation vs R_S

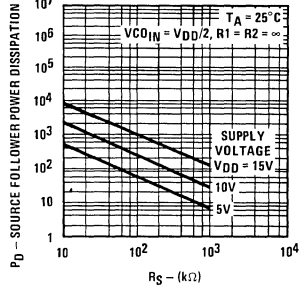


FIGURE 6c TL/F/5968-11

Typical VCO Linearity vs R1 and C1

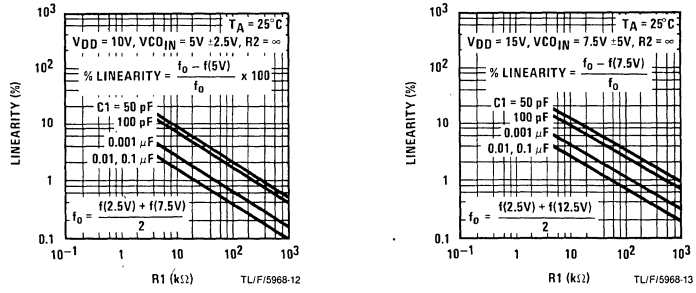


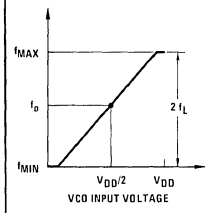
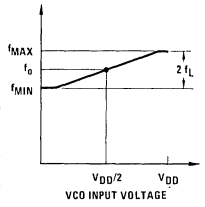
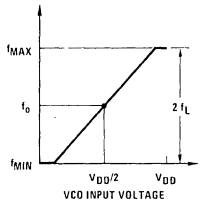
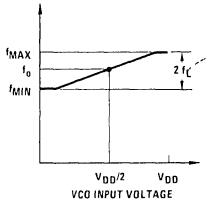
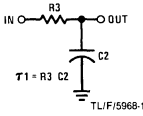
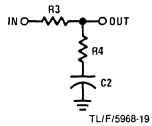
FIGURE 7

Note. To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

Design Information

This information is a guide for approximating the value of external components for the CD4046B in a phase-locked-loop system. The selected external components must be within the following ranges: R1, R2 $\geq$ 10 kΩ, $R_S \geq$ 10 kΩ, C1 $\geq$ 50 pF.

In addition to the given design information, refer to *Figure 5* for R1, R2 and C1 component selections.

CHARACTERISTICS	USING PHASE COMPARATOR I		USING PHASE COMPARATOR II	
	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET	VCO WITHOUT OFFSET R2 = ∞	VCO WITH OFFSET
VCO Frequency	 TL/F/5968-14	 TL/F/5968-15	 TL/F/5968-16	 TL/F/5968-17
For No Signal Input	VCO in PLL system will adjust to center frequency, f_o		VCO in PLL system will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, 2 f_L	2 f_L = full VCO frequency range 2 f_L = $f_{max} - f_{min}$			
Frequency Capture Range, 2f_C	 TL/F/5968-18 $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$		$f_C = f_L$	
Loop Filter Component Selection	 TL/F/5968-19	For 2 f_C, see Ref.		
Phase Angle Between Signal and Comparator	90° at center frequency (f_o), approximating 0° and 180° at ends of lock range (2 f_L)		Always 0° in lock	
Locks on Harmonics of Center Frequency	Yes		No	
Signal Input Noise Rejection	High		Low	
VCO Component Selection	–Given: f_o –Use f_o with *Figure 5a* to determine R1 and C1	–Given: f_o and f_L –Calculate f_{min} from the equation $f_{min} = f_o - f_L$ –Use f_{min} with *Figure 5b* to determine R2 and C1 –Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ –Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1	–Given: f_{max} –Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ –Use f_o with *Figure 5a* to determine R1 and C1	–Given: f_{min} and f_{max} –Use f_{min} with *Figure 5b* to determine R2 and C1 –Calculate $\frac{f_{max}}{f_{min}}$ –Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1

REF. G.S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
Floyd Gardner, "Phaselock Techniques," John Wiley & Sons, 1966.

5

National Semiconductor

CD4047BM/CD4047BC Low Power Monostable/Astable Multivibrator

General Description

CD4047B is capable of operating in either the monostable or astable mode. It requires an external capacitor (between pins 1 and 3) and an external resistor (between pins 2 and 3) to determine the output pulse width in the monostable mode, and the output frequency in the astable mode.

Astable operation is enabled by a high level on the astable input or low level on the $\overline{\text{astable}}$ input. The output frequency (at 50% duty cycle) at Q and $\overline{Q}$ outputs is determined by the timing components. A frequency twice that of Q is available at the Oscillator Output; a 50% duty cycle is not guaranteed.

Monostable operation is obtained when the device is triggered by low-to-high transition at + trigger input or high-to-low transition at − trigger input. The device can be retriggered by applying a simultaneous low-to-high transition to both the + trigger and retrigger inputs.

A high level on Reset input resets the outputs Q to low, $\overline{Q}$ to high.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

SPECIAL FEATURES

- Low power consumption: special CMOS oscillator configuration
- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required

MONOSTABLE MULTIVIBRATOR FEATURES

- Positive- or negative-edge trigger
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse width expansion
- Long pulse widths possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

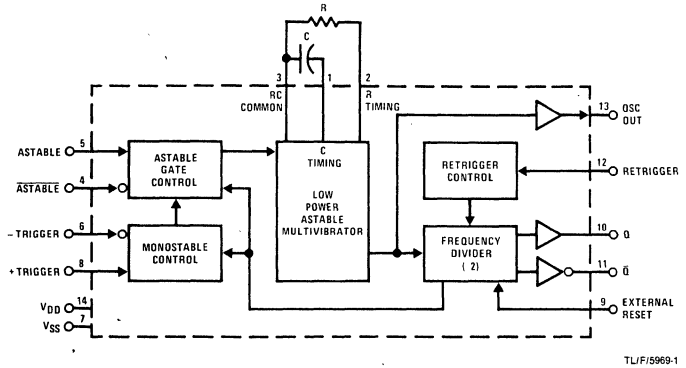
ASTABLE MULTIVIBRATOR FEATURES

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available
- Good astable frequency stability
  typical frequency deviation = ±2% + 0.03%/°C @ 100 kHz
  = ±0.5% + 0.015%/°C @ 10 kHz
  (circuits trimmed to frequency V_{DD} = 10 V ± 10%)

Applications

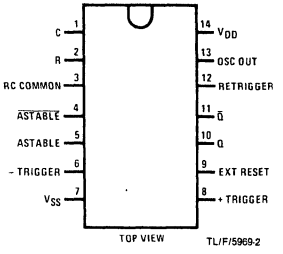
- Frequency discriminators
- Timing circuits
- Time-delay applications
- Envelope detection
- Frequency multiplication
- Frequency division

Block and Connection Diagrams



TL/F/5969-1

Dual-In-Line Package



TOP VIEW TL/F/5969-2

Order Number CD4047BMJ or CD4047BCJ
See NS Package J14A

Order Number CD4047BMN or CD4047BCN
See NS Package N14A

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4047BM	−55°C to +125°C
CD4047BC	−40°C to +85°C

DC Electrical Characteristics CD4047BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4047BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

DC Electrical Characteristics (Cont'd.) CD4047BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

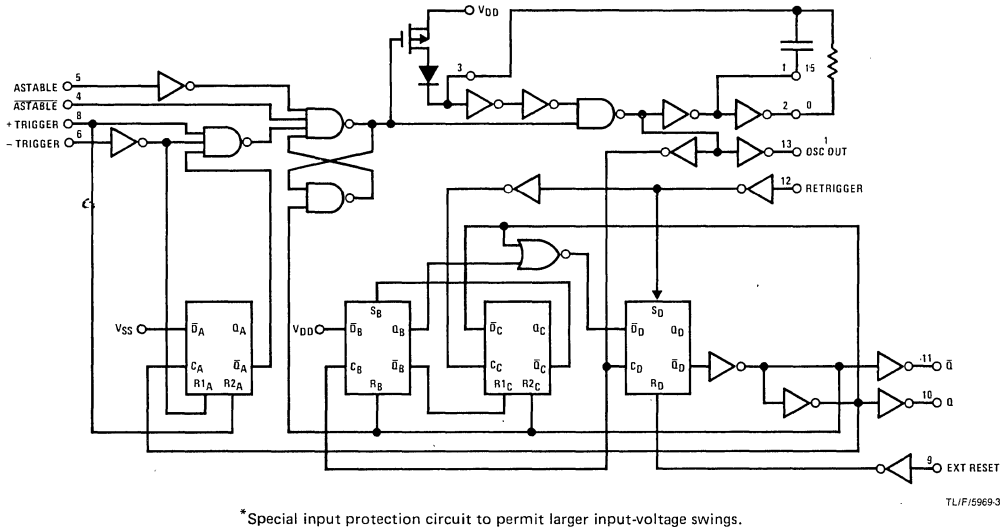
Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics CD4047B

T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_r = t_f = 20 ns, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time Astable, $\overline{\text{Astable}}$ to Osc Out	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_{PHL}, t_{PLH}	Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$	V_{DD} = 5V		550	900	ns
		V_{DD} = 10V		250	500	ns
		V_{DD} = 15V		200	400	ns
t_{PHL}, t_{PLH}	+ Trigger, − Trigger to Q, $\overline{Q}$	V_{DD} = 5V		700	1200	ns
		V_{DD} = 10V		300	600	ns
		V_{DD} = 15V		240	480	ns
t_{PHL}, t_{PLH}	+ Trigger, Retrigger to Q, $\overline{Q}$	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		175	300	ns
		V_{DD} = 15V		150	250	ns
t_{PHL}, t_{PLH}	Reset to Q, $\overline{Q}$	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		125	250	ns
		V_{DD} = 15V		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q, $\overline{Q}$, Osc Out	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Duration	Any Input				
		V_{DD} = 5V		500	1000	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		160	320	ns
t_{RCL}, t_{FCL}	+ Trigger, Retrigger, Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			5	μs
		V_{DD} = 15V			5	μs
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

Logic Diagram



TL/F/5969-3

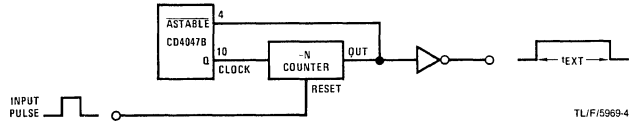
*Special input protection circuit to permit larger input-voltage swings.

Truth Table

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	TYPICAL OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator					
Free-Running	4, 5, 6, 14	7, 8, 9, 12		10, 11, 13	$t_A(10, 11) = 4.40\ RC$
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	$t_A(13) = 2.20\ RC$
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	$t_M(10, 11) = 2.48\ RC$
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown*	14	5, 6, 7, 8, 9, 12	(See Figure)	(See Figure)	(See Figure)

Note: External resistor between terminals 2 and 3. External capacitor between terminals 1 and 3.

*** Typical Implementation of External Countdown Option**

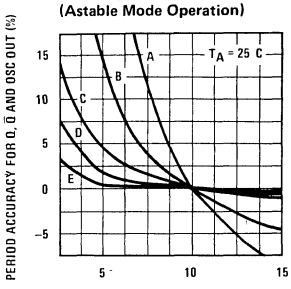


TL/F/5969-4

$$t_{EXT} = (N - 1)\ t_A + (t_M + t_A/2)$$

Typical Performance Characteristics

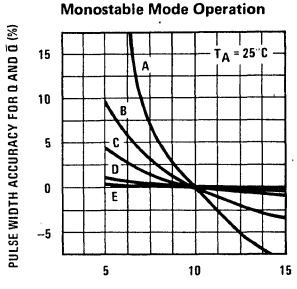
Typical Q, $\overline{Q}$, Osc Out Period Accuracy vs Supply Voltage (Astable Mode Operation)



TL/F/5969-5

	$f_{Q, \overline{Q}}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF
E	100 Hz	2.2M	1000 pF

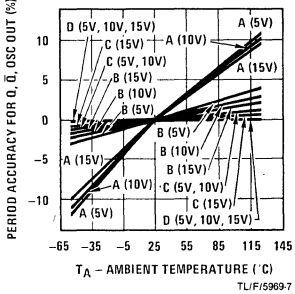
Typical Q, $\overline{Q}$, Pulse Width Accuracy vs Supply Voltage Monostable Mode Operation



TL/F/5969-6

	t_M	R	C
A	2 μs	22k	10 pF
B	7 μs	22k	100 pF
C	60 μs	220k	100 pF
D	550 μs	220k	1000 pF
E	5.5 ms	2.2M	1000 pF

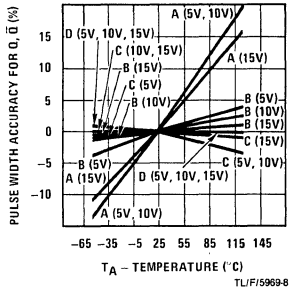
Typical Q, $\overline{Q}$ and Osc Out Period Accuracy vs Temperature Astable Mode Operation



TL/F/5969-7

	$f_{Q, \overline{Q}}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF

Typical Q and $\overline{Q}$ Pulse Width Accuracy vs Temperature Monostable Mode Operation

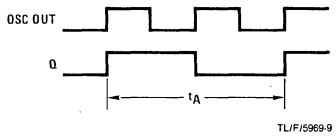


TL/F/5969-8

	t_M	R	C
A	2 μs	22k	10 pF
B	7 μs	22k	100 pF
C	60 μs	220k	100 pF
D	550 μs	220k	1000 pF

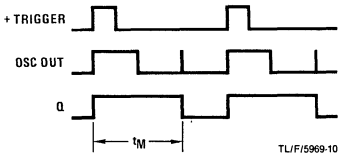
Timing Diagram

Astable Mode



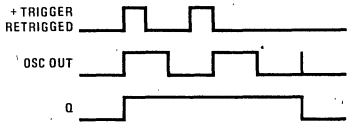
TL/F/5969-9

Monostable Mode



TL/F/5969-10

Retrigger Mode



TL/F/5969-11

National Semiconductor

CD4048BM/CD4048BC TRI-STATE® Expandable 8-Function 8-Input Gate

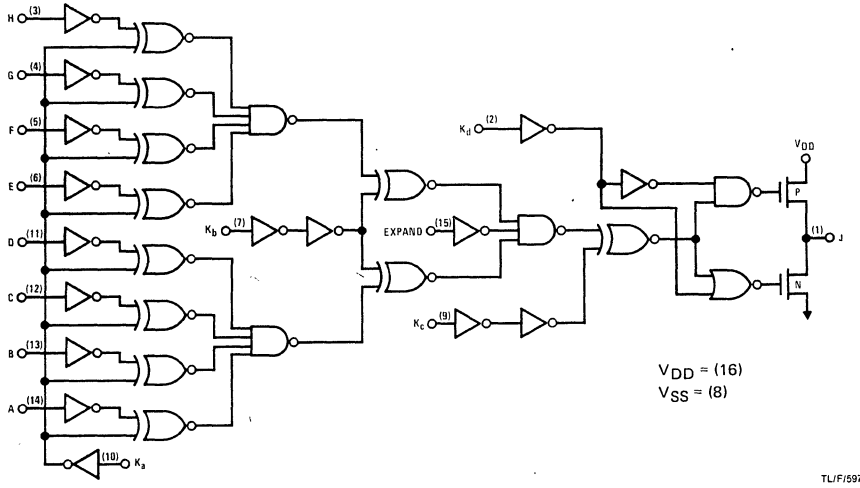
General Description

The CD4048BM/CD4048BC is a progammable 8-input gate. Three binary control lines K_a, K_b, and K_c determine the 8 different logic functions of the gate. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR. A fourth input, K_d, is a TRI-STATE control. When K_d is high, the output is enabled; when K_d is low, the output is a high impedance. This feature enables the user to connect the device to a common bus line. The Expand input permits the user to increase the number of gate inputs. For example, two 8-input CD4048's can be cascaded into a 16-input multifunction gate. When the Expand input is not used, it should be connected to V_{SS}. All inputs are buffered and protected against electrostatic effects.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- High sink and source current capability
- TTL compatibility — drives 1 standard TTL load at V_{CC} = 5V, over full temperature range
- Many logic functions in one package

Logic Diagram

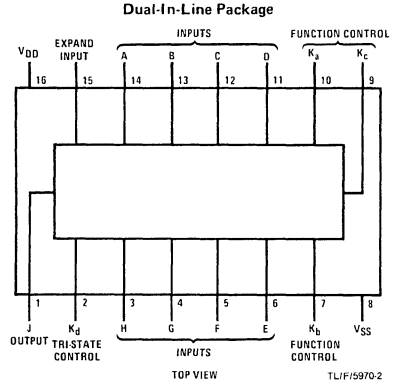


V_{DD} = (16)
V_{SS} = (8)

TL/F/5970-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5970-2

Order Number CD4048BMJ or CD4048BCJ
See NS Package J16A

Order Number CD4048BMN or CD4048BCN
See NS Package N16E

5

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4048BM	−55°C to +125°C
CD4048BC	−40°C to +85°C

DC Electrical Characteristics CD4048BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.01	5.0		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V, V_O = 0.4V	2.8		2.3	4.0		1.6		mA
		V_{DD} = 10V, V_O = 0.5V	6.4		5.2	11		3.6		mA
		V_{DD} = 15V, V_O = 1.5V	14		11.5	23		8.0		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V, V_O = 4.6V	−2.8		−2.3	−4.0		−1.6		mA
		V_{DD} = 10V, V_O = 9.5V	−6.4		−5.2	−11		−3.6		mA
		V_{DD} = 15V, V_O = 13.5V	−14		−11.5	−23		−8.0		mA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15V, V_O = 0V		−0.2		−0.002	−0.2		−2	μA
		V_{DD} = 15V, V_O = 15V		0.2		0.002	0.2		2	μA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4048BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

DC Electrical Characteristics (Cont'd.) CD4048BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	(Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	2.3		2.0	4.0		1.6		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	5.2		4.5	11		3.6		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	11.5		9.8	23		8.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	(Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−2.3		−2.0	−4.0		−1.6		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−5.2		−4.5	−11		−3.6		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−11.5		−9.8	−23		−8.0		mA
I_{TL}	TRI-STATE Leakage	$V_{DD} = 15V$, $V_O = 0V$		−0.6		−0.005	−0.6		−2	μA
	Current	$V_{DD} = 15V$, $V_O = 15V$		0.6		0.005	0.6		2	μA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, and $t_r = t_f = 20\,ns$, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		425	850	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{PLZ}, t_{PHZ}	Propagation Delay Time, K_d to	$R_L = 1.0k\Omega$				
	High Impedance (From Active	$V_{DD} = 5V$		175	350	ns
	Low or High Level)	$V_{DD} = 10V$		125	250	ns
		$V_{DD} = 15V$		100	200	ns
t_{PZL}, t_{PZH}	Propagation Delay Time, K_d to	$R_L = 1.0k\Omega$				
	Active High or Low Level	$V_{DD} = 5V$		225	450	ns
	(From High Impedance)	$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		70	140	ns
t_{THL}, t_{TLH}	Output Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance				22.5	pF

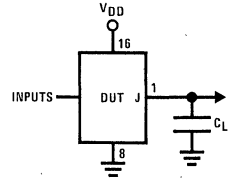
Truth Table

OUTPUT FUNCTION	BOOLEAN EXPRESSION	CONTROL INPUTS K_a	K_b	K_c	K_d	UNUSED INPUTS
NOR	$J = \overline{A + B + C + D + E + F + G + H}$	0	0	0	1	V_{SS}
OR	$J = A + B + C + D + E + F + G + H$	0	0	1	1	V_{SS}
OR/AND	$J = (A + B + C + D) \cdot (E + F + G + H)$	0	1	0	1	V_{SS}
OR/NAND	$J = \overline{(A + B + C + D) \cdot (E + F + G + H)}$	0	1	1	1	V_{SS}
AND	$J = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$	1	0	0	1	V_{DD}
NAND	$J = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$	1	0	1	1	V_{DD}
AND/NOR	$J = \overline{(A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)}$	1	1	0	1	V_{DD}
AND/OR	$J = (A \cdot B \cdot C \cdot D) + (E \cdot F \cdot G \cdot H)$	1	1	1	1	V_{DD}
Hi-Z		X	X	X	0	X

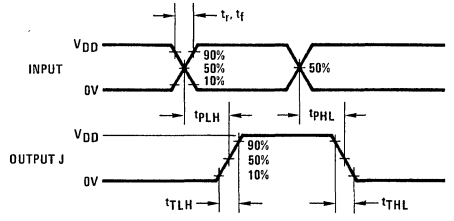
Positive logic: 0 = low level, 1 = high level, X = irrelevant, EXPAND input tied to V_{SS}.

AC Test Circuits and Switching Time Waveforms

Logic Propagation Delay Time Tests

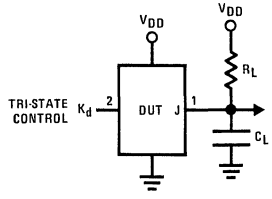


TL/F/5970-3

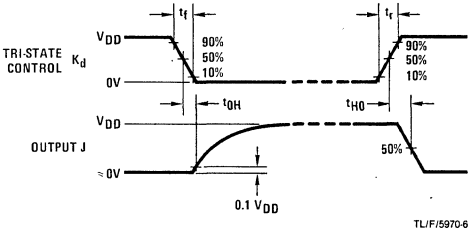


TL/F/5970-4

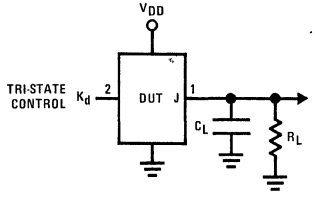
TRI-STATE Propagation Delay Time Tests



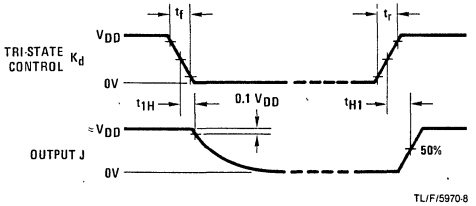
TL/F/5970-5



TL/F/5970-6



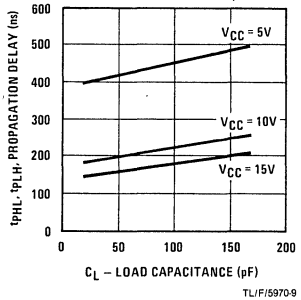
TL/F/5970-7



TL/F/5970-8

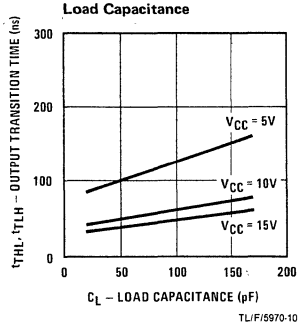
Typical Performance Characteristics

Propagation Delay vs Load Capactiance



TL/F/5970-9

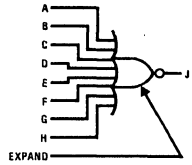
Output Transition Time vs Load Capacitance



TL/F/5970-10

Basic Logic Configurations

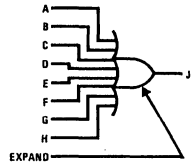
NOR



$K_aK_bK_c = 000$

TL/F/5970-11

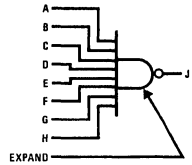
OR



= 001

TL/F/5970-12

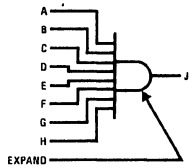
NAND



= 101

TL/F/5970-13

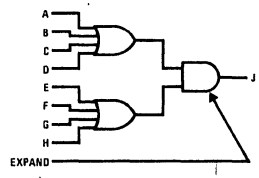
AND



= 100

TL/F/5970-14

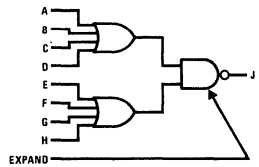
OR/AND



= 010

TL/F/5970-15

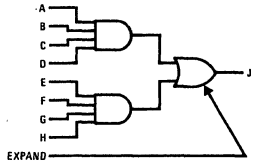
OR/NAND



= 011

TL/F/5970-16

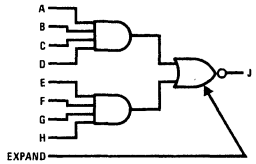
AND/OR



= 111

TL/F/5970-17

AND/NOR

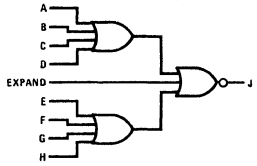


= 110

TL/F/5970-18

Actual Circuit Configurations

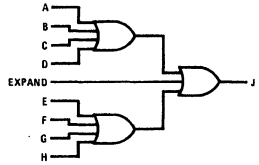
NOR



$K_aK_bK_c = 000$

TL/F/5970-19

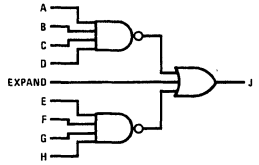
OR



= 001

TL/F/5970-20

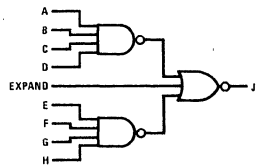
NAND



= 101

TL/F/5970-21

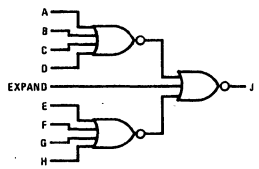
AND



= 100

TL/F/5970-22

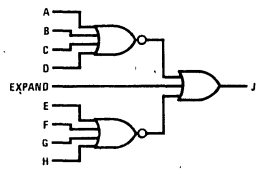
OR/AND



= 010

TL/F/5970-23

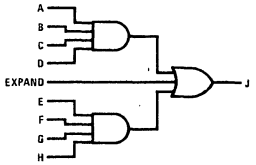
OR/NAND



= 011

TL/F/5970-24

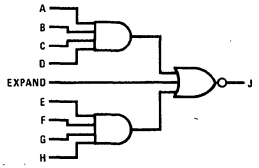
AND/OR



= 111

TL/F/5970-25

AND/NOR



= 110

TL/F/5970-26

5

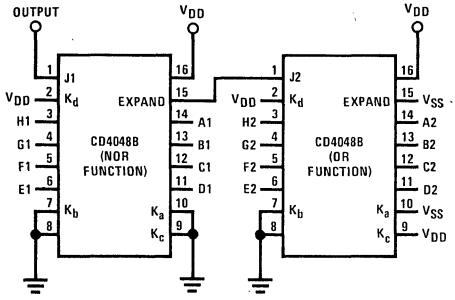
Truth Table for EXPAND Feature

COMBINED OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J = \overline{(A + B + C + D + E + F + G + H) + (EXP)}$
OR	OR	$J = (A + B + C + D + E + F + G + H) + (EXP)$
AND	NAND	$J = \overline{(ABCDEFGH) \cdot (EXP)}$
NAND	NAND	$J = \overline{(ABCDEFGH) \cdot (EXP)}$
OR/AND	NOR	$J = \overline{(A + B + C + D) \cdot (E + F + G + H) \cdot (EXP)}$
OR/NAND	NOR	$J = \overline{(A + B + C + D) \cdot (E + F + G + H) \cdot (EXP)}$
AND/NOR	AND	$J = \overline{(ABCD) + (EFGH) + (EXP)}$
AND/OR	AND	$J = (ABCD) + (EFGH) + (EXP)$

Note. Positive logic is assumed. (EXP) represents the logic level present at the EXPAND input.

Typical Applications of EXPAND Feature

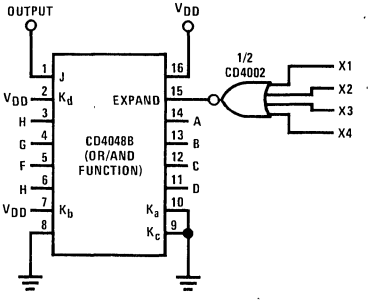
16-Input NOR Gate



$$\text{Output} = \overline{A1 + B1 + C1 + D1 + E1 + F1 + G1 + H1 + A2 + B2 + C2 + D2 + E2 + F2 + G2 + H2}$$

TL/F/5970-27

12-Input OR/AND Gate



Output = (A + B + C + D) • (E + G + H) • (X1 + X2 + X3 + X4) F +

TL/F/5970-28

National Semiconductor

CD4049UBM/CD4049UBC Hex Inverting Buffer
CD4050BM/CD4050BC Hex Non-Inverting Buffer

General Description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at $V_{DD} = 5.0\,V$, they can drive directly two DTL/TTL loads over the full operating temperature range.

Features

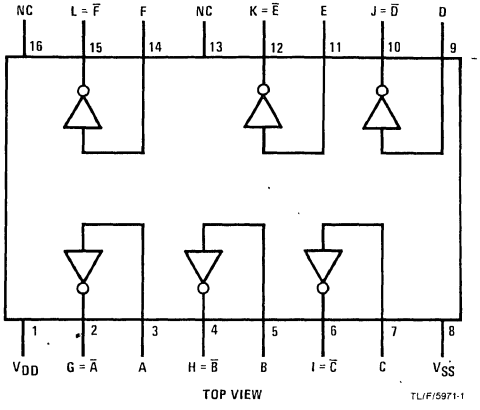
- Wide supply voltage range 3.0 V to 15 V
- Direct drive to 2 TTL loads at 5.0 V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

Applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic level converter

Connection Diagrams

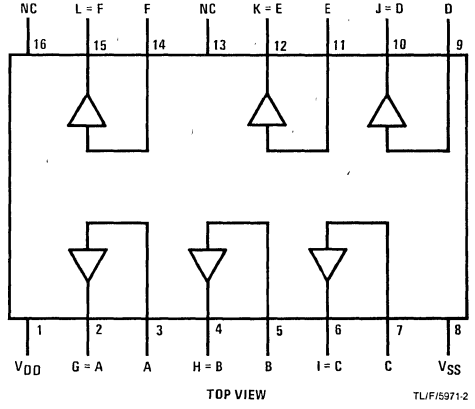
CD4049UBM/CD4049UBC
Dual-In-Line Package



TOP VIEW TL/F/5971-1

Order Number CD4049UBMJ, CD4049UBCJ, CD4050BMJ or CD4050BCJ
See NS Package J16A

CD4050BM/CD4050BC
Dual-In-Line Package

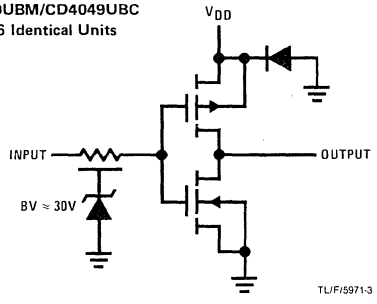


TOP VIEW TL/F/5971-2

Order Number CD4049UBMN, CD4049UBCN, CD4050BMN or CD4050BCN
See NS Package N16E

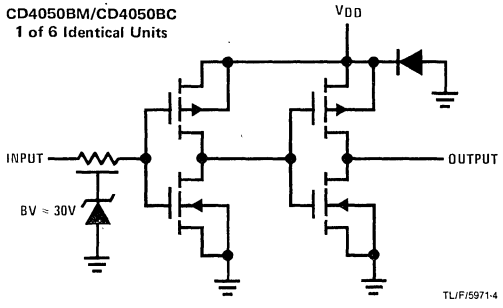
Schematic Diagrams

CD4049UBM/CD4049UBC
1 of 6 Identical Units



TL/F/5971-3

CD4050BM/CD4050BC
1 of 6 Identical Units



TL/F/5971-4

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to +18V
V_{OUT} Voltage at Any Output Pin	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to 15V
V_{OUT} Voltage at Any Output Pin	0 to V_{DD}
T_A Operating Temperature Range	
CD4049M, CD4050BM	−55°C to +125°C
CD4049C, CD4050BC	−40°C to +85°C

DC Electrical Characteristics CD4049M/CD4050BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		30	μA
		V_{DD} = 10V		2.0		0.01	2.0		60	μA
		V_{DD} = 15V		4.0		0.03	4.0		120	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0, $\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0, $\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage (CD4050BM Only)	$\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL}	Low Level Input Voltage (CD4049UBM Only)	$\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH}	High Level Input Voltage (CD4050BM Only)	$\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH}	High Level Input Voltage (CD4049UBM Only)	$\lvert I_O \rvert$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	5.6		4.6	5		3.2		mA
		V_{DD} = 10V, V_O = 0.5V	12		9.8	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	35		29	40		20		mA
I_{OH}	High Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−1.3		−1.1	−1.6		−0.72		mA
		V_{DD} = 10V, V_O = 9.5V	−2.6		−2.2	−3.6		−1.5		mA
		V_{DD} = 15V, V_O = 13.5V	−8.0		−7.2	−12		−5.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time. I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics CD4049C/CD4050BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.03	4.0		30	μA
		V_{DD} = 10V		8		0.05	8.0		60	μA
		V_{DD} = 15V		16		0.07	16.0		120	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage (CD4050BC Only)	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL}	Low Level Input Voltage (CD4049UBC Only)	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH}	High Level Input Voltage (CD4050BC Only)	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH}	High Level Input Voltage (CD4049UBC Only)	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	4.6		4.0	5		3.2		mA
		V_{DD} = 10V, V_O = 0.5V	9.8		8.5	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	29		25	40		20		mA
I_{OH}	High Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−1.0		−0.9	−1.6		−0.72		mA
		V_{DD} = 10V, V_O = 9.5V	−2.1		−1.9	−3.6		−1.5		mA
		V_{DD} = 15V, V_O = 13.5V	−7.1		−6.2	−12		−5		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V	−0.3		−0.3	-10^{-5}			−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V	0.3		0.3	10^{-5}			1.0	μA

5

AC Electrical Characteristics CD4049UBM/CD4049UBC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified.

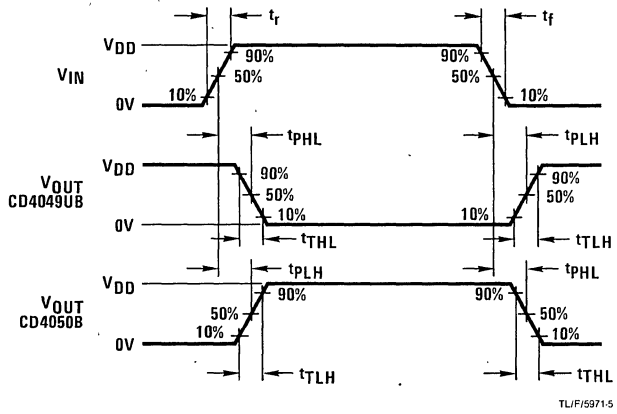
SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time High-to-Low Level	$V_{DD} = 5V$		30	65	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{PLH}	Propagation Delay Time Low-to-High Level	$V_{DD} = 5V$		45	85	ns
		$V_{DD} = 10V$		25	45	ns
		$V_{DD} = 15V$		20	35	ns
t_{THL}	Transition Time High-to-Low Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		15	22.5	pF

AC Electrical Characteristics CD4050BM/CD4050BC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified.

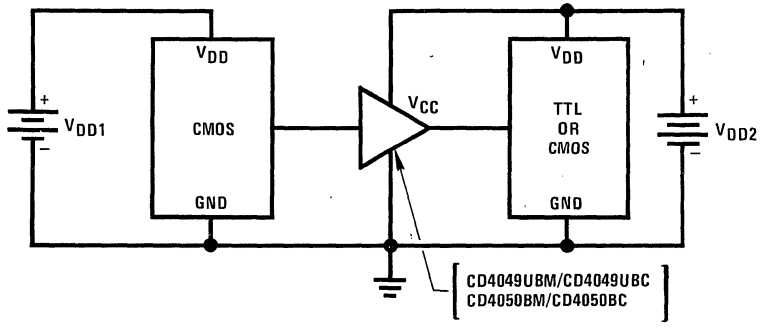
SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time High-to-Low Level	$V_{DD} = 5V$		60	110	ns
		$V_{DD} = 10V$		25	55	ns
		$V_{DD} = 15V$		20	30	ns
t_{PLH}	Propagation Delay Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
t_{THL}	Transition Time High-to-Low Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Switching Time Waveforms



Typical Applications

CMOS to TTL or CMOS at a Lower V_{DD}



Note: $V_{DD1} \geq V_{DD2}$

Note: In the case of the CD4049M/CD4049C the output drive capability increases with increasing input voltage. E.g., If V_{DD1}= 10V the CD4049M/CD4049C could drive 4 TTL loads.

National Semiconductor

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD}=5V$, $V_{SS}=0V$ and $V_{EE}=-5V$, analog signals from $-5V$ to $+5V$ can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs. A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

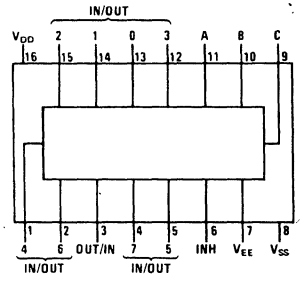
Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to $15V_{p-p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD}-V_{EE}=15V$
- High "OFF" resistance: channel leakage of ± 10 pA (typ.) at $V_{DD}-V_{EE}=10V$
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD}-V_{SS}=3-15V$) to switch analog signals to 15 V_{p-p} ($V_{DD}-V_{EE}=15V$)
- Matched switch characteristics: $\Delta R_{ON}=5\Omega$ (typ.) for $V_{DD}-V_{EE}=15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at $V_{DD}-V_{SS}=V_{DD}-V_{EE}=10V$
- Binary address decoding on chip

Connection Diagrams

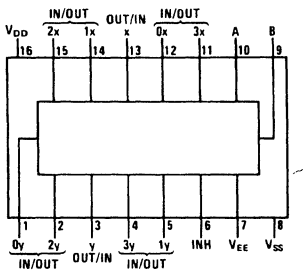
Dual-In-Line Packages

CD4051BM/CD4051BC



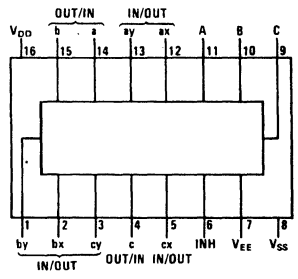
TOP VIEW

CD4052BM/CD4052BC



TOP VIEW

CD4053BM/CD4053BC



TOP VIEW TL/F/5662–1

Order Number CD4051BMJ, CD4051BCJ, CD4052BMJ, CD4052BCJ, CD4053BMJ, or CD4053BCJ
See NS Package J16A

Order Number CD4051BMN, CD4051BCN, CD4052BMN, CD4052BCN, CD4053BMN, or CD4053BCN
See NS Package N16E

Absolute Maximum Ratings

V_{DD}	DC Supply Voltage	−0.5 Vdc to +18 Vdc
V_{IN}	Input Voltage	−0.5 Vdc to V_{DD} +0.5 Vdc
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	260°C

Recommended Operating Conditions

V_{DD}	DC Supply Voltage	+5 Vdc to +15 Vdc
V_{IN}	Input Voltage	0V to V_{DD} Vdc
T_A	Operating Temperature Range	
	4051BM/4052BM/4053BM	−55°C to +125°C
	4051BC/4052BC/4053BC	−40°C to +85°C

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		−55°C		+25°			+125°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$			5			5		150	μA
		$V_{DD}=10V$			10			10		300	μA
		$V_{DD}=15V$			20			20		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \le V_{IS} \le V_{DD}$)	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$		800		270	1050		1300	Ω
			$V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$		310		120	400		550	Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$		200		80	240		320	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD}=7.5V$, $V_{EE}=-7.5V$ $O/I=\pm7.5V$, $I/O=0V$			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit=7.5V $V_{DD}=7.5V$, $V_{EE}=-7.5V$, $O/I=0V$, $I/O=\pm7.5V$	CD4051		±200		±0.08	±200		±2000	nA
			CD4052		±200		±0.04	±200		±2000	nA
			CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to V_{SS} $I_{IS}<2\ \mu A$ on all OFF channels $V_{IS}=V_{DD}$ thru 1 kΩ									
		$V_{DD}=5V$			1.5			1.5		1.5	V
		$V_{DD}=10V$			3.0			3.0		3.0	V
		$V_{DD}=15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5$		3.5		3.5			3.5		V
		$V_{DD}=10$		7		7			7		V
		$V_{DD}=15$		11		11			11		V
I_{IN}	Input Current	$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=0V$			−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=15V$			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range", they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics (Note 2) (Continued)

Symbol	Parameter	Conditions		−40°C		+25°C			+85°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$			20			20		150	μA
		$V_{DD}=10V$			40			40		300	μA
		$V_{DD}=15V$			80			80		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE}\leq V_{IS}\leq V_{DD}$)	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$		850		270	1050		1200	Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$		330		120	400		520	Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$		210		80	240		300	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD}=7.5V$, $V_{EE}=-7.5V$ $O/I=\pm7.5V$, $I/O=0V$			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V $V_{DD}=7.5V$, $V_{EE}=-7.5V$, $O/I=0V$	CD4051		±200		±0.08	±200		±2000	nA
			CD4052		±200		±0.04	±200		±2000	nA
		$I/O=\pm7.5V$	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to V_{SS} $I_{IS}<2\ \mu A$ on all OFF Channels $V_{IS}=V_{DD}$ thru 1 kΩ									
		$V_{DD}=5V$			1.5			1.5		1.5	V
		$V_{DD}=10V$			3.0			3.0		3.0	V
		$V_{DD}=15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5$		3.5		3.5			3.5		V
		$V_{DD}=10$		7		7			7		V
		$V_{DD}=15$		11		11			11		V
I_{IN}	Input Current	$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=0V$			−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=15V$			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

AC Electrical Characteristics

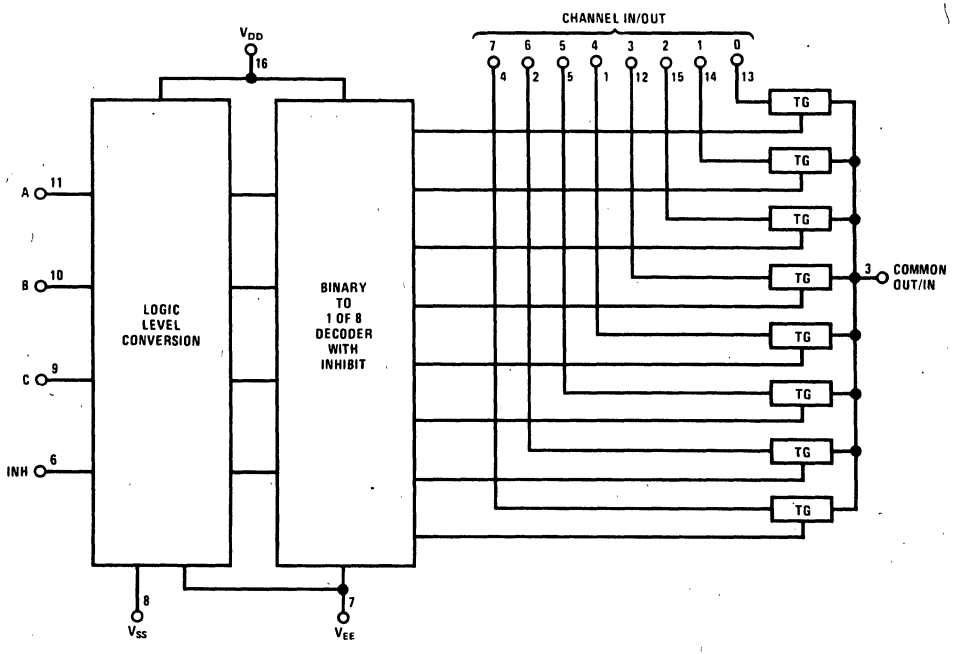
$T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

Symbol	Parameter	Conditions	V_{pp}	Min	Typ	Max	Units
t_{PZH}	Propagation Delay Time from	$V_{EE} = V_{SS} = 0V$	5V		600	1200	ns
t_{PZL}	Inhibit to Signal Output (channel turning on)	$R_L = 1\ k\Omega$, $C_L = 50$ pF	10V 15V		225 160	450 320	ns ns
t_{PHZ}	Propagation Delay Time from	$V_{EE} = V_{SS} = 0V$	5V		210	420	ns
t_{PLZ}	Inhibit to Signal Output (channel turning off)	$R_L = 1\ k\Omega$, $C_L = 50$ pF	10V 15V		100 75	200 150	ns ns
C_{IN}	Input Capacitance Control input Signal Input (IN/OUT)				 5 10	 7.5 15	 pF pF
C_{OUT}	Output Capacitance (common OUT/IN)						
	CD4051 CD4052 CD4053	$V_{EE} = V_{SS} = 0V$	10V 10V 10V		30 15 8		pF pF pF
C_{IOS}	Feedthrough Capacitance				0.2		pF
C_{PD}	Power Dissipation Capacitance						
	CD4051 CD4052 CD4053				110 140 70		pF pF pF
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response (Distortion)	$R_L = 10\ k\Omega$ $f_{IS} = 1$ kHz $V_{IS} = 5\ V_{p-p}$ $V_{EE} = V_{SI} = 0V$	10V		0.04		%
	Frequency Response, Channel "ON" (Sine Wave Input)	$R_L = 1\ k\Omega$, $V_{EE} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -3$ dB	10V		40		MHz
	Feedthrough, Channel "OFF"	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -40$ dB	10V		10		MHz
	Crosstalk Between Any Two Channels (frequency at 40 dB)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$ $20 \log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3)	10V		3		MHz
t_{PHL} t_{PLH}	Propagation Delay Signal Input to Signal Output	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		25 15 10	55 35 25	ns ns ns
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal Crosstalk	$V_{EE} = V_{SS} = 0V$, $R_L = 10\ k\Omega$ at both ends of channel. Input Square Wave Amplitude = 10V	10V		65		mV (peak)
t_{PHL}, t_{PLH}	Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF")	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		500 180 120	1000 360 240	ns ns ns

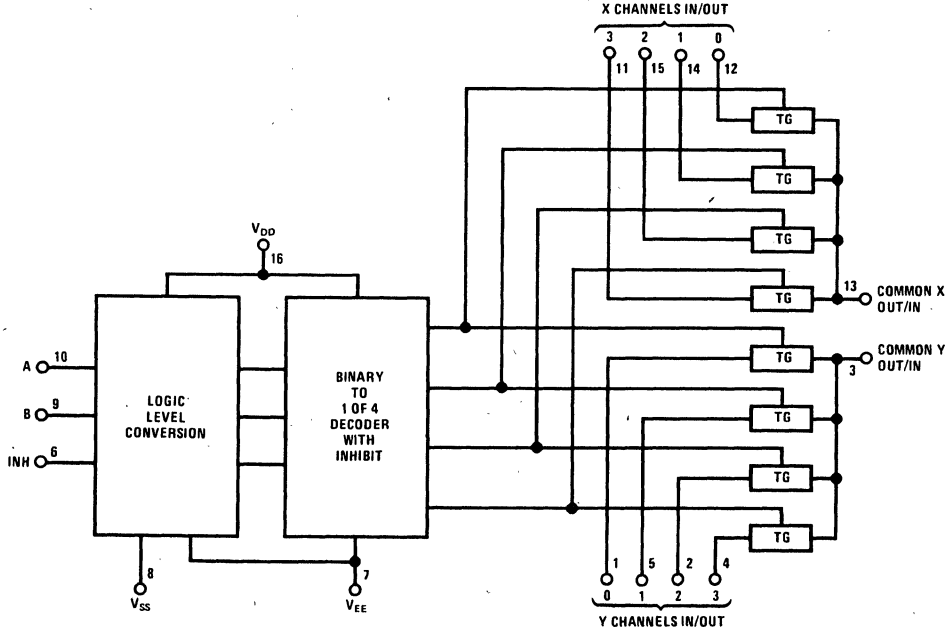
Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF".

Block Diagrams

CD4051BM/CD4051BC



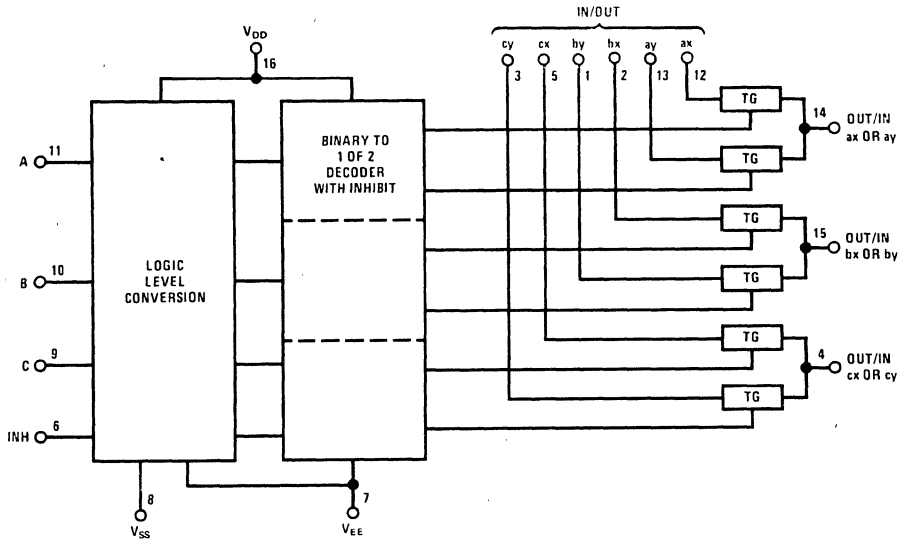
CD4052BM/CD4052BC



TL/F/5662–2

Block Diagrams (Continued)

CD4053BM/CD4053BC



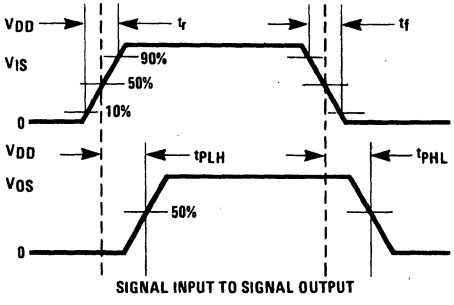
TL/F/5662–3

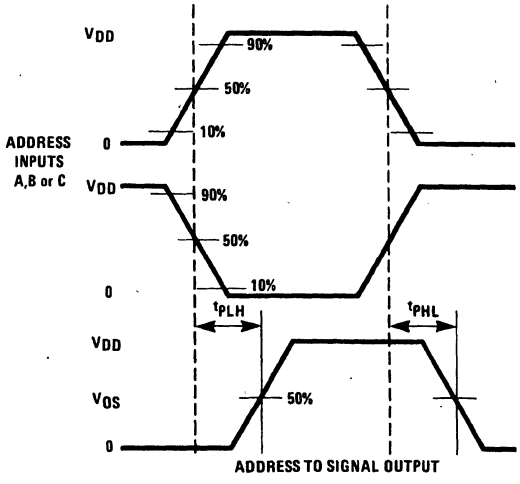
Truth Table

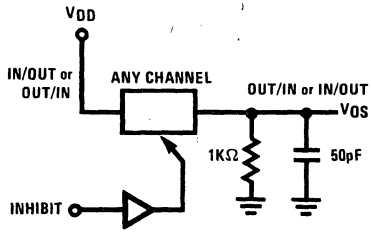
INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

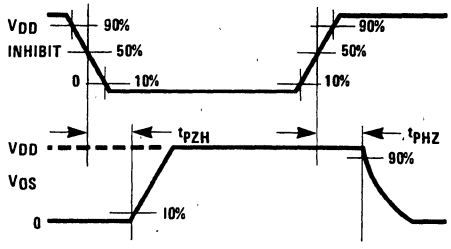
*Don't Care condition.

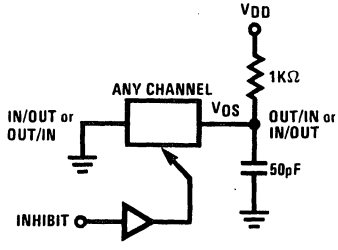
Switching Time Waveforms

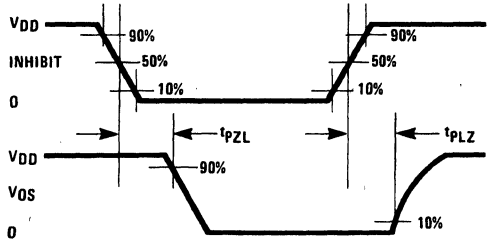












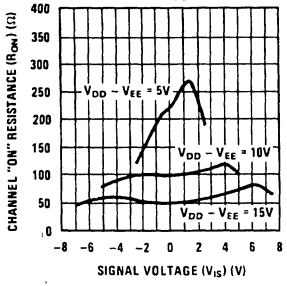
TL/F/5662–4

Special Considerations

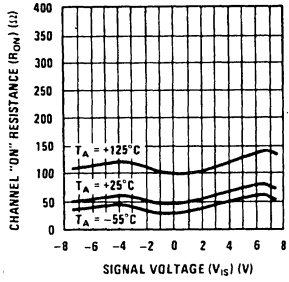
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

Typical Performance Characteristics

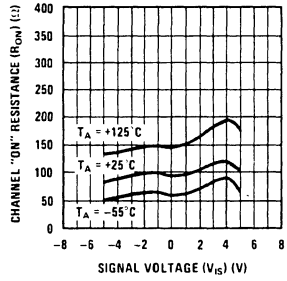
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



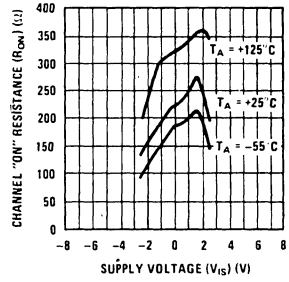
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



TL/F/5662–5

National Semiconductor

CD4066BM/CD4066BC Quad Bilateral Switch

General Description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

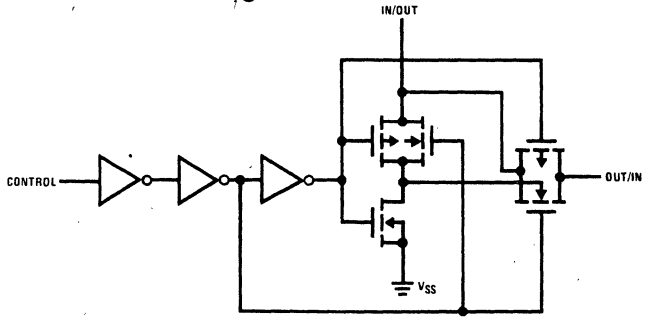
Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Wide range of digital and analog switching — ±7.5 V_{PEAK}
- "ON" resistance for 15V operation — 80Ω
- Matched "ON" resistance over 15V signal input — ΔR_{ON} = 5Ω (typ.)
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB (typ.) @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree linearity — 0.1% distortion (typ.) @ f_{is} = 1 kHz, V_{is} = $5V_{p-p}$, $V_{DD}-V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage — 0.1 nA (typ.) @ $V_{DD}-V_{SS}$ = 10V, T_A = 25°C
- Extremely high control input impedance — 10^{12}Ω (typ.)
- Low crosstalk between switches — −50 dB (typ.) @ f_{is} = 0.9 MHz, R_L = 1kΩ
- Frequency response, switch "ON" — 40 MHz (typ.)

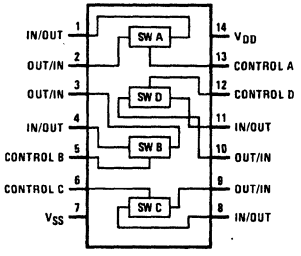
Applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal-gain

Schematic and Connection Diagrams



Dual-In-Line Package



Top View

Order Number CD4066BMJ or CD4066BCJ
NS Package Number J14A

Order Number CD4066BMN or CD4066BCN
NS Package Number N14A

TL/F/5665–1

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions (Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

DC Electrical Characteristics CD4066BM (Note 2)

Symbol	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		0.25		0.01	0.25		7.5	μA
		$V_{DD}=10V$		0.5		0.01	0.5		15	μA
		$V_{DD}=15V$		1.0		0.01	1.0		30	μA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=5V$		2000		270	2500		3500	Ω
		$V_{DD}=10V$		400		120	500		550	Ω
		$V_{DD}=15V$		220		80	280		320	Ω
ΔR_{ON}	Δ"ON" Resistance Between any 2 of 4 Switches	$R_L=10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C=V_{DD}$, $V_{IS}=V_{SS}$ to V_{DD}								
		$V_{DD}=10V$				10				Ω
		$V_{DD}=15V$				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C=0$ $V_{IS}=15V$ and 0V, $V_{OS}=0V$ and 15V		±50		±0.1	±50		±500	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS}=V_{SS}$ and V_{DD} $V_{OS}=V_{DD}$ and V_{SS} $I_{IS}=\pm 10\mu A$								
		$V_{DD}=5V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V$		3.0		4.5	3.0		3.0	V
		$V_{DD}=15V$		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	$V_{DD}=5V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10V$ (see note 6)	7.0		7.0	5.5		7.0		V
		$V_{DD}=15V$	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD}-V_{SS}=15V$ $V_{DD}\geq V_{IS}\geq V_{SS}$ $V_{DD}\geq V_C\geq V_{SS}$		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA

DC Electrical Characteristics CD4066BC (Note 2)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$		1.0		0.01	1.0		7.5	μA
		$V_{DD}=10V$		2.0		0.01	2.0		15	μA
		$V_{DD}=15V$		4.0		0.01	4.0		30	μA

DC Electrical Characteristics (Continued) CD4066BC (Note 2)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	$R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_C = V_{DD}$, V_{SS} to V_{DD}								
		$V_{DD} = 5V$		2000		270	2500		3200	Ω
		$V_{DD} = 10V$		450		120	500		520	Ω
		$V_{DD} = 15V$		250		80	280		300	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any 2 of 4 Switches	$R_L = 10\ k\Omega$ to $\frac{V_{DD}-V_{SS}}{2}$ $V_{CC} = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
		$V_{DD} = 10V$				10				Ω
		$V_{DD} = 15V$				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	$V_C = 0$		±50		±0.1	±50		±200	nA
Control Inputs										
V_{ILC}	Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD} $V_{OS} = V_{DD}$ and V_{SS} $I_{IS} = \pm 10\mu A$								
		$V_{DD} = 5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	$V_{DD} = 5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$ (See note 6)	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	$V_{DD} - V_{SS} = 15V$ $V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$, $C_L = 50$ pF, (*Figure 1*) $R_L = 200k$				
		$V_{DD} = 5V$		25	55	ns
		$V_{DD} = 10V$		15	35	ns
		$V_{DD} = 15V$		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, (*Figures 2* and *3*)				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, (*Figures 2* and *3*)				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
	Sine Wave Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$ $R_L = 10\ k\Omega$, $V_{IS} = 5V_{p-p}$, $f = 1$ kHz, (*Figure 4*)		0.1		%
	Frequency Response-Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5V_{p-p}$, 20 $\text{Log}_{10}\ V_{OS}/V_{OS}$ (1 kHz) − dB, (*Figure 4*)		40		MHz

AC Electrical Characteristics (Continued) $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
	Feedthrough — Switch "OFF" (Frequency at −50 dB)	$V_{DD} = 5.0V$, $V_{CC} = V_{SS} = -5.0V$, $R_L = 1\ k\Omega$, $V_{IS} = 5.0V_{p-p}$, 20 Log_{10}, $V_{OS}/V_{IS} = -50$ dB, (*Figure 4*)		1.25		
	Crosstalk Between Any Two Switches (Frequency at −50 dB)	$V_{DD} = V_{C(A)} = 5.0V$; $V_{SS} = V_{C(B)} = 5.0V$, R_L 1 kΩ, $V_{IS(A)} = 5.0\ V_{p-p}$, 20 Log_{10}, $V_{OS(B)}/V_{IS(A)} = -50$ dB (*Figure 5*)		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$, $R_{IN} = 1.0\ k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$ pF (*Figure 6*)		150		mV_{p-p}
	Maximum Control Input	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, (*Figure 7*) $V_{OS(f)} = \frac{1}{2}\ V_{OS}$(1.0 kHz)				
		$V_{DD} = 5.0V$		6.0		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		8.5		MHz
C_{IS}	Signal Input Capacitance			8.0		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		8.0		pF
C_{IOS}	Feedthrough Capacitance	$V_C = 0V$		0.5		pF
C_{IN}	Control Input Capacitance			5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

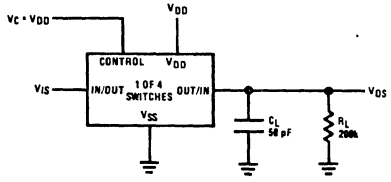
Note 4: In all cases, there is approximately 5pF of probe and jig capacitance in the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: Conditions for V_{IHC}:

a) $V_{IS} = V_{DD}$, I_{OS} = standard B series I_{OH} b) $V_{IS} = 0V$, I_{OL} = standard B series I_{OL}.

AC Test Circuits and Switching Time Waveforms



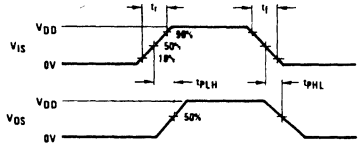
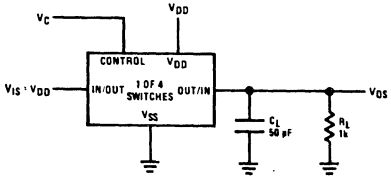


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output



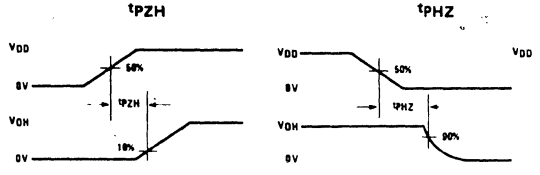
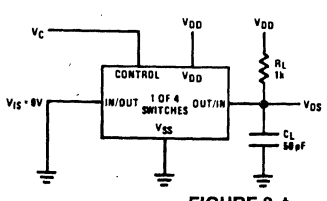
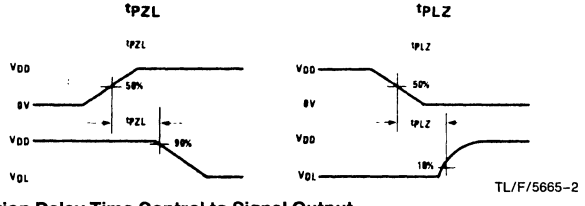


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output





TL/F/5665–2

FIGURE 3. t_{PZL}, t_{PLZ} Propagtion Delay Time Control to Signal Output

AC Test Circuits and Switching Time Waveforms (Continued)

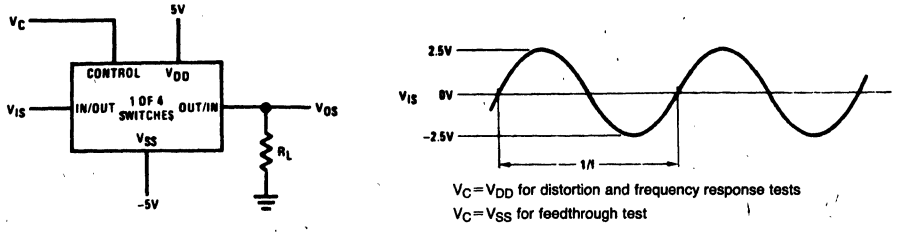


FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

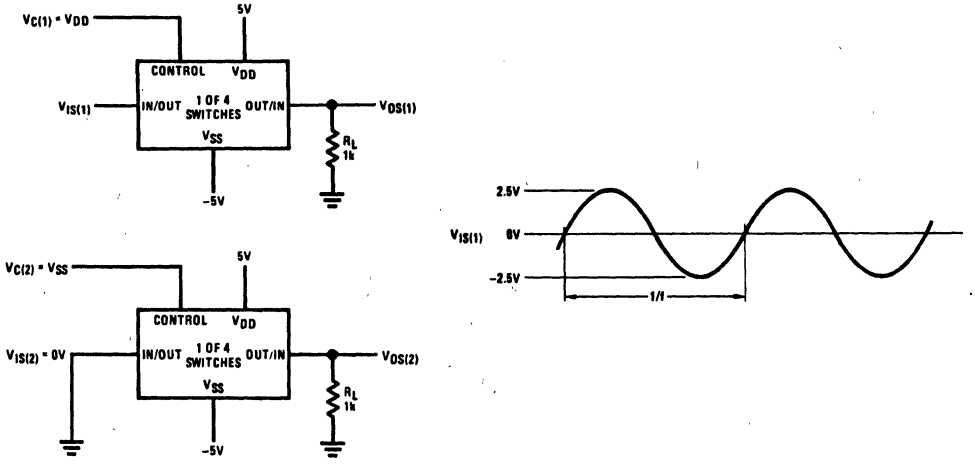


FIGURE 5. Crosstalk Between Any Two Switches

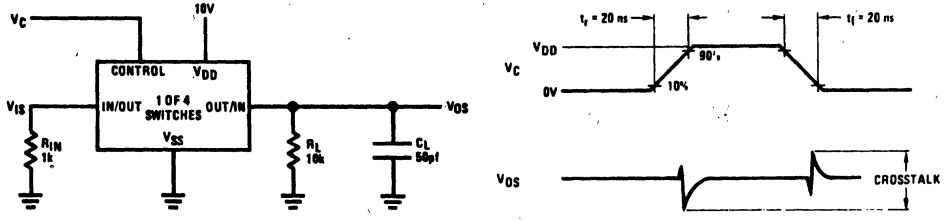
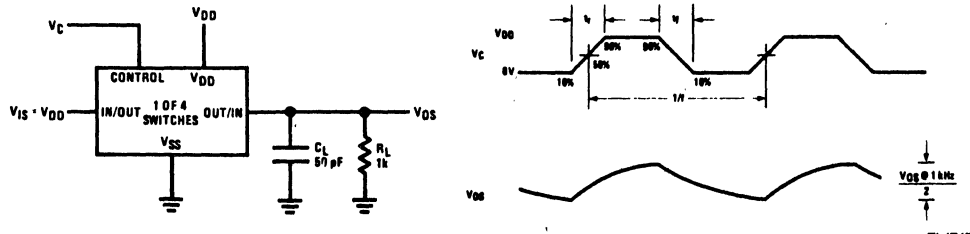


FIGURE 6. Crosstalk: Control Input to Signal Output

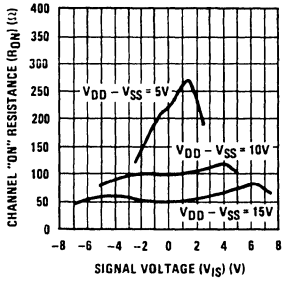


TL/F/5665–3

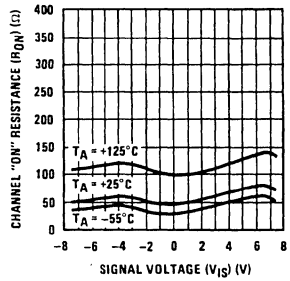
FIGURE 7. Maximum Control Input Frequency

Typical Performance Characteristics

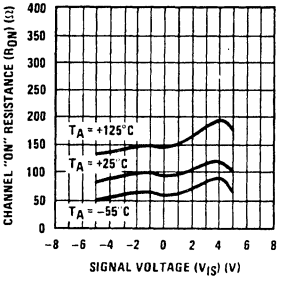
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



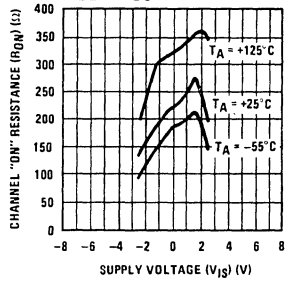
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$



TL/F/5665–4

Special Considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action of the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

5

National Semiconductor

CD4069UBM/CD4069UBC Inverter Circuits

General Description

The CD4069UB consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity, and symmetric controlled rise and fall times.

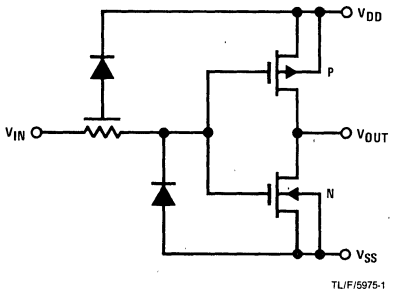
This device is intended for all general purpose inverter applications where the special characteristics of the MM74C901, MM74C903, MM74C907, and CD4049A Hex Inverter/Buffers are not required. In those applications requiring larger noise immunity the MM74C14 or MM74C914 Hex Schmitt Trigger is suggested.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

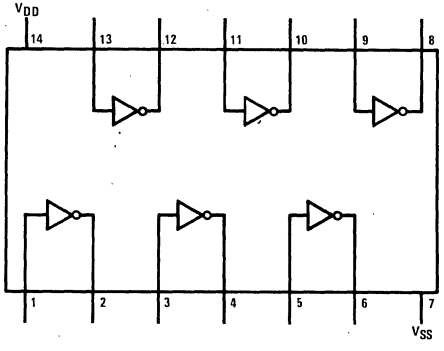
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} typ.
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Equivalent to MM54C04/MM74C04

Schematic and Connection Diagrams



TL/F/5975-1

Dual-In-Line Package



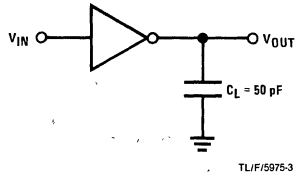
TOP VIEW

TL/F/5975-2

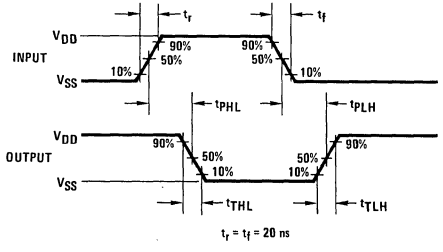
Order Number CD4069UBMJ or CD4069UBCJ
See NS Package J14A

Order Number CD4069UBMN or CD4069UBCN
See NS Package N14A

AC Test Circuits and Switching Time Waveforms



TL/F/5975-3



$t_r = t_f = 20$ ns

TL/F/5975-4

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4069M	−55°C to +125°C
CD4069C	−40°C to +85°C

DC Electrical Characteristics CD4069M (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25			0.25		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.5			0.5		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.0			1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0			2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0			3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0			4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0			8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0			12.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

5

DC Electrical Characteristics CD4069C (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.0			1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0			2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0			3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0			4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0			8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0			12.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, t_r and $t_f \leq$ 20 ns, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	V_{DD} = 5V		50	90	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		80	150	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Gate		6	15	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 4)		12		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

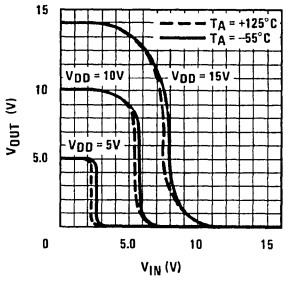
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

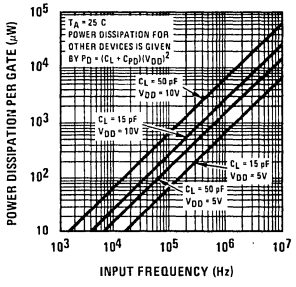
Typical Performance Characteristics

Gate Transfer Characteristics



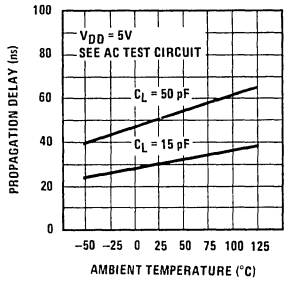
TL/F/5975-5

Power Dissipation vs Frequency



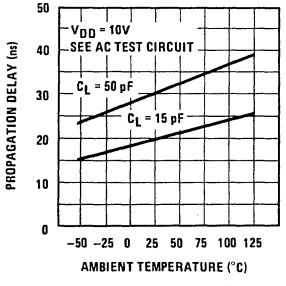
TL/F/5975-6

Propagation Delay vs Ambient Temperature



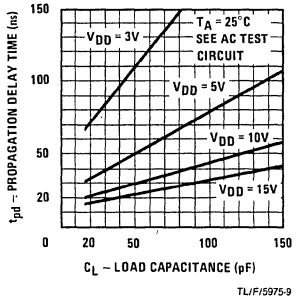
TL/F/5975-7

Propagation Delay vs Ambient Temperature



TL/F/5975-8

Propagation Delay Time vs Load Capacitance



TL/F/5975-9

5

National Semiconductor

CD4070BM/CD4070BC Quad 2-Input EXCLUSIVE-OR Gate

General Description

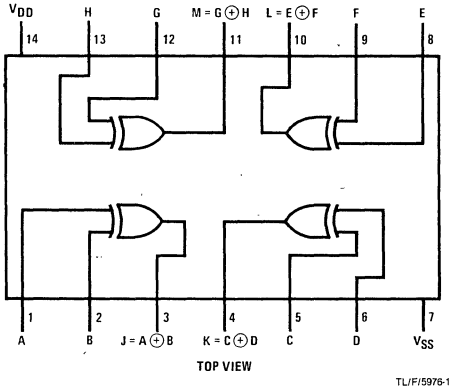
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption, and high noise margin, this gate provides basic functions used in the implementation of digital integrated circuit systems. The N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No DC power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} typ.
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Pin compatible to CD4030A
- Equivalent to MM54C86/MM74C86 and MC14507B

Connection Diagram

Dual-In-Line Package



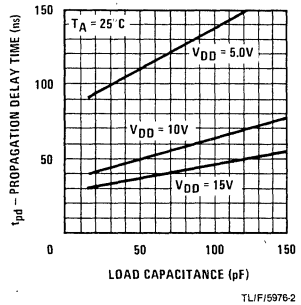
TL/F/5976-1

Order Number CD4070BMJ or CD4070BCJ
See NS Package J14A

Order Number CD4070BMN or CD4070BCN
See NS Package N14A

Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance



TL/F/5976-2

Truth Table

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4070BC	−40°C to +85°C
CD4070BM	−55°C to +125°C

DC Electrical Characteristics CD4070BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		0.25			0.25		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		0.5			0.5		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4070BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and $t_f \leq$ 20 ns, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	V_{DD} = 5V		110	185	ns
		V_{DD} = 10V		50	90	ns
		V_{DD} = 15V		40	75	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Input (Note 4)		20		pF

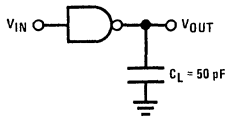
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

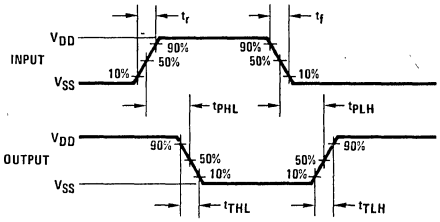
Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

AC Test Circuit and Switching Time Waveforms



TL/F/5976-3

Note: Delays measured with input t_r, t_f = 20 ns.



TL/F/5976-4

National Semiconductor

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate
CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

General Description

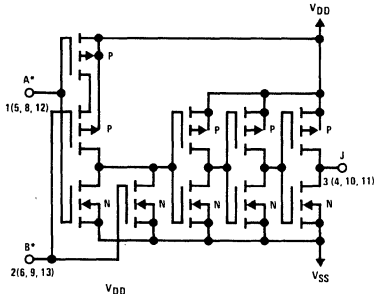
These quad gates are monolithic complementary MOS (CMOS) integrated circuits consructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs protected against static discharge with diodes to V_{DD} and V_{SS}.

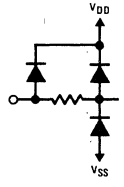
Features

- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

Schematic and Connection Diagrams



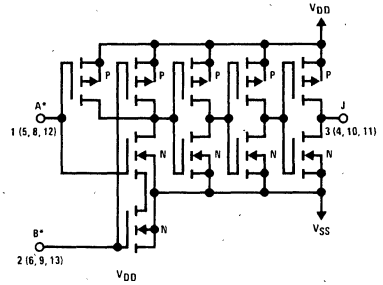
TL/F/5977-1

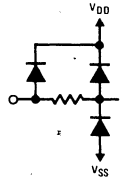


1/4 of device shown

J = A + B
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit





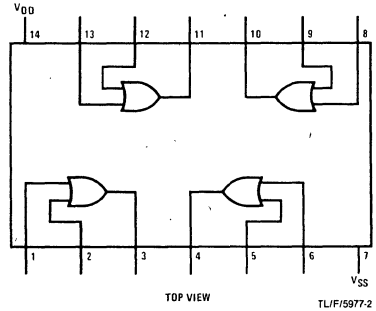
1/4 of device shown

J = A · B
Logical "1" = High
Logical "0" = Low

TL/F/5977-3

*All inputs protected by standard CMOS protection circuit.

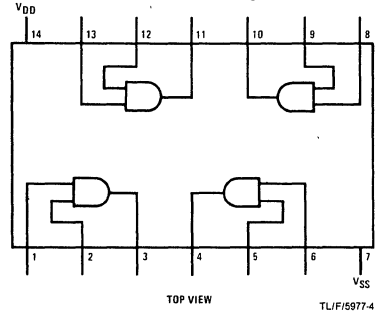
CD4071B
Dual-In-Line Package



TOP VIEW

TL/F/5977-2

CD4081B
Dual-In-Line Package



TOP VIEW

TL/F/5977-4

Order Number CD4071BMJ, CD4071BCJ, CD4081BMJ or CD4081BCJ
See NS Package J14A

Order Number CD4071BMN, CD4071BCN, CD4081BMN or CD4081BCN
See NS Package N14A

Absolute Maximum Ratings

(Notes 1 and 2)

Voltage at Any Pin	−0.5V to V_{DD} + 0.5V
Package Dissipation	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

Operating V_{DD} Range	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4071BM, CD4081BM	−55°C to +125°C
CD4071BC, CD4081BC	−40°C to +85°C

DC Electrical Characteristics — CD4071BM/CD4081BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C MIN	−55°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+125°C MIN	+125°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V		0.50		0.005	0.50		15	μA
		V_{DD} = 15V		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics

CD4071BC/CD4081BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.004	1		7.5	μA
		V_{DD} = 10V		2		0.005	2		15	μA
		V_{DD} = 15V		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics

CD4071BC/CD4071BM

T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF. R_L=200KΩ Typical temperature coefficient is 0.3%/°C

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	100	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	90	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics CD4081BC/CD4081BM

$T_A = 25°C$, Input t_r; $t_f = 20$ ns. $C_L = 50$ pF. $R_L = 200K$ Typical temperature coefficient is 0.3%/°C

SYMBOL	PARAMETER	CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	$V_{DD} = 5V$	100	250	ns
		$V_{DD} = 10V$	40	100	ns
		$V_{DD} = 15V$	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	$V_{DD} = 5V$	120	250	ns
		$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	35	70	ns
t_{THL},t_{TLH}	Transition Time	$V_{DD} = 5V$	90	200	ns
		$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

Typical Performance Characteristics

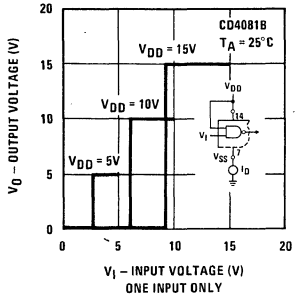


FIGURE 1. Typical Transfer Characteristics

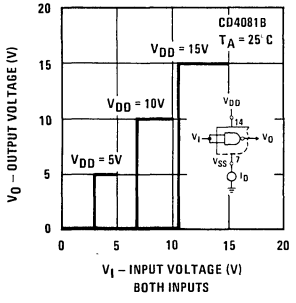


FIGURE 2. Typical Transfer Characteristics

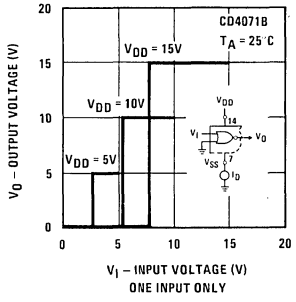


FIGURE 3. Typical Transfer Characteristics

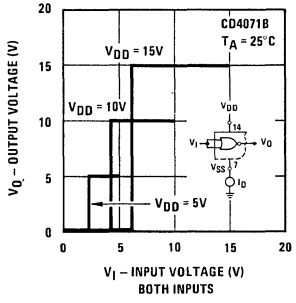


FIGURE 4. Typical Transfer Characteristics

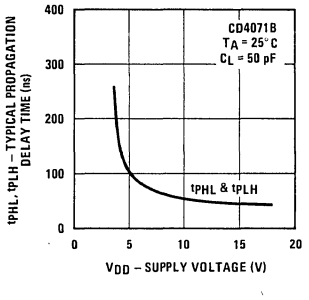


FIGURE 5

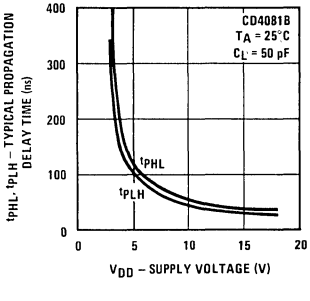


FIGURE 6

Typical Performance Characteristics (Cont'd.)

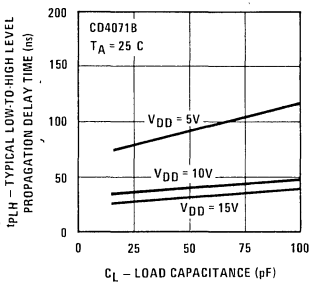


FIGURE 7

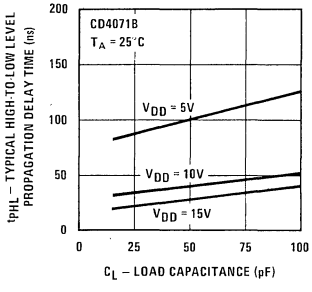


FIGURE 8

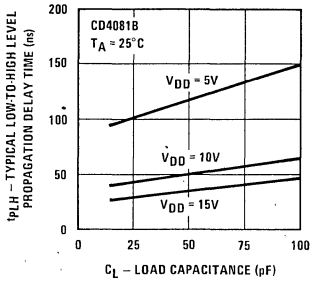


FIGURE 9

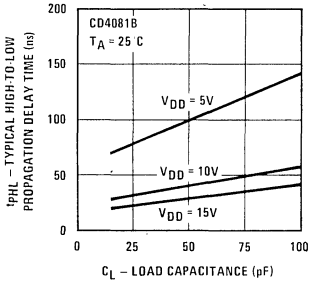


FIGURE 10

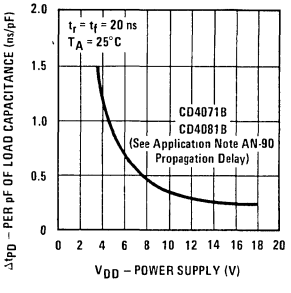


FIGURE 11

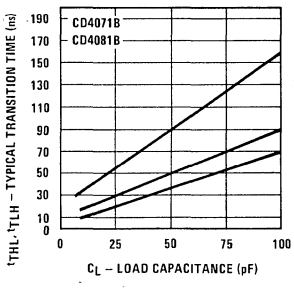


FIGURE 12

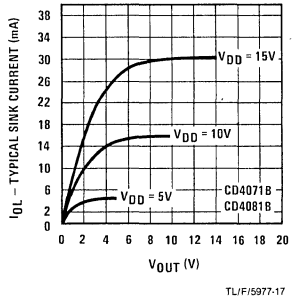


FIGURE 13

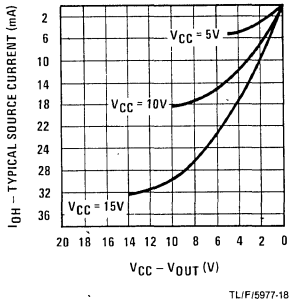


FIGURE 14

National Semiconductor

CD4072BM/CD4072BC Dual 4-Input OR Gate, CD4082BM/CD4082BC Dual 4-Input AND Gate

General Description

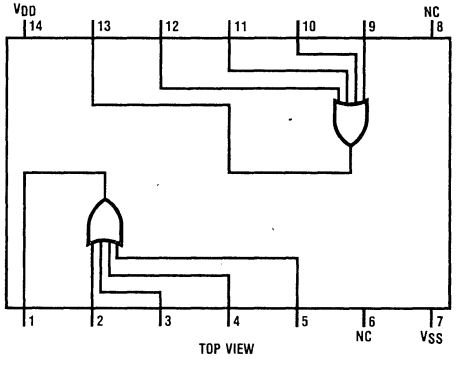
These dual gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity $0.45\,V_{DD}$ (typ.)
- Low power TTL compatibility fanout of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

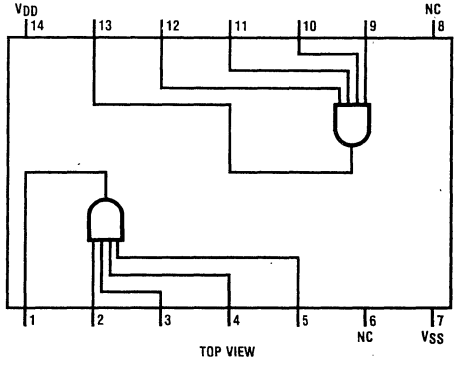
Connection Diagram

CD4072BM/CD4072BC



TL/F/5978-1

CD4082BM/CD4082BC



TL/F/5978-2

Order Number CD4072BMJ, CD4072BCJ, CD4082BMJ or CD4082BCJ
See NS Package J14A

Order Number CD4072BMN, CD4072BCN, CD4082BMN or CD4082BCN
See NS Package N14A

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5 V to +18 V
V_{IN}	Input Voltage	−0.5 to V_{DD}0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD}	Supply Voltage	3.0 to 15 V
V_{IN}	Input Voltage	0 V to V_{DD} V
T_A	Operating Temperature Range	
	CD4072BM, CD4082BM	−55°C to +125°C
	CD4072BC, CD4082BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4072BM, CD4082BM

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0 V		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10 V		0.5		0.005	0.5		15	μA
		V_{DD} = 15 V		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.2		0.90		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−2.2		−0.90		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.0		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Note 3: I_{OL} and I_{OH} are tested one output at a time.

DC Electrical Characteristics (Note 2) — CD4072BC, CD4082BC

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5.0\,V$		1.0		0.004	1.0		7.5	μA
		$V_{DD}=10\,V$		2.0		0.005	2.0		15	μA
		$V_{DD}=15\,V$		4.0		0.006	4.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5.0\,V$		0.05		0	0.05		0.05	V
		$V_{DD}=10\,V$		0.05		0	0.05		0.05	V
		$V_{DD}=15\,V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5.0\,V$	4.95		4.95	5.0		4.95		V
		$V_{DD}=10\,V$	9.95		9.95	10		9.95		V
		$V_{DD}=15\,V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5\,V$, $V_O=0.5\,V$ or $4.5\,V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10\,V$, $V_O=1.0\,V$ or $9.0\,V$		3.0		4.50	3.0		3.0	V
		$V_{DD}=15\,V$, $V_O=1.5\,V$ or $13.5\,V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5.0\,V$, $V_O=0.5\,V$ or $4.5\,V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10\,V$, $V_O=1.0\,V$ or $9.0\,V$	7.0		7.0	5.50		7.0		V
		$V_{DD}=15\,V$, $V_O=1.5\,V$ or $13.5\,V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5.0\,V$, $V_O=0.4\,V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10\,V$, $V_O=0.5\,V$	1.3		1.1	2.2		0.90		mA
		$V_{DD}=15\,V$, $V_O=1.5\,V$	3.6		3.0	8.0		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5.0\,V$, $V_O=4.6\,V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10\,V$, $V_O=9.5\,V$	−1.3		−1.1	−2.2		−0.90		mA
		$V_{DD}=15\,V$, $V_O=13.5\,V$	−3.6		−3.0	−8.0		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15\,V$, $V_{IN}=0\,V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15\,V$, $V_{IN}=15\,V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A=25°C$, $C_L=50\,pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}	Propagation Delay, High to Low Level	$V_{DD}=5.0\,V$		125	250	ns
		$V_{DD}=10\,V$		60	100	ns
		$V_{DD}=15\,V$		45	70	ns
t_{PLH}	Propagation Delay, Low to High Level	$V_{DD}=5.0\,V$		125	250	ns
		$V_{DD}=10\,V$		60	100	ns
		$V_{DD}=15\,V$		45	70	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD}=5.0\,V$		100	200	ns
		$V_{DD}=10\,V$		50	100	ns
		$V_{DD}=15\,V$		40	80	ns
C_{IN}	Average Input Capacitance (Note 4)	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity (Note 5)	Any Gate		20		pF

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics, Application Note AN-90.

National Semiconductor

CD4073BM/CD4073BC Double Buffered Triple 3-Input AND Gate
CD4075BM/CD4075BC Double Buffered Triple 3-Input OR Gate

General Description

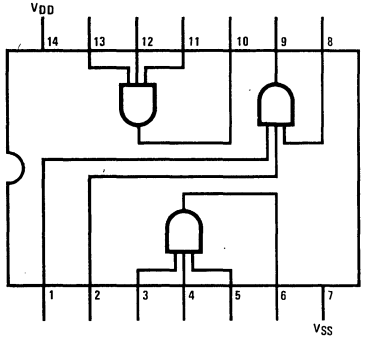
These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} typ.
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V - 10V - 15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range

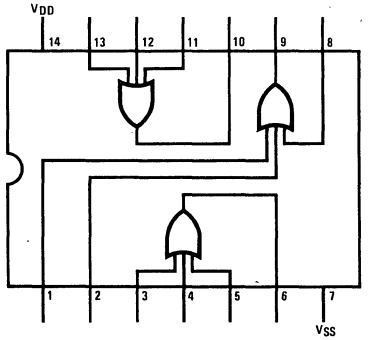
Connection Diagrams Dual-In-Line Packages

CD4073 Triple 3-Input AND Gate



TOP VIEW TL/F/5979-1

CD4075B Triple 3-Input OR Gate



TOP VIEW TL/F/5979-2

Order Number CD4073BMJ, CD4073BCJ, CD4075BMJ or CD4075BCJ
See NS Package J14A

Order Number CD4073BMN, CD4073BCN, CD4075BMN or CD4075BCN
See NS Package N14A

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
V_{IN}	Input Voltage	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
T_S	Storage Temperature Range	$-65°C$ to $+150°C$
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	260°C

Operating Conditions (Note 2)

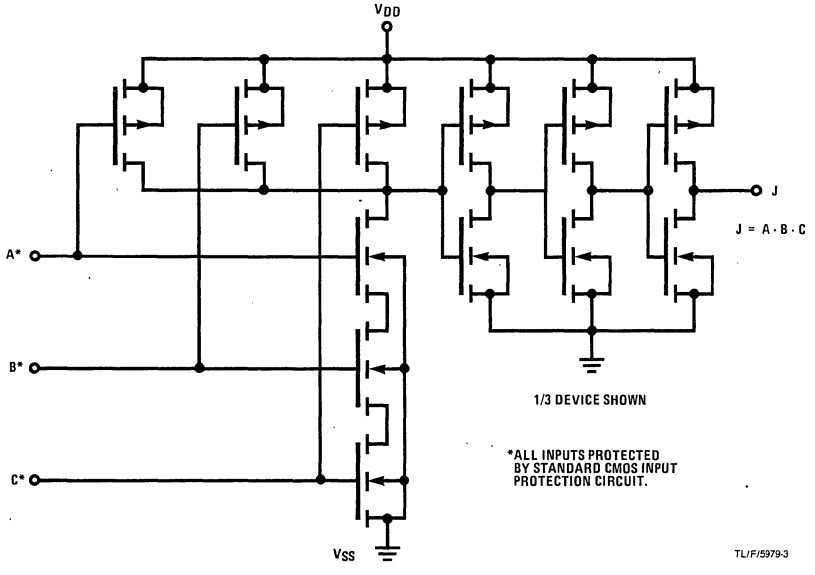
V_{DD}	DC Supply Voltage	$+5\ V_{DC}$ to $+15\ V_{DC}$
V_{IN}	Input Voltage	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
T_A	Operating Temperature Range	
CD4073BM/CD4075BM		$-55°C$ to $+125°C$
CD4073BC/CD4075BC		$-40°C$ to $+85°C$

DC Electrical Characteristics CD4073BM/CD4075BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5V$, $V_{IN} = V_{DD}$ or V_{SS}		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10V$, $V_{IN} = V_{DD}$ or V_{SS}		0.5		0.005	0.5		15	μA
		$V_{DD} = 15V$, $V_{IN} = V_{DD}$ or V_{SS}		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10\ V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15\ V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10\ V$ | $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15\ V$ | $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 0.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		1.5		2	1.5		1.5	V
		$V_{DD} = 10\ V$, $V_O = 1.0\ V$ | $\lvert I_O \rvert < 1\ \mu A$		3.0		4	3.0		3.0	V
		$V_{DD} = 15\ V$, $V_O = 1.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 4.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	3.5		3.5	3		3.5		V
		$V_{DD} = 10\ V$, $V_O = 9.0\ V$ | $\lvert I_O \rvert < 1\ \mu A$	7.0		7.0	6		7.0		V
		$V_{DD} = 15\ V$, $V_O = 13.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5\ V$, $V_O = 0.4\ V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10\ V$, $V_O = 0.5\ V$	1.6		1.3	2.2		0.90		mA
		$V_{DD} = 15\ V$, $V_O = 1.5\ V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5\ V$, $V_O = 4.6\ V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10\ V$, $V_O = 9.5\ V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD} = 15\ V$, $V_O = 13.5\ V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15\ V$, $V_{IN} = 0\ V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15\ V$, $V_{IN} = 15\ V$		0.10		10^{-5}	0.10		1.0	μA

Schematic Diagram

CD4073BC



TL/F/5979-3

DC Electrical Characteristics CD4073BC/CD4075BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1		0.004	1		7.5	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2		0.005	2		15	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V, $\lvert I_O \rvert < 1\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $\lvert I_O \rvert < 1\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V, $\lvert I_O \rvert < 1\,\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V, $\lvert I_O \rvert < 1\,\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10 V, $\lvert I_O \rvert < 1\,\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15 V, $\lvert I_O \rvert < 1\,\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V, $\lvert I_O \rvert < 1\,\mu A$		1.5		2	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V, $\lvert I_O \rvert < 1\,\mu A$		3.0		4	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V, $\lvert I_O \rvert < 1\,\mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 4.5 V, $\lvert I_O \rvert < 1\,\mu A$	3.5		3.5	3		3.5		V
		V_{DD} = 10 V, V_O = 9.0 V, $\lvert I_O \rvert < 1\,\mu A$	7.0		7.0	6		7.0		V
		V_{DD} = 15 V, V_O = 13.5 V, $\lvert I_O \rvert < 1\,\mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 4.6 V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15 V, V_O = 13.5 V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.30		10^{-5}	0.30		1.0	μA

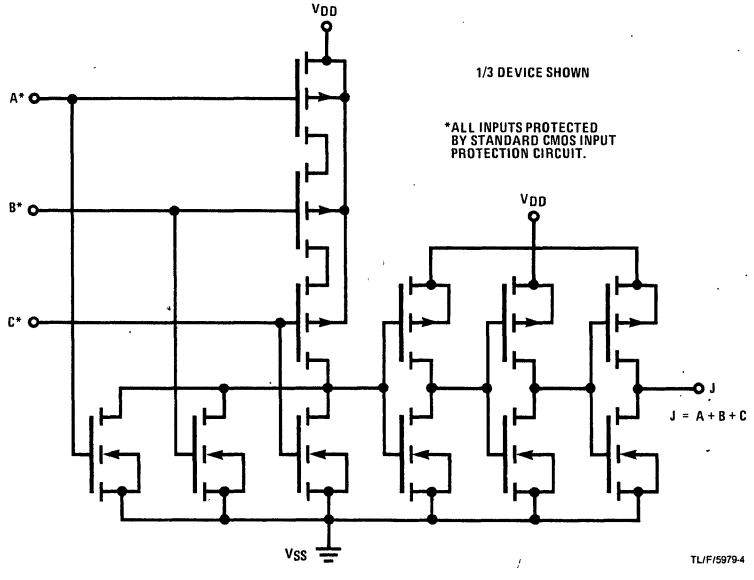
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Schematic Diagram

CD4075BC



AC Electrical Characteristics CD4073BM/CD4073BC/CD4075BM/CD4075BC

$T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$ unless otherwise specified.

SYM	PARAMETER	CONDITIONS	CD4073BC CD4073BM			CD4075BC CD4075BM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay, High to Low Level	$V_{DD} = 5\,V$		130	250		140	250	ns
		$V_{DD} = 10\,V$		60	100		70	100	ns
		$V_{DD} = 15\,V$		40	70		50	70	ns
t_{PLH}	Propagation Delay, Low to High Level	$V_{DD} = 5\,V$		140	250		130	250	ns
		$V_{DD} = 10\,V$		70	100		50	100	ns
		$V_{DD} = 15\,V$		50	70		40	70	ns
t_{THL} t_{TLH}	Transition Time	$V_{DD} = 5\,V$		90	200		90	200	ns
		$V_{DD} = 10\,V$		50	100		50	100	ns
		$V_{DD} = 15\,V$		40	80		40	80	ns
C_{IN}	Average Input Capacitance (See Note 4)	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (See Note 5)	Any Gate		17			17		pF

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family characteristics Application Note AN-90.

National Semiconductor

CD4076BM/CD4076BC TRI-STATE® Quad D Flip-Flop

General Description

The CD4076BM/CD4076BC TRI-STATE quad D flip-flop is a monlithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. The four D type flip-flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disables allow the flip flops to remain in their present state without disrupting the clock. If either of the two input disables is taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip-flops do not change state.

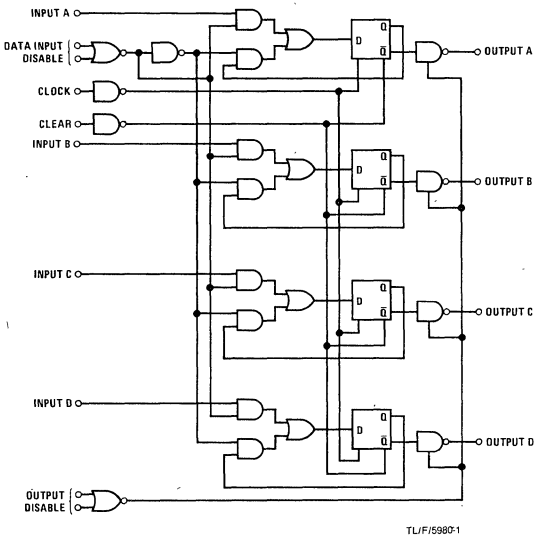
Clearing is enabled by taking the clear input to a logic "1" level. Clocking occurs on the positive-going transition.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

Features

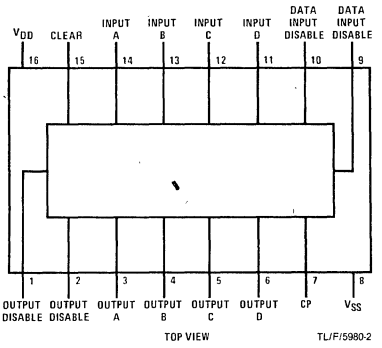
- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- High impedance TRI-STATE outputs
- Inputs can be disabled without gating the clock
- Equivalent to MM54C173/MM74C173

Logic and Connection Diagrams



TL/F/5980-1

Dual-In-Line Package



TOP VIEW

TL/F/5980-2

Order Number CD4076BMJ or CD4076BCJ
See NS Package J16A

Order Number CD4076BMN or CD4076BCN
See NS Package N16E

Truth Table

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions (Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4076BM	−55°C to +125°C
CD4076BC	−40°C to +85°C

DC Electrical Characteristics CD4076BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	Output Current in High Impedance State	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4076BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA

DC Electrical Characteristics (Cont'd.) CD4076BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	Output Current in High Impedance State	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, $R_L = 200k$, Input $t_r = t_f = 20ns$, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Output	V_{DD} = 5V		220	400	ns
		V_{DD} = 10V		80	200	ns
		V_{DD} = 15V		65	160	ns
t_{PHL}	Propagation Delay Time From Clear to Output	V_{DD} = 5V		240	490	ns
		V_{DD} = 10V		90	180	ns
		V_{DD} = 15V		70	145	ns
t_{SU}	Minimum Input Data Set-Up Time	V_{DD} = 5V		40	80	ns
		V_{DD} = 10V		15	30	ns
		V_{DD} = 15V		12	25	ns
t_H	Minimum Input Data Hold Time	V_{DD} = 5V		−40	0	ns
		V_{DD} = 10V		−12	0	ns
		V_{DD} = 15V		−10	0	ns
t_{SU}	Minimum Input Disable Set-Up Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		35	70	ns
		V_{DD} = 15V		28	55	ns
t_H	Minimum Input Disable Hold Time	V_{DD} = 5V		−75	0	ns
		V_{DD} = 10V		−30	0	ns
		V_{DD} = 15V		−25	0	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time From Output Disable to High Impedance State	V_{DD} = 5V, R_L = 1.0k		170	340	ns
		V_{DD} = 10V, R_L 1.0k		70	140	ns
		V_{DD} = 15V, R_L 1.0k		56	115	ns
	Propagation Delay From Output Disable to Logical "1" Level or Logical "0" Level (From High Impedance State)	V_{DD} = 5V, R_L = 1.0k		170	340	ns
		V_{DD} = 10V, R_L = 1.0k		70	140	ns
		V_{DD} = 15V, R_L = 1.0k		56	115	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	3.0	4.0		MHz
		V_{DD} = 10V	7.0	12.0		MHz
		V_{DD} = 15V	8.75	15.0		MHz
t_{WH}	Minimum Clear Pulse Width	V_{DD} = 5V		150		ns
		V_{DD} = 10V		70		ns
		V_{DD} = 15V		56		ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	10			μs
		V_{DD} = 10V	5			μs
		V_{DD} = 15V	2			μs
C_{IN}	Average Input Capacitance	Data Inputs (A, B, C, D)		3	7.5	pF
		Other Inputs		6	15	pF
C_{PD}	Power Dissipation Capacity	All Four Flip-Flops, (Note 4)		100		pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output			15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

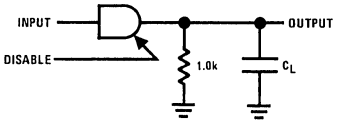
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN–90.

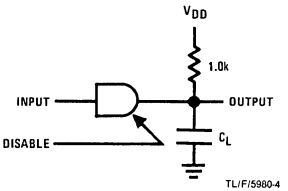
AC Test Circuits and Switching Time Waveforms

t_{PHZ} and t_{PZH}



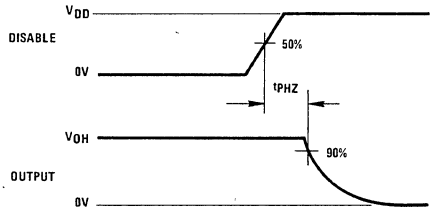
TL/F/5980-3

t_{PLZ} and t_{PZL}



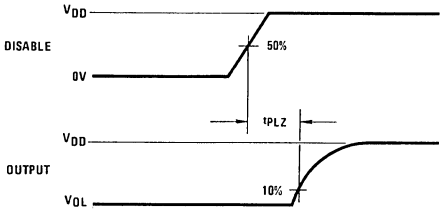
TL/F/5980-4

t_{PHZ}



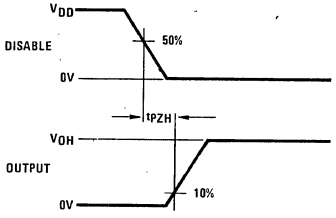
TL/F/5980-5

t_{PLZ}

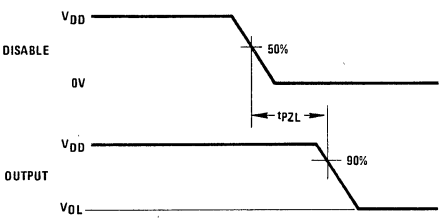


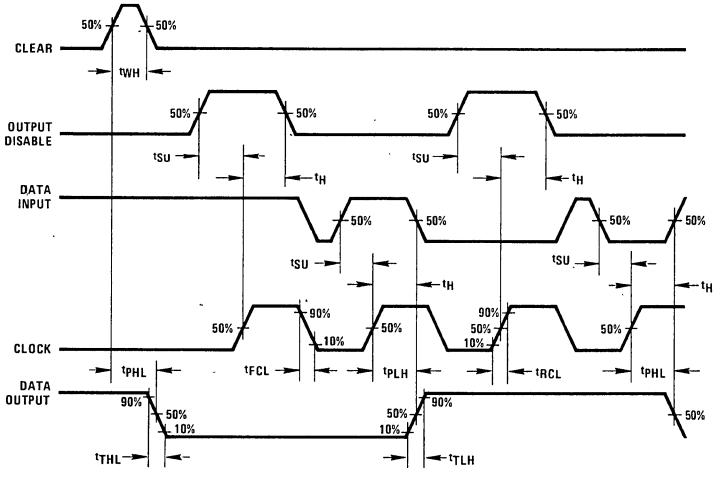
TL/F/5980-6

t_{PZH}



t_{PZL}





TL/F/5980-7

National Semiconductor

CD4089BM/CD4089BC Binary Rate Multiplier
CD4527BM/CD4527BC BCD Rate Multiplier

General Description

The CD4089B is a 4-bit binary rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by $1/16$ times the binary input number. For example, if 5 is the binary input number, there will be 5 output pulses for every 16 clock pulses.

The CD4527B is a 4-bit BCD rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by $1/10$ times the BCD input number. For example, if 5 is the BCD input number, there will be 5 output pulses for every 10 clock pulses.

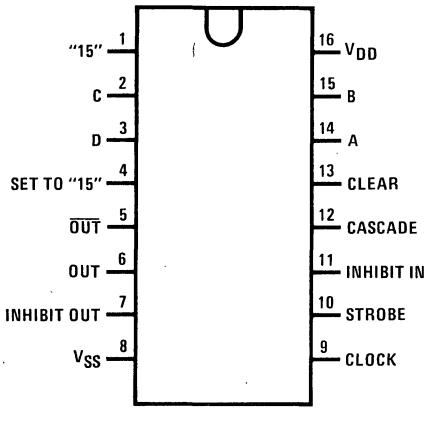
These devices may be used to perform arithmetic operations including multiplication and division, A/D and D/A conversion and frequency division.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} typ.
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Internally synchronous 4-bit counter
- Output clocked on the negative-going edge of clock
- STROBE for inhibiting and enabling outputs
- INHIBIT IN and CASCADE inputs for cascade operation
- Complementary output
- CLEAR and SET inputs
- "9" or "15" output and INHIBIT OUT output

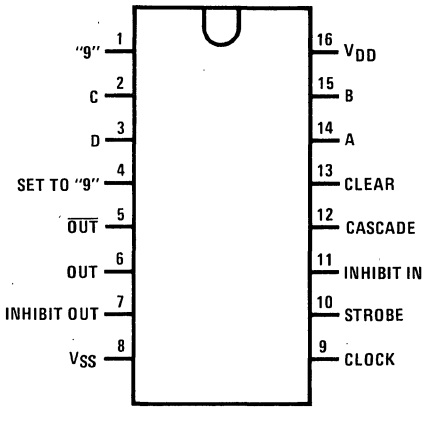
Connection Diagrams

CD4089B
Dual-In-Line Package



TOP VIEW TL/F/5981-1

CD4527B
Dual-In-Line Package



TOP VIEW TL/F/5981-2

Order Number CD4089BMJ, CD4089BCJ, CD4527BMJ or CD4527BCJ
See NS Package J16A

Order Number CD4089BMN, CD4089BCN, CD4527BMN or CD4527BCN
See NS Package N16E

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3 to 15 V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4089BM, CD4527BM	−55°C to +125°C
CD4089BC, CD4527BC	−40°C to +85°C

DC Electrical Characteristics CD4089BM/CD4527BM (note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\,\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\,\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4089BC/CD4527BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\,\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\,\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA

5

DC Electrical Characteristics (Cont'd.) CD4089BC/CD4527BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to Out or $\overline{Out}$	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		60	120	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to E_{OUT}	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		120	240	ns
		V_{DD} = 15V		75	150	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to "9" or "15"	V_{DD} = 5V		280	560	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		70	140	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Set or Clear to Out or $\overline{Out}$	V_{DD} = 5V		500	1100	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		150	300	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Cascade to Out	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		35	70	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Strobe to Out	V_{DD} = 5V		220	440	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		65	130	ns
t_{TLH}, t_{THL}	Transition Time, All Outputs	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
$t_{W(CL)}$	Minimum Clock Pulse Width	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		70	140	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1	2		MHz
		V_{DD} = 10V	2.5	5		MHz
		V_{DD} = 15V	3.5	7		MHz
t_r	Maximum Clock Rise Time	V_{DD} = 5V			5	μs
		V_{DD} = 10V			1.5	μs
		V_{DD} = 15V			1.0	μs
t_f	Maximum Clock Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
$t_{W(S,R)}$	Minimum Set or Clear Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		25	55	ns
t_{REM}	Set Removal Time	V_{DD} = 5V		−45	0	ns
		V_{DD} = 10V		−20	0	ns
		V_{DD} = 15V		−10	0	ns
t_{SET-UP}	Inhibit In Set-Up Time	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		60	120	ns
		V_{DD} = 15V		45	90	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 4)		80		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Truth Tables

CD4089B
Binary Rate Multiplier

INPUTS										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (H OR L)			
D	C	B	A	No. of Clock Pulses	Inh_{In}	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 $\overline{Out}$	Pin 7 Inh Out	Pin 1 "15"
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	0	1	L	H	L	H

*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

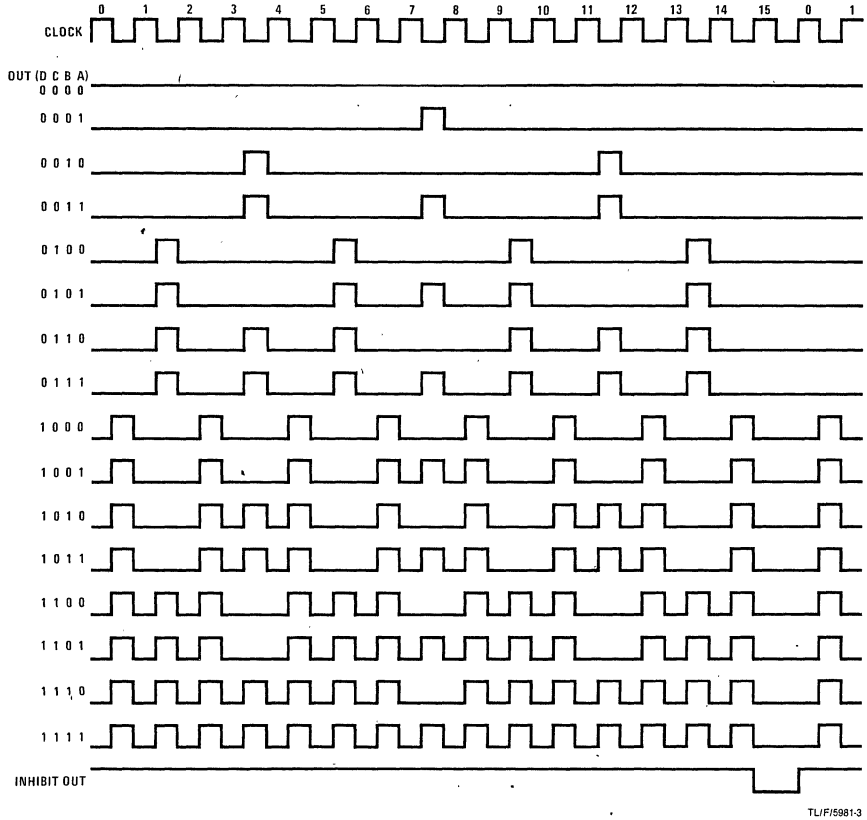
CD4527B
BCD Rate Multiplier

INPUTS										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (H OR L)			
D	C	B	A	No. of Clock Pulses	Inh_{In}	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 $\overline{Out}$	Pin 7 Inh Out	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

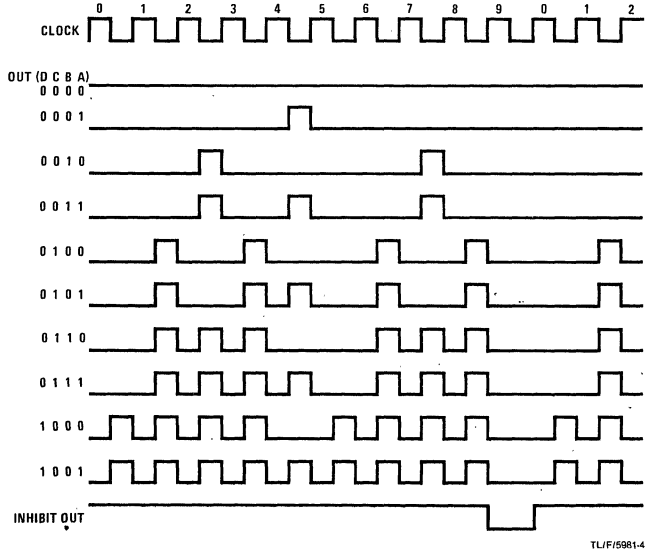
Logic Waveforms

CD4089B
Binary Rate Multiplier



TL/F/5981-3

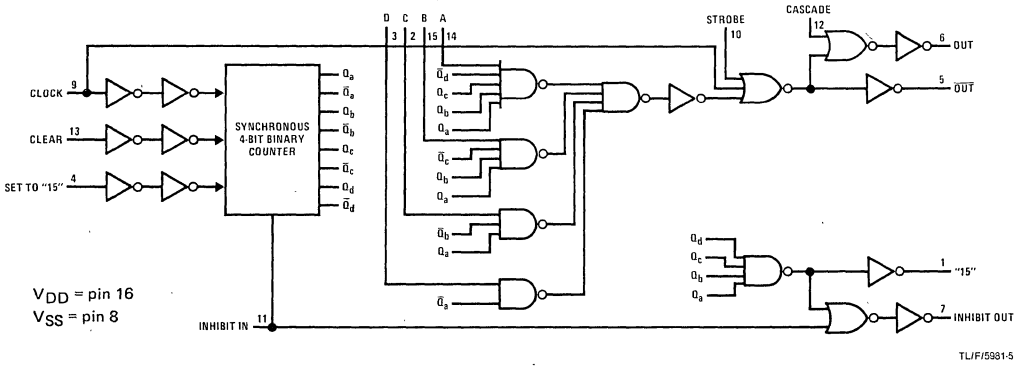
CD4527B
BCD Rate Multiplier



TL/F/5981-4

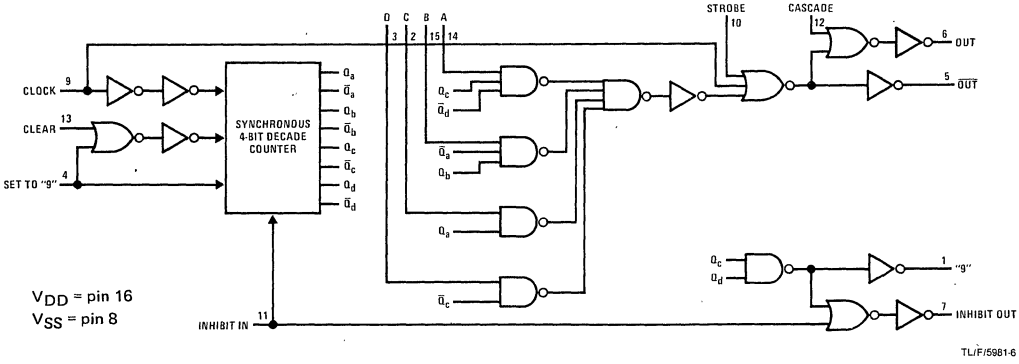
Logic Diagrams

CD4089B
Binary Rate Multiplier



TL/F/5981-5

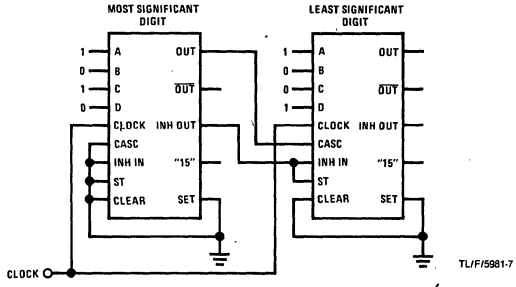
CD4527B
BCD Rate Multiplier



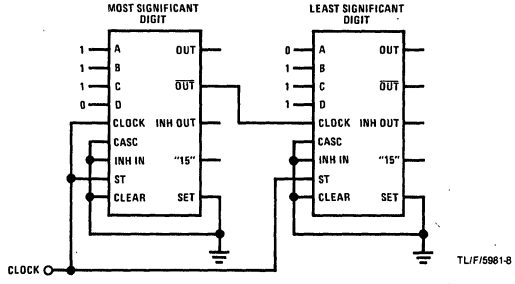
TL/F/5981-6

5

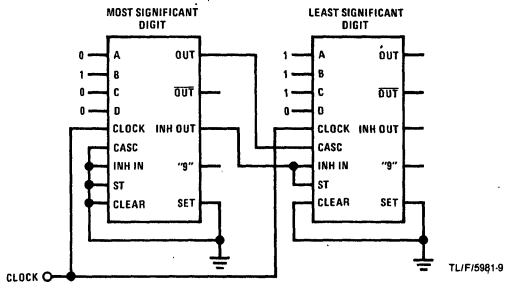
Cascading Packages



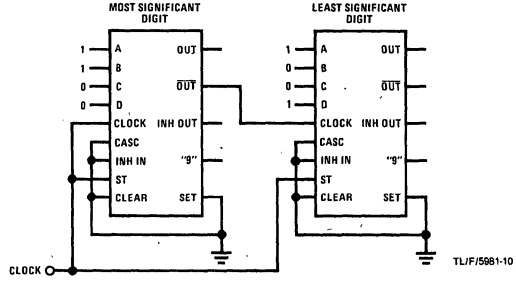
Two CD4089B's cascaded in the "add" mode with a preset number of 89 $\left(\frac{5}{16} + \frac{9}{256} = \frac{89}{256}\right)$



Two CD4089B's cascaded in the "multiply" mode with a preset number of 98 $\left(\frac{7}{16} \times \frac{14}{16} = \frac{98}{256}\right)$



Two CD4527B's cascaded in the "add" mode with a preset number of 27 $\left(\frac{2}{10} + \frac{7}{100} = \frac{27}{100}\right)$



Two CD4527B's cascaded in the "multiply" mode with a preset number of 27 $\left(\frac{3}{10} \times \frac{9}{10} = \frac{27}{100}\right)$

National Semiconductor

CD4093BM/CD4093BC Quad 2-Input NAND Schmitt Trigger

General Description

The CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive (V_T^+) and the negative voltage (V_T^-) is defined as hysteresis voltage (V_H).

All outputs have equal source and sink currents and conform to standard B-series output drive (see Static Electrical Characteristics).

Features

- Wide supply voltage range 3.0 V to 15 V
- Schmitt-trigger on each input with no external components
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall time
- Standard B-series output drive
- Hysteresis voltage (any input) $T_A = 25°C$

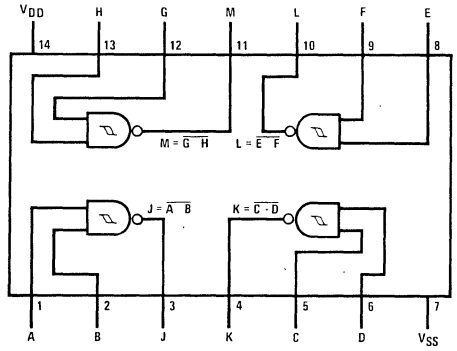
Typical	$V_{DD} = 5.0\,V$	$V_H = 1.5\,V$
	$V_{DD} = 10\,V$	$V_H = 2.2\,V$
	$V_{DD} = 15\,V$	$V_H = 2.7\,V$
Guaranteed		$V_H = 0.1\,V_{DD}$

Applications

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5982-1

Order Number CD4093BMJ or CD4093BCJ
See NS Package J14A

Order Number CD4093BMN or CD4093BCN
See NS Package N14A

5

Absolute Maximum Ratings

(Notes 1 and 2)

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Package Dissipation (P_D)	500 mW
Lead Temperature (Soldering, 10 seconds) (T_L)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4093BM	−55°C to +125°C
CD4093BC	−40°C to +85°C

DC Electrical Characteristics CD4093BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25			0.25		7.5	μA
		V_{DD} = 10V		0.5			0.5		15.0	μA
		V_{DD} = 15V		1.0			1.0		30.0	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{SS}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 4.5V	1.3	2.25	1.5	1.8	2.25	1.5	2.3	V
		V_{DD} = 10V, V_O = 9V	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		V_{DD} = 15V, V_O = 13.5V	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_{T+}	Positive-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 0.5V	2.75	3.65	2.75	3.3	3.5	2.65	3.5	V
		V_{DD} = 10V, V_O = 1V	5.5	7.15	5.5	6.2	7.0	5.35	7.0	V
		V_{DD} = 15V, V_O = 1.5V	8.25	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
	(Any Input)	V_{DD} = 10V	1.0	4.30	1.0	2.2	4.0	0.70	4.0	V
		V_{DD} = 15V	1.5	6.30	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current	V_{IN} = V_{DD}								
	(Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{IN} = V_{SS}								
	(Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4093BC (Note 2)

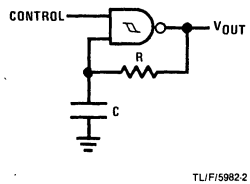
SYM	PARAMETER	CONDITIONS	−40°C		25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		7.5	μA
		V_{DD} = 10V		2.0			2.0		15.0	μA
		V_{DD} = 15V		4.0			4.0		30.0	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{SS}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 4.5V	1.3	2.25	1.5	1.8	2.25	1.5	2.30	V
		V_{DD} = 10V, V_O = 9V	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		V_{DD} = 15V, V_O = 13.5V	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_{T+}	Positive-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 0.5V	2.75	3.6	2.75	3.3	3.5	2.65	3.5	V
		V_{DD} = 10V, V_O = 1V	5.5	7.15	5.5	6.2	7.0	5.35	7.0	V
		V_{DD} = 15V, V_O = 1.5V	8.25	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
	(Any Input)	V_{DD} = 10V	1.0	4.3	1.0	2.2	4.0	0.70	4.0	V
		V_{DD} = 15V	1.5	6.3	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current	V_{IN} = V_{DD}								
	(Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{IN} = V_{SS}								
	(Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, $R_L = 200k$, Input t_r, $t_f = 20ns$, unless otherwise specified.

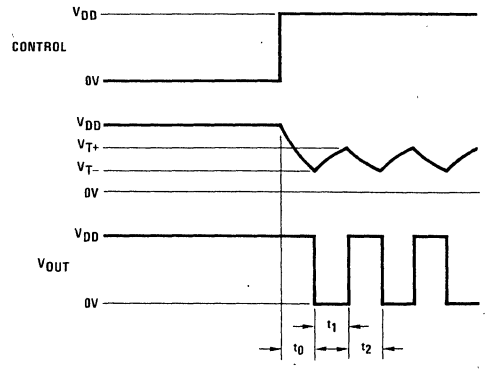
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	450	ns
		V_{DD} = 10V		120	210	ns
		V_{DD} = 15V		80	160	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		90	145	ns
		V_{DD} = 10V		50	75	ns
		V_{DD} = 15V		40	60	ns
C_{IN}	Input Capacitance	(Any Input)		5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Per Gate)		24		pF

Typical Applications

Gated Oscillator



TL/F/5982-2



TL/F/5982-3

Assume $t_1 + t_2 >> t_{PHL} + t_{PLH}$ then:

$t_0 = RC \ln [V_{DD}/V_{T-}]$

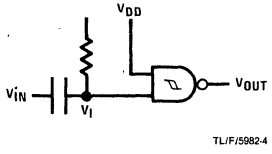
$t_1 = RC \ln [(V_{DD} - V_{T-})/(V_{DD} + V_{T+})]$

$t_2 = RC \ln [V_{T+}/V_{T-}]$

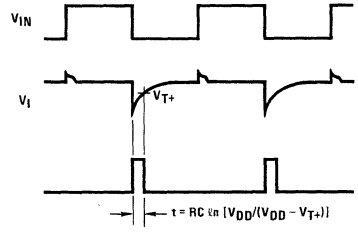
$$f = \frac{1}{t_1 + t_2} = \frac{1}{RC \ln \dfrac{(V_{T+})(V_{DD} - V_{T-})}{(V_{T-})(V_{DD} - V_{T+})}}$$

Gated One-Shot

(a) Negative-Edge Triggered

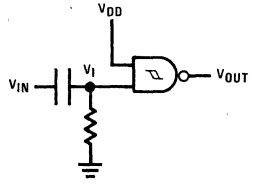


TL/F/5982-4

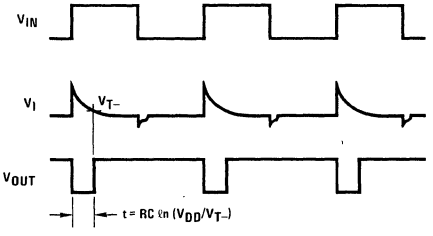


TL/F/5982-5

(b) Positive-Edge Triggered



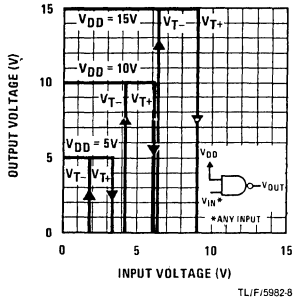
TL/F/5982-6



TL/F/5982-7

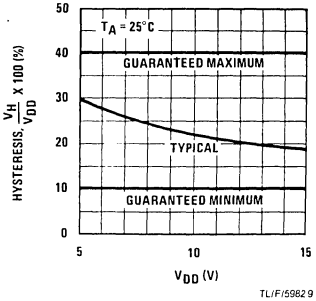
Typical Performance Characteristics

Typical Transfer Characteristics



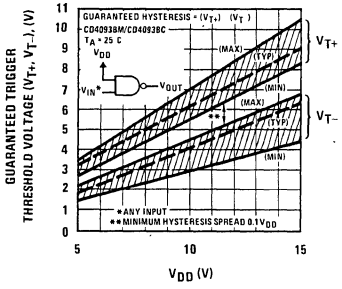
TL/F/5982-8

Guaranteed Hysteresis vs V_{DD}



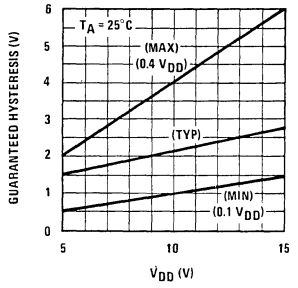
TL/F/5982 9

Guaranteed Trigger Threshold Voltage vs V_{DD}



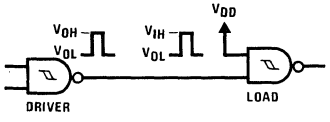
TL/F/5982-10

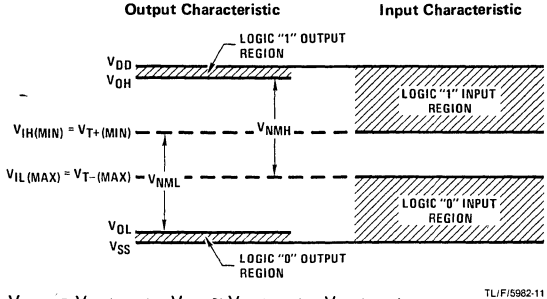
Guaranteed Hysteresis vs V_{DD}



TL/F/5982-11

Input and Output Characteristics



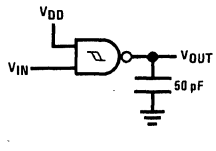


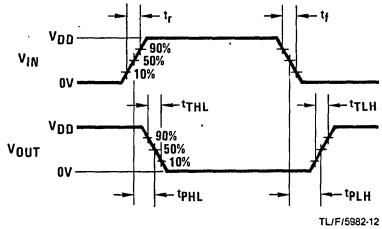
TL/F/5982-11

$V_{NML} = V_{IH(MIN)} - V_{OL} \cong V_{IH(MIN)} = V_{T+(MIN)}$

$V_{NMH} = V_{OH} - V_{IL(MAX)} \cong V_{DD} - V_{IL(MAX)} = V_{DD} - V_{T-(MAX)}$

AC Test Circuits and Switching Time Waveforms





TL/F/5982-12

National Semiconductor

CD4094BM/CD4094BC 8-Bit Shift Register/Latch with TRI-STATE® Outputs

General Description

The CD4094BM/CD4094BC consists of an 8-bit shift register and a TRI-STATE 8-bit latch. Data is shifted serially through the shift register on the positive transition of the clock. The output of the last stage (Q_S) can be used to cascade several devices. Data on the Q_S output is transferred to a second output, Q'_S, on the following negative clock edge.

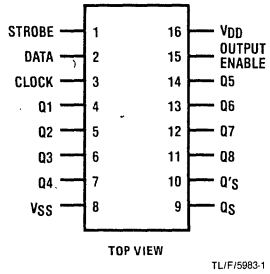
The output of each stage of the shift register feeds a latch, which latches data on the negative edge of the STROBE input. When STROBE is high, data propagates through the latch to TRI-STATE output gates. These gates are enabled when OUTPUT ENABLE is taken high.

Features

- Wide supply voltage range — 3.0V to 18V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- TRI-STATE outputs

Connection Diagram

Dual-In-Line Package

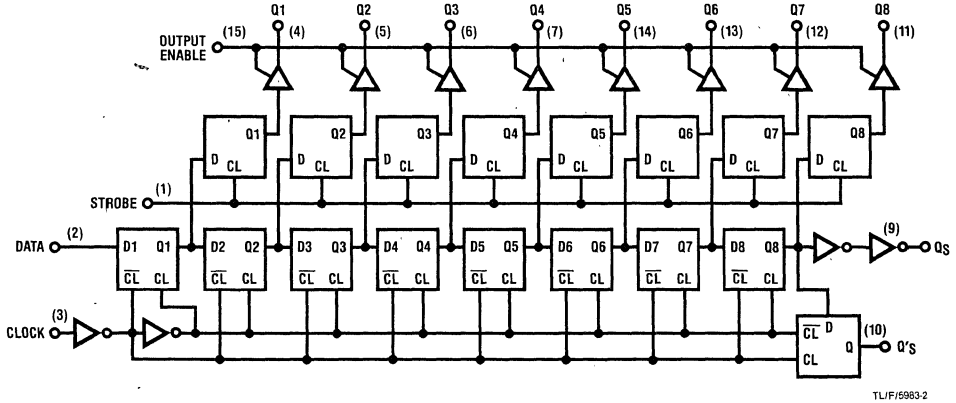


TL/F/5983-1

Order Number CD4094BMJ or CD4094BCJ
See NS Package J16A

Order Number CD4094BMN or CD4094BCN
See NS Package N16E

Block or Logic Diagram



TL/F/5983-2

Absolute Maximum Ratings
(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions
(Note 2)

V_{DD} DC Supply Voltage	+3.0 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4094BM	−55°C to +125°C
CD4094BC	−40°C to +85°C

DC Electrical Characteristics CD4094BM (Note 2)

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0 V		5.0			5.0		150	μA
		V_{DD} = 10 V		10			10		300	μA
		V_{DD} = 15 V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O \rvert \leq 1\,\mu A$	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V, $\lvert I_O \rvert \leq 1\,\mu A$	9.95		9.95	10.0		9.95		V
		V_{DD} = 15 V, $\lvert I_O \rvert \leq 1\,\mu A$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	2.55		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1			−0.1		1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1			0.1		1.0	μA
I_{OZ}	TRI-STATE Output Leakage Current	V_{DD} = 15 V, V_{IN} = 0 V or 15 V		0.3			±0.3		±9	μA

DC Electrical Characteristics CD4094BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0 V		20			20		150	μA
		V_{DD} = 10 V		40			40		300	μA
		V_{DD} = 15 V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V, $\lvert I_O \rvert \leq 1.0\,\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_O \rvert \leq 1\,\mu A$	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V, $\lvert I_O \rvert \leq 1\,\mu A$	9.95		9.95	10.0		9.95		V
		V_{DD} = 15 V, $\lvert I_O \rvert \leq 1\,\mu A$	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 0.4 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0	8.8		2.4		mA

DC Electrical Characteristics (cont'd) CD4094BC (Note 2)

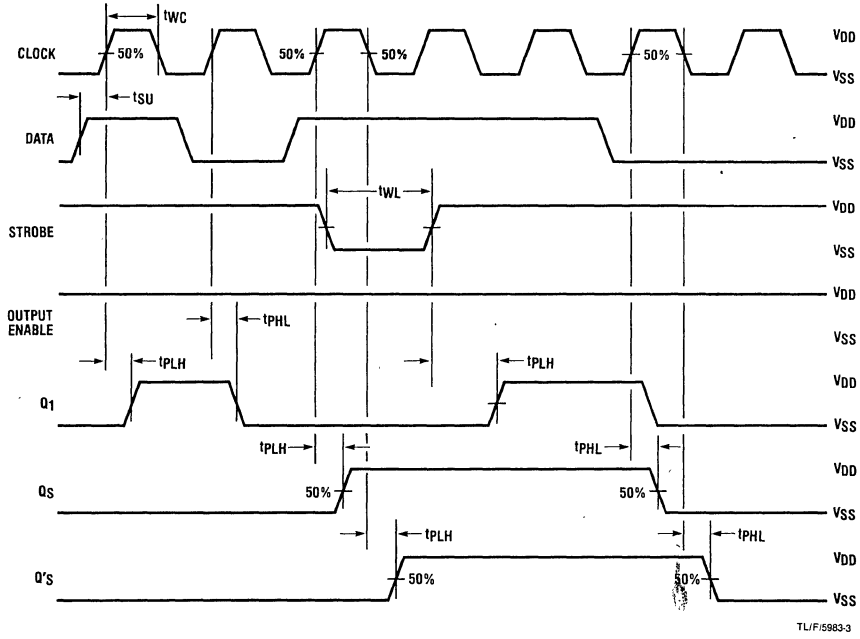
Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5.0\,V$, $V_O=4.6\,V$	−0.52		−0.44	0.88		−0.36		mA
		$V_{DD}=10\,V$, $V_O=9.5\,V$	−1.3		−1.1	2.55		−0.9		mA
		$V_{DD}=15\,V$, $V_O=13.5\,V$	−3.6		−3.0	8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15\,V$, $V_{IN}=0\,V$		−0.3			−0.3		−1.0	μA
		$V_{DD}=15\,V$, $V_{IN}=15\,V$		0.3			0.3		1.0	μA
I_{OZ}	TRI-STATE Output Leakage Current	$V_{DD}=15\,V$, $V_{IN}=0\,V$ or $15\,V$		1			1		10	μA

AC Electrical Characteristics $T_A=25°C$, $C_L=50\,pF$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q_S	$V_{DD}=5.0\,V$		300	600	ns
		$V_{DD}=10\,V$		125	250	ns
		$V_{DD}=15\,V$		95	190	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Q'_S	$V_{DD}=5.0\,V$		230	460	ns
		$V_{DD}=10\,V$		110	220	ns
		$V_{DD}=15\,V$		75	150	ns
t_{PHL}, t_{PLH}	Propagation Delay Clock to Parallel Out	$V_{DD}=5.0\,V$		420	840	ns
		$V_{DD}=10\,V$		195	390	ns
		$V_{DD}=15\,V$		135	270	ns
t_{PHL}, t_{PLH}	Propagation Delay Strobe to Parallel Out	$V_{DD}=5.0\,V$		290	580	ns
		$V_{DD}=10\,V$		145	290	ns
		$V_{DD}=15\,V$		100	200	ns
t_{PHZ}	Propagation Delay High Level to High Impedance	$V_{DD}=5.0\,V$		140	280	ns
		$V_{DD}=10\,V$		75	150	ns
		$V_{DD}=15\,V$		55	110	ns
t_{PLZ}	Propagation Delay Low Level to High Impedance	$V_{DD}=5.0\,V$		140	280	ns
		$V_{DD}=10\,V$		75	150	ns
		$V_{DD}=15\,V$		55	110	ns
t_{PZH}	Propagation Delay High Impedance to High Level	$V_{DD}=5.0\,V$		140	280	ns
		$V_{DD}=10\,V$		75	150	ns
		$V_{DD}=15\,V$		55	110	ns
t_{PZL}	Propagation Delay High Impedance to Low Level	$V_{DD}=5.0\,V$		140	280	ns
		$V_{DD}=10\,V$		75	150	ns
		$V_{DD}=15\,V$		55	110	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD}=5.0\,V$		100	200	ns
		$V_{DD}=10\,V$		50	100	ns
		$V_{DD}=15\,V$		40	80	ns
t_{SU}	Set-up Time Data to Clock	$V_{DD}=5.0\,V$	80	40		ns
		$V_{DD}=10\,V$	40	20		ns
		$V_{DD}=15\,V$	20	10		ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{DD}=5.0\,V$	1			ms
		$V_{DD}=10\,V$	1			ms
		$V_{DD}=15\,V$	1			ms
t_{PC}	Minimum Clock Pulse Width	$V_{DD}=5.0\,V$	200	100		ns
		$V_{DD}=10\,V$	100	50		ns
		$V_{DD}=15\,V$	83	40		ns
t_{PS}	Minimum Strobe Pulse Width	$V_{DD}=5.0\,V$	200	100		ns
		$V_{DD}=10\,V$	80	40		ns
		$V_{DD}=15\,V$	70	35		ns
f_{MAX}	Maximum Clock Frequency	$V_{DD}=5.0\,V$	1.5	3.0		MHz
		$V_{DD}=10\,V$	3.0	6.0		MHz
		$V_{DD}=15\,V$	4.0	8.0		MHz
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.
Note 2: $V_{SS}=0\,V$ unless otherwise specified.
Note 3: I_{OH} and I_{OL} are tested one output at a time.

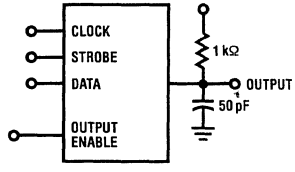
Timing Diagram



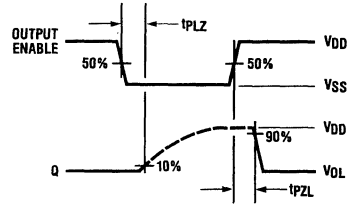
TL/F/5983-3

Test Circuits and Timing Diagrams for TRI-STATE

t_{PZL}, t_{PLZ}

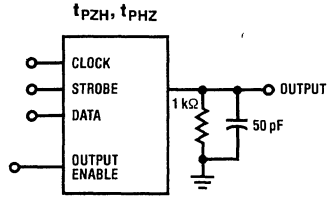


TL/F/5983-4

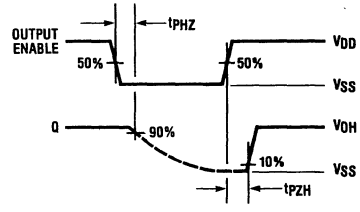


TL/F/5983-5

t_{PZH}, t_{PHZ}



TL/F/5983-6



TL/F/5983-7

Logic Truth Table

Clock	Output Enable	Strobe	Data	Parallel Outputs		Serial Outputs	
				Q1	Q_N	Q_S*	Q'_S
↑	0	X	X	Hi-Z	Hi-Z	Q7	No Chg.
↓	0	X	X	Hi-Z	Hi-Z	No Chg.	Q7
↑	1	0	X	No Chg.	No Chg.	Q7	No Chg.
↑	1	1	0	0	$Q_N - 1$	Q7	No Chg.
↑	1	1	1	1	$Q_N - 1$	Q7	No Chg.
↓	1	1	1	No Chg.	No Chg.	No Chg.	Q7

X = Don't Care
*At the positive clock edge, information in the 7th shift register stage is transferred to Q8 and Q_S.

National Semiconductor

CD4099BM/CD4099BC 8-Bit Addressable Latch

General Description

The CD4099B is an 8-bit addressable latch with three address inputs (A0-A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D), and eight outputs (Q0-Q7).

Data is entered into a particular bit in the latch when that bit is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry is inhibited when enable ($\overline{E}$) is high.

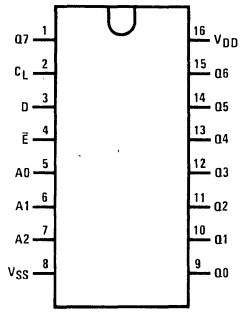
When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high and enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = low), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = high, CL = low).

Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

Connection Diagram

CD4099B
Dual-In-Line Package



TL/F/5984-1

TOP VIEW

Order Number CD4099BMJ or CD4099BCJ
See NS Package J16A

Order Number CD4099BMN or CD4099BCN
See NS Package N16E

Truth Table

MODE SELECTION				
$\overline{E}$	CL	ADDRESSED LATCH	UNADDRESSED LATCH	MODE
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Holds Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3.0 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4099BM	−55°C to +125°C
CD4099BC	−40°C to +85°C

DC Electrical Characteristics CD4099BM (Note 2)

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5.0		0.02	5.0		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.02	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4099BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.02	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.02	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics (cont'd) CD4099BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5.0V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5.0V$, $V_O=4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.30		-10^{-5}	−0.30		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A=25°C$, $C_L=50pF$, $R_L=200k$, Input $t_r=t_f=20ns$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Date to Output	$V_{DD}=5.0V$		200	400	ns
		$V_{DD}=10V$		75	150	ns
		$V_{DD}=15V$		50	100	ns
t_{PLH}, t_{PHL}	Propagation Delay Enable to Output	$V_{DD}=5.0V$		200	400	ns
		$V_{DD}=10V$		80	160	ns
		$V_{DD}=15V$		60	120	ns
t_{PHL}	Propagation Delay Clear to Output	$V_{DD}=5.0V$		175	350	ns
		$V_{DD}=10V$		80	160	ns
		$V_{DD}=15V$		65	130	ns
t_{PLH}, t_{PHL}	Propagation Delay Address to Output	$V_{DD}=5.0V$		225	450	ns
		$V_{DD}=10V$		100	200	ns
		$V_{DD}=15V$		75	150	ns
t_{THL}, t_{TLH}	Transition Time (Any Output)	$V_{DD}=5.0V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
t_{WH}, T_{WL}	Minimum Data Pulse Width	$V_{DD}=5.0V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
t_{WH}, t_{WL}	Minimum Address Pulse Width	$V_{DD}=5.0V$		200	400	ns
		$V_{DD}=10V$		100	200	ns
		$V_{DD}=15V$		65	125	ns
t_{WH}	Minimum Clear Pulse Width	$V_{DD}=5.0V$		75	150	ns
		$V_{DD}=10V$		40	75	ns
		$V_{DD}=15V$		25	50	ns
t_{SU}	Minimum Set-Up Time Data to E	$V_{DD}=5.0V$		40	80	ns
		$V_{DD}=10V$		20	40	ns
		$V_{DD}=15V$		15	30	ns
t_H	Minimum Hold Time Data to E	$V_{DD}=5.0V$		60	120	ns
		$V_{DD}=10V$		30	60	ns
		$V_{DD}=15V$		25	50	ns
t_{SU}	Minimum Set-Up Time Address to E	$V_{DD}=5.0V$		−15	50	ns
		$V_{DD}=10V$		0	30	ns
		$V_{DD}=15V$		0	20	ns
t_H	Minimum Hold Time Address to E	$V_{DD}=5.0V$		−50	15	ns
		$V_{DD}=10V$		−20	10	ns
		$V_{DD}=15V$		−15	5	ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		100		pF
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

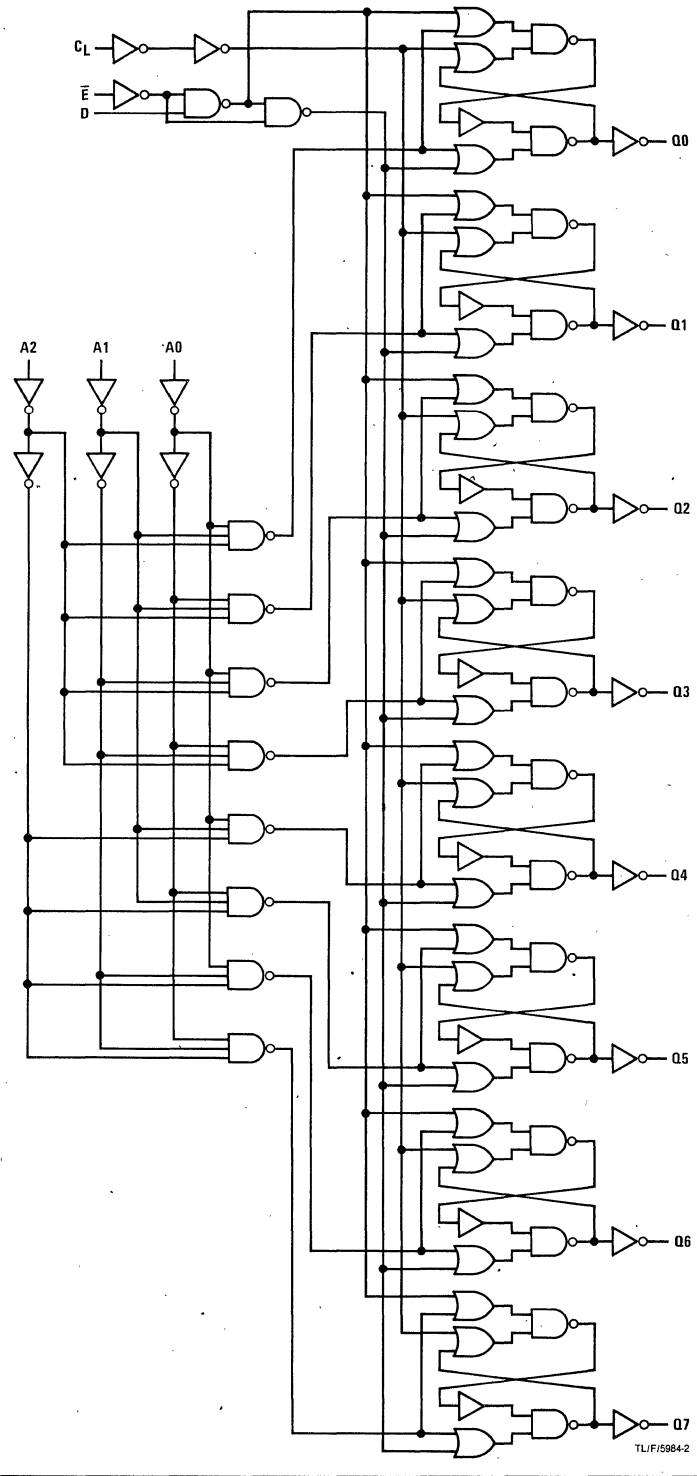
Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Dynamic power dissipation (P_D) is given by: $P_D=(C_{PD}+C_L)V_{CC}^2f+P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see application note AN-90, "54C/74C Family Characteristics".

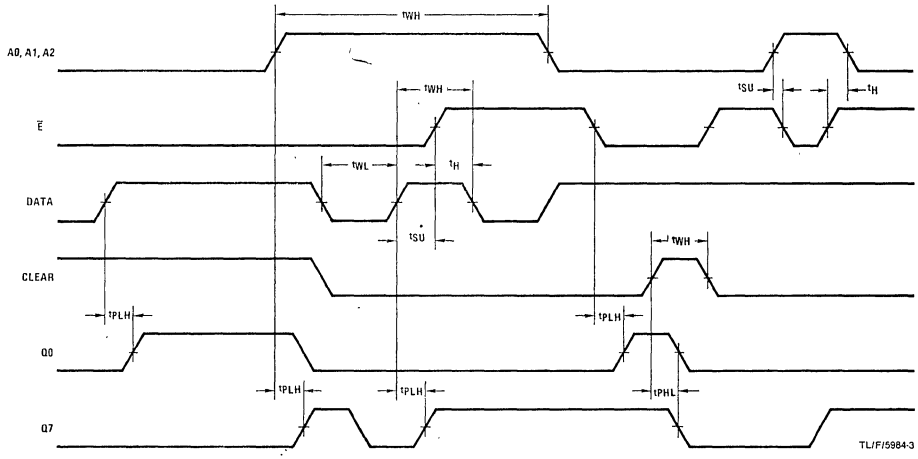
Logic Diagram

CD4099B



TL/F/5984-2

Switching Time Waveforms



National Semiconductor

CD40106BM/CD40106BC Hex Schmitt Trigger

General Description

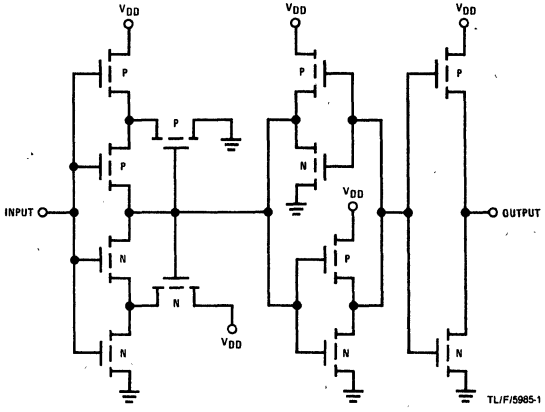
The CD40106B Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{DD} = 10V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{DD}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

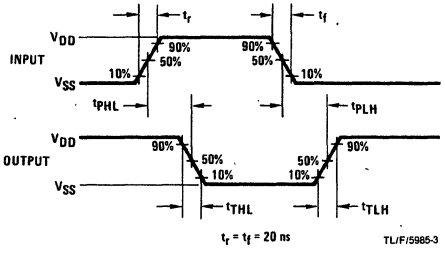
Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.7 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Hysteresis — 0.4 V_{DD} typ, 0.2 V_{DD} guaranteed
- Equivalent to MM54C14/MM74C14
- Equivalent to MC14584B

Schematic Diagram

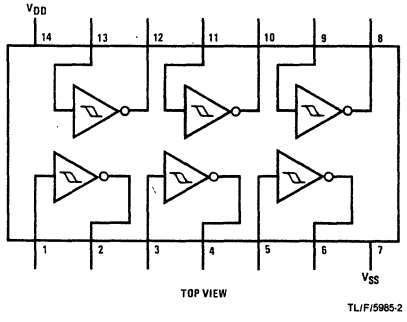


Switching Time Waveforms



Connection Diagram

Dual-In-Line Package



Order Number CD40106BMJ or CD40106BCJ
See NS Package J14A

Order Number CD40106BMN or CD40106BCN
See NS Package N14A

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40106BM	−55°C to +125°C
CD40106BC	−40°C to +85°C

DC Electrical Characteristics CD40106BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	V_{DD} = 5V, V_O = 4.5V	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		V_{DD} = 10V, V_O = 9V	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		V_{DD} = 15V, V_O = 13.5V	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	V_{DD} = 5V, V_O = 0.5V	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		V_{DD} = 10V, V_O = 1V	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		V_{DD} = 15V, V_O = 1.5V	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		V_{DD} = 10V	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		V_{DD} = 15V	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

5

DC Electrical Characteristics CD40106BC (Note 2)

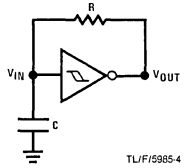
SYM	PARAMETER	CONDITIONS	−40°C		25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4.0			4.0		30	μA
		V_{DD} = 10V		8.0			8.0		60	μA
		V_{DD} = 15V		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	V_{DD} = 5V, V_O = 4.5V	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		V_{DD} = 10V, V_O = 9V	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		V_{DD} = 15V, V_O = 13.5V	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	V_{DD} = 5V, V_O = 0.5V	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		V_{DD} = 10V, V_O = 1V	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		V_{DD} = 15V, V_O = 1.5V	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		V_{DD} = 10V	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		V_{DD} = 15V	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k$, t_r and $t_f = 20\,ns$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	V_{DD} = 5V		220	400	ns
		V_{DD} = 10V		80	200	ns
		V_{DD} = 15V		70	160	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 4)		14		pF

Typical Applications

Low Power Oscillator



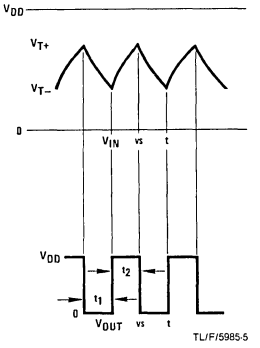
TL/F/5985-4

$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC \ln \frac{V_{DD} - V_{T-}}{V_{DD} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{DD} - V_{T-})}{V_{T-}(V_{DD} - V_{T+})}}$$

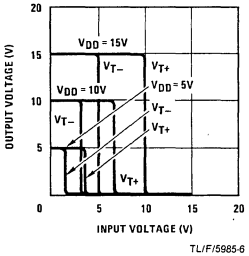
Note: The equations assume
$t_1 + t_2 >> t_{PHL} + t_{PLH}$



TL/F/5985-5

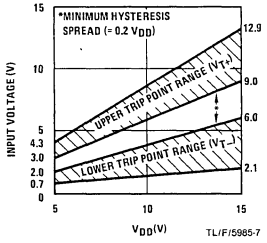
Typical Performance Characteristics

Typical Transfer Characteristics

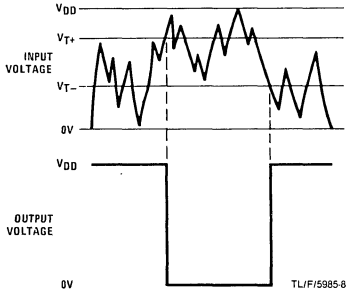


TL/F/5985-6

Guaranteed Trip Point Range



TL/F/5985-7



TL/F/5985-8

5

National Semiconductor

CD40160BM/CD40160BC Decade Counter with Asynchronous Clear
CD40161BM/CD40161BC Binary Counter with Asynchronous Clear
CD40162BM/CD40162BC Decade Counter with Synchronous Clear
CD40163BM/CD40163BC Binary Counter with Synchronous Clear

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the CD40162B and CD40163B is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the CD40160B and CD40161B is asynchronous and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

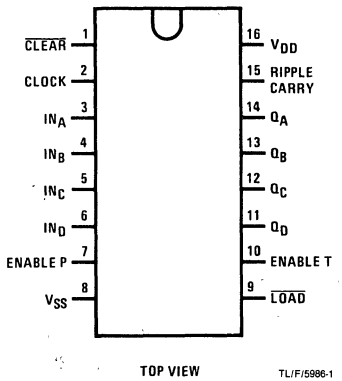
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable
- Equivalent to MC14160B, MC14161B, MC14162B, MC14163B
- Equivalent to MM74C160, MM74C161, MM74C162, MM74C163

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5986-1

Order Number CD40160BMJ, CD40160BCJ, CD40161BMJ, CD40161BCJ, CD40162BMJ, CD40162BCJ, CD40163BMJ or CD40163BCJ
See NS Package J16A

Order Number CD40160BMN, CD40160BCN, CD40161BMN, CD40161BCN, CD40162BMN, CD40162BCN, CD40163BMN or CD40163BCN
See NS Package N16E

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40XXXBM	−55°C to +125°C
CD40XXXBC	−40°C to +85°C

DC Electrical Characteristics CD40160BM/CD40161BM/CD40162BM/CD40163BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics CD40160BC/CD40161BC/CD40162BC/CD40163BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Cont'd.) CD40160BC/CD40161BC/CD40162BC/CD40163BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

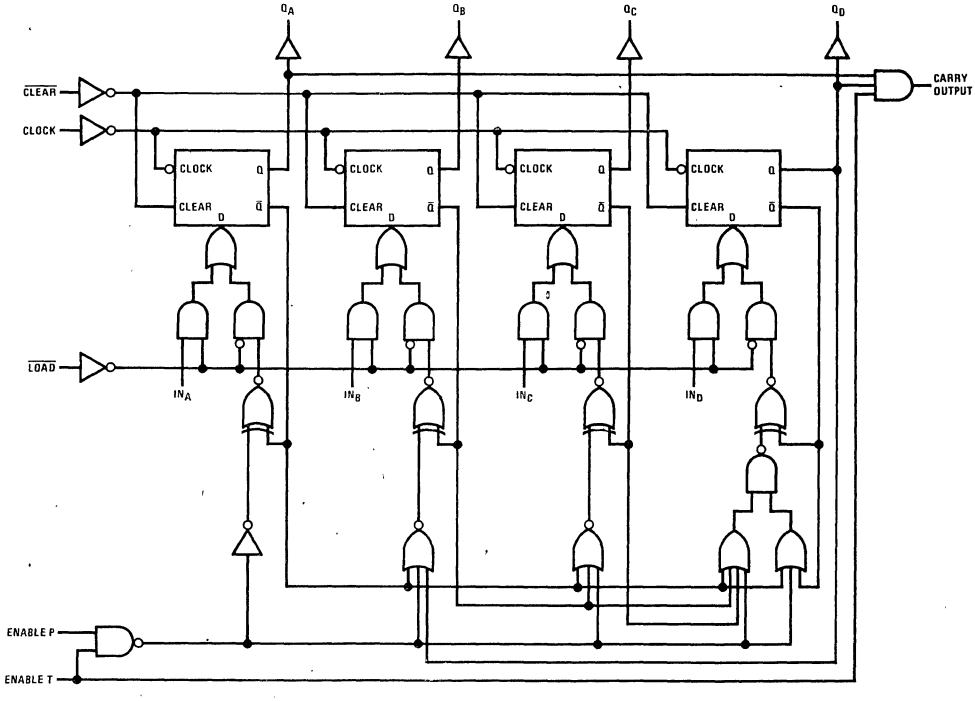
Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Q	V_{DD} = 5V		250	400	ns
		V_{DD} = 10V		100	160	ns
		V_{DD} = 15V		80	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Carry Out	V_{DD} = 5V		290	450	ns
		V_{DD} = 10V		120	190	ns
		V_{DD} = 15V		100	160	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From T Enable to Carry Out	V_{DD} = 5V		180	290	ns
		V_{DD} = 10V		70	130	ns
		V_{DD} = 15V		60	110	ns
t_{PHL}	Propagation Time From Clear to Q (CD40160B, CD40161B Only)	V_{DD} = 5V		190	300	ns
		V_{DD} = 10V		80	150	ns
		V_{DD} = 15V		70	120	ns
t_{SU}	Minimum Time Prior to Clock that Data or Load must be Present	V_{DD} = 5V		120		ns
		V_{DD} = 10V		30		ns
		V_{DD} = 15V		25		ns
t_{SU}	Minimum Time Prior to Clock that Enable P or T must be Present	V_{DD} = 5V		170	280	ns
		V_{DD} = 10V		70	120	ns
		V_{DD} = 15V		60	100	ns
t_{SU}	Minimum Time Prior to Clock that Clear must be Present (CD40162B, CD40163B Only)	V_{DD} = 5V		120	190	ns
		V_{DD} = 10V		50	80	ns
		V_{DD} = 15V		40	70	ns
t_{WL} or t_{WH}	Maximum Clock Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		45	90	ns
		V_{DD} = 15V		35	70	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise or Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			5.0	μs
		V_{DD} = 15V			5.0	μs
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2	4		MHz
		V_{DD} = 10V	5.5	11		MHz
		V_{DD} = 15V	7	14		MHz
t_{THL} or t_{TLH}	Transition Time	All Outputs				
		V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		95		pF

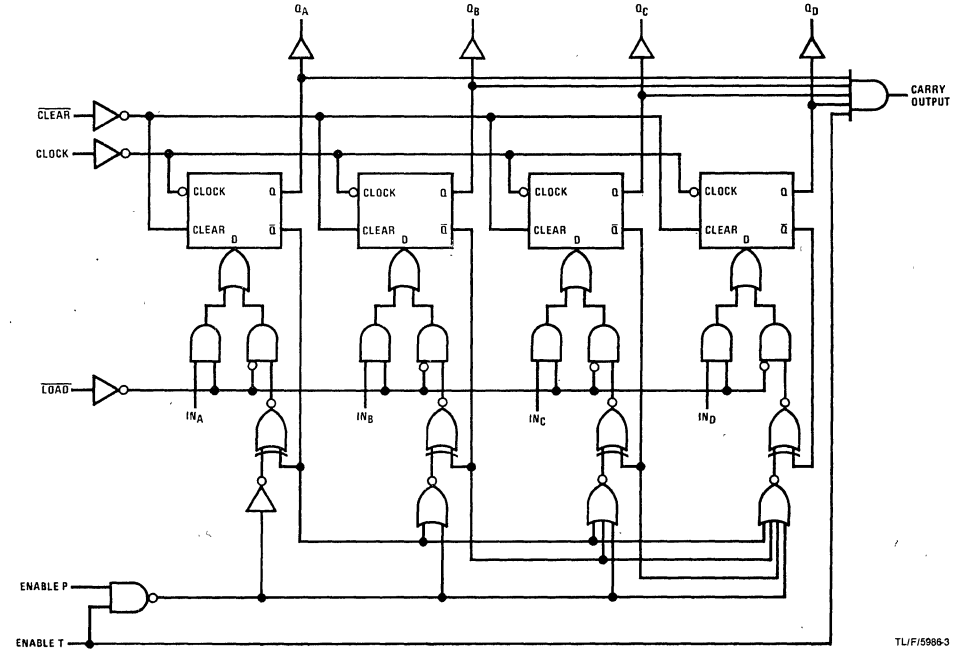
Logic Diagram

CD40160B, CD40162B Clear is Synchronous for the CD40162B



TL/F/5986-2

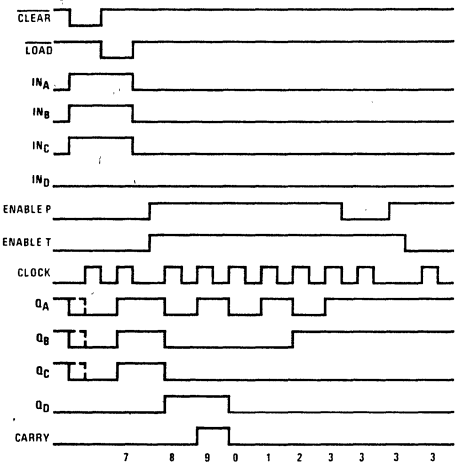
CD40161B, CD40163B Clear is Synchronous for the CD40163B



TL/F/5986-3

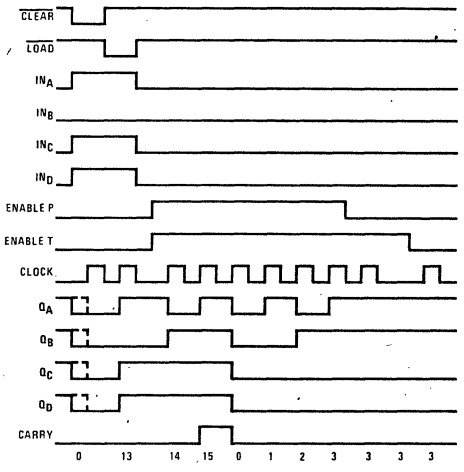
Logic Waveforms

CD40160B, --- CD40162B Decade Counters



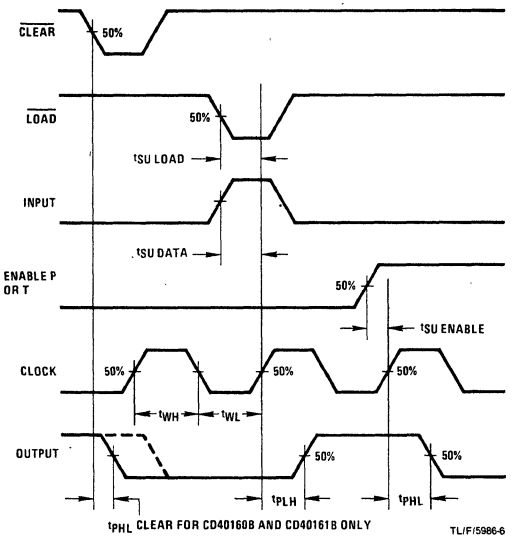
TL/F/5986-4

CD40161B, --- CD40163B Binary Counters



TL/F/5986-5

Switching Time Waveforms

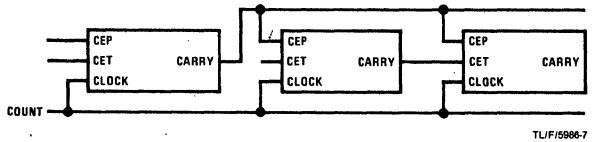


TL/F/5986-6

Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f = 20$ ns PRR $\leq$ 1 MHz duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

Cascading Packages



TL/F/5986-7

National Semiconductor

CD40174BM/CD40174BC Hex D Flip-Flop
CD40175BM/CD40175BC Quad D Flip-Flop

General Description

The CD40174B consists of six positive-edge triggered D-type flip-flops; the true output from each flip-flop are externally available. The CD40175B consists of four positive-edge triggered D-type flip-flops; both the true and complement outputs from each flip-flop are externally available.

All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all Q outputs to logical "0" and $\overline{Q}$'s (CD40175B only) to logical "1,"

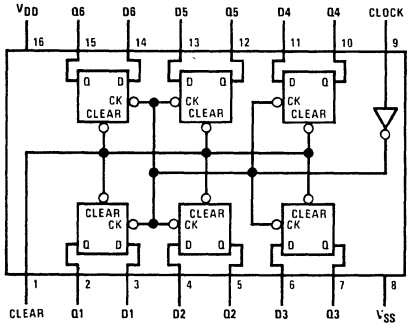
All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Equivalent to MC14174B, MC14175B
- Equivalent to MM74C174, MM74C175

Connection Diagrams

CD40174B
Dual-In-Line Package



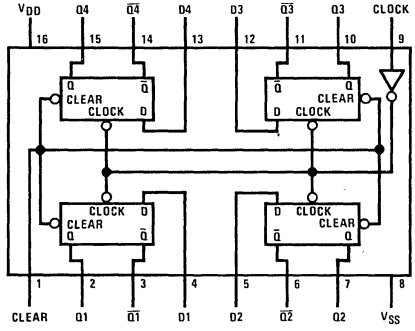
TOP VIEW

TL/F/5987-1

Order Number CD40174BMJ, CD40174BCJ, CD40175BMJ or CD40175BCJ
See NS Package J16A

Order Number CD40174BMN, CD40174BCN, CD40175BMN or CD40175BCN
See NS Package N16E

CD40175B
Dual-In-Line Package



TOP VIEW

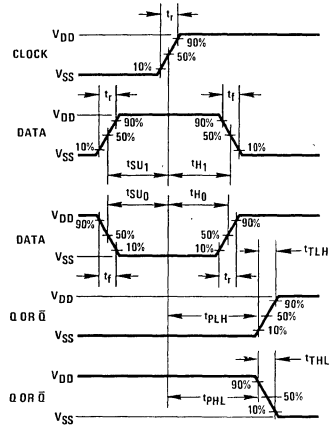
TL/F/5987-2

Truth Table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change
* = $\overline{Q}$ for CD40175B only

Switching Time Waveforms



$t_r = t_f = 20$ ns

TL/F/5987-3

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40XXXBM	−55°C to +125°C
CD40XXXBC	−40°C to +85°C

DC Electrical Characteristics CD40174BM/CD40175BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1.0			1.0		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2.0			2.0		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD40174BC/CD40175BC/ (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4			4		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8			8		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16			16		120	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.41	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, $R_L = 200k$, and $t_r = t_f = 20ns$, unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$ (CD40175 Only)	$V_{DD} = 5V$		190	300	ns
		$V_{DD} = 10V$		75	110	ns
		$V_{DD} = 15V$		60	90	ns
t_{PHL}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{DD} = 5V$		180	300	ns
		$V_{DD} = 10V$		70	110	ns
		$V_{DD} = 15V$		60	90	ns
t_{PLH}	Propagation Delay Time to a Logical "1" from Clear to $\overline{Q}$ (CD40175 Only)	$V_{DD} = 5V$		230	400	ns
		$V_{DD} = 10V$		90	150	ns
		$V_{DD} = 15V$		75	120	ns
t_{SU}	Time Prior to Clock Pulse that Data must be Present	$V_{DD} = 5V$	100	45		ns
		$V_{DD} = 10V$	40	16		ns
		$V_{DD} = 15V$	35	13		ns
t_H	Time after Clock Pulse that Data must be Held	$V_{DD} = 5V$		−11	0	ns
		$V_{DD} = 10V$		−4	0	ns
		$V_{DD} = 15V$		−3	0	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WH}, t_{WL}	Minimum Clock Pulse Width	$V_{DD} = 5V$		130	250	ns
		$V_{DD} = 10V$		45	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}	Minimum Clear Pulse Width	$V_{DD} = 5V$		120	250	ns
		$V_{DD} = 10V$		45	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{RCL}	Maximum Clock Rise Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	5.0			μs
		$V_{DD} = 15V$	5.0			μs
t_{fCL}	Maximum Clock Fall Time	$V_{DD} = 5V$	15	50		μs
		$V_{DD} = 10V$	5.0	50		μs
		$V_{DD} = 15V$	5	50		μs
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.0	3.5		MHz
		$V_{DD} = 10V$	5.0	10		MHz
		$V_{DD} = 15V$	6.0	12		MHz
C_{IN}	Input Capacitance	Clear Input,		10	15	pF
		Other Input		5.0	7.5	pF
C_{PD}	Power Dissipation	Per Package, (Note 4)		130		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

National Semiconductor

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter

General Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The CD40192BM and CD40192BC are BCD counters. While the CD40193BM and CD40193BC are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

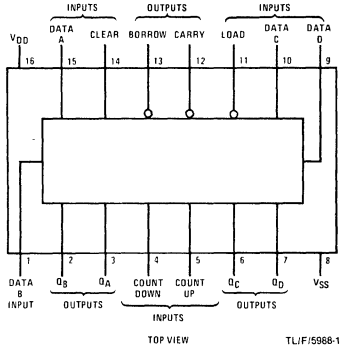
All inputs are protected against damage due to static discharge by clamps to V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Carry and borrow outputs for easy expansion to N-bit by cascading
- Asynchronous clear
- Equivalent to — MM54C192/MM74C192 and MM54C193/MM74C193

Connection Diagram

Dual-In-Line Package

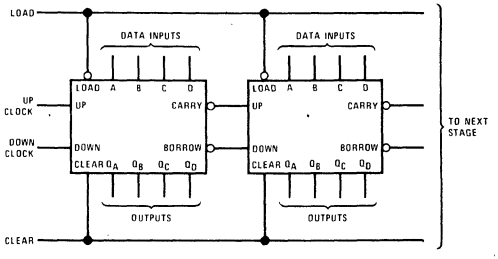


TOP VIEW TL/F/5988-1

Order Number CD40192BMJ, CD40192BCJ, CD40193BMJ or CD40193BCJ
See NS Package J16A

Order Number CD40192BMN, CD40192BCN, CD40193BMN or CD40193BCN
See NS Package N16E

Cascading Packages



TL/F/5988-2

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40192BM, CD40193BM	−55°C to +125°C
CD40192BC, CD40193BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) CD40192BM/CD40193BM

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics (Note 2) CD40192BC/CD40193BC

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, Input $t_r = t_f = 20\,ns$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH} or t_{PHL}	Propagation Delay Time From Count Up Or Count Down To Q	$V_{DD} = 5V$		250	400	ns
		$V_{DD} = 10V$		100	160	ns
		$V_{DD} = 15V$		80	130	ns
t_{PLH} or t_{PHL}	Propagation Delay Time From Count Up To Carry	$V_{DD} = 5V$		120	200	ns
		$V_{DD} = 10V$		50	80	ns
		$V_{DD} = 15V$		40	65	ns
t_{PLH} or t_{PHL}	Propagation Delay Time From Count Down To Borrow	$V_{DD} = 5V$		120	200	ns
		$V_{DD} = 10V$		50	80	ns
		$V_{DD} = 15V$		40	65	ns
t_{SU}	Time Prior To Load That Data Must Be Present	$V_{DD} = 5V$		100	160	ns
		$V_{DD} = 10V$		30	50	ns
		$V_{DD} = 15V$		25	40	ns
t_{PHL}	Propagation Delay Time From Clear To Q	$V_{DD} = 5V$		130	220	ns
		$V_{DD} = 10V$		60	100	ns
		$V_{DD} = 15V$		50	80	ns
t_{PLH} or t_{PHL}	Propagation Delay Time From Load To Q	$V_{DD} = 5V$		300	480	ns
		$V_{DD} = 10V$		120	190	ns
		$V_{DD} = 15V$		95	150	ns
t_{TLH} or t_{THL}	Output Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Count Frequency	$V_{DD} = 5V$	2.5	4		MHz
		$V_{DD} = 10V$	6	10		MHz
		$V_{DD} = 15V$	7.5	12.5		MHz
t_{RCL} or t_{fCL}	Maximum Count Rise Or Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	5			μs
		$V_{DD} = 15V$	1			μs
t_{WH}, t_{WL}	Minimum Count Pulse Width	$V_{DD} = 5V$		120	200	ns
		$V_{DD} = 10V$		35	80	ns
		$V_{DD} = 15V$		28	65	ns
t_{WH}	Minimum Clear Pulse Width	$V_{DD} = 5V$		300	480	ns
		$V_{DD} = 10V$		120	190	ns
		$V_{DD} = 15V$		95	150	ns
t_{WL}	Minimum Load Pulse Width	$V_{DD} = 5V$		100	160	ns
		$V_{DD} = 10V$		40	65	ns
		$V_{DD} = 15V$		32	55	ns
C_{IN}	Average Input Capacitance	Load and Data Inputs (A,B,C,D)		5	7.5	pF
		Count Up, Count Down and Clear		10	15	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

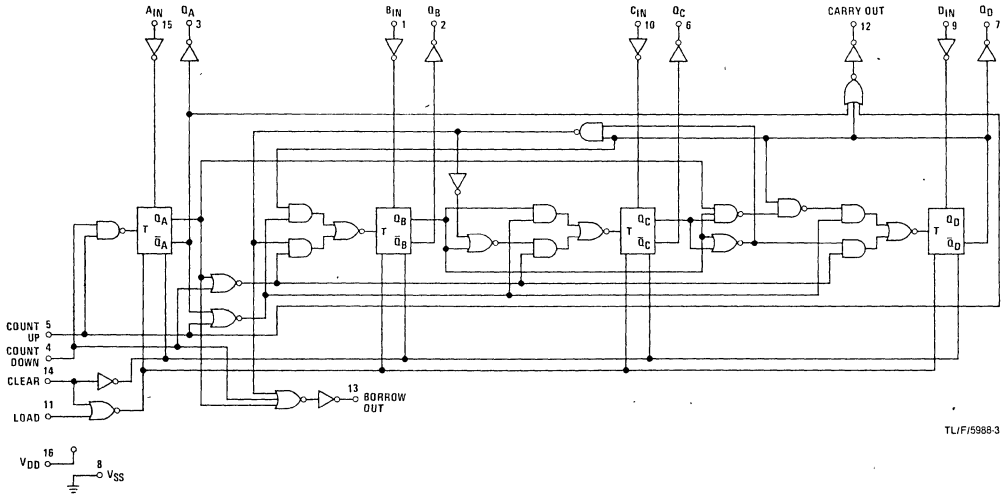
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

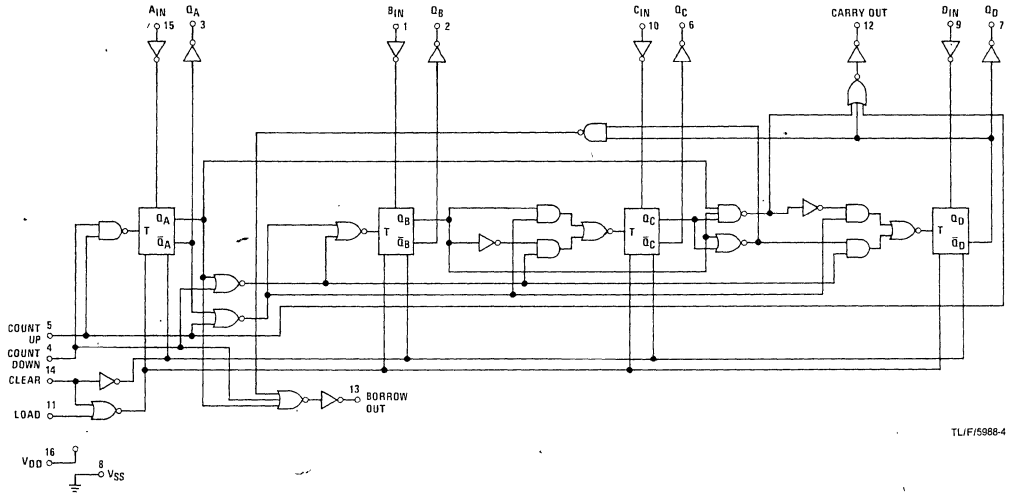
Note 4: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Schematic Diagrams

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter



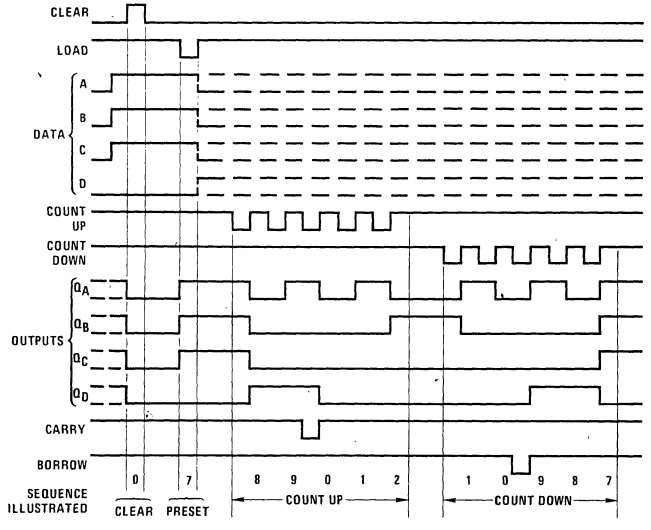
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter



5

Timing Diagrams

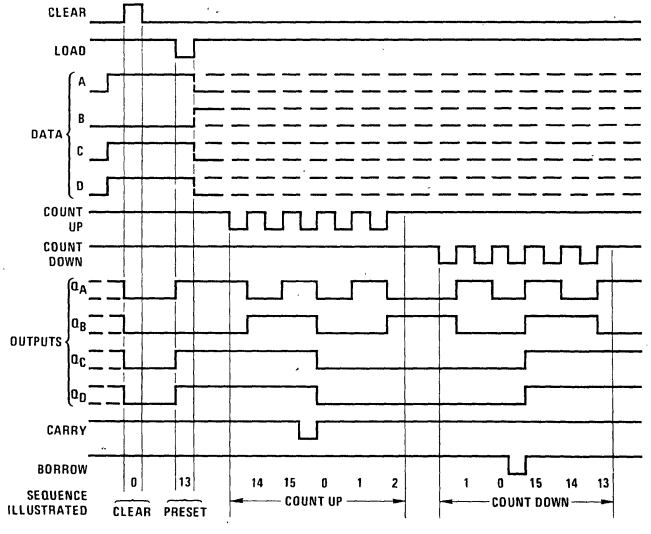
CD40192BM/CD40192BC



TL/F/5988-5

Sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one and two.
4. Count down to one, zero, borrow, nine, eight and seven.

CD40193BM/CD40193BC



TL/F/5988-6

Sequence:
1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one and two.
4. Count down to one, zero, borrow, fifteen, fourteen and thirteen.

National Semiconductor

CD4503BM/CD4503BC Hex Non-Inverting TRI-STATE® Buffer

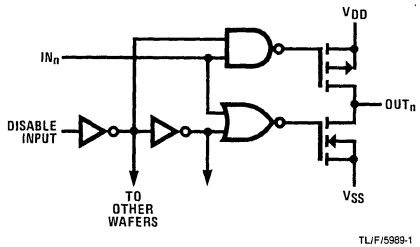
General Description

The CD4503B is a hex non-inverting TRI-STATE buffer with high output current sink and source capability. TRI-STATE outputs make it useful in bus-oriented applications. Two separate disable inputs are provided. Buffers 1 through 4 are controlled by the disable 4 input. Buffers 5 and 6 are controlled by the disable 2 input. A high level on either disable input will cause those gates on its control line to go into a high impedance state.

Features

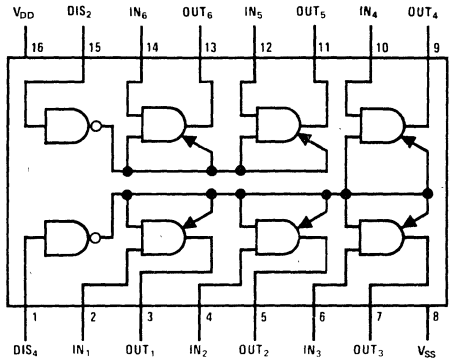
- Wide supply voltage range 3.0 V_{DC} to 18 V_{DC}
- TRI-STATE outputs
- Symmetrical turn on/turn off delays
- Symmetrical output rise and fall times
- Pin-for-pin replacement for MM80C97 and MC14503

Schematic and Connection Diagrams



TL/F/5989-1

Dual-In-Line Package



TL/F/5989-2

TOP VIEW

Order Number CD4503BMJ or CD4503BCJ
See NS Package J16A

Order Number CD4503BMN or CD4503BCN
See NS Package N16E

Truth Table

In	Disable Input	Out
0	0	0
1	0	1
X	1	TRI-STATE

X = Don't Care

5

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} – Supply Voltage	−0.5V to +18V
V_{IN} – Input Voltage	−0.5V to +0.5V
T_S – Storage Temperature Range	−65°C to +150°C
P_D – Power Dissipation	500 mW
T_L – Lead Temperature (soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} – Supply Voltage	3V to 15V
T_A – Operating Temperature Range	
CD4503BM	−55°C to +125°C
CD4503BC	−40°C to +85°C

DC Electrical Characteristics CD4503BM (Note 2)

Sym	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1			1		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2			2		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4			4		120	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD} or 0								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{DD} or 0								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V or 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V or 1.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V or 1.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 4.5V, V_{OL} = 0.4V	2.80		2.30	2.55		1.60		mA
		V_{DD} = 5.0V, V_{OL} = 0.4V	3.00		2.40	2.75		1.75		mA
		V_{DD} = 10V, V_{OL} = 0.5V	7.85		6.35	7.00		4.45		mA
		V_{DD} = 15V, V_{OL} = 1.5V	19.95		16.10	25.00		11.30		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_{OH} = 4.6V	−1.28		−1.02	−1.76		−0.72		mA
		V_{DD} = 10V, V_{OH} = 9.5V	−3.20		−2.60	−4.5		−1.8		mA
		V_{DD} = 15V, V_{OH} = 13.5V	−8.20		−6.80	−17.6		−4.8		mA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15V		±0.1		$\pm 10^{-4}$	±0.1		±1.0	μA
I_{IN}	Input Current	V_{DD} = 15V		±0.1		$\pm 10^{-4}$	±0.1		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

DC Electrical Characteristics CD4503BC (Note 2)

Sym	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4			4		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8			8		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16			16		120	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD} or 0								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{DD} or 0								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V or 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V or 1.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V or 1.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 4.5V, V_{OL} = 0.4V	2.30		1.95	2.65		1.60		mA
		V_{DD} = 5.0V, V_{OL} = 0.4V	2.5		2.10	2.75		1.75		mA
		V_{DD} = 10V, V_{OL} = 0.5V	6.5		5.45	7.0		4.45		mA
		V_{DD} = 15V, V_{OL} = 1.5V	16.50		13.80	25.00		11.30		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_{OH} = 4.6V	−1.04		−0.88	−1.76		−0.7		mA
		V_{DD} = 10V, V_{OH} = 9.5V	−2.60		−2.2	−4.50		−1.8		mA
		V_{DD} = 15V, V_{OH} = 13.5V	−7.2		−6.0	−17.6		−4.8		mA
I_{TL}	TRI-STATE Leakage Current	V_{DD} = 15V		±0.3		$±10^{-4}$	±0.3		±1.0	μA
I_{IN}	Input Current	V_{DD} = 15V		±0.3		$±10^{-5}$	±0.3		±1.0	μA

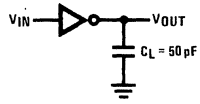
AC Electrical Characteristics CD4503B

T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, Input t_r = t_f = 20 ns, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		75	100	ns
		V_{DD} = 10V		35	40	ns
		V_{DD} = 15V		25	30	ns
t_{PLZ}, t_{PHZ}	Propagation Delay Time, Logical Level to High Impedance State	V_{DD} = 5V		80	125	ns
		V_{DD} = 10V		40	90	ns
		V_{DD} = 15V		35	70	ns
t_{PZL}, t_{PZH}	Propagation Delay Time, High Impedance State to Logical Level	V_{DD} = 5V		95	175	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		35	70	ns
t_{TLH}	Output Rise Time	V_{DD} = 5V		45	80	ns
		V_{DD} = 10V		23	40	ns
		V_{DD} = 15V		18	35	ns
t_{THL}	Output Fall Time	V_{DD} = 5V		45	80	ns
		V_{DD} = 10V		23	40	ns
		V_{DD} = 15V		18	35	ns

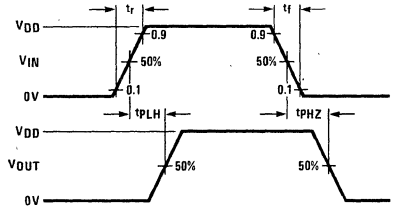
AC Test Circuits and Switching Time Waveforms

t_{PHL}, t_{PLH}



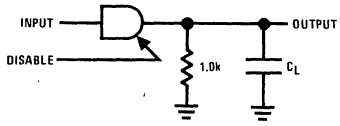
TL/F/5989-3

CMOS to CMOS



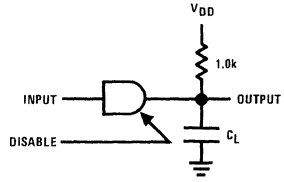
TL/F/5989-4

t_{PHZ} and t_{PZH}



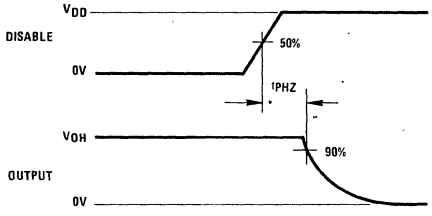
TL/F/5989-5

t_{PLZ} and t_{PZL}



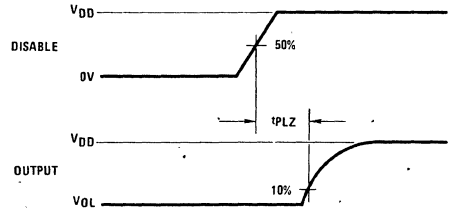
TL/F/5989-6

t_{PHZ}



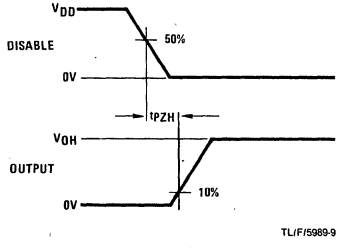
TL/F/5989-7

t_{PLZ}



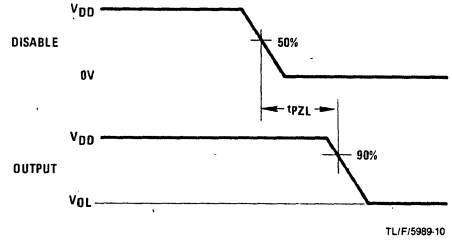
TL/F/5989-8

t_{PZH}



TL/F/5989-9

t_{PZL}



TL/F/5989-10

Note: Delays measured with input t_r, $t_f \leq 20$ ns.

National Semiconductor

CD4510BM/CD4510BC BCD Up/Down Counter
CD4516BM/CD4516BC Binary Up/Down Counter

General Description

The CD4510BM/CD4510BC and CD4516BM/CD4516BC are monolithic CMOS up/down counters which count in BCD and binary, respectively.

The counters count up when the up/down input is at logical "1" and vice versa. A logical "1" preset enable signal allows information at the parallel inputs to preset the counters to any state synchronously with the clock. The counters are advanced one count at the positive-going edge ofthe clock if the carry in, preset enable, and reset inputs are at logical "0". Advancement is inhibited when any of these three inputs are at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" when the counter reaches its maximum count in the "up" mode or its minimum count in the "down" mode, provided the carry input is at logical "0" state. The counters are cleared asynchronously by applying a logical "1" voltage level at the reset input.

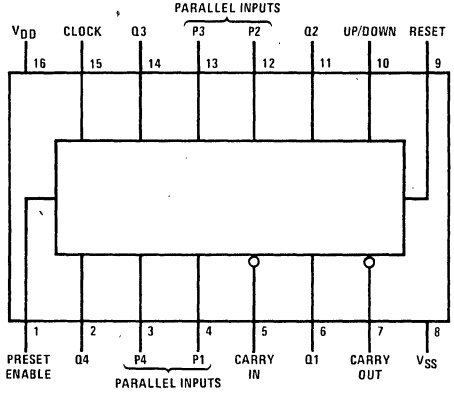
All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Parallel load "jam" inputs
- Low quiescent power dissipation — 0.25 μW/package (typ.) @ V_{CC} = 5.0 V
- Motorola MC14510, MC14516 second source

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5990-1

Order Number CD4510BMJ, CD4510BCJ, CD4516BMJ or CD4516BCJ
See NS Package J16A

Order Number CD4510BMN, CD4510BCN, CD4516BMN or CD4516BCN
See NS Package N16E

Truth Table

CLOCK	RESET	PRESET ENABLE	CARRY IN	UP/DOWN	OUTPUT FUNCTION
X	1	X	X	X	Reset to zero
X	0	1	X	X	Set to P1, P2, P3, P4
↗	0	0	0	1	Count up
↗	0	0	0	0	Count down
↘	0	0	X	X	No change
X	0	0	1	X	No change

↗ = positive transition
↘ = negative transition
X = don't care

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4510BM, CD4516BM	−55°C to +125°C
CD4510BC, CD4516BC	−40°C to +85°C

DC Electrical Characteristics CD4510BM/CD4516BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.05	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.1	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.15	20		600	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\|$ < 1 μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.8		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.0		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.8		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.0		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−7.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4510BC/CD4516BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.05	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.1	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.15	80		600	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0V, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4510BC/CD4516BC (Note 2)

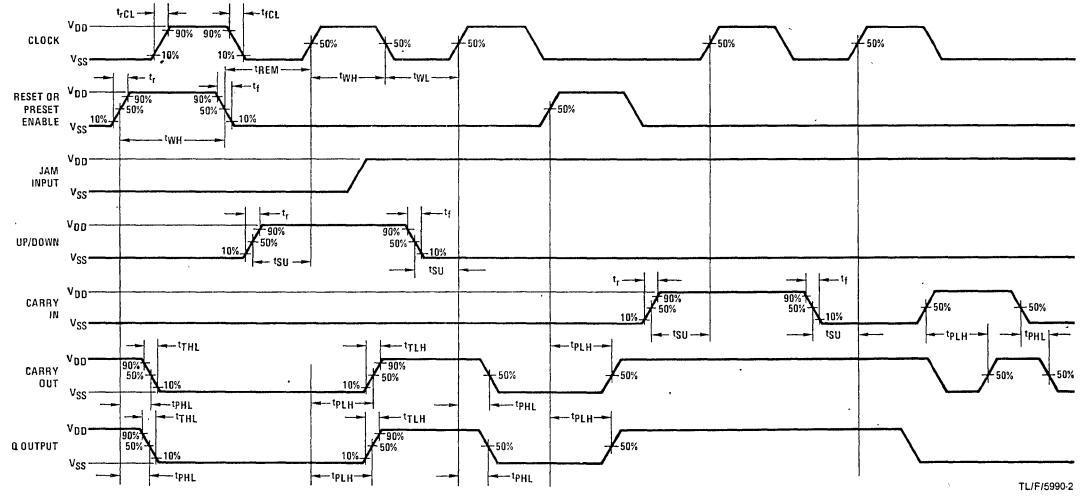
SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	(Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.8		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.0		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	7.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
	(Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.8		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.0		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−7.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Switching Time Waveforms



AC Electrical Characteristics CD4510BM/CD4510BC, CD4516BM/CD4516BC

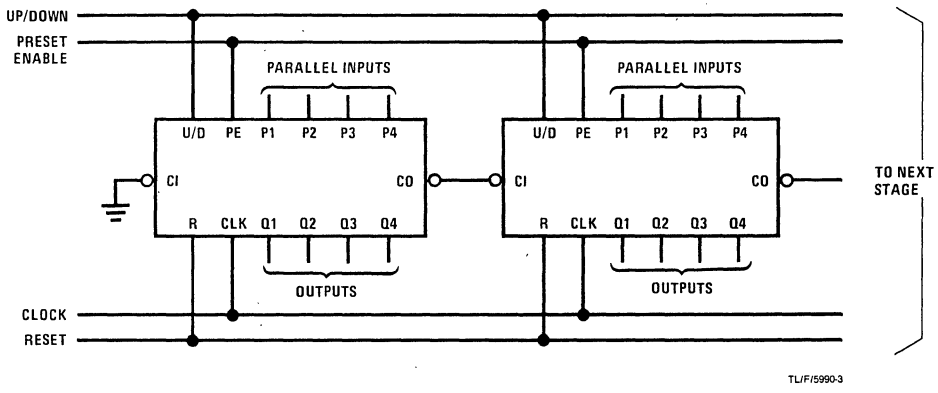
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_{rCL} = t_{fCL} = t_r = t_f = 20$ ns, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q Outputs	$V_{DD} = 5V$		220	500	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Carry Output	$V_{DD} = 5V$		315	630	ns
		$V_{DD} = 10V$		130	260	ns
		$V_{DD} = 15V$		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q and Carry Outputs	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		160	315	ns
		$V_{DD} = 10V$		65	130	ns
		$V_{DD} = 15V$		50	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	15			μs
		$V_{DD} = 15V$	15			μs
t_{SU}	Minimum Carry In Set-Up Time	$V_{DD} = 5V$		100	220	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		35	70	ns
t_{SU}	Minimum Up/Down Set-Up Time	$V_{DD} = 5V$		200	420	ns
		$V_{DD} = 10V$		70	170	ns
		$V_{DD} = 15V$		60	150	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	3.1		MHz
		$V_{DD} = 10V$	3.8	7.6		MHz
		$V_{DD} = 15V$	5.0	10.0		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)	Per Package,		65		pF
RESET/PRESET ENABLE OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Q Output	$V_{DD} = 5V$		285	570	ns
		$V_{DD} = 10V$		115	230	ns
		$V_{DD} = 15V$		95	195	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Carry Output	$V_{DD} = 5V$		420	860	ns
		$V_{DD} = 10V$		170	350	ns
		$V_{DD} = 15V$		140	290	ns
t_{WH}	Minimum Reset/Preset Enable Pulse Width	$V_{DD} = 5V$		90	200	ns
		$V_{DD} = 10V$		40	100	ns
		$V_{DD} = 15V$		35	80	ns
t_{REM}	Minimum Reset/Preset Enable Removal Time	$V_{DD} = 5V$		170	330	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		60	120	ns
CARRY INPUT OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry In to Carry Output	$V_{DD} = 5V$		260	500	ns
		$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		90	180	ns

Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L)V_{DD}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; P_Q = Quiescent Power Dissipation. For further details, see application note AN-90, "54C/74C Family characteristics."

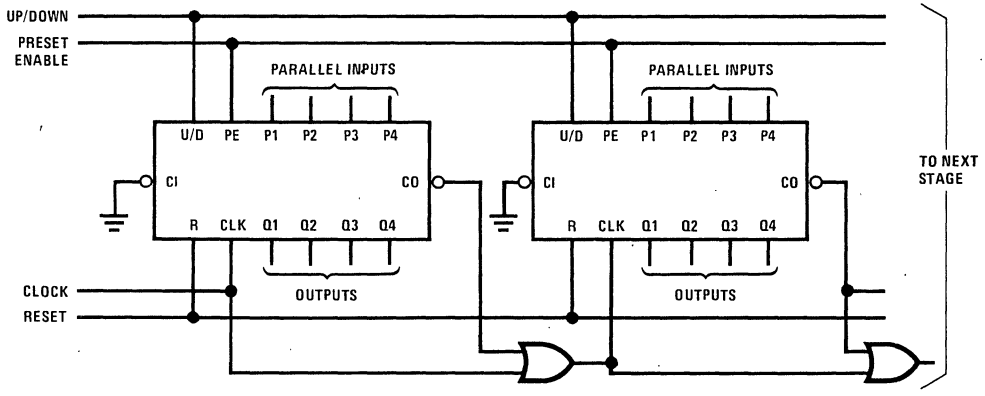
Cascading Packages

Parallel Clocking



TL/F/5990-3

Ripple Clocking



TL/F/5990-4

Schematic Diagrams

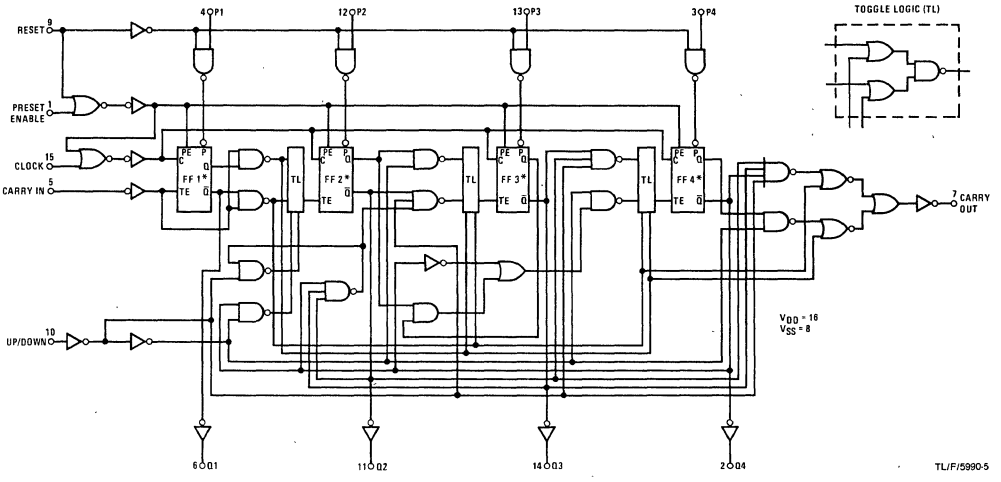
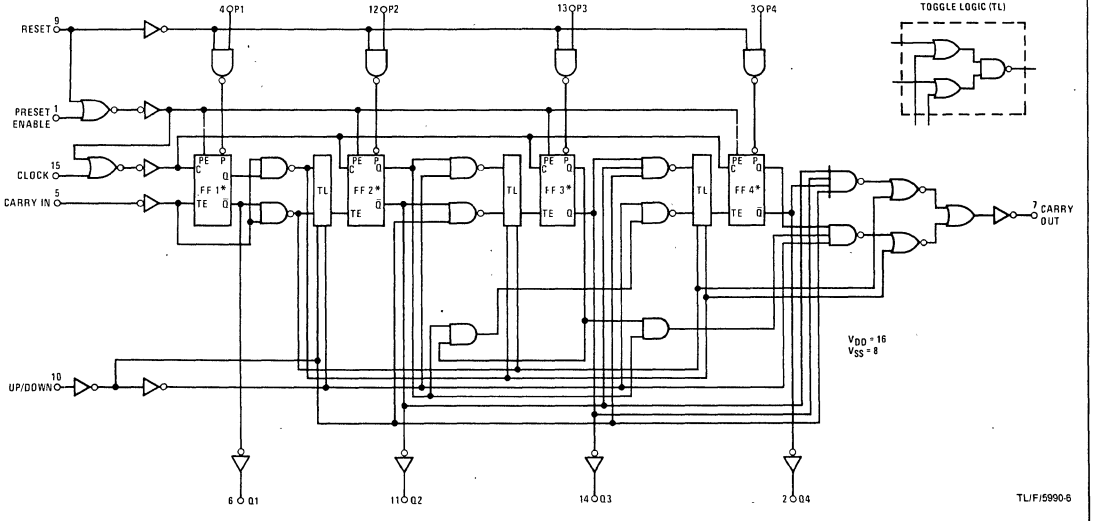


FIGURE 1. CD4510

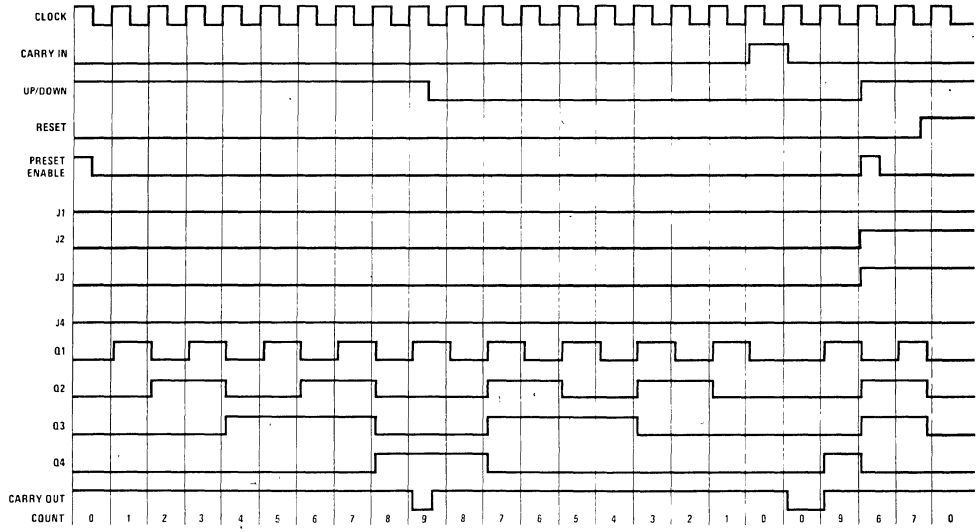


*Flip-flop toggles at the positive-going edge of clock (C) if Toggle Enable (TE) is at logical "1" and Preset Enable (PE) is at logical "0"

FIGURE 2. CD4516

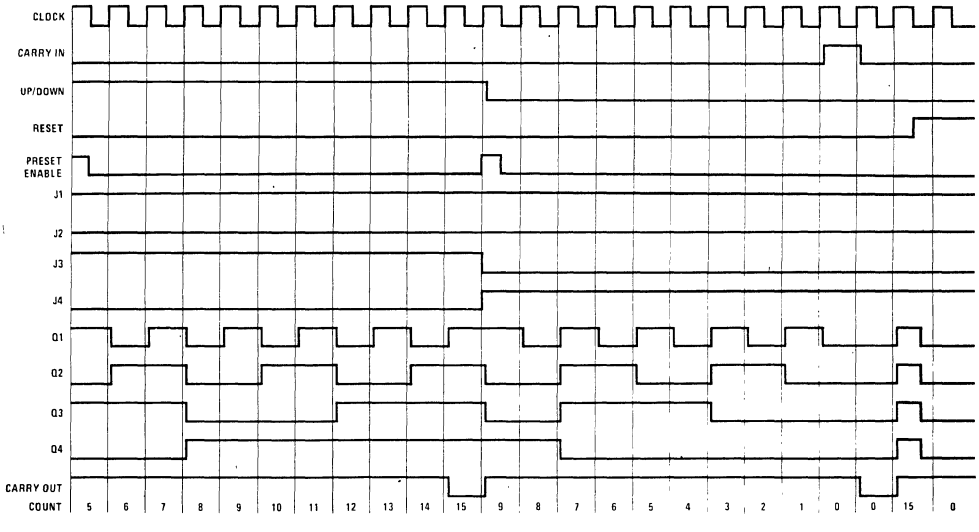
Logic Waveforms

CD4510BM/CD4510BC



TL/F/5990-7

CD4516BM/CD4516BC



TL/F/5990-8

5

National Semiconductor

CD4511BM/CD4511BC BCD-to-7 Segment Latch/Decoder/Driver

General Description

The CD4511BM/CD4511BC BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

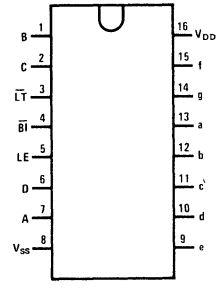
Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

Features

- Low logic circuit power dissipation
- High current sourcing outputs (up to 25mA)
- Latch storage of code
- Blanking input
- Lamp test provision
- Readout blanking on all illegal input combinations
- Lamp intensity modulation capability
- Time share (multiplexing) facility
- Equivalent to Motorola MC14511

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5991-1

Order Number CD4511BMJ or CD4511BCJ
See NS Package J16A

Order Number CD4511BMN or CD4511BCN
See NS Package N16E

Segment Identification

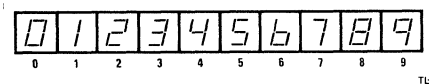
TL/F/5991-3

Truth Table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	B
X	0	1	X	X	X	X	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	X	X	X	X				*				*

X = Don't care
*Depends upon the BCD code applied during the 0 to 1 transition of LE

Display



TL/F/5991-2

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4510BM, CD4516BM	−55°C to +125°C
CD4510BC, CD4516BC	−40°C to +85°C

DC Electrical Characteristics CD4511BM

Sym	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Supply Current	$V_{DD}=5V$, $V_{IN}=V_{DD}$ or V_{SS}		5			5		150	μA
		$V_{DD}=10V$, $V_{IN}=V_{DD}$ or V_{SS}		10			10		300	μA
		$V_{DD}=15V$, $V_{IN}=V_{DD}$ or V_{SS}		20			20		600	μA
V_{OL}	Output Voltage Logical "0" Level	$V_{DD}=5V$		0.01		0	0.01		0.05	V
		$V_{DD}=10V$		0.01		0	0.01		0.05	V
		$V_{DD}=15V$				0				V
V_{OH}	Output Voltage Logical "1" Level	$V_{DD}=5V$	4.1		4.1	4.57		4.1		V
		$V_{DD}=10V$	9.1		9.1	9.58		9.1		V
		$V_{DD}=15V$	14.1		14.1	14.59		14.1		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_{OUT}=3.8V$ or 0.5V		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_{OUT}=8.8V$ or 1.0V		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_{OUT}=13.8V$ or 1.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_{OUT}=0.5V$ or 3.8V	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_{OUT}=1.0V$ or 8.8V	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_{OUT}=1.5V$ or 13.8V	11.0		11.0	9		11.0		V
V_{OH}	Output (Source) Drive Voltage	$V_{DD}=5V$, $I_{OH}=0$ mA	4.1		4.1	4.57		4.1		V
		$V_{DD}=5V$, $I_{OH}=5$ mA				4.24				V
		$V_{DD}=5V$, $I_{OH}=10$ mA	3.9		3.9	4.12		3.5		V
		$V_{DD}=5V$, $I_{OH}=15$ mA				3.94				V
		$V_{DD}=5V$, $I_{OH}=20$ mA	3.4		3.4	3.75		3.0		V
		$V_{DD}=5V$, $I_{OH}=25$ mA				3.54				V
		$V_{DD}=10V$, $I_{OH}=0$ mA	9.1		9.1	9.58		9.1		V
		$V_{DD}=10V$, $I_{OH}=5$ mA				9.26				V
		$V_{DD}=10V$, $I_{OH}=10$ mA	9.0		9.0	9.17		8.6		V
		$V_{DD}=10V$, $I_{OH}=15$ mA				9.04				V
		$V_{DD}=10V$, $I_{OH}=20$ mA	8.6		8.6	8.9		8.2		V
		$V_{DD}=10V$, $I_{OH}=25$ mA				8.75				V
		$V_{DD}=15V$, $I_{OH}=0$ mA	14.1		14.1	14.59		14.1		V
		$V_{DD}=15V$, $I_{OH}=5$ mA				14.27				V
		$V_{DD}=15V$, $I_{OH}=10$ mA	14.0		14.0	14.18		13.6		V
		$V_{DD}=15V$, $I_{OH}=15$ mA				14.07				V
		$V_{DD}=15V$, $I_{OH}=20$ mA	13.6		13.6	13.95		13.2		V
		$V_{DD}=15V$, $I_{OH}=25$ mA				13.8				V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_{OL}=0.4V$	0.64		0.51	0.88		0.36		mA
		$V_{DD}=10V$, $V_{OL}=0.5V$	1.6		1.3	2.25		0.9		mA
		$V_{DD}=15V$, $V_{OL}=1.5V$	4.2		3.4	8.8		2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.10		10^{-5}	0.10		1.0	μA

Note 1: Devices should not be connected with power on.

DC Electrical Characteristics CD4511BC

Sym	Parameter	Conditions	−40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Supply Current	$V_{DD}=5V$		20			20		150	μA
		$V_{DD}=10V$		40			40		300	μA
		$V_{DD}=15V$		80			80		600	μA
V_{OL}	Output Voltage Logical "0" Level	$V_{DD}=5V$		0.01		0	0.01		0.05	V
		$V_{DD}=10V$		0.01		0	0.01		0.05	V
		$V_{DD}=15V$				0				V
V_{OH}	Output Voltage Logical "1" Level	$V_{DD}=5V$	4.1		4.1	4.57		4.1		V
		$V_{DD}=10V$	9.1		9.1	9.58		9.1		V
		$V_{DD}=15V$	14.1		14.1	14.59		14.1		V
V_{IL}	Low Level Input Voltage	$V_{DD}=5V$, $V_{OUT}=3.8V$ or $0.5V$		1.5		2	1.5		1.5	V
		$V_{DD}=10V$, $V_{OUT}=8.8V$ or $1.0V$		3.0		4	3.0		3.0	V
		$V_{DD}=15V$, $V_{OUT}=13.8V$ or $1.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5V$, $V_{OUT}=0.5V$ or $3.8V$	3.5		3.5	3		3.5		V
		$V_{DD}=10V$, $V_{OUT}=1.0V$ or $8.8V$	7.0		7.0	6		7.0		V
		$V_{DD}=15V$, $V_{OUT}=1.5V$ or $13.8V$	11.0		11.0	9		11.0		V
V_{OH}	Output (Source) Drive Voltage	$V_{DD}=5V$, $I_{OH}=0$ mA	4.1		4.1	4.57		4.1		V
		$V_{DD}=5V$, $I_{OH}=5$ mA				4.24				V
		$V_{DD}=5V$, $I_{OH}=10$ mA	3.6		3.6	4.12		3.3		V
		$V_{DD}=5V$, $I_{OH}=15$ mA				3.94				V
		$V_{DD}=5V$, $I_{OH}=20$ mA	2.8		2.8	3.75		2.5		V
		$V_{DD}=5V$, $I_{OH}=25$ mA				3.54				V
		$V_{DD}=10V$, $I_{OH}=0$ mA	9.1		9.1	9.58		9.1		V
		$V_{DD}=10V$, $I_{OH}=5$ mA				9.26				V
		$V_{DD}=10V$, $I_{OH}=10$ mA	8.75		8.75	9.17		8.45		V
		$V_{DD}=10V$, $I_{OH}=15$ mA				9.04				V
		$V_{DD}=10V$, $I_{OH}=20$ mA	8.1		8.1	8.9		7.8		V
		$V_{DD}=10V$, $I_{OH}=25$ mA				8.75				V
		$V_{DD}=15V$, $I_{OH}=0$ mA	14.1		14.1	14.59		14.1		V
		$V_{DD}=15V$, $I_{OH}=5$ mA				14.27				V
		$V_{DD}=15V$, $I_{OH}=10$ mA	13.75		13.75	14.18		13.45		V
		$V_{DD}=15V$, $I_{OH}=15$ mA				14.07				V
		$V_{DD}=15V$, $I_{OH}=20$ mA	13.1		13.1	13.95		12.8		V
		$V_{DD}=15V$, $I_{OH}=25$ mA				13.8				V
I_{OL}	Low Level Output Current	$V_{DD}=5V$, $V_{OL}=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_{OL}=0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15V$, $V_{OL}=1.5V$	3.6		3.0	8.8		2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.30		-10^{-5}	−0.30		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics

$T_A = 25°C$ and $C_L = 50\,pF$, typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

SYM	PARAMETER	CONDITIONS	CD4511BX			UNITS
			MIN	TYP	MAX	
C_{IN}	Input Capacitance	$V_{IN} = 0$		5.0	7.5	pF
t_r	Output Rise Time *(Figure 1a)*	$V_{DD} = 5V$		40	80	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
t_f	Output Fall Time *(Figure 1a)*	$V_{DD} = 5V$		125	250	ns
		$V_{DD} = 10V$		75	150	ns
		$V_{DD} = 15V$		65	130	ns
t_{PLH}	Turn-Off Delay Time (Data) *(Figure 1a)*	$V_{DD} = 5V$		640	1280	ns
		$V_{DD} = 10V$		250	500	ns
		$V_{DD} = 15V$		175	350	ns
t_{PHL}	Turn-On Delay Time (Data) *(Figure 1a)*	$V_{DD} = 5V$		720	1440	ns
		$V_{DD} = 10V$		290	580	ns
		$V_{DD} = 15V$		195	400	ns
t_{PLH}	Turn-Off Delay Time (Blank) *(Figure 1a)*	$V_{DD} = 5V$		320	640	ns
		$V_{DD} = 10V$		130	260	ns
		$V_{DD} = 15V$		100	200	ns
t_{PHL}	Turn-On Delay Time (Blank) *(Figure 1a)*	$V_{DD} = 5V$		485	970	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{PHL}	Turn-Off Delay Time (Lamp Test) *(Figure 1a)*	$V_{DD} = 5V$		313	625	ns
		$V_{DD} = 10V$		125	250	ns
		$V_{DD} = 15V$		90	180	
t_{PHL}	Turn-On Delay Time (Lamp Test) *(Figure 1a)*	$V_{DD} = 5V$		313	625	ns
		$V_{DD} = 10V$		125	250	ns
		$V_{DD} = 15V$		90	180	ns
t_{SETUP}	Setup Time *(Figure 1b)*	$V_{DD} = 5V$	180	90		ns
		$V_{DD} = 10V$	76	38		ns
		$V_{DD} = 15V$	40	20		ns
t_{HOLD}	Hold Time *(Figure 1b)*	$V_{DD} = 5V$	0	−90		ns
		$V_{DD} = 10V$	0	−38		ns
		$V_{DD} = 15V$	0	−20		ns
PW_{LE}	Minimum Latch Enable Pulse Width *(Figure 1c)*	$V_{DD} = 5V$	520	260		ns
		$V_{DD} = 10V$	220	110		ns
		$V_{DD} = 15V$	130	65		ns

Switching Time Waveforms

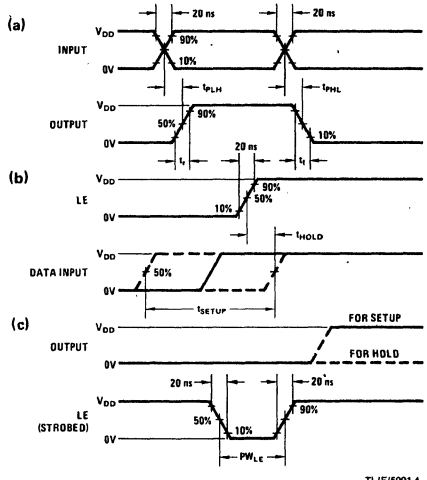
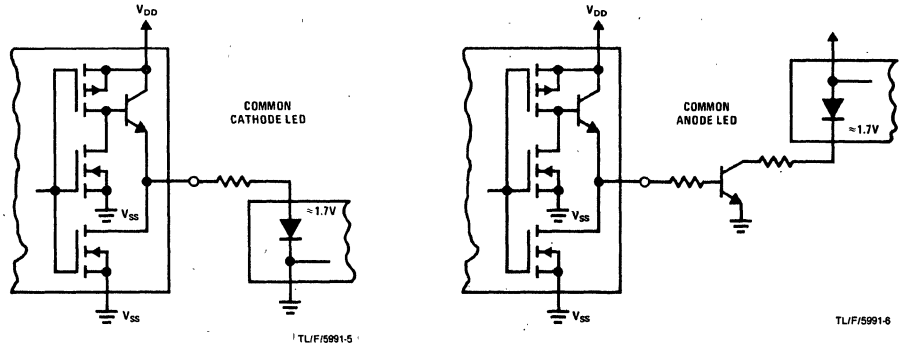


FIGURE 1.

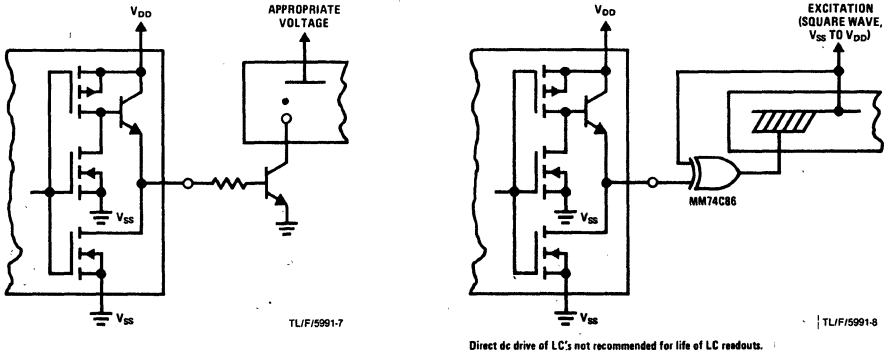
Typical Applications

Light Emitting Diode (LED) Readout



Gas Discharge Readout

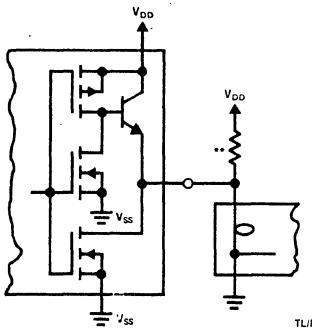
Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts.

Typical Applications (Cont'd.)

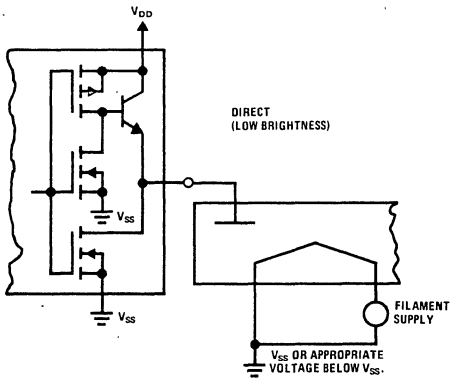
Incandescent Readout



TL/F/5991-9

**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Fluorescent Readout



TL/F/5991-10

5

National Semiconductor

CD4512BM/CD4512BC 8-Channel Buffered Data Selector

General Description

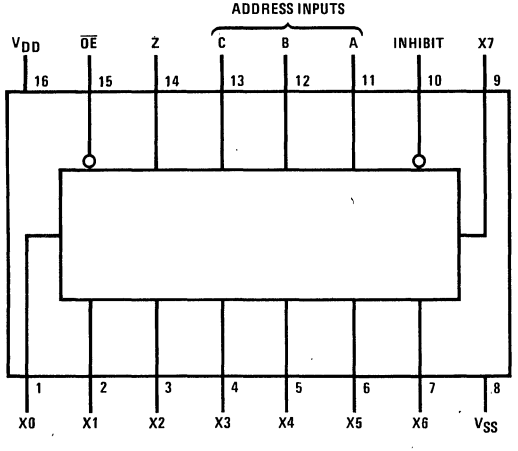
The CD4512BM/CD4512BC buffered 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N- and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a TRI-STATE® output. A high level at the Inhibit input forces a low level at the output. A high level at the Output Enable ($\overline{OE}$) input forces the output into the TRI-STATE condition. Low levels at both the Inhibit and ($\overline{OE}$) inputs allow normal operation.

Features

- Wide supply voltage range 3.0V-15V
- High noise immunity 0.45 V_{DD} (typ.)
- TRI-STATE output
- Low quiescent power dissipation 0.25 μW/package (typ.) @ $V_{CC} = 5.0V$
- Plug-in replacement for Motorola MC14512

Connection Diagram and Truth Table

Dual-In-Line Package



TOP VIEW

TL/F/5993-1

Order Number CD4512BMJ or CD4512BCJ
See NS Package J16A

Order Number CD4512BMN or CD4512BCN
See NS Package N16E

ADDRESS INPUTS			CONTROL INPUTS		OUTPUT
C	B	A	INHIBIT	$\overline{OE}$	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
Ø	Ø	Ø	1	0	0
Ø	Ø	Ø	Ø	1	Hi-Z

Ø = Don't care
Hi-Z = TRI-STATE condition
Xn = Data at input n

Absolute Maximum Ratings

(Notes 1 & 2)

V_{DD} Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3.0 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4512BM	−55°C to +125°C
CD4512BC	−40°C to +85°C

DC Electrical Characteristics CD4512BM (Note 2)

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5.0		0.005	5.0		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.010	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_{OL}\rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $\lvert I_{OL}\rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15 V, $\lvert I_{OL}\rvert$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_{OH}\rvert$ < 1 μA	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V, $\lvert I_{OH}\rvert$ < 1 μA	9.95		9.95	10.0		9.95		V
		V_{DD} = 15 V, $\lvert I_{OH}\rvert$ < 1 μA	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 9.0 V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15 V, V_O = 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.78		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.0		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 4.6 V	−0.25		−0.2			−0.14		mA
		V_{DD} = 10 V, V_O = 9.5 V	−0.62		−0.5			−0.35		mA
		V_{DD} = 15 V, V_O = 13.5 V	−1.8		−1.5			−1.1		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-}	0.1		1.0	μA
I_{OZ}	TRI-STATE Output Current	V_{DD} = 15V, V_O = 0 V		±0.1		-10^{-5}	±0.1		±3.0	μA
		V_{DD} = 15 V, V_O = 15 V				10^{-5}				μA

DC Electrical Characteristics CD4512BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.005	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.010	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_{OL}\rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $\lvert I_{OL}\rvert$ < 1 μA		0.05		0	0.05		0.05	V
		V_{DD} = 15 V, $\lvert I_{OL}\rvert$ < 1 μA		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5.0 V, $\lvert I_{OH}\rvert$ < 1 μA	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V, $\lvert I_{OH}\rvert$ < 1 μA	9.95		9.95	10.0		9.95		V
		V_{DD} = 15 V, $\lvert I_{OH}\rvert$ < 1 μA	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 9.0 V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics (cont'd) CD4512BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5.0V$, $V_O=0.4V$	0.52		0.44	0.78		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.0		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5.0V$, $V_O=2.5V$	−0.2		−0.16			−0.12		mA
		$V_{DD}=10V$, $V_O=9.5V$	−0.5		−0.4			−0.3		mA
		$V_{DD}=15V$, $V_O=113.5V$	−1.4		−1.2			−1.0		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	TRI-STATE Output Current	$V_{DD}=15V$, $V_O=0V$ or 15V		±1.0		$\pm10^{-5}$	±1.0		±7.5	μA

AC Electrical Characteristics $T_A=25°C$, $t_r=t_f=20$ ns, $C_L=50$ pF

Symbol	Parameter	Conditions	CD4512BM			CD4512BC			Units
			Min	Typ	Max	Min	Typ	Max	
t_{PHL}	Propagation Delay High-to-Low Level	$V_{DD}=5.0V$		225	500		225	750	ns
		$V_{DD}=10V$		75	175		75	200	ns
		$V_{DD}=15V$		57	130		57	150	ns
t_{PLH}	Propagation Delay Low-to-High Level	$V_{DD}=5.0V$		225	500		225	750	ns
		$V_{DD}=10V$		75	175		75	200	ns
		$V_{DD}=15V$		57	130		57	150	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD}=5.0V$		70	175		70	175	ns
		$V_{DD}=10V$		35	75		35	75	ns
		$V_{DD}=15V$		25	55		25	55	ns
t_{PHZ}, t_{PLZ}	Propagation Delay into TRI-STATE from Logic Level	$V_{DD}=5.0V$		50	125		50	125	ns
		$V_{DD}=10V$		25	75		25	75	ns
		$V_{DD}=15V$		19	60		19	60	ns
t_{PZH}, t_{PZL}	Propagation Delay to Logic Level from TRI-STATE	$V_{DD}=5.0V$		50	125		50	125	ns
		$V_{DD}=10V$		25	75		25	75	ns
		$V_{DD}=15V$		19	60		19	60	ns
C_{IN}	Input Capacitance	(Note 4)		7.5	15		7.5	15	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 4)		7.5	15		7.5	15	pF
C_{PD}	Power Dissipation Capacity	(Note 5)		150			150		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

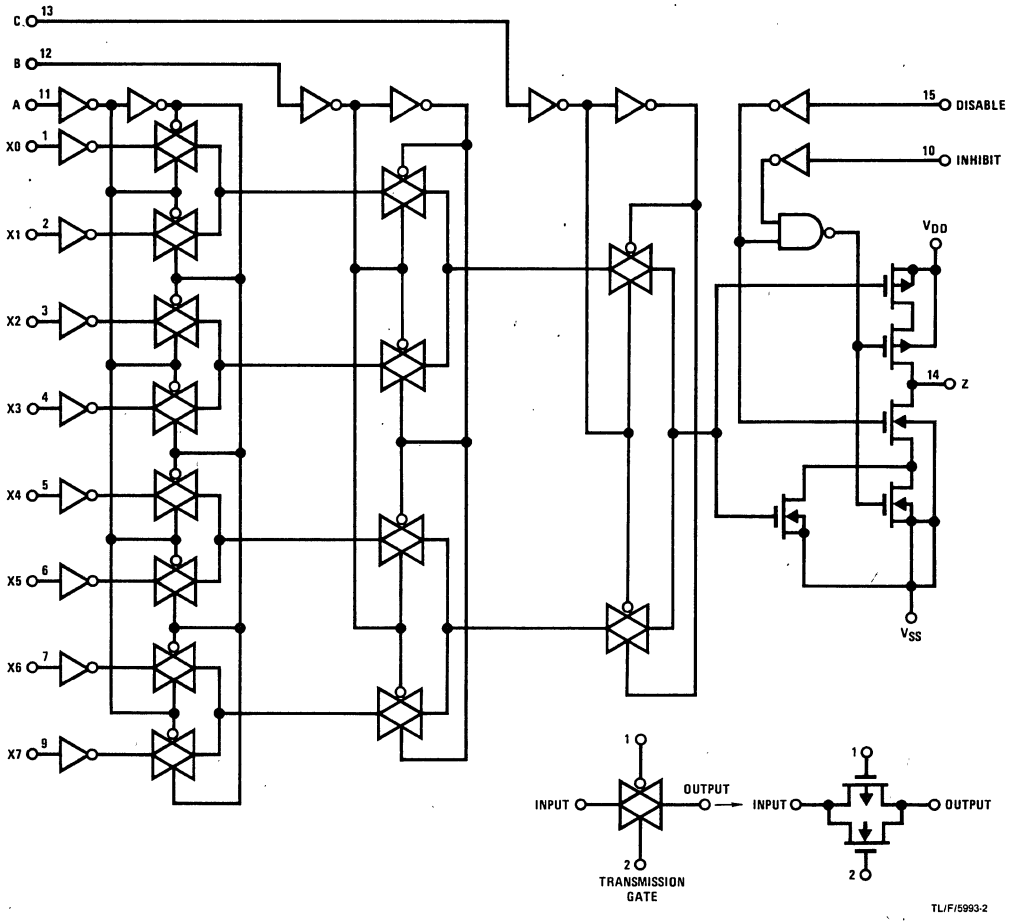
Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Capacitance guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note AN-90.

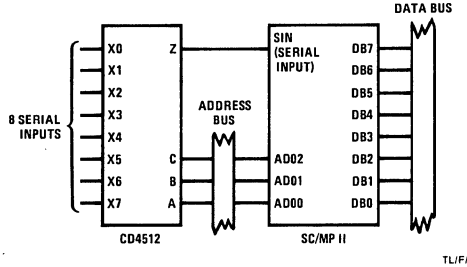
Logic Diagram



TL/F/5993-2

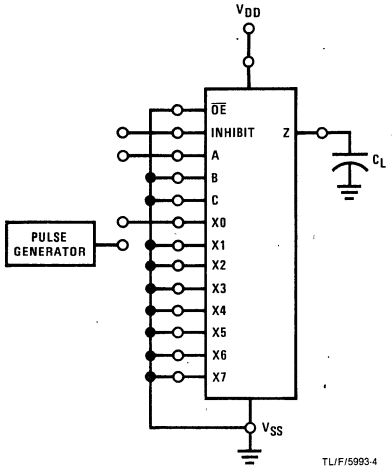
Typical Application

Serial Data Routing Interface

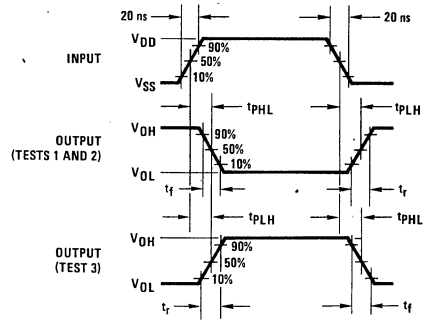


TL/F/5993-3

AC Test Circuit and Switching Time Waveforms



TL/F/5993-4

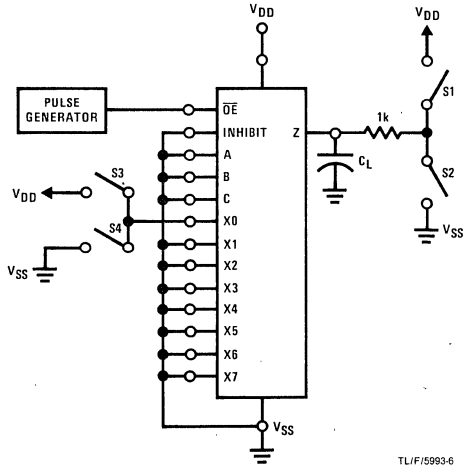


TL/F/5993-5

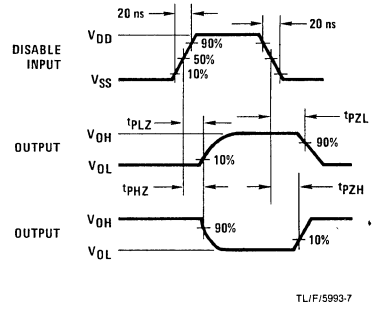
INPUT CONNECTIONS FOR t_r, t_f, t_{PLH}, t_{PHL}

TEST	INHIBIT	A	X0
1	PG	GND	V_{DD}
2	GND	PG	V_{DD}
3	GND	GND	PG

TRI-STATE AC Test Circuit and Switching Time Waveforms



TL/F/5993-6



TL/F/5993-7

SWITCH POSITIONS FOR TRI-STATE TEST

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

National Semiconductor

CD4514BM/CD4514BC, CD4515BM/CD4515BC 4-Bit Latched/4-to-16 Line Decoders

General Description

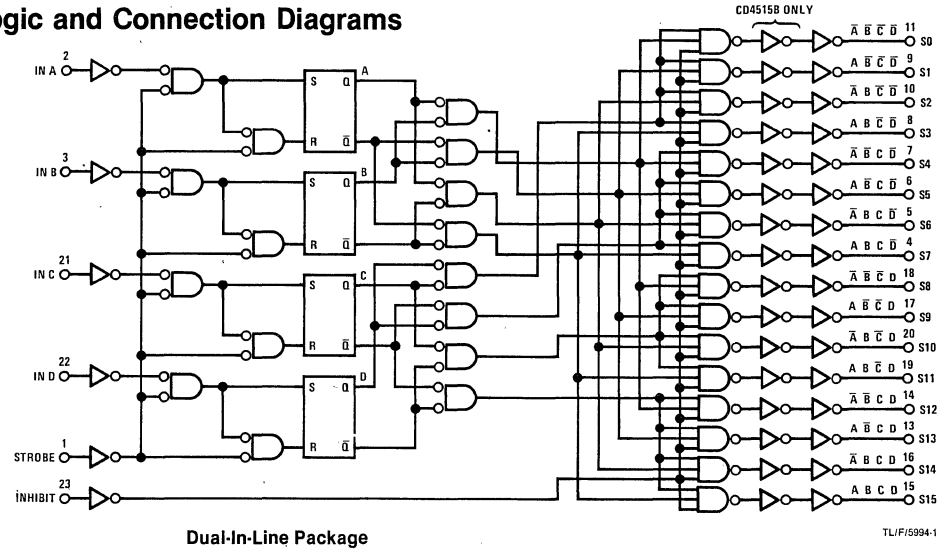
The CD4514B and CD4515B are 4-to-16 line decoders with latched inputs implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. These circuits are primarily used in decoding applications where low power dissipation and/or high noise immunity is required.

The CD4514B (output active high option) presents a logical "1" at the selected output, whereas the CD4515B presents a logical "0" at the selected output. The input latches are R-S type flip-flops, which hold the last input data presented prior to the strobe transition from "1" to "0". This input data is decoded and the corresponding output is activated. An output inhibit line is also available.

Features

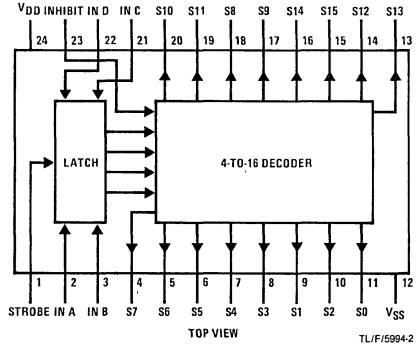
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L
- Low quiescent power dissipation — 0.025 μW/package @ 5.0 V_{DC}
- Single supply operation
- Input impedance $= 10^{12}\Omega$ typically
- Plug-in replacement for MC14514, MC14515

Logic and Connection Diagrams



TL/F/5994-1

Dual-In-Line Package



TL/F/5994-2

Order Number CD4514BMJ, CD4514BCJ, CD4515BMJ or CD4515BCJ
See NS Package J24A

Order Number CD4514BMN, CD4514BCN, CD4515BMN or CD4515BCN
See NS Package N24A

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4514BM, CD4515BM	−55°C to +125°C
CD4514BC, CD4515BC	−40°C to +85°C

DC Electrical Characteristics CD4514BM, CD4515BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5.0		0.005	5.0		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10.0		0.010	10.0		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20.0		0.015	20.0		600	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_{IL} = 0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_{IL} = 0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or 4.5V								
		V_{DD} = 5V, $\|I_O\| < 1\ \mu A$		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_O = 0.5V or 4.5V								
		V_{DD} = 5V, $\|I_O\| < 1\ \mu A$	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.80		2.40		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.80		−2.40		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4514BC, CD4515BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.005	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.010	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V

DC Electrical Characteristics (Continued) CD4514BC, CD4515BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics All types C_L = 50 pF, T_A = 25°C, $t_r = t_f$ = 20 ns unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{THL}, t_{TLH}	Transition Times	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Times	V_{DD} = 5V		550	1100	ns
		V_{DD} = 10V		225	450	ns
		V_{DD} = 15V		150	300	ns
t_{PLH}, t_{PHL}	Inhibit Propagation Delay Times	V_{DD} = 5V		400	800	ns
		V_{DD} = 10V		150	300	ns
		V_{DD} = 15V		100	200	ns
t_{SU}	Set Up Time	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		38	75	ns
t_{WH}	Strobe Pulse Width	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		38	75	ns
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 5)		150		pF
C_{IN}	Input Capacitance	Any Input, (Note 4)		5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C&74C Family Characteristics application note, AN-90.

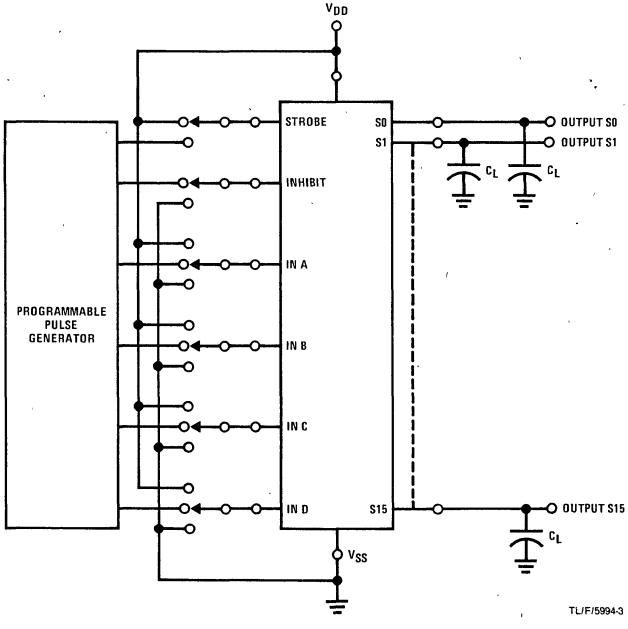
Truth Table

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DATA INPUTS				SELECTED OUTPUT CD4514 = LOGIC "1" CD4515 = LOGIC "0"
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514 All Outputs = 1, CD4515

X = Don't care

AC Test Circuit and Switching Time Waveforms



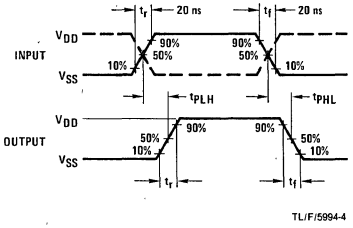


FIGURE 1

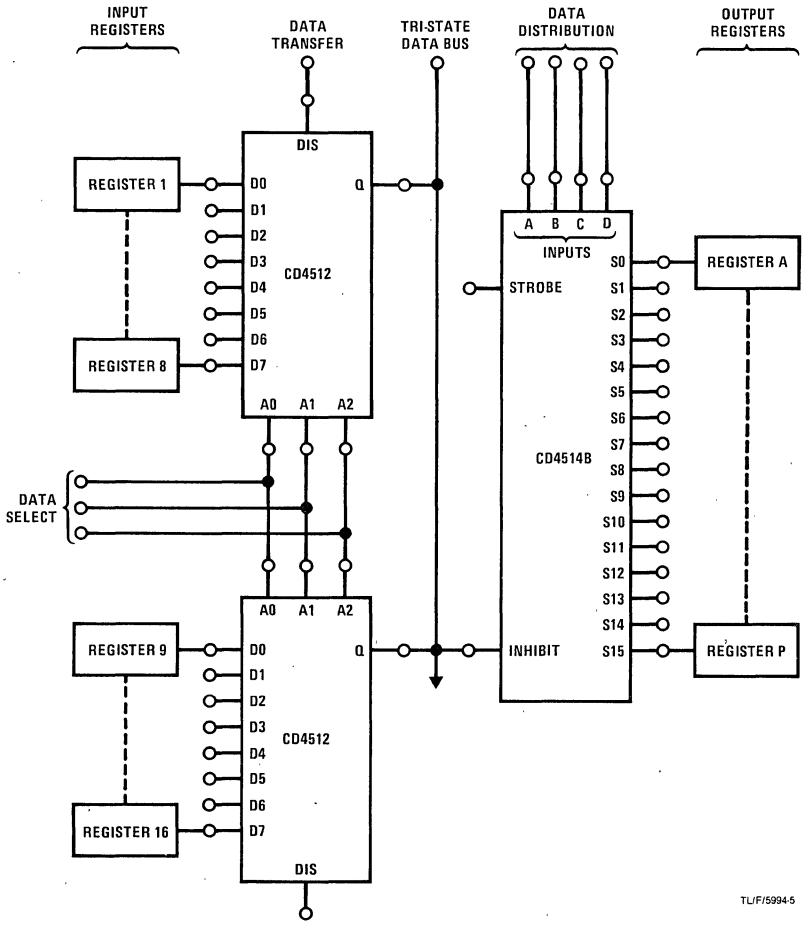
Applications

Two CD4512 8-channel data selectors are used here with the CD4514B 4-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a TRI-STATE data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the 8 inputs on both CD4512 data selectors. One register is assigned to each input. The signals on A0, A1 and A2 choose 1-of-8 inputs for transfer out to the TRI-STATE data bus. A fourth signal, labelled Dis, disables one of the CD4512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1—16, the rate of transfer of the sequential information can also be varied. That is, if the CD4512 were addressed at a rate that is 8 times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the TRI-STATE bus is redistributed by the CD4514B 4-bit latch/decoder. Using the 4-bit address, INA—IND, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A—P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.



National Semiconductor

CD4518BM/CD4518BC, CD4520BM/CD4520BC Dual Synchronous Up Counters

General Description

The CD4518BM/CD4518BC dual BCD counter and the CD4520BM/CD4520BC dual binary counter are implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors.

Each counter consists of two identical, independent, synchronous, 4-stage counters. The counter stages are toggle flip-flops which increment on either the positive-edge of CLOCK or negative-edge of ENABLE, simplifying cascading of multiple stages. Each counter can be asynchronously cleared by a high level on the RESET line. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 6MHz counting rate (typ.) at V_{DD} = 10V

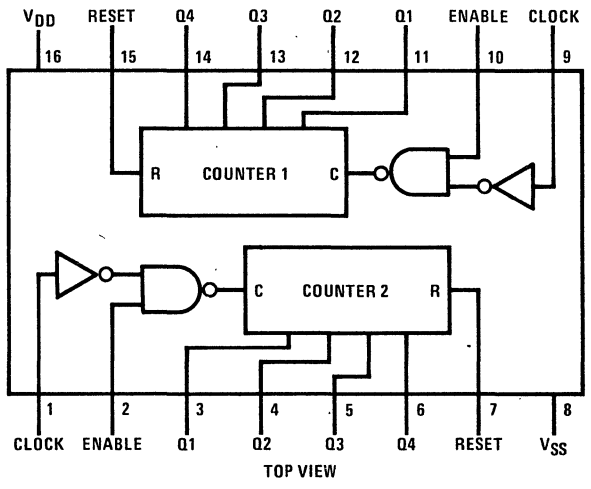
Truth Table

CLOCK	ENABLE	RESET	ACTION
↑	1	0	Increment counter
0	↓	0	Increment counter
↓	X	0	No change
X	↑	0	No change
↑	0	0	No change
1	↓	0	No change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

Connection Diagram

Dual-In-Line and Flat Package



TOP VIEW

TL/F/5995-1

Order Number CD4518BMJ, CD4518BCJ, CD4520BMJ or CD4520BCJ
See NS Package J16A

Order Number CD4518BMN, CD4518BCN, CD4520BMN or CD4520BCN
See NS Package N16E

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4518BM, CD4520BM	−55°C to +125°C
CD4518BC, CD4520BC	−40°C to +85°C

DC Electrical Characteristics CD4518BM/CD4520BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.01	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4518BC/CD4520BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1$ μA, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1$ μA, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4518BC/CD4520BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
	(Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
	(Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, $t_r = t_f = 20\,ns$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock → Q	V_{DD} = 5V		325	650	ns
		V_{DD} = 10V		110	225	ns
		V_{DD} = 15V		85	170	ns
t_{PHL}	Propagation Delay Time Reset → Q	V_{DD} = 5V		220	560	ns
		V_{DD} = 10V		90	230	ns
		V_{DD} = 15V		65	160	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5V	1.5	3		MHz
		V_{DD} = 10V	3.0	6		MHz
		V_{DD} = 15V	4.0	8		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		35	70	ns
t_{RCL}, t_{FC}	Maximum Clock or Enable Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	10			μs
		V_{DD} = 15V	5			μs
t_{WH}, t_{WL}	Minimum Enable Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		55	110	ns
		V_{DD} = 15V		40	80	ns
t_{WH}	Minimum Reset Pulse Width	V_{DD} = 5V		180	375	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	130	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Either Counter, (Note 4)		50		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

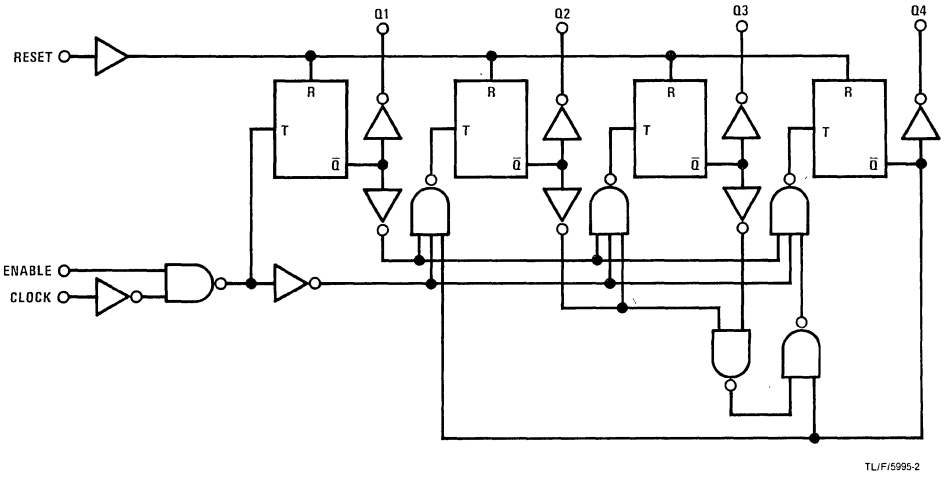
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load ac power consumption of a CMOS device. For a complete explanation, see "54C/74C Family Characteristics," application note AN-90.

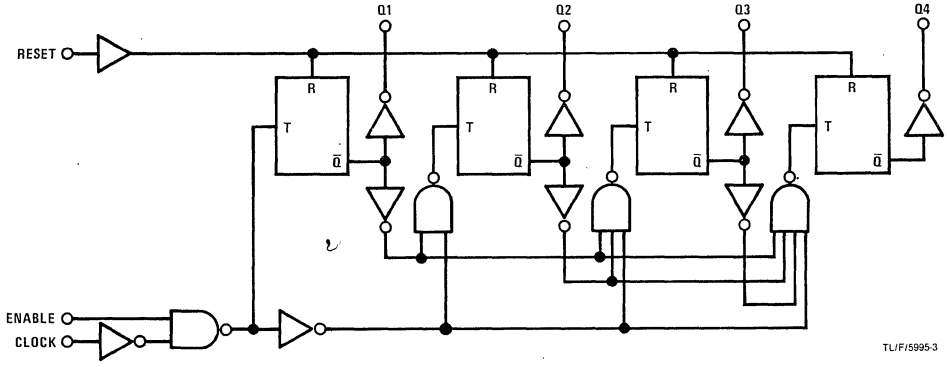
Logic Diagrams

Decade Counter (CD4518B) 1/2 Device Shown



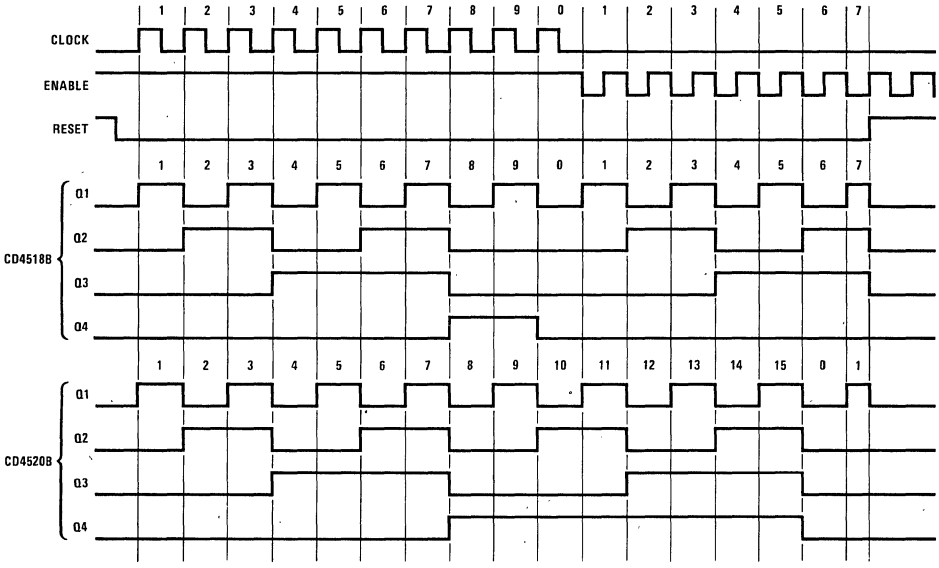
TL/F/5995-2

Binary Counter (CD4520B) 1/2 Device Shown



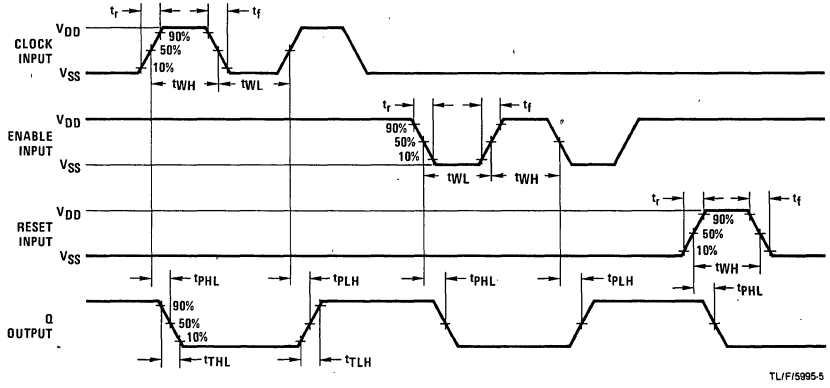
TL/F/5995-3

Timing Diagrams



TL/F/5995-4

Switching Time Waveforms



TL/F/5995-5

National Semiconductor

CD4519BM/CD4519BC 4-Bit AND/OR Selector

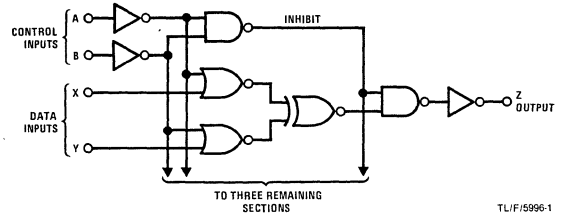
General Description

The CD4519B is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement mode transistors. Depending on the condition of the control inputs, this part provides three functions in one package: a 4-bit AND/OR selector, a quad 2-channel Data Selector, or a Quad Exclusive-NOR Gate. The device outputs have equal source and sink current capabilities and conform to the standard B series output drive and supply voltage ratings.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility fan out of 2 driving 74L or 1 driving 74LS
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range
- Second source of Motorola MC14519

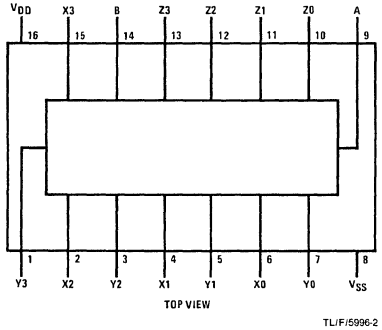
Logic Diagram



TL/F/5996-1

Connection Diagram

Dual-In-Line Package



TL/F/5996-2

Order Number CD4519BMJ or CD4519BCJ
See NS Package J16A

Order Number CD4519BMN or CD4519BCN
See NS Package N16E

Truth Table

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \odot Y_n$

Note: $X_n \odot Y_n = \overline{X_n \oplus Y_n} = X_nY_n + \overline{X}_n\overline{Y}_n$

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4519BM	−55°C to +125°C
CD4519BC	−40°C to +85°C

DC Electrical Characteristics CD4519BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		1		0.005	1		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		2		0.006	2		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		4		0.007	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4519BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		4			4		30	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		8			8		60	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		16			16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

DC Electrical Characteristics (Cont'd.) CD4519BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	6		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, $t_r = t_f = 20\,ns$, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay High-to-Low Level or Low-to-High Level	*(Figure 1)*				
		$V_{DD} = 5V$		180	360	ns
		$V_{DD} = 10V$		75	150	ns
		$V_{DD} = 15V$		60	120	ns
t_{THL}, t_{TLH}	Transition Time	*(Figure 1)*				
		$V_{DD} = 5V$		90	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Average Input Capacitance	Any Input (Note 4)		5	7.5	pF
C_{pd}	Power Dissipation Capacity	Any Gate (Note 5)		25		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

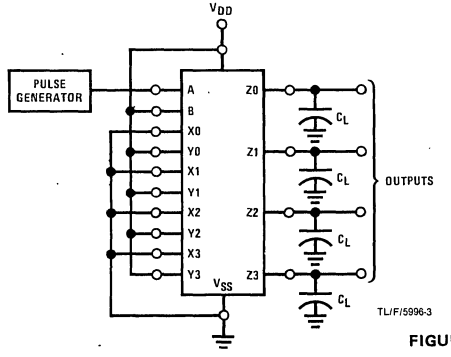
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family characteristics application note AN-90.

AC Test Circuit and Switching Time Waveforms



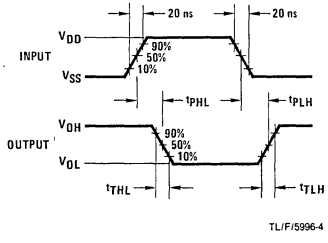
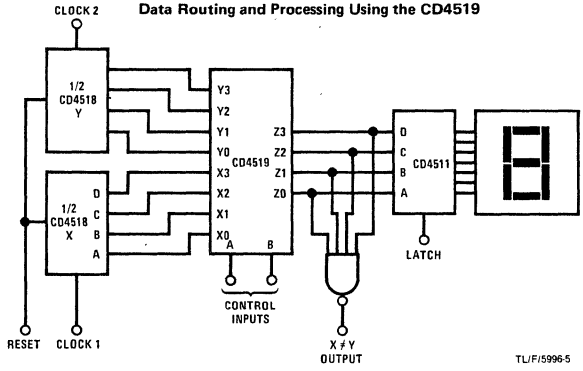


FIGURE 1

Typical Application

Data Routing and Processing Using the CD4519



CONTROL INPUTS		FUNCTION
A	B	
0	0	Display Zero
0	1	Display Counter Y
1	0	Display Counter X
1	1	Compare Counters

National Semiconductor

CD4522BM/CD4522BC Programmable Divide-By-N 4-Bit BCD Counter
CD4526BM/CD4526BC Programmable Divide-By-N 4-Bit Binary Counter

General Description

The CD4522BM/CD4522BC, CD4526BM/CD4526BC are CMOS programmable cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications, the "0" output is applied to the Preset Enable input. For multi-stage applications, the "0" output is used in conjunction with the CF (Cascade Feedback) input to perform the divide-by-N function. The "0" output is normally at logical "0" level; it will go to a logical "1" state only when the counter is at its terminal count (0000) and if CF is at logical "1" level. Thus, CF acts as an active low inhibit for the "0" output. This feature allows cascade divide-by-N operations with no additional gate required (see Applications section). The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Features

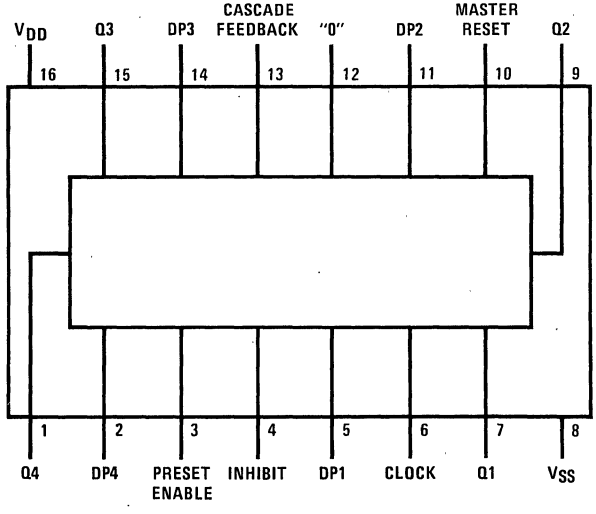
- Wide supply voltage range — 3.0 V to 18 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Quiescent current = 5 nA/package (typ.) @ V_{DD} = 5.0 V
- Internally synchronous for high internal and external speed
- Logic edge-clocked design—incremented on positive transition of Clock or negative transition of Clock Inhibit
- Medium speed — 7.7 MHz (typ.) @ V_{DD} = 10 V
- Asynchronous Preset Enable

Applications

- Programmable down counter
- Programmable frequency divider
- Frequency synthesizers
- Phase-locked loops

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5997-1

Order Number CD4522BMJ, CD4522BCJ, CD4526BMJ or CD4526BCJ
See NS Package J16A

Order Number CD4522BMN, CD4522BCN, CD4526BMN or CD4526BCN
See NS Package N16E

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4522BM, CD4526BM	−55°C to +125°C
CD4522BC, CD4526BC	−40°C to +85°C

DC Electrical Characteristics CD4522BM, CD4526BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.005	5		150	μA
		V_{DD} = 10V		10		0.010	10		300	μA
		V_{DD} = 15V		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4522BC, CD4526BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.010	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Continued) CD4522BC, CD4526BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	(Note 3)	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{THL} or t_{TLH}	Output Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PHL} & t_{PLH}	Propagation Delay Time From Clock to Q Outputs	V_{DD} = 5V		350	825	ns
		V_{DD} = 10V		130	345	ns
		V_{DD} = 15V		90	240	ns
t_{PHL} & t_{PLH}	Propagation Delay Time From Clock to "0" Output	V_{DD} = 5V		200	500	ns
		V_{DD} = 10V		80	250	ns
		V_{DD} = 15V		60	190	ns
PW_C	Minimum Clock Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
f_{CL}	Maximum Clock Pulse Frequency	V_{DD} = 5V	1.5	2.9		MHz
		V_{DD} = 10V	3.0	7.7		MHz
		V_{DD} = 15V	4.0	11		MHz
t_{rCL} & t_{fCL}	Maximum Clock or Inhibit Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	15			μs
		V_{DD} = 15V	15			μs
t_{HOLD}	Hold Time	V_{DD} = 5V		40	125	ns
		V_{DD} = 10V		25	50	ns
		V_{DD} = 15V		20	40	ns
PW_{PE}	Minimum Preset Enable Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
PW_{MR}	Minimum Master Reset Pulse Width	V_{DD} = 5V		160	350	ns
		V_{DD} = 10V		75	180	ns
		V_{DD} = 15V		50	120	ns
C_{IN}	Input Capacitance	(Note 4)		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 5)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

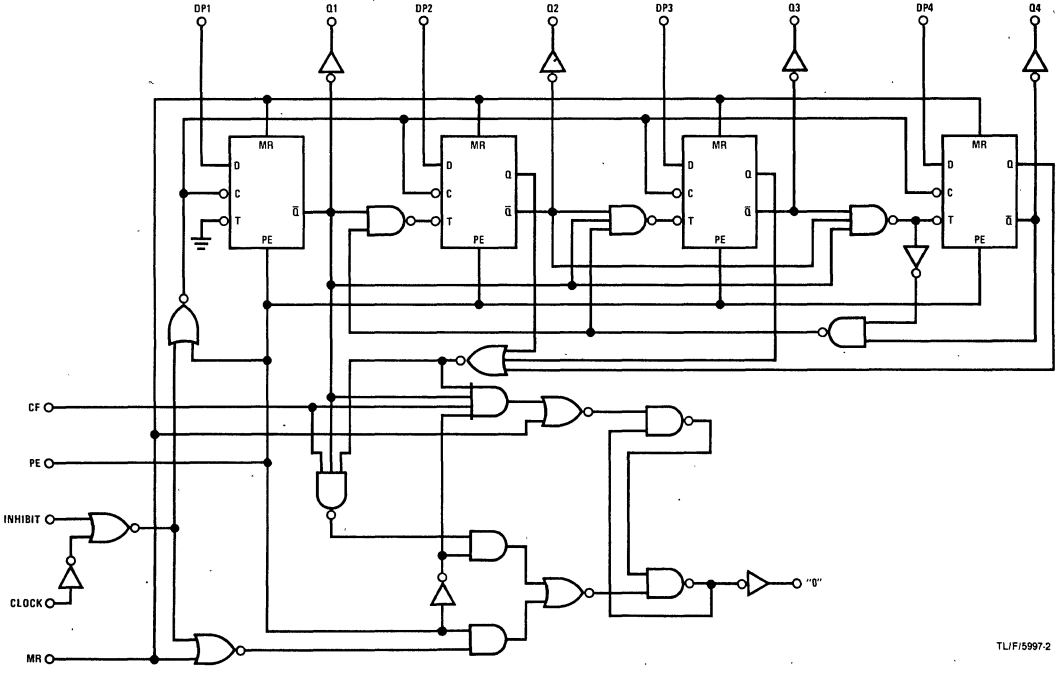
Note 4: Capacitance is guaranteed by periodic testing.

Note 5: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

5

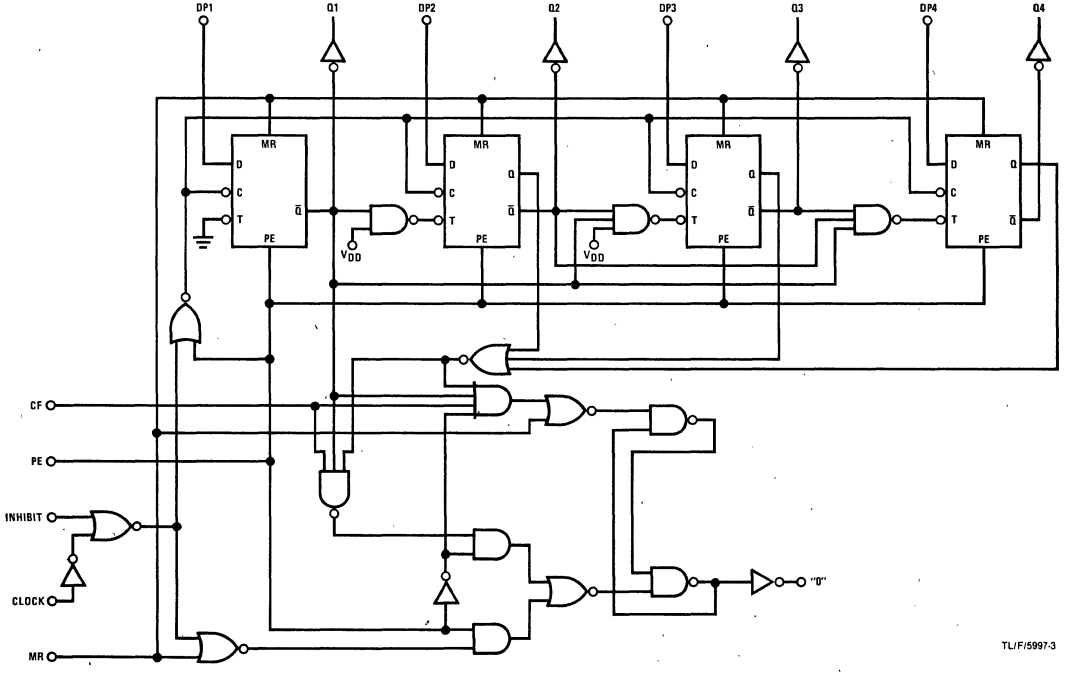
Logic Diagrams

CD4522BM/CD4522BC



TL/F/5997-2

CD4526BM/CD4526BC



TL/F/5997-3

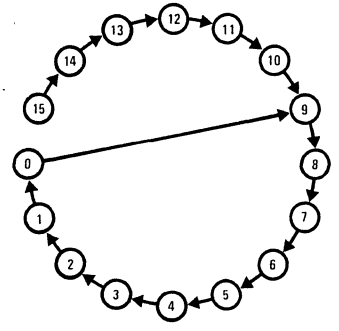
Truth Tables and Count Sequences

Both Types

CLOCK	INHIBIT	PRESET ENABLE	MASTER RESET	ACTION
0	0	0	0	No count
⌐	0	0	0	Count 1
X	1	0	0	No count
1	¬	0	0	Count 1
X	X	1	0	Preset
X	X	X	1	Reset

CD4522BM/CD4522BC

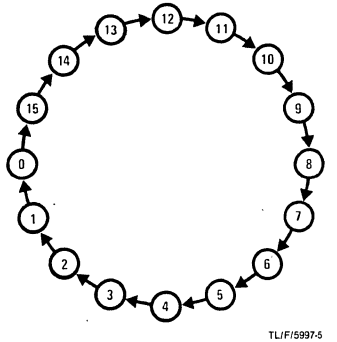
COUNT	OUTPUT			
	Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



TL/F/5997-4

CD4526BM/CD4526BC

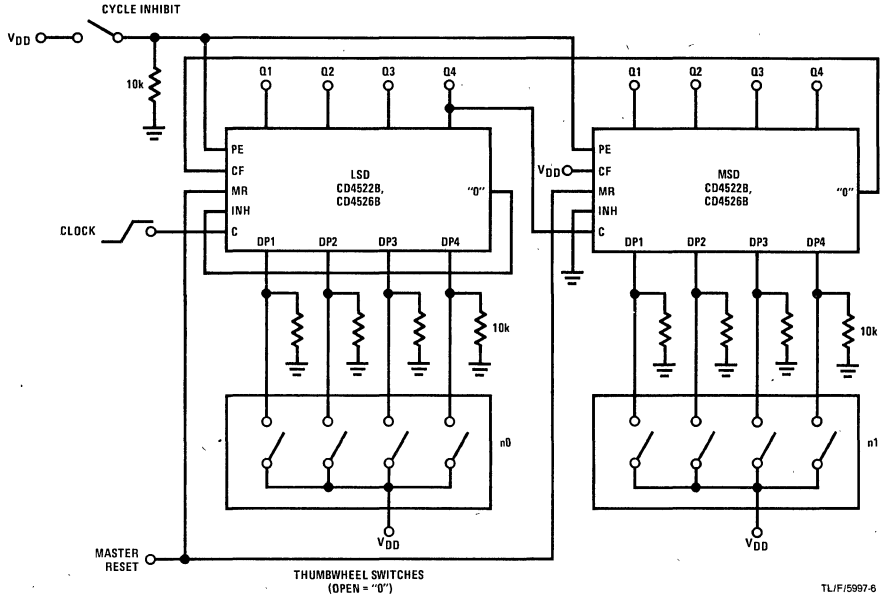
COUNT	OUTPUT			
	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



TL/F/5997-5

Typical Applications

2-Stage Programmable Down Counter

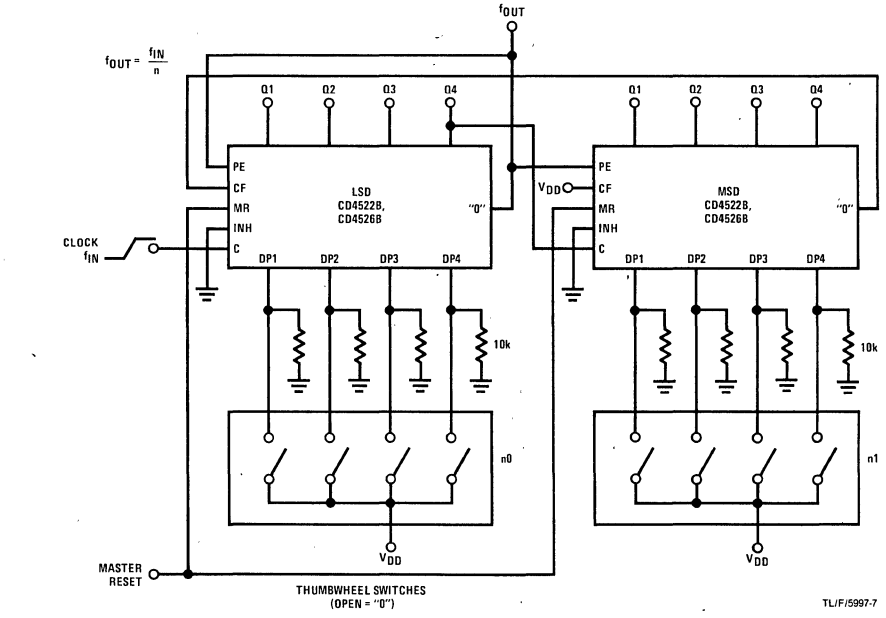


COUNTING CYCLE

LSD	MSD
n0	
n0−1	
.	
.	n1
.	
1	
0	
9 (15)	
8 (14)	
.	
.	n1−1
.	
1	
0	
.	
.	
.	
9 (15)	
8 (14)	
.	
.	0
.	
1	
0	

↓
STOP

2-Stage Programmable Frequency Divider



COUNTING CYCLE

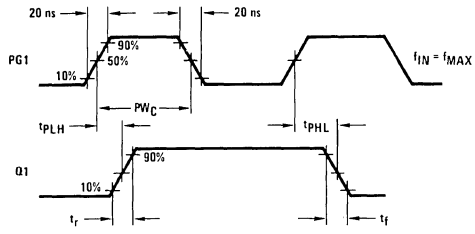
LSD	MSD
n0	
n0−1	
.	
.	n1
.	
1	
0	
9 (15)	
8 (14)	
.	
.	n1−1
.	
1	
0	
.	
.	
.	
9 (15)	
8 (14)	
.	
.	0
.	
1	
0	

↓
REPEAT CYCLE

Note. When cascading more than 2 packages, tie "0" output of the nth package to CF input of the (n−1)th package for all n = 2, 3.

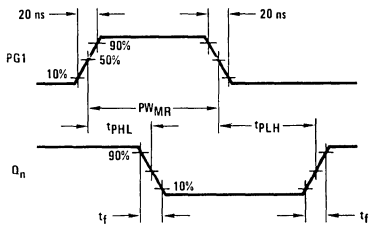
Switching Time Waveforms

Test No. 1



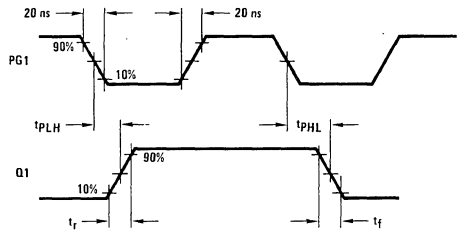
TL/F/5997-8

Test No. 4



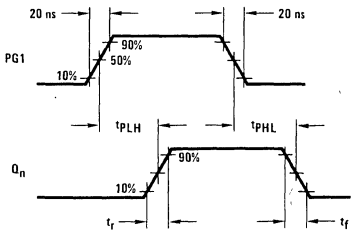
TL/F/5997-9

Test No. 2



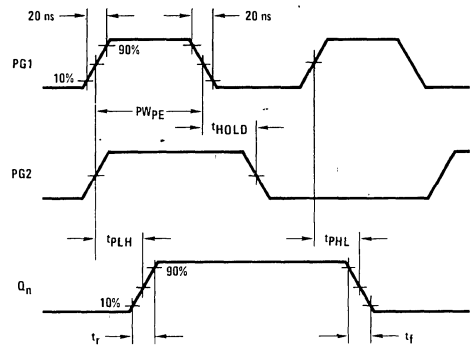
TL/F/5997-10

Tests No. 5 and 7



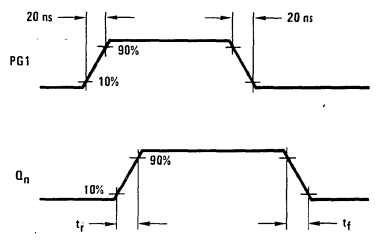
TL/F/5997-11

Test No. 3



TL/F/5997-12

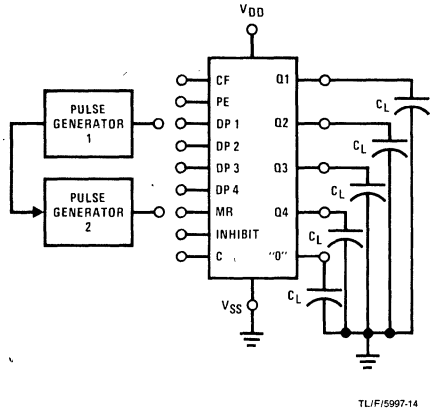
Test No. 6



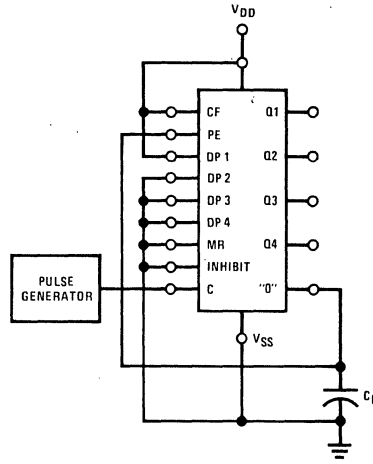
TL/F/5997-13

5

AC Test Circuits



a) Tests No. 1–6



b) Test No. 7

FIGURE 1. Test Circuit

Test Conditions

TABLE I

CHARACTERISTIC	TEST NO.	CLOCK	INHIBIT	PE	MR	DP_n	CF	OUTPUT
t_r, t_f, t_{PLH}, t_{PHL}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
PW_{MR}	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
PW_{PE}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
PW_C	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{MAX}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_{HOLD}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_r, t_f	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	*Fig. 1b*	V_{SS}	*Fig. 1b*	V_{DD}	"0"

National Semiconductor

CD4528BM/CD4528BC Dual Monostable Multivibrator

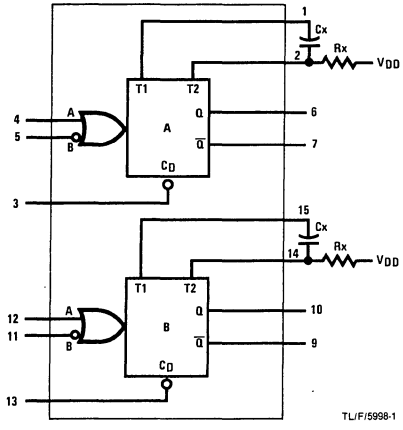
General Description

The CD4528B is a dual monostable multivibrator. Each device is retriggerable and resettable. Triggering can occur from either the rising or falling edge of an input pulse, resulting in an output pulse over a wide range of widths. Pulse duration and accuracy are determined by external timing components R_X and C_X.

Features

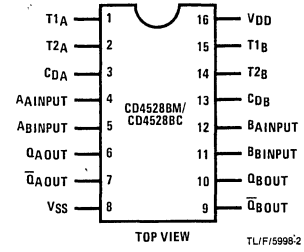
- Wide supply voltage range 3.0 V to 18 V
- Separate reset available
- Quiescent current = 5.0 nA/package (typ.) at 5.0 V_{DC}
- Diode protection on all inputs
- Triggerable from leading or trailing edge pulse
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range

Connection Diagrams



TL/F/5998-1

Dual-In-Line Package



TL/F/5998-2

Order Number CD4528BMJ or CD4528BCJ
See NS Package J16A

Order Number CD4528BMN or CD4528BCN
See NS Package N16E

Truth Tables

Inputs			Outputs	
Clear	A	B	Q	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD}, DC Supply Voltage −0.5VDC to +18VDC
V_{IN}, Input Voltage, All Inputs −0.5VDC to V_{DD} +0.5VDC
T_S, Storage Temperature Range −65°C to +150°C
P_D, Package Dissipation 500 mW
T_L, Lead Temperature (soldering, 10 seconds) 260°C

Recommended Operating Conditions

(Note 2)

V_{DD}, DC Supply Voltage 3V to 15V
V_{IN}, Input Voltage 0V to V_{DD} V_{DC}
T_A, Operating Temperature Range
CD4528BM −55°C to +125°C
CD4528BC −40°C to +85°C

DC Electrical Characteristics CD4528BM (Note 2)

SYM	Parameter	Conditions	−55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5	0.005		5		150	μA
		V_{DD} = 10V		10	0.010		10		300	μA
		V_{DD} = 15V		20	0.015		20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.36		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−0.9		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4528BC (Note 2)

SYM	Parameter	Conditions	-40°C		+25°C			+85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.010	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 0.5V or 4.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	-0.2		-0.16	-0.36		-0.12		mA
		V_{DD} = 10V, V_O = 9.5V	-0.5		-0.4	-0.9		-0.3		mA
		V_{DD} = 15V, V_O = 13.5V	-1.4		-1.2	-3.5		-1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		-0.3		-10^{-5}	-0.3		-1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

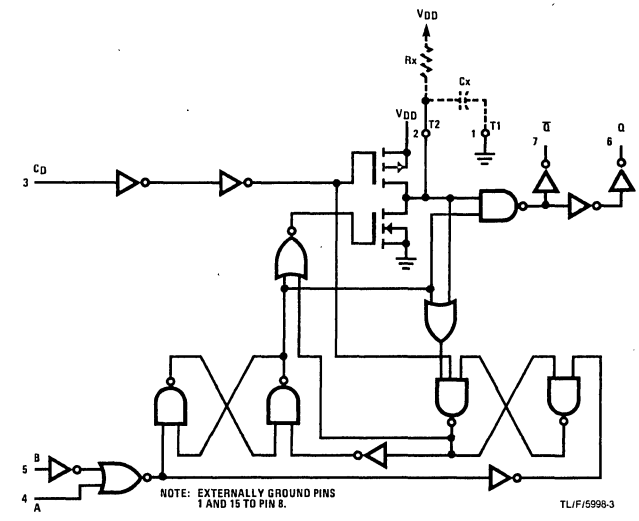
Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics CD4528BM

$T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, Input $t_r = t_f = 20\,ns$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Output Rise Time	$t_r = (3.0\,ns/pF)C_L + 30\,ns$, $V_{DD} = 5.0V$		180	400	ns
	$t_r = (1.5\,ns/pF)C_L + 15\,ns$, $V_{DD} = 10.0V$		90	200	ns
	$t_r = (1.1\,ns/pF)C_L + 10\,ns$, $V_{DD} = 15.0V$		65	160	ns
Output Fall Time	$t_f = (1.5\,ns/pF)C_L + 25\,ns$, $V_{DD} = 5.0V$		100	200	ns
	$t_f = (0.75\,ns/pF)C_L + 12.5\,ns$, $V_{DD} = 10.0V$		50	100	ns
	$t_f = (0.55\,ns/pF)C_L + 9.5\,ns$, $V_{DD} = 15.0V$		35	80	ns
Turn-Off, Turn-On Delay A or B to Q or $\overline{Q}$ Cx = 15 pF, Rx = 5.0 kΩ	$t_{PLH}, t_{PHL} = (1.7\,ns/pF)C_L + 240\,ns$, $V_{DD} = 5.0V$		230	500	ns
	$t_{PLH}, t_{PHL} = (0.66\,ns/pF)C_L + 8\,ns$, $V_{DD} = 10.0V$		100	250	ns
	$t_{PLH}, t_{PHL} = (0.5\,ns/pF)C_L + 65\,ns$, $V_{DD} = 15.0V$		65	150	ns
Turn-Off, Turn-On Delay A or B to Q or $\overline{Q}$ Cx = 100 pF, Rx = 10 kΩ	$t_{PLH}, t_{PHL} = 1.7\,ns/pF)C_L + 620\,ns$, $V_{DD} = 5.0V$		230	500	ns
	$t_{PLH}, t_{PHL} = 0.66\,ns/pF)C_L + 257\,ns$, $V_{DD} = 10.0V$		100	250	ns
	$t_{PLH}, t_{PHL} = (0.5\,ns/pF)C_L + 185\,ns$, $V_{DD} = 15.0V$		65	150	ns
Minimum Input Pulse Width A or B Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 5.0V$		60	150	ns
	$V_{DD} = 10.0V$		20	50	ns
	$V_{DD} = 15.0V$		20	50	ns
Cx = 1000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		60	150	ns
	$V_{DD} = 10.0V$		20	50	ns
	$V_{DD} = 15.0V$		20	50	ns
Output Pulse Width Q or $\overline{Q}$ For Cx < 0.01 μF (see graph for appropriate V_{DD} level) Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 5.0V$		550		ns
	$V_{DD} = 10.0V$		350		ns
	$V_{DD} = 15.0V$		300		ns
For Cx > 0.01 μF use $PW_{out} = 0.2RxCx\ ln[V_{DD} - V_{SS}]$ Cx = 10,000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$	15	29	45	μs
	$V_{DD} = 10.0V$	10	37	90	μs
	$V_{DD} = 15.0V$	15	42	95	μs
Pulse Width Match Between Circuits in the Same Package Cx = 10,000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		6	25	%
	$V_{DD} = 10.0V$		8	35	%
	$V_{DD} = 15.0V$		8	35	%
Reset Propagation Delay, t_{PLH}, t_{PHL} Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 5.0V$		325	600	ns
	$V_{DD} = 10.0V$		90	225	ns
	$V_{DD} = 15.0V$		60	170	ns
Cx = 1000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		7.0		μs
	$V_{DD} = 10.0V$		6.7		μs
	$V_{DD} = 15.0V$		6.7		μs
Minimum Retrigger Time Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 5.0V$		0		
	$V_{DD} = 10.0V$		0		
	$V_{DD} = 15.0V$		0		
Cx = 1000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		0		
	$V_{DD} = 10.0V$		0		
	$V_{DD} = 15.0V$		0		

Logic Diagram (½ of Device Shown)



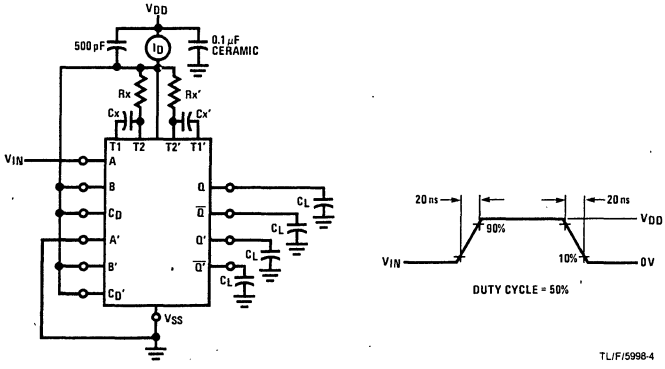
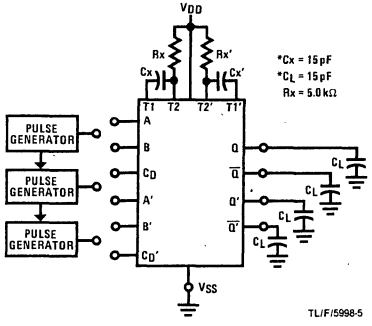


Figure 1. Power Dissipation Test Circuit and Waveforms



Input Connections

Characteristics	C_D	A	B
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, PW_{in}	PG3	PG1	PG2

*INCLUDES CAPACITANCE OF PROBES, WIRING, AND FIXTURE PARASITIC.

NOTE: AC TEST WAVEFORMS FOR PG1, PG2, AND PG3 ON NEXT PAGE.

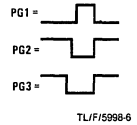


Figure 2. AC Test Circuit

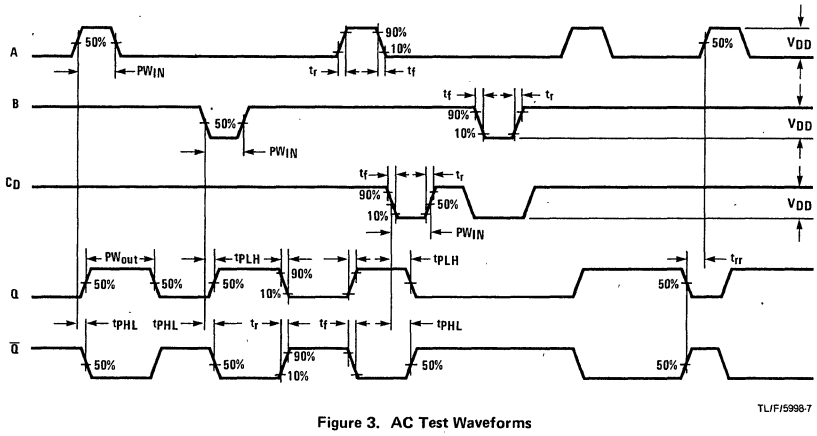


Figure 3. AC Test Waveforms

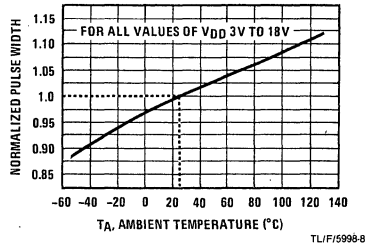


Figure 4. Normalized Pulse Width vs Temperature

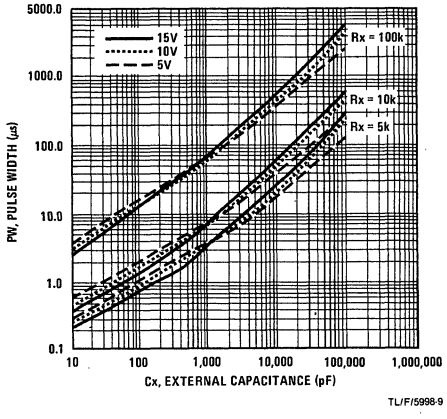


Figure 5. Pulse Width vs Cx

National Semiconductor

CD4529BM/CD4529BC Dual 4-Channel or Single 8-Channel Analog Data Selector

General Description

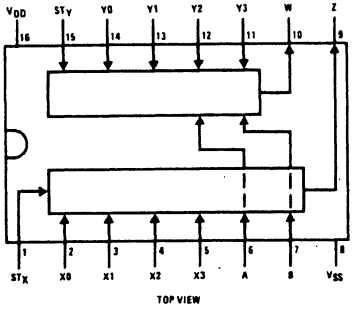
The CD4529B is a dual 4-channel or a single 8-channel analog data selector, implemented with complementary MOS (CMOS) circuits constructed with N- and P-channel enhancement mode transistors. Dual 4-channel or 8-channel mode operation is selected by proper input coding, with outputs Z and W tied together for the single 8-bit mode. The device is suitable for digital as well as analog applications, including various 1-of-4 and 1-of-8 data selector functions. Since the device is analog and bidirectional, it can also be used for dual binary to 1-of-4 or single 1-of-8 decoder applications.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low quiescent power dissipation — 0.005 μW/package (typ.) @ 5.0 V_{DC}
- 10 MHz frequency operation (typ.)
- Data paths are bidirectional
- Linear ON resistance [120 Ω (typ.) @15V]
- TRI-STATE® outputs (high impedance disable strobe)
- Plug-in replacement for MC14529B

Connection Diagram

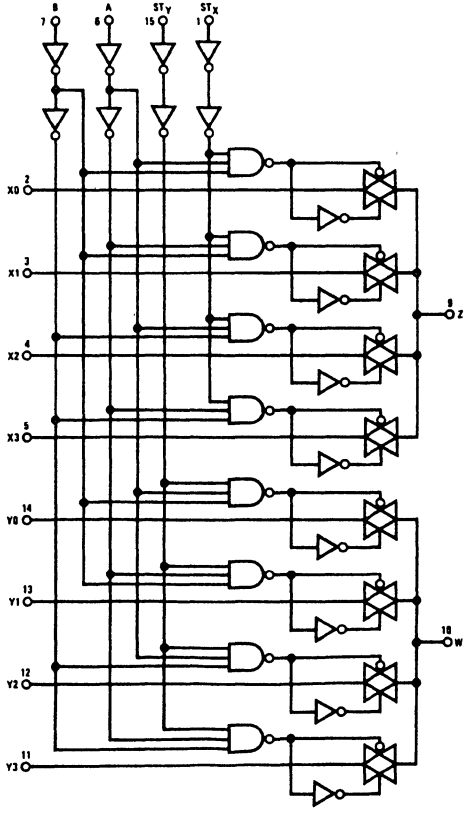
Dual-In-Line Package



TOP VIEW

Order Number CD4529BCJ, N or CD4529BMJ, N
See NS Package J16A or N16E

Logic Diagram



TL/F/5999–1

Truth Table

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X	High Impedance (TRI-STATE)		

X = Don't care

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temp. (Soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

V_{DD} DC Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4529BM	−55°C to +125°C
CD4529BC	−40°C to +85°C

DC Electrical Characteristics CD4529BM (Note 2)

Symbol	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.001	1.0		60	μA
		V_{DD} = 10V		1.0		0.002	1.0		60	μA
		V_{DD} = 15V		2.0		0.003	2.0		120	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		400		165	480		640	Ω
		V_{IN} = −5V		400		100	480		640	Ω
		V_{IN} = ±0.25V		400		155	480		640	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		240		135	270		400	Ω
		V_{IN} = −7.5V		240		75	270		400	Ω
		V_{IN} = ±0.25V		240		100	270		400	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		400		165	480		640	Ω
		V_{IN} = 0.25V		400		100	480		640	Ω
		V_{IN} = 5.6V		400		160	480		640	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		400	Ω
		V_{IN} = 0.25V		250		75	270		400	Ω
		V_{IN} = 9.3V		250		110	270		400	Ω
I_{OFF}	Input to Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V, V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −5V, V_{DD} = 5V, V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±2500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±2500	nA

DC Electrical Characteristics CD4529BC (Note 2) (Continued)

Symbol	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.001	5.0		70	μA
		V_{DD} = 10V		5.0		0.002	5.0		70	μA
		V_{DD} = 15V		10.0		0.003	10.0		140	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\|$ < 1 μA								
		V_{DD} = 5V	4.95		4.95	5.00		4.95		V
		V_{DD} = 10V	9.95		9.95	10.00		9.95		V
		V_{DD} = 15V	14.95		14.95	15.00		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		410		165	480		560	Ω
		V_{IN} = −5V		410		100	480		560	Ω
		V_{IN} = ±0.25V		410		155	480		560	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		250		135	270		350	Ω
		V_{IN} = −7.5V		250		75	270		350	Ω
		V_{IN} = ±0.25V		250		100	270		350	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		410		165	480		560	Ω
		V_{IN} = 0.25V		410		100	480		560	Ω
		V_{IN} = 5.6V		410		160	480		560	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		350	Ω
		V_{IN} = 0.25V		250		75	270		350	Ω
		V_{IN} = 9.3V		250		110	270		350	Ω
I_{OFF}	Input-Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V								
		V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±500	nA
		V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V								
		V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±1000	nA
		V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±1000	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Switch OFF is defined as $|I_O| \leq 10$ μA, switch ON as defined by R_{ON} specification.

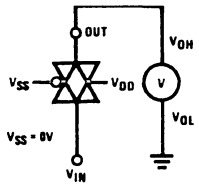
AC Characteristics CD4529BM/CD4539BC

T_A = 25°C, R_L = 1 kΩ, t_r = t_f = 20 ns, unless otherwise specified.

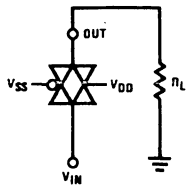
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}, t_{PHL}	V_{IN} to V_{OUT} Propagation Delay	V_{SS} = 0V, C_L = 50 pF				
		V_{DD} = 5V		20	40	ns
		V_{DD} = 10V		10	20	ns
		V_{DD} = 15V		8	15	ns
t_{PLH}, t_{PHL}	Control to Output Propagation Delay	V_{IN} = V_{DD} or V_{SS}, C_L = 50 pF				
		$V_{IN} \leq$ 10V				
		V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		50	120	ns
f_{MAX}	Maximum Control Input Pulse Frequency	V_{SS} = 0V, C_L = 50 pF				
		V_{DD} = 5V		5		MHz
		V_{DD} = 10V		10		MHz
		V_{DD} = 15V		12		MHz
	Crosstalk, Control to Output	R_{OUT} = 10 kΩ, C_L = 50 pF, V_{SS} = 0				
		V_{DD} = 5V		5.0		mV
		V_{DD} = 10V		5.0		mV
		V_{DD} = 15V		5.0		mV
	Noise Voltage	f = 100 Hz, V_{SS} = 0V				
		V_{DD} = 5V		24		nV/√cycle
		V_{DD} = 10V		25		nV/√cycle
		V_{DD} = 15V		30		nV/√cycle
		f = 100 kHz, V_{SS} = 0V				
		V_{DD} = 5V		12		nV/√cycle
		V_{DD} = 10V		12		nV/√cycle
		V_{DD} = 15V		15		nV/√cycle
	Sine Wave (Distortion)	V_{IN} = 1.77Vrms Centered		0.36		%
		at 0V, R_L = 10 kΩ, f = 1 kHz,				
		V_{SS} = −5V, V_{DD} = 5V				
I_{LOSS}	Insertion Loss,	V_{IN} = 177Vrms Centered				
		at 0V, V_{SS} = −5V, V_{DD} = 5V				
	$I_{LOSS} = 20 \log_{10} \frac{V_{OUT}}{V_{IN}}$	R_L = 1 kΩ		2.0		dB
		R_L = 10 kΩ		0.8		dB
		R_L = 100 kΩ		0.25		dB
		R_L = 1 MΩ		0.01		dB
BW	Bandwidth, −3dB	V_{IN} = 177Vrms Centered				
		at 0 Vdc, V_{SS} = −5V, V_{DD} = 5V				
		R_L = 1 kΩ	35			MHz
		R_L = 10 kΩ	28			MHz
		R_L = 100 kΩ	27			MHz
		R_L = 1 MΩ	26			MHz
	Feedthrough and Crosstalk,	V_{SS} = −5V, V_{DD} = 5V				
	$20 \log_{10} \frac{V_{OUT}}{V_{IN}} = -50$ db	R_L = 1 kΩ	850			kHz
		R_L = 10 kΩ	100			kHz
		R_L = 100 kΩ	12			kHz
		R_L = 1 MΩ	1.5			Khz

Test Circuits and Switching Time Waveforms

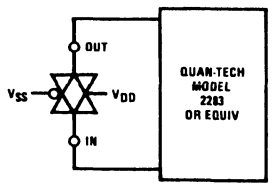
Output Voltage



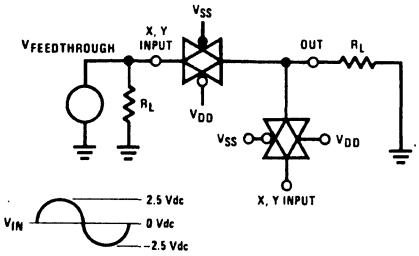
R_{ON} Characteristics



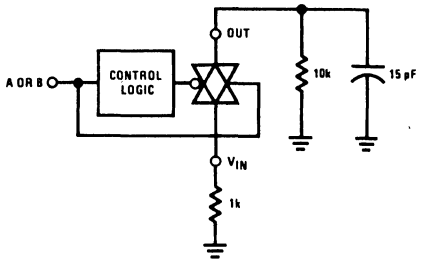
Noise Voltage



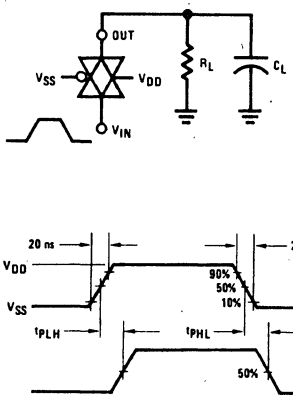
Frequency Response



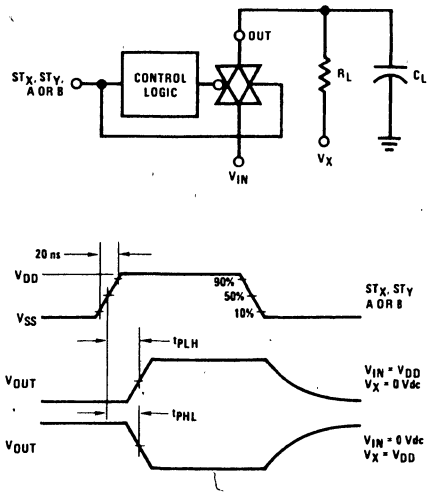
Crosstalk



Propagation Delay



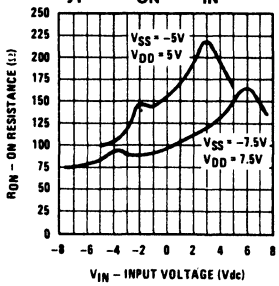
Turn-ON Delay Time



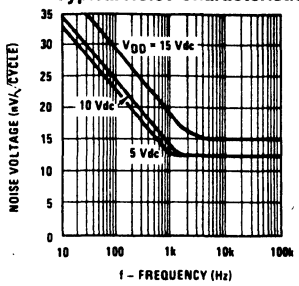
TL/F/5999–2

Typical Performance Characteristics

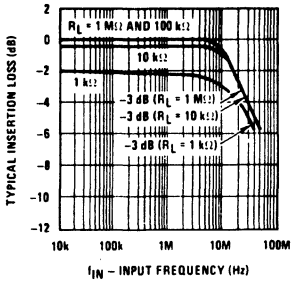
Typical R_{ON} vs V_{IN}



Typical Noise Characteristics



Typical Insertion Loss/ Bandwidth Characteristics



TL/F/5999–3

National Semiconductor

CD4538BM/CD4538BC Dual Precision Monostable

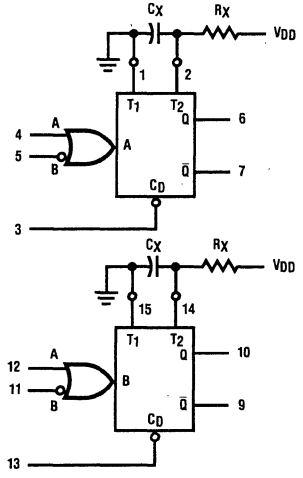
General Description

The CD4538B is a dual, precision monostable multivibrator with independent trigger and reset controls. The device is retriggerable and resettable, and the control inputs are internally latched. Two trigger inputs are provided to allow either rising or falling edge triggering. The reset inputs are active low and prevent triggering while active. Precise control of output pulse-width has been achieved using linear CMOS techniques. The pulse duration and accuracy are determined by external components R_X and C_X. The device does not allow the timing capacitor to discharge through the timing pin on power-down condition. For this reason, no external protection resistor is required in series with the timing pin. Input protection from static discharge is provided on all pins.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} (typ.)
- Low power fan out of 2 driving 74L
  TTL compatibility or 1 driving 74LS
- New Formula: $PW_{OUT} = RC$
  (PW in seconds, R in Ohms, C in Farads)
- ±1.0% pulse-width variation from part to part (typ.)
- Wide pulse-width range 1 μs to ∞
- Separate latched reset inputs
- Symmetrical output sink and source capability
- Low standby current 5 nA (typ.) @ 5 V_{DC}
- Pin Compatible to CD4528B

Block and Connection Diagrams

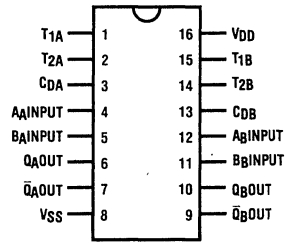


RX AND CX ARE EXTERNAL COMPONENTS
V_{DD} = Pin 16
V_{SS} = Pin 8

TL/F/6000-1

Dual-In-Line Package

CD4538BM
CD4538BC



TOP VIEW

TL/F/6000-2

Order Number CD4538BMJ or CD4538BCJ
See NS Package J16A

Order Number CD4538BMN or CD4538BCN
See NS Package N16E

Truth Table

Inputs			Outputs	
Clear	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

5

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 V to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65 °C to +150 °C
P_D Package Dissipation	500 mW
T_L Lead Temperature (soldering, 10 seconds)	260 °C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4538BM,	−55 °C to +125 °C
CD4538BC	−40 °C to +85 °C

DC Electrical Characteristics (Note 2) — CD4538BM

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, All outputs open		5		0.005	5		150	μA
		V_{DD} = 10 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, All outputs open		10		0.010	10		300	μA
		V_{DD} = 15 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}, All outputs open		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V, $\|I_O\| < 1\mu A$, V_{IH} = V_{DD}, V_{IL} = V_{SS}		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $\|I_O\| < 1\mu A$, V_{IH} = V_{DD}, V_{IL} = V_{SS}		0.05		0	0.05		0.05	V
		V_{DD} = 15 V, $\|I_O\| < 1\mu A$, V_{IH} = V_{DD}, V_{IL} = V_{SS}		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V, $\|I_O\| < 1\mu A$, V_{IH} = V_{DD}, V_{IL} = V_{SS}	4.95		4.95	5		4.95		V
		V_{DD} = 10 V, $\|I_O\| < 1\mu A$, V_{IH} = V_{DD}, V_{IL} = V_{SS}	9.95		9.95	10		9.95		V
		V_{DD} = 15 V, $\|I_O\| < 1\mu A$, V_{IH} = V_{DD}, V_{IL} = V_{SS}	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$, V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		$\|I_O\| < 1\mu A$, V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.50	3.0		3.0	V
		$\|I_O\| < 1\mu A$, V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$, V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		$\|I_O\| < 1\mu A$, V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.50		7.0		V
		$\|I_O\| < 1\mu A$, V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 0.4 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5 V, V_O = 4.6 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V, V_{IH} = V_{DD}, V_{IL} = V_{SS}	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current, pin 2 or 14	V_{DD} = 15 V, V_{IN} = 0 V or 15 V		±0.02		$\pm 10^{-5}$	±0.05		±0.5	μA
I_{IN}	Input Current, other inputs	V_{DD} = 15 V, V_{IN} = 0 V or 15 V		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA

DC Electrical Characteristics (Note 2) — CD4538BC

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$ } $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$, All outputs open		20		0.005	20		150	μA
		$V_{DD}=10V$		40		0.010	40		300	μA
		$V_{DD}=15V$		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{DD}=5V$ } $\lvert I_O\rvert < 1\mu A$, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$		0.05		0	0.05		0.05	V
		$V_{DD}=10V$		0.05		0	0.05		0.05	V
		$V_{DD}=15V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD}=5V$ } $\lvert I_O\rvert < 1\mu A$, $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	4.95		4.95	5		4.95		V
		$V_{DD}=10V$	9.95		9.95	10		9.95		V
		$V_{DD}=15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\lvert I_O\rvert < 1\mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$		3.0		4.50	3.0		3.0	V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\lvert I_O\rvert < 1\mu A$								
		$V_{DD}=5V$, $V_O=0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD}=10V$, $V_O=1.0V$ or $9.0V$	7.0		7.0	5.50		7.0		V
		$V_{DD}=15V$, $V_O=1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=0.4V$ } $V_{IH}=V_{DD}$, $V_{IL}=V_{SS}$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=4.6V$ } $V_{IL}=V_{SS}$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current, pin 2 or 14	$V_{DD}=15V$, $V_{IN}=0V$ or $15V$		±0.02		$\pm 10^{-5}$	±0.05		±0.5	μA
I_{IN}	Input Current, other inputs	$V_{DD}=15V$, $V_{IN}=0V$ or $15V$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, and $t_r = t_f = 20\,ns$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}, t_{THL}	Output Transition Time	$V_{DD} = 5\,V$		100	200	ns
		$V_{DD} = 10\,V$		50	100	ns
		$V_{DD} = 15\,V$		40	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Time	Trigger Operation — A or B to Q or $\overline{Q}$				
		$V_{DD} = 5\,V$		300	600	ns
		$V_{DD} = 10\,V$		150	300	ns
		$V_{DD} = 15\,V$		100	220	ns
		Reset Operation — C_D to Q or $\overline{Q}$				
		$V_{DD} = 5\,V$		250	500	ns
		$V_{DD} = 10\,V$		125	250	ns
		$V_{DD} = 15\,V$		95	190	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width A, B, or C_D	$V_{DD} = 5\,V$		35	70	ns
		$V_{DD} = 10\,V$		30	60	ns
		$V_{DD} = 15\,V$		25	50	ns
t_{RR}	Minimum Retrigger Time	$V_{DD} = 5\,V$			0	ns
		$V_{DD} = 10\,V$		0	0	ns
		$V_{DD} = 15\,V$			0	ns
C_{IN}	Input Capacitance	Pin 2 or 14		10		pF
		other inputs		5	7.5	pF
PW_{OUT}	Output Pulse Width (Q or $\overline{Q}$) (Note: For typical distribution, see Figure 9)	$R_X = 100\,k\Omega$, $C_X = 0.002\,\mu F$, $V_{DD} = 5\,V$	208	226	244	μs
		$R_X = 100\,k\Omega$, $C_X = 0.002\,\mu F$, $V_{DD} = 10\,V$	211	230	248	μs
		$R_X = 100\,k\Omega$, $C_X = 0.002\,\mu F$, $V_{DD} = 15\,V$	216	235	254	μs
		$R_X = 100\,k\Omega$, $C_X = 0.1\,\mu F$, $V_{DD} = 5\,V$	8.83	9.60	10.37	ms
		$R_X = 100\,k\Omega$, $C_X = 0.1\,\mu F$, $V_{DD} = 10\,V$	9.02	9.80	10.59	ms
		$R_X = 100\,k\Omega$, $C_X = 0.1\,\mu F$, $V_{DD} = 15\,V$	9.20	10.00	10.80	ms
		$R_X = 100\,k\Omega$, $C_X = 10.0\,\mu F$, $V_{DD} = 5\,V$	0.87	0.95	1.03	s
		$R_X = 100\,k\Omega$, $C_X = 10.0\,\mu F$, $V_{DD} = 10\,V$	0.89	0.97	1.05	s
		$R_X = 100\,k\Omega$, $C_X = 10.0\,\mu F$, $V_{DD} = 15\,V$	0.91	0.99	1.07	s
Pulse Width Match between circuits in the same package $C_X = 0.1\,\mu F$, $R_X = 100\,k\Omega$		$R_X = 100\,k\Omega$, $C_X = 0.1\,\mu F$, $V_{DD} = 5\,V$		±1		%
		$R_X = 100\,k\Omega$, $C_X = 0.1\,\mu F$, $V_{DD} = 10\,V$		±1		%
		$R_X = 100\,k\Omega$, $C_X = 0.1\,\mu F$, $V_{DD} = 15\,V$		±1		%

Operating Conditions

R_X	External Timing Resistance		5.0		*	kΩ
C_X	External Timing Capacitance		0		No Limit	pF

*The maximum usable resistance R_X is a function of the leakage of the Capacitor C_X, leakage of the CD4538B, and leakage due to board layout, surface resistance, etc.

Logic Diagram

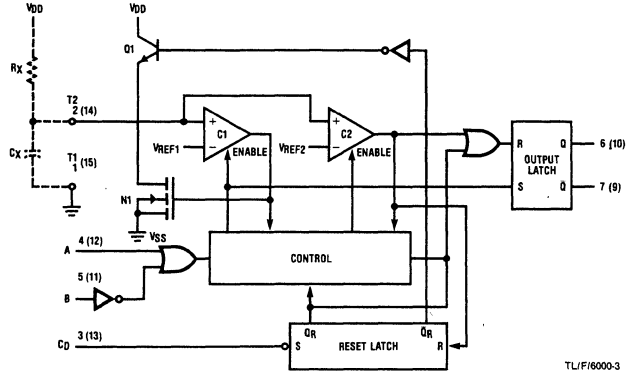


Figure 1

Theory of Operation

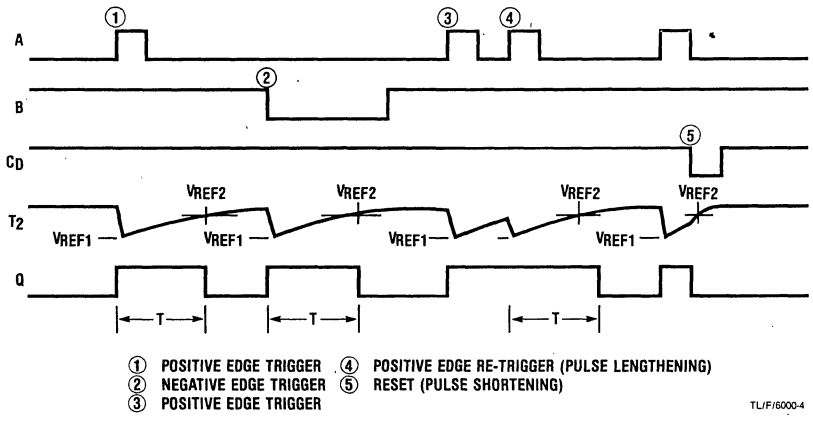


Figure 2

Trigger Operation

The block diagram of the CD4538B is shown in Figure 1, with circuit operation following.

As shown in Figures 1 and 2, before an input trigger occurs, the monostable is in the quiescent state with the Q output low, and the timing capacitor C_X completely charged to V_{DD}. When the trigger input A goes from V_{SS} to V_{DD} (while inputs B and C_D are held to V_{DD}) a valid trigger is recognized, which turns on comparator C1 and N-Channel transistor N1①. At the same time the output latch is set. With transistor N1 on, the capacitor C_X rapidly discharges toward V_{SS} until V_{REF1} is reached. At this point the output of comparator C1 changes state and transistor N1 turns off. Comparator C1 then turns off while at the same time comparator C2 turns on. With transistor N1 off, the capacitor C_X begins to charge through the timing resistor, R_X, toward V_{DD}. When the voltage across C_X equals V_{REF2}, comparator C2 changes state causing the output latch to reset (Q goes low) while at the same time disabling comparator C2. This ends the timing cycle with the monostable in the quiescent state, waiting for the next trigger.

A valid trigger is also recognized when trigger input B goes from V_{DD} to V_{SS} (while input A is at V_{SS} and input C_D is at V_{DD})②.

It should be noted that in the quiescent state C_X is fully charged to V_{DD} causing the current through resistor R_X to be zero. Both comparators are "off" with the total device current due only to reverse junction leakages. An added feature of the CD4538B is that the output latch is set via the input trigger without regard to the capacitor voltage. Thus, propagation delay from trigger to Q is independent of the value of C_X, R_X, or the duty cycle of the input waveform.

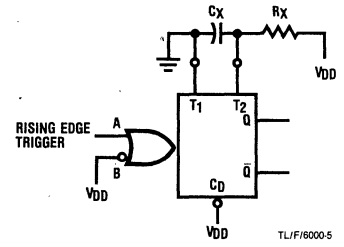
Retrigger Operation

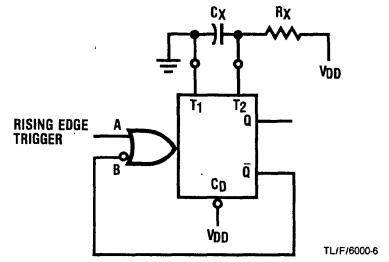
The CD4538B is retriggered if a valid trigger occurs③followed by another valid trigger④before the Q output has returned to the quiescent (zero) state. Any retrigger, after the timing node voltage at pin 2 or 14 has begun to rise from V_{REF1}, but has not yet reached V_{REF2}, will cause an increase in output pulse width T. When a valid retrigger is initiated④ the voltage at T2 will again drop to V_{REF1} before progressing along the RC charging curve toward V_{DD}. The Q output will remain high until time T, after the last valid retrigger.

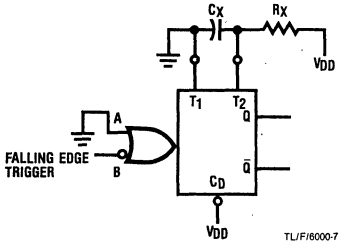
Reset Operation

The CD4538B may be reset during the generation of the output pulse. In the reset mode of operation, an input pulse on C_D sets the reset latch and causes the capacitor to be fast charged to V_{DD} by turning on transistor Q1 ⑤. When the voltage on the capacitor reaches V_{REF2}, the reset latch will clear and then be ready to accept another pulse. If the C_D input is held low, any trigger inputs that occur will be inhibited and the Q and $\overline{Q}$ outputs of the output latch will not change. Since the Q output is reset when an input low level is detected on the C_D input, the output pulse T can be made significantly shorter than the minimum pulse width specification.

Typical Applications







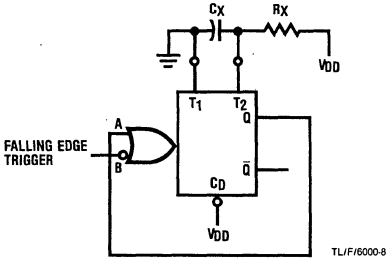


Figure 3. Retriggerable Monostables Circuitry

Figure 4. Non-retriggerable Monostables Circuitry

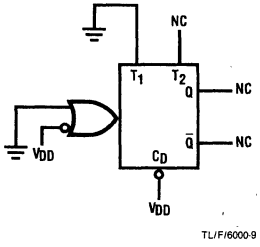


Figure 5. Connection of Unused Sections

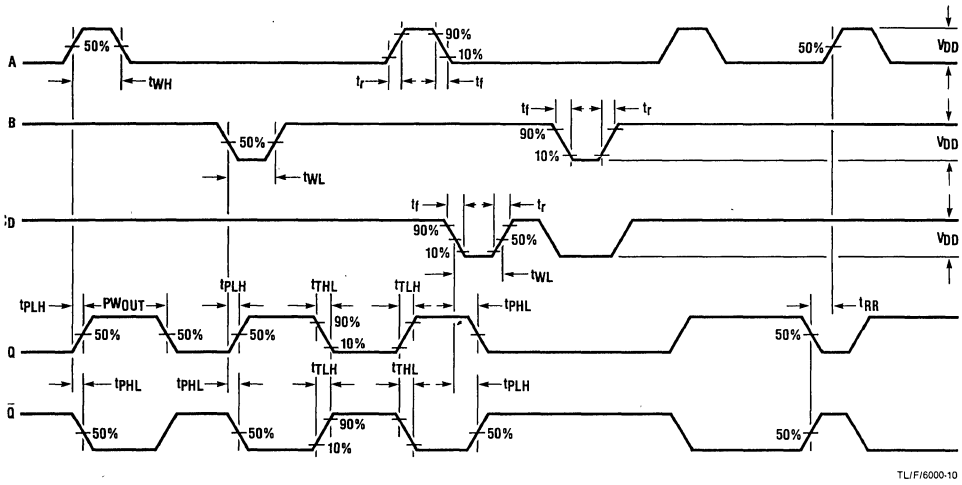
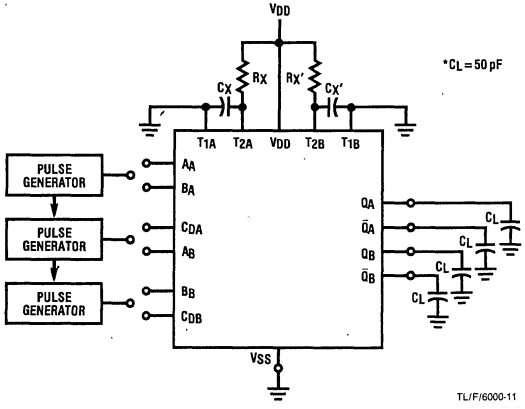
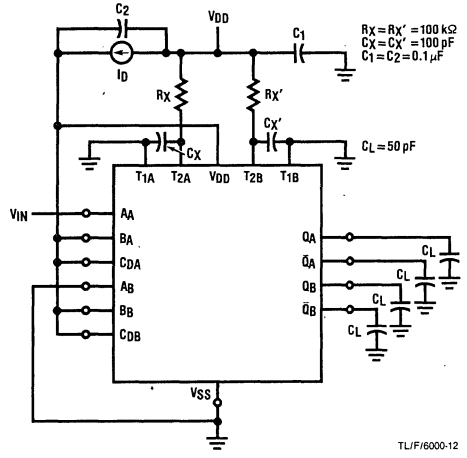


Figure 6. Switching Test Waveforms





INPUT CONNECTIONS

CHARACTERISTICS	CD	A	B
tPLH, tPHL, tTLH, tTHL, PWOUT, tWH, tWL	VDD	PG1	VDD
tPLH, tPHL, tTLH, tTHL, PWOUT, tWH, tWL	VDD	VSS	PG2
tPLH(R), tPHL(R), tWH, tWL	PG3	PG1	PG2

*INCLUDES CAPACITANCE OF PROBES, WIRING, AND FIXTURE PARASITIC

NOTE: SWITCHING TEST WAVEFORMS FOR PG1, PG2, PG3 ARE SHOWN IN FIGURE 6.

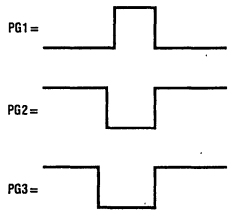


Figure 7. Switching Test Circuit

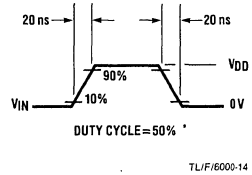


Figure 8. Power Dissipation Test Circuit and Waveforms

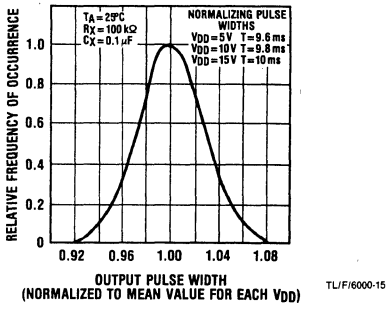


Figure 9. Typical Normalized Distribution of Units for Output Pulse Width

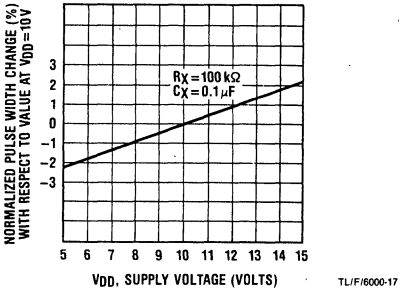


Figure 10. Typical Pulse Width Variation as a Function of Supply Voltage V_{DD}

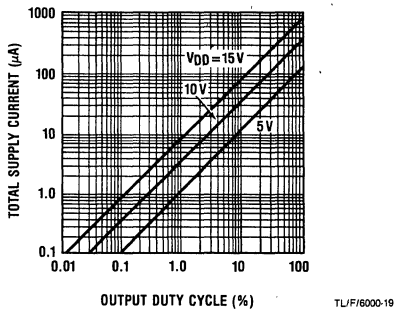


Figure 11. Typical Total Supply Current Versus Output Duty Cycle, $R_X = 100\,k\Omega$, $C_L = 50\,pF$, $C_X = 100\,pF$, One Monostable Switching Only

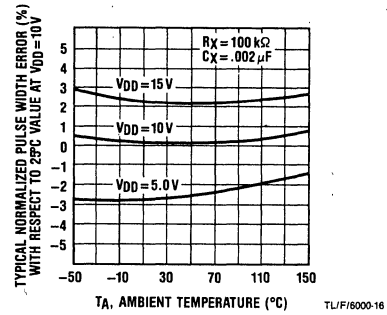


Figure 12. Typical Pulse Width Error Versus Temperature

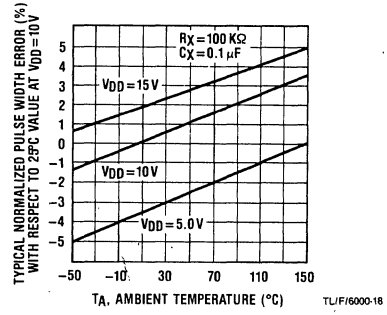


Figure 13. Typical Pulse Width Error Versus Temperature

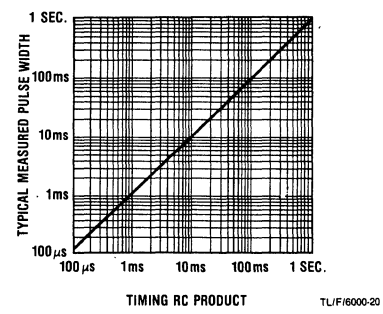


Figure 14. Typical Pulse Width Versus Timing RC Product

National Semiconductor

CD4541BM/CD4541BC Programmable Timer

General Description

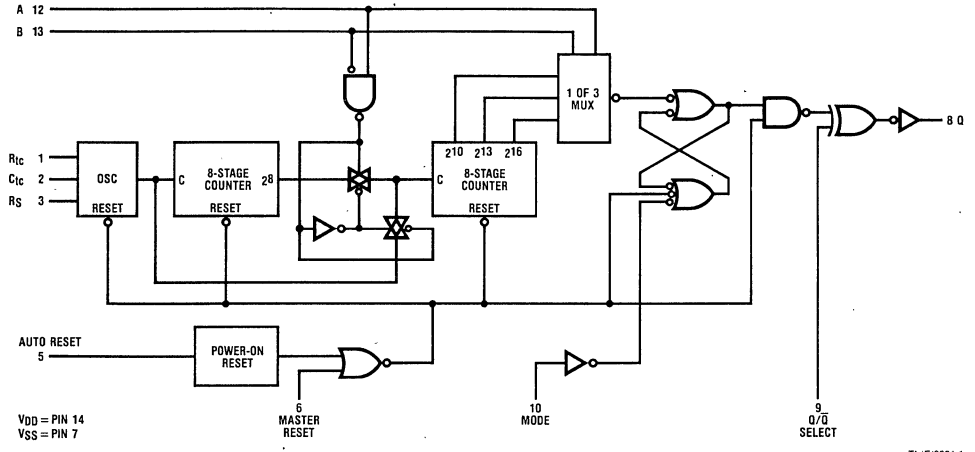
The CD4541B Programmable Timer is designed with a 16-stage binary counter, an integrated oscillator for use with an external capacitor and two resistors, output control logic, and a special power-on reset circuit. The special features of the power-on reset circuit are first, no additional static power consumption and second, the part functions across the full voltage range (3-15V) whether power-on reset is enabled or disabled.

Timing and the counter are initialized by turning on power, if the power-on reset is enabled. When the power is already on, an external reset pulse will also initialize the timing and counter. After either reset is accomplished, the oscillator frequency is determined by the external RC network. The 16-stage counter divides the oscillator frequency by any of 4 digitally controlled division ratios.

Features

- Available division ratios 2^8, 2^{10}, 2^{13}, or 2^{16}
- Increments on positive edge clock transitions
- Built-in low power RC oscillator (±2% accuracy over temperature range and ±10% supply and ±3% over processing @ < 10kHz)
- Oscillator frequency range ≈ DC to 100kHz
- Oscillator may be bypassed if external clock is available (apply external clock to pin 3)
- Automatic reset initializes all counters when power turns on
- External master reset totally independent of automatic reset operation
- Operates as 2^n frequency divider or single transition timer
- Q/$\overline{Q}$ select provides output logic level flexibility
- Reset (auto or master) disables oscillator during resetting to provide no active power dissipation
- Clock conditioning circuit permits operation with very slow clock rise and fall times
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} (typ.)
- 5V-10V-15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15V over full temperature range
- High output drive (pin 8) min. one TTL load

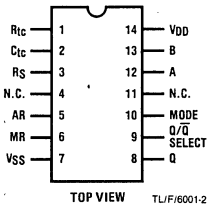
Logic Diagram



TL/F/6001-1

Connection Diagram

Dual-In-Line Package



N.C. — NOT CONNECTED

TOP VIEW TL/F/6001-2

Order Number CD4541BMJ or CD4541BCJ
See NS Package J14A

Order Number CD4541BMN or CD4541BCN
See NS Package N14A

Absolute Maximum Ratings (Notes 1 & 2)

Supply Voltage, V_{DD}	−0.5 to +18V
Input Voltage, V_{IN}	−0.5 to V_{DD} + 0.5V
Storage Temperature Range, T_S	−65°C to +150°C
Package Dissipation, P_D	500 mW
Lead Temperature, T_L (soldering, 10 seconds)	260°C

Recommended Operating Conditions (Note 2)

Supply Voltage, V_{DD}	3 to 15V
Input Voltage, V_{IN}	0 to V_{DD}
Operating Temperature Range	
CD4541BM	−55°C to +125°C
CD4541BC	−40°C to +85°C

DC Electrical Characteristics (Note 2) — CD4541BM

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5		0.005	5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10		0.010	10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V $\|I_O\| < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V $\|I_O\| < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	2.85		2.27	3.6		1.6		mA
		V_{DD} = 10V, V_O = 0.5V	4.96		4.0	9.0		2.8		mA
		V_{DD} = 15V, V_O = 1.5V	19.3		15.6	34.0		10.9		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 2.5V	7.96		6.42	13.0		4.49		mA
		V_{DD} = 10V, V_O = 9.5V	4.19		3.38	8.0		2.37		mA
		V_{DD} = 15V, V_O = 13.5V	16.3		13.2	30.0		9.24		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

DC Electrical Characteristics (Note 2) — CD4541BC

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20		0.005	20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40		0.010	40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V $\|I_O\| < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V $\|I_O\| < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	2.32		1.96	3.6		1.6		mA
		V_{DD} = 10V, V_O = 0.5V	3.18		2.66	9.0		2.18		mA
		V_{DD} = 15V, V_O = 1.5V	12.4		10.4	34.0		8.50		mA

DC Electrical Characteristics (Note 2) — CD4541BC (Cont'd)

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5V$, $V_O=2.5V$	5.1		4.27	13.0		3.5		mA
		$V_{DD}=10V$, $V_O=9.5V$	2.69		2.25	8.0		1.85		mA
		$V_{DD}=15V$, $V_O=13.5V$	10.5		8.8	30.0		7.22		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics $T_A=25°C$, $C_L=50pF$ (refer to test circuits)

Sym	Parameter	Conditions	Min	Typ	Max	Units
t_{TLH}	Output Rise Time	$V_{DD}=5V$		50	200	ns
		$V_{DD}=10V$		30	100	ns
		$V_{DD}=15V$		25	80	ns
t_{THL}	Output Fall Time	$V_{DD}=5V$		50	200	ns
		$V_{DD}=10V$		30	100	ns
		$V_{DD}=15V$		25	80	ns
t_{PLH}, t_{PHL}	Turn-Off, Turn-On Propagation Delay, Clock to Q (2^8 Output)	$V_{DD}=5V$		1.8	4.0	μs
		$V_{DD}=10V$		0.6	1.5	μs
		$V_{DD}=15V$		0.4	1.0	μs
t_{PHL}, t_{PLH}	Turn-On, Turn-Off Propagation Delay, Clock to Q (2^{16} Output)	$V_{DD}=5V$		3.2	8.0	μs
		$V_{DD}=10V$		1.5	3.0	μs
		$V_{DD}=15V$		1.0	2.0	μs
$t_{WH(CL)}$	Clock Pulse Width	$V_{DD}=5V$	400	200		ns
		$V_{DD}=10V$	200	100		ns
		$V_{DD}=15V$	150	70		ns
f_{CL}	Clock Pulse Frequency	$V_{DD}=5V$		2.5	1.0	MHz
		$V_{DD}=10V$		6.0	3.0	MHz
		$V_{DD}=15V$		8.5	4.0	MHz
$t_{WH(R)}$	MR Pulse Width	$V_{DD}=5V$	400	170		ns
		$V_{DD}=10V$	200	75		ns
		$V_{DD}=15V$	150	50		ns
C_I	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)			100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

Truth Table

Pin	State	
	0	1
5	Auto Reset Operating	Auto Reset Disabled
6	Timer Operational	Master Reset On
9	Output Initially Low after Reset	Output Initially High after Reset
10	Single Cycle Mode	Recycle Mode

Division Ratio Table

A	B	Number of Counter Stages n	Count 2^n
0	0	13	8192
0	1	10	1024
1	0	8	256
1	1	16	65536

Operating Characteristics

With Auto Reset pin set to a "0" the counter circuit is initialized by turning on power. Or with power already on, the counter circuit is reset when the Master Reset pin is set to a "1". Both types of reset will result in synchronously resetting all counter stages independent of counter state.

The RC oscillator frequency is determined by the external RC network, i.e.:

$$f = \frac{1}{2.3\ R_{tc}C_{tc}} \quad \text{if } (1\,kHz \leqslant f \leqslant 100\,kHz)$$

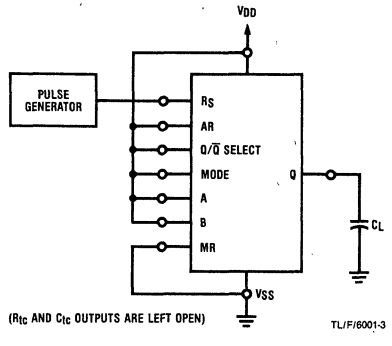
and $R_S \approx 2R_{tc}$ where $R_S \geqslant 10\,k\Omega$

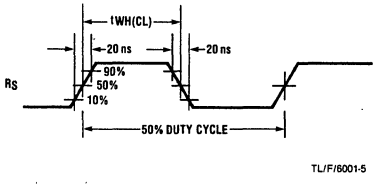
The time select inputs (A and B) provide a two-bit address to output any one of four counter stages (2^8, 2^{10}, 2^{13}, and 2^{16}). The 2^n counts as shown in the Division Ratio Table represent the Q output of the Nth stage of the counter. When A is "1", 2^{16} is selected for both states of B. However, when B is "0", normal counting is interrupted and the 9th counter stage receives its clock directly from the oscillator (i.e., effectively outputting 2^8).

The Q/$\overline{Q}$ select output control pin provides for a choice of output level. When the counter is in a reset condition and Q/$\overline{Q}$ select pin is set to a "0" the Q output is a "0". Correspondingly, when Q/$\overline{Q}$ select pin is set to a "1" the Q output is a "1".

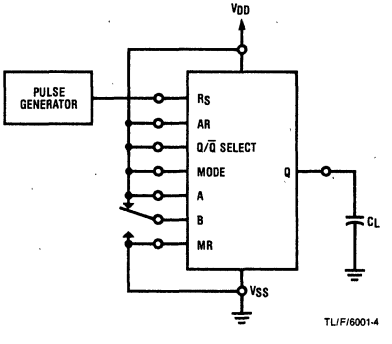
When the mode control pin is set to a "1", the selected count is continually transmitted to the output. But, with mode pin "0" and after a reset condition the RS flip-flop resets (see Logic Diagram), counting commences and after 2^{n-1} counts the RS flip-flop sets which causes the output to change state. Hence, after another 2^{n-1} counts the output will not change. Thus, a Master Reset pulse must be applied or a change in the mode pin level is required to reset the single cycle operation.

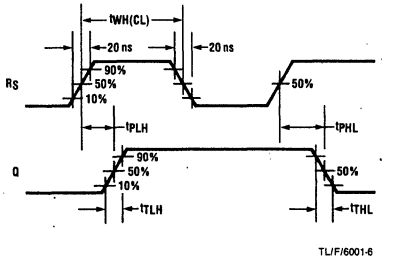
Power Dissipation Test Circuit and Waveform



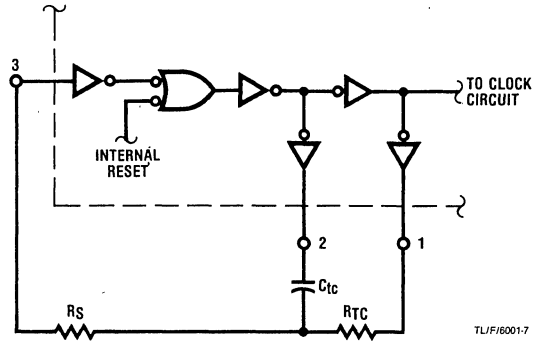


Switching Time Test Circuit and Waveforms

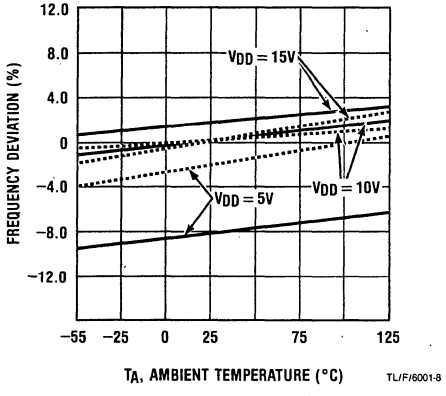




Oscillator Circuit Using RC Configuration



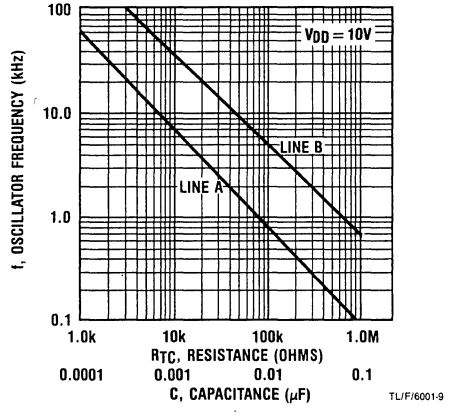
Typical RC Oscillator Characteristics



SOLID LINE = R_{TC} = 56 kΩ, R_S = 1 kΩ AND C = 1000 pF
f = 10.2 kHz @ V_{DD} = 10V AND T_A = 25°C

DASHED LINE = R_{TC} = 56 kΩ, R_S = 120 kΩ AND C = 1000 pF
f = 7.75 kHz @ V_{DD} = 10V AND T_A = 25°C

RC Oscillator Frequency as a Function of R_{TC} and C



LINE A: f AS A FUNCTION OF C AND (R_{TC} = 56 kΩ; R_S = 120k)
LINE B: f AS A FUNCTION OF R_{TC} AND (C = 1000 pF; R_S = 2 R_{TC})

National Semiconductor

CD4543BM/CD4543BC BCD-to-7-Segment Latch/Decoder/Driver for Liquid Crystals

General Description

The CD4543BM/CD4543BC is a monolithic CMOS BCD-to-7-segment latch/decoder/driver for use with liquid crystal and other types of displays. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-7-segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI) and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display, and the outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts, such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Features

■ Wide supply voltage range	3.0 V to 18 V
■ High noise immunity	0.45 V_{DD} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Low power dissipation	50 nA/package (typ.) at V_{DD} = 5.0 V

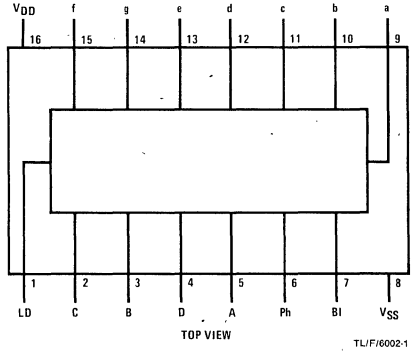
- Latch storage
- Blanking input
- Blank for all illegal inputs
- Direct-drive LCD, LED and VF displays
- Pin-for-pin replacement for CD4056B (with pin 7 tied to V_{SS})
- Pin-for-pin replacement for Motorola MC14543B

Applications

- Instrument (e.g., counter, DVM, etc.) display driver
- Computer/calculator display driver
- Cockput display driver
- Various clock, watch, and timer users

Connection Diagram and Truth Table

Dual-In-Line Package



TOP VIEW

TL/F/6002-1

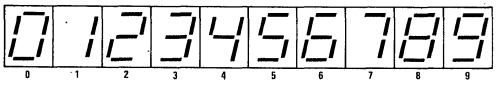
Order Number CD4543BMJ or CD4543BCJ
See NS Package J16A

Order Number CD4543BMN or CD4543BCN
See NS Package N16E

INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as Above

X = Don't care
† = Above combinations
* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.

Display Format



TL/F/6002-2

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 V_{DC} to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4543BM	−55°C to +125°C
CD4543BC	−40°C to +85°C

DC Electrical Characteristics CD4543BM (Note 2)

SYM	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		5			5		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		10			10		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51			0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3			0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4			2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4543BC (Note 2)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V, V_{IN} = V_{DD} or V_{SS}		20			20		150	μA
		V_{DD} = 10V, V_{IN} = V_{DD} or V_{SS}		40			40		300	μA
		V_{DD} = 15V, V_{IN} = V_{DD} or V_{SS}		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44			0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1			0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0			2.4		mA

5

DC Electrical Characteristics CD4543BC (Note 2) (Continued)

SYM	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, V_{SS} = 0, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_r	Output Rise Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_f	Output Fall Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PLH}	Turn-ON Propagation Delay Time	V_{DD} = 5V		450	1100	ns
		V_{DD} = 10V		170	440	ns
		V_{DD} = 15V		110	330	ns
t_{PHL}	Turn-OFF Propagation Delay Time	V_{DD} = 5V		500	1100	ns
		V_{DD} = 10V		180	440	ns
		V_{DD} = 15V		120	330	ns
t_{SET-UP}	Set-Up Time	V_{DD} = 5V		−5	80	ns
		V_{DD} = 10V		−2	30	ns
		V_{DD} = 15V		0	20	ns
t_{HOLD}	Hold Time	V_{DD} = 5V		30	120	ns
		V_{DD} = 10V		20	45	ns
		V_{DD} = 15V		15	30	ns
PW_{LD}	Latch Disable Pulse Width	V_{DD} = 5V		50	250	ns
		V_{DD} = 10V		30	100	ns
		V_{DD} = 15V		20	80	ns
C_{IN}	Input Capacitance	Per Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	See C_{PD} Measurement Waveforms, (Note 4)		300		pF

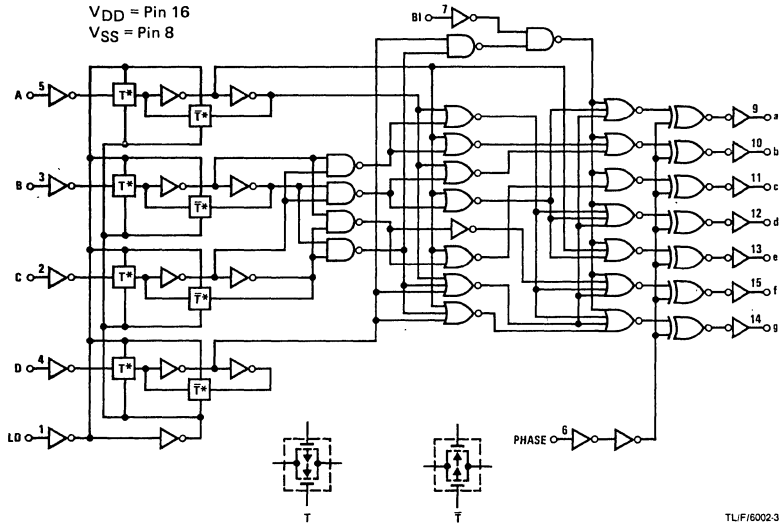
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: C_{PD} determines the no load AC power consumption of a CMOS device. For a complete explanation, see "MM54C/74C Family Characteristics" application note AN-90.

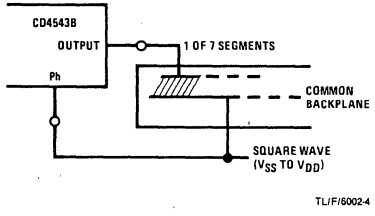
Logic Diagram



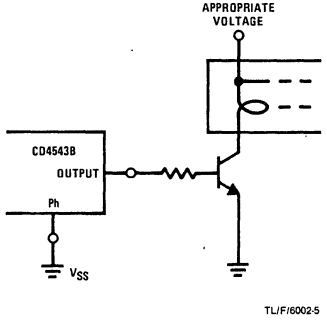
*Transmission gates

Typical Applications

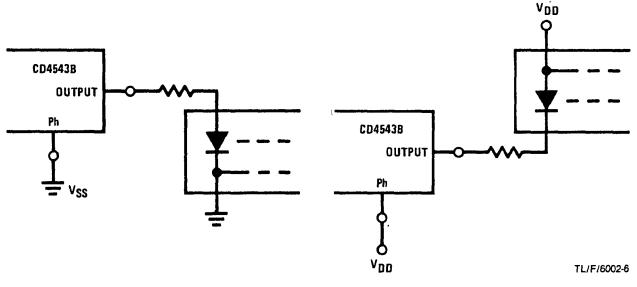
Liquid Crystal (LC) Readout



Incandescent Readout



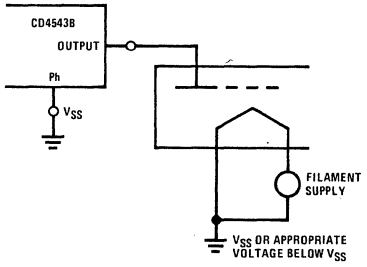
Light Emitting Diode (LED) Readout



Note. Bipolar transistors may be added for gain (for $V_{DD} \leq 10V$ or $I_{OUT} \geq 10$ mA)

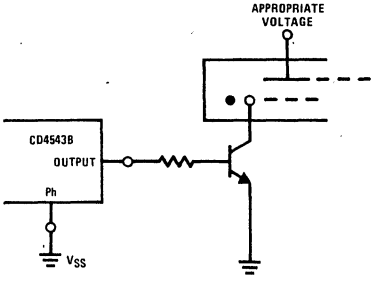
Typical Applications (Continued)

Fluorescent Readout



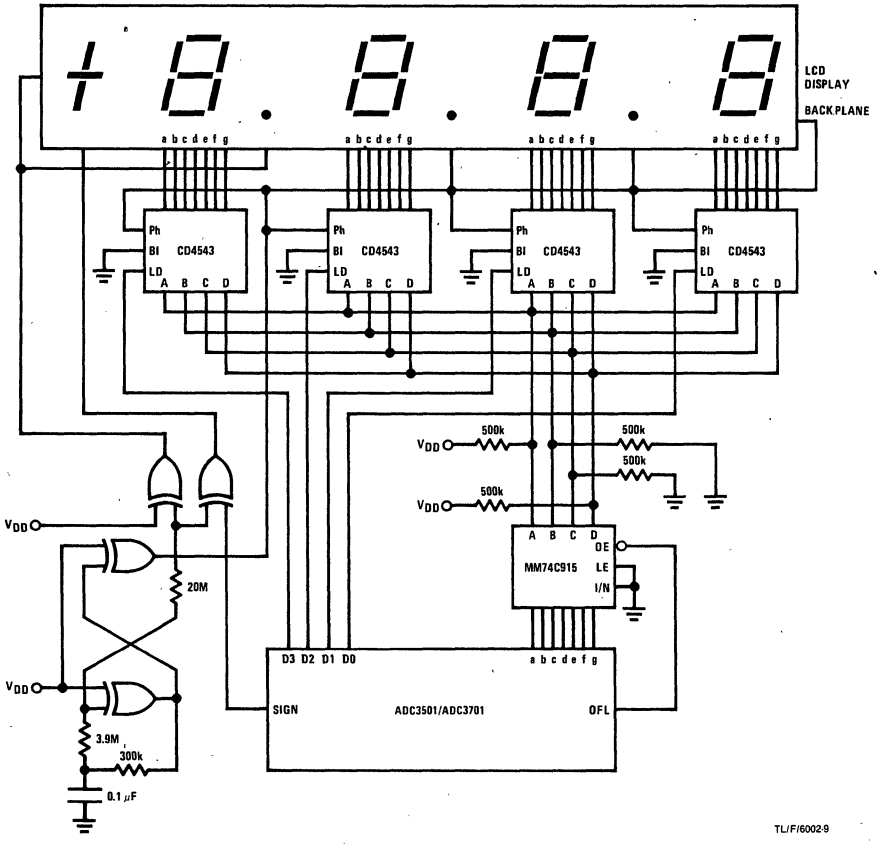
TL/F/6002-7

Gas Discharge Readout



TL/F/6002-8

3 1/2-Digit DVM with LCD Display

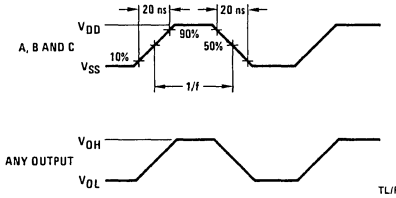


TL/F/6002-9

Display 9.999 when overflowed. All digits can also be blanked at overflow by tying OFL to BI on the CD4543's

Switching Time Waveforms

C_{PD} Measurement Waveforms

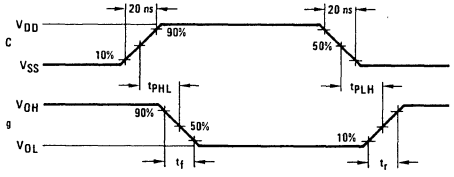


TL/F/6002-10

Inputs BI and Ph low, and inputs D and LD high. f in respect to a system clock.
All outputs connected to respective C_L loads.

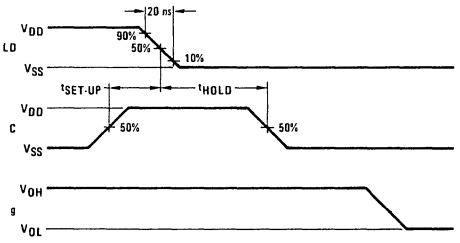
Dynamic Signal Waveforms

(a) Inputs D, Ph and BI low, and inputs A, B and LD high



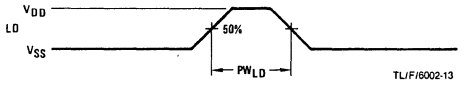
TL/F/6002-11

(b) Inputs D, Ph and BI low, and inputs A and B high



TL/F/6002-12

(c) Data DCBA strobe into latches



TL/F/6002-13

National Semiconductor

CD4723BM/CD4723BC Dual 4-Bit Addressable Latch CD4724BM/CD4724BC 8-Bit Addressable Latch

General Description

The CD4723B is a dual 4-bit addressable latch with common control inputs, including two address inputs (A0, A1), an active low enable input ($\overline{E}$), and an active high clear input (CL). Each latch has a data input (D) and four outputs (Q0-Q3). The CD4724B is an 8-bit addressable latch with three address inputs (A0-A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D) and eight outputs (Q0-Q7).

Data is entered into a particular bit in the latch when that is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry is inhibited when enable ($\overline{E}$) is high.

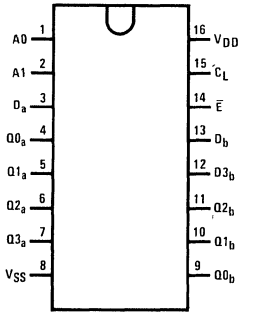
When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high and enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = low), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = high, CL = low).

Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

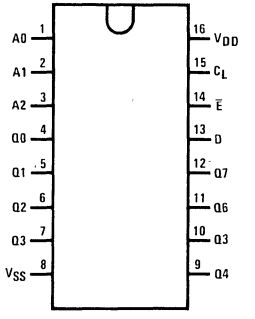
Connection Diagrams

CD4723B
Dual-In-Line Package



TOP VIEW TL/F/6003-1

CD4724B
Dual-In-Line Package



TOP VIEW TL/F/6003-2

Order Number CD4723BMJ, CD4723BCJ, CD4724BMJ or CD4724BCJ
See NS Package J16A

Order Number CD4723BMN, CD4723BCN, CD4724BMN or CD4724BCN
See NS Package N16E

Truth Table

MODE SELECTION				
$\overline{E}$	CL	ADDRESSED LATCH	UNADDRESSED LATCH	MODE
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Holds Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

Absolute Maximum Ratings
(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions
(Note 2)

V_{DD} DC Supply Voltage	3.0 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4723BM/CD4724BM	−55°C to +125°C
CD4723BC/CD4724BC	−40°C to +85°C

DC Electrical Characteristics CD4723BM/CD4724BM (Note 2)

Sym	Parameter	Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0 V		5.0		0.02	5.0		150	μA
		V_{DD} = 10 V		10		0.02	10		300	μA
		V_{DD} = 15 V		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	V_{DD} = 5.0 V, V_O = 4.6 V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4723BC/CD4724BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5.0 V		20		0.02	20		150	μA
		V_{DD} = 10 V		40		0.02	40		300	μA
		V_{DD} = 15 V		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\mu A$								
		V_{DD} = 5.0 V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5.0 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics (Cont'd.) CD4723BC/CD4724BC (Note 2)

Sym	Parameter	Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{OL}	Low Level Output Current (Note 3)	$V_{DD}=5.0V$, $V_O=0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD}=10V$, $V_O=0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD}=15V$, $V_O=1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (Note 3)	$V_{DD}=5.0V$, $V_O=4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD}=10V$, $V_O=9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD}=15V$, $V_O=13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD}=15V$, $V_{IN}=0V$		−0.30		-10^{-5}	−0.30		−1.0	μA
		$V_{DD}=15V$, $V_{IN}=15V$		0.30		10^{-5}	0.30		1.0	μA

AC Electrical Characteristics $T_A=25°C$, $C_L=50pF$, $R_L=200k$, Input $t_r=t_f=20ns$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Date to Output	$V_{DD}=5.0V$		200	400	ns
		$V_{DD}=10V$		75	150	ns
		$V_{DD}=15V$		50	100	ns
t_{PLH}, t_{PHL}	Propagation Delay Enable to Output	$V_{DD}=5.0V$		200	400	ns
		$V_{DD}=10V$		80	160	ns
		$V_{DD}=15V$		60	120	ns
t_{PHL}	Propagation Delay Clear to Output	$V_{DD}=5.0V$		175	350	ns
		$V_{DD}=10V$		80	160	ns
		$V_{DD}=15V$		65	130	ns
t_{PLH}, t_{PHL}	Propagation Delay Address to Output	$V_{DD}=5.0V$		225	450	ns
		$V_{DD}=10V$		100	200	ns
		$V_{DD}=15V$		75	150	ns
t_{THL}, t_{TLH}	Transition Time (Any Output)	$V_{DD}=5.0V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
t_{WH}, T_{WL}	Minimum Data Pulse Width	$V_{DD}=5.0V$		100	200	ns
		$V_{DD}=10V$		50	100	ns
		$V_{DD}=15V$		40	80	ns
t_{WH}, t_{WL}	Minimum Address Pulse Width	$V_{DD}=5.0V$		200	400	ns
		$V_{DD}=10V$		100	200	ns
		$V_{DD}=15V$		65	125	ns
t_{WH}	Minimum Clear Pulse Width	$V_{DD}=5.0V$		75	150	ns
		$V_{DD}=10V$		40	75	ns
		$V_{DD}=15V$		25	50	ns
t_{SU}	Minimum Set-Up Time Data to E	$V_{DD}=5.0V$		40	80	ns
		$V_{DD}=10V$		20	40	ns
		$V_{DD}=15V$		15	30	ns
t_H	Minimum Hold Time Data to E	$V_{DD}=5.0V$		60	120	ns
		$V_{DD}=10V$		30	60	ns
		$V_{DD}=15V$		25	50	ns
t_{SU}	Minimum Set-Up Time Address to E	$V_{DD}=5.0V$		−15	50	ns
		$V_{DD}=10V$		0	30	ns
		$V_{DD}=15V$		0	20	ns
t_H	Minimum Hold Time Address to E	$V_{DD}=5.0V$		−50	15	ns
		$V_{DD}=10V$		−20	10	ns
		$V_{DD}=15V$		−15	5	ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		100		pF
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

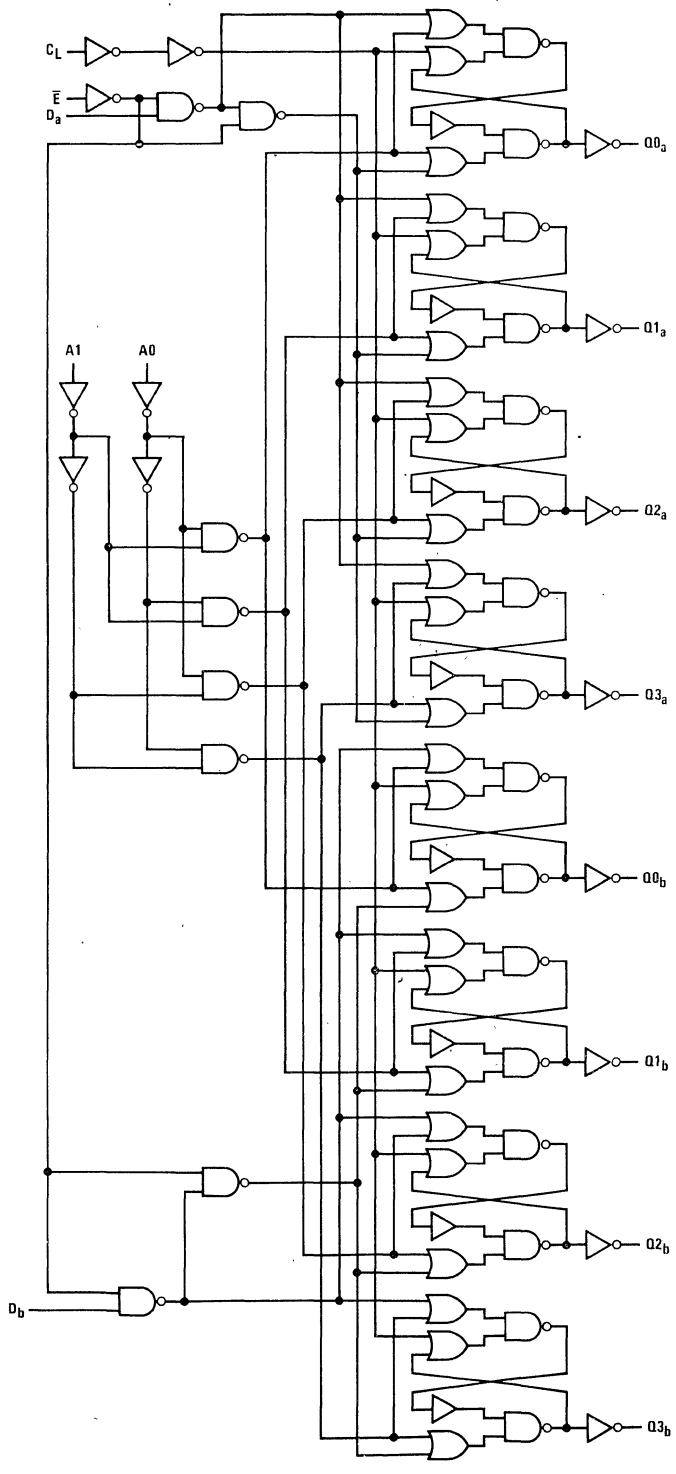
Note 2: $V_{SS}=0V$ unless otherwise specified.

Note 3: I_{OH} and I_{OL} are tested one output at a time.

Note 4: Dynamic power dissipation (P_D) is given by: $P_D=(C_{PD}+C_L)V_{CC}^2f+P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see application note AN-90, "54C/74C Family Characteristics".

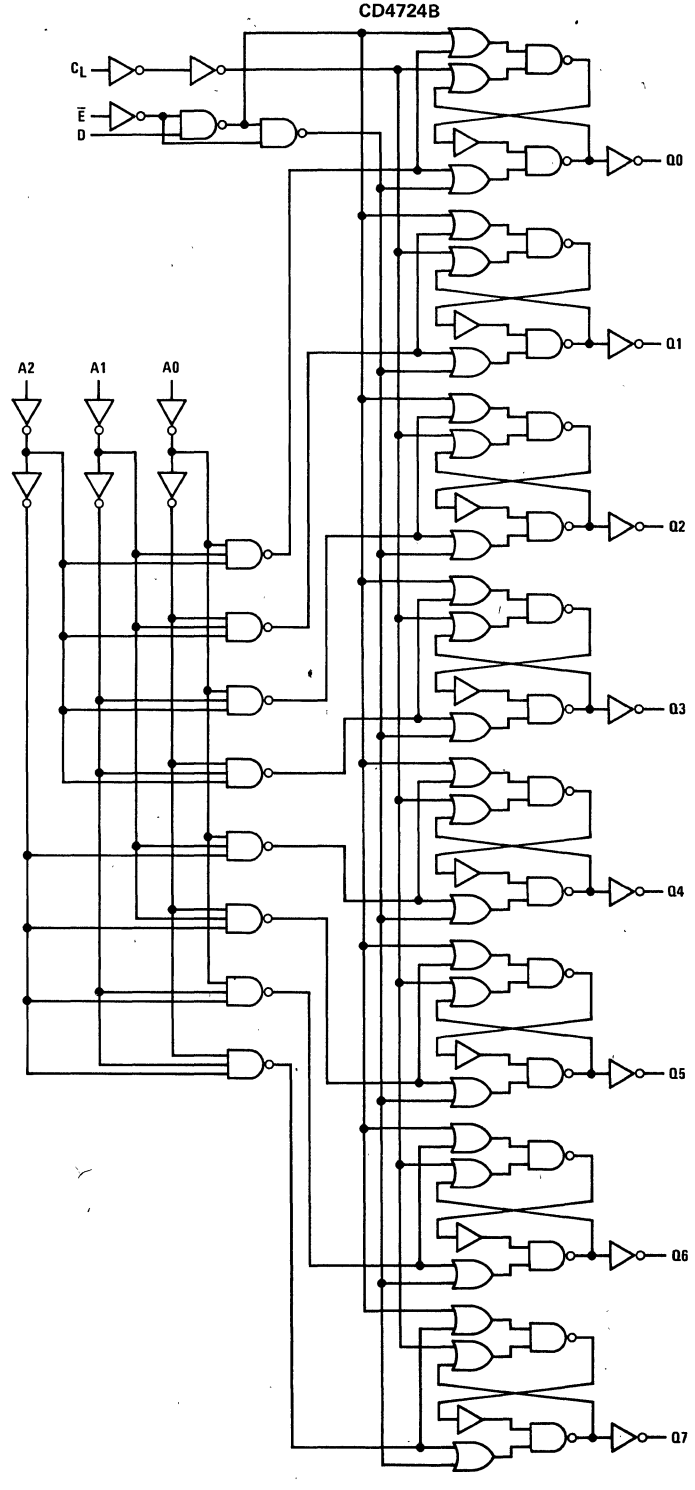
Logic Diagrams

CD4723B

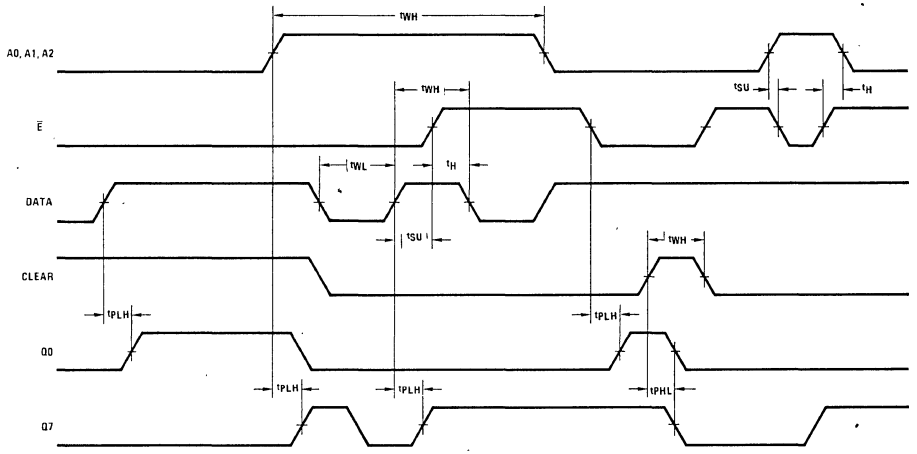


TL/F/6003-3

Logic Diagrams (Cont'd.)



Switching Time Waveforms



TL/F/6003-5

Section 6
MM54CXXX/
MM74CXXX

6

Section Contents

Section Contents (Continued)

National Semiconductor

MM54C00/MM74C00 Quad 2-Input NAND Gate
MM54C02/MM74C02 Quad 2-Input NOR Gate
MM54C04/MM74C04 Hex Inverter
MM54C10/MM74C10 Triple 3-Input NAND Gate
MM54C20/MM74C20 Dual 4-Input NAND Gate

General Description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

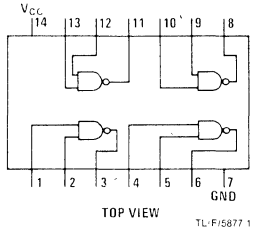
Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power consumption	10 nW/package (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagrams

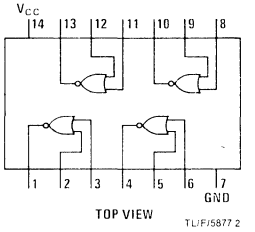
Dual-In-Line Packages

MM54C00/MM74C00



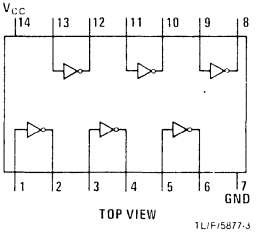
Order Number MM54C00J, MM74C00J, MM54C00N or MM74C00N
See NS Package J14A or N14A

MM54C02/MM74C02



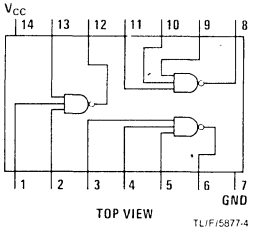
Order Number MM54C02J, MM74C02J, MM54C02N or MM74C02N
See NS Package J14A or N14A

MM54C04/MM74C04



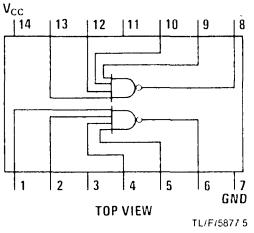
Order Number MM54C04J, MM74C04J, MM54C04N or MM74C04N
See NS Package J14A or N14A

MM54C10/MM74C10



Order Number MM54C10J, MM74C10J, MM54C10N or MM74C10N
See NS Package J14A or N14A

MM54C20/MM74C20



Order Number MM54C20J, MM74C20J, MM54C20N or MM74C20N
See NS Package J14A or N14A

Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Operating V_{CC} Range	3.0V to 15V
Operating Temperature Range		Maximum V_{CC} Voltage	18V
54C	$-55°C$ to $+125°C$	Package Dissipation	500 mW
74C	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.01	15	μA
Low Power to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-10\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-10\mu A$	4.4 4.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=+10\mu A$ 74C, $V_{CC}=4.75V$, $I_O=+10\mu A$			0.4 0.4	V V
CMOS to Low Power						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	4.0 4.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			1.0 1.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0V$, $V_{IN(1)}=5.0V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10V$, $V_{IN(1)}=10V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics

$T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		50	90	ns
		$V_{CC} = 10V$		30	60	ns
C_{IN}	Input Capacitance	(Note 2)		6.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate or Inverter		12		pF
MM54C10/MM74C10						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		60	100	ns
		$V_{CC} = 10V$		35	70	ns
C_{IN}	Input Capacitance	(Note 2)		7.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		18		pF
MM54C20/MM74C20						
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		70	115	ns
		$V_{CC} = 10V$		40	80	ns
C_{IN}	Input Capacitance	(Note 2)		9		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		30		pF

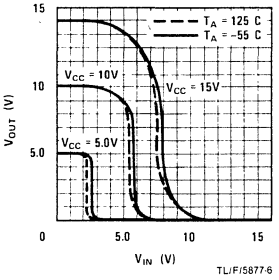
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

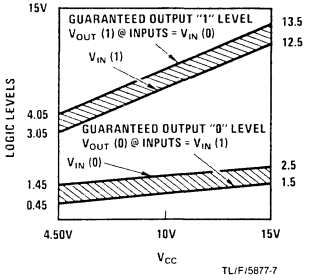
Typical Performance Characteristics

Gate Transfer Characteristics



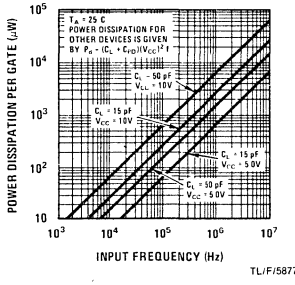
TL/F/5877-6

Guaranteed Noise Margin Over Temperature vs V_{CC}



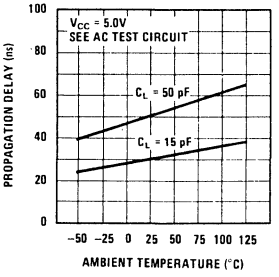
TL/F/5877-7

Power Dissipation vs Frequency MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



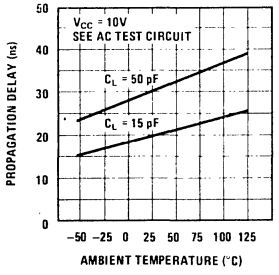
TL/F/5877-8

Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



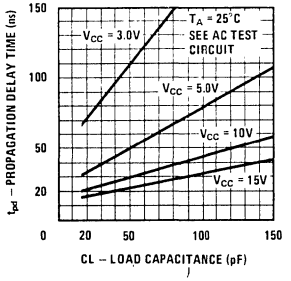
TL/F/5877-9

Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



TL/F/5877-10

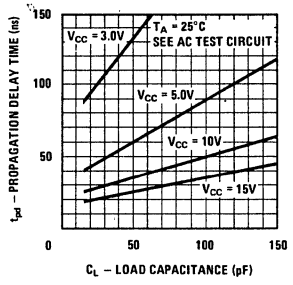
Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



TL/F/5877-11

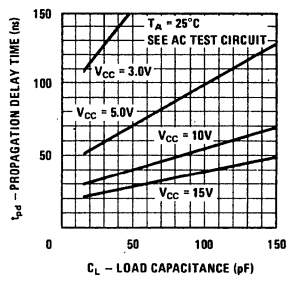
Typical Performance Characteristics (Cont'd)

Propagation Delay Time vs Load Capacitance MM54C10/MM74C10



TL/F/5877-12

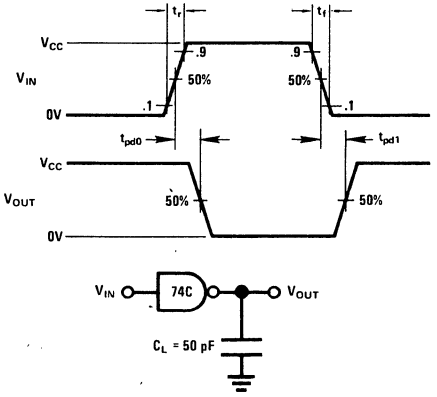
Propagation Delay Time vs Load Capacitance MM54C20/MM74C20



TL/F/5877-13

Switching Time Waveforms and AC Test Circuit

CMOS to CMOS



NOTE: DELAYS MEASURED WITH INPUT t_r, $t_f \leq 20$ ns.

TL/F/5877-14

National Semiconductor

MM54C08/MM74C08 Quad 2-Input AND Gate

General Description

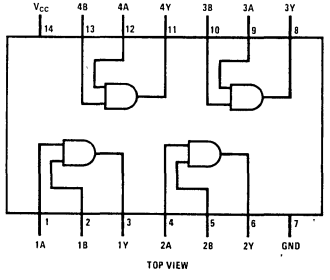
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin, these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	10 nW/package (typ.)

Connection Diagram and Truth Table

Dual-In-Line Package



TL/F/5878-1

Order Number MM54C08J or MM74C08J
See NS Package J14A

Order Number MM54C08N or MM74C08N
See NS Package N14A

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Level L= Low Level

6

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C08, MM54C86	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	18V
MM74C08, MM74C86	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics

Min/max limits apply across the guaranteed temperature range, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.01	15	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=+360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=+360\mu A$			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$, $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$, $T_A=25°C$	-8.0	15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics (MM54C08/MM74C08) $T_A = 25°C$, $C_L = 50pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		80	140	ns
		$V_{CC} = 10V$		40	70	ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		14		pF

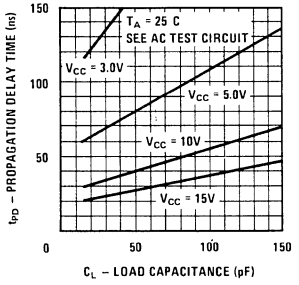
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

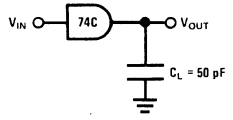
Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance MM54C08/MM74C08



TL/F/5878-2

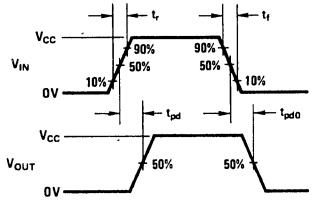
AC Test Circuit



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

TL/F/5878-3

Switching Time Waveforms



TL/F/5878-4

National Semiconductor

MM54C14/MM74C14 Hex Schmitt Trigger

General Description

The MM54C14/MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ. 0.0005 V/°C at $V_{CC} = 10$ V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2 V_{CC}$ is guaranteed.

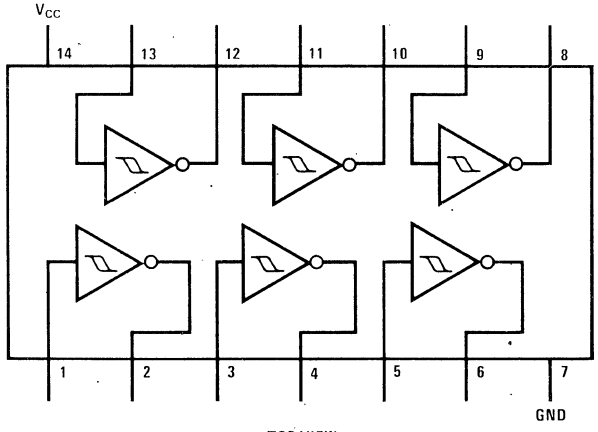
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.70 V_{CC} (typ.)
■ Low power TTL compatibility	0.4 V_{CC} (typ.) 0.2 V_{CC} guaranteed
■ Hysteresis	0.4 V_{CC} typ. 0.2 V_{CC} guaranteed

Connection Diagram

Dual-In-Line Package



TOP VIEW

Order Number MM54C14J or MM74C14J
See NS Package J14A

Order Number MM54C14N or MM74C14N
See NS Package N14A

Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C14	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	18V
MM74C14	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
V_{T+}	Positive Going Threshold Voltage	$V_{CC}=5V$	3.0	3.6	4.3	V
		$V_{CC}=10V$	6.0	6.8	8.6	V
		$V_{CC}=15V$	9.0	10.0	12.9	V
V_{T-}	Negative Going Threshold Voltage	$V_{CC}=5V$	0.7	1.4	2.0	V
		$V_{CC}=10V$	1.4	3.2	4.0	V
		$V_{CC}=15V$	2.1	5.0	6.0	V
$V_{T+}-V_{T-}$	Hysteresis	$V_{CC}=5V$	1.0	2.2	3.6	V
		$V_{CC}=10V$	2.0	3.6	7.2	V
		$V_{CC}=15V$	3.0	5.0	10.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$, $V_{IN}=0V/15V$		0.05	15	μA
		$V_{CC}=5V$, $V_{IN}=2.5V$ (Note 4)		20		μA
		$V_{CC}=10V$, $V_{IN}=5V$ (Note 4)		200		μA
		$V_{CC}=15V$, $V_{IN}=7.5V$ (Note 4)		600		μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5V$	4.3			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5V$			0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5V$, $V_{OUT}=0V$, $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$, $T_A=25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	8.0	16		mA

6

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PD0}, t_{PD1}	Propagation Delay from Input to Output	$V_{CC} = 5V$		220	400	ns
		$V_{CC} = 10V$		80	200	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

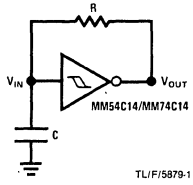
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Note 4: Only one of the six inputs is at 1/2 V_{CC}, the others are either at V_{CC} or GND.

Typical Applications

Low Power Oscillator



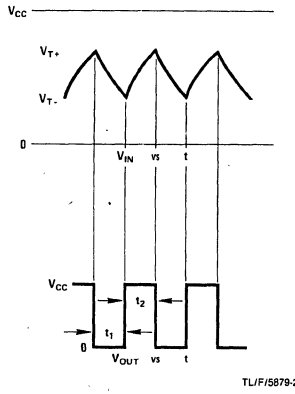
TL/F/5879-1

$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}} \approx \frac{1}{1.7\,RC}$$

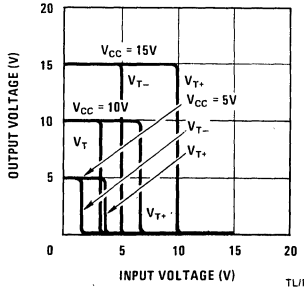
Note: The equations assume $t_1 + t_2 >> t_{pd0} + t_{pd1}$



TL/F/5879-2

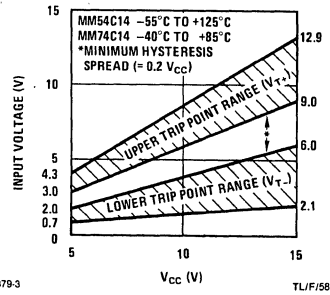
Typical Performance Characteristics

Typical Transfer Characteristics

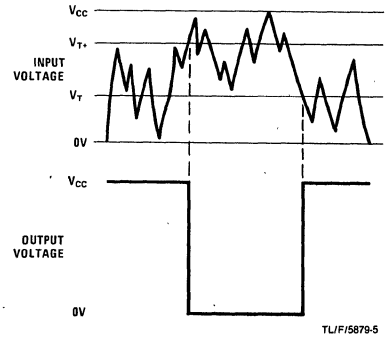


TL/F/5879-3

Guaranteed Trip Point Range



TL/F/5879-4



TL/F/5879-5

Note: For more information on output drive characteristics, power dissipation, and propagation delays, see AN-90.

National Semiconductor

MM54C30/MM74C30 8-Input NAND Gate

General Description

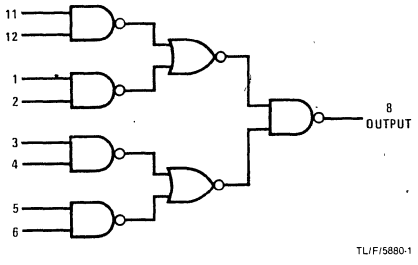
The logic gate employs complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption and high noise immunity. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers familiar with the standard 54/74 logic family.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

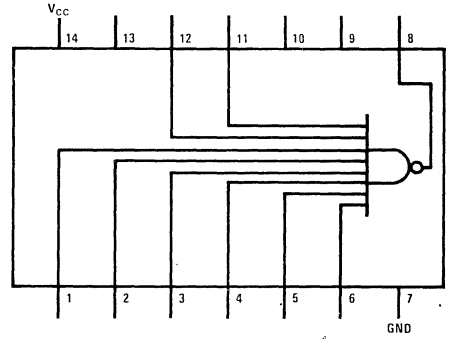
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Logic and Connection Diagrams



TL/F/5880-1

Dual-In-Line Package



TOP VIEW

TL/F/5880-2

Order Number MM54C30J or MM74C30J
See NS Package J14A

Order Number MM54C30N or MM74C30N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C30	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	18V
MM74C30	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=+10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.01	15	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$, $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$, $T_A=25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	$V_{CC} = 5.0V$		125	180	ns
		$V_{CC} = 10V$		55	90	ns
C_{IN}	Input Capacitance	(Note 2)		4.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		26		pF

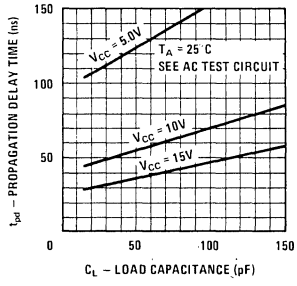
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

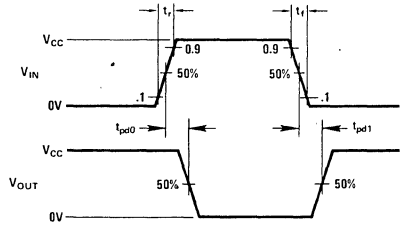
Typical Performance Characteristics

Propagation Delay Time vs Load Capacitance



TL/F/5880-3

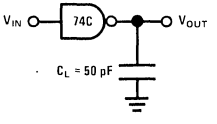
Switching Time Waveforms



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns.

TL/F/5880-4

AC Test Circuit



TL/F/5880-5

6

National Semiconductor

MM54C32/MM74C32 Quad 2-Input OR Gate

General Description

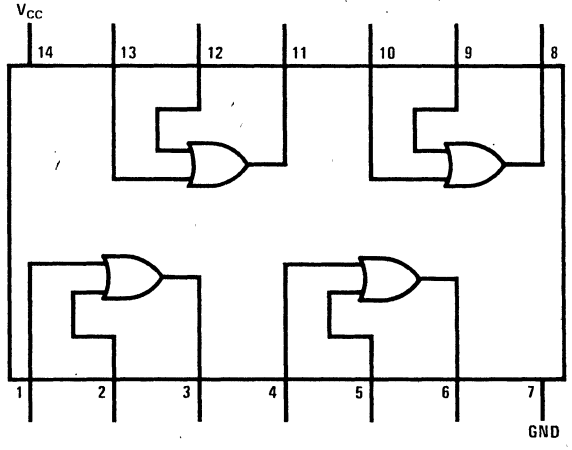
Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5881-1

Order Number MM54C32J or MM74C32J
See NS Package J14A

Order Number MM54C32N or MM74C32N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C32	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	18V
MM74C32	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	15	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C32	$V_{CC}=4.5V$	$V_{CC}-1.5$			V
	MM74C32	$V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C32	$V_{CC}=4.5V$			0.8	V
	MM74C32	$V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage					
	MM54C32	$V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
	MM74C32	$V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM54C32	$V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
	MM74C32	$V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$, $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$, $T_A=25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics

$T_A=25°C$, $C_L=50pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	$V_{CC}=5.0V$		80	150	ns
		$V_{CC}=10V$		35	70	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Gate (Note 3)		15		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

National Semiconductor

MM54C42/MM74C42 BCD-to-Decimal Decoder

General Description

The MM54C42/MM74C42 one-of-ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. This decoder produces a logical "0" at the output corresponding to a four bit binary input from zero to nine, and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1".

■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	10 MHz (typ.) with 10V V_{CC}

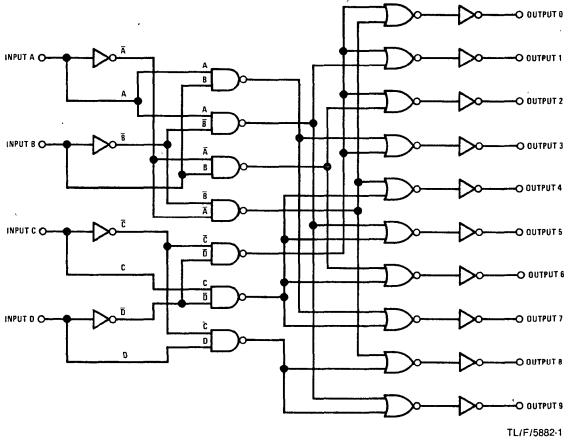
Features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads

Applications

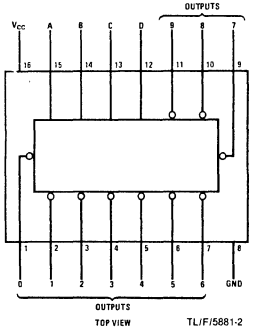
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Schematic and Connection Diagrams



TL/F/5882-1

Dual-In-Line Package



TL/F/5881-2

Order Number MM54C42J or MM74C42J
See NS Package J16A

Order Number MM54C42N or MM74C42N
See NS Package N16E

Truth Table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$		
Operating Temperature Range		Package Dissipation	500 mW
MM54C42	$-55°C$ to $+125°C$	Operating V_{CC} Range	3.0V to 15V
MM74C42	$-40°C$ to $+85°C$	Absolute Maximum V_{CC}	18V
Storage Temperature Range	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min /max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$	4.5			V
		$V_{CC}=10V$, $I_O=-10\mu A$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=10\mu A$			0.5	V
		$V_{CC}=10V$, $I_O=10\mu A$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0		300	μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$	$V_{CC}-1.5$			V
		74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$			0.8	V
		74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$	2.4			V
		74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$			0.4	V
		74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet) $T_A=25°C$ **(short circuit current)**						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0V$, $V_{IN(0)}=0V$, $V_{OUT}=0V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10V$, $V_{IN(0)}=0V$, $V_{OUT}=0V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0V$, $V_{IN(1)}=5.0V$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10V$, $V_{IN(1)}=10V$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A=25°C$, $C_L=50pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{pd}	Propagation Delay Time to Logical "0" or "1"	$V_{CC}=5.0V$		200	300	ns
		$V_{CC}=10V$		90	140	ns
C_{IN}	Input Capacitance	(See note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(See note 3)		50		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

National Semiconductor

MM54C48/MM74C48 BCD-to-7 Segment Decoder

General Description

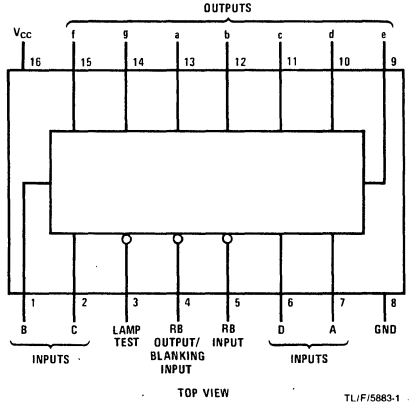
The MM54C48/MM74C48 BCD-to-7 segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test blanking input/ripple-blanking output, and ripple-blanking inputs.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} (typ.)
- Low power fan out of 2
  TTL compatibility driving 74L
- High current sourcing output (up to 50 mA)
- Ripple blanking for leading or trailing zeros (optional)
- Lamp test provision

Connection Diagram

Dual-In-Line Package

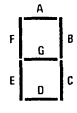


TL/F/5883-1

Order Number MM54C48J or MM74C48J
See NS Package J16A

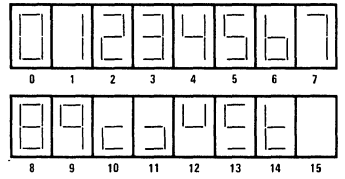
Order Number MM54C48N or MM74C48N
See NS Package N16E

Segment Identification



TL/F/5883-2

Numerical Designations and Resultant Displays



TL/F/5883-3

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C48	−55°C to +125°C
MM74C48	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage (RB Output Only)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
		V_{CC} = 10V, I_O = −10μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10μA			0.5	V
		V_{CC} = 10V, I_O = +10μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15.0V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
		74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (RB Output Only)	54C, V_{CC} = 4.5V, I_O = −50μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −50μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current (P-Channel) (RB Output Only)	V_{CC} = 4.75V, V_{OUT} = 0.4V			−0.80	mA
		V_{CC} = 10V, V_{OUT} = 0.5V			−4.0	mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}	1.75	3.6		mA
		T_A = 25°C				
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}	8.0	16		mA
		T_A = 25°C				
	Output Source Current (NPN Bipolar)	V_{CC} = 5.0V, V_{OUT} = 3.4	−20	−50		mA
		V_{CC} = 5.0V, V_{OUT} = 3.0		−65		mA
		V_{CC} = 10V, V_{OUT} = 8.4	−20	−50		mA
		V_{CC} = 10V, V_{OUT} = 8.0		−65		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

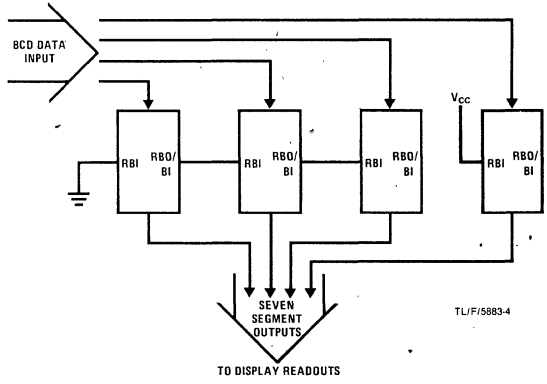
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay to a "1" or "0" on Segment Outputs from Data Inputs	$V_{CC} = 5.0V$		450	1500	ns
		$V_{CC} = 10V$		160	500	ns
t_{pd0}	Propagation Delay to a "0" on Segment Outputs from RB Input	$V_{CC} = 5.0V$		500	1600	ns
		$V_{CC} = 10V$		180	550	ns
t_{pd0}	Propagation Delay to a "0" on Segment Outputs from Blanking Input	$V_{CC} = 5.0V$		350	1200	ns
		$V_{CC} = 10V$		140	450	ns
t_{pd1}	Propagation Delay to a "1" on Segment Outputs from Lamp Test	$V_{CC} = 5.0V$		450	1500	ns
		$V_{CC} = 10V$		160	500	ns
t_{pd1}	Propagation Delay to a "1" on RB Output from RB Input	$V_{CC} = 5.0V$		600	2000	ns
		$V_{CC} = 10V$		250	800	ns
t_{pd0}	Propagation Delay to a "0" on RB Output from RB Input	$V_{CC} = 5.0V$		140	450	ns
		$V_{CC} = 10V$		50	150	ns

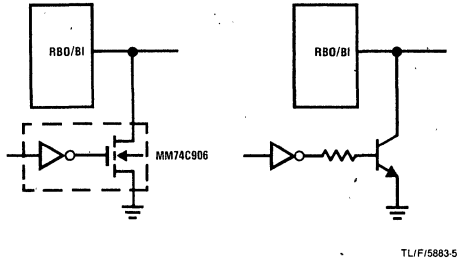
Typical Applications

Typical Connection Utilizing the Ripple-Blanking Feature



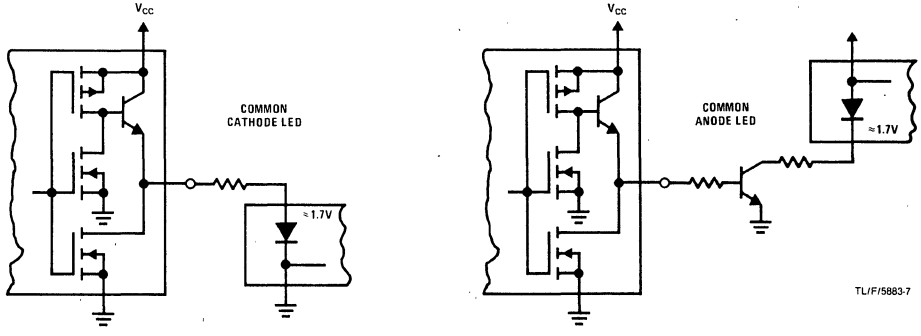
(First three stages will blank leading zeros, the fourth stage will not blank zeros)

Blanking Input Connection Diagram



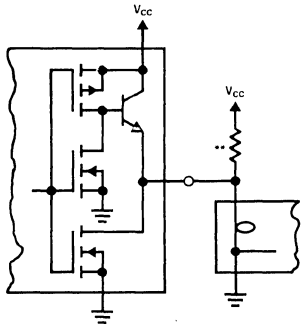
(When RBO/BI is forced low, all segment outputs are off regardless of the state of any other input condition)

Light Emitting Diode (LED) Readout



Typical Applications (Cont'd)

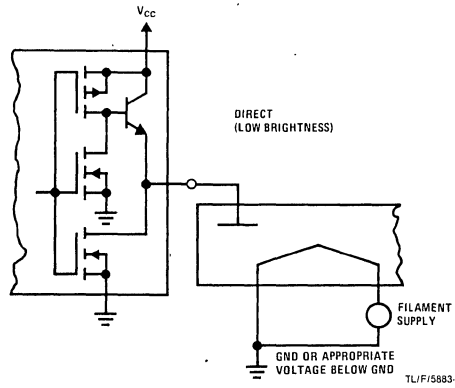
Incandescent Readout



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

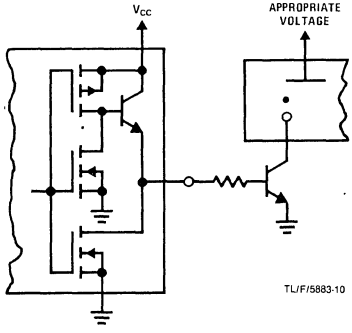
TL/F/5883-8

Fluorescent Readout



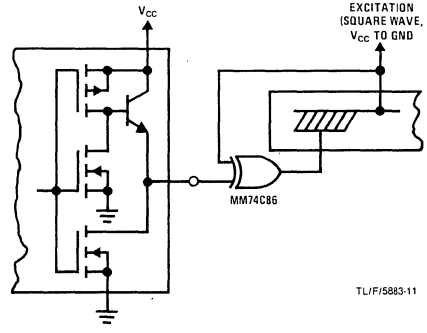
TL/F/5883-9

Gas Discharge Readout



TL/F/5883-10

Liquid Crystal (LC) Readout



TL/F/5883-11

Direct dc drive of LC's not recommended for life of LC readouts.

Truth Table

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

Note 1: The blanking input (BI) must be open when output functions 0–15 are desired. The ripple-blanking input (RBI) must be high, if blanking of a decimal zero is not desired.

Note 2: When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

Note 3: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open and a low is applied to the lamp-test input, all segment outputs are high.

† One BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

National Semiconductor

MM54C73/MM74C73, MM54C76/MM74C76, MM54C107/MM74C107 Dual J-K Flip-Flops with Clear and Preset

General Description

These dual J-K flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N-and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The MM54C76/MM74C76 flip flops also include preset inputs and are supplied in 16 pin packages. These flip-flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

Features

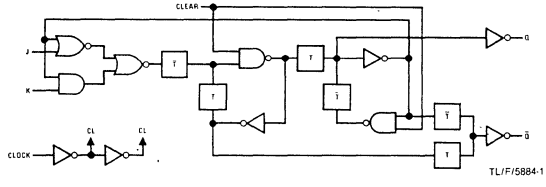
■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	10 MHz (typ.) with 10V supply

Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

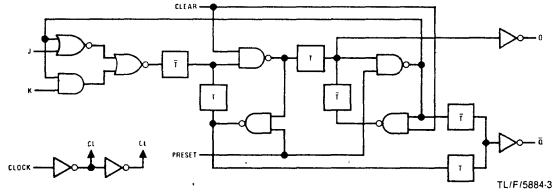
Logic and Connection Diagrams

MM54C73/MM74C73 and MM54C107/MM74C107



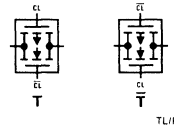
TL/F/5884-1

MM54C76/MM74C76

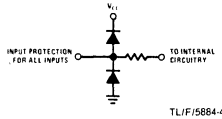


TL/F/5884-3

Transmission Gate

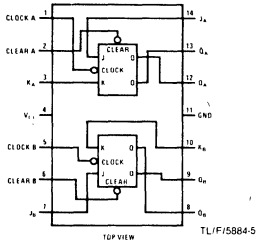


TL/F/5884-2



TL/F/5884-4

MM54C73/MM74C73

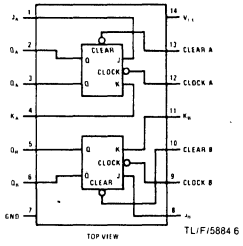


TL/F/5884-5

Note. A logic "0" on clear sets Q to logic "0."

Order Number MM54C73J, MM74C73J, MM54C73N or MM74C73N
See NS Package J14A or N14A

MM54C107/MM74C107

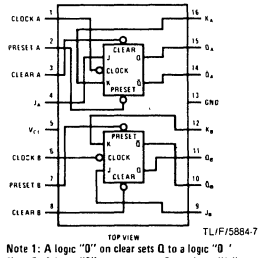


TL/F/5884-6

Note: A logic "0" on clear sets Q to logic "0."

Order Number MM54C107J, MM74C107J, MM54C107N or MM74C107N
See NS Package J14A or N14A

MM54C76/MM74C76



TL/F/5884-7

Note 1: A logic "0" on clear sets Q to a logic "0."
Note 2: A logic "0" on preset sets Q to a logic "1."

Order Number MM54C76J, MM74C76J, MM54C76N or MM74C76N
See NS Package J16A or N16A

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Lead Temperature (Soldering, 10 seconds)	300°C
MM54CXX	−55°C to 125°C	Operating V_{CC} Range	+3V to 15V
MM74CXX	−40°C to +85°C	V_{CC} (Max)	18V
Storage Temperature	−65°C to 150°C		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$	4.5			V
		$V_{CC}=10V$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$			0.5	V
		$V_{CC}=10V$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15.0V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15.0V$	−1.0			μA
I_{CC}	Supply Current	$V_{CC}=15.0V$		0.050	60	μA
Low Power TTL to CMOS Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0V$, $V_{IN(1)}=5.0V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10V$, $V_{IN(1)}=10V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

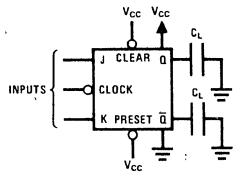
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
C_{IN}	Input Capacitance	Any Input		5		pF
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	300 130	ns ns
t_{pd}	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	300 130	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0V$ $V_{CC} = 10V$		110 45	175 70	ns ns
t_H	Time after Clock Pulse that J and K must be Held	$V_{CC} = 5.0V$ $V_{CC} = 10V$		−40 −20	0 0	ns ns
t_{PW}	Minimum Clock Pulse Width $t_{WL} = t_{WH}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		120 50	190 80	ns ns
t_{PW}	Minimum Preset and Clear Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		90 40	130 60	ns ns
f_{MAX}	Maximum Toggle Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.5 7.0	4.0 11.0		MHz MHz
t_r, t_f	Clock Pulse Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$			15 5	μs μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

AC Test Circuit



TL/F/5884-8

Truth Table

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

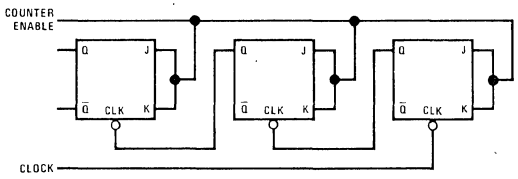
t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	*Q_n	*$\overline{Q}_n$

*No change in output from previous state.

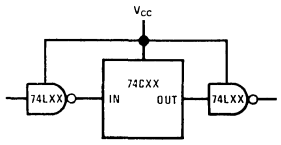
Typical Applications

Ripple Binary Counters



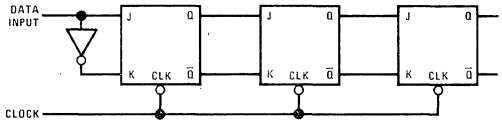
TL/F/5884-9

74C Compatibility



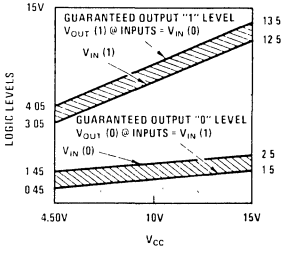
TL/F/5884-10

Shift Registers



TL/F/5884-11

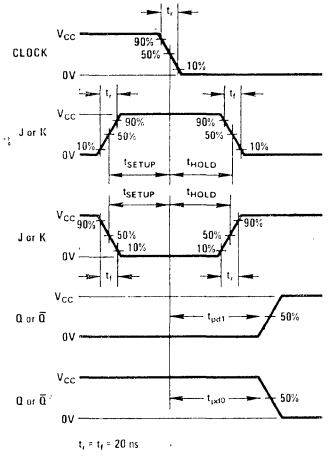
Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5884 12

Switching Time Waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

TL/F/5884-13

National Semiconductor

MM54C74/MM74C74 Dual D Flip-Flop

General Description

The MM54C74/MM74C74 dual D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

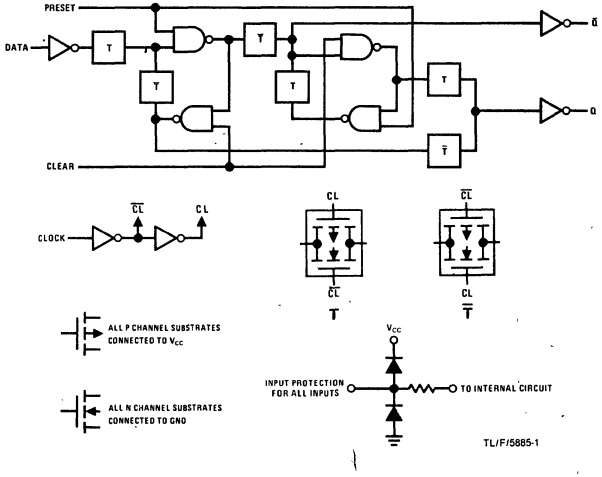
Features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2LPT^{2}L loads
■ High noise immunity	0.45 V_{CC} (typ)
■ Low power	50 nW (typ)
■ Medium speed operation	10 MHz (typ) with 10V supply

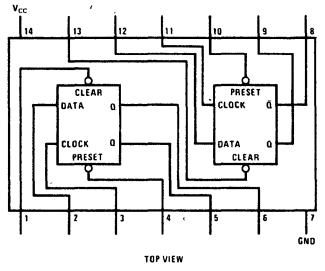
Applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

Logic and Connection Diagrams



Dual-In-Line Package



Note: A logic "0" on clear sets Q to logic "0." A logic "0" on preset sets Q to logic "1." TL/F/5885-2

Order Number MM54C74J or MM74C74J
See NS Package J14A

Order Number MM54C74N or MM74C74N
See NS Package N14A

Truth Table

Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	*Q_n	*$\overline{Q}_n$

*No change in output from previous state.

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C74	$-55°C$ to $125°C$
MM74C74	$-40°C$ to $+85°C$
Storage Temperature	$-65°C$ to $150°C$
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C
Operating V_{CC} Range	+3V to +15V
V_{CC} (Max)	18V

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	3.5			V
		$V_{CC}=10V$	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			1.5	V
		$V_{CC}=10V$			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$	4.5			V
		$V_{CC}=10V$	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$			0.5	V
		$V_{CC}=10V$			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15.0V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15.0V$	−1.0			μA
I_{CC}	Supply Current	$V_{CC}=15.0V$		0.05	60	μA
Low Power TTL/CMOS Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$			
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.75V$ 74C, $V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_D=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_D=-360\mu A$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_D=360\mu A$ 74C, $V_{CC}=4.75V$, $I_D=360\mu A$			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10V$, $V_{IN(0)}=0V$ $T_A=25°C$, $V_{OUT}=0V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0V$, $V_{IN(1)}=5.0V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10V$, $V_{IN(1)}=10V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance	Any Input (See Note 2)		5.0		pF
t_{pd}	Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from Clock to Q or $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Preset or Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "1" from Preset or Clear	$V_{CC} = 5.0V$ $V_{CC} = 10V$		250 100	400 150	ns ns
t_{S0}, t_{S1}	Time Prior to Clock Pulse that Data must be Present t_{SETUP}	$V_{CC} = 5.0V$ $V_{CC} = 10V$	100 40	50 20		ns ns
t_{H0}, t_{H1}	Time after Clock Pulse that Data must be Held	$V_{CC} = 5.0V$ $V_{CC} = 10V$		−20 −8.0	0 0	ns ns
t_{PW1}	Minimum Clock Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		100 40	250 100	ns ns
t_{PW2}	Minimum Preset and Clear Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		100 40	160 70	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	15.0 5.0			μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.0 5.0	3.5 8.0		MHz MHz
C_{PD}	Power Dissipation Capacitance	See Note 3		40		pF

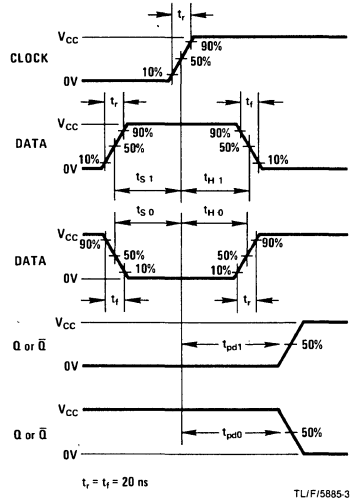
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

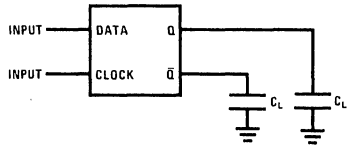
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Switching Time Waveforms

CMOS to CMOS



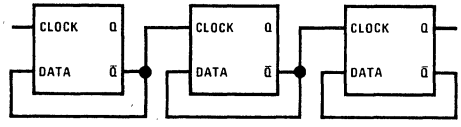
AC Test Circuit



TL/F/5885-4

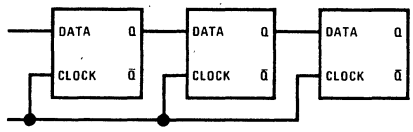
Typical Applications

Ripple Counter (Divide by 2^n)



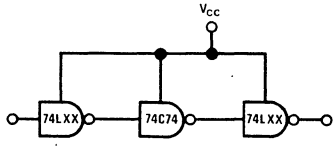
TL/F/5885-5

Shift Register



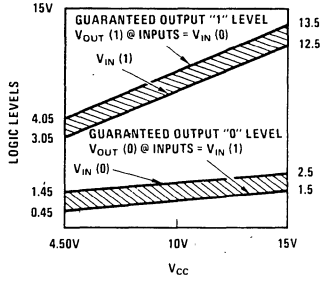
TL/F/5885-6

74C Compatibility



TL/F/5885-7

Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5885-8

National Semiconductor

MM54C83/MM74C83 4-Bit Binary Full Adder

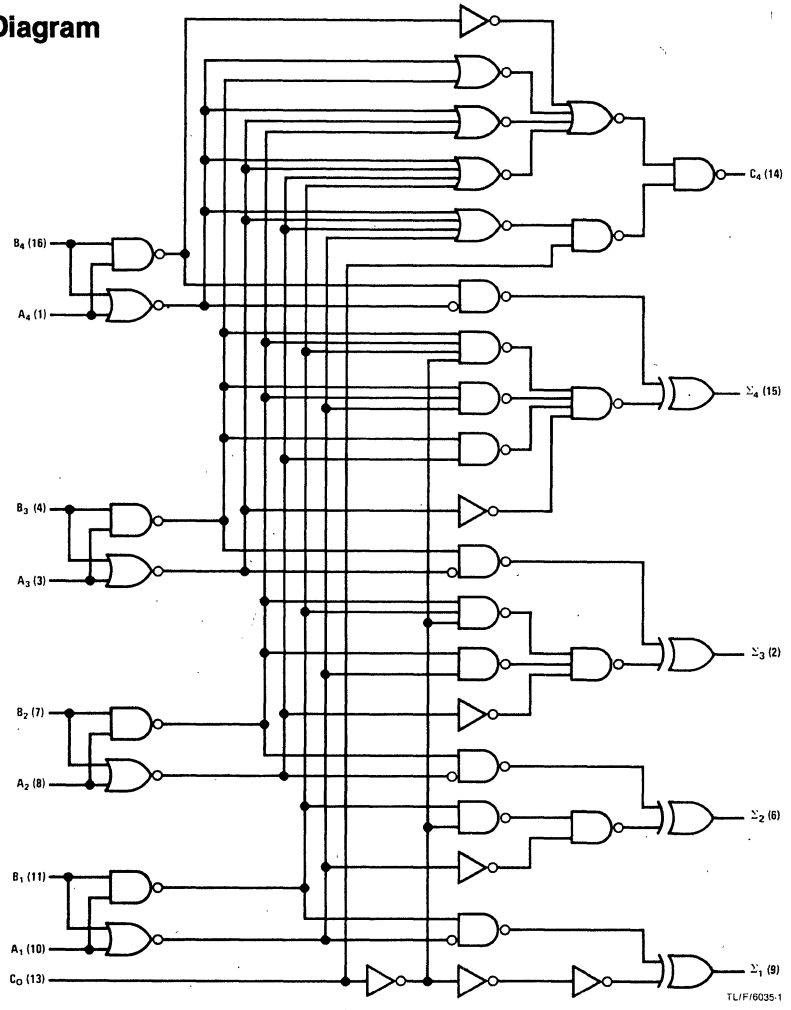
General Description

The MM54C83/MM74C83 4-bit binary full adder performs the addition of two 4-bit binary numbers. A carry input (C_0) is included and the sum (Σ) outputs are provided for each bit and the resultant carry C_4) is obtained from the fourth bit. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Also, the logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

Features

■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Fast carry ripple (C_0 to C_4)	50 ns (typ.)@V_{CC} = 10V and C_L = 50 pF
■ Fast summing (Σ_{IN} to Σ_{OUT})	125 ns (typ.)@V_{CC} = 10V and C_L = 50 pF

Logic Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C83	$-55°C$ to $125°C$
MM74C83	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

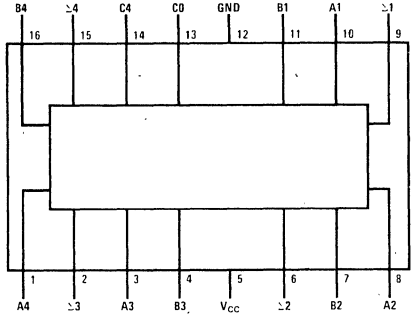
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay from C_0 to C_4	$V_{CC} = 5.0V$ $V_{CC} = 10V$		120 50	200 80	ns ns
t_{pd1}	Propagation Delay from Sum Inputs to C_4	$V_{CC} = 5.0V$ $V_{CC} = 10V$		250 90	450 150	ns ns
t_{pd1}	Propagation Delay from C_0 to Sum Outputs	$V_{CC} = 5.0V$ $V_{CC} = 10V$		350 125	550 200	ns ns
t_{pd1}	Propagation Delay from Sum Inputs to Sum Outputs	$V_{CC} = 5.0V$ $V_{CC} = 10V$		300 90	550 150	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		120		pF

Connection Diagram

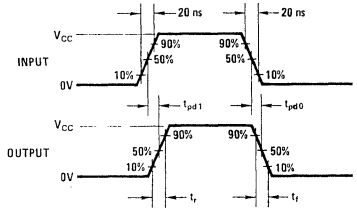
Dual-In-Line Package



Order Number MM54C83J or MM74C83J
See NS Package J16A

Order Number MM54C83N or MM74C83N
See NS Package N16E

Switching Time Waveforms



Inputs must be tied to appropriate logic level.

TL/F/6035-3

Truth Table

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
						WHEN C2 = L			WHEN C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	L	H	H	H	H	H	H

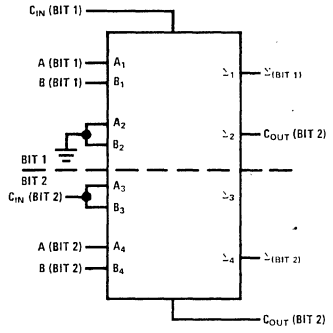
H = high level, L = low level

Note: Input conditions at A3, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Typical Applications

APPLICATION

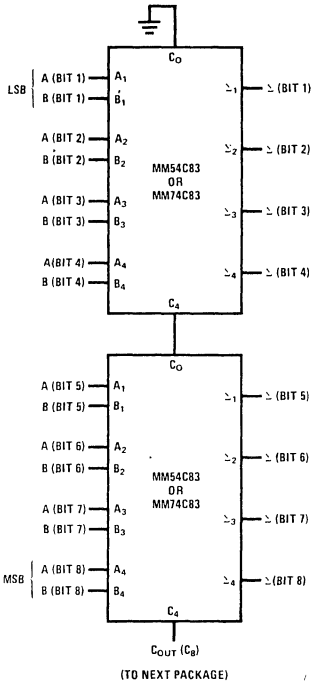
Connect the MM54C83/MM74C83 in the following manner to implement a dual single bit full adder.



TL/F/6035-4

CASCADING

Connect the MM54C83/MM74C83 in the following manner to implement full adders with more than 4 bits.



TL/F/6035-5

6

National Semiconductor

MM54C85/MM74C85 4-Bit Magnitude Comparator

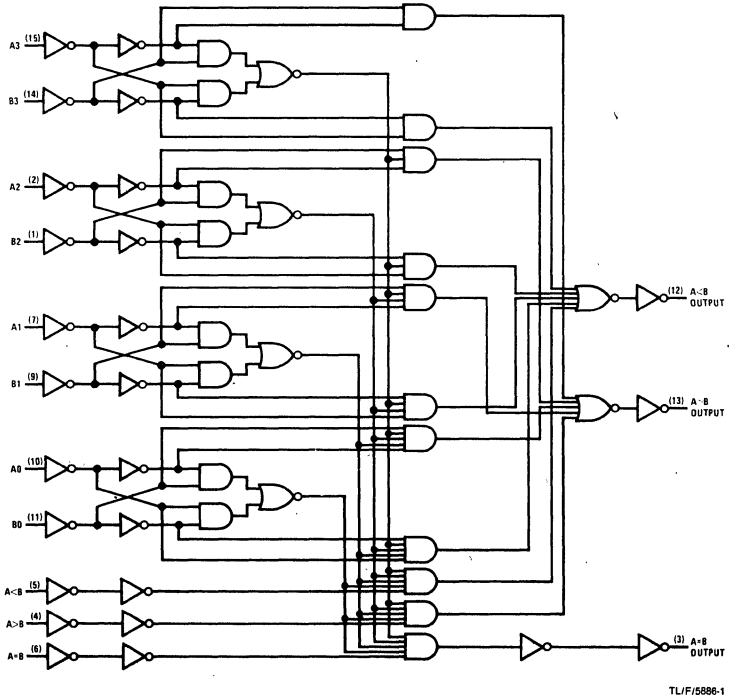
General Description

The MM54C85/MM74C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A > B, A < B and A = B), and three outputs (A > B, A < B and A = B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A > B, A < B, and A = B) of the least significant stage to the cascade inputs (A > B, A < B and A = B) of the next-significant stage. In addition the least significant stage must have a high level voltage ($V_{IN(1)}$ applied to the A = B input and low level voltages ($V_{IN(0)}$) applied to A > B and A < B inputs.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Expandable to 'N' stages	
■ Applicable to binary or BCD	
■ Low power pinout: 54L85/74L85	

Logic Diagram



TL/F/5886-1

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C85	$-55°C$ to $+125°C$	V_{CC}	18V
MM74C85	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics $T_A=25°C$, $C_L=50pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay from any A or B Data Input to any Data Output	$V_{CC}=5.0V$ $V_{CC}=10V$		250 100	600 300	ns ns
t_{pd}	Propagation Delay Time from any Cascade Input to any Output	$V_{CC}=5.0V$ $V_{CC}=10V$		200 100	500 250	ns ns
C_{IN}	Input Capacitance	Any Input		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Package		45		pF

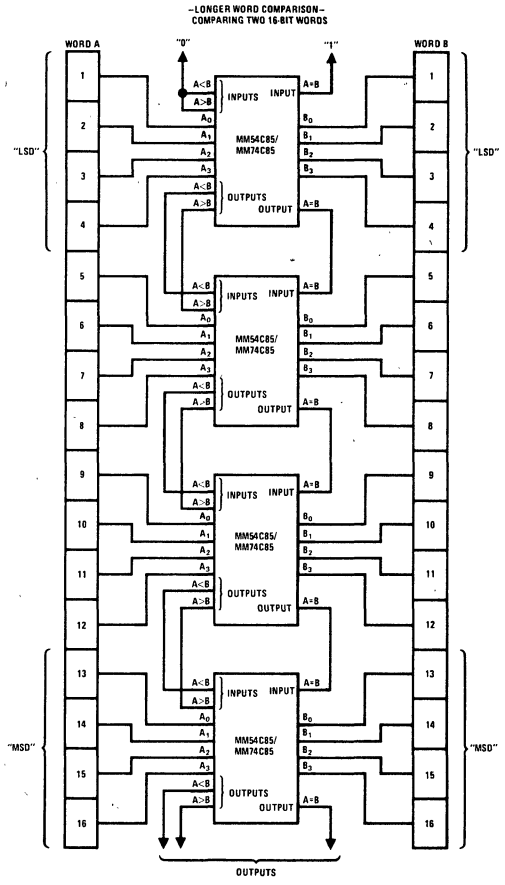
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

Typical Applications

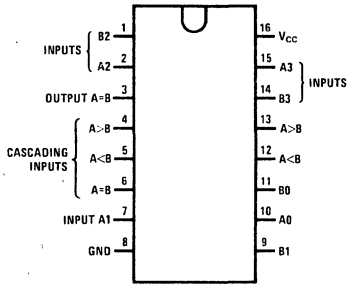
Four Digit Comparator



TL/F/5886-2

Connection Diagram

Dual-In-Line Package

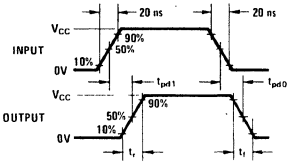


TOP VIEW TL/F/5886-3

Order Number MM54C85J or MM74C85J
See NS Package J16A

Order Number MM54C85N or MM74C85N
See NS Package N16E

Switching Time Waveforms



Unused inputs must be tied to an appropriate logic level. TL/F/5886-4

Truth Table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

National Semiconductor

MM54C86/MM74C86 Quad 2-Input EXCLUSIVE-OR Gate

General Description

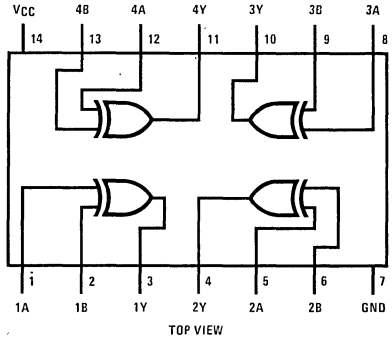
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	10 nW/package (typ.)
■ The MM54C86/MM74C86 follows the MM54LS86/MM74LS86 Pinout.	

Connection Diagram

Dual-In-Line Package



TL/F/5887-1

Order Number MM54C86J or MM74C86J
See NS Package J14A

Order Number MM54C86N or MM74C86N
See NS Package N14A

Truth Table

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Level L= Low Level

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C86	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	18V
MM74C86	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.01	15	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=+360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=+360\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics

(MM54C86/MM74C86) $T_A=25°C$, $C_L=50pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Time to Logical "1" or "0"	$V_{CC}=5.0V$ $V_{CC}=10V$		110 50	185 90	ns ns
C_{IN}	Input Capacitance	Note 2		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

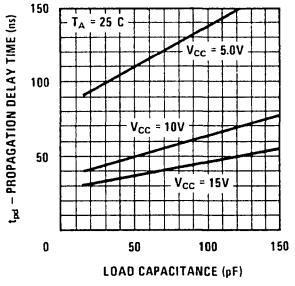
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

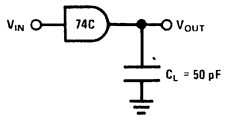
Typical Performance Characteristics

Propagation Delay Time vs
Load Capacitance
MM54C86/MM74C86



TL/F/5887-2

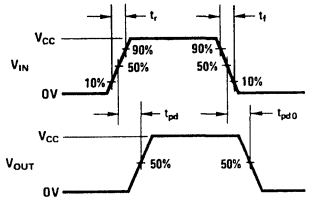
AC Test Circuit



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

TL/F/5887-3

Switching Time Waveforms



TL/F/5887-4

National Semiconductor

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE data output lines working in conjunction with the memory enable input provide for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different that the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

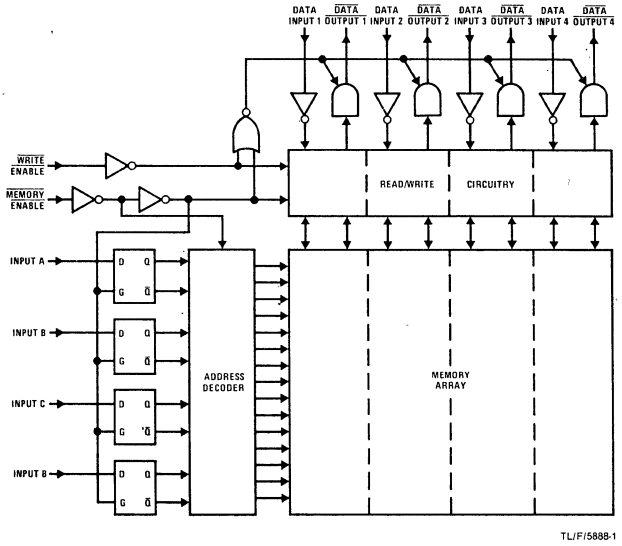
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

Features

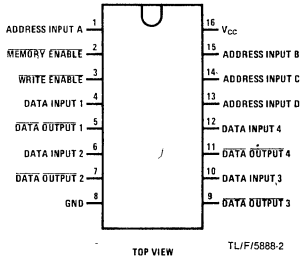
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Low power consumption	100 nW/package (typ.)
■ Fast access time	130 ns (typ.) at V_{CC} = 10V
■ TRI-STATE output	

Logic and Connection Diagrams



TL/F/5888-1

Dual-In-Line Package



TOP VIEW

TL/F/5888-2

Order Number MM54C89J or MM74C89J
See NS Package J16A

Order Number MM54C89N or MM74C89N
See NS Package N16E

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C89	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	18V
MM74C89	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		−0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{OZ}	Output Current in High Impedance State	$V_{CC}=15V$, $V=15V$ $V_{CC}=15V$, $V_O=0V$	 −1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=+360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=+360\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics $T_A=25°C$, $C_L=50pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay from Memory Enable	$V_{CC}=5.0V$ $V_{CC}=10V$		270 100	500 220	ns ns
t_{ACC}	Access Time from Address Input	$V_{CC}=5.0V$ $V_{CC}=10V$		350 130	650 280	ns ns
t_{SA}	Address Setup Time	$V_{CC}=5.0V$ $V_{CC}=10V$	150 60			ns ns
t_{HA}	Address Hold Time	$V_{CC}=5.0V$ $V_{CC}=10V$	60 40			ns ns
t_{ME}	Memory Enable Pulse Width	$V_{CC}=5.0V$ $V_{CC}=10V$	400 150	250 90		ns ns
t_{ME}	Memory Enable Pulse Width	$V_{CC}=5.0V$ $V_{CC}=10V$	400 150	200 70		ns ns

AC Electrical Characteristics (Cont'd.) $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{SR}	Write Enable Setup Time for a Read	$V_{CC} = 5.0V$ $V_{CC} = 10V$	0 0			ns ns
t_{WS}	Write Enable Setup Time for a Write	$V_{CC} = 5.0V$ $V_{CC} = 10V$			t_{ME} t_{ME}	ns ns
t_{WE}	Write Enable Pulse Width	$V_{CC} = 5.0V$, $t_{WS} = 0$ $V_{CC} = 10V$, $t_{WS} = 0$	300 100	160 60		ns ns
t_{HD}	Data Input Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 25			ns ns
t_{SD}	Data Input Setup	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 25			ns ns
t_{1H}, t_{0H},	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Memory Enable	$V_{CC} = 5.0V$, $C_L = 5.0pF$, $R_L = 10k$ $V_{CC} = 10V$, $C_L = 5.0pF$, $R_L = 10k$		180 −85	300 120	ns ns
t_{1H}, t_{0H},	Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from Write Enable	$V_{CC} = 5.0V$, $C_L = 5.0pF$, $R_L = 10k$ $V_{CC} = 10V$, $C_L = 5.0pF$, $R_L = 10k$		180 85	300 120	ns ns
C_{IN}	Input Capacity	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity	Any Output (Note 2)		6.5		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

AC Electrical Characteristics (Guaranteed across the specified temperature range, $C_L = 50pF$)

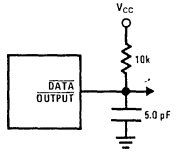
Parameter	Conditions	MM54C89 $T_A = -55°C$ to $+125°C$		MM74C89 $T_A = -45°C$ to $+85°C$		Units
		Min	Max	Min	Max	
t_{PD}	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 15V$		700 310 250		600 265 210	ns ns ns
t_{ACC}	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 15V$		910 400 320		780 345 270	ns ns ns
t_{SA}	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 15V$	210 90 70		180 80 60		ns ns ns
t_{HA}	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 15V$	80 55 45		70 50 40		ns ns ns
t_{ME}	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 15V$	560 210 170		480 180 150		ns ns ns
t_{ME}	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 15V$	560 210 170		480 180 150		ns ns ns
t_{WE}	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 15V$	420 140 110		360 120 100		ns ns ns
t_{HD}	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 15V$	70 35 30		60 30 25		ns ns ns
t_{SA}	$V_{CC} = 5.0V$ $V_{CC} = 10V$ $V_{CC} = 15V$	70 35 30		60 30 25		ns ns ns
t_{1H}, t_{0H},	$V_{CC} = 5.0V$ $V_{CC} = 10V$, $C_L = 5.0pF$ $V_{CC} = 15V$, $R_L = 10k\Omega$		420 170 135		360 145 115	ns ns ns

Truth Table

ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI STATE
H	H	Inhibit, Storage	TRI-STATE

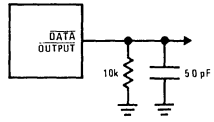
AC Test Circuits

t_{0H}



TL/F/5888-3

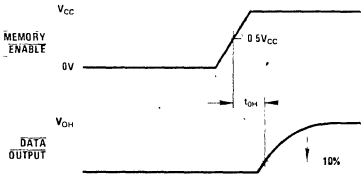
t_{1H}



TL/F/5888-4

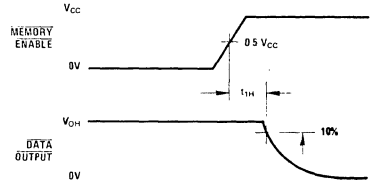
Switching Time Waveforms

t_{0H}



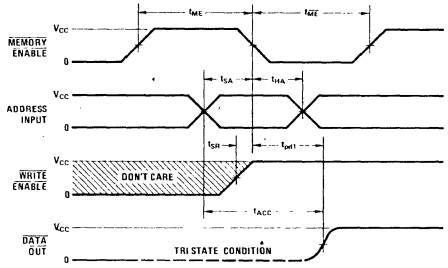
TL/F/5888-5

t_{1H}



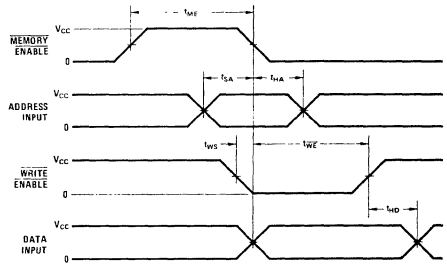
TL/F/5888 6

Read Cycle



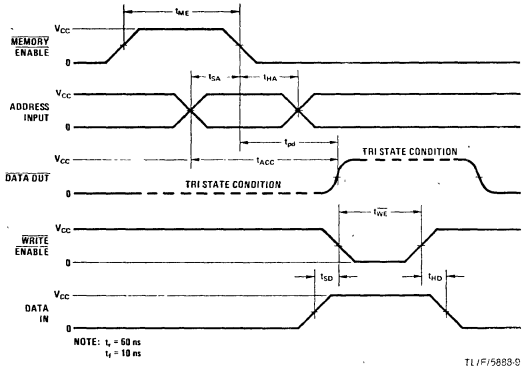
TL/F/5888-7

Write Cycle



TL/F/5888-8

Read Modify Write Cycle



TL/F/5888-9

National Semiconductor

MM54C90/MM74C90 4-Bit Decade Counter
MM54C93/MM74C93 4-Bit Binary Counter

General Description

The MM54C90/MM74C90 decade counter and the MM54C93/MM74C93 binary counter and complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. The 4-bit decade counter can reset to zero or preset to nine by applying appropriate logic level on the R_{01}, R_{02}, R_{91} and R_{92} inputs. Also, a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02}, and a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative going edge of the input pulse.

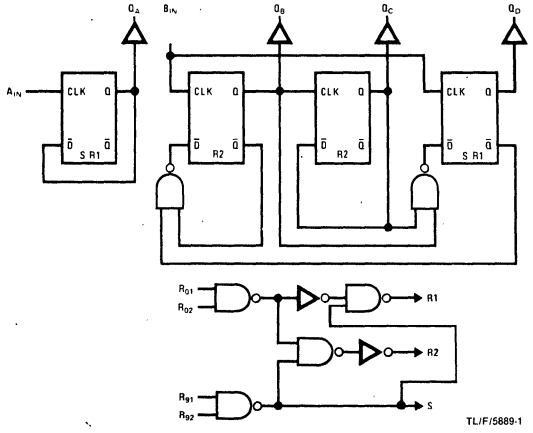
All inputs are protected against static discharge damage.

Features

- Wide supply voltage range — 3V to 15V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L
- The MM54C93/MM74C93 follows the MM54L93/MM74L93 Pinout

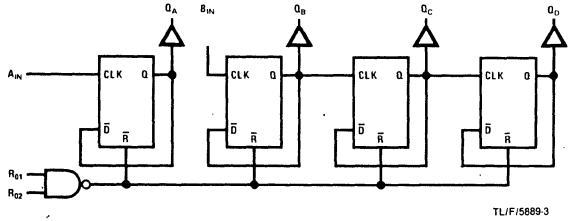
Logic and Connection Diagrams

MM54C90/MM74C90



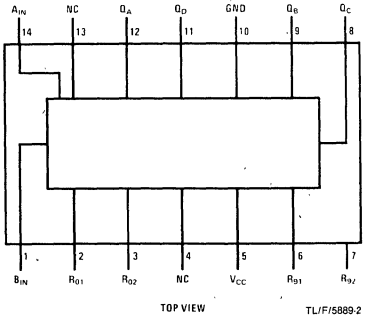
TL/F/5889-1

MM54C93/MM74C93



TL/F/5889-3

MM54C90/MM74C90
Dual-In-Line Package

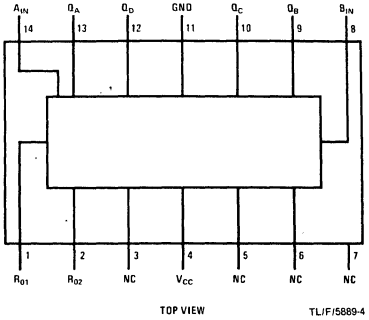


TOP VIEW TL/F/5889-2

Order Number MM54C90J or MM74C90J
See NS Package J14A

Order Number MM54C90N or MM74C90N
See NS Package N14A

MM54C93/MM74C93
Dual-In-Line Package



TOP VIEW TL/F/5889-4

Order Number MM54C93J or MM74C93J
See NS Package J14A

Order Number MM54C93N or MM74C93N
See NS Package N14A

Absolute Maximum Ratings

Voltage at Any Pin (Note 1)	$-0.3V$ to $V_{CC}+0.3V$	Operating V_{CC} Range	3V to 15V
Operating Temperature Range		Absolute Maximum V_{CC}	18V
MM54C90, MM54C93	$-55°C$ to $+125°C$	Storage Temperature Range	$-65°C$ to $+150°C$
MM74C90, MM74C93	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	500 mW		

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage MM54C90, MM54C93 MM74C90, MM74C93	 $V_{CC}=4.5V$ $V_{CC}=4.75V$	 $V_{CC}-1.5$ $V_{CC}-1.5$			 V V
$V_{IN(0)}$	Logical "0" Input Voltage MM54C90, MM54C93 MM74C90, MM74C93	 $V_{CC}=4.5V$ $V_{CC}=4.75V$			 0.8 0.8	 V V
$V_{OUT(1)}$	Logical "1" Output Voltage MM54C90, MM54C93 MM74C90, MM74C93	 $V_{CC}=4.5V$, $I_O=-360\mu A$ $V_{CC}=4.75V$, $I_O=-360\mu A$	 2.4 2.4			 V V
$V_{OUT(0)}$	Logical "0" Output Voltage MM54C90, MM54C93 MM74C90, MM74C93	 $V_{CC}=4.5V$, $I_O=360\mu A$ $V_{CC}=4.75V$, $I_O=360\mu A$			 0.4 0.4	 V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	-8	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	8	16		mA

AC Electrical Characteristics

$T_A=25°C$, $C_L=50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_A	$V_{CC}=5.0V$ $V_{CC}=10V$		200 80	400 150	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_B (MM54C93/MM74C93)	$V_{CC}=5.0V$ $V_{CC}=10V$		450 160	850 300	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_B (MM54C90/MM74C90)	$V_{CC}=5.0V$ $V_{CC}=10V$		450 160	800 300	ns ns

AC Electrical Characteristics (Cont'd.) $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_C (MM54C93/MM74C93)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		500 200	1050 400	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_C (MM54C90/MM74C90)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		500 200	1000 400	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_D (MM54C93/MM74C93)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		600 250	1200 500	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from A_{IN} to Q_D (MM54C90/MM74C90)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 160	800 300	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (MM54C93/MM74C93)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		150 75	300 150	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (MM54C90/MM74C90)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 75	400 150	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time from R_{91} or R_{92} to Q_A or Q_D (MM54C90/MM74C90)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		250 100	500 200	ns ns
t_{PW}	Min. R_{01} or R_{02} Pulse Width (MM54C93/MM74C93)	$V_{CC} = 5.0V$ $V_{CC} = 10V$	600 300	250 125		ns ns
t_{PW}	Min. R_{01} or R_{02} Pulse Width (MM54C90/MM74C90)	$V_{CC} = 5.0V$ $V_{CC} = 10V$	600 300	250 125		ns ns
t_{PW}	Min. R_{91} or R_{92} Pulse Width (MM54C90/MM74C90)	$V_{CC} = 5.0V$ $V_{CC} = 10V$	500 250	200 100		ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 10V$ $V_{CC} = 10V$			15 5	μs μs
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$	250 100	100 50		ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2 5			MHz MHz
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		45		pF

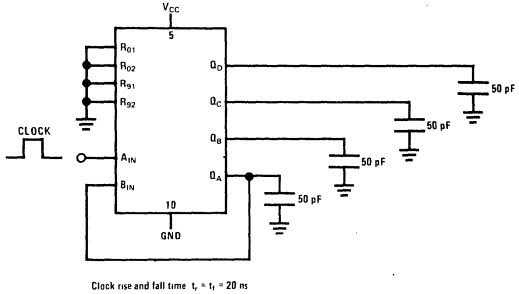
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

AC Test Circuits

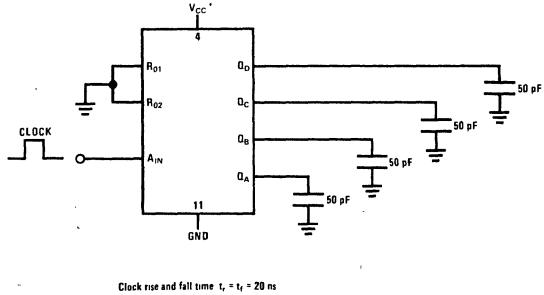
MM54C90/MM74C90



Clock rise and fall time $t_r = t_f = 20$ ns

TL/F/5889-5

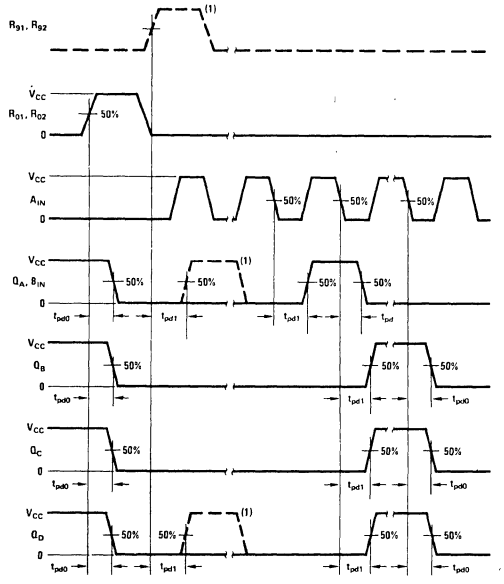
MM54C93/MM74C93



Clock rise and fall time $t_r = t_f = 20$ ns

TL/F/5889-6

Switching Time Waveforms



Note 1: MM54C90, MM74C90 and MM54C93, MM74C93 are solid line waveforms. Dashed line waveforms are for MM54C90/MM74C90 only.

TL/F/5889-7

Truth Tables

MM54C90/MM74C90 4-Bit Decade Counter

BCD Count Sequence

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Output Q_A is connected to input B for BCD count.

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS				OUTPUT			
R_{01}	R_{02}	R_{91}	R_{92}	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

MM54C93/MM74C93 4-Bit Binary Counter

Binary Count Sequence

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B for binary count sequence

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS		OUTPUT			
R_{01}	R_{02}	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

National Semiconductor

MM54C95/MM74C95 4-Bit Right-Shift Left-Shift Register

General Description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right-shift or left-shift register.

When a logical "0" level is applied to the mode control input, the output of each flip flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip flop and serial data is entered at input D.

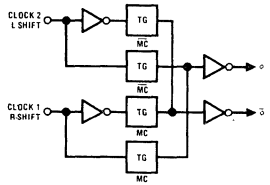
Features

- Medium speed operation — 10 MHz (typ.) $V_{CC} = 10V$, $C_L = 50pF$
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 100 nW/ (typ.)
- Tenth power TTL compatible — Drive 2 LTTL loads
- Wide supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip flop
- Negative edge triggered clocking
- The MM54C95/MM74C95 follows the MM54L95/MM74L95 Pinout.

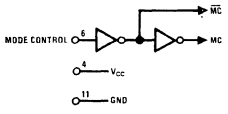
Applications

- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

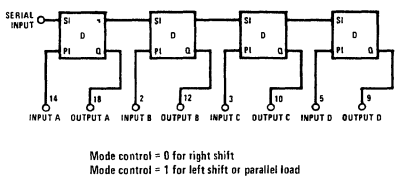
Block and Connection Diagrams



TL/F/5890-1



TL/F/5890-2



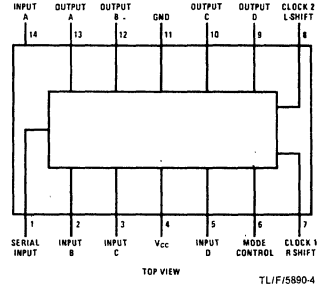
TL/F/5890-3

Function Table

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS		SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↑	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	L	H	X	X	X	X	X	Undefined			
↓	H	L	X	X	X	X	X	Operating Conditions			

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.
H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)
↓ = transition from high to low level, ↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock

Dual-In-Line Package



TL/F/5890-4

Order Number MM54C95J or MM74C95J
See NS Package J14A

Order Number MM54C95N or MM74C95N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC}+0.3 V	Maximum V_{CC} Voltage	18V
Operating Temperature		Package Dissipation	500 mW
MM54C95	−55°C to +125°C	Operating V_{CC} Range	+3 V to +15 V
MM74C95	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Sym	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	4.5 9			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			0.5 1	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V			1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V	−1			μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.050	300	μA
Low Power TTL/CMOS Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5 V 74C, V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5 V 74C, V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5 V, I_O = 360 μA 74C, V_{CC} = 4.75 V, I_O = 360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5 V, I_O = 360 μA 74C, V_{CC} = 4.75 V, I_O = 360 μA			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, unless otherwise noted.

Sym	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or Q	V_{CC} = 5.0 V V_{CC} = 10 V		200 80	400 160	ns ns
t_{S0}, t_{S1}	Time Prior to Clock Pulse that Data must be Preset	V_{CC} = 5.0 V V_{CC} = 10 V	60 25	30 10		ns ns
t_{H0}, t_{H1}	Time After Clock Pulse that Data must be Held	V_{CC} = 5.0 V V_{CC} = 10 V	25 10	10 50		ns ns
t_{PW}	Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0 V V_{CC} = 10 V		100 50		ns ns
t_{SM}	Time Prior to Clock Pulse that Mode Control must be Preset	V_{CC} = 5.0 V V_{CC} = 10 V	200 100	100 50		ns ns
f_{MAX}	Maximum Input Clock Frequency	V_{CC} = 5.0 V V_{CC} = 10 V	3 6.5	5 10		MHz MHz
C_{IN}	Input Capacitance	Any Input. (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

National Semiconductor

MM54C150/MM74C150 16-Line to 1-Line Multiplexer MM72C19/MM82C19 TRI-STATE® 16-Line to 1-Line Multiplexer

General Description

The MM54C150/MM74C150 and MM72C19/MM82C19 multiplex 16 digital lines to 1 output. A 4-bit address code determines the particular 1-of-16 inputs which is routed to the output. The data is inverted from input to output.

A strobe override places the output of MM54C150/MM74C150 in the logical "1" state and the output of MM72C19/MM82C19 in the high-impedance state.

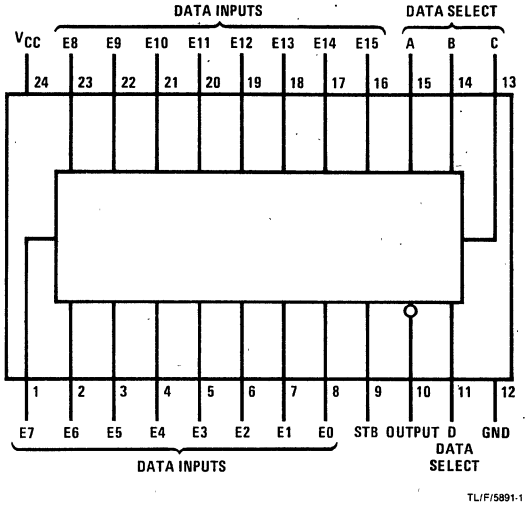
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	Drive 1 TTL Load

Connection Diagram

Dual-In-Line Package



TL/F/5891-1

Order Number MM54C150J, MM74C150J, MM72C19J or MM82C19J
See NS Package J24A

Order Number MM54C150N, MM74C150N, MM72C19N or MM82C19N
See NS Package N24A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0 V to 15 V
MM54C150, MM72C19	−55°C to +125°C	V_{CC}	18 V
MM74C150, MM82C19	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{OZ}	Output Current in High Impedance State MM72C19/MM82C19	 $V_{CC}=15\,V$, $V_O=15\,V$ $V_{CC}=15\,V$, $V_O=0\,V$	 −1.0	 0.005 −0.005	 1.0	 μA μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
TTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, 72C $V_{CC}=4.5\,V$ 74C, 82C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, 72C $V_{CC}=4.5\,V$ 74C, 82C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, 72C $V_{CC}=4.5\,V$, $I_O=-1.6\,mA$ 74C, 82C $V_{CC}=4.75\,V$, $I_O=-1.6\,mA$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, 72C $V_{CC}=4.5\,V$, $I_O=1.6\,mA$ 74C, 82C $V_{CC}=4.75\,V$, $I_O=1.6\,mA$			0.4 0.4	V V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=0\,V$, $T_A=25°C$	−4.35	−8		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10\,V$, $V_{OUT}=0\,V$, $T_A=25°C$	−20	−40		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	4.35	8		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10\,V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	20	40		mA

6

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Inputs to Output	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$ $V_{CC} = 5.0\,V$, $C_L = 150\,pF$ $V_{CC} = 10\,V$, $C_L = 150\,pF$		250 110 290 120	600 300 650 330	ns ns ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Select Inputs to Output	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		290 120	650 330	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Strobe to Output MM54C150/MM74C150	$V_{CC} = 5.0\,V$ $V_{CC} = 10V$		120 55	300 150	ns ns
t_{1H}, t_{0H}	Delay from Strobe to High Impedance State MM72C19/MM82C19	$V_{CC} = 5.0\,V$, $R_L = 10k$, $C_L = 5\,pF$ $V_{CC} = 10\,V$, $R_L = 10k$, $C_L = 5\,pF$		80 60	200 150	ns ns
t_{H1}, t_{H0}	Delay from Strobe to Logical "1" Level or to Logical "0" Level (from High Impedance State) MM72C19/MM82C19	$V_{CC} = 5.0\,V$, $R_L = 10k$, $C_L = 5\,pF$ $V_{CC} = 10\,V$, $R_L = 10k$, $C_L = 5\,pF$		80 30	250 120	ns ns
C_{IN}	Input Capacitance	Any Input, (Note 2)		5.0		pF
C_{OUT}	Output Capacitance MM72C19/MM82C19	(Note 2)		11.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Truth Table

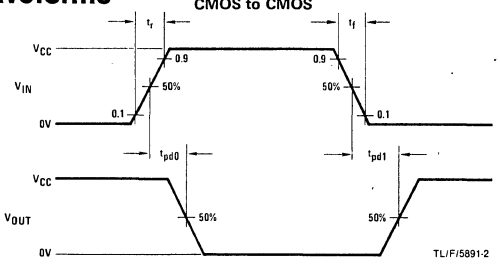
MM54C150/MM74C150

INPUTS																			OUTPUT
D	C	B	A	STROBE	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1*
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

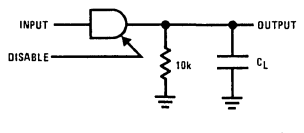
*For MM72C19/MM82C19 this would be Hi-Z, everything else is the same.

Switching Time Waveforms

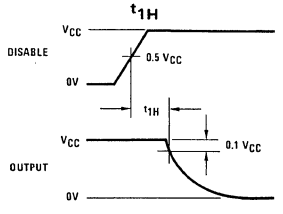
CMOS to CMOS



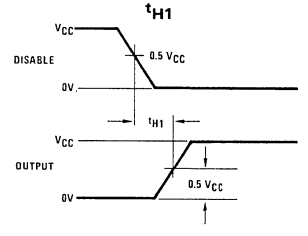
t_{1H} and t_{H1}



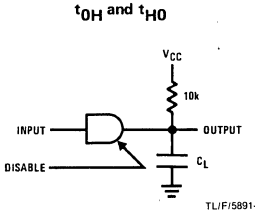
t_{1H}



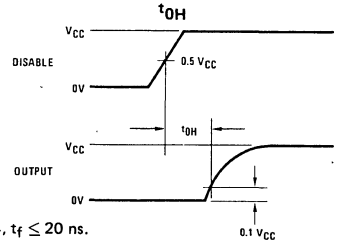
t_{H1}



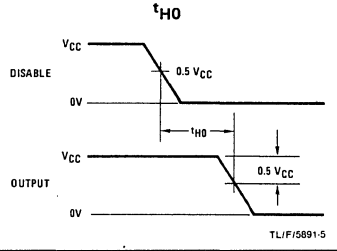
t_{0H} and t_{H0}



t_{0H}



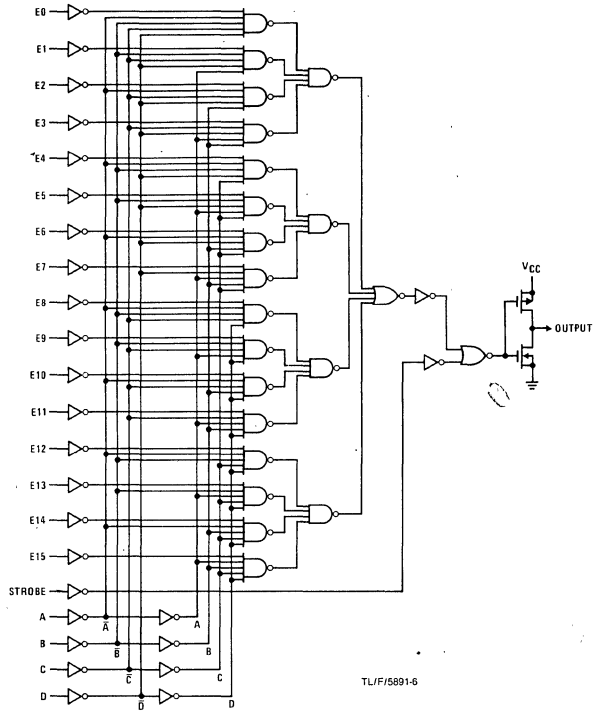
t_{H0}



Note: Delays measured with input t_r, $t_f \leq 20$ ns.

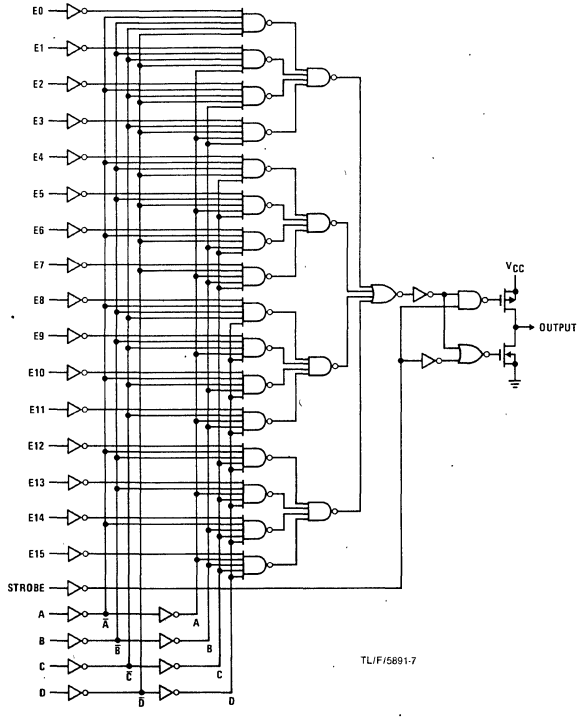
Logic Diagrams

MM54C150/MM74C150



TL/F/5891-6

MM72C19/MM82C19



TL/F/5891-7

National Semiconductor

MM54C151/MM74C151 8-Channel Digital Multiplexer

General Description

The MM54C151/MM74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors.

This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical "1" on the strobe input forces W to a logical "1" and Y to a logical "0".

All inputs are protected against electrostatic effects.

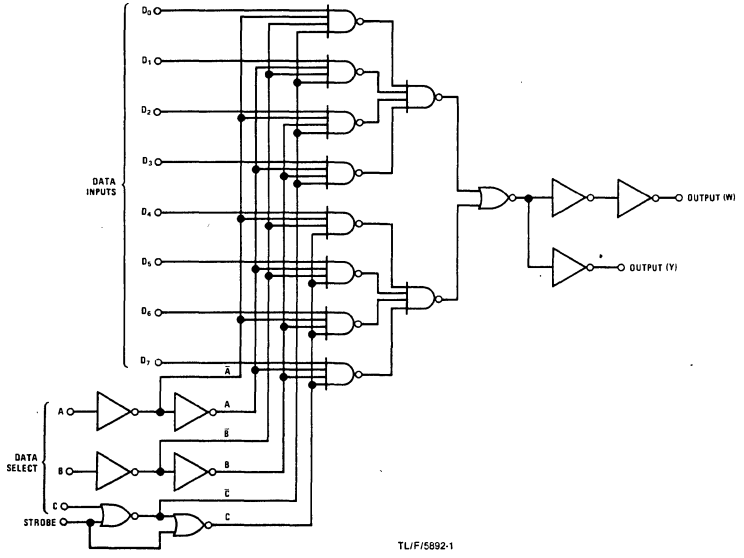
Features

- Supply voltage range 3 V to 15 V
- Tenth power TTL compatible drive 2 LPTTL loads
- High noise immunity 0.45 V_{CC} (typ.)
- Low power 50 nW (typ.)

Applications

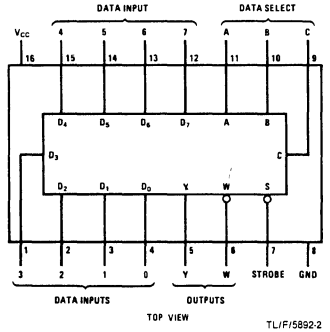
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic and Connection Diagrams



TL/F/5892-1

Dual-In-Line Package



TL/F/5892-2

Order Number MM54C151J or MM74C151J
See NS Package J16A

Order Number MM54C151N or MM74C151N
See NS Package N16E

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Maximum V_{CC} Voltage	18 V
Operating Temperature Range		Package Dissipation	500 mW
MM54C151	$-55°C$ to $+125°C$	Operating V_{CC} Range	3 V to 15 V
MM74C151	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	-1.0			μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
CMOS to LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V mA
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\,\mu A$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0\,V$, $V_{IN(1)}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10\,V$, $V_{IN(1)}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

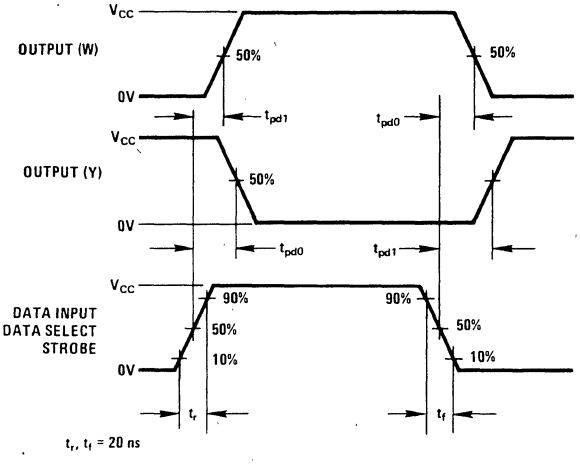
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data to Y	$V_{CC} = 5.0\,V$, $V_{CC} = 10\,V$		170 80	270 130	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data to W	$V_{CC} = 5.0\,V$, $V_{CC} = 10\,V$		200 90	300 140	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Strobe or Data Select to Y	$V_{CC} = 5.0\,V$, $V_{CC} = 10\,V$		240 110	360 170	ns ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		50		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

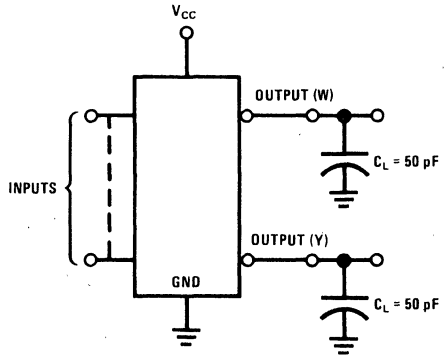
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



TL/F/5892-3

AC Test Circuit



TL/F/5892-4

Truth Table

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

National Semiconductor

MM54C154/MM74C154 4-Line to 16-Line Decoder/Demultiplexer

General Description

The MM54C154/MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

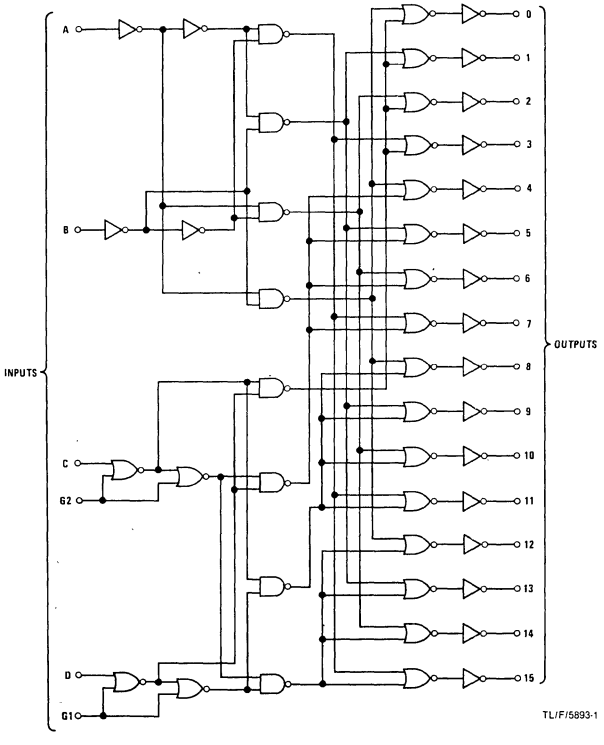
Features

■ Supply voltage range	3 V to 15 V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise margin	1 V guaranteed
■ High noise immunity	0.45 V_{CC} (typ.)

Applications

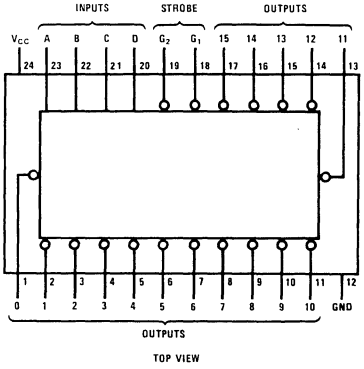
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic and Connection Diagrams



TL/F/5893-1

Dual-In-Line Package



TL/F/5893-2

Order Number MM54C154J or MM74C154J
See NS Package J24A

Order Number MM54C154N or MM74C154N
See NS Package N24A

6

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Maximum V_{CC} Voltage	18 V
Operating Temperature Range		Package Dissipation	500 mW
MM54C154	$-55°C$ to $+125°C$	Operating V_{CC} Range	3 V to 15 V
MM74C154	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
CMOS to LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-100\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-100\,\mu A$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0\,V$, $V_{IN(1)}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10\,V$, $V_{IN(1)}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

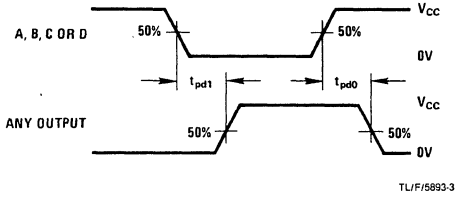
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}	Propagation Delay to a Logical "0" From Any Input to Any Output	$V_{CC} = 5.0\,V$, $V_{CC} = 10\,V$		275 100	400 200	ns ns
t_{pd0}	Propagation Delay to a Logical "0" from G1 or G2 to Any Output	$V_{CC} = 5.0\,V$, $V_{CC} = 10\,V$		275 100	400 200	ns ns
t_{pd1}	Propagation Delay to a Logical "1" from Any Input to Any Output	$V_{CC} = 5.0\,V$, $V_{CC} = 10\,V$		265 100	400 200	ns ns
t_{pd1}	Propagation Delay to a Logical "1" from G1 or G2 to Any Output	$V_{CC} = 5.0\,V$, $V_{CC} = 10\,V$		265 100	400 200	ns ns
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		60		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

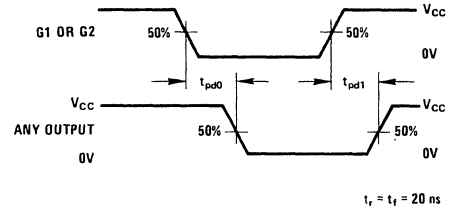
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



TL/F/5893-3



$t_r = t_f = 20$ ns

TL/F/5893-4

Truth Table

INPUTS						OUTPUTS														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

National Semiconductor

MM54C157/MM74C157 Quad 2-Input Multiplexers

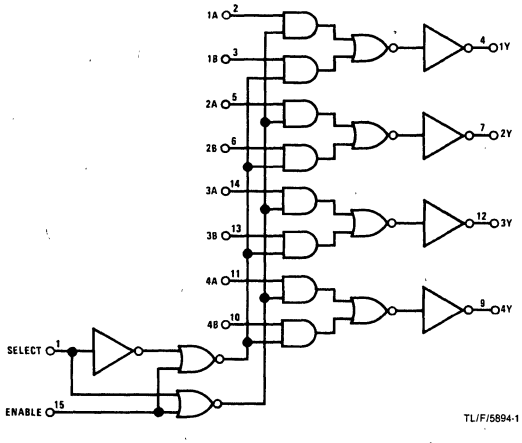
General Description

These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. They consist of four 2-input multiplexers with common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1", the outputs assume logical "0". Select decoding is done internally resulting in a single select input only.

Features

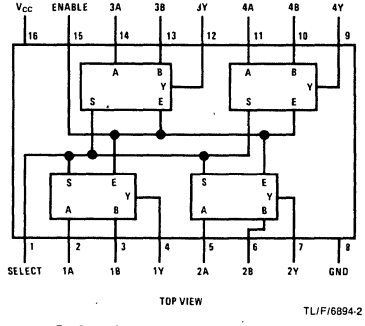
- Supply voltage range — 3 V to 15 V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 50 nW (typ.)
- Tenth power TTL compatible — drive 2 LPTTL loads

Logic and Connection Diagrams



TL/F/5894-1

Dual-In-Line Package



TOP VIEW

TL/F/6894-2

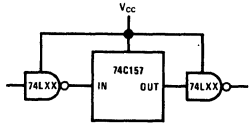
Order Number MM54C157J or MM74C157J
See NS Package J16A

Order Number MM54C157N or MM74C157N
See NS Package N16E

Truth Table

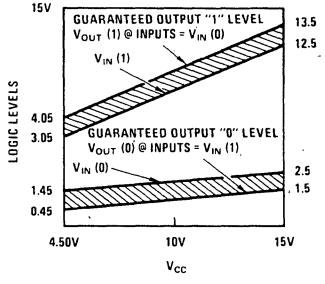
ENABLE	SELECT	A	B	OUTPUT Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1

74L Compatibility



TL/F/5894-3

Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5894-4

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC}+0.3 V	Maximum V_{CC} Voltage	18 V
Operating Temperature Range		Package Dissipation	500 mW
MM54C157	−55°C to +125°C	Operating V_{CC} Range	3 V to 15 V
MM74C157	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V,	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.05	60	μA
CMOS to Tenth Power Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −360 μA 74C V_{CC} = 4.75 V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = 360 μA 74C V_{CC} = 4.75 V, I_O = 360 μA			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay from Data to Output	V_{CC} = 5.0 V V_{CC} = 10 V		150 70	250 110	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Select to Output	V_{CC} = 5.0 V V_{CC} = 10 V		180 80	300 130	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Enable to Output	V_{CC} = 5.0 V V_{CC} = 10 V		180 80	300 130	ns ns
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

6

National Semiconductor

MM54C160/MM74C160 Decade Counter with Asynchronous Clear
MM54C161/MM74C161 Binary Counter with Asynchronous Clear
MM54C162/MM74C162 Decade Counter with Synchronous Clear
MM54C163/MM74C163 Binary Counter with Synchronous Clear

General Description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

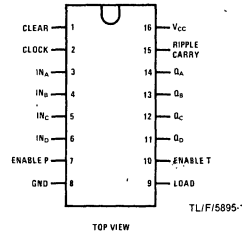
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

Features

- High noise margin — 1 V guaranteed
- High noise immunity — 0.45 V_{CC} (typ.)
- Tenth power TTL compatible — drives 2 LPTTL loads
- Wide supply voltage range — 3 V to 15 V
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable

Connection Diagram

Dual-In-Line Package



TL/F/5895-1

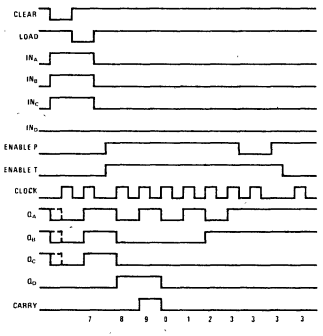
TOP VIEW

Order Number MM54C160J, MM74C160J, MM54C161J, MM74C161J, MM54C162J, MM74C162J, MM54C163J or MM74C163J
See NS Package J16A

Order Number MM54C160N, MM74C160N, MM54C161N, MM74C161N, MM54C162N, MM74C162N, MM54C163N or MM74C163N
See NS Package N16E

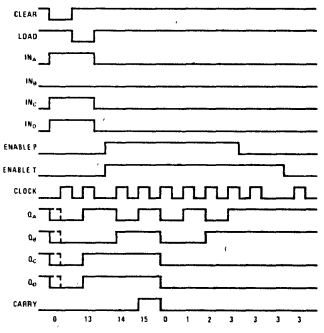
Logic Waveforms

C160, --- C162 Decade Counters



TL/F/5895-2

C161, --- C163 Binary Counters



TL/F/5895-3

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC}+0.3 V	Maximum V_{CC} Voltage	18 V
Operating Temperature Range		Package Dissipation	500 mW
MM54C160/1/2/3	−55°C to +125°C	Operating V_{CC} Range	3 V to 15 V
MM74C160/1/2/3	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V, I_O = −10 μA V_{CC} = 10 V, I_O = −10 μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V, I_O = +10 μA V_{CC} = 10 V, I_O = +10 μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V, V_{IN} = 15 V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V, V_{IN} = 0 V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.05	300	μA
CMOS to LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −360 μA 74C V_{CC} = 4.75 V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = +360 μA 74C V_{CC} = 4.75 V, I_O = +360 μA			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Sym	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time from Clock to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		250 100	400 160	ns ns
t_{pd}	Propagation Delay Time from Clock to Carry Out	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		290 120	450 190	ns ns
t_{pd}	Propagation Delay Time from T Enable to Carry Out	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		180 70	290 120	ns ns
t_{pd}	Propagation Time from Clear to Q (C160 and C161 only)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		190 80	300 150	ns ns
t_S	Time prior to Clock that Data or Load must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			120 30	ns ns
t_S	Time prior to Clock that Enable P or T must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		170 70	280 120	ns ns
t_S	Time prior to Clock that Clear must be Present (162, 163 only)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 50	190 80	ns ns
t_W	Minimum Clock Pulses Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		90 35	170 70	ns ns
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			15 5.0	μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.5	3.0 8.5		MHz MHz
C_{PD}	Power Dissipation Capacitance	Note 3		95		pF
C_{IN}	Input Capacitance	Note 2		5.0		pF

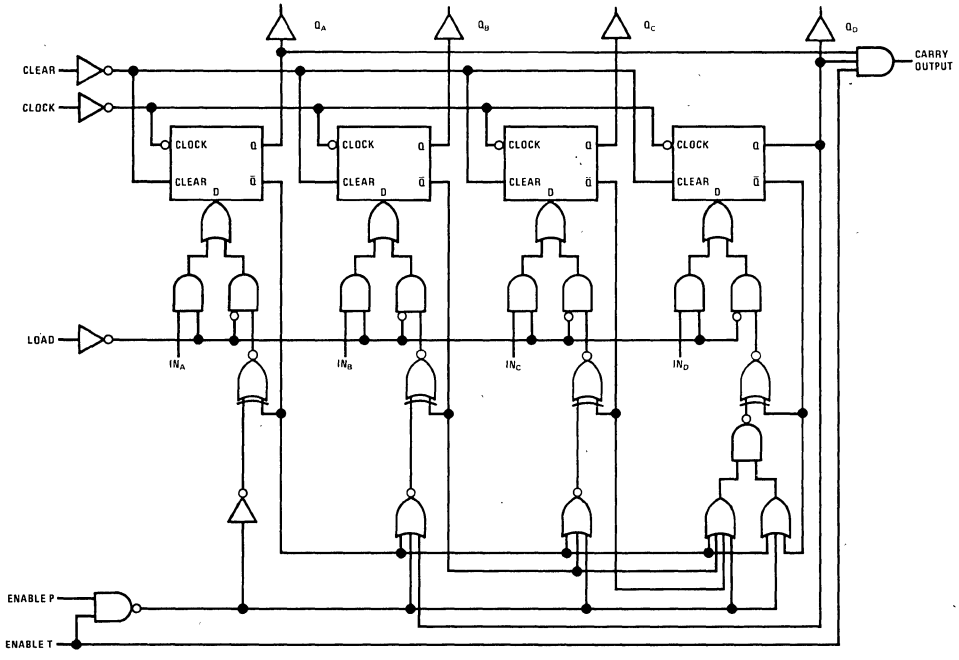
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

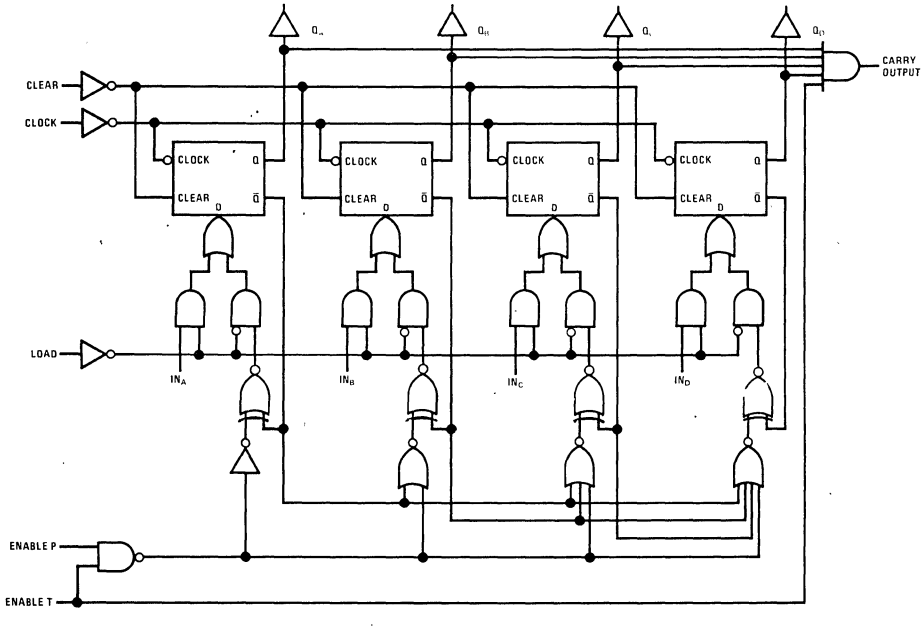
Logic Diagrams

MM74C160, MM74C162; Clear is Synchronous for the MM74C162



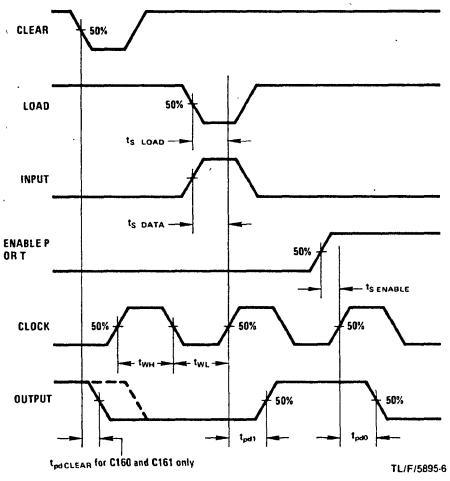
TL/F/5895-4

MM74C161, MM74C163; Clear is Synchronous for the MM74C163



TL/F/5895-5

Switching Time Waveforms

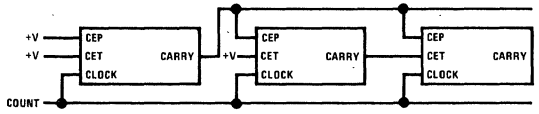


TL/F/5895-6

Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f =$ 20 ns PRR $\leq$ 1 MHz duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

Cascading Packages



TL/F/5895-7

National Semiconductor

MM54C164/MM74C164 8-Bit Parallel-Out Serial Shift Register

General Description

The MM54C164/MM74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip flop. A high-level input enables the other input which will then determine the state of the flip flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

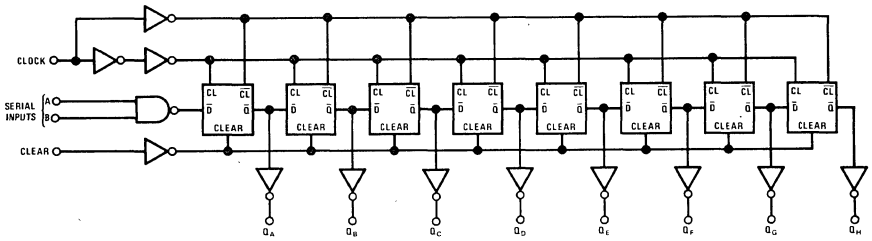
Features

■ Supply voltage range	3 V to 15 V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power	50 nW (typ.)
■ Medium speed operation	8.0 MHz (typ.) with 10 V supply

Applications

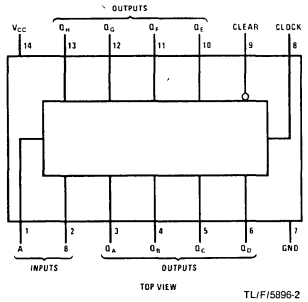
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Block and Connection Diagrams



TL/F/5896-1

Dual-In-Line Package



TL/F/5896-2

Order Number MM54C164J or MM74C164J
See NS Package J14A

Order Number MM54C164N or MM74C164N
See NS Package N14A

Truth Table

Serial Inputs A and B

INPUTS t_n		OUTPUT t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

6

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Absolute Maximum V_{CC}	18 V
Operating Temperature Range		Package Dissipation	500 mW
MM54C164	$-55°C$ to $+125°C$	Operating V_{CC} Range	3 V to 15 V
MM74C164	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\mu A$ $V_{CC}=10\,V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\mu A$ $V_{CC}=10\,V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
CMOS to LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0\,V$, $V_{IN(1)}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10\,V$, $V_{IN(1)}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

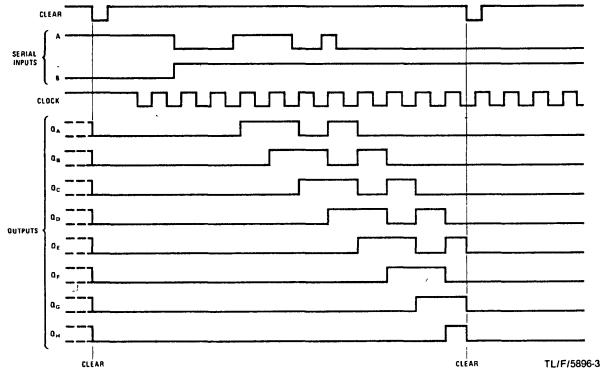
Sym	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay Time to a Logical "0" or a Logical "1" from Clock to Q	$V_{CC} = 5.0V$ $V_{CC} = 10V$		230 90	310 120	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5.0V$ $V_{CC} = 10V$		280 110	380 150	ns ns
t_S	Time Prior to Clock Pulse that Data Must be Present	$V_{CC} = 5.0V$ $V_{CC} = 10V$	200 80	110 30		ns ns
t_H	Time After Clock Pulse that Data Must be Held	$V_{CC} = 5.0V$ $V_{CC} = 10V$	0 0	0 0		ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.0 5.5	3 8		MHz MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		150 55	250 90	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	15 5.0			μs μs
C_{IN}	Input Capacitance	Any Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		140		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

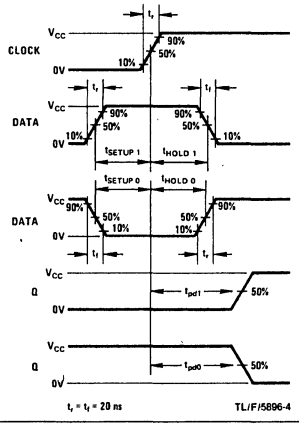
Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Logic Waveforms

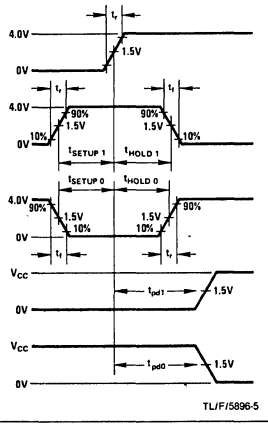


Switching Time Waveforms

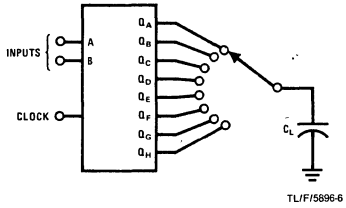
CMOS to CMOS



TTL to CMOS



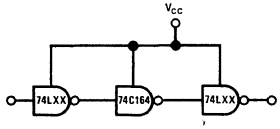
AC Test Circuit



TL/F/5896-6

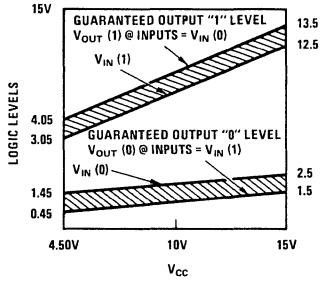
Typical Applications

74C Compatibility



TL/F/5896-7

Guaranteed Noise Margin as a Function of V_{CC}



TL/F/5896-8

National Semiconductor

MM54C165/MM74C165 Parallel-Load 8-Bit Shift Register

General Description

The MM54C165/MM74C165 is an 8-bit serial shift register which shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the shift/load input. Also included is a gated clock input and a complementary output from the eighth bit.

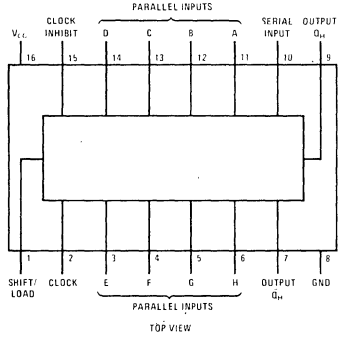
Clocking is accomplished through a 2-input NOR-gate permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the shift/load high enables the other clock input. Data transfer occurs on the positive edge of the clock. The clock inhibit input should be changed to a high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Direct overriding load	
■ Gated clock inputs	
■ Fully static operation	

Connection and Block Diagrams

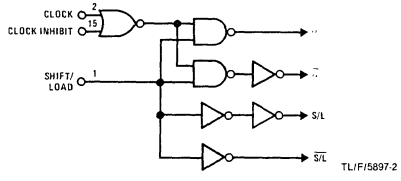
Dual-In-Line Package



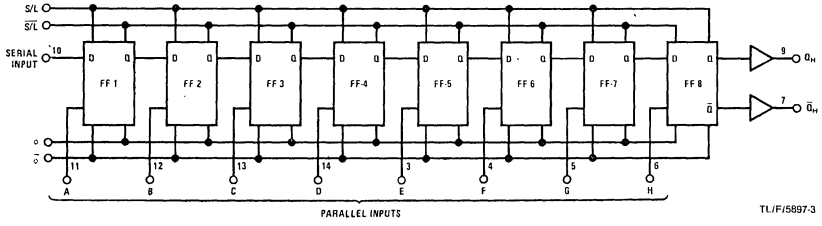
TL/F/5897-1

Order Number MM54C165J or MM74C165J
See NS Package J16A

Order Number MM54C165N or MM74C165N
See NS Package N16E



TL/F/5897-2



TL/F/5897-3

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Absolute Maximum V_{CC}	18 V
Operating Temperature Range		Package Dissipation	500 mW
MM54C165	$-55°C$ to $+125°C$	Operating V_{CC} Range	3 V to 15 V
MM74C165	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
CMOS to LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

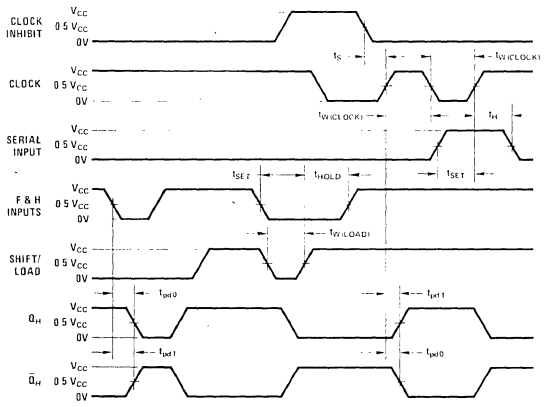
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock or Load to Q or $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	400 200	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from H to Q or $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	400 200	ns ns
t_S	Clock Inhibit Set-up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	150 60	75 30		ns ns
t_S	Serial Input Set-up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 30	25 15		ns ns
t_H	Serial Input Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 30	0 0		ns ns
t_S	Parallel Input Set-up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	150 60	75 30		ns ns
t_H	Parallel Input Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 30	0 0		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		70 30	200 100	ns ns
t_W	Minimum Load Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		85 30	180 90	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.5 5.0	6.0 12		MHz MHz
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	10 5.0			μs μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		65		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



Note A The remaining six data and the serial input are low

Note B Prior to test, high level data is loaded into H input

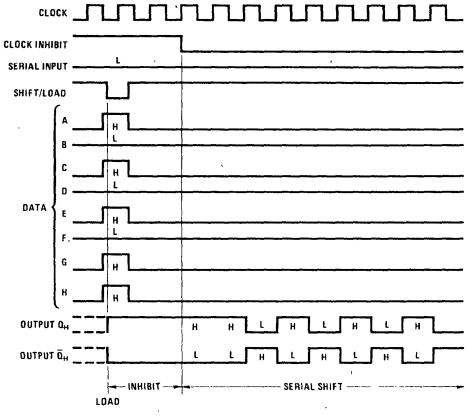
TL/F/5897-4

Truth Table

INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = $V_{IN(1)}$, L = $V_{IN(0)}$
X = irrelevant
↑ = transition from $V_{IN(0)}$ to $V_{IN(1)}$
a . . . h = the level at data inputs A thru H
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, before the indicated input conditions were established
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most recent ↑ transition of the clock.

Logic Waveforms



TL/F/5697-5

National Semiconductor

MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop

General Description

The MM54C173/MM74C173 TRI-STATE quad D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. The four D-type flip flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus-organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip flops to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip flops do not change state.

Clearing is enabled by taking the input to a logic "1" level. Clocking occurs on the positive-going transition.

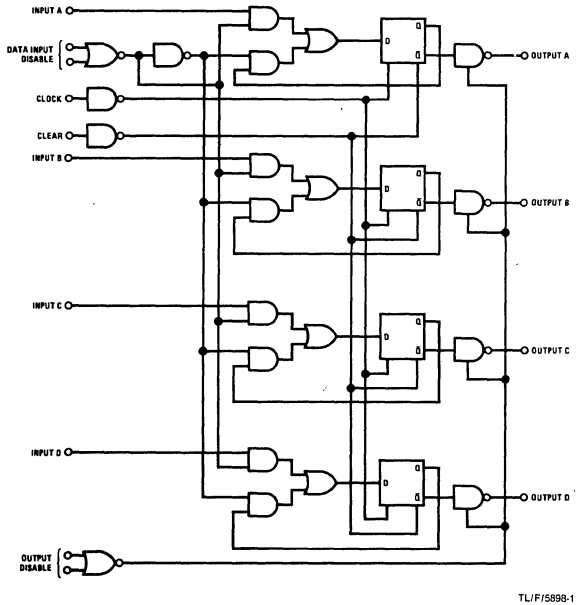
Features

- Supply voltage range 3 V to 15 V
- Tenth power TTL compatible Drive 2 LPTTL loads
- High noise immunity 0.45 V_{CC} (typ.)
- Low power
- Medium speed operation
- High impedance TRI-STATE
- Input disable without gating the clock

Applications

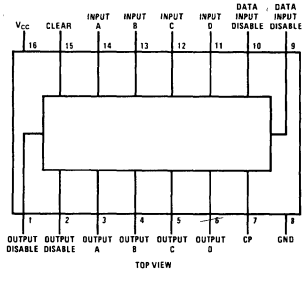
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

Logic and Connection Diagrams



TL/F/5898-1

Dual-In-Line Package



TL/F/5898-2

Order Number MM54C173J or MM74C173J
See NS Package J16A

Order Number MM54C173N or MM74C173N
See NS Package N16E

Truth Table

(Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Maximum V_{CC} Voltage	18 V
Operating Temperature Range		Package Dissipation	500 mW
MM54C173	$-55°C$ to $+125°C$	Operating V_{CC} Range	3 V to 15 V
MM74C173	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $V_{CC}=10\,V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		-1.0	-0.005		μA
I_{OZ}	Output Current in High Impedance State	$V_{CC}=15\,V$; $V_O=15\,V$ $V_{CC}=15\,V$, $V_O=0\,V$	 -1.0	0.001 0.001	1.0	μA μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
Low Power TTL/CMOS Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\,\mu A$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock	$V_{CC}=5.0\,V$, $C_L=50\,pF$, $T_A=25°C$		500		ns
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0\,V$, $V_{IN(1)}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10\,V$, $V_{IN(1)}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

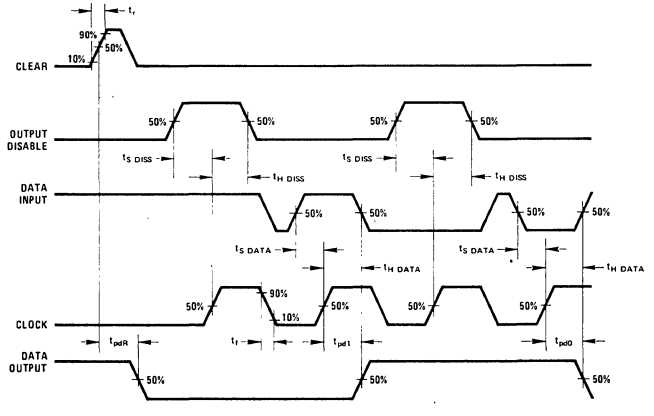
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Output	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		220 80	400 200	ns ns
t_S	Input Data Set-up Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		40 15	80 30	ns ns
t_H	Input Data Hold Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	0	0 0	ns 0	 ns
t_S	Input Disable Set-up Time, $t_{S\ DISS}$	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 35	200 70	ns ns
t_H	Input Disable Hold Time, $t_{H\ DISS}$	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		0 0	0 0	ns ns
t_{1H}, t_{0H}	Delay from Output Disable to High Impedance State (from Logical "1" or Logical "0" Level)	$V_{CC} = 5.0\,V$, $R_L = 10\,k$ $V_{CC} = 10\,V$, $R_L = 10\,k$		170 70	340 140	ns ns
t_{H1}	Delay from Output Disable to Logical "1" Level (from High Impedance State)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		170 70	340 140	ns ns
t_{H0}	Delay from Output Disable to Logical "0" Level (from High Impedance State)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		170 70	340 140	ns ns
t_{pd0}, t_{pd1}	Propagation Delay from Clear to Output	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		240 90	490 180	ns ns
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	3.0 7.0	4.0 12		MHz MHz
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 70		ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	10 5.0			μs μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)				

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms



TL/F/5898-3

National Semiconductor

MM54C174/MM74C174 Hex D Flip-Flop

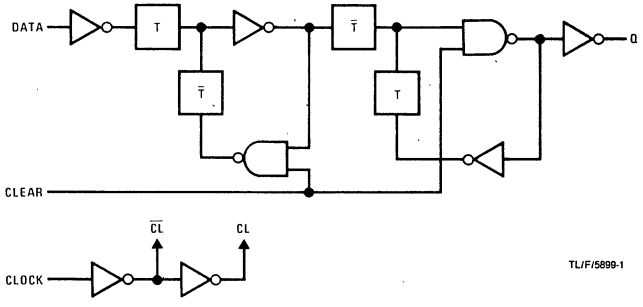
General Description

The MM54C174/MM74C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes To V_{CC} and GND.

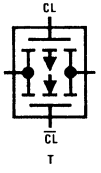
Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

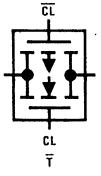
Logic and Connection Diagrams



TL/F/5899-1

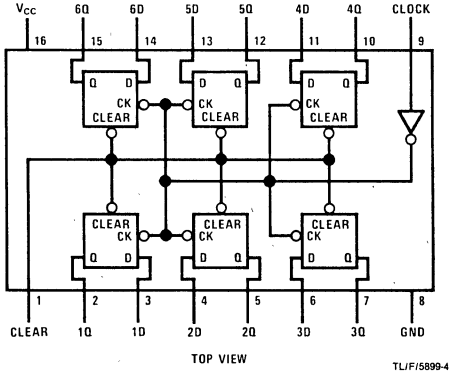


TL/F/5899-2



TL/F/5899-3

Dual-In-Line Package



TOP VIEW

TL/F/5899-4

Order Number MM54C174J or MM74C174J
See NS Package J16A

Order Number MM54C174N or MM74C174N
See NS Package N16E

Truth Table

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0 V to 15 V
MM54C174	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	18 V
MM74C174	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 70	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Clear	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		110 50	300 110	ns ns
t_{S1}, t_{S0}	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	75 25			ns ns
t_{H1}, t_{H0}	Time after Clock Pulse that Data must be Held	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	0 0	−10 −5.0		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		50 35	250 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		65 35	140 70	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	15 5.0	>1200 >1200		μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.0	6.5 12		MHz MHz
C_{IN}	Input Capacitance	Clear Input (Note 2) Any Other Input		11 5.0		pF pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		95		pF

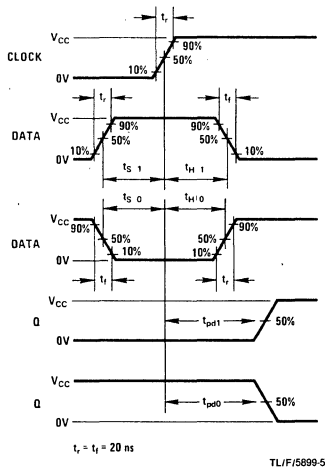
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

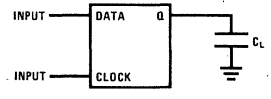
Switching Time Waveforms

CMOS to CMOS



TL/F/5899-5

AC Test Circuit



TL/F/5899-6

National Semiconductor

MM54C175/MM74C175 Quad D Flip-Flop

General Description

The MM54C175/MM74C175 consists of four positive-edge triggered D type flip-flops implemented with monolithic CMOS technology. Both are true and complemented outputs from each flip-flop are externally available. All four flip flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all four Q outputs to logical "0" and Q's to logical "1".

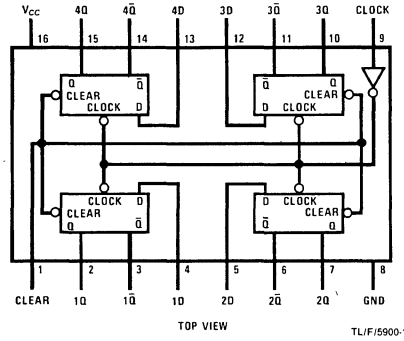
All inputs are protected from static discharge by diode clamps to V_{CC} and GND.

Features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagram and Truth Table

Dual-In-Line Package



TOP VIEW TL/F/5900-1

Order Number MM54C175J or MM74C175J
See NS Package J16A

Order Number MM54C175N or MM74C175N
See NS Package N16E

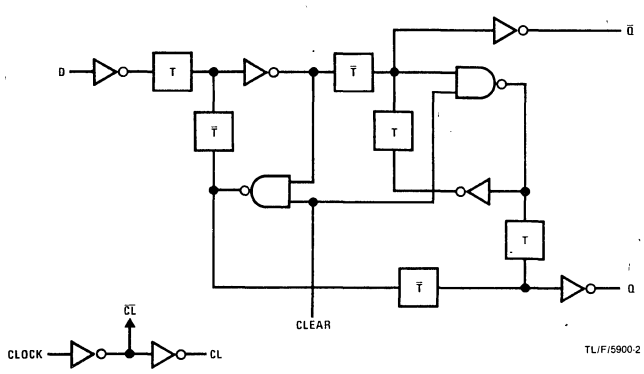
Each Flip-Flop

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

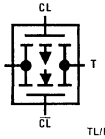
H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change

Logic Diagram

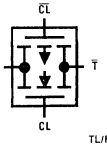
Typical One of Four



TL/F/5900-2



TL/F/5900-3



TL/F/5900-4

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3 V to 15 V
MM54C175	−55°C to +125°C	Absolute Maximum V_{CC}	18 V
MM74C175	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

Sym	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		190 75	300 110	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	300 110	ns ns
t_{pd}	Propagation Delay time to a Logical "1" from Clear to Q	$V_{CC} = 5.0V$ $V_{CC} = 10V$		230 90	400 150	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0V$ $V_{CC} = 10V$	100 40	45 16		ns ns
t_H	Time After Clock Pulse that Data must be Held	$V_{CC} = 5.0V$ $V_{CC} = 10V$	0 0	−11 −4		ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		130 45	250 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$		120 45	250 100	ns ns
t_r	Maximum Clock Rise Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	15 5.0	450 125		μs μs
t_f	Maximum Clock Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	15 5.0	50 50		μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.0 5.0	3.5 10		MHz MHz
C_{IN}	Input Capacitance	Clear Input (Note 2) Any Other Input		10 5.0		pF pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		130		pF

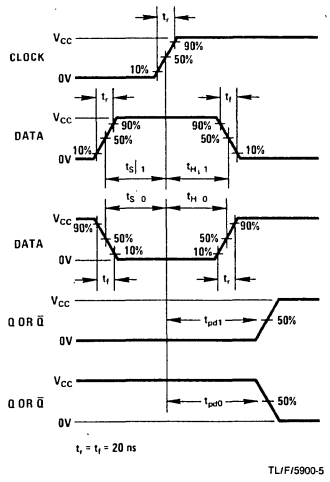
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Switching Time Waveforms

CMOS to CMOS



National Semiconductor

MM54C192/MM74C192 Synchronous 4-Bit Up/Down Decade Counter
MM54C193/MM74C193 Synchronous 4-Bit Up/Down Binary Counter

General Description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM54C192 and MM74C192 are BCD counters, while the MM54C193 and MM74C193 are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

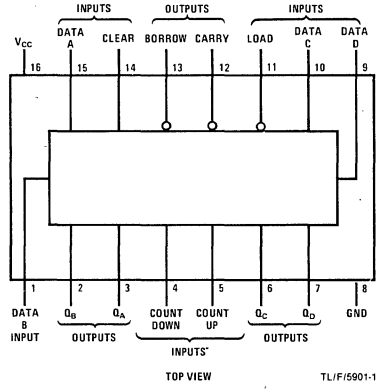
These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at a logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

Features

- High noise margin — 1 V guaranteed
- Tenth power TTL compatible — drive 2 LPTTL loads
- Wide supply range — 3 V to 15 V
- Carry and borrow outputs for N-bit cascading
- Asynchronous clear
- High noise immunity — 0.45 V_{CC} (typ.)

Connection Diagram

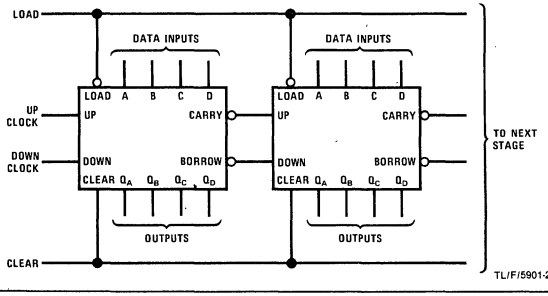
Dual-In-Line Package



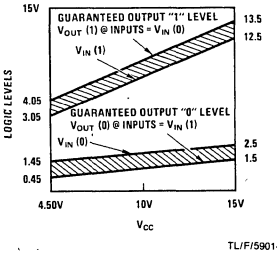
Order Number MM54C192J, MM74C192J, MM54C193J or MM74C193J
See NS Package J16A

Order Number MM54C192N, MM74C192N, MM54C193N or MM74C193N
See NS Package N16E

Cascading Packages



Guaranteed Noise Margin as A Function of V_{CC}



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Maximum V_{CC} Voltage	18 V
Operating Temperature Range		Package Dissipation	500 mW
MM54C154	$-55°C$ to $+125°C$	Operating V_{CC} Range	3 V to 15 V
MM74C154	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
CMOS to LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-100\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-100\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-1.75			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-8.0			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0\,V$, $V_{IN(1)}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current	$V_{CC}=10\,V$, $V_{IN(1)}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Q from Count Up or Down	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		250 100	400 160	ns ns
t_{pd}	Propagation Delay Time to Borrow from Count Down	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 50	200 80	ns ns
t_{pd}	Propagation Delay Time to Carry from Count Up	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 50	200 80	ns ns
t_S	Time Prior to Load that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 30	160 50	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		300 120	480 190	ns ns
t_W	Minimum Load Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 40	160 65	ns ns
t_{pd0}, t_{pd1}	Propagation Delay Time to Q from Load	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		300 120	480 190	ns ns
t_W	Minimum Count Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		120 35	200 80	ns ns
f_{MAX}	Maximum Count Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.5 6	4 10		MHz MHz
t_r, t_f	Count Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$			15 5	μs μs
C_{IN}	Input Capacitance	(Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

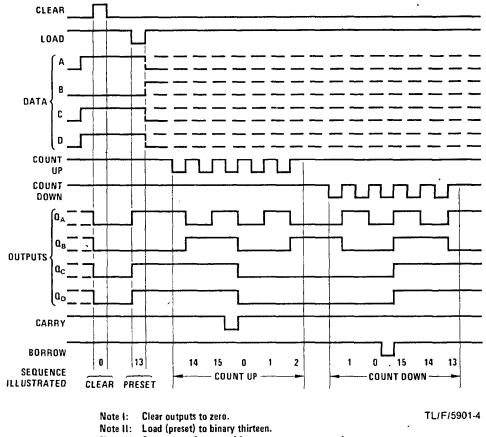
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Timing Diagrams

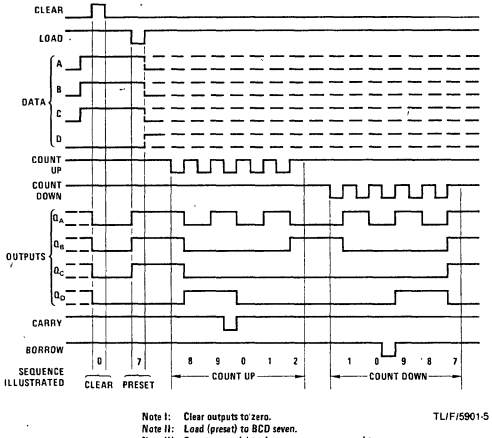
MM54C192/MM74C192



Note I: Clear outputs to zero.
Note II: Load (preset) to binary thirteen.
Note III: Count up to fourteen, fifteen, carry, zero, one and two.
Note IV: Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

TL/F/5901-4

MM54C193/MM74C193



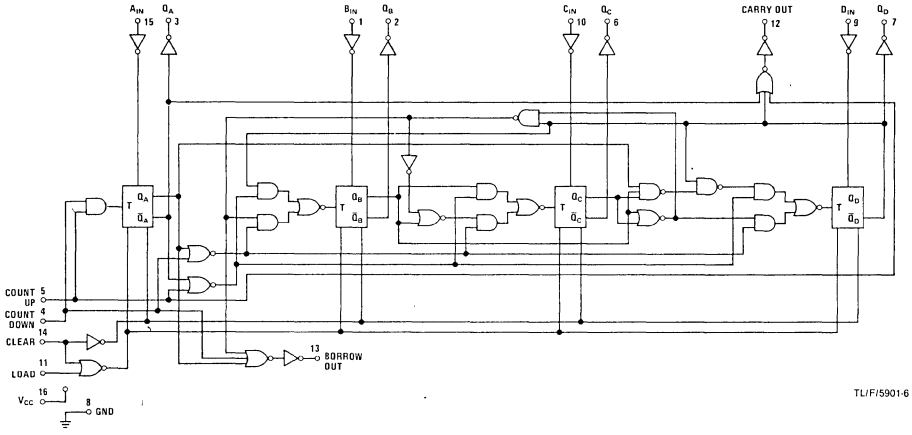
Note I: Clear outputs to zero.
Note II: Load (preset) to BCD seven.
Note III: Count up to eight, nine, carry, zero, one, and two.
Note IV: Count down to one, zero, borrow, nine, eight, and seven.

TL/F/5901-5

NOTE A: Clear overrides load, data, and count inputs.
NOTE B. When counting up, count down input must be high; when counting down, count-up input must be high.

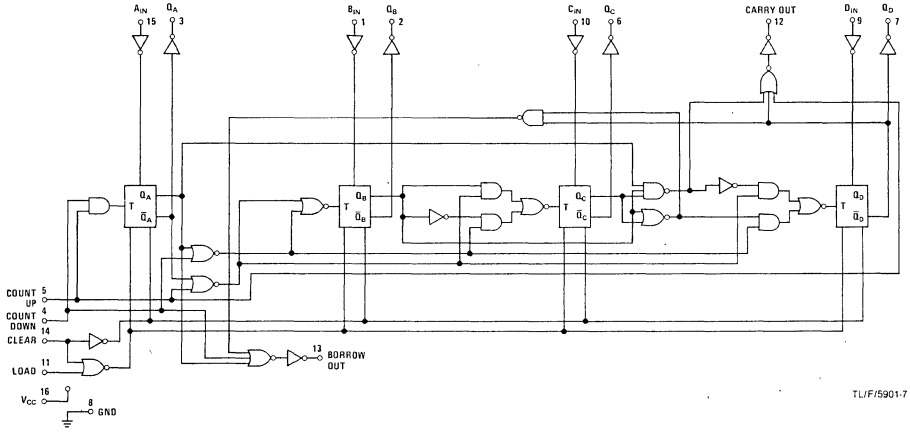
Schematic Diagrams

MM54C192 Synchronous 4-Bit Up/Down Decade Counter



TL/F/5901-6

MM54C193 Synchronous 4-Bit Up/Down Binary Counter



TL/F/5901-7

6

National Semiconductor

MM54C195/MM74C195 4-Bit Registers

General Description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible:

Parallel Load
Shift in direction Q_A towards Q_D

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control of input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-K inputs. These inputs allow the first stage to perform as a J-K, D, or T-type flip flop as shown in the truth table.

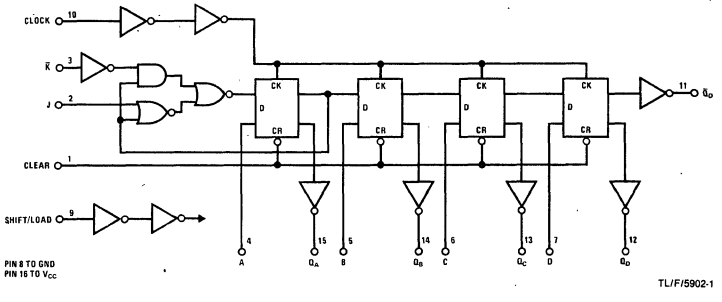
Features

- Medium speed operation — 8.5 MHz (typ.) with 10 V supply and 50 pF load
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 100 nW (typ.)
- Tenth power TTL compatible — drive 2 LPTTL loads
- Supply voltage range — 3 V to 15 V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and K inputs to first stage
- Complementary outputs from last stage
- Positive-edge triggered clocking
- Diode clamped inputs to protect against static charge

Applications

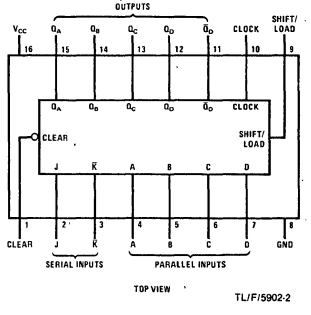
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

Schematic and Connection Diagrams



TL/F/5902-1

Dual-In-Line Package



TL/F/5902-2

Order Number MM54C195J or MM74C195J
See NS Package J16A

Order Number MM54C195N or MM74C195N
See NS Package N16E

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3 V to V_{CC} + 0.3 V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0 V to 15 V
MM54C195	−55°C to +125°C	Absolute Maximum V_{CC}	18 V
MM74C195	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

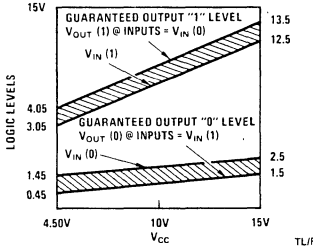
Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0 V V_{CC} = 10 V			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0 V V_{CC} = 10 V	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0 V, V_{CC} = 10 V			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15 V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15 V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15 V		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V	V_{CC} − 1.5 V_{CC} − 1.5		 V	V
$V_{IN(0)}$	Logical "0" Input Voltage	54C V_{CC} = 4.5 V 74C V_{CC} = 4.75 V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C V_{CC} = 4.5 V, I_O = −360 μA 74C V_{CC} = 4.75 V, I_O = −360 μA	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C V_{CC} = 4.5 V, I_O = 360 μA 74C V_{CC} = 4.75 V, I_O = 360 μA			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−1.75			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V T_A = 25°C, V_{OUT} = 0 V	−8.0			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
I_{SINK}	Output Sink Current	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Truth Table

INPUTS AT t_n		OUTPUTS AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Note. H = HIGH LEVEL, L = LOW LEVEL
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_{An} = State of Q_A at t_n

Guaranteed noise Margin as a Function of V_{CC}



TL/F/5902-3

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Sym	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 75	300 130	ns ns
t_{pd}	Propagation Delay Time to a Logical "0" or Logical "1" from Clear to Q or $\overline{Q}$	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		150 50	300 130	ns ns
t_S	Time Prior to Clock Pulse that Data must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		80 35	200 70	ns ns
t_S	Time Prior to Clock Pulse that Shift/Load must be Present	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		110 60	150 90	ns ns
t_H	Time After Clock Pulse that Data must be Held	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		−10 −5.0	0 0	ns ns
t_W	Minimum Clear Pulse Width ($t_{WL} = t_{WH}$)	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		100 50	200 100	ns ns
t_W	Minimum Clear Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		90 40	130 60	ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	5.0 2.0			μs μs
f_{MAX}	Maximum Input Clock Frequency	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	2.0 5.5	3.0 8.5		MHz MHz
C_{IN}	Input Capacitance	(Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

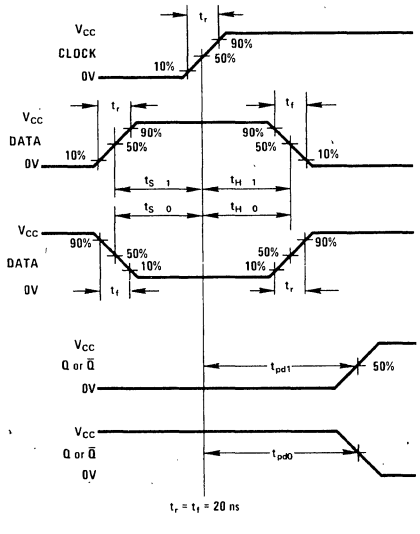
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

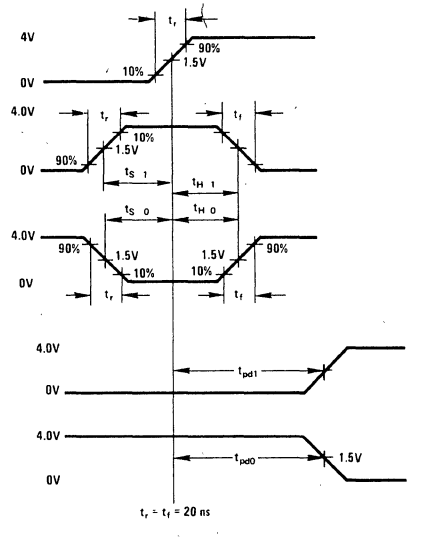
Switching Time Waveforms

CMOS to CMOS



TL/F/5902-4

TTL to CMOS



TL/F/5902-5

National Semiconductor

MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. The internal address register, latches, and address information are on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line, working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs, provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is therefore unnecessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different from the DM74200 in that a positive to negative transition of the $\overline{CE}_3$ must occur for the memory to be selected.

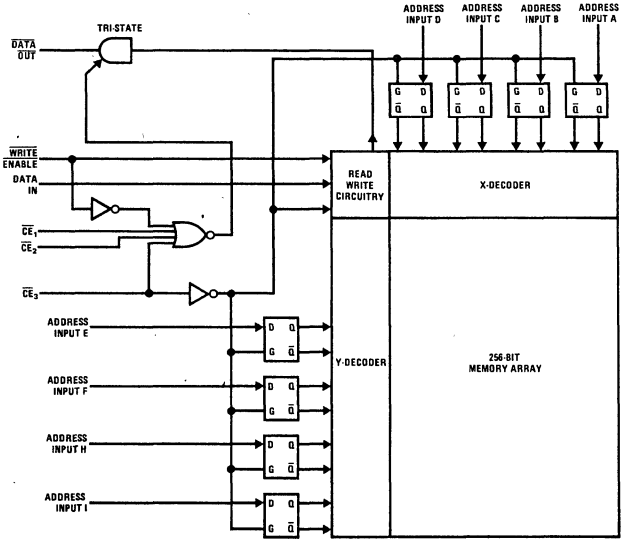
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and $\overline{WE}$ high. Holding either $\overline{CE}_1$, $\overline{CE}_2$, or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus-organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control provides for fast access times by not totally disabling the chip.

Write Operation: Data is written into the memory with $\overline{CE}_3$ low and $\overline{WE}$ low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with $\overline{WE}$ low.

Features

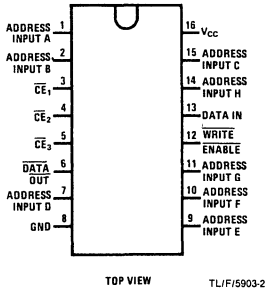
■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW (typ.)
■ Internal address register	

Logic and Connection Diagrams



TL/F/5903-1

Dual-In-Line Package



TOP VIEW TL/F/5903-2

Order Number MM54C200J or MM74C200J
See NS Package J16A

Order Number MM54C200N or MM74C200N
See NS Package N16E

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0 V to 15 V
MM54C200	−55°C to +125°C	Absolute Maximum V_{CC}	18 V
MM74C200	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.10	600	μA
CMOS/TTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-1.6\,mA$ 74C $V_{CC}=4.75$, $I_O=-1.6\,mA$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=1.6\,mA$ 74C $V_{CC}=4.75$, $I_O=1.6\,mA$			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=0\,V$ $T_A=25°C$	−4.0 −1.8	−6.0		mA mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10\,V$, $V_{OUT}=0\,V$ $T_A=25°C$	−16.0 −1.5	−25		mA mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	5.0	8.0		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10\,V$, $V_{OUT}=V_{CC}$ $T_A=°C$	20	30		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Sym	Parameter	Conditions	Min	Typ	Max	Units
t_{ACC}	Access Time from Address	$V_{CC} = 5.0V$ $V_{CC} = 10V$		450 200	900 400	ns ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		360 120	700 300	ns ns
t_{pCE1}	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		250 85	700 200	ns ns
t_{SA}	Address Setup Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	200 100	80 30		ns ns
t_{HA}	Address Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 25	15 5.0		ns ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$	300 150	160 70		ns ns
t_{CE}	$\overline{CE}_3$ Pulse Widths	$V_{CC} = 5.0V$ $V_{CC} = 10V$	400 160	200 80		ns ns
C_{IN}	Input Capacity	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacity in TRI-STATE	(Note 2)		9.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		400		pF

$C_L = 50\,pF$

Sym	Parameter	Conditions	MM54C200 $T_A = -55°C$ to $+125°C$		MM74C200 $T_A = -45°C$ to $+85°C$		Units
			Min	Max	Min	Max	
t_{ACC}	Access Time from Address	$V_{CC} = 5.0V$ $V_{CC} = 10V$		1200 520		1100 480	ns ns
t_{pd}	Propagation Delay from $\overline{CE}_3$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		950 400		850 360	ns ns
$t_{pd\overline{CE1}}$	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	$V_{CC} = 5.0V$ $V_{CC} = 10V$		650 300		600 275	ns ns
t_{SA}	Address Setup Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	250 120		250 120		ns ns
t_{HA}	Address Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	100 50		100 50		ns ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$	450 225		400 200		ns ns
t_{CE}	Disable Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$	500 250		460 230		ns ns
t_{HD}	Data Hold Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	50 25		50 25		ns ns

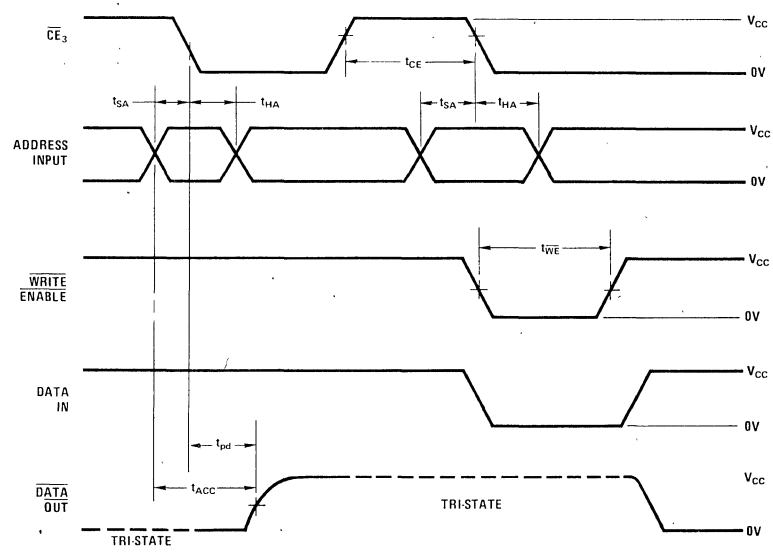
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

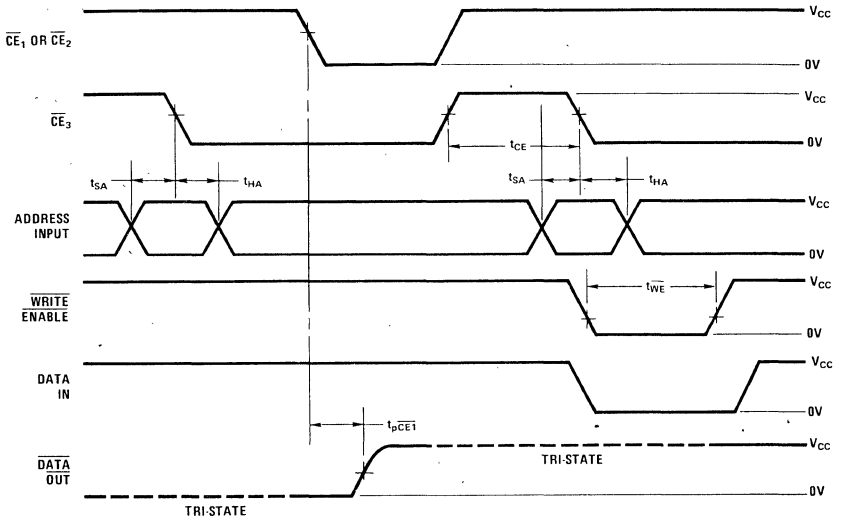
Switching Time Waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1 = \overline{CE}_2$ = logic 0)



TL/F/5903-3

Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.

TL/F/5903-4

National Semiconductor

MM54C221/MM74C221 Dual Monostable Multivibrator

General Description

The MM54C221/MM74C221 dual monostable multivibrator is a monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transtion-triggered input and a positive-transition-triggered input, either of which can be used as an inhibit input, and a clear input.

Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT}. The pulse width is stable over a wide range of temperature and V_{CC}.

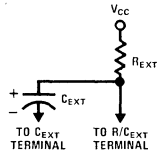
Pulse stability will be limited by the accuracy of external timing components. The pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT}\ R_{EXT}$. For further information and applications, see AN-138.

Features

- Wide supply voltage range — 4.5 V to 15 V
- Guaranteed noise margin — 1.0 V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power TTL compatibility — fan out of 2 driving 74L

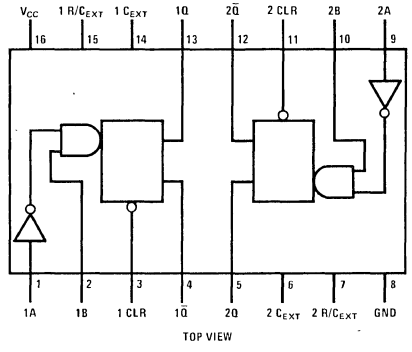
Connection Diagrams

Timing Component



TL/F/5904-1

Dual-In-Line Package



TL/F/5904 2

Order Number MM54C221J or MM74C221J
See NS Package J16A

Order Number MM54C221N or MM74C221N
See NS Package N16E

Truth Table

INPUTS			OUTPUTS	
CLEAR.	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎴
H	↓	H	⎍	⎴

H = High level
L = Low level
↑ = Transition from low to high
↓ = Transition from high to low
⎍ = One high level pulse
⎴ = One low level pulse
X = Irrelevant

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	4.5 V to 15 V
MM54C221	−55°C to +125°C	Absolute Maximum V_{CC}	18 V
MM74C221	−40°C to +85°C	$R_{EXT} \geq 80\,V_{CC}$ (Ω)	
Storage Temperature Range	−65°C to +150°C	Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Max/min limits apply across temperature range, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current (Standby)	$V_{CC}=15\,V$, $R_{EXT}=\infty$, Q1, Q2 = Logic "0" (Note 3)		0.05	300	μA
I_{CC}	Supply Current (During Output Pulse)	$V_{CC}=15\,V$, Q1 = Logic "1", Q2 = Logic "0" (Figure 4)		15		mA
		$V_{CC}=5.0\,V$, Q1 = Logic "1", Q2 = Logic "0" (Figure 4)		2.0		mA
	Leakage Current at R/C_{EXT} Pin	$V_{CC}=15\,V$, $V_{CEXT}=5.0\,V$		0.01	3.0	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\,\mu A$	2.4 2.4			V V
$V_{OUT(O)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=360\,\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−1.75			mA
I_{SOURCE}	Output Source Current (P-channel)	$V_{CC}=10\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	−8.0			mA
I_{SINK}	Output Sink Current (N-channel)	$V_{CC}=5.0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	1.75			mA
I_{SINK}	Output Sink Current (N-channel)	$V_{CC}=10\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	8.0			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Sym	Parameter	Conditions	Min	Typ	Max	Units
$t_{pd\ A,B}$	Propagation Delay from Trigger Input (A,B) to Output Q, $\overline{Q}$	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		250 120	500 250	ns ns
$t_{pd\ CL}$	Propagation Delay from Clear Input (CL) to Output Q, $\overline{Q}$	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		250 120	500 250	ns ns
t_S	Time Prior to Trigger Input (A,B) that Clear must be Set	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	150 60	50 20		ns ns
$t_{W(A,B)}$	Trigger Input (A,B) Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	150 70	50 30		ns ns
$t_{W(CL)}$	Clear Input (CL) Pulse Width	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$	150 70	50 30		ns ns
$t_{W(OUT)}$	Q or $\overline{Q}$ Output Pulse Width	$V_{CC} = 5.0\,V$, $R_{EXT} = 10\,k$, $C_{EXT} = 0\,pF$		900		ns
		$V_{CC} = 10\,V$, $R_{EXT} = 10\,k$, $C_{EXT} = 0\,pF$		350		ns
		$V_{CC} = 15\,V$, $R_{EXT} = 10\,k$, $C_{EXT} = 0\,pF$		320		ns
		$V_{CC} = 5.0\,V$, $R_{EXT} = 10\,k$, $C_{EXT} = 1000\,pF$ (Fig. 1)	9.0	10.6	12.2	μs
		$V_{CC} = 10\,V$, $R_{EXT} = 10\,k$, $C_{EXT} = 1000\,pF$ (Fig. 1)	9.0	10	11	μs
		$V_{CC} = 15\,V$, $R_{EXT} = 10\,k$, $C_{EXT} = 1000\,pF$ (Fig. 1)	8.9	9.8	10.8	μs
		$V_{CC} = 5.0\,V$, $R_{EXT} = 10\,k$, $C_{EXT} = 0.1\,\mu F$ (Fig. 2)	900	1020	1200	μs
		$V_{CC} = 10\,V$, $R_{EXT} = 10\,k$, $C_{EXT} = 0.1\,\mu F$ (Fig. 2)	900	1000	1100	μs
		$V_{CC} = 15\,V$, $R_{EXT} = 10\,k$, $C_{EXT} = 0.1\,\mu F$ (Fig. 2)	900	990	1100	μs
R_{ON}	ON Resistance of Transistor between R/C_{EXT} to C_{EXT}	$V_{CC} = 5.0\,V$ (Note 4) $V_{CC} = 10\,V$ (Note 4) $V_{CC} = 15\,V$ (Note 4)		50 25 16.7	150 65 45	Ω Ω Ω
	Output Duty Cycle	$R = 10\,k$, $C = 1000\,pF$ $R = 10\,k$, $C = 0.1\,\mu F$ (Note 5)			90 90	% %
C_{IN}	Input Capacitance	R/C_{EXT} Input (Note 2) Any Other Input (Note 2)		15 5.0	25	pF pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

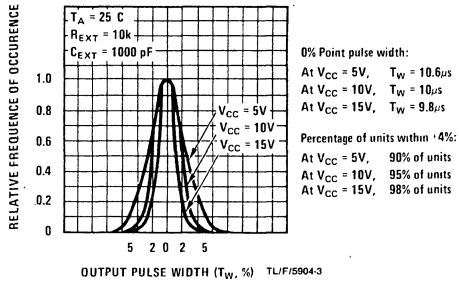
Note 3: In Standby (Q = Logic "0") the power dissipated equals the leakage current plus V_{CC}/R_{EXT}.

Note 4: See AN-138 for detailed explanation of R_{ON}.

Note 5: Maximum output duty cycle = $R_{EXT} / R_{EXT} + 1000$.

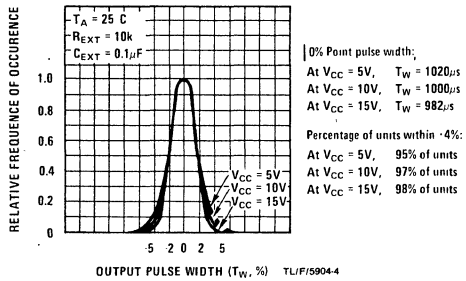
6

Typical Performance Characteristics



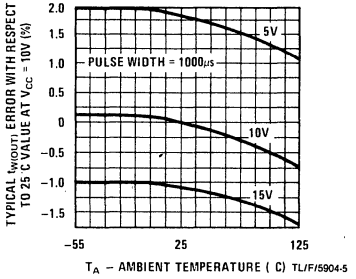
TL/F/5904-3

Figure 1. Typical Distribution of Units for Output Pulse Width



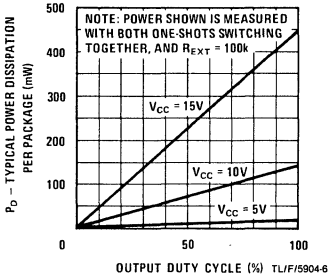
TL/F/5904-4

Figure 2. Typical Distribution of Units for Output Pulse Width



TL/F/5904-5

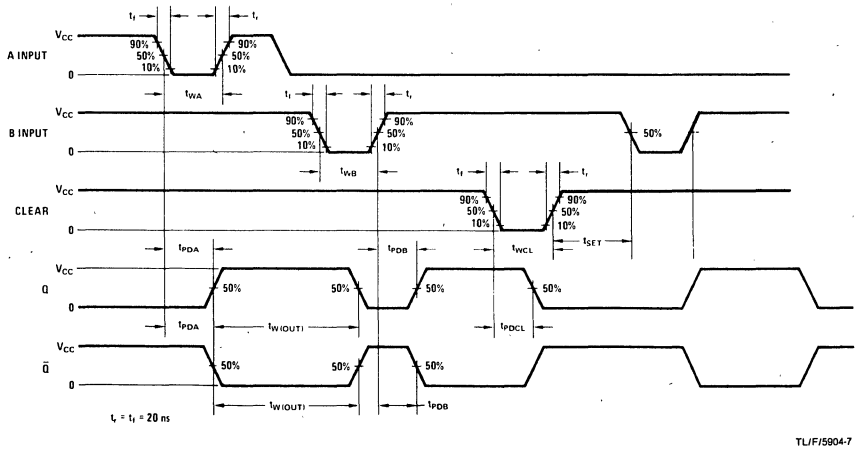
Figure 3. Typical Variation in Output Pulse Width vs Temperature



TL/F/5904-6

Figure 4. Typical Power Dissipation per Package

Switching Time Waveforms



TL/F/5904-7

National Semiconductor

MM54C240/MM74C240 Inverting
MM54C244/MM74C244 Non-Inverting
Octal Buffers and Line Drivers with TRI-STATE® Outputs

General Description

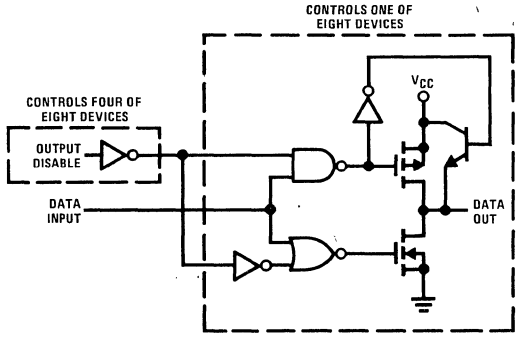
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state. For improved TTL input compatibility see MM74C941.

Features

- Wide supply voltage range (3V to 15V)
- High noise immunity (0.45 V_{CC} typ)
- Low power consumption
- High capacitive load drive capability
- TRI-STATE outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package
- High speed 25 ns (typ.) @ 10V, 50 pF (MM74C244)

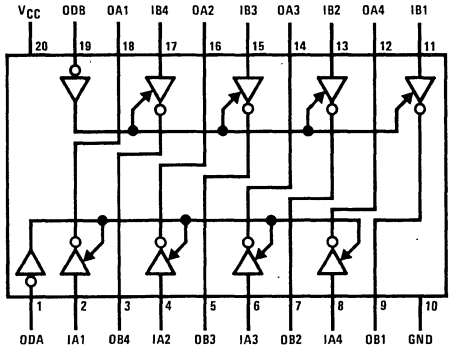
Logic and Connection Diagrams

MM54C240/MM74C240



TL/F/5905-1

MM54C240/MM74C240 Dual-In-Line Package

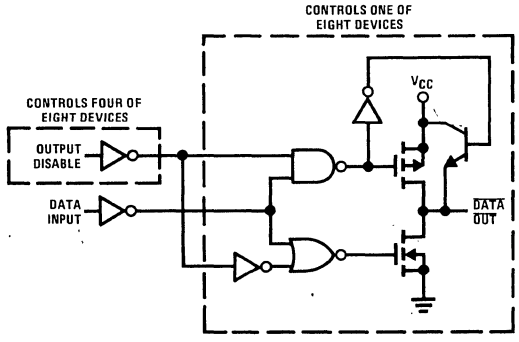


TOP VIEW

TL/F/5905-2

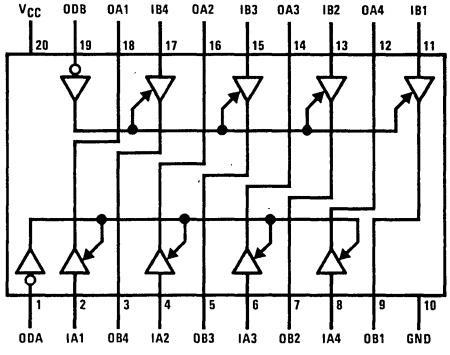
Order Number MM54C240J, MM74C240J, MM54C240N or MM74C240N
See NS Package J20A or N20A

MM54C244/MM74C244



TL/F/5905-3

MM54C244/MM74C244 Dual-In-Line Package



TOP VIEW

TL/F/5905-4

Order Number MM54C244J, MM74C244J, MM54C244N or MM74C244N
See NS Package J20A or N20A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3V to 15V
MM54C240, MM54C244	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	18V
MM74C240, MM74C244	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\ \mu A$ $V_{CC}=10V$, $I_O=-10\ \mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=10\ \mu A$ $V_{CC}=10V$, $I_O=10\ \mu A$			0.5 1.0	V V
I_{OZ}	TRI-STATE Output Current	$V_{CC}=10V$, $OD=V_{IH}$			± 10	μA
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-450\ \mu A$ 74C, $V_{CC}=4.75V$, $I_O=-450\ \mu A$	$V_{CC}-0.4$ $V_{CC}-0.4$			V V
		54C, $V_{CC}=4.5V$, $I_O=-2.2\ mA$ 74C, $V_{CC}=4.75V$, $I_O=-2.2\ mA$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=2.2\ mA$ 74C, $V_{CC}=4.75V$, $I_O=2.2\ mA$			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	-14.0	-30.0		mA
		$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	-36.0	-70.0		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	12.0	20.0		mA
		$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	48.0	70.0		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

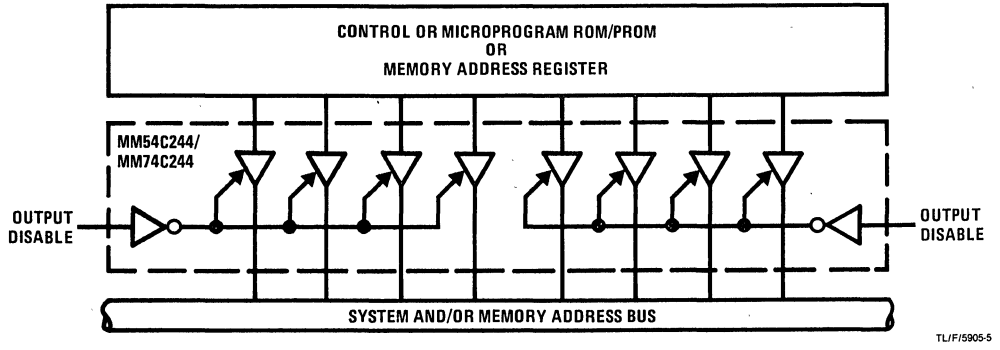
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{Pd(1)}$, $t_{Pd(0)}$	Propagation Delay (Data In to Out) MM54C240/MM74C240	$V_{CC} = 5V$, $C_L = 50$ pF		60	90	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		40	70	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		80	110	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		60	90	ns
	MM54C244/MM74C244	$V_{CC} = 5V$, $C_L = 50$ pF		45	70	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		25	50	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		60	90	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		40	70	ns
t_{1H}, t_{0H}	Propagation Delay Output Disable to High Impedance State (from a Logic Level)	$R_L = 1k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		45	80	ns
		$V_{CC} = 10V$		35	60	ns
t_{H1}, t_{H0}	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		50	90	ns
		$V_{CC} = 10V$		30	60	ns
$t_{T(HL)}$, $t_{T(LH)}$	Transition Time	$V_{CC} = 5V$, $C_L = 50$ pF		45	80	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		30	60	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		75	140	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		50	100	ns
C_{PD}	Power Dissipation Capacitance (Output Enabled Per Buffer)	(See Note 3)				
	MM54C240/MM74C240			100		pF
	MM54C244/MM74C244			100		pF
	(Output Disabled Per Buffer)					
	MM54C240/MM74C240			10		pF
	MM54C244/MM74C244			0		pF
C_{IN}	Input Capacitance (Any Input)	$V_{IN} = 0V$, $f = 1MHz$, $T_A = 25°C$		10		pF
C_O	Output Capacitance (Output Disabled)	$V_{IN} = 0V$, $f = 1MHz$, $T_A = 25°C$		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Typical Application



TL/F/5905-5

Truth Tables

MM54C240/MM74C240

ODA	IA	OA
1	X	Z
1	X	Z
0	0	1
0	1	0

ODB	IB	OB
1	X	Z
1	X	Z
0	0	1
0	1	0

MM54C244/MM74C244

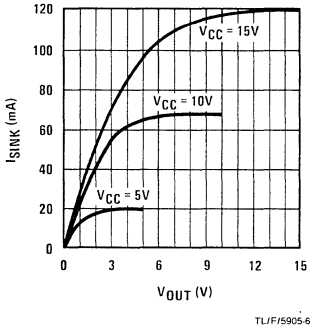
ODA	IA	OA
1	X	Z
1	X	Z
0	0	0
0	1	1

ODB	IB	OB
1	X	Z
1	X	Z
0	0	0
0	1	1

1 = High
0 = Low
X = Don't Care
Z = TRI-STATE

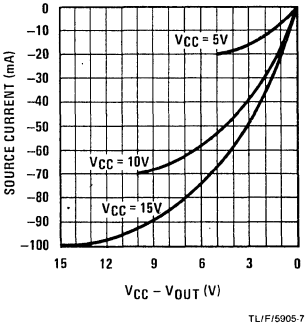
Typical Performance Characteristics

N-Channel Output Drive @ 25°C



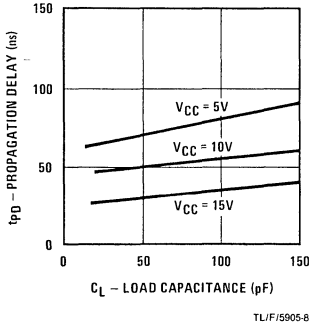
TL/F/5905-6

P-Channel Output Drive @ 25°C



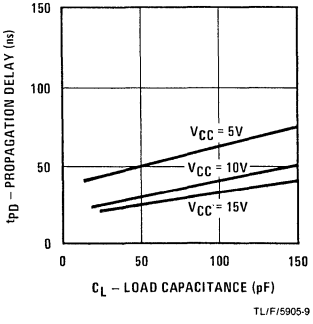
TL/F/5905-7

MM54C240/MM74C240 Propagation Delay Vs. Load Capacitance



TL/F/5905-8

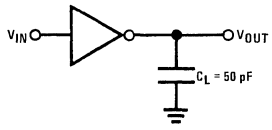
MM54C244/MM74C244 Propagation Delay Vs. Load Capacitance



TL/F/5905-9

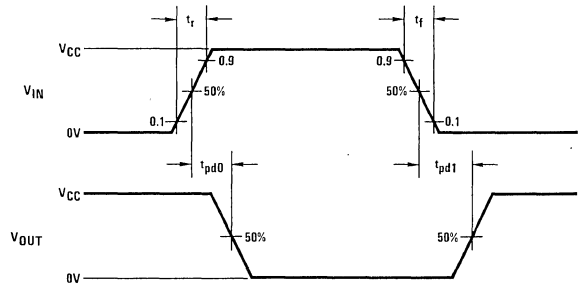
AC Test Circuits and Switching Time Waveforms

t_{pd0}, t_{pd1}



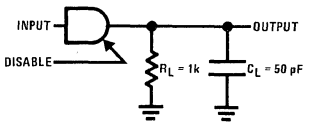
TL/F/5905-10

CMOS to CMOS



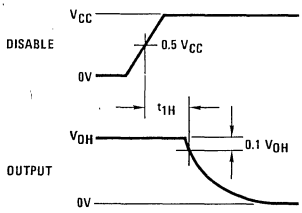
TL/F/5905-11

t_{1H} and t_{H1}

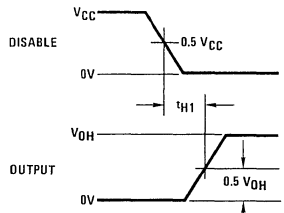


TL/F/5905-12

t_{1H}



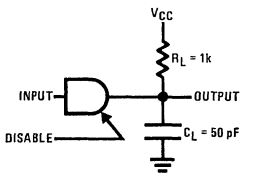
t_{H1}



TL/F/5905-13

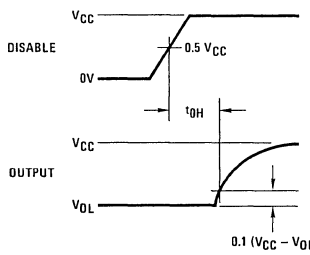
Note: V_{OH} is defined as the DC output high voltage when the device is loaded with a 1 kΩ resistor to ground.

t_{0H} and t_{H0}

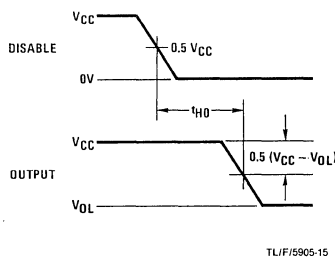


TL/F/5905-14

t_{0H}



t_{H0}



TL/F/5905-15

Note: V_{OL} is defined as the DC output low voltage when the device is loaded with a 1 kΩ resistor to V_{CC}.

Note: Delays measured with input t_r, $t_f \leq 20$ ns

National Semiconductor

MM54C373/MM74C373 TRI-STATE® Octal D-Type Latch
MM54C374/MM74C374 TRI-STATE Octal D-Type Flip-Flop

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When $\overline{\text{LATCH ENABLE}}$ is high, the Q outputs will follow the D inputs. When $\overline{\text{LATCH ENABLE}}$ goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until $\overline{\text{LATCH ENABLE}}$ returns high again.

The MM54C374/MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

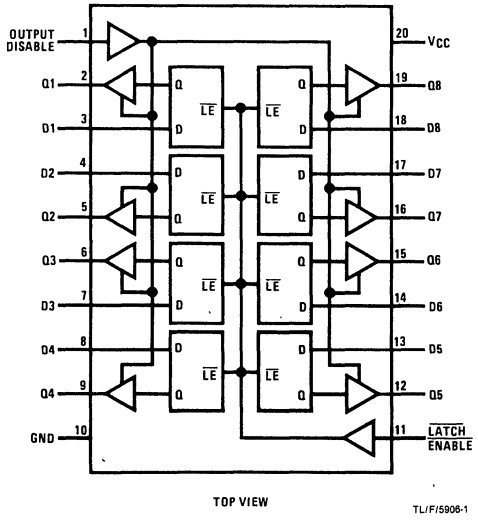
Both the MM54C373/MM74C373 and the MM54C374/MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300" pin centers.

Features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power consumption
- TTL compatibility — fan-out of 1 driving standard TTL
- Bus driving capability
- TRI-STATE outputs
- Eight storage elements in one package
- Single CLOCK/$\overline{\text{LATCH ENABLE}}$ and OUTPUT DISABLE control inputs
- 20-pin dual-in-line package with 0.300" centers takes half the board space of a 24-pin package

Connection Diagrams

MM54C373/MM74C373
Dual-In-Line Package



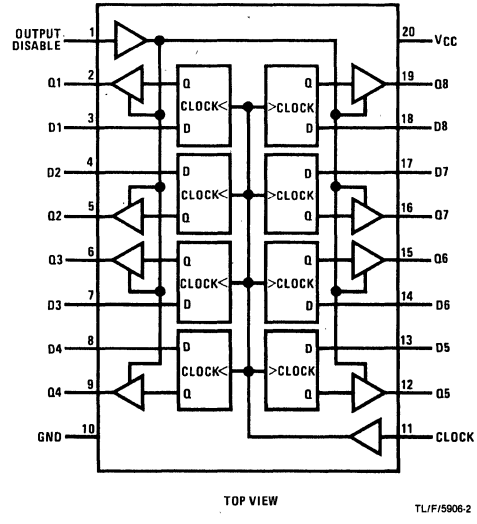
TOP VIEW

TL/F/5906-1

Order Number MM54C373J or MM74C373J
See NS Package J20A

Order Number MM54C373N or MM74C373N
See NS Package N20A

MM54C374/MM74C374
Dual-In-Line Package



TOP VIEW

TL/F/5906-2

Order Number MM54C374J or MM74C374J
See NS Package J20A

Order Number MM54C374N or MM74C374N
See NS Package N20A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3 V to 15 V
MM54C373	−55°C to +125°C	Absolute Maximum V_{CC}	18 V
MM74C373	−40°C to +85°C	Lead Temperature (Soldering, 10 sec.)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $I_O=+10\,\mu A$ $V_{CC}=10\,V$, $I_O=+10\,\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{OZ}	TRI-STATE Leakage Current	$V_{CC}=15\,V$, $V_O=15\,V$ $V_{CC}=15\,V$, $V_O=0\,V$	 −1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-360\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-360\,\mu A$	$V_{CC}-0.4$ $V_{CC}-0.4$			V V
		54C $V_{CC}=4.5\,V$, $I_O=-1.6\,mA$ 74C $V_{CC}=4.75\,V$, $I_O-1.6\,mA$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=1.6\,mA$ 74C $V_{CC}=4.75\,V$, $I_O=1.6\,mA$			0.4 0.4	V V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\,V$, $V_{OUT}=0\,V$ $T_A=25°C$ (Note 4)	−12	−24		mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\,V$, $V_{OUT}=0\,V$ $T_A=25°C$ (Note 4)	−24	−48		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=V_{CC}$ $T_A=25°C$ (Note 4)	6.0	12		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10\,V$, $V_{OUT}=V_{CC}$ $T_A=25°C$ (Note 4)	24	48		mA

6

AC Electrical Characteristics

MM54C373/MM74C373 $T_A = 25°C$, $C_L = 50\,pF$, $t_r = t_f = 20\,ns$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay, $\overline{\text{LATCH ENABLE}}$ to Output	$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		165	330	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		70	140	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		195	390	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		85	170	ns
t_{pd0}, t_{pd1}	Propagation Delay Data In to Output	$\overline{\text{LATCH ENABLE}} = V_{CC}$				
		$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		155	310	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		70	140	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		185	370	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		85	170	ns
$t_{SET\text{-}UP}$	Minimum Set-Up Time Data In to CLOCK/$\overline{\text{LATCH ENABLE}}$	$t_{HOLD} = 0\,ns$				
		$V_{CC} = 5.0\,V$		70	140	ns
		$V_{CC} = 10\,V$		35	70	ns
f_{MAX}	Maximum $\overline{\text{LATCH ENABLE}}$ Frequency	$V_{CC} = 5.0\,V$	3.5	6.7		MHz
		$V_{CC} = 10\,V$	4.5	9.0		MHz
t_{PWH}	Minimum $\overline{\text{LATCH ENABLE}}$ Pulse Width	$V_{CC} = 5.0\,V$		75	150	ns
		$V_{CC} = 10\,V$		55	110	ns
t_r, t_f	Maximum $\overline{\text{LATCH ENABLE}}$ Rise and Fall Time	$V_{CC} = 5.0\,V$		NA		μs
		$V_{CC} = 10\,V$		NA		μs
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	$R_L = 10\,k$, $C_L = 5\,pF$				
		$V_{CC} = 5.0\,V$		105	210	ns
		$V_{CC} = 10\,V$		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	$R_L = 10\,k$, $C_L = 50\,pF$				
		$V_{CC} = 5.0\,V$		105	210	ns
		$V_{CC} = 10\,V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		65	130	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		35	70	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		110	220	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		70	140	ns
C_{LE}	Input Capacitance	$\overline{\text{LE}}$ Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 2)		5.0	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		200		pF

AC Electrical Characteristics

MM54C374/MM74C374 $T_A = 25°C$, $C_L = 50\,pF$, $t_r = t_f = 20\,ns$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay, CLOCK to Output	$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		150	300	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		65	130	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		180	360	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		80	160	ns
t_{SET-UP}	Minimum Set-Up Time Data In to CLOCK/$\overline{\text{LATCH ENABLE}}$	$t_{HOLD} = 0\,ns$				
		$V_{CC} = 5.0\,V$		70	140	ns
		$V_{CC} = 10\,V$		35	70	ns
t_{PWH}, t_{PWL}	Minimum CLOCK Pulse Width	$V_{CC} = 5.0\,V$		70	140	ns
		$V_{CC} = 10\,V$		50	100	ns
f_{MAX}	Maximum CLOCK Frequency	$V_{CC} = 5.0\,V$	3.5	7.0		MHz
		$V_{CC} = 10\,V$	5.0	10		MHz
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (from a Logic Level)	$R_L = 10k$, $C_L = 50\,pF$				
		$V_{CC} = 5.0\,V$		105	210	ns
		$V_{CC} = 10\,V$		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (from High Impedance State)	$R_L = 10k$, $C_L = 50\,pF$				
		$V_{CC} = 5.0\,V$		105	210	ns
		$V_{CC} = 10\,V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5.0\,V$, $C_L = 50\,pF$		65	130	ns
		$V_{CC} = 10\,V$, $C_L = 50\,pF$		35	70	ns
		$V_{CC} = 5.0\,V$, $C_L = 150\,pF$		110	220	ns
		$V_{CC} = 10\,V$, $C_L = 150\,pF$		70	140	ns
t_r, t_f	Maximum CLOCK Rise and Fall Time	$V_{CC} = 5.0\,V$	15	>2000		μs
		$V_{CC} = 10\,V$	5.0	>2000		μs
C_{CLK}	Input Capacitance	CLOCK Input (Note 2)		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input (Note 2)		5.0	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		250		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

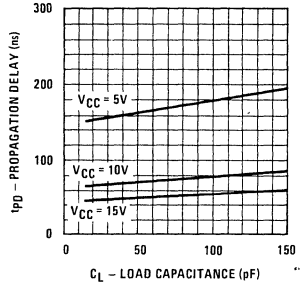
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA max.

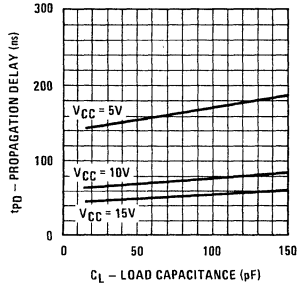
Typical Performance Characteristics $T_A = 25°C$

MM54C373/MM74C373
Propagation Delay, $\overline{\text{LATCH ENABLE}}$ to Output vs Load Capacitance



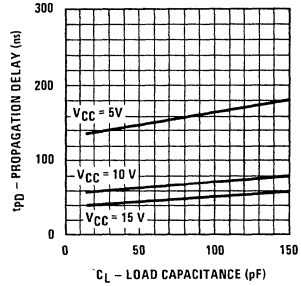
TL/F/5906-3

MM54C373/MM74C373
Propagation Delay, Data In to Output vs Load Capacitance



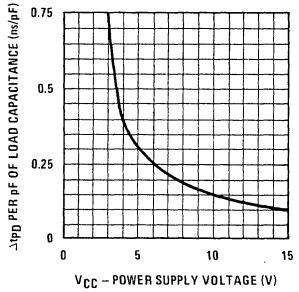
TL/F/5906-4

MM54C374/MM74C374
Propagation Delay, CLOCK to Output vs Load Capacitance



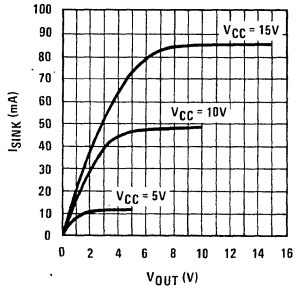
TL/F/5906-5

MM54C373/MM74C373,
MM54C374/MM74C374
Change in Propagation Delay per pF of Load Capacitance ($\Delta t_{PD}/pF$) vs Power Supply Voltage



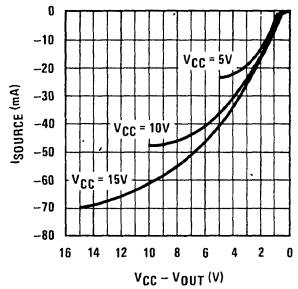
TL/F/5906-6

MM54C373/MM74C373,
MM54C374/MM74C374
Output Sink Current vs V_{OUT}



TL/F/5906-7

MM54C373/MM74C373,
MM54C374/MM74C374 Output Source Current vs $V_{CC} - V_{OUT}$



TL/F/5906-8

Truth Tables

MM54C373/MM74C373

OUTPUT DISABLE	$\overline{\text{LATCH ENABLE}}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Hi-Z

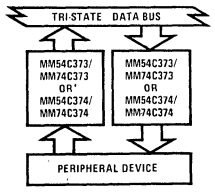
MM54C374/MM74C374

OUTPUT DISABLE	CLOCK	D	Q
L	⌐	H	H
L	⌐	L	L
L	L	X	Q
L	H	X	Q
H	X	X	Hi-Z

L = low logic level
H = high logic level
X = irrelevant
⌐ = low to high logic level transition
Q = preexisting output level
Hi-Z = high impedance output state

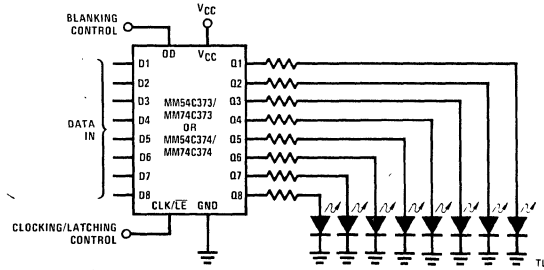
Typical Applications

Data Bus Interfacing Element



TL/F/5906-9

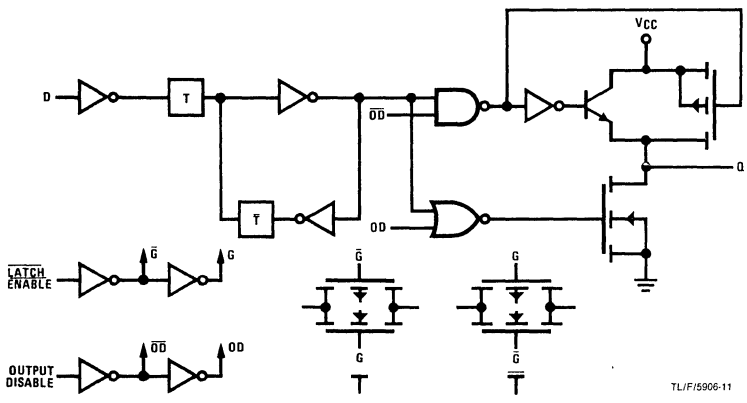
Simple, Latching, Octal, LED Indicator Driver with Blanking For Use As Data Display, Bus Monitor, μP Front Panel Display, Etc.



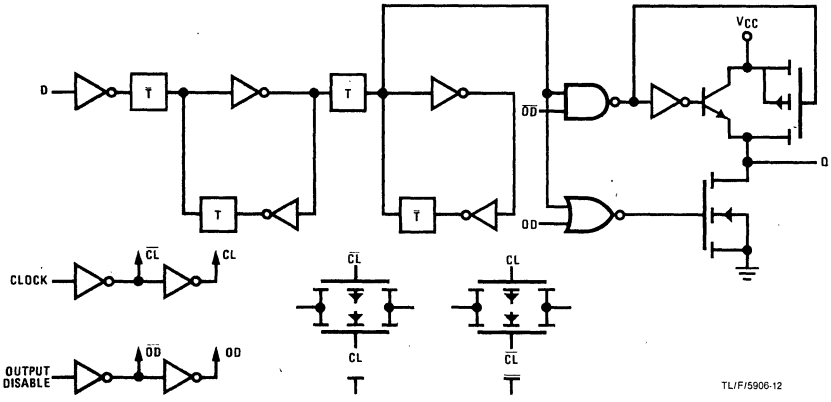
TL/F/5906 10

Logic Diagrams

MM54C373/MM74C373 (1 of 8 Latches)

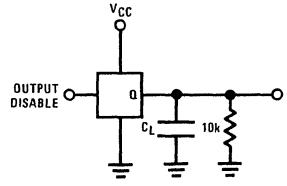


MM54C374/MM74C374 (1 of 8 Flip-Flops)

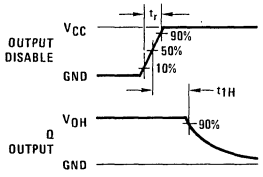


TRI-STATE Test Circuits and Switching Time Waveforms

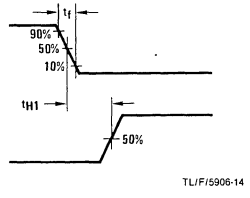
t_{1H}, t_{H1}



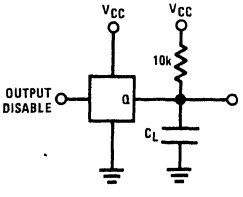
t_{1H}, C_L = 5 pF



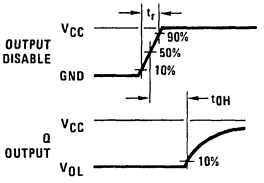
t_{H1}, C_L = 50 pF



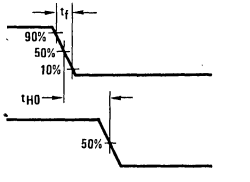
t_{0H}, t_{H0}



t_{0H}, C_L = 5 pF

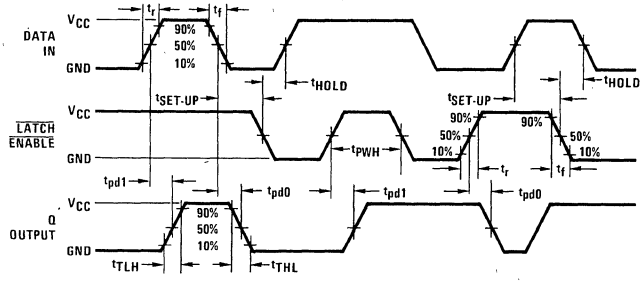


t_{H0}, C_L = 50 pF



Switching Time Waveforms

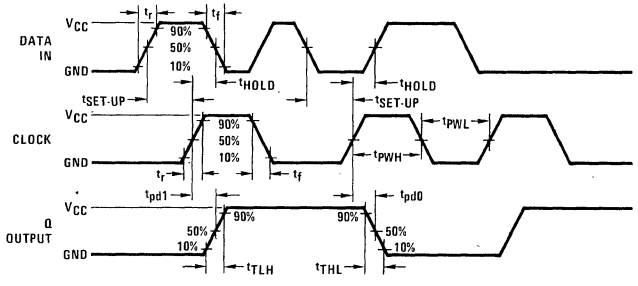
MM54C373/MM74C373



OUTPUT DISABLE = GND

TL/F/5906-17

MM54C374/MM74C374



OUTPUT DISABLE = GND

TL/F/5906-18

National Semiconductor

MM54C901/MM74C901 Hex Inverting TTL Buffer
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer
MM54C903/MM74C903 Hex Inverting CMOS Buffer
MM54C904/MM74C904 Hex Non-Inverting CMOS Buffer

General Description

These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, and high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply. For specific applications see MOS Brief 18 in the back of this catalog.

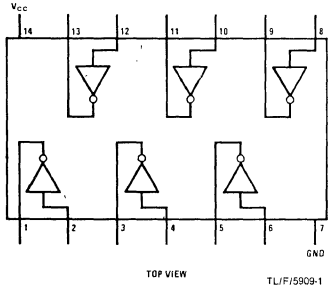
Features

■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatibility	fan out of 2 driving standard TTL

Connection and Logic Diagrams

Dual-In-Line Package

MM54C901/MM74C901
MM54C903/MM74C903

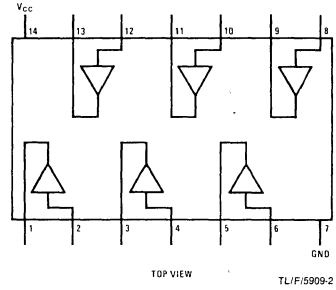


TOP VIEW TL/F/5909-1

Order Number MM54C901J, MM74C901J, MM54C903J, MM74C903J, MM54C901N, MM74C901N, MM54C903N or MM74C903N
See NS Package J14A or N14A

Dual-In-Line Package

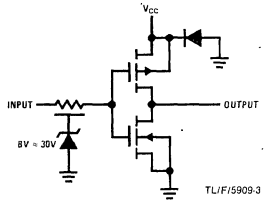
MM54C902/MM74C902
MM54C904/MM74C904



TOP VIEW TL/F/5909-2

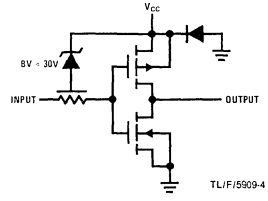
Order Number MM54C902J, MM74C902J, MM54C904J, MM74C904J, MM54C902N, MM74C902N, MM54C904N or MM74C904N
See NS Package J14A or N14A

MM54C901/MM74C901
CMOS to TTL Inverting Buffer



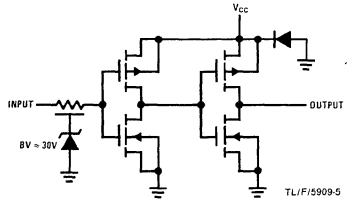
TL/F/5909-3

MM54C903/MM74C903
PMOS to TTL or CMOS Inverting Buffer



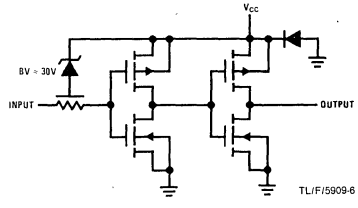
TL/F/5909-4

MM54C902/MM74C902
CMOS to TTL Buffer



TL/F/5909-5

MM54C904/MM74C904
PMOS to TTL or CMOS Buffer



TL/F/5909-6

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Operating Temperature Range	
Voltage at any Input Pin		MM54C901, MM54C902,	
MM54C901/MM74C901	$-0.3\,V$ to $+15\,V$	MM54C903, MM54C904	$-55°C$ to $+125°C$
MM54C902/MM74C902	$-0.3\,V$ to $+15\,V$	MM74C901, MM74C902,	
MM54C903/MM74C903	$V_{CC}-17\,V$ to $V_{CC}+0.3\,V$	MM74C903, MM74C904	$-40°C$ to $+85°C$
MM54C904/MM74C904	$V_{CC}-17\,V$ to $V_{CC}+0.3\,V$	Operating V_{CC} Range	$3.0\,V$ to $15\,V$
Storage Temperature Range	$-65°C$ to $+150°C$	Absolute Maximum V_{CC}	$18\,V$
Package Dissipation	500 mW	Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$, $I_O=-10\,\mu A$ $V_{CC}=10\,V$, $I_O=-10\,\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $V_{CC}=10\,V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	15	μA
TTL to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C $V_{CC}=4.5\,V$ 74C $V_{CC}=4.75\,V$			0.8 0.8	V V
CMOS to TTL						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C901, MM54C903	$V_{CC}=4.5\,V$	4.0			V
	MM54C902, MM54C904	$V_{CC}=4.5\,V$	$V_{CC}-1.5$			V
	MM74C901, MM74C903	$V_{CC}=4.75\,V$	4.25			V
	MM74C902, MM74C904	$V_{CC}=4.75\,V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C901, MM54C903	$V_{CC}=4.5\,V$			1.0	V
	MM54C902, MM54C904	$V_{CC}=4.5\,V$			1.5	V
	MM74C901, MM74C903	$V_{CC}=4.75\,V$			1.0	V
	MM74C902, MM74C904	$V_{CC}=4.75\,V$			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C $V_{CC}=4.5\,V$, $I_O=-800\,\mu A$ 74C $V_{CC}=4.75\,V$, $I_O=-800\,\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage					
	MM54C901, MM54C903	$V_{CC}=4.5\,V$, $I_O=2.6\,mA$			0.4	V
	MM54C902, MM54C904	$V_{CC}=4.5\,V$, $I_O=3.2\,mA$			0.4	V
	MM74C901, MM74C903	$V_{CC}=4.75\,V$, $I_O=2.6\,mA$			0.4	V
	MM74C902, MM74C904	$V_{CC}=4.75\,V$, $I_O=3.2\,mA$			0.4	V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current) (MM54C901/MM74C901, MM54C903/MM74C903)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=0\,V$ $T_A=25°C$, $V_{IN}=0\,V$	−5.0			mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10\,V$, $V_{OUT}=0\,V$ $T_A=25°C$, $V_{IN}=0\,V$	−20			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=V_{CC}$ $T_A=25°C$, $V_{IN}=V_{CC}$	9.0			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0\,V$, $V_{OUT}=0.4\,V$ $T_A=25°C$, $V_{IN}=V_{CC}$	3.8			mA

DC Electrical Characteristics (cont'd) Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Output Drive (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current) (MM54C902/MM74C902, MM54C902/MM74C902)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 5.0\,V$, $V_{OUT} = 0\,V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	−5.0			mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC} = 10\,V$, $V_{OUT} = 0\,V$ $T_A = 25°C$, $V_{IN} = V_{CC}$	−20			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0\,V$, $V_{OUT} = V_{CC}$ $T_A = 25°C$, $V_{IN} = 0\,V$	9.0			mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC} = 5.0\,V$, $V_{OUT} = 0.4\,V$ $T_A = 25°C$, $V_{IN} = 0\,V$	3.8			mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MM54C901/MM74C901, MM54C903/MM74C903						
t_{pd1}	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		38 22	70 30	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		21 13	35 20	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		14		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		30		pF
MM54C902/MM74C902, MM54C904/MM74C904						
t_{pd1}	Propagation Delay Time to a Logical "1"	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		57 27	90 40	ns ns
t_{pd0}	Propagation Delay Time to a Logical "0"	$V_{CC} = 5.0\,V$ $V_{CC} = 10\,V$		54 25	90 40	ns ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		50		pF

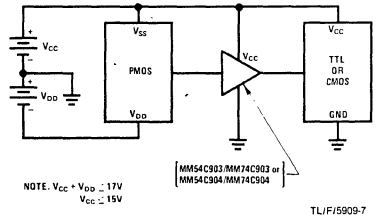
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

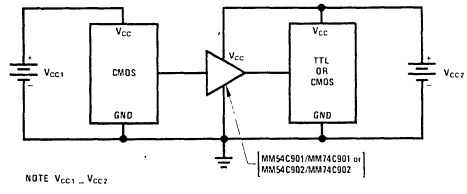
Typical Applications

PMOS to CMOS or TTL Interface



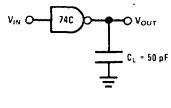
TL/F/5909-7

CMOS to TTL or CMOS at a Lower V_{CC}



TL/F/5909-8

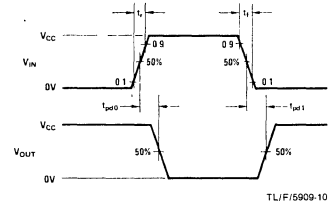
AC Test Circuit and Switching Time Waveforms



Note: Delays measured with input t_r, t_f = 20 ns.

TL/F/5909-9

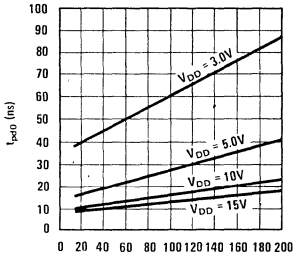
CMOS to CMOS



TL/F/5909-10

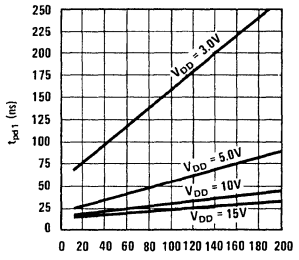
Typical Performance Characteristics

Typical Propagation Delay to a Logical "0" for the MM54C901/ MM74C901 and MM54C903/ MM74C903



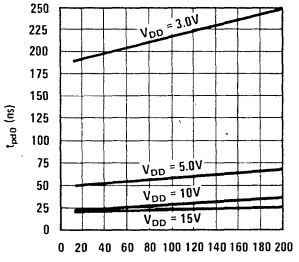
TL/F/5909-11

Typical Propagation Delay to a Logical "1" for the MM54C901/ MM74C901 and MM54C903/ MM74C903



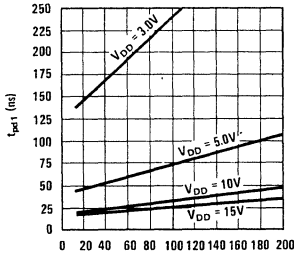
TL/F/5909-12

Typical Propagation Delay to a Logical "0" for the MM54C902/ MM74C902 and MM54C904/ MM74C904



TL/F/5909-13

Typical Propagation Delay to a Logical "1" for the MM54C902/ MM74C902 and MM54C904/ MM74C904



TL/F/5909-14

National Semiconductor

MM54C905/MM74C905 12-Bit Successive Approximation Register

General Description

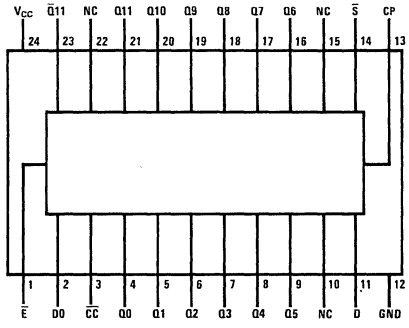
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

Connection Diagram

Dual-In-Line Package



TL/F/5910-1

Order Number MM54C905J or MM74C905J
See NS Package J24A

Order Number MM54C905N or MM74C905N
See NS Package N24A

Truth Table

TIME	INPUTS			OUTPUTS													
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C905	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	16V
MM74C905	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

DC Electrical Characteristics

Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=10\mu A$ $V_{CC}=10V$, $I_O=10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$		0.05	300	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage MM54C905 MM74C905	 $V_{CC}=4.5V$ $V_{CC}=4.75V$	 $V_{CC}-1.5$ $V_{CC}-1.5$			 V V
$V_{IN(0)}$	Logical "0" Input Voltage MM54C905 MM74C905	 $V_{CC}=4.5V$ $V_{CC}=4.75V$			 0.8 0.8	 V V
$V_{OUT(1)}$	Logical "1" Output Voltage MM54C905 MM74C905	 $V_{CC}=4.5V$, $I_O=-360\mu A$ $V_{CC}=4.75V$, $I_O=-360\mu A$	 2.4 2.4			 V V
$V_{OUT(0)}$	Logical "0" Output Voltage MM54C905 MM74C905	 $V_{CC}=4.5V$, $I_O=360\mu A$ $V_{CC}=4.75V$, $I_O=360\mu A$			 0.4 0.4	 V V
Output Drive (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$ $T_A=25°C$	-1.75	-3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$ $T_A=25°C$	-8.0	-15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$ $T_A=25°C$ $V_{CC}=10V\pm5\%$	8.0	16		mA
R_{SOURCE}	Q11-Q0 Outputs	$V_{OUT}=V_{CC}-0.3V$ $T_A=25°C$	150		350	Ω
R_{SINK}	Q11-Q0 Outputs	$V_{CC}=10V\pm5\%$ $V_{OUT}=0.3V$ $T_A=25°C$	80		230	Ω

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time from Clock Input to Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		200 80	350 150	ns ns
t_{pd}	Propagation Delay Time from Clock Input to D0 ($t_{pd(D0)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		180 70	325 125	ns ns
t_{pd}	Propagation Delay Time from Register Enable (E) to Output (Q11) ($t_{pd(E)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		190 75	350 150	ns ns
t_{pd}	Propagation Delay Time from Clock to CC ($t_{pd(CC)}$)	$V_{CC} = 5.0V$ $V_{CC} = 10V$		190 75	350 0.50	ns ns
t_S	Data Input Set-Up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	80 30			ns ns
t_S	Start Input Set-Up Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$	80 30			ns ns
t_W	Minimum Clock Pulse Width	$V_{CC} = 5.0V$ $V_{CC} = 10V$	250 100	125 50		ns ns
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5.0V$ $V_{CC} = 10V$			15 5.0	μs μs
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$ $V_{CC} = 10V$	2.0 5.0	4.0 10		MHz MHz
C_{CK}	Clock Input Capacitance	Clock Input (Note 2)		10		pF
C_{IN}	Input Capacitance	Any other Input (Note 2)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

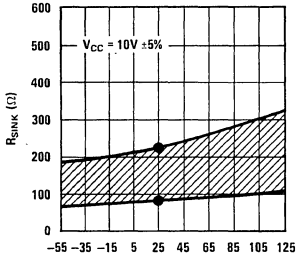
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90.

6

Typical Performance Characteristics

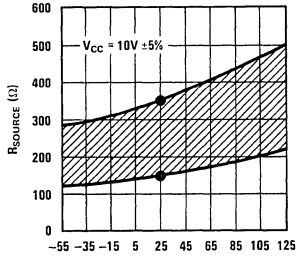
R_{SINK} vs Temperature



● These points are guaranteed by automatic testing.

TL/F/5910-2

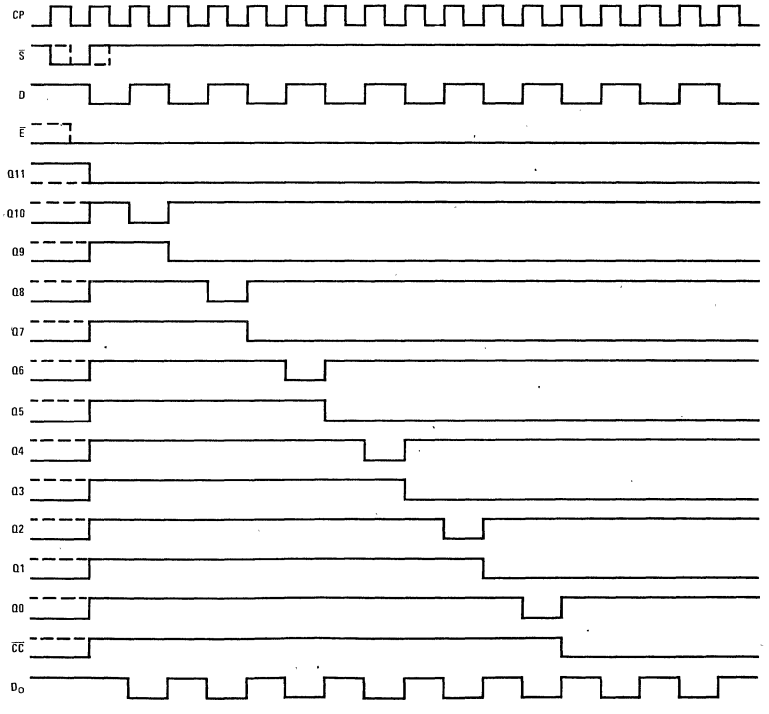
R_{SOURCE} vs Temperature



● These points are guaranteed by automatic testing.

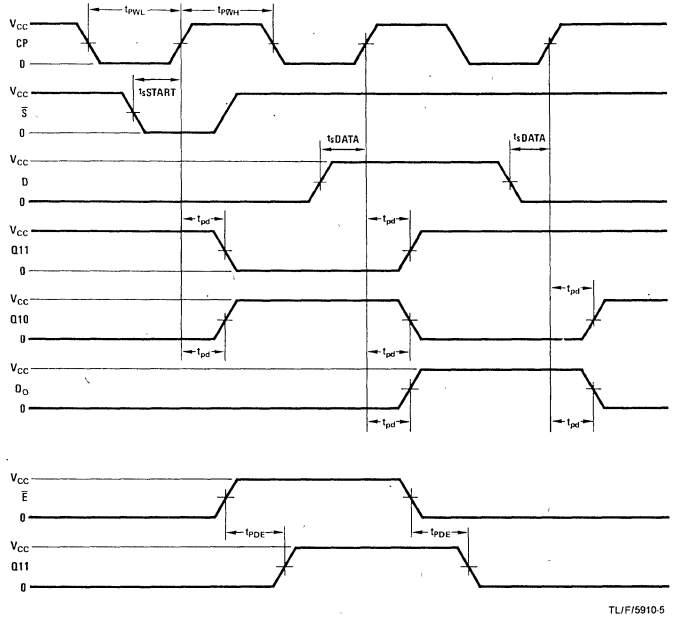
TL/F/5910-3

Timing Diagram



TL/F/5910-4

Switching Time Waveforms



TL/F/5910-5

USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +1/2 LSB and using the complement of the MSB Q11 as the sign bit.

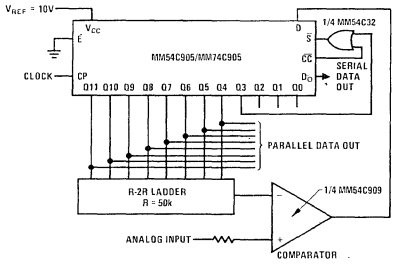
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

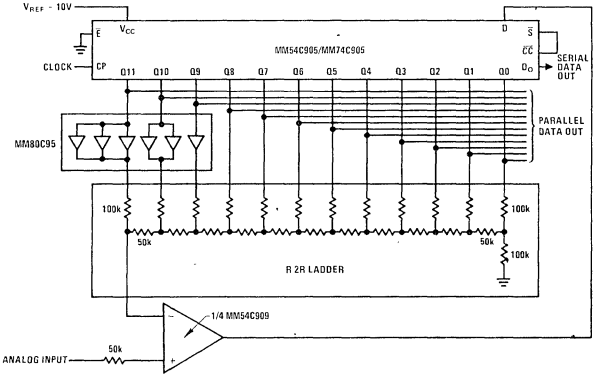
Typical Applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



TL/F/5910 6

12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



TL/F/5910-7

Definition of Terms

CP: Register *clock* input.

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q11}$: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

National Semiconductor

MM54C906/MM74C906 Hex Open Drain N-Channel Buffers
MM54C907/MM74C907 Hex Open Drain P-Channel Buffers

General Description

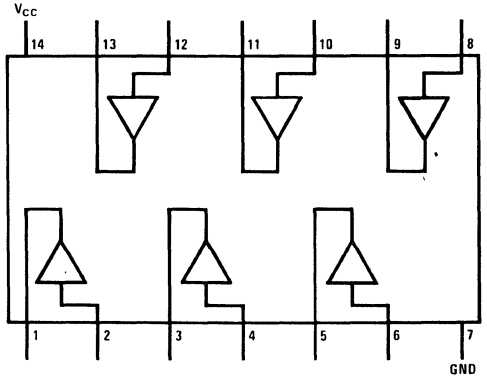
These buffers employ monolithic CMOS technology in achieving open drain outputs. The MM54C906/MM74C906 consists of six inverters driving six N-channel devices; and the MM54C907/MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

Features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} (typ.)
- High current sourcing and sinking open drain outputs

Connection and Logic Diagrams

Dual-In-Line Package

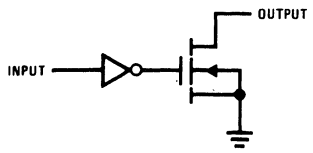


TOP VIEW TL/F/5911-1

Order Number MM54C906J, MM74C906J, MM54C907J or MM74C907J
See NS Package J14A

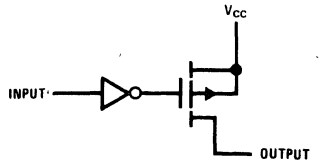
Order Number MM54C906N, MM74C906N, MM54C907N or MM74C907N
See NS Package N14A

MM54C906/MM74C906



TL/F/5911-2

MM54C907/MM74C907



TL/F/5911-3

Absolute Maximum Ratings (Note 1)

Voltage at Any Input Pin	$-0.3V$ to $V_{CC}+0.3V$
Voltage at any Output Pin	
MM54C906/MM74C906	$-0.3V$ to $+18V$
MM54C907/MM74C907	$V_{CC}-18$ to $V_{CC}+0.3V$
Operating Temperature Range	
MM54C906/MM54C907	$-55°C$ to $+125°C$
MM74C906/MM74C907	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$, Output Open		0.05	15	μA
	Output Leakage MM54C906	$V_{CC}=4.5V$, $V_{IN}=V_{CC}-1.5$ $V_{CC}=4.5V$, $V_{OUT}=18V$		0.005	5	μA
	MM74C906	$V_{CC}=4.75V$, $V_{IN}=V_{CC}-1.5$ $V_{CC}=4.75V$, $V_{OUT}=18V$		0.005	5	μA
	MM54C907	$V_{CC}=4.5V$, $V_{IN}=1.0V+0.1V_{CC}$ $V_{CC}=4.5V$, $V_{OUT}=V_{CC}-18V$		0.005	5	μA
	MM74C907	$V_{CC}=4.75V$, $V_{IN}=1.0V+0.1V_{CC}$ $V_{CC}=4.75V$, $V_{OUT}=V_{CC}-18V$		0.005	5	μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, $V_{CC}=4.5V$ 74C, $V_{CC}=4.75V$			0.8 0.8	V V
Output Drive Current						
	MM54C906	$V_{CC}=4.5V$, $V_{IN}=1.0V+0.1V_{CC}$ $V_{CC}=4.5V$, $V_{OUT}=0.5V$ $V_{CC}=4.5V$, $V_{OUT}=1.0V$	 2.1 4.2	 8.0 12		 mA mA
	MM74C906	$V_{CC}=4.75V$, $V_{IN}=1.0V+0.1V_{CC}$ $V_{CC}=4.75V$, $V_{OUT}=0.5V$ $V_{CC}=4.75V$, $V_{OUT}=1.0V$	 2.1 4.2	 8.0 12		 mA mA
	MM74C907	$V_{CC}=4.5V$, $V_{IN}=V_{CC}-1.5V$ $V_{CC}=4.5V$, $V_{OUT}=V_{CC}-0.5V$ $V_{CC}=4.5V$, $V_{OUT}=V_{CC}-1.0V$	 −1.05 −2.1	 −1.5 −3.0		 mA mA
	MM74C907	$V_{CC}=4.75V$, $V_{IN}=V_{CC}-1.5V$ $V_{CC}=4.75V$, $V_{OUT}=V_{CC}-0.5V$ $V_{CC}=4.75V$, $V_{OUT}=V_{CC}-1.0V$	 −1.05 −2.1	 −1.5 −3.0		 mA mA
	MM54C906/MM74C906	$V_{CC}=10V$, $V_{IN}=2.0V$ $V_{CC}=10V$, $V_{OUT}=0.5V$ $V_{CC}=10V$, $V_{OUT}=1.0V$	 4.2 8.4	 −20 −30		 mA mA
	MM54C907/MM74C907	$V_{CC}=10V$, $V_{IN}=8.0V$ $V_{CC}=10V$, $V_{OUT}=9.5V$ $V_{CC}=10V$, $V_{OUT}=9.0V$	 −2.1 −4.2	 −4.0 −8.0		 mA mA

6

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to a Logical "0"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$, $R = 10k$			150	ns
		$V_{CC} = 10V$, $R = 10k$			75	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$, (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$, (Note 4)			75 + 0.7 RC	ns
t_{pd}	Propagation Delay Time to a Logical "1"					
	MM54C906/MM74C906	$V_{CC} = 5.0V$, (Note 4)			150 + 0.7 RC	ns
		$V_{CC} = 10V$, (Note 4)			75 + 0.7 RC	ns
	MM54C907/MM74C907	$V_{CC} = 5.0V$, $R = 10k$			150	ns
		$V_{CC} = 10V$, $R = 10k$			75	ns
C_{IN}	Input Capacity	(Note 2)		5.0		pF
C_{OUT}	Output Capacity	(Note 2)		20		pF
C_{PD}	Power Dissipation Capacity	(Note 3) Per Buffer		30		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

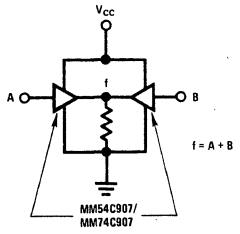
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90. (Assumes outputs are open.)

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capactiy (C_{OUT}).

Typical Applications

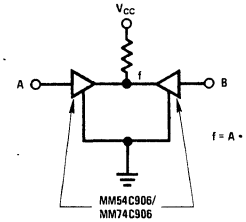
Wire OR Gate



Note: Can be extended to more than 2 inputs.

TL/F/5911-4

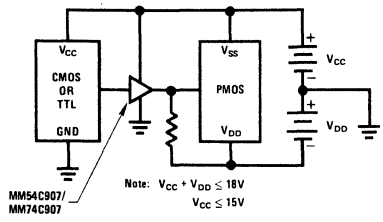
Wire AND Gate



Note: Can be extended to more than 2 inputs.

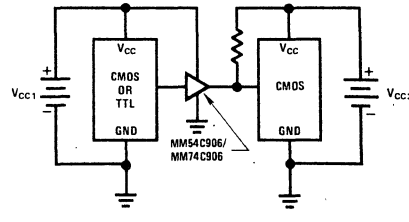
TL/F/5911-5

CMOS or TTL to PMOS Interface



TL/F/5911-6

CMOS or TTL to CMOS at a Higher V_{CC}



TL/F/5911-7

National Semiconductor

MM54C909/MM74C909 Quad Comparator

General Description

The MM54C909/MM74C909 contains four independent bipolar voltage comparators designed to operate from standard 54C/74C power supplies. The output allows current sinking only, thus the wire OR function is possible using a common resistor pull-up.

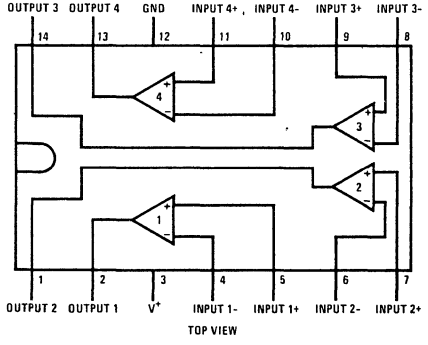
Not only does the MM54C909/MM74C909 function as a comparator for analog inputs, but also has many applications as a voltage translator and buffer when interfacing the 54C/74C family to other logic systems.

Features

■ Wide supply voltage range	3.0 V to 15 V
■ TTL compatibility	fan out of 1 driving 74
■ Low power consumption	$I_{CC} = 800\,\mu A$ (typ.) at $V_{CC} = 5.0\,V_{DC}$
■ Low input bias current	250 nA max.
■ Low input offset current	±50 nA max.
■ Low input offset voltage	±5.0 mV max.
■ Large common mode input voltage range	0 V to $V_{CC} - 1.5$ V
■ Large differential input voltage range	V_{CC}

Connection Diagram

Dual-In-Line Package



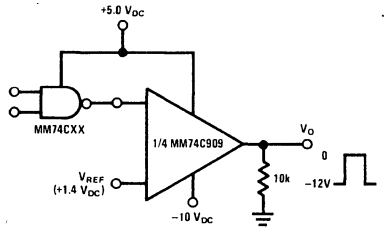
TL/F/5913-1

Order Number MM54C909J or MM74C909J
See NS Package J14A

Order Number MM54C909N or MM74C909N
See NS Package N14A

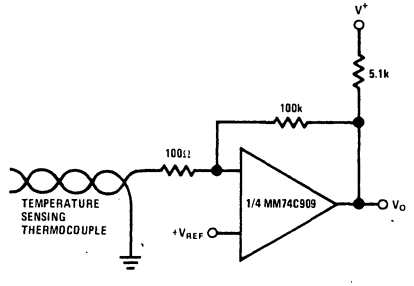
Typical Applications ($V^+ = 5.0\,V_{DC}$)

CMOS/TTL to MOS Logic Converter



TL/F/5913-2

Ground Referenced Thermoucouple in Single Supply System



TL/F/5913-3

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Package Dissipation (Notes 2 and 3)	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C909	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C909	−40°C to +85°C	Input Current (V_{IN} < −0.3V) (Note 4)	50 mA
Storage Temperature Range	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Min/max limits apply across temperature range, unless otherwise noted. (V_{CC} = +5.0 V_{DC})

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 9)				±9	mV
	T_A = 25°C		±2	±5	mV
Input Bias Current ($I_{IN(+)}$ or $I_{IN(-)}$) (Note 5)	T_A = 25°C, With Output in Linear Range		25	250	nA
				400	nA
Input Offset Current ($I_{IN(+)} - I_{IN(-)}$)				±150	nA
	T_A = 25°C		±5	±50	nA
Input Common Mode Voltage (Note 6)		0		V_{CC}−2	V
	T_A = 25°C	0		V_{CC}−1.5	V
Supply Current (I_{CC})	T_A = 25°C, R_L = ∞ On All Outputs		800	2000	μA
Voltage Gain	T_A = 25°C, $R_L \geq$ 15 kΩ		200		V/mV
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Sink Current (I_{SINK})					
MM54C909	V_{CC} = 4.50V	1.6	3.2		mA
MM74C909	V_{CC} = 4.75V, V_{OUT} = 0.4V				
	$V_{IN(-)} \geq$ 1.0 V_{DC}				
	$V_{IN(+)}$ = 0 V_{DC}				
Output Leakage Current	$V_{IN(+)} \geq$ 1.0 V_{DC}, $V_{IN(-)}$ = 0 V_{DC}, V_{OUT} = 15 V_{DC}			1	μA
	$V_{IN(+)} \geq$ 1.0 V_{DC}, $V_{IN(-)}$ = 0 V_{DC}, V_{OUT} = 5 V_{DC}, T_A = 25°C		0.1		nA
Differential Input Voltage (Note 8)	All V_{IN}'s $\geq$ 0 V_{DC}			15	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: For operating at high temperatures, the MM74C909 must be derated based on +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies to the device soldered in a printed circuit board, operating in a still air ambient. The MM54C909 must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output sink current is within specified limits.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. There is a lateral NPN parasitic transistor action on the IC chip. The transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than −0.3V.

Note 5: The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ − 1.5V, but either or both inputs can go to +15V without damage.

Note 7: The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: The positive excursions of the input can equal V_{CC} supply voltage level, and if the other input voltage remains within the common-mode voltage range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V.

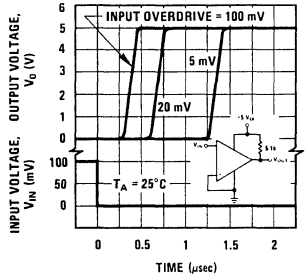
Note 9: At output switch point, V_O = 1.4 V_{DC}, R_S = 0Ω with V^+ from 5 V_{DC} to 30 V_{DC} and over the full input common mode range (0V_{DC}) to V^+ ±1.5 V_{DC}).

AC Electrical Characteristics R_L = 5.1 kΩ, V_{RL} = 5.0 V_{DC}, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Large Signal Response Time	V_{IN} = TTL Swing V_{REF} = 1.4 V_{DC}		300		ns
Response Time	T_A = 25°C (Note 7)		1.3		μs

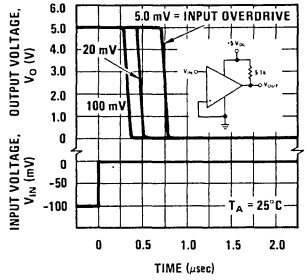
Typical Performance Characteristics

Response Time for Various Input Overdrives — Positive Transition



TL/F/5913-4

Response Time for Various Input Overdrives — Negative Transition



TL/F/5913-5

Application Hints

The MM54C909/MM74C909 is a high gain, wide bandwidth device; which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to <10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the MM54C909/MM74C909 establishes an I_{CC} current which is independent of the magnitude of the power supply voltage over the range of from 3.0V to 15V.

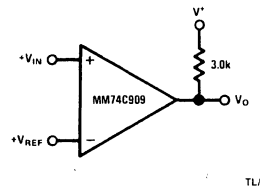
It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode and input resistor can be used as shown in the applications section.

Many outputs can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the MM54C909/MM74C909 package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the gain of the output device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly.

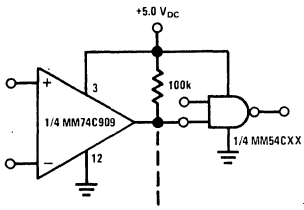
Typical Applications (Continued) (V^+ = 5.0 V_{DC})

Basic Comparator



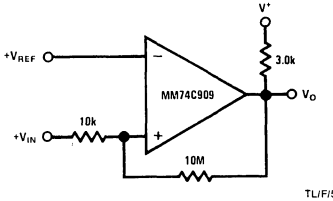
TL/F/5913-6

Driving CMOS



TL/F/5913-7

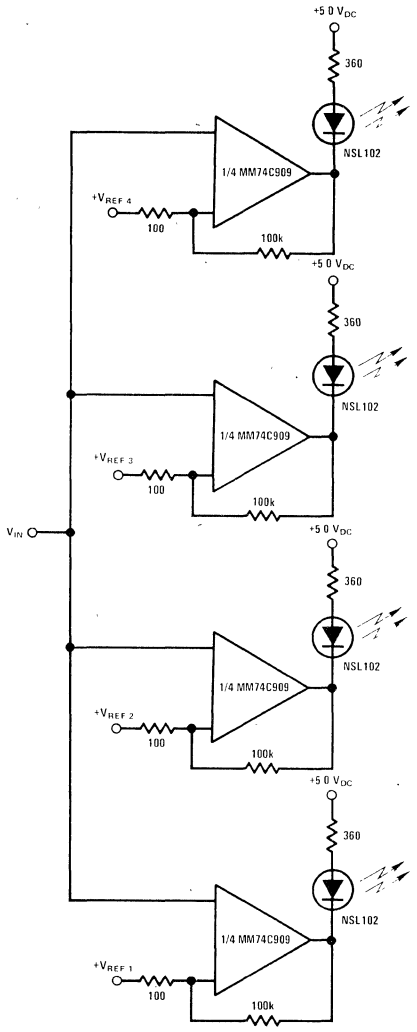
Non-Inverting Comparator with Hysteresis



TL/F/5913-8

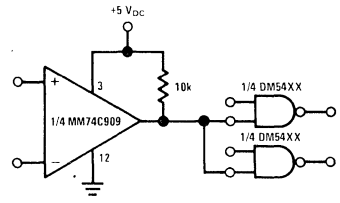
Typical Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

Visible Voltage Indicator



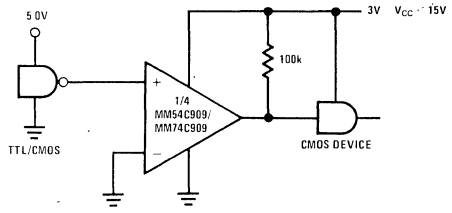
TL/F/5913 9

Driving TTL



TL/F/5913 10

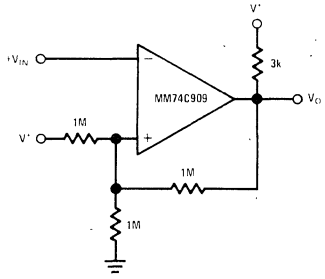
5V Logic to CMOS Operating at $V_{CC} \neq 5V$



Note For inverting buffer reverse input connection.

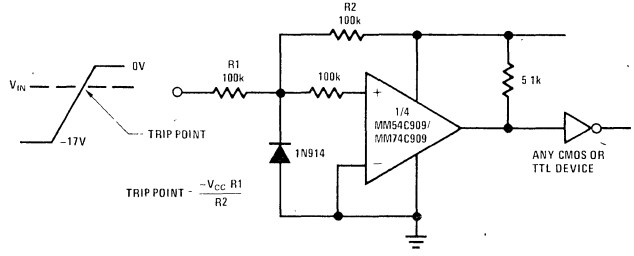
TL/F/5913-11

Inverting Comparator with Hysteresis



TL/F/5913-12

Hi Voltage Inverting PMOS to CMOS or TTL

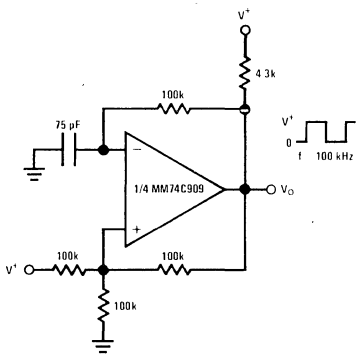


Note For non inverting buffer reverse input connection

TL/F/5913-13

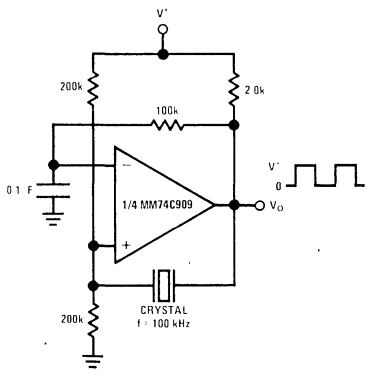
Typical Applications (Continued) ($V^+ = 5.0\ V_{DC}$)

Squarewave Oscillator



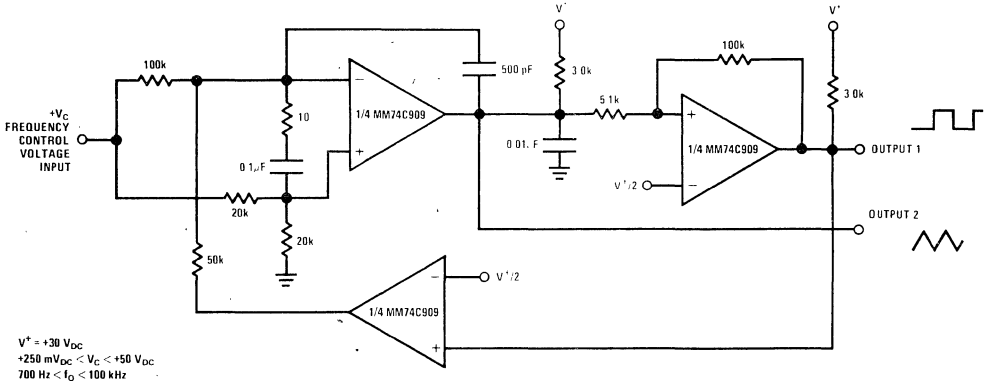
TL/F/5913-14

Crystal Controlled Oscillator



TL/F/5913-15

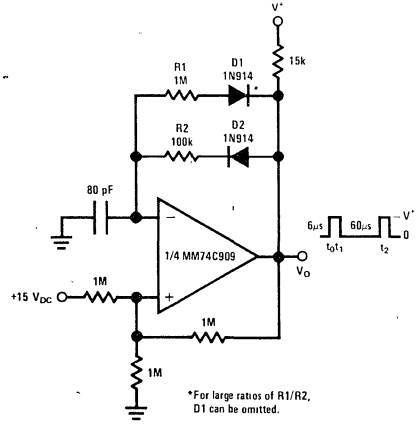
Two-Decade High-Frequency VCO



$V^+ = +30\ V_{DC}$
$+250\ mV_{DC} < V_C < +50\ V_{DC}$
$700\ Hz < f_O < 100\ kHz$

TL/F/5913-16

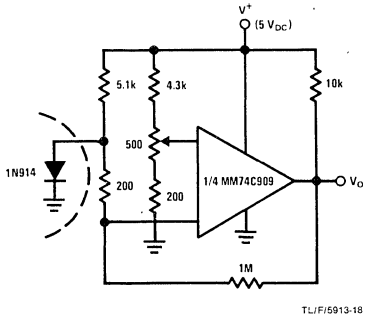
Pulse Generator



*For large ratios of R1/R2, D1 can be omitted.

TL/F/5913-17

Remote Temperature Sensing



TL/F/5913-18

National Semiconductor

MM54C910/MM74C910 256 Bit TRI-STATE® Random Access Read/Write Memory

General Description

The MM54C910/MM74C910 is a 64 word by 4-bit random access memory. Inputs consist of six address lines, four data input lines, a $\overline{WE}$, and a $\overline{ME}$ line. The six address lines are internally decoded to select one of the 64 word locations. An internal address register latches the address information on the positive to negative transition of $\overline{ME}$. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of $\overline{ME}$, and (t_{HA}) after the positive to negative transition of $\overline{ME}$. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if $\overline{WE}$ goes low while $\overline{ME}$ is low. $\overline{WE}$ must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after $\overline{WE}$ returns high.

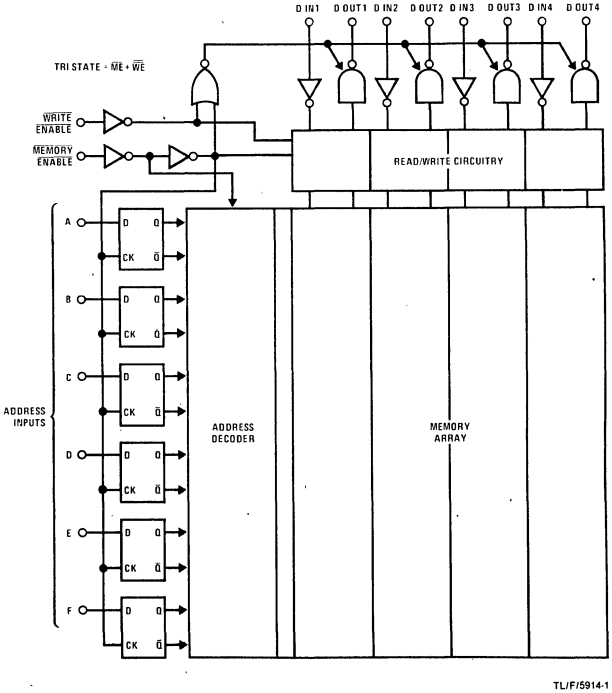
Read Operation: Data is nondestructively read from a memory location by an address operation with $\overline{WE}$ held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

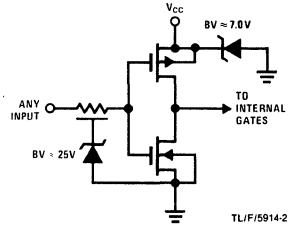
Features

- Supply voltage range — 3.0V to 5.5V
- High noise immunity — 0.45 V_{CC} (typ.)
- TTL compatible fan out — 1 TTL load
- Input address register
- Low power consumption — 250nW/package (typ.) (chip enabled or disabled)
- Fast access time — 250ns (typ.) at 5.0V
- TRI-STATE outputs
- High voltage inputs

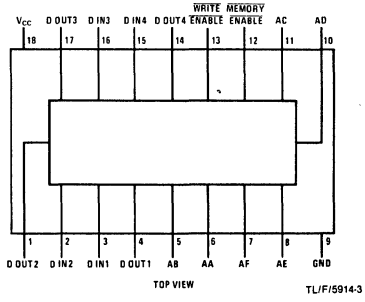
Logic and Connection Diagrams



Input Protection



Dual-In-Line Package



Order Number MM54C910J or MM74C910J
See NS Package J18A

Order Number MM54C910N or MM74C910N
See NS Package N18A

Absolute Maximum Ratings (Note 1)

Voltage at any Output Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$
Voltage at any Input Pin	$-0.3\,V$ to $+15\,V$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0 V to 5.5 V
Standby V_{CC} Range	1.5 V to 5.5 V
Absolute Maximum V_{CC}	6.0 V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C

DC Electrical Characteristics

Min /max limits apply across the temperature and power supply range indicated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN}=15\,V$ $V_{IN}=5.0\,V$		0.005 0.005	2.0 1.0	μA μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN}=0\,V$	−1.0	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=-150\,\mu A$ $I_O=-400\,\mu A$	$V_{CC}-0.5$ 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6\,mA$			0.4	V
I_{OZ}	Output Current in High Impedance State	$V_O=5.0\,V$ $V_O=0\,V$	 −1.0	0.005 −0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC}=5.0\,V$		5.0	300	μA

AC Electrical Characteristics $T_A=25°C$, $V_{CC}=5.0\,V$, $C_L=50\,pF$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{ACC}	Access Time from Address			250	500	ns
t_{pd}	Propagation Delay from $\overline{ME}$			180	360	ns
t_{SA}	Address Input Set-Up Time		140	70		ns
t_{HA}	Address Input Hold Time		20	10		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width		200	100		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width		400	200		ns
t_{SD}	Data Input Set-Up Time		0			ns
t_{HD}	Data Input Hold Time		30	15		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width		140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)			100	200	ns
Capacitance						
C_{IN}	Input Capacity Any Input (Note 2)			5.0		pF
C_{OUT}	Output Capacity Any Output (Note 2)			9.0		pF
C_{PD}	Power Dissipation Capacity (Note 3)			350		pF

AC Electrical Characteristics (cont'd) $T_A = 25°C$, $V_{CC} = 5.0V$, $C_L = 50pF$

Symbol	Parameter	MM54C910 $T_A = -55°C$ to $+125°C$ $V_{CC} = 4.5V$ to $5.5V$		MM74C910 $T_A = -40°C$ to $+85°C$ $V_{CC} = 4.75V$ to $5.25V$		Units
		Min	Max	Min	Max	
t_{ACC}	Access Time from Address		860		700	ns
t_{pd1}, t_{pd0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

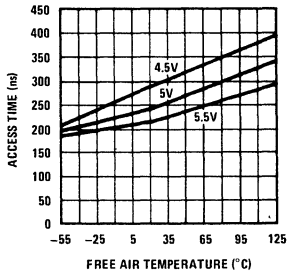
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

Note 4: See AC test circuits for t_{1H}, t_{0H}.

Typical Performance Characteristics

Typical Access Time vs Ambient Temperature



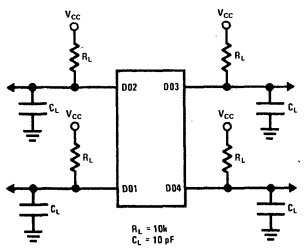
TL/F/5914-4

Truth Table

$\overline{ME}$	$\overline{WE}$	OPERATION	OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

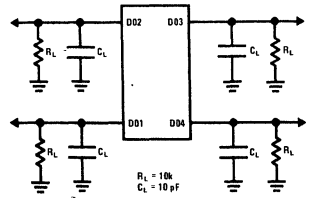
AC Test Circuits

t_{0H}



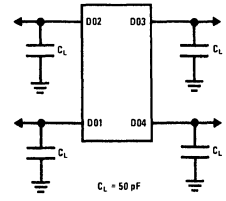
TL/F/5914-5

t_{1H}



TL/F/5914-6

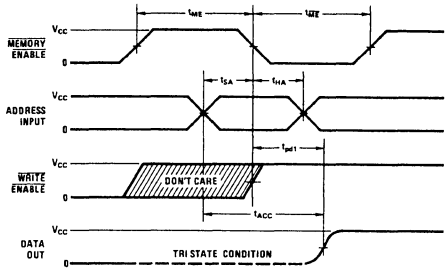
All Other AC Tests



TL/F/5914-7

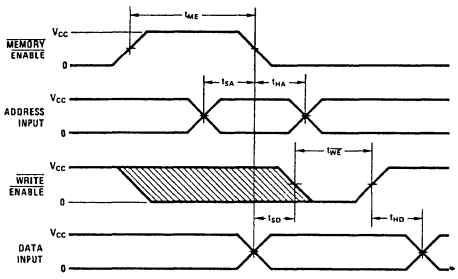
Switching Time Waveforms

Read Cycle
(See Note 1)



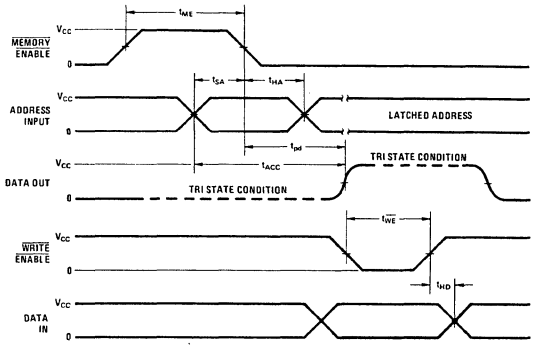
TL/F/5914-8

Write Cycle
(See Note 1)



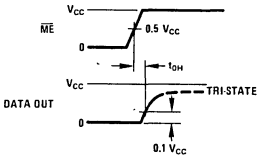
TL/F/5914-9

Read Modify Write Cycle
(See Note 1)

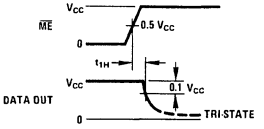


TL/F/5914-10

t_{0H}



t_{1H}



TL/F/5914-11

Note 1: MEMORY ENABLE must be brought high for t_{ME} nanoseconds between every address change.
Note 2: $t_r = t_f = 20$ ns for all inputs.

National Semiconductor

MM54C914/MM74C914 Hex Schmitt Trigger with Extended Input Voltage

General Description

The MM54C914/MM74C914 is a monolithic CMOS Hex Schmitt trigger with special input protection scheme. This scheme allows the input voltage levels to exceed V_{CC} or ground by at least 10V (V_{CC} − 25V to GND + 25V), and is valuable for applications involving voltage level shifting or mismatched power supplies.

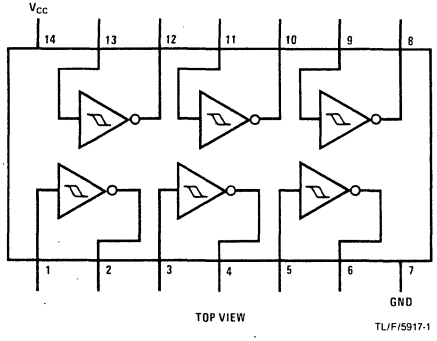
The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{CC} = 10V). And the hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

Features

■ Hysteresis	0.45 V_{CC} (typ.) 0.2 V_{CC} guaranteed
■ Special input protection	Extended Input Voltage Range
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.70 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L

Connection Diagram

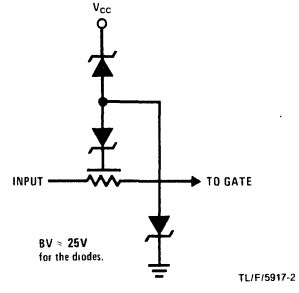
Dual-In-Line Package



Order Number MM54C914J or MM74C914J
See NS Package J14A

Order Number MM54C914N or MM74C914N
See NS Package N14A

Special Input Protection



Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{CC}-25V$ to GND + 25V	Storage Temperature Range	−65°C to +150°C
Voltage at Any Other Pin	−0.3V to V_{CC} + 0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C914	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C914	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
V_{T+}	Positive Going Threshold Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$ $V_{CC}=15V$	3.0 6.0 9.0	3.6 6.8 10	4.3 8.6 12.9	V V
V_{T-}	Negative Going Threshold Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$ $V_{CC}=15V$	0.7 1.4 2.1	1.4 3.2 5.0	2.0 4.0 6.0	V V
$V_{T+}-V_{T-}$	Hysteresis	$V_{CC}=5.0V$ $V_{CC}=10V$ $V_{CC}=15V$	1.0 2.0 3.0	2.2 3.6 5.0	3.6 7.2 10.8	V V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0V$, $I_O=-10\mu A$ $V_{CC}=10V$, $I_O=-10\mu A$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0V$, $I_O=+10\mu A$ $V_{CC}=10V$, $I_O=+10\mu A$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=25V$		0.005	5.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=-10V$	−100	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$, $V_{IN}=-10V/25V$ $V_{CC}=5.0V$, $V_{IN}=-2.5V$ (Note 4) $V_{CC}=10V$, $V_{IN}=5.0V$ (Note 4) $V_{CC}=15V$, $V_{IN}=7.5V$ (Note 4)		0.05 20 200 600	300	μA μA μA μA
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$	4.3			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$			0.7	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=-360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=-360\mu A$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, $V_{CC}=4.5V$, $I_O=360\mu A$ 74C, $V_{CC}=4.75V$, $I_O=360\mu A$			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=5.0V$, $V_{OUT}=0V$, $T_A=25°C$	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	$V_{CC}=10V$, $V_{OUT}=0V$, $T_A=25°C$	−8.0	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=5.0V$, $V_{OUT}=V_{CC}$ $T_A=25°C$	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	$V_{CC}=10V$, $V_{OUT}=V_{CC}$, $T_A=25°C$	8.0	16		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
C_{pd}	Propagation Delay from Input to Output	$V_{CC} = 5.0V$		220	400	ns
		$V_{CC} = 10V$		80	200	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{PD}	Power Dissipation Capacitance	(Note 3) Per Gate		20		pF

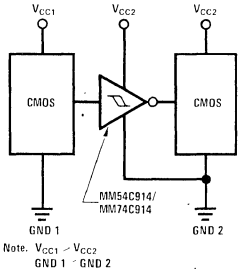
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

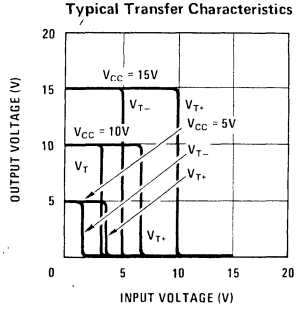
Note 4: Only one input is at 1/2 V_{CC}, the others are either at V_{CC} or GND.

Typical Application

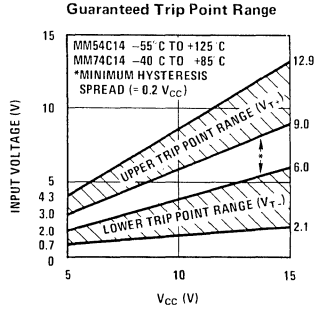


TL/F/5917-3

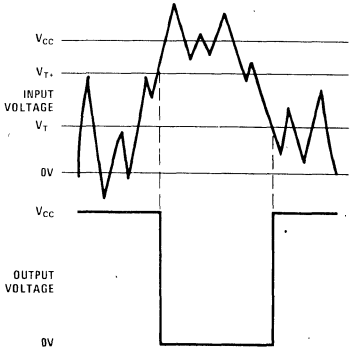
Typical Performance Characteristics



TL/F/5917-4



TL/F/5917-5



TL/F/5917-6

National Semiconductor

MM54C915/MM74C915 7-Segment-to-BCD Converter

General Description

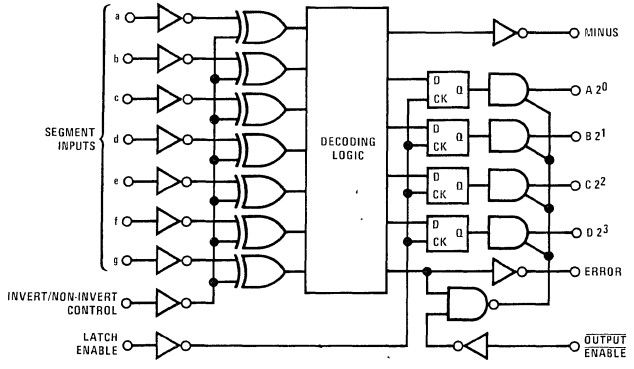
The MM54C915/MM74C915 is a monolithic complementary MOS (CMOS) integrated circuit, constructed with N and P-channel enhancement-mode transistors. This circuit accepts 7-segment information and converts it into BCD information. The true state of the Segment inputs can be selected by use of the Invert/Non-invert control pin. A logical "0" on the Invert/Non-invert control pin selects active high true decoding at the Segment inputs. A logical "1" on the Invert/Non-invert control pin selects active low true decoding at the Segment inputs. In addition to 4 TTL compatible BCD outputs, an Error output and Minus output are available. The Error output goes to an active "1" whenever a non-standard 7-segment code appears at the Segment inputs. The BCD outputs are forced into a TRI-STATE® condition when an error is detected. This allows the user to program his own error code by tying the BCD outputs to V_{CC} or Ground via high value resistors (~ 500k). The BCD outputs may also be forced into TRI-STATE by a logical "1" on output enable ($\overline{OE}$).

The Minus output goes to a logical "1" whenever a minus code is detected and is useful as a microprocessor interrupt. The BCD outputs are in a flow-though condition when Latch Enable (LE) is at a logical "0", and latched when LE is at a logical "1". The inputs will not clamp signals to the positive supply, allowing simple level translation from MOS to TTL.

Features

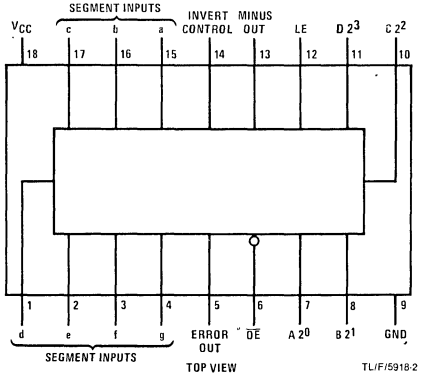
- Wide supply range — 3V–15V
- High noise immunity — 0.45 V_{CC} (typ.)
- TTL compatible fan out — 1 TTL load
- Selectable active true inputs
- TRI-STATE outputs
- On-chip latch
- Error output
- Minus output

Logic and Connection Diagrams



TL/F/5918-1

Dual-In-Line Package



TL/F/5918-2

Order Number MM54C915J or MM74C915J
See NS Package J18A

Order Number MM54C915N or MM74C915N
See NS Package N18A

Absolute Maximum Ratings

Voltage at Any Output	$-0.3V$ to $V_{CC}+0.3V$
Voltage at Any Input	$-0.3V$ to $18V$
Operating Temperature Range	
MM54C915	$-55°C$ to $+125°C$
MM74C915	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	4.0V to 15V
Maximum V_{CC}	18V
Lead Temperature, (Soldering, 10 seconds)	$300°C$

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5V$	3.5			V
		$V_{CC}=10V$	8			V
		$V_{CC}=15V$	12.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5V$			1.5	V
		$V_{CC}=10V$			2	V
		$V_{CC}=15V$			2.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN}=15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN}=0V$	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=10\mu A$				
		$V_{CC}=5V$	4.5			V
		$V_{CC}=10V$	9			V
		$V_{CC}=15V$	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=10\mu A$				
		$V_{CC}=5V$			0.5	V
		$V_{CC}=10V$			1	V
		$V_{CC}=15V$			1.5	V
I_{CC}	Supply Current	$V_{CC}=5V$		0.25	1	mA
		$V_{CC}=10V$		0.75	2.5	mA
		$V_{CC}=15V$		1.00	3	mA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C915	$V_{CC}=4.5V$	$V_{CC}-1.7$			V
	MM74C915	$V_{CC}=4.75V$	$V_{CC}-1.7$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C915	$V_{CC}=4.5V$			0.8	V
	MM74C915	$V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=-360\mu A$				
	MM54C915	$V_{CC}=4.5V$	2.4			V
	MM74C915	$V_{CC}=4.75V$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6$ mA				
	MM54C915	$V_{CC}=4.5V$			0.4	V
	MM74C915	$V_{CC}=4.75V$			0.4	V
OUTPUT DRIVE (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$T_A=25°C$, $V_O=0V$,				
	P-Channel	(Note 2)				
		$V_{CC}=5V$	−1.75	−3.3		mA
		$V_{CC}=10V$	−8	−15		mA
		$V_{CC}=15V$	−15	−25		mA
I_{SINK}	Output Sink Current	$T_A=25°C$, $V_O=V_{CC}$				
	N-Channel	(Note 2)				
		$V_{CC}=5V$	5	8		mA
		$V_{CC}=10V$	20	30		mA
		$V_{CC}=15V$	30	50		mA

AC Electrical Characteristics $T_A = 25°C$

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}, t_{pd1}	Propagation Delay Time to	C_L = 50 pF				
	Logical "0" or a Logical "1"	V_{CC} = 5V		500	1000	ns
		V_{CC} = 10V		300	600	ns
		V_{CC} = 15V		300	600	ns
t_{0H}, t_{1H}	Propagation Delay Time From	R_L = 10k, C_L = 10 pF				
	Logical "0" or Logical "1"	V_{CC} = 5V		110	200	ns
	into High Impedance State	V_{CC} = 10V		75	130	ns
		V_{CC} = 15V		60	110	ns
t_{H0}, t_{H1}	Propagation Delay Time From	R_L = 10k, C_L = 50 pF				
	High Impedance State to a	V_{CC} = 5V		150	250	ns
	Logical "0" or Logical "1"	V_{CC} = 10V		80	140	ns
		V_{CC} = 15V		70	125	ns
t_S	Input Data Set-Up Time	C_L = 50 pF				
		V_{CC} = 5V		500	1000	ns
		V_{CC} = 10V		300	600	ns
		V_{CC} = 15V		300	600	ns
t_H	Input Data Hold Time	C_L = 50 pF				
		V_{CC} = 5V		−150	0	ns
		V_{CC} = 10V		−100	0	ns
		V_{CC} = 15V		−100	0	ns
C_{IN}	Input Capacitance	Any Input, (Note 3)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output, (Note 3)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply to transient operation. It is not meant to imply that the device should be operated at these limits in sustained operation.

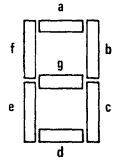
Note 3: Capacitance is guaranteed by periodic testing.

Truth Table

CHARACTER AT SEGMENT INPUTS	BCD OUTPUTS D 2^3	C 2^2	B 2^1	A 2^0	NON-BCD OUTPUTS ERROR	MINUS
0	0	0	0	0	0	0
1	0	0	0	1	0	0
2	0	0	0	1	0	0
3	0	0	1	0	0	0
4	0	0	1	1	0	0
5	0	1	0	0	0	0
6	0	1	0	1	0	0
7	0	1	1	0	0	0
8	0	1	1	0	0	0
9	0	1	1	1	0	0
10	1	0	0	0	0	0
11	1	0	0	1	0	0
12	1	0	0	1	0	0
13	1	1	1	1	0	0
-	X	X	X	X	1	1
All other input	X	X	X	X	1	0
combinations	X	X	X	X	1	0

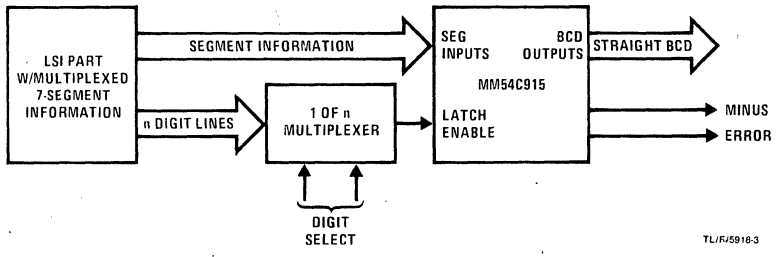
X = represents TRI-STATE condition

SEGMENT IDENTIFICATION



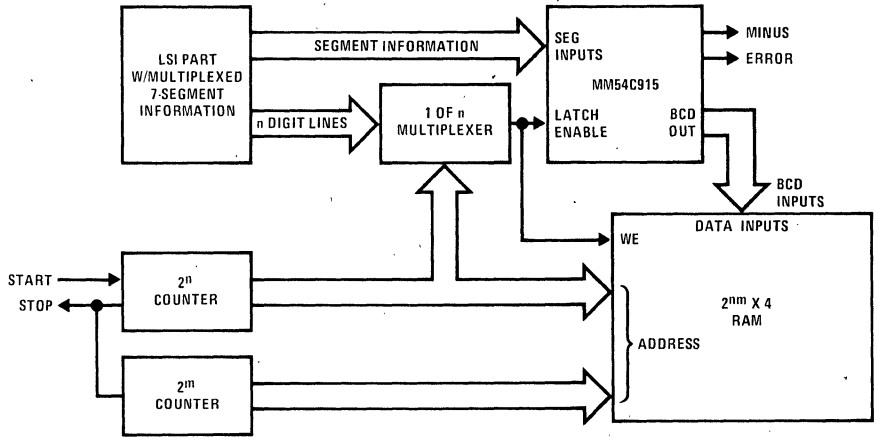
Typical Applications

Multiplex 7-Segment to Straight BCD



TL/F/5918-3

Memory Expansion from 7-Segment Outputs



TL/F/5918-4

National Semiconductor

MM54C922/MM74C922 16-Key Encoder
MM54C923/MM74C923 20-Key Encoder

General Description

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two key roll over is provided between any two switches.

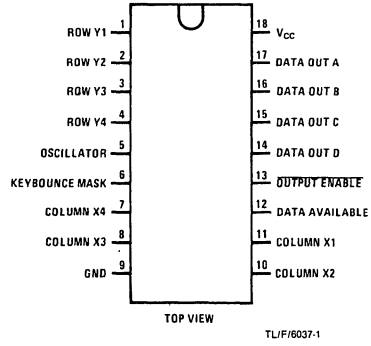
An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

Features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE outputs LPTTL compatible
- Wide supply range 3V to 15V
- Low power consumption

Connection Diagrams

Dual-In-Line Package

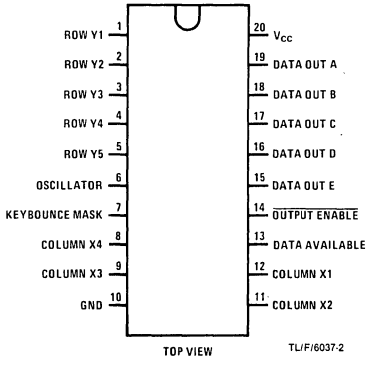


TL/F/6037-1

Order Number MM54C922J or MM74C922J
See NS Package J18A

Order Number MM54C922N or MM74C922N
See NS Package N18A

Dual-In-Line Package



TL/F/6037-2

Order Number MM54C923J or MM74C923J
See NS Package J20A

Order Number MM54C923N or MM74C923N
See NS Package N20A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$V_{CC} - 0.3V$ to $V_{CC} + 0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3V to 15V
MM54C922, MM54C923	−55°C to +125°C	V_{CC}	18V
MM74C922, MM74C923	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/Max limits apply across temperature range unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	3	3.6	4.3	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	6	6.8	8.6	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	9	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	0.7	1.4	2	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	1.4	3.2	4	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	2.1	5	6	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,	3.5	4.5		V
		V_{CC} = 10V,	8	9		V
		V_{CC} = 15V,	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,		0.5	1.5	V
		V_{CC} = 10V,		1	2	V
		V_{CC} = 15V,		1.5	2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		−2	−5	μA
		V_{CC} = 10V		−10	−20	μA
		V_{CC} = 15V		−22	−45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10μA	4.5			V
		V_{CC} = 10V, I_O = −10μA	9			V
		V_{CC} = 15V, I_O = −10μA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10μA			0.5	V
		V_{CC} = 10V, I_O = 10μA			1	V
		V_{CC} = 15V, I_O = 10μA			1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
		V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current Osc at 0V, (one Y low)	V_{CC} = 5V,		0.55	1.1	mA
		V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
		74C, V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V

DC Electrical Characteristics (Cont'd.)

Min/Max limits apply across temperature range unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet) (Short Circuit Current)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

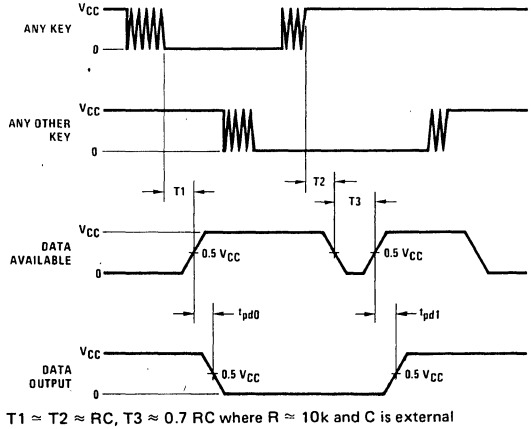
AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0},t_{pd1}	Propagation Delay Time to Logical "0" or Logical "1" from D.A.	C_L = 50 pF, *(Figure 1)*				
		V_{CC} = 5V		60	150	ns
		V_{CC} = 10V		35	80	ns
		V_{CC} = 15V		25	60	ns
t_{0H},t_{1H}	Propagation Delay Time from Logical "0" or Logical "1" into High Impedance State	R_L = 10k, C_L = 10pF *(Figure 2)*				
		V_{CC} = 5V R_L = 10k		80	200	ns
		V_{CC} = 10V C_L = 10 pF		65	150	ns
		V_{CC} = 15V		50	110	ns
t_{H0},t_{H1}	Propagation Delay Time from High Impedance State to a Logical "0" or Logical "1"	R_L = 10k, C_L = 50 pF, *(Figure 2)*				
		V_{CC} = 5V R_L = 10k		100	250	ns
		V_{CC} = 10V C_L = 50 pF		55	125	ns
		V_{CC} = 15V		40	90	ns
C_{IN}	Input Capacitance	Any Input, (Note 2)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output, (Note 2)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

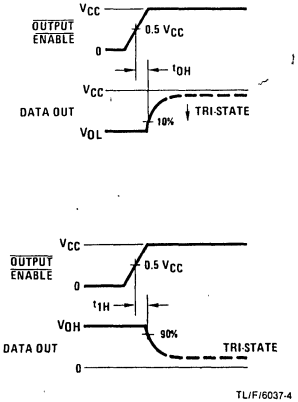
Switching Time Waveforms



$T1 \simeq T2 \approx RC$, $T3 \approx 0.7\,RC$ where $R \simeq 10k$ and C is external capacitor at KBM input.

TL/F/6037-3

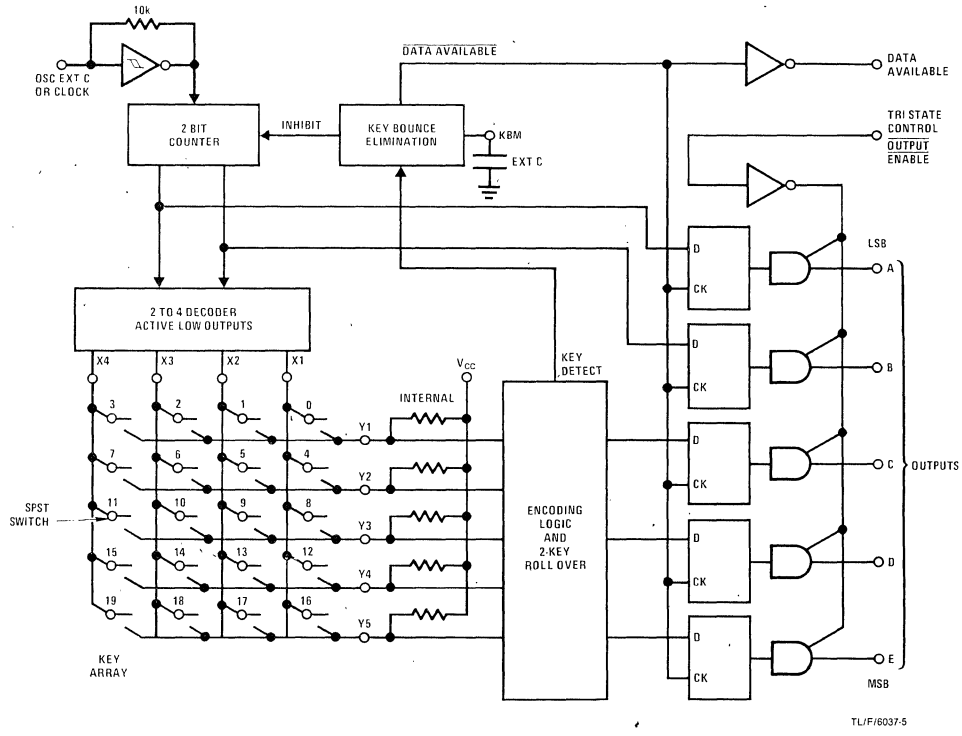
FIGURE 1



TL/F/6037-4

FIGURE 2

Block Diagram



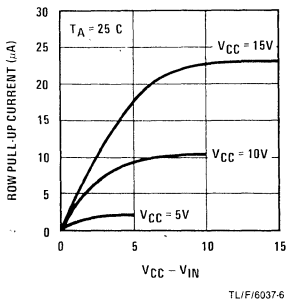
Truth Table

SWITCH POSITION	0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5*,X1	17 Y5*,X2	18 Y5*,X3	19 Y5*,X4
DATA OUT A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
DATA OUT B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
DATA OUT C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
DATA OUT D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
DATA OUT E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

*Omit for MM54C922/MM74C922

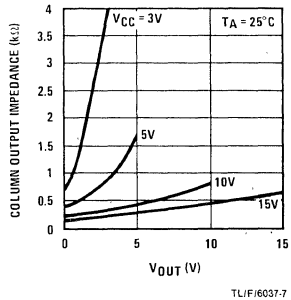
Typical Performance Characteristics

Typical I_{rp} vs V_{IN} at Any Y Input



TL/F/6037-6

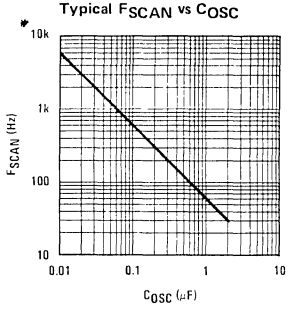
Typical R_{on} vs V_{OUT} at Any X Output



TL/F/6037-7

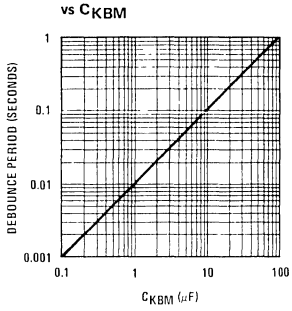
Typical Performance Characteristics (Cont'd.)

Typical F_{SCAN} vs C_{OSC}



TL/F/6037-8

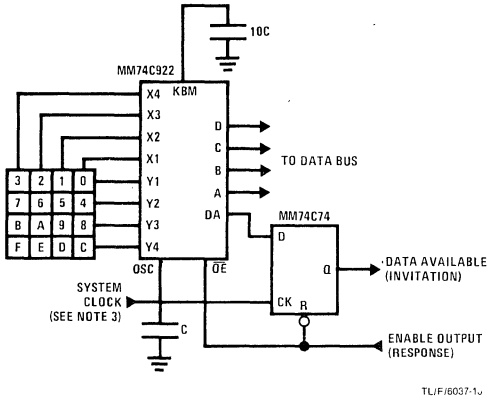
Typical Debounce Period vs C_{KBM}



TL/F/6037-9

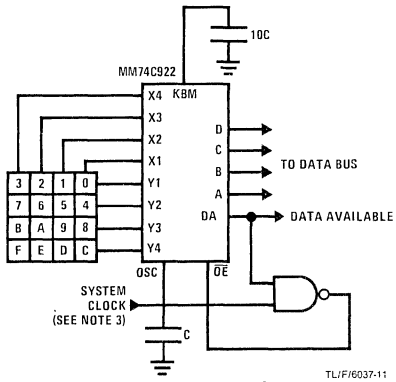
Typical Applications

Synchronous Handshake (MM74C922)



TL/F/6037-10

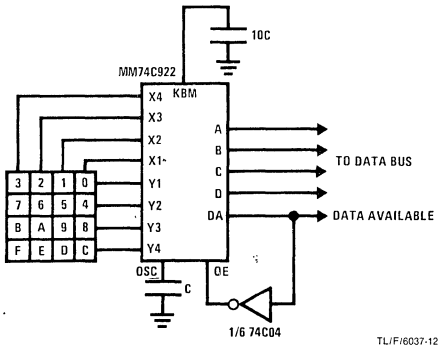
Synchronous Data Entry Onto Bus (MM74C922)



TL/F/6037-11

Outputs are enabled when valid entry is made and go into TRI-STATE when key is released.

Asynchronous Data Entry Onto Bus (MM74C922)



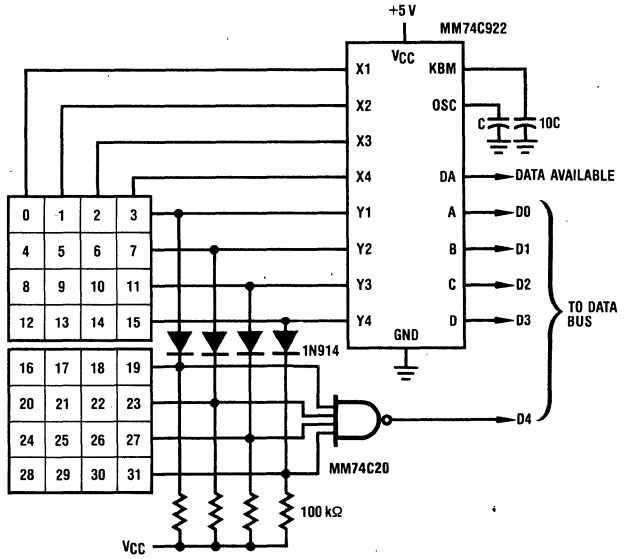
TL/F/6037-12

Outputs are in TRI-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to TRI-STATE.

Note 3: The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

Typical Application (Cont'd.)

Expansion to 32 Key Encoder (MM74C922)



TL/F/6037-13

Theory of Operation

The MM74C922/MM74C923 Keyboard Encoders implement all the logic necessary to interface a 16 or 20 SPST key switch matrix to a digital system. The encoder will convert a key switch closer to a 4(MM74C922) or 5(MM74C923) bit nibble. The designer can control both the keyboard scan rate and the key debounce period by altering the oscillator capacitor, C_{OSE}, and the key bounce mask capacitor, C_{MSK}. Thus, the MM74C922/MM47C923's performance can be optimized for many keyboards.

The keyboard encoders connect to a switch matrix that is 4 rows by 4 columns (MM74C922) or 5 rows by 4 columns (MM74C923). When no keys are depressed, the row inputs are pulled high by internal pull-ups and the column outputs sequentially output a logic "0". These outputs are open drain and are therefore low for 25% of the time and otherwise off. The column scan rate is controlled by the oscillator input, which consists of a Schmitt trigger oscillator, a 2-bit counter, and a 2-4-bit decoder.

When a key is depressed, key 0, for example, nothing will happen when the X1 input is off, since Y1 will remain high. When the X1 column is scanned, X1 goes low and Y1 will go low. This disables the counter and keeps X1 low. Y1 going low also initiates the key bounce circuit timing and locks out the other Y inputs. The key code to be outputted is a combination of the frozen counter value and the decoded Y inputs. Once the key bounce circuit times out, the data is latched, and the Data Available (DAV) output goes high.

If, during the key closure the switch bounces, Y1 input will go high again, restarting the scan and resetting the key bounce circuitry. The key may bounce several times, but as soon as the switch stays low for a debounce period, the closure is assumed valid and the data is latched.

A key may also bounce when it is released. To ensure that the encoder does not recognize this bounce as another key closure, the debounce circuit must time out before another closure is recognized.

The two key roll over feature can be illustrated by assuming a key is depressed, and then a second key is depressed. Since all scanning has stopped, and all other Y inputs are disabled, the second key is not recognized until the first key is lifted and the key bounce circuitry has reset.

The output latches feed TRI-STATE, which are enabled when the Output Enable ($\overline{OE}$) input is taken low.

National Semiconductor

MM54C932/MM74C932 Phase Comparator

General Description

The MM74C932/MM54C932 consists of two independent output phase comparator circuits. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

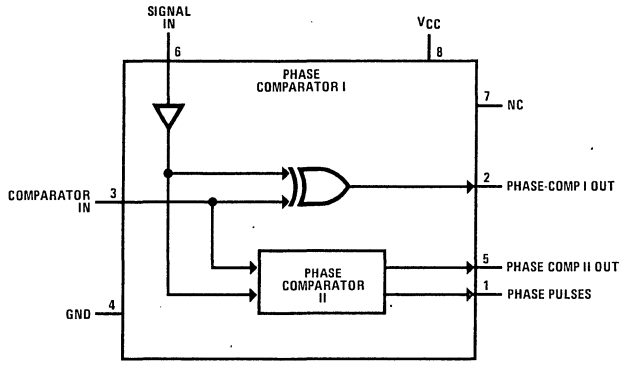
Phase comparator I, an exclusive-OR gate, provides a digital error signal (phase comp. I out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II out) and lock in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

Features

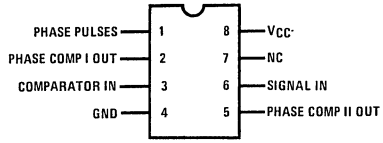
- Wide supply voltage range
- Convenient mini-DIP package
- TRI-STATE® phase-comparator output (comparator II)
- 200 mV input voltage (signal in) sensitivity (typical)

Block and Connection Diagrams



TL/F/5921-1

Dual-In-Line Package



TOP VIEW

TL/F/5921-2

Order Number MM54C932N or MM74C932N
See NS Package N08E

Absolute Maximum Ratings Note 1

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3V to 15V
MM54C932	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C932	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics

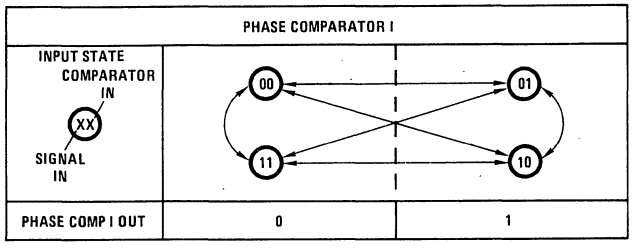
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Quiescent Device Current	PIN 5 = V_{CC}, PIN 8 = V_{CC}, PIN 3 = 0V				
		V_{CC} = 5V		0.005	150	μA
		V_{CC} = 10V		0.01	300	μA
		V_{CC} = 15V		0.015	600	μA
		PIN 6 = Open, PIN 3 = GND				
		V_{CC} = 5V		5	205	μA
		V_{CC} = 10V		20	710	μA
		V_{CC} = 15V		50	1800	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 5V		0	0.05	V
		V_{CC} = 10V		0	0.05	V
		V_{CC} = 15V		0	0.05	V
V_{OH}	High Level Output Voltage	V_{CC} = 5V	4.95	5		V
		V_{CC} = 10V	9.95	10		V
		V_{CC} = 15V	14.95	15		V
V_{IL}	Low Level Input Voltage Comparator and Signal	V_{CC} = 5V, V_O = 0.5V or 4.5V			1.5	V
		V_{CC} = 10V, V_O = 1V or 9V			3.0	V
		V_{CC} = 15V, V_O = 1.5V or 13.5V			4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal	V_{CC} = 5V, V_O = 0.5V or 4.5V	3.5			V
		V_{CC} = 10V, V_O = 1V or 9V	7.0			V
		V_{CC} = 15V, V_O = 1.5V or 13.5V	11.0			V
I_{OL}	Low Level Output Current	V_{CC} = 5V, V_O = 0.4V	0.36	0.88		mA
		V_{CC} = 10V, V_O = 0.5V	0.9	2.25		mA
		V_{CC} = 15V, V_O = 1.5V	2.4	8.8		mA
I_{OH}	High Level Output Current	V_{CC} = 5V, V_O = 4.6V	−0.36	−0.88		mA
		V_{CC} = 10V, V_O = 9.5V	−0.9	−2.25		mA
		V_{CC} = 15V, V_O = 13.5V	−2.4	−8.8		mA
I_{IN}	Input Current	All Inputs Except Signal Input				
		V_{CC} = 15V, V_{IN} = 0V		-10^{-5}	−1.0	μA
		V_{CC} = 15V, V_{IN} = 15V		10^{-5}	1.0	μA
C_{IN}	Input Capacitance	Any Input			7.5	pF
P_D	Total Power Dissipation	f_O = 10 kHz, R1 = 1 MΩ R2 = ∞, VCO_{IN} = V_{CC}/2				
		V_{CC} = 5V		0.07		mW
		V_{CC} = 10V		0.6		mW
		V_{CC} = 15V		2.4		mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

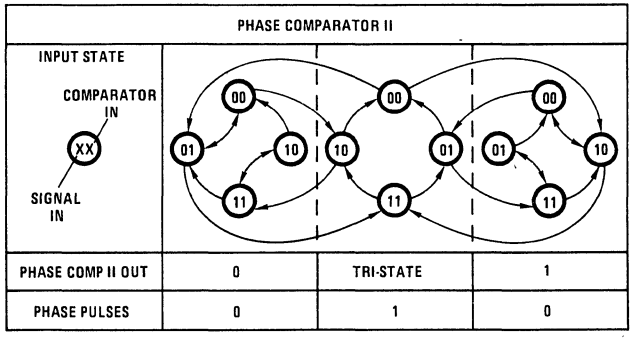
Electrical Characteristics

SYMBOL	Parameter	Conditions	Min	Typ	Max	Units
	Phase Comparators					
R_{IN}	Input Resistance Signal Input	$V_{CC} = 5V$	1.0	3.0		MΩ
		$V_{CC} = 10V$	0.2	0.7		MΩ
		$V_{CC} = 15V$	0.1	0.3		MΩ
	Comparator Input	$V_{CC} = 5V$		10^6		MΩ
		$V_{CC} = 10V$		10^6		MΩ
		$V_{CC} = 15V$		10^6		MΩ
	AC Coupled Signal Input Voltage Sensitivity	$C_{SERIES} = 1000pF$ f = 50kHz				
		$V_{CC} = 5V$		200	400	mV
		$V_{CC} = 10V$		400	800	mV
		$V_{CC} = 15V$		700	1400	mV

Phase Comparator State Diagrams



TL/F/5921-3



TL/F/5921-4

Figure 1

Typical Waveforms

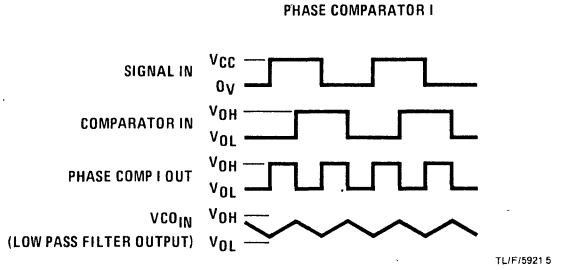


Figure 2. Typical Waveform Employing Phase Comparator I in Locked Condition

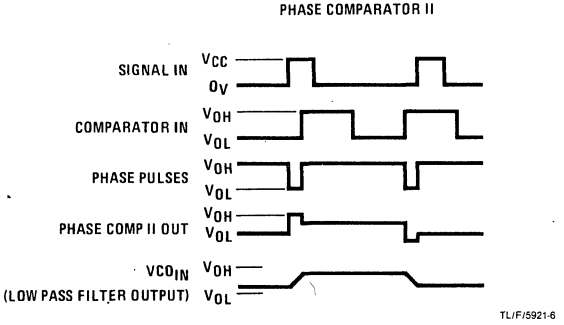
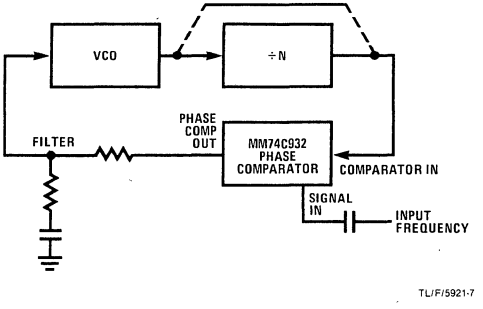


Figure 3. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Phase Locked Loop



National Semiconductor

MM54C941/MM74C941 Octal Buffers/Line Receivers/ Line Drivers with TRI-STATE® Outputs

General Description

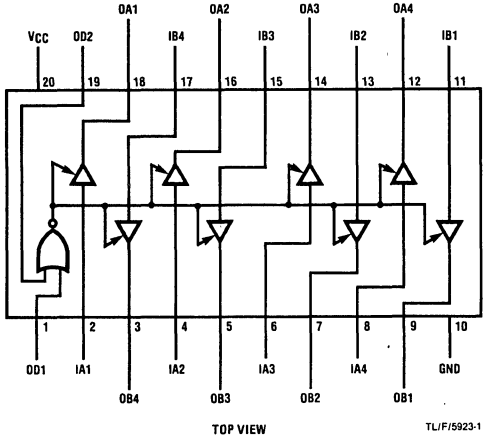
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. When $V_{CC} = 5V$, inputs can accept true TTL high and low logic levels.

Features

- Wide supply voltage range (3V to 15V)
- Low power consumption
- TTL compatibility (Improved on the inputs)
- High capacitive load
- TRI-STATE outputs
- Input protection
- 20-pin dual-in-line package
- High output drive

Connection and Logic Diagrams

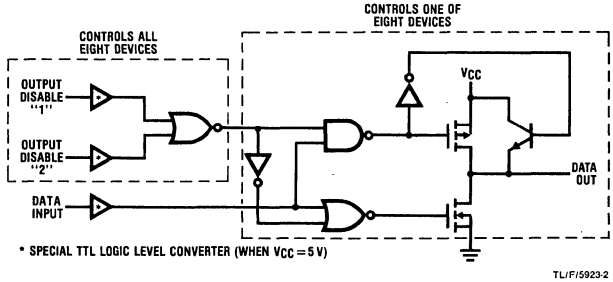
Dual-In-Line Package



TOP VIEW TL/F/5923-1

Order Number MM54C941J or MM74C941J
See NS Package J20A

Order Number MM54C941N or MM74C941N
See NS Package N20A



* SPECIAL TTL LOGIC LEVEL CONVERTER (WHEN $V_{CC} = 5V$)

TL/F/5923-2

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	0.3V to V_{CC} + 0.3V	Package Dissipation	500mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C941	−55°C to +125°C	V_{CC}	18V
MM74C941	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V	2.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V V_{CC} = 10V			0.8 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I8 = +10μA			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
I_{OZ}	TRI-STATE Leakage	V_{CC} = 15V, V_{OUT} = 0V or 15V			±10	μA
CMOS/TTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 2.5 V_{CC} − 2.5			V V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −450μA 74C, V_{CC} = 4.75V, I_O = −450μA 54C, V_{CC} = 4.5V, I_O = −2.2mA 74C, V_{CC} = 4.75V, I_O = −2.2mA	V_{CC} − 0.4 V_{CC} − 0.4 2.4 2.4			V V V V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = +2.2mA 74C, V_{CC} = 4.75V, I_O = +2.2mA			0.4 0.4	V V
Output Drive (See 54C/74C Family Characteristics Data Sheet)						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−14.0	−30.0		mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−36.0	−70.0		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	+12.0	+20.0		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	+48.0	+70.0		mA

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}, t_{pd0}	Propagation Delay (Data IN to OUT)	$V_{CC} = 5.0V$, $C_L = 50pF$		70	140	ns
		$V_{CC} = 10V$, $C_L = 50pF$		35	70	ns
		$V_{CC} = 5.0V$, $C_L = 150pF$		90	160	ns
		$V_{CC} = 10V$, $C_L = 150pF$		45	90	ns
t_{IH}, t_{OH}	Propagation Delay Output Disable to Logic Level (from High Impedance State) (from a Logic Level)	$R_L = 1k\Omega$, $C_L = 50pF$				
		$V_{CC} = 5.0V$		100	200	ns
		$V_{CC} = 210V$		55	110	ns
t_{H1}, t_{H0}	Propagation Delay Output Disable to Logic Level (from High Impedance State)	$R_L = 1k\Omega$, $C_L = 50pF$				
		$V_{CC} = 5.0V$		100	200	ns
		$V_{CC} = 10V$		55	110	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5.0V$, $C_L = 50pF$		50	100	ns
		$V_{CC} = 10V$, $C_L = 50pF$		30	60	ns
		$V_{CC} = 5.0V$, $C_L = 150pF$		80	160	ns
		$V_{CC} = 10V$, $C_L = 150pF$		50	100	ns
C_{PD}	Power Dissipation Capacitance (Output Enabled per Buffer)	(See Note 3)		100		pF
	(Output Disabled per Buffer)			10		pF
C_{IN}	Input Capacitance (Any Input)	(See Note 2) $V_{IN} = 0V$, $f = 1MHz$ $T_A = 25°C$		10		pF
C_O	(Output Capacitance) (Output Disabled)	$V_{IN} = 0v$, $f = 1MHz$, $T_A = 25°C$		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

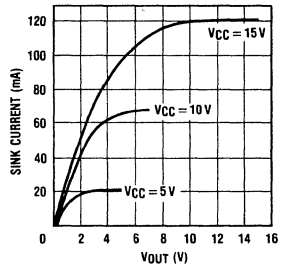
6

Truth Table

OD1	OD2	Input	Output
0	0	0	0
0	0	1	1
0	1	X	Z
1	0	X	Z
1	1	X	Z

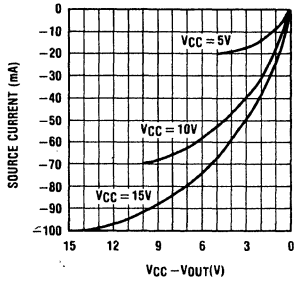
1 = High
0 = Low
X = Don't Care
Z = TRI-STATE

N-Channel Output Drive @ 25°C



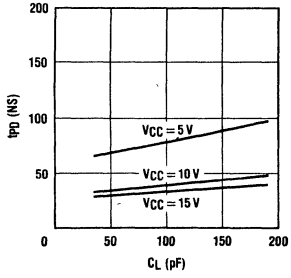
TL/F/5923-3

P-Channel Output Drive @ 25°C



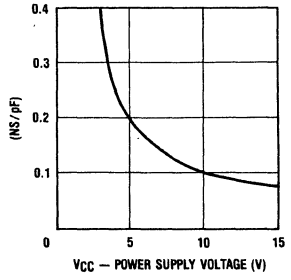
TL/F/5923-4

Propagation Delay vs. Load Capacitance



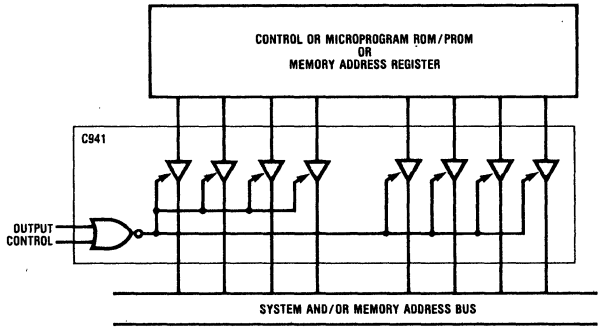
TL/F/5923-5

Δ tPD per pF of Load Capacitance



TL/F/5923-6

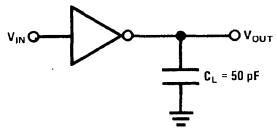
Applications



TL/F/5923-7

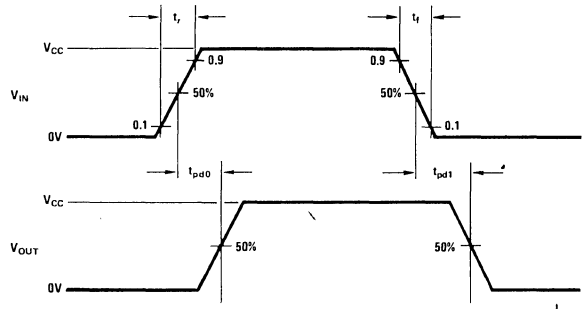
AC Test Circuits and Switching Time Waveforms

t_{pd0}, t_{pd1}



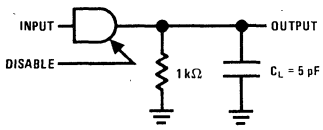
TL/F/5923 8

CMOS to CMOS



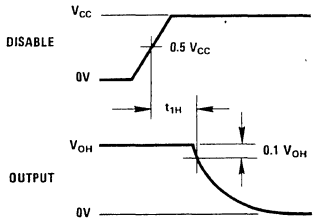
TL/F/5923-9

t_{1H} and t_{H1}

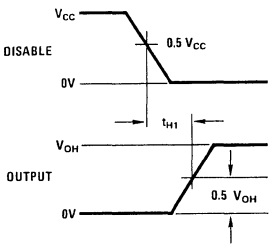


TL/F/5923-10

t_{1H}



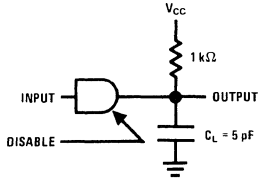
t_{H1}



TL/F/5923-11

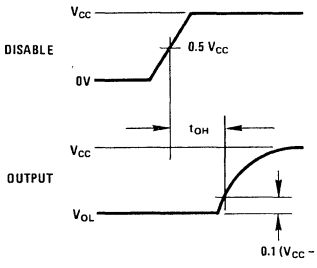
NOTE: V_{OH} IS DEFINED AS THE DC OUTPUT HIGH VOLTAGE WHEN THE DEVICE IS LOADED WITH A 1 kΩ RESISTOR TO GROUND.

t_{0H} and t_{H0}

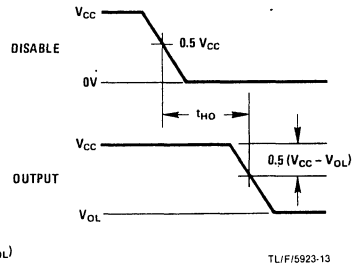


TL/F/5923-12

t_{0H}



t_{H0}



TL/F/5923-13

NOTE: V_{OL} IS DEFINED AS THE DC OUTPUT LOW VOLTAGE WHEN THE DEVICE IS LOADED WITH A 1 kΩ RESISTOR TO V_{CC}.

Note: Delays measured with input t_r, $t_f \leq 20$ ns

National Semiconductor

MM54C989/MM74C989 64-Bit (16 x 4) TRI-STATE® RAM

General Description

The MM54C989/MM74C989 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of 4 address lines, 4 data input lines, a write enable line and a memory enable line. The 4 binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register latches the address information on the positive to negative transition of the memory enable input. The 4 TRI-STATE data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note. The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

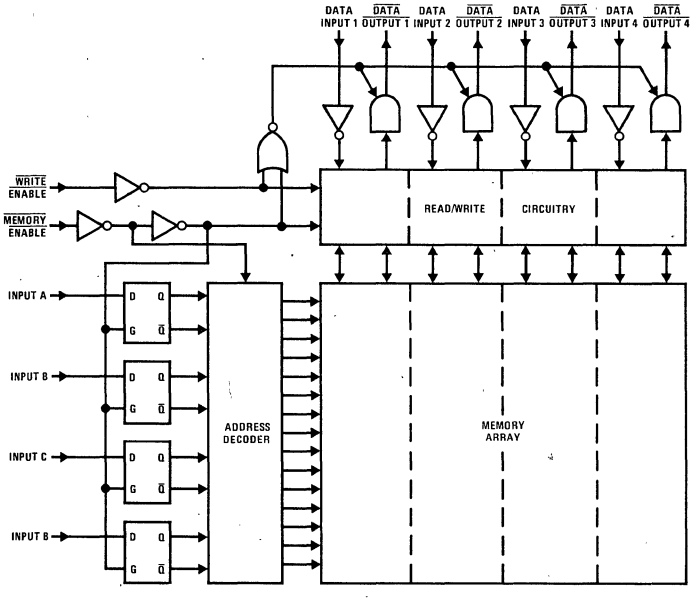
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the 4 outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

When the device is writing or disabled the output assumes a TRI-STATE (Hi-Z) condition.

Features

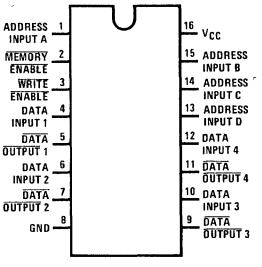
■ Wide supply voltage range	3.0V to 5.5V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ.)
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Input address register	
■ Low power consumption	250 nW/package (typ.) @ V_{CC} = 5V
■ Fast access time	140 ns (typ.) at V_{CC} = 5V
■ TRI-STATE output	

Logic and Connection Diagrams



TL/F/5925-1

Dual-in-Line Package



TOP VIEW

TL/F/5925-2

Order Number
MM54C989J or MM74C989J
See NS Package J16A

Order Number
MM54C989N or MM74C989N
See NS Package N16A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Package Dissipation	500 mW
Absolute Maximum V_{CC}	7.0V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C989	4.7	5.5	V
MM74C989	4.75	5.25	V
Temperature (T_A)			
MM54C989	−55	+125	°C
MM74C989	−40	+85	°C
Operating V_{CC} Range			3.0V to 5.5V
Standby V_{CC} Range			1.5V to 5.5V

DC Electrical Characteristics MM54C989/MM74C989

(Min/max limits apply across the temperature and power supply range indicated).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA I_O = −150 μA	2.4 V_{CC}−0.5			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 360 μA			0.4	V
I_{OZ}	Output Current in High Impedance State	V_O = 5V V_O = 0	 −1	0.005 −0.005	1	μA μA
I_{CC}	Supply Current (Active)	$\overline{ME}$ = 0, V_{CC} = 5V		0.05	150	μA
I_{CC}	Supply Current (Stand-By)	$\overline{ME}$ = 5V			3	μA

AC Electrical Characteristics MM54C989/MM74C989

T_A = 25°C, V_{CC} = 5V, C_L = 50 pF

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{ACC}	Access Time From Address		140	500	ns
t_{PD}	Propagation Delay From $\overline{ME}$		110	360	ns
t_{SA}	Address Input Set-Up Time	140	30		ns
t_{HA}	Address Input Hold Time	20	15		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	200	80		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	100		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	20		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{0H}	Delay to TRI-STATE , C_L = 5 pF, R_L = 10k, (Note 4)		100	200	ns
CAPACITANCE					
C_{IN}	Input Capacity, Any Input, (Note 2)		5		pF
C_{OUT}	Output Capacity, Any Output, (Note 2)		8		pF
C_{PD}	Power Dissipation Capacity, (Note 3)		350		pF

AC Electrical Characteristics (Continued)

MM54C989: $T_A = -55°C$ to $+125°C$, $V_{CC} = 4.5V$ to $5.5V$. $C_L = 50$ pF
MM74C989: $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.75V$ to $5.25V$. $C_L = 50$ pF

SYMBOL	PARAMETER	MM54C989		MM74C989		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time From Address		500		620	ns
t_{PD1}, t_{PD0}	Propagation Delay From $\overline{ME}$		350		430	ns
t_{SA}	Address Input Set-Up Time	150		140		ns
t_{HA}	Address Input Hold Time	50		60		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	250		310		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	520		400		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	60		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	220		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE®, (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

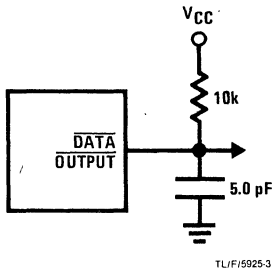
Note 4: See AC test circuit for t_{1H}, t_{0H}.

Truth Table

$\overline{ME}$	$\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

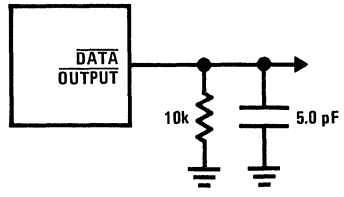
AC Test Circuits

t_{0H}



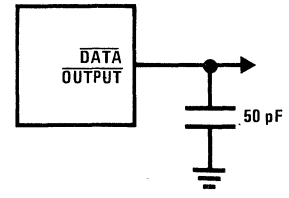
TL/F/5925-3

t_{1H}



TL/F/5925-4

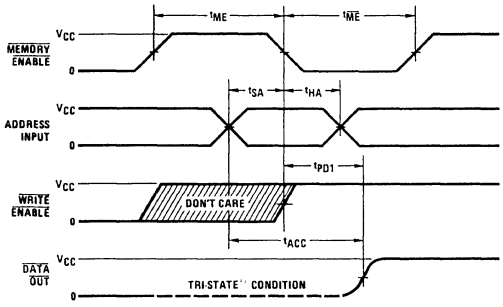
All Other AC Tests



TL/F/5925-5

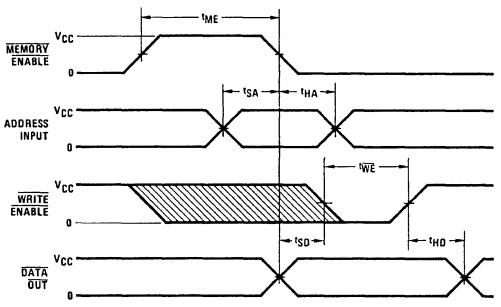
Switching Time Waveforms

Read Cycle (Note 1)



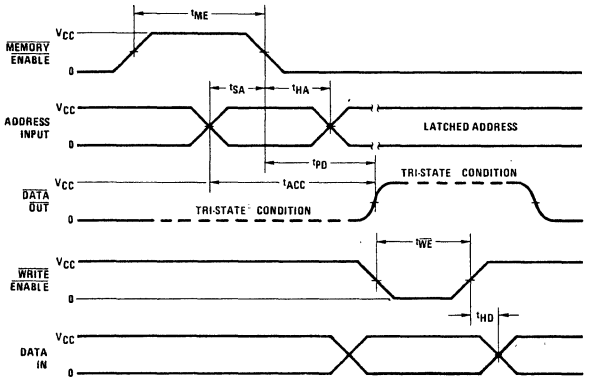
TL/F/5925-6

Write Cycle (Note 1)



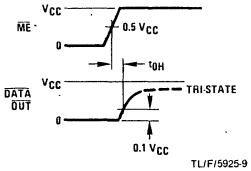
TL/F/5925-7

Read-Modify-Write Cycle (Note 1)



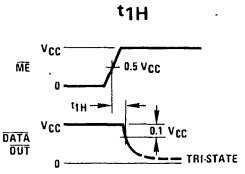
TL/F/5925-8

t_{0H}



TL/F/5925-9

t_{1H}



TL/F/5925-10

Note 1: $\overline{\text{MEMORY ENABLE}}$ must be brought high for t_{ME} ns between every address change.

Note 2: $t_r = t_f = 20$ ns for all inputs.

6

National Semiconductor

MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® Hex Buffers
MM70C96/MM80C96, MM70C98/MM80C98 TRI-STATE Hex Inverters

General Description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. The MM70C95/MM80C95 and the MM70C97/MM80C97 convert CMOS or TTL outputs to TRI-STATE outputs with no logic inversion, the MM70C96/MM80C96 and the MM70C98/MM80C98 provide the logical opposite of the input signal. The MM70C95/MM80C95 and the MM70C96/MM80C96 have common TRI-STATE controls for all six devices. The MM70C97/MM80C97 and the MM70C98/MM80C98 have two TRI-STATE controls; one for two devices and one for the other four devices. Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

Features

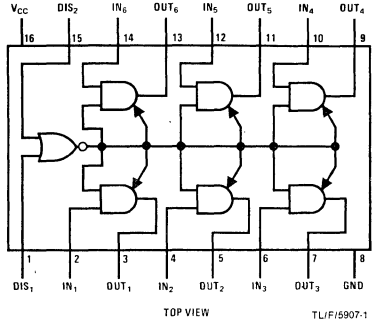
■ Wide supply voltage range	3.0 V to 15 V
■ Guaranteed noise margin	1.0 V
■ High noise immunity	0.45 V_{CC} (typ.)
■ TTL compatible	drive 1 TTL Load

Applications

■ Bus drivers — Typical propagation delay into 150 pF load is 40 ns.

Connection Diagrams (Dual-In-Line Packages)

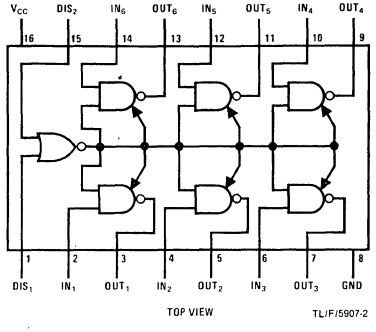
MM70C95/MM80C95



TOP VIEW TL/F/5907-1

Order Number MM70C95J, MM70C95N, MM80C95J or MM80C95N
See NS Package J16A or N16E

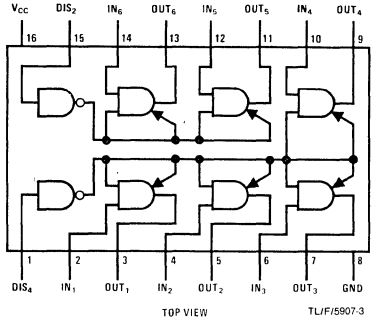
MM70C96/MM80C96



TOP VIEW TL/F/5907-2

Order Number MM70C96J, MM70C96N, MM80C96J or MM80C96N
See NS Package J16A or N16E

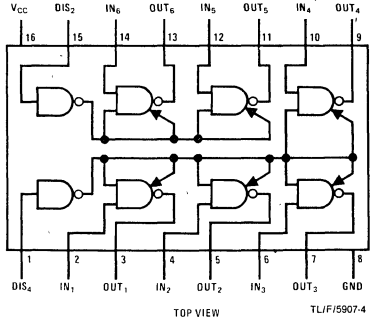
MM70C97/MM80C97



TOP VIEW TL/F/5907-3

Order Number MM70C97J, MM70C97N, MM80C97J or MM80C97N
See NS Package J16A or N16E

MM70C98/MM80C98



TOP VIEW TL/F/5907-4

Order Number MM70C98J, MM70C98N, MM80C98J or MM80C98N
See NS Package J16A or N16E

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3\,V$ to $V_{CC}+0.3\,V$	Storage Temperature Range	$-65°C$ to $+150°C$
Operating Temperature Range		Package Dissipation	500 mW
MM70CXX	$-55°C$ to $+125°C$	Power Supply Voltage (V_{CC})	18 V
MM80CXX	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 sec.)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	4.5 9.0			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	$V_{CC}=5.0\,V$, $V_{CC}=10\,V$			0.5 1.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		-1.0	-0.005		μA
I_{OZ}	Output Current in High Impedance State	$V_{CC}=15\,V$, $V_O=15\,V$ $V_{CC}=15\,V$, $V_O=0\,V$	 -1.0	0.005 -0.005	1.0	μA μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.01	15	μA
TTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage	70C $V_{CC}=4.5\,V$ 80C $V_{CC}=4.75\,V$	$V_{CC}-1.5$ $V_{CC}-1.5$			V V
$V_{IN(0)}$	Logical "0" Input Voltage	70C $V_{CC}=4.5\,V$ 80C $V_{CC}=4.75\,V$			0.8 0.8	V V
$V_{OUT(1)}$	Logical "1" Output Voltage	70C $V_{CC}=4.5\,V$, $I_O=-1.6\,mA$ 80C $V_{CC}=4.75\,V$, $I_O=-1.6\,mA$	2.4 2.4			V V
$V_{OUT(0)}$	Logical "0" Output Voltage	70C $V_{CC}=4.5\,V$, $I_O=1.6\,mA$ 80C $V_{CC}=4.75\,V$, $I_O=1.6\,mA$			0.4 0.4	V V
Output Drive (Short Circuit Current)						
I_{SOURCE}	Output Source Current	$V_{CC}=5.0\,V$, $V_{IN(1)}=5.0\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-4.35			mA
I_{SOURCE}	Output Source Current	$V_{CC}=10\,V$, $V_{IN(1)}=10\,V$ $T_A=25°C$, $V_{OUT}=0\,V$	-20			mA
I_{SINK}	Output Sink Current	$V_{CC}=5.0\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	4.35			mA
I_{SINK}	Output Sink Current	$V_{CC}=10\,V$, $V_{IN(0)}=0\,V$ $T_A=25°C$, $V_{OUT}=V_{CC}$	20			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5.0V$		60	100	ns
		$V_{CC} = 10V$		25	40	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5.0V$		70	150	ns
		$V_{CC} = 10V$		35	75	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5.0V$, $C_L = 150pF$		85	160	ns
		$V_{CC} = 10V$, $C_L = 150pF$		40	80	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5.0V$, $C_L = 150pF$		95	210	ns
		$V_{CC} = 10V$, $C_L = 150pF$		45	110	ns
t_{1H}, t_{0H}	Delay from Disable Input to High Impedance State, (from Logical "1" or Logical "0")	$R_L = 10k$, $C_L = 5.0pF$				
	MM70C95/MM80C95	$V_{CC} = 5.0V$		80	135	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5.0V$		100	180	ns
		$V_{CC} = 10V$		70	125	ns
	MM70C97/MM80C97	$V_{CC} = 5.0V$		70	125	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C98/MM80C98	$V_{CC} = 5.0V$		90	170	ns
		$V_{CC} = 10V$		70	125	ns
t_{H1}, t_{H0}	Delay from Disable Input to Logical "1" Level (from High Impedance State)	$R_L = 10k$, $C_L = 50pF$				
	MM70C95/MM80C95	$V_{CC} = 5.0V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5.0V$		130	225	ns
		$V_{CC} = 10V$		60	110	ns
	MM70C97/MM80C97	$V_{CC} = 5.0V$		95	175	ns
		$V_{CC} = 10V$		40	80	ns
	MM70C98/MM80C98	$V_{CC} = 5.0V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacitance TRI-STATE	Any Output (Note 2)		11		pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		60		pF

Truth Tables

MM70C95/MM80C95

DISABLE DIS_1	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C96/MM80C96

DISABLE DIS_1	INPUT DIS_2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

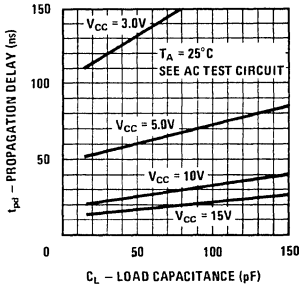
MM70C98/MM80C98

DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
X	1	X	H-z*
1	X	X	H-z**

*Output 5-6 only
**Output 1-4 only
X = Irrelevant

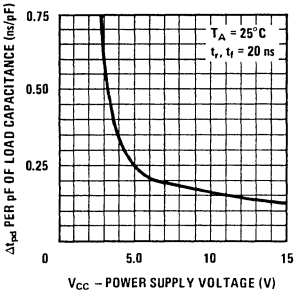
Typical Performance Characteristics

Propagation Delay vs Load Capacitance



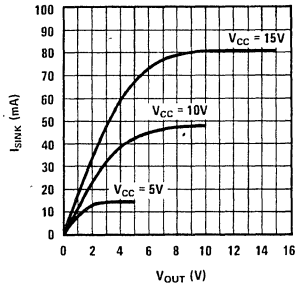
TL/F/5907-5

Δt_{pd}/pF vs Power Supply Voltage



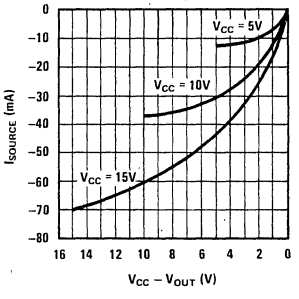
TL/F/5907-6

N-Channel Output Drive @ 25°C



TL/F/5907-7

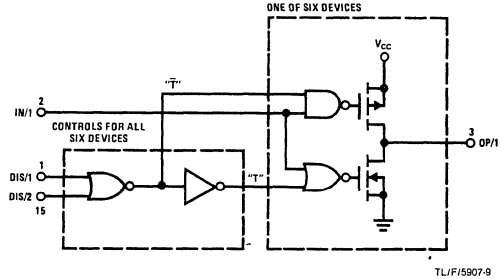
P-Channel Output Drive @ 25°C



TL/F/5907-8

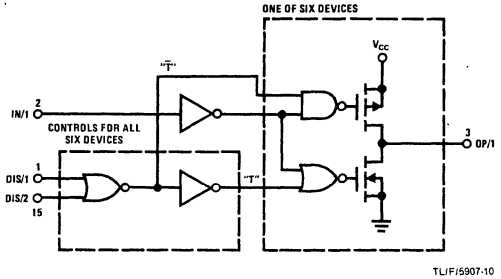
Schematic Diagrams

MM70C95/MM80C95 TRI-STATE



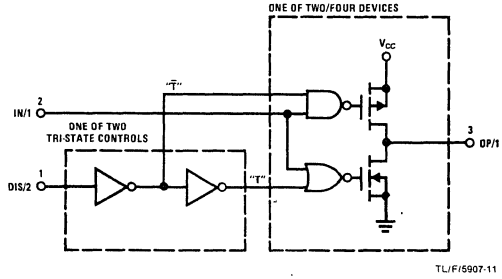
TL/F/5907-9

MM70C96/MM80C96 TRI-STATE



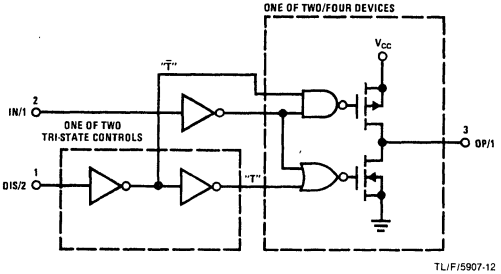
TL/F/5907-10

MM70C97/MM80C97 TRI-STATE



TL/F/5907-11

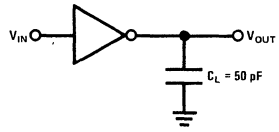
MM70C98/MM80C98 TRI-STATE



TL/F/5907-12

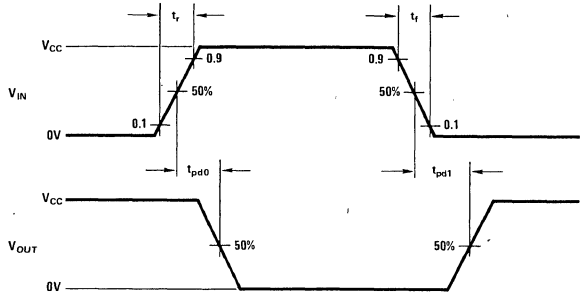
AC Test Circuits and Switching Time Waveforms

t_{pd0}, t_{pd1}



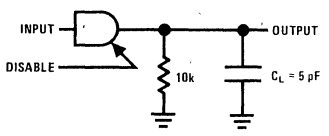
TL/F/5907-13

CMOS to CMOS



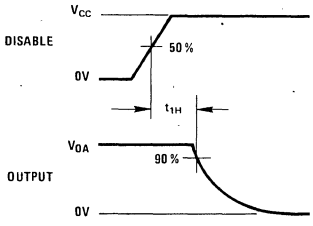
TL/F/5907-14

t_{1H} and t_{H1}

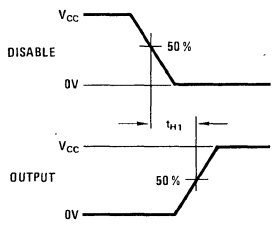


TL/F/5907-15

t_{1H}

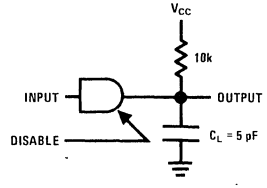


t_{H1}



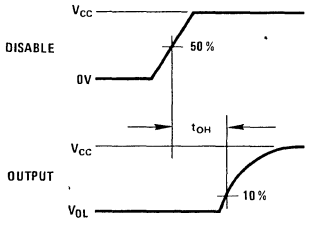
TL/F/5907-16

t_{0H} and t_{H0}

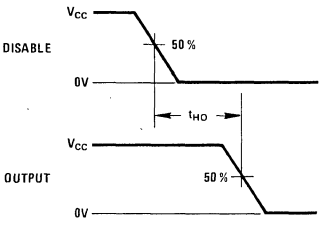


TL/F/5907-17

t_{0H}



t_{H0}



TL/F/5907-18

Note: Delays measured with input t_r, $t_f \leq 20$ ns

National Semiconductor

MM74C908, MM74C918 Dual CMOS 30-Volt Relay Driver

General Description

The MM74C908 and MM74C918 are general purpose dual high voltage drivers, each capable of sourcing a minimum of 250 mA at $V_{OUT} = V_{CC} - 3V$, and $T_J = +65°C$.

The MM74C908 and MM74C918 consist of two CMOS NAND gates driving an emitter follower darlington output to achieve high current drive and high voltage capabilities. In the "OFF" state the outputs can withstand a maximum of −30V across the device. These CMOS drivers are useful in interfacing normal CMOS voltage levels to driving relays, regulators, lamps, etc.

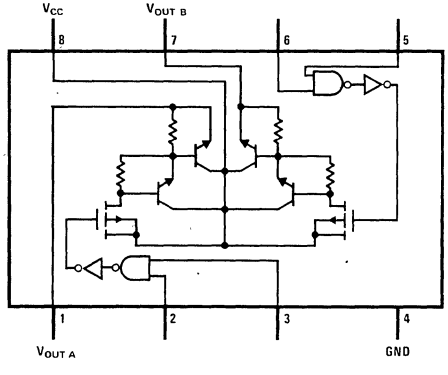
Features

■ Wide supply voltage range	3V to 18V
■ High noise immunity	$0.45V_{CC}$ (typ.)
■ Low output "ON" resistance	8Ω (typ.)
■ High voltage	−30V
■ High current	250 mA

Connection Diagrams

Dual-In-Line Package

MM74C908

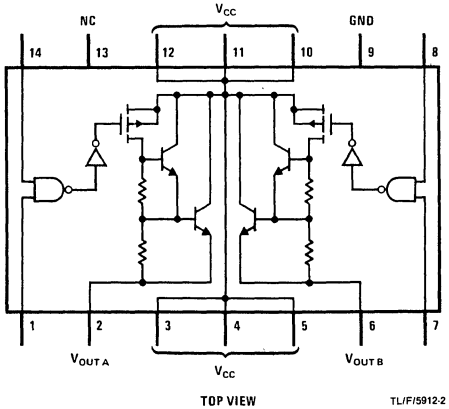


TOP VIEW TL/F/5912-1

Order Number MM74C908N
See NS Package N08E

Dual-In-Line Package

MM74C918



TOP VIEW TL/F/5912-2

Order Number MM74C918J
See NS Package J14A

Order Number MM74C918N
See NS Package N14A

6

Absolute Maximum Ratings (Note 1)

Voltage at Any Input Pin	$-0.3V$ to $V_{CC}+0.3V$	I_{SOURCE}	500 mA
Voltage at Any Output Pin	32V	Storage Temperature Range	$-65°C$ to $+150°C$
Operating Temperature Range		Lead Temperature (Soldering, 10 seconds)	300°C
MM74C908/MM74C918	$-40°C$ to $+85°C$	Package Dissipation	Refer to Maximum Power Dissipation vs Ambient Temperature Graph
Operating V_{CC} Range	4V to 18V		
Absolute Maximum V_{CC}	19V		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

Sym	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0V$ $V_{CC}=10V$			1.5 2.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15V$, $V_{IN}=15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15V$, $V_{IN}=0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC}=15V$, Outputs Open Circuit		0.05	15	μA
	Output "OFF" Voltage	$V_{IN}=V_{CC}$, $I_{OUT}=-200\mu A$		-30		V
CMOS/LPTTL Interface						
$V_{IN(1)}$	Logical "1" Input Voltage MM74C908/MM74C918	$V_{CC}=4.75V$	$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage MM74C908/MM74C918	$V_{CC}=4.75V$			0.8	V
Output Drive						
V_{OUT}	Output Voltage	$I_{OUT}=-300mA$, $V_{CC}\geq 5.0V$, $T_J=25°C$ $I_{OUT}=-250mA$, $V_{CC}\geq 5.0V$, $T_J=65°C$ $I_{OUT}=-175mA$, $V_{CC}\geq 5.0V$, $T_J=150°C$	$V_{CC}-2.7$ $V_{CC}-3.0$ $V_{CC}-3.15$	$V_{CC}-1.8$ $V_{CC}-1.9$ $V_{CC}-2.0$		V V V
R_{ON}	Output Resistance	$I_{OUT}=-300mA$, $V_{CC}\geq 5.0V$, $T_J=25°C$ $I_{OUT}=-250mA$, $V_{CC}\geq 5.0V$, $T_J=65°C$ $I_{OUT}=-175mA$, $V_{CC}\geq 5.0V$, $T_J=150°C$		6.0 7.5 10	9.0 12 18	Ω Ω Ω
	Output Resistance Coefficient			0.55	0.80	%/°C
θ_{JA}	Thermal Resistance MM74C908 MM74C918	 (Note 3) (Note 3)		 100 45	 110 55	 °C/W °C/W

AC Electrical Characteristics

Sym	Parameter	Conditions	Min	Typ	Max	Units
t_{pd1}	Propagation Delay to a Logic "1"	$V_{CC}=5.0V$, $R_L=50\Omega$, $C_L=50pF$, $T_A=25°C$ $V_{CC}=10V$, $R_L=50\Omega$, $C_L=50pF$, $T_A=25°C$		150 65	300 120	ns ns
t_{pd0}	Propagation Delay to a Logic "0"	$V_{CC}=5.0V$, $R_L=50\Omega$, $C_L=50pF$, $T_A=25°C$ $V_{CC}=10V$, $R_L=50\Omega$, $C_L=50pF$, $T_A=25°C$		2.0 4.0	10 20	μs μs
C_{IN}	Input Capacitance	(Note 2)		5.0		pF

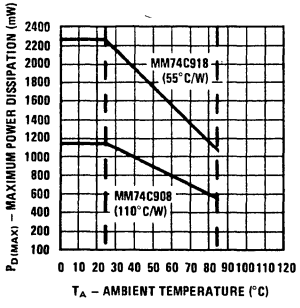
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: θ_{JA} measured in free air with device soldered into printed circuit board.

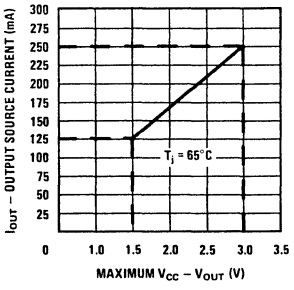
Typical Performance Characteristics

Maximum Power Dissipation vs Ambient Temperature



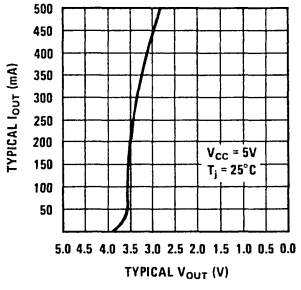
TL/F/5912-3

Maximum $V_{CC} - V_{OUT}$ vs I_{OUT}



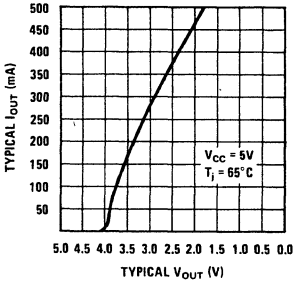
TL/F/5912-4

Typical I_{OUT} vs Typical V_{OUT}



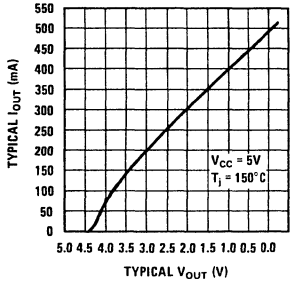
TL/F/5912-5

Typical I_{OUT} vs Typical V_{OUT}



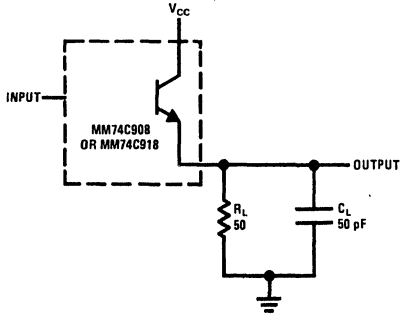
TL/F/5912-6

Typical I_{OUT} vs Typical V_{OUT}



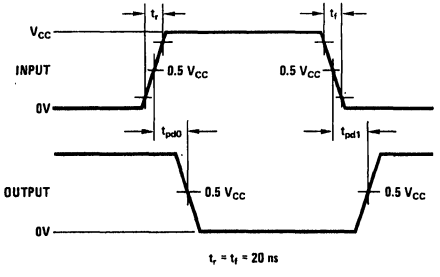
TL/F/5912-7

AC Test Circuit



TL/F/5912-8

Switching Time Waveforms



TL/F/5912-9

6

Power Considerations

Calculating Output "ON" Resistance ($R_L > 18\Omega$)

The output "ON" resistance, R_{ON}, is a function of the junction temperature, T_j, and is given by:

$$R_{ON} = 9\ (T_j - 25)\ (0.008) + 9 \qquad (1)$$

and T_j is given by:

$$T_j = T_A + P_{DAV}\ \theta_{jA}, \qquad (2)$$

where T_A = ambient temperature, θ_{jA} = thermal resistance, and P_{DAV} is the average power dissipated within the device. P_{DAV} consists of normal CMOS power terms (due to leakage currents, internal capacitance, switching, etc.) which are insignificant when compared to the power dissipated in the outputs. Thus, the output power term defines the allowable limits of operation and includes both outputs, A and B, P_D is given by:

$$P_D = I_{OA}^2\ R_{ON} + I_{OB}^2\ R_{ON}, \qquad (3)$$

where I_O is the output current, given by:

$$I_O = \frac{V_{CC} - V_L}{R_{ON} + R_L} \qquad (4)$$

V_L is the load voltage.

The average power dissipation, P_{DAV}, is a function of the duty cycle:

$$P_{DAV} = I_{OA}^2\ R_{ON}\ (\text{Duty Cycle}_A) + I_{OB}^2\ R_{ON}\ (\text{Duty Cycle}_B) \qquad (5)$$

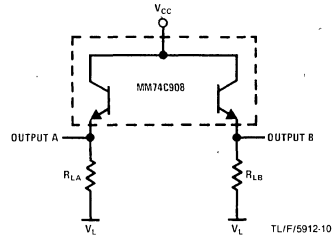
where the duty cycle is the % time in the current source state. Substituting equations (1) and (5) into (2) yields:

$$T_j = T_A + \theta_{jA}\ [9\ (T_j - 25)\ (0.008) + 9]\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)] \qquad (6a)$$

simplifying:

$$T_j = \frac{T_A + 7.2\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]} \qquad (6b)$$

Equations (1), (4), and (6b) can be used in an iterative method to determine the output current, output resistance and junction temperature.



For example, let $V_{CC} = 15V$, $R_{LA} = 100\Omega$, $R_{LB} = 100\Omega$, $V_L = 0V$, $T_A = 25°C$, $\theta_{jA} = 110°C/W$, Duty Cycle$_A$ = 50%, Duty Cycle$_B$ = 75%.
Assuming $R_{ON} = 11\Omega$, then:

$$I_{OA} = \frac{V_{CC} - V_L}{R_{ON} + R_{LA}} = \frac{15}{11 + 100} = 135.1\ \text{mA},$$

$$I_{OB} = \frac{V_{CC} - V_L}{R_{ON} + R_{LB}} = 135.1\ \text{mA}$$

and

$$T_j = \frac{T_A + 7.2\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}$$

$$T_j = \frac{25 + (7.2)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}{1 - (0.072)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}$$

$T_j = 52.6°C$

and $R_{ON} = 9\ (T_j - 25)\ (0.008) + 9 =$

$9\ (52.6 - 25)\ (0.008) + 9 = 11\Omega$

Applications

(See AN-177 for applications.)

National Semiconductor

MM74C911 4-Digit Expandable Segment Display Controller

General Description

The MM74C911 display controller is an interface element with memory that drives a 4-digit, 8-segment LED display. The MM74C911 allows individual control of any segment in the 4-digit display. The number of segments per digit can be expanded without any external components. For example, two MM74C911's can be cascaded to drive a 16-segment alpha-numeric display.

The display controllers receive data information through 8 data lines a, b . . . DP, and digit information through 2 address inputs K1 and K2. The input data is written into the register selected by the address information when Chip Enable, $\overline{CE}$, and Write Enable, $\overline{WE}$, are low and is latched when either $\overline{CE}$ or $\overline{WE}$ return high. Data hold time is not required.

A self-contained internal oscillator sequentially presents the stored data to high drive (100 mA typ) TRI-STATE® output drivers which directly drive the LED display. The drivers are active when the control pin labeled Segment Output Enable, $\overline{SOE}$, is low and go into TRI-STATE when $\overline{SOE}$ is high. This feature allows for duty cycle brightness control, or for disabling the output drive for power conservation.

The digit outputs directly drive the base of the digit transistor when the control pin labeled Digit Input Output, $\overline{DIO}$, is low. When $\overline{DIO}$ is high, the digit lines turn into inputs and the internal scanning multiplexer is disabled.

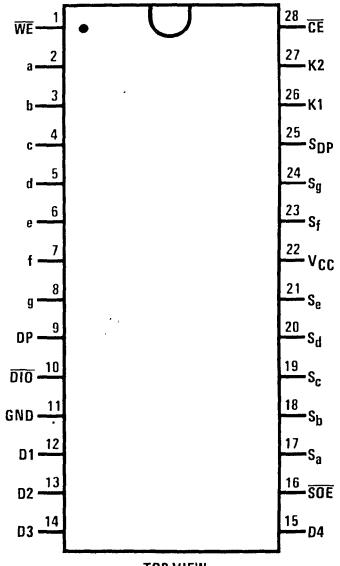
When any digit line is forced high by an external device, usually another MM74C911, the data information for that digit is presented to the output. In this manner, 16-segment alpha-numeric displays, 24 or 32-segment displays, or an array of discrete LED's can be controlled by the simple cascading of expandable segment display controllers. All inputs except digit inputs are TTL compatible and do not clamp input voltages above V_{CC}.

Features

- Direct segment drive (100 mA typ) TRI-STATE
- 4 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor
- Segment expandability without external components
- TTL compatible inputs
- Power saver mode—5 μW (typ.)

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5915-1

Order Number MM74C911N
See NS Package N28B

Truth Tables

Input Control

$\overline{CE}$	DIGIT ADDRESS		$\overline{WE}$	OPERATION
	K2	K1		
0	0	0	0	Write digit 1
0	0	0	1	Latch digit 1
0	0	1	0	Write digit 2
0	0	1	1	Latch digit 2
0	1	0	0	Write digit 3
0	1	0	1	Latch digit 3
0	1	1	0	Write digit 4
0	1	1	1	Latch digit 4
1	X	X	X	Disable writing

Output Control

$\overline{DIO}$	$\overline{SOE}$	DIGIT LINES				OPERATION
		D4	D3	D2	D1	
0	0	R	R	R	R	Refresh display
0	1	R	R	R	R	Disable segment outputs
1	0	0	0	0	0	Digits are now inputs
1	0	0	0	0	1	Display digit 1
1	0	0	0	1	0	Display digit 2
1	0	0	1	0	0	Display digit 3
1	0	1	0	0	0	Display digit 4
1	1	0	0	0	0	Power saver mode

R = Refresh (digit lines sequentially pulsed)
X = Don't care

Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Inputs	$-0.3V$ to $V_{CC} + 0.3V$	Package Dissipation	Refer to $P_{D(MAX)}$ vs T_A Graph
Voltage at Any Input Except Digits	$-0.3V$ to $+15V$	Operating V_{CC} Range	3V to 6V
Operating Temperature Range, T_A	$-40°C$ to $+85°C$	Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply at $-40°C \leq T_J \leq +85°C$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current (Normal)	$V_{CC} = 5V$. Outputs Open		0.50	2.5	mA
I_{CC}	Supply Current (Power Saver)	$V_{CC} = 5V$, $\overline{SOE}$, $\overline{DIO}$ = "1", D1, D2, D3, D4 = "0"		1	600	μA
I_{OUT}	TRI-STATE Output Current	$V_O = 5V$ $V_O = 0V$	 -10	0.03 -0.03	10	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC}-2.0$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	$V_{CC} = 5V$, $V_O = 3.4V$ $T_J = 25°C$ $T_J = 100°C$	 -60 -40	 -100 -60		 mA mA
I_{DH}	High Level Digit Current	$V_{CC} = 5V$, $V_O = 3V$ $T_J = 25°C$ $T_J = 100°C$ $V_{CC} = 5V$, $V_O = 1V$ $T_J = 25°C$ $T_J = 100°C$	 -10 -7 -15 -10	 -20 -10 -40 -15		 mA mA mA mA
$V_{OUT(1)}$	Logical "1" Output Voltage, Any Digit	$V_{CC} = 5V$, $I_O = -360\ \mu A$	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage Any Output	$V_{CC} = 5V$, $I_O = 360\ \mu A$			0.4	V
θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltage reference to ground.

Note 3: θ_{JA} measured in free-air with device soldered into printed circuit board.

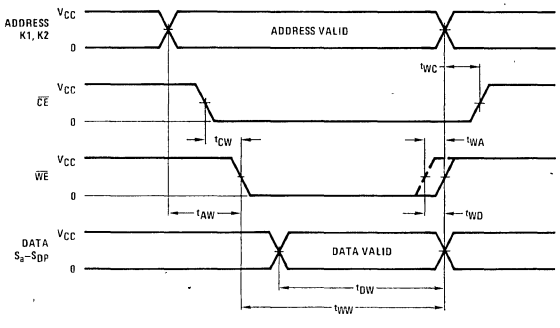
AC Electrical Characteristics $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $C_L = 50$ pF

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{CW}	Chip Enable to Write Enable Set-Up Time	$T_J = 25°C$	35	15		ns
		$T_J = 125°C$	50	20		ns
t_{AW}	Address to Write Enable Set-Up Time	$T_J = 25°C$	35	15		ns
		$T_J = 125°C$	50	20		ns
t_{WW}	Write Enable Width	$T_J = 25°C$	400	225		ns
		$T_J = 125°C$	450	250		ns
t_{DW}	Data to Write Enable Set-Up Time	$T_J = 25°C$	390	225		ns
		$T_J = 125°C$	430	250		ns
t_{WD}	Write Enable to Data Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WA}	Write Enable to Address Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WC}	Write Enable to Chip Enable Hold Time	$T_J = 25°C$	55	30		ns
		$T_J = 125°C$	75	40		ns
t_{1H}, t_{0H}	Logical "1", Logical "0" Levels into TRI-STATE	$R_L = 10k$, $C_L = 10$ pF				
		$T_J = 25°C$		275	500	ns
		$T_J = 125°C$		325	600	ns
t_{H1}, t_{H0}	TRI-STATE to Logical "1" or Logical "0" Levels	$R_L = 10k$, $C_L = 50$ pF				
		$T_J = 25°C$		325	600	ns
		$T_J = 125°C$		375	700	ns
t_{D1}, t_{D0}	Propagation Delay From Digit Input to Segment Output	$T_J = 25°C$		500	1000	ns
		$T_J = 125°C$		700	1400	ns
t_{IB}	Interdigit Blanking Time	$T_J = 25°C$	5	10		μs
		$T_J = 125°C$	10	20		μs
f_{MUX}	Multiplex Scan Frequency	$T_J = 25°C$		525		Hz
		$T_J = 125°C$		375		Hz
C_{IN}	Input Capacitance	(Note 4)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 4)		30	50	pF

Note 4: Capacitance guaranteed by periodic testing.

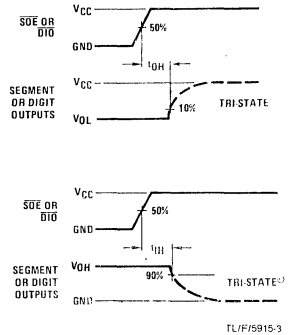
Switching Time Waveforms

Write Data Waveforms



TL/F/5915-2

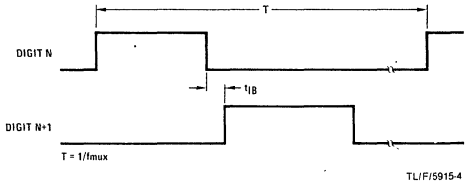
TRI-STATE Waveforms



TL/F/5915-3

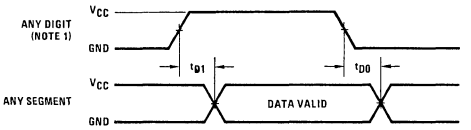
Switching Time Waveforms (Continued)

Multiplexing Output Waveforms



TL/F/5915-4

Read Data Waveforms



TL/F/5915-5

Note 1: All other digit lines are at a low level. $\overline{DIO}$ at a high level.

Functional Description

The MM74C911 display controller is manufactured on standard metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin to suppress current transients.

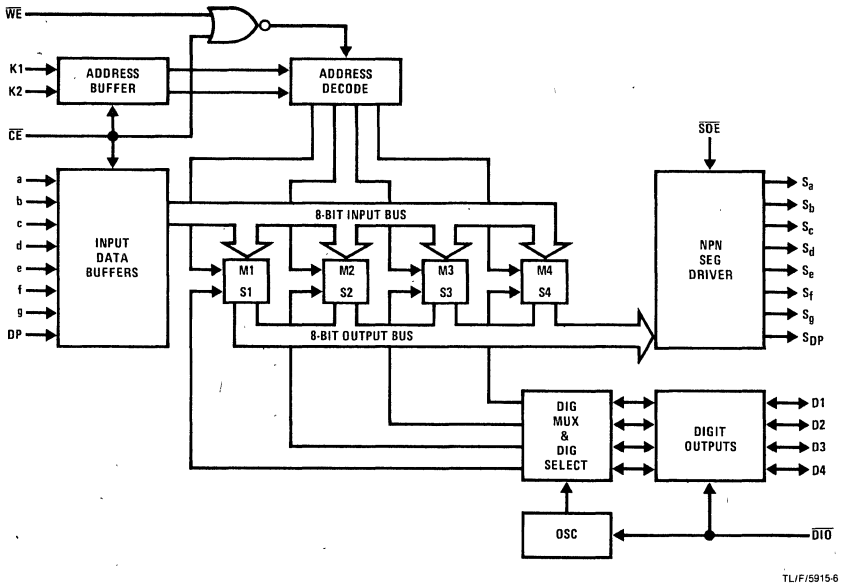
The digit outputs directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration. If an MM74C911 is driving a digit transistor and also supplying digit information to a cascaded MM74C911, base resistors are needed in the digit transistors to provide an adequate high level to the digit inputs of the cascaded MM74C911.

As seen in the block diagram, these display controllers contain four 8-bit registers; any one may be randomly written into. In normal operation, the internal multiplexer scans the registers and refreshes the display. In cascaded operation, 1 MM74C911 serves as a master refresh device and cascaded MM74C911's are slaved to it through digit lines operating as inputs.

The MM74C911 appears to a microprocessor as memory and to the user as a self-scan display. Since every segment is under microprocessor control, great versatility is obtained.

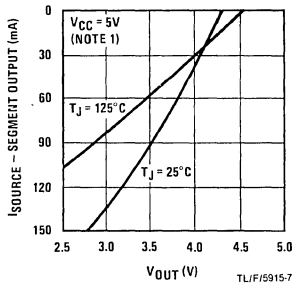
Low power standby operation occurs with both $\overline{SOE}$ and $\overline{DIO}$ inputs high. This condition forces the MM74C911 to a quiescent state typically drawing less than 1 μA of supply current with a standby supply voltage as low as 3V.

Block Diagram

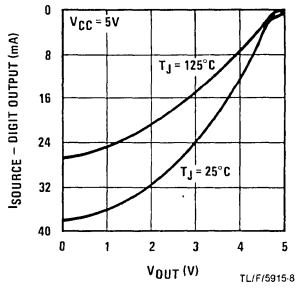


TL/F/5915-6

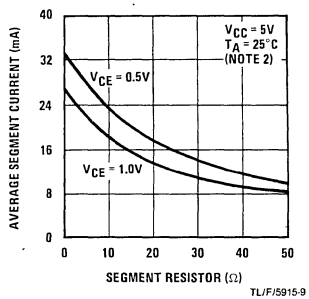
Typical Performance Characteristics



TL/F/5915-7

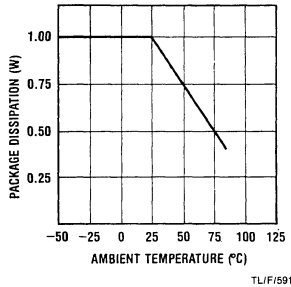


TL/F/5915-8



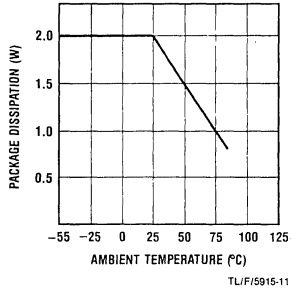
TL/F/5915-9

Power Dissipation vs. Temperature for Plastic Packages



TL/F/5915-10

Power Dissipation vs. Temperature for Ceramic Packages



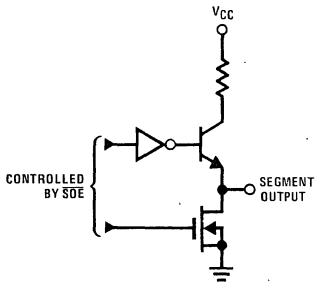
TL/F/5915-11

Note 1: Segment outputs if shorted to ground will exceed maximum power dissipation of the device.

Note 2: V_{CE} is the saturation voltage of the digit drive transistor.

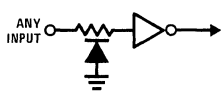
Applications

Segment Output Structure



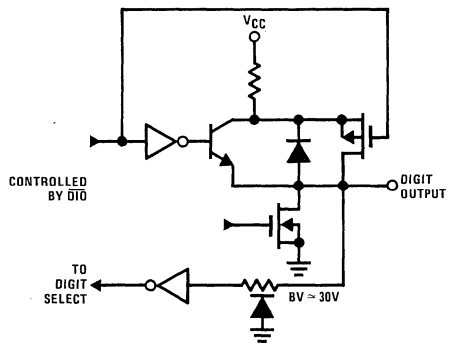
TL/F/5915-12

Input Protection



TL/F/5915-13

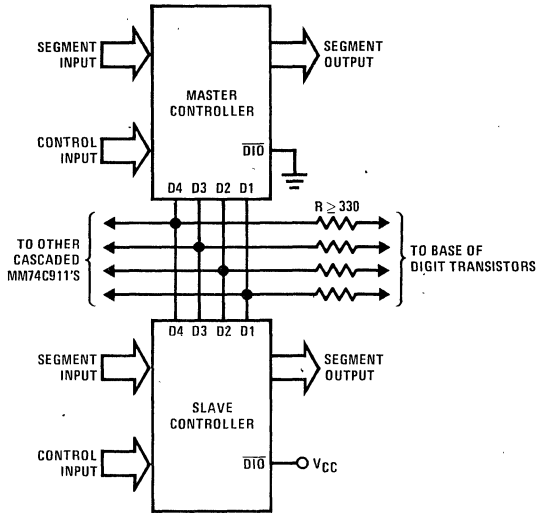
Digit Output Structure



TL/F/5915-14

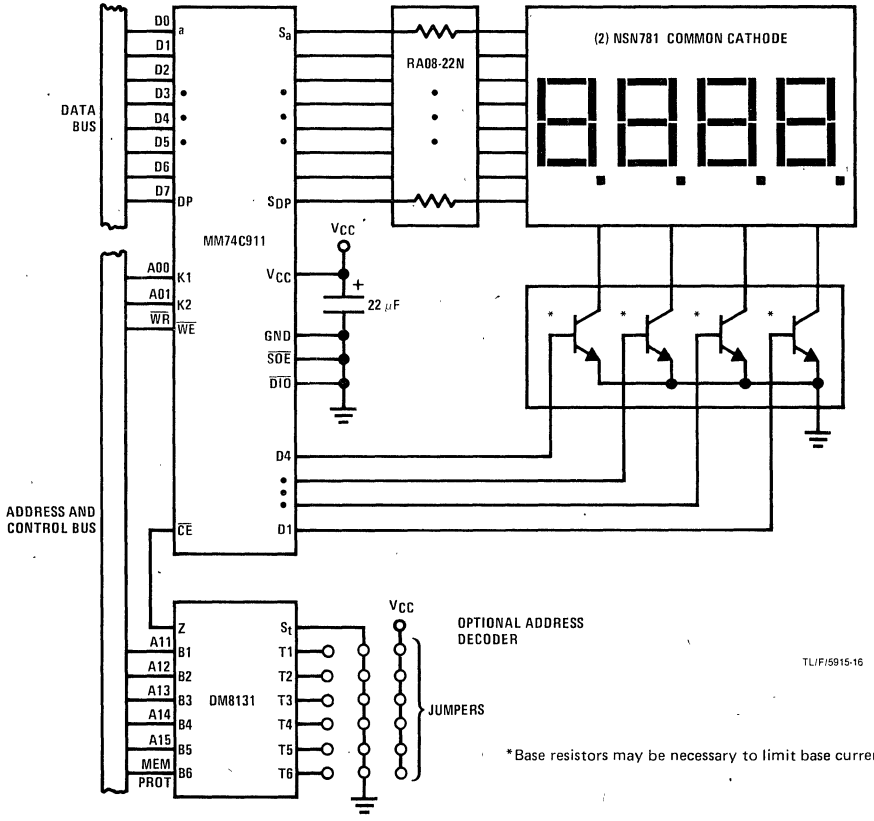
Applications (Continued)

Segment Expansion



TL/F/5915-15

Typical Application

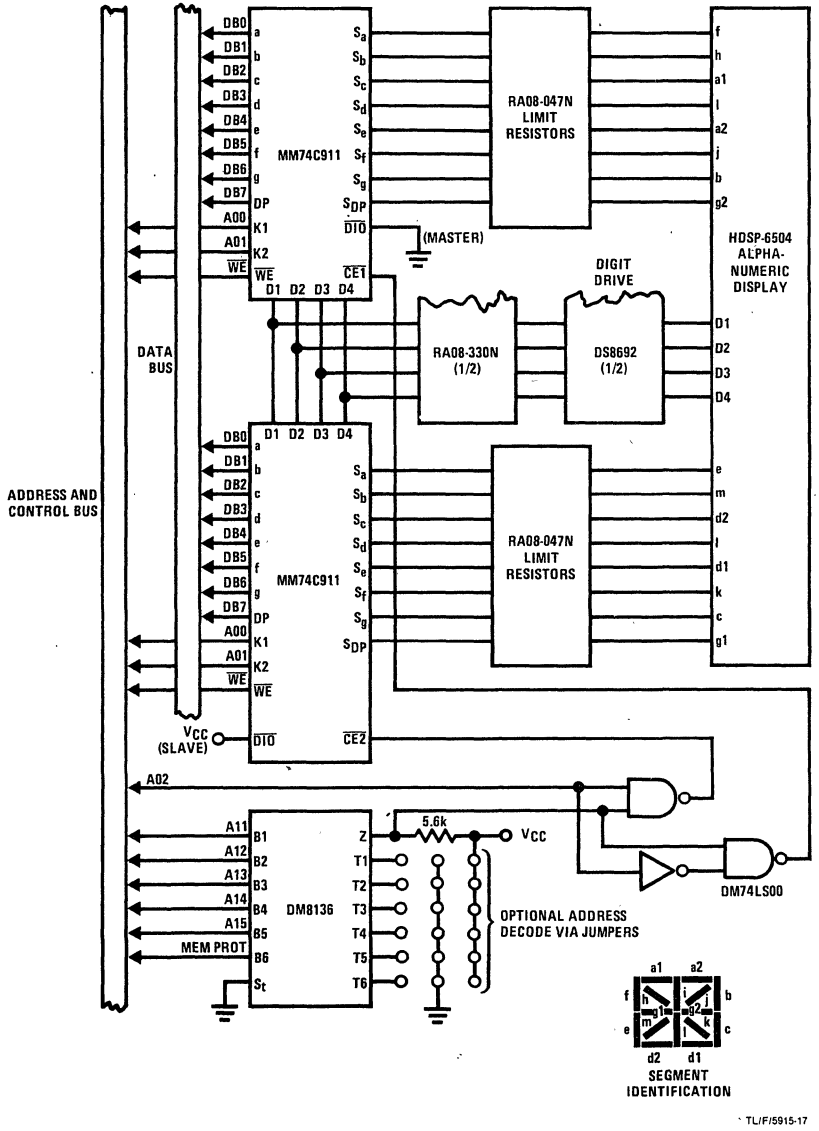


TL/F/5915-16

*Base resistors may be necessary to limit base current.

Applications (Continued)

4-Digit, 16-Segment Alpha-Numeric Display



National Semiconductor

MM74C912 6-Digit BCD Display Controller/Driver
MM74C917 6-Digit Hex Display Controller/Driver

General Description

The MM74C912, MM74C917 display controllers are interface elements, with memory, that drive a 6-digit, 8-segment LED display.

The display controllers receive data information through 5 data inputs A, B, C, D and DP, and digit information through 3 address inputs K1, K2 and K3.

The input data is written into the register selected by the address information when CHIP ENABLE, $\overline{CE}$, and WRITE ENABLE, $\overline{WE}$, are low and is latched when either $\overline{CE}$ or $\overline{WE}$ return high. Data hold time is not required. A self-contained internal oscillator sequentially presents the stored data to a decoder where 4 data bits control the format of the displayed character and 1 bit controls the decimal point. The internal oscillator is controlled by a control input labeled OSCILLATOR ENABLE, $\overline{OSE}$, which is tied low in normal operation. A high level at $\overline{OSE}$ prevents automatic refresh of the display.

The 7-segment plus decimal point output information directly drives a LED display through high drive (100 mA typ) output drivers. The drivers are active when the control pin labeled SEGMENT OUTPUT ENABLE, $\overline{SOE}$, is low and go into TRI-STATE® when $\overline{SOE}$ is high. This feature allows for duty cycle brightness control and for disabling the output drivers for power conservation.

The MM74C912 segment decoder converts BCD data into 7-segment format. The MM74C917 converts binary data into hex format.

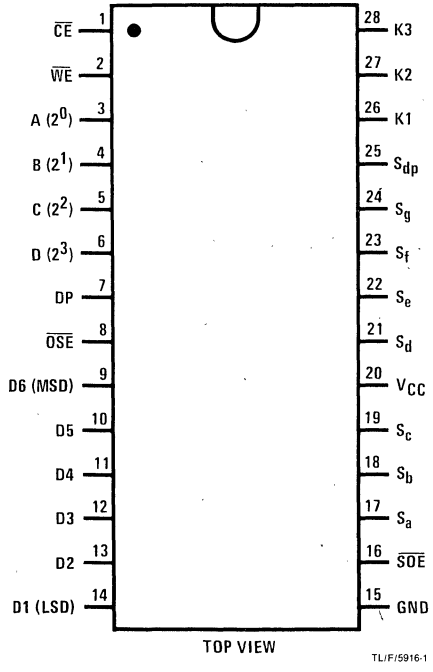
All inputs are TTL compatible and do not clamp to the V_{CC} supply.

Features

- Direct segment drive (100 mA typ) TRI-STATE
- 6 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor (20 mA typ)
- Internal segment decoder
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/5916-1

Order Number MM74C912N or MM74C917N
See NS Package N28B

Truth Tables

Input Control

$\overline{CE}$	DIGIT ADDRESS			$\overline{WE}$	OPERATION
	K3	K2	K1		
0	0	0	0	0	Write Digit 1
0	0	0	0	1	Latch Digit 1
0	0	0	1	0	Write Digit 2
0	0	0	1	1	Latch Digit 2
0	0	1	0	0	Write Digit 3
0	0	1	0	1	Latch Digit 3
0	0	1	1	0	Write Digit 4
0	0	1	1	1	Latch Digit 4
0	1	0	0	0	Write Digit 5
0	1	0	0	1	Latch Digit 5
0	1	0	1	0	Write Digit 6
0	1	0	1	1	Latch Digit 6
0	1	1	0	0	Write Null Digit
0	1	1	0	1	Latch Null Digit
0	1	1	1	0	Write Null Digit
0	1	1	1	1	Latch Null Digit
1	X	X	X	X	Disable Writing

X = don't care

Output Control

$\overline{SOE}$	$\overline{OSE}$	OPERATION
0	0	Refresh Display
0	1	Stop Oscillator*
1	0	Disable Segment Outputs
1	1	Standby Mode

*Segment drive may exceed maximum display dissipation.

Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Inputs	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	Refer to $P_{D\ MAX}$ vs T_A Graph
Voltage at Any Input	$-0.3V$ to $+15V$	Operating V_{CC} Range	3V to 6V
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$	Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 seconds)	$300°C$

DC Electrical Characteristics Min/max limits apply at $40°C \leq T_J \leq 85°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5V$			1.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current	$V_{CC} = 5V$, Outputs Open		0.5	2	mA
I_{OUT}	TRI-STATE Output Current	$V_{CC} = 5V$, $V_O = 5V$ $V_{CC} = 5V$, $V_O = 0V$	 -10	0.03 -0.03	10	μA μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC}-2.0$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	$V_{CC} = 5V$, $V_O = 3.4V$, $T_J = 25°C$ $T_J = 100°C$	 -60 -40	 -100 -60		mA mA
I_{DH}	High Level Digit Current	$V_{CC} = 5V$, $V_O = 1V$, $T_J = 25°C$ $T_J = 100°C$	 -10 -7	 -20 -15		 mA mA
$V_{OUT(1)}$	Logical "1" Output Voltage Any Digit	$V_{CC} = 5V$, $I_O = -360\ \mu A$	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage Any Output	$V_{CC} = 5V$, $I_O = 360\ \mu A$			0.4	V
Θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages reference to ground.

Note 3: Θ_{JA} measured in free air with device soldered into printed circuit board.

AC Electrical Characteristics $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $C_L = 50$ pF

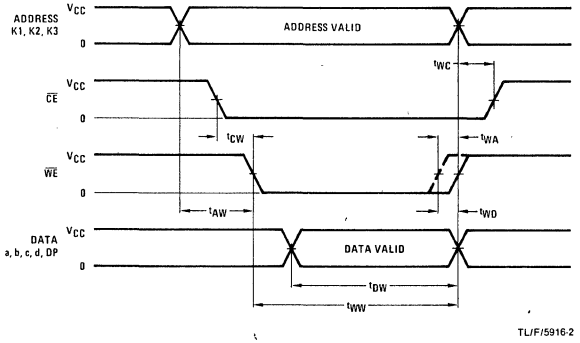
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{CW}	Chip Enable to Write Enable Setup Time	$T_J = 25°C$ $T_J = 125°C$	35 50	15 20		ns ns
t_{AW}	Address to Write Enable Setup Time	$T_J = 25°C$ $T_J = 125°C$	35 50	15 20		ns ns
t_{WW}	Write Enable Width	$T_J = 25°C$ $T_J = 125°C$	400 450	225 250		ns ns

AC Electrical Characteristics (Continued) $V_{CC} = 5V$, $t_r = t_f = 20$ ns, $C_L = 50$ pF

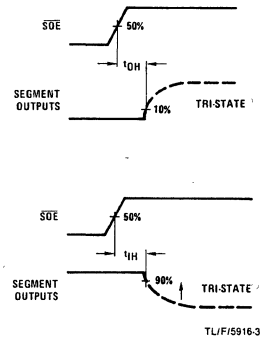
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{DW}	Data to Write Enable Setup Time	$T_J = 25°C$	390	225		ns
		$T_J = 125°C$	430	250		ns
t_{WD}	Write Enable to Data Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WA}	Write Enable to Address Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WC}	Write Enable to Chip Enable Hold Time	$T_J = 25°C$	50	30		ns
		$T_J = 125°C$	75	40		ns
t_{1H}, t_{0H}	Logical "1", Logical "0" Levels Into TRI-STATE	$R_L = 10k$, $T_J = 25°C$		275	500	ns
		$C_L = 10$ pF, $T_J = 125°C$		325	600	ns
t_{H1}, t_{H0}	TRI-STATE to Logical "1" to Logical "0" Level	$R_L = 10k$, $T_J = 25°C$		325	600	ns
		$C_L = 50$ pF, $T_J = 125°C$		375	700	ns
t_{IB}	Interdigit Blanking Time	$T_J = 25°C$	5	10		μs
		$T_J = 125°C$	10	20		μs
f_{MUX}	Multiplex Scan Frequency	$T_J = 25°C$		350		Hz
		$T_J = 125°C$		250		Hz
C_{IN}	Input Capacitance	Note 4		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Note 4		30	50	pF

Note 4: Capacitance is guranteed by periodic testing.

Switching Time Waveforms

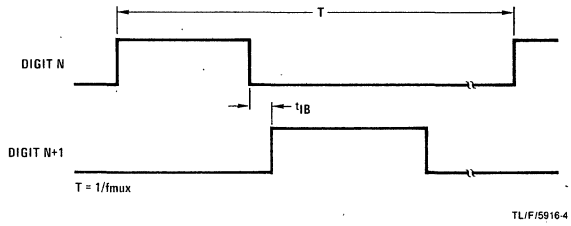


TL/F/5916-2



TL/F/5916-3

Multiplexing Output Waveforms



TL/F/5916-4

Functional Description

Character Font

MM74C917	Hi-Z	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F	.
MM74C912	Hi-Z	0	1	2	3	4	5	6	7	8	9	°	⁻	_	_			°
Input A 2^0	X	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
Data B 2^1	X	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
C 2^2	X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
D 2^3	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DP	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Output Enable $\overline{SOE}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Segment Identification

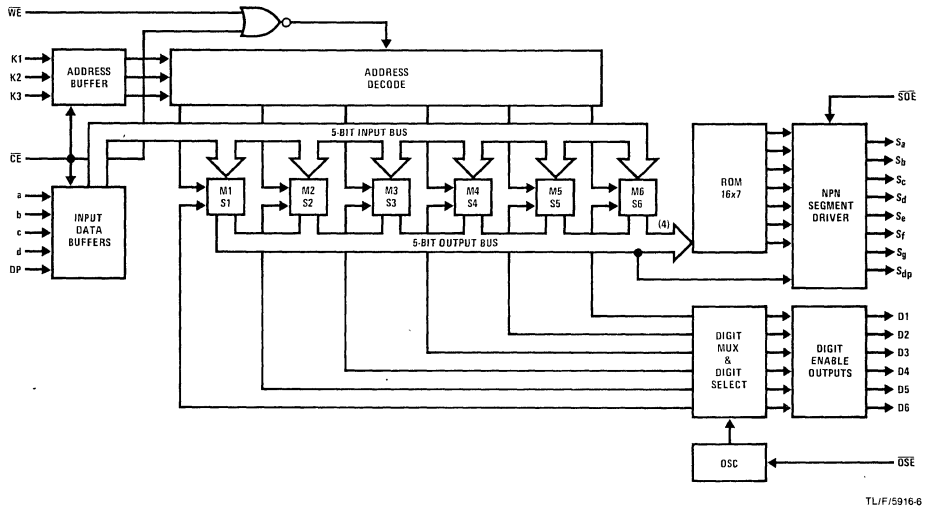
TL/F/5916 5

The MM74C912, MM74C917 display controllers are manufactured using metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin.

All inputs are TTL compatible; the segment outputs drive the LED display directly through current limiting resistors. The digit outputs are designed to directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration.

As seen in the block diagram, these display controllers contain six 5-bit registers; any one of which may be randomly written. The internal multiplexer scans the registers and refreshes the display. This combination of write only memory and self-scan display makes the display controller a "refreshing experience" for an overburdened microprocessor.

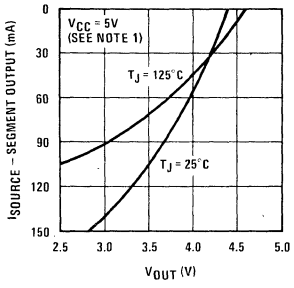
Block Diagram



TL/F/5916-6

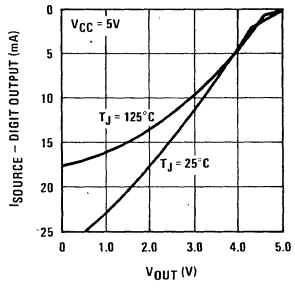
Typical Performance Characteristics

I_{SH} vs V_{OUT}



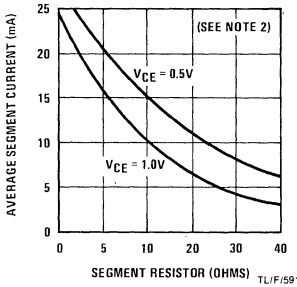
TL/F/5916-7

I_{DH} vs V_{OUT}



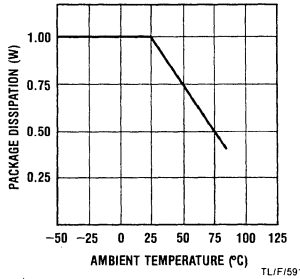
TL/F/5916-8

I_{AVG} vs R_{LIM}



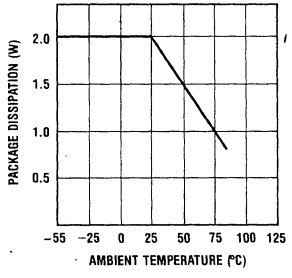
TL/F/5916-9

Power Dissipation vs. Temperature for Plastic Packages



TL/F/5916-10

Power Dissipation vs. Temperature for Ceramic Packages

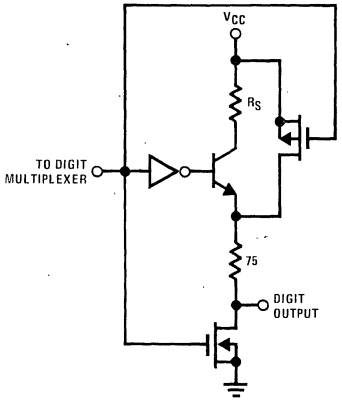


TL/F/5916-11

Note 1: Segment outputs if shorted to ground will exceed maximum power dissipation of the device.

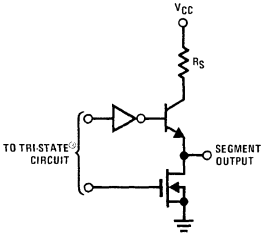
Note 2: V_{CE} is the saturation voltage of the digit drive transistor.

Digit Output Structure



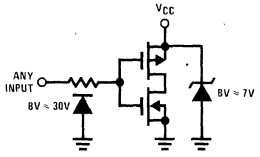
TL/F/5916-12

Segment Output Structure



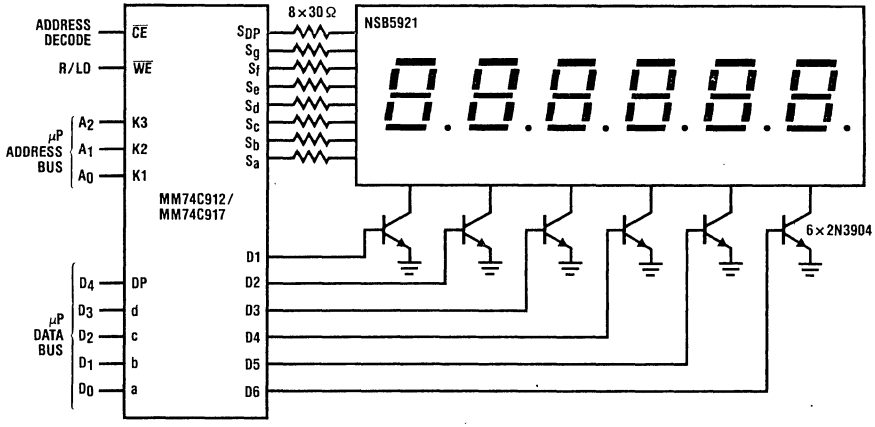
TL/F/5916-13

Input Protection



TL/F/5916-14

Typical Application



TL/F/5916-15

National Semiconductor

MM74C925, MM74C926, MM74C927, MM74C928 4-Digit Counters with Multiplexed 7-Segment Output Drivers

General Description

These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero, and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.

The MM74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The MM74C926 is like the MM74C925 except that it has a display select and a carry-out used for cascading counters. The carry-out signal goes high at 6000, goes back low at 0000.

The MM74C927 is like the MM74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The MM74C928 is like the MM74C926 except the most significant digit divides by 2 rather than 10 and the carry-out is an overflow indicator which is high at 2000, and it goes back low only when the counter is reset. Thus, this is a 3 1/2-digit counter.

Features

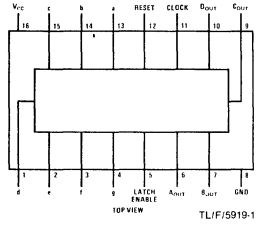
- Wide supply voltage range — 3V to 6V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} (typ.)
- High segment sourcing current — 40 mA @ V_{CC} − 1.6V, V_{CC} = 5V
- Internal multiplexing circuitry

Design Considerations

Segment resistors are desirable to minimize power dissipation and chip heating. The DS75492 serves as a good digit driver when it is desired to drive bright displays. When using this driver with a 5V supply at room temperature, the display can be driven without segment resistors to full illumination. The user must use caution in this mode however, to prevent overheating of the device by using too high a supply voltage or by operating at high ambient temperatures.

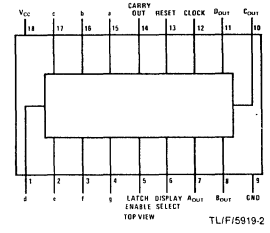
The input protection circuitry consists of a series resistor, and a diode to ground. Thus input signals exceeding V_{CC} will not be clamped. This input signal should not be allowed to exceed 15V.

Connection Diagram (Dual-In-Line Packages)



TL/F/5919-1

Order Number MM74C925N
See NS Package N16E
Order Number MM74C925J
See NS Package J16A



TL/F/5919-2

Order Number MM74C926N, MM74C927N or MM74C928N
See NS Package N18A

Order Number MM74C926J, MM74C927J or MM74C928J
See NS Package J18A

Functional Description

Reset — Asynchronous, active high

Display Select — High, displays output of counter
Low, displays output of latch

Latch Enable — High, flow through condition
Low, latch condition

Clock — Negative edge sensitive

Segment Output — Current sourcing with 40 mA @ V_{OUT} = V_{CC} − 1.6V (typ.)
Also, sink capability = 2 LTTL loads

Digit Output — Current sourcing with 1 mA @ V_{OUT} = 1.75V. Also, sink capability = 2 LTTL loads

Carry-out — 2 LTTL loads. See carry-out waveforms.

Absolute Maximum Ratings (Note 1)

Voltage at Any Output Pin	Gnd − 0.3V to V_{CC}+0.3V	Package Dissipation	Refer to $P_{D(MAX)}$ vs T_A Graph
Voltage at Any Input Pin	Gnd − 0.3V to +15V	Operating V_{CC} Range	3V to 6V
Operating Temperature Range (T_A)	−40°C to +85°C	V_{CC}	6.5V
Storage Temperature Range	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply at $-40°C \leq T_j \leq +85°C$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-out and Digit Output Only)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10μA			0.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.0V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.0V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5.0V, Outputs Open Circuit, V_{IN} = 0V or 5V		20	1000	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC}−2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 4.75V, I_O = −360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C	V_{CC}−2.0	V_{CC}−1.3		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C	V_{CC}−1.6	V_{CC}−1.2		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C	V_{CC}−2	V_{CC}−1.4		V
R_{ON}	Output Resistance (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		20	32	Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C		30	40	Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C		35	50	Ω
	Output Resistance (Segment Output) Temperature Coefficient			0.6	0.8	%/°C
I_{SOURCE}	Output Source Current (Digit Output)	V_{CC} = 4.75V, V_{OUT} = 1.75V, T_j = 150°C	−1	−2		mA
I_{SOURCE}	Output Source Current (Carry-out)	V_{CC} = 5V, V_{OUT} = 0V, T_j = 25°C	−1.75	−3.3		mA
I_{SINK}	Output Sink Current (All Outputs)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_j = 25°C	1.75	3.6		mA
θ_{jA}	Thermal Resistance	MM74C925 (Note 4)		75	100	°C/W
		MM74C926, MM74C927, MM74C928		70	90	°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

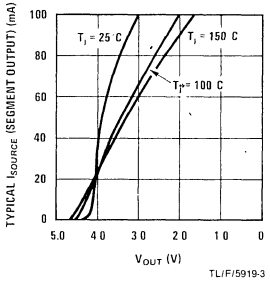
Note 4: θ_{jA} measured in free-air with device soldered into printed circuit board.

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50pF$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$,	$T_j = 25°C$	2	4		MHz
		Square Wave Clock	$T_j = 100°C$	1.5	3		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0V$				15	μs
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
t_{WLE}	Latch Enable Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
$t_{SET(CK,LE)}$	Clock to Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	2500	1250		ns
			$T_j = 100°C$	3200	1600		ns
t_{LR}	Latch Enable to Reset Wait Time	$V_{CC} = 5.0V$	$T_j = 25°C$	0	−100		ns
			$T_j = 100°C$	0	−100		ns
$t_{SET(R,LE)}$	Reset to Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	320	160		ns
			$T_j = 100°C$	400	200		ns
f_{MUX}	Multiplexing Output Frequency	$V_{CC} = 5.0V$			1000		Hz
C_{IN}	Input Capacitance	Any Input (Note 2)			5		pF

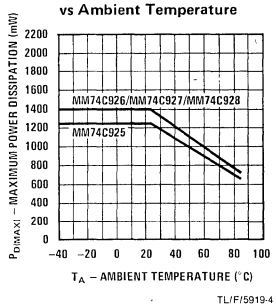
Typical Performance Characteristics

Typical Segment Current vs Output Voltage



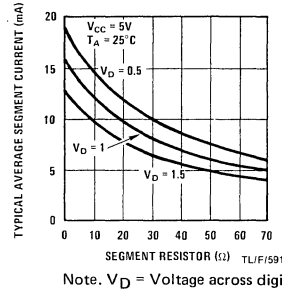
TL/F/5919-3

Maximum Power Dissipation vs Ambient Temperature



TL/F/5919-4

Typical Average Segment Current vs Segment Resistor Value

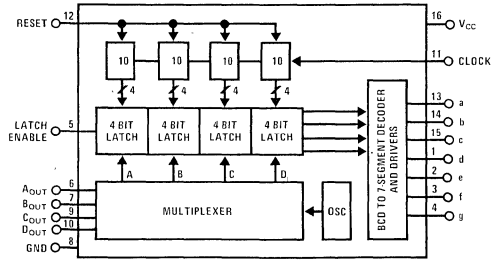


TL/F/5919-5

Note. V_D = Voltage across digit driver.

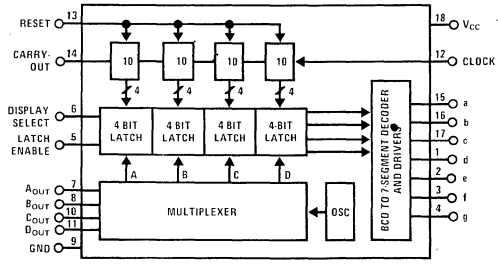
Logic and Block Diagrams

MM74C925



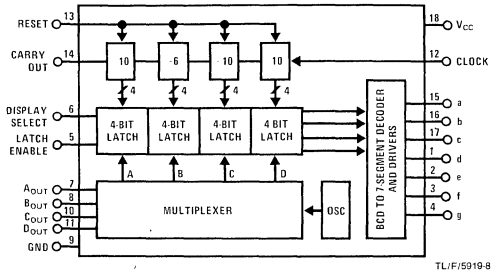
TL/F/5919-6

MM74C926



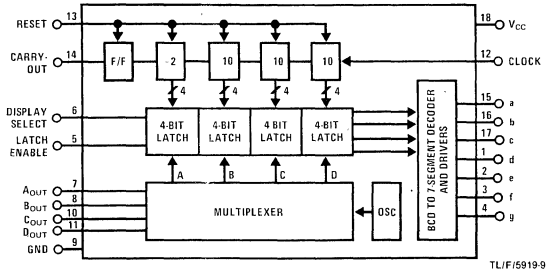
TL/F/5919-7

MM74C927



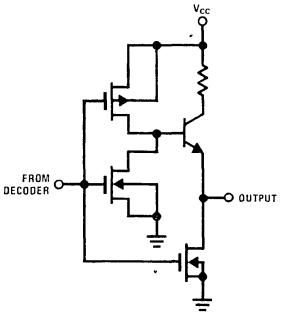
TL/F/5919-8

MM74C928



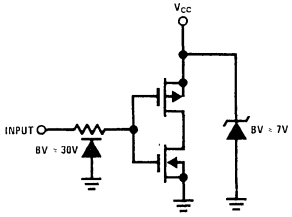
TL/F/5919-9

Segment Output Driver



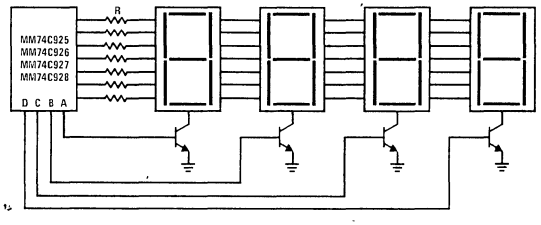
TL/F/5919-10

Input Protection



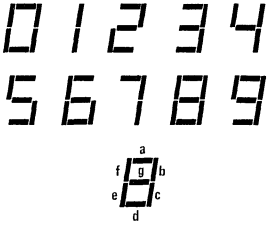
TL/F/5919-11

Common Cathode LED Display



TL/F/5919-12

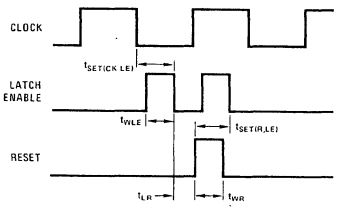
Segment Identification



TL/F/5919-13

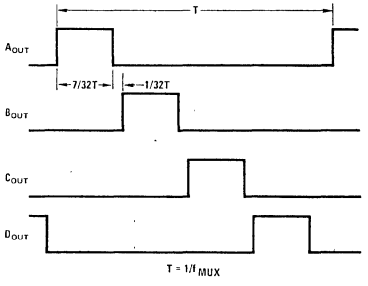
Switching Time Waveforms

Input Waveforms



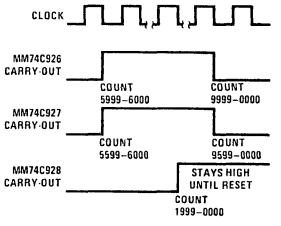
TL/F/5919-14

Multiplexing Output Waveforms



TL/F/5919-15

Carry-Out Waveforms



TL/F/5919-16

National Semiconductor

PRELIMINARY

MM74C945, MM74C947 4-Digit Up/Down Counter/Latch/Decoder Driver

General Description

The MM74C945, MM74C947 are 4-digit counters for directly driving LCD displays. The MM74C945 contains a 4-decade up/down counter, output latches, counter/latch select multiplexer and 7-segment decoders. Also included are the backplane oscillator/driver, segment drivers and display blanking circuitry.

The MM74C947 differs from the MM74C945 in that it has no counter/latch multiplexer, but provides true leading zero blanking. All leading zeroes are automatically blanked except the least significant digit, which can be optionally blanked.

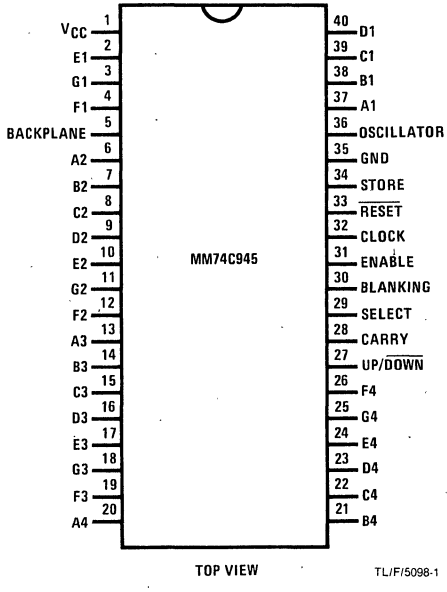
Both devices provide 28-segment outputs to drive a 4-digit display. Segment and backplane waveforms are generated internally, but can also be slaved to an external signal. This facilitates cascading of multiple displays.

Features

- 4-decade up/down count
- Direct 4-digit drive for high contrast and long display life
- Carry/borrow out for cascading counters
- Schmitt trigger clock input
- MM74C945 has display select to allow viewing of counter or latch
- Store and reset inputs allow operation as frequency or period counter
- MM74C947 has true ripple blanking; least significant digit may be optionally blanked

Connection Diagrams

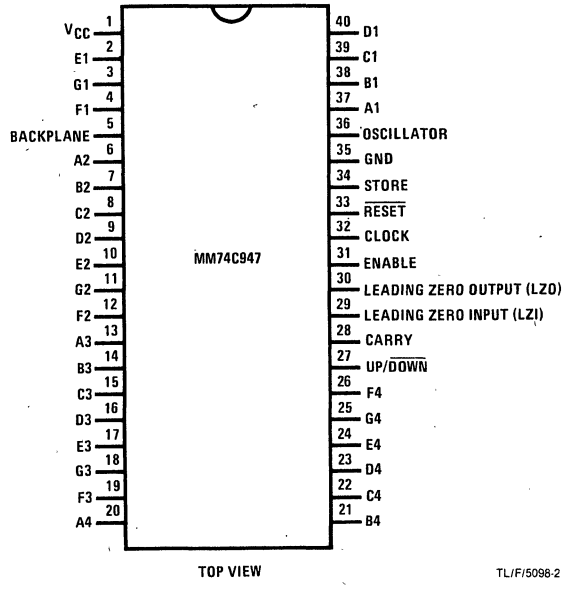
Dual-In-Line Package



TOP VIEW TL/F/5098-1

Order Number MM74C945N
See NS Package N40A

Dual-In-Line Package



TOP VIEW TL/F/5098-2

Order Number MM74C947N
See NS Package N40A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 6.0V
MM74C945/MM74C947	$-40°C$ to $+85°C$	Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Only)	$V_{CC}=5V$, V_{IN} (0→5) V	2.5	2.9	3.25	V
V_{T-} Negative Going Threshold Voltage (Clock Only)	$V_{CC}=5V$, V_{IN} (5→0) V	1.5	2.2	2.4	V
Hysteresis ($V_{T+}-V_{T-}$) (Clock Only)	$V_{CC}=5V$	0.1	0.7	1.75	V
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC}=5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC}=5V$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=-10\ \mu A$	4.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=+10\ \mu A$			0.5	V
Clock Input Current $\lvert I_{IN}\rvert$	$V_{CC}=5V$, $V_{IN}=5V/0V$		0.005	1.0	μA
Input Current @ Pins 29, 31, 33 and 34 (Note 2)	$V_{CC}=5V$, $V_{IN}=0V$	−2.0	−12	−25	μA
Oscillator Input Current (I_{OSL})	$V_{CC}=5V$, $V_{IN}=0V/5V$		±1	±10.0	μA
Supply Current (I_{CC}) (Note 3)	$V_{CC}=5V$, $V_{IN}=0V/5V$		10	60	μA
Oscillator Input Voltage $V_{IH(OSC)}$ $V_{IL(OSC)}$	When Driving Oscillator Pin with External Signal	 0.2 V_{CC}		$V_{CC}-0.2$	 V V
DC Offset Voltage (Note 4)	$V_{CC}=5V$			25	mV
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC}=4.75V$	$V_{CC}-1.5V$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC}=4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC}=4.75V$, $I_O=-360\ \mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC}=4.75V$, $I_O=360\ \mu A$			0.4	V
OUTPUT DRIVE (SHORT CIRCUIT CURRENT)					
Output Source Current (I_{SOURCE}) (LZO and Carry)	$V_{CC}=5V$, $V_{OUT}=0V$ $T_A=25°C$	1.75	2.7		mA
Output Sink Current (I_{SINK}) (LZO and Carry)	$V_{CC}=5V$, $V_{OUT}=5V$ $T_A=25°C$	1.75	3.2		mA
Output Source Current (I_{SOURCE}) (Segment Outputs)	$V_{CC}=5V$, $V_{OUT}=0V$ $T_A=25°C$	1.4	2.0		mA
Output Sink Current (I_{SINK}) (Segment Output)	$V_{CC}=5V$, $V_{OUT}=5V$ $T_A=25°C$	1.4	2.2		mA
Output Source Current (I_{SOURCE}) (Backplane Output)	$V_{CC}=5V$, $V_{OUT}=0V$ $T_A=25°C$	12.6	15.0		mA
Output Sink Current (I_{SINK}) (Backplane Output)	$V_{CC}=5V$, $V_{OUT}=5V$ $T_A=25°C$	12.6	20.0		mA

AC Electrical Characteristics $T_j = 25°C$, $C_L = 50$ pF, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Clock to Carry	$V_{CC} = 5.0V$		375	600	ns
f_{CLK}	Maximum Clock Frequency	$V_{CC} = 5.0V$	2	3		MHz
t_r, t_f	Clock Input Rise or Fall Time	$V_{CC} = 5.0V$			No Limit	
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$	180	120		ns
t_{WS}	Store Pulse Width	$V_{CC} = 5.0V$	150	80		ns
$t_{SU(CK, S)}$	Clock to Store Set-Up Time	$V_{CC} = 5.0V$	500	270		ns
t_{SR}	Store to Reset Wait Time	$V_{CC} = 5.0V$	280	170		ns
$t_{SU(E, CK)}$	Enable to Clock Set-Up Time	$V_{CC} = 5.0V$	140	80		ns
t_{RR}	Reset Removal	$V_{CC} = 5.0V$	50	0		ns
$t_{SU(U/D, CK)}$	Up/Down to Clock Set-Up Time	$V_{CC} = 5.0V$	300	190		ns
f_{BP}	Backplane Output Frequency	Pin 36 Floating, $V_{CC} = 5V$		85		Hz
C_{IN}	Input Capacitance	Logic Inputs (Note 2)		5		pF
t_{rfs}	Segment Rise/Fall Time	$C_{load} = 200$ pF		0.5		μs
t_{rfb}	Backplane Rise/Fall Time	$C_{load} = 5000$ pF		1.5		μs
f_{osc}	Oscillator Frequency	Pin 36 Floating, $V_{CC} = 5V$		11		kHz

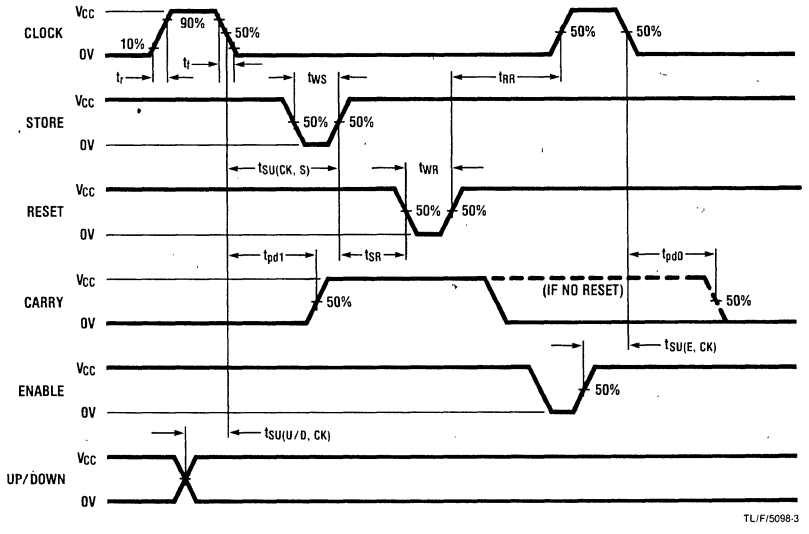
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Does not apply to backplane and oscillator pins.

Note 3: Display blanked. See Test Circuit.

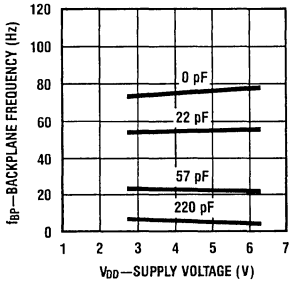
Note 4: DC offset voltage is the effective DC voltage the LCD will have between any segment and the backplane.

AC Waveforms



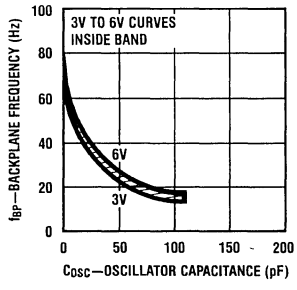
Typical Characteristics

Backplane Frequency as a Function of Supply Voltage



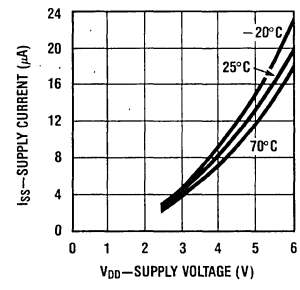
TL/F/5098-11

Backplane Frequency as a Function of Oscillator Capacitor (C_{OSC})



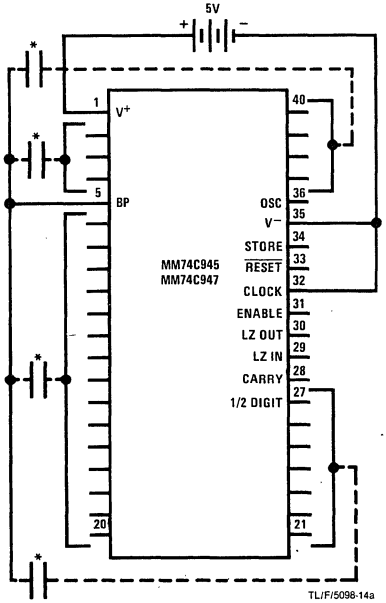
TL/F/5098-12

Operating Supply Current (I_{SS}) as a Function of Supply Voltage (V_{DD})



TL/F/5098-13

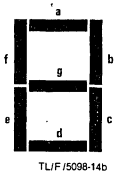
Test Circuit



TL/F/5098-14a

*Each segment to backplane with 200 pF capacitor.

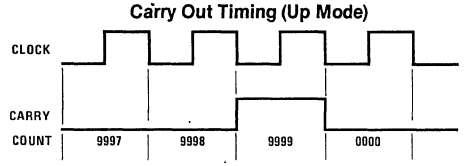
Segment Identification



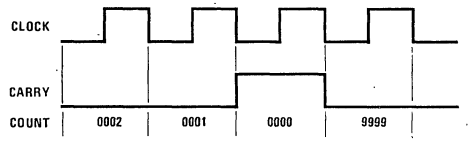
TL/F/5098-14b

Timing Diagrams

Carry Out Timing (Up Mode)



Carry Out Timing (Down Mode)

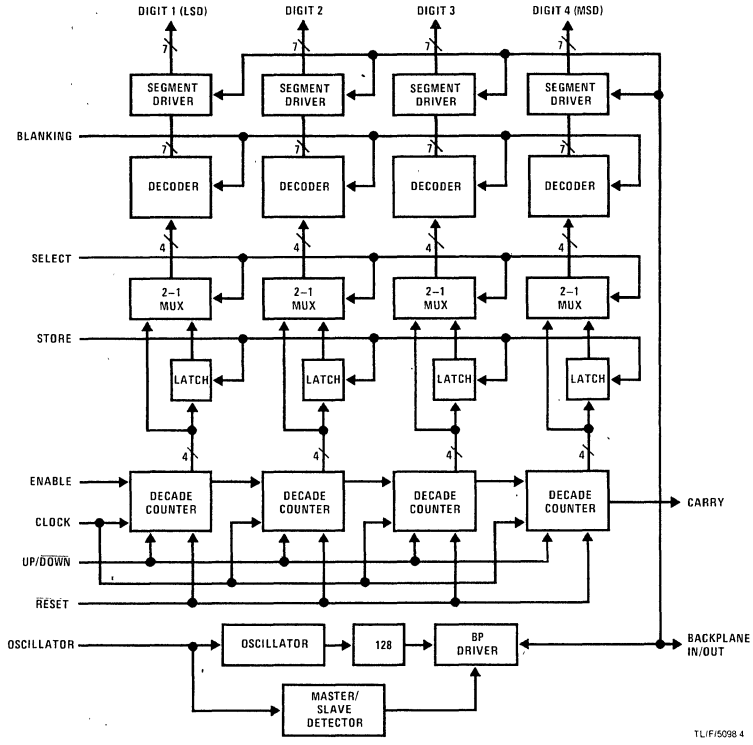


TL/F/5098-6

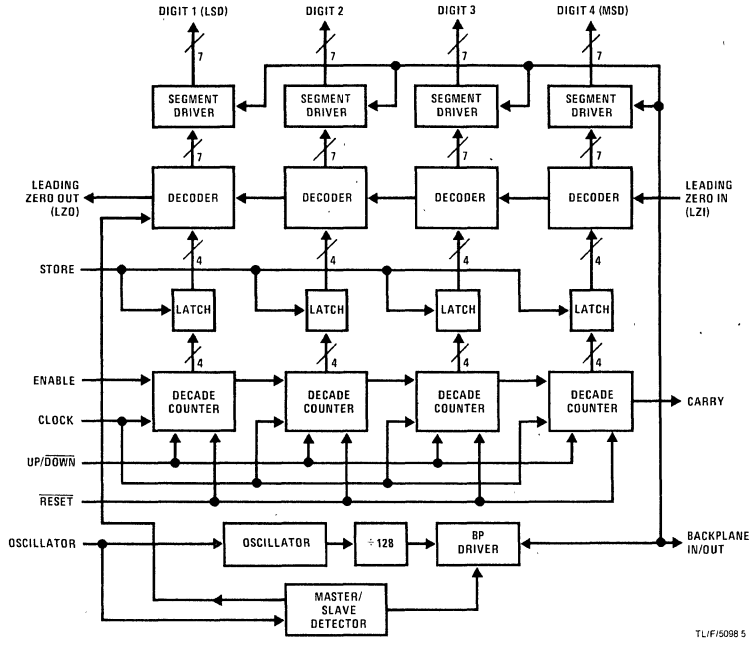
6

Block Diagrams

MM74C945



MM74C947



Pin Description

Backplane In/Out—When the oscillator input is grounded this pin is an input allowing an external device to generate a backplane waveform. When the oscillator input is left open this pin is an output supplying backplane drive for the display.

Oscillator—The oscillator frequency may be lowered by tying a capacitor (C_{OSC}) to this pin. On the MM74C947, when the oscillator pin is open, the LSD is inhibited from blanking when leading zero blanking is enabled. If this pin is grounded, the backplanes on both parts become inputs, slaving the device to an external backplane.

Store—This input controls the on-chip latches. When low, the latches are in flow-through mode (latch outputs follow counter), but when taken high, the data on the counter outputs are stored in the latches.

$\overline{\text{Reset}}$—When low, counters are reset to zero.

Clock—Advances counters on negative edge.

Enable—When low, halts counter operation.

Leading Zero Input (LZI)—(MM74C947) When high, enables leading zero blanking.

Leading Zero Output (LZO)—(MM74C947) This output goes high when the latch contents equal zero, LZI is high and the oscillator pin is open.

Blanking—(MM74C945) When high, blanks display.

Select—(MM74C945) When high, the contents of the counter are displayed. When low, the contents of the latch are displayed.

Carry—This output goes high when 9999 is reached (up) or 0000 is reached (down).

Up/$\overline{\text{Down}}$—When high, the counter counts up. When low, the counter counts down.

A1-G1—Digit 1 segment outputs.

A2-G2—Digit 2 segment outputs.

A3-G3—Digit 3 segment outputs.

A4-G4—Digit 4 segment outputs.

Application Hints

Display Circuitry Description

The MM74C945 and MM74C947 have 28 segment outputs capable of directly driving 4 digits of 7 segments. Both the segment and backplane drivers are designed to provide matched rise and fall times eliminating possible DC components in the driving waveforms which could degrade display life (i.e., DC offset voltage).

The backplane driver can be disabled by grounding the oscillator pin. This enables the segment output waveforms to be synchronized to an external signal applied to the backplane pin. Several devices can then be driven by a single master backplane waveform which can be generated by another MM74C945, MM74C947 or an external oscillator. Thus single backplane displays with 8, 12, 16, etc. digits can be driven with several counters. The maximum fanout of a master backplane driver is limited by its total capacitive load, which is the sum of the slaved backplane input capacitances and the display backplane capacitance. (The MM74C947 oscillator pin controls the least significant digit blanking as well.)

An on-board oscillator/divider generates the segment/backplane waveforms. Its output frequency is typically 85 Hz, but may be lowered by connecting an external capacitor (C_{OSC}) between the oscillator pin and ground. The oscillator pin may also be driven by an external waveform but the input low level must not go to ground or else the backplane pin will be put in the slave (input) mode (see $V_{IH(OSC)}$ and $V_{IL(OSC)}$ specifications).

Counter Circuitry Description

The MM74C945, MM74C947 are 4-decade up/down counters. The direction of the count is controlled by the up/$\overline{\text{down}}$ input. A high level on this pin causes the counter to count up. The counter advances on the negative clock edge. The carry output is high for one clock period during a count of 9999 in up mode, or during a count of 0000 in down mode. The carry is designed to allow cascading of several circuits in either ripple carry or synchronous modes.

Reset and Enable controls are provided to allow period and frequency measurements. The Reset control clears the counter when low and the Enable control disables counting when taken low.

The counter chain feeds a series of 4-bit flow-through latches. These latches enable the display to follow the counter when the Store input is low. When the Store pin is taken high the data on the counter outputs at this time become latched and the display will remain unchanged. (Assuming the latch display is selected on MM74C945.)

On the MM74C945 the latch outputs feed a multiplexer which selects either the latch outputs or counter outputs for display. This allows an intermediate count to be stored in the latches while the counter continues to be displayed. This is equivalent to a stopwatch lap feature.

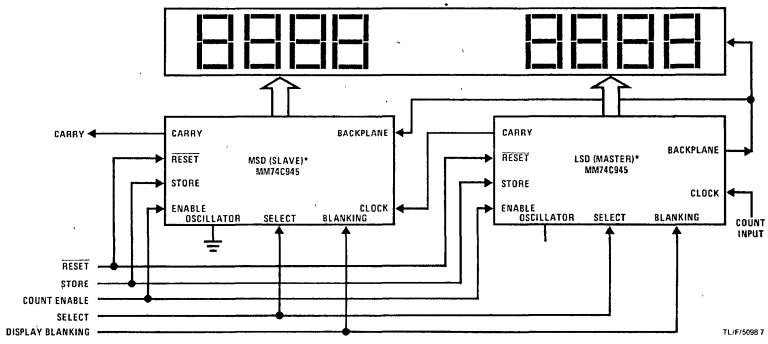
The output of the MM74C945's multiplexer feeds a decoder which converts 4-bit input to 7-segment outputs. A blanking control into these decoders blanks the display.

On the MM74C947 the latch outputs feed the decoders directly, but these decoders have a special ripple blanking capability that enables all leading zeroes except the least significant digit (LSD) to be blanked, even when counters are cascaded. Thus when the entire counter reads zero, instead of blanking all digits, the LSD will remain on. (When multiple counters are cascaded, all except the least significant counter will blank entirely on zeroes.) This feature is properly implemented by configuring the least significant device as the master (oscillator pin ungrounded) thereby inhibiting LSD blanking.

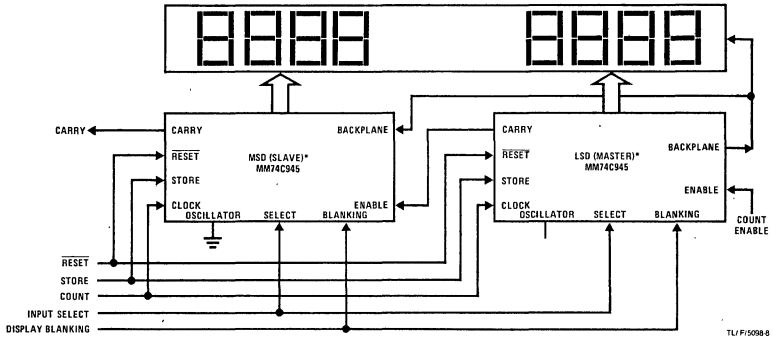
The outputs of the decoders for both devices control the segment drivers, which in turn enable display operation.

Typical Applications

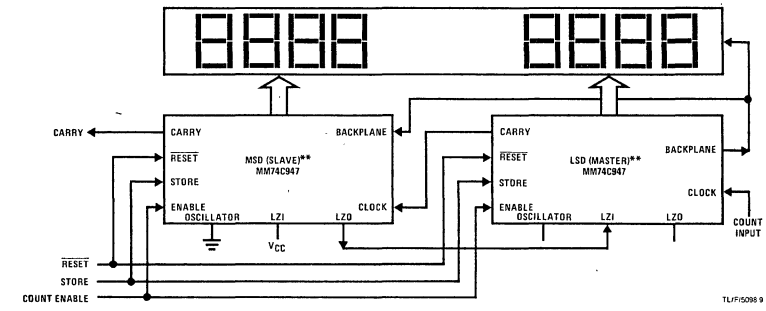
Ripple Carry Cascading—MM74C945



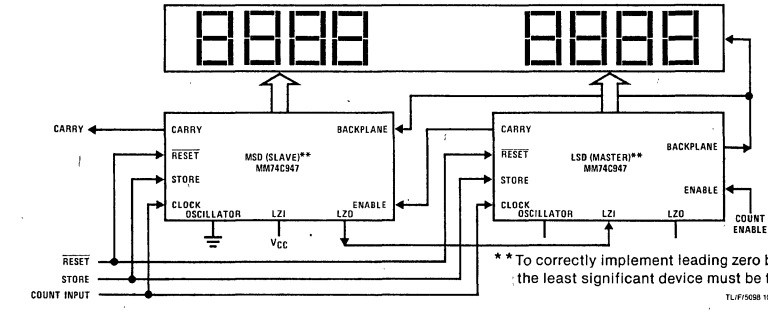
Synchronous Cascading—MM74C945



Ripple Cascading—MM74C947



Synchronous Cascading—MM74C947



** To correctly implement leading zero blanking, the least significant device must be the master.

* Master/slave selection is arbitrary and dependent only on which oscillator pin is grounded.

National Semiconductor

PRELIMINARY

MM74C946 4½-Digit Counter/Decoder/Driver for LCD Displays

General Description

The MM74C946 is a 4½-digit CMOS counter which contains a counter chain, decoders, output latches, LCD segment drivers, count inhibit and backplane oscillator/driver circuitry. This device also contains leading zero blanking and a carry output to increase flexibility and facilitate cascading of multiple 4-digit sections.

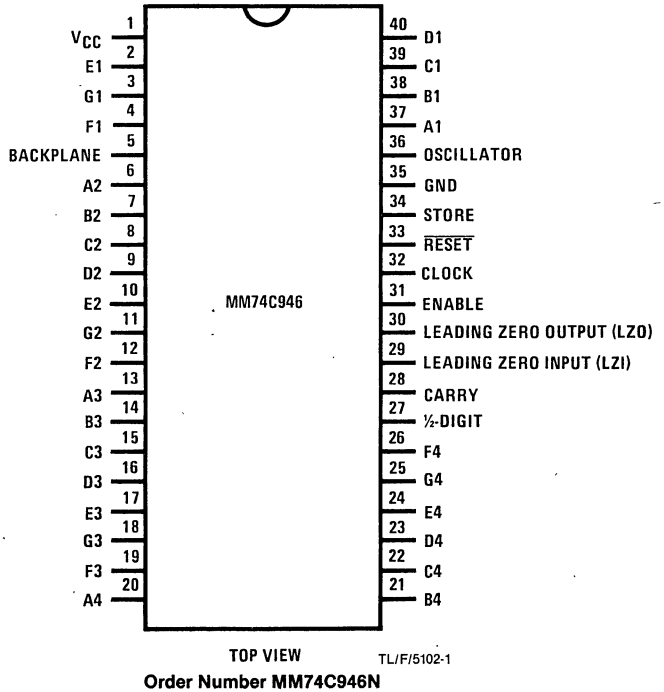
This device provides 29 segment outputs to drive a standard 4½-digit liquid crystal display. An on-chip backplane oscillator/driver is also provided. This can be disabled by grounding the oscillator pin, thus allowing the device to be slaved to an external backplane signal via the backplane pin.

Features

- Low power operation—less than 100 μW quiescent
- Direct 4½-digit 7-segment display drive for higher contrast and long display life
- Pin compatible to Intersil's ICM7224
- Store and $\overline{\text{Reset}}$ inputs permit operation as frequency or period counter
- True count inhibit disables first counter stage
- Carry output for cascading 4-digit blocks
- Schmitt trigger on the clock input allows operation in noisy environments or with slowly changing inputs
- Leading zero blanking input and output for correct leading zero blanking with cascaded devices
- On-chip backplane oscillator/driver which can be disabled to permit slaving of multiple devices to an external backplane signal

Connection Diagram

Dual-In-Line Package



TOP VIEW TL/F/5102-1

Order Number MM74C946N
See NS Package N40A

6

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 6.0V
MM74C946	$-40°C$ to $+85°C$	Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage (Clock Input)	$V_{CC}=5V$, V_{IN} (0→5) V	2.5	2.9	3.25	V
V_{T-} Negative Going Threshold Voltage (Clock Input)	$V_{CC}=5V$, V_{IN} (5→0) V	1.5	2.2	2.4	V
Hysteresis ($V_{T+}-V_{T-}$) (Clock Input)	$V_{CC}=5V$	0.1	0.7	1.75	V
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC}=5V$	3.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC}=5V$			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=-10\ \mu A$	4.5			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC}=5V$, $I_O=+10\ \mu A$			0.5	V
Clock Input Current $\lvert I_{IN}\rvert$	$V_{CC}=5V$, $V_{IN}=5V/0V$		0.005	1.0	μA
Input Current @ Pins 29, 31, 33 and 34 (Note 2)	$V_{CC}=5V$, $V_{IN}=0V$	-2.0	-12.0	-25.0	μA
Oscillator Input Current (I_{OSL})	$V_{CC}=5V$, $V_{IN}=0V/5V$		± 1.0	± 10.0	μA
Supply Current (I_{CC}) (Note 3)	$V_{CC}=5V$, $V_{IN}=0V/5V$		10	60	μA
Oscillator Input Voltage $V_{IH\ (OSC)}$ $V_{IL\ (OSC)}$	When Driving Oscillator Pin with External Signal	 $0.2\ V_{CC}$		$V_{CC}-0.2$	 V V
DC Offset Voltage (Note 4)	$V_{CC}=5V$			25	mV
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC}=4.75V$	$V_{CC}-1.5V$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC}=4.75V$			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (LZO and Carry)	$V_{CC}=4.75V$, $I_O=-360\ \mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$) (LZO and Carry)	$V_{CC}=4.75V$, $I_O=360\ \mu A$			0.4	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These input pins have pull-ups to V_{CC}.

Note 3: See test circuit. Display blanked.

Note 4: DC offset voltage is the effective DC voltage the LCD will have between any segment and the backplane.

DC Electrical Characteristics (Continued)

Min/max limits apply across temperature range, unless otherwise noted.

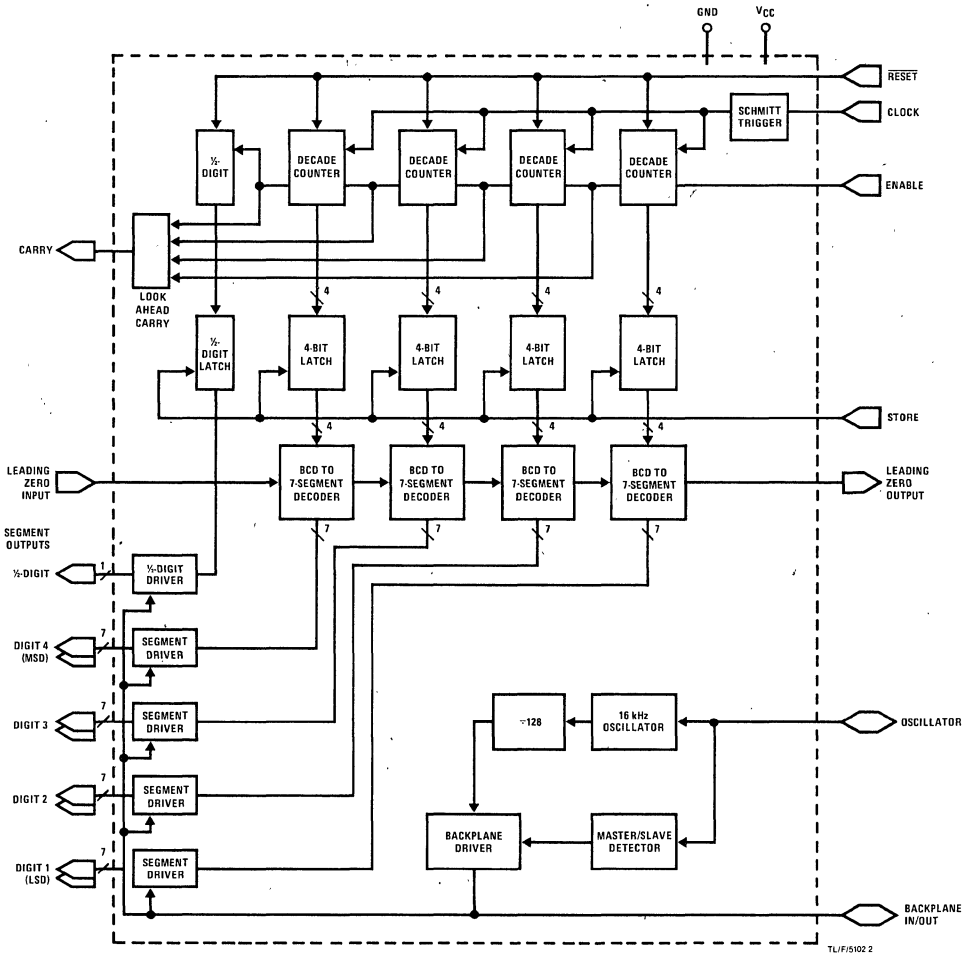
Parameter	Conditions	Min	Typ	Max	Units
OUTPUT DRIVE (SHORT CIRCUIT CURRENT)					
Output Source Current (I_{SOURCE}) (LZO and Carry)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	1.75	2.7		mA
Output Sink Current (I_{SINK}) (LZO and Carry)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	1.75	3.2		mA
Output Source Current (I_{SOURCE}) (Segment Outputs)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	1.4	2.0		mA
Output Sink Current (I_{SINK}) (Segment Outputs)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	1.4	2.2		mA
Output Source Current (I_{SOURCE}) (Backplane Output)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	12.6	15.0		mA
Output Sink Current (I_{SINK}) (Backplane Output)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	12.6	20.0		mA
Output Source Current (I_{SOURCE}) (½-Digit)	$V_{CC} = 5V$, $V_{OUT} = 0V$ $T_A = 25°C$	2.8	3.4		mA
Output Sink Current (I_{SINK}) (½-Digit)	$V_{CC} = 5V$, $V_{OUT} = 5V$ $T_A = 25°C$	2.8	5.0		mA

AC Electrical Characteristics $T_j = 25°C$, $C_L = 50$ pF, unless otherwise specified.

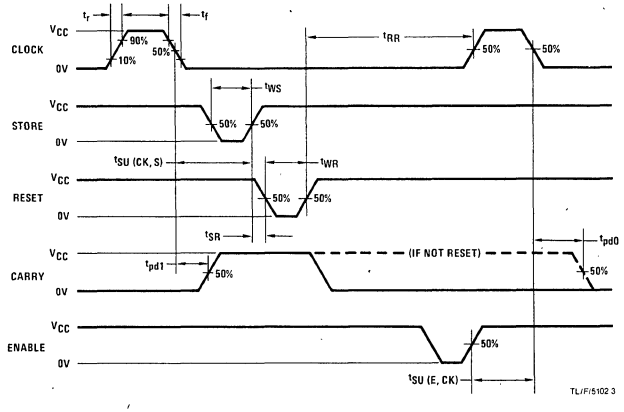
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Clock to Carry	$V_{CC} = 5.0V$		375	600	ns
f_{CLK}	Maximum Clock Frequency	$V_{CC} = 5.0V$	2	3		MHz
t_r, t_f	Clock Input Rise or Fall Time	$V_{CC} = 5.0V$			No Limit	
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$	180	120		ns
t_{WS}	Store Pulse Width	$V_{CC} = 5.0V$	150	80		ns
$t_{SU(CK, S)}$	Clock to Store Set-Up Time	$V_{CC} = 5.0V$	500	270		ns
t_{SR}	Store to Reset Wait Time	$V_{CC} = 5.0V$	280	170		ns
$t_{SU(E, CK)}$	Enable to Clock Set-Up Time	$V_{CC} = 5.0V$	140	80		ns
t_{RR}	Reset Removal	$V_{CC} = 5.0V$	50	0		ns
f_{BP}	Backplane Output Frequency	Pin 36 Floating, $V_{CC} = 5V$		85		Hz
C_{IN}	Input Capacitance	Logic Inputs (Note 5)		5		pF
t_{rfs}	Segment Rise/Fall Time	$C_{load} = 200$ pF		0.5		μs
t_{rfb}	Backplane Rise/Fall Time	$C_{load} = 5000$ pF		1.5		μs
f_{osc}	Oscillator Frequency	Pin 36 Floating, $V_{CC} = 5V$		11		kHz

Note 5: Does not apply to backplane and oscillator pins.

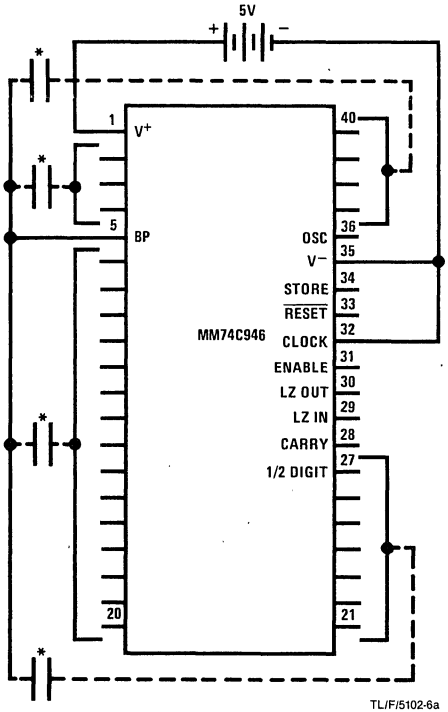
Block Diagram



AC Waveforms



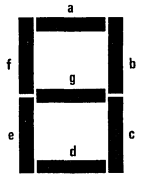
Test Circuit



TL/F/5102-6a

* Each segment to backplane with 200 pF capacitor.

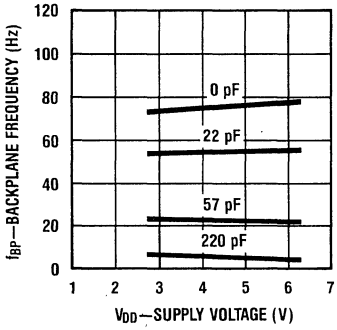
Segment Identification



TL/F/5102-6b

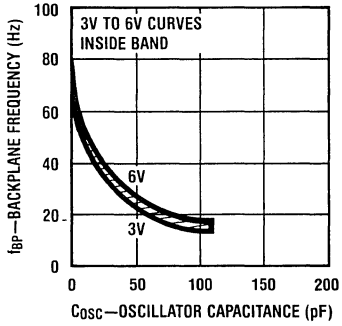
Typical Characteristics

Backplane Frequency as a Function of Supply Voltage



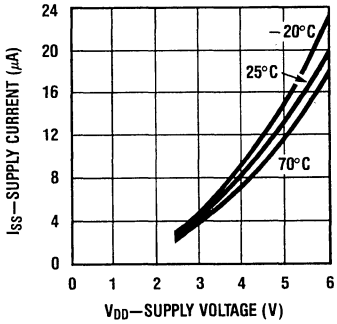
TL/F/5102-7

Backplane Frequency as a Function of Oscillator Capacitor (C_{OSC})



TL/F/5102-8

Operating Supply Current (I_{SS}) as a Function of Supply Voltage (V_{DD})



TL/F/5102-9

Control Pin Description

Backplane In/Out—When the oscillator pin is grounded this pin is an input allowing an external device to generate the backplane waveform. When the oscillator pin is left open this pin is an output supplying backplane drive for an LCD.

Oscillator—The oscillator frequency may be lowered by tying a capacitor (C_{OSC}) between this pin and ground. If this pin is grounded the backplane pin becomes an input.

Store Input—This controls the latches. When low, the latches are in flow-through mode (latch outputs follow counter), but when taken high data on counter outputs is stored in latches and displayed.

$\overline{\text{Reset}}$ Input—When low, counters are reset to zero.

Clock Input—Advances counter on negative edge.

Enable Input—When low, halts counter operation.

Leading Zero Input (LZI)—When high, enables leading zero blanking.

Leading Zero Output (LZO)—This signal goes high when counter equals zero and LZI is high.

Carry Output—Goes high for one clock period when count of 9999 is reached.

A1-G1—Digit 1 segment outputs.

A2-G2—Digit 2 segment outputs.

A3-G3—Digit 3 segment outputs.

A4-G4—Digit 4 segment outputs.

½-Digit Output—Goes high when count goes from 9999 to 0000 and stays high until $\overline{\text{Reset}}$ goes low.

Application Hints

Counter Circuitry Description

The MM74C946 contains a 4-digit resettable synchronous counter with a Schmitt trigger on the clock input. An additional D flip-flop clocked by the counter carry out provides a true ½-digit, or it can be used to indicate an overflow condition. The counters increment on the negative clock edge. The ½-digit sets on the negative clock edge which increments the counter past 9999. It can be reset only when the counter is reset by taking the reset pin to ground. The counter and carry output operation is independent of the state of the ½-digit flip-flop.

The carry output goes high on the negative edge of the clock when the transition from 9998 to 9999 occurs and then goes low on the next count. Thus counters may be cascaded in a ripple carry mode or synchronous mode by using the enable input.

The counter can be inhibited from responding to clock input pulses by taking the enable input low, thus freezing the counter to its state prior to the event.

The counter outputs feed a series of flow-through latches. When the store input is low, the latch outputs follow their inputs. When the store input is taken high, the contents of the counter are stored in the latches and are displayed.

The latch outputs feed 4 BCD to 7-segment decoders which include circuitry to provide leading zero blanking. When the leading zero input is low or the ½-digit is set, leading zero blanking is inhibited. When the leading zero input is high, all leading zeroes will be blanked. A leading zero output is provided to allow correct blanking of all leading zeroes in multiple device designs. This output will be high when all 4 digits are blanked. (Remember the leading zero input must be high and the ½-digit must be reset.)

Display Circuitry Description

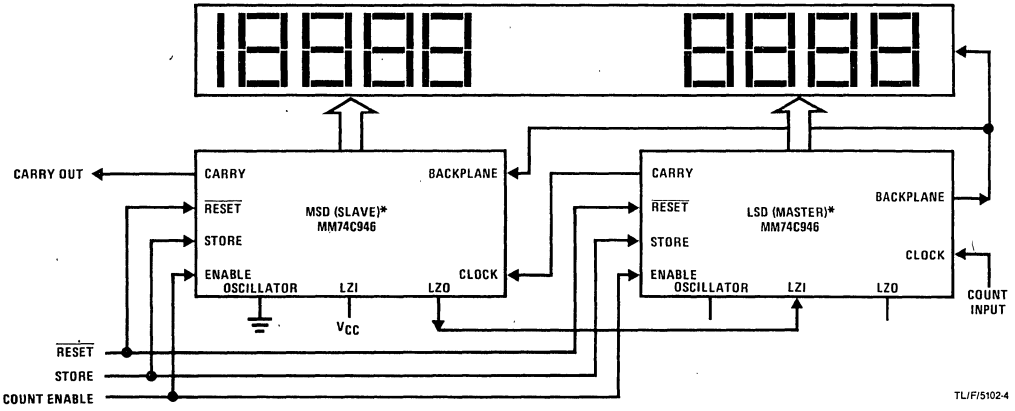
The MM74C946 has 29 segment outputs capable of directly driving 4 digits of 7 segments plus an additional ½-digit of 2 segments. The segment and backplane drivers are designed to provide matched rise and fall times eliminating possible DC components in the driving waveforms which could degrade display life (i.e., DC offset voltage).

The backplane driver can be disabled by grounding the oscillator pin. This enables the segment output waveforms to be synchronized to an external signal applied to the backplane pin. This allows several devices to be driven by a single master backplane waveform which can be generated by another MM74C946 or an external oscillator. Thus single backplane displays with 8, 12, 16, etc. digits can be driven by multiple counters. The maximum fanout of a master backplane driver is limited by its total capacitive load which is the sum of the slaved backplane input capacitances and the display backplane capacitance.

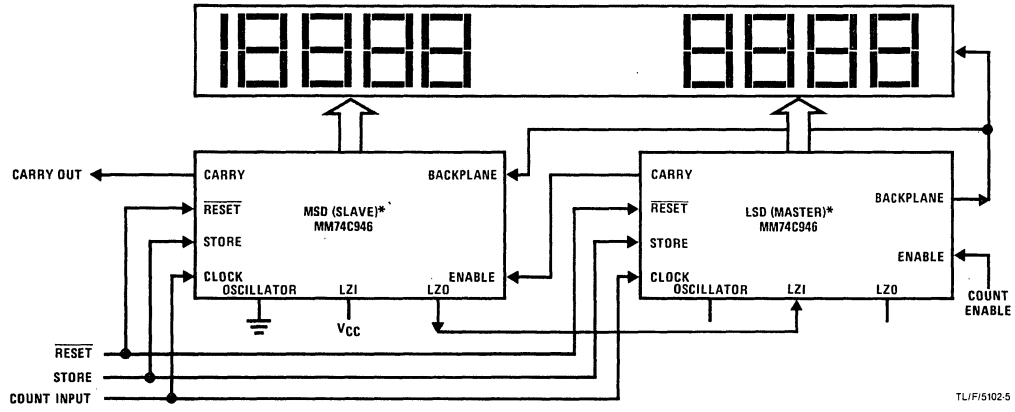
An on-board oscillator/divider generates the segment/backplane waveforms. Its output frequency typically is 85 Hz, but may be slowed by connecting an external capacitor between the oscillator pin and ground. The oscillator pin may also be driven by an external waveform but the input low level must not go to ground or else the backplane will be put in the slave mode (see $V_{IH\,(OSC)}$ and $V_{IL\,(OSC)}$ specifications).

Typical Applications

Ripple Carry Cascading



Synchronous Cascading



*Master/slave selection is arbitrary and dependent only on which oscillator pin is grounded.

National Semiconductor

MM74C956 4-Digit, 17-Segment Alpha-Numeric Display Driver, with Memory, Decoder, and LED Drivers

General Description

The MM74C956 monolithic LED intelligent display driver circuit is manufactured using standard complementary MOS technology. The convention and speed of the data entry procedure is designed to be microprocessor bus and TTL compatible with no interface circuitry required.

The integrated circuit has memory to store four 7-bit ASCII words corresponding to the four digits, an ASCII to 17-segment alpha-numeric ROM decoder, multiplexing and drive circuitry to drive four 17-segment digits. It has direct drive capabilities of 2.5 mA/segment average current.

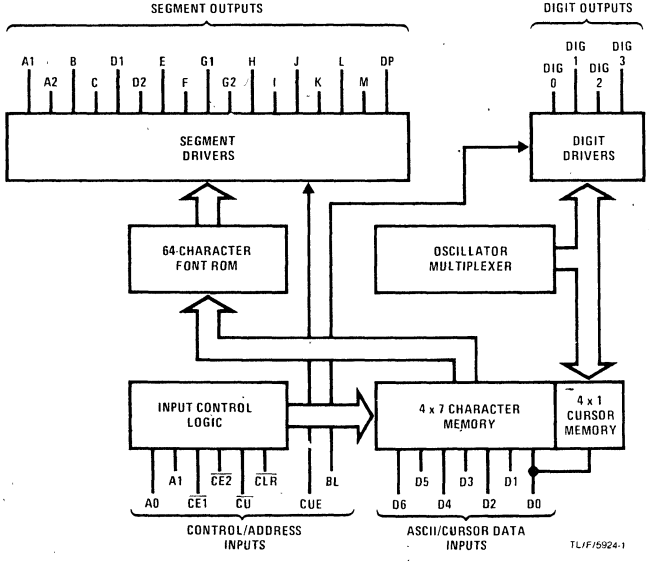
The internal memory can be written asynchronously through the 7-bit data bus (D0–D6) into the digit location addressed by the 2-bit address bus (A0, A1). For multiple chip circuits, two chip select inputs ($\overline{CE1}$, $\overline{CE2}$) can be decoded or a one-of-n decoder can be used for displays incorporating more than four MM74C956's.

The cursor function will cause all segments of a digit to be lit but will not write over the contents of the memory corresponding to that digit. Therefore, when the cursor is erased, the original character will reappear at that digit location.

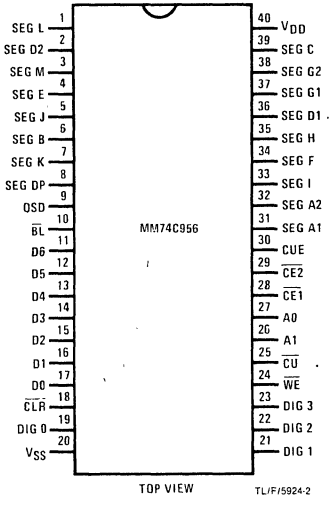
Features

- Microprocessor bus compatible
- All inputs are TTL compatible; 5V power supply
- On-chip memory
- On-chip decoder converts from standard 7-bit ASCII to alpha-numeric
- On-chip multiplexing with LED segment and digit drivers
- Independent and asynchronous digit access
- Independent cursor function: can be disabled
- Display clear function
- Display blank function
- Two chip select inputs for multiple chip systems

Block and Connection Diagrams

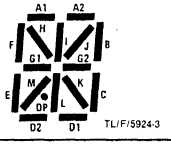


Dual-In-Line Package



Order Number MM74C956N
See NS Package N40A

Segment Designation



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC}+0.3V$	Package Dissipation	700 mW
Operating Temperature Range		Operating V_{CC} Range	4.5V to 5.5V
MM74C956	$-40°C$ to $+85°C$	V_{CC}	6.0V
Storage Temperature Range	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $T_A = 25°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5.0V$	2.4			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 5.0V$			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5V$, $V_{IN} = 5V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5V$, $V_{IN} = 0V$	-100.0	25.0		μA
I_{CC}	Supply Current	$V_{CC} = 5V$ @ $T_A = 25°C$ All Outputs Open All Inputs @ 5V		0.5	1.0	mA
OUTPUT DRIVE (Notes 2 and 3)						
Peak Output Source Current (I_{SOURCE}) (P-Channel Segment Driver with 1 Segment On)		$V_{CC} = 5.0V$, $V_{OUT} = 1.9V$ $T_A = 25°C$			14.8	mA
Peak Output Source Current (I_{SOURCE}) (P-Channel Segment Driver with 17 Segments On)		$V_{CC} = 10V$, $V_{OUT} = 3.3V$ $T_A = 25°C$	4.2			mA
Peak Output Sink Current (I_{SINK}) (N-Channel Digit Driver with 3 Segments On)		$V_{CC} = 5.0V$, $V_{OUT} = 0.25V$ $T_A = 25°C$	18.5			mA
Peak Output Sink Current (I_{SINK}) (N-Channel Digit Driver with 17 Segments On)		$V_{CC} = 10V$, $V_{OUT} = 1.3V$ $T_A = 25°C$			172.0	mA

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$

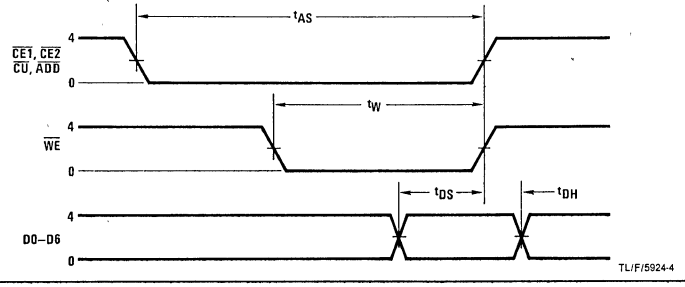
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_W	Write Pulse Width	All Inputs Swing from 0V–4V	240			ns
t_{DS}	Data Set-Up Time	All Inputs Swing from 0V–4V	100			ns
t_{DH}	Data Hold Time	All Inputs Swing from 0V–4V	50			ns
t_{AS}	Address Set-Up Time	All Inputs Swing from 0V–4V	300			ns
t_{AH}	Address Hold Time	All Inputs Swing from 0V–4V	0			ns
t_{CLR}	Clear Time	All Inputs Swing from 0V–4V	1			μs

Note 1: Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. Except for Operating Range they are not meant to imply that the devices should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

Note 2: Average drive current ≈ peak drive current ÷ 4.

Note 3: Current/segment is dependent upon total number of segments on. Maximum current occurs with 1 segment on; minimum current occurs with 17 segments on.

Timing Diagram for data access



TL/F/5924-4

Functional Description

Entry into Data Memory

To enter an ASCII code, the $\overline{CE1}$ and $\overline{CE2}$ inputs must be low, $\overline{CU}$ must be high. When the address is set up at A0 and A1, the $\overline{WE}$ can go low, at which time the internal RAM will respond to the data inputs (D0–D6). Note that the data need not be set up prior to the $\overline{WE}$ transition.

All digits can be cleared by holding the $\overline{CLR}$ input low for the specified interval.

Entry into Cursor Memory

This is accomplished by setting the $\overline{CE1}$ and $\overline{CE2}$ inputs as well as the $\overline{CU}$ input low. The cursor memory consists of 4 bits corresponding to the four digits, each one addressable by way of the A0 and A1 inputs. Once the address is stable, the $\overline{WE}$ input must go low and the cursor memory will respond to the D0 input. That is, if D0 is high, a cursor will be written and if D0 is low, the cursor will be erased. $\overline{CLR}$ will not erase a cursor. A cursor will only be displayed when CUE is high and the cursor function can be bypassed by tying CUE low. A flashing cursor can be implemented by pulsing CUE; this results in alternately displaying the cursor and the character originally written in that digit. CUE will not alter the contents of either the cursor or data memory.

Blanking the Display

Display blanking can be realized by using the $\overline{BL}$ input. By taking $\overline{BL}$ low, the display will be disabled while leaving the contents of the data and cursor memory unchanged. A flashing display will occur if $\overline{BL}$ is pulsed. The display is blanked by $\overline{BL}$ regardless of whether a cursor or character is being displayed.

Illegal Code

If an illegal ASCII code is entered into the data memory (*i.e.*, D6 = D5) the display will automatically be blanked for the corresponding digit.

OSD Pin

Taking the OSD pin high disables the internal oscillator and prohibits normal multiplex scanning. This pin is pulled low internally and is primarily meant to be used in testing the part only. This pin should be grounded or left open in normal operation.

Clearing the Display

Pulsing the $\overline{CLR}$ pin low for the specified time will clear all internal data memories while leaving the cursor memories unchanged.

TABLE I. DATA AND CURSOR ENTRY FUNCTION EXAMPLE

Assume initially D6 = 1 and D5 – D0 = 0 for all internal digit memories. Cursor memory is cleared. Table is intended to be read in sequence.

	$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A1	A0	D6	D5	D4	D3	D2	D1	D0	DIG 3	DIG 2	DIG 1	DIG 0
DATA ENTRY FUNCTION	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X				
	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X				
	1	0	1	X	X	X	1	X	X	X	X	X	X	X	X	X				
	1	0	0	X	X	1	1	X	X	X	X	X	X	X	X	X				
	1	0	0	X	1	0	1	0	0	1	0	0	0	1	1	1				
	1	0	0	X	1	0	1	1	0	0	1	1	0	1	0	0				
	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X				
	1	0	0	X	1	0	1	0	0	1	0	0	0	0	0	1				
	1	0	0	X	1	0	1	0	1	1	0	0	0	0	1	0				
	1	0	0	X	1	0	1	1	0	1	0	0	0	0	1	1				
	1	0	0	X	1	0	1	1	1	1	0	0	0	1	0	0				
CURSOR ENTRY FUNCTION	1	0	0	1	0	0	1	0	0	X	X	X	X	X	X	1				
	1	0	0	1	0	0	1	0	1	X	X	X	X	X	X	1				
	1	0	0	1	0	0	1	1	1	X	X	X	X	X	X	1				
	1	0	0	1	0	0	1	1	0	X	X	X	X	X	X	1				
	1	X	X	0	1	1	1	X	X	X	X	X	X	X	X	X				
	1	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X				
	1	0	0	1	0	0	1	0	0	X	X	X	X	X	X	0				
	1	0	0	0	0	0	1	1	0	X	X	X	X	X	X	0				
	1	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X				
	0	X	X	X	1	1	1	X	X	X	X	X	X	X	X	X				
	1	X	X	1	1	1	1	X	X	X	X	X	X	X	X	X				
	1	X	X	1	1	X	0	X	X	X	X	X	X	X	X	X				
	1	0	0	1	0	0	1	1	1	X	X	X	X	X	X	0				
	1	0	0	1	0	0	1	0	1	X	X	X	X	X	X	0				

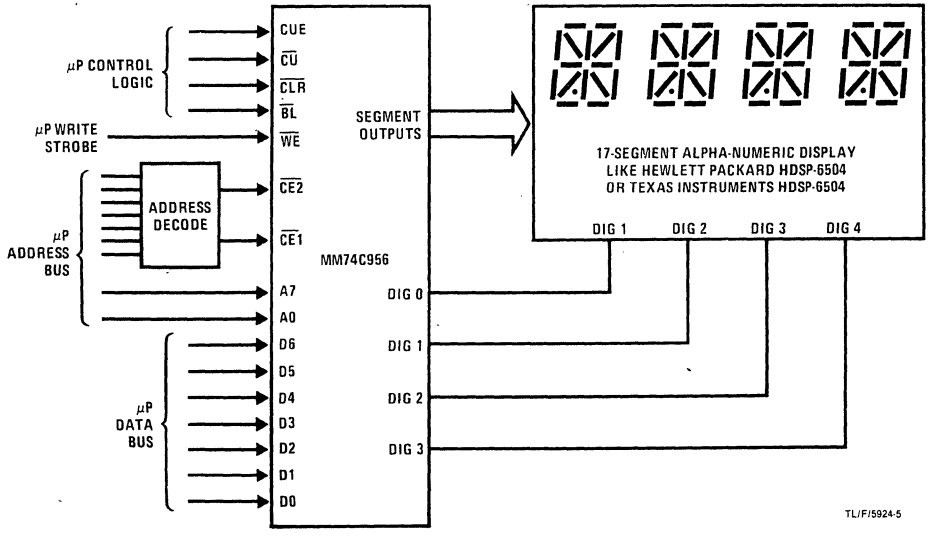
X = don't care

Functional Description (Continued)

TABLE II. ROM OUTPUT FONT FOR ASCII TO ALPHA-NUMERIC DECODING

Character Set				D0	L	H	L	H	L	H	L	H
				D1	L	L	H	H	L	L	H	H
				D2	L	L	L	L	H	H	H	H
D6	D5	D4	D3									
L	H	L	L									
L	H	L	H									
L	H	H	L									
L	H	H	H									
H	L	L	L									
H	L	L	H									
H	L	H	L									
H	L	H	H									

Typical Application



National Semiconductor

MM78C29/MM88C29 Quad Single-Ended Line Driver
MM78C30/MM88C30 Dual Differential Line Driver

General Description

The MM78C30/MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry of the MM78C30/MM88C30 allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM78C30 line driver. The differential output of the MM78C30/MM88C30 eliminates ground-loop errors.

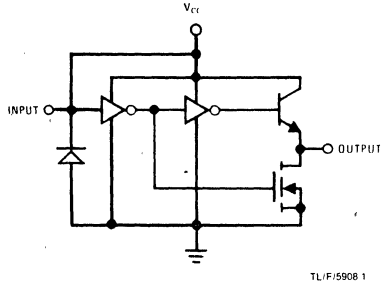
The MM78C29/MM88C29 is a non-inverting single-wire transmission line driver. Since the output ON resistance is a low 20Ω typ., the device can be used to drive lamps, relays, solenoids, and clock lines, besides driving data lines.

Features

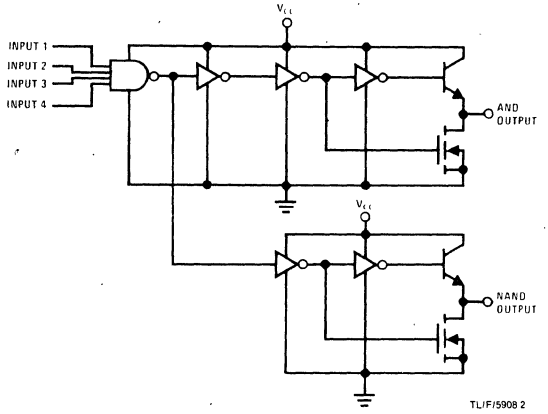
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} (typ.)
- Low output ON resistance 20Ω (typ.)

Logic and Connection Diagrams

1/4 MM78C29/MM88C29

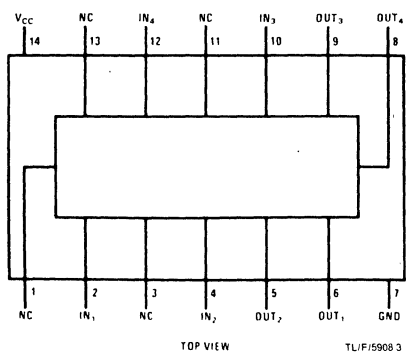


1/2 MM78C30/MM88C30



Dual-In-Line Package

MM78C29/MM88C29

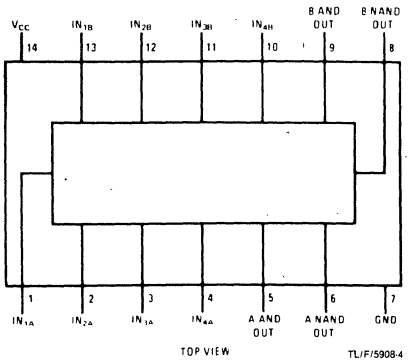


Order Number MM78C29J or MM88C29J
See NS Package J14A

Order Number MM78C29N or MM88C29N
See NS Package N14A

Dual-In-Line Package

MM78C30/MM88C30



Order Number MM78C30J or MM88C30J
See NS Package J14A

Order Number MM78C30N or MM88C30N
See NS Package N14A

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin (Note 1)	$-0.3\,V$ to $V_{CC}+16\,V$	Absolute Maximum V_{CC}	18 V
Operating Temperature Range		Average Current at Output	
MM78C29/MM78C30	−55°C to +125°C	MM78C30/MM88C30	50 mA
MM88C29/MM88C30	−40°C to +85°C	MM78C29/MM88C29	25 mA
Storage Temperature	−65°C to +150°C	Maximum Junction Temperature, T_j	150°C
Package Dissipation	500 mW	Lead Temperature (Soldering, 10 sec.)	300°C
Operating V_{CC} Range	3.0 V to 15 V		

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted

Sym	Parameter	Conditions	Min	Typ	Max	Units
CMOS to CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$	3.5 8.0			V V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5.0\,V$ $V_{CC}=10\,V$			1.5 2.0	V V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC}=15\,V$, $V_{IN}=15\,V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC}=15\,V$, $V_{IN}=0\,V$	−1.0	−0.005		μA
I_{CC}	Supply Current	$V_{CC}=15\,V$		0.05	100	μA
Output Drive						
	Output Source Current MM78C29/MM78C30	$V_{OUT}=V_{CC}-1.6\,V$, $V_{CC}\geq 4.5\,V$, $T_j=25°C$ $T_j=125°C$	 −57 −32	 −80 −50		 mA mA
	MM88C29/MM88C30	$V_{OUT}=V_{CC}-1.6\,V$, $V_{CC}\geq 4.75\,V$, $T_j=25°C$ $T_j=85°C$	 −47 −32	 −80 −60		 mA mA
	MM78C29/MM88C29 MM78C30/MM88C30	$V_{OUT}=V_{CC}-0.8\,V$ $V_{CC}\geq 4.5\,V$	 −2.0	 −20		 mA
	Output Sink Current MM78C29/MM78C30	$V_{OUT}=0.4\,V$, $V_{CC}=4.50\,V$, $T_j=25°C$ $T_j=125°C$	 11 8.0	 20 14		 mA mA
		$V_{OUT}=0.4\,V$, $V_{CC}=10\,V$, $T_j=25°C$ $T_j=125°C$	 22 16	 40 28		 mA mA
	MM88C29/MM88C30	$V_{OUT}=0.4\,V$, $V_{CC}=4.75\,V$, $T_j=25°C$ $T_j=85°C$	 9.5 8.0	 22 18		 mA mA
		$V_{OUT}=0.4\,V$, $V_{CC}=10\,V$, $T_j=25°C$ $T_j=125°C$	 19 15.5	 40 33		 mA mA
	Output Source Resistance MM78C29/MM78C30	$V_{OUT}=V_{CC}-1.6\,V$, $V_{CC}\geq 4.5\,V$, $T_j=25°C$ $T_j=125°C$		 20 32	 28 50	 Ω Ω
	MM88C29/MM88C30	$V_{OUT}=V_{CC}-1.6\,V$, $V_{CC}\geq 4.75\,V$, $T_j=25°C$ $T_j=85°C$		 20 27	 34 50	 Ω Ω

6

DC Electrical Characteristics (cont'd)

Min/max limits apply across temperature range, unless otherwise noted.

Sym	Parameter	Conditions	Min	Typ	Max	Units
	Output Sink Resistance					
	MM78C29/MM78C30	$V_{OUT} = 0.4\,V$, $V_{CC} = 4.50\,V$,				
		$T_j = 25°C$		20	36	Ω
		$T_j = 125°C$		28	50	Ω
		$V_{OUT} = 0.4\,V$, $V_{CC} = 10\,V$,				
		$T_j = 25°C$		10	18	Ω
		$T_j = 125°C$		14	25	Ω
	MM88C29/MM88C30	$V_{OUT} = 0.4\,V$, $V_{CC} = 4.75\,V$,				
		$T_j = 25°C$		18	41	Ω
		$T_j = 85°C$		22	50	Ω
		$V_{OUT} = 0.4\,V$, $V_{CC} = 10\,V$,				
		$T_j = 25°C$		10	21	Ω
		$T_j = 85°C$		12	26	Ω
	Output Resistance Temperature Coefficient					
	Source			0.55		%/°C
	Sink			0.40		%/°C
θ_{JA}	Thermal Resistance					
	MM78C29/MM78C30					
	(D-Package)			100		°C/W
	MM88C29/MM88C30					
	(N-Package)			150		°C/W

AC Electrical Characteristics $T_A = 25°C$, $C_L = 50\,pF$

Sym	Parameter	Conditions	Min	Typ	Max	Units
t_{pd}	Propagation Delay Time to Logical "1" or "0"	*(See Figure 2)*				
	MM78C29/MM88C29	$V_{CC} = 5.0\,V$		80	200	ns
		$V_{CC} = 10\,V$		35	100	ns
	MM78C30/MM88C30	$V_{CC} = 5.0\,V$		110	350	ns
		$V_{CC} = 10\,V$		50	150	ns
t_{pd}	Differential Propagation Delay Time to Logical "1" or "0"	$R_L = 100\,\Omega$, $C_L = 5000\,pF$ *(See Figure 1)*				
	MM78C30/MM88C30	$V_{CC} = 5.0\,V$			400	ns
		$V_{CC} = 10\,V$			150	ns
C_{IN}	Input Capacitance					
	MM78C29/MM88C29	(Note 3)		5.0		pF
	MM78C30/MM88C30	(Note 3)		5.0		pF
C_{PD}	Power Dissipation Capacitance					
	MM78C29/MM88C29	(Note 3)		150		pF
	MM78C30/MM88C30	(Note 3)		200		pF

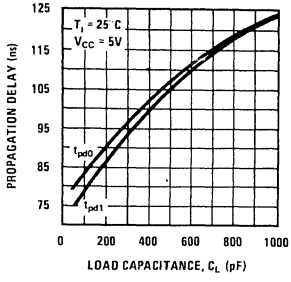
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note AN-90.

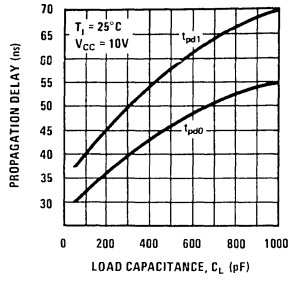
Typical Performance Characteristics

MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



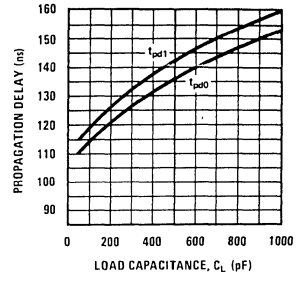
TL/F/5908-5

MM78C29/MM88C29
Typical Propagation Delay vs Load Capacitance



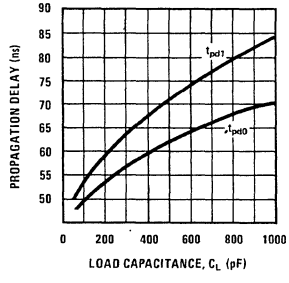
TL/F/5908-6

MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



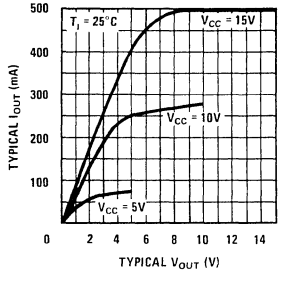
TL/F/5908-7

MM78C30/MM88C30
Typical Propagation Delay vs Load Capacitance



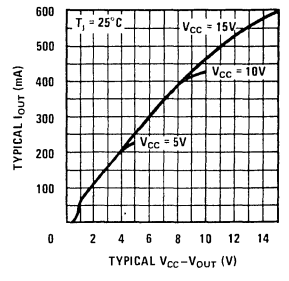
TL/F/5908-8

Typical Sink Current vs Output Voltage



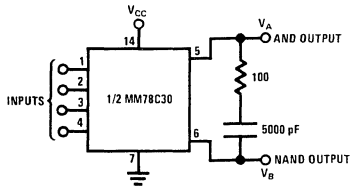
TL/F/5908-9

Typical Source Current vs Output Voltage

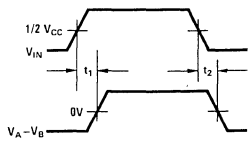


TL/F/5908-10

AC Test Circuits

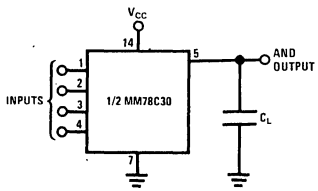


TL/F/5908-11

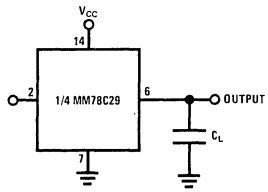


TL/F/5908-12

FIGURE 1



TL/F/5908-13

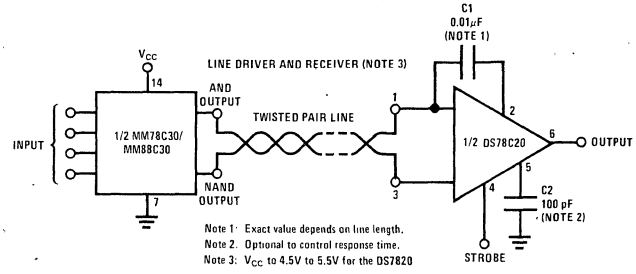


TL/F/5908-14

FIGURE 2

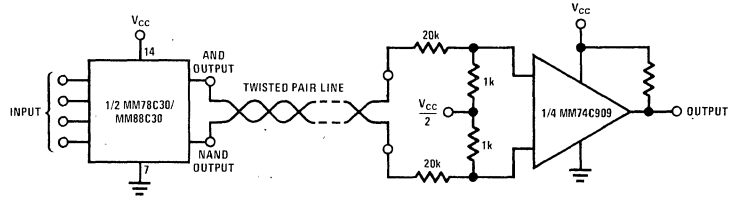
Typical Applications

Digital Data Transmission

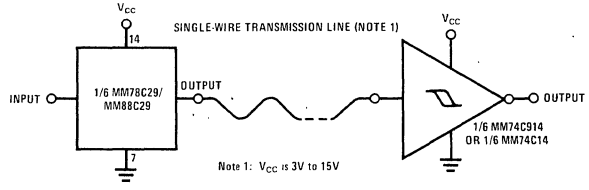


Note 1: Exact value depends on line length.
Note 2. Optional to control response time.
Note 3: V_{CC} to 4.5V to 5.5V for the DS7820

TL/F/5908-15



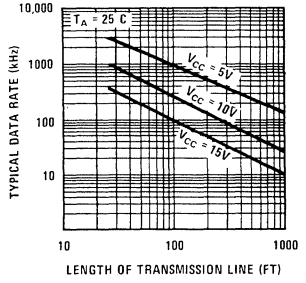
TL/F/5908-16



Note 1: V_{CC} is 3V to 15V

TL/F/5908-17

Typical Data Rate vs Transmission Line Length



Note 1: The transmission line used was #22 gauge unshielded twisted pair (40k termination).

Note 2: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.

TL/F/5908-18

Section 7

LSI/VLSI

7

Section Contents

National Semiconductor

MM5034, MM5035 Octal 80-Bit Static Shift Register

General Description

The MM5034 octal 80-bit shift register is a monolithic MOS integrated circuit utilizing N-channel low threshold enhancement mode and ion-implanted depletion mode devices.

The MM5034 is designed for use in computer display peripherals. All inputs and outputs are TTL compatible. The clocks and recirculate logic are internal to reduce system component count, and TRI-STATE® output buffers provide bus interface. Because of its N-channel characteristics, single 5V power supply operation is required.

Simple interface to the NSC CRT DP8350 controller and character generator to incorporate an entire CRT terminal is feasible with the MM5034.

The MM5034 is available in a 22-lead dual-in-line package.

The MM5035 is a 20-pin version of the MM5034 with the TRI-STATE output select feature omitted, for a simple data in/data out operation.

Features

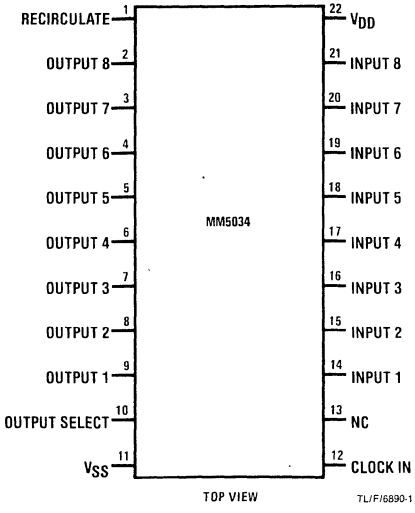
- Single 5V power supply
- Internal clocks
- High speed and static operation
- TRI-STATE output buffer
- Recirculate and output select independent
- TTL compatible

Applications

- CRT displays
- Computer peripherals

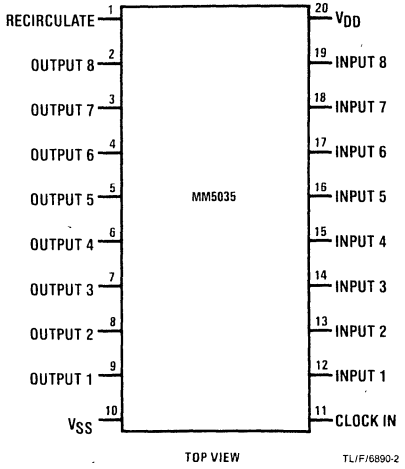
Connection Diagrams

Dual-in-Line-Package



Order Number MM5034N
See NS Package N22A

Dual-in-Line-Package



Order Number MM5035N
See NS Package N20A

7

Absolute Maximum Ratings

Supply Voltage	7 V_{DC}	Storage Temperature Range	−65°C to +150°C
Input Voltage	7 V_{DC}	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	750 mW		

Electrical Characteristics V_{DD} = 5V ±5%, T_A = 0°C to +70°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Input					
Logical "1" Input Voltage		2.2			V
Logical "0" Input Voltage				0.8	V
Data and Control Inputs					
Logical "1" Input Voltage		2.2			V
Logical "0" Input Voltage				0.8	V
Data, Clock and Control Inputs					
Logical "1" Input Current	V_{IN} = 5V			5.0	μA
Input Capacitance	V_{IN} = 2.5V		5.0	8.0	pF
Outputs					
Logical "1" Output Voltage	I_{OUT} = 100 μA	2.4	2.8		V
Logical "0" Output Voltage	I_{OUT} = 1.6 mA		0.25	0.4	V
TRI-STATE Output Current	V_{OUT} = 5V			−5.0	μA
	V_{OUT} = 0V			5.0	μA
Supply Current			60	90	mA
Timing					
Clock Frequency		0		3.0	MHz
Clock Pulse Width High	*(Figure 1)*	125		10,000	ns
Clock Pulse Width Low	(Note 1)	125		∞	ns
Output Rise and Fall Time (t_r, t_f)	*(Figure 1)*		40	50	ns
Set-Up Time	*(Figure 1)*	100			ns
Hold Time	*(Figure 1)*	0			ns
Output Enable Time	*(Figure 1)*			185	ns
Output Disable Time	*(Figure 1)*			185	ns
Clock Rise and Fall Time	*(Figure 1)*			5.0	μs
Output Delay, (t_{PD})			80	185	ns

Note 1: The clock input must be at a low level for DC storage. Minimum pulse width assumes 10 ns t_r and t_f.

Recirculate and TRI-STATE Operation

Recirculate is used to maintain data in the shift register after it has been loaded. While the shift register is being loaded, Recirculate must be at a logical "0". When the loading is completed, Recirculate should be brought to a logical "1". This disables the data input and feeds the output of the last shift cell back to the input of the first shift cell for each of the 8 registers.

For the output to be in the TRI-STATE mode output-select should be at the logical '1' level.

AC Test Circuits and Switching Time Waveforms

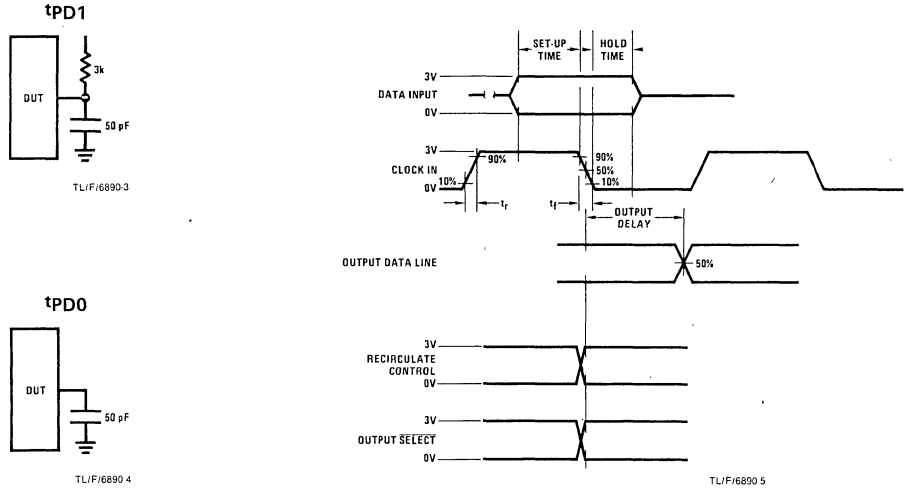


FIGURE 1

Typical Application

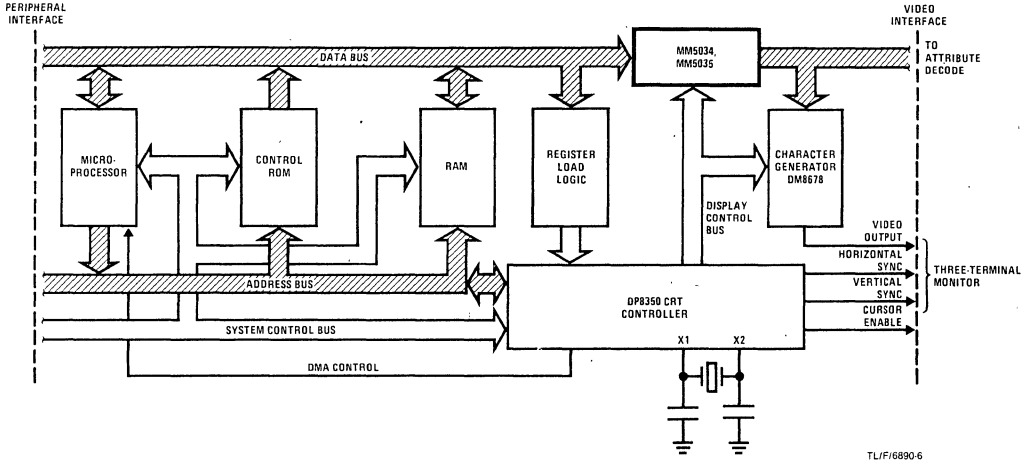


FIGURE 2. CRT System Diagram Using the MM5034, MM5035 as a Line Buffer with DMA

National Semiconductor

MM5307 Baud Rate Generator/Programmable Divider

General Description

The National Semiconductor MM5307 baud rate generator/programmable divider is a MOS/LSI P-channel enhancement mode device. A master clock for the device is generated either externally or by an on-chip crystal oscillator (Note 4). An internal ROM controls a divider circuit which produces the output frequency. Logic levels on the four control pins select between sixteen output frequencies. The frequencies are chosen from the following possible divisors: 2N, for $3 \leq N \leq 2048$; 2N + 1 and 2N + 0.5 for $4 \leq N \leq 2048$. Also one of the sixteen frequencies may be gated from the external frequency input. The MM5307AA is supplied with the divisors shown in the Control Table.

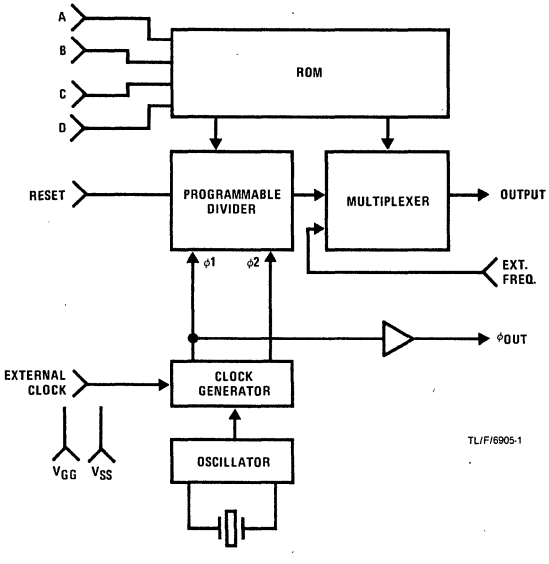
Features

- On-chip crystal oscillator
- Choice of 16 output frequencies from 1 crystal
- External frequency input pin
- Internal ROM allows generation of other frequencies on order
- Bipolar compatibility
- 0.01% accuracy (typ) exclusive of crystal
- 1 MHz master clock frequency

Applications

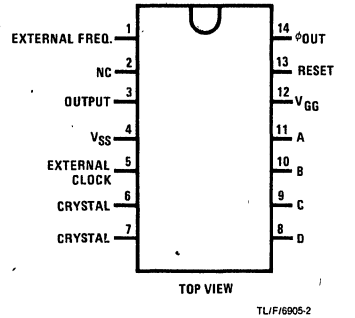
- UART clocks
- System clocks
- Electrically programmable counters

Schematic and Connection Diagrams



TL/F/6905-1

Dual-In-Line Package



TOP VIEW

TL/F/6905-2

Order Number MM5307N
See NS Package N14A

Absolute Maximum Ratings

Voltage at Any Pin With Respect to V_{SS}	+0.3V to V_{SS} − 20V	Operating Temperature	0°C to +70°C
Power Dissipation	700 mW	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics

T_A within operating range, V_{SS} = 5V ±5%, V_{GG} = −12V ±5%, unless otherwise specified.

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	All Inputs (Except Crystal Pins)					
V_{IH}	Logical High Level		V_{SS}−1.5		V_{SS}+0.3	V
V_{IL}	Logical Low Level		V_{SS}−18		V_{SS}−4.2	V
	Leakage	V_{IN} = −10V, T_A = 25°C, All Other Pins GND			0.5	μA
	Capacitance	V_{IN} = 0V, f = 1 MHz, All Other Pins GND, (Note 1)			7.0	pF
	External Clock Duty Cycle		40%		60%	
	Capacitance Measured Across Crystal Pins	f = 1 MHz, (Note 3)			5.0	pF
	Output Levels					
V_{OH}	Logical High Level	I_{SOURCE} = −0.5 mA	V_{SS}−2.6	V_{SS}		V
V_{OL}	Logical Low Level	I_{SINK} = 1.6 mA			V_{SS}−4.6	V
I_{GG}	Power Supply Current	f = 1 MHz			35	mA

AC Electrical Characteristics

T_A within operating range V_{SS} = 5V ±5%, V_{GG} = −12V ±5%, unless otherwise specified.

SYM	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Master Frequency		0.8		1.0	MHz
t_A	Access Time	C_L = 50 pF, (Note 2)			16	μs
t_{RD}	Reset Delay Time	f = Master Clock Frequency			500 + 4/f	ns
R_{PW}	Reset Pulse Width		500 + 4/f			ns
t_{OD}	Output Delay From Reset				500 + 4/f	ns
	Output Duty Cycle = 0.5T ± 1/f	T = Output Period f = Master Frequency	0.5T−1/f		0.5T+1/f	

Note 1: Capacitance is guaranteed by periodic measurement.

Note 2: Access time is defined as the time from a change in control inputs (A, B, C, D) to a stable output frequency. Access time is a function of frequency. The following formula may be used to calculate maximum access time for any master frequency: $T_A = 2.8\mu s + 1/f \times 13$, f is in MHz.

Note 3: The MM5307 is designed to operate with a 921.6 kHz parallel resonant crystal. When ordering the crystal a value of load capacitance (C_L) must be specified. This is the capacitance "seen" by the crystal when it is operating in the circuit. The value of C_L should match the capacitance measured at the crystal frequency across the crystal input pins on the MM5307. Any mismatch will be reflected as a very small error in the operating frequency. To achieve maximum accuracy, it may be necessary to add a small trimmer capacitor across the terminals.

Note 4: If the crystal oscillator is used Pin 5 (external clock) is connected to V_{SS}. If an external clock is used Pin 7 is connected to V_{SS}.

Control Table

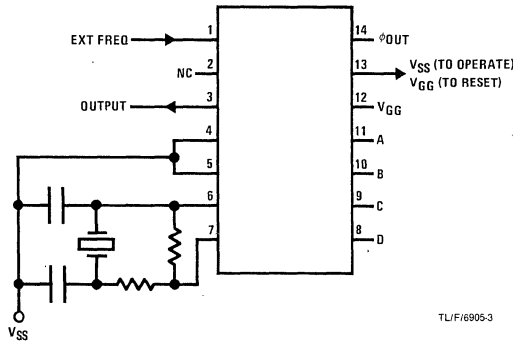
Input Freq: 921.6 kHz Master Clock

CONTROL PINS				NOMINAL BAUD RATES (OUTPUT FREQUENCY/16)			DIVISOR FOR AA
A	B	C	D	AA	AB	FAG	
0	0	0	1	50	50	50	1152
0	0	1	0	75	200	75	768
0	0	1	1	110	110	110	524
0	1	0	0	134.5	134.5	134.5	428.5
0	1	0	1	150	150	150	384
0	1	1	0	300	300	300	192
0	1	1	1	600	600	600	96
1	0	0	0	900	900	1050	64
1	0	0	1	1200	1200	1200	48
1	0	1	0	1800	1800	45.5	32
1	0	1	1	2400	2400	2400	24
1	1	0	0	3600	3600	56.9	16
1	1	0	1	4800	4800	4800	12
1	1	1	0	7200	75	66.7	8
1	1	1	1	9600	9600	9600	6
0	0	0	0	EXTERNAL FREQ			

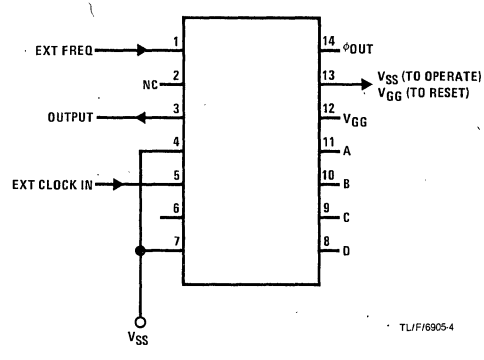
Positive Logic: $1 = V_H$
$0 \equiv V_L$

Typical Applications

Internal Oscillator



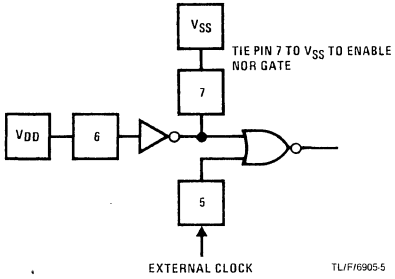
External Clock



Application Hints

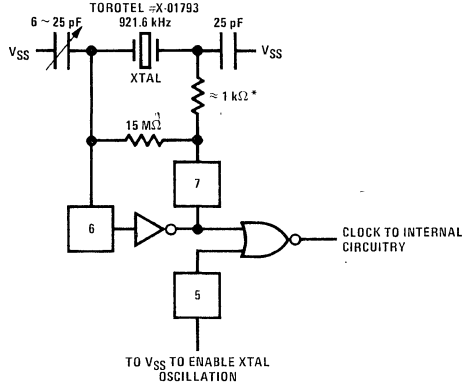
The external clock is brought in on pin 5 and pin 7 is tied to V_{SS} to enable the external clock input. Pin 6 can be left open; however, this may cause some current flow that can be eliminated by connecting pin 6 to V_{DD}.

1) To use the MM5307 with an external clock, hook it up as follows:



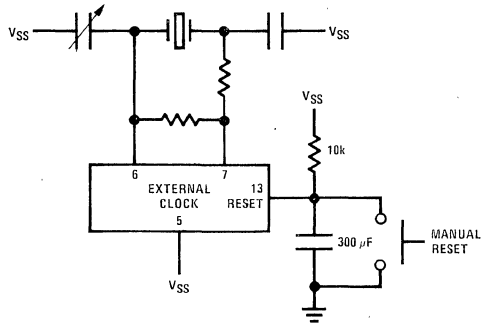
TL/F/6905-5

2) To use a crystal directly:



TL/F/6905-6

*Component values should be selected based on crystal used.



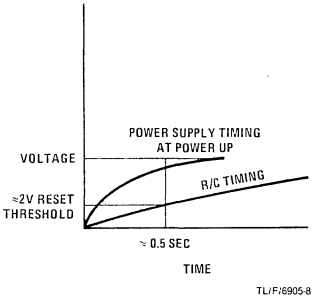
TL/F/6905-7

3) Reset (pin 13) must be at V_{SS} to operate. It may be necessary to take this to GND or V_{GG} to reset the ROM select circuit. An option is to tie ϕ out (pin 14) to external Freq In (pin 1), if not otherwise used.

4) An interesting application might use two MM5307's in series to generate additional frequencies, i.e., with one programmed from the 921.6 kHz to 800 Hz out, a second could divide that by 16 to give a 50 Hz crystal controlled signal.

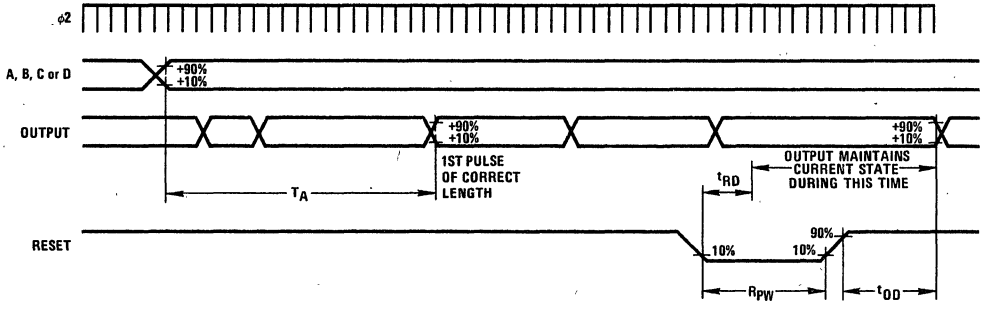
5) MM5307AA divisors are on the data sheet. AB divisors are the same as the AA except: 1) Code 0010 is divided by 288 → 32 kHz out, 200 baud; 2) Code 1110 is divided by 768 → 1.2 kHz, 75 baud.

The MM5307 does not always generate an output when the power is up, even though the oscillator seems to be operating properly. In order to eliminate this problem, it is necessary to reset the chip at power "ON". This can be done manually, with a reset signal by a host system, or automatically by using R/C timing elements. The reset is done internally, when program inputs change. When using an R/C combination for auto resetting, the time constant must be several times larger than that of the power supply. For example, most lab power supplies take at least 0.5 sec for the voltage to reach 90% of full level. A 10 kΩ resistor and 300 μF capacitor combination should be adequate for most applications.

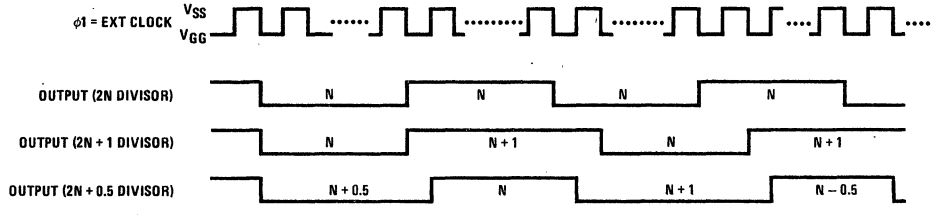


TL/F/6905-8

Timing Diagrams



TL/F/6905-9



TL/F/6905-10

National Semiconductor

MM5368 CMOS Oscillator Divider Circuit

General Description

The MM5368 is a CMOS integrated circuit generating 50 or 60 Hz, 10 Hz, and 1 Hz outputs from a 32 kHz crystal (32,768 Hz). For the 60 Hz selected output the input time base is divided by 546.133, for the 50 Hz mode it is divided by 655.36. The 50/60 Hz output is then divided by 5 or 6 to obtain a 10 Hz output which is further divided to obtain a 1 Hz output. The 50/60 Hz select input can be floated for a counter reset.

Features

- 50/60 Hz output
- 1 Hz output
- 10 Hz output
- Low power dissipation
- Fully static operation
- Counter reset
- 3V–15V supply range
- On-chip oscillator — tuning and load capacitors are the only required external components besides the crystal. (For operation below 5V it may be necessary to use an ~ 1MΩ pullup on the oscillator output to insure start-up.)

Block and Connection Diagrams

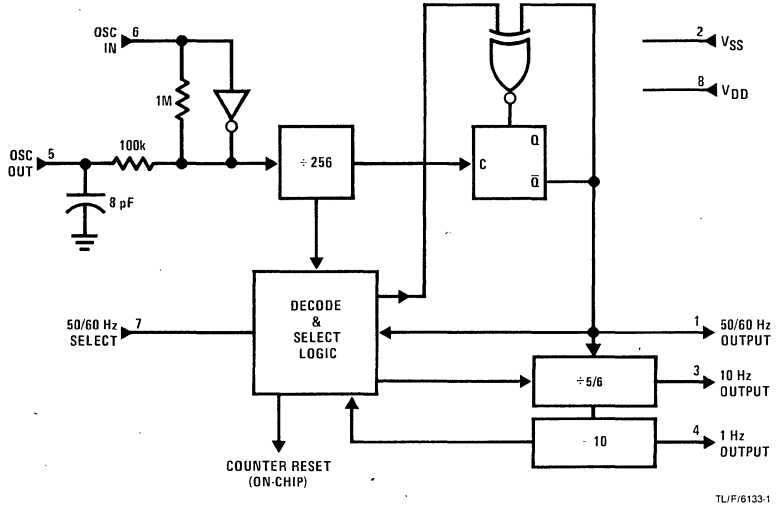
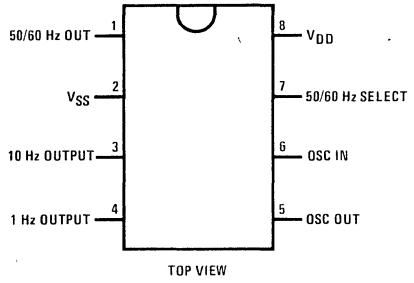


FIGURE 1

Dual-In-Line Package



Order Number MM5368N
See NS Package N08E

FIGURE 2

Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to $V_{DD} + 0.3V$	Maximum V_{DD} Voltage	16V
Operating Temperature	$0°C$ to $+70°C$	Operating V_{DD} Range	$3V \leq V_{DD} \leq 15V$
Storage Temperature	$-65°C$ to $+150°C$	Lead Temperature (Soldering, 10 seconds)	$300°C$

Electrical Characteristics T_A within operating range, $V_{SS} = 0V$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	$V_{DD} = 15V$; 50/60 Select Floating			10	μA
Operating Current Drain	$f_{IN} = 32$ kHz, $V_{DD} = 3V$			50	μA
	$f_{IN} = 32$ kHz, $V_{DD} = 15V$			1500	μA
Maximum Input Frequency	$V_{DD} = 3V$			64	kHz
	$V_{DD} = 15V$			500	kHz
Output Current Levels	$V_{DD} = 5V$				
Logical "1", Source	$V_{OH} = V_{SS} + 2.7V$			−400	μA
Logical "0", Sink	$V_{OL} = V_{SS} + 0.4V$	400			μA
	$V_{DD} = 9V$				
Logical "1", Source	$V_{OH} = V_{SS} + 6.7V$			−1500	μA
Logical "0", Sink	$V_{OL} = V_{SS} + 0.4V$	1500			μA
Input Current Levels	50/60 Select Input				
Logical "1" (I_{IH})	$V_{DD} = 3V$, $V_{IN} \geq 0.9V_{DD}$			50	μA
Logical "1" (I_{IH})	$V_{DD} = 15V$, $V_{IN} \geq 0.9V_{DD}$			3	mA
Logical "0" (I_{IL})	$V_{DD} = 3V$, $V_{IN} \leq 0.1V_{DD}$			20	μA
Logical "0" (I_{IL})	$V_{DD} = 15V$, $V_{IN} \leq 0.1V_{DD}$			1	mA

Functional Description *(Figure 1)*

The MM5368 initially divides the input time base by 256. From the resulting frequency (128 Hz for 32 kHz crystal) 8 clock periods are dropped or eliminated during 60 Hz operation and 28 clock periods are eliminated during 50 Hz operation. This frequency is then divided by 2 to obtain a 50 or 60 Hz output. This output is not periodic from cycle to cycle; however, the waveform repeats itself every second. Straight divide by 5 or 6 and 10 are used to obtain the 10 Hz output and the 1 Hz outputs.

The 60 Hz mode is obtained by tying pin 7 to V_{DD}. The 60 Hz output waveform can be seen in *Figure 3.* The 10 Hz and 1 Hz outputs have an approximate 50% duty cycle. In the 50 Hz mode the 50/60 select input is tied to V_{SS}. The 50 Hz output waveform can be seen in *Figure 3.* The 10 Hz output has an approximate 40% duty cycle and the 1 Hz output has an approximate 50% duty cycle.

For the 50/60 Hz select input floating, the counter chain is held reset, except for the initial toggle flip-flop which is needed for the reset function. A reset may also occur when the input is switched *(Figure 4).* To insure the floating state, current sourced from the input must be limited to 1.0 μA and current sunk by the input must be limited to 1.0 μA for $V_{DD} = 3V$.

Timing Diagrams

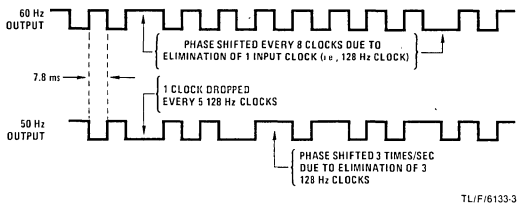


FIGURE 3. 50/60 Hz Output

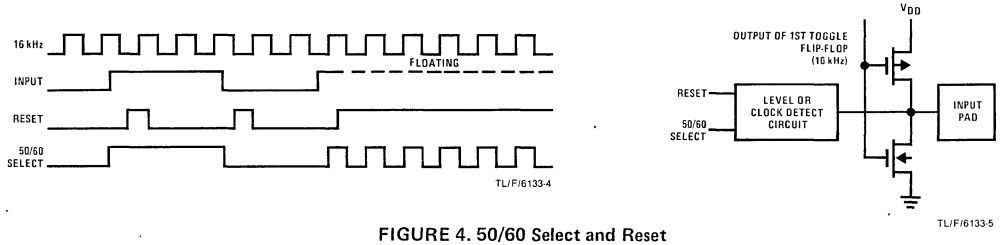
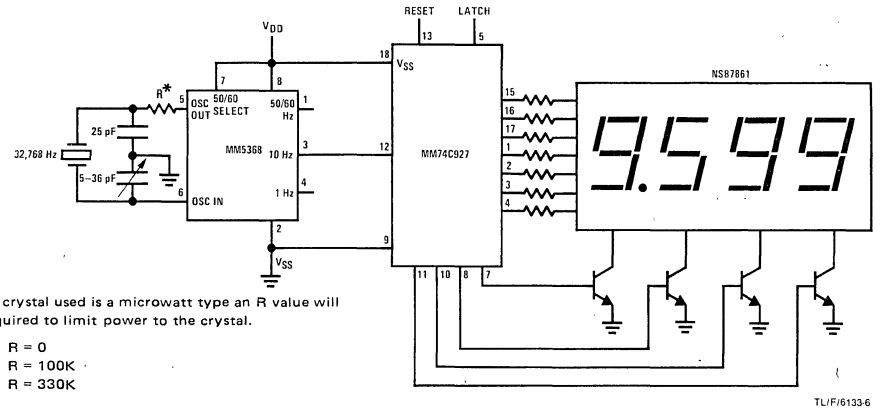


FIGURE 4. 50/60 Select and Reset

Typical Applications



*If the crystal used is a microwatt type an R value will be required to limit power to the crystal.

3V	R = 0
5V	R = 100K
10V	R = 330K

FIGURE 5. 10 Minute (9:59.9) Timer

National Semiconductor

MM5369 Series 17 Stage Oscillator/Divider

General Description

The MM5369 is a CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise reference from commonly available high frequency quartz crystals. An internal pulse is generated by mask programming the combinations of stages 1 through 4, 16 and 17 to set or reset the individual stages. The MM5369 is advanced one count on the positive transition of each clock pulse. Two buffered outputs are available: the crystal frequency for tuning purposes and the 17th stage output. The MM5369 is available in an 8-lead dual-in-line epoxy package.

Features

- Crystal oscillator
- Two buffered outputs
  - Output 1 crystal frequency
  - Output 2 full division
- High speed (4 MHz at V_{DD} = 10V)
- Wide supply range 3–15V
- Low power
- Fully static operation
- 8 lead dual-in-line package
- Low current

Options

■ MM5369AA	3.58 MHz to 60 Hz
■ MM5369EYR	3.58 MHz to 50 Hz
■ MM5369EST	3.58 MHz to 100 Hz

Connection and Block Diagrams

Dual-In-Line Package

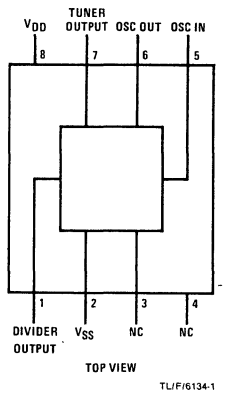


FIGURE 1

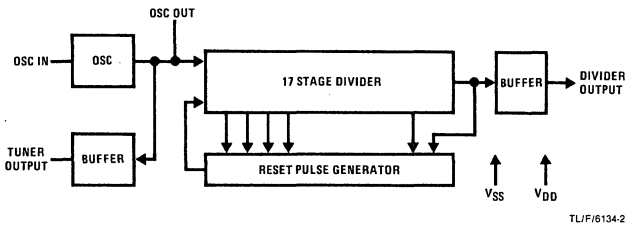


FIGURE 2

Order Number MM5369N
See NS Package N08E

Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to V_{DD} $+0.3V$	Maximum V_{CC} Voltage	16V
Operating Temperature	0°C to +70°C	Operating V_{CC} Range	3V to 15V
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	500 mW		

Electrical Characteristics

T_A within operating temperature range, V_{SS} = GND, $3V \leq V_{DD} \leq 15V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	V_{DD} = 15V			10	μA
Operating Current Drain	V_{DD} = 10V, f_{IN} = 4.19 MHz		1.2	2.5	mA
Frequency of Oscillation	V_{DD} = 10V	DC		4.5	MHz
	V_{DD} = 6V	DC		2	MHz
Output Current Levels	V_{DD} = 10V V_O = 5V				
Logical "1" Source		500			μA
Logical "0" Sink		500			μA
Output Voltage Levels	V_{DD} = 10V I_O = 10 μA				
Logical "1"		9.0			V
Logical "0"				1.0	V

Note: For 3.58 MHz operation, V_{DD} must be $\geq$ 10V.

Functional Description

A connection diagram for the MM5369 is shown in *Figure 1* and a block diagram is shown in *Figure 2*.

TIME BASE

A precision time base is provided by the interconnection of a 3,579,545 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the OSC IN and the OSC OUT terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

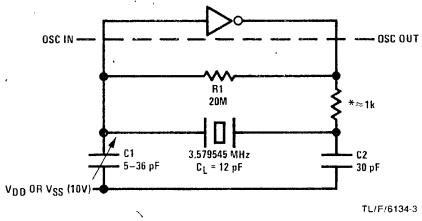
DIVIDER

A pulse is generated when divider stages 1 through 4, 16 and 17 are in the correct state. By mask options, this pulse is used to set or reset individual stages of the counter. *Figure 4* shows the relationship between the duty cycle and the programmed modulus.

OUTPUTS

The Tuner Output is a buffered output at the crystal oscillator frequency. This output is provided so that the crystal frequency can be obtained without disturbing the crystal oscillator. The Divide Output is the input frequency divided by the mask programmed number. Both outputs are push-pull outputs.

Functional Description (Continued)



*To be selected based on xtal used

FIGURE 3. Crystal Oscillator Network

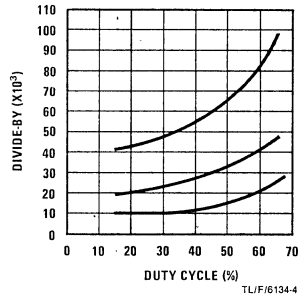


FIGURE 4. Plot of Divide-By vs Duty Cycle

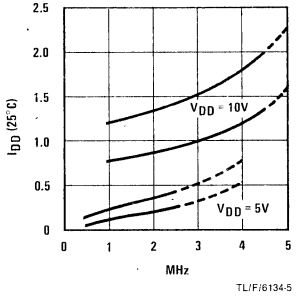


FIGURE 5. Typical Current Drain vs Oscillator Frequency

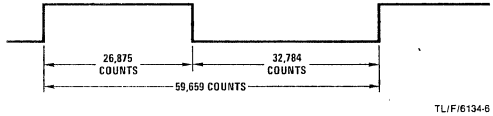


FIGURE 6. Output Waveform for Standard MM5369AA

National Semiconductor

MM53107 Series 17-Stage Oscillator/Divider

General Description

The MM53107 is a low threshold voltage CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise reference from a 2.097152 MHz quartz crystal. An internal pulse is generated by the combinations of stages 1–4, 16 and 17 to set or reset the individual stages. The MM53107 is advanced one count on the positive transition of each clock pulse. One buffered output is available: the 17th stage 60 Hz output. The MM53107 is available in an 8-lead dual-in-line epoxy package.

Features

- Input frequency—2.097152 MHz
- Output frequency—60Hz
- Crystal oscillator
- High speed (2 MHz at V_{DD} = 2.5V)
- Wide supply range 2.5V—6V
- Low power (0.5 mW @ 2 MHz/2.5V)
- Fully static operation
- 8-lead dual-in-line package

Block and Connection Diagrams

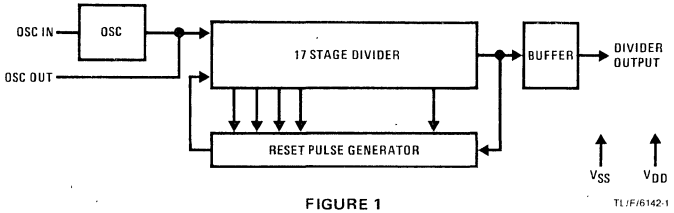
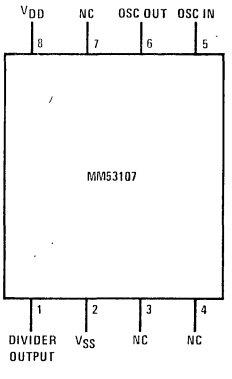


FIGURE 1

TL/F/6142-1

Dual-In-Line Package



TOP VIEW

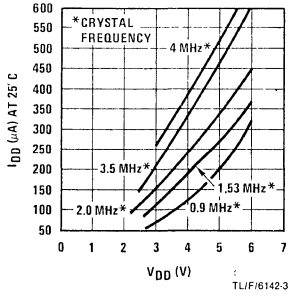
TL/F/6142-2

FIGURE 2

Order Number MM53107N
See NS Package N08E

Typical Performance Characteristics

Typical Current Drain vs Oscillator Frequency



TL/F/6142-3

Absolute Maximum Ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Maximum V_{CC} Voltage	7V
Operating Temperature	0°C to +70°C	Operating V_{CC} Range	2.5V to 6V
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	500 mW		

Electrical Characteristics

T_A within operating temperature range, V_{SS} = Gnd, 2.5V ≤ V_{DD} ≤ 6V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	V_{DD} = 6V			10	μA
Operating Current Drain	V_{DD} = 2.5V, f_{IN} = 2.1 MHz			200	μA
Frequency of Oscillation	V_{DD} = 2.4V	dc		2.1	MHz
	V_{DD} = 6V	dc		4.0	MHz
Output Current Levels					
Logical "1" Source	V_{DD} = 4V,	100			μA
Logical "0" Sink	V_{OUT} = 2V	100			μA
Output Voltage Levels					
Logical "1"	V_{DD} = 6V I_OSource = 10 μA	5.0			V
Logical "0"	I_OSink = −10 μA			1.0	V

Functional Description

A connection diagram for the MM53107 is shown in *Figure 2* and a block diagram is shown in *Figure 1.*

TIME BASE

A precision time base is provided by the interconnection of a 2,097,152 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the Osc In and the Osc Out terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

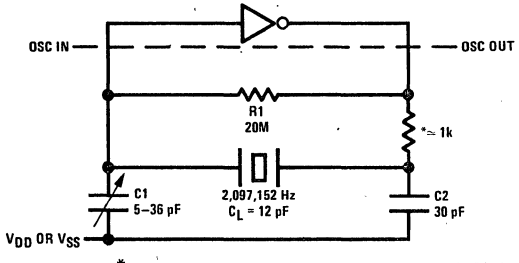
The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

DIVIDER

A pulse is generated when divider stages 1–4, 16 and 17 are in the correct state. This pulse is used to set or reset individual stages of the counter, the modulus of the counter is 34,952 to provide 60 Hz.

OUTPUT

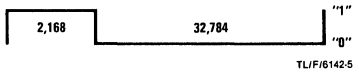
The Divide Output is the input frequency divided by 34,952. The output is a push-pull output.



*To be selected based on the crystal used

TL/F/6142-4

FIGURE 3. Crystal Oscillator Network



TL/F/6142-5

FIGURE 4. Duty Cycle for MM53107

National Semiconductor

MM53126 Infrared Remote Control Transmitter

General Description

The MM53126 is an infrared remote control transmitter circuit using low threshold N-channel enhancement and depletion devices. This versatile circuit is ideal for sophisticated TV/HiFi consumer applications. The transmission of information is achieved using bursts of pulse code modulated infrared light. Each burst consists of a fixed number of constant amplitude pulses with binary coded spaces. This system allows high pulse current drive to the transmitter diodes, and also high data integrity with noise immunity. The circuit features very low quiescent current drain guaranteeing long battery life.

Features

- 64 commands to 4 addresses
- Simple interface to Standby 9V battery
- 'One-Shot' word transmission capability
- Very low standby current — 10μA typical
- Pin compatible with ITT 1050/1250
- 0.1% IR drive ensures long battery life
- 6-bit data word, 2-bit address word
- Simple RC oscillator only requires 3 external components
- Keyswitch requirements allow use of low cost keyboard
- Simple interface to high current IR diodes
- Double key depression detection

Applications

- Remote control of TV
- Remote control of HiFi
- Remote machine control
- Remote ASCII keyboard
- Serial keyboard encoder

Block Diagram

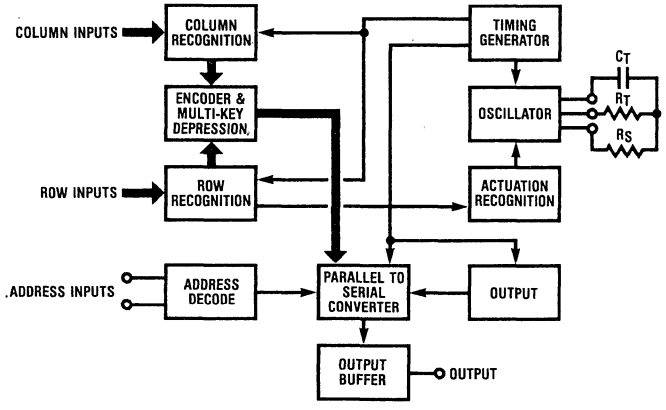


Figure 1

Absolute Maximum Ratings

Voltage at Any Pin	−0.5 to 12V
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering 10 seconds)	300°C

Electrical Characteristics

$T_A = 0°C$, $V_{SS} = 0V$, $V_{DD} = 6.5V$ to 7.5V, unless otherwise specified.

Sym	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		6.5		7.5	V
I_{DD}	Supply Current	$V_{DD} = 9V$ No key depressed		10	20	μA
		$V_{DD} = 7V$ Valid key depressed (See Figure 5)			10	mA
	Oscillator Frequency	$C_T = 47pF$ 2% $R_T = 33k$ 1% $R_S = 33k$ 5% (See Figure 5)	160		220	kHz
	Output Logic Levels					
	Serial Out Logic "0"	1 Sink = 0.2mA			0.2	V
	Logic "1"	1 Source = 0.2mA	1.0			V

Functional Description

The block diagram of the MM53126 is shown in Figure 1. A connection diagram is shown in Figure 2.

The MM53126 operates using a simple 8 × 8 keyboard giving 64 different commands. The two inputs FA and FB are address inputs which allow a total of 256 messages to be transmitted. These commands are transmitted using pulse position modulation. See Figure 4.

The row and column circuitry recognizes when a single row is connected to a single column and removes the reset from the circuit. This activates the oscillator whose frequency is determined by the external components C_T, R_T and R_S. If a row input is connected to a column input for greater than 40k clocks the message is transmitted using 14 pulses of data. For the period that the row is connected to the column the message is transmitted every 40k clocks.

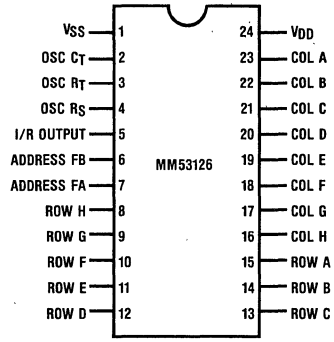
Releasing the Row-Column connection powers down the circuit to a standby condition of very low current consumption to conserve battery power. If the key contact is released during the transmission of a message, the circuit will complete the transmission before powering down.

The multi-key depression detection circuit inhibits the output if more than one key is depressed.

The encoder provides at the output, via the parallel to serial converter, one of 64 codes (see Table 1). One of four addresses may be selected (see Table 2) giving a total of 256 commands that may be transmitted.

Connection Diagram

Dual-In-Line Package



Top View

TL/F/6998-2

Figure 2

Order Number MM53126N
See NS Package N24A

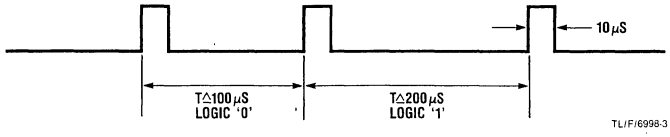
Typical Keyboard Specifications

R_{ON}	5k max
R_{OFF}	300k min

Format of Transmitted Signal:

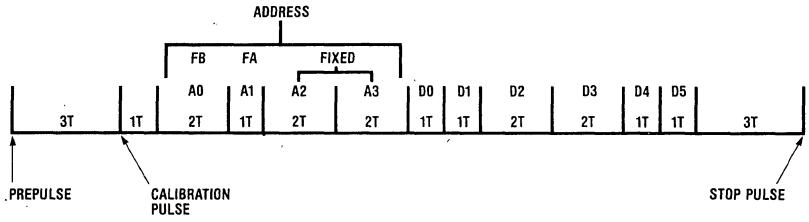
The information is transmitted in coded groups of infrared light pulses. The binary value of a single bit is represented by the time space between leading edges of two consecutive pulses. With an input oscillator frequency of 200kHz a time T$\triangle$ 100μs is defined as the unit space (1T) representing a binary zero, a double space (2T) represents a binary one. See Figure 3.

Eleven pulses are required for each word consisting of 4 bits for address and 6 bits for data. Each word is preceded by a calibration and start pulse at intervals of 1T and 3T respectively. A stop pulse is transmitted 3T after the last data pulse.



All times are related to an input oscillator frequency of approximately 200 kHz

Figure 3



Format of message 001100 to address 1101

Figure 4

Table 1. Instruction Table

	Row Input								Column Input								Binary Code 6 Bit Data						International REF 6 Bit ASCII Code
	a	b	c	d	e	f	g	h	A	B	C	D	E	F	G	H	MSB					LSB	
1.	x								x								0	0	0	0	0	0	@
2.	x									x							0	0	0	0	0	1	A
3.	x										x						0	0	0	0	1	0	B
4.	x											x					0	0	0	0	1	1	C
5.	x												x				0	0	0	1	0	0	D
6.	x													x			0	0	0	1	0	1	E
7.	x														x		0	0	0	1	1	0	F
8.	x															x	0	0	0	1	1	1	G
9.		x							x								0	0	1	0	0	0	H
10.		x								x							0	0	1	0	0	1	I
11.		x									x						0	0	1	0	1	0	J
12.		x										x					0	0	1	0	1	1	K
13.		x											x				0	0	1	1	0	0	L
14.		x												x			0	0	1	1	0	1	M
15.		x													x		0	0	1	1	1	0	N
16.		x														x	0	0	1	1	1	1	O
17.			x						x								0	1	0	0	0	0	P
18.			x							x							0	1	0	0	0	1	Q
19.			x								x						0	1	0	0	1	0	R
20.			x									x					0	1	0	0	1	1	S
21.			x										x				0	1	0	1	0	0	T
22.			x											x			0	1	0	1	0	1	U
23.			x												x		0	1	0	1	1	0	V
24.			x													x	0	1	0	1	1	1	W
25.				x					x								0	1	1	0	0	0	X
26.				x						x							0	1	1	0	0	1	Y
27.				x							x						0	1	1	0	1	0	Z
28.				x								x					0	1	1	0	1	1	[
29.				x									x				0	1	1	1	0	0	\
30.				x										x			0	1	1	1	0	1	]
31.				x											x		0	1	1	1	1	0	^
32.				x												x	0	1	1	1	1	1	—
33.					x				x								1	0	0	0	0	0	SP
34.					x					x							1	0	0	0	0	1	!
35.					x						x						1	0	0	0	1	0	"
36.					x							x					1	0	0	0	1	1	#
37.					x								x				1	0	0	1	0	0	$
38.					x									x			1	0	0	1	0	1	%
39.					x										x		1	0	0	1	1	0	&
40.					x											x	1	0	0	1	1	1	'
41.						x			x								1	0	1	0	0	0	(
42.						x				x							1	0	1	0	0	1	)
43.						x					x						1	0	1	0	1	0	*
44.						x						x					1	0	1	0	1	1	+
45.						x							x				1	0	1	1	0	0	,
46.						x								x			1	0	1	1	0	1	—
47.						x									x		1	0	1	1	1	0	.
48.						x										x	1	0	1	1	1	1	/
49.							x		x								1	1	0	0	0	0	0
50.							x			x							1	1	0	0	0	1	1
51.							x				x						1	1	0	0	1	0	2
52.							x					x					1	1	0	0	1	1	3
53.							x						x				1	1	0	1	0	0	4
54.							x							x			1	1	0	1	0	1	5
55.							x								x		1	1	0	1	1	0	6
56.							x									x	1	1	0	1	1	1	7
57.								x	x								1	1	1	0	0	0	8
58.								x		x							1	1	1	0	0	1	9
59.								x			x						1	1	1	0	1	0	:
60.								x				x					1	1	1	0	1	1	;
61.								x					x				1	1	1	1	0	0	<
62.								x						x			1	1	1	1	0	1	=
63.								x							x		1	1	1	1	1	0	>
64.								x								x	1	1	1	1	1	1	?

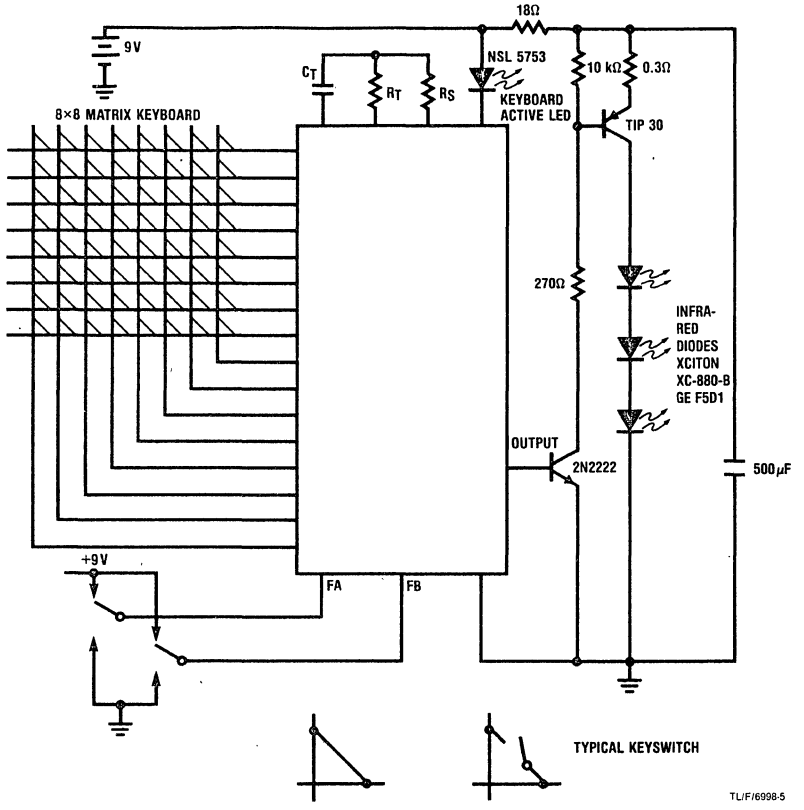
Address Decoding

FA	FB	Address
1	1	1 1 1 1
1	0	1 1 1 0
0	1	1 1 0 1
0	0	1 1 0 0

Address 1100 enables one shot mode which allows the message to be transmitted only once for each key depression.

Table 2

Typical Application Diagram (256 code transmitter with visual *feedback)



*If not required LED can be replaced by three 1N914 diodes

Oscillator Typical Values

C_T 47pF 2% polystyrene or silver mica
R_T 1% metal oxide
R_S 5%

Figure 5

National Semiconductor

MM53226 Infrared Remote Control Transmitter

General Description

The MM53226 is an infrared remote control transmitter circuit using low threshold N-channel enhancement and depletion devices. This versatile circuit is ideal for sophisticated TV/HiFi consumer applications. The transmission of information is achieved using bursts of pulse code modulated infrared light, each burst consists of a fixed number of constant amplitude pulses with binary coded spaces. This system allows high pulse current drive to the transmitter diodes, and also high data integrity with noise immunity. The circuit features very low quiescent current drain guaranteeing long battery life.

Features

- 64 commands to 4 addresses
- Simple interface to Standby 9V battery
- Very low standby current — 10μA typical
- Pin compatible with ITT 1050/1250
- 0.1% IR drive ensures long battery life
- 6-bit data word, 2-bit address word
- Simple RC oscillator only requires 3 external components
- Keyswitch requirements allow use of low cost keyboard
- Simple interface to high current IR diodes
- Double key depression detection

Applications

- Remote control of TV
- Remote control of HiFi
- Remote machine control
- Remote ASCII keyboard
- Serial keyboard encoder

Block Diagram

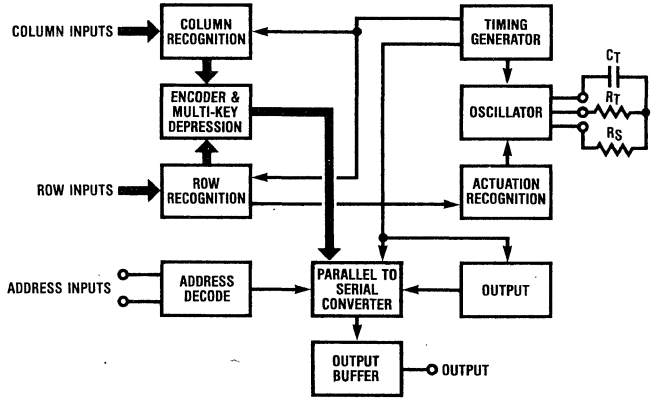


Figure 1

Absolute Maximum Ratings

Voltage at Any Pin	−0.5 to 12V
Storage Temperature	−65°C to 150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

$T_A = 0°C$, $V_{SS} = 0V$, $V_{DD} = 6V$ to 10V unless otherwise specified.

Sym	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		6		10	V
I_{DD}	Supply Current	$V_{DD} = 9V$ No key depressed		10	20	μA
		$V_{DD} = 7V$ Valid key depressed (See Figure 5)			10	mA
	Oscillator Frequency	$C_T = 47pF$ 2% $R_T = 33k$ 1% $R_S = 33k$ 5% (See Figure 5)	160		220	kHz
	Output Logic Levels Serial Out Logic "0" Logic "1"	 1 Sink = 0.2mA 1 Source = 0.2mA	 1.0		 0.2	 V V

Functional Description

The block diagram of the MM53226 is shown in Figure 1. A connection diagram is shown in Figure 2.

The MM53226 operates using a simple 8 × 8 keyboard giving 64 different commands. The two inputs FA and FB are address inputs which allow a total of 256 messages to be transmitted. These commands are transmitted using pulse position modulation. See Figure 4.

The row and column circuitry recognizes when a single row is connected to a single column and removes the reset from the circuit. This activates the oscillator whose frequency is determined by the external components C_T, R_T and R_S. If a row input is connected to a column input for greater than 40k clocks the message is transmitted using 14 pulses of data. For the period that the row is connected to the column the message is transmitted every 40k clocks.

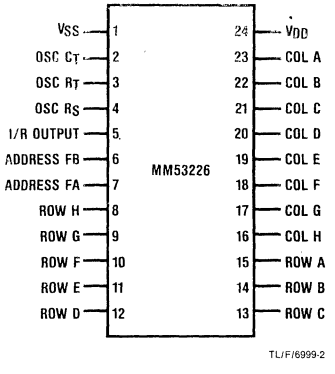
Releasing the row-column connection powers down the circuit to a standby condition of very low current consumption to conserve battery power. If the key contact is released during the transmission of a message the circuit will complete the transmission before powering down.

The multi-key depression detection circuit inhibits the output if more than one key is depressed.

The encoder provides at the output, via the parallel to serial converter, one of 64 codes (see Table 1). One of four addresses may be selected (see Table 2) giving a total of 256 commands that may be transmitted.

Connection Diagram

Dual-In-Line Package



Top View

Figure 2

Order Number MM53226N
See NS Package N24A

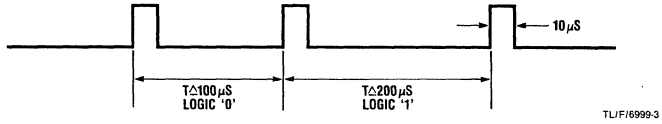
Typical Keyboard Specifications

R_{ON}	5 kΩ max
R_{OFF}	300 kΩ min

Format of Transmitted Signal:

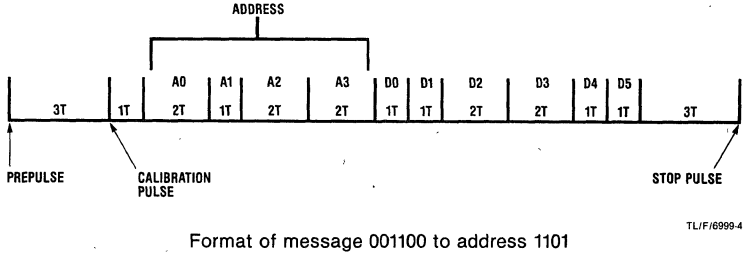
The information is transmitted in coded groups of infrared light pulses. The binary value of a single bit is represented by the time space between leading edges of two consecutive pulses. With an input oscillator frequency of 200kHz a time T$\triangle$ 100μs is defined as the unit space (1T) representing a binary zero, a double space (2T) represents a binary one. See Figure 3.

Eleven pulses are required for each word consisting of 4 bits for address and 6 bits for data. Each word is preceded by a calibration and start pulse at intervals of 1T and 3T respectively. A stop pulse is transmitted 3T after the last data pulse.



All times are related to an input oscillator frequency of approximately 200kHz.

Figure 3



Format of message 001100 to address 1101

Figure 4

Table 1. Instruction Table

	Row Input								Column Input								Binary Code 6 Bit Data						International REF 6 Bit ASCII Code
	a	b	c	d	e	f	g	h	A	B	C	D	E	F	G	H	MSB					LSB	
1.	x								x								0	0	0	0	0	0	@
2.	x									x							0	0	0	0	0	1	A
3.	x										x						0	0	0	0	1	0	B
4.	x											x					0	0	0	0	1	1	C
5.	x												x				0	0	0	1	0	0	D
6.	x													x			0	0	0	1	0	1	E
7.	x														x		0	0	0	1	1	0	F
8.	x															x	0	0	0	1	1	1	G
9.		x							x								0	0	1	0	0	0	H
10.		x								x							0	0	1	0	0	1	I
11.		x									x						0	0	1	0	1	0	J
12.		x										x					0	0	1	0	1	1	K
13.		x											x				0	0	1	1	0	0	L
14.		x												x			0	0	1	1	0	1	M
15.		x													x		0	0	1	1	1	0	N
16.		x														x	0	0	1	1	1	1	O
17.			x						x								0	1	0	0	0	0	P
18.			x							x							0	1	0	0	0	1	Q
19.			x								x						0	1	0	0	1	0	R
20.			x									x					0	1	0	0	1	1	S
21.			x										x				0	1	0	1	0	0	T
22.			x											x			0	1	0	1	0	1	U
23.			x												x		0	1	0	1	1	0	V
24.			x													x	0	1	0	1	1	1	W
25.				x					x								0	1	1	0	0	0	X
26.				x						x							0	1	1	0	0	1	Y
27.				x							x						0	1	1	0	1	0	Z
28.				x								x					0	1	1	0	1	1	[
29.				x									x				0	1	1	1	0	0	\
30.				x										x			0	1	1	1	0	1	]
31.				x											x		0	1	1	1	1	0	^
32.				x												x	0	1	1	1	1	1	—
33.					x				x								1	0	0	0	0	0	SP
34.					x					x							1	0	0	0	0	1	!
35.					x						x						1	0	0	0	1	0	"
36.					x							x					1	0	0	0	1	1	#
37.					x								x				1	0	0	1	0	0	$
38.					x									x			1	0	0	1	0	1	%
39.					x										x		1	0	0	1	1	0	&
40.					x											x	1	0	0	1	1	1	'
41.						x			x								1	0	1	0	0	0	(
42.						x				x							1	0	1	0	0	1	)
43.						x					x						1	0	1	0	1	0	*
44.						x						x					1	0	1	0	1	1	+
45.						x							x				1	0	1	1	0	0	,
46.						x								x			1	0	1	1	0	1	—
47.						x									x		1	0	1	1	1	0	.
48.						x										x	1	0	1	1	1	1	/
49.							x		x								1	1	0	0	0	0	0
50.							x			x							1	1	0	0	0	1	1
51.							x				x						1	1	0	0	1	0	2
52.							x					x					1	1	0	0	1	1	3
53.							x						x				1	1	0	1	0	0	4
54.							x							x			1	1	0	1	0	1	5
55.							x								x		1	1	0	1	1	0	6
56.							x									x	1	1	0	1	1	1	7
57.								x	x								1	1	1	0	0	0	8
58.								x		x							1	1	1	0	0	1	9
59.								x			x						1	1	1	0	1	0	:
60.								x				x					1	1	1	0	1	1	;
61.								x					x				1	1	1	1	0	0	<
62.								x						x			1	1	1	1	0	1	=
63.								x							x		1	1	1	1	1	0	>
64.								x								x	1	1	1	1	1	1	?

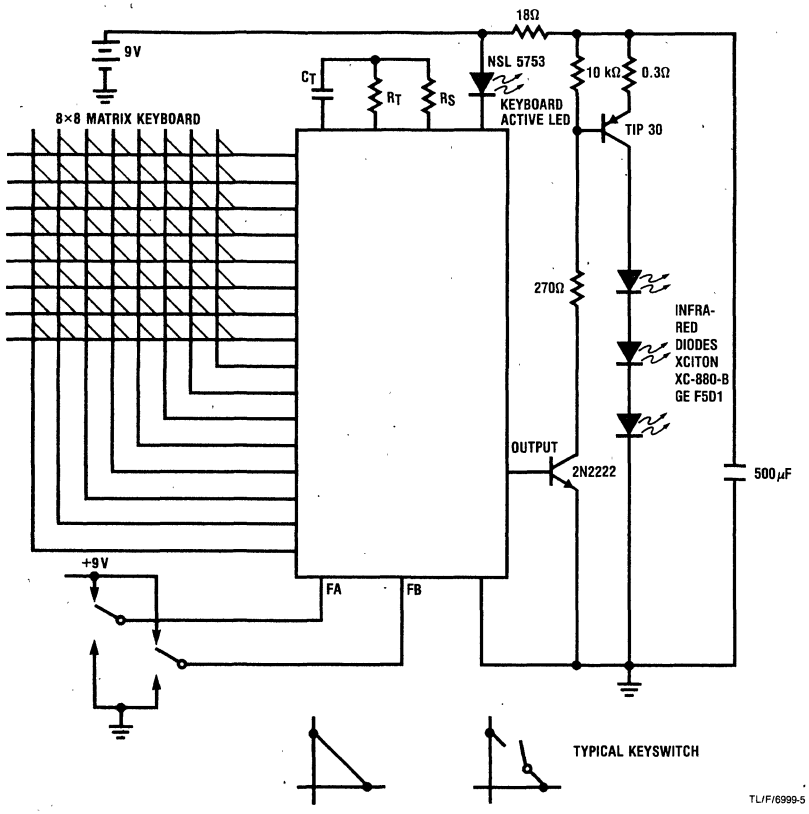
Address Decoding

FA	FB	Address MSB			LSB	
1	1	0	0	0	0	Note 1
1	0	1	1	1	0	
0	1	1	0	0	1	
0	0	0	0	0	0	

Note 1: When a key is depressed with FA = FB = 1 the first message is transmitted with address 0000, all following messages are transmitted with address 1111 for as long as the key is depressed.

Table 2

Typical Application Diagram (256 code transmitter with visual *feedback)



*If not required Keyboard Active LED can be replaced by three 1N914 diodes

Oscillator Typical Values

C_T 47pF 2% polystyrene or silver mica
R_T 1% metal oxide
R_S 5%

Figure 5

National Semiconductor

MM5437 Digital Noise Source

General Description

The MM5437 device is a monolithic metal gate NMOS integrated circuit which may be used as a digital noise source or a pseudo-random number generator. The part is designed to produce a broadband white noise signal with uniform noise quality and output amplitude. Two outputs are provided. The first, OUT 1, is sequence-limited to reduce "thumps." The other output, OUT 2, is the last stage of the shift register when $\overline{\text{CONTROL 2}}$ is left floating or is pulled up. Typical cycle time is one minute. Data is clocked in and out on the rising edge of the clock.

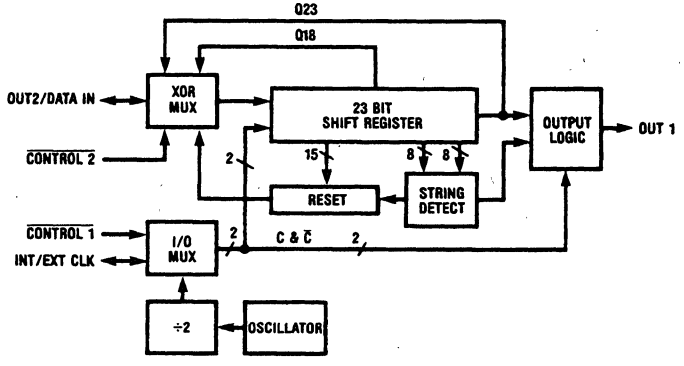
Features

- Internal self-contained oscillator
- Single supply voltage range of 4.5V to 11V
- TTL compatible at 5V
- Normal and sequence-limited outputs
- Low power consumption
- One minute cycle time
- External loading and clocking capability
- Automatic reset for all-zeros state
- Uniform noise quality
- Uniform noise amplitude
- Eliminate noise preamps
- Single component insertion

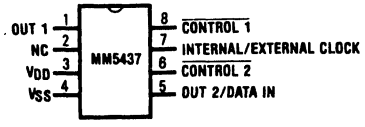
Applications

- Electronic musical rhythm instrument sound generators
- Music synthesizer white and pink noise generators
- Room acoustics testing/equalization
- Pseudo-random number generator

Block and Connection Diagrams



TL/F/5260–1



TL/F/5260–2

Top View

Order Number MM5437N
See NS Package Number N08E

Absolute Maximum Ratings

Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

Operating Supply Voltage, V_{DD}	12V
Storage Temperature, T_S	−65°C to +150°C
Operating Temperature, T_A	−40°C to +85°C
DC Output Current, per pin	±12 mA
Lead Temp. (Soldering, 10 seconds)	+300°C

DC Electrical Characteristics T_A within operating range, V_{SS} = 0V, V_{DD} = 11V, unless specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage (V_{DD})		4.5		11	V
Supply Current (I_{DD})	V_{DD} = 4.5V (No load) V_{DD} = 11V (No load)			4 5	mA mA
Output Voltage Levels Logic '0' Logic '1'	 I_{OL} = +1.6 mA, V_{DD} = 4.5V I_{OH} = −400 μA, V_{DD} = 4.5V	 V_{SS} 2.4		 0.4 V_{DD}	 V V
Input Voltage Levels Logic '0' Logic '1'		 2.0		 0.8 	 V
Input Currents Logic '0' Logic '1'	 V_{IN} = 0.4V V_{IN} = 2.4V			 200 200	 μA μA
Half Power Point*		30		140	kHz
Cycle Time		25		110	sec.

*Half Power Point = 0.45 (Shift Register Clock Frequency)

AC Timing $-40°C \le T_A \le +85°C$, $4.5V \le V_{DD} \le 11V$

Symbol	Parameter	Min	Max	Units
t_S	Data Set Up Time Prior to Clock	100		ns
t_H	Data Hold Time After Clock	100		ns
t_{C2DV}	$\overline{\text{CONTROL 2}}$ to Data Out Valid		100	ns
t_{CLKDV}	Clock to Data Out Valid		700	ns
t_{PH}	Clock Pulse Width High	1.5		μs
t_{PL}	Clock Pulse Width Low	1.5		μs
t_r, t_f	Input Rise and Fall Times		220	ns

Inputs/Outputs

$\overline{\text{CONTROL 1}}$: A mode switch input, which when held at a logic "1" or left floating, gates the internal oscillator onto the INT/EXT CLK pin. When $\overline{\text{CONTROL 1}}$ is at a logic "0", the shift register can be driven externally through the INT/EXT CLK pin.

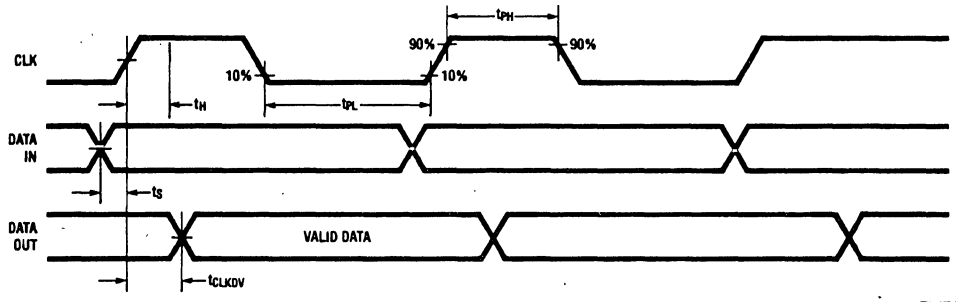
$\overline{\text{CONTROL 2}}$: A mode switch input, which when held at a logic "1" or left floating, gates the last stage of the shift register onto the OUT 2/DATA IN pin. When $\overline{\text{CONTROL 2}}$ is at a logic "0", the shift register can be loaded externally through the OUT 2/DATA IN pin.

OUT 1: An output pin for the sequence-limited output from the shift register.

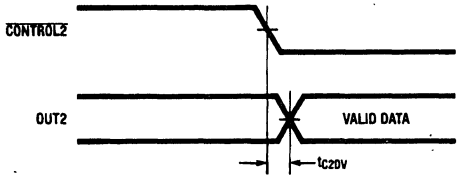
INT/EXT CLK: An input/output pin. See $\overline{\text{CONTROL 1}}$ for description.

OUT 2/DATA IN: An input/output pin. See $\overline{\text{CONTROL 2}}$ for description.

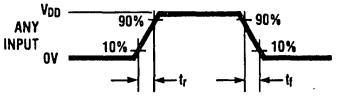
Timing Diagrams



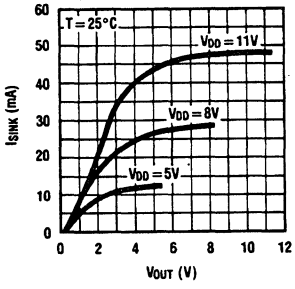
TL/F/5260–3



TL/F/5260–4

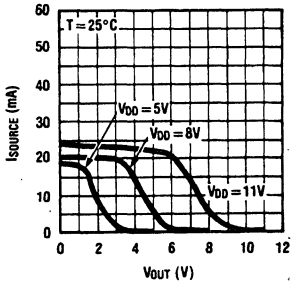


TL/F/5260–5



TL/F/5260–6

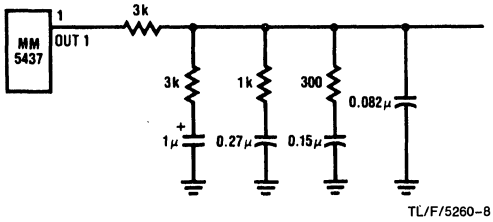
FIGURE 1. I_{SINK} vs V_{OUT}



TL/F/5260–7

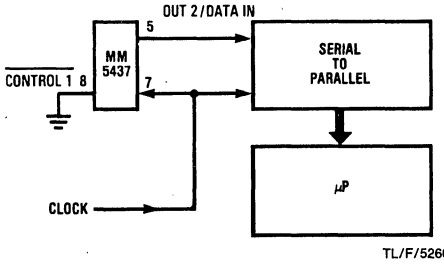
FIGURE 2. I_{SOURCE} vs V_{OUT}

Typical Applications



TL/F/5260–8

FIGURE 3. Pink Noise Generator



TL/F/5260–9

FIGURE 4. Pseudo-Random Number Generator

National Semiconductor

MM5450, MM5451 LED Display Drivers

General Description

The MM5450 and MM5451 are monolithic MOS integrated circuits utilizing N-channel metal-gate low threshold, enhancement mode, and ion-implanted depletion mode devices. They are available in 40-pin molded or cavity dual-in-line packages. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD}.

Features

- Continuous brightness control
- Serial data input
- No load signal required
- Enable (on MM5450)
- Wide power supply operation
- TTL compatibility
- 34 or 35 outputs, 15 mA sink capability
- Alphanumeric capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block Diagram

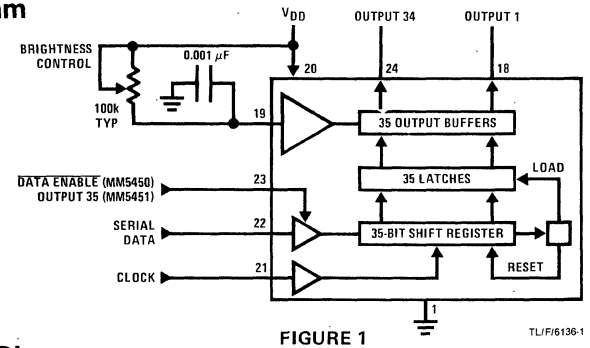


FIGURE 1

Connection Diagrams (Dual-In-Line Packages)

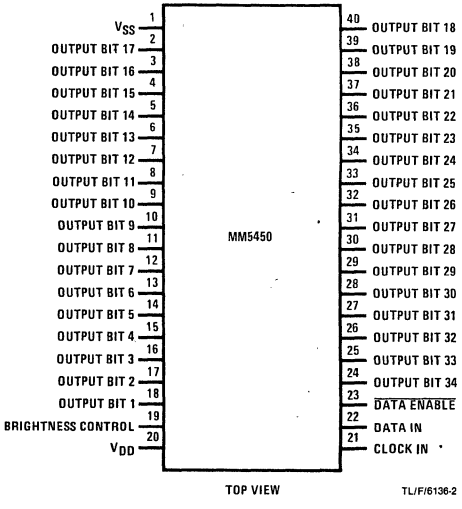


FIGURE 2a

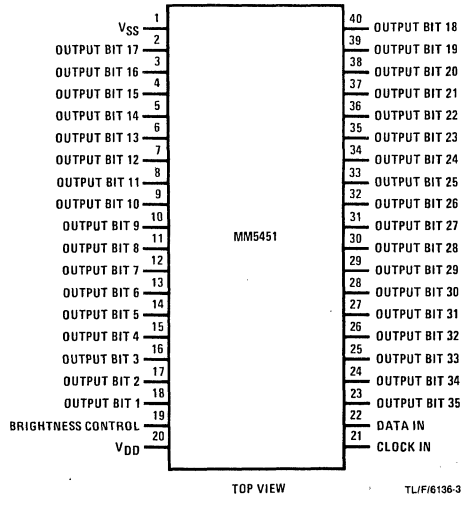


FIGURE 2b

Order Number MM5450N or MM5451N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to V_{SS} + 12V	Power Dissipation	560 mW at +85°C
Operating Temperature	−25°C to +85°C		1W at +25°C
Storage Temperature	−65°C to +150°C	Junction Temperature	+150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A within operating range, $V_{DD} = 4.5V$ to 11.0V, $V_{SS} = 0V$ unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		4.75		11	V
Power Supply Current	Excluding Output Loads			7	mA
Input Voltages					
Logical "0" Level (V_L)	± 10 μA Input Bias	−0.3		0.8	V
Logical "1" Level (V_H)	$4.75 \leq V_{DD} \leq 5.25$	2.2		V_{DD}	V
	$V_{DD} > 5.25$	$V_{DD} - 2$		V_{DD}	V
Brightness Input (Note 2)		0		0.75	mA
Output Sink Current					
Segment OFF	$V_{OUT} = 3.0V$			10	μA
Segment ON	$V_{OUT} = 1V$ (Note 3)	0		15	mA
	Brightness Input = 0 μA	0		10	μA
	Brightness Input = 100 μA	2.0	2.7	4	mA
	Brightness Input = 750 μA	15		25	mA
Brightness Input Voltage (Pin 19)	Input Current = 750 μA	3.0		4.3	V
Output Matching (Note 1)				± 20	%
Clock Input	(Notes 5 and 6)				
Frequency, f_C				500	kHz
High Time, t_h		950			ns
Low Time, t_l		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hole Time, t_{DH}		300			ns
Data Enable Input					
Set-Up Time, t_{DES}		100			ns

Note 1: Output matching is calculated as the percent variation $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: See *Figures 5, 6 and 7* for Recommended Operating Conditions and limits. Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user. See *Figures 6 and 7* for allowable V_{OUT} vs I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ± 10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

Both the MM5450 and the MM5451 are specifically designed to operate 4 or 5-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 capacitor should be connected to brightness control, pin 19, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. For the MM5450 a $\overline{\text{DATA ENABLE}}$ is used instead of the 35th output. The $\overline{\text{DATA ENABLE}}$ input is a metal option for the MM5450. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all

Functional Description (Continued)

the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 2 shows the pin-out of the MM5450 and MM5451. Bit 1 is the first bit following the start bit and it will appear on pin 18. A logical "1" at the input will turn on the appropriate LED.

Figure 3 shows the timing relationships between data, clock and $\overline{\text{DATA ENABLE}}$. A max clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$$T_j = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(124^\circ\text{C/W}) + T_A$$

where:

T_j = junction temperature +150°C max

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

124°C/W = thermal coefficient of the package

T_A = ambient temperature

The above equation was used to plot *Figure 5, Figure 6, and Figure 7.*

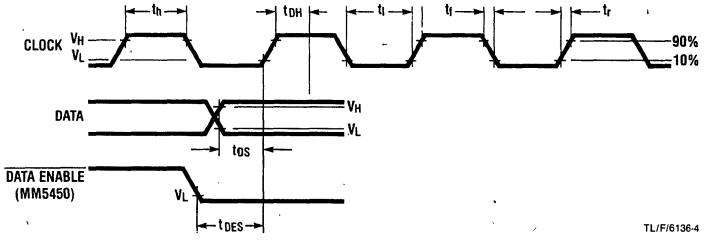


FIGURE 3

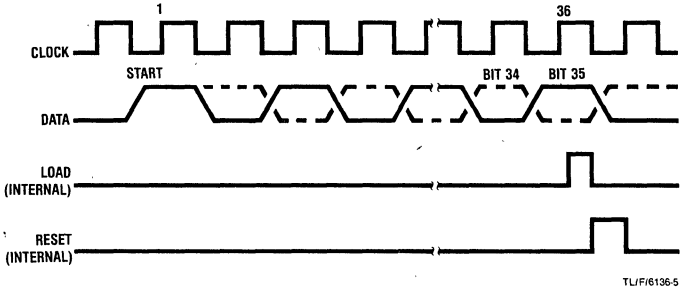


FIGURE 4. Input Data Format

Typical Applications

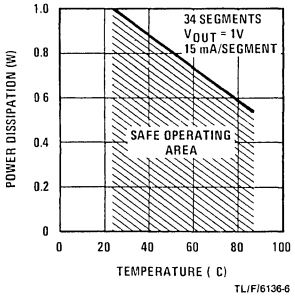


FIGURE 5

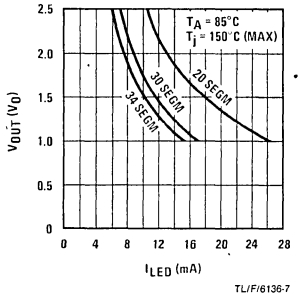


FIGURE 6

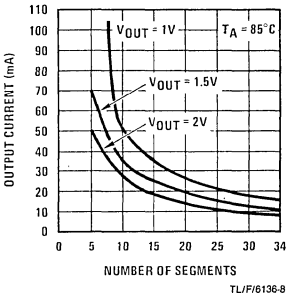


FIGURE 7

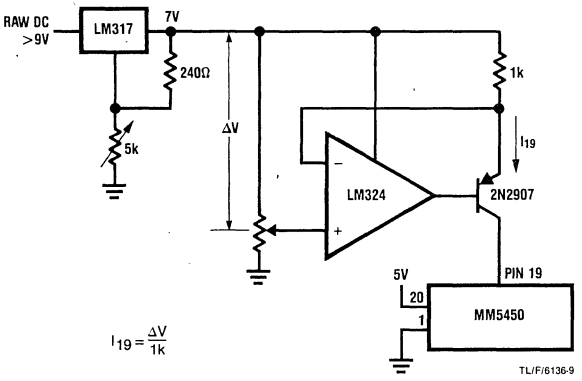


FIGURE 8. Typical Application of Constant Current Brightness Control

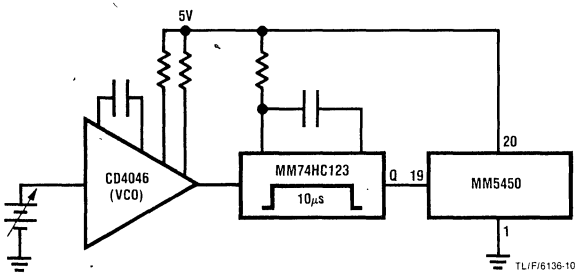
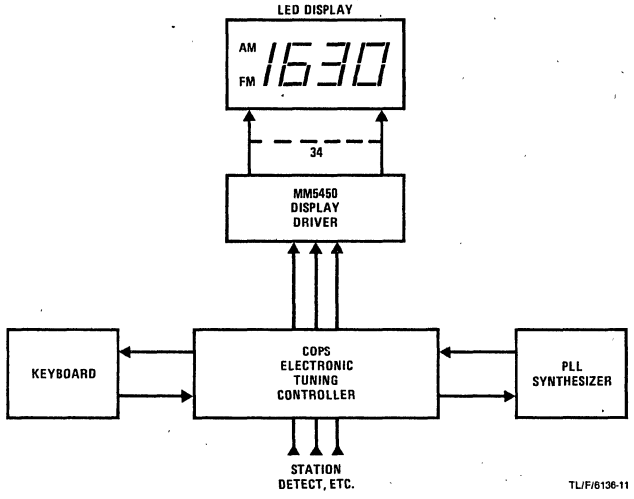


FIGURE 9. Brightness Control Varying the Duty Cycle

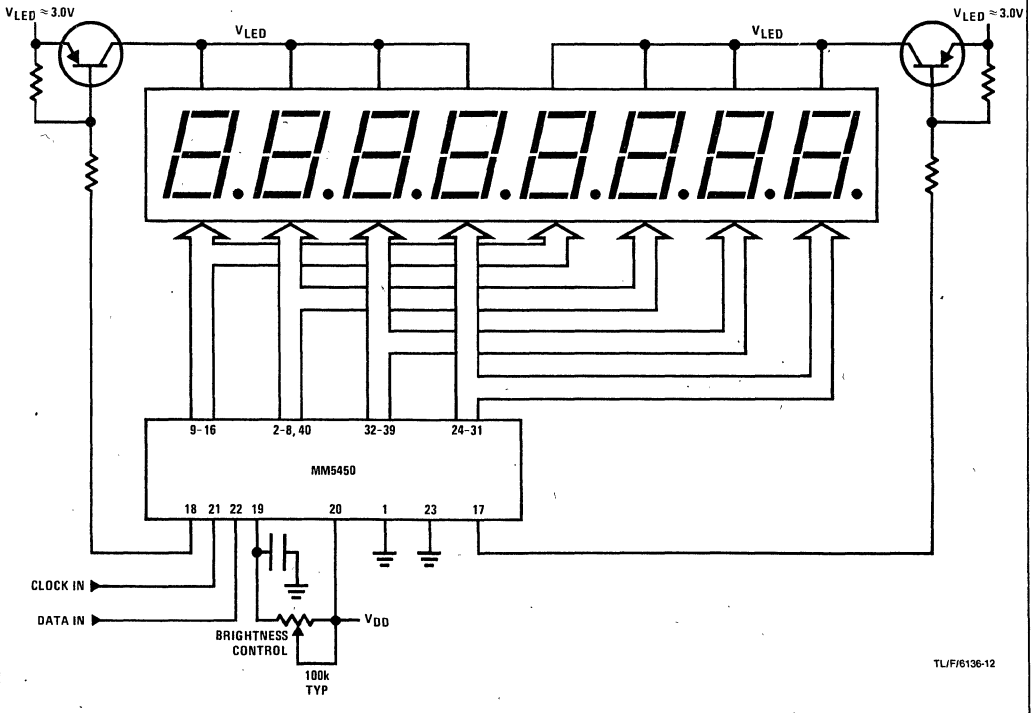
7

Typical Applications (Continued)

Basic Electronically Tuned Radio System



Duplexing 8 Digits with One MM5450



National Semiconductor

MM5452, MM5453 Liquid Crystal Display Drivers

General Description

The MM5452 is a monolithic integrated circuit utilizing CMOS metal gate, low threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 32 segments of LCD and can be paralleled to increase this number. The chip is capable of driving a 4 1/2-digit 7-segment display with minimal interface between the display and the data source.

The MM5452 stores the display data in latches after it is clocked in, and holds the data until new display data is received.

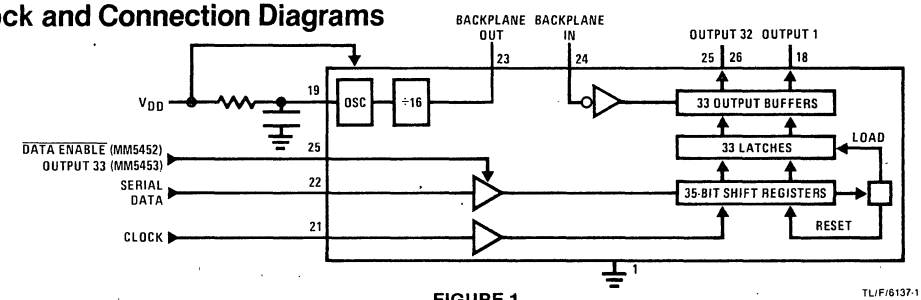
Features

- Serial data input
- No load signal required
- $\overline{\text{DATA ENABLE}}$ (MM5452)
- Wide power supply operation
- TTL compatibility
- 32 or 33 outputs
- Alphanumeric and bar graph capability
- Cascaded operation capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

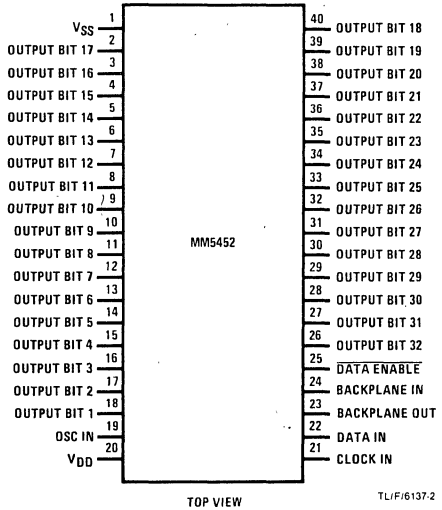
Block and Connection Diagrams



TL/F/6137-1

FIGURE 1

Dual-In-Line Package

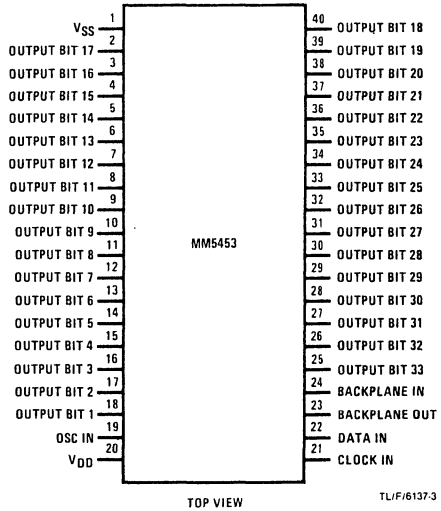


TOP VIEW

TL/F/6137-2

FIGURE 2a

Dual-In-Line Package



TOP VIEW

TL/F/6137-3

FIGURE 2b

Order Number MM5452D, MM5453D, MM5452N or MM5453N
See NS Package D40C or N40A

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to V_{SS} + 10V	Power Dissipation	300 mW at + 70°C 350 mW at + 25°C
Operating Temperature	0°C to + 70°C		
Storage Temperature	− 65° to + 150°C	Junction Temperature	+ 150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A within operating range, $V_{DD} = 3.0V$ to 10V, $V_{SS} = 0V$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3		10	V
Power Supply Current	Excluding Outputs OSC = V_{SS}, BP IN @ 32 Hz V_{DD} = 5V, Open Outputs, No Clock			40 10	μA μA
Clock Frequency				500	kHz
Input Voltages					
Logical '0' Level	$V_{DD} < 4.75$ $V_{DD} \geq 4.75$	− 0.3 − 0.3		0.1 V_{DD} 0.8	V V
Logical '1' Level	$V_{DD} > 5.25$ $V_{DD} \leq 5.25$	0.8 V_{DD} 2.0		V_{DD} V_{DD}	V V
Output Current Levels					
Segments					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			− 20	μA
Source	V_{DD} = 3V, $V_{OUT} = V_{DD} - 0.3V$	20			μA
Backplane					
Sink	V_{DD} = 3V, V_{OUT} = 0.3V			− 320	μA
Source	V_{DD} = 3V, $V_{OUT} = V_{DD} - 0.3V$	320			μA
Output Offset Voltage	Segment Load 250 pF Backplane Load 8750 pF (Note 1)			± 50	mV
Clock Input Frequency, f_C	(Notes 2 and 3)			500	kHz
High Time, t_h		950			ns
Low Time, t_l		950			ns
Data Input					
Set-Up Time, t_{DS}		300			ns
Hold Time, t_{DH}		300			ns
Data Enable Input					
Set-Up Time, t_{DES}		100			ns

Note 1: This parameter is guaranteed (not 100% production tested) over operating temperature and supply voltage ranges. Not to be used in Q.A. testing.

Note 2: AC input waveform for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ± 10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5452 is specifically designed to operate 4 1/2-digit 7-segment displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Since the MM5452 does not contain a character generator, the formatting of the segment information must be done prior to inputting the data to the MM5452. Using a format of a leading "1" followed by the 32 data bits allows data transfer without an additional load signal. The 32 data bits are latched after the 36th clock is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time.

A block diagram is shown in *Figure 1.* For the MM5452 a DATA ENABLE is used instead of the 33rd output. If the DATA ENABLE signal is not required, the 33rd output can be brought out. This is the MM5453 device.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 32 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 32 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

If the clock is not continuous, there must be a complete set of 36 clocks otherwise the shift registers will not clear.

Figure 2a shows the pin-out of the MM5452. Bit 1 is the first bit following the start bit and it will appear on pin 18.

Figure 3 shows the timing relationships between data, clock and DATA ENABLE.

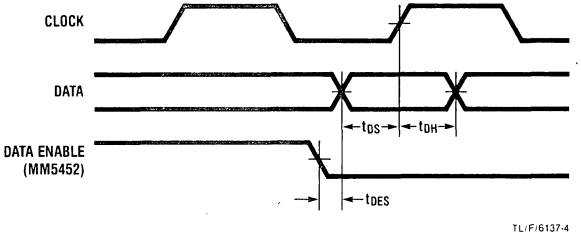


FIGURE 3

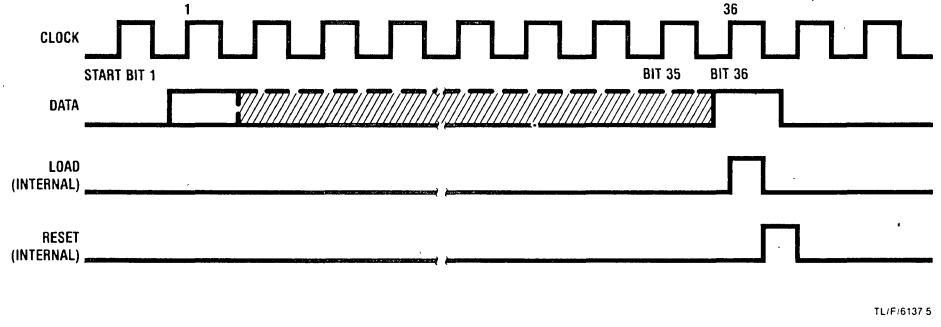


FIGURE 4. Input Data Format

Functional Description (Continued)

Figure 5 shows a typical application. Note how the input data maps to the output pins and the display. The MM5452 and MM5453 do not have format restrictions, as all outputs are controllable. This application assumes a specific display pinout. Different display/driver connection patterns will, of course, yield a different input data format.

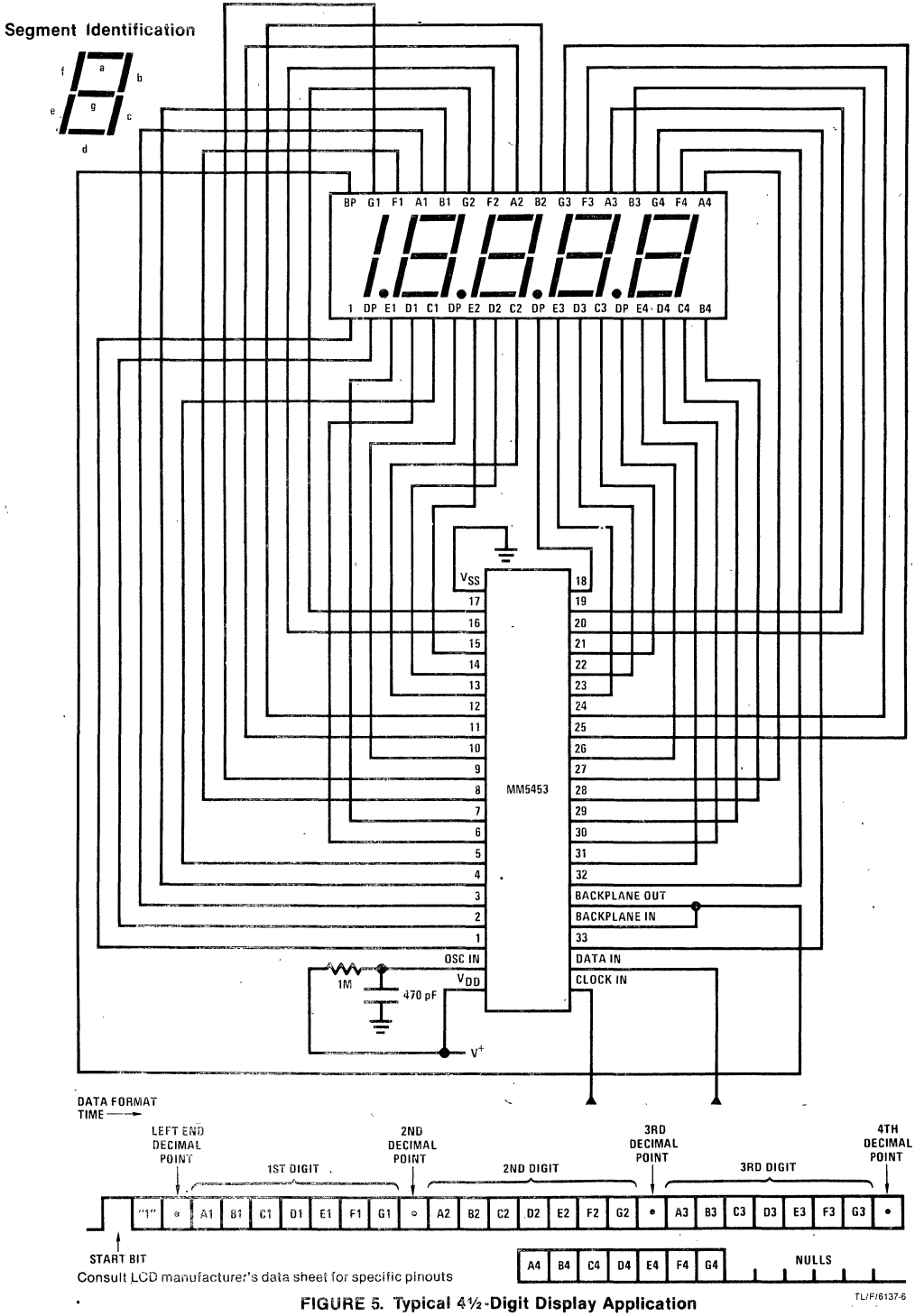


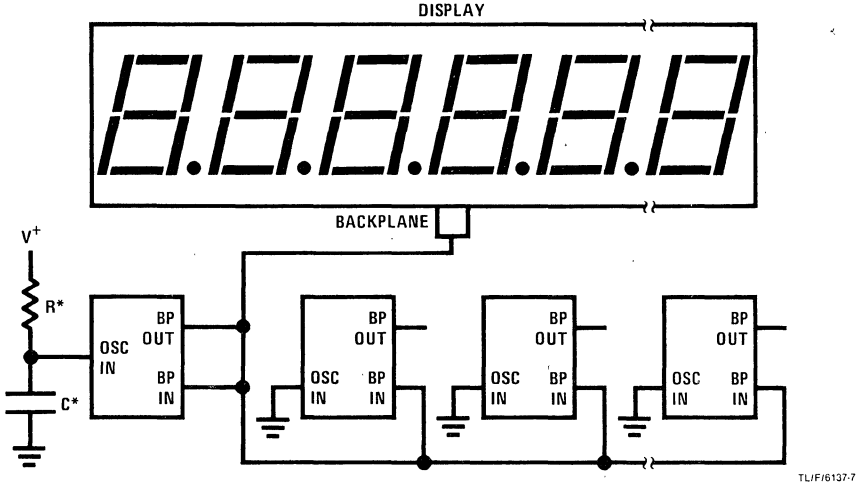
FIGURE 5. Typical 4½-Digit Display Application

Functional Description (Continued)

Figure 8 shows a four wire remote display that takes advantage of the device's serial input to move many bits of display information on a few wires.

Using an External Clock

The MM5452, MM5453 LCD Drivers can be used with an externally supplied clock, provided it has a duty cycle of 50%. Deviations from a 50% duty cycle result in an offset voltage on the LCD. In *Figure 7*, a flip flop is used to assure a 50% duty cycle. The oscillator input is grounded to prevent oscillation and reduce current consumption in the chips. The oscillator is not used.



* The minimum recommended value for R for the oscillator input is 9 kΩ. An RC time constant of approximately 4.91×10^{-4} should produce a backplane frequency between 30 Hz and 150 Hz.

FIGURE 6. Parallel Backplane Outputs

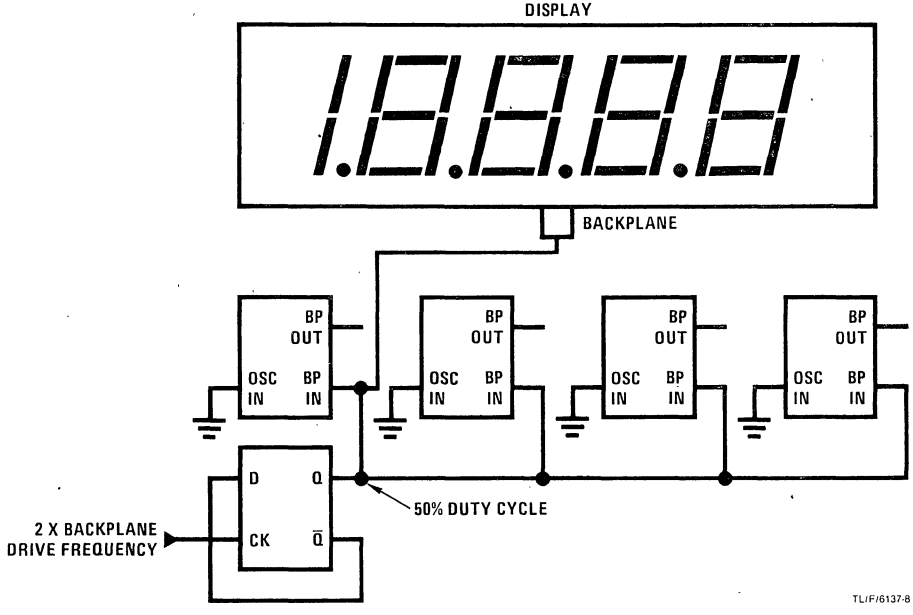


FIGURE 7. External Backplane Clock

Functional Description (Continued)

Using an external clock allows synchronizing the display drive with AC power, internal clocks, or DVM integration time to reduce interference from the display.

Figure 9 is a general block diagram that shows how the device's serial input can be used to advantage in an analog display. The analog voltage input is compared with a staircase voltage generated by a counter and a digital-to-analog converter or resistor array. The result of this comparison is clocked into the MM5452, MM5453. The next clock pulse increments the staircase and clocks the new data in.

With a buffer amplifier, the same staircase waveform can be used for many displays. The digital-to-analog converter need not be linear; logarithmic or other non-linear functions can be displayed by using weighted resistors or special DACs. This system can be used for status indicators, spectrum analyzers, audio level and power meters, tuning indicators, and other applications.

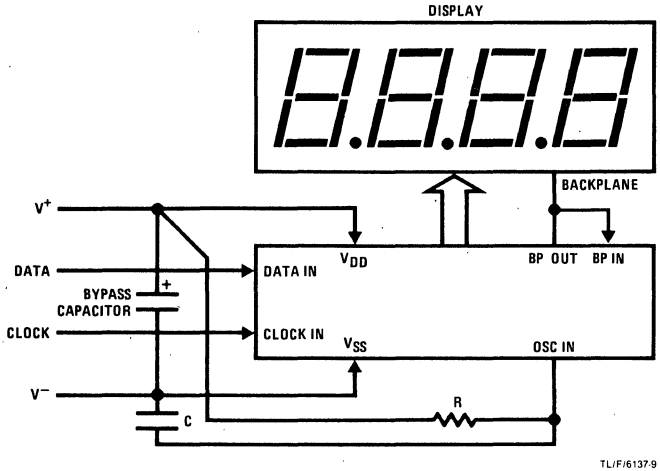
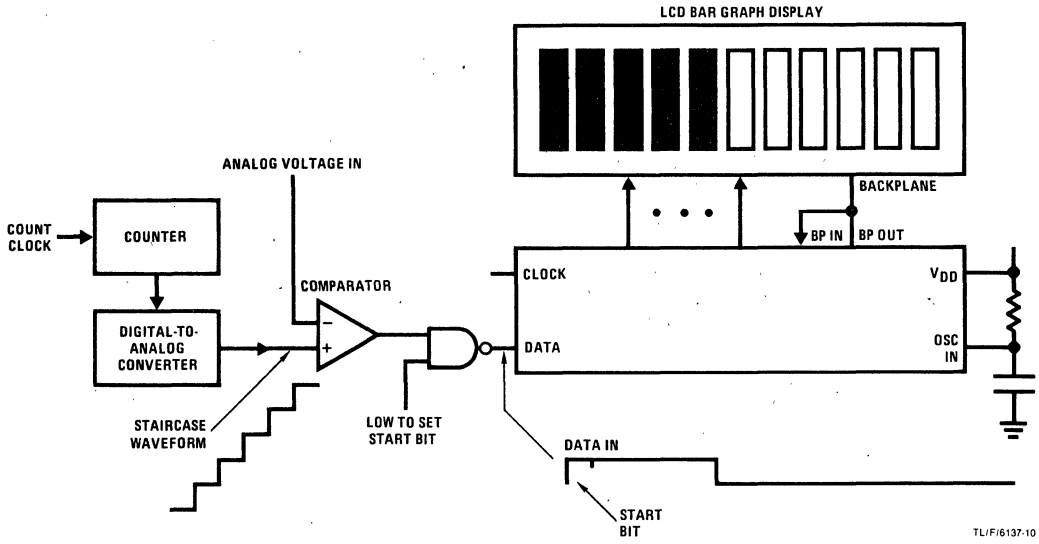


FIGURE 8. Four Wire Remote Display



Data is high until staircase>input

FIGURE 9. Analog Display

National Semiconductor

MM5480 LED Display Driver

General Description

The MM5480 is a monolithic MOS integrated circuit utilizing N-channel metal gate low threshold, enhancement mode and ion-implanted depletion mode devices. It utilizes the MM5451 die packaged in a 28-pin package making it ideal for a 3½ digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 11V maximum.

Features

- Continuous brightness control
- Serial data input
- No load signal required
- Wide power supply operation
- TTL compatibility
- Alphanumeric capability
- 3½ digit displays

Applications

- COPS or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts

Block Diagram

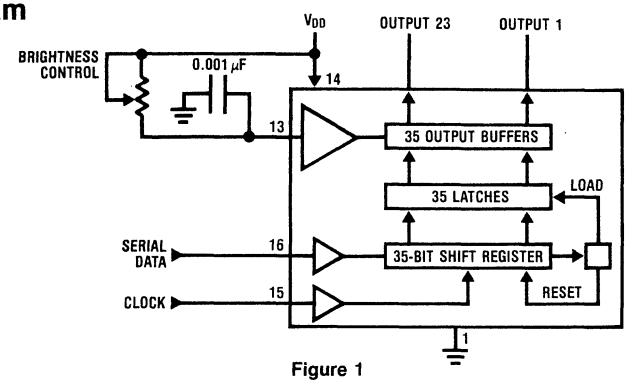
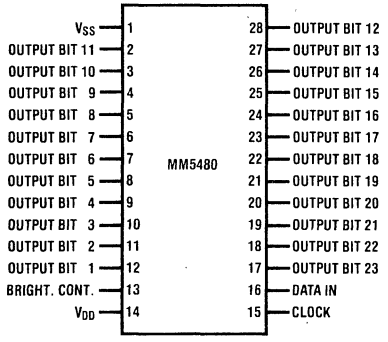


Figure 1

TL/F/6138-1

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6138-2

Figure 2

Order Number MM5480N
See NS Package N28B

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to $V_{SS}+12V$	Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	490mW at +85°C		
	940mW at +25°C		

Electrical Characteristics $T_A = -25°C$ to $+85°C$, $V_{DD} = 4.75V$ to 11.0V, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
	Input Voltages					
V_{IL}	Logical "0" Level	± 10 μA Input Bias	−0.3		0.8	V
V_{IH}	Logical "1" Level	$4.75 \le V_{DD} \le 5.25$	2.2		V_{DD}	V
		$V_{DD} > 5.25$	$V_{DD}-2$		V_{DD}	V
I_{BR}	Brightness Input Current (Note 2)		0		0.75	mA
	Output Sink Current (Note 3)					
I_{OH}	Segment OFF	$V_{OUT} = 3.0V$			10.0	μA
I_{OL}	Segment ON	$V_{OUT} = 1V$				
		Brightness Input = 0 μA	0		10.0	μA
		Brightness Input = 100 μA	2.0	2.7	4.0	mA
		Brightness Input = 750 μA	15.0		25.0	mA
V_{IBR}	Brightness Input Voltage (Pin 19)	Input Current = 750 μA	3.0		4.3	V
OM	Output Matching (Note 1)				± 20	%

AC Electrical Characteristics $T_A = -25°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 5 and 6)	DC		500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
	Data Input					
t_{DS}	Set-Up Time		300			ns
t_{DH}	Hold Time		300			ns

Note 1: Output matching is calculated as the percent variation from $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user.

Note 5: AC input waveform specification for test purpose: $t_r \le 20$ ns, $t_f \le 20$ ns, f = 500 kHz, 50% ± 10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5480 is specifically designed to operate 3½-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF ceramic or mica disc capacitor should be connected to brightness control, pin 13, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. The output current is typically 20 times greater than the current into pin 13, which is set by an external variable resistor. There is an internal llmiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 5 shows the Output Data Format for the 5480. Because it uses only 23 of the possible 35 outputs, 12 of the bits are 'Don't Cares'.

Figure 3 shows the timing relationships between data and clock. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$T_j = (V_{OUT})\,(I_{LED})$ (No. of segments) (132 °C/W) + T_A
where:

T_j = junction temperature + 150 °C max.
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
132 °C/W = thermal coefficient of the package
T_A = ambient temperature

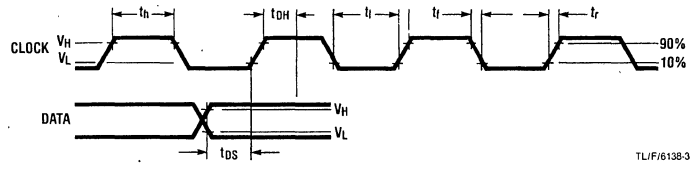


Figure 3

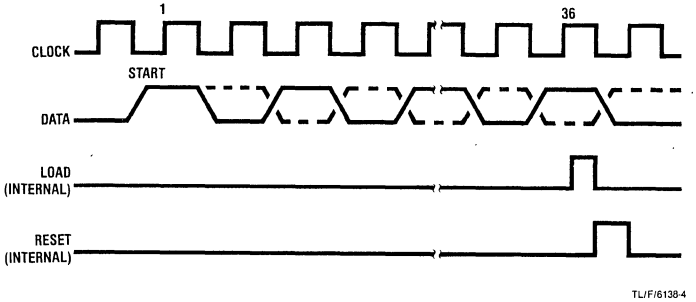


Figure 4. Input Data Format

START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	5451
START	X	1	2	3	4	5	6	7	X	X	X	8	9	10	11	X	X	X	X	12	13	14	15	16	17	X	18	X	X	19	20	21	22	23	X	5480

TL/F/6138-5

Figure 5. Output Data Format

Functional Description (Continued)

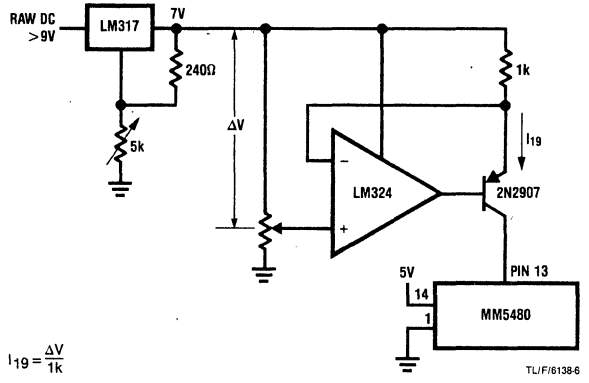


Figure 6. Typical Application of Constant Current Brightness Control

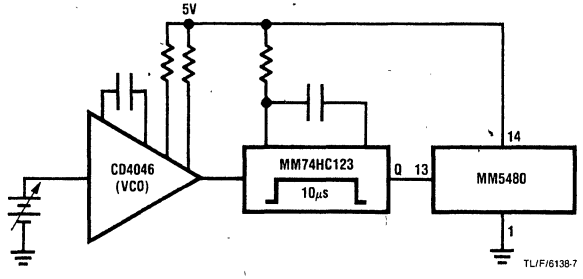
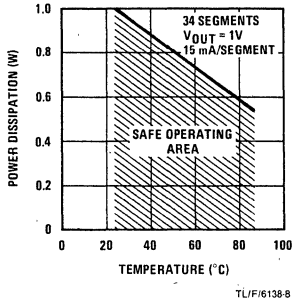
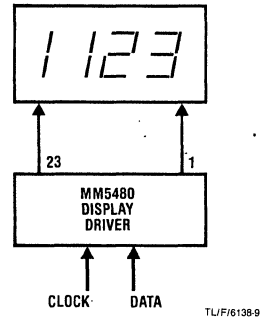


Figure 7. Brightness Control Varying the Duty Cycle

Safe Operating Area



Basic 3½-Digit Interface



National Semiconductor

MM5481 LED Display Driver

General Description

The 5481 is a monolithic MOS integrated circuit utilizing N-channel metal gate low threshold, enhancement mode and ion-implanted depletion mode devices. It utilizes the MM5450 die packaged in a 20-pin package making it ideal for a 2 digit display. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected either to V_{DD} or to a separate supply of 11V maximum.

- Wide power supply operation
- TTL compatibility
- Alphanumeric capability
- 2 digit LED driver

Features

- Continuous brightness control
- Serial data input
- No load signal required
- Data enable

Applications

- COPS or microprocessor displays
- Industrial control indicator
- Relay driver
- Instrumentation readouts

Block and Connection Diagrams

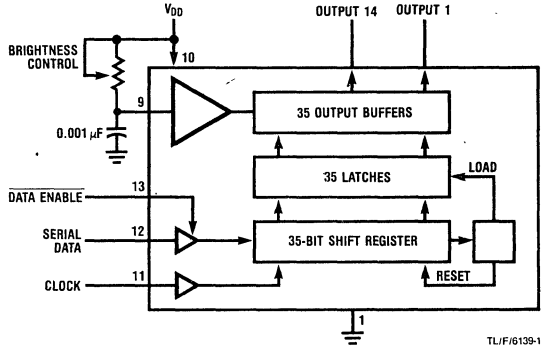


Figure 1
Dual-In-Line Package

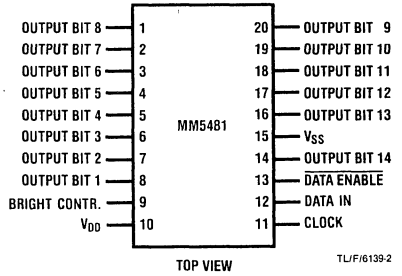


Figure 2

Order Number MM5481N
NS Package N20A

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to $V_{SS}+12V$	Junction Temperature	+150°C
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	450mW at +85°C 860mW at +25°C		

Electrical Characteristics $T_A = -25°C$ to $+85°C$, $V_{DD} = 4.75V$ to $11.0V$, $V_{SS} = 0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
	Input Voltages					
V_{IL}	Logical "0" Level	±10 μA Input Bias	−0.3		0.8	V
V_{IH}	Logical "1" Level	$4.75 \le V_{DD} \le 5.25$	2.2		V_{DD}	V
		$V_{DD} > 5.25$	$V_{DD}-2$		V_{DD}	V
I_{BR}	Brightness Input Current (Note 2)		0		0.75	mA
	Output Sink Current (Note 3)					
I_{OH}	Segment OFF	$V_{OUT} = 3.0V$			10.0	μA
I_{OL}	Segment ON	$V_{OUT} = 1V$ (Note 4)				
		Brightness Input = 0 μA	0		10.0	μA
		Brightness Input = 100 μA	2.0	2.7	4.0	mA
		Brightness Input = 750 μA	15.0		25.0	mA
V_{IBR}	Brightness Input Voltage (Pin 19)	Input Current = 750 μA	3.0		4.3	V
OM	Output Matching (Note 1)				±20	%

AC Electrical Characteristics $T_A = -25°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Input Frequency	(Notes 5 and 6)	DC		500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
	Data Input					
t_{DS}	Set-Up Time		300			ns
t_{DH}	Hold Time		300			ns
t_{DES}	Data Enable Input Set-Up Time		100			ns

Note 1: Output matching is calculated as the percent variation from $I_{MAX} + I_{MIN}/2$.

Note 2: With a fixed resistor on the brightness input pin some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user.

Note 5: AC input waveform specification for test purpose: $t_r \le 20$ ns, $t_f \le 20$ ns, f = 500 kHz, 50% ± 10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5481 uses the MM5450 die which is packaged to operate 2-digit alphanumeric displays with minimal interface to the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 2 signals, serial data and clock. Using a format of a leading "1" followed by the 35 data bits allows data transfer without an additional load signal. The 35 data bits are latched after the 36th bit is complete, thus providing non-multiplexed, direct drive to the display. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF capacitor should be connected to brightness control, pin 9, to prevent possible oscillations.

A block diagram is shown in *Figure 1*. The output current is typically 20 times greater than the current into pin 9, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

Figure 4 shows the input data format. A start bit of logical "1" precedes the 35 bits of data. At the 36th clock a LOAD signal is generated synchronously with the high state of the clock, which loads the 35 bits of the shift registers into the latches. At the low state of the clock a RESET signal is generated which clears all the shift registers for the next set of data. The shift registers are static master-slave configuration. There is no clear for the master portion of the first shift register, thus allowing continuous operation.

There must be a complete set of 36 clocks or the shift registers will not clear.

When the chip first powers ON an internal power ON reset signal is generated which resets all registers and all latches. The START bit and the first clock return the chip to its normal operation.

Figure 5 shows the Output Data Format for the MM5481. Because it uses only 14 of the possible 34 outputs, 20 of the bits are 'Don't Cares'. Note that only alternate groups of 4 outputs are used.

Figure 3 shows the timing relationships between data, clock, and data enable. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1V V_{OUT}. The following equation can be used for calculations.

$$T_j = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(145\,^\circ\text{C/W}) + T_A$$

where:

T_j = junction temperature + 150 °C max.
V_{OUT} = the voltage at the LED driver outputs
I_{LED} = the LED current
145 °C/W = thermal coefficient of the package
T_A = ambient temperature

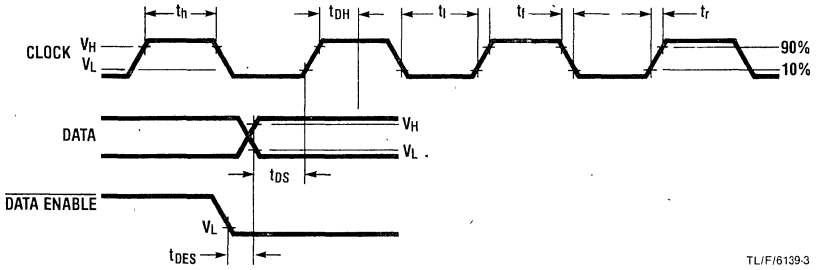


Figure 3. Timing

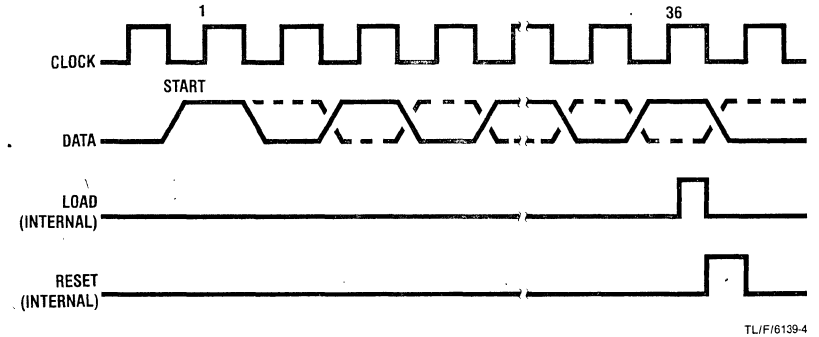


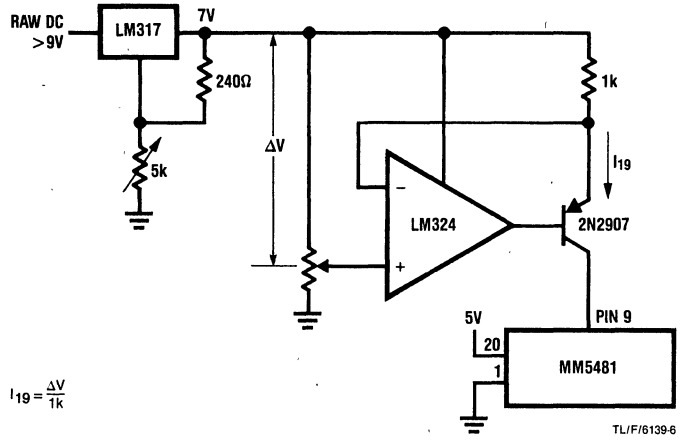
Figure 4. Input Data Format

START	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	5450
START	X	X	X	X	1	2	3	4	X	X	X	X	5	6	7	8	X	X	X	X	9	10	11	12	X	X	X	X	13	14	X	X	X	X	5481

Figure 5. Output Data Format

TL/F/6139-5

Functional Description (Continued)



$I_{19} = \frac{\Delta V}{1k}$

Figure 6. Typical Application of Constant Current Brightness Control

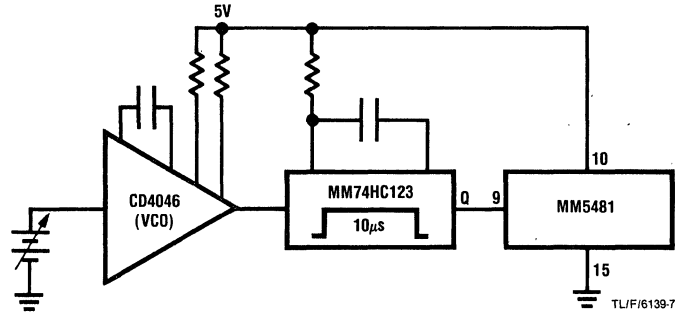
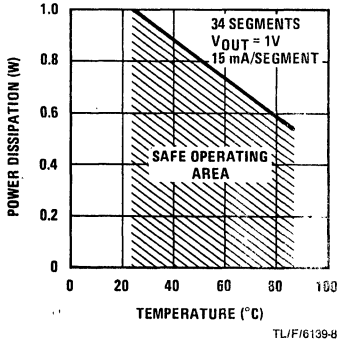
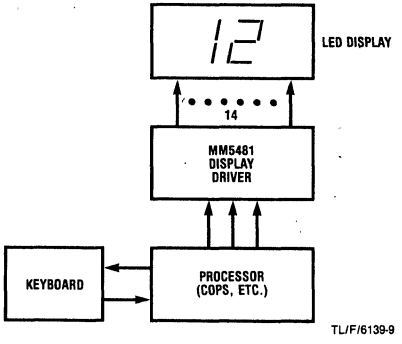


Figure 7. Brightness Control Varying the Duty Cycle

Safe Operating Area



Basic Electronically Tuned Television System



National Semiconductor

MM5483 Liquid Crystal Display Driver

General Description

The MM5483 is a monolithic integrated circuit utilizing CMOS metal-gate low-threshold enhancement mode devices. It is available in a 40-pin molded package. The chip can drive up to 31 segments of LCD and can be cascaded to increase this number. This chip is capable of driving a 4½-digit 7-segment display with minimal interface between the display and the data source.

The MM5483 stores the display data in latches after it is latched in, and holds the data until another load pulse is received.

Features

- Serial data input
- Serial data output
- Wide power supply operation
- TTL compatibility
- 31 segment outputs
- Alphanumeric and bar graph capability
- Cascade capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Remote displays

Block and Connection Diagrams

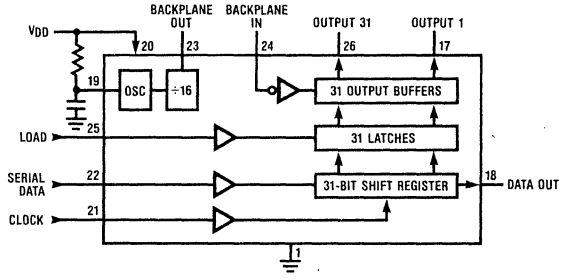


Figure 1

Dual-in-Line Package

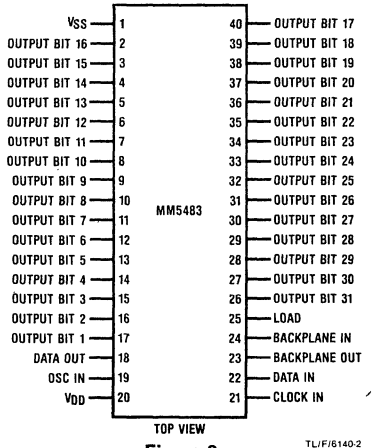


Figure 2

Order Number MM5483N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to $V_{SS}+10V$	Power Dissipation	300 mW at +85°C 350 mW at +25°C
Operating Temperature	−40°C to +85°C		
Storage Temperature	−65°C to +150°C	Junction Temperature	+150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

T_A within operating range, $V_{DD}=3.0V$ to 10V, $V_{SS}=0V$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Power Supply		3.0		10	V
Power Supply Current	R = 1M, C = 470pF, Outputs Open				
	$V_{DD}=3.0V$		9	15	μA
	$V_{DD}=5.0V$		17	25	μA
	$V_{DD}=10.0V$		35	45	μA
	OSC = 0V, Outputs Open, BPIN = 32Hz, $V_{DD}=3.0V$		1.5	2.5	μA
Input Voltage Levels	Load, Clock, Data				
Logic "0"	$V_{DD}=5.0V$			0.9	V
Logic "1"	$V_{DD}=5.0V$	2.4			V
Logic "0"	$V_{DD}=3.0V$			0.4	V
Logic "1"	$V_{DD}=3.0V$	2.0			V
Output Current Levels					
Segments and Data Out					
Sink	$V_{DD}=3.0V$, $V_{OUT}=0.3V$	20			μA
Source	$V_{DD}=3.0V$, $V_{OUT}=2.7V$	20			μA
BPOUT					
Sink	$V_{DD}=3.0V$, $V_{OUT}=0.3V$	320			μA
Source	$V_{DD}=3.0V$, $V_{OUT}=2.7V$	320			μA

AC Electrical Characteristics

$V_{DD} \geq 4.7V$, $V_{SS}=0V$ unless otherwise specified.

Symbol	Parameter		Min	Typ	Max	Units
f_C	Clock Frequency, $V_{DD}=3V$				500	kHz
t_{CH}	Clock Period High	(Notes 1, 2)	500			ns
t_{CL}	Clock Period Low		500			ns
t_{DS}	Data Set-Up Before Clock		300			ns
t_{DH}	Data Hold Time After Clock		100			ns
t_{LW}	Minimum Load Pulse Width		500			ns
t_{LTC}	Load to Clock		400			ns
t_{CDO}	Clock to Data Valid			400	750	ns

Note 1: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 500 kHz, 50% ± 10% duty cycle.

Note 2: Clock input rise and fall times must not exceed 300 ns.

Note 3: Output offset voltage is ± 50 mV with $C_{SEGMENT}=250$ pF, $C_{BP}=8750$ pF.

Functional Description

A block diagram for the MM5483 is shown in *Figure 1* and a package pinout is shown in *Figure 2*. *Figure 3* shows a possible 3-wire connection system with a typical signal format for *Figure 3*. Shown in *Figure 4*, the load input is an asynchronous input and lets data through from the shift register to the output buffers any time it is high. The load input can be connected to V_{DD} for 2-wire control as shown in *Figure 5*. In the 2-wire control mode, 31 bits (or less depending on the number of segments used) of data are clocked into the MM5483 in a short time frame (with less than 0.1 second there probably will be no noticeable flicker) with no more clocks until new information is to be displayed. If data was slowly clocked in, it can be seen to "walk" across the display in the 2-wire mode. An AC timing diagram can be seen in *Figure 6*. It should be noted that data out is not a TTL-compatible output.

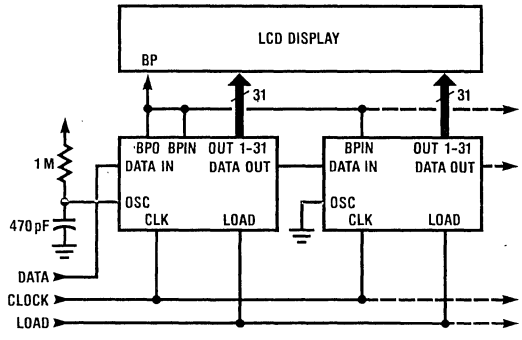


Figure 3. Three-Wire Control Mode

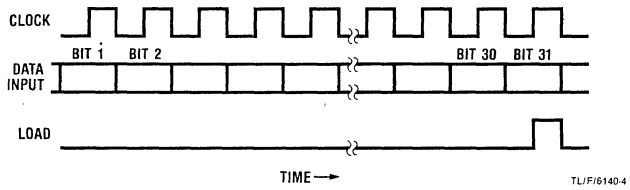


Figure 4. Data Format Diagram

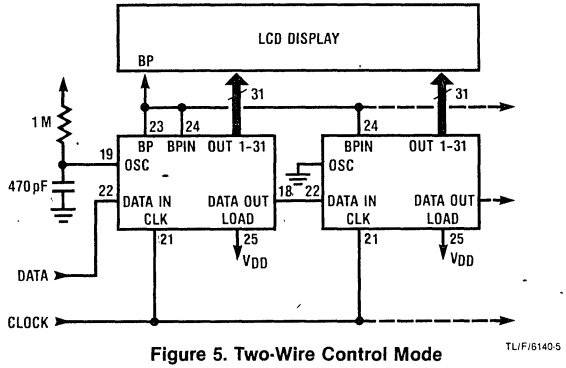


Figure 5. Two-Wire Control Mode

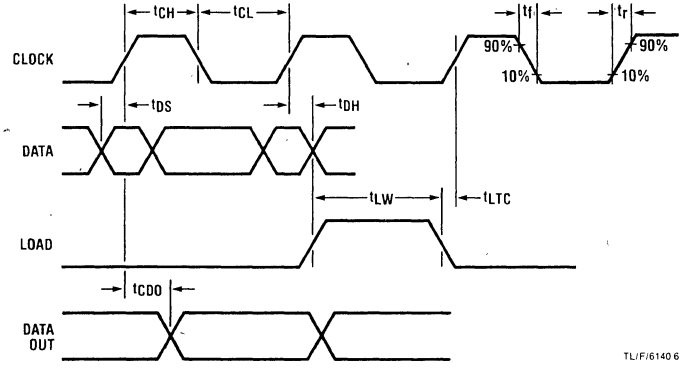


Figure 6. Timing Diagram

National Semiconductor

MM5484, MM5485 16-, 11-Segment LED Display Drivers

General Description

The MM5484, MM5485 are low threshold N-channel metal gate circuits using low threshold enhancement and ion implanted depletion devices. the MM5484 is available in a 22-pin molded package and is capable of driving 16 LED segments while the MM5485 is available in a 16-pin molded package and is capable of driving 11 LED segment outputs.

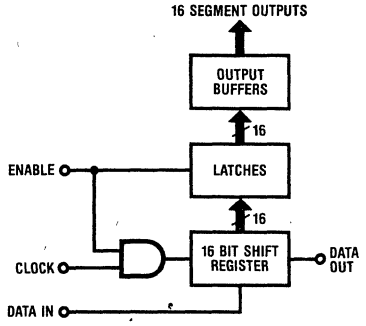
Features

- Serial data input
- Wide power supply operation
- 16 or 11 outputs, 15mA sink capability
- MM5484 is cascadeable
- TTL compatibility
- No load signal required
- Non multiplex display
- 2½ digit capability—MM5484
  1½ digit capability—MM5485

Applications

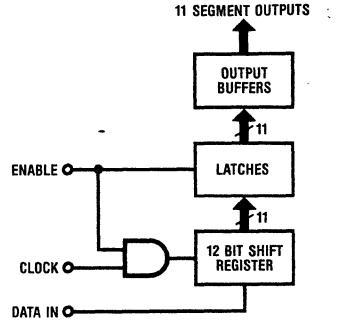
- COPS™ or microprocessor displays
- Instrumentation readouts
- Industrial control indicator
- Relay driver

Block and Connection Diagrams



TL/F/6141-1

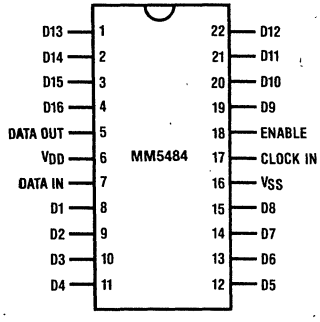
Figure 1. MM5484



TL/F/6141-2

Figure 2. MM5485

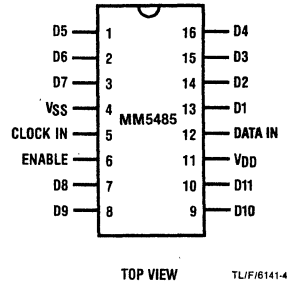
Dual-In-Line Package



TOP VIEW TL/F/6141-3

Order Number MM5484N
See NS Package N16E

Dual-In-Line Package



TOP VIEW TL/F/6141-4

Order Number MM5485N
See NS Package N16E

Absolute Maximum Ratings

Voltage at LED outputs	$V_{SS}-0.5V$ to $V_{SS}+12V$	Maximum Power Dissipation	
Voltage at other pins	$V_{SS}-0.5V$ to $V_{SS}+10V$	MM5484	500 mW
Operating Temperature	−40°C to 85°C	MM5485	400 mW
Storage Temperature	−40°C to 150°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics $V_{DD}=4.5$ to 9V, $T_A=-40°C$ to 85°C unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage		4.5		9	V
Supply Current			5	10	mA
Logic One					
Input High Level V_{IH}		2.4		$V_{DD}+0.5$	V
Logic Zero					
Input Low Level V_{IL}		0		0.8	V
Input Current	High or Low Level			±1	μA
Input Capacitance				7.5	pF
Outputs					
Data Output Voltage	(Only for MM5484)				
High Level V_{OH}	$I_{OUT}=0.1$ mA	$V_{DD}-0.5$			V
Low Level V_{OL}	$I_{OUT}=-0.1$ mA			0.5	V
Segment Off (logic zero on input)	$V_{OUT}=12V$ $R_{EXT}=400\ \Omega$			50	μA
Output Current					
Segment On (logic one on input)					
Output Voltage	$I_{OUT}=15$ mA $V_{DD}\geq 6V$		0.5	1.0	V

AC Electrical Characteristics (See Figure 3.) $V_{DD}=4.5$ to 9V, $T_A=-40°C$ to 85°C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_C	Clock Frequency				0.5	MHz
t_h	High Time		0.95			μs
t_l	Low Time		0.95			μs
t_{S1}	Data Setup Time		0.5			μs
t_{H1}	Data Hold Time		0.5			μs
t_{S2}	Enable Setup Time		0.5			μs
t_{H2}	Enable Hold Time		0.5			μs
t_{pd}	Data Out Delay				0.5	μs

Note 1: Under no condition should the power dissipated by the segment driver exceed 50 mW nor the entire chip power dissipation exceed 500 mW for the MM5484 and 400 mW for the MM5485.

Note 2: AC input waveform specification for test purpose: $t_r\leq 20$ ns, $t_f\leq 20$ ns, $f=500$ kHz, 50% ± 10% duty cycle.

Note 3: Clock input rise and fall times must not exceed 500 ns.

Functional Description

The MM5484 and MM5485 are designed to drive LED displays directly. Serial data transfer from the data source to the display driver is accomplished with 3 signals, DATA IN, CLOCK and ENABLE. The signal ENABLE acts as an envelope and only while this signal is at a logic '1' do the circuits recognize the clock signal.

While ENABLE is high, data on the serial data input is transferred and shifted in the internal shift register on the rising clock edge, i.e. a logic '0' to logic '1' transition.

When the ENABLE signal goes to a low (logic zero state), the contents of the shift register is latched and the display will show the new data. While new data is being loaded into the SR the display will continue to show the old data.

For the MM5484, data is output from the serial DATA OUT pin on the falling edge of clock so cascading is made simple with race hazards eliminated.

The MM5485 is essentially a metal mask option of the MM5484 where only 11 segments are used. However, the MM5485 contains a 12-bit shift register and so when entering new data to this device 12 clock pulses should be input with the data in a 'don't care' state for the 12th clock pulse. See Figure 2.

When the chip first powers on, an internal power on reset signal is generated which resets the SR and latches to zero so that the display will be off.

Timing Diagram

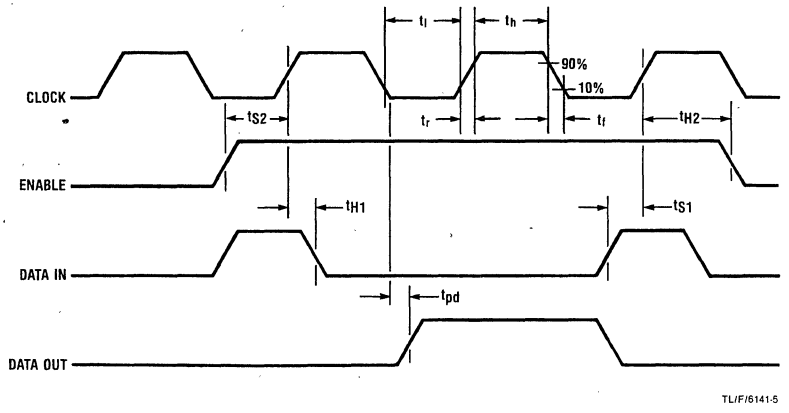


Figure 3

National Semiconductor

MM5486 LED Display Driver

General Description

The MM5486 is a monolithic MOS integrated circuit utilizing N-channel metal-gate low-threshold, enhancement mode and ion-implanted depletion mode devices. It is available in a 40-pin molded dual-in-line package. A single pin controls the LED display brightness by setting a reference current through a variable resistor connected to V_{DD}.

Features

- Continuous brightness control
- Serial data input/output
- External load input
- Cascaded operation capability
- Wide power supply operation
- TTL compatibility
- 33 outputs, 15mA sink capability
- Alphanumeric capability

Applications

- COPS™ or microprocessor displays
- Industrial control indicator
- Relay driver
- Digital clock, thermometer, counter, voltmeter
- Instrumentation readouts
- Reference MOS Brief #1

Block and Connection Diagrams

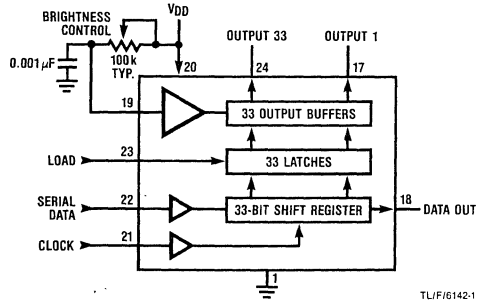


Figure 1

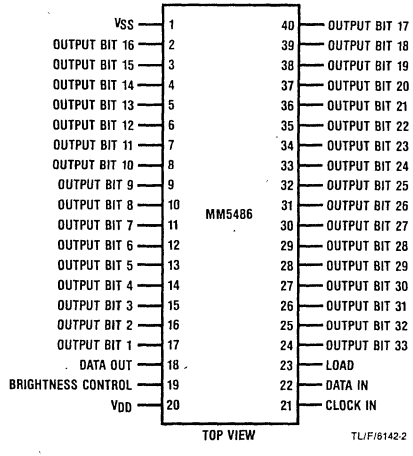


Figure 2

Order Number MM5486N
See Package N40A

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} to V_{SS} +12V	Junction Temperature	+150°C
Operating Temperature	−25°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature	−65°C to +150°C		
Power Dissipation	560 mW at +85°C 1W at +25°C		

Electrical Characteristics

T_A within operating range, $V_{DD} = 4.75V$ to 11.0V, $V_{SS} = 0V$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply		4.75		11	V
I_{DD}	Power Supply Current	Excluding Output Loads			7	mA
	Input Voltages					
V_{IL}	Logic "0" Level	± 10 μA Input Bias	−0.3		0.8	V
V_{IH}	Logic "1" Level	$4.75 \le V_{DD} \le 5.25$	2.2		V_{DD}	V
		$V_{DD} > 5.25$	$V_{DD} - 2$		V_{DD}	V
I_{BR}	Brightness Input (Note 2)		0		0.75	mA
	Output Sink Current (Note 3)					
I_{OH}	Segment OFF	$V_{OUT} = 3.0V$			10	μA
I_{OL}	Segment ON	$V_{OUT} = 1V$ (Note 4)				
		Brightness Input = 0 μA	0		10	μA
		Brightness Input = 100 μA	2.0	2.7	4	mA
		Brightness Input = 750 μA	15		25	mA
I_O	Maximum Segment Current				40	mA
V_{IBR}	Brightness Input Voltage (Pin 19)	Input Current = 750 μA	3.0		4.3	V
OM	Output Matching (Note 1)				± 20	%
	Data Output					
V_{OL}	Logical "0" Level	$I_{OUT} = 0.5$ mA	V_{SS}		0.4	V
V_{OH}	Logical "1" Level	$I_{OUT} = 100$ μA	2.4		V_{DD}	V
	Clock Input	(Notes 5 and 6)				
f_C	Frequency				500	kHz
t_h	High Time		950			ns
t_l	Low Time		950			ns
	Data Input					
t_{DS}	Set-Up Time		300			ns
t_{DH}	Hold Time		300			ns
	Data Enable Input					
t_{DES}	Set-Up Time		100			ns

Note 1: Output matching is calculated as the percent variation $(I_{MAX} + I_{MIN})/2$.

Note 2: With a fixed resistor on the brightness input pin, some variation in brightness will occur from one device to another. Maximum brightness input current can be 2 mA as long as Note 3 and junction temperature equation are complied with.

Note 3: Absolute maximum for each output should be limited to 40 mA.

Note 4: The V_{OUT} voltage should be regulated by the user. See *Figures 6 and 7* for allowable V_{OUT} vs I_{OUT} operation.

Note 5: AC input waveform specification for test purpose: $t_r \le 20$ ns, $t_f \le 20$ ns, f = 500 kHz, 50% ± 10% duty cycle.

Note 6: Clock input rise and fall times must not exceed 300 ns.

Functional Description

The MM5486 is specifically designed to operate four-digit alphanumeric displays with minimal interface with the display and the data source. Serial data transfer from the data source to the display driver is accomplished with 3 signals, serial data, clock, and load. The 33 data bits are latched by a positive-level load signal, thus providing non-multiplexed, direct drive to the display. When load is high, the data in the shift registers is displayed on the output drivers. Outputs change only if the serial data bits differ from the previous time. Display brightness is determined by control of the output current for LED displays. A 0.001 μF capacitor should be connected to brightness control, pin 19, to prevent possible oscillations. The output current is typically 20 times greater than the current into pin 19, which is set by an external variable resistor. There is an internal limiting resistor of 400Ω nominal value.

A block diagram is shown in *Figure 1.*

Figure 4 shows the input data format. Bit "1" is the first bit into the data input pin and it will appear on pin 17. A logical "1" at the input will turn on the appropriate LED. The load signal latches the 33 bits of the shift registers into the latches. The data out pin allows for cascading the shift registers for more than 33 output drivers.

When the chip first powers ON, an internal power ON reset signal is generated which resets all registers and latches. The leading clock returns the chip to its normal operation.

Figure 3 shows the timing relationship between data, clock and data enable. A maximum clock frequency of 0.5 MHz is assumed.

For applications where a lesser number of outputs are used, it is possible to either increase the current per output, or operate the part at higher than 1 V V_{OUT}. The following equation can be used for calculations:

$T_J = (V_{OUT})\,(I_{LED})\,(\text{No. of segments})\,(124°C/W) + T_A$

where:

T_J = junction temperature +150°C max.

V_{OUT} = the voltage at the LED driver outputs

I_{LED} = the LED current

124°C/W = thermal coefficient of the package

T_A = ambient temperature

The above equation was used to plot *Figure 6, Figure 7,* and *Figure 8.*

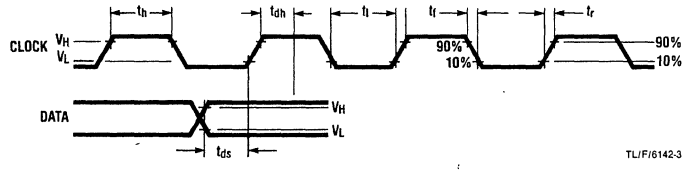
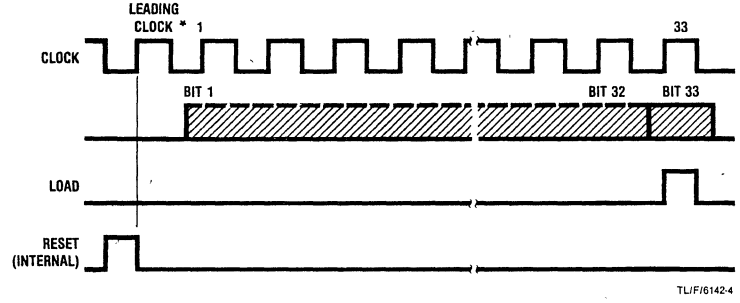


Figure 3



*This leading clock is necessary only after power ON.

Figure 4. Input Data Format

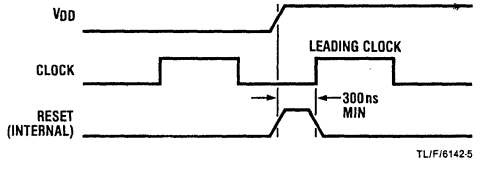


Figure 5

Typical Applications

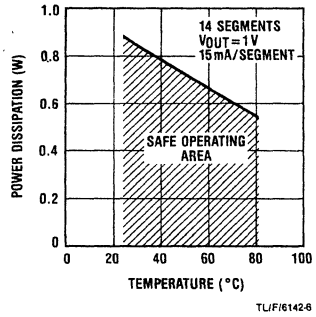


Figure 6

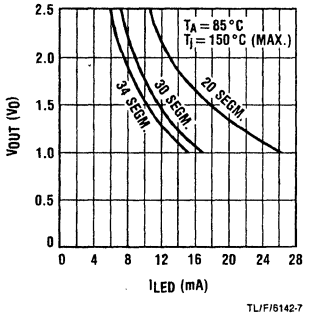


Figure 7

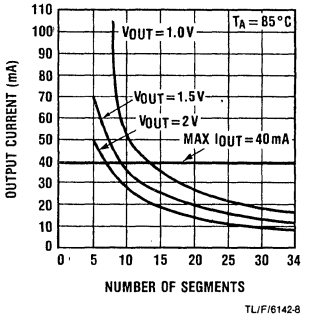


Figure 8

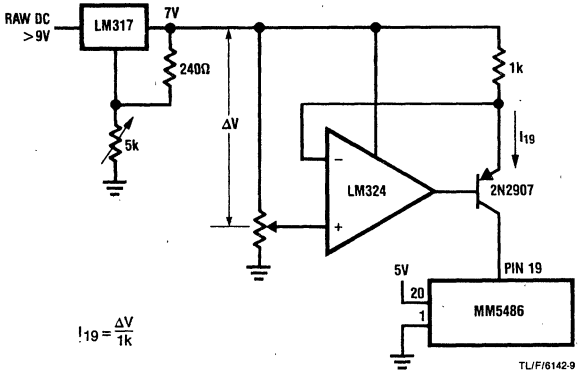


Figure 9. Constant Current Brightness Control

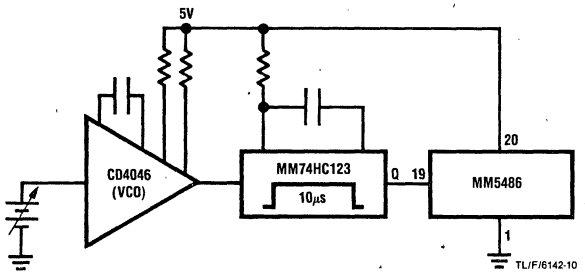
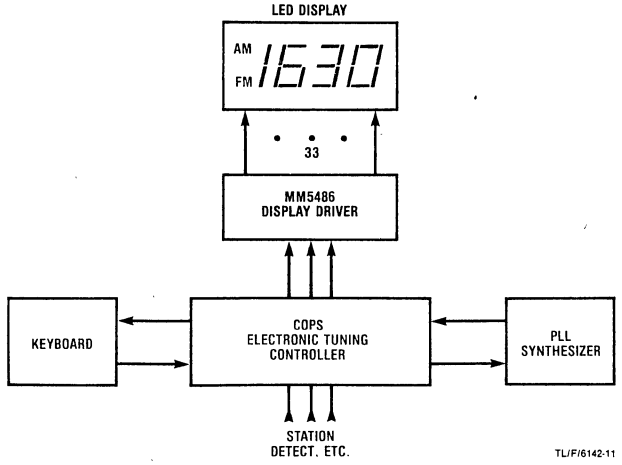


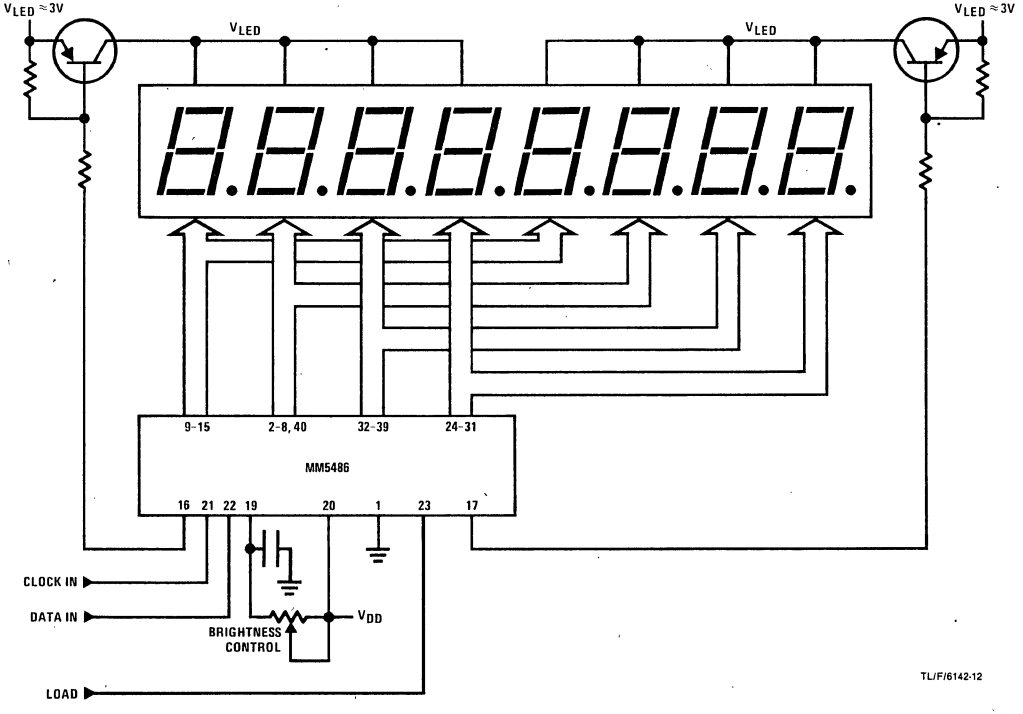
Figure 10. Brightness Control Varying the Duty Cycle

Typical Applications (Continued)

Basic Electronically Tuned Radio System



Duplexing 8 Digits with One MM5486



*This driver has 7 segments only.

National Semiconductor

MM54240 Asynchronous Receiver/Transmitter Remote Controller

General Description

The MM54240 is a monolithic MOS integrated circuit utilizing N-channel low-threshold, enhancement mode and ion-implanted depletion mode devices. The circuit is designed for processor-type remote control applications. The data transmission consists of a pulse width modulated serial data stream of 18 bits. This stream consists of 7 address bits, 1 command bit, 8 data bits, 1 parity bit and 1 dummy bit in that order.

The MM54240 can be operated in two modes; namely "master" and "slave". The master interfaces to a processor bus, and is capable of polling and controlling 128 slave circuits. The slave circuits are interfaced to remote data sources and/or data destinations.

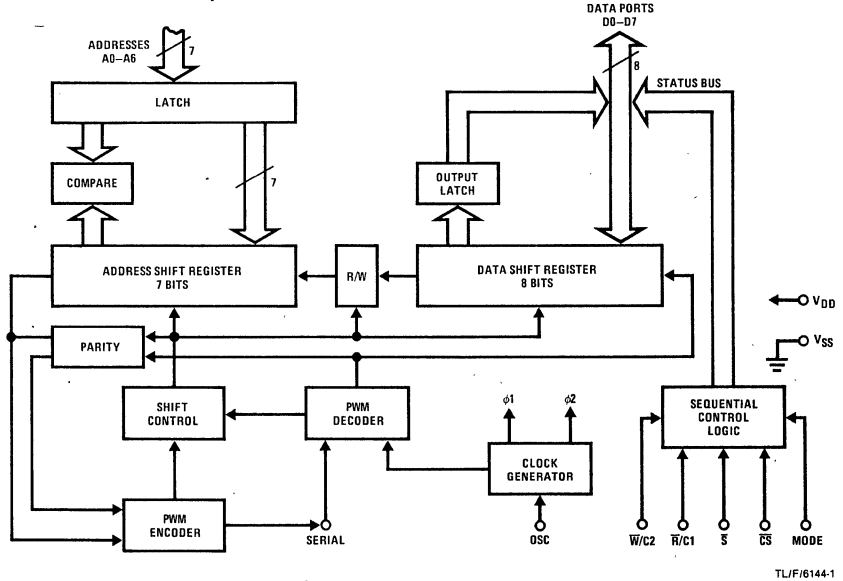
Applications

The MM54240 finds application in transmitting data to and receiving data from remote A-D/D-A, remote microprocessor units, remote digital transducer or remote data peripheral devices.

Features

- Supply voltage range — 4.75V to 11.5V single supply
- Low quiescent current — 5.0 mA maximum
- On-chip oscillator based on inexpensive R-C components
- Pulse width modulation techniques minimize error and maximize frequency tolerance
- Mode input for either master or slave operations
- Chip select ($\overline{CS}$) input in the master mode
- Selectable output port options in the slave mode
- Transmit/receive control output ($\overline{CS}$) in the slave mode

Functional Block Diagram



Pin Configuration

1	V_{SS}
2	D7 (MSB)
3	D6
4	D5
5	D4
6	D3
7	D2
8	D1
9	D0 (LSB)
10	Serial
11	Mode
12	$\overline{CS}$
13	V_{DD}
14	$\overline{R}$/C1
15	$\overline{W}$/C2
16	$\overline{S}$
17	OSC
18	A6 (MSB)
19	A5
20	A4
21	A3
22	A2
23	A1
24	A0 (LSB)

Order Number MM54240N
See NS Package N24C

Absolute Maximum Ratings (exceeding these ratings could result in permanent damage to the device)

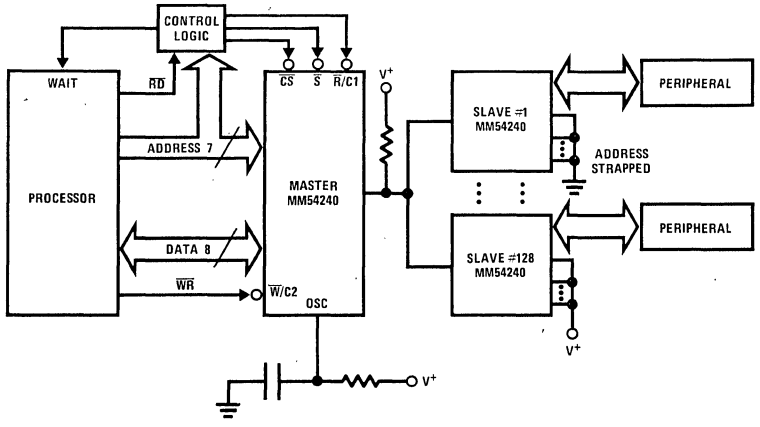
Voltage on Any Pin with Respect to V_{SS}	−0.5V to +12.0V	Storage Temperature	−65°C to +150°C
Operating Temperature	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics T_A within operating range, $V_{SS} = 0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage		4.75		11.5	V
I_{DD}	Supply Current, Quiescent	$V_{DD} = 4.75V$ to 11.5V			5.0	mA
	Input Voltage					
V_{IL}	Logic "0"	$V_{DD} = 4.75V$ to 11.5V	0		0.8	V
V_{IH}	Logic "1"	$V_{DD} = 4.75V$ to 5.25V	2.4		V_{DD}	V
V_{IH}	Logic "1"	$V_{DD} = 5.25V$ to 11.5V	$V_{DD}-2.85$		V_{DD}	V
	Output Current (D0–D7)					
I_{OL}	$V_{OL} = 0.4V$	$V_{DD} = 4.75V$ to 11.5V	2.0			mA
I_{OH}	$V_{OH} = 2.4V$	$V_{DD} = 4.75V$ to 5.25V	200			μA
I_{OH}	$V_{OH} = 0.5\ V_{DD}$	$V_{DD} = 5.25V$ to 11.5V	200			μA
I_{OH}	$V_{OH} = 0.6\ V_{DD}$ (Weak V_{OH})	$V_{DD} = 4.75V$ to 11.5V	0.5		30	μA
I_{OS}	Short Circuit Output Current	$V_{DD} = 4.75V$ to 5.25V		5		mA
	Output ($\overline{CS}$ Slave)					
I_{OL}	$V_{OL} = 0.5V$	$V_{DD} = 4.75V$ to 11.5V	0.4			mA
	Frequency RC Input					
F	For a Fixed $(RC)_1$ (Note 1)	$V_{DD} = 4.75V$ to 7.0V	200	400	600	kHz
F	For a Fixed $(RC)_2$ (Note 1)	$V_{DD} = 7.0V$ to 11.5V	200	400	600	kHz
	Output Current (Serial)					
I_{OL}	$V_{OL} = 0.4V$	$V_{DD} = 4.75V$ to 11.5V	2.0			mA
I_{LEAK}	Open-Drain Leakage	$V_{DD} = 4.75V$ to 11.5V			10	μA
	Internal Input Pull-Up Resistors; $\overline{CS}$, Mode					
I_{IL}	$V_{IN} = V_{SS}$	$V_{DD} = 4.75V$ to 11.5V	15		100	μA

Note 1: $(RC)_1$ or $(RC)_2$: suggested R 1 kΩ–10 kΩ, suggested C 50 pFd–500 pFd.

Typical Application



TL/F/6144-2

Circuit Description

The MM54240 consists of four major logic blocks: Sequential Control, Shift Register, PWM Encoder and PWM Decoder.

Data Ports (D0-D7): The data ports are bidirectional and have three output levels (high, low and weak pull-up). The weak pull-up mode is only available when the MM54240 is a slave device. For the master circuit, the outputs are configured with standard high and low states coincident with properly enabled $\overline{CS}$ and $\overline{R}$. This permits direct interface or buffered interface with the standard bus structure of a processor system. The first three data ports (D0, D1, D2) also serve as status pins coincident with enabled $\overline{CS}$ and $\overline{S}$.* For the slave circuit, specialized input and output options are available by selecting the C1 and C2 inputs. The data port can still be read even if it is configured as an output port.

Address Ports (A0-A6): The address ports are for the input of address information into the MM54240. For the master circuit, the input must be valid during the $\overline{R}$ and $\overline{W}$ command strobes. For the slave circuit, a unique hardwired code must be on the address ports. This code is the address of the slave circuit for addressing purposes. No internal pull-ups are provided.

Mode: This input is low for slave and high (or open) for master selections. An internal pull-up resistor is provided.

Chip Select ($\overline{CS}$): This pin has an internal pull-up resistor to V_{DD}. In the master mode, $\overline{CS}$ is an input and has to be pulled low before the $\overline{R}$, $\overline{W}$, or $\overline{S}$ strobes can be acknowledged. When $\overline{CS}$ is a logic high, the data port pins are high impedance. In the slave mode, $\overline{CS}$ is an output. It is a logic "0" when the circuit is expecting to receive a transmission. $\overline{CS}$ is intended only for controlling a transceiver buffer device. During the receive mode, $\overline{CS}$ will produce a high-going pulse when the dummy bit is received, but prior to the internal address compare. Thus, all slaves (addressed or not addressed) will produce this pulse when receiving a transmission. The slave that is addressed will keep $\overline{CS}$ high until it completes the transmission to the master.

Read/Control 1 ($\overline{R}$/C1): In the master mode, while $\overline{CS}$ is active low, this input can be used to initiate either of the following three operations depending upon the present status of the circuit.

1. To initiate a read command
2. To enable output ports if transmission received is valid
3. To terminate read command if transmission received is incorrect (if master is in state 4 awaiting data from slave, a dummy read will set master to initialize)

In the slave mode, this input, together with $\overline{W}$/C2, selects the specialized output port configuration.

Write/Control 2 ($\overline{W}$/C2): In the master mode, while $\overline{CS}$ is active low, this input can be used to initiate a write command. In the slave mode, this input, together with $\overline{R}$/C1, selects the specialized output port configuration.

Status ($\overline{S}$): In the master mode, while $\overline{CS}$ is active low, this input enables circuit status information to be output at the first three data ports. The other five data ports will be at logic "0". In the slave mode, this input sets all the output (D0-D7) latches to the logic "1" state. In the slave mode, status cannot be interrogated.

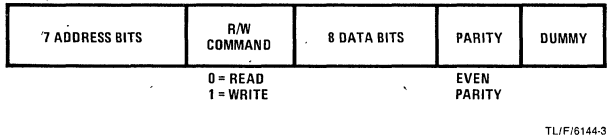
OSC: This input is for connection to a resistor-capacitor circuit for the on-chip oscillator. Frequency tolerance is specified for two voltage ranges. In a master-slave system, if no one circuit has a frequency more than a factor of 2 different from any other circuit, then, valid transmission is guaranteed. Nominal setting is 400 kHz.

Serial: Input and output pin for serial transmission. Output has open-drain configuration.

*The other data ports will output logic "0".

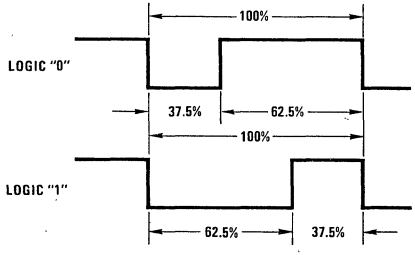
Data Format

1. Serially transmitted data



TL/F/6144-3

2. Pulse width modulation coding

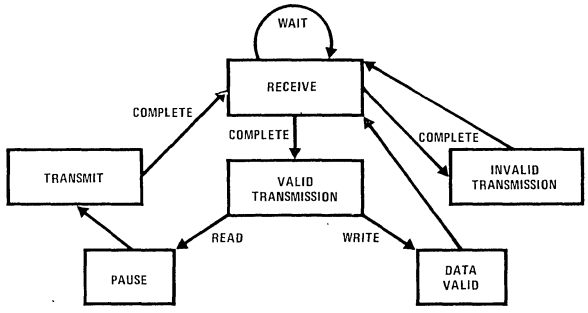


TL/F/6144-4

A bit is equivalent to 96 clocks of the R-C oscillator frequency i.e.; when R-C frequency = 400 kHz, 1 bit = 240 μs, 1 word = 4.32 ms.

Circuit Description (Continued)

Slave Circuit Logic Flow Diagram



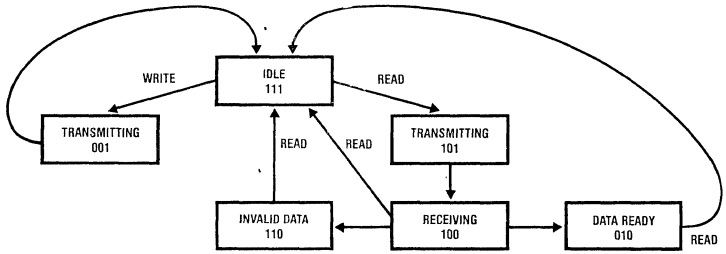
TL/F/6144-5

SPECIALIZED OUTPUT OPTIONS FOR SLAVE CIRCUITS

C1	C2	Description
1	1	All 8 pins are high impedance input ports
0	1	All 8 pins are standard low impedance output ports
0	0	D1-D4 are standard low impedance output ports D5-D8 are high impedance input ports
1	0	* Logic "0" outputs are low impedance output ports Logic "1" outputs are weak pull-ups to V_{DD}

* In this option, the slave data ports can be connected in a wired-OR configuration with open-collector or open-drain outputs on the peripheral.

Master Circuit Logic Flow Diagram



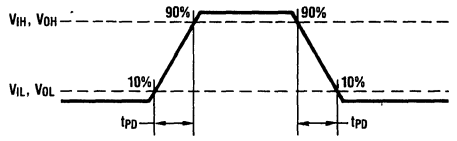
TL/F/6144-6

MASTER CONFIGURATION STATE CHART

Status Register			Description
D2	D1	D0	
0	0	0	Not used
0	0	1	In process of transmitting to slave during write slave mode
0	1	0	Valid data received from slave
0	1	1	Not used
1	0	0	Awaiting data from slave during read slave mode
1	0	1	In process of transmitting to slave during read slave mode
1	1	0	Invalid data received from slave*
1	1	1	Initialization/idle condition

*This state is entered if address or parity do not match.

Timing Diagram Description



TL/F/6144-7

Symbol	Parameter	Min	Max	Units
t_{DS}	Data and Address Set-Up Time	—	2	t_{OSC}
t_{DH}	Data and Address Hold Time	5	—	t_{OSC}
t_{PV}	Serial Port Valid	—	5	t_{OSC}
t_{PF}	Serial Port Float	—	1733	t_{OSC}
t_{DV}	Output Data Valid	—	1.0	μs
t_{DF}	Output Data Float	0		ns
t_1	Overlap Requirement		none	—
t_2	Delay Between Master-Slave Transmission	0.2	1.4	ms
t_3	CS • Function	3	—	t_{OSC}
t_{PD}	Rise and Fall Time	—	100	ns

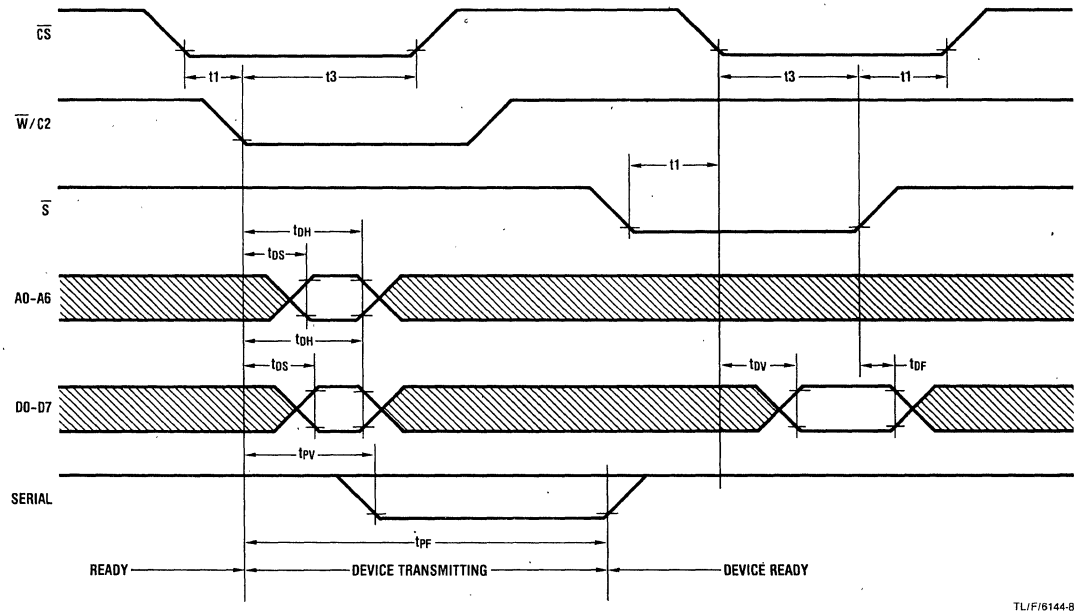
OSCILLATOR CALCULATIONS

Conditions:
$V = 5V \pm 5\%$
$F \approx 400$ kHz
$-40°C \leq T \leq 85°C$

$$F = \frac{K}{RC}$$

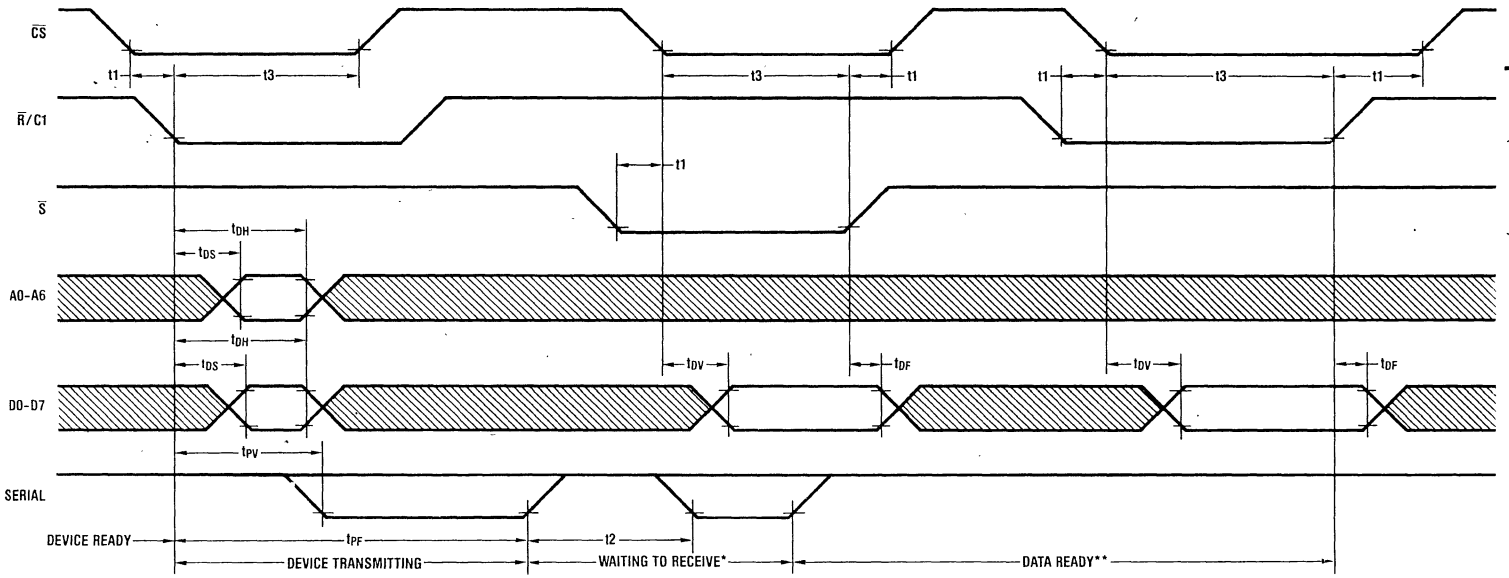
where $0.8 \leq K \leq 1.4$

Master Write Operation



TL/F/6144-8

Master Read Operation



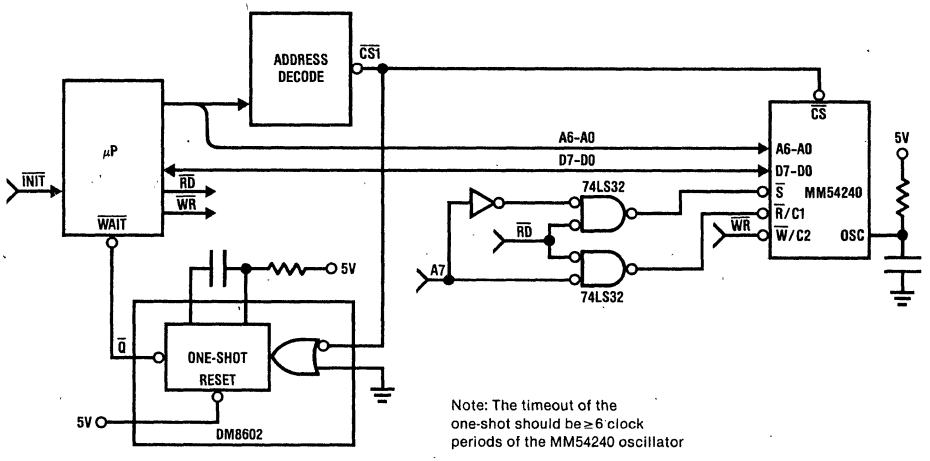
TL/F/6144-9

t1—there is no overlap requirement for CHIP SELECT
t2—delay between master-slave transmission 0.2 ms to 1.4 ms
t3—minimum duration is 3 cycles of oscillator clock

*During "waiting to receive" state, CS coupled with R/C1 will force device into the device ready state.
**If address or parity do not match, the data invalid state is entered. CS coupled with R/C1 will force device into the device ready state.

Typical Applications

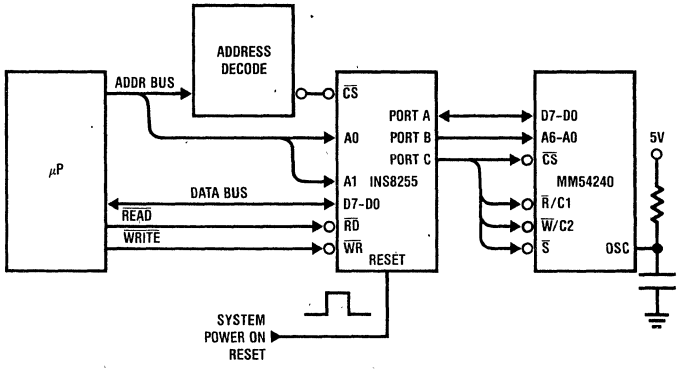
Microprocessor Interface to Master



Note: The timeout of the one-shot should be ≥ 6 clock periods of the MM54240 oscillator

TL/F/6144-10

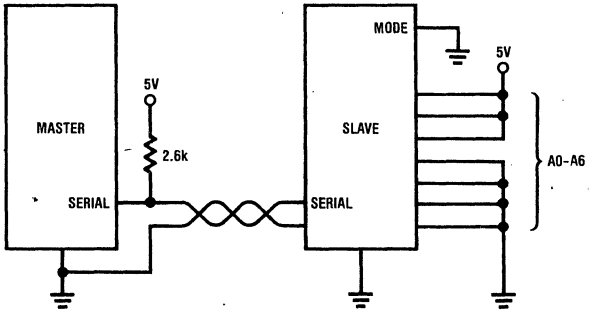
Microprocessor Interface to Master



TL/F/6144-11

Note: The INS8255 is specified by the microprocessor to operate in mode 0. Port A is configured as input or output. Ports B and C are configured as output only. Load ports A and B prior to loading port C.

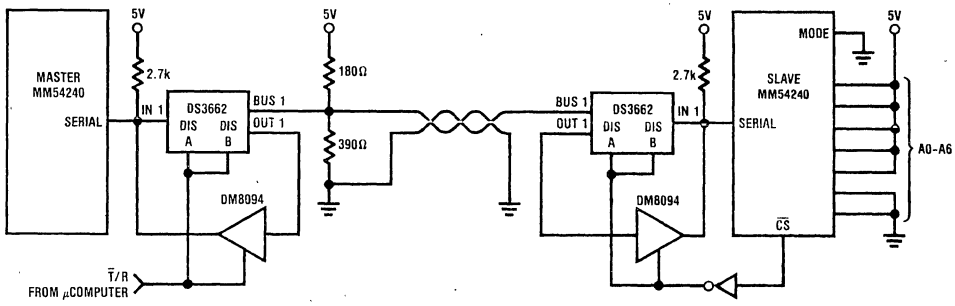
Master to Slave (Short Distance)



TL/F/6144-12

Typical Applications (Continued)

Master to Slave (Long Haul)



TL/F/6144-13

National Semiconductor

MM58167A Microprocessor Real Time Clock

General Description

The MM58167A is a low threshold metal gate CMOS circuit that functions as a real time clock in bus oriented microprocessor systems. The device includes an addressable real time counter, 56 bits of RAM, and two interrupt outputs. A $\overline{\text{POWER DOWN}}$ input allows the chip to be disabled from the rest of the system for standby low power operation. The time base is a 32,768 Hz crystal oscillator.

Features

- Microprocessor compatible (8-bit data bus)
- Milliseconds through month counters
- 56 bits of RAM with comparator to compare the real time counter to the RAM data
- 2 INTERRUPT OUTPUTS with 8 possible interrupt signals
- $\overline{\text{POWER DOWN}}$ input that disables all inputs and outputs except for one of the interrupts
- Status bit to indicate rollover during a read
- 32,768 Hz crystal oscillator
- Four-year calendar (no leap year)
- 24-hour clock

Functional Description

Real Time Counter

The real time counter is divided into 4-bit digits with 2 digits being accessed during any read or write cycle. Each digit represents a BCD number and is defined in Table I. Any unused bits are held at a logical zero during a read and ignored during a write. An unused bit is any bit not necessary to provide a full BCD number. For example tens of hours cannot legally exceed the number 2, thus only 2 bits are necessary to define the tens of hours. The other 2 bits in the tens of hours digit are unused. The unused bits are designated in Table I as dashes.

The addressable portion of the counter is from milliseconds to months. The counter itself is a ripple counter. The ripple delay is less than 60 μs above 4.0V and 300 μs at 2.0V.

RAM

56 bits of RAM are contained on-chip. These can be used for any necessary power down storage or as an alarm latch for comparison to the real time counter. The data in the RAM can be compared to the real time counter on a digit basis. The only digits that are not compared are the unit ten thousandths of seconds and tens of days of the week (these are unused in the real time counter). If the two most significant bits of any RAM digit are ones, then this RAM location will always compare.

The RAM is formatted the same as the real time counter, 4 bits per digit, 14 digits, however there are no unused bits. The unused bits in the real time counter will compare only to zeros in the RAM.

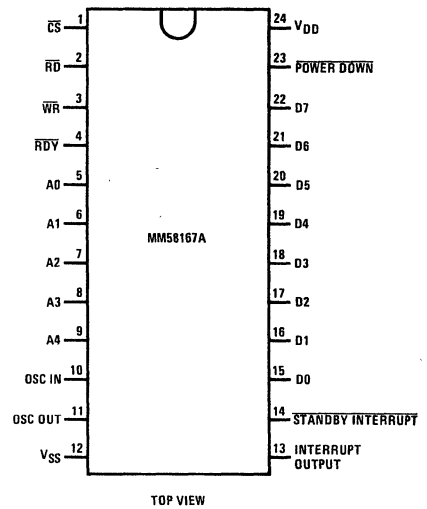
Interrupts and Comparator

There are two interrupt outputs. The first and most flexible is the INTERRUPT OUTPUT (a true high signal). This output can be programmed to provide 8 different output signals. They are: 10 Hz, 1 Hz, once per minute, once per hour, once a day, once a week, once a month, and when a RAM/real time counter comparison occurs. To enable the output a one is written into the interrupt control register at the bit location corresponding to the desired output frequency *(Figure 1)*. Once one or more bits have been set in the interrupt control register, the corresponding counter's rollover to its reset state will clock the interrupt status register and cause the interrupt output to go high. To reset the interrupt and to identify which frequency caused the interrupt, the interrupt status register is read. Reading this register places the contents of the status register on the data bus. The interrupting frequency will be identified by a one in the respective bit position. Removing the read will reset the interrupt.

The second interrupt is the $\overline{\text{STANDBY INTERRUPT}}$ (open drain output, active low). This interrupt occurs when enabled and when a RAM/real time counter comparison occurs. The $\overline{\text{STANDBY INTERRUPT}}$ is enabled by writing a one on the D0 line at address 16_H or disabled by writing a zero on the D0 line. This interrupt is not triggered by the edge of the compare signal, but rather by the level. Thus if the compare is enabled when the $\overline{\text{STANDBY INTERRUPT}}$ is enabled, the interrupt will turn on immediately.

Connection Diagram

Dual-In-Line Package



TOP VIEW

TL/F/6148-1

Order Number MM58167AN
See NS Package N24A

Absolute Maximum Ratings

Voltage at All Pins	$V_{SS}-0.3V$ to $V_{DD}+0.3V$	$V_{DD}-V_{SS}$	6.0V
Operating Temperature	0°C to 70°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature	−65°C to 150°C		

Electrical Characteristics $V_{SS}=0V$, $0°C \le T_A \le 70°C$

Parameter	Conditions	Min	Max	Units
Supply Voltage				
V_{DD}	Outputs Enabled	4.0	5.5	V
V_{DD}	$\overline{\text{POWER DOWN}}$ Mode	2.0	5.5	V
Supply Current				
I_{DD}, Static	Outputs TRI-STATE®			
	$f_{IN}=DC$, $V_{DD}=5.5V$		10	μA
I_{DD}, Dynamic	Outputs TRI-STATE			
	$f_{IN}=32$ kHz, $V_{DD}=5.5V$			
	$V_{IH} \ge V_{DD}-0.3V$			
	$V_{IL} \le V_{SS}+0.3V$		20	μA
I_{DD}, Dynamic	Outputs TRI-STATE			
	$f_{IN}=32$ kHz, $V_{DD}=5.5V$			
	$V_{IH}=2.0V$, $V_{IL}=0.8V$		5	mA
Input Voltage				
Logical Low		0.0	0.8	V
Logical High		2.0	V_{DD}	V
Input Leakage Current	$V_{SS} \le V_{IN} \le V_{DD}$	−1	1	μA
Output Impedance	I/O and INTERRUPT OUT			
Logical Low	$V_{DD}=4.5V$, $I_{OL}=1.6$ mA		0.4	V
Logical High	$V_{DD}=4.5V$, $I_{OH}=-400$ μA	2.4		V
	$I_{OH}=-10$ μA	$0.8\ V_{DD}$		V
TRI-STATE	$V_{SS} \le V_{OUT} \le V_{DD}$	−1	1	μA
Output Impedance	$\overline{\text{RDY}}$ and $\overline{\text{STANDBY}}$ $\overline{\text{INTERRUPT}}$			
	(Open Drain Devices)			
Logical Low, Sink	$V_{DD}=4.5V$, $I_{OL}=1.6$ mA		0.4	V
Logical High, Leakage	$V_{OUT} \le V_{DD}$		10	μA

Functional Description (Continued)

TABLE I. Real Time Counter Format

Counter Addressed		Units D0	D1	D2	D3	Max BCD Code	Tens D4	D5	D6	D7	Max BCD Code
1/10,000 of Seconds	(00_H)	-	-	-	-	0	D4	D5	D6	D7	9
Hundredths and Tenths Sec	(01_H)	D0	D1	D2	D3	9	D4	D5	D6	D7	9
Seconds	(02_H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Minutes	(03_H)	D0	D1	D2	D3	9	D4	D5	D6	-	5
Hours	(04_H)	D0	D1	D2	D3	9	D4	D5	-	-	2
Day of the Week	(05_H)	D0	D1	D2	-	7	-	-	-	-	0
Day of the Month	(06_H)	D0	D1	D2	D3	9	D4	D5	-	-	3
Month	(07_H)	D0	D1	D2	D3	9	D4	-	-	-	1

(-) indicates unused bits

Functional Description (Continued)

TABLE II. Address Codes and Functions

A4	A3	A2	A1	A0	Function
0	0	0	0	0	Counter—Ten Thousandths of Seconds
0	0	0	0	1	Counter—Hundredths and Tenths of Seconds
0	0	0	1	0	Counter—Seconds
0	0	0	1	1	Counter—Minutes
0	0	1	0	0	Counter—Hours
0	0	1	0	1	Counter—Day of Week
0	0	1	1	0	Counter—Day of Month
0	0	1	1	1	Counter—Month
0	1	0	0	0	RAM—Ten Thousandths of Seconds
0	1	0	0	1	RAM—Hundredths and Tenths of Seconds
0	1	0	1	0	RAM—Seconds
0	1	0	1	1	RAM—Minutes
0	1	1	0	0	RAM—Hours
0	1	1	0	1	RAM—Day of Week
0	1	1	1	0	RAM—Day of Month
0	1	1	1	1	RAM—Months
1	0	0	0	0	Interrupt Status Register
1	0	0	0	1	Interrupt Control Register
1	0	0	1	0	Counters Reset
1	0	0	1	1	RAM Reset
1	0	1	0	0	Status Bit
1	0	1	0	1	GO Command
1	0	1	1	0	$\overline{\text{STANDBY INTERRUPT}}$
1	1	1	1	1	Test Mode

All others unused

Functional Description (Continued)

The comparator is a cascaded exclusive NOR. Its output is latched 61 μs after the rising edge of the 1 kHz clock signal (input to the ten thousandths of seconds counter). This allows the counter to ripple through before looking at the comparator. For operation at less than 4.0V, the thousandths of seconds counter should not be included in a compare because of the possibility of having a ripple delay greater than 61 μs. (For output timing see Interrupt Timing.)

Power Down Mode

The $\overline{\text{POWER DOWN}}$ input is essentially a second chip select. It disables all inputs and outputs except for the $\overline{\text{STANDBY INTERRUPT}}$. When this input is at a logical zero, the device will not respond to any external signals. It will, however, maintain timekeeping and turn on the $\overline{\text{STANDBY INTERRUPT}}$ if programmed to do so. (The programming must be done before the $\overline{\text{POWER DOWN}}$ input goes to a logical zero.) When switching V_{DD} to the standby or power down mode, the $\overline{\text{POWER DOWN}}$ input should go to a logical zero at least 1 μs before V_{DD} is switched. When switching V_{DD} all other inputs must remain between $V_{SS} - 0.3V$ and $V_{DD} + 0.3V$. When restoring V_{DD} to the normal operating mode, it is necessary to insure that all other inputs are at valid levels before switching the $\overline{\text{POWER DOWN}}$ input back to a logical one. These precautions are necessary to insure that no data is lost or altered when changing to or from the power down mode.

Counter and RAM Resets; GO Command

The counters and RAM can be reset by writing all 1's (FF) at address 12_H or 13_H respectively.

A write pulse at address 15_H will reset the thousandths, hundredths, tenths, units, and tens of seconds counters. This GO command is used for precise starting of the clock. The data on the data bus is ignored during the write. If the seconds counter is at a value greater than 39 when the GO is issued, the minute counter will increment; otherwise the minute counter is unaffected. This command is not necessary to start the clock, but merely a convenient way to start precisely at a given minute.

Status Bit

The status bit is provided to inform the user that the clock is in the process of rolling over when a counter is read. The status bit is set if this 1 kHz clock occurs during or after any counter read. This tells the user that the clock is rippling through the real time counter. Because the clock is rippling, invalid data may be read from the counter. If the status bit is set following a counter read, the counter should be reread.

The status bit appears on D0 when address 14_H is read. All the other data lines will be zero. The bit is set when a logical one appears. This bit should be read every time a counter read or after a series of counter reads are done. The trailing edge of the read at address 14_H will reset the status bit.

Oscillator

The oscillator used is the standard Pierce parallel resonant oscillator. Externally, 2 capacitors, a 20 MΩ resistor and the crystal are required. The 20 MΩ resistor is connected between OSC IN and OSC OUT to bias the internal inverter in the linear region. For micropower crystals a resistor in series with the oscillator output may be necessary to insure the crystal is not overdriven. This resistor should be approximately 200 kΩ. The capacitor values should be typically 20 pF–25 pF. The crystal frequency is 32,768 Hz.

The oscillator input can be externally driven, if desired. In this case the output should be left floating and the input levels should be within 0.3V of the supplies.

A ground line or ground plane between pins 9 and 10 may be necessary to prevent interference of the oscillator by the A4 address.

Control Lines

The $\overline{\text{READ}}$, $\overline{\text{WRITE}}$, and $\overline{\text{CHIP SELECT}}$ signals are active low inputs. The $\overline{\text{READY}}$ signal is an open drain output. At the start of each read or write cycle the $\overline{\text{READY}}$ line (open drain) will pull low and will remain low until valid data from a chip read appears on the bus or data on the bus is latched in during a write. $\overline{\text{READ}}$ and $\overline{\text{WRITE}}$ must be accompanied by a $\overline{\text{CHIP SELECT}}$ (see *Figures 3 and 4* for read and write cycle timing).

During a read or write, address bits must not change while chip select and control strobes are low.

Test Mode

The test mode is merely a mode for production testing. It allows the counters to count at a higher than normal rate. In this mode the 32 kHz oscillator input is connected directly to the ten thousandths of seconds counter. The chip select and write lines must be low and the address must be held at $1F_H$.

Functional Description (Continued)

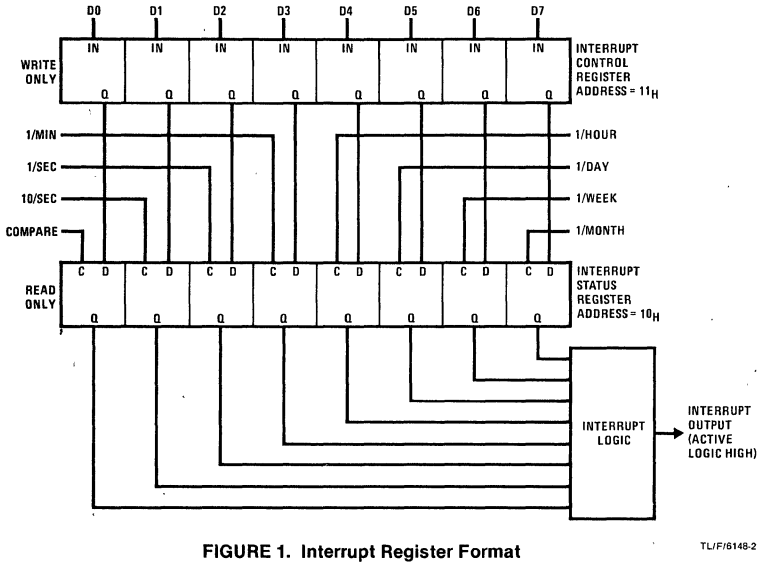


FIGURE 1. Interrupt Register Format

Standby Interrupt Typical Characteristics

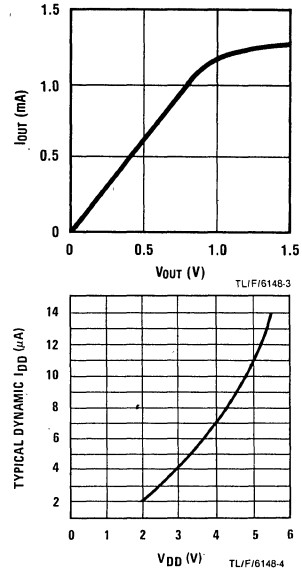


FIGURE 2. Typical Supply Current vs Supply Voltage During Power Down

Interrupt Timing $0°C \le T_A \le 70°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

Sym	Parameter	Min	Max	Units
t_{INTON}	Status Register Clock to INTERRUPT OUTPUT (Pin 13) High (Note 1)		5	μs
t_{SBYON}	Compare Valid to $\overline{\text{STANDBY INTERRUPT}}$ (Pin 14) Low (Note 1)		5	μs
t_{INTOFF}	Trailing Edge of Status Register Read to INTERRUPT OUTPUT Low		5	μs
t_{SBYOFF}	Trailing Edge of Write Cycle (D0 = 0; Address = 16_H) to $\overline{\text{STANDBY INTERRUPT}}$ Off (High Impedance State)		5	μs

Note 1: The status register clocks are: the corresponding counter's rollover to its reset state or the compare becoming valid. The compare becomes valid 61 μs after the 1/10,000 of a second counter is clocked, if the real time counter data matches the RAM data.

Read Cycle Timing $0°C \le T_A \le 70°C$, $4.5V \le V_{DD} \le 5.5V$, $V_{SS} = 0V$

Sym	Parameter	Min	Max	Units
t_{AR}	Address Bus Valid to Read Strobe	100		ns
t_{CSR}	Chip Select to Read Strobe	0		ns
t_{RRY}	Read Strobe to Ready Strobe		150	ns
t_{RYD}	Ready Strobe to Data Valid		800	ns
t_{AD}	Address Bus Valid to Data Valid		1050	ns
t_{RH}	Data Hold Time From Trailing Edge of Read Strobe	0		ns
t_{HZ}	Trailing Edge of Read Strobe to TRI-STATE Mode		250	ns
t_{RYH}	Read Hold Time after Ready Strobe	0		ns
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	50		ns
t_{RYDV}	Rising Edge of Ready to Data Valid		100	ns

Note 2: If $t_{AR} = 0$ and Chip Select, Address Valid or Read are coincident then they must exist for 1050 ns.

Write Cycle Timing $0°C \leq T_A \leq 70°C$, $4.5V \leq V_{DD} \leq 5.5V$, $V_{SS} = 0V$

Sym	Parameter	Min	Max	Units
t_{AW}	Address Valid to Write Strobe	100		ns
t_{CSW}	Chip Select to Write Strobe	0		ns
t_{DW}	Data Valid before Write Strobe	100		ns
t_{WRY}	Write Strobe to Ready Strobe		150	ns
t_{RY}	Ready Strobe Width		800	ns
t_{RYH}	Write Hold Time after Ready Strobe	0		ns
t_{WD}	Data Hold Time after Write Strobe	110		ns
t_{WA}	Address Hold Time after Write Strobe	50		ns

Note 3: If data changes while $\overline{CS}$ and $\overline{WR}$ are low, then they must remain coincident for 1050 ns after the data change to ensure a valid write.

Data bus loading is 100 pF.

Ready output loading is 50 pF and 3 kΩ pull-up.

Input and output AC timing levels:
Logical one = 2.0V
Logical zero = 0.8V

Read and Write Cycle Timing Diagrams

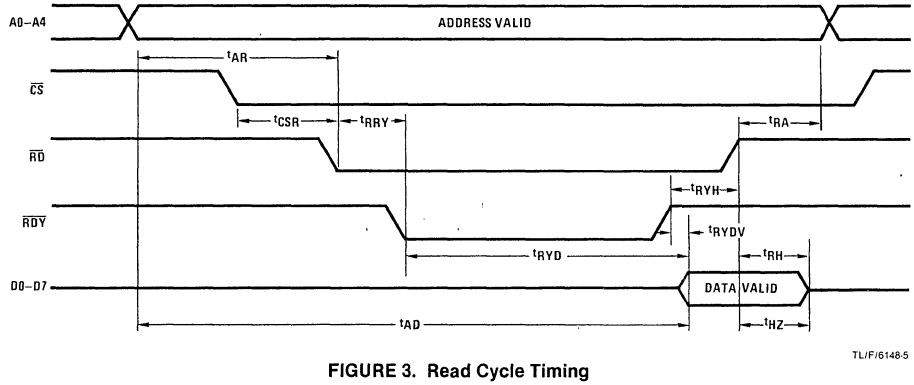


FIGURE 3. Read Cycle Timing

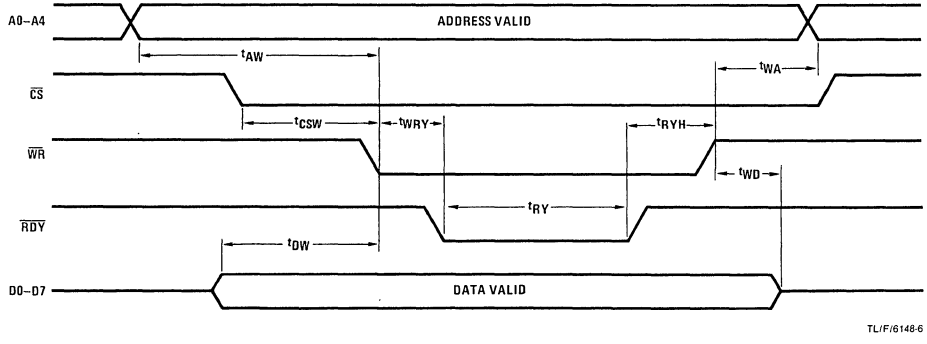
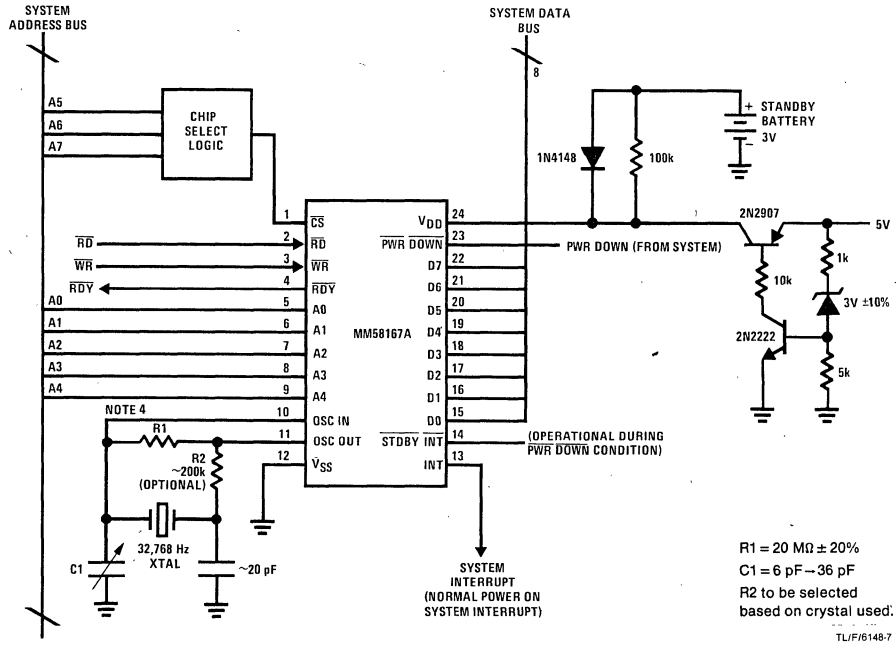


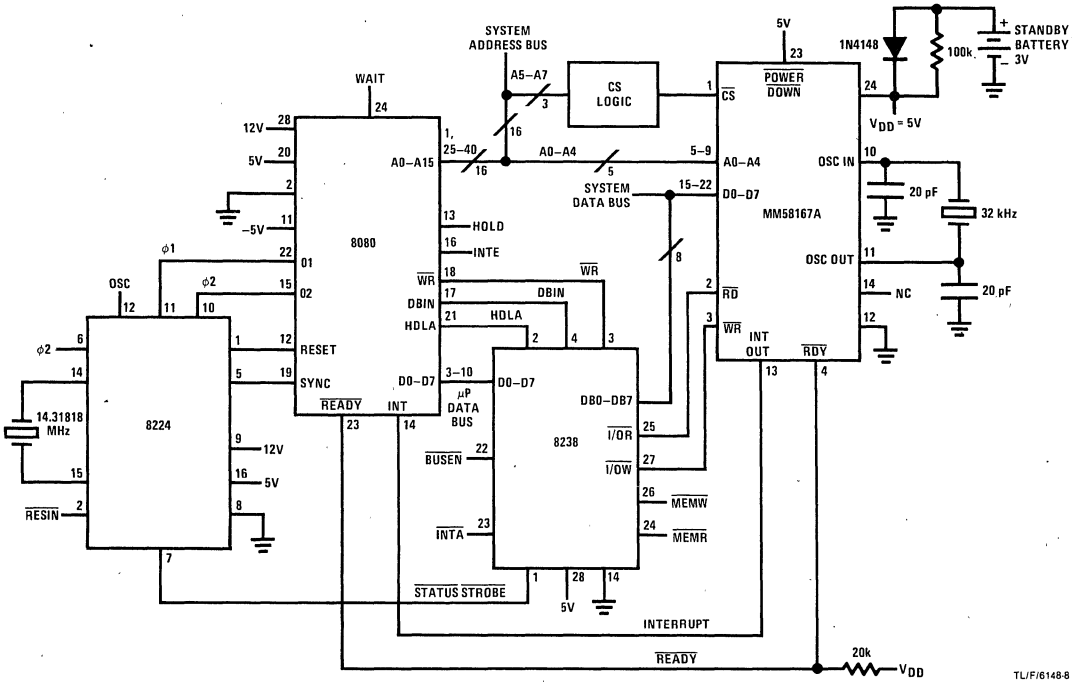
FIGURE 4. Write Cycle Timing

Typical Applications



Note 4: A ground line or ground plane guard trace should be included between pins 9 and 10 to insure the oscillator is not disturbed by the address line.

FIGURE 5. Typical Connection Diagram



Note 5: Must use 8238 or equivalent logic to insure advanced I/OW pulse; so that the ready output of the MM58167A is valid by the end of $\phi 2$ during the T2 microcycle.

Note 6: $t_{\phi 2} \geq t_{RS8080} + t_{DL8238} + t_{WRY58167A}$.

FIGURE 6. 8080 System Interface with Battery Backup

Block Diagram

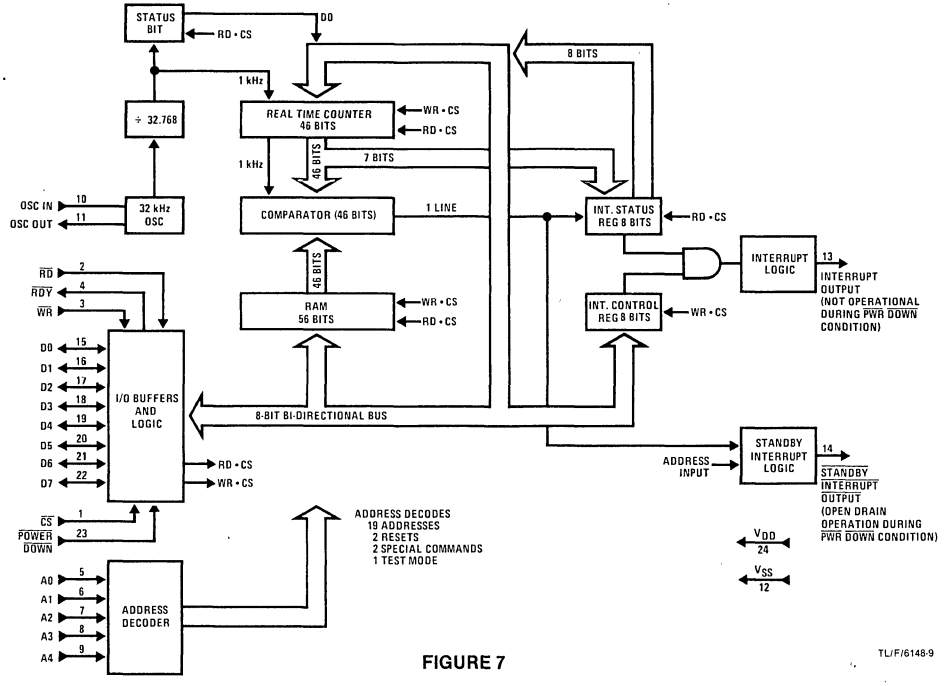


FIGURE 7

TL/F/6148-9

National Semiconductor

MM58174A Microprocessor-Compatible Real-Time Clock

General Description

The MM58174A is a low-threshold metal-gate CMOS circuit that functions as a real-time clock and calendar in bus-oriented microprocessor systems. The device includes an interrupt timer which may be programmed to one of three times. Time-keeping is maintained down to 2.2V to allow low power standby battery operation. The timebase is generated from a 32768Hz crystal-controlled oscillator.

- TTL compatible
- Low power standby operation (2.2V, 10μA)
- Low cost internally biased oscillator
- Low cost 16-pin dual-in-line package
- Available for commercial and military temperature ranges

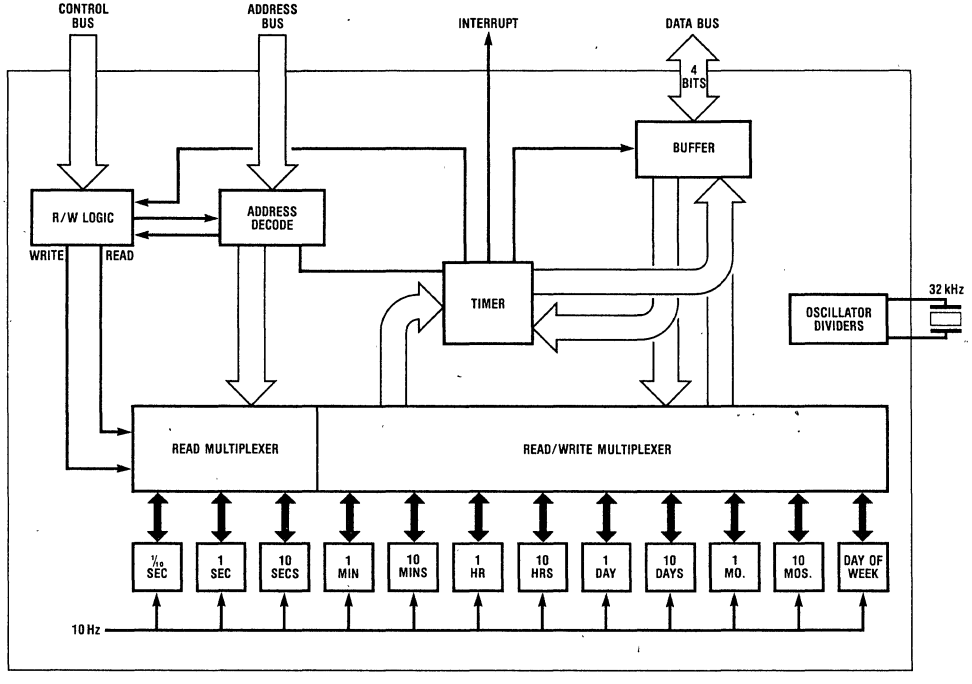
Features

- Microprocessor compatible
- Tenths of seconds, seconds, tens of seconds, minutes, tens of minutes, day of week, days, tens of days, months, tens of months, independent registers
- Automatic leap year calculation
- Internal pull-ups to safeguard data
- Protection for read during data changing
- Independent interrupt system with open drain output

Applications

- Point-of-sale terminals
- Word processors
- Teller terminals
- Event recorders
- Microprocessor-controlled instrumentation
- Microprocessor time clock
- TV/VCR reprogramming
- Intelligent telephone

Block Diagram



TL/F/6681-1

Figure 1

Absolute Maximum Ratings

Voltage at All Inputs and Outputs $V_{DD} + 0.3$ to $V_{SS} - 0.3$
Operating Temperature
MM58174AN $-40°C$ to $+85°C$
Storage Temperature $-65°C$ to $+150°C$
$V_{DD} - V_{SS}$ 6.5V
Lead Temperature (Soldering, 10 seconds) 300°C

Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{SS} = 0V$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply Voltage	Standby mode (no READ or WRITE instructions)	2.2		5.5	V
		Operational mode	4.5		5.5	V
I_{DD}	Supply Current	$V_{DD} = 2.2V$ (Standby) MM58174AN			10	μA
		$V_{DD} = 5V$ (Operating)			1	mA
	Input Logic Levels For Signals: $AD_0 - AD_3$, $DB_0 - DB_3$, WR, RD, CS	$V_{DD} = 5V$				
	Logic "1"		2			V
	Logic "0"				0.8	V
	Input Capacitance				10	pF
	Input Current Levels	$V_{DD} = 5V$				
	Current to V_{SS} For Signals: $AD_0 - AD_3$, $DB_0 - DB_3$, $\overline{RD}$	$V_{IN} = V_{DD}$			30	μA
	Internal Resistor to V_{DD} For Signals:					
	$\overline{WR}$		30	100		kΩ
	$\overline{CS}$		30	100		kΩ
	Output Logic Levels For Signals: $DB_0 - DB_3$	$V_{DD} = 5V$				
	Logic "1"	$I_{OH} = 0.1mA$	2.4			V
	Logic "0"	$I_{OL} = 1.6mA$			0.4	V
	INTERRUPT (Open Drain)					
	Logic "0"	For $I_{DS} = -1.6$ mA			0.4	V
	Off Leakage	$V_{OUT} = 5V$			5	μA

7

Functional Description

The MM58174 is a microprocessor bus-oriented real-time clock. The circuit includes addressable real-time counters for tenths of seconds through months and a write only register for leap year calculation. The counters are arranged as bytes of four bits each. When addressed a byte will appear on the data I/O bus so that each word can be accessed independently. If any byte does not contain four bits (e.g. days of the week uses only 3 bits), the unused bits will be unrecognized during a write operation and tied to V_{SS} during a read operation.

The addressable reset latch causes the pre-scaler, tenths of seconds, seconds, and tens of seconds to be held in a reset condition. If a register is updated during a read operation the I/O data is prevented from updating and a subsequent read will return the illegal b.c.d. code '1111'. The interrupt timer may be programmed for intervals of 0.5 second, 5 seconds, or 60 seconds and may be coded as a single or repeated operation. The open drain interrupt output is pulled to V_{SS} when the timer times out and reading the interrupt register provides the internal selected information.

Circuit Description

The block diagram shown in Figure 1 shows the structure of the CMOS clock chip. A 16-pin DIL package is used.

Crystal Oscillator

This consists of a CMOS inverter/amplifier with on-chip bias resistor and capacitors. A single 6-36 pF trimmer is all that is required to fine tune the crystal (see Figure 2). However, for improved stability, some crystals may require a capacitor of typical value 20 pF to be added between pin 14 and ground. The output of the oscillator is blocked by the start/stop F/F.

Non-Integer Divider

This counter divides the incoming 32,768 Hz frequency by 15/16 down to 30,720 Hz.

Fixed Divider (512)

This is a standard 9-stage binary ripple counter. Output frequency is 60 Hz. This counter is reset to zero by start/stop F/F.

Fixed Divider (6)

This is a 3-stage Johnson counter with a 10 Hz output signal. This counter is reset to zero state by the start/stop F/F.

Synchronization Stage

Both 10 Hz and 32,768 Hz clocks are fed into this section. It is used to generate a pulse of 15.25 μs width on the rising edge of each 10 Hz pulse.

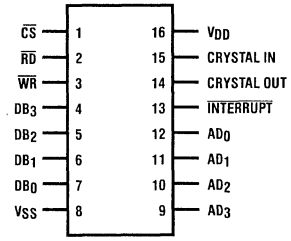
This pulse is used to increment all the seconds, minutes, hours, days, months, and year counter and also to set the data changed F/F.

Data Changed F/F

This is set by the rising edge of each 10 Hz pulse to indicate that the clock value has changed since the last read operation. It is reset by any clock read command.

Connection Diagram

Dual-In-Line Package



Top View TL/F/6681-2

Order Number MM58174AN
See NS Package N16E

The flip-flop sets all data bus bits to a "1" during RD time indicating that a register has been updated. This transient condition may occur at the end of the Read Data strobe. Hence, invalid data may still be read from the clock, if the strobe width was less than 3 μs.

The possibility may be overcome by implementing a further read of the tenths of seconds register at the end of every series of reads (starting with a read at the tenths of seconds register) and checking for unchanged data.

Seconds Counters

There are three counters for Seconds:

a) tenths of seconds

b) units of seconds

c) tens of seconds

The outputs of all three counters can be separately multiplexed on to the command 4-bit output bus. Table I shows the address decoding for each counter. All three counters are reset to zero by the start/stop F/F.

Minutes Counters

There are two Minutes counters:

a) units of minutes

b) tens of minutes

Both counters are parallel loaded with data from the 4-bit input bus when addressed by the microprocessor and a Write Data Strobe pulse given. Similarly, the output of both counters can be read separately onto the common 4-bit output bus (Table I).

Hours Counters

There are two Hours counters which will count in a 24-hour mode:

a) units of hours

b) tens of hours

Both counters have identical parallel load and read multiplex features to the Minutes counters.

Seven Day Counter

There is a 7-state counter which increments every 24 hours. It will have identical parallel load and read multiplex capabilities to the Minutes and Hours counters. The counter counts cyclically from 1-7.

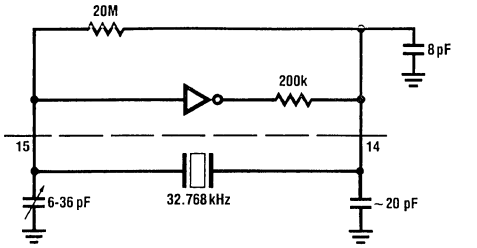


Figure 2. Crystal Oscillator

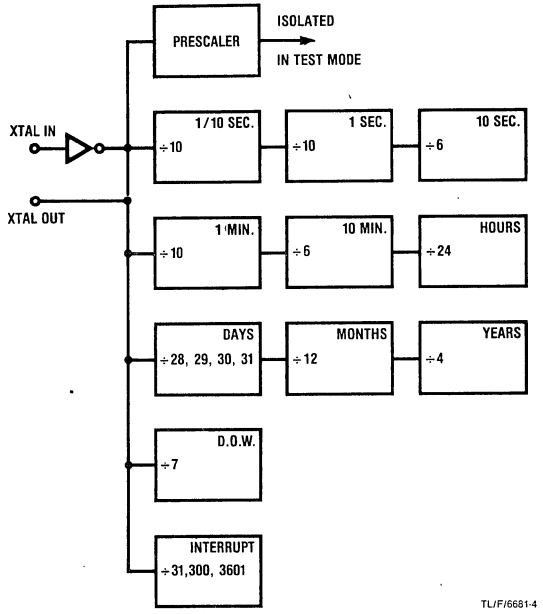


Figure 3. Test Mode Organization

Days Counter

There are two Days counters:

a) units of days

b) tens of days

The Days counters will count up to 28, 29, 30, or 31 days depending on the state of the Months counters and the Years Status Register. Days counters have parallel load and read multiplex capabilities.

Months Counters

There are two Months counters:

a) units of months

b) tens of months

The Months counters have parallel load and read multiplex capabilities.

Years Status Register

The Years Status register is a shift register of 4 bits. It will be shifted every year on December 31st. The status register must be set in accordance with Table III. No readout capability is provided.

Chip Select ($\overline{CS}$)

An external chip select is provided. The chip enable is active low.

Counter and Register Selection

Table 1 shows the coding on the address lines AD_0–AD_3 which select the registers in the circuit to be either parallel loaded or read on to the output bus.

Start/Stop (Reset) Latch

A logic "1" on DB_0 at chip address 14 (E) will start the clock running, a logic "0" will stop the clock. This function allows the loading of time data into the clock and its precise starting. The clock starts at 0.1 seconds.

Test Mode

This mode is incorporated to facilitate production testing of the circuit. In this mode, the 32,768Hz clock is fed forward as shown in *Figure 3*. For normal operation, the circuit must be set to the non-test mode as part of the system initialization. This is accomplished by writing a logic "0" to DB_3 at AD_0.

Table I. Address Decoding for Internal Registers

Selected Counter	Address Bits AD_3	AD_2	AD_1	AD_0	Mode
0 Test Only	0	0	0	0	Write Only
1 Tenths of secs.	0	0	0	1	Read Only
2 Units of secs.	0	0	1	0	Read Only
3 Tens of secs.	0	0	1	1	Read Only
4 Units of mins.	0	1	0	0	Read or Write
5 Tens of mins.	0	1	0	1	Read or Write
6 Units of hours	0	1	1	0	Read or Write
7 Tens of hours	0	1	1	1	Read or Write
8 Units of days	1	0	0	0	Read or Write
9 Tens of days	1	0	0	1	Read or Write
10 Day of week	1	0	1	0	Read or Write
11 Units of months	1	0	1	1	Read or Write
12 Tens of months	1	1	0	0	Read or Write
13 Years	1	1	0	1	Write Only
14 Stop/Start	1	1	1	0	Write Only
15 Interrupt	1	1	1	1	Read or Write

Table IIa. Interrupt Selection Data

Mode: Address 15, Write Mode				
Function	**DB_3**	**DB_2**	**DB_1**	**DB_0**
No Interrrupt	X	0	0	0
Int. at 60 sec. intervals*	0/1	1	0	0
Int. at 5.0 sec. intervals*	0/1	0	1	0
Int. at 0.5 sec. intervals*	0/1	0	0	1

* +16.6 ms

$DB_3 = 0$, single interrupt $DB_3 = 1$, repeated interrupt

Table IIb. Interrupt Read Back (Status)

Mode: Address 15, Read Mode				
Interrupt Status	**DB_3**	**DB_2**	**DB_1**	**DB_0**
Reset	X	0	0	0
60 sec. signal	X	1	0	0
5.0 sec. signal	X	0	1	0
0.5 sec. signal	X	0	0	1

X = don't care state

Table III. Years Status Register

Mode: Address 13, Write Mode				
	DB_3	**DB_2**	**DB_1**	**DB_0**
Leap year	1	0	0	0
Leap year – 1	0	1	0	0
Leap year – 2	0	0	1	0
Leap year – 3	0	0	0	1

Note: Leap year counter rolls over on Dec. 31 @23:59:59

Interrupt System

The interrupt output and its frequency of operation is enabled by writing to address 15 (see Table IIa). To ensure correct operation, the interrupt should be serviced within 16.6 ms.

The interrupt is initialized by writing "0" to address 15 and reading the interrupt, i.e., reading at address 15 three times. Initialization must be performed at power on and also if the interrupt is not serviced correctly within 16.6 ms.

Servicing the Interrupt

In a typical system the open drain interrupt output is wired to the processor interrupt system. Hence, when the interrupt timer times out, the interrupt output is pulled low and the processor is interrupted.

The processor may then reset the interrupt by utilizing the following procedure:

Read Address 15 three times.

This resets the interrupt output and restarts the interrupt timer when in the repeat mode.

It is recommended that the interrupt output is connected to a unique processor port.

Crystal Parameters

Figure 4 is an electrical representation of the crystal along with some typical values. The 32.768 kHz crystal is an NT CUT (tuning fork type) or XY BAR for use in a parallel resonant Pierce oscillator.

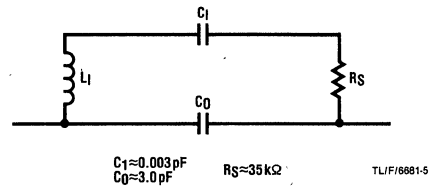


Figure 4. Typical Crystal Parameters

Device Initialization and Oscillator Setting

When first installed or if the battery back-up has failed, the MM58174A will require to be properly initialized. The following sequence is a suggested flow of operations to achieve this.

Action	Result
1) Apply power.	
2) Write '0' to address 15.	Clears interrupt timer chain.
3) Read 3 times from address 15.	Clears interrupt output logic.
4) Write '0' on DB3 to address 0.	Clears test mode.
5) Write '0' on DB0 to address 14.	Stops clock running.
6) Set up time-keeping registers.	Load real-time into device time registers, minutes to leap years.
7) Write '1' on DB0 to address 14.	Starts time-keeping synchronized to an external time source.
8) Program and start interrupts.	Commence interrupt timing, if so required.

Oscillator Setting

Directly connecting a frequency meter to the Crystal Out pin (14) will not allow correct frequency setting because of the extra capacitive loading of the meter. One possibility for setting is to use a high impedance probe or a CMOS buffer to keep the loading as low as possible (e.g., 100 × 2 pF probe). Alternatively, a buffered output of 16.384 kHz (OSC/2) can be produced on DB0 by applying the following procedure:

Action	Result
1) Write a '1' on DB3 to address 0.	Selects test mode.
2) Write a '1' on DB0 to address 14.	Starts clock timing.
3) Read at address 1 (tenths of secs).	'Data Changed' signal is read.
4) Read at address 1 and HOLD the strobe LOW.	16.384 kHz appears on DB0.
5) Adjust trimmer capacitor.	

There must be no extra activity on the $\overline{RD}$ line between steps 3 and 4 or only the normal 'Data Changed' signal will be observed on the data bus. Thus if the normal host processor system is being used to generate the chip waveforms, proper care must be taken.

Timing Waveforms

Read Mode

Figure 6 gives detailed timing for the transfer of data from peripheral to microprocessor. See Table IV.

All times are measured from (or to) valid logic "0" level = 0.8V or valid logic "1" level = 2.0V.

Write Mode

Figure 7 gives detailed timing for the transfer of data from microprocessor to peripheral. See Table V.

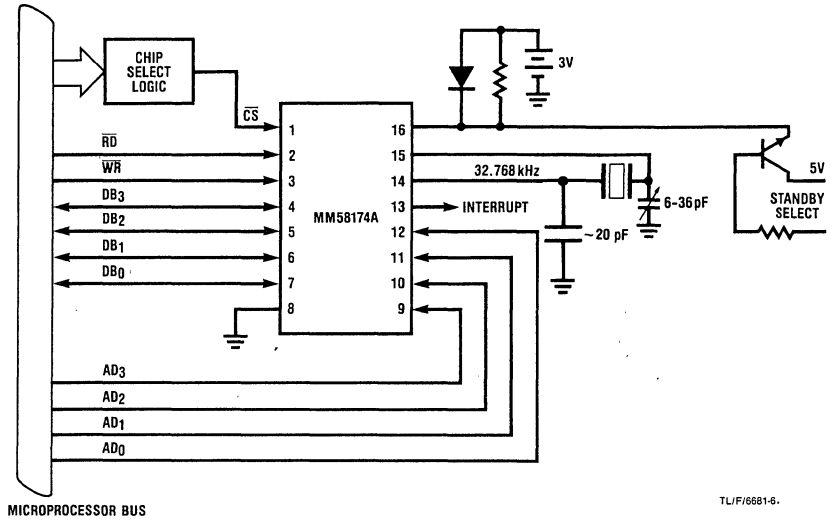


Figure 5. Typical Microprocessor Interface

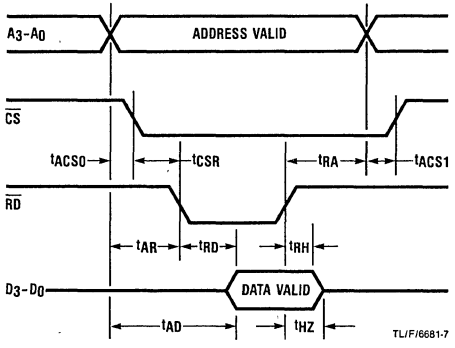


Figure 6. Read Cycle Waveforms

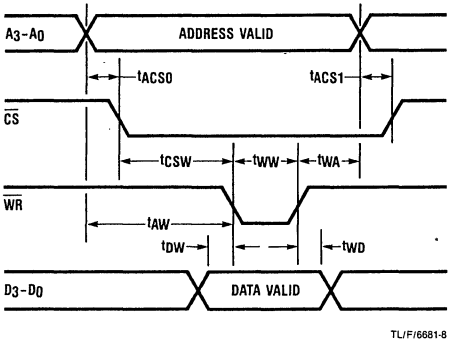


Figure 7. Write Cycle Waveforms

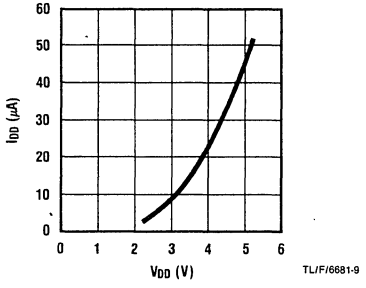


Figure 8. Typical Supply Current vs Supply Voltage During Power Down

Operating Conditions

MM58174AN $T_A = -40°C$ to $+85°C$
$V_{DD} = 5V$

Table IV. Read Timing: Data from Peripheral to Microprocessor

Symbol	Parameter	MM58174AN		Typ	Units	Comments
		Min	Max			
t_{ACS0}	Address Bus Valid to Chip Select ON ($\overline{CS} = 0$)	0			ns	
t_{CSR}	Chip Select ON to Read Strobe	0			ns	
t_{RD}	Read Cycle Access Time from Read Strobe to Data Bus Valid		900	450	ns	CL = 100 pF
t_{RH}	Data Hold Time from Trailing Edge of Read Strobe	0	330		ns	
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	70		500	ns	
t_{ACS1}	Address Change to Chip Select OFF	0		40	ns	
t_{AD}	Address Bus Valid to Data Valid		1850	850	ns	CL = 100 pF
t_{HZ}	Time from Trailing Edge of Read Strobe until Interface Device Bus Drivers are in TRI-STATE® Mode	0	330		ns	
t_{RW}	Read Strobe Width		14		μs	
t_{AR}	Address Bus Valid to Read Strobe	500			ns	

Note 1: In order not to degrade timekeeping accuracy, the number of Read strobes in any one second should be less than 10,000.

Table V. Write Timing: Data from Microprocessor to Peripheral

Symbol	Parameter	MM58174AN		Typ	Units	Comments
		Min	Max			
t_{ACS0}	Address Bus Valid to Chip Select ON ($\overline{CS} = 0$)	0			ns	
t_{CSW}	Chip Select ON to Write Strobe	0		450	ns	
t_{AW}	Address Bus Valid to Write Strobe	725			ns	
t_{WW}	Write Strobe Width	670			ns	
t_{DW}	Data Bus Valid Before Write Strobe	70			ns	
t_{WA}	Address Bus Hold Time Following Write Strobe	165			ns	
t_{WD}	Data Bus Hold Time Following Write Strobe	185			ns	
t_{ACS1}	Address Change to Chip Select OFF ($\overline{CS} = 1$)	0			ns	

Note 1: If address and write occur simultaneously, then they must exist for t_{AW} and t_{WW}.

National Semiconductor

MM58201 Multiplexed LCD Driver

General Description

The MM58201 is a monolithic CMOS LCD driver capable of driving up to 8 backplanes and 24 segments. A 192-bit RAM stores the data for the display. Serial input and output pins are provided to interface with a controller. An RC oscillator generates the timing necessary to refresh the display. The magnitude of the driving waveforms can be adjusted with the V_{TC} input to optimize display contrast. Four additional bits of RAM allow the user to program the number of backplanes being driven, and to designate the driver as either a master or slave for cascading purposes. When two or more drivers are cascaded, the master chip drives the backplane lines, and the master and each slave chip drive 24 segment lines. Synchronizing the cascaded drivers is accomplished by tying the RC OSC pins together and the BP1 pins together.

The MM58201 is packaged in a 40-lead dual-in-line package.

Features

- Drives up to 8 backplanes and 24 segment lines
- Stores data for display
- Cascadable
- Low power
- Fully static operation

Applications

- Dot matrix LCD driver
- Multiplexed 7-segment LCD driver
- Serial in/serial out memory

Block and Connection Diagrams

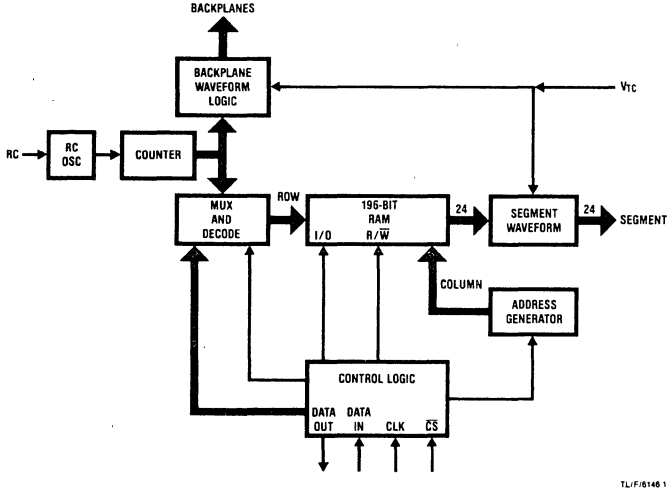


FIGURE 1

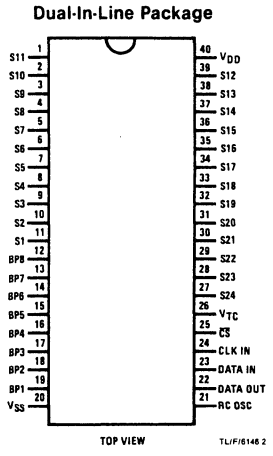


FIGURE 2

Order Number MM58201D
See NS Package D40C

Order Number MM58201N
See NS Packaage N40A

Absolute Maximum Ratings

Voltage at Any Pin	$V_{SS}-0.3V$ to $V_{SS}+18V$	Package Dissipation	500 mW
Operating Temperature Range	0°C to 70°C	Operating V_{DD} Range	$V_{SS}+7.0V$ to $V_{SS}+18.0V$
Storage Temperature Range	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

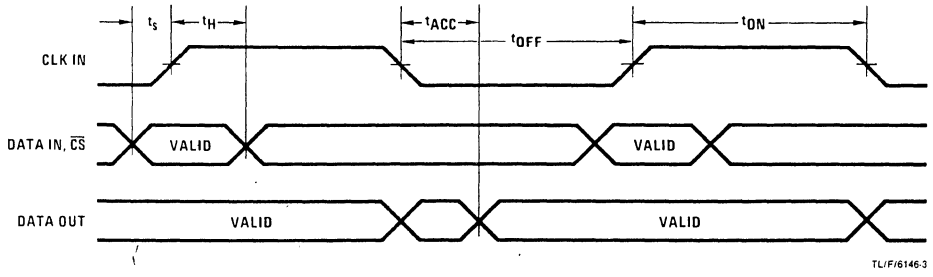
Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Quiescent Supply Current				0.3	mA
$V_{IN(1)}$	Logical "1" Input Voltage		0.45 V_{DD}		$V_{DD}+0.3$	V
$V_{IN(0)}$	Logical "0" Input Voltage		$V_{SS}-0.3$		1.0	V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_{SINK}=0.6$ mA			0.4	V
$I_{OUT(1)}$	Logical "1" Output Leakage Current	$V_{OUT}=V_{DD}$	0		±10	μA
$I_{IN(1)}$	Logical "1" Input Leakage Current	$V_{IN}=V_{DD}$	0		1.0	μA
$I_{IN(0)}$	Logical "0" Input Leakage Current	$V_{IN}=V_{SS}$	−1.0		0	μA
V_{TC}	Input Voltage		4.5		$V_{DD}+0.3$	V
V_{TC}	Input Impedance		10		30	kΩ
Z_{OUT}	Output Impedance	Backplane and Segment Outputs			10	kΩ
	DC Offset Voltage	Between Any Backplane and Segment Output	0		±10	mV

AC Electrical Characteristics T_A and V_{DD} within operating range unless otherwise noted.

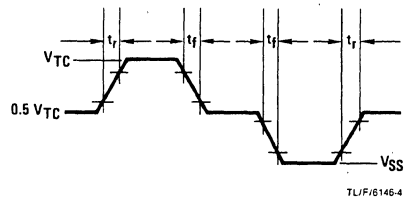
Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{OSC}	Oscillator Frequency*		128η		400η	Hz
$f_{CLK\ IN}$	Clock Frequency		DC		100	kHz
t_{ON}	Clock Pulse Width		5.0			μs
t_{OFF}	Clock OFF Time		5.0			μs
t_s	Input Data Set-Up Time		2.0			μs
t_H	Input Data Hold Time		1.0			μs
t_{ACC}	Access Time		5.0			μs
t_r	Rise Time	Backplane, Segment Outputs $C_L=2000$ pF			60	μs
t_f	Fall Time	Backplane, Segment Outputs $C_L=2000$ pF			60	μs

* η is the number of backplanes programmed.

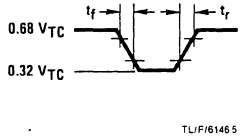
Switching Time Waveforms



Backplane Output



Segment Output



Functional Description

A functional diagram of the MM58201 LCD driver is shown in *Figure 1*. A connection diagram is shown in *Figure 2*.

Serial Inputs and Output

A negative-going edge on the $\overline{CS}$ input initiates a frame. The $\overline{CS}$ input must then stay low for at least one rising edge of CLK IN, and may not be pulsed low again for the next 31 clocks. At least one clock must occur while $\overline{CS}$ is high. If CLK IN is held at a logic "1", $\overline{CS}$ is disabled. This allows the signal that drives $\overline{CS}$ to be used for other purposes when the MM58201 is not being addressed.

CLK IN latches data from the DATA IN input on its rising edge. Data from the DATA OUT pin changes on the falling edge of CLK IN and is valid before the next rising edge.

The first five bits of data following $\overline{CS}$ are the address bits *(Figure 3)*. The address selects the column where the operation is to start. Bit 1 is the MSB and bit 5 is the LSB. The sixth bit is the read/write bit. A logic "1" specifies a read operation and a logic "0" specifies a write operation. Tne next 24 bits are the data bits. The first data bit corresponds to the BP1 row of the display, the second data bit to the BP2 row, and so on. After the eighth and sixteenth data bits, the column pointer is incremented. When starting address 10110 or 10111 is specified, the column pointer increments from 10111 to 00000.

During a read or write cycle, the LCD segment outputs do not reflect the data in the RAM. To avoid disrupting the pattern viewed on the display, the read or write cycle time should be kept short. Since the LCD turn-on time can be as little as 30 ms, a clock rate of at least 10 kHz would be required in order to address the entire contents of the RAM within that time interval. The formula below can be used to estimate the minimum clock rate:

$$f_{CLK\ IN} = \frac{30}{(t_{LCD} - 7t_s)}$$

where t_s is the processor's set-up time between each read or write cycle, and t_{LCD} is the minimum turn-on or turn-off time of the LCD as specified by the LCD manufacturer.

The DATA OUT output is an open drain N-channel device to V_{SS} *(Figure 4)*. With an external pull-up this configuration allows the controller to operate at a lower supply voltage, and also permits the DATA OUT output to be wired in parallel with the DATA OUT outputs from any other drivers in the system.

To program the number of backplanes being driven and the M/$\overline{S}$ bit, load address 11000, a write bit, three bits for the number of backplanes (Table I), and the M/$\overline{S}$ bit. The remaining 20 data bits will be ignored but it is necessary to provide 21 more clocks before initiating another frame.

TABLE I. Backplane Select

Number of Backplanes	B2	B1	B0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

Functional Description (Continued)

RC OSC Pin

This oscillator generates the timing required for multiplexing the liquid crystal display. The oscillator operates at a frequency that is 4η times the refresh rate of the display, where η is the number of backplanes programmed. Since the refresh rate should be in the range from 32 Hz to 100 Hz, the oscillator frequency must be:

$$128\eta \leq f_{OSC} \leq 400\eta$$

The frequency of oscillation is related to the external R and C components in the following way:

$$f_{OSC} = \frac{1}{1.25\ RC} \pm 30\%$$

The value used for the external resistor should be in the range from 10 kΩ to 1 MΩ.

The value used for the external capacitor should be less than 0.005 μF.

V_{TC} Pin

The V_{TC} pin is an analog input that controls the contrast of the segments on the LCD. If eight backplanes are being driven ($\eta = 8$), a voltage of typically 8V is required at 25°C. The voltage for optimum contrast will vary from display to display. It also has a significant negative temperature coefficient.

The voltage source on the V_{TC} input must be of relatively low impedance since the input impedance of V_{TC} ranges from 10 kΩ to 30 kΩ. A suitable circuit is shown in *Figure 5.*

In a standby mode, the V_{TC} input can be set to V_{SS}. This reduces the supply current to less than 300 μA per driver.

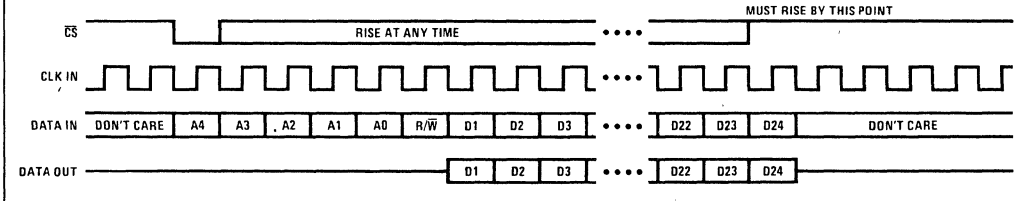
Backplane and Segment Outputs

Connect the backplane and segment outputs directly to the LCD row and column lines. The outputs are designed to drive a display with a total ON capacitance of up to 2000 pF.

The output structure consists of transmission gates tapped off of a resistor string driven by V_{TC} *(Figure 6).*

A critical factor in the lifetime of an LCD is the amount of DC offset between a backplane and segment signal. Typically, 50 mV of offset is acceptable. The MM58201 guarantees an offset of less than 10 mV.

The BP1 output is disabled when the M/$\overline{S}$ bit is set to zero. This allows the BP1 output from the master chip to be connected directly to it so that synchronizing signals can be generated. Synchronization occurs once each refresh cycle, so the cascaded chips are assured of remaining synchronized.



	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17	S18	S19	S20	S21	S22	S23	S24	
BP1													D1	D9	D17										B2
BP2													D2	D10	D18										B1
BP3													D3	D11	D19										B0
BP4													D4	D12	D20										M/S
BP5													D5	D13	D21										
BP6													D6	D14	D22										
BP7													D7	D15	D23										
BP8													D8	D16	D24										

A4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
A3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1
A2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0
A1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
A0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Diagram above shows where data will appear on display if starting address 01100 is specified in data format. TL/F/6146-6

FIGURE 3. Data Format

Functional Description (Continued)

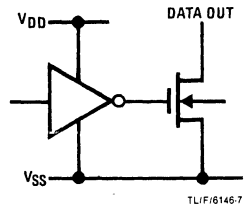


FIGURE 4. DATA OUT Structure

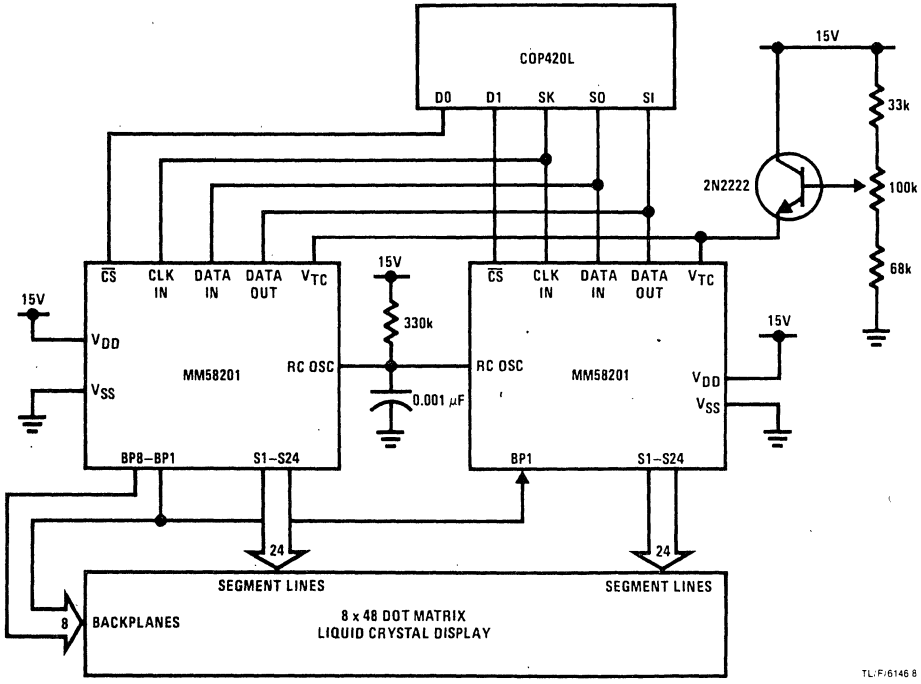


FIGURE 5. Typical Application

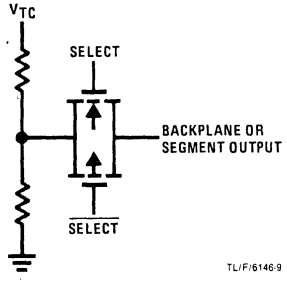


FIGURE 6. Structure of LCD Outputs

National Semiconductor

MM58241 High Voltage Display Driver

General Description

The MM58241 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58241 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 32-digit alphanumeric or dot matrix display).

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block and Connection Diagrams

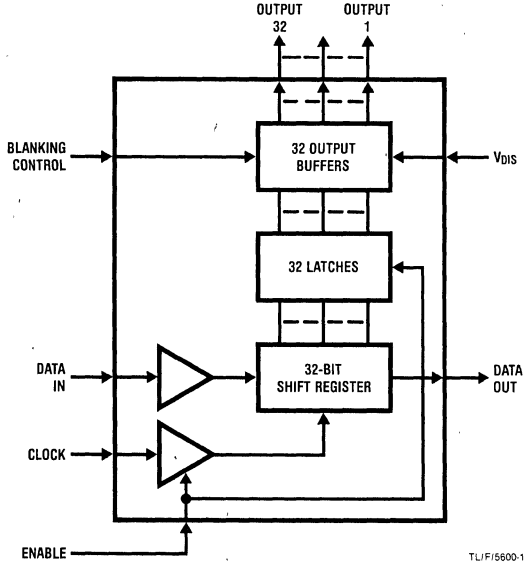


FIGURE 1

Dual-In-Line Package

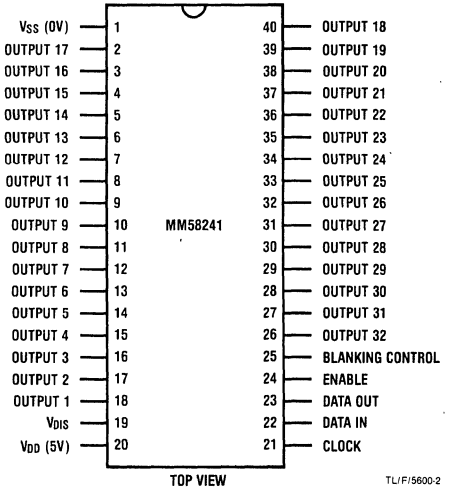


FIGURE 2

Order Number MM58241N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-62.5V$
$V_{DD}+\lvert V_{DIS}\rvert$	62.5V
Storage Temperature	$-65°C$ to $+150°C$
Power Dissipation	500 mW at $+85°C$
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS}=0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics $T_A=-40°C$ to $+85°C$, $V_{DD}=5V\pm0.5V$, $V_{SS}=0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN}=V_{SS}$ or V_{DD}, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-55V$ All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	$I_{OUT}=400\ \mu A$			0.4	V
V_{OH}	Logic '1'	$I_{OUT}=-10\ \mu A$	$V_{DD}-0.5$			V
V_{OH}	Logic '1'	$I_{OUT}=-500\ \mu A$	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN}=0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	$V_{DD}=5.5V$, $V_{SS}=0V$				
R_{OFF}	Output Off (*Figure 3a*)	$V_{DIS}=-25V$	60		400	kΩ
		$V_{DIS}=-40V$	70		550	kΩ
		$V_{DIS}=-55V$	80		650	kΩ
R_{ON}	Output On (*Figure 3b*)	$V_{DIS}=-25V$		3.0	4.0	kΩ
		$V_{DIS}=-40V$		2.6	3.7	kΩ
		$V_{DIS}=-55V$		2.3	3.4	kΩ
V_{DOL}	Display Output Low Voltage	$V_{DD}=5.5V$, $I_{OUT}=$ Open Circuit, $-55V\le V_{DIS}\le-25V$	V_{DIS}		$V_{DIS}+4$	V

Note 1: 74LSTTL $V_{OH}=2.7V$ @ $I_{OUT}=-400\ \mu A$, TTL $V_{OH}=2.4V$ @ $I_{OUT}=-400\ \mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input	(Notes 3 and 4)				
Frequency, f_C				800	kHz
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns
Enable Input					
Set-Up Time, t_{ES}		100			ns
Hold Time, t_{EH}		100			ns
Data Output	$C_L = 50$ pF				
CLOCK Low to Data Out Time, t_{CDO}				500	ns

Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, $f = 800$ kHz, 50% ± 10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58241 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58241 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58241 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following ENABLE high. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58241, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.

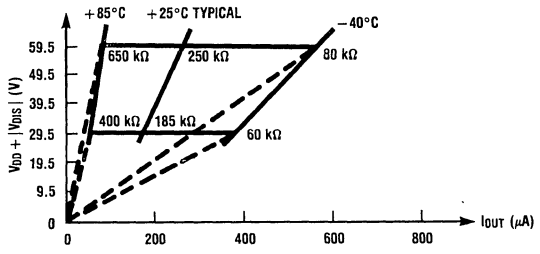
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58241.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

In *Figure 5*, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58241, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

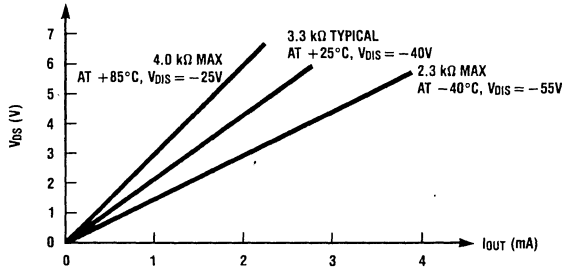
Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58241 is used to provide the grid drive for a 32-digit 5 × 7 dot matrix vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58248, which does not require an externally generated load signal.

Functional Description (Continued)



TL/F/5600-3

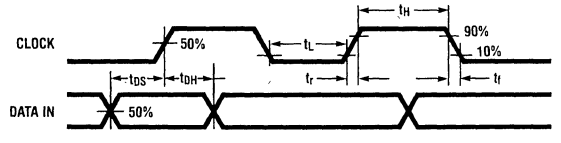
FIGURE 3a. Output Impedance Off



TL/F/5600-4

FIGURE 3b. Output Impedance On

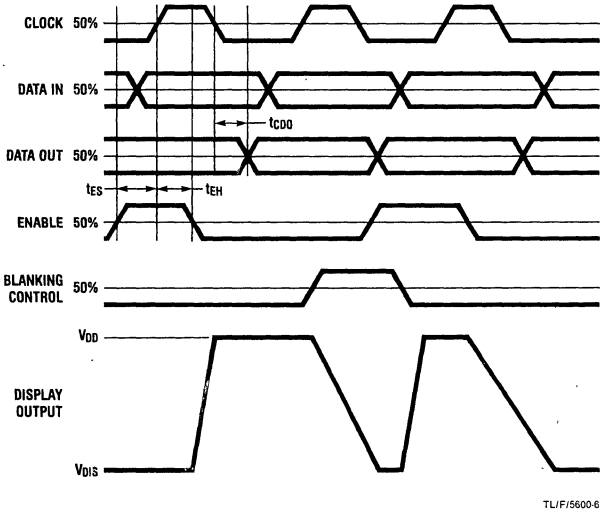
Timing Diagrams



TL/F/5600-5

For the purposes of AC measurements, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

FIGURE 4. Clock and Data Timings



TL/F/5600-6

FIGURE 5. MM58241 Timings (Data Format)

Typical Application

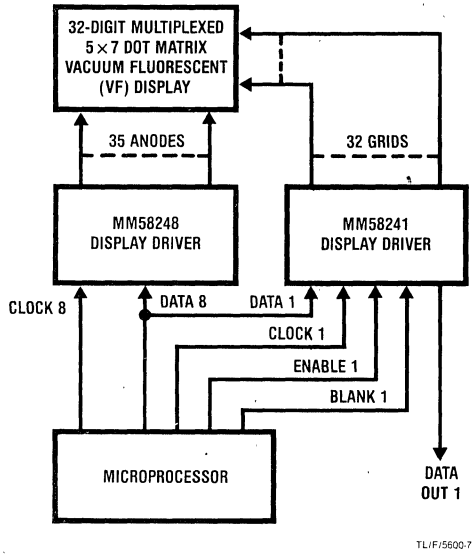


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58242 High Voltage Display Driver

General Description

The MM58242 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58242 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block and Connection Diagrams

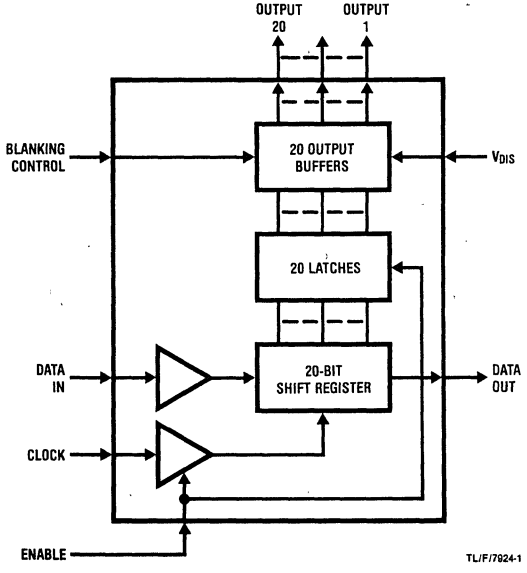


FIGURE 1

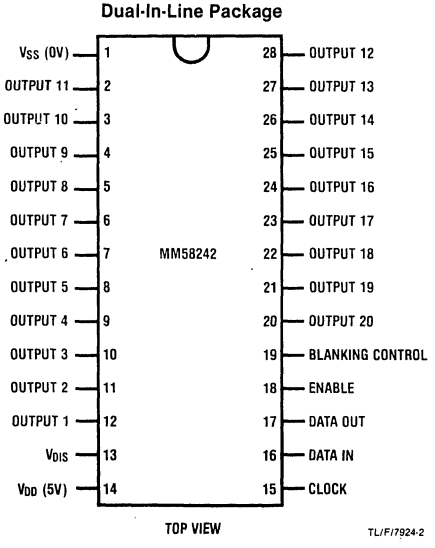


FIGURE 2

Order Number MM58242N
See NS Package N28B

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-62.5V$
$V_{DD}+\lvert V_{DIS}\rvert$	62.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS}=0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics $T_A=-40°C$ to $+85°C$, $V_{DD}=5V\pm0.5V$, $V_{SS}=0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN}=V_{SS}$ or V_{DD}, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-55V$ All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	$I_{OUT}=400\ \mu A$			0.4	V
V_{OH}	Logic '1'	$I_{OUT}=-10\ \mu A$	$V_{DD}-0.5$			V
V_{OH}	Logic '1'	$I_{OUT}=-500\ \mu A$	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN}=0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	$V_{DD}=5.5V$, $V_{SS}=0V$				
R_{OFF}	Output Off (*Figure 3a*)	$V_{DIS}=-25V$	60		400	kΩ
		$V_{DIS}=-40V$	70		550	kΩ
		$V_{DIS}=-55V$	80		650	kΩ
R_{ON}	Output On (*Figure 3b*)	$V_{DIS}=-25V$		3.0	4.0	kΩ
		$V_{DIS}=-40V$		2.6	3.7	kΩ
		$V_{DIS}=-55V$		2.3	3.4	kΩ
V_{DOL}	Display Output Low Voltage	$V_{DD}=5.5V$, $I_{OUT}=$ Open Circuit, $-55V\le V_{DIS}\le-25V$	V_{DIS}		$V_{DIS}+4$	V

Note 1: 74LSTTL $V_{OH}=2.7V$ @ $I_{OUT}=-400\ \mu A$, TTL $V_{OH}=2.4V$ @ $I_{OUT}=-400\ \mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input	(Notes 3 and 4)				
Frequency, f_C				800	kHz
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns
Enable Input					
Set-Up Time, t_{ES}		100			ns
Hold Time, t_{EH}		100			ns
Data Output	$C_L = 50$ pF				
CLOCK Low to Data Out Time, t_{CDO}				500	ns

Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: $t_r \leq 20$ ns, $t_f \leq 20$ ns, $f = 800$ kHz, 50% ± 10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58242 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58242 is shown in *Figure 1*.

Figure 2 shows the pinout of the MM58242 device, where output 1 (pin 12) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58242, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.

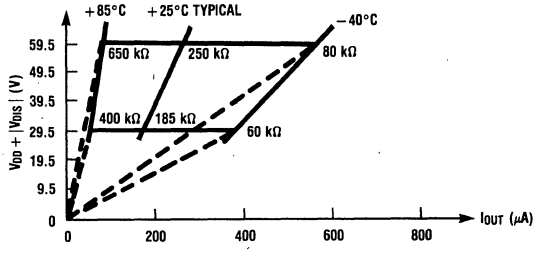
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58242.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

In *Figure 5*, the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58242 being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

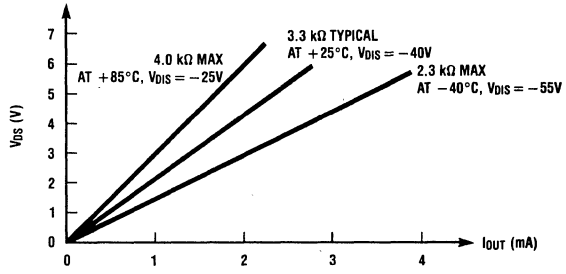
Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58242 is used to provide the grid drive for a 40-digit 2 line 5 × 7 multiplexed vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58248, which does not require an externally generated load signal.

Functional Description (Continued)



TL/F/7924-3

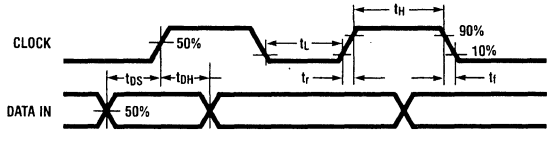
FIGURE 3a. Output Impedance Off



TL/F/7924-4

FIGURE 3b. Output Impedance On

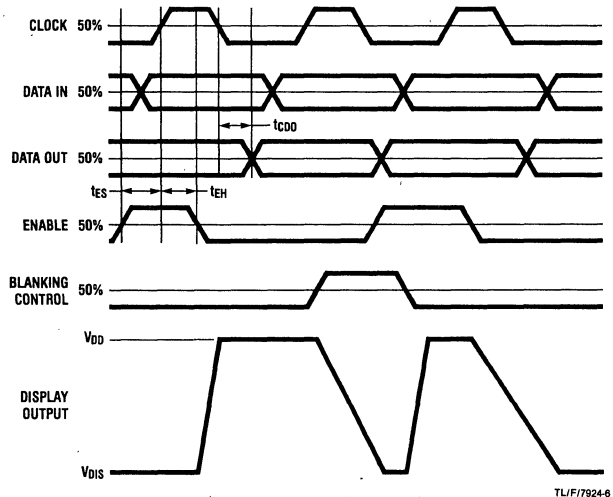
Timing Diagrams



TL/F/7924-5

For the purposes of AC measurements, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

FIGURE 4. Clock and Data Timings



TL/F/7924-6

FIGURE 5. MM58242 Timings (Data Format)

Typical Application

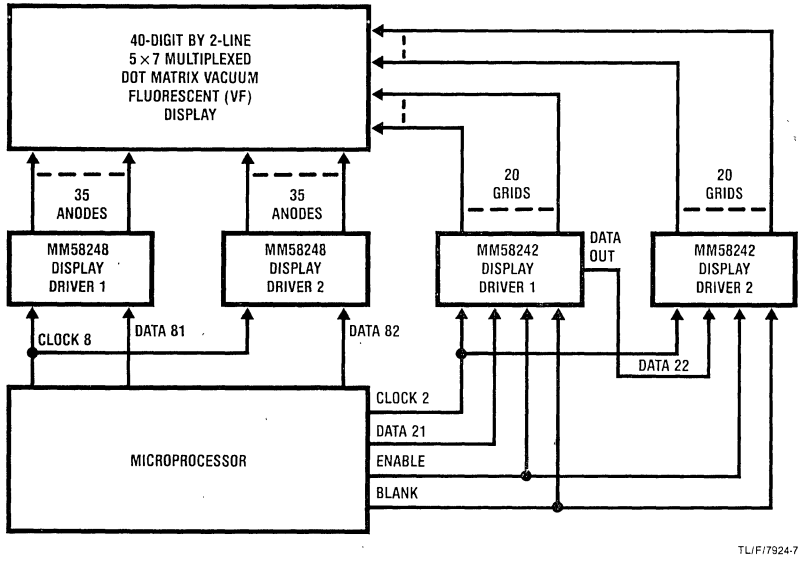


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58248 High Voltage Display Driver

General Description

The MM58248 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58248 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 5 × 7 dot matrix display).

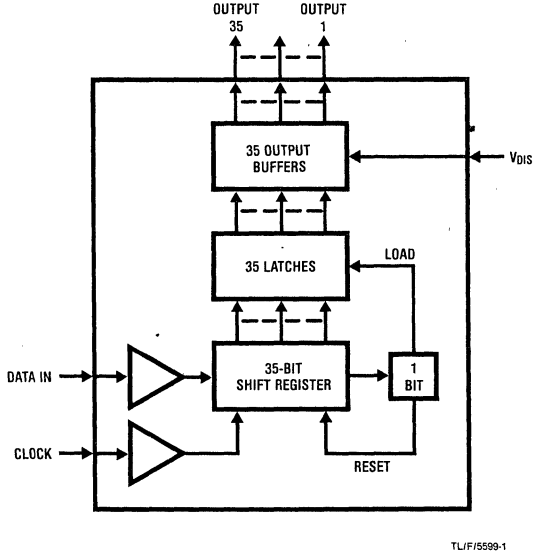
Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- No load signal required

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

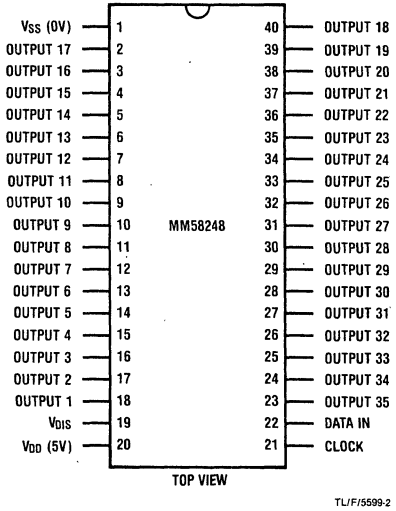
Block and Connection Diagrams



TL/F/5599-1

FIGURE 1

Dual-In-Line Package



TL/F/5599-2

FIGURE 2

Order Number MM58248N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-62.5V$
$V_{DD}+\lvert V_{DIS}\rvert$	62.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS}=0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−55	−25	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics $T_A=-40°C$ to $+85°C$, $V_{DD}=5V\pm0.5V$, $V_{SS}=0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN}=V_{SS}$ or V_{DD}, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-55V$ All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
I_{IN}	Input Currents DATA IN, CLOCK	$V_{IN}=0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK				15	pF
	Display Output Impedances	$V_{DD}=5.5V$, $V_{SS}=0V$				
R_{OFF}	Output Off (*Figure 3a*)	$V_{DIS}=-25V$	60		400	kΩ
		$V_{DIS}=-40V$	70		550	kΩ
		$V_{DIS}=-55V$	80		650	kΩ
R_{ON}	Output On (*Figure 3b*)	$V_{DIS}=-25V$		3.0	4.0	kΩ
		$V_{DIS}=-40V$		2.6	3.7	kΩ
		$V_{DIS}=-55V$		2.3	3.4	kΩ
V_{DOL}	Display Output Low Voltage	$V_{DD}=5.5V$, $I_{OUT}=$ Open Circuit, $-55V\le V_{DIS}\le-25V$	V_{DIS}		$V_{DIS}+4$	V

Note 1: 74LSTTL $V_{OH}=2.7V$ @ $I_{OUT}=-400\,\mu A$, TTL $V_{OH}=2.4V$ @ $I_{OUT}=-400\,\mu A$.

7

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input	(Notes 2 and 3)				
Frequency, f_C				1.0	MHz
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input	$C_L = 50$ pF				
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns

Note 2: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, f = 1 MHz, 50% ± 10% duty cycle.
Note 3: Clock input rise and fall times must not exceed 5 μs.

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58248 uses two signals, DATA IN and CLOCK, with a format of a leading '1' followed by the 35 data bits, hence allowing data transfer without an additional signal. A block diagram of the MM58248 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58248 device, where output 1 (pin 18) is equivalent to bit 1, i.e., the first bit of data to be loaded into the shift register following the start bit. A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by the use of the MM58248, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.

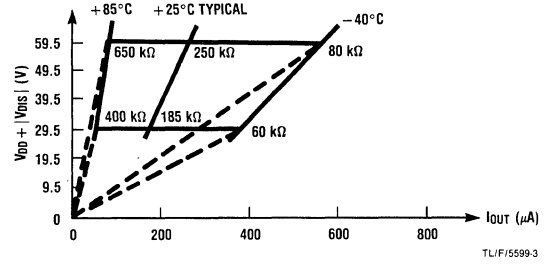


FIGURE 3a. Output Impedance Off

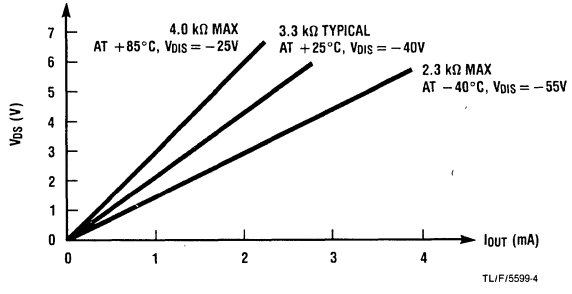


FIGURE 3b. Output Impedance On

Functional Description (Continued)

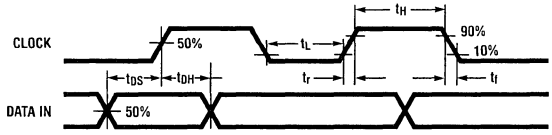
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58248.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of the start bit and the first clock pulse, and so all interface signals should be inactive at power on.

In *Figure 5,* a start bit of logic '1' precedes the 35 bits of data, each bit being accepted on the rising edge of CLOCK, i.e., a '0'–'1' transition. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, thus loading the 35 bits of the shift register into the latches. At the low state of the clock, a RESET signal is generated, clearing all bits of the shift register for the next set of data. Hence, a complete set of 36 clock pulses is needed for the MM58248, or the shift register will not clear. If, at any given time, it is required that the display be cleared under microprocessor control, i.e., without power on reset, then the following flushing routine may be used. Clock in 36 'zeroes', followed by a 'one' (start bit), followed by 35 'zeroes'. This procedure will completely blank the display.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58248 is used to provide the anode drive for a 32-digit 5 × 7 dot matrix vacuum fluorescent (VF) display. The grid drive in this example is provided by another member of the high voltage display driver family, namely the MM58241, which has the additional features of a BLANKING CONTROL pin, a DATA OUT pin, and an ENABLE (external load signal) pin.

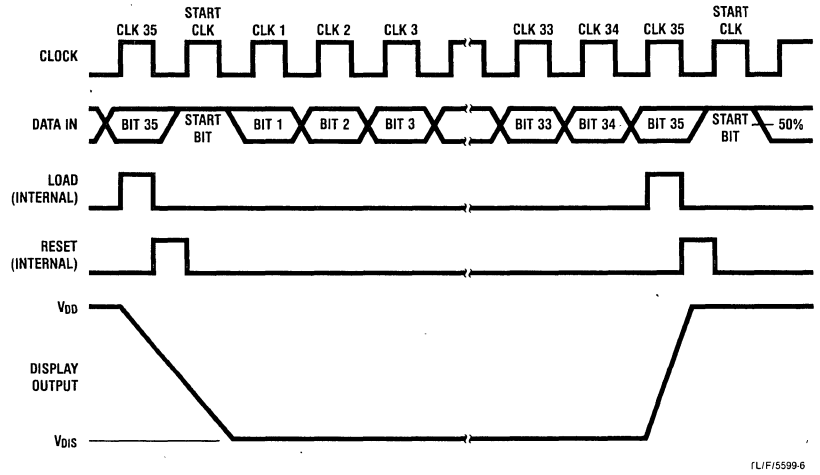
Timing Diagrams



TL/F/5599-5

For the purposes of AC measurement, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$

FIGURE 4. Clock and Data Timings



TL/F/5599-6

FIGURE 5. MM58248 Timings (Data Format)

Typical Application

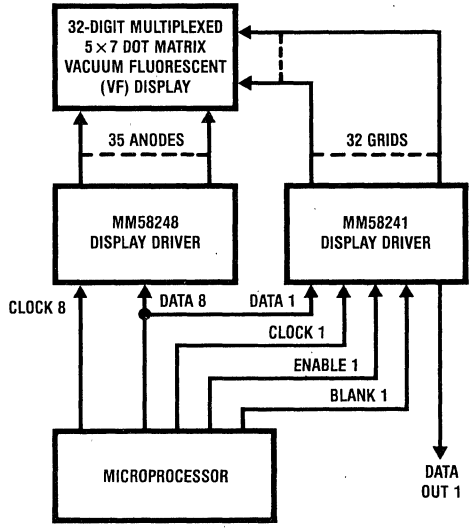


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

PRELIMINARY

MM58250 Infrared Transmitter

General Description

The infrared transmitter is designed to drive an infrared LED (only one external npn transistor is required) with data encoded in a pulse-width-modulated (pwm) format. To get a better signal-to-noise-ratio the pwm scheme amplitude modulates a 38kHz carrier. The data to be transmitted is input in two ways. The primary data input mode (MS = 1) is through a 4-by-8 single-contact keyboard which is interpreted by on-chip logic. The second input mode (MS = 0) is the direct input mode. In this mode a five-bit parallel word and a load pulse are applied to the inputs. The five-bit word is then converted to the pwm format and transmitted.

The chip is designed for battery operation, so it employs a number of power-saving techniques. The chip is implemented in CMOS, so the supply current required by the logic is low. The oscillator can be disabled, allowing the stand-by current to be less than 1 μA. Although the continuous transmission of the data stream is possible, the repetition rate of the continuous transmission is restricted, and the majority of the codes transmittable are repeated only three times. (Twelve outputs can be repeated continuously for analog functions such as volume and channel scanning).

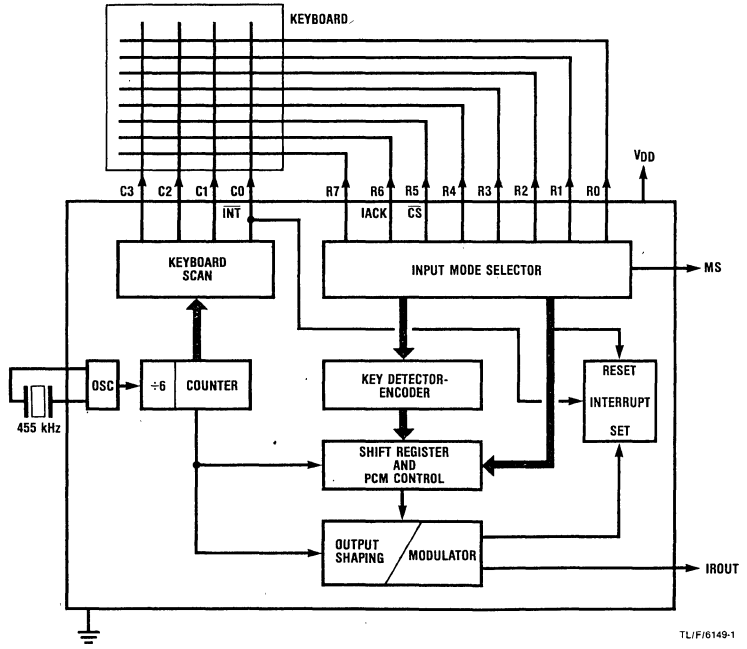
Features

- Up to 32 functions decoded and transmitted
- Single-contact scanned keyboard
- Low standby current (CMOS)
- 455kHz on-chip oscillator
- Wide power supply range (3V-10V)
- Keyboard or direct load modes
- Direct load mode TTL compatible
- 38kHz carrier for improved signal-to-noise-ratio
- High current output stage

Applications

- TV remote control transmitter
- 5-bit wireless asynchronous transmitter

Block Diagram



Absolute Maximum Ratings

Voltage at Any Pin	$-0.3V$ to $V_{DD}+0.3V$	$V_{DD}-V_{SS}$	12V
Operating Temperature	0°C to 70°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature	−65°C to +150°C	DC Current at IR Output	−20mA
Package Dissipation	500mW		

Electrical Characteristics

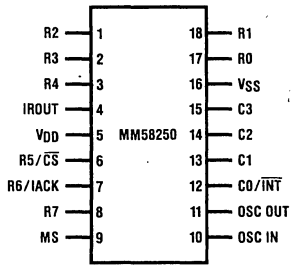
$V_{DD}=3.0V$ to 10V, $T_A=\pm 0°C$ to 70°C unless otherwise specified.

Sym	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply					
V_{DD}	Supply Voltage		3.0		10	V
V_{DD}	Supply Current (Active)				5	mA
V_{DD}	Supply Current (Standby)				1	μA
	Oscillator Frequency*			455		kHz
IR	Output Voltage					
	Logic "0"	150μA Sink			0.6	V
	Logic "1"	10mA Source	$V_{DD}-1.4$			V
IR	Output Current (Note: no short-circuit protection)	$V_{DD}-1.4V$	−10		−20	mA
	Input Levels	MS = 0, $4.5 \leq V_{DD} \leq 5.5$ Direct Mode				
	Logic "0"				0.5	V
	Logic "1"		2.4			V
	Input Current	MS = 0, $4.5V \leq V_{DD} \leq 5.5V$ Direct Mode				
	R_0-R_6, MS	$0V \leq V_{IN} \leq V_{DD}$	−1		1.0	μA
	R_7	$V_{IN}=0.4V$	0.06		0.6	mA
	Input Current	MS = 1, $3.0V \leq V_{DD} \leq 10V$ Keyboard Mode				
	R_0-R_7	$V_{IN}=0.4V$	0.024		1.6	mA
	MS	$0V \leq V_{IN} \leq V_{DD}$	−1		1	μA
	Output Current	MS = 1				
	C_0-C_1					
	Logic "1" Source	$V_{DD}=3V$, $V_{OUT}=V_{DD}-1V$	−40			μA
	"1" Source	$V_{DD}=10V$, $V_{OUT}=V_{DD}-1V$	−150			μA
	Logic "0" Sink	$V_{DD}=3V$, $V_{OUT}=0.4V$	260			μA
	"0" Sink	$V_{DD}=10V$, $V_{OUT}=0.5V$	1.6			mA
	Output Current	MS = 0, $4.5V \leq V_{DD} \leq 5.5V$				
	$C_0/\overline{Int}$ (Open Drain)					
	Logic "1"	$0 \leq V_{OUT} \leq V_{DD}$			1	μA
	Logic "0"	$V_{OUT}=0.4V$	2.5			mA

*Determined by external components.

Connection Diagram

Dual-In-Line Package



Order Number MM58250N
See NS Package N18A

Pin Definitions

Mode Select (MS): This pin selects between the two modes of the MM58250's operation.

MS = "0": Parallel input mode. This mode is designed to allow five bits of data to be written to the MM58250 in a parallel fashion with all the appropriate handshaking signals required to facilitate interfacing a microprocessor.

MS = "1": Keyboard input mode. Data is input from a keyboard configured as a matrix of four column conductors and eight row conductors separated at each point of the matrix by a single contact.

$R_0/-R_7/$:

Keyboard Mode (MS = 1):

$R_0/-R_7/$: Act as row inputs for a scanned column keyboard. Internal to the MM58250, these are encoded such that if just one input is low during a scan of the column outputs, (see the discussion of pins $C_0/-C_3/$) a parallel-in-serial-out transmit buffer is loaded with the binary representation of the low row input and the scanning column. (The binary number loaded is equal to the decimal number in the pin name, i.e. binary 5 is stored for the R_5 input.) In addition $R_3/-R_5/$ cause the MM58250 to continuously transmit the data stored in its transmit buffer (see Figure 6) as long as a switch closure exists.

Parallel Mode (MS = 0):

$R_0/-R_4/$: These five inputs act as a parallel, non-inverting, 5-bit data entry path.

$R_5/$-CS/: This active low input is used to latch in the data at the $R_0/-R_4/$ inputs, as well as beginning the transmit cycle. The part will continue to transmit as long as this input is low and continue to transmit two to three transmit cycles after the input switches to logic "1", depending on where (see Figures 7 and 8) in the transmit cycle the logic change occured. (Note: the data on $R_0/-R_4/$ should be held stable a minimum of 60ms.)

$R_6/$-IACK: This input is used to reset the INT/ signal. It is active high. (See Figure 7)

$R_7/$: $R_7/$ enables two functions that were designed to facilitate the testing of the MM58250 quickly that might prove useful to some users.

The divide-by-six prescaler can be by-passed by applying a logic "0" to $R_7/$ when $R_6/$ = "1" and MS = "0". The by-pass is implemented by setting an RS-flip-flop that controls the multiplexing of the main clock line from the output of the divide-by-six prescaler to the output of the oscillator, by-passing the divide-by-six prescaler. The RS-flip-flop is reset by the main internal reset which is made active at the end of the transmit cycle, *begun before* the by-pass was activated. If the MM58250 is waiting for a new input, switching $R_7/$ low will have no effect.

The second special mode forces the main internal reset active. This causes the chip to load in new data to be transmitted and initializes the chip to the beginning of the word cycle it was currently in or in the word cycle folowing it, depending on where in the word cycle the reset occurred. If a transmit cycle has been completed this mode has no effect. A transmit cycle consists of three word cycles. If no new data is loaded, the MM58250 will go into its idle state within 45ms. See Figures 9-11 for examples of how to use these features.

$C_0/-C_3/$:

Keyboard Mode (MS = 1):

$C_0/-C_3/$: These outputs are normally low when MM58250 is waiting for a new input contact closure to occur. A contact closure causes the low signal on the column inputs to be passed to the appropriate row input. This input going low initiates the transmit cycle. As the transmit cycle begins, the oscillator is enabled and begins to oscillate within 6ms. As soon as the oscillator is enabled all the column outputs are switched to the logic "1" state. 40.9ms later, as clocked by the on-chip oscillator, these outputs are individually switched to the logic "0" state (see Figure 5) and the row inputs are sampled. If the sampling of the row inputs does not show any of these inputs low (see Figure 6b), the transmit cycle is aborted. If any of the row inputs is low, the binary representation of the low row input and the binary representation of the low column output are stored in the transmit buffer. If the low row input was $R_0/$, $R_1/$, $R_2/$, $R_6/$, or $R_7/$ the outputs $C_0/-C_3/$ all switch low, so internal logic can detect when all keyboard switches have been opened. This feature allows the MM58250 to terminate transmission after three iterations (see Figure 6a) of the output data, even when a contact closure exists longer than the time required to transmit the data three times.

Parallel Mode (MS = 0):

$C_0/-C_3/$: In the parallel mode only one of the column outputs is still used. This output is used as the $C_0/$ strobe in the keyboard mode. It is used in this mode as an active low processor interrupt (INT/). This output is designed to drive one TTL input with a 10k pullup resistor. It is reset by the IACK pin. When $R_5/\overline{CS}$ is a logic 1, this signal goes low after the last transmission is complete.

IROUT: This is the output that provides the drive signal for the transmission (see Figures 3 and 4). IROUT provides at least 10mA of current, sufficient to drive a single npn transistor hard enough to provide the 200mA of drive current for the infra-red diodes. The data is output in a serial mode with a start bit and a stop bit bracketing the five data bits. The pwm format used has a 1.6ms bit time with a 75% duty cycle for a '1' and a 25% duty cycle for a '0'. The start and stop bits are zeros.

Timing Specification

Input Timing	Min	Max	Units
Microprocessor Mode			
Data Set-up Time	0		s
Data Hold Time	50		ms
$\overline{CS}$ (minimum pulse width)	250		ns
IACK (minimum pulse width)	250		ns
Output Timing			
Oscillator Start up (Subject to external components)		9	ms

All of the following data is based on an oscillator frequency = 455kHz and will vary as the oscillator frequency varies.

Keyboard Switch Specifications

Bounce	40 ms max
R_{ON}	50Ω max
R_{OFF}	1 MΩ min

Timing Diagrams

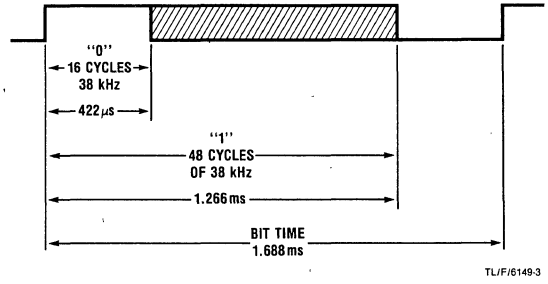


Figure 2. Bit Timing

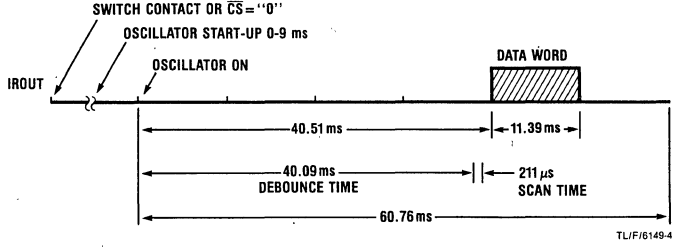


Figure 3. 1/3 Transmit Cycle

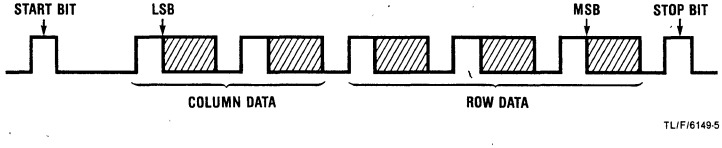


Figure 4. Data Word

Timing Diagrams (Continued)

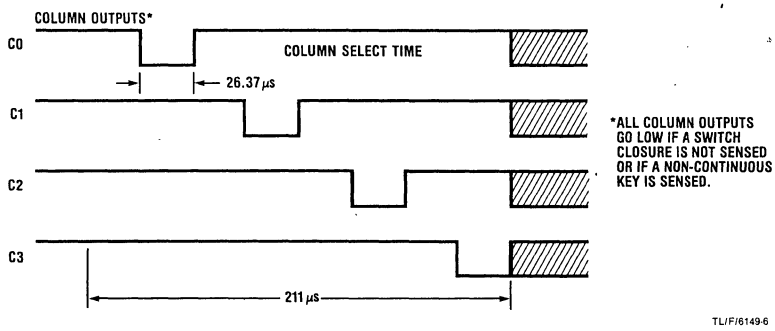


Figure 5. Column Scan Timing

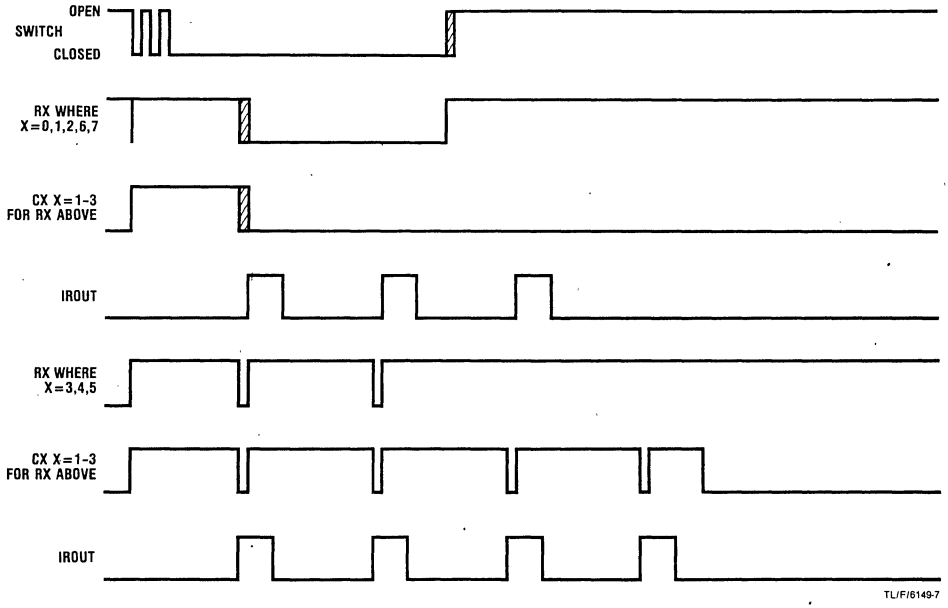


Figure 6a. Typical Transmit Cycles

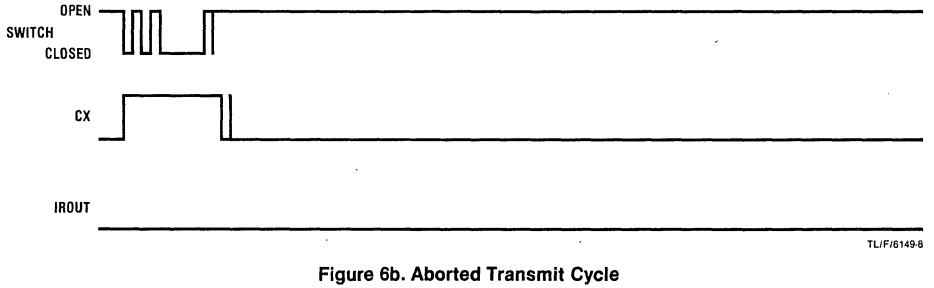


Figure 6b. Aborted Transmit Cycle

Timing Diagrams (Continued)

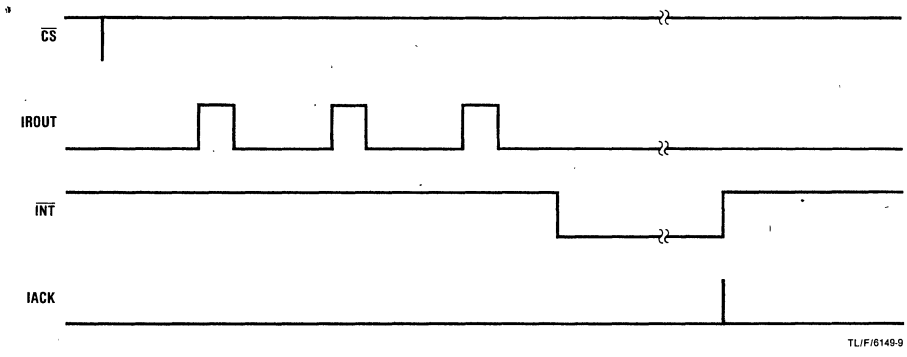


Figure 7. Interrupt Timing

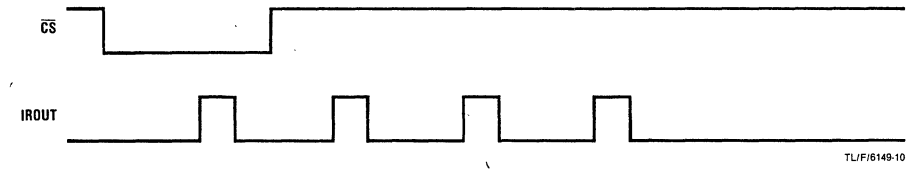


Figure 8. Typical Microprocessor Transmit Cycle

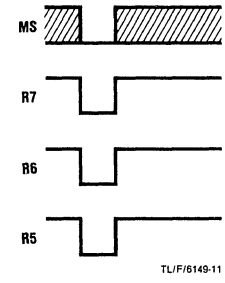


Figure 9. Reset Chip to Beginning of Transmit Cycle

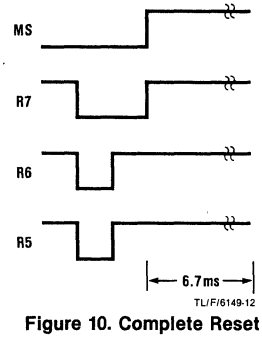


Figure 10. Complete Reset

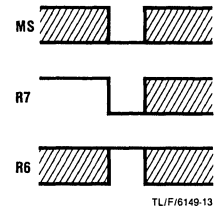


Figure 11. 6X Speed up of Transmit Cycle

Transmitter Functions

#	Code					Row								Column				Function	Notes
	16	8	4	2	1	0	1	2	3	4	5	6	7	0	1	2	3		
0	0	0	0	0	0	x								x				0 Direct Entry	1
1	0	0	0	0	1	x									x			1 Direct Entry	1
2	0	0	0	1	0	x										x		2 Direct Entry	1
3	0	0	0	1	1	x											x	3 Direct Entry	1
4	0	0	1	0	0		x							x				4 Direct Entry	1
5	0	0	1	0	1		x								x			5 Direct Entry	1
6	0	0	1	1	0		x									x		6 Direct Entry	1
7	0	0	1	1	1		x										x	7 Direct Entry	1
8	0	1	0	0	0			x						x				8 Direct Entry	1
9	0	1	0	0	1			x							x			9 Direct Entry	1
10	0	1	0	1	0			x								x		Memory Up	1
11	0	1	0	1	1			x									x	On/Off	1
12	0	1	1	0	0				x					x				Slow Up	2
13	0	1	1	0	1				x						x			Slow Down	2
14	0	1	1	1	0				x							x		Search Up	2
15	0	1	1	1	1				x								x	Mute	2
16	1	0	0	0	0					x				x				Analog I Down	2
17	1	0	0	0	1					x					x			Analog I Up	2
18	1	0	0	1	0					x						x		Analog II Down	2
19	1	0	0	1	1					x							x	Analog II Up	2
20	1	0	1	0	0						x			x				Analog III Down	2
21	1	0	1	0	1						x				x			Analog III Up	2
22	1	0	1	1	0						x					x		Analog IV Down	2
23	1	0	1	1	1						x						x	Analog IV Up	2
24	1	1	0	0	0							x		x				Not Defined	1
25	1	1	0	0	1							x			x				
26	1	1	0	1	0							x				x			
27	1	1	0	1	1							x					x		
28	1	1	1	0	0								x	x					
29	1	1	1	0	1								x		x				
30	1	1	1	1	0								x			x			
31	1	1	1	1	1								x				x		

Note 1: Three transmissions.

Note 2: Continuous transmission.

Typical Applications

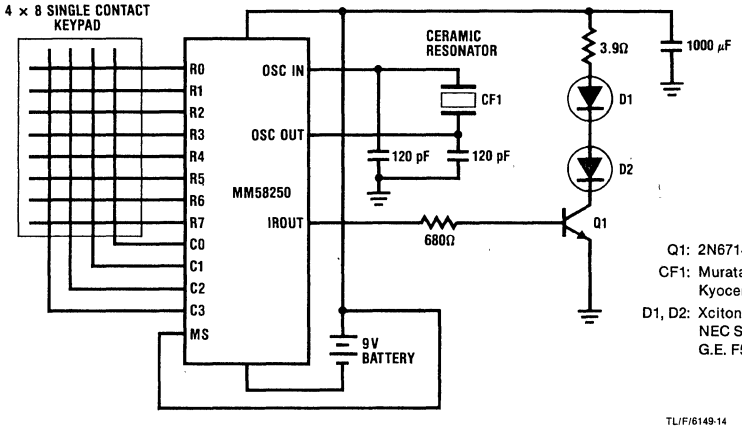


Figure 12

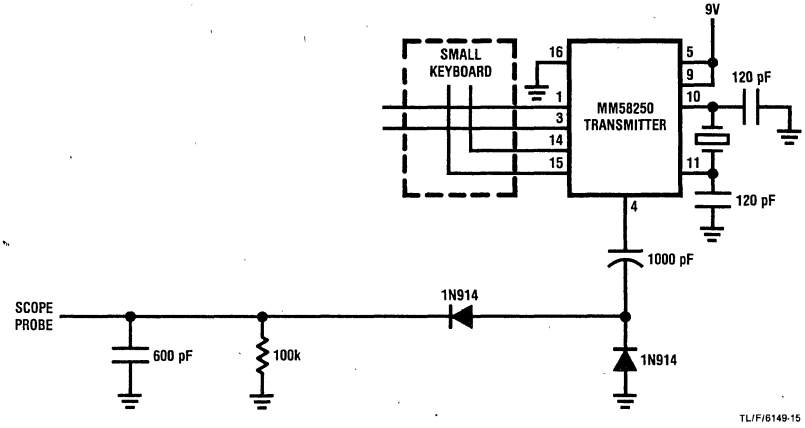


Figure 13. Quick Checkout Circuit

National Semiconductor

MM58274 Microprocessor Compatible Real Time Clock

General Description

The MM58274 is fabricated using low threshold metal gate CMOS technology and is designed to operate in bus oriented microprocessor systems where a real time clock and calendar function are required. The on-chip 32.768 kHz crystal controlled oscillator will maintain timekeeping down to 2.2V to allow low power standby battery operation. This device is pin compatible with the MM58174A but continues timekeeping up to tens of years. Faster access times are also offered.

Applications

- Point of sale terminals
- Teller terminals
- Word processors
- Data logging
- Industrial process control

Features

- Same pin-out as MM58174A
- Timekeeping from tenths of seconds to tens of years in independently accessible registers
- Leap year register
- Hours counter programmable for 12 or 24-hour operation
- Buffered crystal frequency output in test mode for easy oscillator setting
- Data-changed flag allows simple testing for time rollover
- Independent interrupting timer with open drain output
- Fully TTL compatible
- Low power standby operation (10 μA at 2.2V)
- Low cost 16-pin DIP

Block Diagram

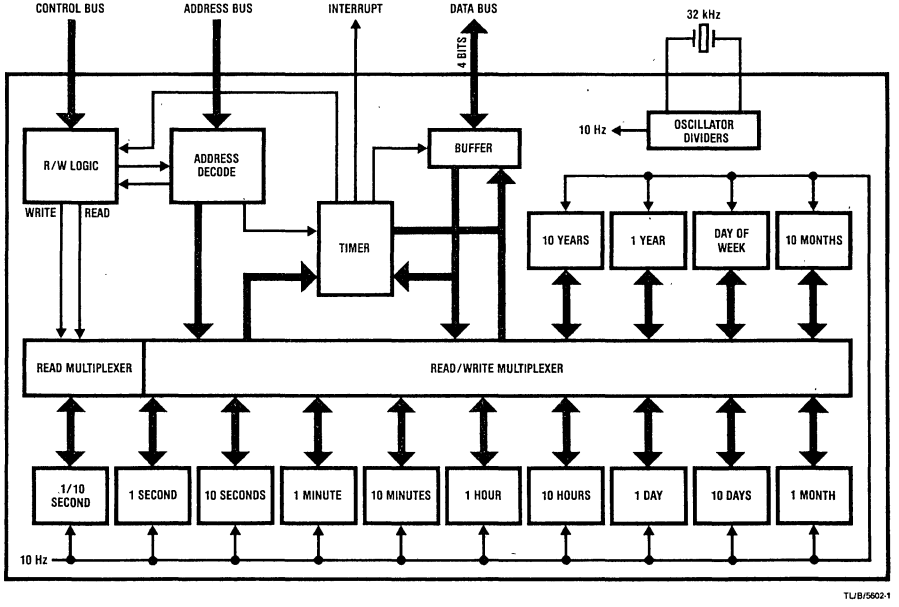


FIGURE 1

Absolute Maximum Ratings (Note 1)

DC Input or Output Voltage	$-0.3V$ to $V_{DD}+0.3V$
DC Input or Output Diode Current	± 5.0 mA
Storage Temperature, T_{STG}	$-65°C$ to $+150°C$
Supply Voltage, V_{DD}	6.5V
Power Dissipation, P_D	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Operating Supply Voltage	4.5	5.5	V
Standby Mode Supply Voltage	2.2	5.5	V
DC Input or Output Voltage	0	V_{DD}	V
Operating Temperature Range	−40	85	°C

Electrical Characteristics $V_{DD}=5V\pm10\%$, $T=-40°C$ to $+85°C$ unless otherwise stated

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage (except XTAL IN)		2.0			V
V_{IL}	Low Level Input Voltage (except XTAL IN)				0.8	V
V_{OH}	High Level Output Voltage (DB0-DB3)	$I_{OH}=-20\ \mu A$ $I_{OH}=-1.6$ mA	$V_{DD}-0.1$ 3.7			V V
V_{OH}	High Level Output Voltage (INT)	$I_{OH}=-20\ \mu A$ (In Test Mode)	$V_{DD}-0.1$			V
V_{OL}	Low Level Output Voltage (DB0-DB3, INT)	$I_{OL}=20\ \mu A$ $I_{OL}=1.6$ mA			0.1 0.4	V V
I_{IL}	Low Level Input Current (AD0-AD3, DB0-DB3)	$V_{IN}=V_{SS}$ (Note 2)			−80	μA
I_{IL}	Low Level Input Current ($\overline{WR}$, $\overline{RD}$)	$V_{IN}=V_{SS}$ (Note 2)			−190	μA
I_{IL}	Low Level Input Current ($\overline{CS}$)	$V_{IN}=V_{SS}$ (Note 2)			−550	μA
I_{OZH}	Output High Level Leakage Current (INT)	$V_{OUT}=V_{DD}$			2.0	μA
I_{DD}	Average Supply Current	$V_{DD}=2.2V$ (Standby Mode) $V_{DD}=5.0V$ (Active Mode)		4	10 1	μA mA
C_{IN}	Input Capacitance			5	10	pF
C_{OUT}	Output Capacitance	(Outputs Disabled)		10		pF

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. All voltages referenced to ground unless otherwise noted.

Note 2: The DB0-DB3 and AD0-AD3 lines all have active P-channel pull-up transistors which will source current. The $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ lines have internal pull-up resistors to V_{DD}.

AC Switching Characteristics

READ TIMING: DATA FROM PERIPHERAL TO MICROPROCESSOR $V_{DD} = 5V \pm 0.5V$, $C_L = 100$ pF

Symbol	Parameter	Commercial Specification $T_A = -40°C$ to $+85°C$			Units
		Min	Typ	Max	
t_{AD}	Address Bus Valid to Data Valid		500	850	ns
t_{CSD}	Chip Select On to Data Valid		250	425	ns
t_{RD}	Read Strobe On to Data Valid		250	425	ns
t_{RW}	Read Strobe Width (Note 3)			DC	
t_{RA}	Address Bus Hold Time from Trailing Edge of Read Strobe	0			ns
t_{CSH}	Chip Select Hold Time from Trailing Edge of Read Strobe	0			ns
t_{RH}	Data Hold Time from Trailing Edge of Read Strobe	100	250		ns
t_{HZ}	Time from Trailing Edge of Read Strobe Until O/P Drivers are TRI-STATE®	200	250	340	ns

WRITE TIMING: DATA FROM MICROPROCESSOR TO PERIPHERAL $V_{DD} = 5V \pm 0.5V$

Symbol	Parameter	Commercial Specification $T_A = -40°C$ to $+85°C$			Units
		Min	Typ	Max	
t_{AW}	Address Bus Valid to Write Strobe ↓ (Note 4)	600			ns
t_{CSW}	Chip Select On to Write Strobe ↓	350	175		ns
t_{DW}	Data Bus Valid to Write Strobe ↓	600	400		ns
t_{WW}	Write Strobe Width	350			ns
t_{WCS}	Chip Select Hold Time Following Write Strobe ↓	0			ns
t_{WA}	Address Bus Hold Time Following Write Strobe ↓	0			ns
t_{WD}	Data Bus Hold Time Following Write Strobe ↓	200			ns

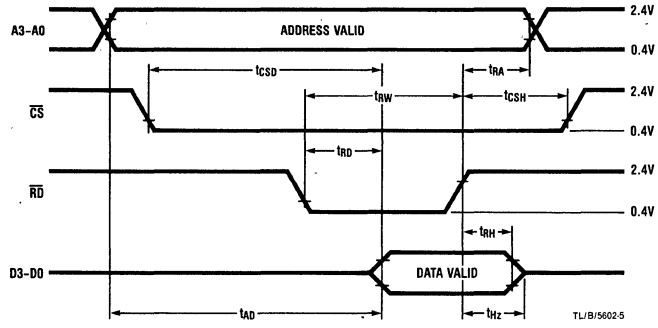
Note 3: Except for special case restriction: with interrupts programmed, max read strobe width of control register (ADDR 0) is 30 ms. See section on Interrupt Programming.

Note 4: All timings measured to the trailing edge of write strobe (data latched by the trailing edge of $\overline{WR}$).

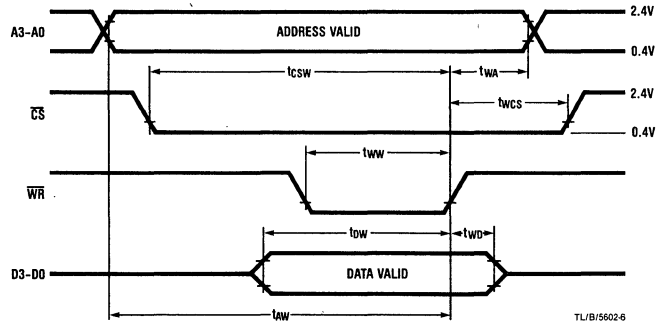
Note 5: Input test waveform peak voltages are 2.4V and 0.4V. Output signals are measured to their 2.4V and 0.4V levels.

Switching Time Waveforms

Read Cycle Timing (Note 5)



Write Cycle Timing (Note 5)



Connection Diagram

Dual-In-Line Package

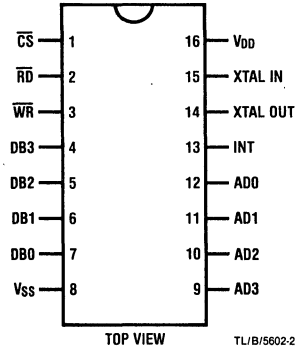


FIGURE 2

Order Number MM58274N
See NS Package N16E

Functional Description

The MM58274 is a bus oriented microprocessor real time clock. It has the same pin-out as the MM58174A while offering extended timekeeping up to units and tens of years. To enhance the device further, a number of other features have been added including: 12 or 24 hours counting, a testable data-changed flag giving easy error-free time reading and simplified interrupt control.

A buffered oscillator signal appears on the interrupt output when the device is in test mode. This allows for easy oscillator setting when the device is initially powered up in a system.

The counters are arranged as 4-bit words and can be randomly accessed for time reading and setting. The counters output in BCD (binary coded decimal) 4-bit numbers. Any register which has less than 4 bits (e.g., days of week uses only 3 bits) will return a logic 0 on any unused bits. When written to, the unused inputs will be ignored.

Functional Description (Continued)

Writing a logic 1 to the clock start/stop control bit resets the internal oscillator divider chain and the tenths of seconds counter. Writing a logic 0 will start the clock timing from the nearest second. The time then updates every 100 ms with all counters changing synchronously. Time changing during a read is detected by testing the data-changed bit of the control register after completing a string of clock register reads.

Interrupt delay times of 0.1s, 0.5s, 1s, 5s, 10s, 30s or 60s can be selected with single or repeated interrupt outputs. The open drain output is pulled low whenever the interrupt timer times out and is cleared by reading the control register.

CIRCUIT DESCRIPTION

The block diagram in *Figure 1* shows the internal structure of the chip. The 16-pin package outline is shown in *Figure 2.*

Crystal Oscillator

This consists of a CMOS inverter/amplifier with an on-chip bias resistor. Externally a 20 pF capacitor, a 6 pF–36 pF trimmer capacitor and a crystal are required to complete the 32.768 kHz timekeeping oscillator circuit.

The 6 pF–36 pF trimmer fine tunes the crystal load impedance, optimizing the oscillator stability. When properly adjusted (i.e., to the crystal frequency of 32.768 kHz), the circuit will display a frequency variation with voltage of less than 3 ppm/V.

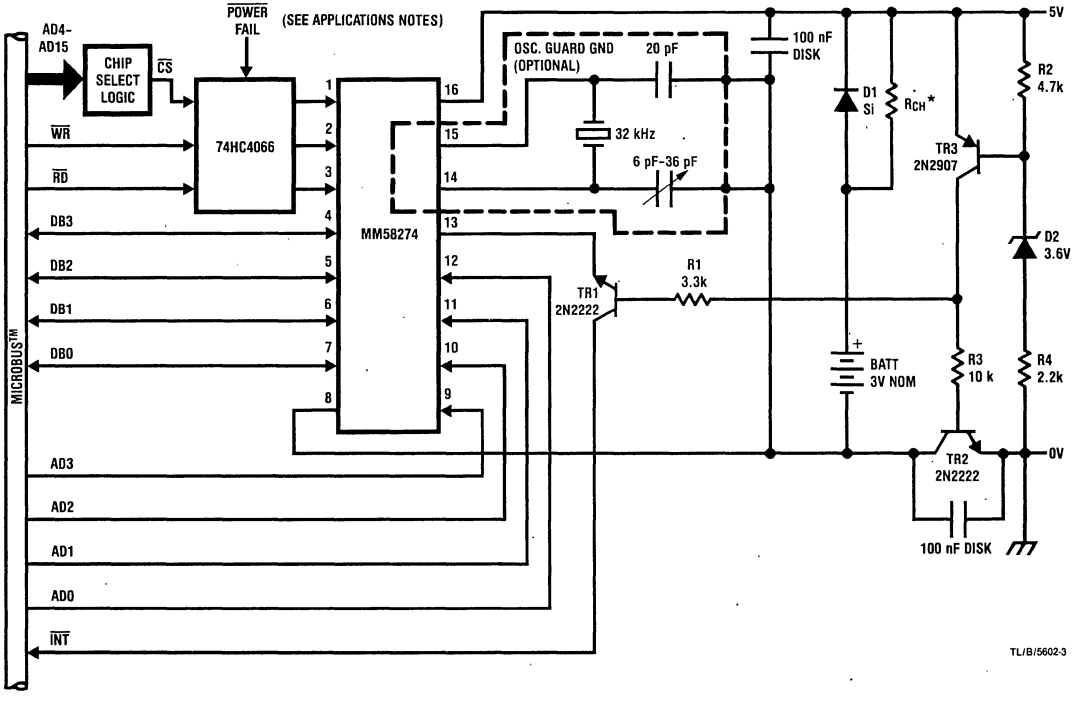
When the chip is enabled into test mode, the oscillator is gated onto the interrupt output pin giving a buffered oscillator output that can be used to set the crystal frequency when the device is installed in a system. For further information see the section on Test Mode.

Divider Chain

The crystal oscillator is divided down in three stages to produce a 10 Hz frequency setting pulse. The first stage is a non-integer divider which reduces the 32.768 kHz input to 30.720 kHz. This is further divided by a 9-stage binary ripple counter giving an output frequency of 60 Hz. A 3-stage Johnson counter divides this by six, generating a 10 Hz output. The 10 Hz clock is gated with the 32.768 kHz crystal frequency to provide clock setting pulses of 15.26 μs duration. The setting pulse drives all the time registers on the device which are synchronously clocked by this signal. All time data and the data-changed flag change on the falling edge of the clock setting pulse.

Data-Changed Flag

The data-changed flag is set by the clock setting pulse to indicate that the time data has been altered since the clock was last read. This flag occupies bit 3 of the control register where it can be tested by the processor to sense data-changed. It will be reset by a read of the control register. See the section, "Methods of Device Operation", for suggested clock reading techniques using this flag.



*Resistor is only used with Ni-CAD cells. Omit for lithium, silver or other primary cells.

FIGURE 3. Typical System Connection Diagram

Functional Description (Continued)

Seconds Counters

There are three counters for seconds:

a) tenths of seconds

b) units of seconds

c) tens of seconds.

The registers are accessed at the addresses shown in Table I. The tenths of seconds register is reset to 0 when the clock start/stop bit (bit 2 of the control register) is set to logic 1. The units and tens of seconds are set up by the processor, giving time setting to the nearest second. All three registers can be read by the processor for time output.

Minutes Counters

There are two minutes counters:

a) units of minutes

b) tens of minutes.

Both registers may be read to or written from as required.

Hours Counters

There are two hours counters:

a) units of hours

b) tens of hours.

Both counters may be accessed for read or write operations as desired.

In 12-hour mode, the tens of hours register has only one active bit and the top three bits are set to logic 0. Data bit 1 of the clock setting register is the AM/PM indicator; logic 0 indicating AM, logic 1 for PM.

When 24-hour mode is programmed, the tens of hours register reads out two bits of data and the two most significant bits are set to logic 0. There is no AM/PM indication and bit 1 of the clock setting register will read out a logic 0.

In both 12/24-hour modes, the units of hours will read out four active data bits. 12 or 24-hour mode is selected by bit 0 of the clock setting register; logic 0 for 12-hour mode, logic 1 for 24-hour mode.

Days Counters

There are two days counters:

a) units of days

b) tens of days.

The days counters will count up to 28, 29, 30 or 31 depending on the state of the months counters and the leap year counter. The microprocessor has full read/write access to these registers.

Months Counters

There are two months counters:

a) units of months

b) tens of months.

Both these counters have full read/write access.

Years Counters

There are two years counters:

a) units of years

b) tens of years.

Both these counters have full read/write access. The years will count up to 99 and roll over to 00.

TABLE I. Address Decoding of Real-Time Clock Internal Registers

Register Selected		Address (Binary)				(Hex)	Access
		AD3	AD2	AD1	AD0		
0	Control Register	0	0	0	0	0	Split Read and Write
1	Tenths of Seconds	0	0	0	1	1	Read Only
2	Units Seconds	0	0	1	0	2	R/W
3	Tens Seconds	0	0	1	1	3	R/W
4	Units Minutes	0	1	0	0	4	R/W
5	Tens Minutes	0	1	0	1	5	R/W
6	Units Hours	0	1	1	0	6	R/W
7	Tens Hours	0	1	1	1	7	R/W
8	Units Days	1	0	0	0	8	R/W
9	Tens Days	1	0	0	1	9	R/W
10	Units Months	1	0	1	0	A	R/W
11	Tens Months	1	0	1	1	B	R/W
12	Units Years	1	1	0	0	C	R/W
13	Tens Years	1	1	0	1	D	R/W
14	Day of Week	1	1	1	0	E	R/W
15	Clock Setting/ Interrupt Registers	1	1	1	1	F	R/W

Functional Description (Continued)

Day of Week Counter

The day of week counter increments as the time rolls from 23:59 to 00:00 (11:59 PM to 12:00 AM in 12-hour mode). It counts from 1 to 7 and rolls back to 1. Any day of the week may be specified as day 1.

Clock Setting Register/Interrupt Register

The interrupt select bit in the control register determines which of these two registers is accessible to the processor at address 15. Normal clock and interrupt timing operations will always continue regardless of which register is selected onto the bus. The layout of these registers is shown in Table II.

The clock setting register is comprised of three separate functions:

a) leap year counter: bits 2 and 3

b) AM/PM indicator: bit 1

c) 12/24-hour mode set: bit 0 (see Table IIA).

The leap year counter is a 2-stage binary counter which is clocked by the months counter. It changes state as the time rolls over from 11:59 on December 31 to 00:00 on January 1.

The counter should be loaded with the 'number of years since last leap year' e.g., if 1980 was the last leap year, a clock programmed in 1983 should have 3 stored in the leap year counter. If the clock is programmed during a leap year, then the leap year counter should be set to 0. The contents of the leap year counter can be read by the μP.

The AM/PM indicator returns a logic 0 for AM and a logic 1 for PM. It is clocked when the hours counter rolls from 11:59 to 12:00 in 12-hour mode. In 24-hour mode this bit is set to logic 0.

The 12/24-hour mode set determines whether the hours counter counts from 1 to 12 or from 0 to 23. It also controls the AM/PM indicator, enabling it for 12-hour mode and forcing it to logic 0 for the 24-hour mode. The 12/24-hour mode bit is set to logic 0 for 12-hour mode and it is set to logic 1 for 24-hour mode.

IMPORTANT NOTE: *Hours mode and AM/PM bits cannot be set in the same write operation. See the section on* Initialization (Methods of Device Operation) *for a suggested setting routine.*

All bits in the clock setting register may be read by the processor.

The interrupt register controls the operation of the timer for interrupt output. The processor programs this register for single or repeated interrupts at the selected time intervals.

The lower three bits of this register set the time delay period that will occur between interrupts. The time delays that can be programmed and the data words that select these are outlined in Table IIB.

Data bit 3 of the interrupt register sets for either single or repeated interrupts; logic 0 gives single mode, logic 1 sets for repeated mode.

Using the interrupt is described in the Device Operation section.

TABLE IIA. Clock Setting Register Layout

Function	Data Bits Used				Comments	Access
	DB3	DB2	DB1	DB0		
Leap Year Counter	X	X			0 Indicates a Leap Year	R/W
AM/PM Indicator (12-Hour Mode)			X		0 = AM 1 = PM 0 in 24-Hour Mode	R/W
12/24-Hour Select Bit				X	0 = 12-Hour Mode 1 = 24-Hour Mode	R/W

TABLE IIB. Interrupt Control Register

Function	Comments	Control Word			
		DB3	DB2	DB1	DB0
No Interrupt	Interrupt output cleared, start/stop bit set to 1.	X	0	0	0
0.1 Second	DB3 = 0 for single interrupt DB3 = 1 for repeated interrupt	0/1	0	0	1
0.5 Second		0/1	0	1	0
1 Second		0/1	0	1	1
5 Seconds		0/1	1	0	0
10 Seconds		0/1	1	0	1
30 Seconds		0/1	1	1	0
60 Seconds		0/1	1	1	1
Timing Accuracy: single interrupt mode (all time delays): ± 1 ms Repeated Mode: ± 1 ms on initial timeout, thereafter synchronous with first interrupt (i.e., timing errors do not accumulate).					

Functional Description (Continued)

Control Register

There are three registers which control different operations of the clock:

a) the clock setting register

b) the interrupt register

c) the control register.

The clock setting and interrupt registers both reside at address 15, access to one or the other being controlled by the interrupt select bit; data bit 1 of the control register.

The clock setting register programs the timekeeping of the clock. The 12/24-hour mode select and the AM/PM indicator for 12-hour mode occupy bits 0 and 1, respectively. Data bits 2 and 3 set the leap year counter.

The interrupt register controls the operation of the interrupt timer, selecting the required delay period and either single or repeated interrupt.

The control register is responsible for controlling the operations of the clock and supplying status information to the processor. It appears as two different registers; one with write only access and one with read only access.

The write only register consists of a bank of four latches which control the internal processes of the clock.

The read only register contains two output data latches which will supply status information for the processor. Table III shows the mapping of the various control latches and status flags in the control register. The control register is located at address 0.

The write only portion of the control register contains four latches:

A logic 1 written into the test bit puts the device into test mode. This allows setting of the oscillator frequency as well as rapid testing of the device registers, if required. A more complete description is given in the Test Mode section. For normal operation the test bit is loaded with logic 0.

The clock start/stop bit stops the timekeeping of the clock and resets to 0 the tenths of seconds counter. The time of day may then be written into the various clock registers and the clock restarted synchronously with an external time source. Timekeeping is maintained thereafter.

A logic 1 written to the start/stop bit halts clock timing. Timing is restarted when the start/stop bit is written with a logic 0.

The interrupt select bit determines which of the two registers mapped onto address 15 will be accessed when this address is selected.

A logic 0 in the interrupt select bit makes the clock setting register available to the processor. A logic 1 selects the interrupt register.

The interrupt start/stop bit controls the running of the interrupt timer. It is programmed in the same way as the clock start/stop bit; logic 1 to halt the interrupt and reset the timer, logic 0 to start interrupt timing.

When no interrupt is programmed (interrupt control register set to 0), the interrupt start/stop bit is automatically set to a logic 1. When any new interrupt is subsequently programmed, timing will not commence until the start/stop bit is loaded with 0.

In the single interrupt mode, interrupt timing stops when a timeout occurs. The processor restarts timing by writing logic 0 into the start/stop bit.

In repeated interrupt mode the interrupt timer continues to count with no intervention by the processor necessary.

Interrupt timing may be stopped in either mode by writing a logic 1 into the interrupt start/stop bit. The timer is reset and can be restarted in the normal way, giving a full time delay period before the next interrupt.

In general, the control register is set up such that writing 0's into it will start anything that is stopped, pull the clock out of test mode and select the clock setting register onto the bus. In other words, writing 0 will maintain normal clock operation and restart interrupt timing, etc.

The read only portion of the control register has two status outputs:

Since the MM58274 keeps real time, the time data changes asynchronously with the processor and this may occur while the processor is reading time data out of the clock.

Some method of warning the processor when the time data has changed must thus be included. This is provided for by the data-changed flag located in bit 3 of the control register. This flag is set by the clock setting pulse which also clocks the time registers. Testing this bit can tell the processor whether or not the time has changed. The flag is cleared by a read of the control register but not by any write operations. No other register read has any effect on the state of the data-changed flag.

Data bit 0 is the interrupt flag. This flag is set whenever the interrupt timer times out, pulling the interrupt output low. In a polled interrupt routine the processor can test this flag to determine if the MM58274 was the interrupting device. This interrupt flag and the interrupt output are both cleared by a read of the control register.

TABLE III. The Control Register Layout

Access (addr0)	DB3	DB2	DB1	DB0
Read From:	Data-Changed Flag	0	0	Interrupt Flag
Write To:	Test 0 = Normal 1 = Test Mode	Clock Start/Stop 0 = Clock Run 1 = Clock Stop	Interrupt Select 0 = Clock Setting Register 1 = Interrupt Register	Interrupt Start/Stop 0 = Interrupt Run 1 = Interrupt Stop

Functional Description (Continued)

Both of the flags and the interrupt output are reset by the trailing edge of the read strobe. The flag information is held latched during a control register read, guaranteeing that stable status information will always be read out by the processor.

Interrupt timeout is detected and stored internally if it occurs during a read of the control register, the interrupt output will then go low only after the read has been completed.

A clock setting pulse occurring during a control register read will *not* affect the data-changed flag since time data read out before or after the control read will not be affected by the time change.

METHODS OF DEVICE OPERATION

Test Mode

National Semiconductor uses test mode for functionally testing the MM58274 after fabrication and again after packaging. Test mode can also be used to set up the oscillator frequency when the part is first commissioned.

Figure 4 shows the internal clock connections when the device is written into test mode. The 32.768 kHz oscillator is gated onto the interrupt output to provide a buffered output for initial frequency setting. This signal is driven from a TRI-STATE output buffer, enabling easy oscillator setting in systems where interrupt is not normally used and there is no external resistor on the pin.

If an interrupt is programmed, the 32.768 kHz output is switched off to allow high speed testing of the interrupt timer. The interrupt output will then function as normal.

The clock start/stop bit can be used to control the fast clocking of the time registers as shown in *Figure 4*.

MM58274 Initialization

When it is first installed and power is applied, the device will need to be properly initialized. The following operation steps are recommended when the device is set up (all numbers are decimal):

1) Disable interrupt on the processor to allow oscillator setting. Write 15 into the control register: *The clock and interrupt start/stop bits are set to 1, ensuring that the clock and interrupt timers are both halted. Test mode and the interrupt register are selected.*

2) Write 0 to the interrupt register: *Ensure that there are no interrupts programmed and that the oscillator will be gated onto the interrupt output.*

3) Set oscillator frequency: *All timing has been halted and the oscillator is buffered out onto the interrupt line.*

4) Write 5 to the control register: *The clock is now out of test mode but is still halted. The clock setting register is now selected by the interrupt select bit.*

5) Set 12/24 Hours Mode: *Write to the clock setting register to select the hours counting mode required.*

6) Load Real-Time Registers: *All time registers (including Leap Years and AM/PM bit) may now be loaded in any order. Note that when writing to the clock setting register to set up Leap Years and AM/PM, the Hours Mode bit must not be altered from the value programmed in step 5.*

7) Write 0 to the control register: *This operation finishes the clock initialization by starting the time. The final control register write should be synchronized with an external time source.*

In general, timekeeping should be halted before the time data is altered in the clock. The data can, however, be altered at any time if so desired. Such may be the case if the user wishes to keep the clock corrected without having to stop and restart it; i.e., winter/summer time changing can be accomplished without halting the clock. This can be done in software by sensing the state of the data-changed flag and only altering time data just after the time has rolled over (data-changed flag set).

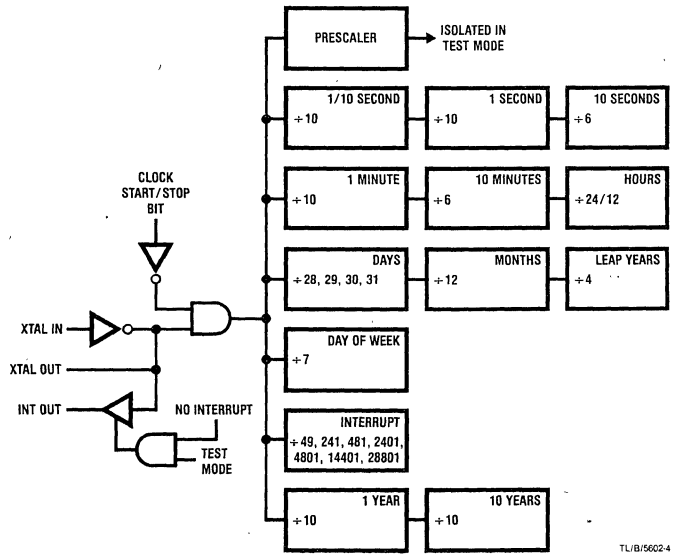


FIGURE 4. Test Mode Organization

Functional Description (Continued)

Reading the Time Registers

Using the data-changed flag technique supports microprocessors with block move facilities, as all the necessary time data may be read sequentially and then tested for validity as shown below.

1) Read the control register, address 0: *This is a dummy read to reset the data-changed flag (DCF) prior to reading the time registers.*

2) Read time registers: *All desired time registers are read out in a block.*

3) Read the control register and test DCF: *If DCF is cleared (logic 0), then no clock setting pulses have occurred since step 1. All time data is guaranteed good and time reading is complete.*

If DCF is set (logic 1), then a time change has occurred since step 1 and time data may not be consistent. Repeat steps 2 and 3 until DCF is clear. The control read of step 3 will have reset DCF, automatically repeating the step 1 action.

Interrupt Programming

The interrupt timer generates interrupts at time intervals which are programmed into the interrupt register. A single interrupt after delay or repeated interrupts may be programmed. Table IIB lists the different time delays and the data words that select them in the interrupt register.

Once the interrupt register has been used to set up the delay time and to select for single or repeat, it takes no further part in the workings of the interrupt system. All activity by the processor then takes place in the control register.

Initializing:

1) Write 3 to the control register (AD0): *Clock timing continues, interrupt register selected and interrupt timing stopped.*

2) Write interrupt control word to address 15: *The interrupt register is loaded with the correct word (chosen from Table IIB) for the time delay required and for single or repeated interrupts.*

3) Write 0 or 2 to the control register: *Interrupt timing commences. Writing 0 selects the clock setting register onto the data bus; writing 2 leaves the interrupt register selected. Normal timekeeping remains unaffected.*

On Interrupt:

Read the control register and test for Interrupt Flag (bit 0).

If the flag is cleared (logic 0), then the device is not the source of the interrupt.

If the flag is set (logic 1), then the clock did generate an interrupt. The flag is reset and the interrupt output is cleared by the control register read that was used to test for interrupt.

Single Interrupt Mode:

When appropriate, write 0 or 2 to the control register to restart the interrupt timer.

Repeated Interrupt Mode:

Timing continues, synchronized with the control register write which originally started interrupt timing. No further intervention is necessary from the processor to maintain timing.

In either mode interrupt timing can be stopped by writing 1 into the control register (interrupt start/stop set to 1). Timing for the full delay period recommences when the interrupt start/stop bit is again loaded with 0 as normal.

IMPORTANT NOTE: Using the interrupt timer places a constraint on the maximum Read Strobe width which may be applied to the clock. Normally all registers may be read from with a t_{RW} down to DC (i.e., $\overline{CS}$ and $\overline{RD}$ held continuously low). When the interrupt timer is active however, the maximum read strobe width that can be applied to the control register (Addr 0) is 30 ms.

This restriction is to allow the interrupt timer to properly reset when it times out. Note that it only affects reading of the control register—all other addresses in the clock may be accessed with DC read strobes, regardless of the state of the interrupt timer. Writes to any address are unaffected.

NOTES ON AC TIMING REQUIREMENTS

Although the Switching Time Waveforms show Microbus control signals used for clock access, this does not preclude the use of the MM58274 in other non-Microbus systems. *Figure 5* is a simplified logic diagram showing how the control signals are gated internally to control access to the clock registers. From this diagram it is clear that $\overline{CS}$ could be used to generate the internal data transfer strobes, with $\overline{RD}$ and $\overline{WR}$ inputs set up first. This situation is illustrated in *Figure 6.*

The internal data busses of the MM58274 are fully CMOS, contributing to the flexibility of the control inputs. When determining the suitability of any given control signal pattern for the MM58274, the timing specifications in AC Switching Characteristics should be examined. As long as these timings are met (or exceeded) the MM58274 will function correctly.

When the MM58274 is connected to the system via a peripheral port, the freedom from timing constraints allows for very simple control signal generation, as in *Figure 7.* For reading (*Figure 7a),* Address, $\overline{CS}$ and $\overline{RD}$ may be activated simultaneously and the data will be available at the port after t_{AD}-max (850 ns). For writing (*Figure 7b*), the address and data may be applied simultaneously and $\overline{CS}$ and $\overline{WR}$ strobed together.

Functional Description (Continued)

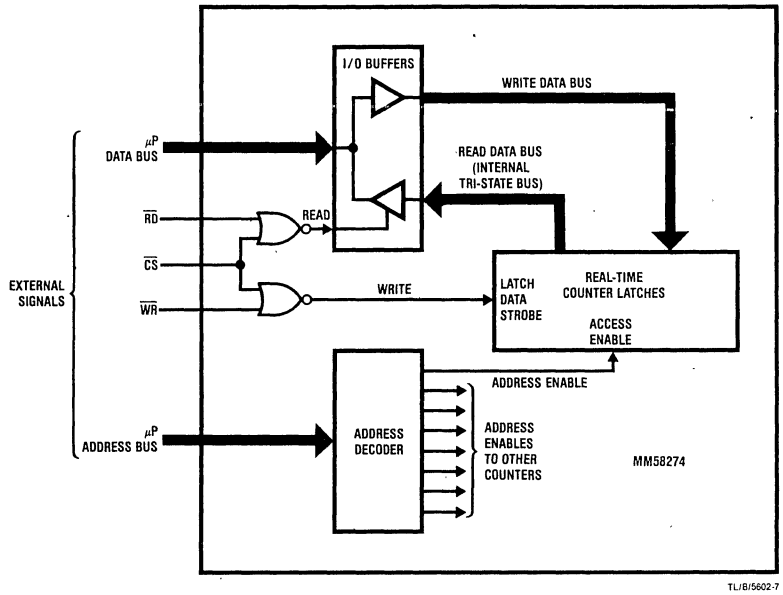


FIGURE 5. MM58274 Microprocessor Interface Diagram

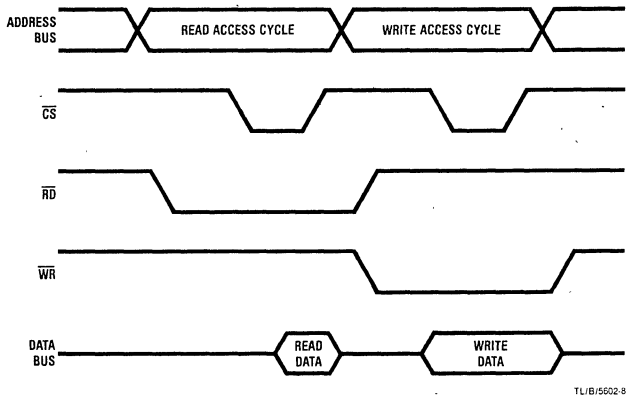
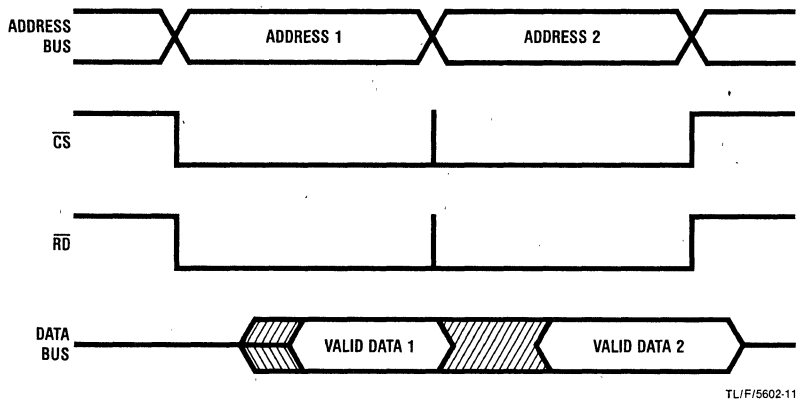
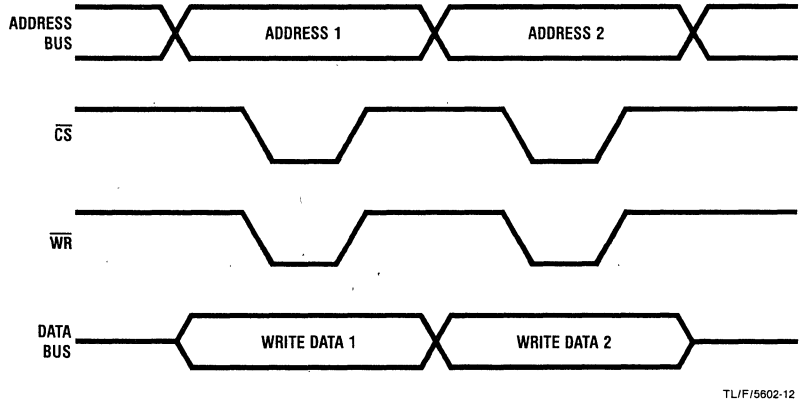


FIGURE 6. Valid MM58274 Control Signals Using Chip Select Generated Access Strobes

Functional Description (Continued)



a. Port Generated Read Access—2 Addresses Read Out



b. Port Generated Write Access—2 Addresses Written To

FIGURE 7. Simple Port Generated Control Signals

Functional Description (Continued)

APPLICATION NOTES

Time Reading Using Interrupt

In systems such as point of sale terminals and data loggers, time reading is usually only required on a random demand basis. Using the data-changed flag as outlined in the section on methods of operation is ideal for this type of system. Some systems, however, need to sense a change in real time; e.g., industrial timers/process controllers, TV/VCR clocks, any system where real time is displayed.

The interrupt timer on the MM58274 can generate interrupts synchronously with the time registers changing, using software to provide the initial synchronization.

In single interrupt mode the processor is responsible for initiating each timing cycle and the timed period is accurate to ± 1 ms.

In repeated interrupt mode the period from the initial processor start to the first timeout is also only accurate to ± 1 ms. The following interrupts maintain accurate delay periods relative to the first timeout. Thus, to utilize interrupt to control time reading, we will use repeated interrupt mode.

In repeated mode the time period between interrupts is exact, which means that timeouts will always occur at the same point relative to the internal clock setting pulses. The case for 0.1s interrupts is shown in *Figure A-1*. The same is true for other delay periods, only there will be more clock setting pulses between each interrupt timeout. If we set up the interrupt timer so that interrupt always times out just after the clock setting pulse occurs (*Figure A-2*), then there is no need to test the data-changed flag as we know that the time data has just changed and will not alter again for another 100 ms.

This can be achieved as outlined below:

1) Follow steps 1 and 2 of the section on interrupt programming. In step 2 set up for repeated interrupt.

2) Read control register AD0: *This is a dummy read to reset the data-changed flag.*

3) Read control register AD0 until data-changed flag is set.

4) Write 0 or 2 to control register. Interrupt timing commences.

Time Reading with Very Slow Read Cycles

If a system takes longer than 100 ms to complete reading of all the necessary time registers (e.g., when CMOS processors are used) or where high level interpreted language routines are used, then the data-changed flag will always be set when tested and is of no value. In this case, the time registers themselves must be tested to ensure data accuracy.

The technique below will detect both time changing *between* read strobes (i.e., between reading tens of minutes and units of hours) and also time changing *during* read, which can produce invalid data.

1) Read and store the value of the *lowest* order time register required.

2) Read out all the time registers required. The registers may be read out in any order, simplifying software requirements.

3) Read the lowest order register and compare it with the value stored previously in step 1. If it is still the same, then all time data is good. If it has changed, then store the new value and go back to step 2.

In general, the rule is that the first and last reads *must* both be of the lowest order time register. These two values can then be compared to ensure that no change has occurred. This technique works because for any higher order time register to change, all the lower order registers must also change. If the lowest order register does not change, then no higher order register has changed either.

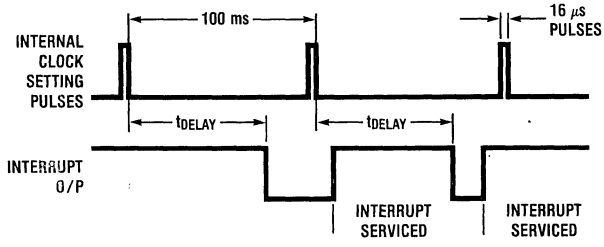


FIGURE A-1. Time Delay from Clock Setting Pulses to Interrupt is Constant

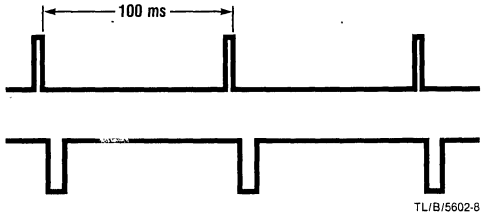


FIGURE A-2. Interrupt Timer Synchronized with Clock Setting Pulses

National Semiconductor

MM58341 High Voltage Display Driver

General Description

The MM58341 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58341 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays, (e.g., a 32-digit alphanumeric or dot matrix display).

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block and Connection Diagrams

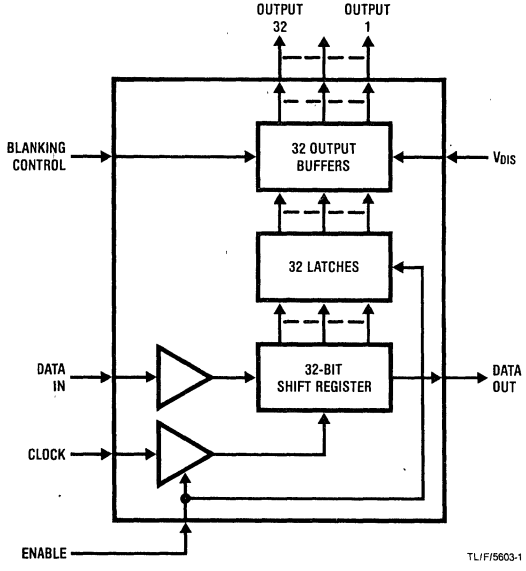


FIGURE 1

Dual-In-Line Package

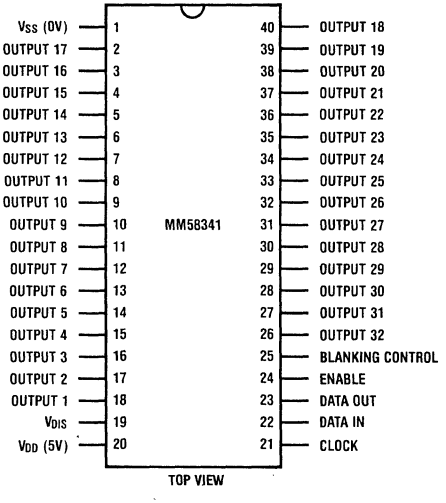


FIGURE 2

Order Number MM58341N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-36.5V$
$V_{DD}+\lvert V_{DIS}\rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS}=0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics $T_A=-40°C$ to $+85°C$, $V_{DD}=5V\pm0.5V$, $V_{SS}=0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN}=V_{SS}$ or V_{DD}, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-30V$, All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	$I_{OUT}=400\ \mu A$			0.4	V
V_{OH}	Logic '1'	$I_{OUT}=-10\ \mu A$	$V_{DD}-0.5$			V
V_{OH}	Logic '1'	$I_{OUT}=-500\ \mu A$	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN}=0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	$V_{DD}=5.5V$, $V_{SS}=0V$				
R_{OFF}	Output Off (*Figure 3a*)	$V_{DIS}=-10V$	55		250	kΩ
		$V_{DIS}=-20V$	60		300	kΩ
		$V_{DIS}=-30V$	65		400	kΩ
R_{ON}	Output On (*Figure 3b*)	$V_{DIS}=-10V$		700	800	Ω
		$V_{DIS}=-20V$		600	750	Ω
		$V_{DIS}=-30V$		500	680	Ω
V_{DOL}	Display Output Low Voltage	$V_{DD}=5.5V$, $I_{OUT}=$ Open Circuit, $-30V\le V_{DIS}\le-10V$	V_{DIS}		$V_{DIS}+2$	V

Note 1: 74LSTTL $V_{OH}=2.7V$ @ $I_{OUT}=-400\ \mu A$, TTL $V_{OH}=2.4V$ @ $I_{OUT}=-400\ \mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input	(Notes 3 and 4)				
Frequency, f_C				800	kHz
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns
Enable Input					
Set-Up Time, t_{ES}		100			ns
Hold Time, t_{EH}		100			ns
Data Output	$C_L = 50$ pF				
Clock Low to Data Out Time, t_{CDO}				500	ns

Note 2: Note that, for timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 800 kHz, 50% ± 10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58341 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58341 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58341 device, where output 1 (pin 18) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58341, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58341.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'–'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58341, being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58341 is used to provide the grid drive for a 32-digit 5 × 7 dot matrix vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.

Functional Description (Continued)

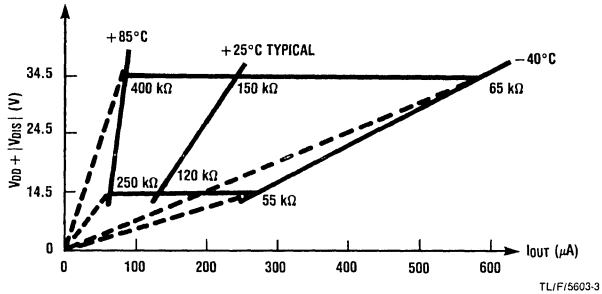


FIGURE 3a. Output Impedance Off

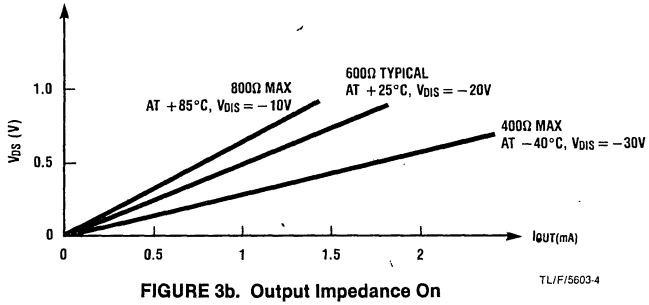
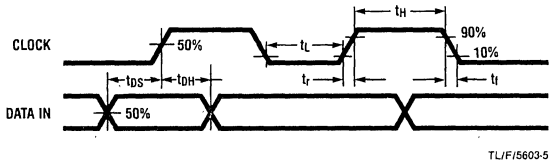


FIGURE 3b. Output Impedance On

Timing Diagrams



For the purposes of AC measurements, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

FIGURE 4. Clock and Data Timings

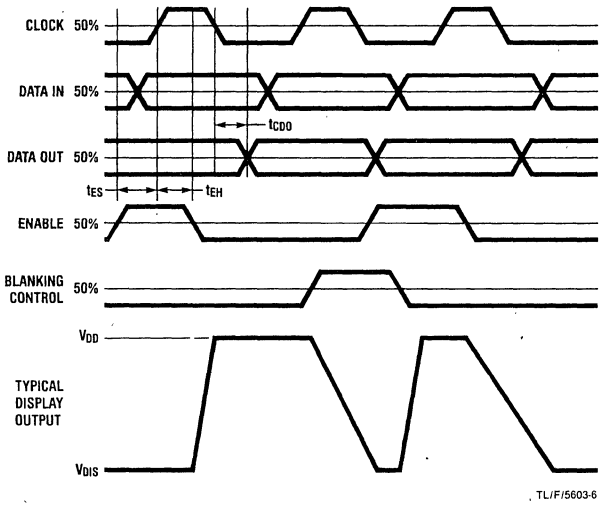


FIGURE 5. MM58341 Timings (Data Format)

7

Typical Application

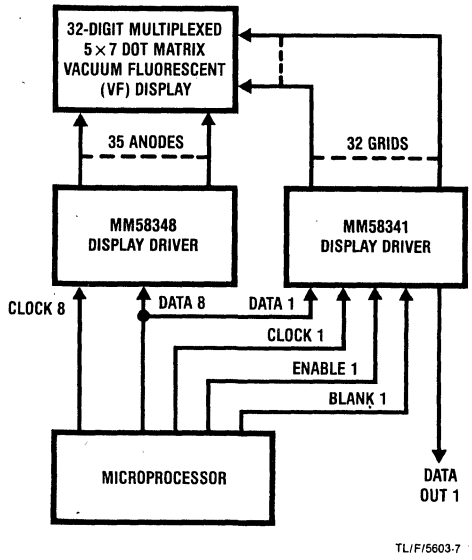


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

MM58342 High Voltage Display Driver

General Description

The MM58342 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 28-pin molded dual-in-line packages or as dice. The MM58342 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 20-digit alphanumeric or dot matrix display).

Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block and Connection Diagrams

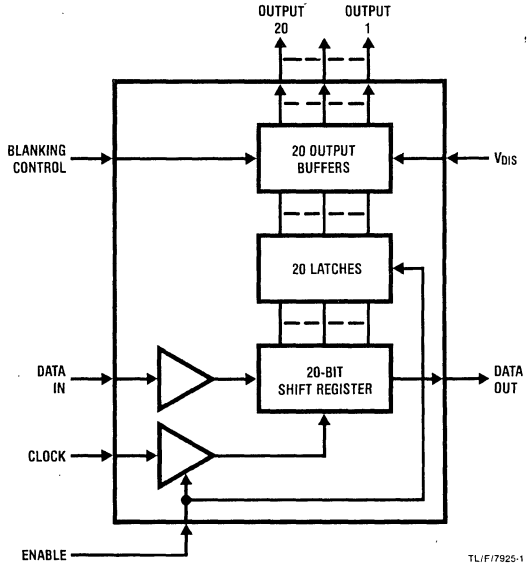


FIGURE 1

Dual-In-Line Package

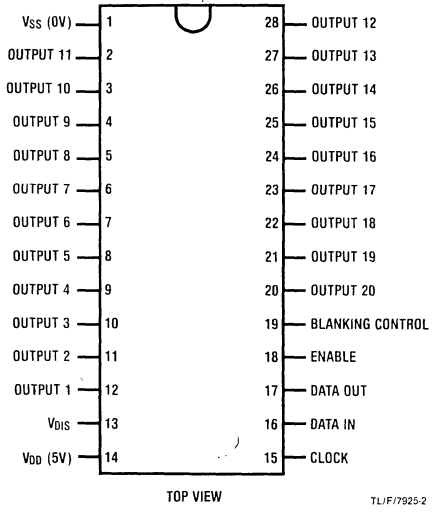


FIGURE 2

Order Number MM58342N
See NS Package N28B

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-36.5V$
$V_{DD}+\lvert V_{DIS}\rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS}=0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics $T_A=-40°C$ to $+85°C$, $V_{DD}=5V\pm0.5V$, $V_{SS}=0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN}=V_{SS}$ or V_{DD}, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-30V$ All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK ENABLE, BLANK					
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'	(Note 1)	2.4			V
	Data Output Logic Levels					
V_{OL}	Logic '0'	$I_{OUT}=400\ \mu A$			0.4	V
V_{OH}	Logic '1'	$I_{OUT}=-10\ \mu A$	$V_{DD}-0.5$			V
V_{OH}	Logic '1'	$I_{OUT}=-500\ \mu A$	2.8			V
I_{IN}	Input Currents DATA IN, CLOCK ENABLE, BLANK	$V_{IN}=0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK ENABLE, BLANK				15	pF
	Display Output Impedances	$V_{DD}=5.5V$, $V_{SS}=0V$				
R_{OFF}	Output Off (*Figure 3a*)	$V_{DIS}=-10V$	55		250	kΩ
		$V_{DIS}=-20V$	60		300	kΩ
		$V_{DIS}=-30V$	65		400	kΩ
R_{ON}	Output On (*Figure 3b*)	$V_{DIS}=-10V$		700	800	Ω
		$V_{DIS}=-20V$		600	750	Ω
		$V_{DIS}=-30V$		500	680	Ω
V_{DOL}	Display Output Low Voltage	$V_{DD}=5.5V$, $I_{OUT}=$ Open Circuit, $-30V\le V_{DIS}\le-10V$	V_{DIS}		$V_{DIS}+2$	V

Note 1: 74LSTTL $V_{OH}=2.7V$ @ $I_{OUT}=-400\ \mu A$, TTL $V_{OH}=2.4V$ @ $I_{OUT}=-400\ \mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input	(Notes 3 and 4)				
Frequency, f_C				800	kHz
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns
Enable Input					
Set-Up Time, t_{ES}		100			ns
Hold Time, t_{EH}		100			ns
Data Output	$C_L = 50$ pF				
CLOCK Low to Data Out Time, t_{CDO}				500	ns

Note 2: For timing purposes, the signals ENABLE and BLANK can be considered to be totally independent of each other.

Note 3: AC input waveform specification for test purposes: t_r, $t_f \leq 20$ ns, $f = 800$ kHz, 50% ± 10% duty cycle.

Note 4: Clock input rise and fall times must not exceed 5 μs.

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58342 uses three signals, DATA IN, CLOCK and ENABLE, where ENABLE acts as an external load signal. Display blanking can be achieved by means of the BLANKING CONTROL input, and a logic '1' will turn off all sections of the display. A block diagram of the MM58342 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58342 device, where output 1 (pin 12) is equivalent to bit 1 (i.e., the first bit of data to be loaded into the shift register following ENABLE high). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58342, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.

Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58342.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of ENABLE, and so all interface signals should be inactive at power on.

In *Figure 5,* the ENABLE signal acts as an envelope, and only while this signal is at a logic '1' does the circuit accept CLOCK input signals. Data is transferred and shifted in the internal shift register on the rising clock edge, i.e., '0'-'1' transition. When the ENABLE signal goes low, the contents of the shift registers are latched, and the display will show new data. During data transfer, the display will show old data. DATA OUT is also provided on the MM58342 being output on the falling edge. At any time, the display may be blanked under processor control, using the BLANKING CONTROL input.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58342 is used to provide the grid drive for a 40-digit 2 line 5 × 7 multiplexed vacuum fluorescent (VF) display. The anode drive in this example is provided by another member of the high voltage display driver family, namely the MM58348, which does not require an externally generated load signal.

Functional Description (Continued)

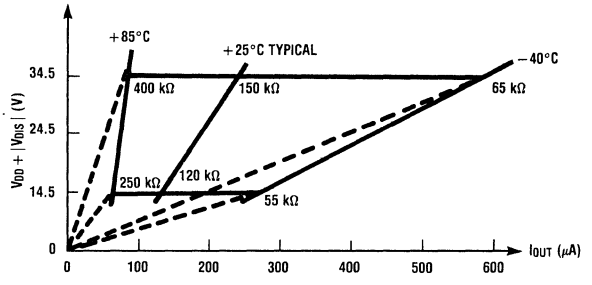


FIGURE 3a. Output Impedance Off

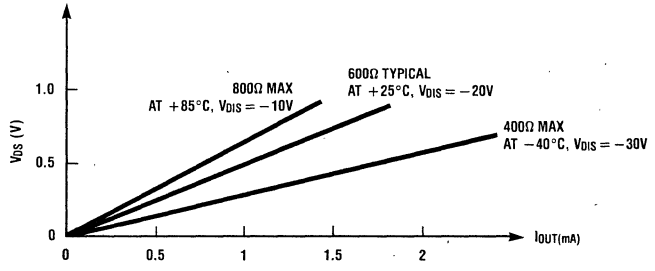
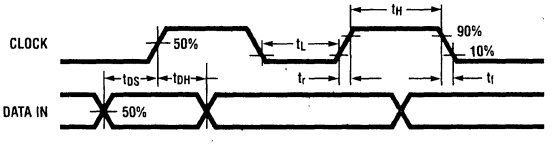


FIGURE 3b. Output Impedance On

Timing Diagrams



For the purposes of AC measurements, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$.

FIGURE 4. Clock and Data Timings

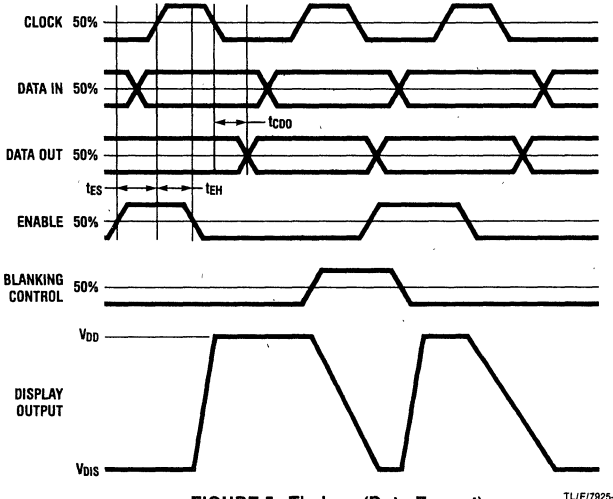


FIGURE 5. Timings (Data Format)

Typical Application

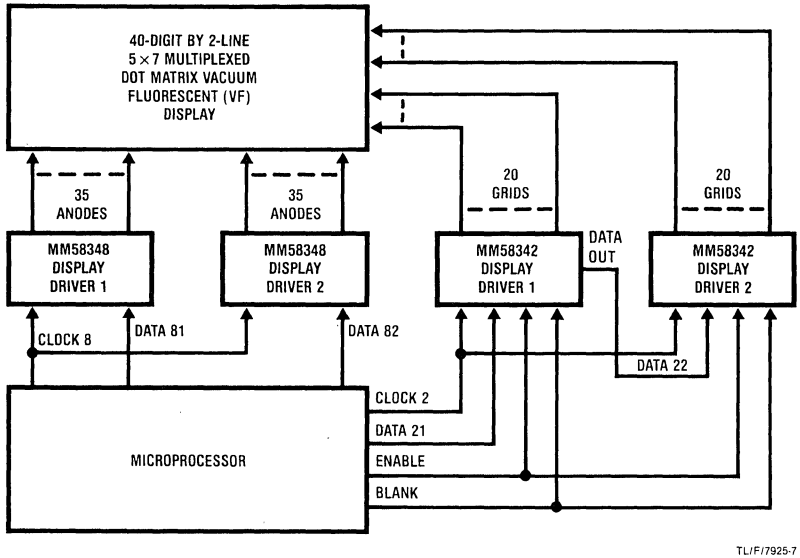


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

PRELIMINARY

MM58348 High Voltage Display Driver

General Description

The MM58348 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58348 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays (e.g., a 5 x 7 dot matrix display).

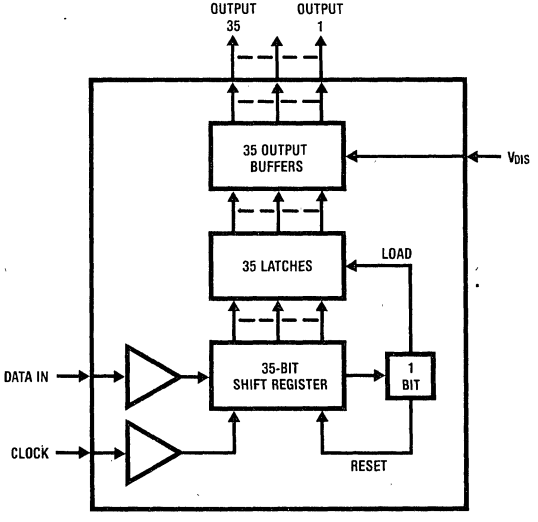
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- No load signal required

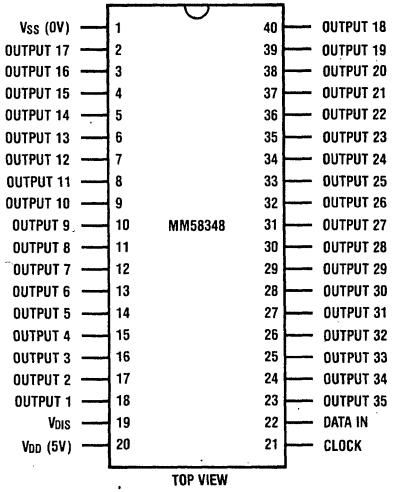
Block and Connection Diagrams



TL/F/5601-1

FIGURE 1

Dual-In-Line Package



TL/F/5601-2

FIGURE 2

Order Number MM58348N
See NS Package N40A

Absolute Maximum Ratings

Voltage at Any Input Pin	$V_{DD}+0.3V$ to $V_{SS}-0.3V$
Voltage at Any Display Pin	V_{DD} to $V_{DD}-36.5V$
$V_{DD}+\lvert V_{DIS}\rvert$	36.5V
Storage Temperature	−65°C to +150°C
Power Dissipation	500 mW at +85°C
Junction Temperature	130°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{DD}) $V_{SS}=0V$	4.5	5.5	V
Display Voltage (V_{DIS})	−30	−10	V
Temperature Range	−40	+85	°C

DC Electrical Characteristics $T_A=-40°C$ to $+85°C$, $V_{DD}=5V\pm0.5V$, $V_{SS}=0V$ unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Power Supply Currents					
I_{DD}		$V_{IN}=V_{SS}$ or V_{DD}, $V_{DD}=5.5V$, $V_{SS}=0V$, V_{DIS} Disconnected			150	μA
I_{DIS}		$V_{DD}=5.5V$, $V_{SS}=0V$, $V_{DIS}=-30V$, All Outputs Low			10	mA
	Input Logic Levels DATA IN, CLOCK	(Note 1)				
V_{IL}	Logic '0'				0.8	V
V_{IH}	Logic '1'		2.4			V
I_{IN}	Input Currents DATA IN, CLOCK	$V_{IN}=0V$ or V_{DD}	−10		10	μA
C_{IN}	Input Capacitance DATA IN, CLOCK				15	pF
	Display Output Impedances	$V_{DD}=5.5V$, $V_{SS}=0V$				
R_{OFF}	Output Off (*Figure 3a*)	$V_{DIS}=-10V$	55		250	kΩ
		$V_{DIS}=-20V$	60		300	kΩ
		$V_{DIS}=-30V$	65		400	kΩ
R_{ON}	Output On (*Figure 3b*)	$V_{DIS}=-10V$		700	800	Ω
		$V_{DIS}=-20V$		600	750	Ω
		$V_{DIS}=-30V$		500	680	Ω
V_{DOL}	Display Output Low Voltage	$V_{DD}=5.5V$, $I_{OUT}=$ Open Circuit, $-30V\le V_{DIS}\le-10V$	V_{DIS}		$V_{DIS}+2$	V

Note 1: 74LSTTL $V_{OH}=2.7V$ @ $I_{OUT}=-400\,\mu A$, TTL $V_{OH}=2.4V$ @ $I_{OUT}=-400\,\mu A$.

AC Electrical Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V \pm 0.5V$

Parameter	Conditions	Min	Typ	Max	Units
Clock Input	(Notes 2 and 3)				
Frequency, f_C				1.0	MHz
High Time, t_H		300			ns
Low Time, t_L		300			ns
Data Input					
Set-Up Time, t_{DS}		100			ns
Hold Time, t_{DH}		100			ns

Note 2: AC input waveform specification for test purpose: $t_r \leq 20$ ns, $t_f \leq 20$ ns, f = 1 MHz, 50% ± 10% duty cycle.
Note 3: Clock input rise and fall times must not exceed 5 μs.

Functional Description

This product is specifically designed to drive multiplexed or non-multiplexed high voltage alphanumeric or dot matrix vacuum fluorescent (VF) displays. Character generation is done externally in the microprocessor, with a serial data path to the display driver. The MM58348 uses two signals, DATA IN and CLOCK, with a format of a leading '1' followed by the 35 data bits, hence allowing data transfer without an additional signal. A block diagram of the MM58348 is shown in *Figure 1.*

Figure 2 shows the pinout of the MM58348 device, where output 1 (pin 18) is equivalent to bit 1, (i.e., the first bit of data to be loaded into the shift register following the start bit). A logic '1' at the input will turn on the corresponding display digit/segment/dot output.

A significant reduction in discrete board components can be achieved by use of the MM58348, because external pull-down resistors are not required. Due to the nature of the output stage, both its on and off impedance values vary as a function of the display voltage applied. However, *Figures 3a and 3b* show that this output impedance will remain constant for a fixed value of display voltage.

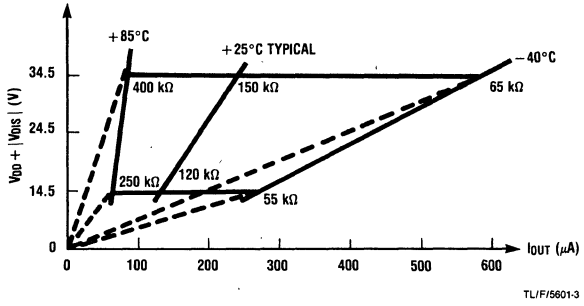


FIGURE 3a. Output Impedance Off

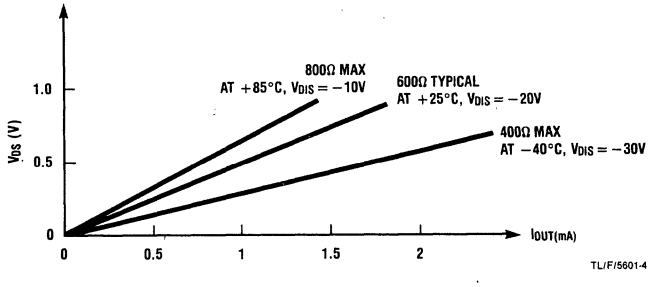


FIGURE 3b. Output Impedance On

Functional Description (Continued)

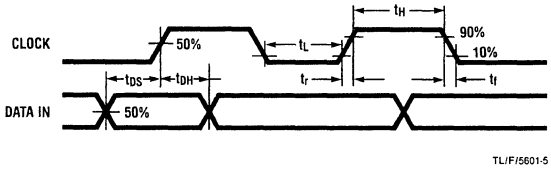
Figure 4 demonstrates the critical timing requirements between CLOCK and DATA IN for the MM58348.

When the chip first powers on, an internal reset is generated, resetting all registers and latches. The chip returns to normal operation on application of the start bit and the first clock pulse, and so all interface signals should be inactive at power on.

In *Figure 5,* a start bit of logic '1' precedes the 35 bits of data, each bit being accepted on the rising edge of CLOCK, i.e., a '0'-'1' transition. At the 36th clock, a LOAD signal is generated synchronously with the high state of the clock, thus loading the 35 bits of the shift register into the latches. At the low state of the clock, a RESET signal is generated, clearing all bits of the shift register for the next set of data. Hence, a complete set of 36 clock pulses is needed for the MM58348, or the shift register will not clear. If, at any given time, it is required that the display be cleared under microprocessor control, i.e., without power on reset, then the following flushing routine may be used. Clock in 36 'zeroes', followed by a 'one' (start bit), followed by 35 'zeroes'. This procedure will completely blank the display.

Figure 6 shows a schematic diagram of a microprocessor-based system where the MM58348 is used to provide the anode drive for a 32-digit 5 x 7 dot matrix vacuum fluorescent (VF) display. The grid drive in this example is provided by another member of the high voltage display driver family, namely the MM58341, which has the additional features of a BLANKING CONTROL pin, a DATA OUT pin, and an ENABLE (external load signal) pin.

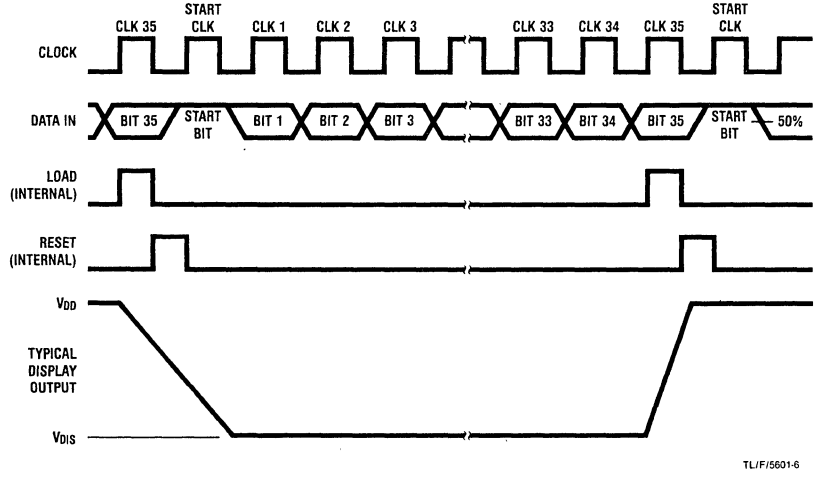
Timing Diagrams



TL/F/5601-5

For the purpose of AC measurement, $V_{IH} = 2.4V$, $V_{IL} = 0.8V$

FIGURE 4. Clock and Data Timings



TL/F/5601-6

FIGURE 5. MM58348 Timings (Data Format)

Typical Application

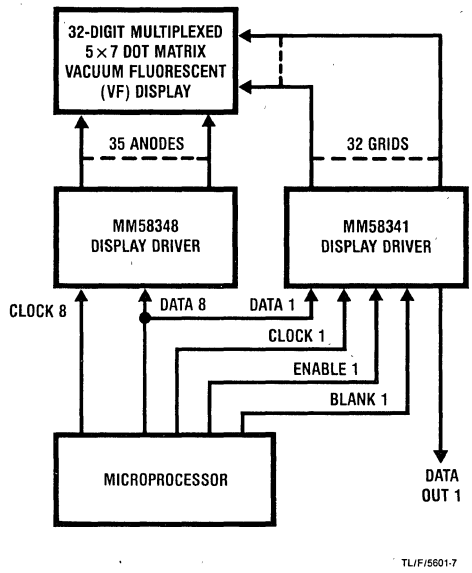


FIGURE 6. Microprocessor-Controlled Word Processor

National Semiconductor

PRELIMINARY

MM58438 32-Bit LCD Display Driver

General Description

The MM58438 is a CMOS metal gate circuit which is capable of driving up to 32 LCD segments and is available in a 40-pin molded package. In addition, MM58438 dice is available for PCB module assembly systems. The circuit requires a minimum of interface between data source and display and can be cascaded where larger displays are required.

Features

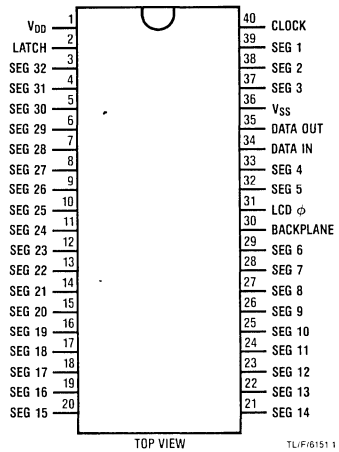
- Serial data input
- 32 segment outputs
- Cascaded operation capability
- Alphanumeric and bar graph capability
- TTL compatibility
- Non-multiplex display
- Compatible with HLCD 0438, HLCD 0438A
- Stable oscillator only requires one external component

Applications

- COPS™ or microprocessor displays
- Instrumentation readouts
- Digital clock, thermometer, counter, voltmeter displays
- Industrial control indicator
- Serial to parallel converter

Connection and Block Diagrams

Dual-In-Line Package



Order Number MM58438N
See NS Package N40A

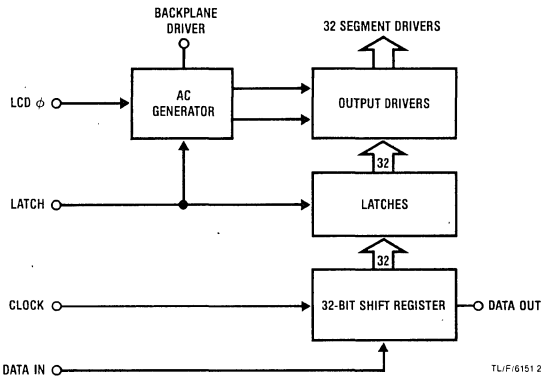


FIGURE 1

7

Absolute Maximum Ratings

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
V_{DD} Supply Voltage	18V
Operating Temperature	−40°C to +85°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics V_{DD} = 3.0V to 15V, T_A = −40°C to +85°C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Voltage V_{DD}		3.0		15	V
Supply Current I_{DD}	Oscillating or Driven Mode, V_{DD} = 5V			60	μA
Input High Level V_{IH}	V_{DD} = 4.5V to 5.5V V_{DD} = 5.5V to 15V	2.4 0.5 V_{DD}		V_{DD} V_{DD}	V V
Input Low Level V_{IL}	V_{DD} = 4.5V to 5.5V V_{DD} = 5.5V to 15V	0 0		0.8 0.1 V_{DD}	V V
Input Current (Any Input)				±10	μA
Input Capacitance				10	pF
Output Current Levels Segments Sink I_{OL} Source I_{OH}	 V_{DD} = 4.5V, V_{OUT} = 0.2V V_{DD} = 4.5V, V_{OUT} = V_{DD} − 0.2V	 20 20			 μA μA
Backplane Sink I_{OL} Source I_{OH}	 V_{DD} = 4.5V, V_{OUT} = 0.2V V_{DD} = 4.5V, V_{OUT} = V_{DD} − 0.2V	 320 320			 μA μA
Data Output Sink Source	 V_{DD} = 4.5V, V_{OUT} = 0.5V V_{DD} = 4.5V, V_{OUT} = V_{DD} − 0.5V	 100		−100	 μA μA

Note 1: Output offset voltage with segment capacitance = 250 pF and backplane capacitance = 8750 pF is ±50 mV.

AC Electrical Characteristics V_{DD} = 3.0V to 15V, T_A = −40°C to +85°C unless otherwise specified *(Figure 2)*

Parameter	Conditions	Min	Typ	Max	Units
t1 Data Hold Time		0.1			μs
t2 Data Set-Up Time		0.1			μs
t3 Latch Pulse Width		1			μs
t4 Clock to Latch Time		0.1			μs
t_{pd} Data Out Delay				500	ns
Clock Frequency f		DC		500	kHz
Clock Period t(= 1/f)		2			μs
Backplane Frequency	C_{EXT} = 47 pF		100		Hz
Oscillator Stability	V_{DD} = 5V			±50	%

Note 2: V_{DD} rise time (0V to 5V) must not exceed 5 ms.

Functional Description

The connection diagram for the MM58438 is shown on the first page. The circuit is designed to drive LCD displays directly. Serial data transfer from the data source to the display driver is accomplished with 3 signals, SERIAL DATA, CLOCK and LATCH.

The MM58438 uses a latch mode of microprocessor data transfer whereby the signal LATCH acts as a latch to the input data *(Figure 2)*. Data is input to and output from the internal shift register on the negative clock edge (i.e., a logic '1' to logic '0' transition) while the LATCH pin is held low. The contents of the shift register are latched to the output latches and display drivers on the logic '0' to logic '1' transition of the LATCH pin when it is pulsed high.

The MM58438 can be cascaded when a larger display is required where it can be considered to be driven or oscillating.

In the oscillating mode, the BACKPLANE frequency is determined by the capacitor connected to the LCD ϕ pin. When two circuits are cascaded the second LCD ϕ input is driven by the first backplane output.

When the circuit is first powered on, an internal power on reset signal is generated which primes the mode detect logic and sets the BACKPLANE to a logical high level. If the circuit is in the oscillating mode the LCD ϕ pin is connected to a capacitor which is held low by a high impedance internal pull down transistor. If the circuit is in the driven mode the LCD ϕ pin is connected to the previous BACKPLANE output and is forced high by this low impedance output. When the first LATCH pulse goes to a logic '1' the level on the LCD ϕ pin is internally latched which indicates to the rest of the logic whether the circuit is driven or oscillating.

The oscillator on the oscillating device starts as soon as the LATCH pin goes to a logic '1'.

In the driven mode, the BACKPLANE frequency is in phase with the input frequency on the LCD ϕ.

To ensure the correct latching of this function, the LATCH input must be held at a logic '0' level for a minimum of 10 μs at power on.

Once the initial conditions on power up have been obeyed, the circuit can be used as serial to parallel converters with the polarity of the output data determined by the logic level on the LCD ϕ input. A logic '1' on the LCD ϕ input produces inverted data.

Timing Diagram

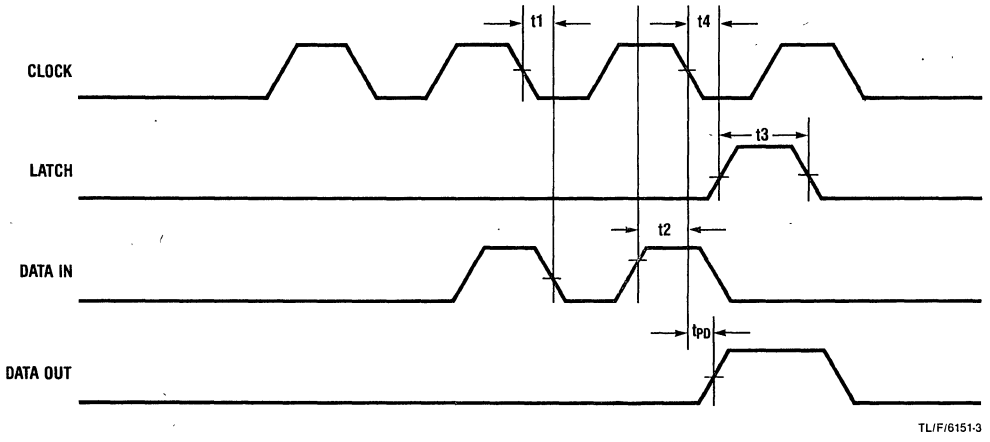


FIGURE 2

Typical Application

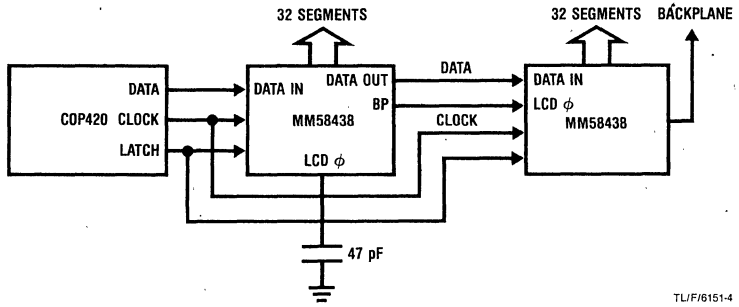


FIGURE 3. 64-Segment Display Cascading Two MM58438s

National Semiconductor

PRELIMINARY

MM58538 Multiplexed LCD Driver

General Description

The MM58538 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P- and N-channel devices, which drives an 8 row by 26 column dot matrix LCD array directly under the control of an external microprocessor. The MM58538 can be used with an MM58539 to drive a display that has up to 8 rows and an arbitrary number of columns. Data is input serially from the microprocessor which will service the drivers in response to an interrupt signal.

The circuit is available in a 40-pin molded dual-in-line package or dice.

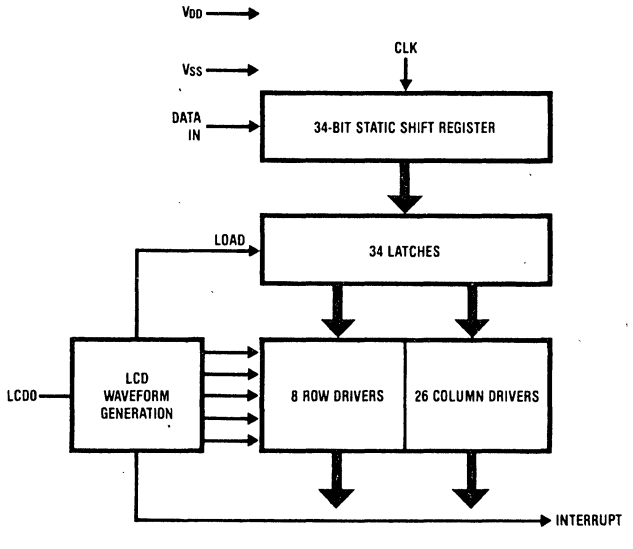
Features

- Drives up to 8 rows and 26 columns
- Expandable to larger displays with MM58539
- Flexible organization allows any display pattern
- Simple 3 line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On chip oscillator
- Compatible with HLCD 0538

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

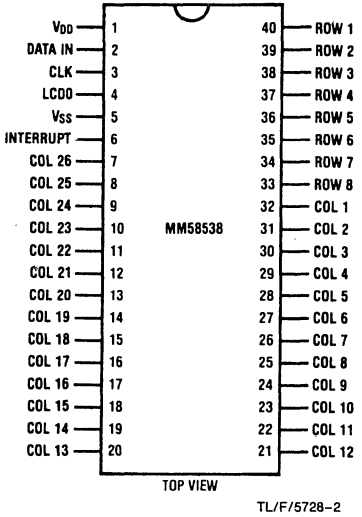
Block and Connection Diagrams



TL/F/5728–1

FIGURE 1

Dual-In-Line Package



TL/F/5728–2

FIGURE 2

Absolute Maximum Ratings (Note 1)

DC Input or Output Voltage	$-0.3V$ to $V_{DD}+0.3V$
Storage Temperature, T_{stg}	$-65°C$ to $150°C$
Storage Voltage, V_{DD}	18V
Power Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Operating Supply Voltage	3	15	V
DC Input or Output Voltage	0	V_{DD}	V
Operating Temperature Range			
MM58539	-40	85	°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	T = −40°C to 70°C			Units
			Min	Typ	Max	
V_{IH}	High Level Input Voltage (except LCD0)	All V_{DD} (Note 2)	$0.75V_{DD}$			V
		V_{DD} = 5V	3.75			V
		V_{DD} = 15V	11.25			V
V_{IL}	Low Level Input Voltage (except LCD0)	All V_{DD} (Note 2)			$0.25V_{DD}$	V
		V_{DD} = 5V			1.25	V
		V_{DD} = 15V			3.75	V
V_{IH}	High Level Input Voltage, LCD0	All V_{DD} (Note 2)	$0.9V_{DD}$			V
		V_{DD} = 5V	4.5			V
		V_{DD} = 15V	13.5			V
V_{IL}	Low Level Input Voltage, LCD0	All V_{DD} (Note 2)	$V_{DD}-15$		$0.1V_{DD}$	V
		V_{DD} = 5V	−10		0.5	V
		V_{DD} = 15V	0		1.5	V
V_{OH}	High Level Row Output Voltage	$I_{OUT} = 0\mu A$			V_{DD}	V
V_{OL}	Low Level Row Output Voltage	$I_{OUT} = 0\mu A$	V_{SS}			V
V_{OH}	Unselected Row Output Voltage	$I_{OUT} = 0\mu A$		$0.5V_{DD}$		V
V_{OH}	High Level Column Output Voltage	$I_{OUT} = 0\mu A$		$0.68V_{DD}$		V
V_{OL}	Low Level Column Output Voltage	$I_{OUT} = 0\mu A$		$0.32V_{DD}$		V
R_{OUT}	Row or Column Output Impedance	$I_{OUT} = \pm 10\mu A$, V_{DD} = 5.0V,			40	kΩ
V_{OFF}	Average DC offset Any Display Element	$I_{OUT} = 0\mu A$ (Note 2)			100	mV
V_{OL}	Low Level Interrupt Output Voltage	$I_{OUT} = 100\mu A$			0.1	V
I_{IN}	Input Current	$V_{IN} = V_{SS}$ or V_{DD}			5	μA
I_{DD}	Quiescent Supply Current	V_{DD} = 5.0V,			400	μA
R_{IN}	Input Resistance, LCD0 Inputs	V_{DD} = 5.0V	1.0		3.0	MΩ
C_{IN}	Input Capacitance			5	10	pF

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. All Voltages referenced to ground unless otherwise noted.

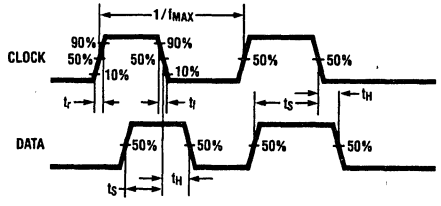
Note 2: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

AC Electrical Characteristics $V_{DD}=5.0V$, $C_L=50$ pF, and $T_A=25°C$, $t_r=t_f=20$ ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Clock Frequency		DC		1.5	MHz
t_S	Setup Time Data to Clock	(Falling Edge)	300			ns
t_H	Hold Time Clock to Data	(Falling Edge)	100			ns
t_{PHL}, t_{PLH}	Propagation Delay LCD0 to Interrupt				300	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time				200	ns
f_{OSC}	Oscillator Frequency	$R_{OSC}=1.2$ MΩ $C_{OSC}=470$ pF $V_{CC}=5.0V$ $V_{CC}=15.0V$		 2.9 3.6		 kHz kHz

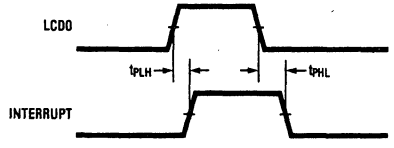
Switching Waveforms

Data Setup and Hold



TL/F/5728–5

Interrupt Propagation Delay



TL/F/5728–6

Functional Description

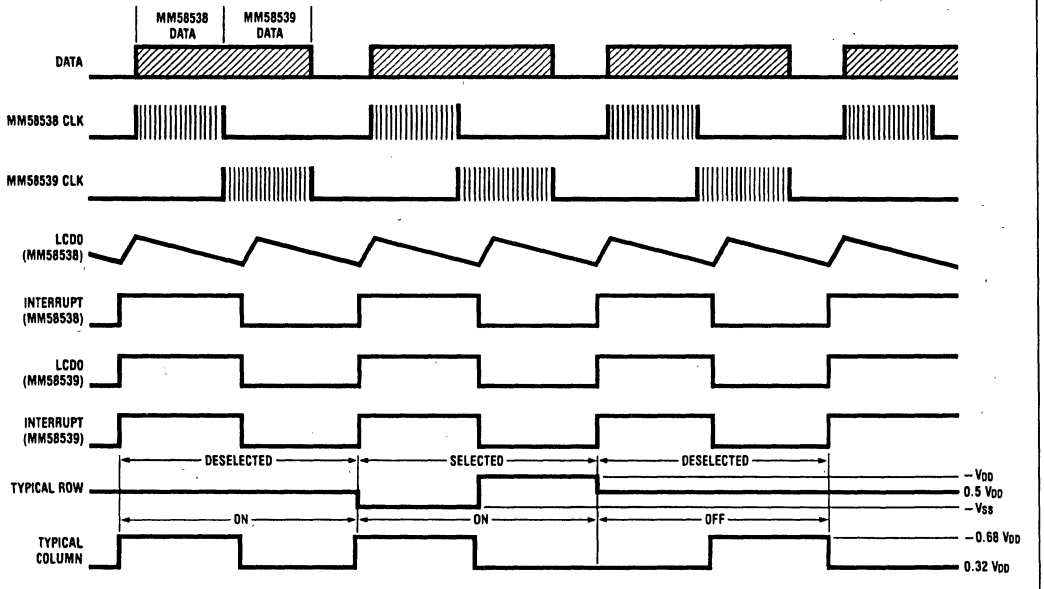
A block diagram of the MM58538 LCD driver is shown in *Figure 1*. Connection diagrams are shown in *Figure 2*.

MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock. A data logic '1' on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer from the shift register to the latches occurs and the row and column outputs change accordingly. This Interrupt signal also acts as a refresh request and new data must be loaded before the next Interrupt signal. The output locations correspond to a clockwise advancing shift register. Pin 40 is the last bit of data loaded and pin 7 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown for an MM58538 together with an MM58539 (slave column driver) in *Figure 3*. Rows generated from the MM58538 are out of phase with Interrupt if selected and at mid point voltage otherwise; levels are V_{DD}, V_{SS} and $V_{DD}/2$. Columns generated from both the MM58538 and the MM58539 are in phase with Interrupt if selected and out of phase if not selected; levels are $0.32V_{DD}$ and $0.68V_{DD}$. Backplanes, i.e., rows, should be addressed sequentially and individually. If the supply voltage has to be altered to optimise LCD contrast or for temperature compensation it is recommended that all positive supply terminals be connected together and the negative supply varied.



TL/F/5728–3

FIGURE 3. Typical Waveforms

Functional Description (Continued)

LCD0 INPUT

This input can be used in two modes:

1 Oscillating Mode

When this pin is connected with an external resistor and capacitor in parallel to V_{SS}, this input operates as an RC oscillator. This frequency is divided by two to provide a 50% duty cycle and will then appear at the Interrupt output as a frequency of approximately 1/RC, where R should exceed 1 MΩ.

The Interrupt output frequency should be greater than the minimum no-flicker frequency (approximately 30 Hz) multiplied by the number of backplanes used.

2 Driven Mode

In this mode, the Interrupt output will follow the waveform input on the LCD0 pin.

LCD0 of a driven mode device should preferably be connected to the Interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% ±1% duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes the mode detect logic. This signal sets all the row outputs to the Deselected state, all the Column outputs to the off state and the Interrupt output high. If the circuit is in the Oscillating mode, the LCD0 pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCD0 pin is held high by the low impedence Interrupt output of the previous device. When the first clock pulse goes to a logic '1', the level on the LCD0 pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating.

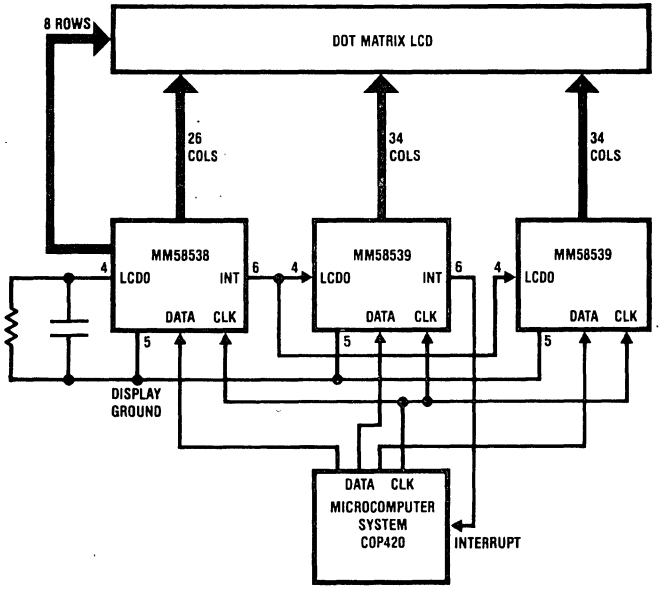
The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the Driven mode, the Interrupt frequency is in phase with the input frequency on LCD0.

CASCADING

Figure 4 shows an application where two or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The Interrupt output from the 'master' oscillating circuit is connected to the LCD0 input of the other 'slave' circuits, with the 'slave' Interrupt going to the microprocessor. It would also be possible to connect all LCD0 inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and separate data bus lines or vice versa.



TL/F/5728–4

FIGURE 4. Typical Application Diagram

National Semiconductor

PRELIMINARY

MM58539 Multiplexed LCD Driver

General Description

The MM58539 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P- and N-channel devices, which can drive up to 34 columns of a dot matrix LCD array directly under the control of an external processor. The MM58539 should be used with an MM58538 or MM58548 to drive a display that has up to 8 or 16 rows and an arbitrary number of columns. Data is input serially from the microprocessor which will service the drivers in response to an interrupt signal.

The circuit is available in a 40-pin molded dual-in-line package or dice.

Features

- Drives up to 34 columns
- Used with the MM58538 or MM58548 for expanding to larger displays
- Flexible organization allows any display pattern
- Simple 3 line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On chip oscillator
- Compatible with HLCD 0539

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

Block and Connection Diagrams

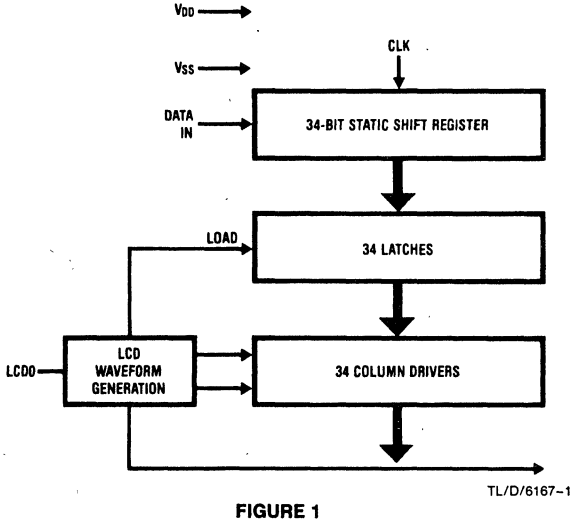
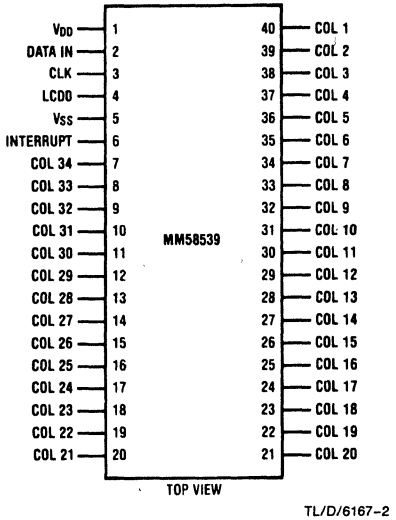


FIGURE 1

Dual-In-Line Package



TL/D/6167–2

FIGURE 2

Absolute Maximum Ratings (Note 1)

DC Input or Output Voltage	$-0.3V$ to $V_{DD}+0.3V$
Storage Temperature, T_{STG}	$-65°$ to $150°C$
Supply Voltage, V_{DD}	18V
Power Dissipation, P_D	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Operating Supply Voltage	3	15	V
DC Input or Output Voltage	0	V_{DD}	V
Operating Temperature Range			
MM58539	−40	85	°C

DC Electrical Characteristics

Symbol	Parameter	Conditions	$T_A = -40°C$ to $70°C$			Units
			Min	Typ	Max	
V_{IH}	High Level Input Voltage (except LCD0)	All V_{DD} (Note 2)	0.75 V_{DD}			V
		V_{DD} = 5V	3.75			V
		V_{DD} = 15V	11.25			V
V_{IL}	Low Level Input Voltage (except LCD0)	All V_{DD} (Note 2)			0.25 V_{DD}	V
		V_{DD} = 5V			1.25	V
		V_{DD} = 15V			3.75	V
V_{IH}	High Level Input Voltage, LCD0	All V_{DD} (Note 2)	0.9 V_{DD}			V
		V_{DD} = 5V	4.5			V
		V_{DD} = 15V	13.5			V
V_{IL}	Low Level Input Voltage, LCD0	All V_{DD} (Note 2)	V_{DD}-15		0.1 V_{DD}	V
		V_{DD} = 5V	−10		0.5	V
		V_{DD} = 15V	0		1.5	V
V_{OH}	High Level Column Output Voltage	$I_{OUT} = 0\ \mu A$		0.68 V_{DD}		V
V_{OL}	Low Level Column Output Voltage	$I_{OUT} = 0\ \mu A$		0.32 V_{DD}		V
R_{OUT}	Column Output Impedance	$I_{OUT} = \pm 10\ \mu A$, V_{DD}=5.0V			40	KΩ
V_{OFF}	Average DC Offset Any Display Element	$I_{OUT} = 0\ \mu A$ (Note 2)			100	mV
V_{OL}	Low Level Interrupt Output Voltage	$I_{OUT} = 100\ \mu A$			0.1	V
I_{IN}	Input Current	$V_{IN} = V_{SS}$ or V_{DD}			5	μA
I_{DD}	Quiescent Supply Current	V_{DD} = 5.0V			400	μA
R_{IN}	Input Resistance, LCD0 Inputs	V_{DD} = 5.0V	1.0		3.0	MΩ
C_{IN}	Input Capacitance			5	10	pF

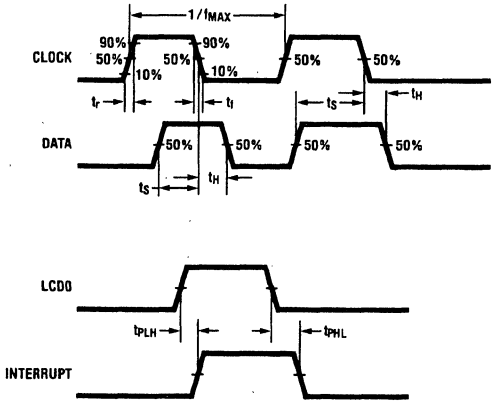
Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. All Voltages referenced to ground unless otherwise noted.

Note 2: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

AC Electrical Characteristics V_{DD} = 5.0V, C_L = 50 pF, T_A = 25°C, t_r, t_f = 20 ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Clock Frequency		DC		1.5	MHz
t_S	Setup Time Data to Clock	(Falling Edge)	300			ns
T_H	Hold Time Clock to Data	(Falling Edge)	100			ns
t_{PHL}, t_{PLH}	Progagation Delay LCD0 to Int. Out				300	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time				200	ns
f_{OSC}	Oscillator Frequency	R_{OSC} = 1.2 MΩ C_{OCS} = 470 pF V_{CC} = 5.0V V_{CC} = 15.0V		 2.9 3.6		 kHz kHz

Timing Waveforms



TL/D/6167–8

Functional Description

A block diagram of the MM58539 LCD driver is shown in *Figure 1*. Connection diagrams are shown in *Figure 2*.

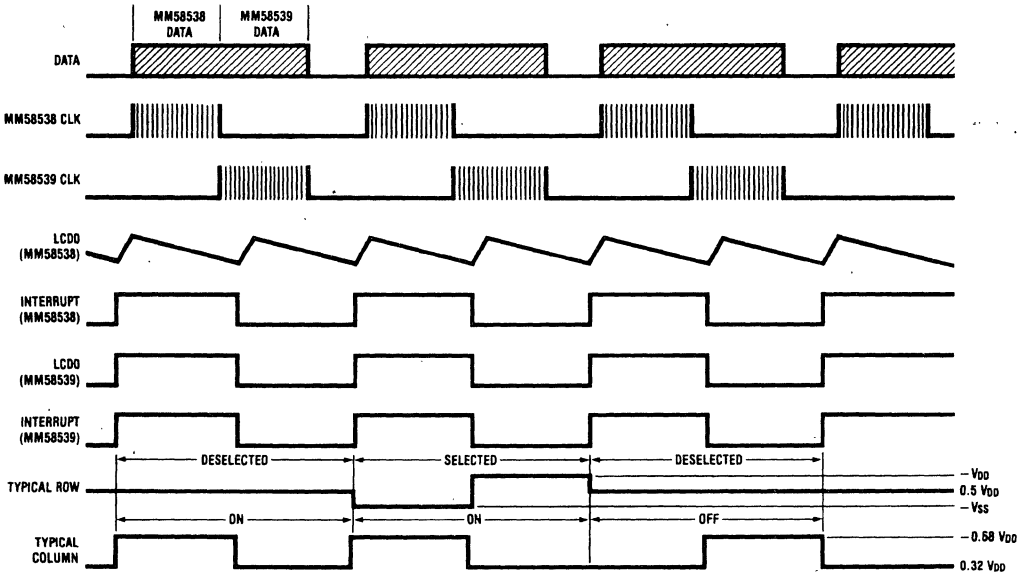
MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface when the MM58539 is used with the MM58538 to provide row and column information. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock. A data logic "1" on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer from the shift register to the latches occurs and the row and column outputs change accordingly. This Interrupt signal also acts as a refresh request and new data must be loaded before the next Interrupt signal. The output locations correspond to a clockwise advancing shift register. Pin 40 is the last bit of data loaded and pin 7 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown for an MM58539 together with an MM58538 in *Figure 3*.

Rows generated from the MM58538 are out of phase with Interrupt if selected and at midpoint voltage otherwise; levels are V_{DD}, V_{SS} and $V_{DD}/2$. Columns generated from both the MM58538 and the MM58539 are in phase with Interrupt if selected and out of phase if not selected; levels are $0.32V_{DD}$ and $0.68V_{DD}$. Backplanes, ie rows, should be addressed sequentially and individually. If the supply voltage has to be altered to optimise LCD contrast or for temperature compensation it is recommended that all positive supply terminals be connected together and the negative supply varied.



TL/D/6167–3

FIGURE 3. Waveforms

Functional Description (Continued)

LCD0 INPUT

This input can be used in two modes:

1 Oscillating Mode

When this pin is connected with an external resistor and capacitor in parallel to V_{SS}, this input operates as an RC oscillator. This frequency is divided by two to provide a 50% duty cycle and will then appear at the Interrupt output as a frequency of approximately 1/RC, where R should exceed 1 MΩ.

The Interrupt output frequency should be the minimum no-flicker frequency (greater than approximately 30Hz) multiplied by the number of backplanes used.

2 Driven Mode

In this mode, the Interrupt output will follow the waveform input on the LCD0 pin.

LCD0 of a driven mode device should preferably be connected to the Interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% ±1% duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes the mode detect logic. This signal sets all the Row outputs to the Deselected state, all the Column outputs to the Off state and the Interrupt output high. If the circuit is in the Oscillating mode, the LCD0 pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCD0 pin is held high by the low impedance Interrupt output of the previous device. When the first clock pulse goes to a logic "1", the level on the LCD0 pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating.

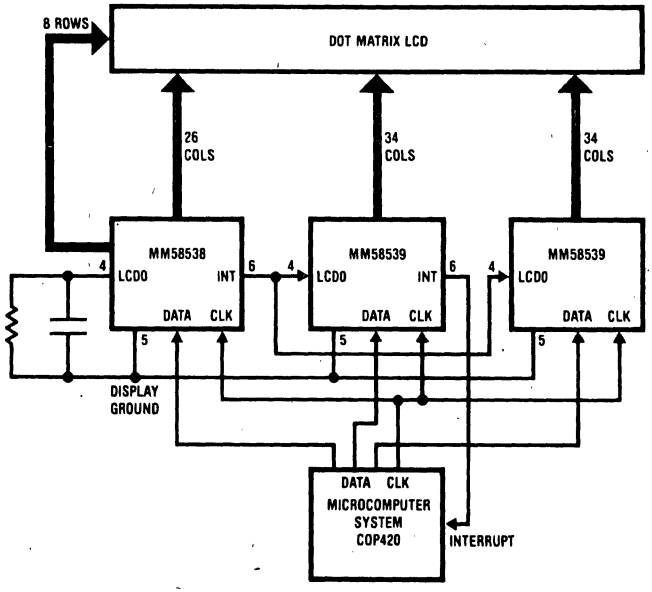
The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the Driven mode, the Interrupt frequency is in phase with the input frequency on LCD0.

CASCADING

Figure 4 shows an application where two or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The Interrupt output from the "master" oscillating circuit is connected to the LCD0 input of the other "slave" circuits, with the "slave" Interrupt going to the microprocessor. It would also be possible to connect all LCD0 inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and separate data bus lines or vice versa.



TL/D/6167–4

FIGURE 4. Typical Application Diagram

National Semiconductor

MM58540 Multiplexed LCD Driver

General Description

The MM58540 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P and N-channel devices. It can be externally programmed to drive either 32 rows or 32 columns under control of the ROW/COL pin. A high level selects all rows and a low level all columns. Two MM58540s with opposite selections can therefore be used to drive a 32 × 32 display. Data can be input serially from the microprocessor provided that CLKEN is high. This is done in response to an interrupt signal.

The circuit is available in either 40-pin molded dual-in-line packages or dice.

Features

- Drives either 32 rows or 32 columns
- Cascadable for larger displays
- Flexible organization allows any display pattern
- Simple 4-line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On-chip oscillator
- Compatible with HLCD 0540

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

Block and Connection Diagrams

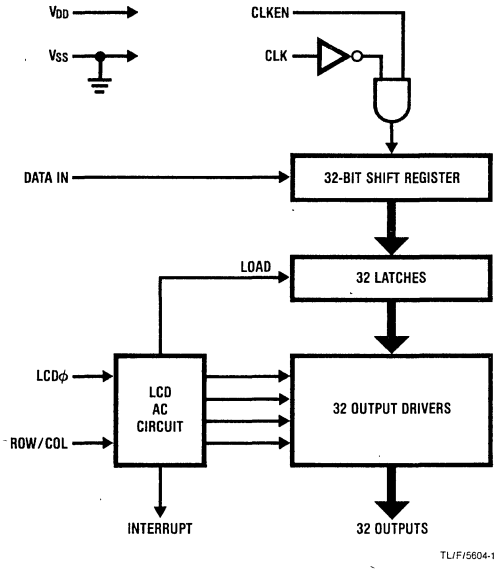


FIGURE 1

Dual-In-Line Package

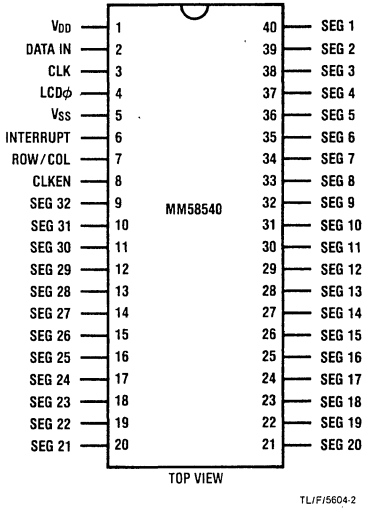


FIGURE 2

Order Number MM58540N
See NS Package N40A

Absolute Maximum Ratings (Note 1)

DC Input or Output Voltage	$-0.3V$ to $V_{DD}+0.3V$
Storage Temperature, T_{STG}	$-65°C$ to $150°C$
Supply Voltage, V_{DD}	18V
Power Dissipation, P_D	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Operating Supply Voltage	3	15	V
DC Input or Output Voltage	0	V_{DD}	V
Operating Temperature Range	−40	85	°C

DC Electrical Characteristics $T = -40°C$ to $70°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage (except LCD0)	All V_{DD} (Note 2)	0.75 V_{DD}			V
		$V_{DD}=5V$	3.75			V
		$V_{DD}=15V$	11.25			V
V_{IL}	Low Level Input Voltage (except LCD0)	All V_{DD} (Note 2)			0.25 V_{DD}	V
		$V_{DD}=5V$			1.25	V
		$V_{DD}=15V$			3.75	V
V_{IH}	High Level Input Voltage, LCD0	All V_{DD} (Note 2)	0.9 V_{DD}			V
		$V_{DD}=5V$	4.5			V
		$V_{DD}=15V$	13.5			V
V_{IL}	Low Level Input Voltage, LCD0	All V_{DD} (Note 2)	$V_{DD}-15$		0.1 V_{DD}	V
		$V_{DD}=5V$	−10		0.5	V
		$V_{DD}=15V$	0		1.5	V
V_{OH}	High Level Row Output Voltage	$I_{OUT}=0\ \mu A$			V_{DD}	V
V_{OL}	Low Level Row Output Voltage	$I_{OUT}=0\ \mu A$	V_{SS}			V
V_{OH}	Unselected Row Output Voltage	$I_{OUT}=0\ \mu A$		0.5 V_{DD}		V
V_{OH}	High Level Column Output Voltage	$I_{OUT}=0\ \mu A$		0.68 V_{DD}		V
V_{OL}	Low Level Column Output Voltage	$I_{OUT}=0\ \mu A$		0.32 V_{DD}		V
R_{OUT}	Row or Column Output Impedance	$I_{OUT}=\pm 10\ \mu A$, $V_{DD}=5.0V$			40	kΩ
V_{OFF}	Average DC Offset Any Display Element	$I_{OUT}=0\ \mu A$			100	mV
V_{OL}	Low Level Interrupt Output Voltage	$I_{OUT}=100\ \mu A$			0.1	V
I_{IN}	Input Current	$V_{IN}=V_{SS}$ or V_{DD}			5	μA
I_{DD}	Quiescent Supply Current	$V_{DD}=5.0V$			400	μA
R_{IN}	Input Resistance, LCD0 Inputs	$V_{DD}=5.0V$	1.0		3.0	MΩ
C_{IN}	Input Capacitance			5	10	pF

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. All voltages referenced to ground unless otherwise noted.

Note 2: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

AC Electrical Characteristics $V_{DD} = 5.0V$, $C_L = 50$ pF, $T_A = 25°C$, $t_r = t_f = 20$ ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Clock Frequency		DC		1.5	MHz
t_S	Set-Up Time Data to Clock	(Falling Edge)	300			ns
t_H	Hold Time Clock to Data	(Falling Edge)	100			ns
t_{PHL}, t_{PLH}	Propagation Delay LCD0 to Interrupt Out				300	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time				200	ns
f_{OSC}	Oscillator Frequency	$R_{OSC} = 1.2$ MΩ $C_{OSC} = 470$ pF $V_{CC} = 5.0V$ $V_{CC} = 15.0V$		 2.9 3.6		 kHz kHz

Functional Description

A block diagram of the MM58540 LCD driver is shown in *Figure 1*. A connection diagram is shown in *Figure 2*.

MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock provided that CLKEN is high. A data logic '1' on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer from the shift register to the latches occurs and the row and column outputs change accordingly. This interrupt signal also acts as a refresh request and new data must be loaded before the next interrupt signal. The output locations correspond to a clockwise advancing shift register. Pin 40 is the last bit of data loaded and pin 9 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown for two separate devices in *Figure 3*. Rows are out of phase with interrupt if selected and at midpoint voltage otherwise; levels are V_{DD}, V_{SS} and $V_{DD}/2$. Columns are in phase with interrupt if selected and out of phase if not selected; levels are $0.32\,V_{DD}$ and $0.68\,V_{DD}$. Backplanes, i.e., rows, should be addressed sequentially and individually. If the supply voltage has to be altered to optimize LCD contrast or for temperature compensation, it is recommended that all positive supply terminals be connected together and the negative supply varied.

LCDϕ INPUT

This input can be used in two modes:

1) Oscillating Mode

When this pin is connected with an external resistor and capacitor in parallel to V_{SS}, this input operates as an RC oscillator. This frequency is divided by 2 to provide a 50% duty cycle and will then appear at the interrupt output as a frequency of approximately 1/RC, where R should exceed 1 MΩ.

The interrupt output frequency should be the minimum no-flicker frequency (approximately 30 Hz) multiplied by the number of backplanes used.

2) Driven Mode

In this mode, the interrupt output will follow the waveform input on the LCDϕ pin.

LCDϕ of a driven mode device should preferably be connected to the interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% ±1% duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes the mode detect logic. This signal sets all the row outputs to the deselected state, all the column outputs to the off state and the interrupt output high. If the circuit is in the oscillating mode, the LCDϕ pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCDϕ pin is held high by the low impedance interrupt output of the previous devices. When the first clock pulse goes to a logic '1', the level on the LCDϕ pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating. The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the driven mode, the interrupt frequency is in phase with the input frequency on LCDϕ.

CASCADING

Figure 4 shows an application where 2 or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The interrupt output from the 'master' oscillating circuit is connected to the LCDϕ input of the other 'slave' circuits, with the 'slave' interrupt going to the microprocessor. It would also be possible to connect all LCDϕ inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and data with separate clock-enable lines or by holding CLKEN high and having a common clock and separate data bus lines or vice-versa.

Functional Description (Continued)

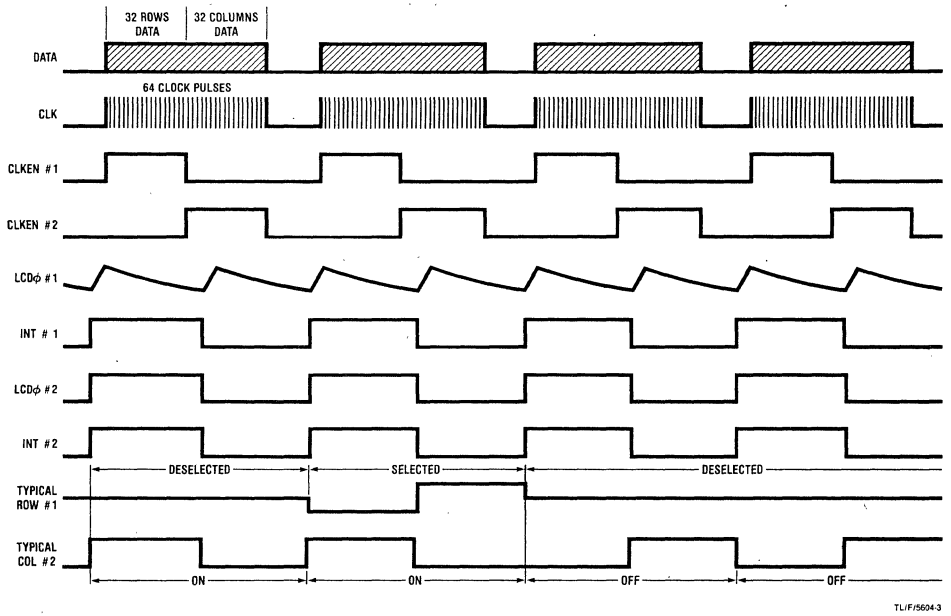


FIGURE 3

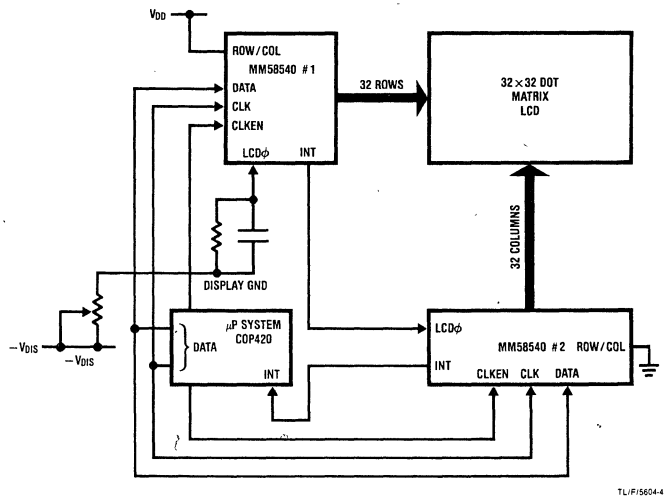
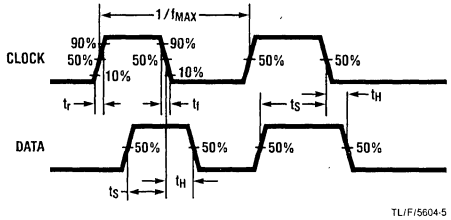


FIGURE 4

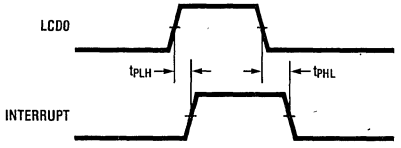
Switching Waveforms

Data Setup and Hold



TL/F/5604-5

Interrupt Propagation Delay



TL/F/5604-6

National Semiconductor

MM58548 Multiplexed LCD Driver

General Description

The MM58548 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P and N-channel devices. It drives a 16-row by 16-column dot matrix LCD array directly under control of an external microprocessor. The MM58548 can be used with an MM58539 to drive a display that has up to 16 rows and an arbitrary number of columns. Data is input serially from the microprocessor which will service the drivers in response to an interrupt signal.

The circuit is available in either 40-pin molded dual-in-line packages or dice.

Features

- Drives up to 16 rows and 16 columns
- Expandable to larger displays with MM58539
- Flexible organization allows any display pattern
- Simple 3-line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On-chip oscillator
- Compatible with HLCD 0548

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

Block and Connection Diagrams

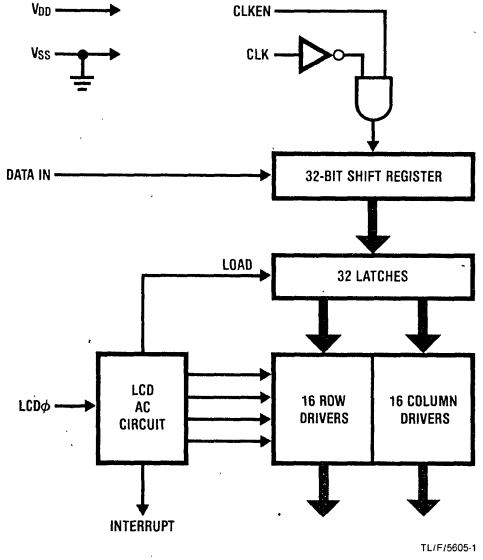


FIGURE 1

Dual-In-Line Package

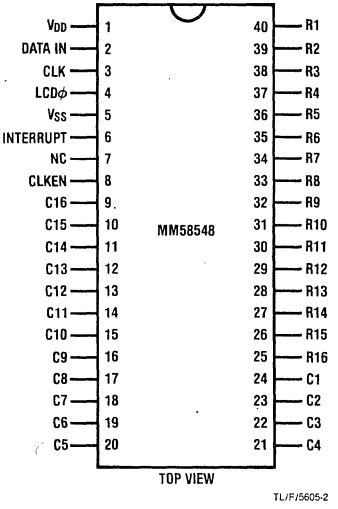


FIGURE 2

Order Number MM58548N
See NS Package N40A

Absolute Maximum Ratings (Note 1)

DC Input or Output Voltage	$-0.3V$ to $V_{DD}+0.3V$
Storage Temperature, T_{STG}	$-65°C$ to $150°C$
Supply Voltage, V_{DD}	18V
Power Dissipation, P_D	500 mW
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Operating Supply Voltage	3	15	V
DC Input or Output Voltage	0	V_{DD}	V
Operating Temperature Range	−40	85	°C

DC Electrical Characteristics $T = -40°C$ to $70°C$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	High Level Input Voltage (except LCD0)	All V_{DD} (Note 2)	0.75 V_{DD}			V
		$V_{DD}=5V$ $V_{DD}=15V$	3.75 11.25			V V
V_{IL}	Low Level Input Voltage (except LCD0)	All V_{DD} (Note 2)			0.25 V_{DD}	V
		$V_{DD}=5V$ $V_{DD}=15V$			1.25 3.75	V V
V_{IH}	High Level Input Voltage, LCD0	All V_{DD} (Note 2)	0.9 V_{DD}			V
		$V_{DD}=5V$ $V_{DD}=15V$	4.5 13.5			V V
V_{IL}	Low Level Input Voltage, LCD0	All V_{DD} (Note 2)	$V_{DD}-15$		0.1 V_{DD}	V
		$V_{DD}=5V$ $V_{DD}=15V$	−10 0		0.5 1.5	V V
V_{OH}	High Level Row Output Voltage	$I_{OUT}=0\ \mu A$			V_{DD}	V
V_{OL}	Low Level Row Output Voltage	$I_{OUT}=0\ \mu A$	V_{SS}			V
V_{OH}	Unselected Row Output Voltage	$I_{OUT}=0\ \mu A$		0.5 V_{DD}		V
V_{OH}	High Level Column Output Voltage	$I_{OUT}=0\ \mu A$		0.68 V_{DD}		V
V_{OL}	Low Level Column Output Voltage	$I_{OUT}=0\ \mu A$		0.32 V_{DD}		V
R_{OUT}	Row or Column Output Impedance	$I_{OUT}=\pm 10\ \mu A$ $V_{DD}=5.0V$			40	kΩ
V_{OFF}	Average DC Offset Any Display Element	$I_{OUT}=0\ \mu A$			100	mV
V_{OL}	Low Level Interrupt Output Voltage	$I_{OUT}=100\ \mu A$			0.1	V
I_{IN}	Input Current	$V_{IN}=V_{SS}$ or V_{DD}			5	μA
I_{DD}	Quiescent Supply Current	$V_{DD}=5.0V$			400	μA
R_{IN}	Input Resistance, LCD0 Inputs	$V_{DD}=5.0V$	1.0		3.0	MΩ
C_{IN}	Input Capacitance			5	10	pF

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur. All voltages referenced to ground unless otherwise noted.

Note 2: Guaranteed (but not 100% production tested) over the operating temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

AC Electrical Characteristics $V_{DD}=5.0V$, $C_L=50$ pF, $T_A=25°C$, $t_r=t_f=20$ ns

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{MAX}	Clock Frequency		DC		1.5	MHz
t_S	Set-Up Time Data to Clock	(Falling Edge)	300			ns
t_H	Hold Time Clock to Data	(Falling Edge)	100			ns
t_{PHL}, t_{PLH}	Propagation Delay LCD0 to Interrupt Out				300	ns
t_r, t_f	Maximum Clock Input Rise and Fall Time				200	ns
f_{OSC}	Oscillator Frequency	$R_{OSC}=1.2$ MΩ $C_{OSC}=470$ pF $V_{CC}=5.0V$ $V_{CC}=15.0V$		 2.9 3.6		 kHz kHz

Functional Description

A block diagram of the MM58548 LCD driver is shown in *Figure 1*. A connection diagram is shown in *Figure 2*.

MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock. A data logic '1' on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer of data from the shift register to the latches occurs and the row and column outputs change accordingly. This interrupt signal also acts as a refresh request and new data must be loaded before the next interrupt signal. The output locations correspond to a clockwise advancing shift register. Pin 40 is the last bit of data loaded and pin 9 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown in *Figure 3*. Rows are out of phase with interrupt if selected and at midpoint voltage otherwise; levels are V_{DD}, V_{SS} and $V_{DD}/2$. Columns are in phase with interrupt if selected and out of phase if not selected; levels are 0.32 V_{DD} and 0.68 V_{DD}. Backplanes, i.e., rows, should be addressd sequentially and individually. If the supply voltage has to be altered to optimize LCD contrast or for temperature compensation, it is recommended that all positive supply terminals be connected together and the negative supply varied.

LCDϕ INPUT

This input can be used in two modes:

1) Oscillating Mode

When this pin is connected with an external resistor and capacitor in parallel to V_{SS}, this input operates as an RC oscillator. This frequency is divided by two to provide a 50% duty cycle and will then appear at the interrupt output as a frequency of approximately 1/RC, where R should exceed 1MΩ.

The interrupt output frequency should be the minimum no-flicker frequency (approximately 30 Hz) multiplied by the number of backplanes used.

2) Driven Mode

In this mode, the interrupt output will follow the waveform input on the LCDϕ pin.

LCDϕ of a driven mode device should preferably be connected to the interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% ±1% duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes the mode detect logic. This signal sets all the row outputs to the deselected state, all the column outputs to the off state and the interrupt output high. If the circuit is in the oscillating mode, the LCDϕ pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCDϕ pin is held high by the low impedance interrupt output of the previous device. When the first clock pulse goes to a logic '1', the level on the LCDϕ pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating. The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the driven mode, the interrupt frequency is in phase with the input frequency on LCDϕ.

CASCADING

Figure 4 shows an application where 2 or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The interrupt output from the 'master' oscillating circuit is connected to the LCDϕ input of the other 'slave' circuits, with the 'slave' interrupt going to the microprocessor. It would also be possible to connect all LCDϕ inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and data with separate clock-enable lines or by holding CLKEN high and having a common clock and separate data bus lines or vice-versa.

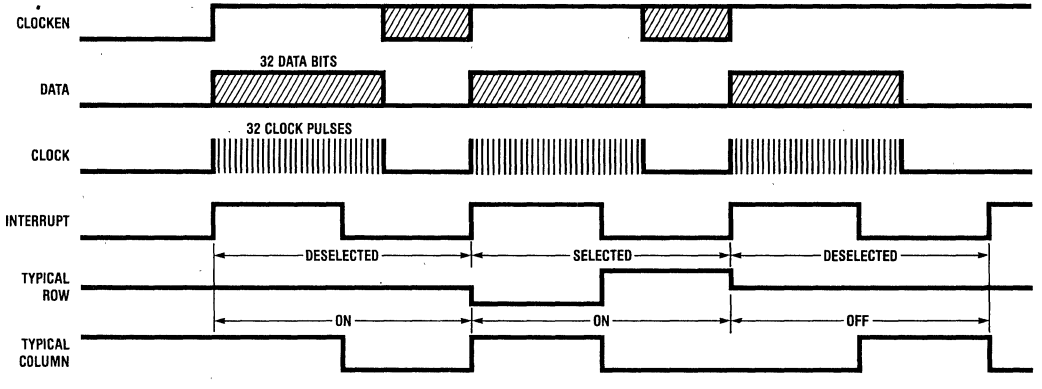


FIGURE 3

TL/F/5605-3

Functional Description (Continued)

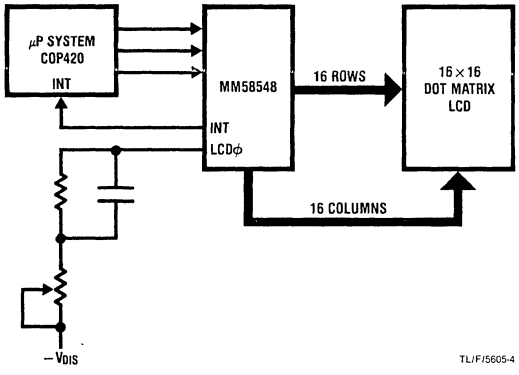
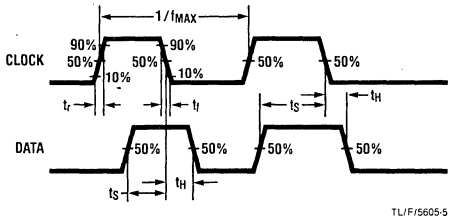


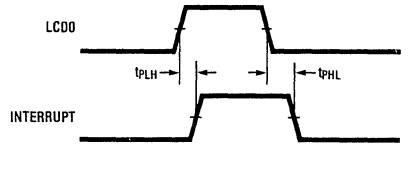
FIGURE 4

Switching Waveforms

Data Setup and Hold



Interrupt Propagation Delay



Section 8
Appendices/
Physical Dimensions

8

Section Contents

INTRODUCTION TO THE RELIABILITY MILITARY/AEROSPACE PROGRAMS

History

In the mid 1960's the various government agencies responsible for semiconductor reliability saw that screenable defects were resulting in an in-equipment failure rate of about 1% per thousand hours. In-depth failure analysis allowed them to determine what the predominate failure mechanisms were. The Solid State Applications Branch of the Air Force's Rome Air Development Center (RADC) was assigned the task of developing a screening procedure which would remove the infant mortality failures which had led to the high failure rate previously encountered. Working closely with other semiconductor reliability experts, the RADC staff developed MIL-STD-883, which was first issued in 1968. The objective of MIL-STD-883 was to create an economically feasible, standardized integrated circuit screening flow which would achieve an in-equipment failure rate of 0.08% per thousand hours for Class B and 0.004% per thousand hours for Class A (which was later superseded by Class S). Over the years this standard has grown and matured with a number of new test methods added as reliability information and failure analysis results became more detailed. These developments have led to one of the strongest and most comprehensive screening specs available, MIL-STD-883.

Purpose and Structure

MIL-STD-883 states: this standard establishes uniform methods and procedures for testing microelectronic devices, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations, and physical and electrical tests. What does this mean to the semiconductor user? To understand this, one must subdivide MIL-STD-883 into two primary areas: 1) Detailed how-to specifications (methods 1001 through 4007) and 2) Screening and qualification and/or quality conformance testing requirements (methods 5001 through 5009). By examining each of these areas the thrust of MIL-STD-883 will become apparent.

Detailed How-to Specifications

MIL-STD-883 is a collection of environmental, mechanical, visual, and electrical test methods. These methods define tests which enable manufacturers and users to screen for specific reliability concerns. The tests covered include moisture resistance, high temperature storage, neutron irradiation, shock and acceleration tests, visual radiography, and dimensional tests, to mention only a few. In the electrical test section, there are tests to examine load conditions, power supplies, short circuit currents, and other tests. Each of these tests is designed to look at specific reliability and quality concerns that affect semiconductor products.

Screening Flows

The overall reliability requirements for a system depend upon a number of factors, including cost-effectiveness. For example, a deep space probe, where component replacement is impossible once the system is launched, requires very high reliability, despite the inherent cost of complex screening. On the other hand, a ground-based radio unit can use a less stringent reliability testing sequence, since a failed component can be easily replaced at moderate cost. In line with this range of needs, MIL-STD-883 established three distinct product assurance levels to provide reliability commensurate with the product's intended application. The three levels are Class S (intended for critical applications, such as space), Class B (intended for less critical applications, such as airborne or ground systems), and Class C (intended for easily replaceable systems, which has since been eliminated).

National and MIL-M-38510

A major thrust exists among integrated circuit users, suppliers, and the U.S. Government to avoid proliferation of military procurement specifications by turning instead to standardized high reliability microcircuits. National Semiconductor endorses and supports this trend.

One major program to which National is heavily committed is the JAN MIL-M-38510 IC program. This is a standardization program administered by the U.S. Defense Department which allows a user to purchase a broad line of standard products from a variety of qualified suppliers.

There is only one MIL-M-38510 program. National is committed to supplying only QPL devices, and discourages any "pseudo-38150" alternates.

There are two levels specified within MIL-M-38510 — Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems.

MIL-M-38510

The Defense Electronic Supply Center (DESC) administers the integrated circuit standardization program known as MIL-M-38510 (sometimes referred to as the JAN IC Program). The specification set used to define the program consists of four documents: general specification MIL-M-38510, which is an overall definition of the processing and testing to be performed; detail specifications (referred to as "slash sheets"), each of which defines the performance parameters for a unique generic device or a family of devices; MIL-STD-883, which defines specific screening procedures; and MIL-STD-976, which defines line certification requirements.

When a user orders a MIL-M-38510 device, he is guaranteed that he will get a device fully conformant with the detail specification and which has also met all of the general testing and processing requirements. DESC requires semiconductor suppliers to become formally qualified under the MIL-M-38510 program and to be listed on the current Qualification Products List (QPL) before they are allowed to legally ship JAN devices.

Advantages to the User

The JAN 38510 program has numerous advantages for the integrated circuit user.

- A single explicit specification eliminates guesswork concerning device electrical characteristics or processing flow.
- The rigorous schedule of quality conformance testing that is a mandatory part of the MIL-M-38510 program assures the user of long-term stability.
- Since the electrical characteristics of the devices are at least as tight as the "standard industry data sheet" parameters, device performance will meet the vast majority of system design requirements. Additionally, min./max. limits replace many data sheet typicals, making circuit design and worst case design analysis decisions easier.
- The user is spared the expense of researching and preparing his own procurement document.
- The user is spared the expense of qualification testing. The QPL tells him which suppliers have qualified the device he requires.
- The QPL gives the user a choice of qualified suppliers for devices that are fully interchangeable. In addition, the presence of several sources guarantees competitive pricing that is typically lower than for devices to a user's own specifications.
- Since MIL-M-38510 is a standard program, procurement lead times will be shorter. With a large number of programs using JAN devices, distributors and manufacturers are able to establish inventories of JAN devices. National in particular is committed to maintaining finished goods and work-in-process inventories to support our customers' needs.
- Spare parts will be readily available without excessive minimum order requirements.
- Standard parts with volume requirements will remain in production longer.
- Device markings are consistent from one manufacturer to another.
- The program is extremely cost-effective. A user can purchase a few devices for engineering evaluation and prototyping and know that they will be identical to the devices he will get during production. When the cost factors associated with spec. writing, supplier qualification, maintaining voluminous parts control documentation, and the more intangible benefits of device availability are totaled, use of JAN ICs is overwhelmingly the most cost-effective approach.

Advantages to the Supplier

What motivates a supplier like National Semiconductor to be so heavily committed to the MIL-M-38510 program? National has the *broadest* range of reliability processed products available in the semiconductor industry. A program such as MIL-M-38510 helps to standardize the processing required and to minimize the number of individual user specifications. This allows National to concentrate more resources on this program, thereby improving product quality and availability.

The Most Frequently Asked Questions and Answers about MIL-M-38510

There are many questions which are frequently asked regarding the MIL-M-38510 program. We would like to answer some of them.

Q. WHAT MUST A MANUFACTURER DO TO GET HIS PARTS LISTED ON THE QPL?

A. There are two things which a manufacturer is required to do. First, he must get his facilities (including wafer fab, assembly, and rel processing areas) certified by DESC. This requires that each fab area used for QPL devices must be approved. Second, for each specific device and package combination listed on the QPL, the manufacturer must perform extensive qualification testing and provide detailed device information to DESC. This data is typically supplied in two phases.

In the first phase, the manufacturer must supply detailed information concerning the device construction and electrical characteristics. Once this data has been verified by DESC to confirm that the manufacturer's device meets the MIL-M-38510 requirements, the manufacturer is listed on Part II of the QPL. At this point the manufacturer is legally able to supply full JAN qualified devices meeting ALL of the MIL-M-38510 requirements. The manufacturer must then perform the full qualification testing of Method 5005 of MIL-STD-883 as specified in paragraph 4.4 of MIL-M-38510. Once this data has been reviewed and accepted by DESC, the manufacturer is listed on Part I of the QPL.

Q. IS THERE ANY DIFFERENCE IN DEVICES PRODUCED WHILE A MANUFACTURER IS LISTED ON PART II OF THE QPL AND THOSE PRODUCED AFTER PART I QUALIFICATION IS COMPLETED?

A. There is absolutely *no difference*. A supplier must meet all of the device screening and quality conformance requirements no matter what his QPL status.

Q. HOW DOES A USER KNOW WHAT DEVICES ARE COVERED BY SLASH SHEET SPECIFICATIONS?

A. Supplement 1 to MIL-M-38510 contains a listing of the slash sheet specifications and a cross reference to the generic part type. This is updated as new slash sheets are released. National's Reliability Handbook also contains a cross reference.

Q. HOW CAN A USER OBTAIN COPIES OF THE QPL, SUPPLEMENT 1 OF MIL-M-38510, MIL-M-38510 ITSELF, AND MIL-STD-883?

A. Copies of these and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

Q. WHAT ABOUT THOSE DEVICES FOR WHICH NO DETAIL SPECIFICATION EXISTS?

A. The ultimate aim of a standardization program must be to furnish *all* parts. Requests for addition of a part to MIL-M-38510 should be made to DESC Directorate of Engineering, Dayton, Ohio 45444, indicating a need for slash sheets and/or suppliers to be qualified for the additional devices. National has a form (available through local sales offices) which may be used for this purpose. In addition, if only some parts are available, a user can still see significant savings on those that are available.

Q. HOW IS A JAN QPL DEVICE MARKED?

A. Tables I and II explain the details of the marking for JAN ICs.

TABLE I. MIL-M-38510 Part Marking

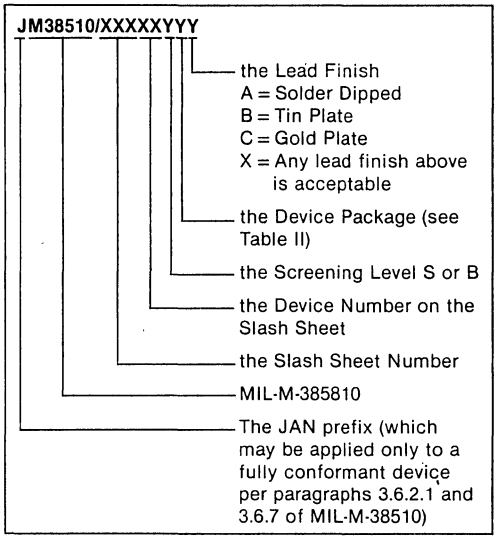


TABLE II. JAN Package Codes

38510 PACKAGE DESIGNATION	MICROCIRCUIT INDUSTRY DESCRIPTION
A	14-pin 1/4″ × 1/4″ (metal) flatpack
B	14-pin 3/16″ × 1/4″ flatpack
C	14-pin 1/4″ × 3/4″ dual-in-line
D	14-pin 1/4″ × 3/8″ (ceramic) flatpack
E	16-pin 1/4″ × 7/8″ dual-in-line
F	16-pin 1/4″ × 3/8″ (metal or ceramic) flatpack
G	8-pin TO-99 can or header
H	10-pin 1/4″ × 1/4″ (metal) flatpack
I	10-pin TO-100 can or header
J	24-pin 1/2″ × 1-1/4″ dual-in-line
K	24-pin 3/8″ × 5/8″ flatpack
M	12-pin TO-101 can or header
P	8-pin 1/4″ × 3/8″ dual-in-line
Q	40-pin 8/16″ × 2-1/16″ dual-in-line
R	26-pin 1/4″ × 1-1/16″ dual-in-line
S	20-pin 1/4″ × 1/2″ flatpack
V	18-pin 3/8″ × 1-15/16″ dual-in-line
W	22-pin 3/8″ × 1-1/8″ dual-in-line
X, Y, Z	Unassigned — Reserved for identifying special packages whose dimensions are carried in the detail specifications.

Q. ARE DEVICES CALLED "M38510, JAN PROCESSED, JAN EQUIVALENT, ETC." REALLY QPL PRODUCTS?

A. *Absolutely not.* There is only one QPL product — it is a JM38510 marked device. "JAN Equivalent" is expressly forbidden by para-

graphs 3.1 and 3.6.7 of MIL-M-38510. MIL-M-38510 does provide for the production of devices when no qualified sources exist, but this may be done only with prior DESC approval, and products produced under this provision must meet all requirements of MIL-M-38510 other than qualification.

Q. HOW LONG CAN A SUPPLIER REMAIN ON PART II OF THE QPL?

A. For Class B, a manufacturer can remain on Part II for two years or until 90 days after another supplier becomes qualified for the same device package, screening level, and lead finish combination on Part I of the QPL. Class S devices may remain on Part II for one year after another manufacturer reaches Part I.

Q. WHEN ANOTHER SUPPLIER OBTAINS PART I QUALIFICATION, ARE THE OTHER QUALIFIED SUPPLIERS REMOVED FROM PART II IMMEDIATELY?

A. No. The supplier is given 90 days before being removed from Part II for a Class B device and one year for a Class S device. During that time a supplier may legally accept orders for those devices. After the end of the 90-day or one year period, he may no longer accept orders but may complete and ship those orders received prior to that time, no matter how long it takes him to complete them.

Q. IS A SUPPLIER EVER REMOVED FROM PART I QUALIFICATION?

A. Generally not. As long as a supplier continues to manufacture the device, maintains appropriate facility approvals, and submits all required reports and information to DESC within stipulated time limits, he will retain QPL I listing. Violation of these requirements can be cause for removal from QPL.

Q. CAN AN AUTHORIZED DISTRIBUTOR SHIP JAN DEVICES FROM HIS SHELVES IF THE MANUFACTURER HAS LOST HIS QPL LISTING FOR THOSE DEVICES?

A. Yes. As long as those devices were ordered by the authorized distributor while the manufacturer had QPL listing for those devices, the distributor may subsequently ship those devices from his shelves.

Q. CAN A MANUFACTURER LEGALLY SHIP JAN QPL MATERIAL HE ASSEMBLED AND TESTED BEFORE HE RECEIVED A QPL LISTING?

A. Yes. The manufacturer must assemble and screen parts to prove his ability to comply with the specifications before he can be placed on QPL. As a result, his first lot of material, which is fully conformant to QPL product requirements, will have a date code that is earlier than the date he is placed on the QPL. However, the manufacturer may *not* begin to assemble and test unless he has a line certification and an approval to proceed with qualification.

Q. WHAT IS THE RELATIONSHIP BETWEEN MIL-M-38510 AND MIL-STD-883?

A. MIL-M-38510 defines complete program requirements and the detail device electrical performance parameters. The device processing requirements are specified in MIL-STD-883.

Q. SUPPOSE DEVICES ARE KEPT ON A MANUFACTURER'S OR DISTRIBUTOR'S SHELVES FOR A PERIOD OF TIME; MUST THEY EVER BE RETESTED TO VALIDATE THAT THEY STILL MEET SLASH SHEET CHARACTERISTICS?

A. Yes. Devices held by a manufacturer or by his authorized distributor which have a date code older than 36 months must be retested by the manufacturer in accordance with Group A sampling requirements prior to shipment to a customer or return to inventory.

Q. WHY SHOULD A USER SPECIFY "X" IN THE LEAD FINISH DESIGNATION FOR A PART TYPE?

A. A manufacturer who receives an order for a specific lead finish for which he is qualified but has no inventory at the time of order may not be able to fill the order in a timely manner, even though he might have substantial inventory of another lead finish. Unless a user has a specific reason for wanting a particular lead finish, he should allow his suppliers the flexibility of shipping whatever finish is available.

Q. WHAT DATA IS A MANUFACTURER REQUIRED TO SHIP WITH A JAN PART?

A. A certificate of conformance is all that is required. However, he must retain all data for three years.

Q. CAN A DEVICE FOR WHICH THERE IS NO SLASH SHEET BE PROCESSED TO MIL-M-38510?

A. Since MIL-M-38510 invokes a combination of the processing requirements of MIL-STD-883 and the detail device performance parameters contained in each individual slash sheet, the answer is obviously no. However, National's 883B/RETS™ program does provide parts which meet all of the screening requirements of the MIL-STD-883 specification and which have been subjected to all of the MIL-M-38510 controls (except for domestic assembly).

TABLE III. Sample MIL-M-38510 Listing

GOVERNMENT DESIGNATION				TEST REPORT NUMBER	MANUFACTURER'S NAME
DEVICE TYPE*	DEVICE CLASS	CASE OUTLINE	LEAD MATERIAL AND FINISH		
M38510/008					
01	S only	A	C	38510-953-81	National Semiconductor Corp.
01	B	C	A	38510-953-81	National Semiconductor Corp.
02		D	B	38510-30-7T	
03	B	C	A	38510-520-83	National Semiconductor Corp.
			B		

*"M38510" is the military designator for MIL-M-38510. The QPL shows this notation even though the parts are fully qualified devices and are marked JM38510/XXXXXYYY.

Q. WHAT DOES A QPL LISTING LOOK LIKE AND HOW DO YOU READ IT?

A. Sample QPL listings are shown in Table III.

JM38510/00801SAC
JM38510/00801BCA
JM38510/00801BCB
JM38510/00801BDA
JM38510/00801BDB
JM38510/00802BCA
JM38510/00802BCB
JM38510/00802BDA
JM38510/00802BDB
JM38510/00803BCA
JM38510/00803BCB

Q. WHAT QUALITY CONFORMANCE TESTS ARE CONDUCTED? ARE ALL DEVICES IN A GENERIC FAMILY EVENTUALLY SUBJECTED TO QUALITY CONFORMANCE TESTING?

A. For B level devices quality conformance tests must be conducted as follows:

Group A—Each inspection lot or sublot.

Group B—Each inspection lot for each package type and lead finish on each detail specification.

Group C—Periodically at 3-month intervals on one device type or one inspection lot from each mircocircuit group in which a manufacturer has qualified device types (die related tests).

Group D—Periodically at a 6-month interval for each package type for which a manufacturer holds qualifications (package related tests).

Different devices within a generic family are chosen for successive quality conformance tests until all of the devices have been subjected to testing. The sequence is then repeated. The manufacturer must submit attributes data to DESC for all quality conformance tests performed.

Q. HOW IS AN INSPECTION LOT DEFINED?

A. For Class B devices, each inspection lot shall consist of microcircuits of a single device type, in a single package type and lead finish, or may consist of inspection sublots of several different device types, in a single package type and lead finish, defined by a single detail specification. Each inspection lot shall be manufactured on the same production line(s) through final seal by the same production techniques, and to the same device design rules and case with the same material requirements, and sealed within the same period not exceeding 6 weeks.

Q. WHAT IS NATIONAL SEMICONDUCTOR'S COMMITMENT TO MIL-M-38510?

A. National Semiconductor is convinced that the level of standardization offered by a program like MIL-M-38510 is the key to long-term military component procurement viability. We have a corporate commitment to MIL-M-38510. We believe that the program will be of significant benefit in lessening the problem of product obsolescence, for the volume provided will help to keep many key devices in production. We believe that the program will make possible the procurement of devices in small quantities with reasonable lead times for long-term spares or field maintenance requirements.

National Semiconductor will continue to maintain a broad base of line certifications and an extensive list of Class B and Class S device qualifications. We will continue to work with the Department of Defense, concerned users, and other semiconductor manufacturers to update and redefine the applicable specifications. We feel that this level of support is essential if MIL-M-38510 is to remain the strongest standardization program available.

In addition, we will continue to add capacity and to build up substantial inventories of a large spectrum of products to ensure the

availability and the lead times that are needed for key military programs.

National Mil/Aero Standardization Programs

Your customer has imposed upon you requirements for product reliability that you must meet on every single component you buy. In most cases, these requirements mandate that you buy JAN MIL-M-38510 parts where they are available, and that all other devices must be as close to JAN as is achievable. We don't consider this unreasonable. In fact, we believe that this is the only reasonable and intelligent approach.

To meet this objective, we designed our 883B/RETS program around requirements that were already imposed for the MIL-M-38510 program.* We realize that there are many so-called standardization programs available in the marketplace which lack the compliance that you need. Our 883B/RETS program is totally compliant. We invite you to make this comparison between what we offer and what you need. Our screening flow, our 5% PDA, our quality conformance test frequency, and the other items that you consider important, match exactly the requirements defined in MIL-M-38510.** If they did not, we could not offer ***Total Standardization***.

Standardization provides the manufacturing efficiencies needed by the semiconductor manufacturers if they are to meet military semiconductor needs. To the user, standardization offers the highest guarantee of quality and reliability through production consistency and uniformity. The most significant benefit of standardization to the Department of Defense, however, is that it ensures the availability of component level spares to key programs with the pricing, delivery, and reliability needed for the field support and maintenance of our key defense electronics systems.

National's MIL-M-38510 Emphasis

To implement this view of standardization, we have based our entire approach to military screening upon the Class S and Class B requirements of MIL-M-38510. We are convinced that to do less than this would be to provide an inferior product, one that does not meet the true needs of the Department of Defense. Our 883B/RETS microcircuits are processed through the most comprehensive and compliant Class B screening program offered by any semiconductor manufacturer. We have tried to emulate MIL-M-38510 to the fullest extent possible, with the same production controls, calibration schedules, rework and resubmission procedures, operator certification requirements, and all of the other key elements of MIL-M-38510. The procedures that we employ in the production of MIL-M-38510 devices are used for all of the military devices we manufacture.

Our 883S/RETS microcircuits are processed through a screening flow that matches the MIL-M-38510 Class S flow exactly. Our commitment to MIL-M-38510 Class S is such that once qualified for a given device type we will sell that part only as a JAN Class S part. Class S QPL listing will result in the immediate removal from production of the 883S/RETS version of the device.

National's Commitment

But compliance flows are obviously meaningless unless the capacity is in place to support them. We have the industry's largest screening capacity. Over the past few years we have reinvested substantial sums in additional capital equipment in both buildings and the equipment with which to fill those buildings. Our Tucson, Arizona plant was the first plant in the entire industry to be totally dedicated to the production of military integrated circuits. We will continue to add capacity for military assembly and test, even during those periods when others turn away from the military marketplace in pursuit of what they view to be the more attractive commercial market. We feel that a commitment to the needs of the military/aerospace user community should not be based upon the conditions encountered in the commercial marketplace. We have no plans for other than a continued long-term commitment to military/aerospace component production and screening. And we will not deviate from the highest standards of quality and reliability in our execution of that commitment. There are no shortcuts to semiconductor reliability. It can only be achieved through rigid adherence to established standards.

However, we also acknowledge the quite obvious fact that through refinement and redefinition, standards are subject to change. As those changes occur, we will update our current procedures to reflect the changes that find their way into MIL-M-38510 and MIL-STD-883. We will, where our understanding of semiconductor reliability and screening indicates the need, actively pursue those changes that we feel will allow our industry to provide a better product to the systems manufacturers. We will also steadfastly resist those changes which we feel sacrifice reliability to the less important question of expediency.

*Requirements that were subsequently incorporated into MIL-STD-883

**and MIL-STD-883.

National's Standard Programs

MIL-M-38510 is the key military standardization program for ICs. National is equally committed to the support of the requirements of the space segment of the market for MIL-M-38510 Class S devices. To support these needs we have established dedicated Class S assembly and test facilities. The realization that users could not obtain all the device types they required through these programs led National's Military/Aerospace Products Group to the development of two of the strongest and most compliant in-house programs in the industry. National programs for 883B/RETS and 883S/RETS microcircuits provide the systems manufacturer with an easy mechanism for obtaining those devices not listed on the MIL-M-38510 QPL. In response to other user needs, National also developed a program for radiation hardened devices (both CMOS and linear), a comprehensive program for radiation susceptibility testing for Class S devices, and a program for the production of devices in leadless chip carriers (LCCs).

RETS and Burn-In

One of the primary advantages of MIL-M-38510 is its clear definition and standardization of electrical test and burn-in requirements. One of the major drawbacks seen in the standard reliability screening programs of most semiconductor manufacturers is that electrical testing is invariably performed to some document that is not available to the user. The user has the right to know what he is buying. At National that testing is never vague or undefined. Both in-house programs (883B/RETS and 883S/RETS) are based upon a document called the RETS (an acronym for Reliability Electrical Test Specification. The RETS is a simplified but complete description of the testing performed as part of National's standard Rel electrical test programs, and is controlled by our QA department. The burn-in circuits and electrical test parameters for the MIL-M-38510 Class S and Class B devices produced by National Semiconductor are defined by the applicable detail specification.

Ordering ICs from National

Ordering National Semiconductor High Reliability integrated circuits is very simple. National sales offices and sales representatives can provide price and delivery information on our entire line of JM38510 Class B, JM38510 Class S, 883B/RETS and 883S/RETS microcircuits. A large percentage of these devices are available from inventory at either the factory or at one of our many distributors.

Ordering to Control Specifications

We also acknowledge the fact that many military systems manufacturers must, for contractual purposes, maintain their own specifications for many of the devices that they purchase. We have no objection to the use of contractor prepared procurement specifications, for we have found that the majority of these documents are written in compliance with the requirements of MIL-M-38510. Where this is true, we have found that they are also totally compatible with our in-house standardization programs. Where drawings submitted to National differ from the requirements outlined in MIL-M-38510, we welcome the opportunity to work with our customers to develop specifications which do meet the intent of MIL-M-38510.

Where customer specifications and our 883B/RETS product specifications correspond, we have the ability to expedite delivery by adding the customer part number in addition to the basic 883B/RETS part number. Customers who understand our program and wish to use the program in their parts procurement may order by placing "M/O" after their part number on their purchase order, thus allowing us to mark their part number on our 883B/RETS devices without the lengthy delay normally required for a comprehensive specifications review cycle. We have tried to provide programs that offer the maximum level of flexibility within the constraints of standardization.

Standardization is the key to cost-effective procurement of high reliability semiconductor devices. National Semiconductor Corporation is committed to that standardization.

Military Processing: A Corporate Commitment

The National Semiconductor Military/Aerospace Products Division draws upon the total resources of National Semiconductor. National is one of the world's largest manufacturers of semiconductor products, offering the largest number of product types available from any single source in the industry. This product line is growing faster than that of any other worldwide semiconductor manufacturer. Each new product is carefully evaluated for possible military/aerospace usage potential, and new product designs must comply with the reliability and quality constraints required by that segment of the industry. All new product designs are targeted to full military temperature range operation.

In addition, a dedicated Reliability Engineering Department within the Military/Aerospace Prod-

ucts Division coordinates burn-in circuit design, test tape development, test fixturing, support documentation, and new product release paperwork to ensure the earliest possible introduction of fully compliant 883B/RETS versions of the new products introduced by the company.

We are able to do this well, for National is no newcomer to this business. Founded in Danbury, Connecticut in 1959, National acquired an entire new management team in 1967 and moved corporate headquarters to Santa Clara, California. The new management team focused its attention on the transistor product line, and rapidly made that line profitable. Then the company's talents were turned to the development of linear, digital, and MOS integrated circuits — the fastest-growing segments of the semiconductor marketplace. Finally, an OEM representative and distributor network was established to develop and service a broad customer base, and facilities were added around the world to provide competitive products to worldwide markets.

The Reliability Test Department was initially formed in 1968 and reported at that time to the Director of Quality Assurance. The Rel Department developed the same rapid growth rate that the company as a whole had shown. From a small staff occupying several thousand square feet in Santa Clara, these reliability test operations grew until today they employ over 3000 people worldwide. Well over 200,000 square feet are devoted to the testing and assembly of high reliability products. During 1981, the Military/Aerospace Products Group became the Military/Aerospace Products Division. The company is currently involved in a number of military research and development programs, including a Phase I VHSIC contract.

VHSIC involvement was natural since National's technological leadership has enabled the company to consistently be one of the major suppliers of military/aerospace semiconductors. Having continued to develop a high technology image through the development olf Megarad hardened CMOS and linear device types, and the development of TRI-CODE™ logic, National is now expanding technology frontiers in the areas of memory, microprocessor, and data acquisition products. As a result of all this innovation, National has become the only company in the entire semiconductor industry capable of providing high reliability devices from all of the following product lines:

- linear
- hybrid
- CMOS logic
- Megarad CMOS logic
- bipolar memory
- MOS RAMs
- CMOS RAMs
- MOS EPROMs
- CMOS EPROMs
- MOS EEPROMs
- data acquisition devices
- standard TTL
- low power TTL
- low power Schottky
- standard Schottky
- interface devices
- bipolar microprocessors
- MOS microprocessors
- CMOS microprocessors
- COPS™ microcontrollers
- high-speed CMOS Schottky
- advanced low power Schottky
- advanced Schottky

National Semiconductor has wafer fabrication plants in Santa Clara, California; Salt Lake City, Utah; Arlington, Texas; and Danbury, Connecticut. Many of these fabrication plants, along with our assembly and test lines in Santa Clara, California and Tucson, Arizona, have been fully certified for the production of Class S and Class B MIL-M-38510 circuits.

To support the requirements of the Class S marketplace, we have our own SEM and radiation testing facilities. Our screening capabilities are backed up by one of the most extensive failure analysis labs in the industry.

National is the leader in the military/aerospace integrated circuit market. We have achieved that leadership by offering an unmatched combination of technology, product breadth, understanding, commitment and capacity.

883B/883S/RETS Screening Flows

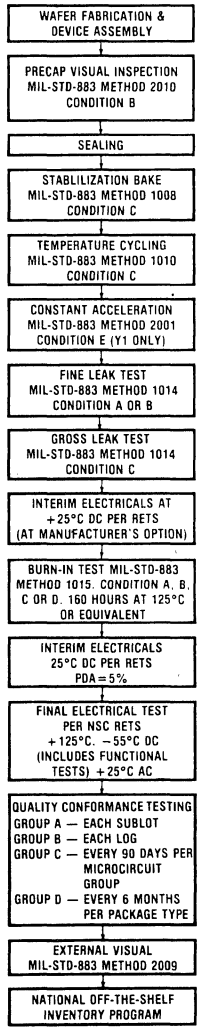
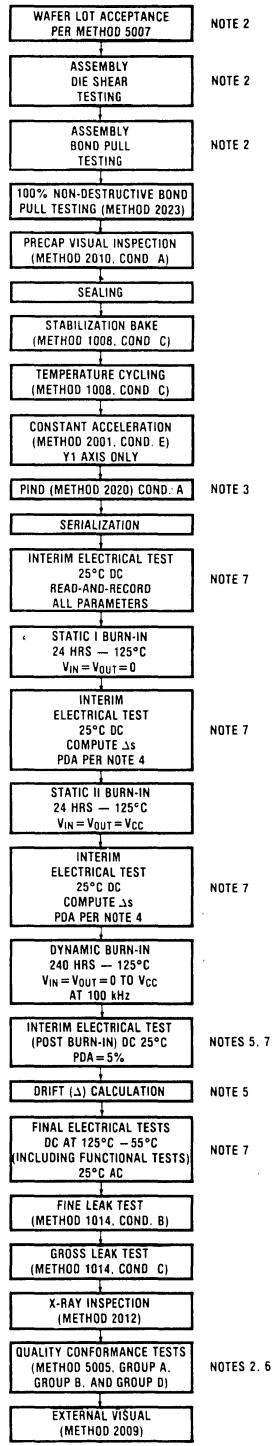


FIGURE 1. National's 883B/RETS Class B Screening Flow



NOTES:
1. ALL METHODS REFERENCED ARE MIL-STD-883 TEST METHODS.
2. THESE TESTS ARE PERFORMED ON A SAMPLE BASIS. ALL OTHER TESTS ARE PERFORMED 100%.
3. ACCEPTANCE CRITERIA SHALL BE IN ACCORDANCE WITH MIL-M-38510.
4. THE PDA FOR STATIC I AND STATIC II BURN-IN SHALL BE 5% TOTAL.
5. THE PDA INCLUDES Δ FAILURES.
6. GROUP A AND BOND PULL AND DIE SHEAR TESTING OF GROUP B MAY BE PERFORMED ON-LINE.
7. ALL ELECTRICAL TESTING SHALL BE IN ACCORDANCE WITH THE APPLICABLE RETS OR THE APPLICABLE MIL-S-38510 DETAIL SPECIFICATION.

FIGURE 2. National's 883S/RETS Class S Screening Flow

CD40XX, 54CXX Product Availability

The following list of products represents what is currently available for 883B. As new products are brought on board, notification will take place through news releases. For further data on the products and families, please contact your local sales office.

PACKAGE CROSS REFERENCE

NSC ORDER NUMBER	RCA EQUIVALENT DESIGNATION	MOTOROLA EQUIVALENT DESIGNATION	PACKAGE
CD40XXMJ/883B	CD40XXAF	MC140XXAL	Cavity DIP (J)

For B series, NSC order number is CD40XXBMX/883B.

INDUSTRY ID	NSC ID	INDUSTRY ID	NSC ID
CD4001BMJ/883	MM4601BJ/883	CD4512BMJ/883	MM14512BMJ/883
CD4002BMJ/883	MM4602BJ/883	CD4514BMJ/883	MM14514BMJ/883
CD4006BMJ/883	MM4606BJ/883	CD4515BMJ/883	MM14515BMJ/883
CD4007MJ/883	MM4607AJ/883	CD4516BMJ/883	MM14516BMJ/883
CD4008BMJ/883	MM4608BJ/883	CD4518BMJ/883	MM14518BMJ/883
CD4009MJ/883	MM4609AJ/883	CD4519BMJ/883	MM14519BMJ/883
CD40106BMJ/883	MM54C14J/883	CD4520BMJ/883	MM14520BMJ/883
CD4011BMJ/883	MM4611BJ/883	CD4522BMJ/883	MM14522BMJ/883
CD4012BMJ/883	MM4612BJ/883	CD4526BMJ/883	MM14526BMJ/883
CD4014BMJ/883	MM4614BJ/883	CD4528BMJ/883	MM14528BMJ/883
CD4015BMJ/883	MM4615BJ/883	CD4529BMJ/883	MM14529BMJ/883
CD4016BMJ/883	MM4616BJ/883	CD4538BMJ/883	MM14538BMJ/883
CD40160BMJ/883	MM54C160J/883	CD4541BMJ/883	MM14541BMJ/883
CD40161BMJ/883	MM54C161J/883	CD4543BMJ/883	MM14543BMJ/883
CD40162BMJ/883	MM54C162J/883	CD4723BMJ/883	MM14723BMJ/883
CD40163BMJ/883	MM54C163J/883	CD4724BMJ/883	MM14724BMJ/883
CD40174BMJ/883	MM54C174J/883		
CD40175BMJ/883	MM54C175J/883	MM54C00J/883	MM54C00J/883
CD40192BMJ/883	MM54C192J/883	MM54C02J/883	MM54C02J/883
CD40193BMJ/883	MM54C193J/883	MM54C04J/883	MM54C04J/883
CD4020BMJ/883	MM4620BJ/883	MM54C08J/883	MM54C08J/883
CD4021BMJ/883	MM4621BJ/883	MM54C10J/883	MM54C10J/883
CD4023BMJ/883	MM4623BJ/883	MM54C107J/883	MM54C107J/883
CD4025BMJ/883	MM4625BJ/883	MM54C14J/883	MM54C14J/883
CD4030MJ/883	MM4630AJ/883	MM54C150J/883	MM54C150J/883
CD4034BMJ/883	MM4634BJ/883	MM54C151J/883	MM54C151J/883
CD4035BMJ/883	MM4635BJ/883	MM54C154J/883	MM54C154J/883
CD4040BMJ/883	MM4640BJ/883	MM54C157J/883	MM54C157J/883
CD4041MJ/883	MM4641AJ/883	MM54C160J/883	MM54C160J/883
CD4043BMJ/883	MM4643BJ/883	MM54C161J/883	MM54C161J/883
CD4044MJ/883	MM4644AJ/883	MM54C162J/883	MM54C162J/883
CD4046BMJ/883	MM4646BJ/883	MM54C163J/883	MM54C163J/883
CD4049UBMJ/883	MM4649UBJ/883	MM54C164J/883	MM54C164J/883
CD4060BMJ/883	MM4660BJ/883	MM54C165J/883	MM54C165J/883
CD4066BMJ/883	MM4666BJ/883	MM54C173J/883	MM54C173J/883
CD4069MJ/883	MM54C04J/883	MM54C174J/883	MM54C174J/883
CD4070BMJ/883	MM54C86J/883	MM54C175J/883	MM54C175J/883
CD4071BMJ/883	MM4671BJ/883	MM54C192J/883	MM54C192J/883
CD4072BMJ/883	MM4672BJ/883	MM54C193J/883	MM54C193J/883
CD4073BMJ/883	MM4673BJ/883	MM54C195J/883	MM54C195J/883
CD4075BMJ/883	MM4675BJ/883	MM54C20J/883	MM54C20J/883
CD4076BMJ/883	MM54C173J/883	MM54C200J/883	MM54C200J/883
CD4081BMJ/883	MM4681BJ/883	MM54C221J/883	MM54C221J/883
CD4089BMJ/883	MM4689BJ/883	MM54C240J/883	MM54C240J/883
CD4093BMJ/883	MM4693BJ/883	MM54C244J/883	MM54C244J/883
CD4099BMJ/883	MM4699BJ/883	MM54C30J/883	MM54C30J/883
CD4503BMJ/883	MM14503BMJ/883	MM54C32J/883	MM54C32J/883
CD4510BMJ/883	MM14510BMJ/883	MM54C373J/883	MM54C373J/883
CD4511BMJ/883	MM14511BMJ/883	MM54C374J/883	MM54C374J/883

INDUSTRY ID	NSC ID
MM54C42J/883	MM54C42J/883
MM54C48J/883	MM54C48J/883
MM54C73J/883	MM54C73J/883
MM54C74J/883	MM54C74J/883
MM54C76J/883	MM54C76J/883
MM54C83J/883	MM54C83J/883
MM54C85J/883	MM54C85J/883
MM54C86J/883	MM54C86J/883
MM54C89J/883	MM54C89J/883
MM54C90J/883	MM54C90J/883
MM54C901J/883	MM54C901J/883
MM54C902J/883	MM54C902J/883
MM54C903J/883	MM54C903J/883
MM54C904J/883	MM54C904J/883

INDUSTRY ID	NSC ID
MM54C905J/883	MM54C905J/883
MM54C906J/883	MM54C906J/883
MM54C907J/883	MM54C907J/883
MM54C909J/883	MM54C909J/883
MM54C910J/883	MM54C910J/883
MM54C914J/883	MM54C914J/883
MM54C915J/883	MM54C915J/883
MM54C922J/883	MM54C922J/883
MM54C923J/883	MM54C923J/883
MM54C93J/883	MM54C93J/883
MM54C941J/883	MM54C941J/883
MM54C95J/883	MM54C95J/883
MM54C989J/883	MM54C989J/883

54HC/54HCT Product Availability

The following list of products represents what is currently available for 883B. As new products are brought on board, notification will take place through news releases. For further data on the products and families, please contact your local sales office.

PACKAGE CROSS REFERENCE

NSC ORDER NUMBER	MOTOROLA EQUIVALENT DESIGNATION	PACKAGE
54HC/HCTXXJ/883B	54HC/HCTXXBCAJC	Cavity DIP (J-14)
54HC/HCTXXJ/883B	54HC/HCTXXBEAJC	Cavity DIP (J-16)
54HC/HCTXXJ/883B	54HC/HCTXXBRAJC	Cavity DIP (J-20)
54HC/HCTXXJ/883B	54HC/HCTXXBJAJC	Cavity DIP (J-24)

INDUSTRY ID	NSC ID
MM54HCU04J/883	MM54HCU04J/883
MM54HC00J/883	MM54HC00J/883
MM54HC02J/883	MM54HC02J/883
MM54HC03J/883	MM54HC03J/883
MM54HC04J/883	MM54HC04J/883
MM54HC08J/883	MM54HC08J/883
MM54HC10J/883	MM54HC10J/883
MM54HC107J/883	MM54HC107J/883
MM54HC109J/883	MM54HC109J/883
MM54HC11J/883	MM54HC11J/883
MM54HC112J/883	MM54HC112J/883
MM54HC113J/883	MM54HC113J/883
MM54HC123AJ/883	MM54HC123AJ/883
MM54HC125J/883	MM54HC125J/883
MM54HC132J/883	MM54HC132J/883
MM54HC133J/883	MM54HC133J/883
MM54HC137J/883	MM54HC137J/883
MM54HC138J/883	MM54HC138J/883
MM54HC139J/883	MM54HC139J/883
MM54HC14J/883	MM54HC14J/883
MM54HC147J/883	MM54HC147J/883
MM54HC149J/883	MM54HC149J/883
MM54HC151J/883	MM54HC151J/883
MM54HC153J/883	MM54HC153J/883
MM54HC154J/883	MM54HC154J/883
MM54HC155J/883	MM54HC155J/883
MM54HC157J/883	MM54HC157J/883
MM54HC158J/883	MM54HC158J/883
MM54HC160J/883	MM54HC160J/883
MM54HC161J/883	MM54HC161J/883
MM54HC162J/883	MM54HC162J/883
MM54HC163J/883	MM54HC163J/883
MM54HC164J/883	MM54HC164J/883
MM54HC165J/883	MM54HC165J/883
MM54HC173J/883	MM54HC173J/883
MM54HC174J/883	MM54HC174J/883
MM54HC175J/883	MM54HC175J/883
MM54HC181J/883	MM54HC181J/883
MM54HC182J/883	MM54HC182J/883
MM54HC190J/883	MM54HC190J/883
MM54HC191J/883	MM54HC191J/883
MM54HC192J/883	MM54HC192J/883
MM54HC193J/883	MM54HC193J/883
MM54HC194J/883	MM54HC194J/883
MM54HC195J/883	MM54HC195J/883
MM54HC20J/883	MM54HC20J/883

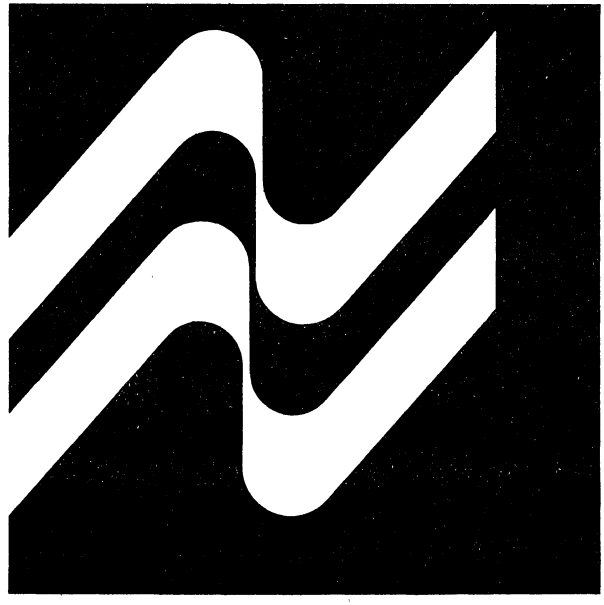
INDUSTRY ID	NSC ID
MM54HC221AJ/883	MM54HC221AJ/883
MM54HC237J/883	MM54HC237J/883
MM54HC240J/883	MM54HC240J/883
MM54HC241J/883	MM54HC241J/883
MM54HC242J/883	MM54HC242J/883
MM54HC243J/883	MM54HC243J/883
MM54HC244J/883	MM54HC244J/883
MM54HC245J/883	MM54HC245J/883
MM54HC251J/883	MM54HC251J/883
MM54HC253J/883	MM54HC253J/883
MM54HC257J/883	MM54HC257J/883
MM54HC259J/883	MM54HC259J/883
MM54HC266J/883	MM54HC266J/883
MM54HC27J/883	MM54HC27J/883
MM54HC273J/883	MM54HC273J/883
MM54HC280J/883	MM54HC280J/883
MM54HC283J/883	MM54HC283J/883
MM54HC298J/883	MM54HC298J/883
MM54HC299J/883	MM54HC299J/883
MM54HC30J/883	MM54HC30J/883
MM54HC32J/883	MM54HC32J/883
MM54HC354J/883	MM54HC354J/883
MM54HC356J/883	MM54HC356J/883
MM54HC365J/883	MM54HC365J/883
MM54HC366J/883	MM54HC366J/883
MM54HC367J/883	MM54HC367J/883
MM54HC368J/883	MM54HC368J/883
MM54HC373J/883	MM54HC373J/883
MM54HC374J/883	MM54HC374J/883
MM54HC390J/883	MM54HC390J/883
MM54HC393J/883	MM54HC393J/883
MM54HC4002J/883	MM54HC4002J/883
MM54HC4016J/883	MM54HC4016J/883
MM54HC4017J/883	MM54HC4017J/883
MM54HC4020J/883	MM54HC4020J/883
MM54HC4024J/883	MM54HC4024J/883
MM54HC4040J/883	MM54HC4040J/883
MM54HC4046J/883	MM54HC4046J/883
MM54HC4049J/883	MM54HC4049J/883
MM54HC4050J/883	MM54HC4050J/883
MM54HC4051J/883	MM54HC4051J/883
MM54HC4052J/883	MM54HC4052J/883
MM54HC4053J/883	MM54HC4053J/883
MM54HC4060J/883	MM54HC4060J/883
MM54HC4066J/883	MM54HC4066J/883
MM54HC4075J/883	MM54HC4075J/883

INDUSTRY ID	NSC ID
MM54HC4078J/883	MM54HC4078J/883
MM54HC42J/883	MM54HC42J/883
MM54HC423AJ/883	MM54HC423AJ/883
MM54HC4316J/883	MM54HC4316J/883
MM54HC4511J/883	MM54HC4511J/883
MM54HC4514J/883	MM54HC4514J/883
MM54HC4538J/883	MM54HC4538J/883
MM54HC4543J/883	MM54HC4543J/883
MM54HC51J/883	MM54HC51J/883
MM54HC521J/883	MM54HC521J/883
MM54HC533J/883	MM54HC533J/883
MM54HC534J/883	MM54HC534J/883
MM54HC540J/883	MM54HC540J/883
MM54HC541J/883	MM54HC541J/883
MM54HC563J/883	MM54HC563J/883
MM54HC564J/883	MM54HC564J/883
MM54HC573J/883	MM54HC573J/883
MM54HC574J/883	MM54HC574J/883
MM54HC58J/883	MM54HC58J/883
MM54HC589J/883	MM54HC589J/883
MM54HC590J/883	MM54HC590J/883
MM54HC592J/883	MM54HC592J/883
MM54HC593J/883	MM54HC593J/883
MM54HC595J/883	MM54HC595J/883
MM54HC597J/883	MM54HC597J/883
MM54HC640J/883	MM54HC640J/883
MM54HC643J/883	MM54HC643J/883
MM54HC646J/883	MM54HC646J/883
MM54HC648J/883	MM54HC648J/883
MM54HC688J/883	MM54HC688J/883
MM54HC73J/883	MM54HC73J/883
MM54HC74J/883	MM54HC74J/883
MM54HC75J/883	MM54HC75J/883
MM54HC76J/883	MM54HC76J/883
MM54HC86J/883	MM54HC86J/883
MM54HCT00J/883	MM54HCT00J/883
MM54HCT04J/883	MM54HCT04J/883
MM54HCT05J/883	MM54HCT05J/883
MM54HCT08J/883	MM54HCT08J/883

INDUSTRY ID	NSC ID
MM54HCT109J/883	MM54HCT109J/882
MM54HCT112J/883	MM54HCT112J/883
MM54HCT138J/883	MM54HCT138J/883
MM54HCT139J/883	MM54HCT139J/883
MM54HCT149J/883	MM54HCT149J/883
MM54HCT155J/883	MM54HCT155J/883
MM54HCT157J/883	MM54HCT157J/883
MM54HCT158J/883	MM54HCT158J/883
MM54HCT164J/883	MM54HCT164J/883
MM54HCT191J/883	MM54HCT191J/883
MM54HCT193J/883	MM54HCT193J/883
MM54HCT240J/883	MM54HCT240J/883
MM54HCT241J/883	MM54HCT241J/883
MM54HCT244J/883	MM54HCT244J/883
MM54HCT245J/883	MM54HCT245J/883
MM54HCT257J/883	MM54HCT257J/883
MM54HCT273J/883	MM54HCT273J/883
MM54HCT299J/883	MM54HCT299J/883
MM54HCT34J/883	MM54HCT34J/883
MM54HCT373J/883	MM54HCT373J/883
MM54HCT374J/883	MM54HCT374J/883
MM54HCT521J/883	MM54HCT521J/883
MM54HCT533J/833	MM54HCT533J/883
MM54HCT534J/883	MM54HCT534J/883
MM54HCT540J/883	MM54HCT540J/883
MM54HCT541J/883	MM54HCT541J/883
MM54HCT563J/883	MM54HCT563J/883
MM54HCT564J/883	MM54HCT564J/883
MM54HCT573J/883	MM54HCT573J/883
MM54HCT574J/883	MM54HCT574J/883
MM54HCT590J/883	MM54HCT590J/883
MM54HCT592J/883	MM54HCT592J/883
MM54HCT593J/883	MM54HCT593J/883
MM54HCT640J/883	MM54HCT640J/883
MM54HCT643J/883	MM54HCT643J/883
MM54HCT688J/883	MM54HCT688J/883
MM54HCT74J/883	MM54HCT74J/883
MM54HCT76J/883	MM54HCT76J/883

Radiation Hardened Technologies

from National Semiconductor



RADIATION HARDENED TECHNOLOGIES FROM NATIONAL SEMICONDUCTOR

For many years, military, aerospace and satellite programs have depended on bipolar transistor and integrated circuit technology in the fabrication of airborne systems. Development of bipolar technology is an outgrowth, in part, of avionics and space applications needs. Despite their relatively high immunity or resistance to high levels of both constant and burst radiation in the form of gamma rays, x-rays, cosmic rays, and so on, bipolar devices have two drawbacks: a susceptibility to damage from neutron fluxes, and high power consumption, which adds to the power supply requirements and subtracts from the usable payload of spacecraft and missiles. In addition, recent decreases in bipolar feature sizes and changes in bipolar design and fabrication techniques have led to bipolar devices which exhibit the same level of susceptibility to ionizing radiation that had historically been seen in MOS devices. The spacecraft and missile industry has long needed a radiation hardened logic technology with low power consumption that would readily lend itself to reliable fabrication processes with reasonable repeatability. The purpose of this brochure is to provide some information to the potential user regarding National Semiconductor's solutions to radiation problems.

CMOS Radiation Hardened Products

Over the years, the development of sophisticated space, satellite and military systems and mission requirements fostered an active search for a radiation hardened logic circuit technology that consumes less power and offers a higher degree of circuit integration on a single silicon chip. Metal oxide semiconductor (MOS) devices, particularly complementary MOS (CMOS), provided just such an alternative. But standard CMOS devices, even those qualified to MIL-M-38510 (JAN) requirements, proved sensitive to relatively low levels of gamma (or total dose) radiation, as low in many cases as 3×10^3 rads (Si)[1]. Early generations of mass-producible specifically radiation hardened CMOS devices were able to withstand only 10^5 rads (Si), while many space, satellite and missile systems require circuitry resistance levels at least ten times higher, 10^6 rads (Si).

National Semiconductor developed a solution to this problem: a complete line of megarad hardened CMOS logic products utilizing a radiation hardening process that is compatible with volume processing. Products hardened to withstand 10 megarads [devices capable of tolerating total dose radiation of 10^7 rads (Si)] are the result of an intensive multi-year research and development program in cooperation with Sandia Laboratories (Albuquerque, NM). This program has enabled National Semiconductor to offer radiation hard versions of virtually our entire metal-gate CMOS product line.

Devices ranging in complexity from simple gates to large scale integration (LSI) random access memories have been hardened using the processes we developed. The achievement of this level of radiation resistance in a mass production CMOS process required that we implement major modifications to the basic commercial process, in the gate oxidation, substrate and P-tub surface concentrations, and metallization. We are currently in the process of research and development efforts aimed at extending these radiation improvements into complex metal gate devices (such as analog-to-digital converters and gate arrays), and into silicon gate processes. This will enable us to provide radiation hardened devices within our 54HC logic family, our microCMOS memories and microprocessors, and our microCMOS gate arrays.

Bipolar vs. CMOS

Bipolar devices and CMOS devices respond differently to different forms of radiation as a result of basic differences in both structure and operation. As Figure 1 shows, bipolar devices depend upon the diffusion of minority carriers for current flow through the base region. When bipolar devices are subject to neutron irradiation, the resulting crystal damage decreases minority carrier lifetime, causing severe performance degradation. On the other hand, bipolar devices are usually relatively insensitive to surface effects resulting from charge buildup in the oxide layer. Thus ionizing radiation has little effect on many bipolar structures. However, some

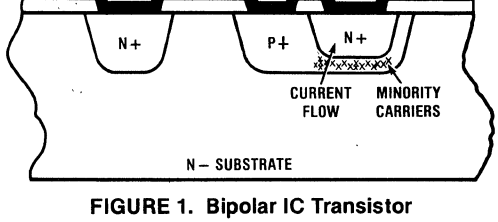


FIGURE 1. Bipolar IC Transistor

1. One rad (Si) is the quantity of any type of ionizing radiation which imparts 100 ergs of energy per gram of silicon.

recently developed bipolar technologies contain unhardened parasitic MOS structures as a result of the oxide isolations and walled emitter processes that they utilize.

CMOS devices (see Figure 2) are surface effect devices. The equivalent operating elements, gate, source and drain, are at the surface, and the flow of current occurs horizontally across the device, very close to the silicon/silicon-dioxide interface. Their characteristics are determined by electrostatic conditions at the silicon/silicon-dioxide interface. Carriers originate in the source region, and CMOS devices depend upon majority carriers for their operation. They are therefore not seriously affected by the minority carrier lifetime degradation resulting from neutron irradiation. They are, however, susceptible to charge in the oxide or at the oxide-substrate interface. Although gamma radiation will ionize both the oxide and the substrate, the resulting ionic charge cannot become trapped in the relatively conductive substrate as easily as it can be trapped in the insulating oxide. CMOS devices are therefore much more susceptible than bipolar devices to degradation from gamma radiation.

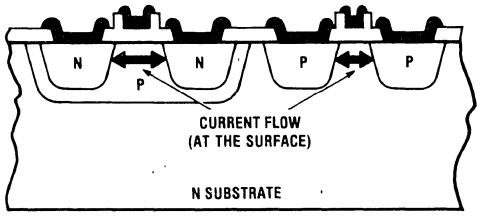


FIGURE 2. CMOS IC Transistor

CMOS IC Transistor Structures

Complementary MOS, or CMOS, combines two types of MOS devices, P-channel and N-channel structures, into a single functioning unit. The lower power dissipation and high stability resulting from this complementary combination is particularly attractive in the design of portable battery-powered electronic units, or for applications where a battery provides standby power.

MOS structures, both N- and P-types, perform in two modes; enhancement and depletion. In an N-channel enhancement mode MOS device, for example, the gate controls the current flow between the source and drain. In this device, when a positive voltage is applied to the gate with respect to the source, a field is set up across the gate dielectric, producing a negatively charged conductive path, a channel, between the source and the drain. This is known as an enhancement mode device because zero gate to source voltage turns off the device. In the alternative mode, depletion, current flows despite the gate voltage being zero, because sufficient charge is present at the silicon/silicon-dioxide interface to induce a conductive path between the device source and drain regions. The P-channel MOS transistor is similar to the N-channel alternative, except that negative voltage applied to the gate, with respect to source, induces a positively charged conductive path between source and drain to turn the device on.

Conventional CMOS logic circuits are produced with only enhancement mode N- and P-channel devices. The process is designed to give turn on (threshold) voltage values for both types of devices which insure proper circuit performance. Figure 3 illustrates the cross section of a CMOS structure connected in a simple inverter configuration. To form the standard metal gate CMOS structure, a lightly doped P-tub is formed by diffusion into an N-type substrate with the tub becoming the substrate for the N-channel transistor. The N+ and P+ impurities are diffused into P-tub and N-substrates to become the N- and P-channel transistors' source and drain regions, respectively. These diffusions also serve as contacting regions to the positively biased N-substrate and the normally grounded P-tub regions (V_{DD} and V_{SS}, respectively).

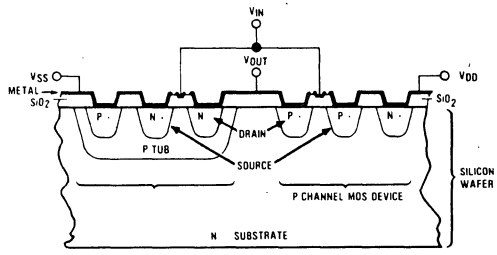


FIGURE 3. CMOS Transistor Structure in Simple Inverter Configuration

A gate oxide is grown such that a thin film of dielectric oxide material bridges all source/drain regions. Finally, contact apertures are etched to the source/drain regions and an aluminum film evaporated and etched to form gate electrodes, contacts to device terminals, and interconnecting conductor lines.

Effects of Ionizing Radiation

A CMOS transistors' radiation resistance is primarily determined by formation of the gate structures in both P-channel and N-channel devices. The gate structures are used to turn the MOS devices on or off; that is, to enable or prevent a flow of current from the source to the

drain. Ionizing radiation induces unwanted positive charge into the gate oxide structure, resulting in lower threshold voltages for both actual circuit devices and parasitic field oxide devices by as much as 30V or more. Figure 4 shows the charge buildup mechanisms in an N-channel gate oxide during irradiation under worst-case bias. In establishing a radiation hardened CMOS process, it is necessary to incorporate processing steps which minimize these radiation-induced shifts in critical locations of the IC structure.

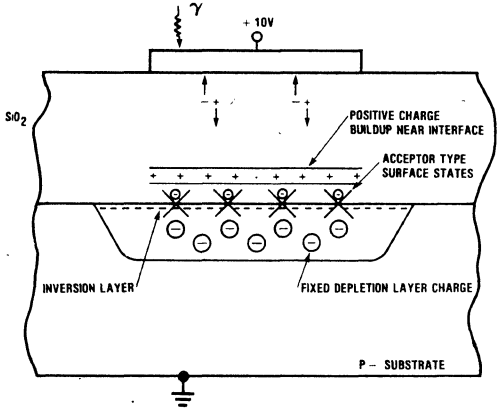


FIGURE 4. Charge Buildup Mechanisms in an N-Channel Gate Oxide during Irradiation under Worst-Case Bias

The impact of radiation-induced oxide charge on operating CMOS devices is to decrease the N-channel threshold voltage, V_{TN}, and increase the magnitude of the P-channel threshold voltage, V_{TP}. The most serious problem occurs when sufficient reduction in V_{TN} occurs to cause the N-channel device to go from enhancement to depletion mode operation. This results in excessive power supply current drain and loss of circuit functionality. The most severe stress on an N-channel device occurs when its gate is positively biased during irradiation. This causes positive charge in the oxide to be driven closer to the Si-SiO_2 interface where it is more effective in causing inversion at the P-type substrate surface.

In normal operation, positive bias cannot appear between the gate and substrate of P-channel devices because the substrate is already at the most positive circuit potential, V_{DD}. The absolute value of V_{TP} always increases with exposure to irradiation, and the magnitude of the shift is usually smaller than the V_{TN} shift. The effect of the V_{TN} is less deleterious to circuits, however, since the devices will never reach depletion mode.

CMOS Process Modification

Gate Oxidation

To minimize both the radiation-induced positive oxide charge and formation of Si-SiO_2 interface states, a dry oxidation step is used. The gate oxide is thermally grown in a dry oxygen atmosphere at 1000°C, followed by a nitrogen anneal at 850°C. This cycle has been empirically found to produce oxides having a high degree of resistance to ionizing radiation effects as well as excellent pre-radiation MOS characteristics.[2] The need to thermally grow gate oxides at 1000°C in dry oxygen for optimal radiation hardness is one of the more intriguing aspects of this experimentally deduced cycle.

Metallization

A by-product of the E-beam aluminum evaporation process commonly used in commercial IC fabrication is soft X-radiation. This radiation produces the same type of positive charge in the gate oxide and interface states which a radiation hardened oxide should resist. Although these harmful effects in the gate oxide can be removed by an anneal cycle, the annealled devices are significantly less resistant to subsequent ionizing radiation. Use of a non-E-beam metallization technique circumvents the problem of high threshold shifts due to irradiation under zero and negative gate bias associated with soft X-ray damage. For this reason, induction heated evaporation of aluminum is used to fabricate radiation hardened CMOS products.

Substrate and P-Tub Surface

The deleterious effect of ionizing radiation on V_{TN} and V_{TP} values in a CMOS device can be minimized through process modification. In anticipation of these threshold voltage shifts, radiation hardened CMOS devices are designed with the initial value of V_{TN} as high as possible and V_{TP} as close to zero as possible without sacrificing pre-radiation circuit performance. Both the substrate resistivity and the P-tub surface concentration have been modified with the initial value of V_{TN} being increased to 1.8 volts from the standard value of 1.3 volts and V_{TP} being changed from the standard -1.7 volts to -1.3 volts.

2. *W. R. Dawes, Jr., G. F. Derbenwich and B. L. Gregory, "Process Technology for Radiation Hardened CMOS Integrated Circuits," IEEE Journal of Solid State Circuits, SC-11, No. 4, p. 459, August 1976.*

Performance Characteristics

Extended Total Dose Rate [to 10^8 Rads (Si)]

Data generated in the course of our testing indicates that the resistance of our CMOS products extends at least one order of magnitude above the 10^7 level we now offer. Figure 5 illustrates measured shifts from pre-irradiation values in P-and N-channel threshold voltage, V_{TP} and V_{TN}, respectively, up to total dose levels of 10^8 rads (Si). Of special interest is the change in slope of the V_{TN} versus dose characteristic at levels just above the 10^6 rads (Si). At this level, a reduction in the net positive charge trapped in the gate oxide is observed. This causes V_{TN} to return toward its initial value as dose level is increased even further while increases in V_{TP} still remain within reasonable limits for satisfactory circuit operation.

The distributions of the V_{TN} and V_{TP} data are found to be normal both before and after irradiation. The mean value of V_{TN} and V_{TP}, and the standard deviation from the mean for both N- and P-channel devices, remain fairly constant from the unirradiated state through 10^6 rads (Si) dosage. The values shown remain well above the 300mV V_{TN} lower limit, below which the device would tend toward N-channel depletion mode behavior with a risk of lost circuit functionality as well as excessive supply current drain.

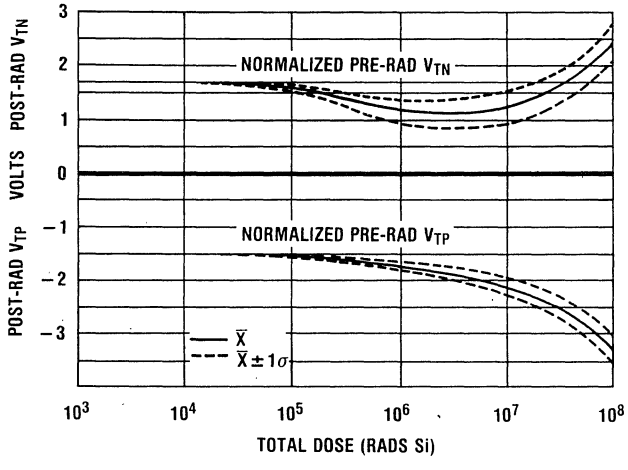


FIGURE 5. Variation of V_{TN} and V_{TP} with Radiation

8

Figure 6 illustrates the supply quiescent current (I_{SS}) variation as a function of dose. Since I_{SS} is a function of die size, curves have been plotted for three levels of integration, SSI, MIS, and LSI. In all cases, the leakage level at 10^6 rads (Si) does not increase by more than an order of magnitude from the initial value. The 30μA reading at 10^6 rads (Si) for LSI is far below the high temperature (125°C) specification of 600μA for standard devices. Similar comparisons can be made for MSI and SSI.

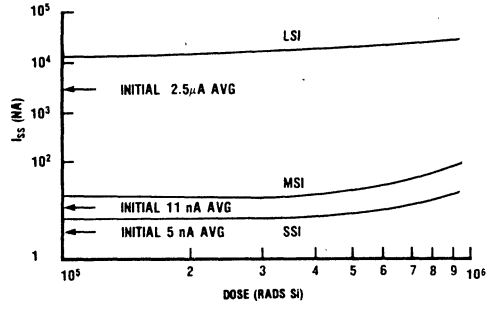


FIGURE 6. I_{SS} vs. Dose

Figure 7 illustrates circuit propagation delay, t_{PD}, as a function of dose. The plot, similar to Figure 6, is divided into three categories (LSI, MSI, and SSI). The propagation delay value at 10^6 rads (Si) for all three categories increased roughly 20-25% from the initial value, well within desirable operating tolerances. In Figures 5 through 7, the biasing conditions during irradiation were: $V_{DD} = 10V$, $V_{IN} = 10V$, $V_{SS} = 0V$.

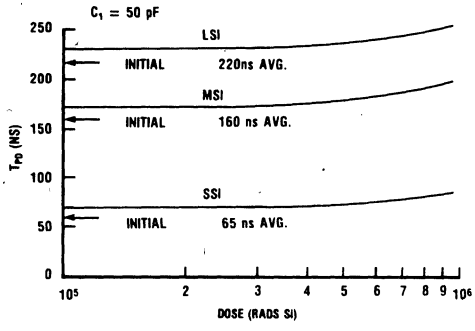


FIGURE 7. t_{PD} vs. Dose

Hardness Assurance and Reliability

Sampling plans have been established to ensure radiation hardness to 10^5, 10^6, or 10^7 rads (Si), as applicable, since ionizing radiation degrades IC performance and irradiated devices cannot be used for production (thus making 100% screening impossible). In addition, an ongoing program has been established to evaluate the reliability characteristics of radiation hardened CMOS circuits. 476 devices of the CD4001AD-RH, CD4011AD-RH, and MM54C200-RH types were initially tested and operated for over 800,000 hours without a failure. This corresponds to a failure rate less than 0.125%/1000 hours at 125°C with a 60% confidence level. The continuing testing is aimed at verifying 10,000 hours per device of reliable operation.

Table I outlines National Semiconductor's Radiation Hardness Assurance Sampling Plan, which is totally compliant with MIL-STD-883, Method 1019. This plan is used to assure hardness of devices built from a given wafer or inspection lot. Sample devices are assembled in accordance with sampling plan A or B. Sample devices are tested, irradiated, and retested, and must pass the appropriate post-radiation electrical limits for the lot to be qualified. The production units are capable of meeting MIL-M-38510 electrical test limits, when available, as well as National's RETS limits.

TABLE I. Hardness Assurance Plan

I. Plan A — Class B only: Qualification to 1×10^5, 1×10^6, or 1×10^7 rads (Si)	
Sample Size per QCI Inspection Lot	11
Accept Level	0 Rejects
Reject Level	1 Reject
II. Plan B — Class B or S: Qualification to 1×10^5, 1×10^6, or 1×10^7 rads (Si)	
Sample	Each wafer
Sample Size (Devices/Wafer)	4
Accept Level	0 Rejects per wafer
Reject Level	1 Reject per wafer
III. Product Flow (per MIL-STD-883, Method 1019):	
A. Assemble sample devices in appropriate production package.	
B. Read-and-record electrical parameters (pre-radiation).	
C. Irradiate to applicable total gamma dose.	
D. Read-and-record electrical parameters (post-radiation).	
E. Evaluate performance per applicable specification.	

TABLE II-A. Pre- and Post-Radiation Specification 10^5 Rads (Si)

PARAMETER		V_{DD}	CONDITIONS	LIMITS (Note 1)						UNITS
				−55°C		+25°C		+125°C		
				Min	Max	Min	Max	Min	Max	
I_{DD}	Gate	5	$V_{IN} = V_{DD}$ or V_{SS} All Valid Input Combinations		0.02		0.02		0.2	μA
		10			0.04		0.04		0.4	
		15			0.075		0.075		0.75	
	Buffer F/F	5			0.3		0.3		3.0	μA
		10			0.4		0.4		4.0	
		15			0.5		0.5		5.0	
	MSI	5			0.3		0.3		3.0	μA
		10			0.4		0.4		4.0	
		15			0.5		0.5		5.0	
	LSI	5			10		10		150	μA
		10			20		20		300	
		15			40		40		600	
V_{OL}		5	$V_{IN} = V_{DD}$ or V_{SS} $\|IO\| < 10\mu A$		0.05		0.05		0.05	V
		10			0.05		0.05		0.05	
		15			0.05		0.05		0.05	
V_{OH}		5	$V_{IN} = V_{DD}$ or V_{SS} $\|IO\| < 10\mu A$	4.95		4.95		4.95		V
		10		9.95		9.95		9.95		
		15		14.95		14.95		14.95		
V_{IL}	Buffered	5	VO = 0.5V, 4.5V		1.5		1.5		1.5	V
		10	VO = 1V, 9V, $\|IO\| < 10\mu A$		3.0		3.0		3.0	
		15	VO = 1.5V, 13.5V		4.0		4.0		4.0	
	Unbuffered	5	VO = 1.5V, 3.5V		1.5		1.5		1.5	V
		10	VO = 3V, 7V $\|IO\| < 10\mu A$		3.0		3.0		3.0	
		15	VO = 4V, 11V		4.0		4.0		4.0	
V_{IH}	Buffered	5	VO = 0.5V, 4.5V	3.5		3.5		3.5		V
		10	VO = 1V, 9V $\|IO\| < 10\mu A$	7.0		7.0		7.0		
		15	VO = 1.5V, 13.5V	11		11		11		
	Unbuffered	5	VO = 1.5V, 3.5V	3.5		3.5		3.5		V
		10	VO = 3V, 7V $\|IO\| < 10\mu A$	7.0		7.0		7.0		
		15	VO = 4V, 11V	11		11		11		
I_{IN}		15	V_{IN} = 0V or 15V Any Valid Condition		± 10		± 10		± 45	nA
I_{OL}/I_{OH}			Per Applicable Rel Electrical Test Spec (RETS)	Published Data Sheet Limit						
t_{PLH}, t_{PHL} t_{TLH}, t_{THL}			Per Applicable Rel Electrical Test Spec (RETS)	Published Data Sheet Limit						
Functionality			Devices Will Pass Functional Test per Applicable Truth Table							

Note 1: For further device parameters, see individual device specifications.
Note 2: These limits allow no degradation from the published data sheet limits.

8

TABLE II-B. Post-Radiation Specification 10^6 Rads (Si)

PARAMETER		V_{DD}	CONDITIONS	LIMITS (Note 1)						UNITS
				− 55°C		+ 25°C		+ 125°C		
				Min	Max	Min	Max	Min	Max	
I_{DD}	Gate	5	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations		0.5		0.5		5.0	μA
		10			0.75		0.75		7.5	
		15			1.0		1.0		1.0	
	Buffer F/F	5			0.25		0.25		5.0	μA
		10			0.5		0.5		7.5	
		15			1.0		1.0		10.0	
	MSI	5			3.0		3.0		30.0	μA
		10			4.0		4.0		40.0	
		15			5.0		5.0		50.0	
	LSI	5			25		25		300	μA
		10			50		50		400	
		15			100		100		500	
V_{OL}		5	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$		0.25		0.25		0.25	V
		10			0.25		0.25		0.25	
		15			0.25		0.25		0.25	
V_{OH}		5	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$	4.75		4.75		4.75		V
		10		9.75		9.75		9.75		
		15		14.75		14.75		14.75		
V_{IL}	Buffered	5	VO = 0.5V, 4.5V		1.0		1.0		1.0	V
		10	VO = 1V, 9V, $\|IO\| < 10\mu A$		2.0		2.0		2.0	
		15	VO = 1.5V, 13.5V		2.5		2.5		2.5	
	Unbuffered	5	VO = 1V, 4V		1.0		1.0		1.0	V
		10	VO = 2V, 8V $\|IO\| < 10\mu A$		2.0		2.0		2.0	
		15	VO = 2.5V, 12.5V		2.5		2.5		2.5	
V_{IH}	Buffered	5	VO = 0.5V, 4.5V	4.0		4.0		4.0		V
		10	VO = 1V, 9V $\|IO\| < 10\mu A$	8.0		8.0		8.0		
		15	VO = 1.5V, 13.5V	12.5		12.5		12.5		
	Unbuffered	5	VO = 1V, 4V	4.0		4.0		4.0		V
		10	VO = 2V, 8V $\|IO\| < 10\mu A$	8.0		8.0		8.0		
		15	VO = 2.5V, 12.5V	12.5		12.5		12.5		
I_{IN}		15	V_{IN} = 0V or 15V Any Valid Condition		± 100		± 100		± 100	nA
I_{OL}/I_{OH}			Per Applicable Rel Electrical Test Spec (RETS)	Minimum Limit is 75% of Published Data Sheet Limit						
t_{PLH}, t_{PHL} t_{TLH}, t_{THL}			Per Applicable Rel Electrical Test Spec (RETS)	Maximum Limit is 125% of Published Data Sheet Limit						
Functionality			Devices Will Pass Functional Test per Applicable Truth Table							

Note 1: For other device parameters, see individual device specifications.

TABLE II-C. Post-Radiation Specification 10^7 Rads (Si)

PARAMETER		V_{DD}	CONDITIONS	LIMITS (Note 1)						UNITS
				−55°C		+25°C		+125°C		
				Min	Max	Min	Max	Min	Max	
I_{DD}	Gate	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations		3.0 4.0 5.0		3.0 4.0 5.0		10 15 20	μA
	Buffer F/F	5 10 15			3.0 4.0 5.0		3.0 4.0 5.0		5.0 10 20	μA
	MSI	5 10 15			5.0 7.5 10.0		5.0 7.5 10.0		50 75 100	μA
	LSI	5 10 15			50 100 200		50 100 200		500 750 1000	μA
V_{OL}		5 10 15	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$		0.5 0.5 0.5		0.5 0.5 0.5		0.5 0.5 0.5	V
V_{OH}		5 10 15	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$	4.5 9.5 14.5		4.5 9.5 14.5		4.5 9.5 14.5		V
V_{IL}	Buffered	5 10 15	VO = 0.5V, 4.5V VO = 1V, 9V, $\|IO\| < 10\mu A$ VO = 1.5V, 13.5V		1.0 2.0 2.5		1.0 2.0 2.5		1.0 2.0 2.5	V
	Unbuffered	5 10 15	VO = 1V, 4V VO = 2V, 8V $\|IO\| < 10\mu A$ VO = 2.5V, 12.5V		1.0 2.0 2.5		1.0 2.0 2.5		1.0 2.0 2.5	V
V_{IH}	Buffered	5 10 15	VO = 0.5V, 4.5V VO = 1V, 9V $\|IO\| < 10\mu A$ VO = 1.5V, 13.5V	4.0 8.0 12.5		4.0 8.0 12.5		4.0 8.0 12.5		V
	Unbuffered	5 10 15	VO = 1V, 4V VO = 2V, 8V $\|IO\| < 10\mu A$ VO = 2.5V, 12.5V	4.0 8.0 12.5		4.0 8.0 12.5		4.0 8.0 12.5		V
I_{IN}		15	V_{IN} = 0V or 15V Any Valid Condition		± 100		± 100		± 100	nA
I_{OL}/I_{OH}		Per Applicable Rel Electrical Test Spec (RETS)		Minimum Limit is 65% of Published Data Sheet Limit						
t_{PLH}, t_{PHL} t_{TLH}, t_{THL}		Per Applicable Rel Electrical Test Spec (RETS)		Maximum Limit is 140% of Published Data Sheet Limit						
Functionality		Devices Will Pass Functional Test per Applicable Truth Table								

Note 1: For other device parameters, see individual device specifications.

8

TABLE III. Post-Radiation Specification Comparison (25°C)

PARAMETER		V_{DD}	CONDITIONS	LIMITS (Note 1)						UNITS
				10^5 Rads (Si)		10^6 Rads (Si)		10^7 Rads (Si)		
				Min	Max	Min	Max	Min	Max	
I_{DD}	Gate	5 10 15	$V_{IN} = V_{SS}$ or V_{DD} All Valid Input Combinations		0.02 0.04 0.075		0.5 0.75 1.0		3.0 4.0 5.0	μA
	Buffer F/F	5 10 15			0.3 0.4 0.5		0.25 0.5 1.0		3.0 4.0 5.0	μA
	MSI	5 10 15			0.3 0.4 0.5		3.0 4.0 5.0		5.0 7.5 10.0	μA
	LSI	5 10 15			10 20 40		25 50 100		50 100 200	μA
V_{OL}		5 10 15	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$		0.05 0.05 0.05		0.25 0.25 0.25		0.5 0.5 0.5	V
V_{OH}		5 10 15	$V_{IN} = V_{SS}$ or V_{DD} $\|IO\| < 10\mu A$	4.95 9.95 14.95		4.75 9.75 14.75		4.5 9.5 14.5		V
V_{IL}	Buffered	5 10 15	VO = 0.5V, 4.5V VO = 1V, 9V, $\|IO\| < 10\mu A$ VO = 1.5V, 13.5V		1.5 3.0 4.0		1.0 2.0 2.5		1.0 2.0 2.5	V
	Unbuffered	5 10 15	VO = Note 2 $\|IO\| < 10\mu A$		1.5 3.0 4.0		1.0 2.0 2.5		1.0 2.0 2.5	V
V_{IH}	Buffered	5 10 15	VO = 0.5V, 4.5V VO = 1V, 9V $\|IO\| < 10\mu A$ VO = 1.5V, 13.5V	3.5 7.0 11		4.0 8.0 12.5		4.0 8.0 12.5		V
	Unbuffered	5 10 15	VO = Note 2 $\|IO\| < 10\mu A$	3.5 7.0 11		4.0 8.0 12.5		4.0 8.0 12.5		V
I_{IN}		15	$V_{IN} = 0V$ or 15V Any Valid Condition		±10		±100		±100	nA
I_{OL}/I_{OH}		Per Applicable Rel Electrical Test Spec (RETS)		Data Sheet Limit		75% of Data Sheet		60% of Data Sheet		
t_{PLH}, t_{PHL} t_{TLH}, t_{THL}		Per Applicable Rel Electrical Test Spec (RETS)			Data Sheet		125% of Data Sheet		140% of Data Sheet	
Functionality		Devices Will Pass Functional Test per Applicable Truth Table								

Note 1: All 10^5 rads (Si) limits allow no degradation from published data sheet limits.

Note 2: At 10^5 rads (Si), VO will be 10% or 90% of V_{DD}; at 10^6 or 10^7 rads (Si), VO will be 1V or 4V at $V_{DD} = 5V$, 2V or 8V at $V_{DD} = 10V$, and 2.5V or 12.5V at $V_{DD} = 15V$.

Dose Rate Performance

When CMOS ICs are subjected to large bursts of ionizing radiation, hole-electron pairs are created in the silicon substrate. The resultant current flowing through the high resistivity P- and N-substrates can cause voltage differences which may impair circuit performance in one of the following ways.

One: LATCH-UP

A CMOS circuit contains the structural elements required to form a four-layered Schottky diode switching device as illustrated in Figure 8. The emitter-base junctions of the lateral PNP and vertical NPN which comprise the Schottky diode are normally prevented from becoming forward-biased by the circuit metallization. Because of this, the Schottky diode will be in the off state during normal circuit operation and will pose no threat to reliable circuit performance.

Sufficiently high values of burst radiation can cause currents to flow through substrate resistances, R_{N-} and R_{P-}, to cause forward-biasing of the parasitic PNP and NPN emitter-base junctions and turn on the Schottky diode. The excessive flow of supply current which accompanies turn-on of the Schottky diode has been found to occur in the range of 10^8 to 10^1 rads (Si)/sec on many CMOS circuits.

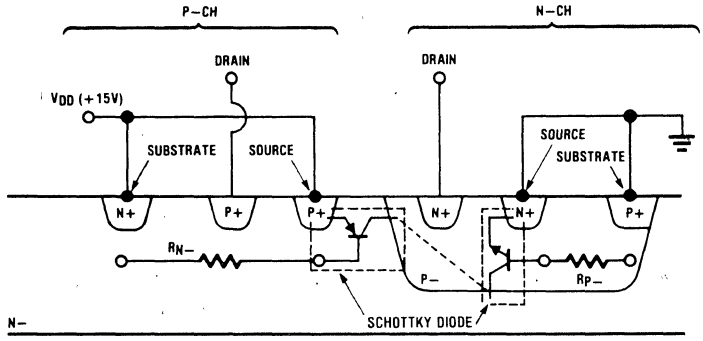


FIGURE 8. Cross Section of CMOS Circuit Elements which May Lead to Latch-Up during Ionizing Radiation Bursts

The basic circuit required for latch-up to occur is illustrated in Figure 9. It consists of a parasitic bipolar NPN and PNP transistor sharing a common collector-base junction. The two requirements necessary for turn on of this device are:

1. The product of the common emitter current gains of the two devices, β and β_{PNP} must satisfy the relationship $(\beta_{NPN})(\beta_{PNP}) \geq 1$, and
2. The emitter-base junction of the two transistors must remain forward-biased to about 0.6V or greater after the NPNP device has been turned on.

In normal operation, condition No. 1 may be met, but condition No. 2 will not be met, permitting latch-up-free operation.

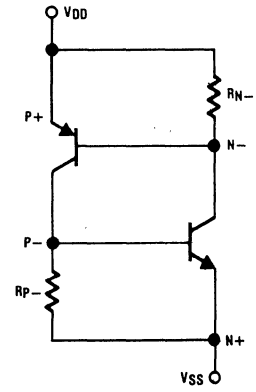


FIGURE 9. Latch-Up Equivalent Circuit for Bulk CMOS Structure

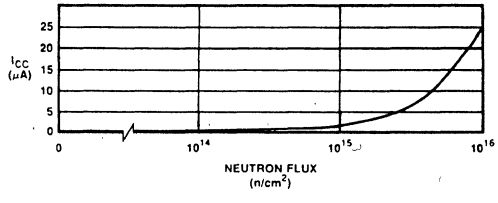
This problem can be completely eliminated by reducing to less than unity the product of the common emitter current gains of the NPN and PNP devices comprising the Schottky diode. One technique which has been successfully employed to eliminate the latch-up problem has been the use of neutron irradiation to lower minority carrier lifetime in the silicon substrate which directly affects parasitic bipolar current gains. As the values in Table IV indicate, neutron treatment of parts which exhibit latch-up at 3×10^8 and 3×10^9 rads (Si)/sec resulted in latch-up-free operation up to the limit of the burst simulation equipment, 10^{10} rads (Si)/sec.

TABLE IV. Latch-Up Performance

DEVICE	V_{DD}	DOSE REQUIRED FOR LATCH-UP		UNITS
		CONTROL (NON-NEUTRON TREATED)	NEUTRON TREATED*	
CD4006	10V	$>9.4 \times 10^9$	$>9.4 \times 10^9$	Rads (Si)/sec
CD4011	10V	3.1×10^9	$>9.4 \times 10^9$	Rads (Si)/sec
CD4012	10V	2.0×10^9	$>2.4 \times 10^9$	Rads (Si)/sec
CD4053	10V	3.2×10^8	$>9.4 \times 10^9$	Rads (Si)/sec
MM54C200	5V	$>2.2 \times 10^{10}$	$>8.8 \times 10^{11}$	Rads (Si)/sec

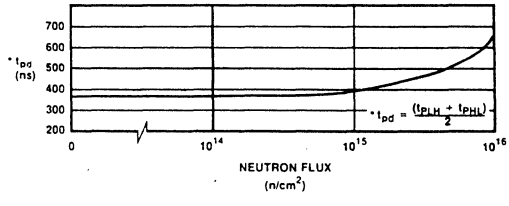
*Neutron treated parts were subjected to a neutron flux of 1×10^{14} neutrons (fast)/cm^2.

By treating wafers with neutron fluxes on the order of 10^{14}/cm^2, this enhanced circuit performance is obtained without sacrificing parametric performance. This is illustrated in Figures 10 and 11, which plot supply drain and propagation delay, respectively, versus neutron flux and show no significant degradation at the 10^{14}/cm^2 level.



DEVICE USED: MM54C200D/RH (256-BIT RAM)

FIGURE 10. Device Quiescent Supply Current vs. Neutron Flux



DEVICE USED: MM54C200D/RH (256-BIT RAM)

FIGURE 11. Propagation Delay vs. Neutron Flux

Another very successful method that has been used to reduce susceptibility to dose rate induced latch-up has been to use low resistivity substrate material with a high resistivity epitaxial layer. This structure introduces a low impedance shunt across R_{N-} in Figure 9, and hence prevents latch-up. Using this technique, devices can be supplied which do not latch-up even when exposed to dose rates of 10^{12} rads/sec.

Two: DATA-UPSET

This effect results in the loss of stored data in a circuit after being subjected to burst radiation. It is typically of most concern in circuits such as memories and shift registers, where stored data bits are not directly coupled to circuit inputs. The problem is again caused by electron hole pair generation during ionizing burst radiation exposure. The resulting photo currents can cause a current flow across a normally reverse-biased PN junction. This current flow can upset the logic level stored at a node associated with the PN junction.

Table V shows the effect that neutron treatment of an MM54C200D/RH 256-bit static RAM has on the dose rate at which upset occurs. The effect of neutron fluxes on data upset is not nearly as dramatic as it is in the case of latch-up. Although neutron fluxes in excess of 10^{15}/cm^2 cause significant alterations in semiconductor material properties and circuit electrical parameters, Figures 10 and 11 indicate that the circuits tested would still meet data sheet requirements after irradiation in excess of 2×10^{15}/cm^2. At this level the tolerance to data upset exhibits about a

TABLE V. Data Upset Performance

NEUTRON FLUX (N-FAST/cm^6)	DOSE RATE NEEDED TO INDUCE DATA UPSET		UNITS
	CD4006D 18-BIT SHIFT REGISTER $V_{DD} = 10V$	MM54C200D (MEMORY ENABLED) 256-BIT RAM, $V_{DD} = 5V$	
0 (control)	4.7×10^8	1.76×10^8	Rads (Si)/sec
1×10^{14}	4.7×10^8	2.00×10^8	Rads (Si)/sec
1×10^{15}	—	5.00×10^8	Rads (Si)/sec
1×10^{16}	—	1.17×10^9	Rads (Si)/sec

threshold improvement over untreated devices. Almost an entire order of magnitude improvements in data upset tolerance can be obtained with treatment at $10^{16}/cm^2$ if the user can tolerate the degraded propagation delay and increased supply current drain occurring at this level.

Rad Hard CMOS Reliability

Radiation hardness, however, is of no value to the system user if it is accomplished at the sacrifice of device reliability. To confirm device reliability, each of 476 units from five lots were subjected to 2.016 hours of burn-in at 125°C. The total device hours were 804,384, which represents a projected 0.11%/1000 hours failure rate at a 60% confidence level. This falls well within the reliability requirements of even the most stringent programs.

In addition to this initial sampling, 100% burn-in screening, as well as operating life testing, has been performed on many lots that have been produced for various customers. The results of this additional testing have continued to demonstrate that rad hard devices are reliable. 10,000-hour life tests are currently underway to further establish long-term reliability. The results of this testing and further testing across our entire rad hard product line will be added to the existing data as they become available.

Radiation Hardened Linear Devices

Although most bipolar logic devices tend to be inherently hard when exposed to total-dose gamma radiation, many bipolar linear devices will begin to degrade when exposed to relatively low levels of such radiation. The causes are similar to those seen in MOS radiation exposure-related failures. Linear devices are more susceptible to low current β degradation than most bipolar technologies. A major cause of of low current β degradation is surface leakage across the emitter-base junction. This surface leakage, like MOS characteristics, is related to the oxide and interface charges which are induced by high levels of radiation.

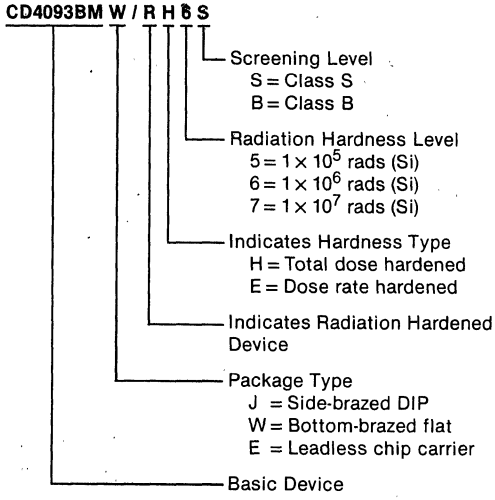
The solution to linear radiation problems, however, is quite different from what we have described above for CMOS devices. Total modification of the fabrication process is needed in order to achieve megarad hardness on linear devices. We have developed megarad versions of the LM108A and LM101A. We have extensive research and development currently underway in this area, for we feel that a broad line of rad hard linear devices is essential if systems designers are to achieve total systems hardness.

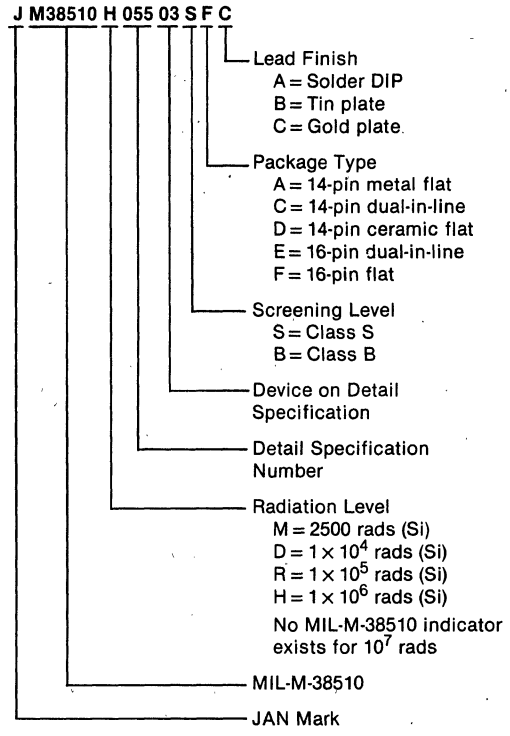
Ordering Information

National Semiconductor's Radiation Hardened CMOS devices are available in three different levels of hardness, one of which is sure to satisfy the needs of your program. The levels available are 1×10^5 rads (Si), 1×10^6 rads (Si), and 1×10^7 rads (Si), with post-radiation test limits as defined in Table II-A, II-B, or II-C of this brochure (as applicable). Each of these can be obtained in either a bottom-brazed flatpack or in a side-brazed dual-in-line package, both of which have solder-sealed lids. In addition, these devices may be obtained with either Class S or Class B screening.* National Semiconductor's 883B/RETS and 883S/RETS microcircuits (which are described in more detail in other brochures) are fully compliant with the 100% screening requirements of Method 5004 and MIL-STD-883 for the applicable screening level and have met the applicable quality conformance requirements of Method 5005 of MIL-STD-883.

National Semiconductor has qualified a number of Radiation Hardened devices in accordance with MIL-M-38510, and

Ordering is quite simple. Parts may be ordered using one of the following part number structures (as applicable).





In addition, we are willing to evaluate contractor-prepared prints for radiation hardened devices.

Radiation Susceptibility Testing

National Semiconductor has also recognized that there is a need on some programs for data relative to the actual hardness level of the product used, even where that product has not been specifically hardened. To address that need, National has developed a radiation susceptibility test program. The intent of this program is to provide, in advance of actual assembly of product, radiation tolerance data which will allow the user to determine whether those devices meet the radiation limits required by his program. Since the testing need not be done to a specific limit, this program is able to provide specific device data for those programs whose radiation tolerance limits are classified. Details on this program will be provided on request.

NATIONAL SEMICONDUCTOR'S MEGARAD RADIATION HARDENED PRODUCT LIST

The following device types were released as of December 1, 1983 by National Semiconductor as radiation hardened products to the 10^5, 10^6, 10^7 rads (Si) levels. These parts will be processed to National's 883S/RETS™ or 883B/RETS™ flow in the bottom-brazed flat ("F"), side-brazed dual-in-line ("D"), or ceramic ("J") and ("W") package configurations. This list supersedes and replaces all previously published lists.

IN DEVELOPMENT		
CD4006B MSI	MM54C08 SSI	MM54C30 SSI
CD4030B MSI	MM54C10 SSI	MM54C32 SSI
MM54C00 SSI	MM54C20 SSI	MM54C221 MSI
MM54C02 SSI		

RAD HARD CMOS						
DEVICE	SERIES	DEVICE	SERIES	DEVICE	SERIES	DEVICE
CD4000 MSI	A	CD4030 SSI	A	CD4082 SSI	B	MM54C89 MSI
CD4001 SSI	A/B	CD4031 MSI	A/B	CD4093 SSI	B	MM54C160 MSI
CD4002 SSI	A/B	CD4034 MSI	B	CD4094 MSI	B	MM54C161 MSI
CD4006 MSI	A	CD4035 MSI	A/B	CD4099 MSI	B	MM54C162 MSI
CD4007 SSI	A/UB	CD4040 MSI	A/B	CD40106 SSI	B	MM54C163 MSI
CD4008 MSI	A/B	CD4041 SSI	A	CD40160 MSI	B	MM54C173 MSI
CD4009 SSI	A	CD4042 MSI	A/B	CD40161 MSI	B	MM54C174 MSI
CD4010 SSI	A	CD4043 MSI	A/B	CD40162 MSI	B	MM54C175 MSI
CD4011 SSI	A/B	CD4044 MSI	A/B	CD40163 MSI	B	MM54C192 MSI
CD4012 SSI	A/B	CD4046 MSI	B	CD40174 MSI	B	MM54C193 MSI
CD4013 MSI	A/B	CD4047 MSI	B	CD40192 MSI	B	MM54C200 LSI
CD4014 MSI	A/B	CD4048 SSI	A/B	CD40193 MSI	B	MM54C240 MSI
CD4015 MSI	A/B	CD4049 SSI	A/UB	CD4510 MSI	B	MM54C244 MSI
CD4016 MSI	A/B	CD4050 SSI	A/B	CD4512 MSI	B	MM54C374 MSI
CD4017 MSI	A/B	CD4051 MSI	A/B	CD4514 MSI	B	MM54C901 SSI
CD4018 MSI	A/B	CD4052 MSI	A/B	CD4516 MSI	B	MM54C902 SSI
CD4019 SSI	A/B	CD4053 MSI	A/B	CD4518 MSI	B	MM54C903 SSI
CD4020 MSI	A/B	CD4066 SSI	A/B	CD4520 MSI	B	MM54C904 SSI
CD4021 MSI	A/B	CD4069 SSI	A/UB	CD4528 MSI	B	MM54C905 MSI
CD4022 MSI	A/B	CD4070 SSI	B	CD4538B MSI	B	MM54C906 SSI
CD4023 SSI	A/B	CD4071 SSI	B	CD4584 SSI	B	MM54C907 SSI
CD4024 MSI	A/B	CD4072 SSI	B	CD4724 MSI		MM54C914 MSI
CD4025 SSI	A/B	CD4073 SSI	B	MM54C04 SSI		MM54C941 MSI
CD4027 MSI	A/B	CD4075 SSI	B	MM54C14 SSI		MM70C95 SSI
CD4028 MSI	A/B	CD4076 MSI	B	MM54C42 MSI		MM70C96 MSI
CD4029 MSI	A/B	CD4081 SSI	B	MM54C85 MSI		MM70C97 SSI
				MM54C86 SSI		MM70C98 MSI
				CD4515 MSI		MM78C29 MSI
						MM78C30 MSI

For additional information regarding these or National's upcoming radiation hardened products, please contact Military/Aerospace Marketing at (408) 721-6670 — Mailstop 16-184.

National's A+ Program

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who cannot perform incoming inspection of ICs or do not wish to do so, yet need significantly better than usual incoming quality and higher reliability levels for their standard integrated circuits.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is a widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the repair and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quailty are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the precentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National has combined the successful B+ program with the Military/Aerospace processing specifications and provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

Five Temperature Cycles (70°C to 100°C)

Exercising each device over a 100° temperature range provides an additional die and package stress.

National's A+ Program (Continued)

High Temperature (100°C) Functional Electrical Test

A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C–15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

Electrical Testing

Every device is tested at 25°C for functional and DC parameters.

Burn-in Test

Each device is burned-in for 160 hours at a minimum junction temperature of +125°C or under equivalent conditions of time and temperature, as established by a time-temperature regression curve based on 0.96eV activation energy. All burn-in done under steady-state conditions unless otherwise specified.

DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-than-normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the A+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with three 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sample plans used in our A+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

National's B+ Program

B+ Program: a comprehensive program that assures high quality *and* high reliability of molded integrated circuits.

The B+ program improves both the quality *and* the reliability of National's digital, linear, and CMOS Epoxy B integrated circuit products. It is intended for the manufacturing user who cannot perform incoming inspection of ICs, or does not wish to do so, yet needs significantly-better-than-usual incoming quality and reliability levels for standard ICs.

Integrated circuit users who specify B+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembled boards.
- Reduces field failures.
- Reduces equipment down time.

Reliability Saves You Money

With the increases population of integrated circuits in modern electronic systems has come an increased concern with IC failures in such systems.

And rightly so, for at least two reasons.

First of all, the effect of component reliability on system reliability can be quite dramatic. For example, suppose that you, as a system manufacturer, were to choose an IC that is 99 percent reliable. You would find that if your system used only 70 such ICs, the overall reliability of the system's IC portion would be only 50 percent. In other words, only one out of two of your systems would operate. The result? A system very costly to produce and probably very difficult to sell.

Secondly, whether the system is large or small you cannot afford to be hounded by the spectre of unnecessary maintenance costs. Not only because labor, repair, and rework costs have risen—and promise to continue to rise—but also because field replacement may be prohibitively expensive. If you ship a system that contains a marginally-performing IC, an IC that later fails in the field, the cost of replacement may be—literally—hundreds of times more than the cost of the failed IC itself.

Improving The Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Now, it's true that reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement, which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate most marginal, short-life parts.

In any test for reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time to failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

Quality Improvement

When an IC vendor specifies 100 percent final testing of its parts then, in theory, every shipped part should be a good part. However, in any population of mass-produced items there does exist some small percentage of defective parts.

One of the best ways to reduce the number of such faulty parts is, simply, to retest the parts prior to shipment. Thus, if there is a one percent chance that a bad part will escape detection initially, retesting the parts reduces that probability to only 0.01 percent. (A comparable tightening of the QC group's sampled-test plan ensures the maintenance of the improved quality level.)

National's B+ Program Gets It All Together

We've stated that the B+ program improves both the quality *and* the reliability of National's molded integrated circuits, and pointed out the difference between those two concepts. Now, how do we bring them together? The answer is in the B+ program processing, which is a continuum of stress and double testing. With the exception of the final QC inspection, which is sampled, all steps of the B+ process are performed on 100 percent of the program parts. The following flow chart shows how we do it, step by step.

SEM

Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Processing for All Molded Parts

At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections, and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake

This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

High Temperature (100°C) Functional Electrical Test

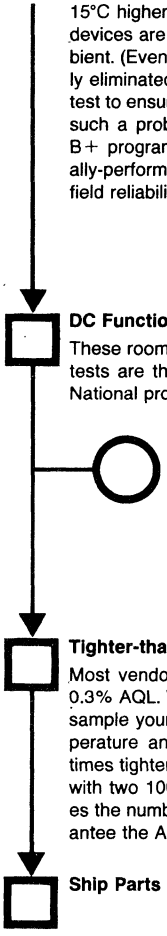
A high temperature test such as this with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C–

Five Temperature Cycles (70°C to 100°C)

Exercising each device over a 100° temperature range provides an additional die and package stress.

National's B+ Program (Continued)

15°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient. (Even though Epoxy B processing has virtually eliminated thermal intermittents, we perform this test to ensure against even the remote possibility of such a problem. Remember, the emphasis in the B+ program is on the elimination of those marginally-performing devices that would otherwise lower field reliability of the parts.)



DC Functional and Parametric Tests

These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Thermal Shock Monitor

Samples from each package type are selected at random each week and submitted to 100 cycles of liquid to liquid thermal shock −65°C to +150°C. In addition, samples are selected every four weeks and subjected to 2000 temperature cycles of 0°C to +25°C.

Tighter-than-normal QC Inspection Plans

Most vendors sample inspect outgoing parts to a 0.3% AQL. When you specify the B+ program, we sample your parts to a 0.035% AQL at room temperature and 0.05% AQL at T_A Max. This eight times tightening (from 0.3 to 0.035% AQL) coupled with two 100% electrical tests, dramatically reduces the number of "escapes" and allows us to guarantee the AQLs listed below.

Ship Parts

Here are the QC sampling plans used in our B+ test program:

Test	Temperature	AQL
Electrical Functionality	25°C	0.035%
Parametric, DC	25°C	
Parametric, AC	25°C	0.1%
Electrical Functionality	At each temperature extreme.	0.05%
Parametric, DC		
Mechanical		
Critical	—	0.01%
Major	—	0.28%

RELIABILITY REPORT

Reliability of

High Speed CMOS Logic

National
Semiconductor

RELIABILITY REPORT

INTRODUCTION

Until recently, the primary reasons for the popularity of CMOS logic circuits have been low power dissipation, tolerance to wider variations in power supply voltage, and the flexibility of using a broader range of power supplies. Although the acceptance of CMOS in logic applications has been increasing over the past decade, its growth has been limited by its inherently slower speed compared with its bipolar counterparts.

The metal gate technology, from which all of the popular CMOS families were built, typically yielded a 90 ns propagation delay for a buffered gate, and a guaranteed maximum more than double that, whereas, the bipolar equivalents in the popular low power Schottky family provided typical delay of 8 ns with maximums of 15. Under real-world demands of increasingly faster computer processing times, many systems simply could not use CMOS and at the same time meet system specifications.

The arrival of the silicon gate process allowed CMOS to make its largest technological improvement since its inception. By employing this process, National Semiconductor has been able to increase CMOS speeds to the point where they are now equal to LS speeds, while still maintaining the earlier power dissipation and supply voltage attractiveness.

Series 54HC/74HC High Speed CMOS was announced in the summer of 1981 and will include, when fully developed, nearly 200 logic devices. Many of these devices will be equivalents to those functions popular today in both "LS" and "4000" families.

KEY FEATURES OF THE SERIES 54HC/74HC FAMILY

- LS speeds at CMOS power
- Operation over a 2V to 6V power supply range
- Output sink and source capability of 4 mA
- AC guarantees across the applicable temperature range

HIGH SPEED (HC) CMOS DEVICE FABRICATION

High Speed CMOS wafer fabrication is designed to produce reliable, high performance devices which require minimum handling restrictions. At National Semiconductor, these objectives are achieved through the use of advanced materials, process innovations, and rigorous controls.

This high speed logic family represents an advanced 3.5 micron, single metal, polysilicon gate, oxide-isolated CMOS process. This process makes use of advanced technologies, including extensive use of ion implantations to tightly control substrate profiles.

National's HC processing permits the fabrication of MOS transistors with threshold voltages on the order of one-half that of the more conventional metal gate process. Coupled with thinner gate oxides and self-aligning gates, these lower threshold voltages allow higher speed circuit operation with lower supply voltages. In addition, the threshold voltage distribution from run to run is much tighter, so that long term uniformity of device characteristics is assured.

Figure 1 represents the cross section of the HC process employed at National.

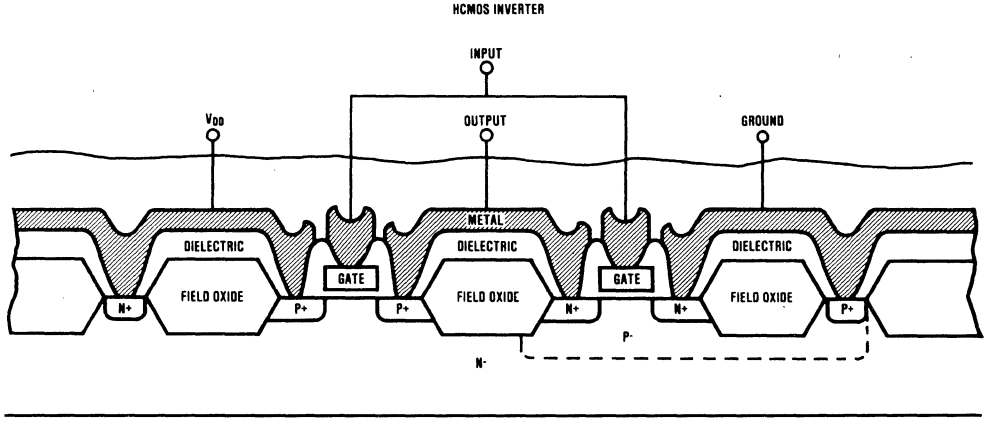


FIGURE 1. HCMOS Cross Section

RELIABILITY REPORT

ACCELERATED LIFE TEST

Accelerated life testing at elevated temperatures is a principal method of simulating long-term operation within a short period of time. This method is particularly useful because it provides a means of accelerating time-to-failure of temperature sensitive failure mechanisms. As a result, data is gathered for failure rate predictions at any operating field ambient.

The following tests have been conducted at an ambient temperature of 125°C with devices biased at a maximum voltage of 5.5 volts. Complete functional and parametric testing to data sheet specifications is performed at reported data points.

HIGH TEMPERATURE BIAS RELIABILITY TEST RESULTS
125°C OPERATION AT 5.5 VOLTS

CERDIP, GLASS SEALED HERMETIC DIP, J

Device	Rel Lot #	SS	168 Hours	500 Hours	1000 Hours
MM54HC04J	RBC71305	51	1 (1)	0	0
MM54HC04J	RBC72012	360	1 (2)	0	0
MM54HC139J	RBC72177	200	0	0	Stopped
MM54HC164J	RBC72178	192	0	0	Stopped
MM54HC00J	RBC72196	256	0	0	0
MM54HC390J	RBC72223	189	0	0	0
MM54HC393J	RBC72224	127	0	0	0
MM54HC04J	RBC72346	324	0	0	0
MM54HC174J	RBC72348	255	0	0	0

Actual Failure Rate = 2/1,757,664 device-hours
= 0.11% per 1000 hrs. at 125°C.

Notes: (1) Parametric Failure
(2) Gate Oxide Rupture

M DIP EPOXY MOLDED, N

Device	Rel Lot #	SS	168 Hours	500 Hours	1000 Hours
MM54HC04N	72011	358	0	0	0
MM54HC04N	72064	384	0	0	0
MM54HC04N	72065	384	0	0	0
MM54HC00N	72084	120	0	0	0
MM54HC164N	72142	256	0	0	0
MM54HC688N	72320	122	0	0	0
MM54HC393N	72339	104	1 (1)	0	0
MM54HC390N	72347	64	0	0	0
MM54HC349N	72349	108	0	0	0

Actual Failure Rate = 1/1,900,000 device-hours
= 0.05% per 1000 hrs. at 125°C.

Notes: (1) Parametric Failure

Quiescent current leakages were measured on molded pieces of two lots subjected to both HTOpL and T&H. Measurements were conducted before and after testing. Results are listed in Table I.

TABLE I
Average I_{CC} Shifts for Lots
MM54HC04A RBC72064 and RBC72065
(Units In Nanoamps)

Test	Leg	SS	Average At 0 Hours	Average At 1000 Hours
HTOpL	A	48	4	3
	B	48	21	25
	C	48	0	2
	D	48	0	0
T&H	A	48	2	19
	B	48	17	12
	C	48	16	14
	D	48	18	18
HTOpL	A	48	0	0
	B	48	0	0
	C	48	0	0
T&H	A	48	0	0
	B	48	0	0
	C	48	0	0

Threshold voltage measurements were also read before and after on one lot of cerdip and two lots of molded DIPs. Results are listed in Table II.

TABLE II
V_T Shifts After 1000 Hours Burn-In
(Units In Volts)

Lot	Leg	SS	Pre		Post	
			Avg. V_{TN}	Avg. V_{TP}	Avg. V_{TN}	Avg. V_{TP}
72012,J	A	48	.387	.579	.390	.580
	B	48	.347	.570	.402	.580
	C	48	.394	.570	.440	.580
	D	48	.350	.567	.336	.580
72064,N	A	48	.470	.580	.472	.570
	B	48	.530	.580	.499	.571
	C	48	.400	.527	.467	.570
	D	48	.471	.519	.518	.575
72065,N	A	48	.428	.580	.423	.572
	B	48	.453	.579	.448	.570
	C	48	.380	.529	.412	.570
	D	48	.402	.526	.453	.572

RESULTS

HC high temperature bias failure rates are calculated and derated at 85°C and 45°C operating environments for molded dual-in-line packages. The Arrhenius relationship is employed to compute the equivalent derated failure rate using an activation energy of 1.0eV. An average confidence limit of 60% is reported for these derated figures as seen in Table III.

Table III
High Temperature Operating Life Test
$T_A = 125°C$, $V_{CC} = 5.5V$ Static
60% Confidence Level

Device	Lots	Qty	Dev. Hours	# Fail	λ @ 125°C	λ @ 85°C	λ @ 45°C
Various	9	1,900	1,900,000	1	0.1032	0.0039	6.7100×10^{-5}

λ = Failure Rate; %/1000 Hours at Temperature.

(This data can be further extrapolated to lower temperatures using a 1.0eV activation energy as illustrated in the failure rate versus temperature plot of *Figure 2.*)

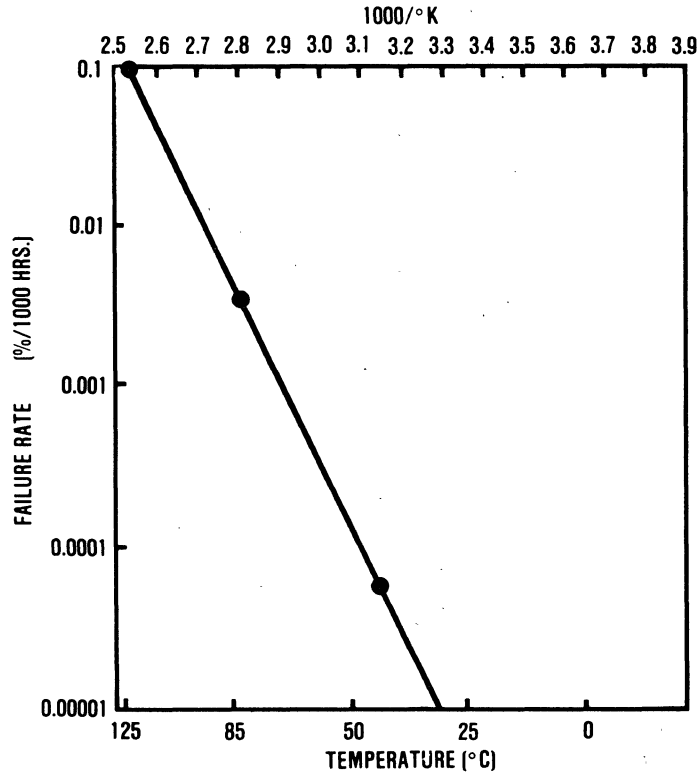


FIGURE 2. Failure Rate vs Temperature

TEMPERATURE HUMIDITY BIAS TEST (THB)

The steady state humidity test at 85°C and 85% relative humidity is the most common temperature/humidity test in use today. This is an accelerated test; that is, it involves stress levels considerably in excess of the field-use levels encountered by a device. The test is intended to trigger moisture-related failure mechanisms occurring over a period of months or years in the field. Results are seen below.

Device	Rel Lot #	SS	168 Hours	500 Hours	1000 Hours
MM54HC04N	RBC72011	340	0	0	0
MM54HC04N	RBC72064	192	0	0	0
MM54HC04N	RBC72065	192	1 (1)	0	1 (1)
MM54HC00N	RBC72084	96	0	1 (1)	0
MM54HC393N	RBC72339	95	2 (1, 2)	0	1 (3)
MM54HC04N	RBC73025	225	0	0	0
MM54HC390N	RBC72347	48	0	0	0

Cumulative Percent Failures at 1000 Hrs. = 6/1188 = 0.51%

Note: 1. Parametric Failures
2. Continuity Failures
3. Functional Failure

BIASED PRESSURE POT TEST

Another commonly used test is the "pressure cooker" test. This test is usually performed with devices in an operating mode while being exposed to saturated steam (100% RH). The most common condition is 115°C. At saturation, this temperature corresponds to a water vapor pressure of 1489mm Hg (28.8 psia). Due to its severity, this test is destructive to virtually all plastic packages. It creates failure mechanisms which would never be triggered at temperature and humidity extremes found in even the most severe application. For this reason, the test is limited to a relative few number of hours, and results are interpreted on a purely qualitative, comparative basis.

Biased Pressure Pot Test Results
$T_A = 115°C$, $V_{CC} = 5.5V$

Device	Rel Lot #	SS	96 Hours	192 Hours
MM54HC04N	RBC72064	75	0	0
MM54HC04N	RBC72065	75	0	0
MM54HC00N	RBC72084	75	0	0
MM54HC04N	RBC73025	148	0	0
MM54HC174N	RBC73024	54	0	1

IMPROVED INPUT PROTECTION

The single most prevalent cause of "infant mortality" field failures in CMOS microcircuits is generally gate oxide damage. This can result from any transient voltage condition, such as electrostatic discharge (ESD), inductive spikes, etc. An improved input protection circuitry which takes full advantage of the HC silicon gate process has been carefully designed to reduce the susceptibility of these HC circuits to oxide ruptures due to large static voltages.

In conjunction with the input protection, the output parasitic diodes also protect the circuit from large static voltages occurring between any input, output, or supply pin.

Figure 3 shows a schematic of the input protection network employed. The network consists of three elements: a polysilicon resistor, a diode connected to V_{CC}, and a distributed diode resistor connected to ground. This HC process utilizes the polyresistor to more effectively isolate the input diodes than the diode resistor used in metal gate CMOS. This resistor will slow down incoming transients and also helps to dissipate some of the energy. Connected to the resistor are the two diodes which clamp the input spike and prevent large voltages from appearing across the transistor. These diodes are larger than those used in metal gate CMOS, to enable greater current shunting and make them less susceptible to damage. The input network is ringed by V_{CC} and ground diffusions, which prevent the substrate currents caused by these transients from affecting other circuitry.

The parasitic output diodes that isolate the output transistor drains from the substrate are also important in preventing damage. They clamp large voltages that appear across the output pins. These diodes are also ringed by V_{CC} and ground diffusions to again shunt substrate currents, thus preventing damage to other parts of the circuit.

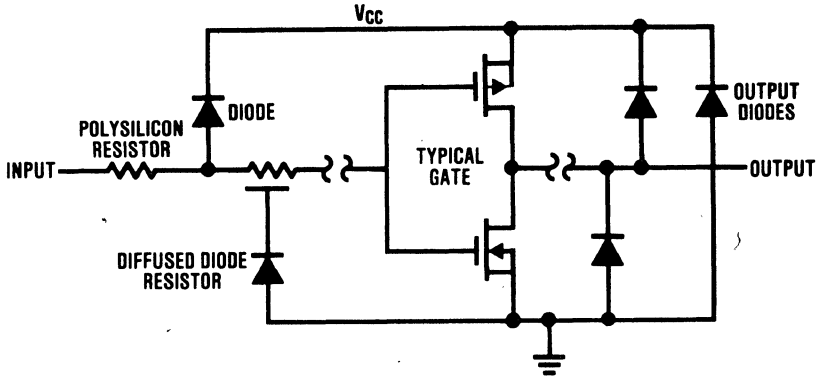
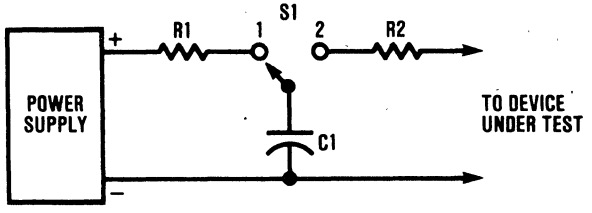


FIGURE 3. Input Protection Network

HIGH SPEED LOGIC INPUT PROTECTION ZAP TEST

Input gates of twenty MM54HC00 were subjected to a high voltage (V_{ZAP}) burst in order to test input protection circuits. The inputs under test were subjected to a voltage pulse from a 100 pF source charged to 1000V and 2000V respectively, according to the test circuit shown in *Figure 4*.



R1 = current limiting resistor; R2 = 1.5k

FIGURE 4. High Speed Logic Input Protection V_{ZAP} Test

Each input under test was subjected to a sequential V_{ZAP} accordingly:

Positive	Negative
(1) V_{DD}	Input
(2) Input	V_{DD}
(3) Input	V_{SS}
(4) V_{SS}	Input
(5) Output	Input
(6) Input	Output

V_{ZAP} six times (6×) for each condition.

ZAP results appear in Table IV.

TABLE IV
V_{ZAP} Test Results

Parameter	Condition 1	Condition 2
Voltage	1000V	2000V
Capacitance	100 pF	100 pF
Energy Discharged	50 μJ	200 μJ
Result	0/20*	0/20*

*Input leakages equal to or less than 4 nA.

HIGH SPEED LOGIC HTOPL BUY-OFF

In addition to ongoing long-term reliability studies and audits, National does an initial 168 hours high temperature bias design buy-off on every single HC product type before it is released into production. The primary reason behind this program is to assure the capture of any design-related reliability problem which might pass through all electrical tests. Accelerated conditions are the same as previously mentioned, i.e., $T_A = 125°C$, $V_{CC} = 5.5$ volts, burn-in time is 168 hours.

Device	SS	Results at 168 Hours
MM74HC00N	45	0
MM74HC02N	50	0
MM74HC04N	50	0
MM74HCU04N	50	0
MM74HC08N	49	0
MM74HC10J	50	0
MM74HC11J	50	0
MM74HC14N	48	0
MM74HC73J	50	0
MM74HC76J	50	0
MM74HC86J	50	0
MM74HC107J	50	0
MM74HC112J	40	0
MM74HC113J	50	0
MM74HC139N	45	0
MM74HC147N	50	0
MM74HC151N	50	0
MM74HC160J	50	0
MM74HC161J	50	0
MM74HC164N	45	0
MM74HC174N	45	0
MM74HC192N	50	0
MM74HC193N	49	0
MM74HC242N	50	0
MM74HC251J	50	0
MM74HC253N	50	0
MM74HC259N	50	0
MM74HC266J	50	0
MM74HC390N	49	0
MM74HC393N	50	0
MM74HC688N	50	0

HANDLING AND TEST GUIDE

Introduction

All CMOS low threshold devices are susceptible to damage by the electrostatic discharge (ESD) of energy through the devices. Although all CMOS devices have input protection networks which are effective in a large number of device-handling situations, they are not effective in 100% of the cases (please refer to specific devices in National's CMOS Databook).

In order to be totally safe, proper handling procedures must be used to eliminate damage and subsequent yield loss caused by static electrical charges. It is the purpose of this application guide to outline proper handling procedures for CMOS devices.

General Handling Procedures

1. The leads of CMOS devices must be in contact with conductive material to avoid build-up of static charge. Containers used for transporting or storing CMOS components should be made of such material or lined with antistatic protection. Rails for handling and shipping MOS devices must be made of electrically conductive material or be made static-free by an appropriate surface coating. In no case will CMOS devices be inserted into polystyrene foam or other high dielectric materials. Any surface coating which is not at ground potential must not come in direct contact with device pins.
2. Devices must be packed in conductive containers, rails or envelopes for storing. In addition, devices must be kept at ground potential and should never come in contact with nonconductive plastics.
3. All electrical equipment must be hard-wired to ground. Soldering iron tips, metal parts of fixtures and tools, and all handling systems must be grounded.

Cleaning

1. Devices should be cleaned by a solvent which will assure complete removal of foreign matter, flux, residual matter, etc., from the exterior of the package.
2. A static neutralizing ion blower should be used when manually cleaning devices or subassemblies with brushes.
3. All automatic cleaning should be grounded.
4. All cleaning baskets should be grounded.

Assembly

1. Subassembly modules and printed circuit boards should be manufactured and handled using the same procedures as those described above for individual CMOS devices.
2. CMOS parts should be the last to be inserted into printed circuit boards or systems so as to avoid overhandling.
3. Circuit boards containing CMOS devices which are being transported between work stations and test areas should be contained in antistatic material or have all board terminals shorted together using a conductive shorting bar. Only handling trays of conductive material should be used.
4. All automatic insertion equipment, solder machines, metallic parts of conveyor systems, and soldering irons should be grounded.

Note: These precautions should be taken until the subassembly is inserted into the complete system in which the proper voltages are applied. Subassemblies should never be constructed, fixtured, stored, or transported in polystyrene or any other high dielectric materials.

General Operating Procedures

The National CMOS product line is comprised of many different device types for a variety of applications. The following operating procedures apply in a general sense to all CMOS devices, but reference to device specification sheets is still necessary to assure correct operating values.

A. Before making any physical connections or applying any external signal sources, be sure that all power supplies are off. Be sure, also, to observe proper static ground conditions.

B. Power supplies should be turned up slowly to the necessary voltages so as to avoid rapid supply changes.

C. After power supplies have been turned on, apply external input signals.

Note: Failure to perform the power-on procedure in this order can result in damage to CMOS circuitry.

D. To power down, remove input signals, then turn power supplies off slowly.

E. If CMOS devices are operated at an elevated environmental temperature, allow devices to reach room temperature before they are powered down.

F. Do not leave inputs to any CMOS device unused. For NAND gates, the unused inputs should be tied to V_{DD}; unused inputs to NOR gates should be tied to ground.

Testing

1. Use grounded metallic fixtures where possible. Any surface that is not at ground potential should not come into direct contact with device pins.
2. Use a static-neutralizing ion air blower when running automatic handlers. Use conductive handling trays when transferring devices.
3. Do not insert devices or boards with power turned on.
4. Ensure that AC signals do not cause excessive current leakage.

Electrical Failure Modes Caused by Improper Handling

If proper handling techniques are not followed, the generation of static electrical discharges may damage the CMOS devices, resulting in inoperable or degraded parts. Typical failure modes are:

a. Shorted or open gates

b. Shorted input protection diodes

c. Open metal paths in the device input circuitry

d. Degraded device characteristics

The presence of these failure modes can be detected easily using a transistor curve tracer.

RELIABILITY REPORT

A New Era in CMOS Logic Molded Dual-In-Line Package Reliability

National
Semiconductor

RELIABILITY REPORT

FOREWORD

This report describes reliability data for National's integrated metal gate 54C/74C and CD4000 CMOS logic families in Epoxy B molding compound. National's approach to achieving the highest reliability is presented through a discussion of design; device fabrication and the Epoxy B package processing flow. A detailed description of environmental tests includes Accelerated Life Test, Analysis of Failure Mechanisms, Arrhenius Modeling, High Temperature Bias with Temperature and Humidity Acceleration, Biased Pressure Pot and Electrostatic Sensitivity (ESD). Results for all of these tests, as well as a comparison of National's products to competitive products in these tests is presented in a comprehensive manner. Tips on general handling procedures are also provided to help the user maintain the integrity of the product during the manufacturing cycle.

TABLE OF CONTENTS

I. A NEW ERA IN CMOS LOGIC MDIP RELIABILITY

National Semiconductor's task force of key design, process, product, test, and reliability personnel has constantly investigated every step in the production of CMOS—with one primary objective: improved quality and reliability. Every step—design, input protection, wafer fabrication passivation, molded assembly, and electrical testing was researched. Each area was evaluated, fine tuned, and re-evaluated until the final product was put on life test and shown to be the most reliable CMOS in the industry. For the first time, the data gathered shows that this improved CMOS product compares favorably with bipolar logic reliability. The following is a summary of the improvements, as well as the results.

A. Design, Excluding Input Protection

National is not content with simply providing the best molded package in the industry. The gate structure of our CMOS ICs has been redesigned to provide insurance against mobile ionic contaminant (principally sodium) penetration into the gate oxide. This achievement alone provides an order of magnitude improvement to the reliability of our CMOS circuits.

B. Input Protection

The single most prevalent cause of "infant mortality" field failures in CMOS microcircuits is gate oxide damage. This can result from any transient voltage condition, i.e., electrostatic discharge (ESD), electrical noise, inductive spikes, etc. Just how easily the devices can be destroyed is a function of the pin-to-pin impedance of the device and the thickness of the insulating oxide layers exposed to the electrostatic charge. The CMOS gate structure is more susceptible than bipolar structures because it presents very high impedance and very thin (easily ruptured) oxide to the electrostatic charge.

Protection against damage is provided by National's input protection circuitry, which limits the voltage impressed on the gate oxide. Just how effective this circuitry is depends on several design variables. National has optimized this protective circuitry through closely controlled doping levels, exact junction depths and other process controls, which lead to extremely consistent zener action of the circuitry. In addition, the layout of the input protection network (*Figure 1*) provides symmetrical protection against both positive and negative-going voltage spikes. Thus, the chance for failure caused by gate oxide rupture is drastically reduced.

This new generation CMOS is protected from voltage transients 3 to 4 times higher than its predecessor. Translated to field performance, this means an absolute minimum of "infant mortality" failures in the operation of CMOS devices in their end-use environment.

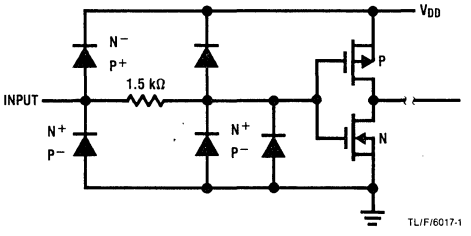


FIGURE 1. National's Improved Protection Network

C. Improved Die Passivation

As in any molded package system, there is a small probability that moisture will penetrate into the interior of the package via the molding compound-to-frame interface and, to a lesser degree, via diffusion through the bulk of the molded package. Since metal gate CMOS devices are subject to an 18V potential and have very low power dissipation, it is possible for moisture to be absorbed on the surface of the die. In addition, moisture usually contains impurities from various sources:

a. flux residues from tin dipping operation

b. ions leached from the molding compound

c. phosphorous penta-oxide present in the phospho-silicate glass passivation, which, combined with moisture, will produce phosphoric acid, an etchant of aluminum according to the following reactions:

$$2P_2O_5 + 6H_2O \rightarrow 4H_3PO_4$$

$$A + H_3PO_4 \rightarrow A\,PO_4 + 3/2\,H_2\uparrow$$

Through its continuing effort to improve reliability performance, National recently developed and introduced an improved CMOS Logic passivation technology *(Figure 2)*. This truly unique and proprietary passivation scheme has led to a virtually defect-free passivation which consistently meets and exceeds National's passivation defect criteria for pinholes, cracks and voids—the toughest standard in the industry. In addition, this improved passivation scheme offers the ability to absorb liquid contaminants onto its surface, thus preventing or inhibiting the final penetration into the interior of the active integrated circuit area.

TL/F/6017-2

FIGURE 2. National's CMOS Logic Passivation Scheme

The major advantages of this improved passivation scheme are as follows:

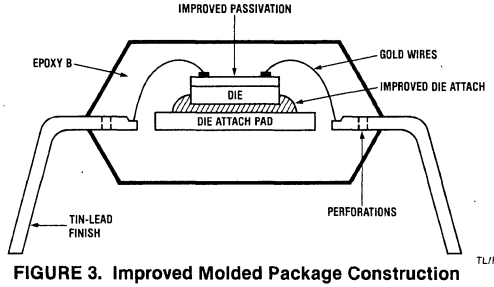
1. Exceedingly high purity passivation composition
2. Defect densities less than 0.01 per 1000 mils^2
3. Wafer fabrication process which easily covers irregular contours and other common defects
4. Inhibits moisture penetration to the surface of the die
5. Highly resistant to heat
6. Its thick resilient layer provides superior mechanical integrity and prevents passivation pinholes, cracks, and voids commonly associated with wafer fabrication, assembly and molding mechanical stresses.

D. Assembly

In its never-ending quest for improved reliability, National has also focused its attention to the molded assembly technology and made major improvements in this area. A close inspection of our improved molded package (*Figure 3*) will reveal:

a. A die attach whose temperatures are well below those associated with gold-silicon eutectic conditions.
b. Frame has an increased surface area which improves frame-to-epoxy adhesion, thus minimizing the chance of moisture penetration.
c. Frames are perforated to allow epoxy to pass through the frame fingers during the molding operation, thus forming a "locking" mechanism. This will prevent frame finger movement during the trim and form operation.
d. Gold wire bonding temperatures have been drastically reduced by using thermosonic bonding rather than commonly used thermocompression bonding.

All of the aforementioned improvements have been combined and the result is superior reliability performance for National molded CMOS Logic products.



TL/F/6017-3

FIGURE 3. Improved Molded Package Construction

II. DEVICE FABRICATION

CMOS wafer fabrication is designed to produce reliable, high-performance devices which require minimum handling restrictions. At National Semiconductor, these objectives are achieved through the use of advanced materials, process innovations, and rigorous process controls.

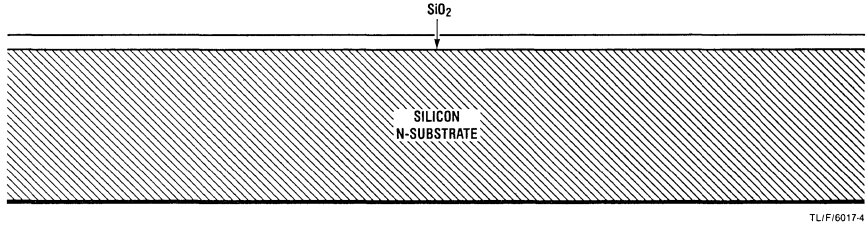
The substrate material used in the CMOS process is [1-0-0] orientation N-type silicon rather than the commonly selected [1-1-1] orientation type. Coupled with controlled processing, this substrate permits the fabrication of MOS transistors with threshold voltages up to half as low as that produced on [1-1-1] orientation silicon. Lower threshold voltages allow higher-speed circuit operation with lower supply voltages. In addition, the threshold voltage distribution from run to run is much tighter so that long term uniformity of device characteristics is assured.

The stability of CMOS characteristics depends directly on the level of contamination in the gate oxide. National's proprietary oxidation procedure and cleaning methods are capable of producing ultra-clean oxides. In order to ensure low levels of oxide contamination in production, all production oxidation and evaporation systems are monitored on a regular basis using the capacitance voltage method. A MOS capacitor is fabricated and drifted under + 15V bias at 300°C for two minutes. The shift in the C-V plot is a measure of the ionic contamination in the oxide under evaluation. This method is also used for investigations of process changes and innovations. These measurements assure rapid detection and correction of production process difficulties before contaminated material can leave the wafer processing area.

An additional check on stability is performed on completed wafers. Fields of $\pm 2 \times 10^6$V/cm are applied to C-V test dots (patterned onto the device die) while the wafer is heated to 300°C for two minutes, then cooled to room temperature. The C-V shift is measured before and after heating for both bias conditions. The maximum permissible shift in threshold voltage is 0.4V with typical shifts running less than 0.15V.

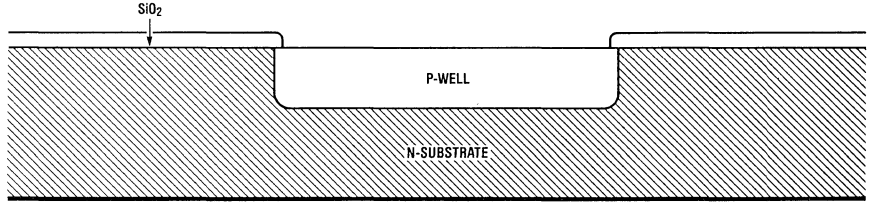
Moreover, National's CMOS devices have a double-input diode protection network designed to prevent catastrophic failures caused by positive or negative-going voltage transients. This effective input protection network, coupled with excellent oxide integrity, reduces the handling restrictions required on CMOS devices. A detailed guide to the handling requirements of CMOS parts is given in the last section of this report.

Figures 4 through 16 offer a pictorial representation of National's CMOS device fabrication. (Please note that the drawings are not to scale.)



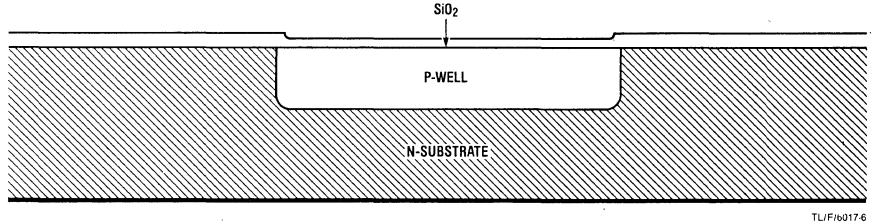
TL/F/6017-4

FIGURE 4. Initial Oxidation, Thermally Grown Silicon Dioxide Layer on Silicon Substrate Surface



TL/F/6017-5

FIGURE 5. P-Mask and Formation of P-Well Tub in which N-Channel Devices will be Located



TL/F/6017-6

FIGURE 6. P-Well Oxidation, Thermally Grown Silicon Dioxide Layer over P-Well Area

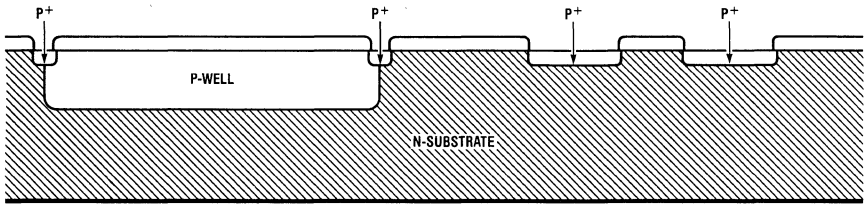


FIGURE 7. P^+ Mask and Formation of Low Resistance P^+ Type Pockets in P-Well and N-Substrate

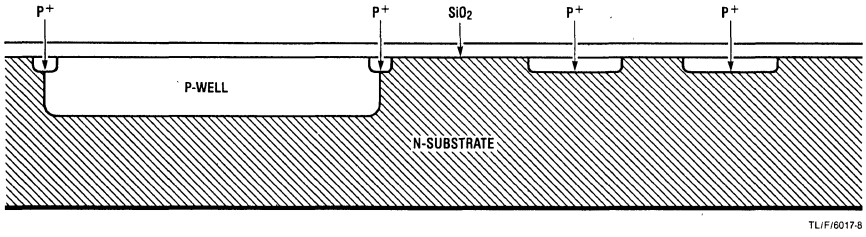


FIGURE 8. P^+ Oxidation, Thermally Grown Silicon Dioxide Layer over P^+ Type Pockets

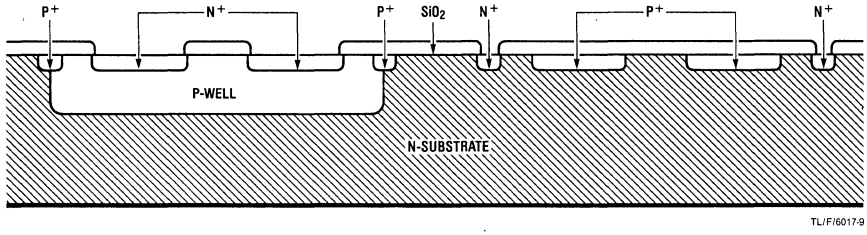


FIGURE 9. N^+ Mask and Formation of Low Resistance N^+ Type Pockets in P-Well and N-Substrate

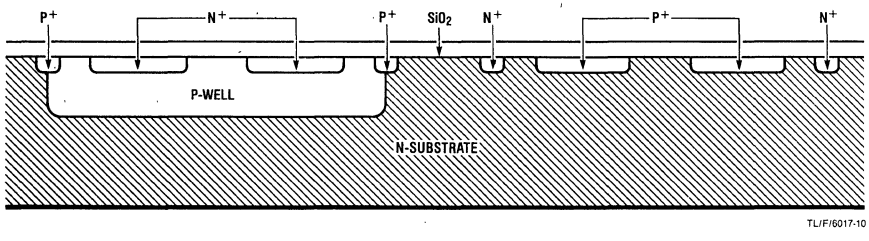


FIGURE 10. N^+ Oxidation, Thermally Grown Silicon Dioxide Layer over N^+ Type Pockets

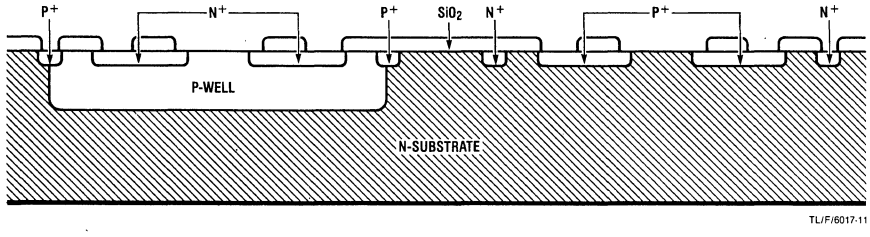


FIGURE 11. Composite Mask and Openings to N and P-Channel Devices

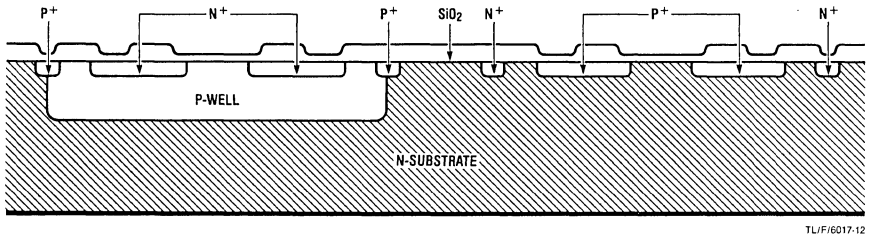


FIGURE 12. Gate Oxidation, Thermally Grown Silicon Dioxide Layer over N and P-Channel Devices

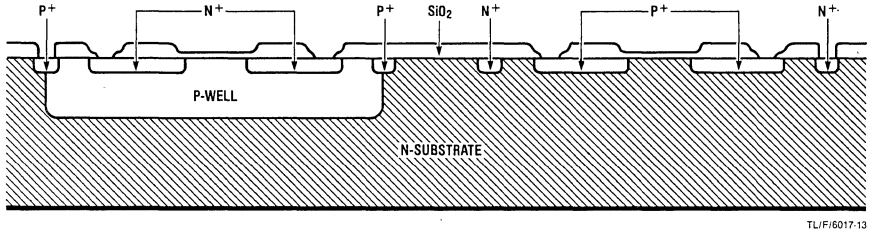


FIGURE 13. Contact Mask and Openings to N and P-Channel Devices

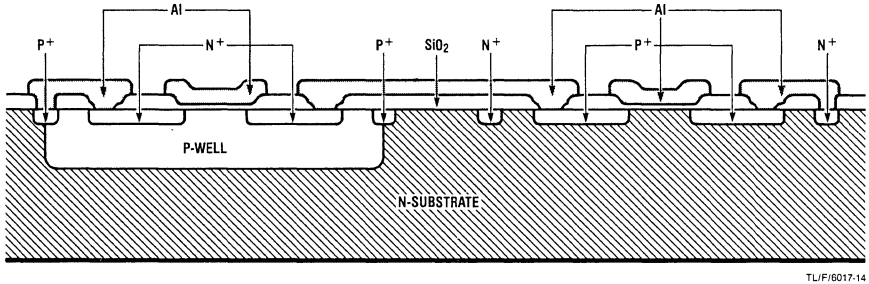


FIGURE 14. Metallization, Metal Mask, Resulting in Gate Metal and Metal Interconnects

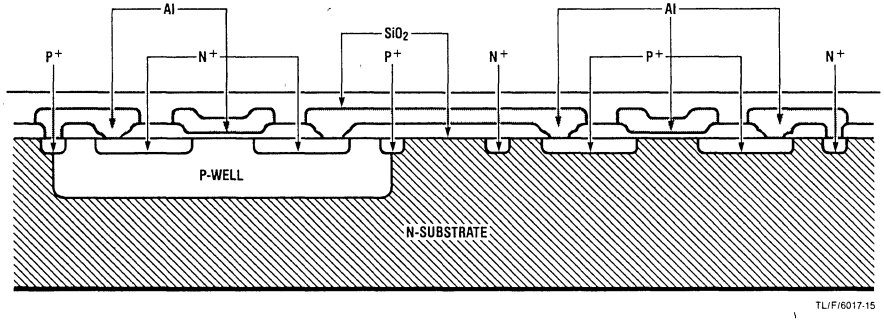
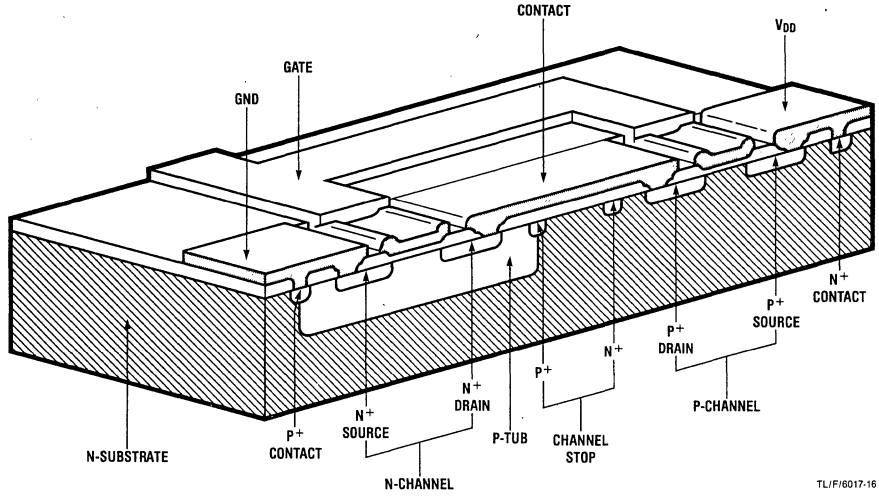


FIGURE 15. Passivation Vapox, Deposited Silicon Dioxide over Entire Die Surface



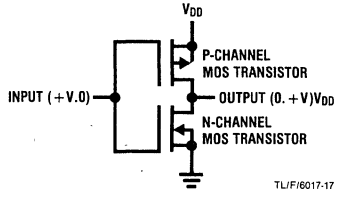
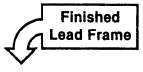


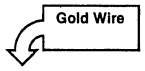
FIGURE 16. Basic CMOS Inverter Circuit

III. MOLDED PACKAGE PROCESSING FLOW CHART

1. **Sorted Wafers are Received**
   All dice on wafers have been 100% electronically tested. Electrical rejects are marked with an ink spot.
2. **100% Diamond Saw-Through, Plunge-Up Die Attach**
   Inked dice are removed.
3. **Optical Die Sort**
   100% optical microscope inspection at 100× to remove potentially unreliable dice.
4. **Quality Control Surveillance—First Check**
   Verification that the optical die sort was performed according to written specifications.

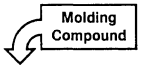


5. **Die Attach**
   Attachment of die to lead frame with a polymer.
6. **Quality Control Surveillance**
   Verification that the die attach operation was performed according to written specifications.



7. **Lead Bond**
   Thermosonic ball-bonding of gold wire to die and lead frame.

8. **Quality Control Surveillance**
   Several times each shift, samples are checked from each bonding machine and from each operator's work.
9. **Quality Assurance Lead Bond Pull Test**
   Samples by lot from each operator are checked a minimum of twice per shift. All bonds are pulled to destruction. The force required to break the bond, and the location of the break, are recorded for process-control purposes.
10. **Pre-Mold Optical Sort**
    100% optical microscope inspection at 30× for assembly defects. Devices are inspected for wafer processing anomalies, assembly work damage, completeness, and accuracy of assembly.
11. **Quality Control Surveillance**
    Samples of each optical sorter's work are inspected to criteria which meet or exceed the applicable requirements of MIL-STD-883B, Method 2010.



12. **Mold and Cure**
    Thermosetting plastic is transfer molded around the completed assembly. The plastic is then cured to insure mechanical and chemical stability.
13. **Trim and Form Leads**
    Frame supports are removed and leads formed to desired configuration.
14. **Quality Control Surveillance**
    Visual and mechanical quality are continuously monitored.
15. **Mark Package**
    Devices are marked with National's part number, a date code (signifying mold week), and the National logo.
16. **Clip Rails**
    Lead-frame rails are removed, leaving finished devices ready for test.
17. **Electrical Test**
    100% electrical test on all data sheet parameters.
18. **Quality Assurance Acceptance**
    Each lot of finished devices is sample inspected and tested by quality assurance inspectors for compliance with specifications.
19. **Pack and Ship**
    Each shipment is inspected by quality assurance to be sure that the right devices are going in the right quantity to the right customer.

IV. ENVIRONMENTAL AND LIFE TEST DATA OF CD4XXXC AND MM74CXXN

Accelerated Life Test

Testing at elevated temperatures is the principal method used to simulate long-term operation within a short period of time. This method is particularly useful because it provides a means of accelerating time-to-failure of temperature sensitive failure mechanisms. As a result, data are gathered for failure rate predictions at any operating field ambient.

Like all system hardware—mechanical, electrical, and electronic—the reliability of CMOS logic conforms to the well known "bathtub" curve, a plot failure rate versus time. As shown in *Figure 17*, the four concepts associated with this curve are infant mortality rate, useful life failure rate, useful life, and wearout failure rate.

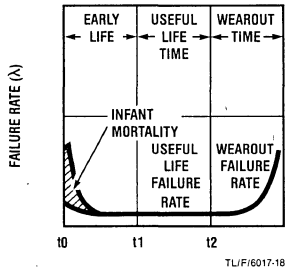


FIGURE 17. Reliability Life Curve

RELIABILITY REPORT

Infant Mortality: These are the devices that fail in the early life of the product, the period t0 to t1. Since the failure rate is decreasing rapidly during this period, and the period is short (dependent upon temperature), the infant mortality is expressed as the percentage of devices that fail from t0 to t1. The infant mortality portion of the curve is shaded because infant mortality is strongly influenced by numerous handling variables such as system-induced voltage transients, temperature, environment, mechanical stresses, etc., and therefore varies widely.

Useful Life Failure Rate: The percentage of devices that fail per-unit-time during the flat portion of the curve (t1 to t2), extending from the end of infant mortality to the onset of wearout. Usually expressed as percent per 1000 hours (sometimes per million hours or FITS), this statistic can also be stated as mean time between failure (MTBF), which is simply the reciprocal of the failure rate.

Useful Life: This is the period extending from the end of infant mortality to the onset of wearout, t1 to t2, at which point the failure rate begins to increase again. The useful life is usually expressed in hours. Although there is insufficient data to define a true useful life in most cases, the minimum life of a device usually suffices to assure adequate design margins. The useful life may be as short as several months but usually extends for decades if adequate design margins are applied. Temperature plays a major role in triggering the onset of wearout mechanisms; but other stresses, such as pressure, mechanical stress, thermal cycling and electrical loads, also play important roles.

Failure Mechanisms

As may be judged from the previous discussion, the failure mechanisms which occur in microcircuits are a function of application and device processing.

As shown in Table I, the main system stress factors contributing to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most infant failures resulting from these causes occur in three stress-producing phases:

1. device burn-in,
2. card assembly and handling,
3. initial system test and operation.

Although device burn-in can serve as an indicator of infant mortality, the carefully controlled burn-in tests seldom resemble the broad range of conditions (especially electrical noise) encountered in actual use. Field reliability data is therefore taken as the best source of infant mortality. This data is readily available and accurate.

TABLE I. Some Common Infant Mortality Failure Mechanisms

Failure Mechanism	Defect	Stress Factors
Oxide ruptures	Thin or defective oxide (masking and oxidation)	• System electrical noise • System power interruptions • Inductive loading
Open wire bonds	Assembly defects	• Ultrasonic exposure during card assembly • Excessive temperature
Lifted die bonds	Assembly defects	• Excessive temperature
Fused Die Metallization Shorts	Inadequate spacing between adjacent stripes	• System electrical noise • System power interruptions
Metallization opens	Inadequate stripe width and/or thickness (masking and evaporation)	• Inductive loading
Corrosion of wire bonds and/or die metallization	Seal leaks (defective encapsulation)	• Handling damage • Excessive solder heat during card assembly

Table II lists the activation energies for some common long-term failure mechanisms. All are essentially wearout mechanisms that have been discussed at length in the literature. The dramatic acceleration effect of temperature on these failure mechanisms is illustrated in *Figure 18*, which shows failure rate versus junction temperature for various activation energies. For instance, a mechanism with 0.99 eV activation energy is accelerated 800 times when junction temperature is increased from 50°C to 125°C. This means that a 1,000 hour life test at 125°C is equivalent to 800,000 hours operation at 50°C. If an increase in failure rate (onset of wearout) was not observed during the test, the 1,000 hour test would substantiate a minimum useful life greater than 90 years.

TABLE II. Common Wearout Failure Mechanisms

Failure Mechanism	Activation Energy
Electromigration in aluminum conductors (glassed, large grain)	1.2 eV
Intermetallic growth in gold/aluminum bond systems	0.99–1.04 eV
Wire and wire bond failures during thermal cycling	a fatigue mechanism
Slow trapping—charge injection	1.0–1.3 eV
Charge accumulation—mobile ions	1.0–1.35 eV

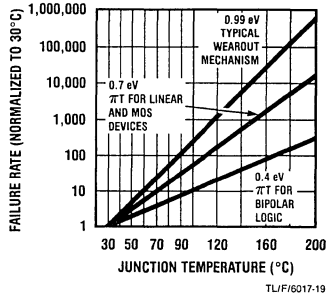


FIGURE 18. Failure Rate as a Function of Junction Temperature

Thermal Resistance—Its Impact on Microcircuit Reliability

Nearly all microcircuit failure mechanisms are accelerated by temperature, but the impact temperature has on accelerating a system failure is a direct function of the failure's thermal activation energy. Thus, the measure of the efficiency of the packaging-die system in removing heat from the active region is important in estimating how reliably that circuit will perform. The unit of measure to be used in estimating the active junction temperature of a microcircuit is its thermal resistance (θ_{JA}).

An exact measurement of the thermal resistance of microprocessors is not possible to obtain for most chips. Therefore, special test packages are commonly monitored to calculate typical package resistance values for reliability models. Acknowledging that the actual circuit thermal resistance is a function of many factors, it is nevertheless possible to presume certain general facts about thermal resistance and then apply them to our microcircuits. These facts are summarized in *Figure 19* for 14-lead packages.

In using the data in the tables, it is necessary to apply the equation:

$$T_J = P_D \times \theta_{JA} + T_A$$

where T_J is the circuit temperature at the active junction region and P_D is the average power consumed during circuit operation in the active junction region. θ_{JA} is the thermal resistance from the active junction region to the environment of the device's use system. At National Semiconductor, thermal resistance testing is done in still air, with either socket mount or a printed circuit board mounting. A generalized curve showing the effects of increasing air flow across the package is shown in *Figure 20*.

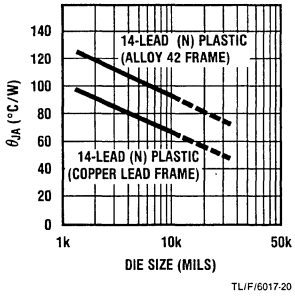


FIGURE 19. Typical Thermal Impedance (θ_{JA}) as a Function of Die Size

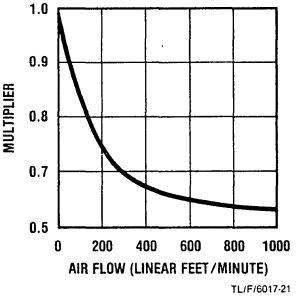


FIGURE 20. Graph Showing Typical Proportionate Decrease in Package Thermal Resistance as a Function of Chamber or System Air Flow

RELIABILITY REPORT

The Arrhenius Model

The time and temperature dependence of virtually all long-term semiconductor failure mechanisms is a well established fact. The occurrence of this failure dependency can be represented by the Arrhenius Model. This model includes the effect of temperature and activation energy of the failure mechanism, permitting it to be used to characterize failure modes and predict reliability at normal operating temperatures based on tests performed at above-normal device junction temperatures.

Originally developed in the 1880's to describe chemical reaction rates, the Arrhenius Model was adapted to accelerated life testing after researchers theorized that chemical processes were the primary cause of degradation of electronic parts. And, since temperature was commonly used in electronics accelerated testing, the Arrhenius Model was applied and found to fit the data. The model was subsequently a validated design tool and a useful adjunct to the state-of-the-art of accelerated life testing technology.

As applied to accelerated life testing of semiconductors, the Arrhenius Model assumes the following formula for defining the lifetime or MTBF at a given temperature stress level when the MTBF at a second temperature stress level is known. (See Equation 1.)

Equation 1:

$$t1 = t2 \exp \frac{E_a}{K} \left[\frac{1}{T1} - \frac{1}{T2}\right]$$

where: $t1$ = MTBF at junction temperature T1
$t2$ = MTBF at junction temperature T2
T = Junction temperature in °K
E_a = Thermal activation energy in electron volts (eV)
K = Boltzman's constant (8.617×10^{-5} eV/°K)

Acceleration Factor F

The acceleration factor F is the factor by which the failure rate can be acclerated by increased temperature. This factor can be readily derived by expressing the failure rate as the reciprocal of MTBF, then reducing the Arrhenius equation to the following form:

Equation 2:

$$\frac{\lambda 1}{\lambda 2} = F = \exp \frac{E_a}{K} \left[\frac{1}{T2} - \frac{1}{T1}\right]$$

where: F = Acceleration factor
$\lambda 1$ = Failure rate at junction temperature T1
$\lambda 2$ = Failure rate at junction temperature T2

Junction Temperature

In calculating the field reliability of a semiconductor device, it is first necessary to calculate the junction temperature both for the reliability test and for actual field operating conditions. In general, the junction temperature will depend on the ambient temperature, cooling, package type, operating cycle times, supply voltage and current. In these terms, the junction temperature, T_J, is given as:

Equation 3:

$$T_J = T_A + (I_{CC} \times V_{CC})(A_f)(\theta_{JA})$$

where: T_J = Junction temperature
T_A = Ambient temperature
I_{CC} = Supply current
V_{CC} = Supply voltage
A_f = Air flow factor (0.75)
θ_{JA} = Package thermal resistance

Activation Energy

Given the temperature and failure rate for a specific reliability test, the remaining unknown is the activation energy, E_a. To derive a simple formula for E, we take the natural log of the failure rate:

Equation 4:

$$\ln_1 - \ln_2 = \frac{E_a}{K} \left[\frac{1}{T1} - \frac{1}{T2}\right]$$

As the slope of the straight line resulting from Equation 4, the activation energy serves as a convenient means of characterizing the failure mechanisms. If the activation energy is known, or can be estimated, the acceleration factor can be determined, allowing field failure rate and useful life to be calculated from the accelerated life tests.

Application of Life Test Data

The life test data presented can be used to fully establish the reliability characteristics of National's CMOS logic products. Using the Arrhenius formulas, the acceleration factors can be calculated for any given operating junction temperature and used to determine failure versus time (the characteristic "bathtub" curve) or long-term failure rate.

Cumulative Total: 6/3,961
Total Device Hours: 3,961,000
Average Failure Rate at 125°C: 0.15%/1000 hours

A. Acceleration Factor at any Field Temperature

Example: Calculate failure rate at desired field temperature (T_f) of 45°C.

From Equation 2, Page 8-60:

$$\frac{\lambda 1}{\lambda 2} = F = \exp \frac{E_a}{K} \left[\frac{1}{T2} - \frac{1}{T1}\right]$$

Given: $E_a = 0.7$ eV
K = Boltzman's constant (8.614×10^{-5})
T = Absolute temperature in °K (C° + 273)

Calculating:

C°	K°	E_a/KT
45	318	$0.7 \text{ eV}/(8.617 \times 10^{-5} \text{ eV/°K})(318\text{°K}) = 25.54552$
125	398	$0.7 \text{ eV}/(8.617 \times 10^{-5} \text{ eV/°K})(398\text{°K}) = 20.41075$

Substituting:

$$\frac{E_a}{KT} = 25.54552 - 20.41075$$

$$\exp \frac{E_a}{KT} = 5.13477$$

$$F = 170$$

Therefore:

a. The acceleration factor between the temperature 45°C and 125°C with an activation energy of 0.7 eV is 170 times.
b. The projected failure rate at 45°C is thus: 0.15%/1000 hrs. ÷ 170 = 0.0009%/1000 hrs.

B. Calculating E_a from Experimental or Published Data.

Example: Calculate E_a used in Steady State Life, Method 1005.3, MIL-STD-883B, 4 Nov. 1980.

Let t1 = 125°C, t2 = 85°C.

From Equation 1, Page 8-60:

$$t1 = t2 \exp \frac{E_a}{K} \left[\frac{1}{T1} - \frac{1}{T2}\right]$$

Rearranging:

$$E_a = K \left[\frac{\ln t1 - \ln t2}{1/T1 - 1/T2}\right]$$

$t1 = 2 \times 10^4$ hrs. at 125°C
$t2 = 5 \times 10^5$ hrs. at 85°C

Therefore:

$$E_a = 8.617 \times 10^{-5} \text{ eV/°K} \quad \frac{\ln 2 \times 10^4 \text{ hrs.} - \ln 5 \times 10^5 \text{ hrs.}}{(0.0025125 \text{ °K}) - (0.0027933 \text{ °K})}$$

$\ln 2 \times 10^4 = 9.90349$
$\ln 5 \times 10^5 = 13.12236$

Substituting:

$$E_a = 8.617 \times 10^{-5} \text{ eV/°K} \left[\frac{9.90349 - 13.12236}{-2.808 \times 10^{-4} \text{ °K}}\right]$$

$= 0.99$ eV (or commonly used 1.0 eV)

Temperature and Humidity Bias Tests

The THB (temperature-humidity-bias) test is now the standard test for evaluating package and IC integrity. It uses above-normal stress levels to trigger within hours moisture-related failure mechanisms that would require years in the field. National Semiconductor runs the THB test at 85°C, 85% RH, and with maximum V_{DD} applied. When used with a valid life-acceleration model, this "85/85" test provides the following information:

1. Valid life acceleration factors.
2. Lifetime in operation or in storage.
3. Worst-case field failure rates.

Temperature and Humidity Acceleration Factors

Various models have been proposed for the THB tests, but the Peck and Zierdt model appears to be the most useful and valid. It provides independent temperature and humidity predictors and appears to be substantiated by work done by other investigators. This model has therefore been used to derive life acceleration factors for temperature and humidity. These are plotted in *Figures 21 and 22* with selected factors listed in *Figures 23 and 24.* In using these curves, all other variables must be kept constant, particularly bias voltage and power dissipation, since chip temperature and voltage gradient both have a first order effect on electrolysis rate. To allow these curves to be used with various levels of internal heating, *Figure 25* provides relative humidity correction for changes in chip temperature.

TABLE III. High Temperature Bias Reliability Test Results Continuous Operation at 15V, 125°C, 1000 Hours

Device	Rel Lot Number	Date Code	Sample Size	1000 Hrs.
MM4612B	E3046	8101	100	0
MM4613B	21025	8101	100	1 (Note 1)
MM4613B	E3051	8104	100	0
MM4611B	E3052	8105	100	0
MM74C901	12102/91179	8107	90	0
MM74C373	91178	8115	100	0
MM4625	91144	8121	83	0
MM4612	12101/91143	8121	100	0
MM4627	12099/91180	8124	100	0
MM4629	12100/91181	8124	100	0
MM4601B	71314	8137	90	0
MM74C902	11486	8143	94	0
MM74C924	71352	8145	126	0
MM4681B	71347	8145	231	0
MM4611B	71346	8145	231	0
MM74C04	11473	8146	75	0
MM74C04	72034	8201	240	3 (Note 1)
MM4613B	72047	8201	292	1 (Note 2)
MM74C02	92271	8202	80	0
MM74C02	92272	8206	80	0
MM4681B	72165	8220	90	0
MM4611B	72163	8220	90	0
MM4601B	72161	8220	90	0
MM4601B	72160	8220	90	0
MM4611B	72333	8225	90	0
MM4611B	72334	8225	90	0
MM4611B	72335	8225	90	0
MM4681B	72277	8228	120	0
MM74C04	72278	8228	150	1 (Note 1)
MM5613B	72279	8228	99	0
MM74C04N	72372	8250	90	0
MM5601BN	72373	8250	90	0
MM5611BN	72374	8250	90	0
MM5673BN	72375	8250	90	0
MM5681BN	72376	8250	90	0

Note 1: Parametric failure

Note 2: Gate oxide rupture

TABLE IV. Temperature—Humidity Bias Test Results
Continuous Operation at 15V, 85°C, 85% Rel. Hum., 1000 Hours

Device	Rel Lot Number	Date Code	Sample Size	1000 Hrs.
MM4612B	E3046	8101	100	0
MM4613B	21025	8101	75	2
MM4613B	E3051	8104	87	0
MM4611B	E3052	8105	100	0
MM74C901	12102/91179	8107	100	0
MM74C373	91178	8115	100	0
MM4625	91144	8121	100	0
MM4612	12101/91143	8121	100	0
MM4627	12099/91180	8124	100	1
MM4629	12100/91181	8124	100	0
MM4601B	71314	8137	90	2
MM74C902	11486	8143	94	0
MM4611B	71346	8145	231	1
MM4681B	71347	8145	231	0
MM74C04	11473	8146	75	0
MM74C04	72034	8201	300	1
MM4613B	72047	8201	340	2
MM74C02	92271	8202	80	1
MM74C02	92272	8206	80	0
MM4681B	72165	8220	90	0
MM4611B	72163	8220	90	1
MM4601B	72161	8220	90	0
MM4601B	72160	8220	90	0
MM5681BN	72277	8228	120	0
MM74C04N	72278	8228	150	0
MM5611BN	72333	8225	90	0
MM5611BN	72334	8225	90	2
MM5611BN	72335	8225	90	0
MM74C04N	72372	8250	120	0
MM5601BN	72373	8250	120	0
MM5611BN	72374	8250	120	0
MM5673BN	72375	8250	120	0

Cumulative Total: 13/3,863
Cumulative Percent Failures at 1000 Hrs: 0.336%

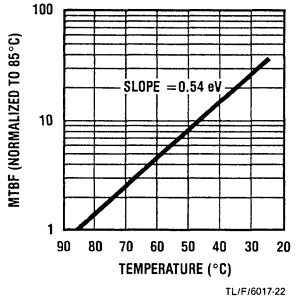


FIGURE 21. Corrosion Failure Rate vs Junction Temperature (Constant Relative Humidity)

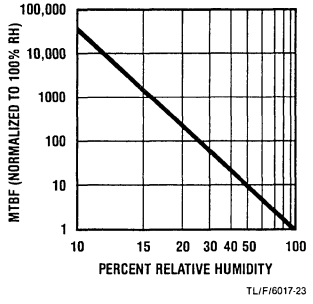


FIGURE 22. Corrosion Failure Rate vs Relative Humidity (Constant Temperature)

Temperature (°C)		Laboratory Acceleration
Field	Laboratory	
30	55	5×
55	85	5×
30	85	24×

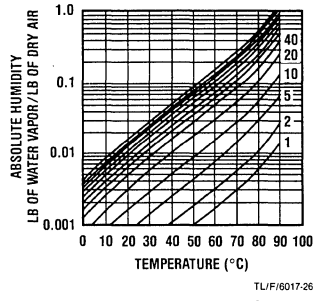
TL/F/6017-24

FIGURE 23. Humidity Acceleration Factors

Relative Humidity (%)		Laboratory Acceleration
Field	Laboratory	
65	85	3×
50	85	10×
20	85	700×
15	85	2,800×
12	85	6,000×

TL/F/6017-25

FIGURE 24. Temperature Acceleration Factors



TL/F/6017-26

FIGURE 25. Lines of Constant Percent Relative Humidity for Varying Temperature and Absolute Humidity

Worst-Case Acceleration Factors

Worst-case field conditions are encountered in the Gulf Coast states, where the typical mean daytime temperature is 30°C and the relative humidity is 65%. Using *Figures 21 through 24*, we can calculate the temperature and humidity acceleration factors. For a non-operating circuit, we can read directly from *Figures 22 and 23*. The temperature acceleration factor is $F_T = 25$, and the humidity acceleration factor is $F_H = 4$. The life acceleration factor is therefore: $F = 4 \times 25 = 100$. Hence, one hour of 85/85 testing is equivalent to 100 hours under worst-case field conditions (non-operating). Since the chip temperature increases when the device is operating, the relative humidity is reduced and the life acceleration factor is increased, resulting in improved reliability when the device is operating.

Biased Pressure Pot Test

Another commonly used test is the "pressure cooker" test. This test is usually performed with devices in an operating mode while being exposed to saturated steam (100% RH). The most common condition is 115°C. At saturation, this temperature corresponds to a water vapor pressure of 1489 mm Hg (28.8 psia). Due to its severity, this test is destructive to virtually all plastic packages. It creates failure mechanisms which would never be triggered at temperature and humidity extremes found in even the most severe application. For this reason, the test is limited to a relatively few number of hours, and results are interpreted on a purely qualitative, comparative basis.

TABLE V. Bias Pressure Pot Test Results
Continuous Operation at 15V, $T_A = 115°C$, Rel. Hum. = 100%, 192 Hours

Device	Rel Lot Number	Date Code	Sample Size	192 Hrs.
MM4601B	RBC72160	8220	59	1
MM4611B	RBC72163	8220	60	1
MM4681B	RBC72165	8220	58	0
MM4681B	RBC72277	8228	120	2
MM74C04N	RBC72372	8250	180	4
MM4601B	RBC72373	8250	100	1
MM4611B	RBC72374	8250	100	1
MM4681B	RBC72376	8250	100	0

V. ELECTROSTATIC SENSITIVITY OF NATIONAL'S INPUT PROTECTION NETWORK

Figure 26 shows a schematic of National's improved protection network employed. The network consists of two elements; three diodes connected to V_{SS} and two distributed diode resistors connected to V_{CC} (⏃). This V_{CC} resistor network will slow down incoming voltage transients and will also help dissipate some of the energy. Both sets of diodes will clamp an input spike and prevent large voltages (>35V) from appearing across the transistor. These diodes are larger than those used previously in metal gate CMOS to enable greater current shunting and make them less susceptible to damage. The input network is ringed by V_{CC} and ground diffusions which prevent substrate currents caused by transients from affecting other circuitry.

The inherent output diodes (⏃) that isolate the output transistor drains from the substrate are also important in preventing damage. They clamp large voltages that appear across the output pins. These diodes are also ringed by V_{CC} and ground diffusions to again shunt substrate currents and prevent damage to other parts of the circuit.

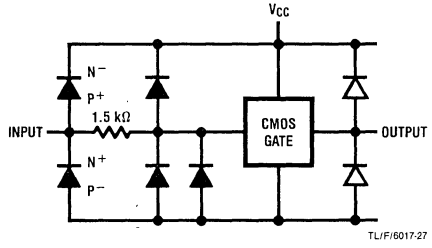
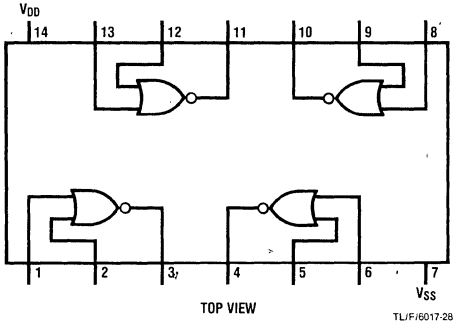


FIGURE 26. National's Improved Protection Network

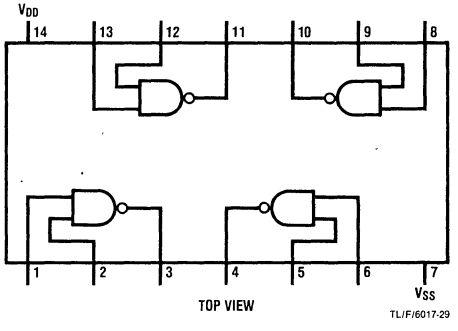
Five different CMOS logic devices were selected for high voltage (V_{ZAP}) testing; their logic functions and truth tables are shown in *Figures 27 through 31*.



TRUTH TABLE

Inputs		Output
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

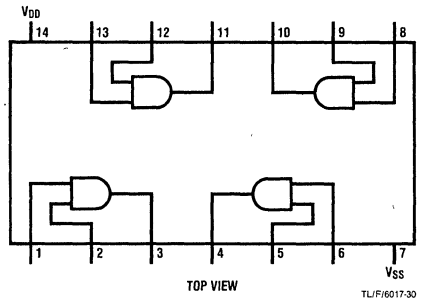
FIGURE 27. Logic Diagram and Truth Table for CD4001BM/CD4001BC, Quad 2-Input NOR Buffered B Series Gate



TRUTH TABLE

Inputs		Output
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

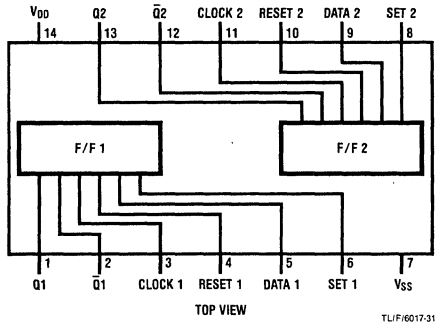
FIGURE 28. Logic Diagram and Truth Table for CD4011BM/CD4011BC, Quad 2-Input NAND Buffered B Series Gate



TRUTH TABLE

Inputs		Output
A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

FIGURE 29. Logic Diagram and Truth Table for CD4081BM/CD4081BC, Quad 2-Input and Buffered B Series Gate

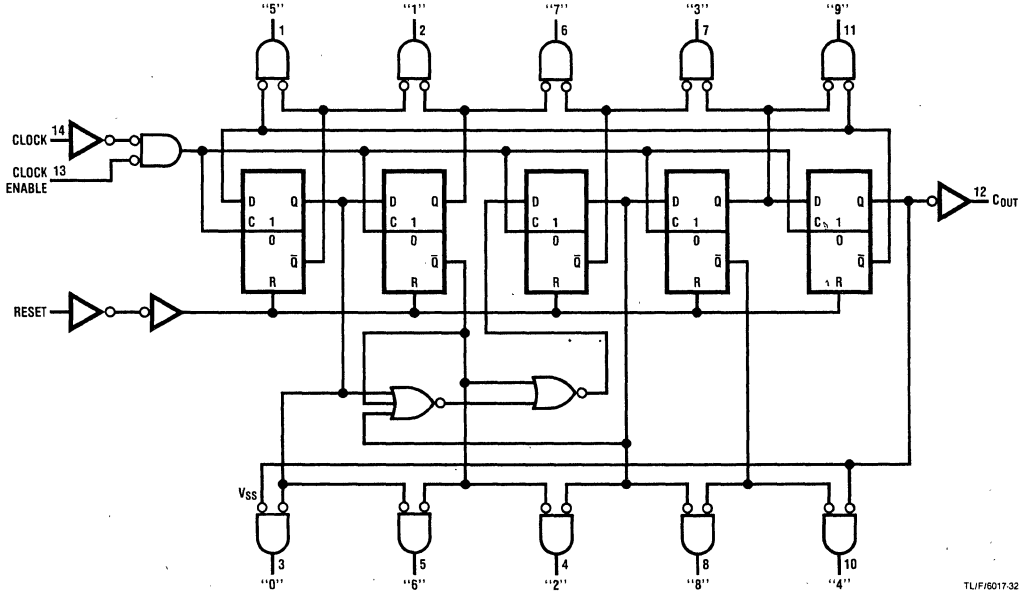


TRUTH TABLE

Inputs				Outputs	
CL†	D	R	S	Q	Q̄
	0	0	0	0	1
	1	0	0	1	0
	X	0	0	Q	Q̄
X	X	1	0	0	1
X	X	0	1	1	0
X	X	1	1	1	1

No change
† = Level change
X = Don't care case

FIGURE 30. Logic Diagram and Truth Table for CD4013BM/CD4013BC, Dual D Flip-Flop



Terminal No. 8 = GND
Terminal No. 16 = V_{DD}

FIGURE 31. Logic Diagram for CD4017BM/CD4017BC, Decode Counter/Divider with 10 Decoded Outputs

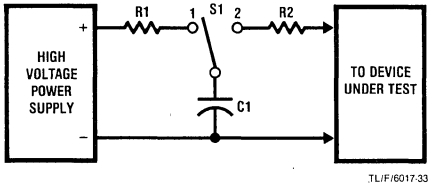
High voltage testing (V_{ZAP}) was conducted. Detail specifications applicable to aforementioned devices. This V_{ZAP} test is considered to represent an equivalent circuit describing the human body model and is shown in *Figure 32.*

Each input under test was subjected to a sequential V_{ZAP} according to Table VI. In addition, each input was subjected to high voltage testing six times (6 ×) for each condition. Ten (10) commercial samples of each device type were subjected to V_{ZAP}.

Input is same pin number in every mode. Output is associated output to input under test in applicable mode.

Testing was conducted by electrical testing for all DC and functional parameters at 25°C per published data specification limits, before and after V_{ZAP} testing. Results appear in Table VII.

National's improved input protection network makes it possible for its devices to withstand high voltage discharges without affecting their electrical performance.



R1 = 25 MΩ; represents protective charging resistance.
R2 = 1.5 kΩ; represents equivalent human body resistance.
C1 = 100 pF; represents equivalent human body capacitance.
S1 = Hg relay; means of transferring V_{ZAP} to device under test.
V_{ZAP} = 1000V, 2000V charge on C1.

FIGURE 32. Input Protection V_{ZAP} Test Conditions

TABLE VI. Sequential V_{ZAP} Test Modes

Mode	Positive Terminal	Negative Terminal
1	V_{DD}	Input
2	Input	V_{DD}
3	Input	V_{SS}
4	V_{SS}	Input
5	Output	Input
6	Input	Output

TABLE VII. V_{ZAP} Test Results

	1000V	2000V
Total Energy Discharge	50μ J	200μ J
CD4001BC	0/10	0/10
CD4011BC	0/10	0/10
CD4081BC	0/10	0/10
CD4013BC	0/10	0/10
CD4017BC	0/10	0/10

VI. HANDLING GUIDE FOR CMOS

Introduction

All CMOS low-threshold devices are susceptible to damage by the electrostatic discharge (ESD) of energy through the devices. Ths is because the gate oxide thickness of such devices is in the range of 1,000 Å to 1,100 Å, which limits the maximum voltage that can be applied (to the input of the device) to 80V with a reasonable safety factor. (For a fuller description of ESD and its possible latent effects on microcircuits, see National Semiconductor's Reliability Physics Brief, RPB-02, July 1978 and Reliability Physics Brief, RPB-07, January 1980.) Although all CMOS devices have input protection networks which are effective in a large number of device-handling situations, they are not effective in 100% of the cases (please refer to specific devices in National's 1984 CMOS Databook).

In order to be totally safe, proper handling procedures must be used to eliminate damage and subsequent yield loss caused by static electrical charges. It is the purpose of this application guide to outline proper handling procedures for CMOS devices.

CMOS Latch-up Free Operation

Latch-up is a common problem encountered by first time users of CMOS logic components. However, if some fundamental precautions are taken, latch-up free system operation can be easily achieved.

Typical CMOS structures have many adjacent closely spaced junction diffusions, which under normal operation, will be reversed-biased. *Figure 33* shows the cross section of two CMOS FETs showing the parasitic transistors connected as a PNPN SCR (silicon controlled rectifier). If one or more of the PN junctions becomes forward-biased, the SCR will be triggered and the result appears to be a short between V_{DD} and V_{SS}. This "latch-up" will continue until power is removed or the device is burned up.

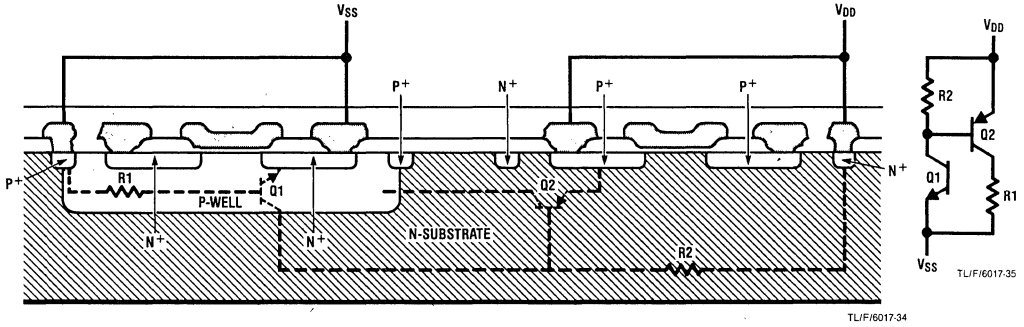


FIGURE 33. A Cross Section of Two CMOS FETs Showing the Parasitic Transistors and Equivalent Circuit

The most common way that these parasitics come into play is to cause an input or output junction to become forward-biased. The voltage required to activate the parasitic SCR decreases as operating temperature increases and is between 0.4V and 0.5V at 125°C. This undesired forward-biasing can be caused by noise on V_{DD} and V_{SS} lines, or noise on the input/output signals, or from a combination of power supply and signal noise.

Latch-up free operation can be achieved by maintaining all input and output levels within a range of $-0.3V$ minimum and $V_{DD} + +0.3V$ maximum. The following precautions will ensure this.

1. V_{DD} and V_{SS} should be applied before any input or output signal is applied.
2. V_{DD} and V_{SS} noise must be minimized through adequate capacitive decoupling, power supply regulation, and good board layout with respect to power distribution. Ground (V_{SS}) differences must be controlled to keep input and output signals from violating the $V_{SS} - 0.3V$ minimum.
3. Signal overshoot (and undershoot) should be controlled to stay within the stated min-max range (transients of 1V for 50 ns can cause latch-up with some device types).

General Handling Procedures

1. The leads of CMOS devices must be in contact with conductive material to avoid build-up of static charge. Containers used for transporting or storing CMOS components should be made of such material or lined with antistatic protection. Rails for handling and shipping MOS devices must be made of electrically conductive material or be made static-free by an appropriate surface coating. In no case will CMOS devices be inserted into polystyrene foam or other high dielectric materials. Any surface coating which is not at ground potential must not come in direct contact with device pins.
2. Devices must be packed in conductive containers, rails or envelopes for storing. In addition, devices must be kept at ground potential and should never come in contact with nonconductive plastics.
3. All electrical equipment must be hard-wired to ground. Soldering iron tips, metal parts of fixtures and tools, and all handling systems must be grounded.

Cleaning

1. Devices should be cleaned by a solvent which will assure complete removal of foreign matter, flux, residual matter, etc., from the exterior of the package.
2. A static neutralizing ion blower should be used when manually cleaning devices or subassemblies with brushes.
3. All automatic cleaning should be grounded.
4. All cleaning baskets should be grounded.

Assembly

1. Subassembly modules and printed circuit boards should be manufactured and handled using the same procedures as those described above for individual CMOS devices.
2. CMOS parts should be the last to be inserted into printed circuit boards or systems so as to avoid overhandling.
3. Circuit boards containing CMOS devices which are being transported between work stations and test areas should be contained in antistatic material or have all board terminals shorted together using a conductive shorting bar. Only handling trays of conductive material should be used.
4. All automatic insertion equipment, solder machines, metallic parts of conveyor systems, and soldering irons should be grounded.

Note: These precautions should be taken until the subassembly is inserted into the complete system in which the proper voltages are applied. Subassemblies should never be constructed, fixtured, stored, or transported in polystyrene or any other highly dielectric materials.

General Operating Procedures

The National CMOS product line is comprised of many different device types for a variety of applications. The following operating procedures apply in a general sense to all CMOS devices, but reference to device specification sheets is still necessary to assure correct operating values.

A. Before making any physical connections or applying any external signal sources, be sure that all power supplies are off. Be sure, also, to observe proper static ground conditions.

B. Power supplies should be turned up slowly to the necessary voltages so as to avoid rapid supply changes.

C. After power supplies have been turned on, apply external input signals.

Note: Failure to perform the power-on procedure in this order can result in damage to CMOS circuitry.

D. To power down, remove input signals, then turn power supplies off slowly.

E. If CMOS devices are operated at an elevated environmental temperature, allow devices to reach room temperature before they are powered down.

F. Do not leave inputs to any CMOS device unused. For NAND gates, the unused inputs should be tied to V_{DD}; unused inputs or NOR gates should be tied to ground.

Testing

1. Use grounded metallic fixtures where possible. Any surface that is not at ground potential should not come into direct contact with device pins.
2. Use a static-neutralizing ion air blower when running automatic handlers. Use conductive handling trays when transferring devices.
3. Do not insert devices or boards with power turned on.
4. Ensure that AC signals do not cause excessive current leakage.

Electrical Failure Modes Caused by Improper Handling

If proper handling tachniques are not followed, the generation of static electrical discharges may damage the CMOS devices, resulting in inoperable or degraded parts. Typical failure modes are:

a. shorted or open gates

b. shorted input protection diodes

c. open metal paths in the device input circuitry

d. degraded device characteristics

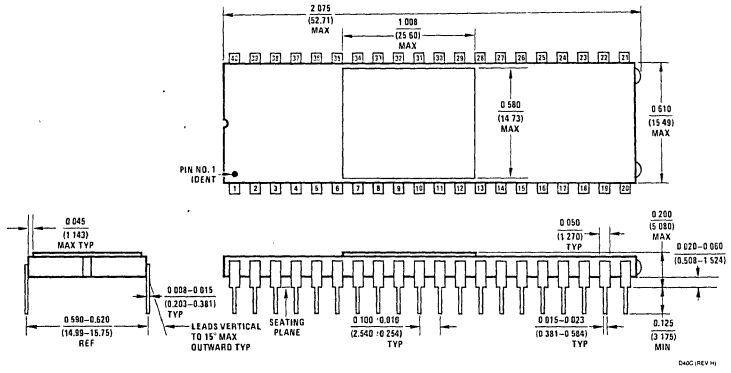
The presence of these failure modes can be detected easily using a transistor curve tracer.

REFERENCES

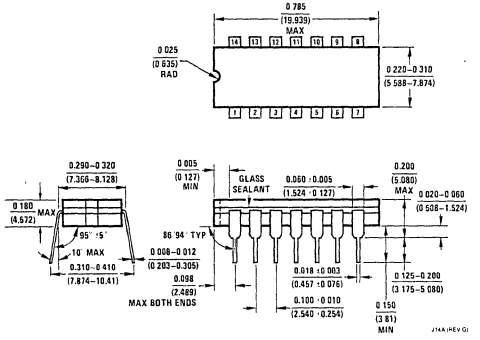
D. S. Peck and C. H. Zierdt, Jr.; *"Temperature-Humidity Acceleration of Metal-Electrolysis Failure in Semiconductor Devices";* 11th Annual Reliability Physics Symposium, Las Vegas, Nevada, April 1973.

R. W. Lawson; *"The Accelerated Testing of Plastic Encapsulated Semiconductor Components";* 12th Annual Reliability Physics Symposium, Las Vegas, Nevada, April 1974.

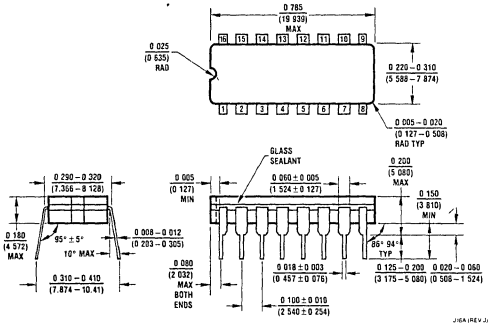
H. Koelmans; *"Metallization Corrosion in Silicon Devices by Moisture-Induced Electrolysis";* 12th Annual Reliability Physics Symposium, Las Vegas, Nevada, April 1974.



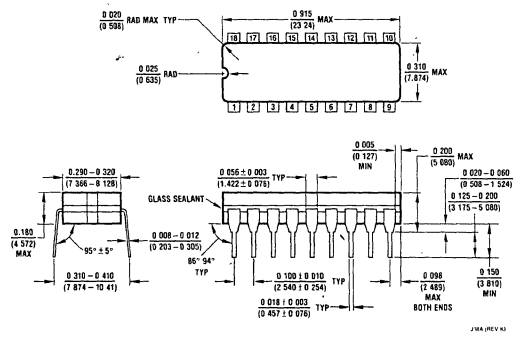
40-Lead Hermetic DIP (D)
NS Package Number D40C



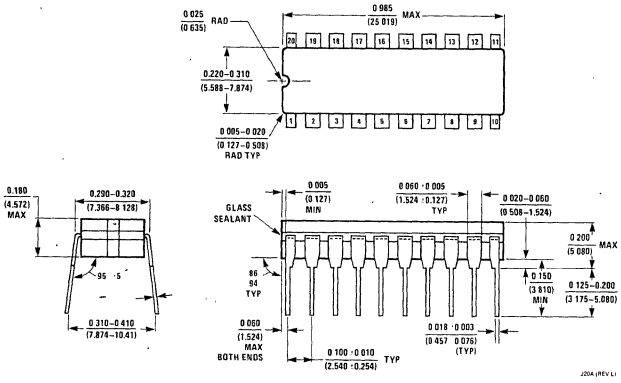
14-Lead CERDIP (J)
NS Package Number J14A



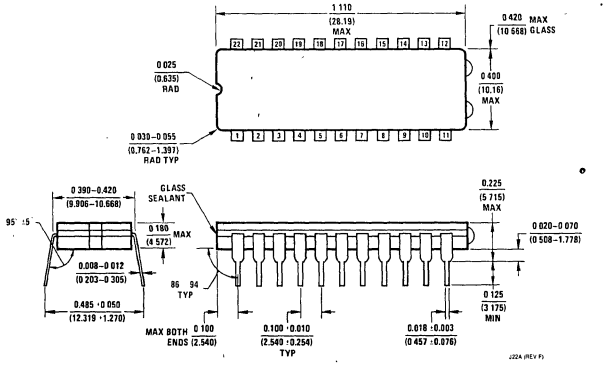
16-Lead CERDIP (J)
NS Package Number J16A



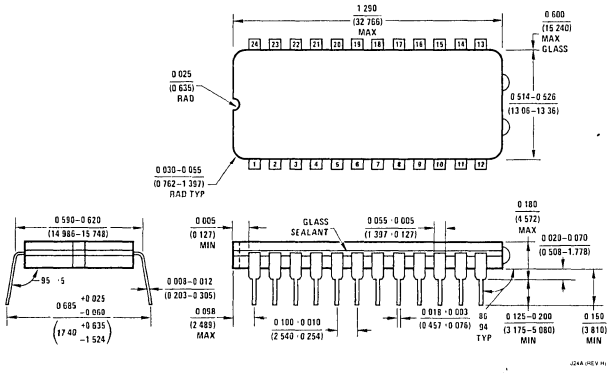
18-Lead CERDIP (J)
NS Package Number J18A



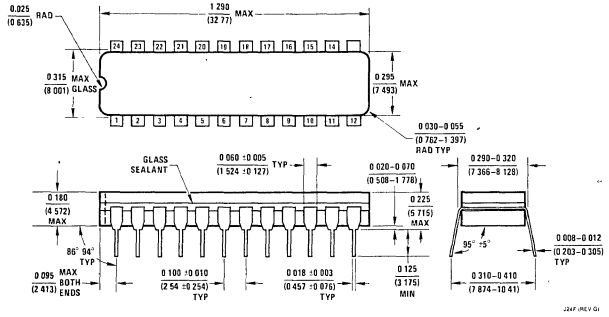
20-Lead CERDIP (J)
NS Package Number J20A



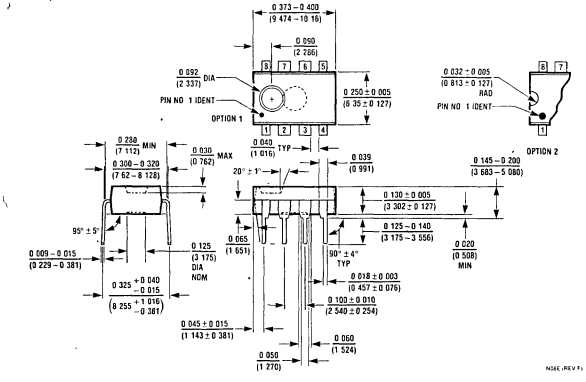
22-Lead CERDIP (J)
NS Package Number J22A



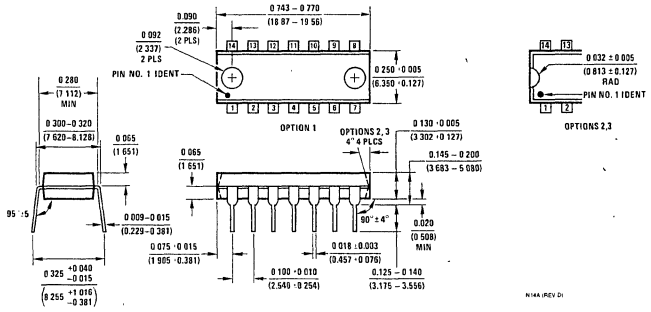
24-Lead CERDIP (J)
NS Package Number J24A



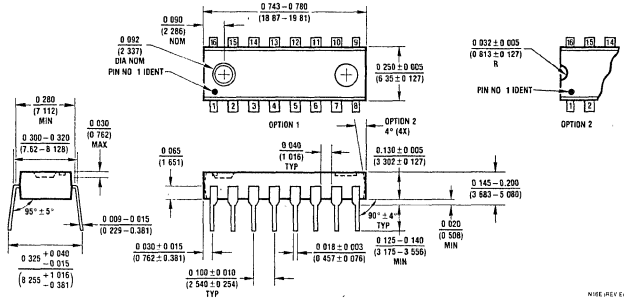
24-Lead CERDIP (J)
0.300 Centers
NS Package Number J24F



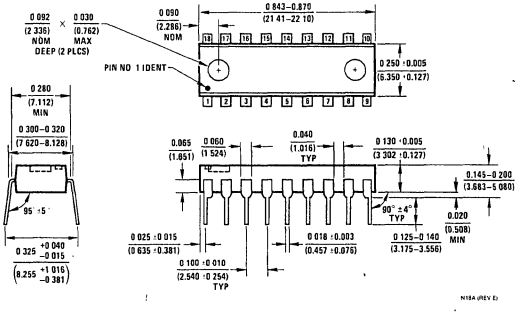
8-Lead Molded DIP (N)
NS Package Number N08E



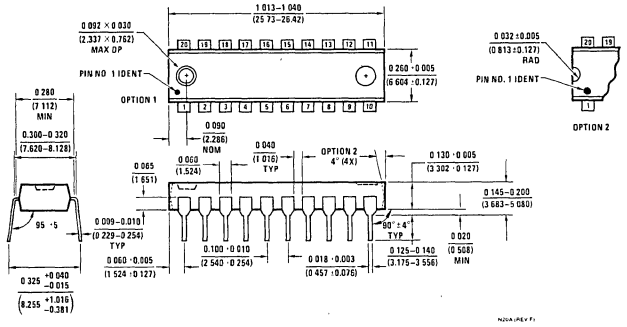
14-Lead Molded DIP (N)
NS Package Number N14A



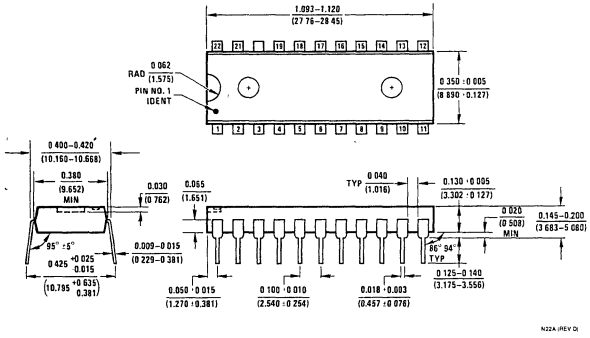
16-Lead Molded DIP (N)
NS Package Number N16E



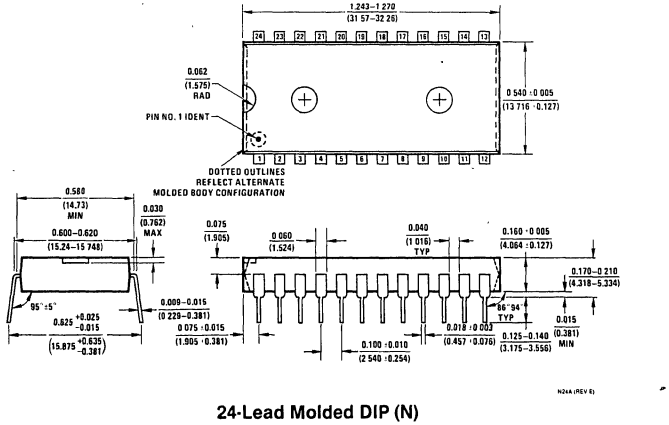
18-Lead Molded DIP (N)
NS Package Number N18A



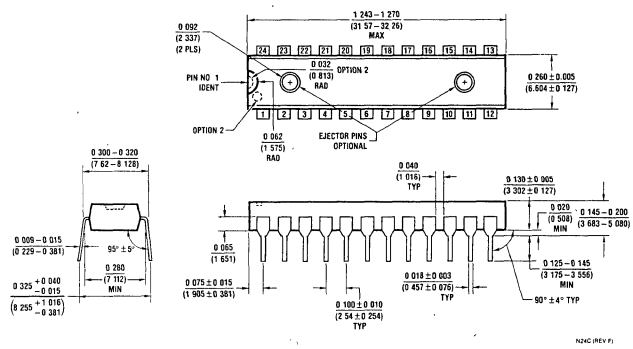
20-Lead Molded DIP (N)
NS Package Number N20A



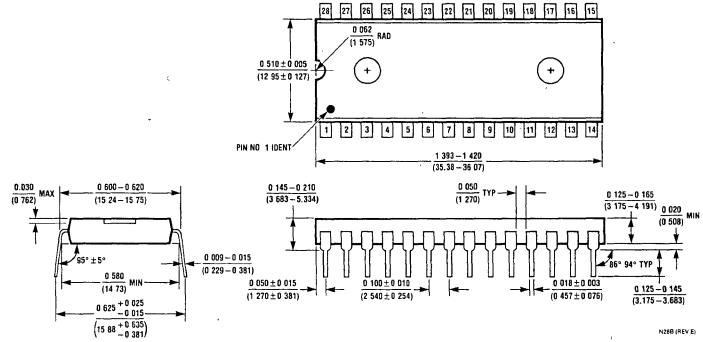
22-Lead Molded DIP (N)
NS Package Number N22A



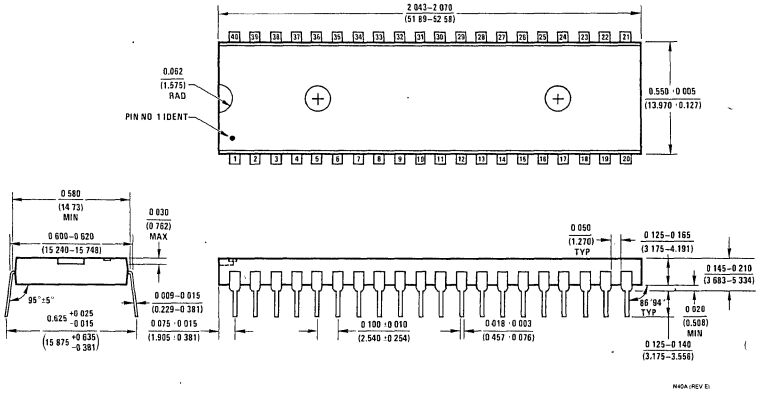
24-Lead Molded DIP (N)
NS Package Number N24A



24-Lead Skinny DIP (SD)
0.300 Centers Molded DIP (N)
NS Package Number N24C



28-Lead Molded DIP (N)
NS Package Number N28B



40-Lead Molded DIP (N)
NS Package Number N40A

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel: (408) 721-5000
TWX: (910) 339-9240

Electronica NSC de Mexico SA
Juventino Rosas No. 118-2
Col Guadalupe Inn
Mexico, 01020 D.F. Mexico
Tel: (905) 524-9402

National Semicondutores Do Brasil Ltda.
8 Andar
01452 Sao Paulo, SP. Brasil
Tel: (55/11) 212-5066
Telex: 391-1131931 NSBR BR

National Semiconductor GmbH
Furstenriederstrasse Nr. 5
D-8000 Munchen 21
West Germany
Tel: (089) 5 60 12-0
Telex: 522772

National Semiconductor (UK) Ltd.
301 Harpur Centre
Horne Lane
Bedford MK40 1TR
United Kingdom
Tel: 0234-47147
Telex: 826 209

National Semiconductor Benelux
Ave Charles Quint 545
B-1080 Bruxelles
Belgium
Tel: (02) 4661807
Telex: 61007

National Semiconductor (UK) Ltd.
1, Bianco Lunos Alle
DK-1868 Copenhagen V
Denmark
Tel: (01) 213211
Telex: 15179

National Semiconductor
Expansion 10000
28, Rue de la Redoute
F-92 260 Fontenay-aux-Roses
France
Tel: (01) 660-8140
Telex: 250956

National Semiconductor S.p.A.
Via Solferino 19
20121 Milano
Italy
Tel: (02) 345-2046/7/8/9
Telex: 332835

National Semiconductor AB
Box 2016
Stensatravagen 4/11 TR
S-12702 Skarholmen
Sweden
Tel: (08) 970190
Telex: 10731

National Semiconductor
Calle Nunez Morgado 9
(Esc. Dcha. 1-A)
E-Madrid 16
Spain
Tel: (01) 733-2954/733-2958
Telex: 46133

National Semiconductor Switzerland
Alte Winterthurerstrasse 53
Postfach 567
CH-8304 Wallisellen-Zurich
Tel: (01) 830-2727
Telex: 59000

National Semiconductor
Pasilanraitio 6C
SF-00240 Helsinki 24
Finland
Tel: (90) 14 03 44
Telex: 124854

NS Japan Ltd.
4-403 Ikebukuro, Toshima-ku
Tokyo 171, Japan
Tel: (03) 988-2131
Fax: 011-81-3-988-1700

N. S. H. K. Ltd.
S. E. Asia Mktg. N. H. K. Sales
Austin Tower, 4th Floor
22-26 Austin Avenue
Tsimshatsui, Kowloon,
Hong Kong
Tel: 3-7231290, 3-7243645
Cable: NSSEAMKTG
Telex: 52996 NSSEA HX

National Semiconductor (Australia) PTY, Ltd.
Cnr. Stud Rd. & Mtn. Highway
Bayswater, Victoria 3153
Australia
Tel: (03) 729-6333
Telex: AA32096

National Semiconductor (PTE), Ltd.
10th Floor
Pub Building, Devonshire Wing
Somerset Road
Singapore 0923
Tel: 652700047
Telex: NAT SEMI RS 21402

National Semiconductor (Far East) Ltd.
Taiwan Branch
P.O. Box 68-332 Taipei
7th Floor, Nan Shan Life Bldg.,
302 Min Chuan East Road,
Taipei, Taiwan R.O.C.
Tel: (02) 501-7227
Telex: 22837 NSTW
Cable: NSTW TAIPEI

National Semiconductor (HK) Ltd.
Korea Liaison Office
6th Floor, Kunwon Bldg.
2-1 GA Mookjung-Dong
Choong-Ku, Seoul, Korea
C.P.O. Box 7941 Seoul, Korea
Tel: 267-9473
Telex: K24942