1984
MOS MEMORY
DATABOOK

NATIONAL
SEMICONDUCTOR
CORPORATION

A Corporate Dedication to Quality and Reliability

National Semiconductor is an industry leader in the manufacture of high quality, high reliability integrated circuits. We have been the leading proponent of driving down IC defects and extending product lifetimes. From raw material through product design, manufacturing and shipping, our quality and reliability is second to none.

We are proud of our success...it sets a standard for others to achieve. Yet, our quest for perfection is ongoing so that you, our customer, can continue to rely on National Semiconductor Corporation to produce high quality products for your systems.

Charles E. Sporck
President,Chief Executive Officer
National Semiconductor Corporation

Wir fühlen uns zu Qualität und Zuverlässigkeit verpflichtet

National Semiconductor Corporation ist führend bei der Harstellung von integrierten Schaltungen hoher Qualität und hoher Zuverlässigkeit. National Semiconductor war schon immer Vorreiter, wenn es galt, die Zahl von IC Ausfällen zu verringern und die Lebensdauern von Produkten zu verbessern. Vom Rohmaterial Uber Entwurf und Herstellung bis zur Auslieferung, die Qualität und die Zuverlässigkeit per Produkte von National Semiconductor sind unübertroffen.

Wir sind stolz auf unseren Erfolg, der Standards setzt, die für andere erstrebenswert sind. Auch ihre Ansprüche steigen ständig, Sie als unser Kunde können sich auch weiterhin auf National Semiconductor verlassen.

La Qualité et La Fiabilité:

Une Vocation Commune Chez National Semiconductor Corporation

National Semiconductor Corporation c'est l'un des leaders industriels qui fabrique des circuits intégrés d'une très grande qualité et d'une fiabilité exceptionnelle. National a été le premier à vouloir faire chuter le nombre de circuits intégrés defectueux et a augmenter la durée de vie des produits. Depuis les matières premières, en passant par la conception du produit sa fabrication et son expédition, partout la qualité et la fiabilité chez National sont sans équivalents.

Nous sommes fiers de notre succès et le standard ainsi défini devrait devenir l'objectif à atteindre par les autres sociétés. Et nous continuons à vouloir faire progresser notre recherche de la perfection; il en résulte que vous, qui êtes notre client, pouvez toujours faire confiance à National Semiconductor Corporation, en produisant des systèmes d'une très grande qualité standard.

Un Impegno Societario di Qualità e Affidabilità

National Semiconductor Corporation è un'industria al vertice nella costruzione di circuiti integrati di altà qualità ed affidabilità. National è stata il principale promotore per l'abbattimento della difettosità dei circuiti integrati e per l'allungamento della vita dei prodotti. Dal materiale grezzo attraverso tutte le fasi di progettazione, costruzione e spedizione, la qualità e affidabilità National non è seconda a nessuno.

Noi siamo orgogliosi del nostro successo che fissa per gli altri un traguardo da raggiungere. Il nostro desiderio di perfezione è d'altra parte illimitato e pertanto tu, nostro cliente, puoi continuare ad affidarti a National Semiconductor Corporation per la produzione dei tuoi sistemi con elevati livelli di qualità.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

MOS MEMORY DATABOOK

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COPS™ microcontrollers
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DIB™
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GENIX™
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ISE™
INFOCHEX™
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MICRO-DAC™
μtalker™
Microtalker™
MICROWIRE™
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MOLE™
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NSC800™
NS16000™
NSX-16™
NSCX-16™
NURAM™
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Perfect Watch™
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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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MOS MEMORY DATABOOK

INTRODUCTION

National Semiconductor Corporation's MOS Memory Databook is a comprehensive collection of information on advanced, high-density memory products covering the spectrum of this mainstream semiconductor component category.

Virtually every electronic system being designed today requires some level of storage capacity. National is committed to designing and supplying high-performance memory products ranging from state-of-the-art dynamic RAMs to programmable non-volatile EPROMs and EEPROMs which are currently finding increasing usage in a wide range of microprocessor-based systems.

National Semiconductor has an array of advanced technology processes to apply to memory design and development. These range from our high-density triple-poly process used in the most advanced RAMs, to our small-geometry, silicon-gate, oxide-isolated microCMOS technology which is now being applied to high-performance memory devices for the first time.

National is committed to technical excellence in design, manufacturing, reliability and service to our customers through the continuing development of new devices. If you don't find the memory products you need in this book, please contact your local National Semiconductor sales office or distributor.

National is also committed to providing the most complete, up-to-date information available on its entire product line, and has accomplished this with its master databook program. This program, of which the MOS Memory Databook is a part, provides one master databook for each product family with periodic supplements designed to keep you abreast of all new and revised information. We are confident that this program will serve your information needs well in the quickly changing world of technology.

DATABOOK MEMOIRES MOS

INTRODUCTION

Le Databook Mémoires MOS édité par National Semiconductor Corporation est un recueil détaillé et complet d'informations portant sur les circuits mémoires de pointe à haute densité, couvrant tout le spectre de cette importante catégorie de composants semiconducteurs.

Pratiquement tout système électronique conçu aujourd'hui nécessite quelquepart un moyen de mémorisation. National s'est engagé à concevoir et à produire des produits mémoires très performants qui vont depuis les RAMs dynamiques nec plus ultra jusqu'aux EPROMs et EEPROMs programmables non volatiles, qui sont actuellement de plus en plus utilisées dans une vaste gamme de systèmes à microprocesseurs.

National Semiconductor dispose d'un ensemble de technologies de pointe pour concevoir et développer ses mémoires. Cet ensemble va de notre technologies haute densité triple-poly utilitsée dans la plupart des RAMs de pointe, à notre technologie microCMOS, à isolation d'oxyde, porte au silicium et petite gédmétrie maintenant mise en oeuvre dans les circuits mémoires à hautes performances, ou la première fois.

National s'est engagé à fournir une qualité technique irréprochable à ses clients, en ce qui concerne la conception, la fabrication, la fiabilité et le service, et ceci tout au long au développement des nos nouveaux circuits. Si vous ne trouvez pas dans cet ouvrage le produit mémoire dont vous avez besoin, veuillez contacter s'il vous plait votre ingénieur commercial National Semiconductor ou votre distributeur le plus proche.

National s'est aussi engagé à fournir l'information la plus compléte et la plus à-jour qui soit; sur toute sa gamme de produits. C'est ce que National vient de faire avec la sortie de son nouveau programme de Databook. Ce programme, dont ce Databook Mémoires MOS fait partie, comprend un Databook pour chaque famille de produits ainsi que des mises à jour périodiques destinées à vous informer de toutes les nouveautés ou révisions. Nous sommes certains que ce programme vous apportera toutes les informations dont vous avez besoin dans ce monde technologique qui change aussi rapidement.

MEMORY DATABOOK

Il catalogo "Memorie MOS" della National Semiconductor è una raccolta di informazioni sui prodotti più avanzati ed ad alta densità in uno dei seitori più importanti dei componenti elettronici.

Teoricamente, ogni sistema elettronico, progettato oggi richiede una certa capacità di memorizzazione la National è impesanta nel progrettare e produrre memorie ad elevate prestazioni: dalle memorie "RAM" dinamiche alle memorie non volatili programmabili quali "EPROM" ed ancora a quelle programmabili e cancellabili elettroicamente "EEPROM" che stanno suscitan do un crescente interesse per applicazioni con i microprocessori.

La National Semiconductor possiede un gran numero di processi tecnologici utilizzabili nella fabbricazione di dispositivi di memoria. Fra i processi più interessanti è da notare quello "Triple-poly" ad alta densità per le più avanzate memorie "RAM" di namiche ed il processo micro-CMOS con geometrie ridottissime. Silicone-gate con isolamento ad ossido. Utilizzato dalla National per la prima volta nella fabbricazione di memorie ad elevate prestazioni.

La National Semiconductor, grazie allo sviluppo continuo di nuovi prodotti si è indirizzata verso la ricerca di altre tecnologie di progetto. Tecniche di fabbricazione specializzate ad alta affidabilita. Tutto per offrire il migliore servizio ai clienti. Se non trovate in questo catalogo il prodotto che vi interessa, non esitate a contattare gli uffici vendite della National Semiconductor od il vostro Distributore.

La National è impegnata a fornire le informazioni più complete e più aggiornate oirca tutti i suoi prodotti; per ciò sta implementando un programma detto "MASTER DATABOOK PROGRAM". Con questo programma, di oui il manuale della Memorie MOS fa parte, viene fornito un volume principale (Master Databook) per ciacuna famiglia di prodotto oltre a supplementi periodici che contengono tutte le informazioni più recenti riguardo ai prodotti. Noi crediamo che con questo programma saremo in grado id darvi tutte le informazione necessarie aggiornando le stesse con la stessa rapidità con cui evolve il mondo tecnologico.

MOS-Speicher-Datenbuch

EINLEITUNG

Das MOS-Speicher-Datenbuch von National Semiconductor ist eine umfangreiche Sammlung von Informationen über fortschrittliche Speicherprodukte hoher Scheltungedichte. Es wird gesamte Spektrum dieser wichtigen Halbleiter-Bauelemente-Kategorie abgedeckt.

Praktisch jedes System, des heute entwickelt wird, beötigt eine gewisse Speicherkepazität. National Semiconductor entwickelt und fertigt Hochleistungs-Speicherbauelemente. Des Typenspektrum reicht vom modernen dynamischen RAM bis zu programmierbaren nichtflüchtigen EPROMs und EEPROMs, die derzeit immer mehr Anwendungen in einem weiten Spektrum von Microprozessorsystemen finden.

National Semiconductor verfügt über ein weites Spektrum an Herstellungsverfahren modernster Art, die bei der Entwicklung und Fertigung von Speichern angewendet werden. Diesen reichen vom Triple-Poly-Prozeß hoher Dichte, der bei den meisten modernen RAMs verwendet wird, bis zur oxidisolierten Silizium-Gate-microCMOS-Technologie mit ihren kleinen Geometrien, die derzeit erstmals bei Hochleistungs-Speicherbauelementen Verwendung findet.

National Semiconductor fühlt sich zu höchster technischer Perfektion bei Entwicklung, Herstellung, Zuverlässigkeit und Kunden-Service verpflichtet. Dies kommt in der kontinuierlichen Entwicklung immer neuer Bauelemente zum Ausdruk. Sollten Sie das von Ihnen benötigte Bauelemente nicht in diesem Datenbuch finden, fragen Sie doch bitte den für Sie zuständigen National-Semiconductor-Distributor oder das nächste Verkaufsbüro.

National Semiconductor möchte Ihnen die vollständigsten und aktuellsten Informationen über alle Produkte zugänglich machen. Dafür wurde das neue Datenbuch-Programm zusammengestellt. Diesen Programm, zu dem auch das MOS-Speicher-Datenbuch gehört, besteht aus jeweils einem Haupt-Datenbuch ("Master Databook") für eine Produktfamilie, das mit periodisch erscheinenden Ergänzungsbänden aktualisiert wird. Damit steht Ihnen die jeweils neueste Produktinformation zur Verfügung. Wir glauben, daß wir auf diese Weise Ihrem Informationsbedürfnis übr die sich schnell ändernde Technologie am besten gerecht werden.

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Section 1

Standard Terminology

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Section Contents

Proposed Standard Terminology

This databook includes a new set of symbols. This new format is a proposed industry standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent.

DC ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

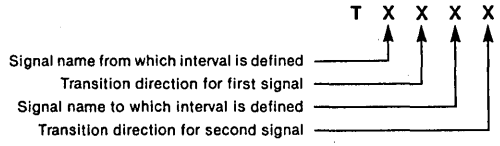
V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies Input (I) or Output (O), and the third letter indicates the High (H), Low (L) or Off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

AC ELECTRICAL PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four or more descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two or more descriptors for each signal point specify the signal name and signal transitions. The format using four descriptors is:



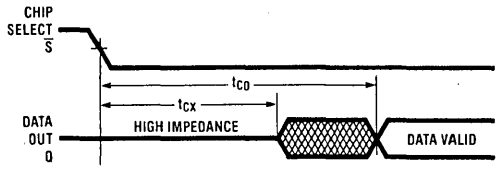
Signal definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

Example:



Chip Select access time, t_{CO}, the time from Chip Select low to Data Out valid, and the time from Chip Select low to Data Out active, t_{CX}, are shown.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view; e.g., the address set-up time is shown as a minimum since the system must supply at least that much time. On the other hand, responses from the memory are specified from the device point of view; e.g., the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

Symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	N/A	HIGH IMPEDANCE

Section 2

MOS Memory Cross Reference Guide

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MOS Memory Cross Reference Guide

Section Contents

MOS Memory Cross Reference and Selection Guide

National Semiconductor offers the widest range of MOS Memory circuits of any manufacturer, both domestic and foreign, with quality and reliability being our primary goal.

Industry Package Cross Reference

Package Type	Molded DIP	CERDIP	Flat Pack
National	N	J	F
AMD	P	D	F
GI	R	C	—
Fujitsu	M	Z	—
Xicor	P	D	—
Hitachi	P	C	—
Intel	P	D	F
Mostek	N	J	F
Motorola	P	D	—
NEC	C	D	—
TI	N	J	U
OKI	RS	AS	F
Synertek	P	D	F
Toshiba	P	C	—

MOS Memory Cross Reference Guide

	AMD	Xicor	Fujitsu	GI	Hitachi	Intel	Mostek	Motorola	NEC	OKI	Synertek	TI	Toshiba	NATIONAL	Pins	Type	Organization
STATICS	AM9114		MBM8114		HM472114	M2114		MCM2114	μPD2114	MSM2114	SY2114	TMS2114	TMM314	[1]MM2114	18	NMOS	1k x 4
	AM9128		MB8128		HM6116P		MK4802	MCM2016	μPD4016	MSM2128	SY2128	TMS4016	TMM2016	[1]NMC2116	24	NMOS	2k x 8
	AM9147		MBM2147		HM4847	D2147H	MK2147H	MCM2147	μPD2147		SY2147	TMS2147	TMM315	•[1]NMC2147H	18	NMOS	4k x 1
	AM9148		MBM2148		HM2148	2148H		MCM2148			SY2148			[1]NMC2148H	18	NMOS	1k x 4
					HM6264	2186							TC5564	[3]NMC6164	28	CMOS	8k x 8
DYNAMICS			MBM8264		HM4864	2164	MK4164	MCM6665	μPD4164	MSM3764		TMS4164	TMM4164	NMC3764	16	NMOS	64k x 1
			MB81257		HM50257		MK4556	MCM6256	μPD41257	MSM41257		TMS41257	TMM41257	[3]NMC41257	16	NMOS	256k x 1
EPROMs	AM2716		MBM2716		HN462716	2716		MCM2716	μPD2716	MSM2716	SY2716	TMS2716	TMM323	•MM2716	24	NMOS	2k x 8
														•NMC27C16	24	CMOS	2k x 8
	AM2732		MBM27C32		HN462732	2732A			μPD2732	MSM2732			TMM2732	•NMC27C32	24	CMOS	2k x 8
						2758				MSM2758		TMS2758		MM2758	24	NMOS	1k x 8
EEPROMs					HN48016	D2816								NMC2816	24	NMOS	2k x 8
					HN48016	D2816								NMC9716	24	NMOS	2k x 8
		[4]X2444		ER59256										NMC9306	8	NMOS	256-bit
				ER5911										[2]NMC9346	8	NMOS	1k-bit
		X2816A				2817A					[4](See Q 52B13)			[3]NMC9817	28	NMOS	2k x 8

•A^+ available
1. Low power available
2. Sole source
3. Future product
4. Not pin compatible

Note: 41257 = Nibble Mode
256 = Page Mode

MOS Memory Selection Guide

Part Number	Organization	Access Time (ns)	Temperature (°C)
NMC6164-10	8k x 8	100	0 to +70
NMC6164-12	8k x 8	120	0 to +70
NMC6164-15	8k x 8	150	0 to +70
NMC6164-20	8k x 8	200	0 to +70
MM2114	1k x 4	450	0 to +70
MM2114-2	1k x 4	200	0 to +70
MM2114-3	1k x 4	300	0 to +70
MM2114-15	1k x 4	150	0 to +70
MM2114-25	1k x 4	250	0 to +70
NMC2147H	4k x 1	70	0 to +70
NMC2147H-1	4k x 1	35	0 to +70
NMC2147H-2	4k x 1	45	0 to +70
NMC2147H-3	4k x 1	55	0 to +70
NMC2148H	1k x 4	70	0 to +70
NMC2148H-2	1k x 4	45	0 to +70
NMC2148H-3	1k x 4	55	0 to +70
MM2716	2k x 8	450	0 to +70
MM2716-1	2k x 8	350	0 to +70
MM2716E	2k x 8	450	−40 to +85
NMC27C16-35	2k x 8	350	0 to +70
NMC27C16-45	2k x 8	450	0 to +70
NMC27C16E-45	2k x 8	450	−40 to +85
*NMC27C16HQ-45	2k x 8	450	0 to +70
NMC27C32-35	4k x 8	350	0 to +70
NMC27C32-45	4k x 8	450	0 to +70
NMC27C32E-45	4k x 8	450	−40 to +70
*NMC27C32H-45	4k x 8	450	0 to +70
MM2758Q	1k x 8	450	0 to +70
NMC2816-25	2k x 8	250	0 to +70
NMC2816-35	2k x 8	350	0 to +70
NMC2816-45	2k x 8	450	0 to +70
NMC2816M-25	2k x 8	250	−55 to +125
NMC2816M-35	2k x 8	350	−55 to +125
NMC2816M-45	2k x 8	450	−55 to +125
NMC3764-15	64k x 1	150	0 to +70
NMC3764-20	64k x 1	200	0 to +70
NMC41257-12	256 x 1	120	0 to +70
NMC41257-15	256 x 1	150	0 to +70
NMC41257-20	256 x 1	200	0 to +70
NMC9817-20	2k x 8	200	0 to +70
NMC9817-25	2k x 8	250	0 to +70
NMC9817-35	2k x 8	350	0 to +70
NMC9346	64 x 16-bit	Serial Access	0 to +70
NMC9306	16 x 16-bit	(N/A Serial Access)	0 to +70
NMC9306E	16 x 16-bit	(N/A Serial Access)	−40 to +85
NMC9716-25	2k x 8	250	0 to +70
NMC9716-35	2k x 8	350	0 to +70
NMC9716-45	2k x 8	450	0 to +70
NMC9716M-25	2k x 8	250	−55 to +125
NMC9716M-35	2k x 8	350	−55 to +125
NMC9716M-45	2k x 8	450	−55 to +125

*H = 10 ms max programming

Section 3

Dynamic RAMs

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Section Contents

National Semiconductor

NMC3764 65,536 × 1-Bit Dynamic RAM

General Description

The NMC3764 is a 65,536 by 1-bit dynamic RAM. It is fabricated with National's XMOS™ N-channel process and uses double polysilicon gate technology. This provides high density and improved reliability. The chip is passivated with a silicone coating for alpha particle immunity.

The NMC3764 operates with a single 5V power supply with ±10% tolerance. All inputs and outputs are TTL compatible.

Multiplexed address inputs with separate row and column strobes allow the NMC3764 to be packaged in a standard 16-pin DIP.

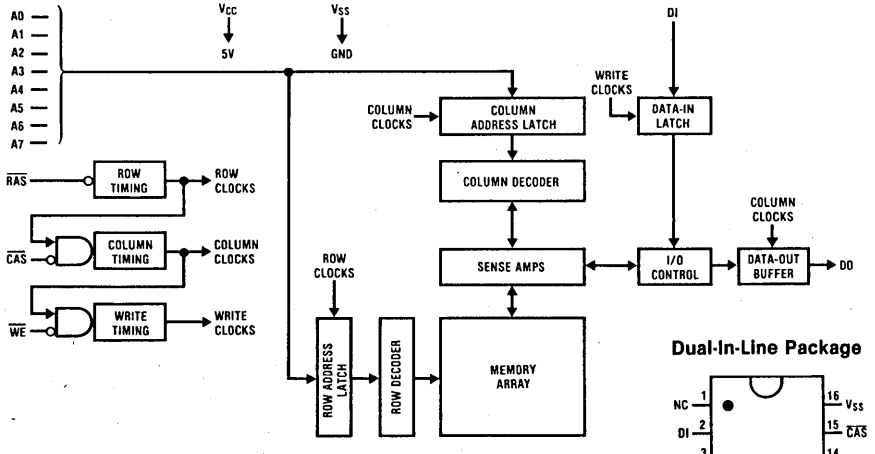
The NMC3764 must be refreshed every 2 ms. This is accomplished by performing any routine which cycles the row address strobe ($\overline{RAS}$) active during each of the 128 different row addresses defined by row address inputs A0–A6 (the additional addresses provided by row address input A7 are not necessary for refreshing.) Any read, write, $\overline{RAS}$-only refresh or hidden refresh cycle refreshes all cells at the selected row address. The $\overline{RAS}$-only refresh mode permits $\overline{RAS}$ to be cycled while the column address strobe ($\overline{CAS}$) is held high, i.e., inactive.

Conversely the buried refresh mode allows the memory to be refreshed by cycling $\overline{RAS}$ while $\overline{CAS}$ is held low, i.e., active, thus maintaining valid data on the output.

Features

- MST™ screen available*
- High performance: 120, 150, 200 ns access times
- Single power supply: 5V ± 10%
- On chip substrate bias generator
- Low power: 248 mW (max) active
- Read, Write and Read-Modify-Write cycles
- Common I/O capability using Early Write cycle
- Page Mode operation
- Gated $\overline{CAS}$-noncritical timing
- $\overline{RAS}$-only Refresh and Buried Refresh capability
- 128 cycle, 2 ms refresh
- TTL compatible: all inputs and outputs
- TRI-STATE® output
- Industry standard 16-pin configuration

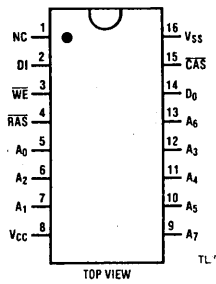
Block And Connection Diagrams



TL/D/5493-1

Pin Names	Function
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A_0–A_7	Address Inputs
DI	Data Input
DO	Data Output
V_{CC}	Power (+5V)
V_{SS}	Ground

Dual-In-Line Package



TL/D/5493-2

Order Number NMC3764N
NS Package Number N16F

*See the MST™ Program.

Absolute Maximum Ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Voltage on Any Pin Relative to VSS	−1.0V to +7V
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	1W	Short Circuit Output Current	50 mA

Recommended DC Operating Conditions

Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature	0	70	°C
V_{CC} V_{SS}	Supply Voltages (Notes 2, 3)	4.5 0	5.5 0	V V
V_{IH}	Input High Voltage, All Inputs (Note 2)	2.4	6.5	V
V_{IL}	Input Low Voltage, All Inputs (Note 2)	−1.0	0.8	V

DC Electrical Characteristics (at recommended operating conditions)

Symbol	Parameter	Min	Max	Units
I_{CC1}	**Operating Current** Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$ Cycling: $t_{RC} = t_{RC}$ MIN, DO = High Impedance) (Note 4)		45	mA
I_{CC2}	**Standby Current** Power Supply Standby Current ($\overline{RAS} = V_{IH}$, DO = High Impedance)		5	mA
I_{CC3}	**Refresh Current** Average Power Supply Current, Refresh Mode ($\overline{RAS}$ Cycling: $t_{RC} = t_{RC}$ MIN, DO = High Impedance) (Note 4)		35	mA
I_{CC4}	**Page Mode Current** Average Power Supply Current, Page Mode ($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling: $t_{PC} = t_{PC}$ MIN, DO = High Impedance) (Note 4)		42	mA
I_{LI}	**Input Leakage** Input Leakage Current, Any Input ($0V < V_{IN} < V_{CC}$, All Other Pins Not Under Test = 0V)	−10	10	μA
I_{LO}	**Output Leakage** Output Leakage Current (DO is Disabled, $0V < V_{OUT} < V_{CC}$)	−10	10	μA
	Output Levels			
V_{OH}	Output High Voltage ($I_{OUT} = -5$ mA)	2.4	V_{CC}	V
V_{OL}	Output Low Voltage (I_{OUT} = 4.2 mA)	0	0.4	V

Capacitance

Symbol	Parameter	Max	Units
C_I	Input Capacitance, A0–A7, DI (Note 5)	5	pF
C_C	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ (Note 5)	10	pF
C_O	Output Capacitance, DO (Note 5)	7	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}.

Note 3: When applying voltages to the device, V_{CC} should never be 1.0V more negative than V_{SS}.

Note 4: I_{CC1}, I_{CC3} and I_{CC4} depend on cycle rate.

Note 5: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = \Delta T/\Delta V$. Capacitance is guaranteed by periodic testing.

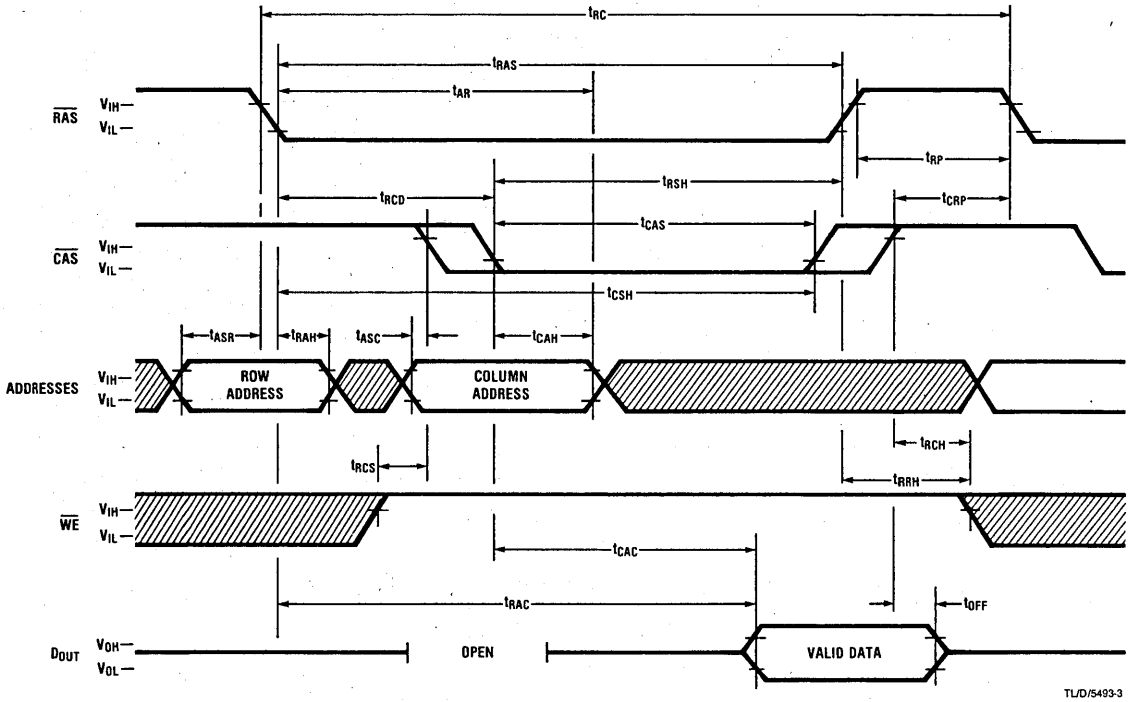
AC Electrical Characteristics (at recommended operating conditions) (Notes 6, 7, 8)

Symbol	Parameter	NMC3764-12		NMC3764-15		NMC3764-20		Units
		Min	Max	Min	Max	Min	Max	
READ, WRITE CYCLES								
t_{RAC}	Access Time from $\overline{RAS}$ (Notes 12, 13)		120		150		200	ns
t_{CAC}	Access Time from $\overline{CAS}$ (Notes 12, 14)		80		100		135	ns
t_{RP}	$\overline{RAS}$ Precharge Time	90		100		120		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	120	10k	150	10k	200	10k	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	80	10k	100	10k	135	10k	ns
t_{RC}	Random Read or Write Cycle Time	240		270		330		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (Note 9)	30	40	30	50	35	65	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	0		0		0		ns
t_{RSH}	$\overline{RAS}$ Hold Time	80		100		135		ns
t_{CSH}	$\overline{CAS}$ Hold Time	120		150		200		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		ns
t_{RAH}	Row Address Hold Time	20		20		25		ns
t_{ASC}	Column Address Set-Up Time	0		0		0		ns
t_{CAH}	Column Address Hold Time	40		45		55		ns
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	80		95		120		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{RCH}	Read Command Hold Time (Note 11)	0		0		0		ns
t_{OFF}	Output Buffer Turn-Off Delay (Note 15)	0	35	0	40	0	50	ns
t_{WP}	Write Command Pulse Width	40		45		55		ns
t_{WCS}	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time (Note 16)	−10		−10		−10		ns
t_{WCH}	Write Command Hold Time	40		45		55		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	80		95		120		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	40		45		55		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	40		45		55		ns
t_{DS}	Data-In Set-Up Time	0		0		0		ns
t_{DH}	Data-In Hold Time	40		45		55		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	80		95		120		ns
t_T	Transition Time (Rise and Fall)	3	35	3	35	3	50	ns
t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	20		20		25		ns
t_{REF}	Refresh Period		2		2		2	ms
READ-MODIFY-WRITE CYCLES								
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	90		110		145		ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay (Note 16)	50		60		80		ns
t_{RWC}	Read-Write-Cycle Time	240		270		330		ns
PAGE MODE CYCLES								
t_{CP}	$\overline{CAS}$ Precharge Time (Note 10)	50		60		80		ns
t_{PC}	Page Mode Cycle Time	150		170		225		ns

Note 6: An initial pause of 100 μs is required after power-up, followed by any 8 RAS cycles, before proper device operation is achieved.
Note 7: Transition times are assumed to be 5 ns.
Note 8: Timing reference points are V_{IH} (min) and V_{IL} (max).
Note 9: If t_{RCD} (min) < t_{RCD} < t_{RCD} (max) the access time is t_{RAC} ($\overline{RAS}$ limited timing). If the t_{RCD} exceeds t_{RCD} (max) the access time is t_{RCD} plus t_{CAC} ($\overline{CAS}$ limited timing).
Note 10: t_{CP} is necessary for $\overline{RAS}/\overline{CAS}$ cycles preceded by a $\overline{CAS}$ only cycle or page mode cycle.
Note 11: t_{RCH} is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.
Note 12: Load = 2 TTL loads and 100 pF.
Note 13: Assumes t_{RCD} < t_{RCD} (max) ($\overline{RAS}$ limited timing).
Note 14: Assumes t_{RCD} > t_{RCD} ($\overline{CAS}$ limited timing).
Note 15: t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
Note 16: The placement of the negative going edge of $\overline{WE}$ with respect to the negative edge of $\overline{CAS}$ determines the type of write cycle. If t_{WCS} is greater than t_{WCS} (min) (negative edge of $\overline{WE}$ before the negative edge of $\overline{CAS}$) the memory is in an early write cycle and data out is TRI-STATE. If t_{CWD} is greater than t_{CWD} (min), the memory is in a read-write or read-modify-write cycle and data out is the original contents of the selected cell. If $\overline{WE}$ goes low between these two times, the cycle is a write cycle and data out is indeterminate.

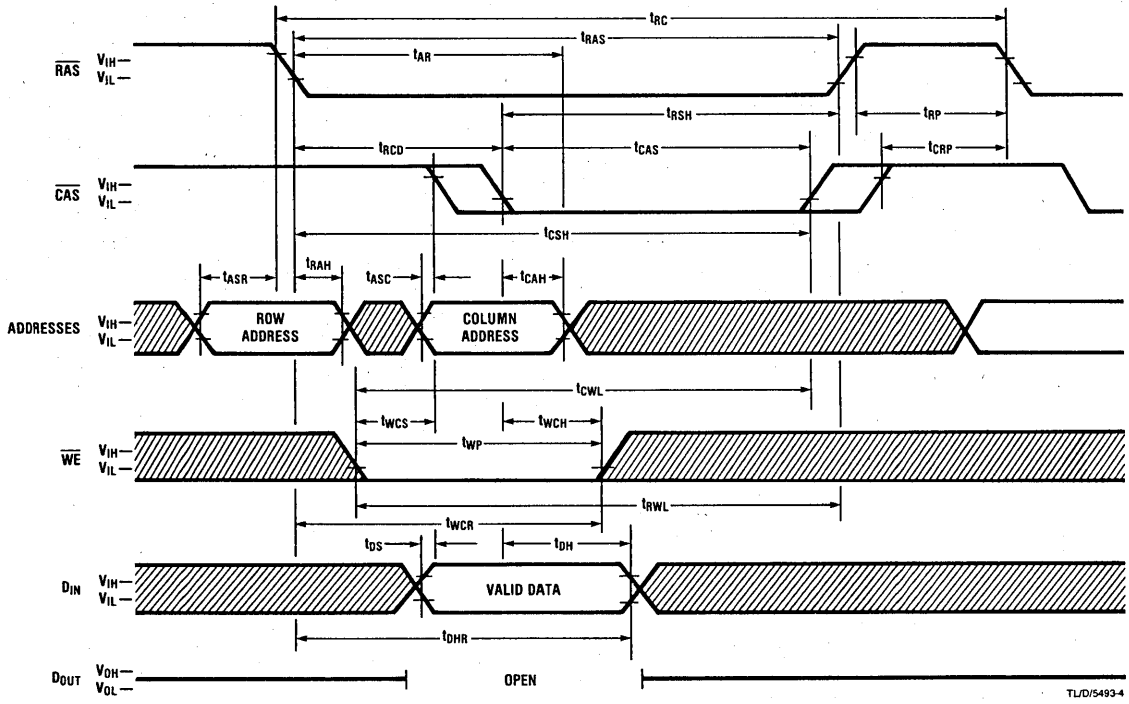
Switching Time Waveforms

Read Cycle Timing



TL/D/5493-3

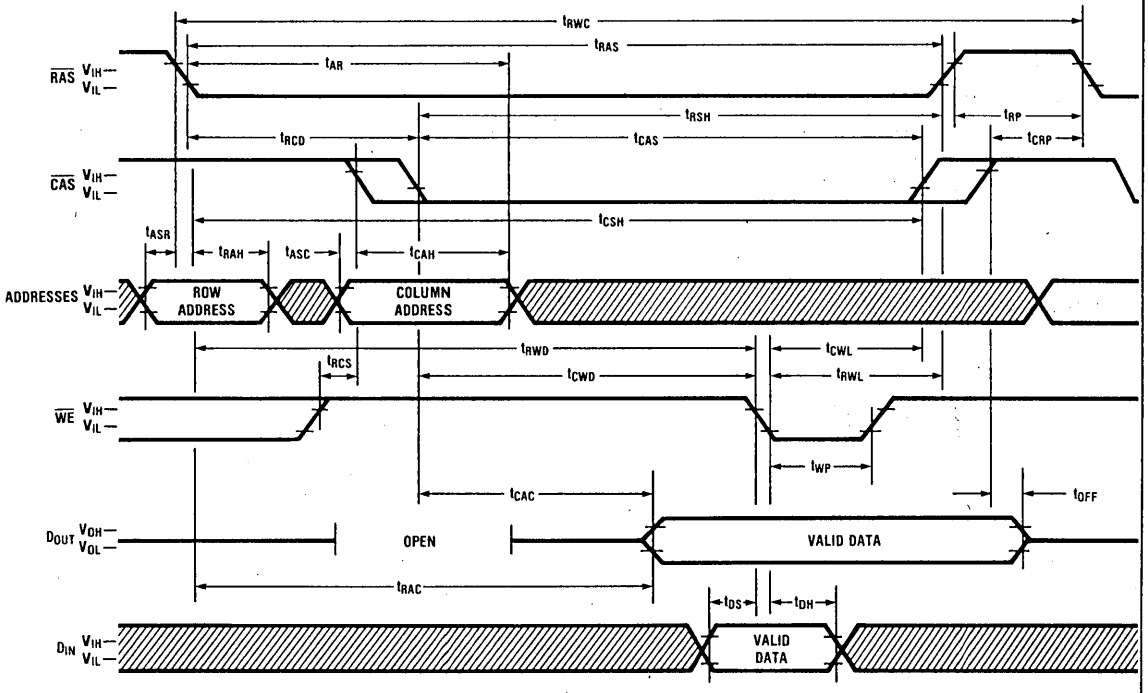
Write Cycle Timing (Early Write)



TL/D/5493-4

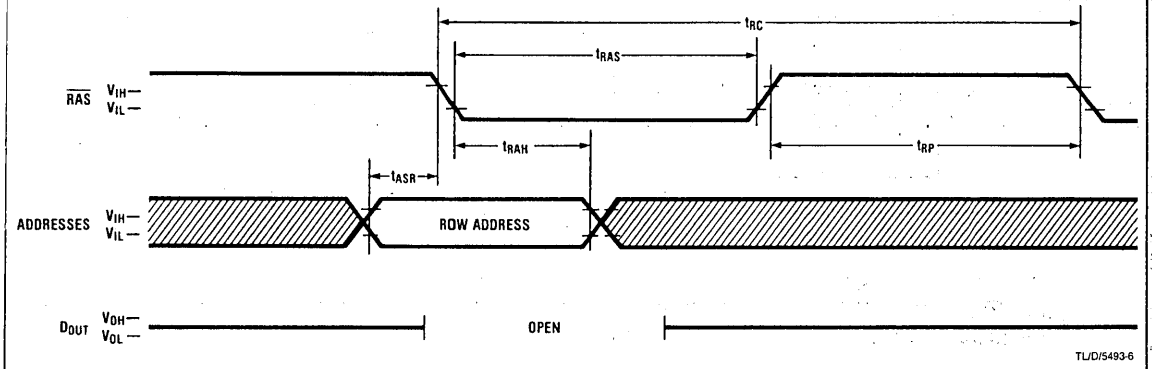
Switching Time Waveforms (Continued)

Read-Write/Read-Modify-Write Cycle



TL/D/5493-5

RAS Only Refresh Timing

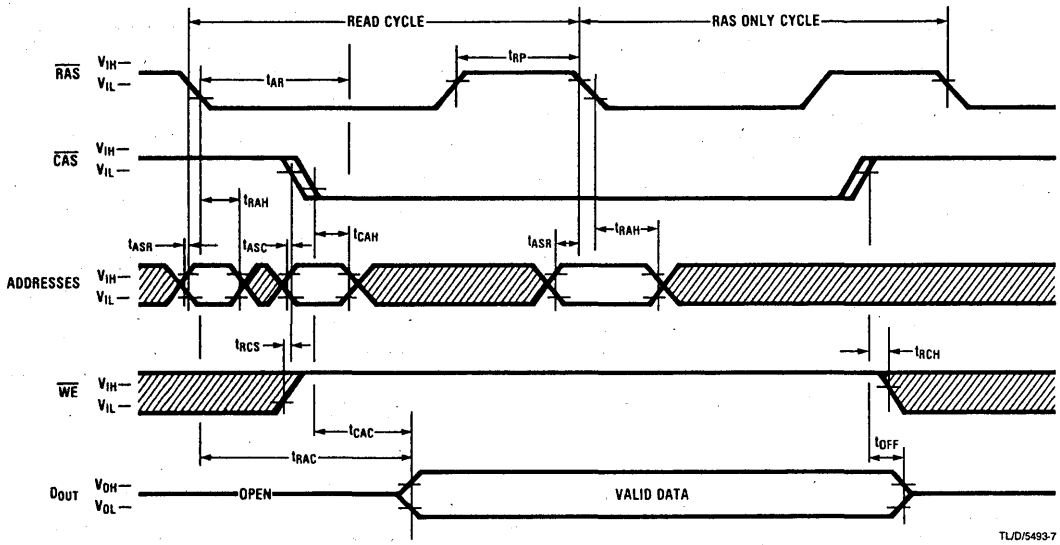


TL/D/5493-6

Note: $\overline{CAS}$: V_{IH}, $\overline{WE}$ and D_{IN}: Don't care.

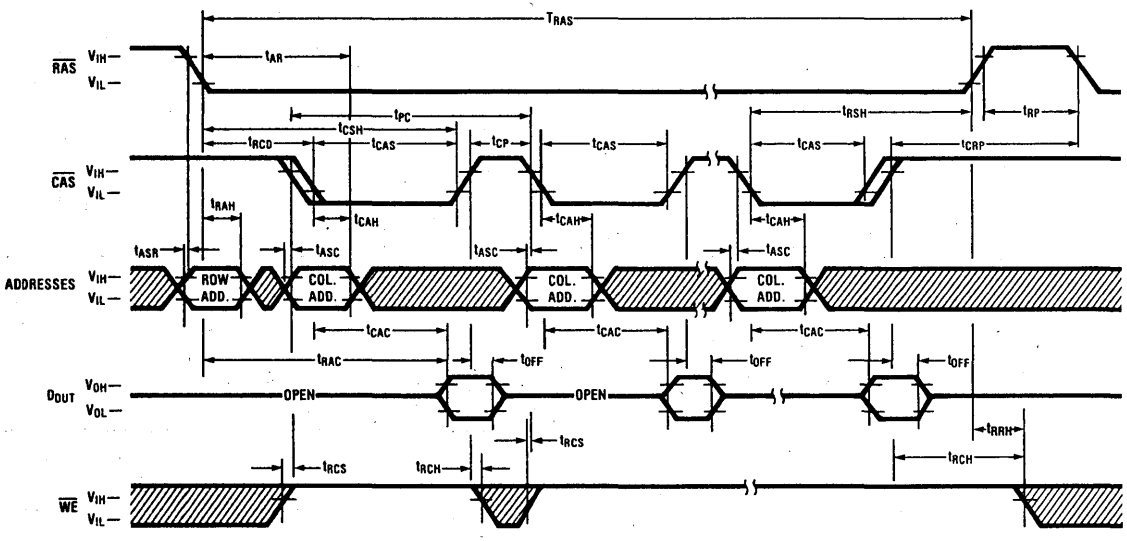
Switching Time Waveforms (Continued)

Hidden Refresh



TL/D/5493-7

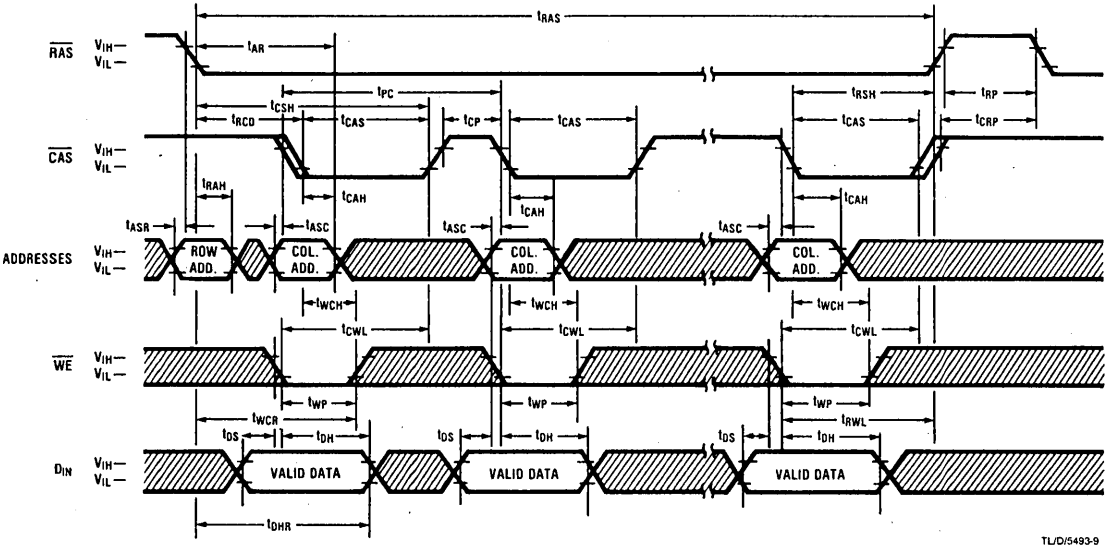
Page Mode Read Cycle



TL/D/5493-8

Switching Time Waveforms (Continued)

Page Mode Write Cycle



TL/D/5493-9

National Semiconductor

PRELIMINARY

NMC41257 262,144 x 1-Bit Dynamic RAM

General Description

The NMC41257 is a 262,144 words by 1-bit new generation dynamic RAM. It is fabricated with National's proprietary N-channel triple-polysilicon technology which combines high performance and high density with improved reliability and excellent alpha radiation tolerance.

The NMC41257 is designed to operate with a single +5V power supply with ±10% tolerance. The use of a single transistor memory cell and advanced dynamic circuitry enable it to achieve high speeds with low power consumption.

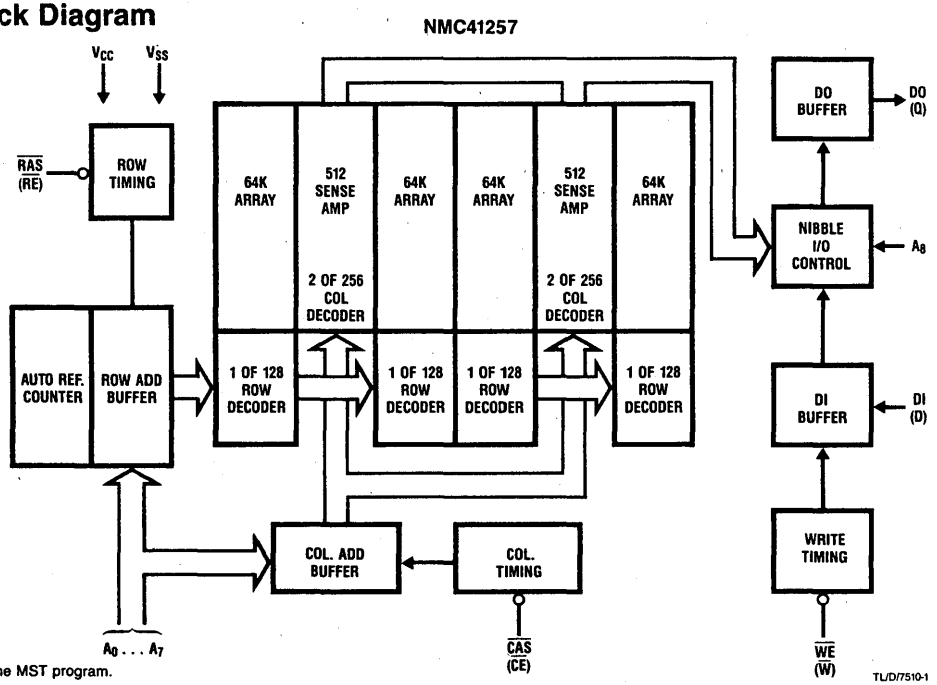
Multiplexed address inputs with separate row and column strobes allow the NMC41257 to be packaged in a standard 16-pin DIP. It is available in both plastic and cerdip packages.

The NMC41257 must be refreshed every 4 ms. This is accomplished by performing any cycle which brings the row address strobe ($\overline{RAS}$) active at each of the 256 row addresses. Thus any read, write, $\overline{RAS}$-only refresh or hidden refresh cycle refreshes all cells at the selected row address. The $\overline{RAS}$-only refresh mode permits the $\overline{RAS}$ to be cycled while the column address strobe ($\overline{CAS}$) is held high, i.e., inactive. In this mode, addresses A0–A7 select the row that is refreshed. In addition, a $\overline{CAS}$ before $\overline{RAS}$ automatic refresh is provided. When $\overline{RAS}$ goes low after $\overline{CAS}$ has been low (by t_{CSR}), the internal refresh counter is activated to generate the addresses to be refreshed. In this mode all address inputs are ignored by the device. A nibble mode is also provided allowing the serial access of 4 bits of data at a very high data rate. Nibble mode address is controlled by the addresses supplied to pin 1 (A8 — Row and Column).

Features

- High performance: 100, 120, 150 ns access time
- Single power supply: 5V ±10%
- Low power: 22 mW (max) standby
  412 mW (max) active
- Wide $\overline{RAS}$ to $\overline{CAS}$ delay windows
- Read, Write and Read-Modify-Write cycles
- Common I/O capability using Early Write cycle
- $\overline{RAS}$-only Refresh and Hidden Refresh capability
- Automatic $\overline{CAS}$ before $\overline{RAS}$ refresh mode
- 256 cycle, 4 ms refresh
- TTL compatible: all inputs and output
- Industry standard 16-pin configuration
- TRI-STATE® output
- Fast nibble mode on either read or write cycles
  — 20 ns access (41257-10)
  — 40 ns cycle (41257-10)
- MST™ screen available*

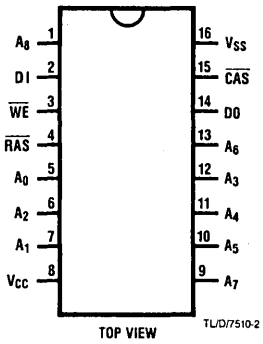
Block Diagram



*See the MST program.

Connection Diagram

Dual-In-Line Package



TOP VIEW

NS Package Number N16A

Pin Names

$\overline{RAS}$ ($\overline{RE}$) Row Address Strobe
$\overline{CAS}$ ($\overline{CE}$) Column Address Strobe
$\overline{WE}$ ($\overline{W}$) Write Enable
A_0–A_8 Address Inputs
DI (D) Data Input
DO (Q) Data Output
V_{CC} Power (5V)
V_{SS} Ground

Absolute Maximum Ratings (Note 1)

Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1 Watt
Voltage on Any Pin Relative to V_{SS}	−1.0V to +7V
Lead Temperature (Soldering, 10 seconds)	300°C

Device	NMC 41257-10	NMC 41257-12	NMC 41257-15
t_{RAC} (ns, Max)	100	120	150
t_{CAC} (ns, Max)	50	60	75
t_{RC} (ns, Min)	200	230	280
I_{CC1} (mA, Max)	75	75	75
I_{CC2} (mA, Max)	4	4	4

Recommended DC Operating Conditions

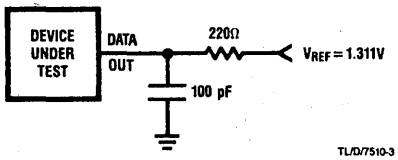
Symbol	Parameter	Min	Max	Units
T_A	Ambient Temperature	0	70	°C
V_{CC}	Supply Voltages (Notes 2 and 3)	4.5	5.5	V
V_{SS}	Supply Voltages (Notes 2 and 3)	0	0	V
V_{IH}	Input High Voltage, All Inputs (Note 2)	2.4	V_{CC} + 1.0	V
V_{IL}	Input Low Voltage, All Inputs (Note 2)	−1.0	0.8	V

DC Electrical Characteristics (at recommended operating conditions)

Symbol	Parameter	Min	Max	Units
I_{CC1}	Operating Current Average Power Supply Operating Current (Note 4) ($\overline{RAS}$, $\overline{CAS}$ Cycling, $t_{RC} = t_{RC\ MIN}$)		75	mA
I_{CC2}	Standby Current Power Supply Standby Current ($\overline{RAS} = \overline{CAS} = V_{IH}$, DO = High Impedance)		4	mA
I_{CC3}	Refresh Current (RAS only) Average Power Supply Current, Refresh Mode (Note 4) ($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC\ MIN}$)		50	mA
I_{CC4}	Refresh Current (automatic $\overline{CAS}$ before $\overline{RAS}$) Average Power Supply Current, Refresh Mode (Note 4) $\overline{CAS} = V_{IL}$, $\overline{RAS}$ Cycling, $t_{RC} = t_{RC\ MIN}$)		50	mA
I_I	Input Leakage Input Leakage Current, Any Input (0V < V_{IN} < V_{CC}, All Other Pins not Under Test = 0V)	−10	10	μA
I_{OZ}	Output Leakage Output Leakage Current (D_0 is Disabled, 0V < V_{OUT} < V_{CC})	−10	10	μA
V_{OH} V_{OL}	Output Levels Output High Voltage (I_{OUT} = −5 mA) Output Low Voltage (I_{OUT} = 4.2 mA)	2.4 0	V_{CC} 0.4	V V

AC Testing Conditions

1. Data Out Load



TL/D/7510-3

2. Input Levels

V_{IL} (Max)	0.8V
V_{IH} (Min)	2.4V

3. Output Levels

V_{OL}	0.4V	I_{OL} = 4.2 mA
V_{OH}	2.4V	I_{OL} = −5.0 mA

4. Transition times are measured between 0.8V (V_{IL} Max) and 2.4V (V_{IH} Min). Rise and fall times are 5 ns.

Capacitance

Symbol	Parameter	Max	Units
CI	Input Capacitance, A0–A8, DI (Note 5)	5	pF
CC	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ (Note 5)	10	pF
CO	Output Capacitance, DO (Note 5)	7	pF

AC Electrical Characteristics (at recommended operating conditions) (Notes 2, 6, 7, and 8)

Symbol	Parameter	NMC41257-10		NMC41257-12		NMC41257-15		Units
		Min	Max	Min	Max	Min	Max	
READ, WRITE CYCLES								
t_{RAC}	Access Time from $\overline{RAS}$ (Notes 11, 12)		100		120		150	ns
t_{CAC}	Access Time from $\overline{CAS}$ (Notes 11, 13)		50		60		75	ns
t_{RP}	$\overline{RAS}$ Precharge Time	90		100		120		ns
t_{RAS}	$\overline{RAS}$ Pulse Width	100	10k	120	10k	150	10k	ns
t_{CAS}	$\overline{CAS}$ Pulse Width	50		60		75		ns
t_{RC}	Random Read or Write Cycle Time	200		230		280		ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time (Note 9)	20	50	25	60	25	75	ns
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		ns
t_{RSH}	$\overline{RAS}$ Hold Time	50		60		75		ns
t_{CSH}	$\overline{CAS}$ Hold Time	100		120		150		ns
t_{ASR}	Row Address Set-Up Time	0		0		0		ns
t_{RAH}	Row Address Hold Time	15		20		20		ns
t_{ASC}	Column Address Set-Up Time	0		0		0		ns
t_{CAH}	Column Address Hold Time	25		30		30		ns
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	75		90		105		ns
t_{RCS}	Read Command Set-Up Time	0		0		0		ns
t_{RCH}	Read Command Hold Time (Note 10)	0		0		0		ns
t_{OFF}	Output Buffer Turn-Off Delay (Note 14)		20		25		25	ns
t_{WP}	Write Command Pulse Width	20		25		30		ns
t_{WCS}	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time (Note 15)	0		0		0		ns
t_{WCH}	Write Command Hold Time	20		25		30		ns
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		100		120		ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	40		45		45		ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	40		45		45		ns
t_{DS}	Data-In Set-Up Time	0		0		0		ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	NMC41257-10		NMC41257-12		NMC41257-15		Units
		Min	Max	Min	Max	Min	Max	
t_{DH}	Data-In Hold Time	20		25		30		ns
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	85		100		120		ns
t_T	Transition Time (Rise and Fall) (Note 7)	3	50	3	50	3	50	ns
t_{REF}	Refresh Period		4		4		4	ms
READ-MODIFY-WRITE CYCLES								
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	100		120		150		ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay (Note 15)	50		60		75		ns
t_{RWC}	Read-Write-Cycle Time	245		280		330		ns
t_{RRW}	RMW Cycle $\overline{RAS}$ Pulse Width	145	10k	170	10k	205	10k	ns
t_{CRW}	RMW Cycle $\overline{CAS}$ Pulse Width	95		110		130		ns
REFRESH CYCLE								
t_{CSR}	Column Address Strobe Setup Time for Auto Refresh	10		10		10		ns
t_{CHR}	Column Address Strobe Hold Time for Auto Refresh	30		30		30		ns
t_{RPC}	Precharge to $\overline{CAS}$ Active Time	0		0		0		ns
NIBBLE MODE CYCLE								
t_{NC}	Nibble Mode Cycle Time	40		50		60		ns
t_{NAC}	Nibble Mode Access Time	20		25		30		ns
t_{NAS}	Nibble Mode Setup Time	20		25		30		ns
t_{NP}	Nibble Mode Precharge Time	10		15		20		ns
t_{NRSH}	Nibble Mode $\overline{RAS}$ Hold Time	20		25		30		ns
t_{NCWD}	Nibble Mode $\overline{CAS}$ to WRITE Delay	20		25		30		ns
t_{NCRW}	Nibble Mode RMW $\overline{CAS}$ Pulse Width	45		55		65		ns
t_{NCWL}	Nibble Mode WRITE to $\overline{CAS}$ Lead Time	20		25		30		ns
AUTO REFRESH COUNTER TEST MODE								
t_{RTC}	Refresh Counter Test Cycle Time (Note 16)	360		410		500		
t_{TRAS}	Refresh Counter Test $\overline{RAS}$ Pulse and Width (Note 16)	260	10k	300	10k	360	10k	
t_{CPT}	Refresh Counter Test $\overline{CAS}$ Precharge Time (Note 16)	50		60		70		

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the device should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}.

Note 3: When applying voltages to the device. V_{CC} should never be 1.0V more negative than V_{SS}.

Note 4: I_{CC1}, I_{CC3}, and I_{CC4} depend on cycle rate measured with output open.

Note 5: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\,\Delta t/\Delta V$ with the recommended DC operating conditions applied to the device. Capacitance is guaranteed by periodic testing.

Note 6: Any 8 cycles that perform refresh must be applied following either power on or periods of no row address strobe activity exceeding 4 ms.

Note 7: Transition times are assumed to be 5 ns.

Note 8: Timing reference points are V_{IH} (min) and V_{IL} (max).

Note 9: If t_{RCD} (min) $< t_{RCD} < t_{RCD}$ (max) the access time is t_{RAC} (row timing limited). If the t_{RCD} exceeds t_{RCD} (max) the access time is t_{RCD} plus t_{CAC} (column timing limited). If -10 ns $< t_{RCD} < t_{RCD}$ (min) the cycle is indeterminate.

Note 10: t_{RCH} is referenced to the first rising edge of $\overline{RAS}$ or $\overline{CAS}$.

Note 11: See AC Testing Conditions for output load.

Note 12: Assumes $t_{RCD} < t_{RCD}$ (max) (row limited timing).

Note 13: Assumes $t_{RCD} > t_{RCD}$ (max) (column limited timing).

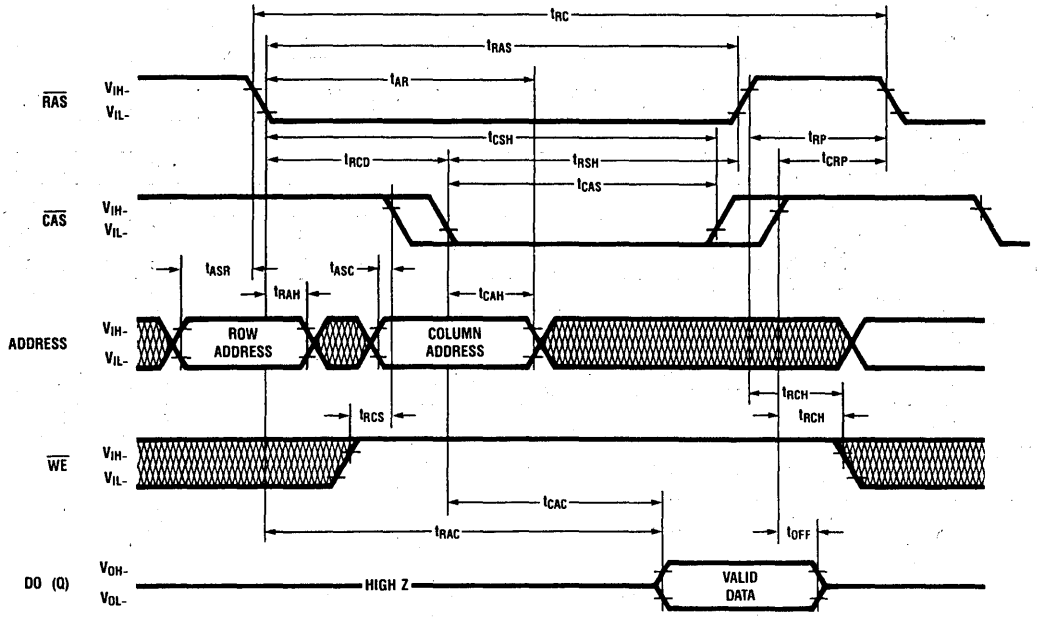
Note 14: t_{OFF} max defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Note 15: The placement of the negative going edge of $\overline{WE}$ with respect to the negative edge of $\overline{CAS}$ determines the type of write cycle. If t_{WCS} is greater than 0 ns (negative edge of $\overline{WE}$ before the negative edge of $\overline{CAS}$) the memory is in an early write cycle and data out is TRI-STATE. If t_{CWD} is greater than t_{CWD} (min) the memory is in a read-write or read-modify-write cycle and data out is the original contents of the selected cell. If $\overline{WE}$ goes low between these two times the cycle is a write cycle and data out is indeterminate.

Note 16: Read-modify-write cycle only.

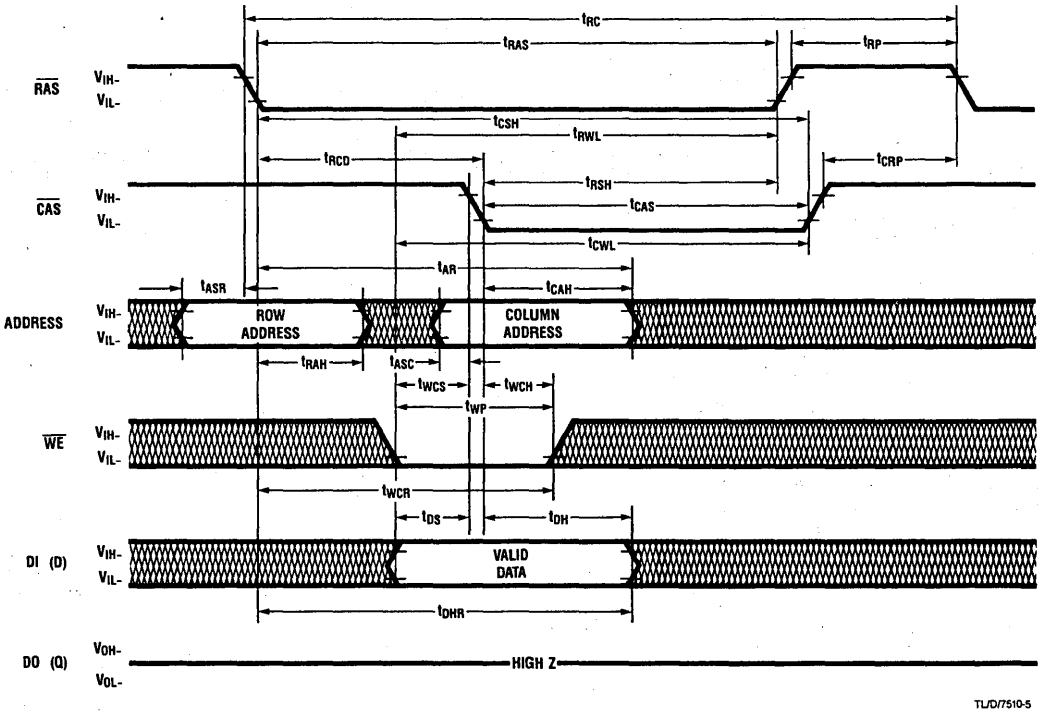
Switching Time Waveforms

Read Cycle Timing



TL/D/7510-4

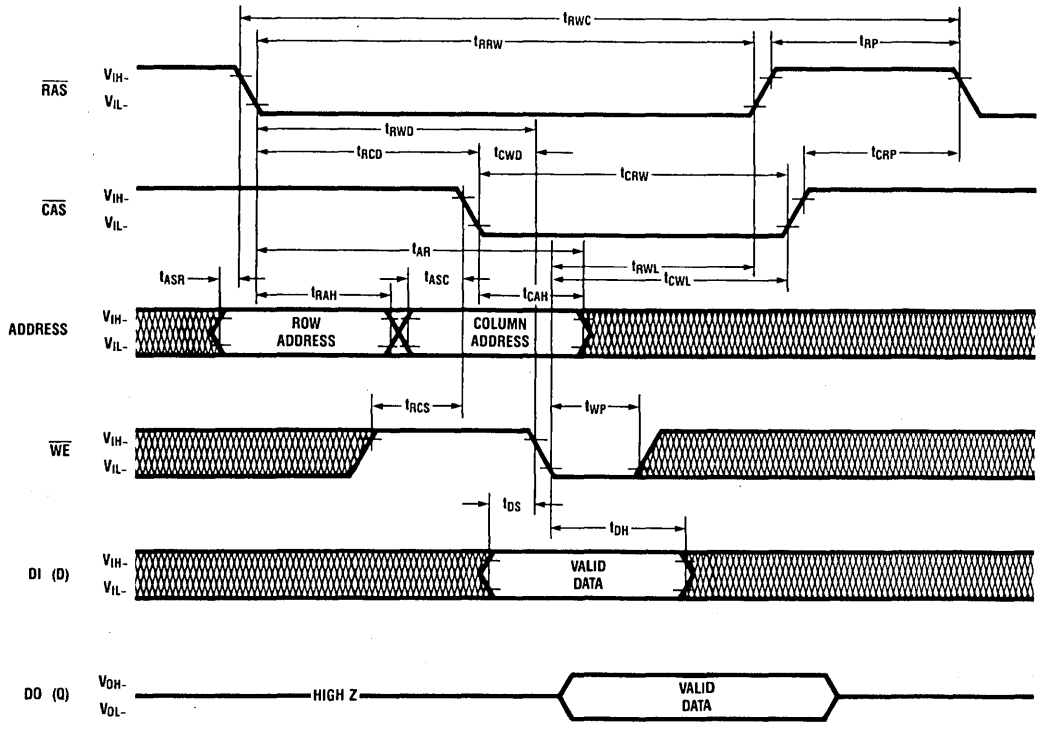
Early Write Cycle



TL/D/7510-5

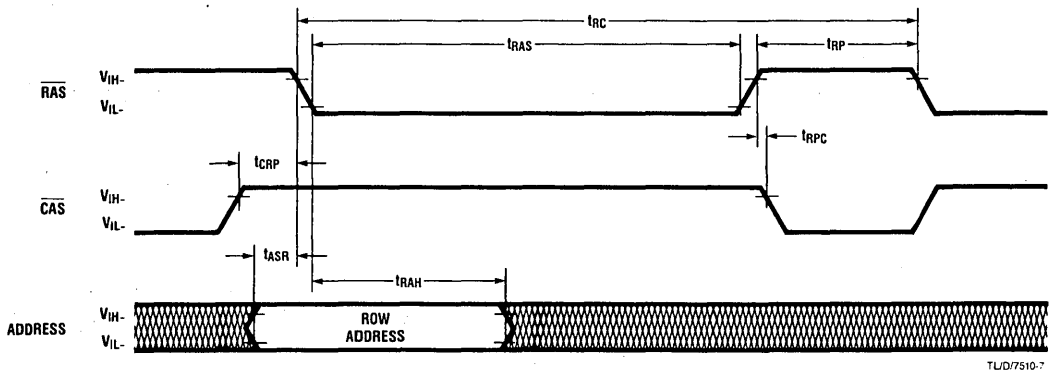
Switching Time Waveforms (Continued)

Read-Modify-Write or Late Write Cycle



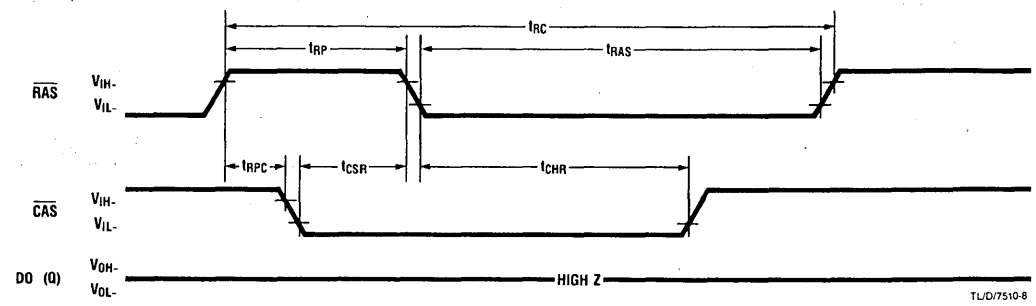
TL/D/7510-6

RAS Only Refresh Cycle
(Data-in and Write are Don't Care)



TL/D/7510-7

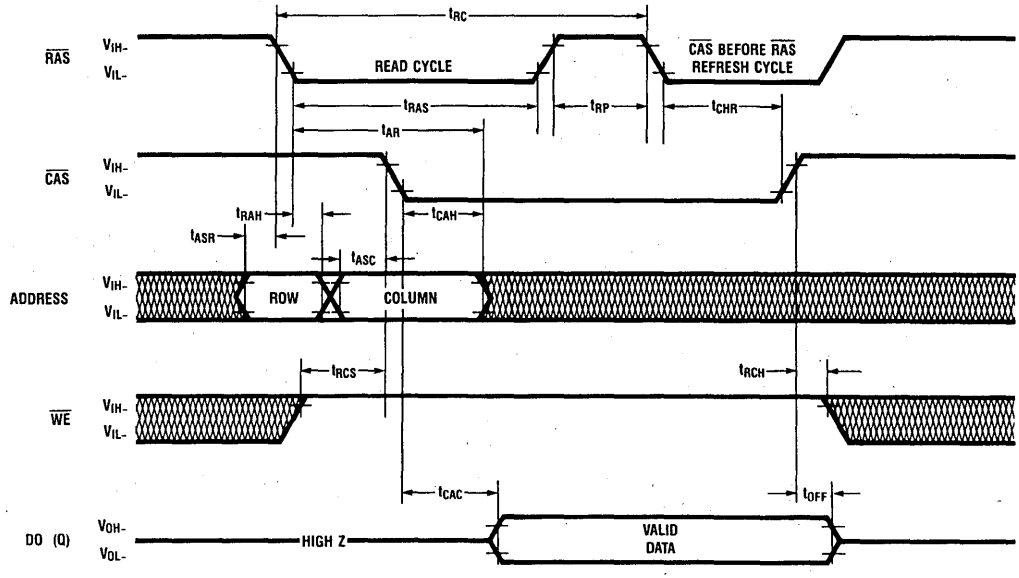
Automatic (CAS Before RAS) Refresh Cycle



TL/D/7510-8

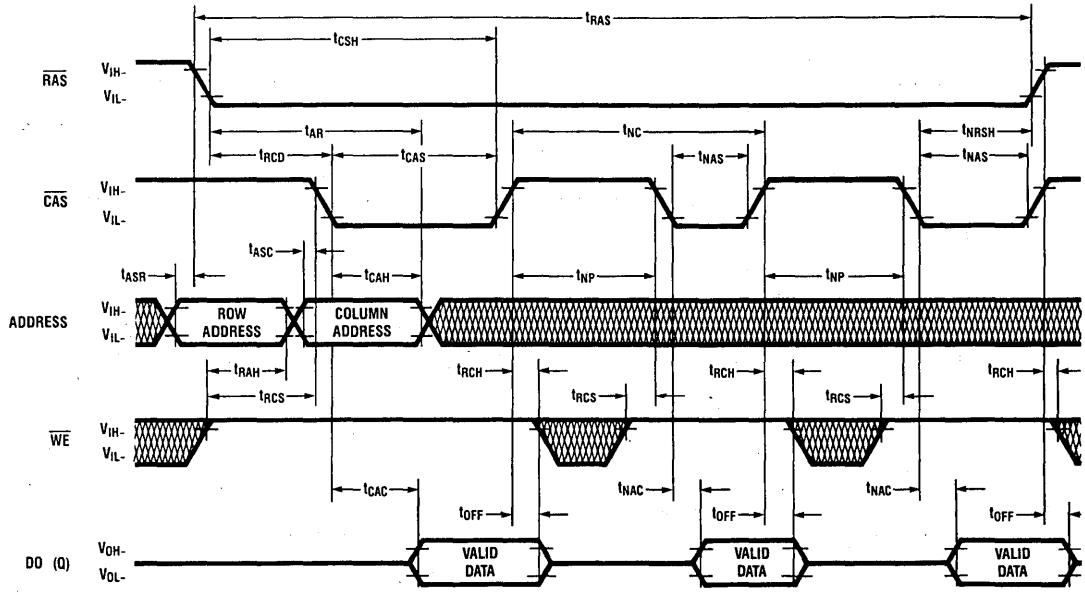
Switching Time Waveforms (Continued)

Hidden Refresh Cycle



TL/D/7510-9

Nibble Mode Read Cycle*

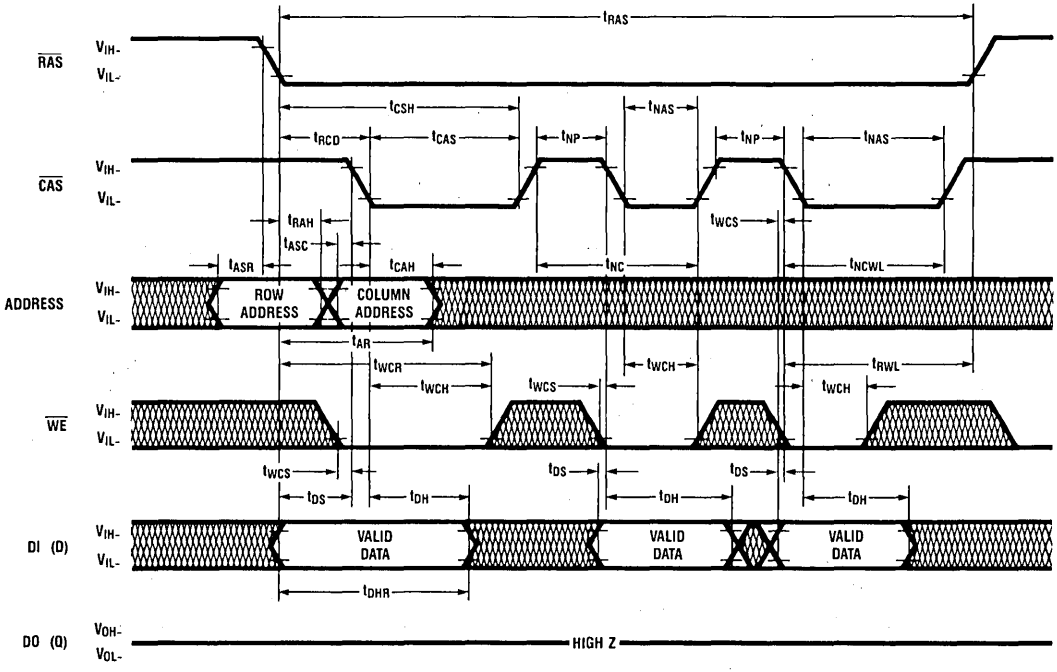


TL/D/7510-10

*Pin 1 at row time and column time determine the starting address of the nibble cycle.

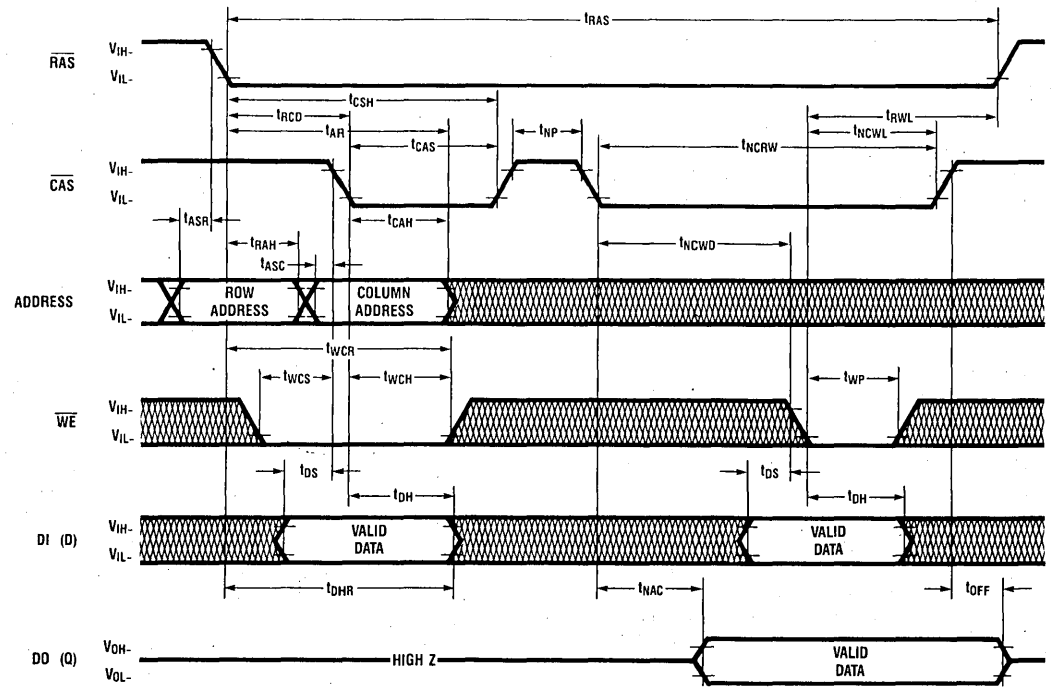
Switching Time Waveforms (Continued)

Nibble Mode Write Cycle (Early Write)



TL/D/7510-11

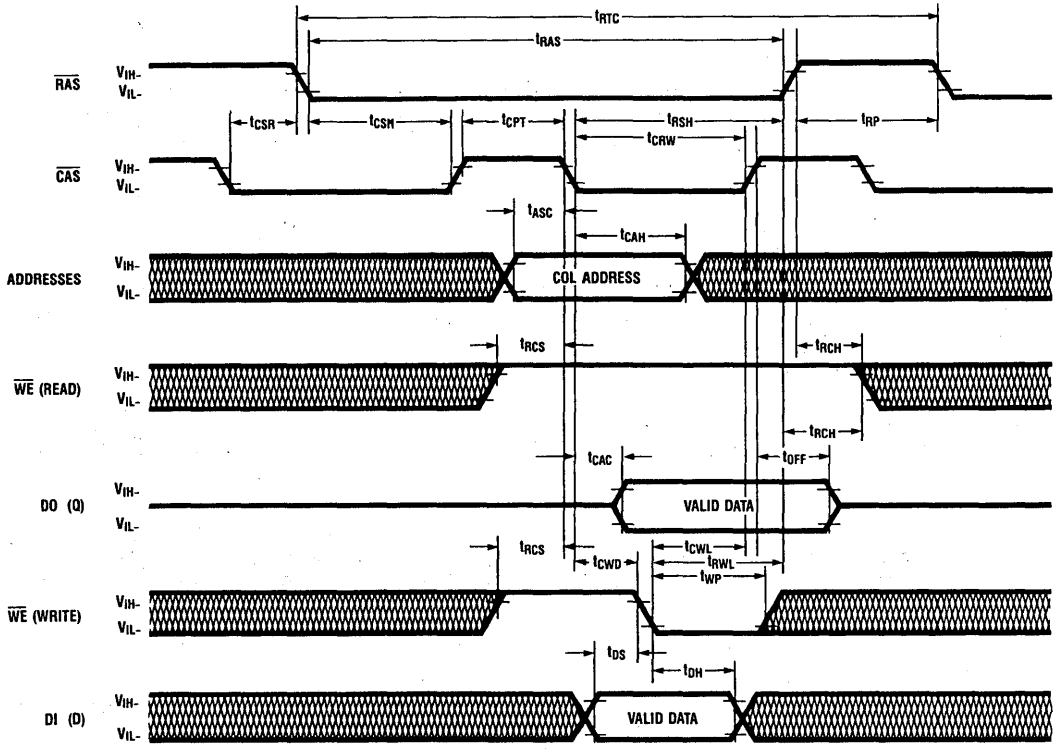
Nibble Mode Read-Modify-Write



TL/D/7510-12

Switching Time Waveforms (Continued)

Auto Refresh Counter Test Cycle



TL/D/7510-13

Functional Description

Device Initialization: The 256K dynamic RAM requires a single +5V supply. After power up an initial 100 microsecond pause is required to allow an internal substrate pump to establish the correct substrate bias. After this pause a minimum of 8 cycles of Row Address Strobe ($\overline{RAS}$) clock must be given to the part to allow the internal dynamic circuitry to reach proper levels. Upon completion of the initialization sequence the part will be ready to operate in accordance with these specifications.

Address Inputs: Eighteen binary address inputs are required to address any one of 262,144 bits in this DRAM. These addresses are multiplexed and strobed into the part in two groups of 9 addresses by the negative going edge of the Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$) clocks. The delay interval between these two clocks (t_{RCD}) describes the minimum time at which the column addresses may follow the row addresses for good device performance and the maximum time at which the column addresses may follow the row addresses before the Access Time (t_{RAC}) will begin to increase beyond the specification.

Reading Data: A read cycle begins by presenting a valid row address to the address inputs and bringing the $\overline{RAS}$ input from V_{IH} to V_{IL}. This causes the row addresses to be latched into the part. This is followed by presenting a valid column address to the address inputs and bringing the $\overline{CAS}$ input from V_{IH} to V_{IL} at which time the column addresses are latched in. If the $\overline{CAS}$ input transition is made before the t_{RCD} maximum time then valid data will appear on data out in time to meet the t_{RAC} specification. If the $\overline{CAS}$ input transition is made after the t_{RCD} maximum time data out will be valid in time to meet the t_{CAC} specification. The external $\overline{CAS}$ signal may become active as soon as the row address hold time (t_{RAH}) specification has been met and defines the t_{RCD} minimum specification. The time difference between t_{RCD} minimum and t_{RCD} maximum can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

Once the clocks have become active, they must stay active for the minimum (t_{RAS}) period for the $\overline{RAS}$ clock and the minimum (t_{CAS}) period for the $\overline{CAS}$ clock. The $\overline{RAS}$ clock must stay inactive for the minimum (t_{RP}) time. The former is for the completion of the cycle in progress, and the latter is for the device internal circuitry to be precharged for the next active cycle.

Data out is not latched and is valid as long as the $\overline{CAS}$ clock is active; the output will switch to the TRI-STATE mode when the $\overline{CAS}$ clock goes inactive. To perform a read cycle, the write ($\overline{WE}$) input must be held at the V_{IH} level from the time the $\overline{CAS}$ clock makes its active transition (t_{RCS}) to the time when it transitions into the inactive (t_{RCH}) mode.

Writing Data: The write cycle is similar to the read cycle except the Write Enable ($\overline{WE}$) clock must be at V_{IL} during the time $\overline{CAS}$ is active. If the $\overline{WE}$ transition is done before the minimum t_{WCS} time, the cycle will be an early write cycle (data out remains in TRI-STATE). If $\overline{WE}$ makes a transition after t_{CWD} minimum time, the cycle will be a read-modify-

Functional Description (Continued)

write cycle. If $\overline{WE}$ makes a transition between t_{WCS} and t_{CWD} time, then the type of cycle is indeterminate.

Data is supplied to the data in input and is latched in with Write Enable ($\overline{WE}$) in the same manner as the addresses are with $\overline{RAS}$ and $\overline{CAS}$ provided the $\overline{WE}$ transition is made after the $\overline{CAS}$ transition. If the $\overline{WE}$ transition is made before the $\overline{CAS}$ transition, then the data is latched by the $\overline{CAS}$ transition.

The Read-Modify-Write Cycle: This type of cycle allows the user to both read and write a single bit in memory during the same cycle.

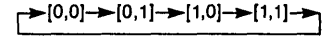
For the read-modify-write cycle a normal read cycle is initiated with the write ($\overline{WE}$) clock at the V_{IH} level until after the t_{CWD} time has elapsed. At this time the write ($\overline{WE}$) clock is asserted. The data in is set up and held with respect to the active edge of the write clock. The cycle described assumes a zero modify time between read and write.

Refreshing the DRAM: The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Therefore, to retain the correct information, the bits need to be refreshed at least once every 4 ms. This is accomplished by sequentially cycling through the 256 row address locations every 4 ms. These row addresses are controlled by address inputs A0 through A7. A normal read or write operation to the RAM will serve to refresh all the bits (1024) associated with that particular row decoded.

For $\overline{RAS}$-Only Refresh type cycle the memory component is in standby. In this refresh method, the user must perform a $\overline{RAS}$-only cycle on all 256 row addresses every 4 ms. The row addresses (A0–A7) are latched with the $\overline{RAS}$ clock, and the associated internal row locations are refreshed. As the heading implies, the $\overline{CAS}$ clock is not required and should be inactive or at a V_{IH} level to conserve power.

For a $\overline{CAS}$ before $\overline{RAS}$ refresh (auto refresh) type cycle $\overline{RAS}$ falls after $\overline{CAS}$ has been low by t_{CSR}. This activates the internal refresh counter which generates the address to be refreshed. Externally applied addresses are ignored during the automatic refresh cycle. If the output buffer was off before the automatic refresh cycle, the output will stay in the high impedance state. If the output was enabled by $\overline{CAS}$ in the previous cycle, the data out will be maintained during the automatic refresh cycle as long as $\overline{CAS}$ is held active (hidden refresh).

The Nibble Mode Cycle: Nibble Mode Operation allows faster successive data operation on 4 bits. The first bit is accessed in the usual manner with read data coming out at t_{CAC} time. By keeping $\overline{RAS}$ low, $\overline{CAS}$ can be cycled up and then down, to read or write the next three bits at a high data rate (t_{NAC}). Row and column addresses need only be supplied for the first access of the cycle. From then on, the falling edge of $\overline{CAS}$ will activate the next bit. After four bits have been accessed, the next bit will be the same as the first bit accessed (wrap-around method).



Pin one (A8) determines the starting point of the circular 4-bit nibble. Row A8 and Column A8 provide the two binary bits needed to select one of four bits. From then on, successive bits come out in a binary fashion; 00→01→10→11 with A8 row being the least significant address.

A nibble cycle can be a read, write, or late write cycle. Any combinations of reads and writes or late writes will be allowed. In addition, the circular wrap-around will continue for as long as $\overline{RAS}$ is kept low.

Section 4

NMOS Static RAMs

4

Section Contents

National Semiconductor

MM2114/MM2114L Family 4096-Bit (1024 x 4) Static RAMs

Maximum Access/Current	MM2114-15L	MM2114-2L	MM2114-25L	MM2114-3L	MM2114-L	MM2114-15	MM2114-2	MM2114-25	MM2114-3	MM2114
Access (TAVQV-ns)	150	200	250	300	450	150	200	250	300	450
Active Current (I_{CC}-mA)	70	70	70	70	70	100	100	100	100	100

General Description

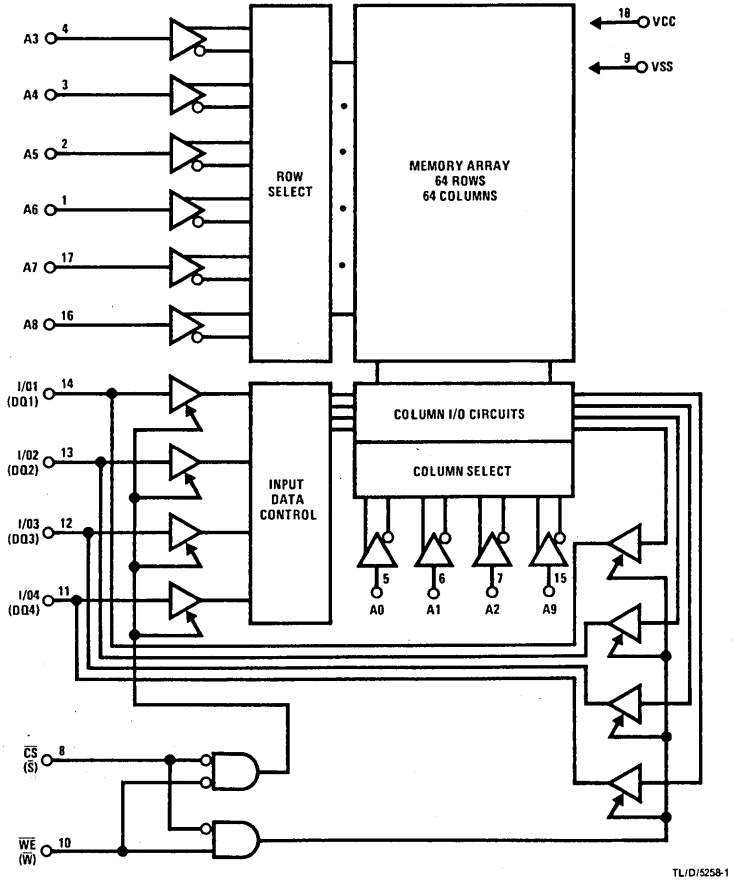
The MM2114 family of 1024-word by 4-bit static random access memories is fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

The separate chip select input ($\overline{CS}$) allows easy memory expansion by OR-tying individual devices to a data bus.

Features

- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Low power—225 mW typical
- High speed—down to 150 ns access time
- TRI-STATE® output for bus interface
- Common Data In and Data Out pins
- Single 5V supply
- Standard 18-pin dual-in-line package
- Available with MIL-STD-883 class B screening

Block Diagram*



TL/D/5258-1

* Symbols in parentheses are proposed industry standard.

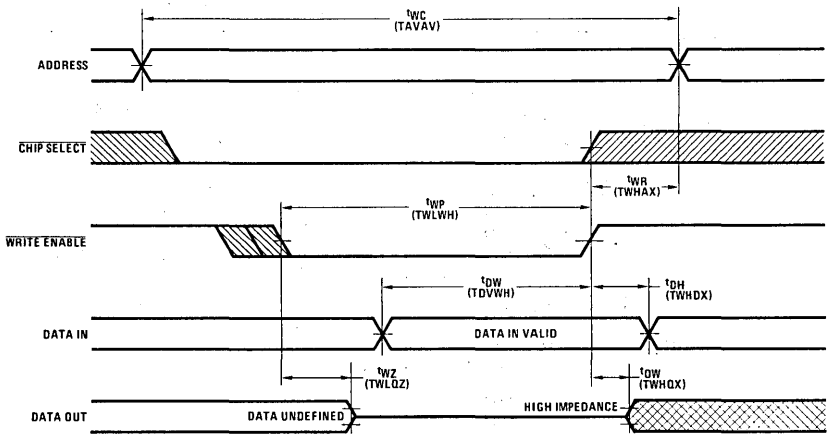
Write Cycle AC Electrical Characteristics (Note 3) $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

Symbol		Parameter	MM2114-15 MM2114-15L		MM2114-2 MM2114-2L		MM2114-25 MM2114-25L		MM2114-3 MM2114-3L		MM2114 MM2114-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	150		200		250		300		450		ns
t_{WP}	TWLWH	Write Pulse Width	90		100		125		150		200		ns
t_{WR}	TWHAX	Write Recovery Time	0		0		0		0		0		ns
t_{DW}	TDVWH	Data Set-Up Time	90		100		125		150		200		ns
t_{DH}	TWHDX	Data Hold Time	0		0		0		0		0		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 5)	0	40	0	40	0	60	0	80	0	100	ns
t_{OW}	TWHQX	Output Active from End of Write ($\overline{WE}$) (Note 5)		80		80		90		100		120	ns

*Symbols in parentheses are proposed industry standard.

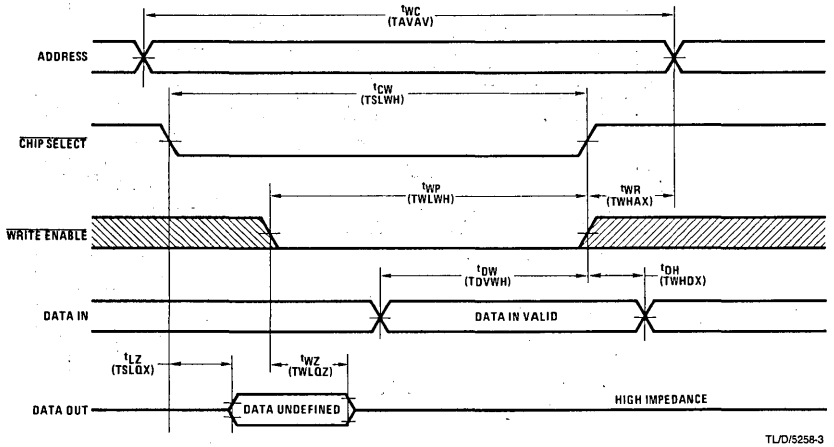
Write Cycle Waveforms* (Note 4)

Write Cycle 1 (Write Enable Limited)



TL/D/5258-2

Write Cycle 2 (Chip Select Limited)



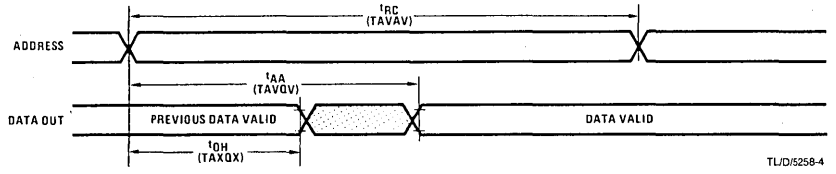
TL/D/5258-3

Read Cycle AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

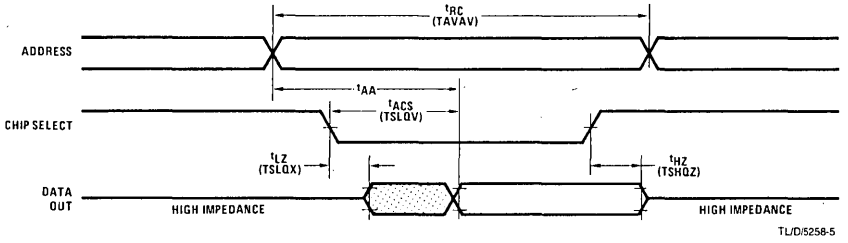
Symbol		Parameter	MM2114-15 MM2114-15L		MM2114-2 MM2114-2L		MM2114-25 MM2114-25L		MM2114-3 MM2114-3L		MM2114 MM2114-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time ($\overline{WE} = V_{IH}$)	150		200		250		300		450		ns
t_{AA}	TAVQV	Address Access Time		150		200		250		300		450	ns
t_{ACS}	TSLQV	Chip Select Access Time		70		70		90		100		120	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 5)	20		20		20		20		20		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 5)	0	40	0	40	0	60	0	80	0	100	ns
t_{OH}	TAXQX	Output Hold from Address Change	15		10		10		10		10		ns

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS} = V_{IL}$, $\overline{WE} = V_{IH}$)



Read Cycle 2 (Chip Select Switched, $\overline{WE} = V_{IH}$)



Note 3: A write occurs during the coincidence low of $\overline{CS}$ and $\overline{WE}$.

Note 4: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions.

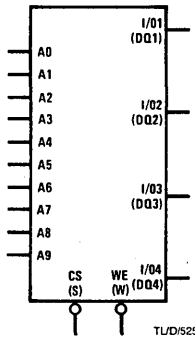
Note 5: Measured ± 50 mV from steady state voltage. This parameter is sampled and not 100% tested.

DC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Conditions	MM2114, MM2114-15, MM2114-2, MM2114-25, MM2114-3		MM2114-L, MM2114-15L, MM2114-2L, MM2114-25L, MM2114-3L		Units
			Min	Max	Min	Max	
I_{LI}	Input Load Current (All Input Pins)	$V_{IN} = 0V$ to $5.25V$	−10	10	−10	10	μA
I_{LO}	Output Leakage Current	$\overline{CS} = V_{IH}$, $V_{OUT} = 0.4V$ to $4V$	−10	10	−10	10	μA
V_{IL}	Input Low Voltage		−0.5	0.8	−0.5	0.8	V
V_{IH}	Input High Voltage		2.0	V_{CC}	2.0	V_{CC}	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA		0.4		0.4	V
V_{OH}	Output High Voltage	$I_{OH} = -1.0$ mA	2.4		2.4		V
I_{CC}	Power Supply Current	$V_{IN} = 5.25V$, $T_A = 0°C$ Outputs Open		100		70	mA

* The symbols in parentheses are proposed industry standard.

Logic Symbol*

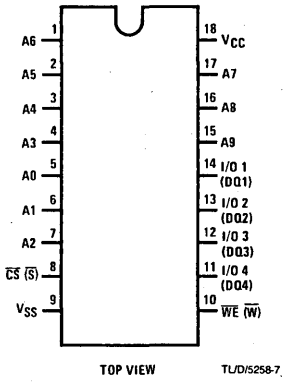


Pin Names*

A0–A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
I/01–I/04 (DQ1–DQ4)	Data Input/Output

Connection Diagram*

Dual-In-Line Package



Order Number MM2114N-15L, MM2114N-15, MM2114N-2L, MM2114N-2, MM2114N-3L, MM2114N-3, MM2114N-L or MM2114N
NS Package Number N18A

Absolute Maximum Ratings

Voltage at Any Pin	−0.5V to +7V
Storage Temperature	−65°C to −150°C
Power Dissipation	1W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.75	5.25	V
Ambient Temperature (T_A)	0	+70	°C

Capacitance $T_A = 25°C$, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	MM2114, MM2114-15, MM2114-2, MM2114-25, MM2114-3		MM2114-L, MM2114-15L, MM2114-2L, MM2114-25L, MM2114-3L		Units
			Min	Max	Min	Max	
C_{IN}	Input Capacitance	All Inputs $V_{IN} = 0V$		5		5	pF
C_{OUT} (Note 2)	Output Capacitance	$V_O = 0V$		5		5	pF

Note 1: This parameter is guaranteed by periodic testing.
Note 2: C_{OUT} is max 10 pF for (J) package.

AC Test Conditions

Input Pulse Levels	0V to 3V	Output Load and Timing Levels	0.8V @ 2.1 mA + 100 pF 2.0V @ −1.0 mA + 100 pF
Input Rise and Fall Times	≤ 10 ns		
Input Timing Level	1.5V		

*Symbols in parentheses are proposed industry standard.

National Semiconductor

NMC2147H 4096 × 1 Static RAM

Max Access/Current	NMC2147H-1	NMC2147H-2	NMC2147H-3	NMC2147H-3L	NMC2147H
Access (TAVQV — ns)	35	45	55	55	70
Active Current (ICC — mA)	180	180	180	125	160
Standby Current (ISB — mA)	30	30	30	20	20

General Description

The NMC2147H is a 4096-word by 1-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

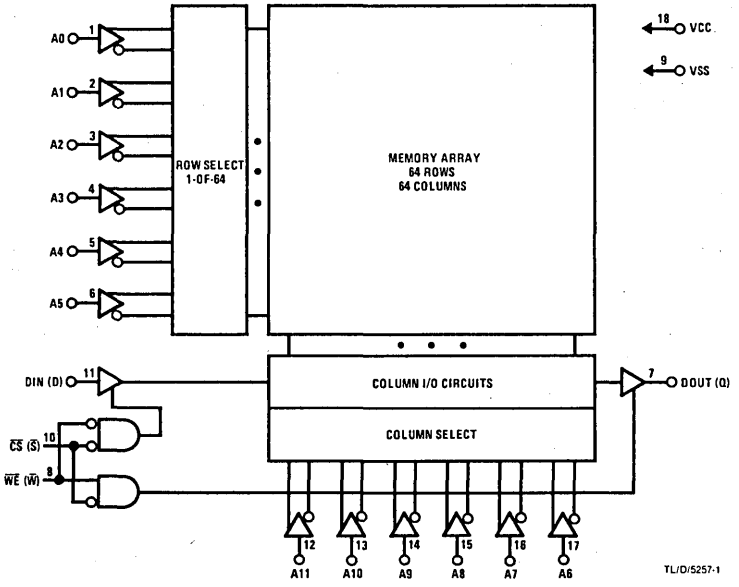
The separate chip select input automatically switches the part to its low power standby mode when it goes high.

The output is held in a high impedance state during write to simplify common I/O applications.

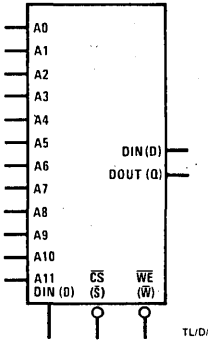
Features

- All inputs and outputs directly TTL compatible
- Static operation — no clocks or refreshing required
- Automatic power-down
- High speed — down to 35 ns access time
- TRI-STATE® output for bus interface
- Separate Data In and Data Out pins
- Single 5V supply
- Standard 18-pin dual-in-line package
- Available in MIL-STD-883 class B screening

Block Diagram*

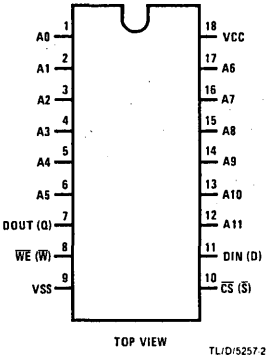


Logic Symbol*



Connection Diagram*

Dual-In-Line Package



Pin Names*

A0-A11	Address Inputs
WE (W)	Write Enable
CS (S)	Chip Select
DIN (D)	Data In
DOUT (Q)	Data Out
VCC	Power (5V)
VSS	Ground

Order Number NMC2147HJ-1, NMC2147HJ-2, NMC2147HJ-3 or NMC2147HJ-3L
NS Package Number J18A
Order Number NMC2147HN-1, NMC2147HN-2, NMC2147HN-3 or NMC2147HN-3L
NS Package Number N18A

* The symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

Voltage on Any Pin Relative to VSS	−3.5V to +7V
Storage Temperature Range	−65°C to +150°C
Power Dissipation	1.2W
DC Output Current	20 mA
Bias Temperature Range	−65°C to +135°C
Lead Temperature (Soldering, 10 seconds)	300°C

Truth Table*

$\overline{CS}$ ($\overline{S}$)	$\overline{WE}$ ($\overline{W}$)	DIN (D)	DOUT (Q)	Mode	Power
H	X	X	Hi-Z	Not Selected	Standby
L	L	H	Hi-Z	Write 1	Active
L	L	L	Hi-Z	Write 0	Active
L	H	X	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2147H-3L		NMC2147H-1 NMC2147H-2 NMC2147H-3		NMC2147H		Units
			Min	Max	Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50		50	μA
VIL	Input Low Voltage		−3.0	0.8	−3.0	0.8	−3.0	0.8	V
VIH	Input High Voltage		2.0	6.0	2.0	6.0	2.0	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180		160	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30		20	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40		30	mA

Capacitance TA = 25°C, f = 1 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
COUT	Output Capacitance	VOUT = 0V		6	pF

Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper orientation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Level (H-1)	1.5V
Output Timing Reference Levels (H-2, H-3, H-3L)	0.8V and 2.0V
Output Load	See *Figure 1*

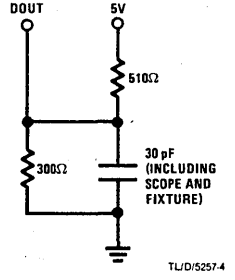


FIGURE 1. Output Load

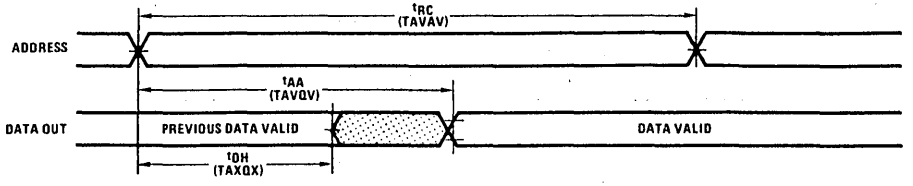
*Symbols in parentheses are proposed industry standard.

Read Cycle AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$ (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	35		45		55		70		ns
t_{AA}	TAVQV	Address Access Time		35		45		55		70	ns
t_{ACS}	TSLQV	Chip Select Access Time (Note 4)		35		45		55		70	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 5)	5		5		10		10		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 5)	0	30	0	30	0	30	0	30	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		20		20		20		30	ns

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



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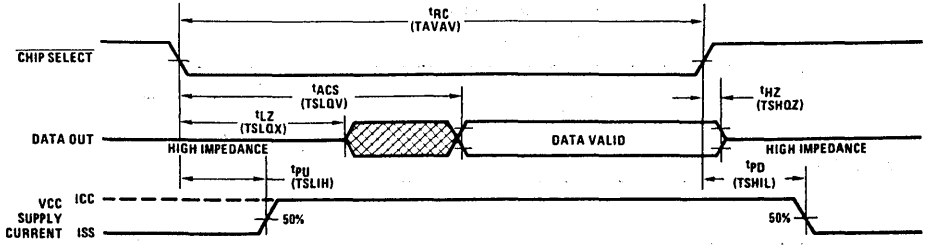
Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)



TL/D/5257-6

Note 4: Address must be valid coincident with or prior to the chip select transition from high to low.

Note 5: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

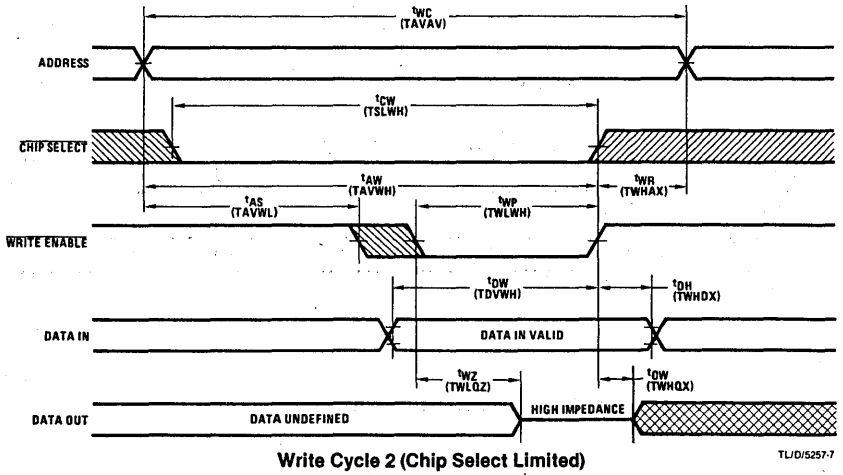
* The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$ (Note 1)

Symbol		Parameter	NMC2147H-1		NMC2147H-2		NMC2147H-3 NMC2147H-3L		NMC2147H		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	35		45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	35		45		45		55		ns
t_{AW}	TAVWH	Address Valid to End of Write	35		45		45		55		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	20		25		25		40		ns
t_{WR}	TWHAX	Write Recovery Time	0		0		10		15		ns
t_{DW}	TDVWH	Data Set-Up Time	20		25		25		30		ns
t_{DH}	TWHDX	Data Hold Time	10		10		10		10		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 5)	0	20	0	25	0	25	0	35	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 5)	0		0		0		0		ns

Write Cycle Waveforms* (Note 6)

Write Cycle 1 (Write Enable Limited)



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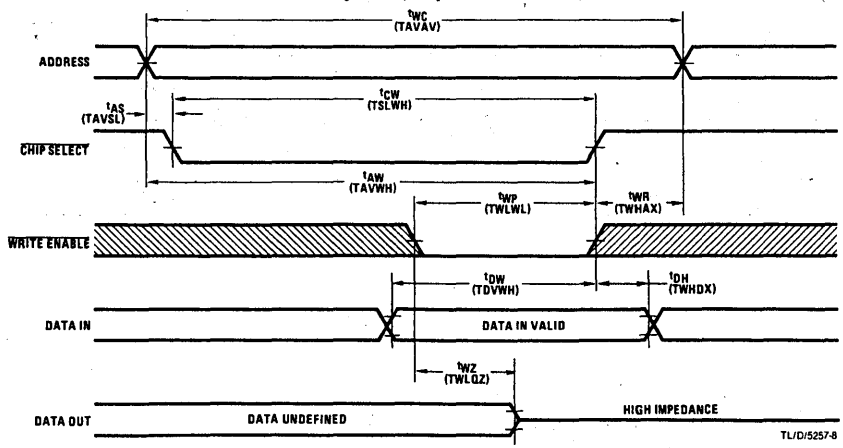
Write Cycle 2 (Chip Select Limited)



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Note 6: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

* The symbols in parentheses are proposed industry standard.

National Semiconductor

NMC2148H 1024 x 4 Static RAM

Max Access/Current	NMC2148H-2	NMC2148H-3	NMC2148H	NMC2148H-3L	NMC2148H-L
Access (TAVQV — ns)	45	55	70	55	70
Active Current (ICC — mA)	180	180	180	125	125
Standby Current (ISB — mA)	30	30	30	20	20

General Description

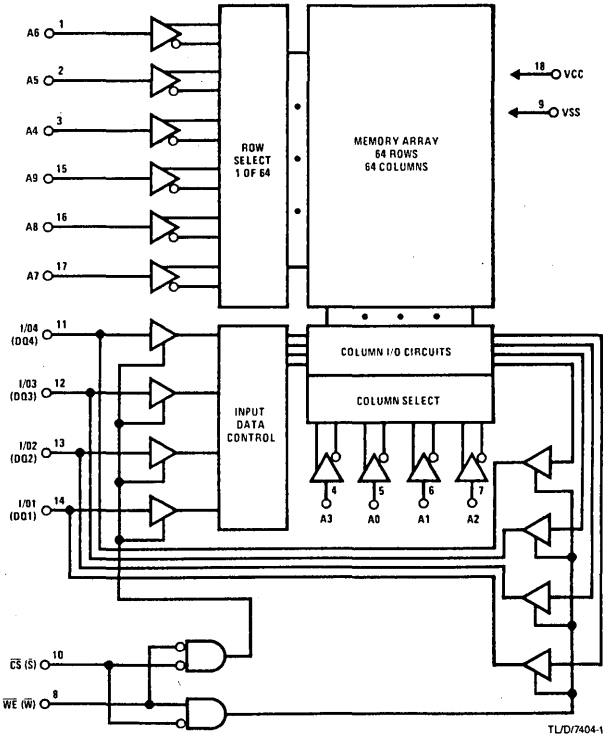
The NMC2148H is a 1024-word by 4-bit static random access memory fabricated using N-channel silicon-gate technology. All internal circuits are fully static and therefore require no clocks or refreshing for operation. The data is read out nondestructively and has the same polarity as the input data.

The separate chip select input automatically switches the part to its low power standby mode when it goes high. Common input/output pins are provided.

Features

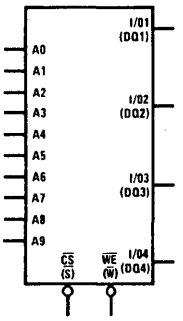
- All inputs and outputs directly TTL compatible
- Static operation—no clocks or refreshing required
- Automatic power-down
- High speed—down to 45 ns access time
- TRI-STATE® output for bus interface
- Common data I/O pins
- Single +5V supply
- Standard 18-pin dual-in-line package

Block Diagram*



TL/D/7404-1

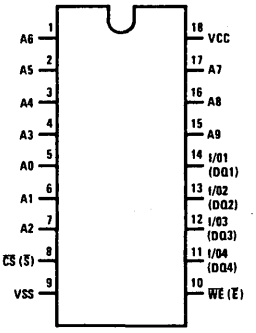
Logic Symbol*



TL/D/7404-2

Connection Diagram*

Dual-In-Line Package



TOP VIEW TL/D/7404-3

Pin Names*

A0-A9	Address Inputs
$\overline{WE}$ ($\overline{W}$)	Write Enable
$\overline{CS}$ ($\overline{S}$)	Chip Select
I/O1-I/O4 (DQ1-DQ4)	Data Input/Output
VCC	Power (5V)
VSS	Ground

Order Number NMC2148HJ-L, NMC2148HJ-3L, NMC2148HJ, NMC2148HJ-2 or NMC2148HJ-3
NS Package Number J18A
Order Number NMC2148HN-L, NMC2148HN-3L, NMC2148HN, NMC2148HN-2 or NMC2148HN-3
NS Package Number N18A

*Symbols in parentheses are proposed industry standard.

Absolute Maximum Ratings

Voltage at Any Pin with Respect to VSS	−3.5V to +7V
Storage Temperature	−65°C to +150°C
Temperature with Bias	−10°C to +85°C
DC Output Current	20 mA
Power Dissipation	1.2W
Lead Temperature (Soldering, 10 seconds)	300°C

Truth Table

$\overline{CS}$	$\overline{WE}$	I/O	Mode	Power
H	X	Hi-Z	Standby	Standby
L	L	H	Write 1	Active
L	L	L	Write 0	Active
L	H	DOUT	Read	Active

DC Electrical Characteristics TA = 0°C to +70°C, VCC = 5V ± 10% (Notes 1 and 2)

Symbol	Parameter	Conditions	NMC2148H-L NMC2148H-3L		NMC2148H NMC2148H-2 NMC2148H-3		Units
			Min	Max	Min	Max	
|ILI|	Input Load Current (All Input Pins)	VIN = 0V to 5.5V, VCC = Max		10		10	μA
|ILO|	Output Leakage Current	$\overline{CS}$ = VIH, VOUT = GND to 4.5V, VCC = Max		50		50	μA
VIL	Input Low Voltage		−2.5	0.8	−2.5	0.8	V
VIH	Input High Voltage		2.1	6.0	2.1	6.0	V
VOL	Output Low Voltage	IOL = 8.0 mA		0.4		0.4	V
VOH	Output High Voltage	IOH = −4.0 mA	2.4		2.4		V
ICC	Power Supply Current	VIN = 5.5V, TA = 0°C, Output Open		125		180	mA
ISB	Standby Current	VCC = Min to Max, $\overline{CS}$ = VIH		20		30	mA
IPO	Peak Power-On Current	VCC = VSS to VCC Min, $\overline{CS}$ = Lower of VCC or VIH Min		30		40	mA
|IOS|	Output Short Circuit Current	VOUT = GND to VCC		250		250	mA

Capacitance TA = 25°C, f = 1.0 MHz (Note 3)

Symbol	Parameter	Conditions	Min	Max	Units
CIN	Address/Control Capacitance	VIN = 0V		5	pF
CI/O	Input/Output Capacitance	VI/O = 0V		7	pF

Note 1: The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.

Note 2: These circuits require 500 μs time delay after VCC reaches the specified minimum limit to ensure proper operation after power-on. This allows the internally generated substrate bias to reach its functional level.

Note 3: This parameter is guaranteed by periodic testing.

AC Test Conditions

Input Test Levels	GND to 3.0V
Input Rise and Fall Times	5 ns
Input Timing Reference Level	1.5V
Output Timing Reference Levels	0.8V and 2.0V
Output Load	See *Figure 1*

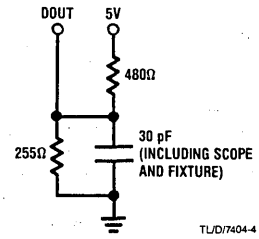


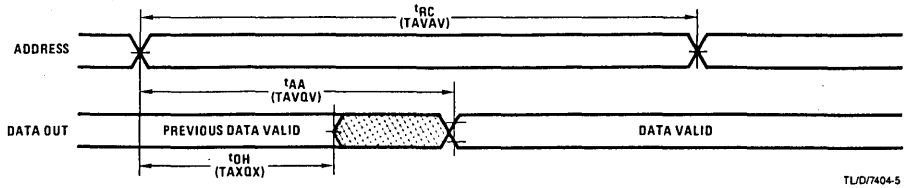
FIGURE 1. Output Load

Read Cycle AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 1)

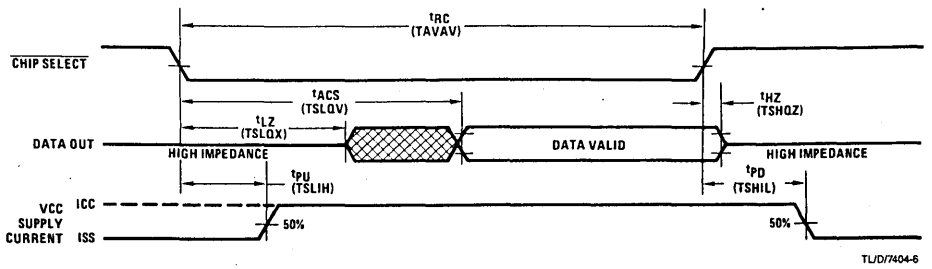
Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{RC}	TAVAV	Read Cycle Time	45		55		70		ns
t_{AA}	TAVQV	Address Access Time		45		55		70	ns
t_{ACS1}	TSLQV1	Chip Select Access Time (Notes 4 and 5)		45		55		70	ns
t_{ACS2}	TSLQV2	Chip Select Access Time (Notes 4 and 6)		55		65		80	ns
t_{LZ}	TSLQX	Chip Select to Output Active (Note 7)	20		20		20		ns
t_{HZ}	TSHQZ	Chip Deselect to Output TRI-STATE (Note 7)	0	20	0	20	0	20	ns
t_{OH}	TAXQX	Output Hold from Address Change	5		5		5		ns
t_{PU}	TSLIH	Chip Select to Power-Up	0		0		0		ns
t_{PD}	TSHIL	Chip Deselect to Power-Down		30		30		30	ns

Read Cycle Waveforms*

Read Cycle 1 (Continuous Selection $\overline{CS}$ = VIL, $\overline{WE}$ = VIH)



Read Cycle 2 (Chip Select Switched, $\overline{WE}$ = VIH) (Note 4)



Note 4: Addresses must be valid coincident with or prior to the chip select transition from high to low.
Note 5: Chip deselected longer than 55 ns.
Note 6: Chip deselected less than 55 ns.
Note 7: Measured ±50 mV from steady state voltage. This parameter is sampled and not 100% tested.

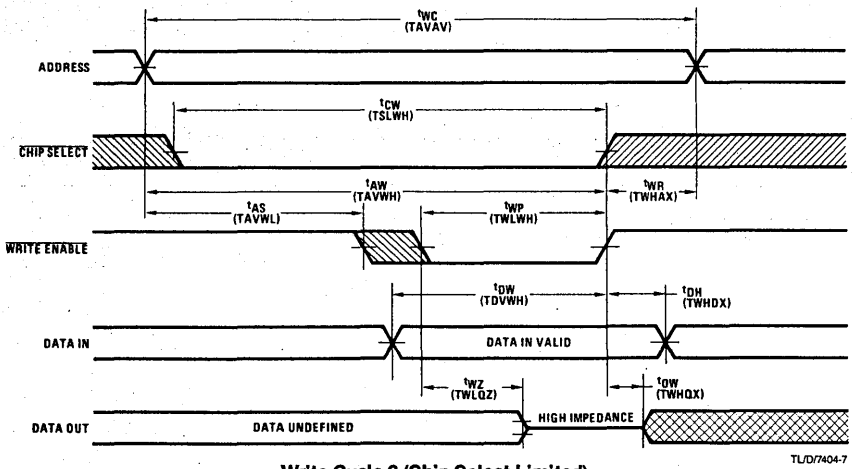
*The symbols in parentheses are proposed industry standard.

Write Cycle AC Electrical Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$ (Note 1)

Symbol		Parameter	NMC2148H-2		NMC2148H-3 NMC2148H-3L		NMC2148H NMC2148H-L		Units
Alternate	Standard		Min	Max	Min	Max	Min	Max	
t_{WC}	TAVAV	Write Cycle Time	45		55		70		ns
t_{CW}	TSLWH	Chip Select to End of Write	40		50		65		ns
t_{AW}	TAVWH	Address Valid to End of Write	40		50		65		ns
t_{AS}	TAVSL TAVWL	Address Set-Up Time	0		0		0		ns
t_{WP}	TWLWH	Write Pulse Width	35		40		50		ns
t_{WR}	TWHAX	Write Recovery Time	5		5		5		ns
t_{DW}	TDVWH	Data Set-Up Time	20		20		25		ns
t_{DH}	TWHDX	Data Hold Time	0		0		0		ns
t_{WZ}	TWLQZ	Write Enable to Output TRI-STATE (Note 7)	0	15	0	20	0	25	ns
t_{OW}	TWHQX	Output Active from End of Write (Note 7)	0		0		0		ns

Write Cycle Waveforms* (Note 8)

Write Cycle 1 (Write Enable Limited)



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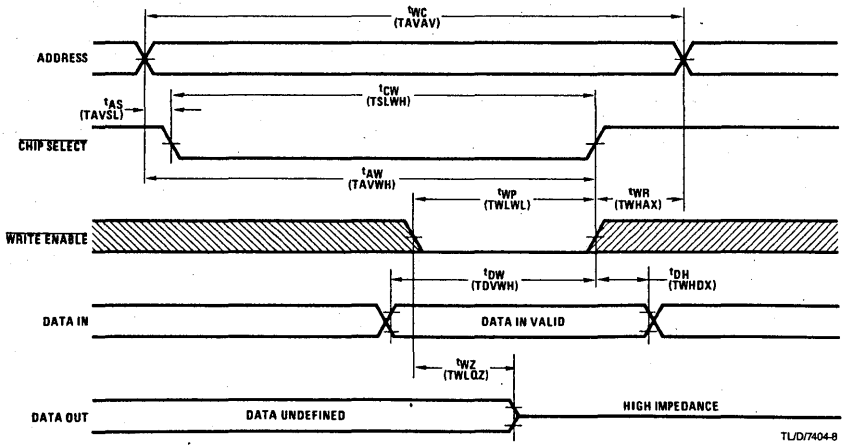
Write Cycle 2 (Chip Select Limited)



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Note 8: The output remains TRI-STATE if the $\overline{CS}$ and $\overline{WE}$ go high simultaneously. $\overline{WE}$ or $\overline{CS}$ or both must be high during the address transitions to prevent an erroneous write.

*Symbols in parentheses are proposed industry standard.

Section 5

CMOS Static RAMs

5

Section 5—CMOS Static RAMs

National Semiconductor

PRELIMINARY

microCMOS

NMC6164/6164L 8192 x 8-Bit Static RAM

General Description

The NMC6164/6164L is a 8192-word by 8-bit, new-generation static RAM. It is fabricated with National's proprietary microCMOS double-polysilicon technology which combines high performance and high density with low power consumption and excellent reliability.

The NMC6164/6164L operates with a single 5V power supply with ± 10% tolerance. Additional battery back-up operation is available (L version) for data retention down to 2V, with low standby current.

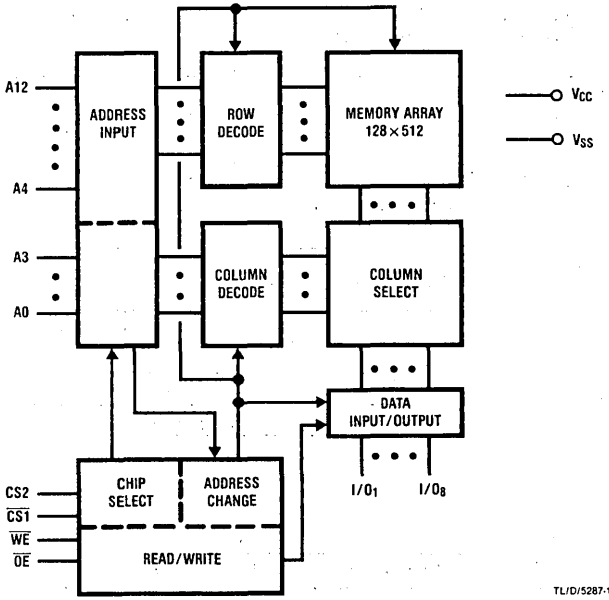
Packaging is in standard 28-pin DIP and is available in both plastic and CERDIP.

In addition to the inputs and outputs being TTL compatible, the outputs are also CMOS compatible, in that capacitive loads are driven to V_{CC} or V_{SS}.

Features

- Single power supply: 5V ± 10%
- Fast access time 100 ns/120 ns/150 ns max
- Equal access and cycle times
- Completely static RAM: no clock or timing strobe required
- Low standby power and low power operation
  Standby: 10 μW, typical
  Operation: 15 mW/MHz, typical
- Battery back-up operation available (L version) with data retention supply voltage: 2V–5.5V
- Common data input and output, TRI-STATE® output
- TTL compatible: all inputs and outputs
- CMOS compatible: outputs drive capacitive loads to V_{CC} or V_{SS}
- Standard 28-pin package configuration

Block and Connection Diagrams



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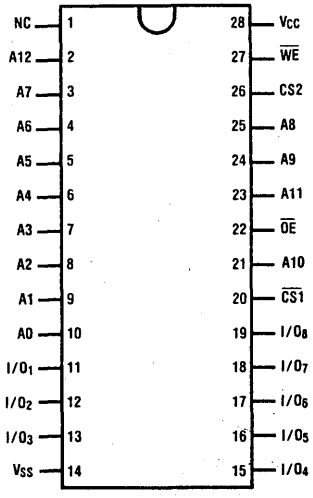
Dual-In-Line Package



TOP VIEW

TL/D/5287-2

Truth Table

Mode	$\overline{WE}$	$\overline{CS1}$	CS2	$\overline{OE}$	I/O	Current
Not Selected (Power Down)	*	H	*	*	Hi-Z	I_{SB}, I_{SB1}
	*	*	L	*	Hi-Z	I_{SB}, I_{SB1}
Output Disabled	H	L	H	H	Hi-Z	I_{CC}, I_{CC1}
Read	H	L	H	L	D_{OUT}	I_{CC}, I_{CC1}
Write	L	L	H	*	D_{IN}	I_{CC}, I_{CC1}

*Don't care (H or L) H = Logic HIGH Level L = Logic LOW Level

Order Number NMC6164J (NMC6164LJ)
NS Package Number J28A
Order Number NMC6164N (NMC6164LN)
NS Package Number N28B

5

Absolute Maximum Ratings

Voltage on Any Pin Relative to V_{SS}	−0.5V to −7V
Storage Temperature, T_{STG}	−55°C to +125°C
Temperature Under Bias, T_{BIAS}	−10°C to +85°C
Power Dissipation, P_D	1.0W
Current Through Any Pin	100 mA

Recommended DC Operating Conditions

	Min	Max	Units
V_{CC} Supply Voltage	4.5	5.5	V
V_{SS} Supply Voltage	0	0	V
V_{IH}, Input High Voltage (Logic 1)			
TTL	2.2	6.0	V
CMOS	$V_{CC}-0.2$	$V_{CC}+0.2$	V
V_{IL}, Input Low Voltage (Logic 0)			
TTL	−0.3	0.8	V
CMOS	−0.2	0.2	V
T_{OPR}, Operating Temp	0	70	°C

DC Electrical Characteristics at recommended operating conditions

Symbol		Parameter	Conditions	Min	Max	Units
I_{LI}		Input Leakage Current	$V_{IN}=V_{SS}$ to V_{CC}	−2	2	μA
I_{LO}		Output Leakage Current	$\overline{CS1}=V_{IH}$ or CS2 = V_{IL} or $\overline{OE}=V_{IH}$ $V_{I/O}=V_{SS}$ to V_{CC}	−2	2	μA
I_{CC}		Active Quiescent Current, TTL	All Inputs at TTL Levels $\overline{CS1}=V_{IL}$, TTL or CS2 = V_{IH}, TTL $I_{I/O}=0$ mA		25	mA
I_{CC}	Std.	Active Quiescent Current, CMOS	All Inputs at CMOS Levels $\overline{CS1}=V_{IL}$, CMOS and CS2 = V_{IH}, CMOS $I_{I/O}=0$ mA		2	mA
	L				100	μA
I_{CC1}		Average Operating Current, TTL	Duty Cycle = 100% All Inputs at TTL Levels		60	mA
		Average Operating Current, CMOS	Duty Cycle = 100% All Inputs at CMOS Levels		40	mA
I_{SB}	Std.	Standby Power Supply Current	$\overline{CS1}=V_{IH}$, TTL or CS2 = V_{IL}, TTL $I_{I/O}=0$ mA		4	mA
	L				2	mA
I_{SB1}	Std.	Standby Power Supply Current	$\overline{CS1}=V_{IH}$, CMOS or CS2 = V_{IL}, CMOS		2	mA
	L				100	μA
V_{OL}		Output Low Voltage, TTL	$I_{OL}=2.1$ mA		0.4	V
		Output Low Voltage, CMOS	$I_{OL}=\pm 10$ μA	−0.2	0.2	V
V_{OH}		Output High Voltage, TTL	$I_{OH}=-1.0$ mA	2.4		V
		Output High Voltage, CMOS	$I_{OH}=\pm 10$ μA	$V_{CC}-0.2$	$V_{CC}+0.2$	V

Capacitance

Symbol	Parameter	Conditions	Max	Units
C_{IN}	Input Capacitance	$V_{IN}=0$V (Note 5)	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}=0$V (Note 5)	8	pF

AC Electrical Characteristics (Note 1) (Standard and L Versions)

Symbol	Parameter	NMC6164/6164L						Units
		-10*		-12*		-15*		
		Min	Max	Min	Max	Min	Max	
READ CYCLE (Note 4)								
t_{RC}	Read Cycle Time	100		120		150		ns
t_{AA}	Address Access Time		100		120		150	ns
t_{CO1}	Chip Selection ($\overline{CS1}$) to Output Valid		100		120		150	ns
t_{CO2}	Chip Selection (CS2) to Output Valid		100		120		150	ns
t_{OE}	Output Enable ($\overline{OE}$) to Output Valid		50		60		70	ns
t_{LZ1}	Chip Selection ($\overline{CS1}$) to Output Active	10		10		15		ns
t_{LZ2}	Chip Selection (CS2) to Output Active	10		10		15		ns
t_{OLZ}	Output Enable ($\overline{OE}$) to Output Active	5		5		5		ns
t_{HZ1}	Chip Deselection (CS1) to Output in Hi-Z (Notes 2 and 3)	0	35	0	40	0	50	ns
t_{HZ2}	Chip Deselection (CS2) to Output in Hi-Z (Notes 2 and 3)	0	35	0	40	0	50	ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z (Notes 2 and 3)	0	35	0	40	0	50	ns
t_{OHA}	Output Hold from Address Change	10		10		15		ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	100		120		150		ns
t_{CW1}	Chip Selection ($\overline{CS1}$) to End of Write (Note 10)	80		85		100		ns
t_{CW2}	Chip Selection ($\overline{CS2}$) to End of Write	80		85		100		ns
t_{AS}	Address Set-Up Time (Note 7)	0		0		0		ns
t_{AW}	Address Valid to End of Write	80		85		100		ns
t_{WP}	Write Pulse Width (Note 6)	60		70		90		ns
t_{WR1}	Write Recovery Time from $\overline{CS1}$ (Note 8)	0		5		10		ns
t_{WR2}	Write Recovery Time from CS2 (Note 8)	0		5		10		ns
t_{WHZ}	Beginning of Write to Output in Hi-Z (Note 9)	0	35	0	40	0	50	ns
t_{DW}	Data Valid to Write Time Overlap	35		40		50		ns
t_{DH}	Data Hold from End of Write	0		0		0		ns
t_{OHZ}	Output Disable ($\overline{OE}$) to Output in Hi-Z	0	35	0	40	0	50	ns
t_{OW}	Output Active from End of Write	5		5		10		ns

*Applies to Standard and L Versions.

Note 1: AC test conditions $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$.

Note 2: t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are determined as:
High to TRI-STATE measured as V_{OH} (DC) − 0.1V
Low to TRI-STATE measured as V_{OL} (DC) + 0.1V

Note 3: At any given temperature and voltage condition, $t_{HZ\,MAX}$ is less than $t_{LZ\,MIN}$, both for a given device and from device to device.

Note 4: $\overline{WE}$ is high for read cycle.

Note 5: $T_A = 25°C$, f = 1.0 MHz. This parameter is sampled and not 100% tested.

Note 6: A write occurs during the overlap (t_{WP}) of a low $\overline{CS1}$ and a high CS2 and a low $\overline{WE}$.

Note 7: t_{AS} is measured from the address changes to the beginning of the write.

Note 8: t_{WR} is measured from the earliest of $\overline{CS1}$ or $\overline{WE}$ going high or CS2 going low to the end of the write cycle.

Note 9: If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. At this time, the data input signals of opposite phase to the outputs must not be applied.

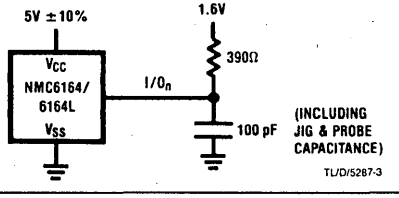
Note 10: If the $\overline{CS1}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, the outputs will remain in a Hi-Z state.

Note 11: CS2 controls the address buffers, $\overline{WE}$ buffer, $\overline{CS1}$ buffer, D_{IN} buffer and $\overline{OE}$ buffer. When CS2 controls the data retention mode, V_{IN} level (address, $\overline{WE}$, $\overline{CS1}$, $\overline{OE}$) can be in the high impedance state. When $\overline{CS1}$ controls the data retention mode, CS2 must be at V_{IH}, CMOS. All other input levels (address, $\overline{WE}$, I/O) can be in the high impedance state.

AC Test Conditions:

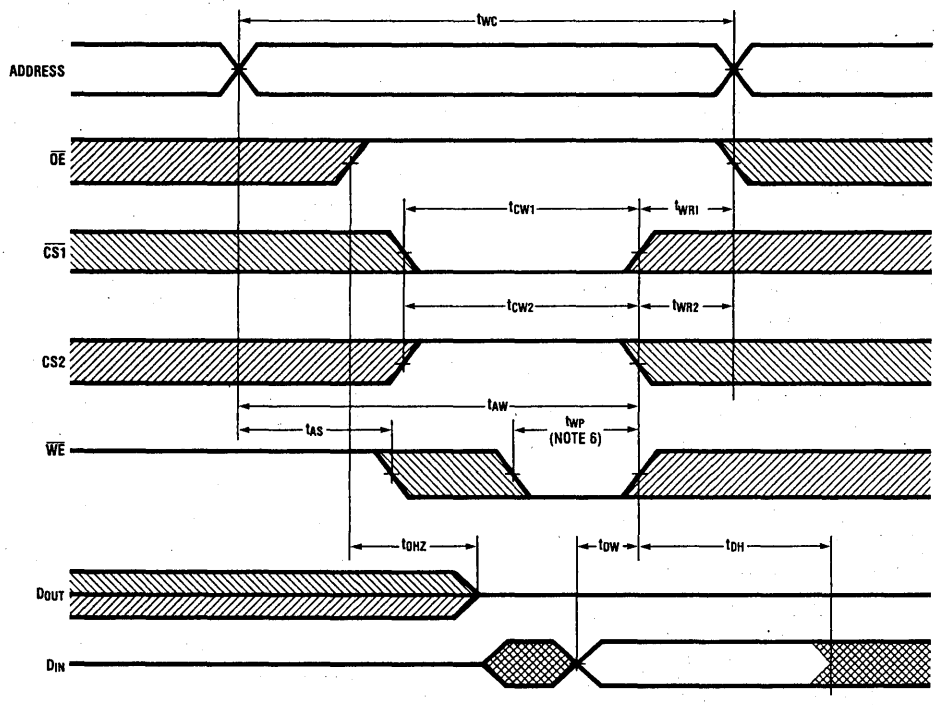
Input pulse levels $V_{IH} = 3.0V$, $V_{IL} = 0.0V$
Input rise and fall times 5 ns
All input and output timing reference levels 1.5V

AC Test Load



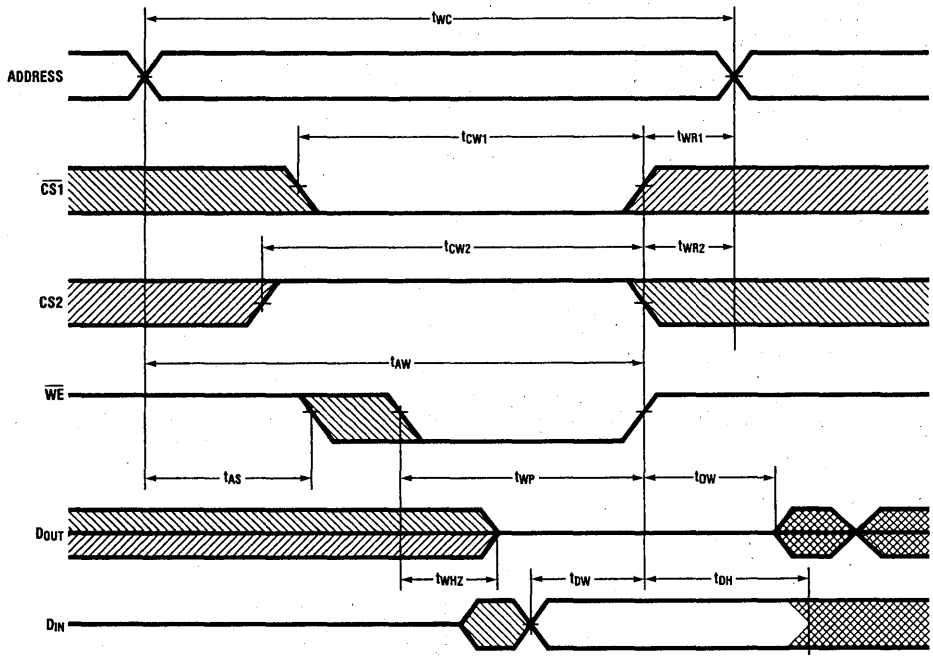
Timing Waveforms

Write Cycle 1 ($\overline{OE}$ Clocked)



TL/D/5287-4

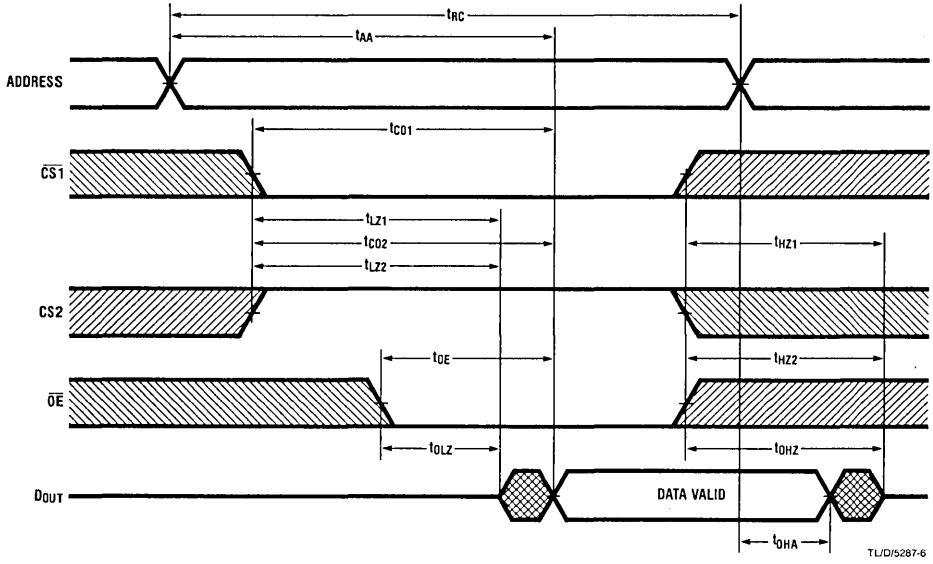
Write Cycle 2 ($\overline{OE}$ Low Fixed)



TL/D/5287-5

Timing Waveforms (Continued)

Read Cycle

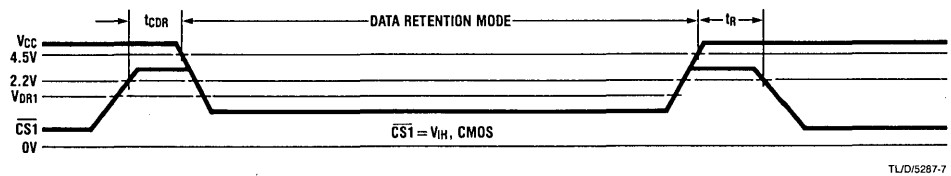


Low V_{CC} Data Retention (L Version)

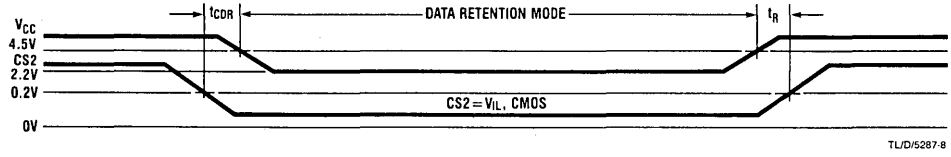
Symbol	Parameter	Conditions	Min	Max	Units
V_{DR1}	V_{CC} for Data Retention	$\overline{CS1} > V_{IH}$, CMOS $CS2 > V_{IH}$, CMOS	2.0		V
V_{DR2}	V_{CC} for Data Retention	$CS2 < V_{IL}$, CMOS	2.0		V
I_{CCDR1}	Data Retention Current (Note 11)	$V_{CC} = 2V$ $\overline{CS1} > V_{IH}$, CMOS $CS2 > V_{IH}$, CMOS		40	μA
I_{CCDR2}	Data Retention Current (Note 11)	$V_{CC} = 2V$ $CS2 < V_{IL}$, CMOS		40	μA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0		ns
t_R	Operation Recovery Time	See Retention Waveform	t_{RC}		ns

Low V_{CC} Data Retention Waveforms

No. 1 (CS1 Controlled)



No. 2 (CS2 Controlled)



Section 6

EPROMs

6

Section Contents

National Semiconductor

MM2716 16,384-Bit (2048 × 8) UV Erasable PROM

Parameter/Order Number	MM2716	MM2716-1	MM2716E
Access Time (ns)	450	350	450
V_{CC} Power Supply	5V ±5%	5V ±10%	5V ±5%

General Description

The MM2716 is a high speed 16k UV erasable and electrically reprogrammable EPROM, ideally suited for applications where fast turnaround and pattern experimentation are important requirements.

The MM2716 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel MOS silicon gate technology.

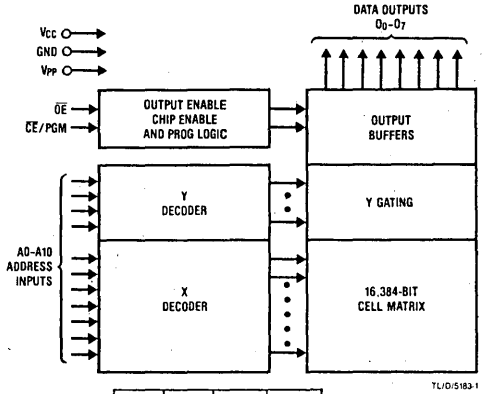
Features

- Access time down to 350 ns
- Low power consumption
  Active power: 525 mW max
  Standby power: 132 mW max (75% savings)
- Single 5V power supply
- Extended temperature range available (MM2716E), −40°C to +85°C, 450 ns ±5% power supply
- Pin compatible to National's higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- TRI-STATE® output

Block and Connection Diagrams

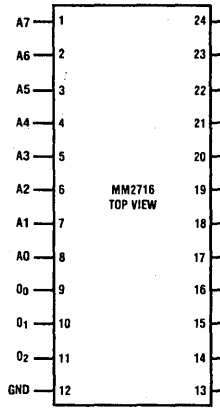
Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect



27C256 27256	27C128 27128	27C64 2764	27C32 2732			27C32 2732	27C64 2764	27C128 27128	27C256 27256
VPP	VPP	VPP		A7	1		VCC	VCC	VCC
A12	A12	A12		A6	2		$\overline{PGM}$	$\overline{PGM}$	A14
A7	A7	A7	A7	A5	3	VCC	NC	A13	A13
A6	A6	A6	A6	A4	4	A8	A8	A8	A8
A5	A5	A5	A5	A3	5	A9	A9	A9	A9
A4	A4	A4	A4	A2	6	A11	A11	A11	A11
A3	A3	A3	A3	A1	7	$\overline{OE}$/VPP	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A2	A2	A2	A2	A0	8	A10	A10	A10	A10
A1	A1	A1	A1	O0	9	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
A0	A0	A0	A0	O1	10	O7	O7	O7	O7
O0	O0	O0	O0	O2	11	O6	O6	O6	O6
O1	O1	O1	O1	GND	12	O5	O5	O5	O5
O2	O2	O2	O2			O4	O4	O4	O4
GND	GND	GND	GND			O3	O3	O3	O3

Dual-In-Line Package



TL/D/5183-2

NS Package Number J24A-Q

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the MM2716 pins.

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
V_{PP} Supply Voltage with Respect to Ground During Program	+26.5V to −0.3V
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 9)

Temperature Range	
MM2716, MM2716-1	0°C to +70°C
MM2716E	−40°C to +85°C
V_{CC} Power Supply (Notes 2 and 3)	
MM2716, MM2716E	5V ± 5%
MM2716-1	5V ± 10%
V_{PP} Power Supply (Note 3)	V_{CC}

READ OPERATION

DC and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE} = V_{IH}$		10	25	mA
I_{CC2} (Note 3)	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$, I/O = 0 mA		57	100	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V

AC Characteristics

Symbol	Parameter	Conditions	MM2716E MM2716		MM2716-1		Units
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		450		350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		450		350	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		120		120	ns
t_{DF}	Output Enable High to Output Float	$\overline{CE} = V_{IL}$	0	100	0	100	ns
t_{OH} (Note 5)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

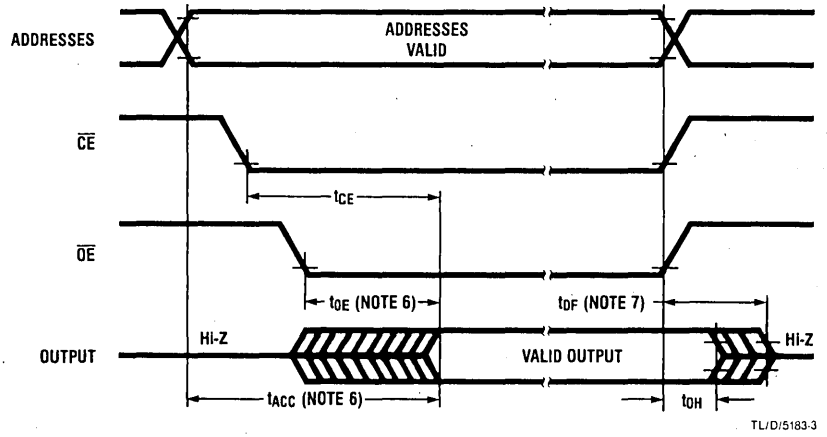
Capacitance (Note 5) ($T_A = +25°C$, f = 1 MHz)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 2)



TL/D/5183-3

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. $I_{CC2} \leq$ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 5: This parameter is only sampled and is not 100% tested.

Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 7: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH} (DC) $- 0.10V$.
Low to TRI-STATE, the measured V_{OL} (DC) $+ 0.10V$

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

PROGRAMMING CHARACTERISTICS (Note 1)

DC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (for Any Input)	$V_{IN} = V_{CC}$ or GND			10	μA
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}/PGM = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				100	mA
V_{IL}	Input Low Level		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC}+1$	V

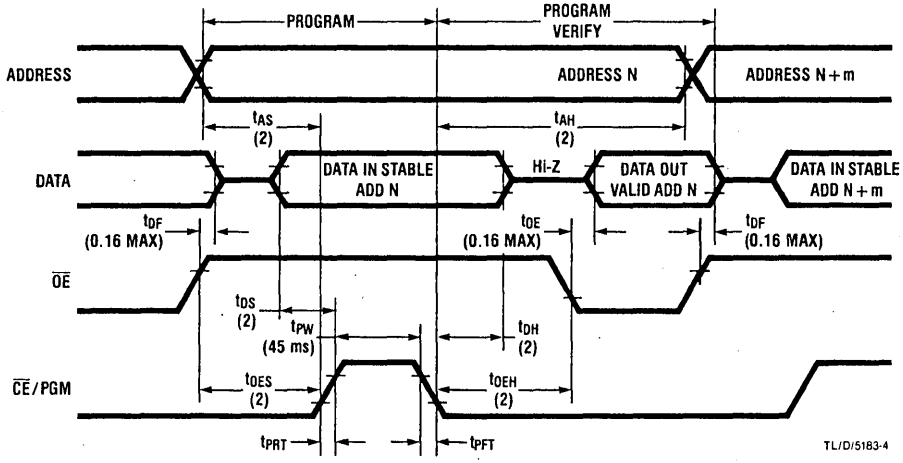
AC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			μs
t_{DS}	Data Set-Up Time		2			μs
t_{AH}	Address Hold Time		2			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		160	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$			160	ns
t_{PW}	Program Pulse Width		45	50	55	ms
t_{PRT}	Program Pulse Rise Time		5			ns
t_{PFT}	Program Pulse Fall Time		5			ns

AC Test Conditions

V_{CC}	$5V \pm 5\%$
V_{PP}	$25V \pm 1V$
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3) ($V_{PP} = 25V \pm 1V$, $V_{CC} = 5V \pm 5\%$)



Note: All times shown in parentheses are minimum times and are in μs unless otherwise specified.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The MM2716 must not be inserted into or removed from a board with V_{PP} at 25V ± 1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description

DEVICE OPERATION

The five modes of operation of the MM2716 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a 5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

Read Mode

The MM2716 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The MM2716 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The MM2716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because MM2716s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 21 (V_{PP}) will damage the MM2716.

Initially, and after each erasure, all bits of the MM2716 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The MM2716 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The MM2716 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple MM2716s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled MM2716s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled MM2716s.

Program Inhibit

Programming multiple MM2716s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel MM2716s may be common. A TTL level program pulse applied to an MM2716's $\overline{CE}$/PGM input with V_{PP} at 25V will program that MM2716. A low level $\overline{CE}$/PGM input inhibits the other MM2716 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at V_{CC}.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	25	5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	25	5	Hi-Z

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the MM2716 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 Å - 4000 Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical MM2716 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the MM2716 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the MM2716 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the MM2716 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The MM2716 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

National Semiconductor

MM2758 8,192-Bit (1024 x 8) UV Erasable PROM

General Description

The MM2758 is a high speed 8k UV erasable and electrically reprogrammable EPROM, ideally suited for applications where fast turnaround and pattern experimentation are important requirements.

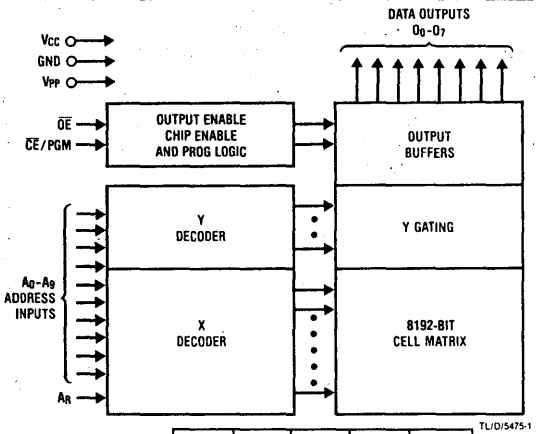
The MM2758 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, N-channel MOS silicon gate technology.

Features

- Access time—450 ns
- Low power consumption
  - Active power: 525 mW max
  - Standby power: 132 mW max (75% savings)
- Single 5V power supply
- Pin compatible to National's higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- TRI-STATE® output

Block and Connection Diagrams



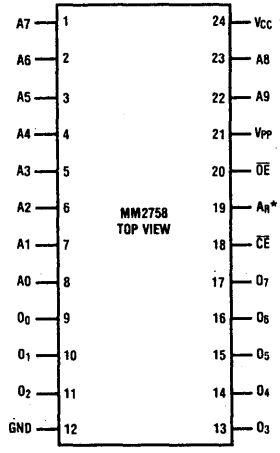
TL/D/5475-1

Pin Names

A0-A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0-O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect
*A_R	Select Reference Input Level

27C256 27256	27C128 27128	27C64 2764	27C32 2732	27C16 2716
V_{PP}	V_{PP}	V_{PP}		
A12	A12	A12		
A7	A7	A7	A7	A7
A6	A6	A6	A6	A6
A5	A5	A5	A5	A5
A4	A4	A4	A4	A4
A3	A3	A3	A3	A3
A2	A2	A2	A2	A2
A1	A1	A1	A1	A1
A0	A0	A0	A0	A0
O_0	O_0	O_0	O_0	O_0
O_1	O_1	O_1	O_1	O_1
O_2	O_2	O_2	O_2	O_2
GND	GND	GND	GND	GND

Dual-In-Line Package



27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C256 27256
		V_{CC}	V_{CC}	V_{CC}
		$\overline{PGM}$	$\overline{PGM}$	A14
V_{CC}	V_{CC}	NC	A13	A13
A8	A8	A8	A8	A8
A9	A9	A9	A9	A9
V_{PP}	A11	A11	A11	A11
$\overline{OE}$	$\overline{OE}$/V_{PP}	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A10	A10	A10	A10	A10
$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
O_7	O_7	O_7	O_7	O_7
O_6	O_6	O_6	O_6	O_6
O_5	O_5	O_5	O_5	O_5
O_4	O_4	O_4	O_4	O_4
O_3	O_3	O_3	O_3	O_3

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the MM2758 pins.

*For MM2758A, $A_R = V_{IL}$ for all operating modes.

*For MM2758B, $A_R = V_{IH}$ for all operating modes.

Order Number MM2758Q-A or MM2758Q-B
NS Package Number J24A-Q

TL/D/5475-2

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6.5V to −0.3V
V_{PP} Supply Voltage with Respect to Ground During Program	+26.5V to −0.3V
Power Dissipation	1.5W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 9)

Temperature Range	0°C-70°C
V_{CC} Power Supply (Notes 2 and 3)	5V ± 5%
V_{PP} Power Supply (Note 3)	V_{CC}

READ OPERATION

DC and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Standby)	$\overline{CE} = V_{IH}$		10	25	mA
I_{CC2} (Note 3)	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$, I/O = 0 mA		57	100	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V

AC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		450	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		120	ns
t_{DF}	Output Enable High to Output Float	$\overline{CE} = V_{IL}$	0	100	ns
t_{OH} (Note 5)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		ns

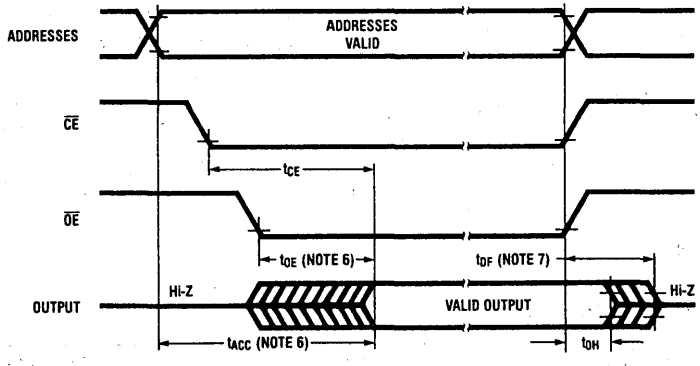
Capacitance (Note 5) ($T_A = +25°C$, f = 1 MHz)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 2)



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Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. $I_{CC2} \leq$ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 5: This parameter is only sampled and is not 100% tested.

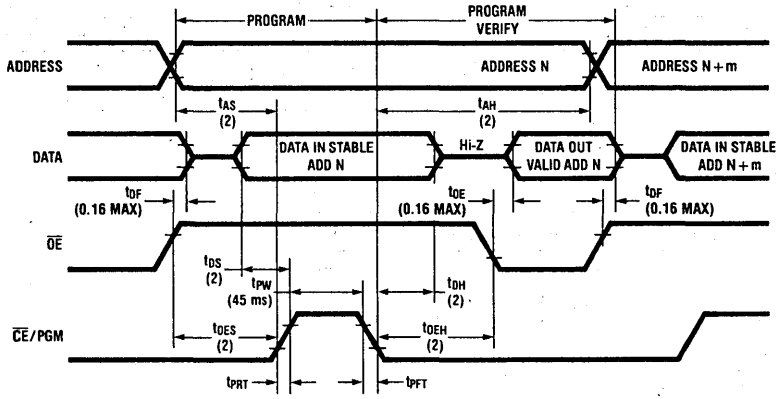
Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 7: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH} (DC) – 0.10V
Low to TRI-STATE, the measured V_{OL} (DC) + 0.10V

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Programming Waveforms (Note 3) ($V_{PP} = 25V \pm 1V$, $V_{CC} = 5V \pm 5\%$)



TL/D/5475-4

Note: All times shown in parentheses are minimum times and are in μs unless otherwise specified.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The MM2758 must not be inserted into or removed from a board with V_{PP} at 25V ± 1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

PROGRAMMING CHARACTERISTICS (Note 1)

DC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (for Any Input)	$V_{IN} = V_{CC}$ or GND			10	μA
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}/PGM = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				100	mA
V_{IL}	Input Low Level		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC}+1$	V

AC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{AS}	Address Set-Up Time		2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			μs
t_{DS}	Data Set-Up Time		2			μs
t_{AH}	Address Hold Time		2			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			μs
t_{DH}	Data Hold Time		2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		160	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$			160	ns
t_{PW}	Program Pulse Width		45	50	55	ms
t_{PRT}	Program Pulse Rise Time		5			ns
t_{PFT}	Program Pulse Fall Time		5			ns

AC Test Conditions

V_{CC}	$5V \pm 5\%$
V_{PP}	$25V \pm 1V$
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Functional Description

DEVICE OPERATION

The five modes of operation of the MM2758 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a 5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

Read Mode

The MM2758 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The MM2758 has a standby mode which reduces the active power dissipation by 75%, from 525 mW to 132 mW. The MM2758 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because MM2758s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 21 (V_{PP}) will damage the MM2758.

Initially, and after each erasure, all bits of the MM2758 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The MM2758 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms, active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms. The MM2758 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming of multiple MM2758s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled MM2758s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled MM2758s.

Program Inhibit

Programming multiple MM2758s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel MM2758s may be common. A TTL level program pulse applied to an MM2758's $\overline{CE}$/PGM input with V_{PP} at 25V will program that MM2758. A low level $\overline{CE}$/PGM input inhibits the other MM2758 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at V_{CC}.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	25	5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	25	5	Hi-Z

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the MM2758 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å-4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical MM2758 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the MM2758 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the MM2758 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the MM2758 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The MM2758 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

Note: The MM2758 may take up to 60 minutes for complete erasure to occur.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

National Semiconductor

microCMOS

NMC27C16 16,384-Bit (2048 × 8) UV Erasable CMOS PROM

Parameter/Order Number	NMC27C16-35	NMC27C16-45 NMC27C16H-45
Access Time (ns)	350	450
V_{CC} Power Supply	5V ± 5%	5V ± 5%

General Description

The NMC27C16 is a high speed 16k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

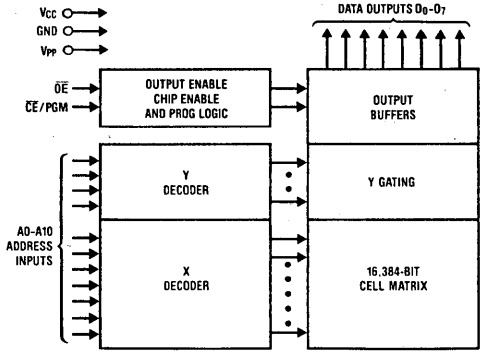
The NMC27C16 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, microCMOS silicon gate technology.

Features

- Access time: 350 ns, 450 ns
- Low CMOS power consumption
  - Active power: 26.25 mW max
  - Standby power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range available (NMC27C16E-45), −40°C to +85°C, 450 ns ± 5% power supply
- 10 ms programming available (NMC27C16H-45), an 80% time savings
- Pin compatible to MM2716 and National's higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- TRI-STATE® output

Block and Connection Diagrams



TL/D/5275-1

Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect

Dual-In-Line Package

27C256 27256	27C128 27128	27C64 2764	27C32 2732				27C32 2732	27C64 2764	27C128 27128	27C256 27256
VPP	VPP	VPP		A7	1	24	VCC		VCC	VCC	VCC
A12	A12	A12		A6	2	23	A8		PGM	PGM	A14
A7	A7	A7	A7	A5	3	22	A9	VCC	NC	A13	A13
A6	A6	A6	A6	A4	4	21	VPP	A8	A8	A8	A8
A5	A5	A5	A5	A3	5	20	$\overline{OE}$	A9	A9	A9	A9
A4	A4	A4	A4	A2	6	19	A10	A11	A11	A11	A11
A3	A3	A3	A3	A1	7	18	$\overline{CE}$	$\overline{OE}$/VPP	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$
A2	A2	A2	A2	A0	8	17	O7	A10	A10	A10	A10
A1	A1	A1	A1	O0	9	16	O6	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$	$\overline{CE}$
A0	A0	A0	A0	O1	10	15	O5	O7	O7	O7	O7
O0	O0	O0	O0	O2	11	14	O4	O6	O6	O6	O6
O1	O1	O1	O1	GND	12	13	O3	O5	O5	O5	O5
O2	O2	O2	O2					O4	O4	O4	O4
GND	GND	GND	GND					O3	O3	O3	O3

NMC27C16
TOP VIEW

TL/D/5275-2

NS Package Number J24A-Q

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C16 pins.

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground	V_{CC} +0.3V to GND −0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 9)

Temperature Range	
NMC27C16-35, NMC27C16-45, NMC27C16H-45	0°C to +70°C
NMC27C16E-45	−40°C to +85°C
V_{CC} Power Supply (Notes 2 and 3)	5V ± 5%
V_{PP} Power Supply (Note 3)	V_{CC}

READ OPERATION

DC and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 4)	Max	Units
I_{LI}	Input Load Current	$V_{IN} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1} (Note 3)	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{IH} or V_{IL}, f = 1 MHz, I/O = 0 mA		2	10	mA
I_{CC2} (Note 3)	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE} =$ VIL, Inputs = V_{CC} or GND f = 1 MHz, I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Characteristics

Symbol	Parameter	Conditions	NMC27C16-35		NMC27C16E-45 NMC27C16-45 NMC27C16H-45		Units
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		350		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		350		450	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$		120		120	ns
t_{DF}	Output Enable High to Output Float	$\overline{CE} = V_{IL}$	0	100	0	100	ns
t_{OH} (Note 5)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

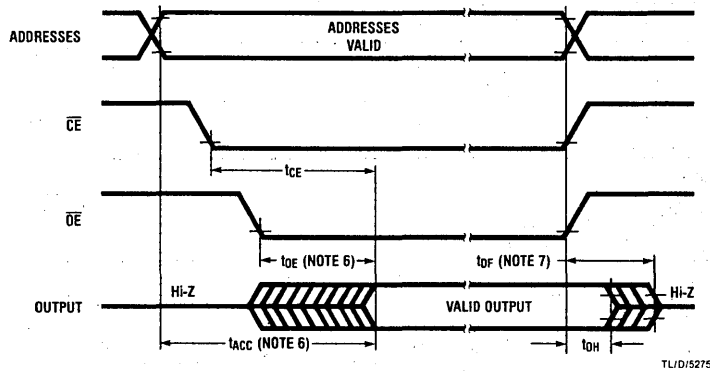
Capacitance (Note 5) (T_A = +25°C, f = 1 MHz)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms (Note 2)



Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

Note 3: V_{PP} may be connected to V_{CC} except during programming. I_{CC1} ≤ the sum of the I_{CC} active and I_{PP} read currents.

Note 4: Typical values are for T_A = +25°C and nominal supply voltages.

Note 5: This parameter is only sampled and is not 100% tested.

Note 6: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

Note 7: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 8: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 9: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 10: The NMC27C16 requires one address transition after initial power-up to reset the outputs.

Note 11: The outputs must be restricted to V_{CC} + 0.3V to avoid latch-up and device damage.

PROGRAMMING CHARACTERISTICS (Note 1)

DC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (for Any Input)	$V_{IN} = V_{CC}$ or GND			10	μA
I_{PP}	V_{PP} Supply Current During Programming Pulse	$\overline{CE}/PGM = V_{IH}$			30	mA
I_{CC}	V_{CC} Supply Current				10	mA
V_{IL}	Input Low Level		−0.1		0.8	V
V_{IH}	Input High Level		2.0		$V_{CC}+1$	V

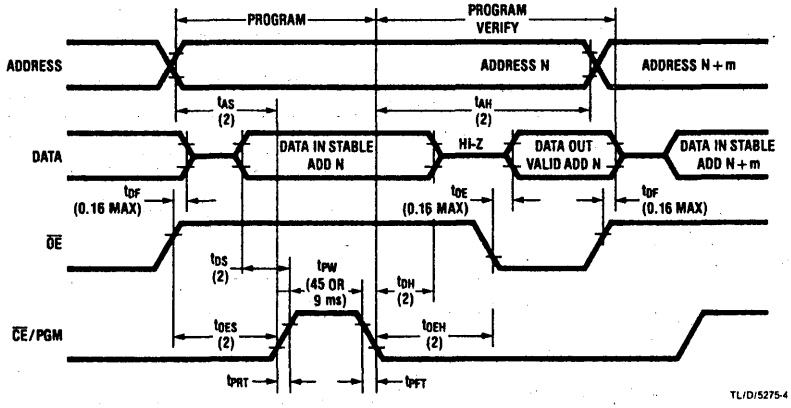
AC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	NMC27C16 Devices			NMC27C16H-45			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Set-Up Time		2			2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			2			μs
t_{DS}	Data Set-Up Time		2			2			μs
t_{AH}	Address Hold Time		2			2			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			2			μs
t_{DH}	Data Hold Time		2			2			μs
t_{DF}	Output Enable to Output Float Delay	$\overline{CE}/PGM = V_{IL}$	0		160	0		160	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE}/PGM = V_{IL}$			160			160	ns
t_{PW}	Program Pulse Width		45	50	55	9	10	11	ms
t_{PRT}	Program Pulse Rise Time		5			5			ns
t_{PFT}	Program Pulse Fall Time		5			5			ns

AC Test Conditions

V_{CC}	5V ± 5%
V_{PP}	25V ± 1V
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.8V to 2.2V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3) ($V_{PP} = 25V \pm 1V$, $V_{CC} = 5V \pm 5\%$)



Note: All times shown in parentheses are minimum and in μs unless otherwise specified.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C16 must not be inserted into or removed from a board with V_{PP} at 25V ± 1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C16 are listed in Table I. It should be noted that all inputs for the five modes are at TTL levels. The power supplies required are a 5V V_{CC} and a V_{PP}. The V_{PP} power supply must be at 25V during the three programming modes, and must be at 5V in the other two modes.

Read Mode

The NMC27C16 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs t_{OE} after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$. The NMC27C16 requires one address transition after initial power-up to reset the outputs.

Standby Mode

The NMC27C16 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C16 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because NMC27C16s are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connections. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 21 (V_{PP}) will damage the NMC27C16.

Initially, and after each erasure, all bits of the NMC27C16 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C16 is in the programming mode when the V_{PP} power supply is at 25V and $\overline{OE}$ is at V_{IH}. It is required that a 0.1 μF capacitor be placed across V_{PP}, V_{CC} to ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms (10 ms for the NMC27C16H-45), active high, TTL program pulse is applied to the $\overline{CE}$/PGM input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms (11 ms for the NMC27C16H-45). The NMC27C16 must not be programmed with a DC signal applied to the $\overline{CE}$/PGM input.

Programming multiple NMC27C16s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C16s may be connected together when they are programmed with the same data. A high level TTL pulse applied to the $\overline{CE}$/PGM input programs the paralleled NMC27C16s.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$/PGM (18)	$\overline{OE}$ (20)	V_{PP} (21)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	V_{CC}	5	D_{OUT}
Standby	V_{IH}	Don't Care	V_{CC}	5	Hi-Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	25	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	25	5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	25	5	Hi-Z

Functional Description (Continued)

Program Inhibit

Programming multiple NMC27C16s in parallel with different data is also easily accomplished. Except for $\overline{CE}$/PGM, all like inputs (including $\overline{OE}$) of the parallel NMC27C16s may be common. A TTL level program pulse applied to an NMC27C16's $\overline{CE}$/PGM input with V_{PP} at 25V will program that NMC27C16. A low level $\overline{CE}$/PGM input inhibits the other NMC27C16 from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify may be performed with V_{PP} at 25V. Except during programming and program verify, V_{PP} must be at V_{CC}.

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C16 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å–4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C16 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC27C16 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the NMC27C16 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C16 is exposure to short wave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The NMC27C16 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

National Semiconductor

microCMOS

NMC27C32 32,768-Bit (4096 × 8) UV Erasable CMOS PROM

Parameter/Order Number	NMC27C32-35	NMC27C32-45 NMC27C32H-45
Access Time (ns)	350	450
V_{CC} Power Supply	5V ± 5%	5V ± 5%

General Description

The NMC27C32 is a high speed 32k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C32 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, microCMOS silicon gate technology.

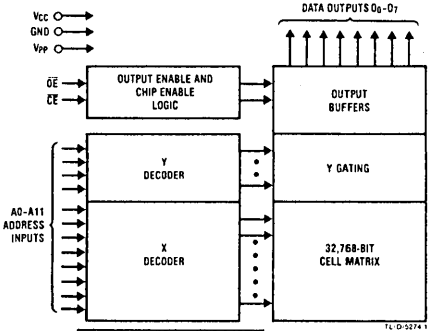
Features

- Access time: 350 ns, 450 ns
- Low CMOS power consumption
  - Active power: 26.25 mW max
  - Standby power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Extended temperature range available (NMC27C32E-45), −40°C to +85°C, 450 ns ±5% power supply
- 10 ms programming available (NMC27C32H-45), an 80% time savings
- Pin compatible to NMC2732 and National's higher density EPROMs
- Static — no clocks required
- TTL compatible inputs/outputs
- Two-line control
- TRI-STATE® output

Block and Connection Diagrams

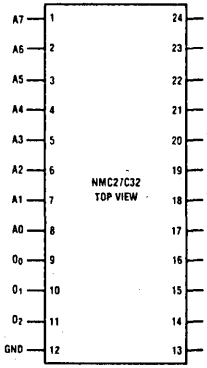
Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect



27C256 27256	27C128 27128	27C64 2764	27C16 2716
VPP	VPP	VPP	
A12	A12	A12	
A7	A7	A7	A7
A6	A6	A6	A6
A5	A5	A5	A5
A4	A4	A4	A4
A3	A3	A3	A3
A2	A2	A2	A2
A1	A1	A1	A1
A0	A0	A0	A0
O0	O0	O0	O0
O1	O1	O1	O1
O2	O2	O2	O2
GND	GND	GND	GND

Dual-In-Line Package



27C16 2716	27C64 2764	27C128 27128	27C256 27256
	VCC	VCC	VCC
	PGM	PGM	A14
VCC	NC	A13	A13
A8	A8	A8	A8
A9	A9	A9	A9
VPP	A11	A11	A11
OE	OE	OE	OE
A10	A10	A10	A10
CE	CE	CE	CE
O7	O7	O7	O7
O6	O6	O6	O6
O5	O5	O5	O5
O4	O4	O4	O4
O3	O3	O3	O3

NS Package Number J24A-Q

TL/D/5274-2

Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C32 pins.

Absolute Maximum Ratings (Note 1)

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input Voltages with Respect to Ground	+6.5V to −0.3V
All Output Voltages with Respect to Ground	V_{CC} + 0.3V to GND − 0.3V
V_{PP} Supply Voltage with Respect to Ground During Programming	+26.5V to −0.3V
Power Dissipation	1.0W
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions (Note 7)

Temperature Range	
NMC27C32-35, NMC27C32-45, NMC27C32H-45	0°C to +70°C
NMC27C32E-45	−40°C to +85°C
V_{CC} Power Supply	5V ± 5%

READ OPERATION

DC and Operating Characteristics

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
I_{LI}	Input Load Current	$V_{IH} = V_{CC}$ or GND			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{CC}$ or GND, $\overline{CE} = V_{IH}$			10	μA
I_{CC1}	V_{CC} Current (Active) TTL Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{IH} or V_{IL}, f = 1 MHz I/O = 0 mA		2	10	mA
I_{CC2}	V_{CC} Current (Active) CMOS Inputs	$\overline{OE} = \overline{CE} = V_{IL}$ Inputs = V_{CC} or GND, f = 1 MHz I/O = 0 mA		1	5	mA
I_{CCSB1}	V_{CC} Current (Standby) TTL Inputs	$\overline{CE} = V_{IH}$		0.1	1	mA
I_{CCSB2}	V_{CC} Current (Standby) CMOS Inputs	$\overline{CE} = V_{CC}$		0.01	0.1	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL1}	Output Low Voltage	I_{OL} = 2.1 mA			0.45	V
V_{OH1}	Output High Voltage	I_{OH} = −400 μA	2.4			V
V_{OL2}	Output Low Voltage	I_{OL} = 0 μA			0.1	V
V_{OH2}	Output High Voltage	I_{OH} = 0 μA	V_{CC} − 0.1			V

AC Characteristics

Symbol	Parameter	Conditions	NMC27C32-35		NMC27C32E-45 NMC27C32-45 NMC27C32H-45		Units
			Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		350		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		350		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		150		150	ns
t_{DF}	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	130	0	130	ns
t_{OH} (Note 3)	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$, Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		ns

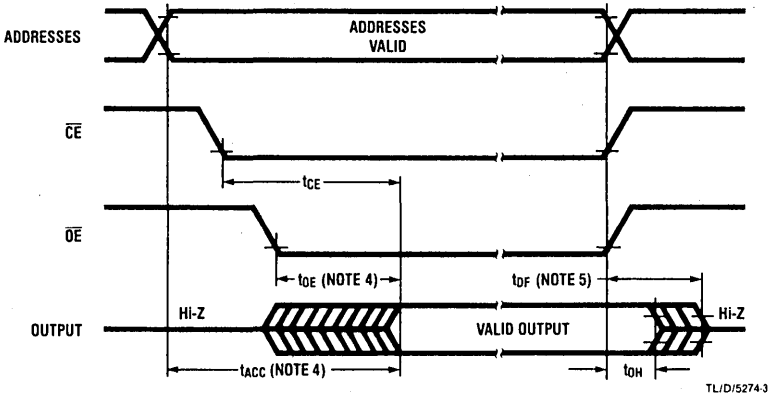
Capacitance (Note 3) ($T_A = +25°C$, f = 1 MHz)

Symbol	Parameter	Conditions	Typ	Max	Units
C_{IN1}	Input Capacitance Except $\overline{OE}/V_{PP}$	$V_{IN} = 0V$	4	6	pF
C_{IN2}	$\overline{OE}/V_{PP}$ Input Capacitance	$V_{IN} = 0V$		20	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	8	12	pF

AC Test Conditions

Output Load	1 TTL Gate and $C_L = 100$ pF
Input Rise and Fall Times	≤ 20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

AC Waveforms



Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: Typical values are for $T_A = +25°C$ and nominal supply voltages.

Note 3: This parameter is only sampled and is not 100% tested.

Note 4: $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impacting t_{ACC}.

Note 5: The t_{DF} compare level is determined as follows:
High to TRI-STATE, the measured V_{OH1} (DC) − 0.10V
Low to TRI-STATE, the measured V_{OL1} (DC) + 0.10V

Note 6: TRI-STATE may be attained using $\overline{OE}$ or $\overline{CE}$.

Note 7: The power switching characteristics of EPROMs require careful device decoupling. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND.

Note 8: The outputs must be restricted to $V_{CC} + 0.3V$ to avoid latch-up and device damage.

PROGRAMMING (Note 1)

DC Programming Characteristics (Notes 2 and 3) ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{CC}$ or GND			10	μA
V_{OL}	Output Low Voltage During Verify	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage During Verify	$I_{OH} = -400$ μA	2.4			V
I_{CC}	V_{CC} Supply Current			2	10	mA
V_{IL}	Input Low Level (All Inputs)		−0.1		0.8	V
V_{IH}	Input High Level (All Inputs Except $\overline{OE}/V_{PP}$)		2.0		$V_{CC}+1$	V
I_{PP}	V_{PP} Supply Current	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{PP}$			30	mA

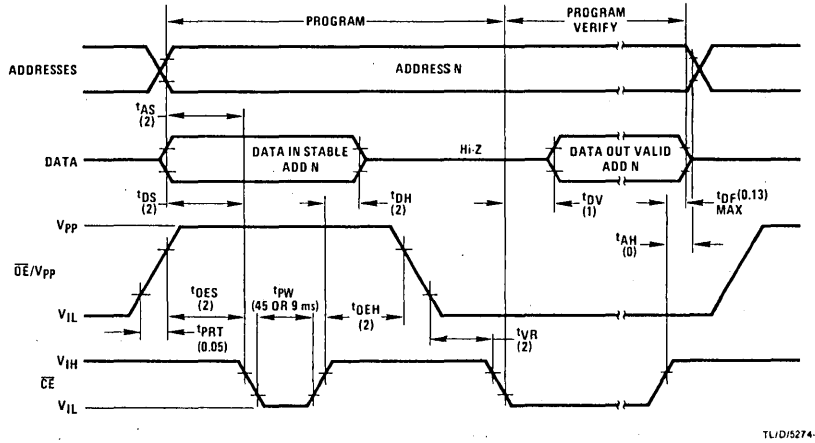
AC Programming Characteristics ($T_A = +25°C \pm 5°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = 25V \pm 1V$)

Symbol	Parameter	Conditions	NMC27C32 Devices			NMC27C32H-45			Units
			Min	Typ	Max	Min	Typ	Max	
t_{AS}	Address Set-Up Time		2			2			μs
t_{OES}	$\overline{OE}$ Set-Up Time		2			2			μs
t_{DS}	Data Set-Up Time		2			2			μs
t_{AH}	Address Hold TIme		0			0			μs
t_{OEH}	$\overline{OE}$ Hold Time		2			2			μs
t_{DH}	Data Hold Time		2			2			μs
t_{DF}	Chip Enable to Output Float Delay		0		130	0		130	ns
t_{DV}	Data Valid from $\overline{CE}$	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IL}$			1			1	μs
t_{PW}	$\overline{CE}$ Pulse Width During Programming		45	50	55	9	10	11	ms
t_{PRT}	$\overline{OE}$ Pulse Rise Time During Programming		50			50			ns
t_{VR}	V_{PP} Recovery Time		2			2			μs

AC Test Conditions

V_{CC}	$5V \pm 5\%$
V_{PP}	$25V \pm 1V$
Input Rise and Fall Times	≤20 ns
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Inputs	1V and 2V
Outputs	0.8V and 2V

Programming Waveforms (Note 3)



Note: All times shown in parentheses are minimum and in μs unless otherwise specified.
The input timing reference level is 1V for a V_{IL} and 2V for a V_{IH}.

Note 1: National's standard product warranty applies only to devices programmed to specifications described herein.

Note 2: V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The NMC27C32 must not be inserted into or removed from a board with V_{PP} at 25V ± 1V to prevent damage to the device.

Note 3: The maximum allowable voltage which may be applied to the V_{PP} pin during programming is 26V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 26V maximum specification. A 0.1 μF capacitor is required across V_{PP}, V_{CC} to GND to suppress spurious voltage transients which may damage the device.

Functional Description

DEVICE OPERATION

The five modes of operation of the NMC27C32 are listed in Table I. A single 5V power supply is required in the read mode. All inputs are TTL levels except for $\overline{OE}/V_{PP}$ during programming. In the program mode the $\overline{OE}/V_{PP}$ input is pulsed from a TTL level to 25V.

Read Mode

The NMC27C32 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{OE}$.

Standby Mode

The NMC27C32 has a standby mode which reduces the active power dissipation by 98%, from 26.25 mW to 0.53 mW. The NMC27C32 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

Output OR-Tying

Because EPROMS are usually used in larger memory arrays, National has provided a 2-line control function that accommodates this use of multiple memory connection. The 2-line control function allows for:

a) the lowest possible memory power dissipation, and

b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded and used as the primary device selecting function, while $\overline{OE}$ (pin 20) be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low power standby modes and that the output pins are active only when data is desired from a particular memory device.

Programming

CAUTION: Exceeding 26.5V on pin 20 (V_{PP}) will damage the NMC27C32.

Initially, and after each erasure, all bits of the NMC27C32 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be presented in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure.

The NMC27C32 is in the programming mode when the $\overline{OE}/V_{PP}$ input is at 25V. It is required that a 0.1 μF capacitor be placed across $\overline{OE}/V_{PP}$, V_{CC}, and ground to suppress spurious voltage transients which may damage the device. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

When the address and data are stable, a 50 ms (10 ms for the NMC27C32H-45), active low, TTL program pulse is applied to the $\overline{CE}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time—either individually, sequentially, or at random. The program pulse has a maximum width of 55 ms (11 ms for the NMC27C32H-45). The NMC27C32 must not be programmed with a DC signal applied to the $\overline{CE}$ input.

Programming of multiple NMC27C32s in parallel with the same data can be easily accomplished due to the simplicity of the programming requirements. Like inputs of the paralleled NMC27C32s may be connected together when they are programmed with the same data. A low level TTL pulse applied to the $\overline{CE}$ input programs the paralleled NMC27C32s.

Program Inhibit

Programming multiple NMC27C32s in parallel with different data is also easily accomplished. Except for $\overline{CE}$, all like inputs (including $\overline{OE}$) of the parallel NMC27C32s may be common. A TTL level program pulse applied to an NMC27C32's $\overline{CE}$ input with $\overline{OE}/V_{PP}$ at 25V will program that NMC27C32. A high level $\overline{CE}$ input inhibits the other NMC27C32s from being programmed.

Program Verify

A verify should be performed on the programmed bits to determine whether they were correctly programmed. The verify is accomplished with $\overline{OE}/V_{PP}$ and $\overline{CE}$ at V_{IL}. Data should be verified t_{DV} after the falling edge of $\overline{CE}$.

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (18)	$\overline{OE}/V_{PP}$ (20)	V_{CC} (24)	Outputs (9-11, 13-17)
Read	V_{IL}	V_{IL}	5	D_{OUT}
Standby	V_{IH}	Don't Care	5	Hi-Z
Program	V_{IL}	V_{PP}	5	D_{IN}
Program Verify	V_{IL}	V_{IL}	5	D_{OUT}
Program Inhibit	V_{IH}	V_{PP}	5	Hi-Z

Functional Description (Continued)

ERASURE CHARACTERISTICS

The erasure characteristics of the NMC27C32 are such that erasure begins to occur when exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000Å-4000Å range. Data shows that constant exposure to room-level fluorescent lighting could erase the typical NMC27C32 in approximately 3 years, while it would take approximately 1 week to cause erasure when exposed to direct sunlight. If the NMC27C32 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the NMC27C32 window to prevent unintentional erasure. Covering the window will also prevent temporary functional failure due to the generation of photo currents.

The recommended erasure procedure for the NMC27C32 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be a minimum of 15W-sec/cm^2. The erasure time with this dosage is approximately 21 minutes using an ultraviolet lamp with a 12,000 μW/cm^2 power rating. The NMC27C32 should be placed within 1 inch of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

An erasure system should be calibrated periodically. The distance from lamp to unit should be maintained at one inch. The erasure time increases as the square of the distance. (If distance is doubled the erasure time increases by a factor of 4.) Lamps lose intensity as they age. When a lamp is changed, the distance has changed or the lamp has aged, the system should be checked to make certain full erasure is occurring. Incomplete erasure will cause symptoms that can be misleading. Programmers, components, and even system designs have been erroneously suspected when incomplete erasure was the problem.

SYSTEM CONSIDERATION

The power switching characteristics of EPROMs require careful decoupling of the devices. The supply current, I_{CC}, has three segments that are of interest to the system designer—the standby current level, the active current level, and the transient current peaks that are produced on the falling and rising edges of chip enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. The associated transient voltage peaks can be suppressed by properly selected decoupling capacitors. It is recommended that a 0.1 μF ceramic capacitor be used on every device between V_{CC} and GND. This should be a high frequency capacitor of low inherent inductance. In addition, a 4.7 μF bulk electrolytic capacitor should be used between V_{CC} and GND for each eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage droop caused by the inductive effects of the PC board traces.

National Semiconductor

PRELIMINARY

microCMOS

NMC27C256
262,144-Bit (32K x 8) UV Erasable CMOS PROM

General Description

The NMC27C256 is a high-speed 256k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C256 is packaged in a 28-pin dual in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, microCMOS silicon gate technology.

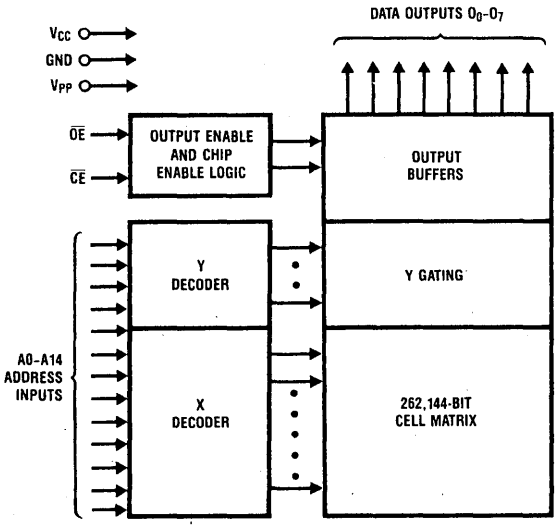
Features

- Access time down to 200 ns, microCMOS technology
- Low CMOS power consumption
- Compatible to high-speed (8 MHz) microprocessors, zero wait state
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Fast and reliable programming
- Static — no clocks required
- TTL compatible inputs/outputs
- CMOS compatible inputs/outputs
- Two-line control
- TRI-STATE® output

Block Diagram

Pin Names

A0–A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
O_0–O_7	Outputs
$\overline{PGM}$	Program
NC	No Connect



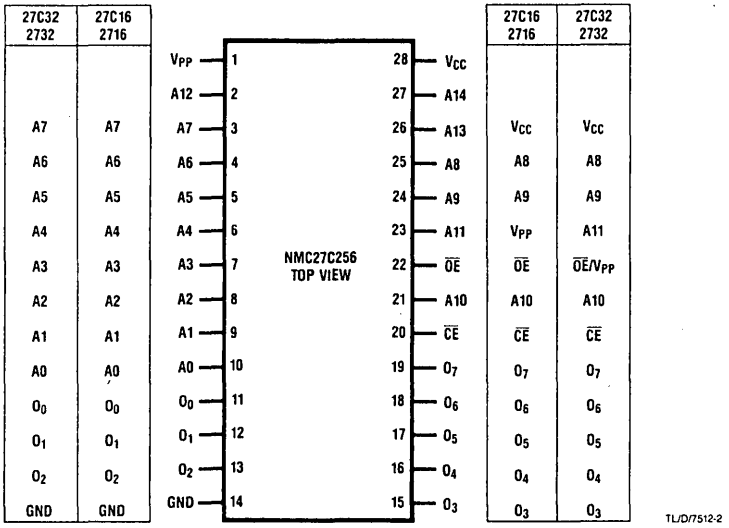
TL/D/7512-1

TABLE I. Mode Selection

Mode \ Pins	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{CC} (28)	Outputs (11–13, 15–19)
Read	V_{IL}	V_{IL}	V_{CC}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{CC}	V_{CC}	High Z
Standby	V_{IH}	X	V_{CC}	V_{CC}	High Z
Verify	V_{IH}	V_{IL}	V_{PP}	V_{CC}	D_{OUT}
Program Inhibit	V_{IH}	V_{IH}	V_{PP}	V_{CC}	High Z

Note: X can be V_{IH} or V_{IL}.

Connection Diagram



Note: National's socket compatible EPROM pin configurations are shown in the blocks adjacent to the NMC27C256 pins.

NS Package Number J24A-Q

Section 7

EEPROMs

7

Section Contents

National Semiconductor

NMC9306/COP494 256-Bit Serial Electrically Erasable Programmable Memory

General Description

The NMC9306/COP494 is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306/COP494 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 x 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams

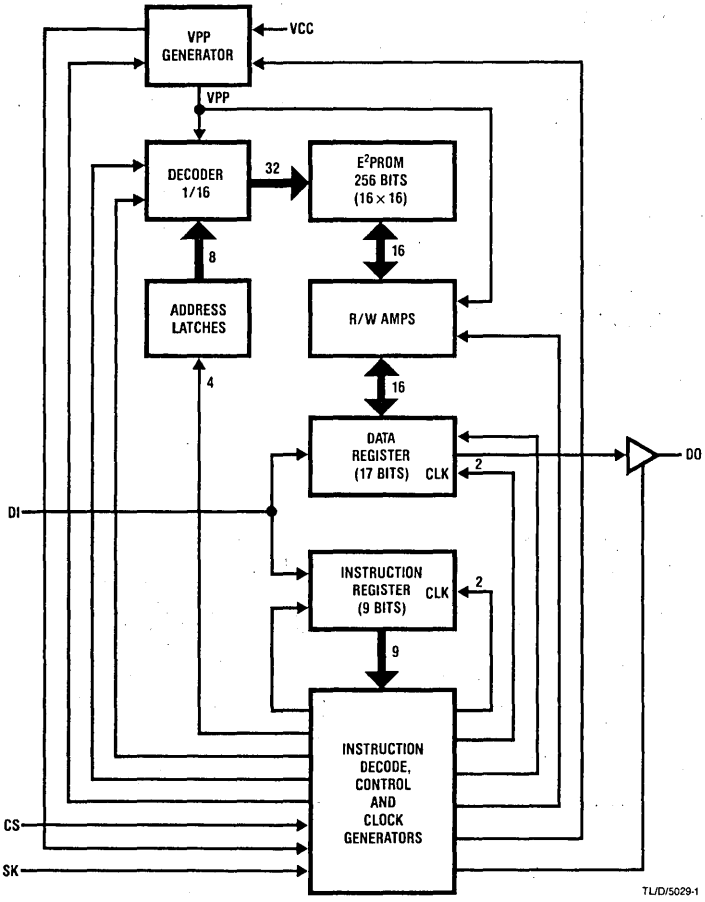


FIGURE 1

Dual-In-Line Package

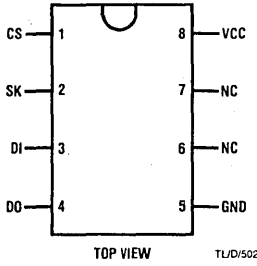


FIGURE 2

Order Number NMC9306N
NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VCC	Power Supply
GND	Ground

7

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature NMC9306/COP494	0°C to +70°C
Ambient Storage Temperature with Data Retention	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics $0°C \le TA \le 70°C$, $VCC = 5V \pm 10\%$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (VCC)		4.5		5.5	V
Operating Current (ICC1)	VCC = 5.5V, CS = 1			10	mA
Standby Current (ICC2)	VCC = 5.5V, CS = 0			3	mA
Input Voltage Levels					
VIL		−0.1		0.8	V
VIH		2.0		VCC + 1	V
Output Voltage Levels					
VOL	IOL = 2.1 mA			0.4	V
VOH	IOH = −400 μA	2.4			V
Input Leakage Current	VIN = 5.5V			10	μA
Output Leakage Current	VOUT = 5.5V, CS = 0			10	μA
SK Frequency		0		250	kHz
SK Duty Cycle		25		75	%
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL = 100 pF				
DO t_{PD1}	VOL = 0.8V, VOH = 2.0V			2	μs
t_{PD0}	VIL = 0.45V, VIH = 2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$)		10		30	ms

Note: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15–D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15–D0	Write all registers

NMC9306/COP494 has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

FIGURE 3

Functional Description

The NMC9306/COP494 is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Six 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (VCC). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. The output data changes during the high states of the system clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE

Like most E^2PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to VIH, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

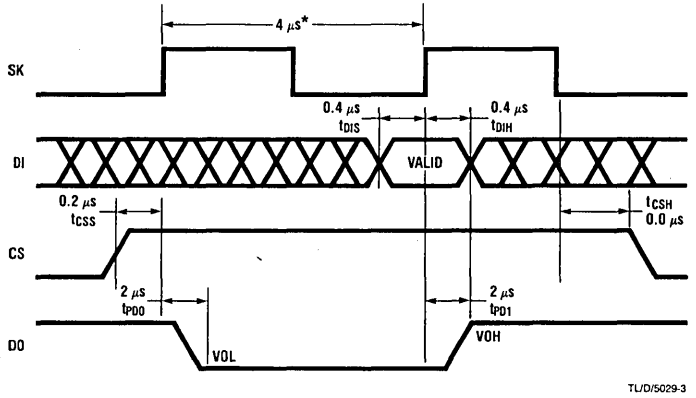
CHIP ERASE

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE

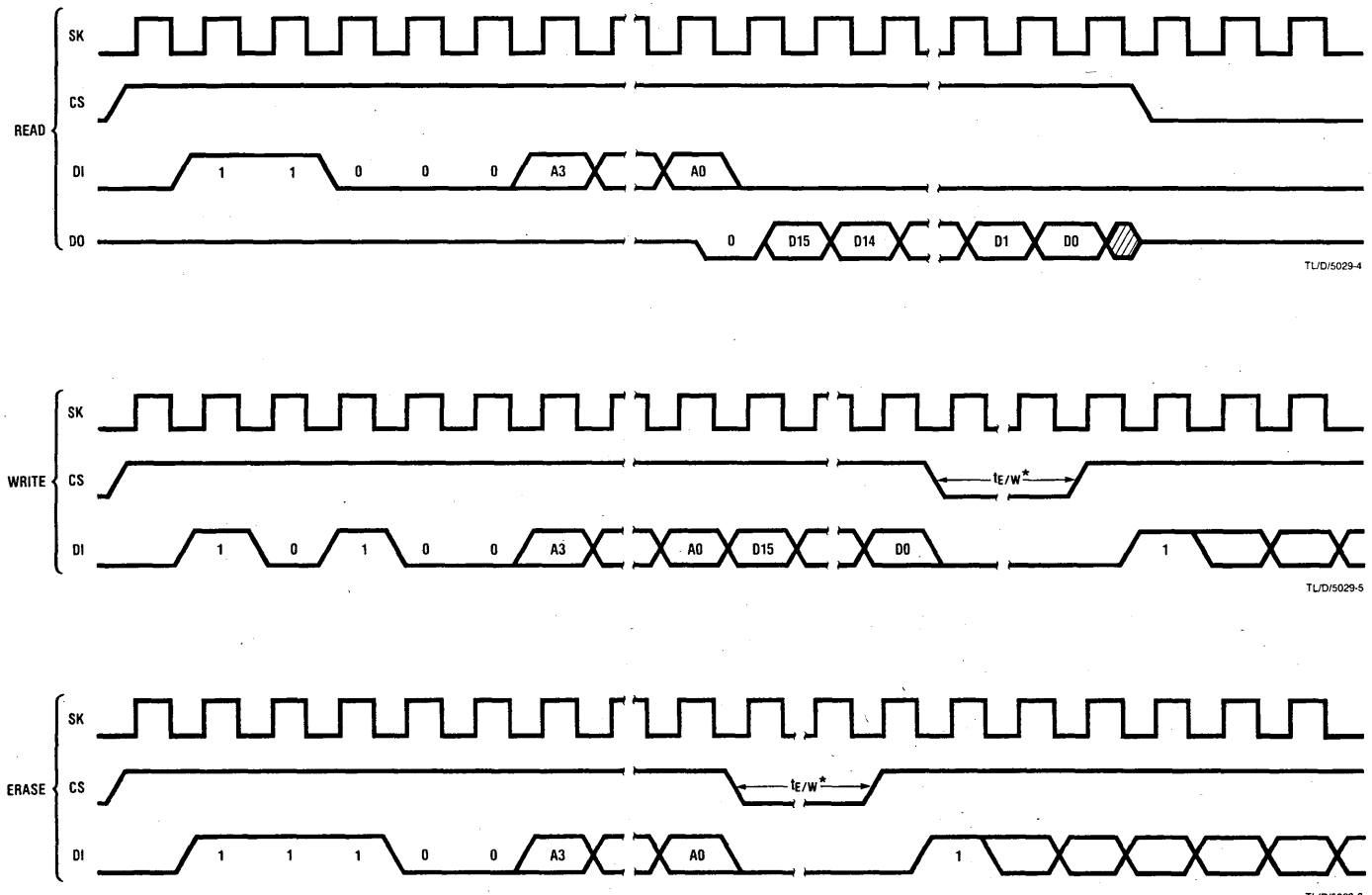
All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Timing Diagrams



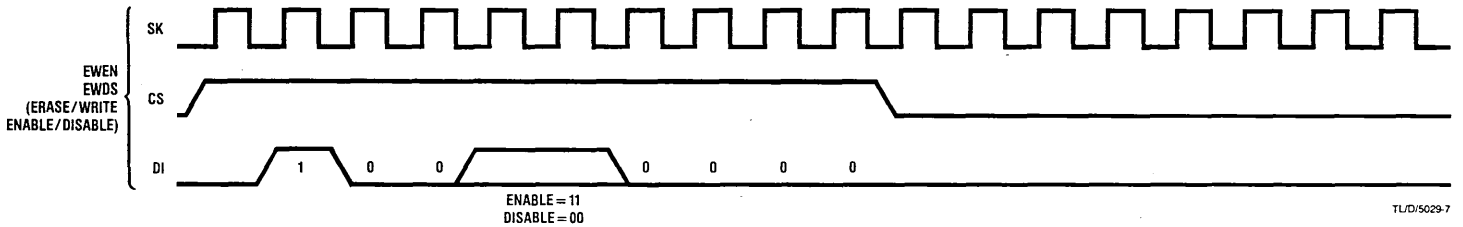
*This is the minimum SK period

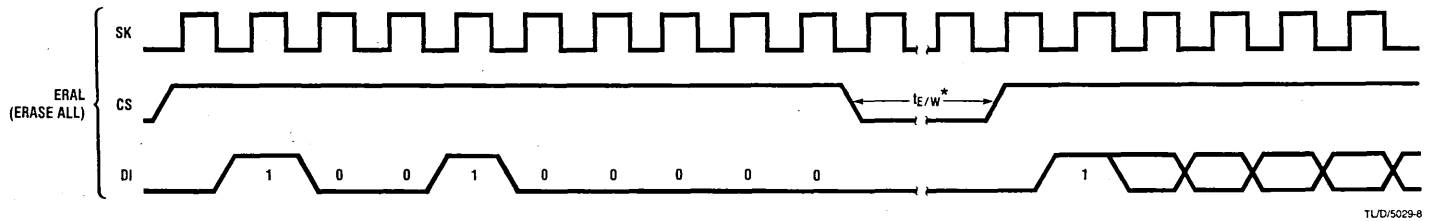
FIGURE 4. Synchronous Data Timing



*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

FIGURE 5. Instruction Timing





*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

FIGURE 5. Instruction Timing (Continued)

National Semiconductor

NMC9306E/COP394 256-Bit Serial Electrically Erasable Programmable Memory

General Description

The NMC9306E/COP494E is a 256-bit non-volatile sequential access memory fabricated using advanced floating gate N-channel E^2PROM technology. It is a peripheral memory designed for data storage and/or timing and is accessed via the simple MICROWIRE™ serial interface. The device contains 256 bits of read/write memory divided into 16 registers of 16 bits each. Each register can be serially read or written by a COP400 series controller. Written information is stored in a floating gate cell with at least 10 years data retention and can be updated by an erase-write cycle. The NMC9306E/COP494E has been designed to meet applications requiring up to 1×10^4 erase/write cycles per register. A power down mode reduces power consumption by 70 percent.

Features

- Low cost
- Single supply operation (5V ± 10%)
- TTL compatible
- 16 x 16 serial read/write memory
- MICROWIRE compatible serial I/O
- Compatible with COP400 processors
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology

Block and Connection Diagrams

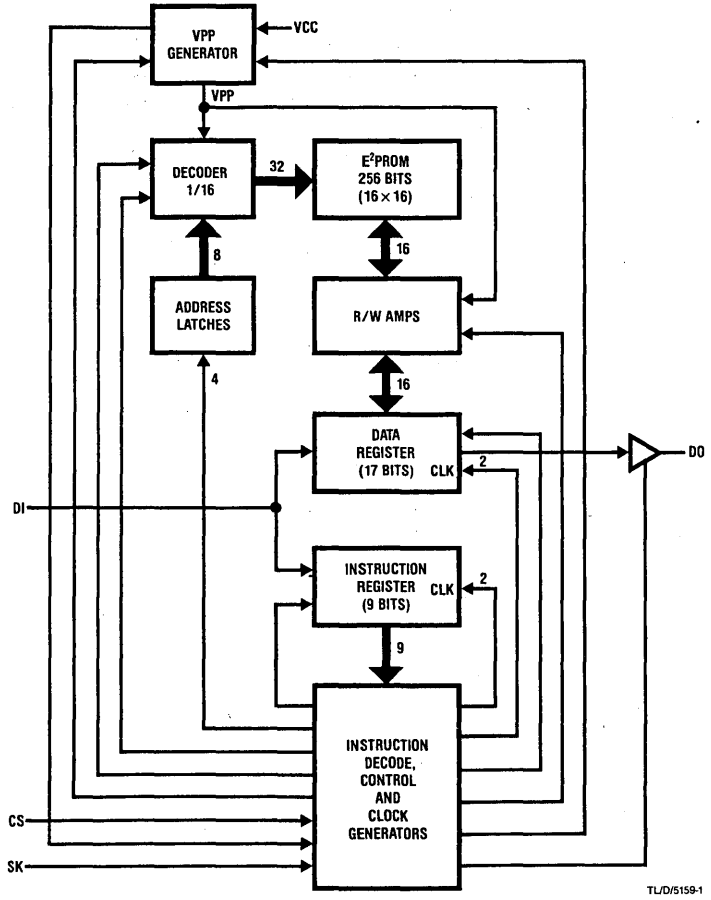


FIGURE 1

Dual-In-Line Package

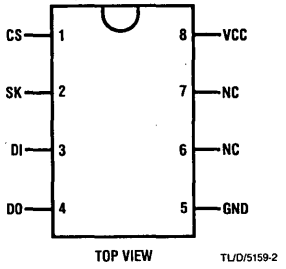


FIGURE 2

Order Number NMC9306NE
NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
VCC	Power Supply
GND	Ground

Absolute Maximum Ratings

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature NMC9306E/COP494E	−40°C to +85°C
Ambient Storage Temperature with Data Retention	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics $-40°C \le TA \le +85°C$, $VCC = 5V \pm 10\%$ unless otherwise specified

Parameter	Conditions	Min	Typ	Max	Units
Operating Voltage (VCC)		4.5		5.5	V
Operating Current (ICC1)	VCC = 5.5V, CS = 1			10	mA
Standby Current (ICC2)	VCC = 5.5V, CS = 0			3	mA
Input Voltage Levels					
VIL		−0.1		0.8	V
VIH		2.0		VCC + 1	V
Output Voltage Levels					
VOL	IOL = 2.1 mA			0.4	V
VOH	IOH = −400 μA	2.4			V
Input Leakage Current	VIN = 5.5V			10	μA
Output Leakage Current	VOUT = 5.5V, CS = 0			10	μA
SK Frequency		0		250	kHz
SK Duty Cycle		25		75	%
Input Set-Up and Hold Times					
CS t_{CSS}		0.2			μs
t_{CSH}		0			μs
DI t_{DIS}		0.4			μs
t_{DIH}		0.4			μs
Output Delay	CL = 100 pF				
DO t_{PD1}	VOL = 0.8V, VOH = 2.0V			2	μs
t_{PD0}	VIL = 0.45V, VIH = 2.40V			2	μs
Erase/Write Pulse Width ($t_{E/W}$)		10		30	ms

Note: $t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

Instruction Set

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10xx	A3A2A1A0		Read register A3A2A1A0
WRITE	1	01xx	A3A2A1A0	D15–D0	Write register A3A2A1A0
ERASE	1	11xx	A3A2A1A0		Erase register A3A2A1A0
EWEN	1	0011	xxxx		Erase/write enable
EWDS	1	0000	xxxx		Erase/write disable
ERAL	1	0010	xxxx		Erase all registers
WRAL	1	0001	xxxx	D15–D0	Write all registers

NMC9306E/COP494E has 7 instructions as shown. Note that MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 4-bit address for 1 of 16, 16-bit registers.

X is a don't care state.

FIGURE 3

Functional Description

The NMC9306E/COP494E is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. Its organization is sixteen registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Six 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, four bits as an op code, and four bits of address. SK clock cycle is necessary after CS equals logical "1" before the instruction can be loaded. The on-chip programming-voltage generator allows the user to use a single power supply (VCC). Only during the read mode is the serial output (DO) pin valid. During all other modes the DO pin is in TRI-STATE®, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a READ instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. The output data changes during the high states of the system clock.

ERASE/WRITE ENABLE AND DISABLE

Programming must be preceded once by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed. The programming disable instruction is provided to protect against accidental data disturb. Execution of a READ instruction is independent of both EWEN and EWDS instructions.

ERASE

Like most E^2PROMS, the register must first be erased (all bits set to 1s) before the register can be written (certain bits set to 0s). After an ERASE instruction is input, CS is dropped low. This falling edge of CS determines the start of programming. The register at the address specified in the instruction is then set entirely to 1s. When the erase/write programming time ($t_{E/W}$) constraint has been satisfied, CS is brought up for at least one SK period. A new instruction may then be input, or a low-power standby state may be achieved by dropping CS low.

WRITE

The WRITE instruction is followed by 16 bits of data which are written into the specified address. This register must have been previously erased. Like any programming mode, erase/write time is determined by the low state of CS following the instruction. The on-chip high voltage section only generates high voltage during these programming modes, which prevents spurious programming during other modes. When CS rises to VIH, the programming cycle ends. All programming modes should be ended with CS high for one SK period, or followed by another instruction.

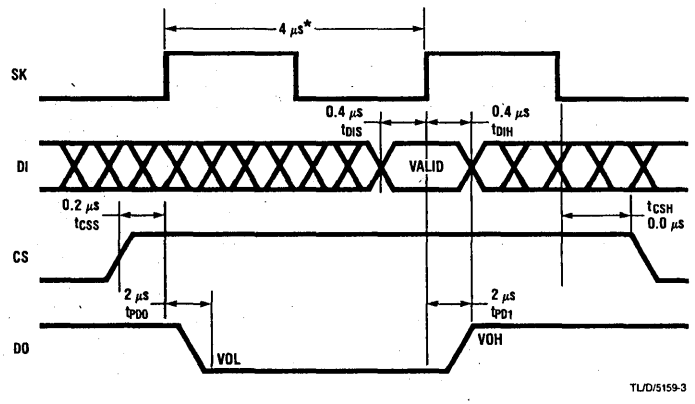
CHIP ERASE

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a 1. Each register is then ready for a WRITE instruction.

CHIP WRITE

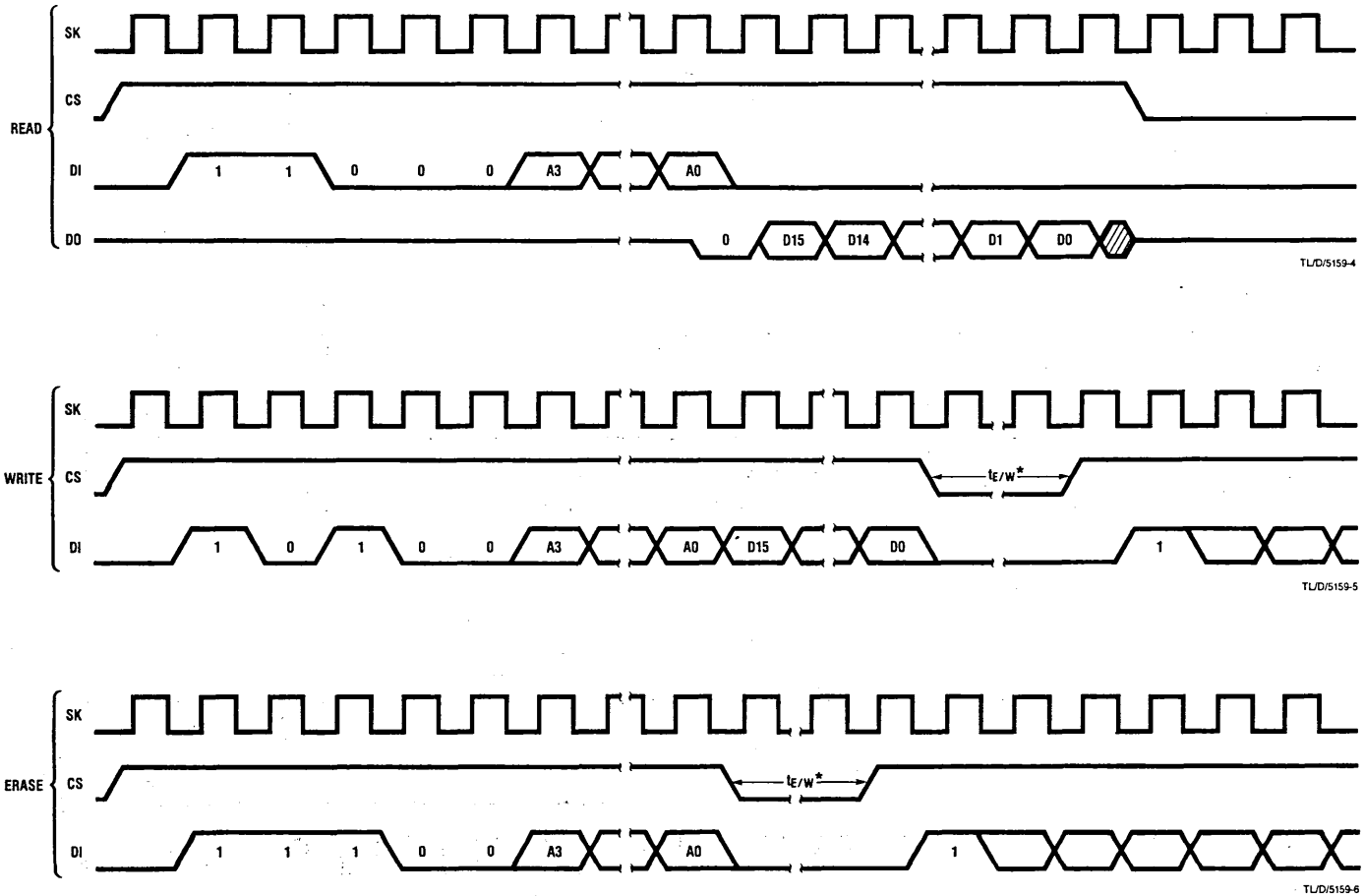
All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle, except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Timing Diagrams



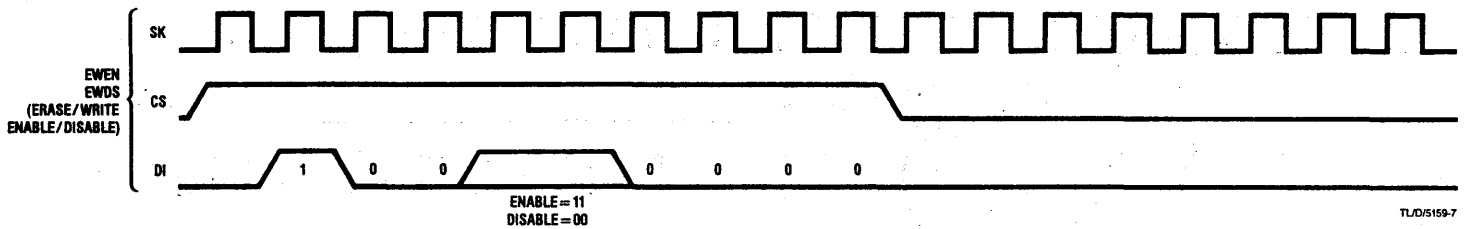
*This is the minimum SK period

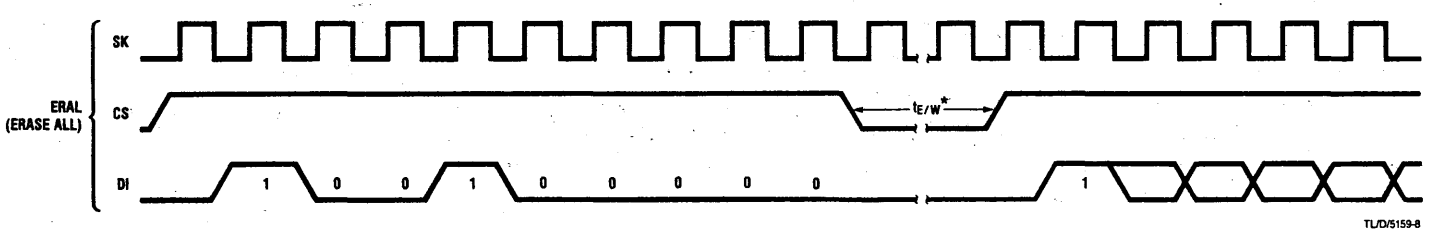
FIGURE 4. Synchronous Data Timing



*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

FIGURE 5. Instruction Timing





*$t_{E/W}$ measured to rising edge of SK or CS, whichever occurs last.

FIGURE 5. Instruction Timing (Continued)

National Semiconductor

NMC9346/COP495 1024-Bit Serial Electrically Erasable Programmable Memory (5V Only)

General Description

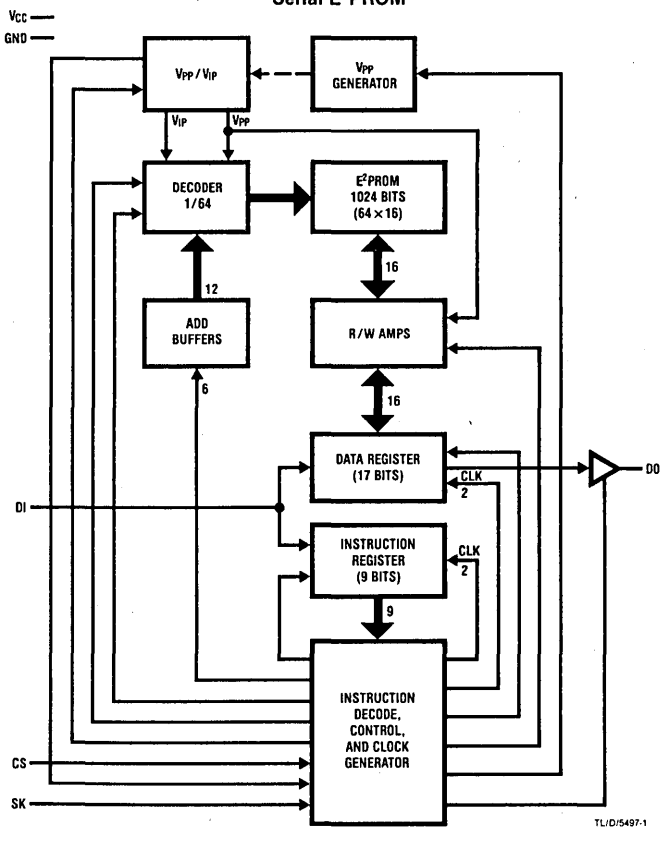
The NMC9346/COP495 is a 1024-bit non-volatile, sequential E^2PROM, fabricated using advanced N-channel E^2PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346/COP495 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

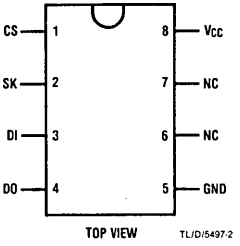
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 × 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block and Connection Diagrams

Serial E^2PROM



Dual-In-Line Package



Order Number NMC9346N
NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

7

Absolute Maximum Ratings (Note 1)

Voltage Relative to GND	+6V to −0.3V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +125°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC and AC Electrical Characteristics $0°C \le T_A \le 70°C$, $V_{CC} = 5V \pm 10\%$ unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current	$V_{CC} = 5.5V$, CS = 1, SK = 1		12	mA
	Erase/Write Operating Current	$V_{CC} = 5.5V$		12	mA
I_{CC2}	Standby Current	$V_{CC} = 5.5V$, CS = 0		3	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	$V_{CC}+1$	V
	Output Voltage Levels				
V_{OL}		$I_{OL} = 2.1$ mA		0.4	V
V_{OH}		$I_{OH} = -400\ \mu A$	2.4		V
I_{LI}	Input Leakage Current	$V_{IN} = 5.5V$		10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$, CS = 0		10	μA
	SK Frequency		0	250	kHz
	SK Duty Cycle		25	75	%
	Inputs				
t_{CSS}	CS		0.2		μs
t_{CSH}			0		μs
t_{DIS}	DI		0.4		μs
t_{DIH}			0.4		μs
	Output	$C_L = 100$ pF			
$t_{pd}1$	DO	$V_{OL} = 0.8V$, $V_{OH} = 2.0V$		2	μs
$t_{pd}0$		$V_{IL} = 0.45V$, $V_{IH} = 2.40V$		2	μs
$t_{E/W}$	Self-Timed Program Cycle			10	ms
t_{CS}	Min CS Low Time		1		μs
t_{SV}	Rising Edge of CS to Status Valid	$C_L = 100$ pF		1	μs
t_{0H}, t_{1H}	Falling Edge of CS to DO TRI-STATE®			0.4	μs

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Instruction Set for NMC9346/COP495

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15-D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/write enable
EWDS	1	00	00xxxx		Erase/write disable
ERAL	1	00	10xxxx		Erase all registers
WRAL	1	00	01xxxx	D15-D0	Write all registers

NMC9346/COP495 has 7 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Functional Description

The NMC9346/COP495 is a small peripheral memory intended for use with COPS™ controllers and other non-volatile memory applications. Its organization is sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Six 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase, chip write) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. The output data changes during the high states of the system clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE

Like most E^2PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μs (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE

Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

CHIP WRITE

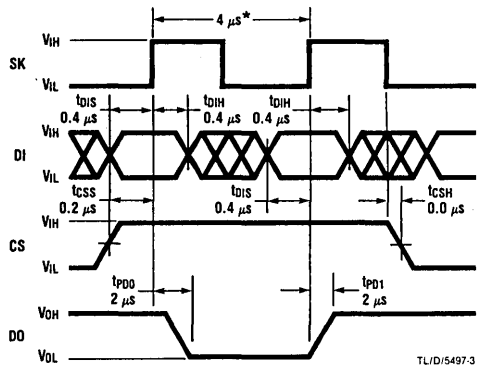
All registers must be erased before a chip write operation. The chip write cycle is identical to the write cycle except for the different op code. All registers are simultaneously written with the data pattern specified in the instruction.

Note 1: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 2: During a programming mode (write, erase, chip erase, chip write), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

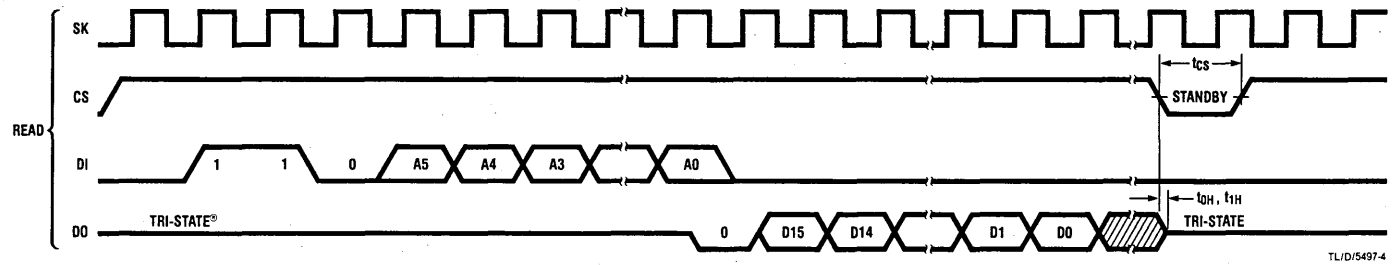
Timing Diagrams

Synchronous Data Timing

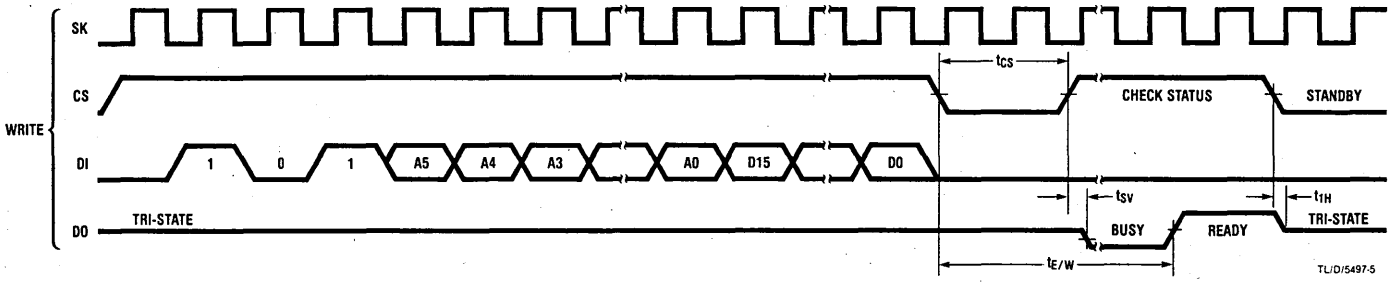


*This is the minimum SK period.

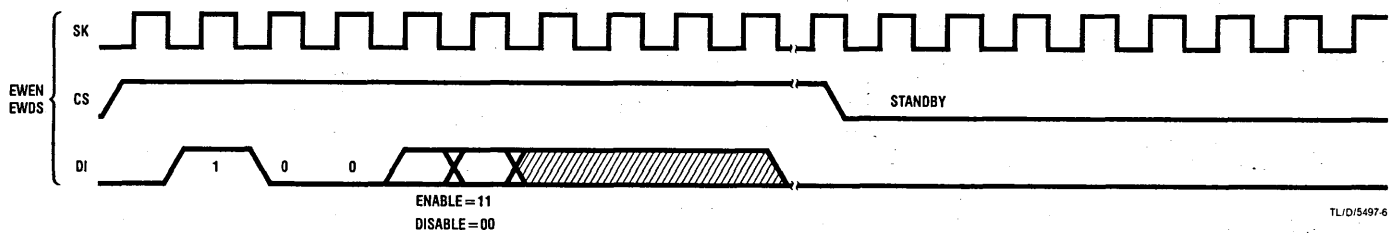
Instruction Timing



TL/D/5497-4

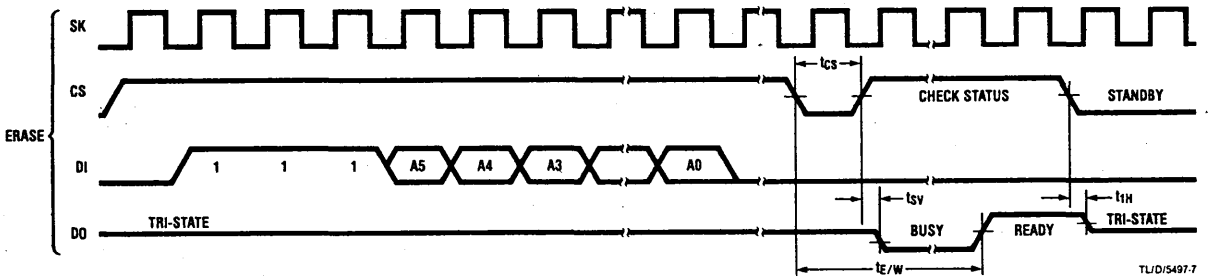


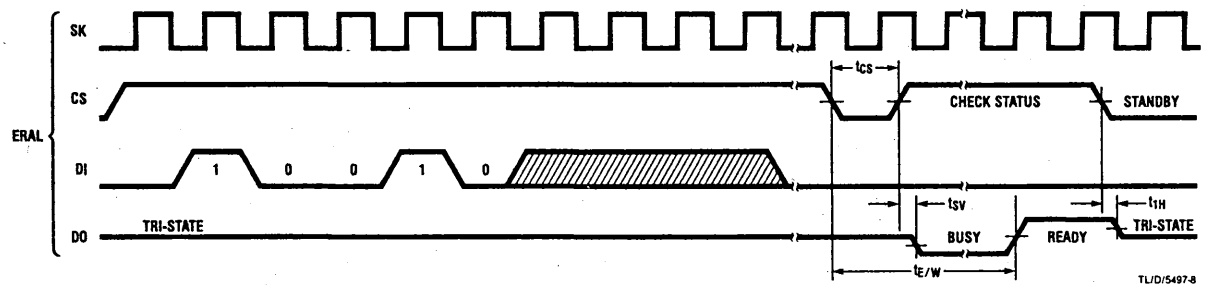
TL/D/5497-5

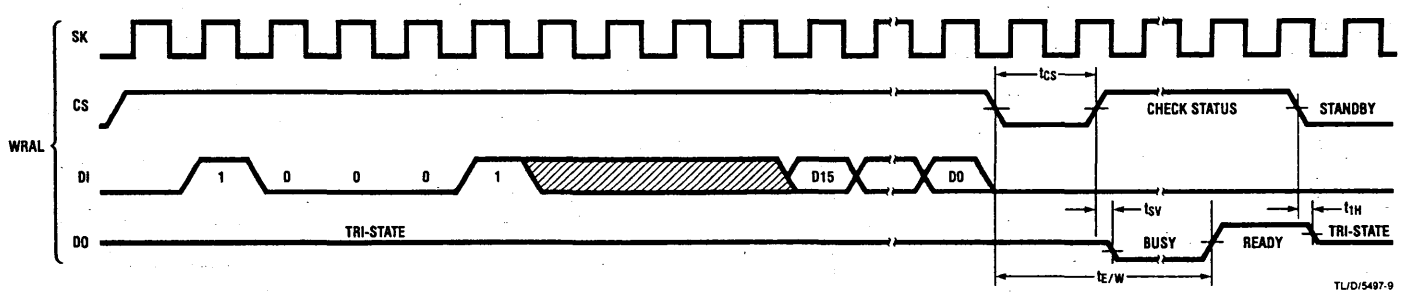


TL/D/5497-6

Instruction Timing







National Semiconductor

NMC9346E/COP395 1024-Bit Serial Electrically Erasable Programmable Memory (5V Only)

General Description

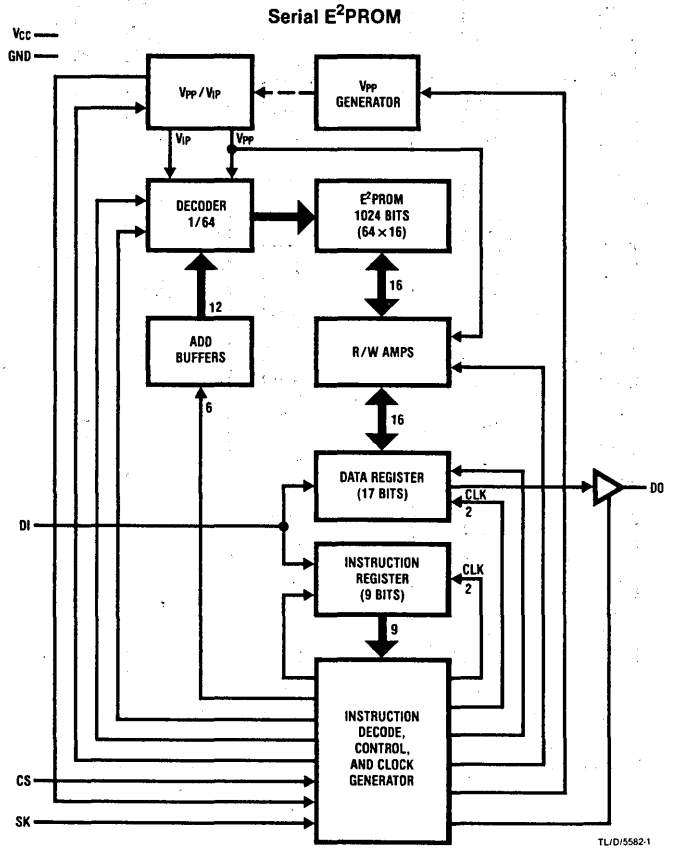
The NMC9346E/COP395 is a 1024-bit non-volatile, sequential E^2PROM, fabricated using advanced N-channel E^2PROM technology. It is an external memory with the 1024 bits of read/write memory divided into 64 registers of 16 bits each. Each register can be serially read or written by a COP400 controller, or a standard microprocessor. Written information is stored in a floating gate cell until updated by an erase and write cycle. The NMC9346E/COP395 has been designed for applications requiring up to 10^4 erase/write cycles per register. A power-down mode is provided by CS to reduce power consumption by 75 percent.

Features

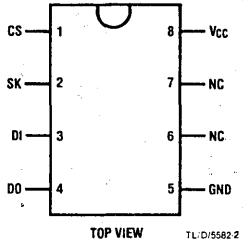
- Low cost
- Single supply read/write/erase operations (5V ± 10%)
- TTL compatible
- 64 x 16 serial read/write memory
- MICROWIRE™ compatible serial I/O
- Simple interfacing
- Low standby power
- Non-volatile erase and write
- Reliable floating gate technology
- Self-timed programming cycle
- Device status signal during programming

Block and Connection Diagrams

Serial E^2PROM



Dual-In-Line Package



Order Number NMC9346NE
NS Package Number N08E

Pin Names

CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings (Note 1)

Voltage Relative to GND	+6V to −0.3V	Ambient Storage Temperature with Data Retention	−65°C to +125°C
Ambient Operating Temperature NMC9346E/COP395	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC and AC Electrical Characteristics −40°C − $T_A \leq$ 85°C, V_{CC} = 5V ± 10% unless specified

Symbol	Parameter	Conditions	Min	Max	Units
V_{CC}	Operating Voltage		4.5	5.5	V
I_{CC1}	Operating Current	V_{CC} = 5.5V, CS = 1, SK = 1		12	mA
	P/E Operating Current	V_{CC} = 5.5V		12	mA
I_{CC2}	Standby Current	V_{CC} = 5.5V, CS = 0		3	mA
	Input Voltage Levels				
V_{IL}			−0.1	0.8	V
V_{IH}			2.0	V_{CC} + 1	V
	Output Voltage Levels				
V_{OL}		I_{OL} = 2.1 mA		0.4	V
V_{OH}		I_{OH} = −400 μA	2.4		V
I_{LI}	Input Leakage Current	V_{IN} = 5.5V		10	μA
I_{LO}	Output Leakage Current	V_{OUT} = 5.5V, CS = 0		10	μA
	SK Frequency		0	250	kHz
	SK Duty Cycle		25	75	%
	Inputs				
t_{CSS}	CS		0.2		μs
t_{CSH}			0		μs
t_{DIS}	DI		0.4		μs
t_{DIH}			0.4		μs
	Output	C_L = 100 pF			
$t_{pd}1$	DO	V_{OL} = 0.8V, V_{OH} = 2.0V		2	μs
$t_{pd}0$		V_{IL} = 0.45V, V_{IH} = 2.40V		2	μs
$t_{E/W}$	Self-Timed Program Cycle			10	ms
t_{CS}	Min CS Low Time		1		μs
t_{SV}	Rising Edge of CS to Status Valid	C_L = 100 pF		1	μs
t_{0H}, t_{1H}	Falling Edge of CS to DO TRI-STATE®			0.4	μs

Note 1: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Instruction Set for NMC9346E/COP395

Instruction	SB	Op Code	Address	Data	Comments
READ	1	10	A5A4A3A2A1A0		Read register A5A4A3A2A1A0
WRITE	1	01	A5A4A3A2A1A0	D15–D0	Write register A5A4A3A2A1A0
ERASE	1	11	A5A4A3A2A1A0		Erase register A5A4A3A2A1A0
EWEN	1	00	11xxxx		Erase/write enable
EWDS	1	00	00xxxx		Erase/write disable
ERAL	1	00	10xxxx		Erase all registers

NMC9346E/COP395 has 6 instructions as shown. Note that the MSB of any given instruction is a "1" and is viewed as a start bit in the interface sequence. The next 8 bits carry the op code and the 6-bit address for 1 of 64, 16-bit registers.

Functional Description

The NMC9346E/COP395 is a small peripheral memory intended for use with COPS™ controllers and other nonvolatile memory applications. Its organization is sixty-four registers and each register is sixteen bits wide. The input and output pins are controlled by separate serial formats. Six 9-bit instructions can be executed. The instruction format has a logical '1' as a start bit, two bits as an op code, and six bits of address. The programming cycle is self-timed, with the data out (DO) pin indicating the ready/busy status of the chip. The on-chip programming voltage generator allows the user to use a single power supply (V_{CC}). It only generates high voltage during the programming modes (write, erase, chip erase) to prevent spurious programming during other modes. The DO pin is valid as data out during the read mode, and if initiated, as a ready/busy status indicator during a programming cycle. During all other modes the DO pin is in TRI-STATE, eliminating bus contention.

READ

The read instruction is the only instruction which outputs serial data on the DO pin. After a read instruction is received, the instruction and address are decoded, followed by data transfer from the memory register into a 16-bit serial-out shift register. A dummy bit (logical '0') precedes the 16-bit data output string. The output data changes during the high states of the system clock.

ERASE/WRITE ENABLE AND DISABLE

When V_{CC} is applied to the part it powers up in the programming disable (EWDS) state, programming must be preceded by a programming enable (EWEN) instruction. Programming remains enabled until a programming disable (EWDS) instruction is executed or V_{CC} is removed from the part. The programming disable instruction is provided to protect against accidental data disturb. Execution of a read instruction is independent of both EWEN and EWDS instructions.

ERASE

Like most E^2PROMs, the register must first be erased (all bits set to logical '1') before the register can be written (certain bits set to logical '0'). After an erase instruction is input, CS is dropped low. This falling edge of CS determines the start of the self-timed programming cycle. If CS is brought high subsequently (after observing the t_{CS} specification), the DO pin will indicate the ready/busy status of the chip. The DO pin will go low if the chip is still programming. The DO pin will go high when all bits of the register at the address specified in the instruction have been set to a logical '1'. The part is now ready for the next instruction sequence.

WRITE

The write instruction is followed by 16 bits of data to be written into the specified address. After the last bit of data (D0) is put on the data in (DI) pin CS must be brought low before the next rising edge of the SK clock. This falling edge of CS initiates the self-timed programming cycle. Like all programming modes, DO indicates the ready/busy status of the chip if CS is brought high after a minimum of 1 μs (t_{CS}). DO = logical '0' indicates that programming is still in progress. DO = logical '1' indicates that the register at the address specified in the instruction has been written with the data pattern specified in the instruction and the part is ready for another instruction. The register to be written into must have been previously erased.

CHIP ERASE

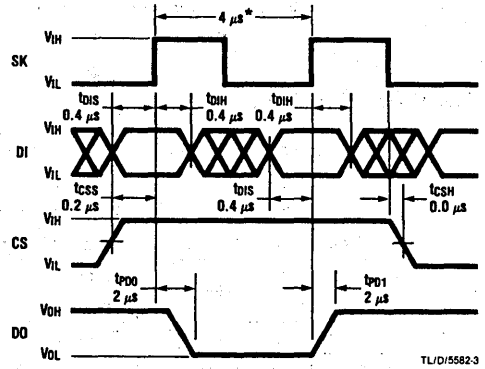
Entire chip erasing is provided for ease of programming. Erasing the chip means that all registers in the memory array have each bit set to a logical '1'. Each register is then ready for a write instruction. The chip erase cycle is identical to the erase cycle except for the different op code.

Note 1: CS must be brought low for a minimum of 1 μs (t_{CS}) between consecutive instruction cycles.

Note 2: During a programming mode (write, erase, chip erase), SK clock is only needed while the actual instruction, i.e., start bit, op code, address and data, is being input. It can remain deactivated during the self-timed programming cycle and status check.

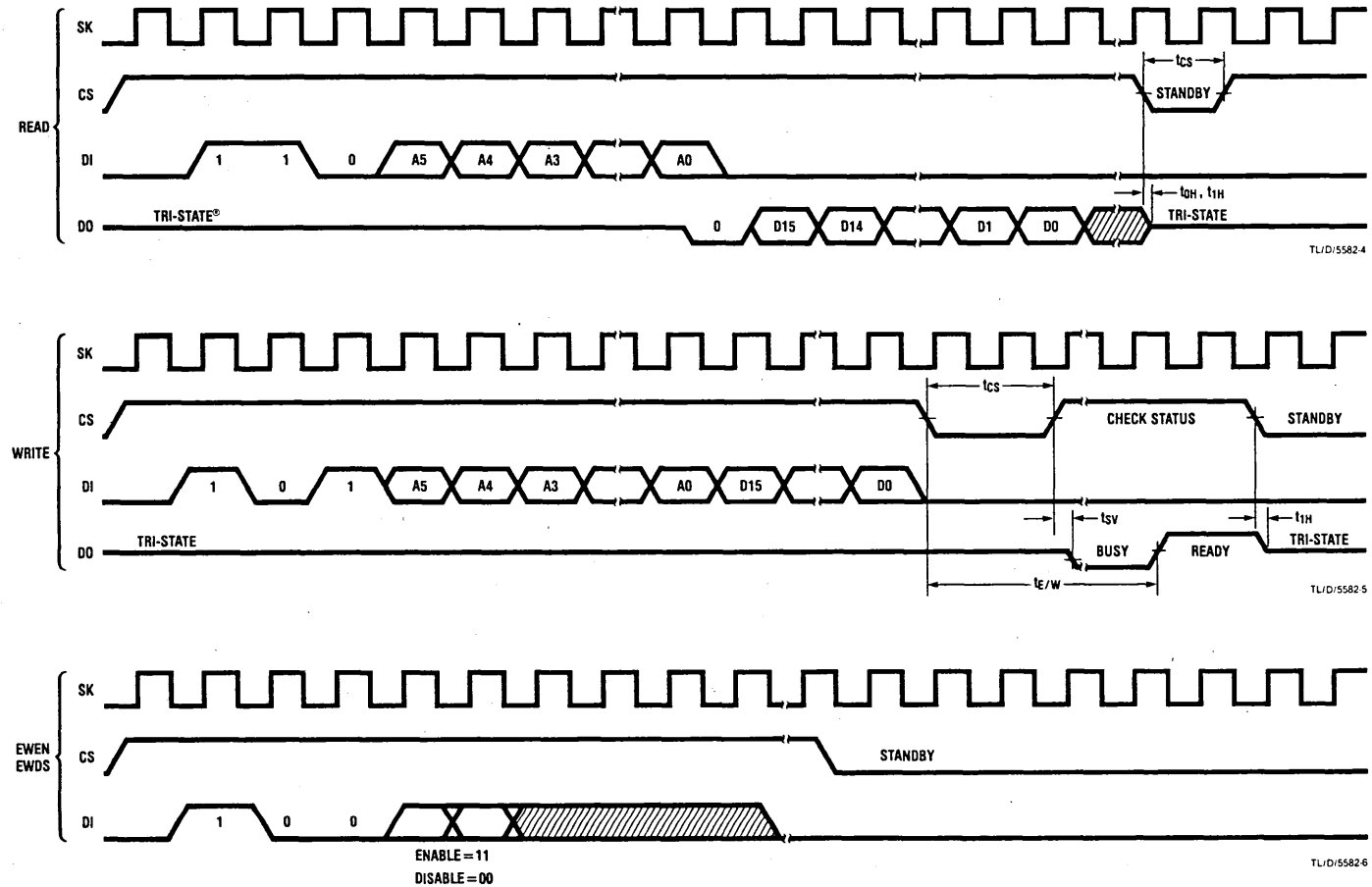
Timing Diagrams

Synchronous Data Timing

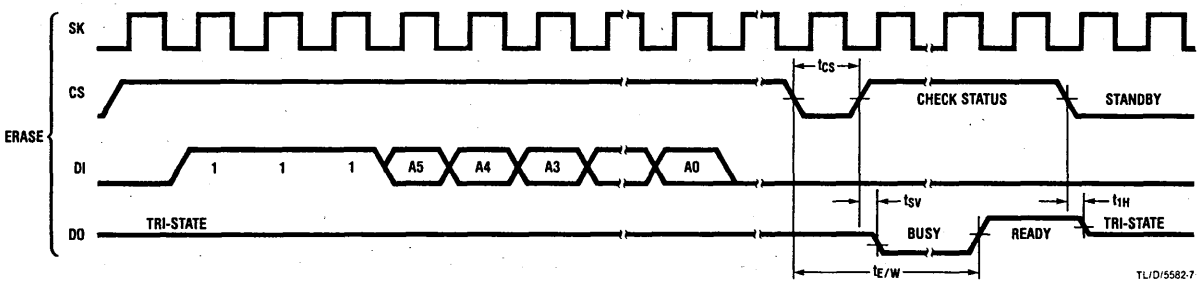


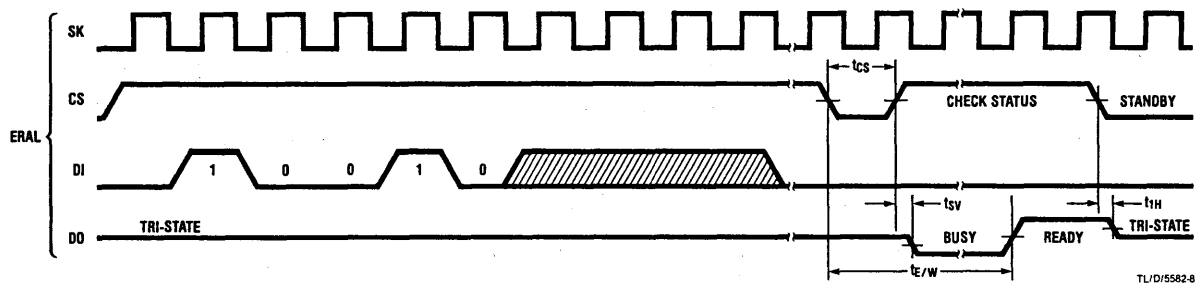
*This is the minimum SK period.

Instruction Timing



Instruction Timing





National Semiconductor

NMC2816 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC2816-25	NMC2816-35	NMC2816-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC2816 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816 is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC2816 also has an output enable control to eliminate bus contention in a system environment.

The NMC2816 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 x 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816-25)
  - 350 ns max (NMC2816-35)
  - 450 ns max (NMC2816-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 610 mW max (active power ICC + IPP)
  - 295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

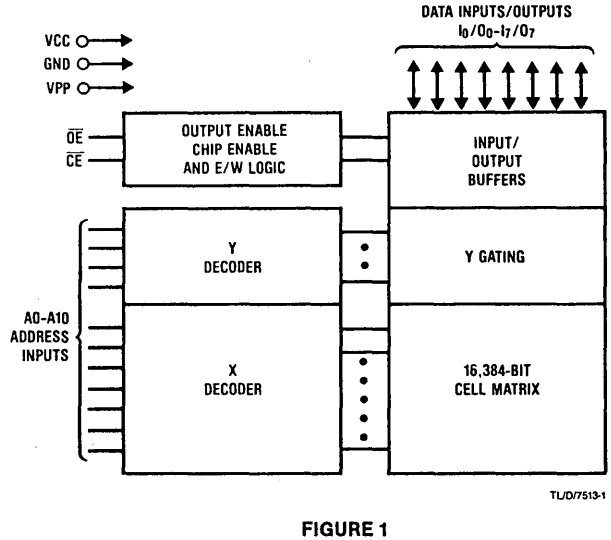


FIGURE 1

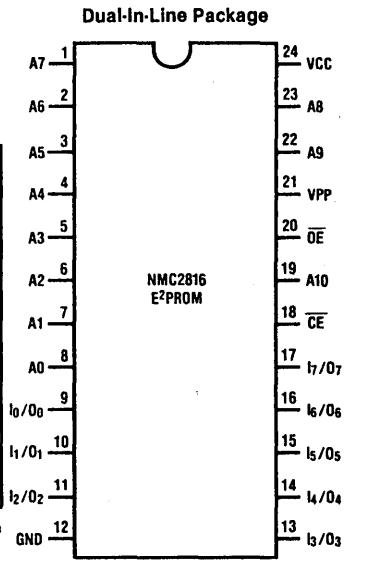


FIGURE 2

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Order Number NMC2816J
NS Package Number J24A

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
VPP Supply Voltage with Respect to Ground During Program	+22.5V to −0.3V
Maximum Duration of VPP Supply at 22V During E/W Inhibit	24 Hrs
Maximum Duration of VPP Supply at 22V During Write/Erase Programming (Note 2)	15 ms
Lead Temperature (Soldering, 10 seconds)	300°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

Temperature Range	0°C to +70°C
VCC Power Supply (Notes 2 and 3)	5V ±5%

DC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ±5% (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
ILI	Input Leakage Current	VIN = 5.25V			10	μA
ILO	Output Leakage Current	VOUT = 5.25V			10	μA
ICC2	VCC Current (Active)	$\overline{OE} = \overline{CE}$ = VIL		50	110	mA
ICC1	VCC Current (Standby)	$\overline{CE}$ = VIH		10	50	mA
IPP(R)	VPP Current (Read)	VPP = 6V, $\overline{CE}$ = VIH or VIL		1	5	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.0		VCC + 1	V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
VPP	Read Voltage		4		6	V
WRITE OPERATION						
VPP	Write/Erase Voltage		20	21	22	V
IPP(W)	VPP Current (Write/Erase)	$\overline{OE}$ = VIH, $\overline{CE}$ = VIL, VPP = 22V		6	15	mA
V$\overline{OE}$	$\overline{OE}$ Voltage (Chip Erase)	I$\overline{OE}$ ≤ 10 μA	9		15	V
IPP(I)	VPP Current (Inhibit)	$\overline{CE}$ = VIH, VPP = 22V		2	5	mA
IPP(C)	VPP Current (Chip Erase)	$\overline{OE}$ = V$\overline{OE}$, $\overline{CE}$ = VIL, VPP = 22V		2	5	mA

Capacitance TA = 25°C, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
CIN	Input Capacitance	VIN = 0V		5	10	pF
COUT	Output Capacitance	VOUT = 0V			10	pF
CVCC	VCC Capacitance	$\overline{OE} = \overline{CE}$ = VIH			500	pF
CVPP	VPP Capacitance	$\overline{OE} = \overline{CE}$ = VIH			50	pF

AC Test Conditions

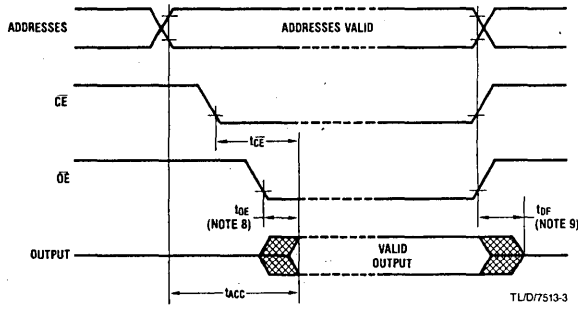
Output Load	1 TTL gate and CL = 100 pF
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Read Mode AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ± 5% (Notes 2 and 3)

Symbol	Parameter	Conditions	NMC2816-25			NMC2816-35			NMC2816-45			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = VIL$			250			350			450	ns
$t_{\overline{CE}}$	$\overline{CE}$ to Output Delay	$\overline{OE} = VIL$			250			350			450	ns
$t_{\overline{OE}}$	Output Enable to Output Delay	$\overline{CE} = VIL$	10		100	10		120	10		120	ns
t_{DF}	Output Disable to Output Float (Note 9)	$\overline{CE} = \overline{OE} = VIL$	0		80	0		80	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = VIL$	0			0			0			ns

Switching Time Waveforms (Note 6)

Read



Write Mode AC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ± 5% (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address Set-Up Time		150			ns
t_{AH}	Address Hold Time		50			ns
t_{CS}	$\overline{CE}$ to VPP Set-Up Time		150			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = VIH$	0			ns
t_{DH}	Data Hold Time	$\overline{OE} = VIH$	50			ns
t_{WP}	Write Pulse Width (Note 4)		9	10	15	ms
t_{WR}	Write Recovery Time		50			ns
t_{OS}	Chip Clear Set-Up Time		0			ns
t_{OH}	Chip Clear Hold Time		0			ns
t_{PRC}	VPP RC Time Constant		450	600	750	μs
t_{PFT}	VPP Fall Time (Note 5)				100	μs
t_{BOS}	Byte Erase/Write Set-Up Time (Note 12)		0			ns
t_{BOH}	Byte Erase/Write Hold Time (Note 12)		0			ns
t_{CH}	Chip Enable High Time		1			μs

Note 1: This parameter is only sampled and not 100% tested.

Note 2: To prevent spurious device erasure or write, VCC must be applied simultaneously or before 21V application of VPP. VPP cannot be driven to 21V without previously applying VCC.

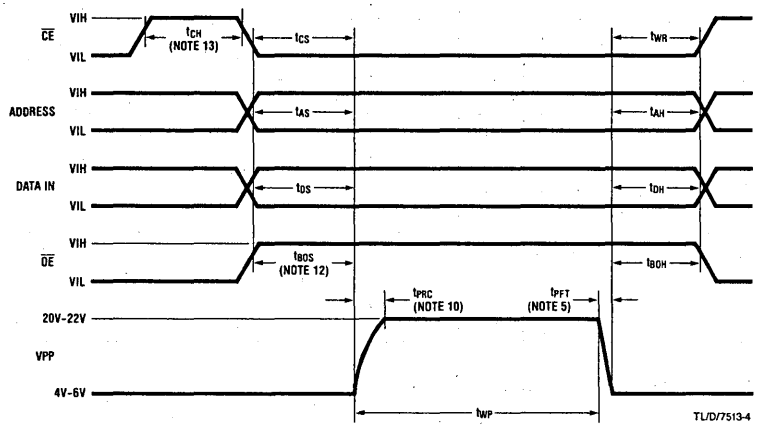
Note 3: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: Adherence to t_{WP} specification is important to device reliability.

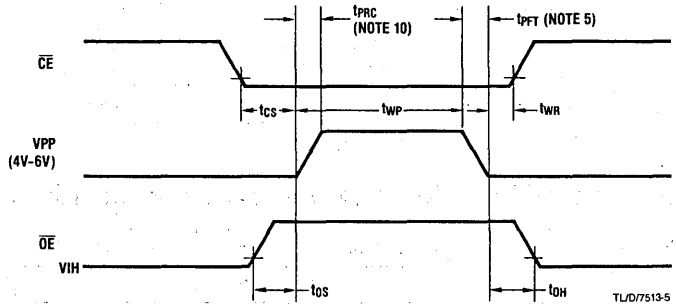
Note 5: To allow immediate read verify capability, VPP can be driven low in less than 50 ns.

Switching Time Waveforms (Note 6)

Byte Erase and Byte Write Programming Cycle (Notes 7 and 12)



Chip Erase (Note 11)



Note 6: All times shown in parentheses are minimum times and are ns unless otherwise specified.

Note 7: Prior to a data write, an erase operation must be performed. For byte erase, data in = VIH, and for chip erase, data in = don't care.

Note 8: $\overline{OE}$ may be delayed up to 230 ns after falling edge of $\overline{CE}$ without impact on t_{CE} for NMC2816-35.

Note 9: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Note 10: The rising edge of VPP must follow an exponential waveform. That waveform's time constant is specified as t_{PRC}.

Note 11: In the chip erase mode DIN = don't care.

Note 12: In byte erase or write mode, $\overline{OE}$ must be at VIH (logic 1 state).

Note 13: $\overline{CE}$ = VIH places the chip in a low power standby condition and must be applied for a minimum time of t_{CH} before the start of any byte programming cycle.

Device Operation

The NMC2816 has six modes of operation, listed in Table I. All operational modes are designed to provide maximum microprocessor compatibility and system consistency. The device pinout is a part of the JEDEC approved byte-wide non-volatile memory family, allowing appropriate and cost-effective density and functionality upgrades.

All control inputs are TTL compatible with the exception of chip erase. The VPP voltage must be pulsed to 21V during write and erase, and held at 5V during the other two modes.

TABLE I. Mode Selection V_{CC} = 5V ±10%

Pin / Mode	$\overline{CE}$ (18)	$\overline{OE}$ (20)	VPP (21)	Inputs/ Outputs
Read	VIL	VIL	4V to 6V	DOUT
Standby	VIH	Don't Care	4V to 6V	Hi-Z
Byte Erase	VIL	VIH	20V to 22V	DIN = VIH
Byte Write	VIL	VIH	20V to 22V	DIN
Chip Erase (Note 11)	VIL	9V to 15V	20V to 22V	DIN = Don't Care
E/W Inhibit	VIH	Don't Care	4V to 22V	Hi-Z

Device Operation (Continued)

READ MODE

Both $\overline{CE}$ and $\overline{OE}$ must be at logic low levels to obtain information from the device. Chip enable ($\overline{CE}$) is the power control pin and could be used for device selection. The output enable ($\overline{OE}$) pin serves to gate internal data to the output pins. Assuming that the address inputs are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after a time delay of $t_{\overline{OE}}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-$t_{\overline{OE}}$.

CHIP ERASE MODE

Should one wish to erase the entire NMC2816 array at once, the device offers a chip erase function. When the chip erase function is performed, all 2k bytes are returned to a logic 1 (FF) state.

The NMC2816's chip erase function is engaged when the output enable ($\overline{OE}$) pin is raised above 9V. When $\overline{OE}$ is greater than 9V and $\overline{CE}$ and VPP are in the normal write mode, the entire array is erased. This chip erase function takes approximately 10 ms. The data input pins are don't care during this time to allow for ease in chip erase. *Figure 3* is an example for an $\overline{OE}$ control switch.

VPP PULSE

The shape of the VPP pulse is important in ensuring long term reliability and operating characteristics. VPP must rise to 21V through an RC waveform (exponential). The t_{PRC} specification has been designed to accommodate changes of RC due to temperature variations.

Figure 4 shows an example for a VPP switch design, useful where programming will occur over the specified temperature and operating voltage conditions.

WRITE MODE

The NMC2816 is erased and reprogrammed electrically rather than optically, as opposed to EPROMs which require UV light. The device offers dramatic flexibility because both byte (single location) and chip erase are possible.

To write a particular location, that byte must be erased prior to a data write. Erasing is accomplished by applying logic 1 (TTL high) inputs to all 8 data input pins, lowering $\overline{CE}$, and applying a 21V programming signal to VPP. The $\overline{OE}$ pin must be equal to VIH during byte erase and write operations. The programming pulse width must be a minimum of 9 ms, and a maximum of 15 ms. The rising edge of VPP must conform to the RC time constant specified previously. Once the location has been erased, the same operation is repeated for a data write. The input pins in this case reflect the byte that is to be stored. $\overline{CE}$ must go from VIH to VIL at the beginning of a byte erase/write cycle and must be held high for a minimum of t_{CH} between E/W cycles.

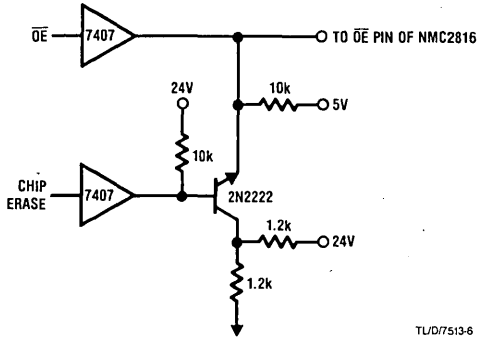
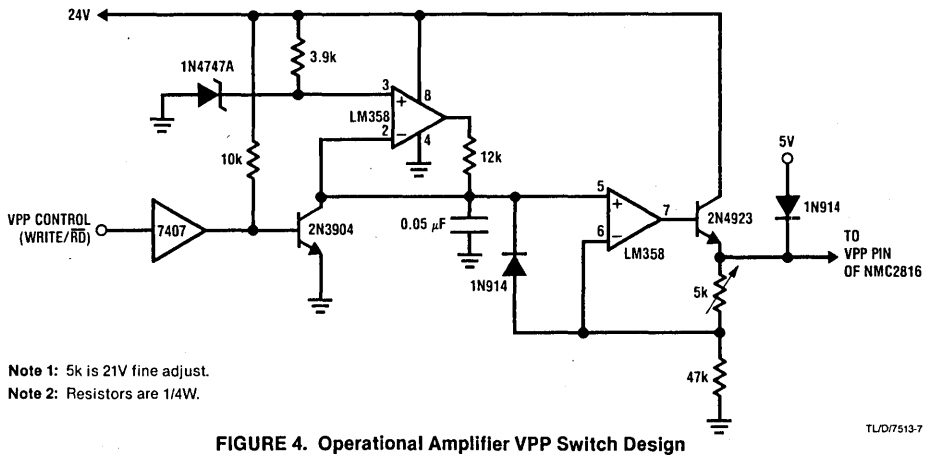


FIGURE 3. $\overline{OE}$ Chip Erase Control



Note 1: 5k is 21V fine adjust.
Note 2: Resistors are 1/4W.

FIGURE 4. Operational Amplifier VPP Switch Design

Device Operation (Continued)

A characteristic of all E^2PROMs is that the total number of erase/write cycles is not unlimited. The NMC2816 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per byte. The erase/write cycling characteristic is completely byte independent. Adjacent bytes are not affected during erase/write cycling.

Because the device is designed to be written in system, all data sheet specifications (including write and erase operations) hold over the full operating temperature range (0°C to 70°C).

OUTPUT OR-TYING

Because NMC2816s are usually used in larger memory arrays, a 2-line control function is provided that accommodates this use of multiple memory connections. The 2-line control function allows low power dissipation (by deselecting unused devices), and the removal of bus contention from the system environment.

To most effectively use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded from addresses as the primary device selection function. $\overline{OE}$ (pin 20) should be made a common connection to all devices in system, and connected to the $\overline{RD}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

STANDBY MODE

The NMC2816 has a standby mode which reduces active power dissipation by 52% from 610 mW to 295 mW (ICC + IPP). The NMC2816 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

National Semiconductor

NMC2816M 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC2816M-25	NMC2816M-35	NMC2816M-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	140	140	140
Max Standby Current (mA)	60	60	60

General Description

The NMC2816M is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC2816M makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC2816M is deselected when pin 18 is high and is automatically placed in the standby mode. This mode provides a 55% reduction in power with no increase in access time. The NMC2816M also has an output enable control to eliminate bus contention in a system environment.

The NMC2816M can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array erased in a chip erase mode. Byte erase mode is identical to byte write mode, with all data inputs at logic ones (TTL high).

Features

- 2048 x 8 organization
- Fully static
- Reliable floating gate technology
- Very fast access time
  - 250 ns max (NMC2816M-25)
  - 350 ns max (NMC2816M-35)
  - 450 ns max (NMC2816M-45)
- Single byte erase/write capability
- 10 ms byte erase/write time
- Chip erase time of 10 ms
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Low power dissipation
  - 800 mW max (active power ICC + IPP)
  - 360 mW max (standby power ICC + IPP)

Block and Connection Diagrams

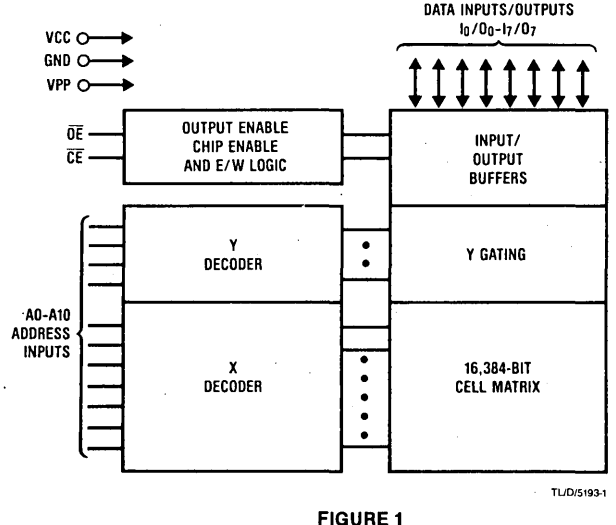


FIGURE 1

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Dual-In-Line Package

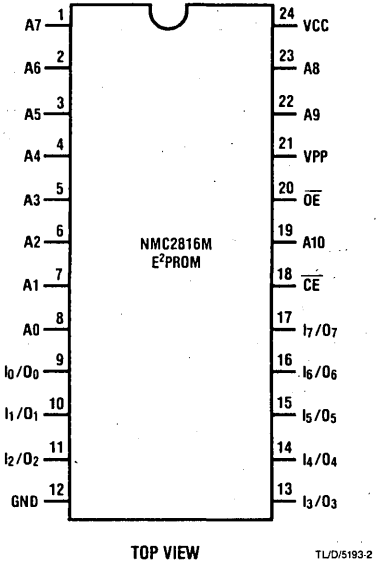


FIGURE 2

Order Number NMC2816MJ
NS Package Number J24A

Absolute Maximum Ratings

Temperature Under Bias	−65°C to +135°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
VPP Supply Voltage with Respect to Ground During Program	+22.5V to −0.3V
Maximum Duration of VPP Supply at 22V During E/W Inhibit	24 Hrs
Maximum Duration of VPP Supply at 22V During Write/Erase Programming (Note 2)	15 ms
Lead Temperature (Soldering, 10 seconds)	300°C

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Conditions

Temperature Range	−55°C to +125°C
VCC Power Supply (Notes 2 and 3)	5V ± 10%

DC Electrical Characteristics $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
ILI	Input Leakage Current	VIN = 5.50V			10	μA
ILO	Output Leakage Current	VOUT = 5.50V			10	μA
ICC2	VCC Current (Active)	$\overline{OE} = \overline{CE} = VIL$		65	140	mA
ICC1	VCC Current (Standby)	$\overline{CE} = VIH$		12	60	mA
IPP(R)	VPP Current (Read)	VPP = 6V, $\overline{CE}$ = VIH or VIL		1	5	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.2		VCC + 1	V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
VPP	Read Voltage		4		6	V
WRITE OPERATION						
VPP	Write/Erase Voltage		20	21	22	V
IPP(W)	VPP Current (Write/Erase)	$\overline{OE}$ = VIH, $\overline{CE}$ = VIL, VPP = 22V		6	15	mA
V$\overline{OE}$	$\overline{OE}$ Voltage (Chip Erase)	I$\overline{OE}$ ≤ 10 μA	9		15	V
IPP(I)	VPP Current (Inhibit)	$\overline{CE}$ = VIH, VPP = 22V		2	5	mA
IPP(C)	VPP Current (Chip Erase)	$\overline{OE}$ = V$\overline{OE}$, $\overline{CE}$ = VIL, VPP = 22V		2	5	mA

Capacitance $T_A = 25°C$, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
CIN	Input Capacitance	VIN = 0V		5	10	pF
COUT	Output Capacitance	VOUT = 0V			10	pF
CVCC	VCC Capacitance	$\overline{OE} = \overline{CE} = VIH$			500	pF
CVPP	VPP Capacitance	$\overline{OE} = \overline{CE} = VIH$			50	pF

AC Test Conditions

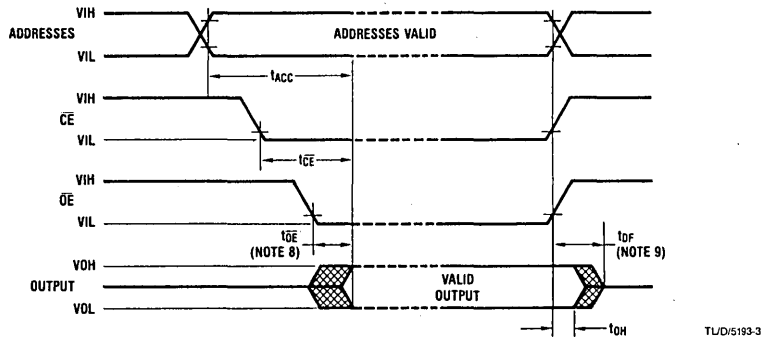
Output Load	1 TTL gate and CL = 100 pF
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	NMC2816M-25			NMC2816M-35			NMC2816M-45			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$			250			350			450	ns
$t_{\overline{CE}}$	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$			250			350			450	ns
$t_{\overline{OE}}$	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		120	10		140	10		140	ns
t_{DF}	Output Disable to Output Float (Note 9)	$\overline{CE} = \overline{OE} = V_{IL}$	0		100	0		100	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0			0			0			ns

Switching Time Waveforms (Note 6)

Read



Write Mode AC Electrical Characteristics $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address Set-Up Time		150			ns
t_{AH}	Address Hold Time		50			ns
t_{CS}	$\overline{CE}$ to VPP Set-Up Time		150			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = V_{IH}$	0			ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	50			ns
t_{WP}	Write Pulse Width (Note 4)		9	10	15	ms
t_{WR}	Write Recovery Time		50			ns
t_{OS}	Chip Clear Set-Up Time		0			ns
t_{OH}	Chip Clear Hold Time		0			ns
t_{PRC}	VPP RC Time Constant		450	600	750	μs
t_{PFT}	VPP Fall Time (Note 5)				100	μs
t_{BOS}	Byte Erase/Write Set-Up Time (Note 12)		0			ns
t_{BOH}	Byte Erase/Write Hold Time (Note 12)		0			ns
t_{CH}	Chip Enable High Time		1			μs

Note 1: This parameter is only sampled and not 100% tested.

Note 2: To prevent spurious device erasure or write, VCC must be applied simultaneously or before 21V application of VPP. VPP cannot be driven to 21V without previously applying VCC.

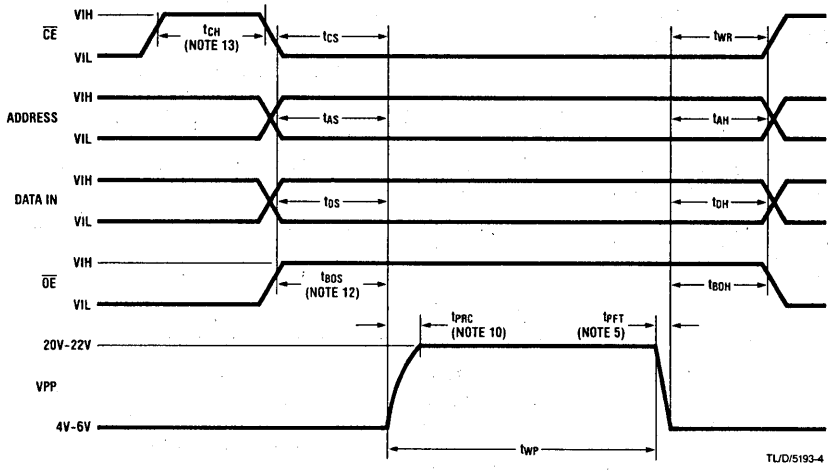
Note 3: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: Adherence to t_{WP} specification is important to device reliability.

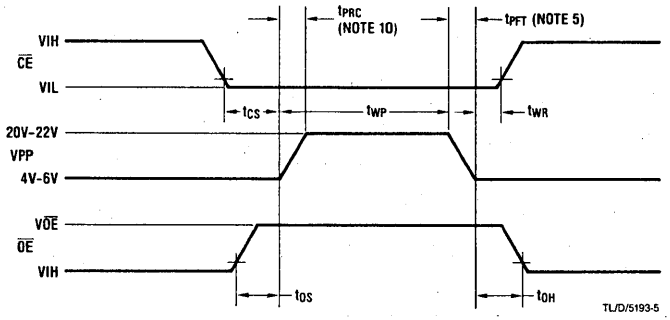
Note 5: To allow immediate read verify capability, VPP can be driven low in less than 50 ns.

Switching Time Waveforms (Note 6)

Byte Erase and Byte Write Programming Cycle (Notes 7 and 12)



Chip Erase (Note 11)



Note 6: All times shown in parentheses are minimum times and are ns unless otherwise specified.

Note 7: Prior to a data write, an erase operation must be performed. For byte erase, data in = VIH, and for chip erase, data in = don't care.

Note 8: $\overline{OE}$ may be delayed up to 210 ns after falling edge of $\overline{CE}$ without impact on t_{CE} for NMC2816M-35.

Note 9: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Note 10: The rising edge of VPP must follow an exponential waveform. That waveform's time constant is specified as t_{PRC}.

Note 11: In the chip erase mode DIN = don't care.

Note 12: In byte erase or write mode, $\overline{OE}$ must be at VIH (logic 1 state).

Note 13: $\overline{CE}$ = VIH places the chip in a low power standby condition and must be applied for a minimum time of t_{CH} before the start of any byte programming cycle.

Device Operation

The NMC2816M has six modes of operation, listed in Table I. All operational modes are designed to provide maximum microprocessor compatibility and system consistency. The device pinout is a part of the JEDEC approved bytewide non-volatile memory family, allowing appropriate and cost-effective density and functionality upgrades.

All control inputs are TTL compatible with the exception of chip erase. The VPP voltage must be pulsed to 21V during write and erase, and held at 5V during the other two modes.

TABLE I. Mode Selection V_{CC} = 5V ±10%

Mode \ Pin	$\overline{CE}$ (18)	$\overline{OE}$ (20)	VPP (21)	Inputs/ Outputs
Read	VIL	VIL	4V to 6V	DOUT
Standby	VIH	Don't Care	4V to 6V	Hi-Z
Byte Erase	VIL	VIH	20V to 22V	DIN = VIH
Byte Write	VIL	VIH	20V to 22V	DIN
Chip Erase (Note 11)	VIL	9V to 15V	20V to 22V	DIN = Don't Care
E/W Inhibit	VIH	Don't Care	4V to 22V	Hi-Z

Device Operation (Continued)

READ MODE

Both $\overline{CE}$ and $\overline{OE}$ must be at logic low levels to obtain information from the device. Chip enable ($\overline{CE}$) is the power control pin and could be used for device selection. The output enable ($\overline{OE}$) pin serves to gate internal data to the output pins. Assuming that the address inputs are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after a time delay of $t_{\overline{OE}}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{\overline{OE}}$.

CHIP ERASE MODE

Should one wish to erase the entire NMC2816M array at once, the device offers a chip erase function. When the chip erase function is performed, all 2k bytes are returned to a logic 1 (FF) state.

The NMC2816M's chip erase function is engaged when the output enable ($\overline{OE}$) pin is raised above 9V. When $\overline{OE}$ is greater than 9V and $\overline{CE}$ and VPP are in the normal write mode, the entire array is erased. This chip erase function takes approximately 10 ms. The data input pins are don't care during this time to allow for ease in chip erase. *Figure 3* is an example for an $\overline{OE}$ control switch.

VPP PULSE

The shape of the VPP pulse is important in ensuring long term reliability and operating characteristics. VPP must rise to 21V through an RC waveform (exponential). The t_{PRC} specification has been designed to accommodate changes of RC due to temperature variations.

Figure 4 shows an example for a VPP switch design, useful where programming will occur over the specified temperature and operating voltage conditions.

WRITE MODE

The NMC2816M is erased and reprogrammed electrically rather than optically, as opposed to EPROMs which require UV light. The device offers dramatic flexibility because both byte (single location) and chip erase are possible.

To write a particular location, that byte must be erased prior to a data write. Erasing is accomplished by applying logic 1 (TTL high) inputs to all 8 data input pins, lowering $\overline{CE}$, and applying a 21V programming signal to VPP. The $\overline{OE}$ pin must be equal to VIH during byte erase and write operations. The programming pulse width must be a minimum of 9 ms, and a maximum of 15 ms. The rising edge of VPP must conform to the RC time constant specified previously. Once the location has been erased, the same operation is repeated for a data write. The input pins in this case reflect the byte that is to be stored. $\overline{CE}$ must go from VIH to VIL at the beginning of a byte erase/write cycle and must be held high for a minimum of t_{CH} between E/W cycles.

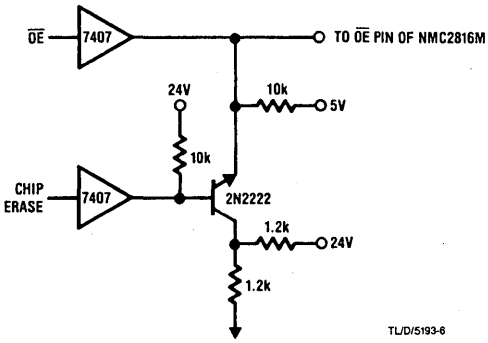
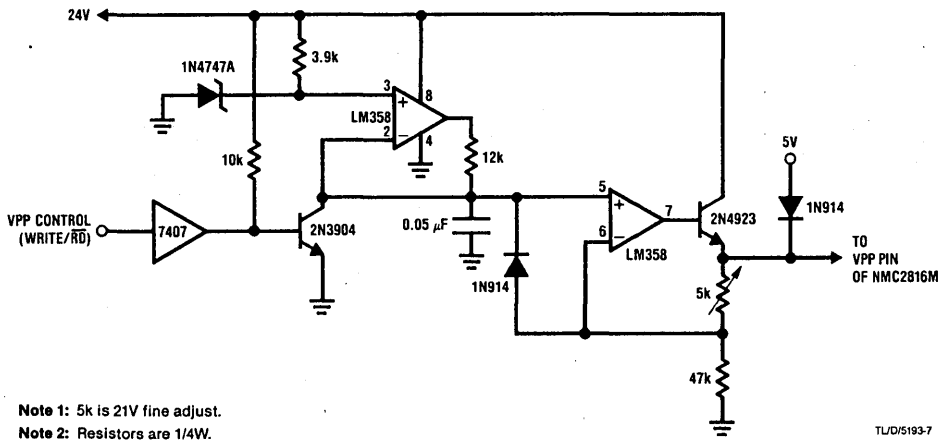


FIGURE 3. $\overline{OE}$ Chip Erase Control



Note 1: 5k is 21V fine adjust.
Note 2: Resistors are 1/4W.

FIGURE 4. Operational Amplifier VPP Switch Design

Device Operation (Continued)

A characteristic of all E^2PROMs is that the total number of erase/write cycles is not unlimited. The NMC2816M has been designed to meet applications requiring up to 1×10^4 erase/write cycles per byte. The erase/write cycling characteristic is completely byte independent. Adjacent bytes are not affected during erase/write cycling.

Because the device is designed to be written in system, all data sheet specifications (including write and erase operations) hold over the full operating temperature range (−55°C to +125°C).

OUTPUT OR-TYING

Because NMC2816Ms are usually used in larger memory arrays, a 2-line control function is provided that accommodates this use of multiple memory connections. The 2-line control function allows low power dissipation (by deselecting unused devices), and the removal of bus contention from the system environment.

To most effectively use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded from addresses as the primary device selection function. $\overline{OE}$ (pin 20) should be made a common connection to all devices in system, and connected to the $\overline{RD}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

STANDBY MODE

The NMC2816M has a standby mode which reduces active power dissipation by 55% from 800 mW to 360 mW. The NMC2816M is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

National Semiconductor

NMC9716 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC9716-25	NMC9716-35	NMC9716-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	110	110	110
Max Standby Current (mA)	50	50	50

General Description

The NMC9716 is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716 makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716 is pin and functionally compatible with the NMC2816 E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC9716 is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 52% reduction in power with no increase in access time. The NMC9716 also has an output enable control to eliminate bus contention in a system environment.

The NMC9716 can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816
- No rise time restriction on erase/write pulse
- 2048 x 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  610 mW max (active power ICC + IPP)
  295 mW max (standby power ICC + IPP)

Block and Connection Diagrams

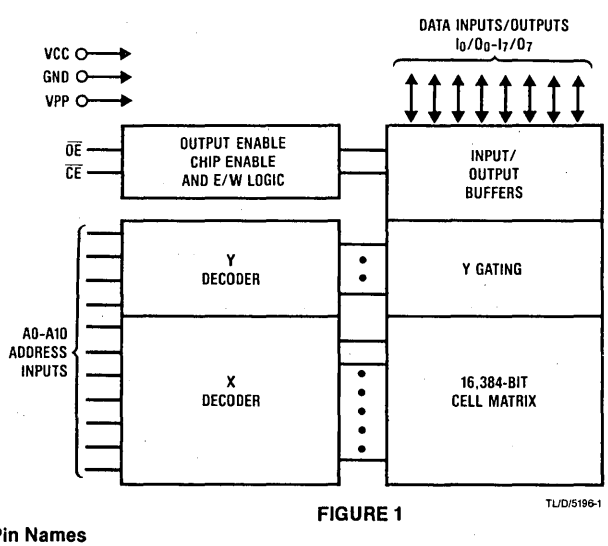


FIGURE 1

Dual-In-Line Package

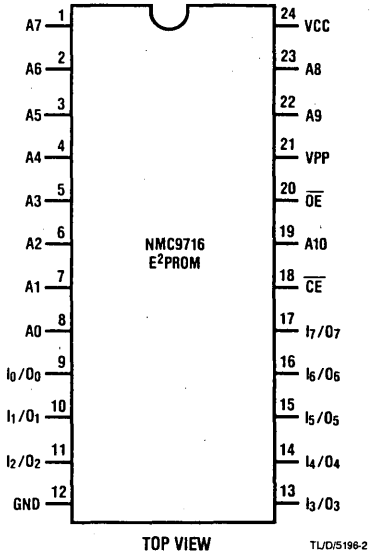


FIGURE 2

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Order Number NMC9716J
NS Package Number J24A

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
VPP Supply Voltage with Respect to Ground During Program	+22.5V to −0.3V
Maximum Duration of VPP Supply at 22V During E/W Inhibit	24 Hrs
Maximum Duration of VPP Supply at 22V During Write/Erase Programming (Note 2)	15 ms
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Temperature Range	0°C to +70°C
VCC Power Supply (Notes 2 and 3)	5V ±5%

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics TA = 0°C to 70°C, VCC = 5V ± 5% (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
ILI	Input Leakage Current	VIN = 5.25V			10	μA
ILO	Output Leakage Current	VOUT = 5.25V			10	μA
ICC2	VCC Current (Active)	$\overline{OE} = \overline{CE}$ = VIL		50	110	mA
ICC1	VCC Current (Standby)	$\overline{CE}$ = VIH		10	50	mA
IPP(R)	VPP Current (Read)	VPP = 6V, $\overline{CE}$ = VIH or VIL		1	5	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.0		VCC +1	V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
VPP	Read Voltage		4		6	V
WRITE OPERATION						
VPP	Write/Erase Voltage		20	21	22	V
IPP(W)	VPP Current (Write/Erase)	$\overline{OE}$ = VIH, $\overline{CE} \leq$ VIL, VPP = 22V		6	15	mA
$V\overline{OE}$	$\overline{OE}$ Voltage (Chip Erase)	$I\overline{OE} \leq 10$ μA	9		15	V
IPP(I)	VPP Current (Inhibit)	$\overline{CE}$ = VIH, VPP = 22V		2	5	mA
IPP(C)	VPP Current (Chip Erase)	$\overline{OE} = V\overline{OE}$, $\overline{CE}$ = VIL, VPP = 22V		2	5	mA

Capacitance TA = 25°C, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
CIN	Input Capacitance	VIN = 0V		5	10	pF
COUT	Output Capacitance	VOUT = 0V			10	pF
CVCC	VCC Capacitance	$\overline{OE} = \overline{CE}$ = VIH			500	pF
CVPP	VPP Capacitance	$\overline{OE} = \overline{CE}$ = VIH			50	pF

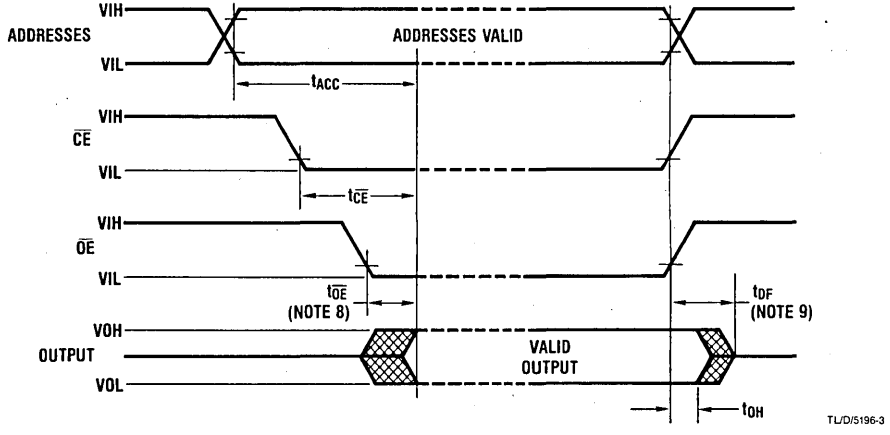
AC Test Conditions

Output Load	1 TTL gate and CL = 100 pF
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	NMC9716-25			NMC9716-35			NMC9716-45			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$			250			350			450	ns
$t_{\overline{CE}}$	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$			250			350			450	ns
$t_{\overline{OE}}$	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		100	10		120	10		120	ns
t_{DF}	Output Disable to Output Float (Note 9)	$\overline{CE} = \overline{OE} = V_{IL}$	0		80	0		80	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0			0			0			ns

Read Waveforms (Note 6)



Note 1: This parameter is only sampled and not 100% tested.

Note 2: To prevent spurious device erasure or write, VCC must be applied simultaneously or before 21V application of VPP. VPP cannot be driven to 21V without previously applying VCC.

Note 3: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: Adherence to t_{WP} specification is important to device reliability.

Note 5: To allow immediate read verify capability, VPP can be driven low in less than 50 ns.

Note 6: All times shown in parentheses are minimum times and are ns unless otherwise specified.

Note 7: Prior to a data write, an erase operation must be performed. For a byte erase, data in = VIH, and for chip erase, data in = don't care.

Note 8: $\overline{OE}$ may be delayed up to 230 ns after falling edge of $\overline{CE}$ without impact on t_{CE} for NMC9716-35.

Note 9: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

Note 10: When programming with VPP, the rising edge of VPP can follow a linear or an exponential waveform. That waveform's rise time or time constant is specified as t_{PRC}. There is no restriction on the rising edge of VPP if programming with $\overline{CE}$.

Note 11: In the chip erase mode DIN = don't care.

Note 12: In byte erase or write mode, $\overline{OE}$ must be equal to VIH.

Note 13: More than one address location can be erase/written without pulsing VPP between every address.

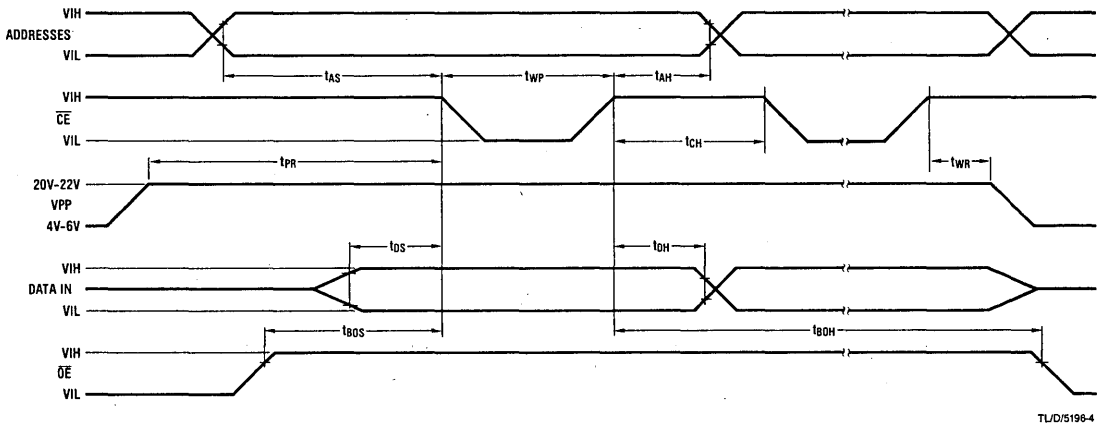
Note 14: $\overline{CE}$ = VIH places the chip in a low power standby condition, and must be applied for a minimum time of t_{CH} before the start of any byte programming cycle.

Write Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address Set-Up Time		150			ns
t_{AH}	Address Hold Time		50			ns
t_{CS}	$\overline{CE}$ Set-Up Time		150			ns
t_{PR}	VPP Set-Up Time		0			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = V_{IH}$	0			ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	50			ns
t_{WP}	Write Pulse Width (Note 4)		9	10	15	ms
t_{WR}	Write Recovery Time		50			ns
t_{OS}	Chip Clear Set-Up Time		0			ns
t_{OH}	Chip Clear Hold Time		0			ns
t_{PRC}	VPP RC Time Constant (Note 10)		0		750	μs
t_{PFT}	VPP Fall Time (Note 5)				100	μs
t_{BOS}	Byte Erase/Write Set-Up Time (Note 12)		0			ns
t_{BOH}	Byte Erase/Write Hold Time (Note 12)		0			ns
t_{CH}	Chip Enable High Time		1			μs

Recommended Erase/Write Waveforms

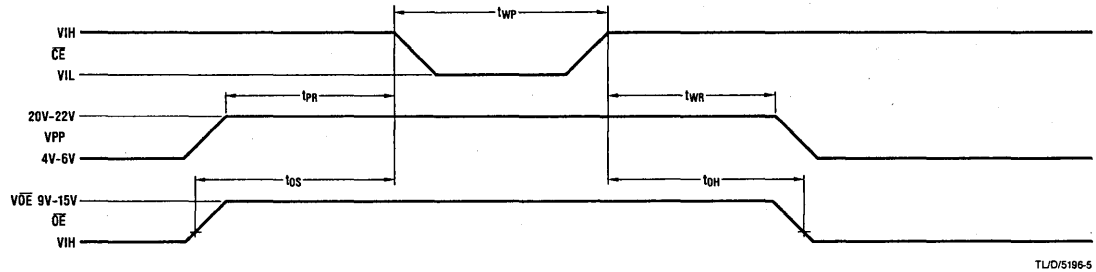
$\overline{CE}$ Pulsed (Notes 7, 12 and 13)



TL/D/5196-4

Chip Erase Waveforms

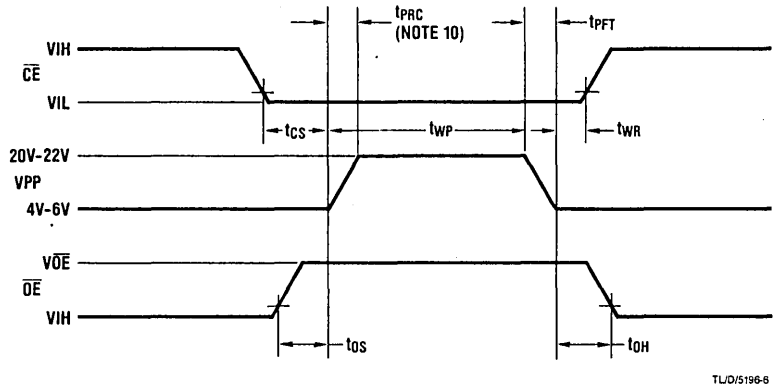
$\overline{CE}$ Pulsed (Note 11)



TL/D/5196-5

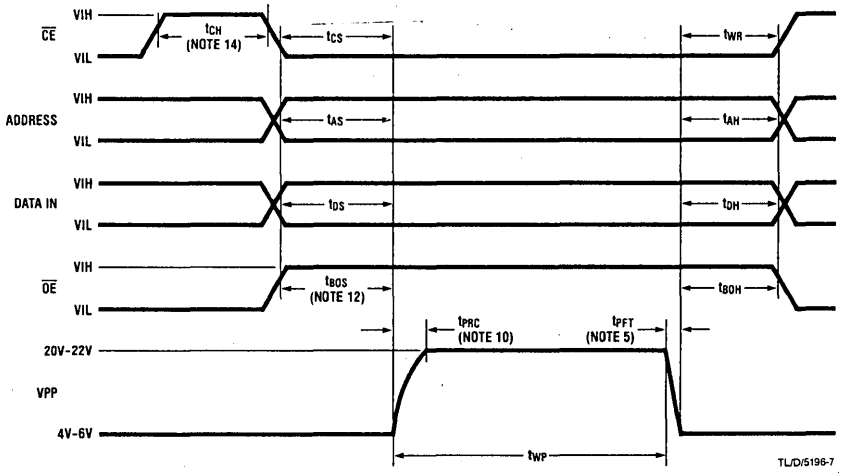
Chip Erase Waveforms (Continued)

Byte Erase and Byte Write Programming Cycle, VPP Pulsed



Alternate Erase/Write Waveforms (NMC2816 compatible) (Note 6)

VPP Pulsed (Note 11)



Device Operation

The NMC9716 has six modes of operation, listed in Table I. All operational modes are designed to provide maximum microprocessor compatibility and system consistency. The device pinout is a part of the JEDEC approved byte-wide non-volatile memory family, allowing appropriate and cost-effective density and functionality upgrades.

All control inputs are TTL compatible with the exception of chip erase. The VPP voltage must be pulsed to 21V during write and erase, and held at 5V during the other two modes.

TABLE I. Mode Selection $V_{CC} = 5V \pm 5\%$

Mode \ Pin	CE (18)	OE (20)	VPP (21)	Inputs/ Outputs
Read	VIL	VIL	4V to 6V	DOUT
Standby	VIH	Don't Care	4V to 6V	Hi-Z
Byte Erase	VIL	VIH	20V to 22V	DIN = VIH
Byte Write	VIL	VIH	20V to 22V	DIN
Chip Erase (Note 11)	VIL	9V to 15V	20V to 22V	DIN = Don't Care
E/W Inhibit	VIH	Don't Care	4V to 22V	Hi-Z

7

Device Operation (Continued)

READ MODE

Both $\overline{CE}$ and $\overline{OE}$ must be at logic low levels to obtain information from the device. Chip enable ($\overline{CE}$) is the power control pin and could be used for device selection. The output enable ($\overline{OE}$) pin serves to gate internal data to the output pins. Assuming that the address inputs are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after a time delay of $t_{\overline{OE}}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{\overline{OE}}$.

CHIP ERASE MODE

Should one wish to erase the entire NMC9716 array at once, the device offers a chip erase function. When the chip erase function is performed, all 2k bytes are returned to a logic 1 (FF) state.

The NMC9716's chip erase function is engaged when the output enable ($\overline{OE}$) pin is raised above 9V. When $\overline{OE}$ is greater than 9V and $\overline{CE}$ and VPP are in the normal write mode, the entire array is erased. This chip erase function takes approximately 10 ms. The data input pins are don't care during this time to allow for ease in chip erase. *Figure 3* is an example for an $\overline{OE}$ control switch.

VPP PULSE

If using VPP to write or erase, the shape of the VPP pulse can rise to 21V through an RC waveform (0 μs–750 μs time constant), such as the NMC2816, or a linear ramp (0 μs–750 μs). There is no restriction on the rising edge of VPP if using $\overline{CE}$ to write or erase.

Figure 4 shows an example for a VPP switch design, useful where programming will occur over the specified temperature and operating voltage conditions.

WRITE MODE

The NMC9716 is erased and reprogrammed electrically rather than optically, as opposed to EPROMs which require UV light. The device offers dramatic flexibility because both byte (single location) and chip erase are possible.

To write a particular location, that byte must be erased prior to a data write. Erasing is accomplished by applying logic 1 (TTL high) inputs to all 8 data input pins, lowering $\overline{CE}$, and applying a 21V programming signal to VPP or raising VPP to 21V and applying a TTL low pulse to $\overline{CE}$. The $\overline{OE}$ pin must be equal to or below VIH during byte erase and write operations. The programming pulse width must be a minimum of 9 ms, and a maximum of 15 ms. Once the location has been erased, the same operation is repeated for a data write. The input pins in this case reflect the byte that is to be stored.

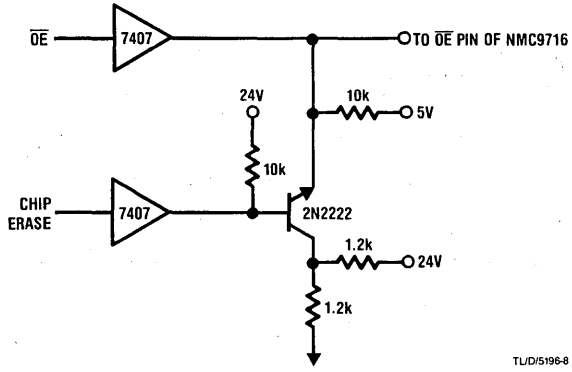


FIGURE 3. $\overline{OE}$ Chip Erase Control

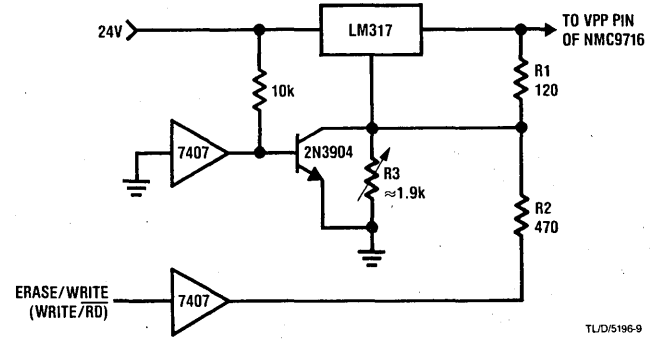


FIGURE 4. VPP Switch Design with Electronic Shutdown for $\overline{CE}$ Pulsed Erase/Write

Device Operation (Continued)

A characteristic of all E^2PROMs is that the total number of erase/write cycles is not unlimited. The NMC9716 has been designed to meet applications requiring up to 1×10^4 erase/write cycles per byte. The erase/write cycling characteristic is completely byte independent. Adjacent bytes are not affected during erase/write cycling.

Because the device is designed to be written in-system, all data sheet specifications (including write and erase operations) hold over the full operating temperature range (0°C to 70°C).

OUTPUT OR-TYING

Because NMC9716s are usually used in larger memory arrays, a 2-line control function is provided that accommodates this use of multiple memory connections. The 2-line control function allows low power dissipation (by deselecting unused devices) and the removal of bus contention from the system environment.

To most effectively use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded from addresses as the primary device selection function. $\overline{OE}$ (pin 20) should be made a common connection to all devices in-system, and connected to the $\overline{RD}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

STANDBY MODE

The NMC9716 has a standby mode which reduces active power dissipation by 52% from 610 mW to 295 mW (ICC + IPP). The NMC9716 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

National Semiconductor

NMC9716M 16k (2k x 8) Electrically Erasable PROM

Max Access/Current	NMC9716M-25	NMC9716M-35	NMC9716M-45
Max Access Time (ns)	250	350	450
Max Active Current (mA)	140	140	140
Max Standby Current (mA)	60	60	60

General Description

The NMC9716M is a 16,384-bit electrically erasable and programmable read-only memory (E^2PROM) fabricated using National's high speed, low power, N-channel double silicon gate technology. The electrical erase/write capability of the NMC9716M makes it ideal for a wide variety of applications requiring in-system, non-volatile erase and write.

The NMC9716M is pin and functionally compatible with the NMC2816M E^2PROM, with the added system feature of erasing/writing with a 5V TTL pulse on chip enable ($\overline{CE}$), while the VPP is held at 21V. The erase/write cycle is very similar to the industry standard 2716 EPROM programming cycle.

The device operates from a 5V power supply in the read mode and, with its very fast read access speed, is compatible with high performance microprocessors.

The NMC9716M is deselected when $\overline{CE}$ input is high and is automatically placed in the standby mode. This mode provides a 55% reduction in power with no increase in access time. The NMC9716M also has an output enable control to eliminate bus contention in a system environment.

The NMC9716M can be easily erased and reprogrammed in a byte-by-byte mode and the entire memory array can be erased with a single programming pulse in the chip erase mode. Byte erase is identical to byte write, with all inputs at logic one (TTL high).

Features

- Erase/write with a 5V TTL pulse or a 21V pulse
- Pin and functionally compatible with the NMC2816M
- No rise time restriction on erase/write pulse
- 2048 x 8 organization
- Conforms to JEDEC byte-wide family standard
- Microprocessor compatible architecture
- Single byte erase/write capability
- 10 ms byte erase/write time
- 10 ms chip erase mode
- Low power dissipation
  - 800 mW max (active power ICC + IPP)
  - 360 mW max (standby power ICC + IPP)

Block and Connection Diagrams

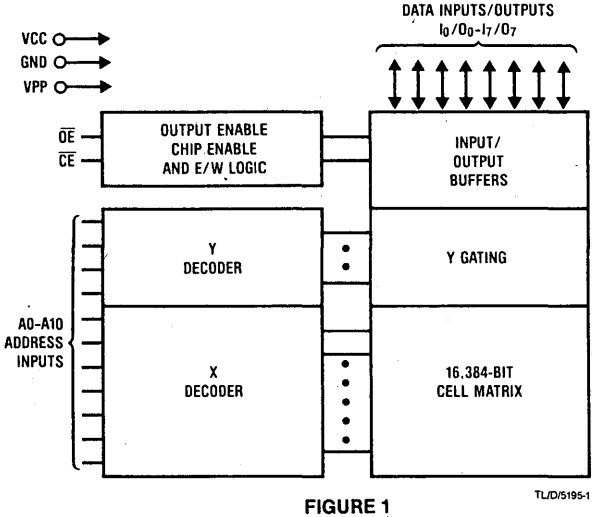


FIGURE 1

Pin Names

A0-A10	Addresses	O_0-O_7	Data Outputs
$\overline{CE}$	Chip Enable	I_0-I_7	Data Inputs
$\overline{OE}$	Output Enable	VPP	Program Voltage

Dual-In-Line Package

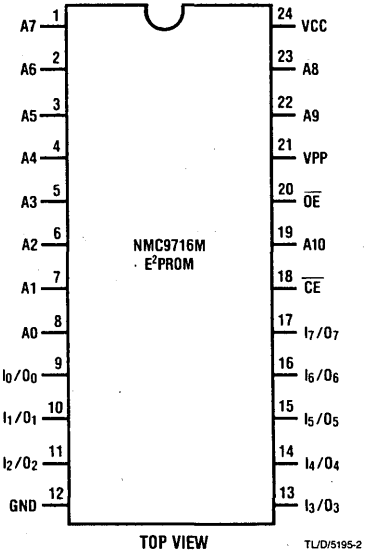


FIGURE 2

Order Number NMC9716MJ
NS Package Number J24A

Absolute Maximum Ratings

Temperature Under Bias	−65°C to +135°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
VPP Supply Voltage with Respect to Ground During Program	+22.5V to −0.3V
Maximum Duration of VPP Supply at 22V During E/W Inhibit	24 Hrs
Maximum Duration of VPP Supply at 22V During Write/Erase Programming (Note 2)	15 ms
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Temperature Range	−55°C to +125°C
VCC Power Supply (Notes 2 and 3)	5V ± 10%

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics TA = −55°C to +125°C, VCC = 5V ± 10% (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
ILI	Input Leakage Current	VIN = 5.50V			10	μA
ILO	Output Leakage Current	VOUT = 5.50V			10	μA
ICC2	VCC Current (Active)	$\overline{OE} = \overline{CE}$ = VIL		65	140	mA
ICC1	VCC Current (Standby)	$\overline{CE}$ = VIH		12	60	mA
IPP(R)	VPP Current (Read)	VPP = 6V, $\overline{CE}$ = VIH or VIL		1	5	mA
VIL	Input Low Voltage		−0.1		0.8	V
VIH	Input High Voltage		2.2		VCC + 1	V
VOL	Output Low Voltage	IOL = 2.1 mA			0.45	V
VOH	Output High Voltage	IOH = −400 μA	2.4			V
VPP	Read Voltage		4		6	V
WRITE OPERATION						
VPP	Write/Erase Voltage		20	21	22	V
IPP(W)	VPP Current (Write/Erase)	$\overline{OE}$ = VIH, $\overline{CE} \leq$ VIL, VPP = 22V		6	15	mA
$V\overline{OE}$	$\overline{OE}$ Voltage (Chip Erase)	$I\overline{OE} \leq 10$ μA	9		15	V
IPP(I)	VPP Current (Inhibit)	$\overline{CE}$ = VIH, VPP = 22V		2	5	mA
IPP(C)	VPP Current (Chip Erase)	$\overline{OE} = V\overline{OE}$, $\overline{CE}$ = VIL, VPP = 22V		2	5	mA

Capacitance TA = 25°C, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
CIN	Input Capacitance	VIN = 0V		5	10	pF
COUT	Output Capacitance	VOUT = 0V			10	pF
CVCC	VCC Capacitance	$\overline{OE} = \overline{CE}$ = VIH			500	pF
CVPP	VPP Capacitance	$\overline{OE} = \overline{CE}$ = VIH			50	pF

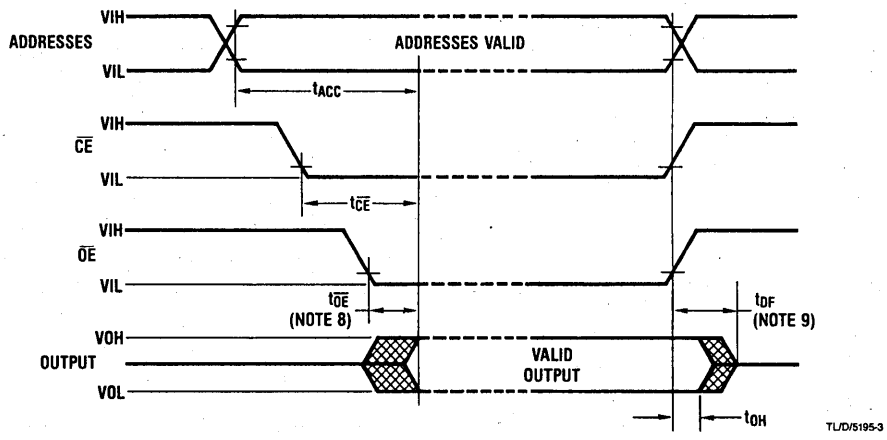
AC Test Conditions

Output Load	1 TTL gate and CL = 100 pF
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = -55°C$ to $+125°C$, $V_{CC} = 5V \pm 10\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	NMC9716M-25			NMC9716M-35			NMC9716M-45			Uni
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$			250			350			450	ns
$t_{\overline{CE}}$	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$			250			350			450	ns
$t_{\overline{OE}}$	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		120	10		140	10		140	ns
t_{DF}	Output Disable to Output Float (Note 9)	$\overline{CE} = \overline{OE} = V_{IL}$	0		100	0		100	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0			0			0			ns

Read Waveforms (Note 6)



Note 1: This parameter is only sampled and not 100% tested.

Note 2: To prevent spurious device erasure or write, VCC must be applied simultaneously or before 21V application of VPP. VPP cannot be driven to 21V without previously applying VCC.

Note 3: VCC must be applied at the same time or before VPP and removed after or at the same time as VPP. To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: Adherence to t_{WP} specification is important to device reliability.

Note 5: To allow immediate read verify capability, VPP can be driven low in less than 50 ns.

Note 6: All times shown in parentheses are minimum times and are ns unless otherwise specified.

Note 7: Prior to a data write, an erase operation must be performed. For a byte erase, data in = VIH, and for chip erase, data in = don't care.

Note 8: $\overline{OE}$ may be delayed up to 210 ns after falling edge of $\overline{CE}$ without impact on t_{CE} for NMC9716M-35.

Note 9: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

Note 10: When programming with VPP, the rising edge of VPP can follow a linear or an exponential waveform. That waveform's rise time or time constant is specified as t_{PRC}. There is no restriction on the rising edge of VPP if programming with $\overline{CE}$.

Note 11: In the chip erase mode DIN = don't care.

Note 12: In byte erase or write mode, $\overline{OE}$ must be equal to VIH.

Note 13: More than one address location can be erase/written without pulsing VPP between every address.

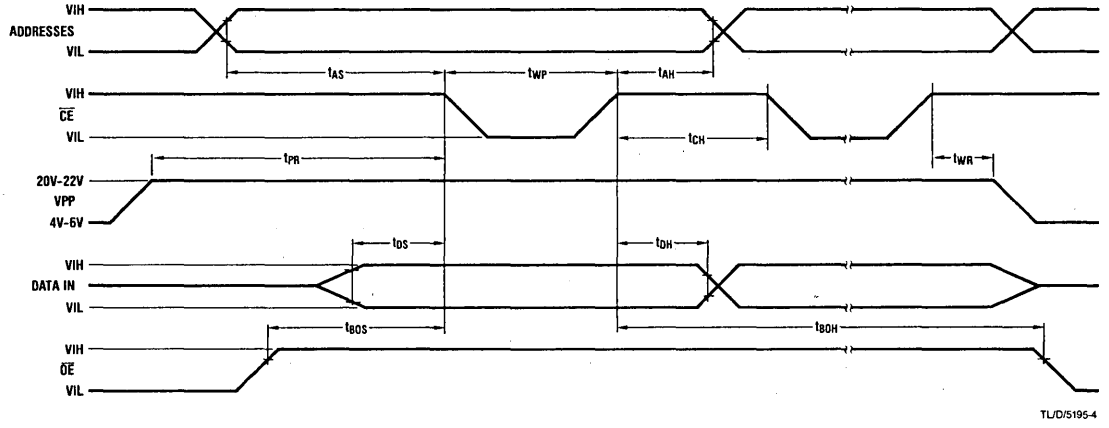
Note 14: $\overline{CE}$ = VIH places the chip in a low power standby condition, and must be applied for a minimum time of t_{CH} before the start of any byte programming cycle.

Write Mode AC Electrical Characteristics TA = −55°C to +125°C, VCC = 5V ± 10% (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address Set-Up Time		150			ns
t_{AH}	Address Hold Time		50			ns
t_{CS}	$\overline{CE}$ Set-Up Time		150			ns
t_{PR}	VPP Set-Up Time		0			ns
t_{DS}	Data Set-Up Time	$\overline{OE}$ = VIH	0			ns
t_{DH}	Data Hold Time	$\overline{OE}$ = VIH	50			ns
t_{WP}	Write Pulse Width (Note 4)		9	10	15	ms
t_{WR}	Write Recovery Time		50			ns
t_{OS}	Chip Clear Set-Up Time		0			ns
t_{OH}	Chip Clear Hold Time		0			ns
t_{PRC}	VPP RC Time Constant (Note 10)		0		750	μs
t_{PFT}	VPP Fall Time (Note 5)				100	μs
t_{BOS}	Byte Erase/Write Set-Up Time (Note 12)		0			ns
t_{BOH}	Byte Erase/Write Hold Time (Note 12)		0			ns
t_{CH}	Chip Enable High Time		1			μs

Recommended Erase/Write Waveforms

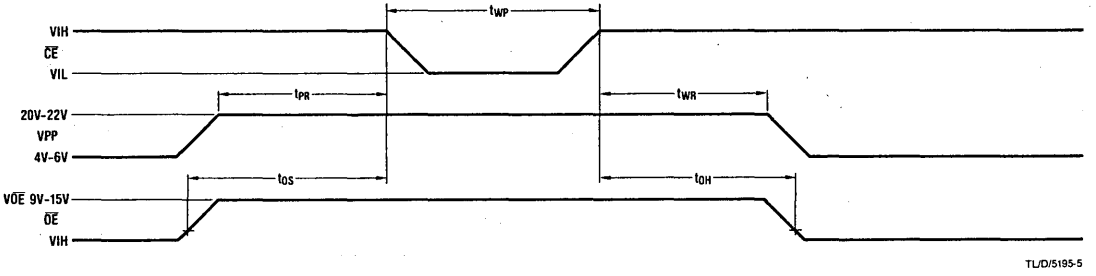
$\overline{CE}$ Pulsed (Notes 7, 12 and 13)



TL/D/5195-4

Chip Erase Waveforms

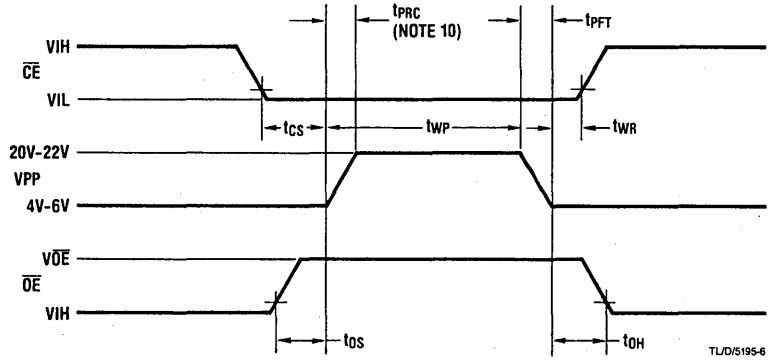
$\overline{CE}$ Pulsed (Note 11)



TL/D/5195-5

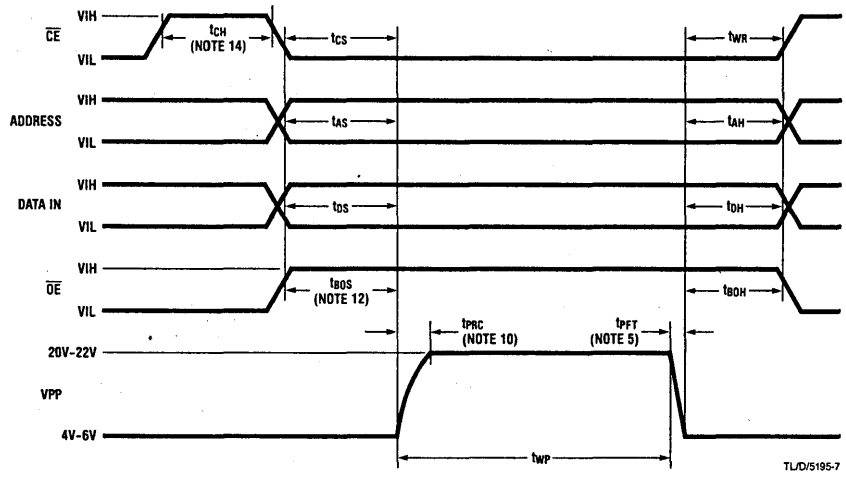
Chip Erase Waveforms (Continued)

VPP Pulsed (Note 11)



Alternate Erase/Write Waveforms (NMC2816M compatible) (Note 6)

Byte Erase and Byte Write Programming Cycle, VPP Pulsed



Device Operation

The NMC9716M has six modes of operation, listed in Table I. All operational modes are designed to provide maximum microprocessor compatibility and system consistency. The device pinout is a part of the JEDEC approved byte-wide non-volatile memory family, allowing appropriate and cost-effective density and functionality upgrades.

All control inputs are TTL compatible with the exception of chip erase. The VPP voltage must be pulsed to 21V during write and erase, and held at 5V during the other two modes.

TABLE I. Mode Selection V_{CC} = 5V ±10%

Pin / Mode	$\overline{CE}$ (18)	$\overline{OE}$ (20)	VPP (21)	Inputs/ Outputs
Read	VIL	VIL	4V to 6V	DOUT
Standby	VIH	Don't Care	4V to 6V	Hi-Z
Byte Erase	VIL	VIH	20V to 22V	DIN = VIH
Byte Write	VIL	VIH	20V to 22V	DIN
Chip Erase (Note 11)	VIL	9V to 15V	20V to 22V	DIN = Don't Care
E/W Inhibit	VIH	Don't Care	4V to 22V	Hi-Z

Device Operation (Continued)

READ MODE

Both $\overline{CE}$ and $\overline{OE}$ must be at logic low levels to obtain information from the device. Chip enable ($\overline{CE}$) is the power control pin and could be used for device selection. The output enable ($\overline{OE}$) pin serves to gate internal data to the output pins. Assuming that the address inputs are stable, address access time (t_{ACC}) is equal to the delay from $\overline{CE}$ to output ($t_{\overline{CE}}$). Data is available at the outputs after a time delay of $t_{\overline{OE}}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}-t_{\overline{OE}}$.

CHIP ERASE MODE

Should one wish to erase the entire NMC9716M array at once, the device offers a chip erase function. When the chip erase function is performed, all 2k bytes are returned to a logic 1 (FF) state.

The NMC9716M's chip erase function is engaged when the output enable ($\overline{OE}$) pin is raised above 9V. When $\overline{OE}$ is greater than 9V and $\overline{CE}$ and VPP are in the normal write mode, the entire array is erased. This chip erase function takes approximately 10 ms. The data input pins are don't care during this time to allow for ease in chip erase. *Figure 3* is an example for an $\overline{OE}$ control switch.

VPP PULSE

If using VPP to write or erase, the shape of the VPP pulse can rise to 21V through an RC waveform (0 μs-750 μs time constant), such as the NMC2816M, or a linear ramp (0 μs-750 μs). There is no restriction on the rising edge of VPP if using $\overline{CE}$ to write or erase.

Figure 4 shows an example for a VPP switch design, useful where programming will occur over the specified temperature and operating voltage conditions.

WRITE MODE

The NMC9716M is erased and reprogrammed electrically rather than optically, as opposed to EPROMs which require UV light. The device offers dramatic flexibility because both byte (single location) and chip erase are possible.

To write a particular location, that byte must be erased prior to a data write. Erasing is accomplished by applying logic 1 (TTL high) inputs to all 8 data input pins, lowering $\overline{CE}$, and applying a 21V programming signal to VPP or raising VPP to 21V and applying a TTL low pulse to $\overline{CE}$. The $\overline{OE}$ pin must be equal to or below VIH during byte erase and write operations. The programming pulse width must be a minimum of 9 ms, and a maximum of 15 ms. Once the location has been erased, the same operation is repeated for a data write. The input pins in this case reflect the byte that is to be stored.

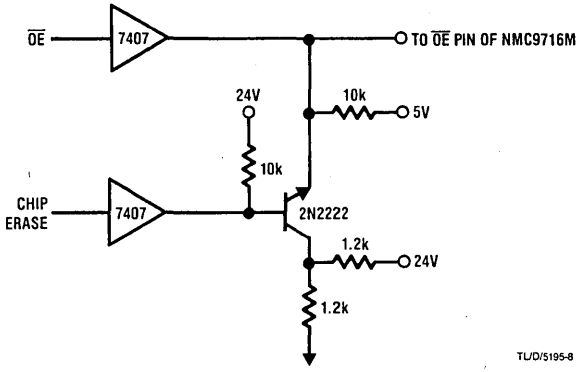


FIGURE 3. $\overline{OE}$ Chip Erase Control

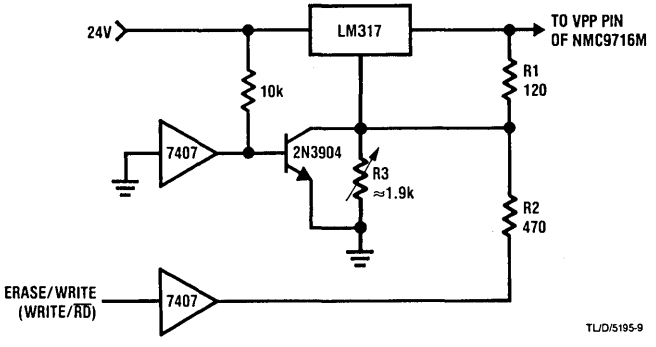


FIGURE 4. VPP Switch Design with Electronic Shutdown for $\overline{CE}$ Pulsed Erase/Write

Device Operation (Continued)

A characteristic of all E^2PROMs is that the total number of erase/write cycles is not unlimited. The NMC9716M has been designed to meet applications requiring up to 1×10^4 erase/write cycles per byte. The erase/write cycling characteristic is completely byte independent. Adjacent bytes are not affected during erase/write cycling.

Because the device is designed to be written in-system, all data sheet specifications (including write and erase operations) hold over the full operating temperature range ($-55°C$ to $+125°C$).

OUTPUT OR-TYING

Because NMC9716Ms are usually used in larger memory arrays, a 2-line control function is provided that accommodates this use of multiple memory connections. The 2-line control function allows low power dissipation (by deselecting unused devices) and the removal of bus contention from the system environment.

To most effectively use these two control lines, it is recommended that $\overline{CE}$ (pin 18) be decoded from addresses as the primary device selection function. $\overline{OE}$ (pin 20) should be made a common connection to all devices in-system, and connected to the $\overline{RD}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

STANDBY MODE

The NMC9716M has a standby mode which reduces active power dissipation by 55% from 800 mW to 360 mW (ICC + IPP). The NMC9716M is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

National Semiconductor

PRELIMINARY

NMC9817 16,384-Bit (2k x 8) E²PROM

General Description

The NMC9817 is a fast 5V-only E²PROM which offers many desired features, making it ideally suited for efficiency and ease in system design. The added features on the NMC9817 include: 5V-only operation provided by an on-chip V_{PP} generator during erase-write; address and data latches to reduce part count and to free the microprocessor while the chip is busy during erase-write; 'Ready' line indicator to indicate status of chip to the microprocessor; and automatic erase before byte-write. It can meet applications requiring up to 10^4 write cycles per byte. The NMC9817 is a product of National's advanced E²PROM stepper technology and uses the powerful XMOS™ process for reliable, non-volatile data storage.

The NMC9817 sharply minimizes the interfacing hardware logic and firmware required to perform data writes. The device has complete self-timing which leaves the processor free to perform other tasks until the NMC9817 signals 'ready'. With an automatic erase before write, the user benefits by saving an erase command contributing to efficient usage of system processing time. On-chip address and data latching further enhances system performance.

The NMC9817's very fast read access times make it compatible with high performance microprocessor applications. It uses the proven two line control architecture which eliminates bus contention in a system environment. Combining these features with the NMC9817's open-drain 'Ready' signal makes the device an extremely powerful, yet simple to use, E²PROM memory.

The density, and level of integrated control, make the NMC9817 suitable for users requiring minimum hardware overhead, high system performance, minimal board space and design ease. Designing with and using the NMC9817 is extremely cost effective as the required high voltage and interfacing hardware required for other E²PROM devices has been eliminated by 5V-only operation and on-chip latches. See *Figures 1, 2, and 3* for the NMC9817 block diagram, pinout, and simple interface requirements.

Features

- Single 5V supply (eliminates an external 21V V_{PP})
- Self-timed byte-write with auto erase
- No external capacitor or pulse shaping circuits
- On-chip address and data latches
- Two line output control
- TRI-STATE® outputs
- RDY pin indicator
- Fast byte-writing
  - Write cycle (2 ms typical)
  - E/W cycle (4 ms typical)
- Very fast access times
  - NMC9817-20—200 ns
  - NMC9817-25—250 ns
  - NMC9817-35—350 ns
- Direct microprocessor interface capability
- No support components needed
- Reliable E²PROM XMOS stepper technology

Block and Connection Diagrams

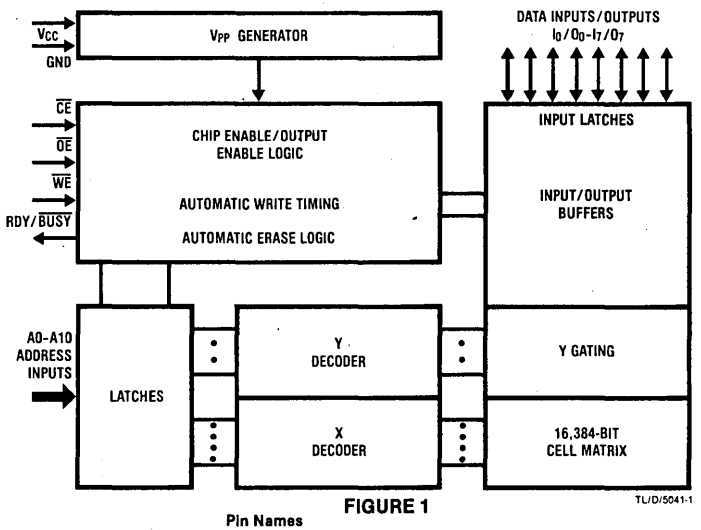


FIGURE 1

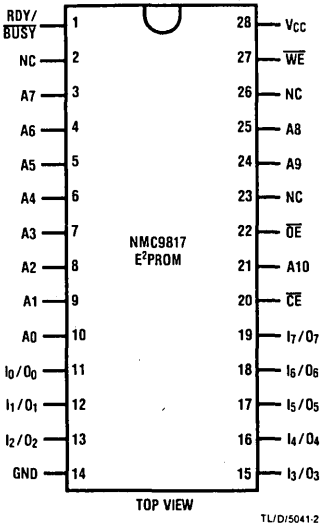


FIGURE 2

Pin Names

A0-A10	Addresses	I_0-I_7	Data Inputs
$\overline{CE}$	Chip Enable	RDY/$\overline{BUSY}$	Device Ready/Busy (Open-Drain Output)
$\overline{OE}$	Output Enable	NC	No Connect
O_0-O_7	Data Outputs		

Order Number NMC9817J-20, NMC9817J-25 or NMC9817J-35
NS Package Number J28A

Absolute Maximum Ratings

Temperature Under Bias	−10°C to +80°C
Storage Temperature	−65°C to +125°C
All Input or Output Voltages with Respect to Ground	+6V to −0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

Temperature Range	0°C to +70°C
V_{CC} Power Supply (Notes 2 and 3)	5V ± 5%

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
READ OPERATION						
I_{LI}	Input Leakage Current	$V_{IN} = 5.25V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.25V$			10	μA
I_{CCA}	V_{CC} Current (Active)	$\overline{OE} = \overline{CE} = V_{IL}$		40	80	mA
I_{CCS}	V_{CC} Current (Standby)	$\overline{CE} = V_{IH}$		12	25	mA
V_{IL}	Input Low Voltage		−0.1		0.8	V
V_{IH}	Input High Voltage		2.0		$V_{CC}+1$	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V
WRITE OPERATION						
I_{CCW}	V_{CC} Current (Write)	RDY/$\overline{BUSY}$ = V_{OL}		40	80	mA

Capacitance $T_A = 25°C$, f = 1 MHz (Note 1)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
C_{IN}	Input Capacitance	$V_{IN} = 0V$		5	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$			10	pF

AC Test Conditions

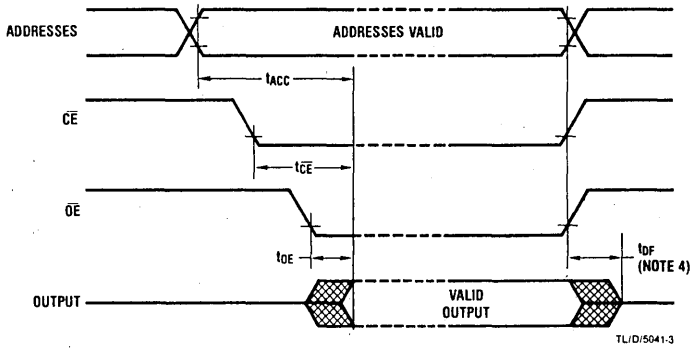
Output Load	1 TTL gate and $C_L = 100$ pF
Input Pulse Levels	0.45V to 2.4V
Timing Measurement Reference Level	
Input	1V and 2V
Output	0.8V and 2V

Read Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	NMC9817-20			NMC9817-25			NMC9817-35			Units
			Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	Min	Typ (Note 1)	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		150	200		200	250		300	350	ns
t_{OE}	Output Enable to Output Delay	$\overline{CE} = V_{IL}$	10		75	10		100	10		120	ns
t_{DF}	Output Disable to Output Float	$\overline{CE}$ or $\overline{OE} = V_{IL}$	0		80	0		100	0		100	ns
t_{OH}	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE}$, $\overline{OE} = V_{IL}$	0			0			0			ns

Switching Time Waveforms

Read



Write Mode AC Electrical Characteristics $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$ (Notes 2 and 3)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
t_{AS}	Address to Write Set-Up Time		20			ns
t_{CS}	$\overline{CE}$ to Write Set-Up Time		20			ns
t_{WP}	Write Pulse Width		100			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Set-Up Time	$\overline{OE} = V_{IH}$	50			ns
t_{DH}	Data Hold Time	$\overline{OE} = V_{IH}$	20			ns
t_{CH}	$\overline{CE}$ Hold Time		20			ns
t_{DB}	Time to Device Busy				120	ns
t_{WR}	Byte-Write Cycle Time			4	10	ms

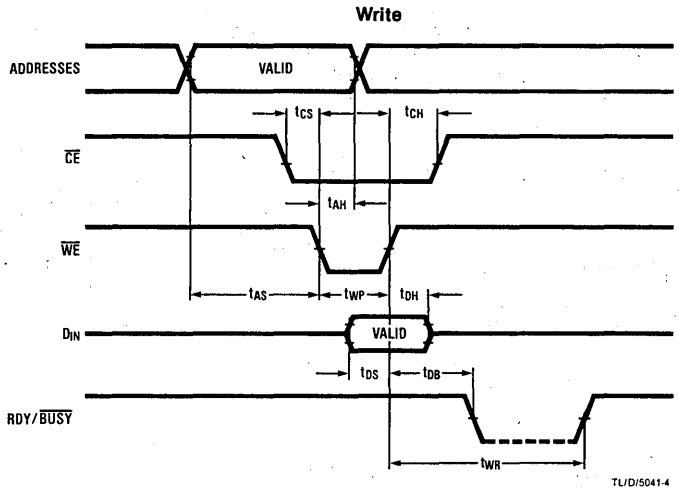
Note 1: This parameter only sampled and not 100% tested.

Note 2: To prevent spurious device erase or write, $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be applied simultaneously or before application of V_{CC}. $\overline{WE}$ or $\overline{CE} = V_{IH}$ must be removed simultaneously or after V_{CC}.

Note 3: To prevent damage to the device it must not be inserted into or removed from a board with power applied.

Note 4: t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

Switching Time Waveforms (Continued)



Device Operation

The NMC9817 has 4 modes of user operation which are detailed in Table I. All modes are designed to enhance the NMC9817's functionality to the user and provide total microprocessor compatibility.

TABLE I. $V_{CC} = 5V$

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I_0/O_0-I_7/O_7	RDY/$\overline{BUSY}$
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Hi-Z
Standby	V_{IH}	X	X	Hi-Z	Hi-Z
Write	V_{IL}	V_{IH}	⊓	D_{IN}	V_{OL}
Busy	X	X	X	Hi-Z	V_{OL}

WRITE MODE

The NMC9817 is programmed electrically in-circuit, yet it provides the non-volatility usually obtained by optical erasure in EPROMS and by batteries with CMOS RAM. Writing to non-volatile memory has never been easier as no high voltage, external latching, erasing or timing is needed. When commanded to byte-write, the NMC9817 automatically latches the address, data, and control signals and starts the write cycle. Concurrently, the 'Ready' line goes low, indicating that the NMC9817 is busy and that it can be deselected to allow the processor to perform other tasks. The Ready/$\overline{Busy}$ signal is an open-drain output. During the write, a high V_{PP} is generated on-chip to perform an automatic byte-erase, then write.

As a precaution against spurious signals which may cause an inadvertant write cycle, or interfere with a valid signal, it is recommended that a pullup resistor be used on the $\overline{WE}$ pin, pin 27 (see *Figure 4*).

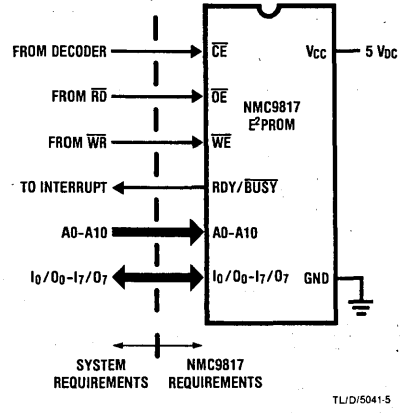


FIGURE 3. Simple NMC9817 Interface Requirements

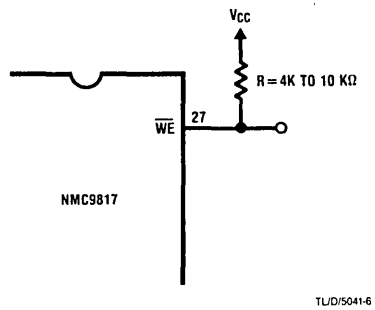


FIGURE 4. Pullup R on $\overline{WE}$

Device Operation (Continued)

READ MODE

One aspect of the NMC9817's high performance is its very fast read access time—typically less than 200 ns. Its read cycle is similar to that of EPROMS and static RAMs. It offers a two line control architecture to eliminate bus contention. The NMC9817 can be selected using decoded system address lines to $\overline{CE}$ and then the device can be read, within the device selection time, using the processor's $\overline{RD}$ signal connected to $\overline{OE}$.

STANDBY MODE

The NMC9817 has a standby mode in which power consumption is reduced by 70%. This offers the user power supply cost benefits when designing a system with NMC9817s. This mode occurs when the device is deselected ($\overline{CE} = V_{IH}$). The data pins are put into the high impedance state regardless of the signals applied to $\overline{OE}$ and $\overline{WE}$ concurrent with the reading and writing of other devices.

SYSTEM IMPLEMENTATION AND APPLICATION

The NMC9817 is compatible with industry standard microprocessors. It requires no interface circuitry and no support circuitry.

The NMC9817 is ideal for non-volatile memory requirements in applications requiring storage of user defined functions, calibration constants, configuration parameters and accumulated totals. Soft key configuration in a graphics terminal is an example where user defined functions, such as protocol, color, margins and character fonts can be keyed in by the user. Calibration constants could be stored by the NMC9817 in the smart interface for a robot's axis of movement. Movement constants, compensation algorithms and learned axis characteristics can be stored. In programmable controllers and data loggers, configuration parameters for polling time, sequence and location, could be stored in the NMC9817. Accumulated totals for dollars, energy consumption, volume and even the logging of service done on computer boards or systems can be stored in the NMC9817.

The NMC9817 is cost effective for lower density E^2PROM applications and can therefore be used to provide a lower system cost to the user compared to the 2816 or 2817. The user will find that tangible cost savings per system include: board space and component reductions, reduced assembly costs, savings in inventory costs, handling costs and quality assurance. The designer will find the NMC9817 reduces design time by a sizable factor over the 2816 or 2817 due to the integration of timing, logic, latching and 5V-only operation.

The NMC9817 will also open up new applications in environments where flexible parameter/data storage could not be implemented before. For example, applications with board space constraints are ideal for the NMC9817. Several NMC9817s can reside in the same space as one (1) 2816 with its support circuits. This is due to the reduction of all components required including the V_{PP} generator.

WRITE TIME CHARACTERISTICS

The NMC9817's internal write cycle contains an automatic erase feature. The 2816 does not have this capability and must be given an external erase cycle prior to a write. Typically, these devices will write in times less than 9 ms, but the worst-case bit defines the minimum specification.

The NMC9817's internal cycle consists of an automatic 2 ms (typical) erase followed by a 2 ms (typical) write. The total cycle is then typically 4 ms. This cycle is the time that 'Ready' is held low by the device. The NMC9817 maximum specification is 10 ms.

National Semiconductor

PRELIMINARY

microCMOS

NMC98C64A, 65,536-Bit (8K × 8) E²PROM

General Description

The NMC98C64A is a 5V-only CMOS E²PROM with desirable ease-of-use features that facilitate in-circuit programming using a single supply and TTL-level signals. In addition, the NMC98C64A is operationally compatible with present high density EPROMs which require high voltage programming and UV erasing. The NMC9864A is a state-of-the-art product that uses the advanced microCMOS stepper-based technology. The process is an enhancement of the proven XMOS™ process for reliable, non-volatile data storage.

Writing data into NMC98C64A is analogous to writing to a SRAM. A 100-ns min TTL pulse to the $\overline{WE}$ pin initiates a byte write operation which is automatically timed out. Address and data latches free the system bus for the duration of the write. Ready/$\overline{busy}$ facilitates service by providing an interrupt to the controller; an open-drain output facilitates "wire-OR" connection in larger systems.

A 32-byte page write allows data to be accepted at an effective rate of 300 μs/page, or 2.6 seconds to write an entire chip. An optional chip erase feature is also available.

The NMC98C64A also features $\overline{data}$ polling, a new feature that enables the E²PROM to signal the processor that a write operation is done, without requiring any extra hardware.

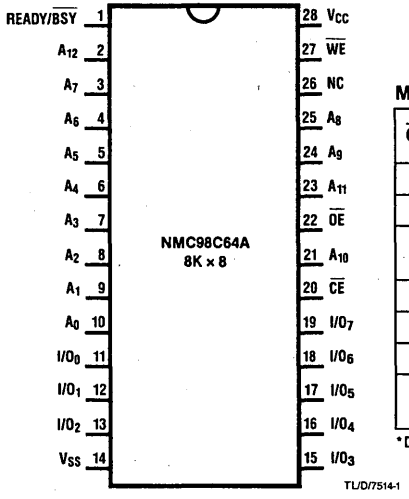
Ready/$\overline{busy}$ interrupt output is another feature that enables the processor to know that a write operation is over. This employs an otherwise no-connect pin 1.

Features

The NMC98C64A offers the following smart features:

- Simple byte and page write
  - Single TTL-level, RAM-like $\overline{WE}$
  - Address and data latches
  - Page mode write up to 32 bytes per page
  - $\overline{DATA}$ polling verification
  - Internal auto erase
  - On-chip timer
  - Optional chip erase
  - Ready/$\overline{busy}$ open-drain interrupt output
  - Write protection
- Byte or page write: 10 ms maximum
  - Effective 300 μs/write page
  - Entire chip write: 2.6 seconds
- Fast access time: 250 ns maximum
- Low CMOS power: 10 mA, active
  100 μA, standby
- Single 5V supply
- 28-pin JEDEC-approved byte-wide pin-out

Connection Diagram



TL/D/7514-1

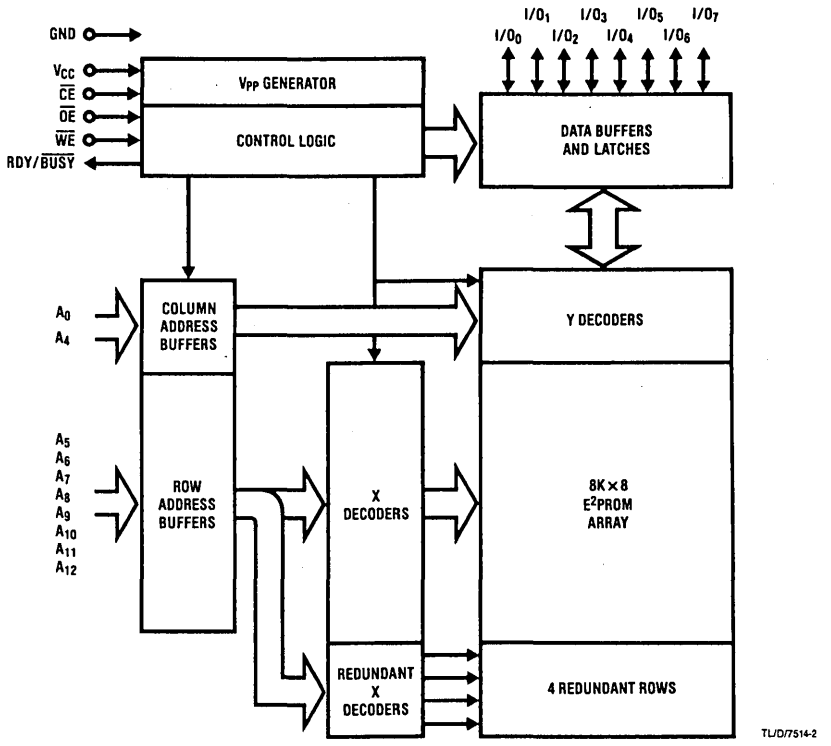
NS Package Number J16A

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Ready/$\overline{Busy}$	Power
L	L	L	Read	D_{OUT}	Hi-Z	Active
L	H	⊓	Write	D_{IN}	0	Active
H	X	X	Standby and Write Inhibit	Hi-Z	Hi-Z	Standby
X	L	X	Write Inhibit	—	Hi-Z	—
X	X	H	Write Inhibit	—	Hi-Z	—
L	V_{OE}	L	Chip Erase	D_{IN} = H	Hi-Z	Active
L	L	H	$\overline{DATA}$ Polling	$I/O_7 = I_7$*	0	Active
				$I/O_7 = I_7$	1	Active

*During write cycle, I/O_0 through I/O_7 are Hi-Z.

Block Diagram



DEVICE OPERATION

Addresses (A_0–A_{12})
E^2PROM bytes are selected for reading or writing by the address pins.

CHIP ENABLE ($\overline{CE}$)

A device is selected when $\overline{CE}$ is LOW. Power is reduced to less than .1% during disable when CE is HIGH.

DATA-IN/DATA-OUT (I/O_0-I/O_7)

Data is written into or read from a selected device through the I/O pins. The I/O pins are in the high impedance state when CE is HIGH, or when OE is HIGH.

OUTPUT ENABLE ($\overline{OE}$)

Reading data from the NMC98C64A is similar to reading data from a static RAM. Data is read from a selected device with WE HIGH and OE LOW.

NMC98C64A uses a 2-line output control architecture to eliminate bus contention in a system environment. The I/O pins are in a high impedance state whenever $\overline{OE}$ or $\overline{CE}$ is HIGH.

WRITE ENABLE ($\overline{WE}$)

Writing data to the NMC98C64A is similar to writing data into a static RAM. A LOW-going $\overline{WE}$ pulse applied to a selected device with $\overline{OE}$ HIGH initiates a cycle that writes data at the I/O pins into a location selected by the address pins. A byte write cycle once initiated will automatically continue to completion in 5 ms typically. During a byte write cycle, addresses are latched on the last falling edge of $\overline{CE}$ or $\overline{WE}$; data is latched on the first rising edge of $\overline{CE}$ or $\overline{WE}$. System design is greatly simplified, since writing requires only a single 5V supply and a single TTL-level $\overline{WE}$ signal. Addresses and data are conveniently latched in less than 100 ns during a byte write. As a precaution against spurious signals which may cause an inadvertant write cycle, or interfere with a valid signal, it is recommended that a pullup resistor be used on the $\overline{WE}$ pin, pin 27 (see *Figure 1*).

AUTOMATIC PAGE WRITE

The page write feature of NMC98C64A allows 1 to 32 bytes of data to be written into the E^2PROM in a single write cycle. Following a byte write signal to the E^2PROM, the user has 300 μs to write 0–31 additional bytes of data into the E^2PROM, providing that the byte addresses are on the same 32-byte page in memory. This page mode allows the entire NMC98C64A to be rewritten in 2.6 sec-

onds. A page is defined by addresses A_5–A_{12}. The 32 bytes within the page are defined by A_0–A_4. All bytes to be written must be loaded within the first 300 μs after initiating the write of the first byte. All subsequent writes during the page load cycle must go to the same page (addresses A_5–A_{12}) as the first byte. The bytes may be written in any order.

OPTIONAL CHIP ERASE

All data can be written to "1", the erase state, in a chip erase cycle by raising $\overline{OE}$ to 15 volts and bringing $\overline{WE}$ low while holding all data inputs high.

$\overline{DATA}$ POLLING

The NMC98C64A features $\overline{DATA}$ polling to signal the completion of a byte or page write cycle. During a write cycle, an attempted read of the last byte written results in the data complement of that byte at I/O_7. After completion of the write cycle, true data is available. $\overline{DATA}$ polling allows a simple read/compare operation to determine the status of the chip, eliminating the need for external hardware.

WRITE PROTECTION

There are three features that protect the nonvolatile data from an inadvertent write.

- Noise Protection — A $\overline{WE}$ pulse of less than 20 ns will not initiate a write cycle.
- V_{CC} Sense—When the V_{CC} is approximately 4 volts, all functions are inhibited.
- Write Inhibit — Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power-on and power-off (V_{CC}).

ENDURANCE

National Semiconductor E^2PROMs are designed for applications requiring up to 10,000 write cycles per byte.

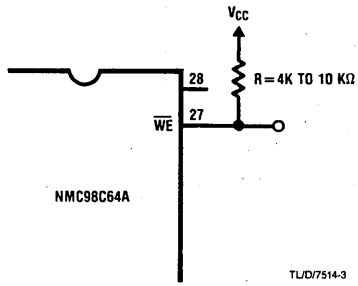


FIGURE 1

Threshold Bit Mapping in EEPROMs (NMC2816)

National Semiconductor
Application Brief 5
Masood Alavi, Sr. Apps. Mgr.
February 1983

Threshold bit mapping is designed to monitor the endurance of an E²PROM cell after a large (>10^5) number of erase/write cycles. The technique calls for monitoring the cell current of a bit under identical voltage, timing and temperature conditions and repeating the same after x-number of erase/write cycles. On a 'good' cell the variation in cell current will be no more than a few (≃ 2μA) microamps over 10,000 cycles under typical conditions of Vcc = Vpp = 5V

Temp = 25°C

V_{in} = 2V

Timing = same for each case

On a cell approaching 'wear out' a much larger variation would be noticed in the cell current. The variation could be in either direction depending on the nature of conductive degradation of the thin tunnel oxide as a result of free charge trapping in the insulation which is a gradual phenomena.

Figure 1 shows a plot of V_{te} and V_{tw} vs number of erase/write cycles. The cell current under both erased and write conditions will hold pretty stable in the flat region.

It must be noted that identical conditions of measurement are very important. The actual value of Vpp and erase/write pulse width must be kept the same prior to measurement.

The NMC2816/9716 are designed with a special test mode, which allow connecting each of the outputs with its respective bit. In this mode each I/O pin gets connected to the drain of the cell transistor allowing a cell-current measurement of the respective bit in the addressed byte.
Figure 2 shows the threshold bit mapping circuit for a single bit. To put the NMC2816/9716 in the threshold bit mapping mode, the following set up is required:

Vcc = Vpp = 5V ± (5%)

$\overline{OE}$ = V_{IH} = Logic 1 state

$\overline{CE}$ = 20V

addresses = selected locations

I/O = force 2V measure current in μAmps

T_A = constant = 25°C (arbitrary)

The cell current of any number of desired bits can be measured in an erased and written state. In the 'erased' state negligible current will exist till the onset of wearout. In the 'written' state a low magnitude current (of 50–60μA) will be measurable till the onset of wearout. It is important that the amplitude and pulse width of erase/write pulse prior to measurement remains identical for all measurements. The measurements can be repeated over a number of erase/write cycles and plotted against the same. At the onset of wearout there will be a radical change in the monitored currents; the erased state current will increase in magnitude while the written state current will fall in magnitude.

It is also possible to calculate V_{te} and V_{tw} from the cell current measurements and plot against erase/write cycles. It must be noticed that the resultant values are at best intelligent approximations designed to give an insight into the wearout phenomena due to erase/write cycles. At present the threshold bit mapping technique remains an observation technique. The purpose of this technique is to study the wearout phenomena and its effects in EEPROMS. It is however not recommended as a screening technique at present.

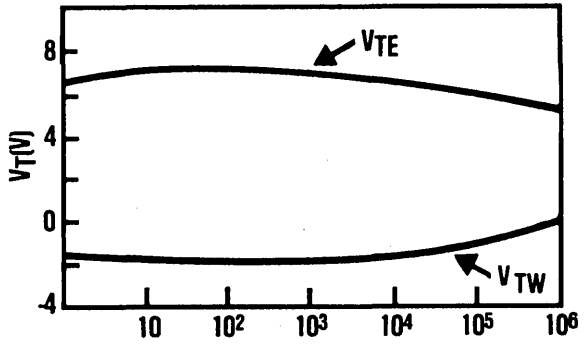
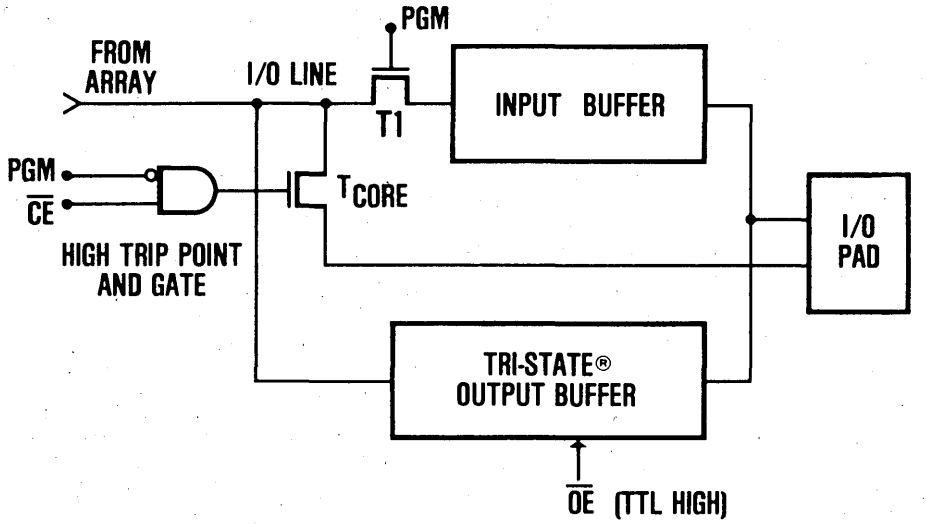


FIGURE 1. ERASE/WRITE Cycles

TL/D/5191–1



TL/D/5191-2

FIGURE 2. Threshold Bit Mapping Circuitry

Protecting Data in the NMC9306/COP494 and NMC9346/COP495 Serial EEPROMs

National Semiconductor
Application Brief 15
Asim Bajwa
May 1984

The NMC9306/COP494 and NMC9346/COP495 are non-volatile serial access memories with the following salient features:

- Low cost
- Single supply read/write/erase operation (5V ± 10%)
- TTL compatible
- MICROWIRE™ compatible I/O
- 16 x 16 serial read/write memory (NMC9306/COP494)
  64 x 16 serial read/write memory (NMC9346/COP495)
- Self-timed programming cycle (NMC9346/COP495 only)
- Ready/busy status signal during programming (NMC9346/COP495 only)
- Read-only mode

The read-only mode is provided to prevent accidental data disturb, especially during V_{CC} power up, power down or excessive noise on the I/O or power supply pins.

Executing the EWDS instruction *(Figure 1)* activates this mode by disabling the programming modes and the high voltage pump. The READ instruction is not affected and can be executed as usual. However, all programming instructions (ERASE, WRITE, ERAL and WRAL) are ignored until the EWEN instruction is executed to enable programming.

On V_{CC} power up the device is designed to automatically enter the read-only mode to avoid accidental data loss due to power up transients. Putting the device in the read-only mode before powering down V_{CC} avoids spurious programming during power down.

The following guidelines are presented and should be incorporated into the user's designs to achieve the maximum possible protection of stored data *(Figure 2)*:

1) The device powers up in the read-only mode. However, as a backup, the EWDS instruction should be executed as soon as possible after V_{CC} to the EEPROM is powered up to ensure that it is in the read-only mode.
2) Immediately preceding a programming instruction (ERASE, WRITE, ERAL or WRAL), the EWEN instruction should be executed to enable the device for programming; the EWDS instruction should be executed immediately following the programming instruction

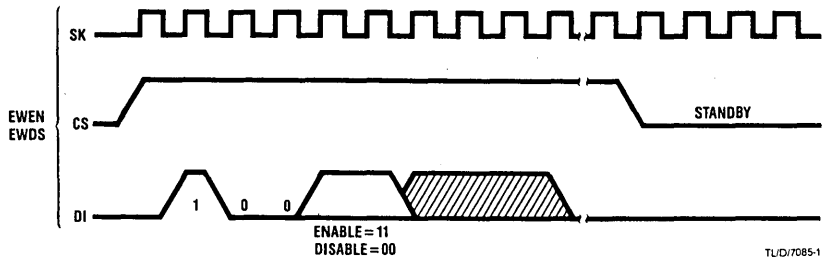
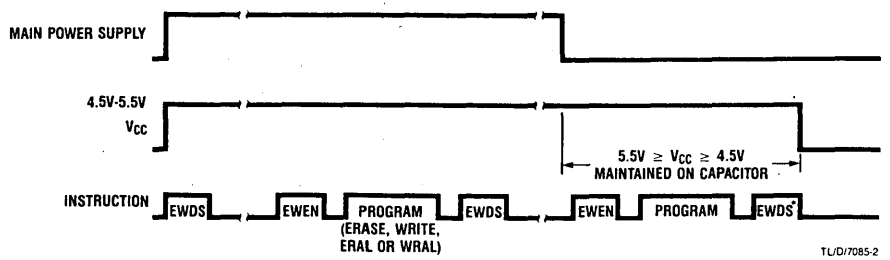


FIGURE 1. EWEN, EWDS Instruction Timing



*EWDS must be executed before V_{CC} drops below 4.5V to prevent accidental data loss during subsequent power down and/or power up transients.

FIGURE 2. Typical Instruction Flow for Maximum Data Protection

to return the device to the read-only mode and protect the stored data from accidental disturb during subsequent power transients or noise.

3) Special care must be taken in designs in which programming instructions are initiated to store data in the EEPROM after the main power supply has gone down. This is usually accomplished by maintaining V_{CC} for the EEPROM and its controller on a capacitor for a sufficient amount of time (approximately 50 ms, depending on the clock rate) to complete these operations. This capacitor must be large enough to maintain V_{CC} between 4.5 and 5.5 volts for the total duration of the store operation, INCLUDING the execution of the EWDS instruction immediately following the last programming instruction. FAILURE TO EXECUTE THE LAST EWDS INSTRUCTION BEFORE V_{CC} DROPS BELOW 4.5 VOLTS MAY CAUSE INADVERTENT DATA DISTURB DURING SUBSEQUENT POWER DOWN AND/OR POWER UP TRANSIENTS.

AN-328
EEPROM Application Note
Vpp Generation on Board

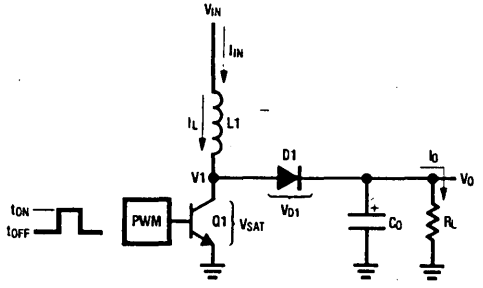
National Semiconducter
Application Note 328
Massood Alavi, Sr. Apps Mgr
February 1983

The NMC2816 requires a 21V pulse for writing and erasing. The rise time on the pulse going from 5–21V is to be 600μs ideally. The NMC 9716 requires a stable 21V. This application note discusses two methods of generating the required Vpp voltage or the high level pulse from a 5V supply.

The first method shows how to generate 21V from a single 5V supply using an LM3524 switching voltage regulator, a power inductor and a number of capacitors as the main active elements. The principle involved is explained by the circuit of Figure 1.

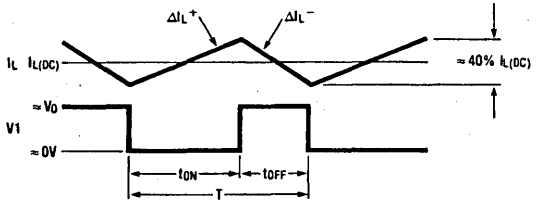
THE STEP-UP SWITCHING REGULATOR

Figure 1 shows the basic circuit for a step-up switching regulator. In this circuit Q1 is used as a switch to alternately apply V_{IN} across inductor L1. During the time, t_{ON}. Q1 is ON and energy is drawn from V_{IN} and stored in L1:D1 is reverse biased and I_o is supplied from the charge stored in C_o. When Q1 opens during t_{OFF}, voltage V1 will rise positively to the point where D1 turns ON. The output current is now supplied through L1,D1 to the load and any charge lost from C_o during t_{ON} is replenished. Here the current through L1 has a DC component plus some ΔI_L. ΔI_L is selected to be approximately 40% of I_L. Figure 2 shows the inductor's current in relation to Q1's ON and OFF times.



TL/D/5152-1

FIGURE 1. Basic Step-Up Switching Regulator



TL/D/5152-2

FIGURE 2. Voltage and Current Waveforms at V1

The following equations are derived to give the reader a theoretical understanding of the operation.

From $\Delta I_L = \frac{V_L T}{L}$, $\Delta I_{L^+} \cong \frac{V_{IN} t_{ON}}{L1}$

and $\Delta I_{L^-} \cong \frac{(V_O - V_{IN}) t_{OFF}}{L1}$

Since $\Delta I_{L^+} = \Delta I_{L^-}$, $V_{IN} t_{ON} = V_O t_{OFF} - V_{IN} t_{OFF}$,

and neglecting V_{SAT} and V_{D1}

$$\boxed{V_O \cong V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)} \quad 1.$$

The above equation shows the relationship between V_{IN}, V_O and duty cycle.

In calculating input current $I_{IN(DC)}$, which equals the inductor's DC current, assume first 100% efficiency:

$P_{IN} = I_{IN(DC)} V_{IN}$

$P_{OUT} = I_O V_O = I_O\ V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$

for $\eta = 100\%$, $P_{OUT} = P_{IN}$

$I_O\ V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right) = I_{IN(DC)}\ V_{IN}$

$I_{IN(DC)} = I_O\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$

This equation shows that the input, or inductor, current is larger than the output current by the factor $(1 + t_{ON}/t_{OFF})$. Since this factor is the same as the relation between V_O and V_{IN}, $I_{IN(DC)}$ can also be expressed as:

$$\boxed{I_{IN(DC)} = I_O\left(\frac{V_O}{V_{IN}}\right)} \quad 2.$$

So far it is assumed $\eta = 100\%$, where the actual efficiency or η_{MAX} will be somewhat less due to the saturation voltage of Q1 and forward on voltage of D1. The internal power loss due to these voltages is the average I_L current flowing, or I_{IN}, through either V_{SAT} or V_{D1}. For $V_{SAT} = V_{D1} = 1V$ this power loss becomes $I_{IN(DC)}$ (1V). η_{MAX} is then:

$$\eta_{MAX} = \frac{P_O}{P_{IN}} = \frac{V_O I_O}{V_O I_O + I_{IN}(1V)} = \frac{V_O I_O}{V_O I_O + I_O\left(1 + \frac{t_{ON}}{t_{OFF}}\right)}$$

From $V_O = V_{IN}\left(1 + \frac{t_{ON}}{t_{OFF}}\right)$,

$$\boxed{\eta_{max} = \frac{V_{IN}}{V_{IN} + 1}} \quad 3.$$

This equation assumes only DC losses, however η_{MAX} is further decreased because of the switching time of Q1 and D1.

In calculating the output capacitor C_O it can be seen that C_O supplies I_O during t_{ON}. The voltage change on C_O during this time will be some $\Delta V_C = \Delta V_O$ or the output ripple of the regulator. Calculation of C_O is:

$\Delta V_O = \frac{I_O t_{ON}}{C_O}$ or $C_O = \frac{I_O t_{ON}}{\Delta V_O}$

From $V_O = V_{IN}\left(\frac{T}{t_{OFF}}\right)$; $t_{OFF} = \frac{V_{IN}}{V_O} T$

where $T = t_{ON} + t_{OFF} = \frac{1}{f}$

$t_{ON} = T - \frac{V_{IN}}{V_O} T = T\left(\frac{V_O - V_{IN}}{V_O}\right)$ therefore:

$$C_O = \frac{I_O T\left(\frac{V_O - V_{IN}}{V_O}\right)}{\Delta V_O} = \boxed{\frac{I_O(V_O - V_{IN})}{f \Delta V_O V_O}} \quad 4.$$

where: C_O is in farads, f is the switching frequency,
ΔV_O is the p-p output ripple

Calculation of inductor L1 is as follows:

$L1 = \frac{V_{IN} t_{ON}}{\Delta I_{L^+}}$, since during t_{ON},

V_{IN} is applied across L1

$\Delta I_{Lp.p} = 0.4 I_L = 0.4 I_{IN} = 0.4 I_O\left(\frac{V_O}{V_{IN}}\right)$, therefore:

$L1 = \frac{V_{IN} t_{ON}}{0.4 I_O\left(\frac{V_O}{V_{IN}}\right)}$ and since $t_{ON} = \frac{T(V_O - V_{IN})}{V_O}$

$$\boxed{L1 = \frac{2.5\ V_{IN}^2 (V_O - V_{IN})}{f\ I_O V_O^2}} \quad 5.$$

where: L1 is in henrys, f is the switching frequency in Hz

To apply the above theory, a complete step-up switching regulator is shown in Figure 3. Since V_{IN} is 5V, V_{REF} is tied to V_{IN}. The input voltage is divided by 2 to bias the error amplifier's inverting input. The output voltage is:

$$V_{OUT} = \left(1 + \frac{R2}{R1}\right) \bullet V_{INV} = 2.5\left(1 + \frac{R2}{R1}\right) \quad 6.$$

The network D1, C1 forms a slow start circuit. This holds the output of the error amplifier initially low thus reducing the duty-cycle to a minimum. Without the slow start circuit the inductor may saturate at turn-on because it has to supply high peak currents to charge the output capacitor from OV. It should also be noted that this circuit has no supply rejection. By adding a reference voltage at the non-inverting input to the error amplifier, see Figure 4, the input voltage variations are rejected.

Using equation 1 any desired supply voltage can be generated at V_o by selecting a suitable value for R_2. If R_2 is a pot in the 25K–50K range, it can be used to set V_o from 15V–27.5V. For standard E²PROM and EPROM applications this range is very suitable for Vpp set up. Table 1 shows various values of R_2 for corresponding values of V_o.

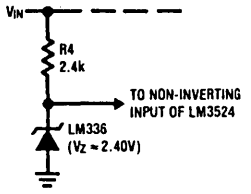


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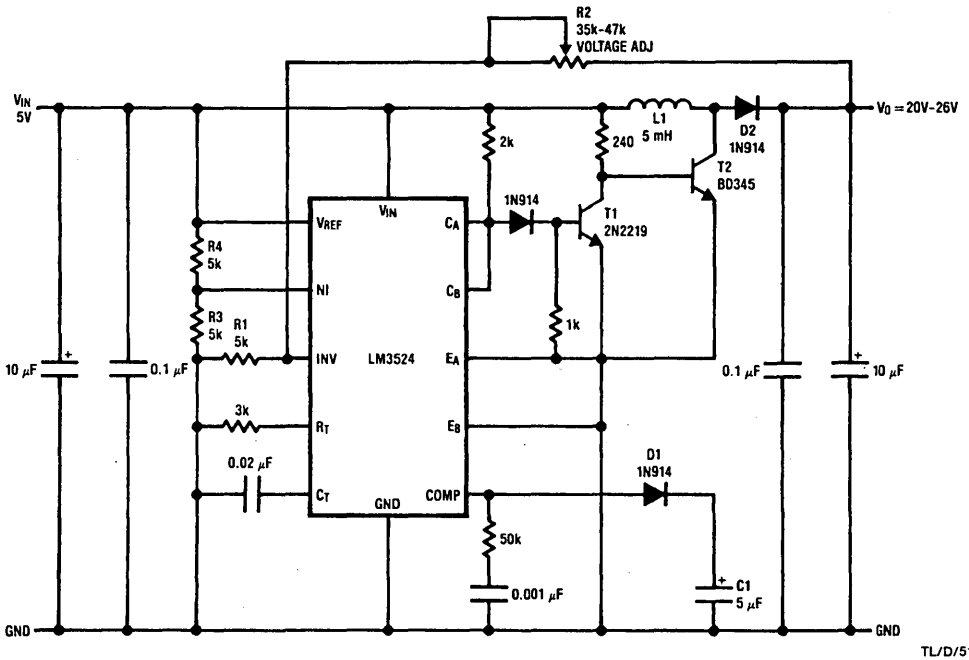
FIGURE 4. Voltage Reference



TL/D/5152–3

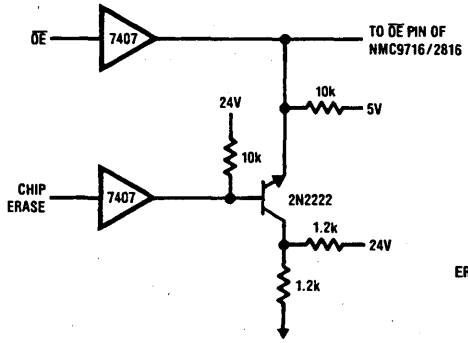
FIGURE 3. A 5V–21V Vpp Voltage Generator Circuit for E²PROM Application

TABLE I

R_2	V_o
47K	26V
45K	25V
43K	24V
41K	23V
39K	22V
37K	21V
35K	20V

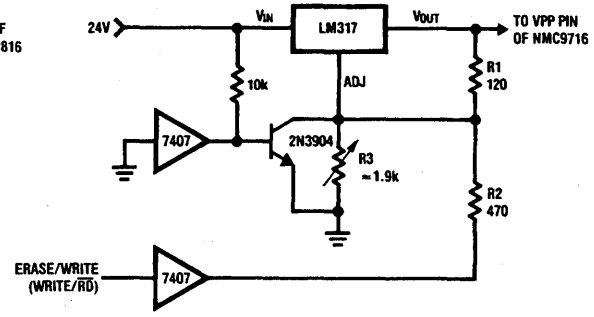
The current sourcing capability of V_o can be made as high as 500mA. If no more than 100mA are desired, T_1 and 240 ohms resistor can be replaced by T_2 alone; the base of T_2 should be connected to the node at base of T_1; T_2 collector and emitter should be left intact. 100mA is sufficient to support up to 20 NMC2816's or NMC9716's.

The Vpp voltage generated by the circuit of Figure 3, can be used to provide the E/W pulses on the NMC2816 or the stable Vpp on NMC9716. The 9V–15V needed for chip erase can also be generated. Figures 5, 6, 7 demonstrate how to achieve that.



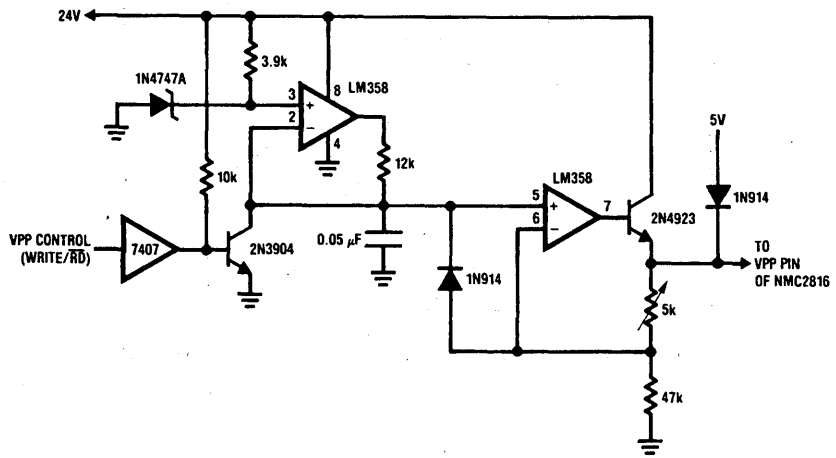
TL/D/5152–5

FIGURE 5. $\overline{OE}$ Chip Erase Control for NMC2816/NMC9716



TL/D/5152–6

FIGURE 6. VPP Switch Design with Electronic Shutdown for $\overline{CE}$ Pulsed Erase/Write for NMC9716



Note 1: 5k is 21V fine adjust.

Note 2: Resistors are ¼W.

TL/D/5152–7

FIGURE 7. Operational Amplifier VPP Switch Design for NMC2816

The following paragraphs outline a second method of generating a 21V pulse from a single 5V supply. Figure 8 shows such a DC-DC converter circuit.

In the circuit, inductor L1 in conjunction with transistors Q1 & Q2 form a self driven 5–30V converter. Transitors Q3 & Q4 are meant to strobe the converter allowing it to draw power and run only when a TTL high is presented at the input node A. Trace A, Figure 9 shows the signal to be applied at the input node. This makes the Q3-Q4 transistor pair conduct biasing Q1 & Q2. Trace B, Figure 9 shows the resultant waveform generated at node B, the collector of Q2. As the converter runs, its output at node C rises to the desired high voltage of 30V quickly. The output is lightly filtered by the .1F capacitor. Trace C, Figure 9 shows this waveform.

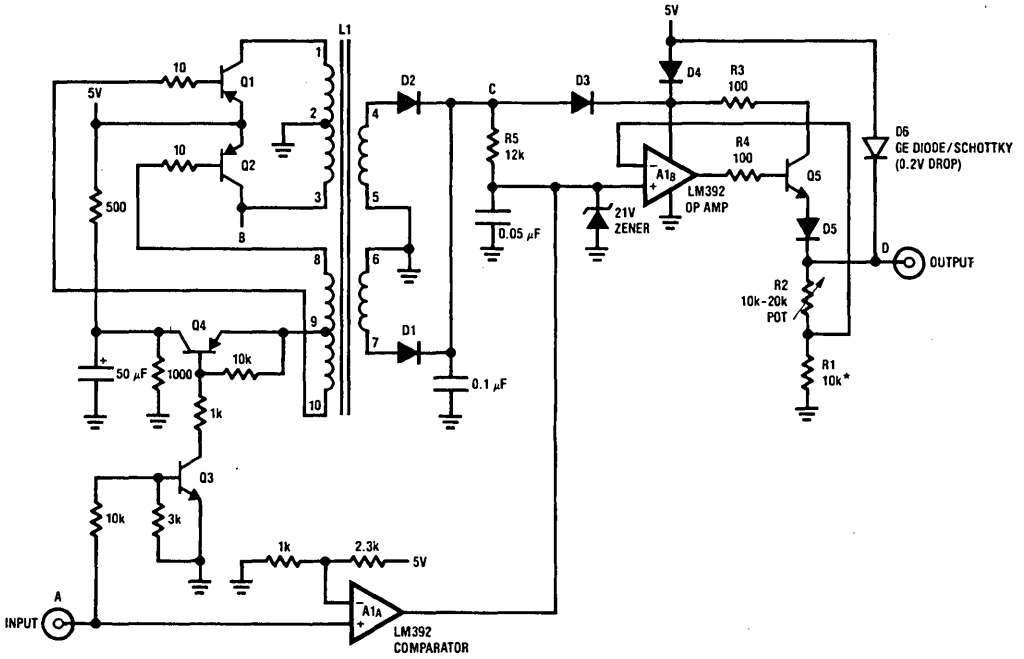
The voltage at node C is used to charge the 12k, .05μF combination at the desired RC of 600μS. This signal cut off at 21V by the Zener at the input to A1B is presented to the amplifier A1B to be outputted to node D as the desired V_{PP}. The amplitude and pulse shape is controlled by setting the cut-off Zener voltage in conjunction with the gain of A1B set by R2. For example, if 7V Zener voltage is used for cut off a gain of 3 will have to be set for A1B to get a 21V output pulse.

When the capacitor reaches the Zener cut off, the Zener clamps, charging ceases and the circuit output sits at 21V.

When the signal at node A goes to TTL low, the open collector output of comparator A1A clamps low, discharging the .05 capacitor and getting the circuit ready for the next pulse. Any EEPROM programming requirement can be met by varying the gain of A1B, the time constant at its input and/or the Zener value across the capacitor. Any TTL detect value can be set by the voltage-divider on the A1A comparator in this case set at about 1.5V.

Transistor Q5 is provided to source boosted output current. Diode D6 is provided to hold the output or V_{PP} as close to Vcc as possible when 21V is not desired. A Ge or Schottky diode must be used to optimize the diode forward drop at $\leq$.2V. D5 is provided to maximize the reverse breakdown from node D to base of Q5, when 21 volts is at node D.

Figure 9 shows the idealized signals generated at various nodes. When the input at node A is at TTL low level, the output D sits at 4.8V. As the input A goes to a TTL high level the output D rises to 21V at RC of 600μS. The waveform at node A may be derived from the $\overline{CE}$ by inverting the $\overline{CE}$ signal. The resulting waveform at node D is used for V_{PP}.



TL/D/5152–8

FIGURE 8. V_{PP} Pulse Generator Circuit

References:

Circuit of Figure 3 is derived from NSC voltage regulator application.

Circuit of Figure 9 is from Electronic design, October 15, 1981.

"Design DC-DC converters to catch noise at source" — J Williams.

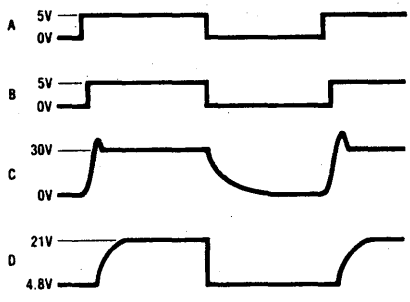


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FIGURE 9. Idealized Signals at Various Nodes

Designing with the NMC9306/COP494 a Versatile Simple to Use E^2 PROM

National Semiconductor
Application Note 338
Masood Alavi
June 1983

This application note outlines various methods of interfacing an NMC9306/COP494 with the COPS™ family of microcontrollers and other microprocessors. *Figures 1-6* show pin connections involved in such interfaces. *Figure 7* shows how parallel data can be converted into a serial format to be inputted to the NMC9306; as well as how serial data outputted from an NMC9306 can be converted to a parallel-format.

The second part of the application note summarizes the key points covering the critical electrical specifications to be kept in mind when using the NMC9306/COP494.

The third part of the application note shows a list of various applications that can use a NMC9306/COP494.

GENERIC CONSIDERATIONS

A typical application should meet the following generic criteria:

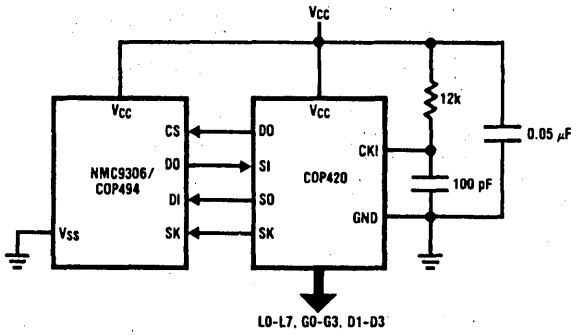
1. allow for no more than 10,000 E/W cycles for optimum and reliable performance.
2. allow for any number of read cycles.
3. allow for an erase or write cycle that operates in the 10–30 ms range, and not in the tens or hundreds of ns range as used in writing RAMs. (Read vs write speeds are distinctly different by orders of magnitude in E^2PROM, not so in RAMs.
4. no battery back-up required for data-retention, which is fully non-volatile for at least 10 years at room-ambient.

SYSTEM CONSIDERATIONS

When the control processor is turned on and off, power supply transitions between ground and operating voltage may cause undesired pulses to occur on data, address and control lines. By using WEEN and WEDS instructions in conjunction with a LO-HI transition on CS, accidental erasing or writing into the memory is prevented.

The duty cycle in conjunction with the maximum frequency translates into having a minimum Hi-time on the SK clock. If the minimum SK clock high time is greater than 1 μs, the duty cycle is not a critical factor as long as the frequency does not exceed the 250 kHz max. On the low side no limit exists on the minimum frequency. This makes it superior to the COP499 CMOS-RAM. The rise and fall times on the SK clock can also be slow enough not to require termination up to reasonable cable-lengths.

Since the device operates off of a simple 5V supply, the signal levels on the inputs are non-critical and may be operated anywhere within the specified input range.



TL/D/5286–1

FIGURE 1. NMC9306/COP494 — COP420 Interface

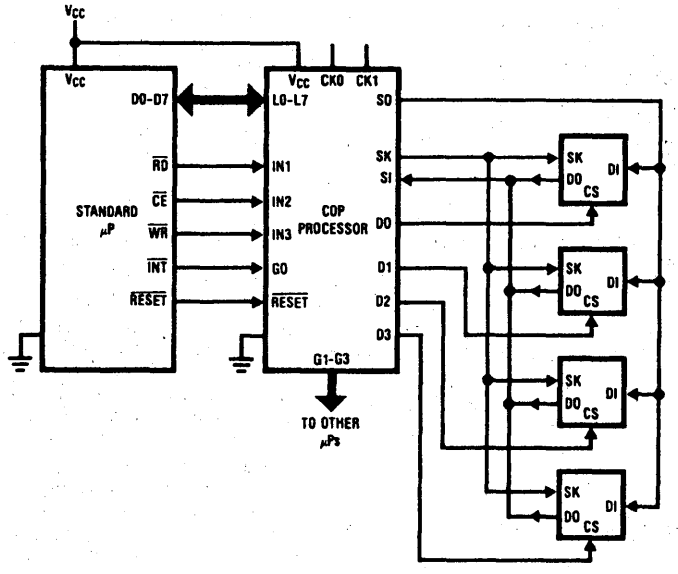
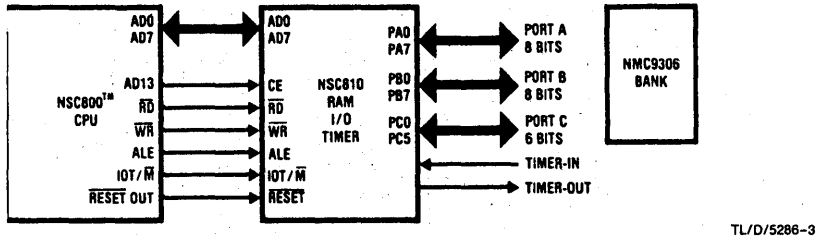


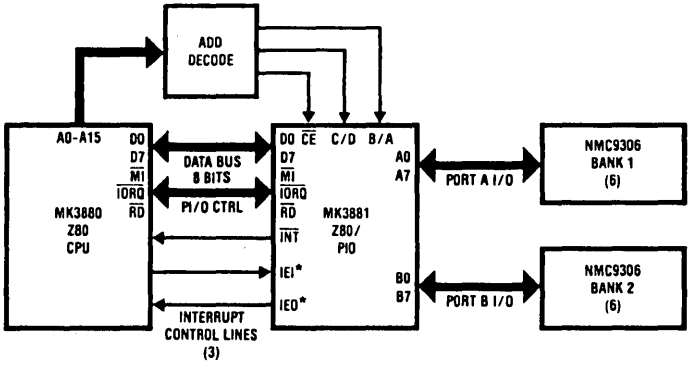
FIGURE 2. NMC93O6 — Standard μP Interface Via COP Processor



PA0 → SK
PA1 → DI/DO } Common to all 9306's
PA2–7 → 6CS for 6– 9306's

* SK is generated on port pins by bit-set and bit-clear operations in software. A symmetrical duty cycle is not critical.
* CS is set in software. To generate 10–30 ms write/erase the timer/counter is used. During write/erase, SK may be turned off.

FIGURE 3. NSC800™ to NMC9306 Interface (also Valid for 8085/8085A and 8156)

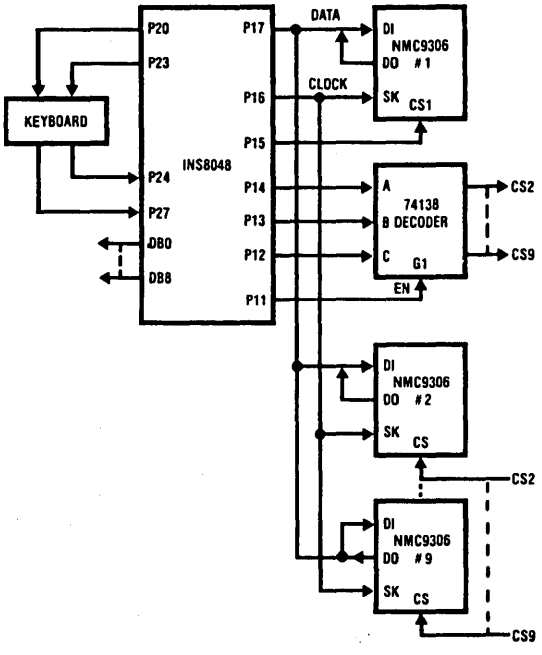


TL/D/5286–4

Z80-P10	9306	
A0	SK	Common to all 9306's (Bank 1)
A1	DI/DO	
A2-A7	CS1-CS6	

* Only used if priority interrupt daisy chain is desired
* Identical connection for Port B

FIGURE 4. Z80 — NMC9306 Interface Using Z80-PIO Chip



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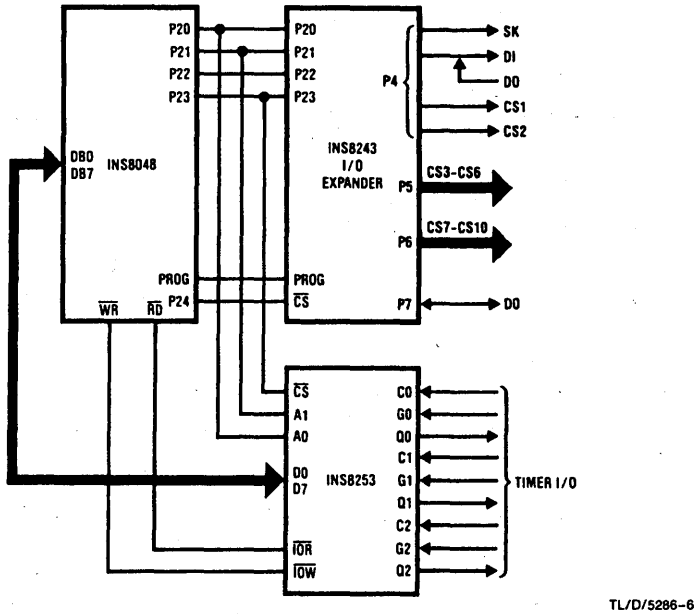
* SK and DI are generated by software. It should be noted that at 2.72 μs/instruction. The minimum SK period achievable will be 10.88 μs or 92 kHz, well within the NMC9306 frequency range.
* DO may be brought out on a separate port pin if desired.

FIGURE 5. 48 Series μP — NMC9306 Interface



Expander outputs

	DI SK	(COMMON)
Port 4	CS1	
	CS2	
Port 5-6	CS3–CS10	
Port 7	DO (COMMON)	

FIGURE 6. 8048 I/O Expansion

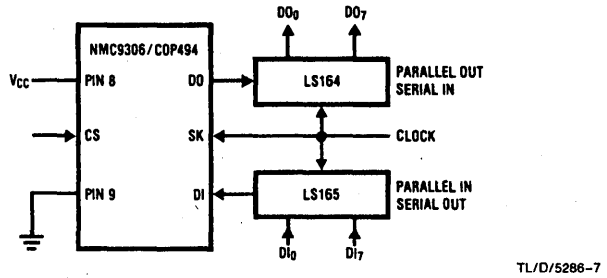
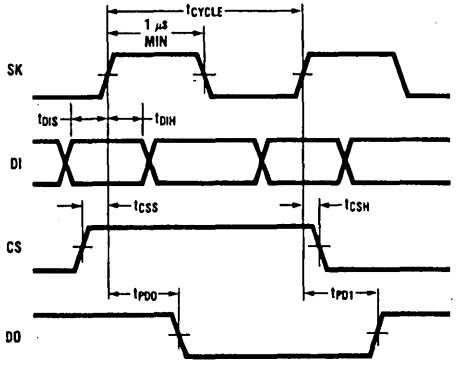


FIGURE 7. Converting Parallel Data into Serial Input for NMC9306/COP494



Min	Max
t_{CYCLE} 0	250 kHz
DUTY CYCLE 25%	75%
t_{DIS} 400	ns
t_{D1H} 400	ns
t_{CSS} 200	ns
t_{CSH} 0	ns
t_{PD0}	2 μs
t_{PD1}	2 μs

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FIGURE 8. NMC9306/COP494 Timing

THE NMC9306/COP494

Extremely simple to interface with any μP or hardware logic. The device has six pins for the following functions:

Pin 1	CS*	HI enabled
Pin 2	SK	Clock input for data bit maneuvering
Pin 3	DI	For instruction or data input
Pin 4	DO**	For data read TRI-STATE® otherwise
Pin 5	GND	
Pin 8	V_{CC}	For 5V power
Pins 6–7	No Connect	No termination required

* Following an E/W instruction feed, CS is also toggled low for 10 ms (typical) for an E/W operation. This internally turns the VPP generator on (HI-LO on CS) and off (LO-HI on CS).

** DI and DO can be on a common line since DO is TRI-STATED when unselected DO is only on in the read mode.

USING THE NMC9306/COP494

The following points are worth noting:

1. SK clock frequency should be in the 0–250 kHz range. With most μPs in the 1–11 MHz range this is easily achieved when implemented in software by bit-set and bit-clear instructions, which take 4 instructions to execute a clock or a frequency in the 100 kHz range for standard μP speeds. Symmetrical duty cycle is irrelevant if SK HI time is ≥ 2 μs.
2. CS low period following an E/W instruction must not exceed the 30 ms max. It should best be set at typical or minimum spec of 10 ms. This is easily done by timer or a software connect. The reason is that it minimizes the 'on time' for the high V_{PP} internal voltage, and so maximizes endurance. SK-clock during this period may be turned off if desired.
3. All E/W instructions must be preceded by EWEN and should be followed by an EWDS. This is to secure the stored data and avoid inadvertent erase or write.
4. A continuously 'on' SK clock does not hurt the stored data. Proper sequencing of instructions and data on DI is essential to proper operation.
5. Stored data is fully non-volatile for up to ten years independent of V_{CC}, which may be on or off. For all practical purposes any number of read cycles have no adverse effects on data retention.
6. Up to 10,000 E/W cycles/register are possible. Under typical conditions, this number may actually approach 1 million. For applications requiring a large number of cycles, redundant use of internal registers beyond 10,000 cycles is recommended.
7. Data shows a fairly constant E/W Programming behavior over temperature. In this sense E^2PROMs supersede EPROMs which are restricted to room temperature programming.
8. As shown in the timing diagrams, the start bit on DI must be set by a ZERO - ONE transition following a CS enable (ZERO - ONE), when executing any instruction. ONE CS enable transition can only execute ONE instruction.
9. In the read mode, following an instruction and data train, the DI can be a don't care, while the data is being outputted i.e., for next 17 bits or clocks. The same is true for other instructions after the instruction and data has been fed in.
10. The data-out train starts with a dummy bit 0 and is terminated by chip deselect. Any extra SK cycle after 16 bits is not essential. If CS is held on after all 16 of the data bits have been outputted, the DO will output the state of DI till another CS LO-HI transition starts a new instruction cycle.
11. When a common line is used for DI and DO, a probable overlap occurs between the last bit on DI and start bit on DO.
12. After a read cycle, the CS must be brought low for 1 SK clock cycle before another instruction cycle can start.

INSTRUCTION SET

Commands	Opcode	Comments
READ	10000A3A2A1A0	Read Register 0–15
WRITE	11000A3A2A1A0	Write Register 0–15
ERASE	10100A3A2A1A0	Erase Register 0–15
EWEN	111000 0 0 1	Write/Erase Enable
ENDS	111000 0 1 0	Write/Erase Disable
***WRAL	111000 1 0 0	Write All Registers
ERAL	111000 1 0 1	Erase All Registers

All commands, data in, and data out are shifted in/out on rising edge of SK clock.

Write/erase is then done by pulsing CS low for 10 ms.

All instructions are initiated by a LO-HI transition on CS followed by a LO-HI transition on DI.

READ — After read command is shifted in DI becomes don't care and data can be read out on data out, starting with dummy bit zero.

WRITE — Write command shifted in followed by data in (16 bits) then CS pulsed low for 10 ms minimum.

ERASE
ERASE ALL — Command shifted in followed by
WRITE ALL — Pulsing CS low for 10 ms.
WRITE
ENABLE/DISABLE — Command shifted in.

*** (This Instruction is not speced on Data sheet.)

The following is a list of various systems that could use a NMC9306/COP494

A. Airline terminal
Alarm system
Analog switch network
Auto calibration system
Automobile odometer
Auto engine control
Avionics fire control

B. Bathroom scale
Blood analyzer
Bus interface

C. Cable T.V. tuner
CAD graphics
Calibration device
Calculator—user programmable
Camera system
Code identifier
Communications controller
Computer terminal
Control panel
Crystal oscillator

D. Data acquisition system
Data terminal

E. Electronic circuit breaker
Electronic DIP switch
Electronic potentiometer
Emissions analyzer
Encryption system
Energy management system

F. Flow computer
Frequency synthesizer
Fuel computer

G. Gas analyzer
Gasoline pump

H. Home energy management
Hotel lock

I. Industrial control
Instrumentation

J. Joulemeter

K. Keyboard -softkey

L. Laser machine tool

M. Machine control
Machine process control
Medical imaging
Memory bank selection
Message center control
Mobile telephone
Modem
Motion picture projector

N. Navigation receiver
Network system
Number comparison

O. Oilfield equipment

P. PABX
Patient monitoring
Plasma display driver
Postal scale
Process control
Programmable communications
Protocol converter

Q. Quiescent current meter

R. Radio tuner
Radar dectector
Refinery controller
Repeater
Repertory dialer

S. Secure communications system
Self diagnostic test equipment
Sona-Bouy
Spectral scanner
Spectrum analyzer

T. Telecommunications switching system
Teleconferencing system
Telephone dialing system
T.V. tuner
Terminal
Test equipment
Test system
TouchTone dialers
Traffic signal controller

U. Ultrasound diagnostics
Utility telemetering

V. Video games
Video tape system
Voice/data phone switch

W. Winchester disk controller

X. X-ray machine
Xenon lamp system

Y. YAG—laser controller

Z. Zone/perimeter alarm system

Designing with the NMC9817, a 2nd Generation E²PROM

National Semiconductor
Application Note 342
Masood Alavi
November 1983

The NMC9817 offers the non volatile memory designer the following features:

- 16K bits of non-volatile storage organized as 2K × 8
- fully 5V only operation in all modes
- address, data and $\overline{WE}$ latches, upward and downward compatible with E²'s, EPROMs, ROMs and SRAMs
- fast read access times
- direct microprocessor interfacing capability
- 10,000 write cycles per byte open-drain ready/$\overline{busy}$
- 10 years data retention

The purpose of this application note is to detail the new features and the simple interface considerations inherent to using the NMC9817.

The JEDEC 28 pin universal memory pin-out has been selected for the NMC9817. *Figure 1* shows this pin-out and how it relates to other memory types.

This philosophy allows for interchanging memory types and to provide the required densities. E²PROMs can be mixed with PROMs, ROMs, RAMs or EPROMs. Upward or downward compatibility is possible in density selection, providing great flexibility in system design requirements, even as they change through the course. New features or upgrades can be added with minimal hardware modifications. With the 28 pin selected pin-out of the NMC9817, E²PROM devices from 4k to 128k will fit perfectly without external interface requirements. The pin-out also allows inserting 24 pin E²PROM devices because of common data, address and control pins.

Figure 2 shows a block diagram of the NMC9817.

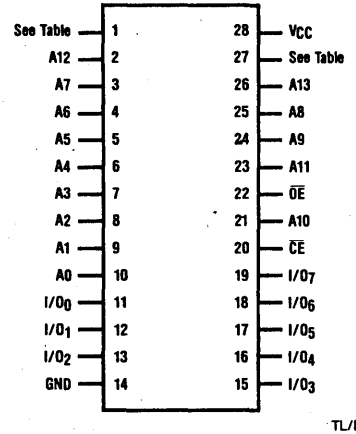
The basic constraints on 1st generation E²PROMs have been quite cumbersome. 10,000 erase/write cycles/byte, 10 ms or more erase/write times, external 21V generation, lack of on-chip buffers and latches have been the important generic considerations. Many support components have been essential to incorporate these requirements.

External programming voltage entailed either a DC-DC converter or a step down voltage regulator (See AN-328). In addition, support circuitry for sequencing write cycles was necessary because 10ms erase/write time is a much longer period than a typical microprocessor cycle. This required external data and address latches and a counter to time out the erase/write periods. Analog pulse-shaping circuitry for erase/write pulses is also an external interface requirement.

Figure 2 shows how all the above interface requirements are integrated on the NMC9817. This allows for a direct interface with any microprocessor capable of providing the required control signals. Even the generic constraint of 10ms write time has been efficiently designed around. To initiate a RAM like write cycle the microprocessor signals with a 100 ns $\overline{WE}$ pulse after $\overline{CE}$ is valid. Only one instruction is required to do so after which the intelligence in the NMC9817 takes care of the rest allowing the microprocessor to execute other instructions while the E²PROM writes the byte. This is so because the NMC9817 contains all the necessary data in on-chip latches. A ready/$\overline{busy}$ output is provided on pin 1 which goes to logic low when the part goes into a write cycle and logic high when the write is done.

Not only can this pin be used to signal an interrupt to the microprocessor to put the E²PROM on or off line, it also serves to optimize the best possible write time that a part has. In other words, if the NMC9817 gets programmed in less than 10 ms, the ready/$\overline{busy}$ line output will allow the microprocessor to take advantage of this. This is implemented by a method referred to as multiple-hits of write pulses. Refer to *Figure 3.*

SRAM	NOVRAM	ROM	EPROM	E²PROM	
8K ↓ 256K	4K ↓ 128K	8K ↓ 256K	8K ↓ 256K	4K ↓ 128K	
A14	$\overline{NE}$	NC	V_{PP}	RDY/$\overline{BUSY}$	Pin 1
$\overline{WE}$	$\overline{WE}$	A14	PGM/A14	$\overline{WE}$	Pin 27



TL/D/5477–1

FIGURE 1. Universal 28-Pin-out

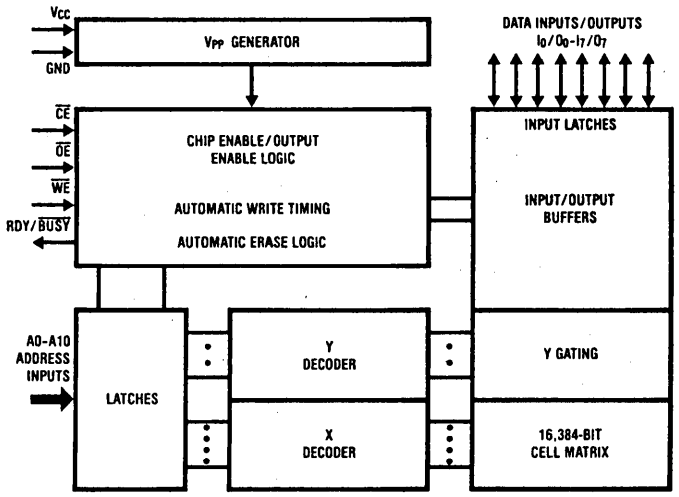


FIGURE 2. Functional Block Diagram

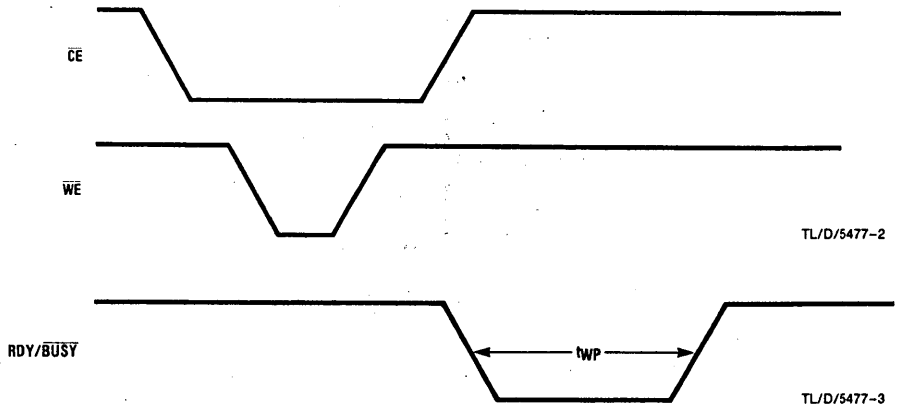


FIGURE 3. Write Waveforms

As soon as the write pulse is detected by the device, the following sequence of events commences:

- Ready/busy goes low and puts the device off the microprocessor bus.
- A read before write is internally initiated to determine whether or not an Erase before write is required.
- If any zero is detected in the byte during the read a 5 ms max Erase cycle is initiated during which internal V_{PP} is raised to 21V. Following the Erase, a 5 ms max write cycle is executed.
- If all ones are detected in the byte during the read, the Erase before write cycle is skipped and a 5 ms max write cycle is executed.
- Once write is verified and completed, the ready/busy is raised to interrupt the microprocessor.

The above sequence allows for achieving fast write times without compromising data retention or data integrity.

For convenience in system design, full 5V operation is designed in the NMC9817. This has been done by incorporating on chip a 5-21V charge pump, a 21 volt regulator and-power up/down sequencer to avoid inadvertent spurious writes. Regulation of the 21V internal supply is an important consideration, more so over temperature since it is directly related to endurance. Voltage spikes can cause early damage to the integrity of the tunnel-oxides.

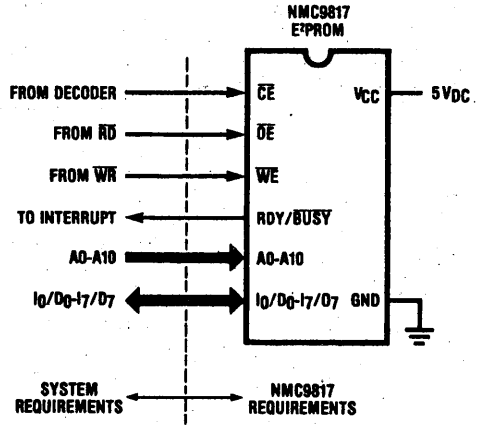
Interface Requirements

Figure 4 shows the simple interface requirements in using the NMC9817. Besides the direct bus connections to the microprocessor, three or four (if ready/$\overline{busy}$ is used) connections are required viz $\overline{CE}$ to decoder, $\overline{OE}$ to $\overline{RD}$, $\overline{WE}$ to $\overline{WR}$ and ready/$\overline{busy}$ to an interrupt. Ready/$\overline{busy}$ may be multiplexed for hardware handling. It can also be OR-tied if desired since it is an open-drain output; the slowest device will control the write time in such a case.

Figure 5 shows a typical large system application with multiplexed ready/$\overline{busy}$.

In summary, the NMC9817 has been designed as a monolithic solution to the problems that arose with the 1st generation of E²PROMs. It attempts to establish a standard for future E²PROMs, both from an electrical parametric viewpoint and ease-of-use system design considerations. It solves the following problems that confronted the 1st generation E²PROMs:

1. A 21V external power supply.
2. A rise time restricted 10 ms wide minimum pulse for erase/write.
3. Lack of on-chip address and data latches.
4. Absence of an interrupt ready/busy output.
5. Non integrated erase before write.
6. Non-upgradable package.



TL/D/5477–4

FIGURE 4. Simple NMC9817 Interface Requirements

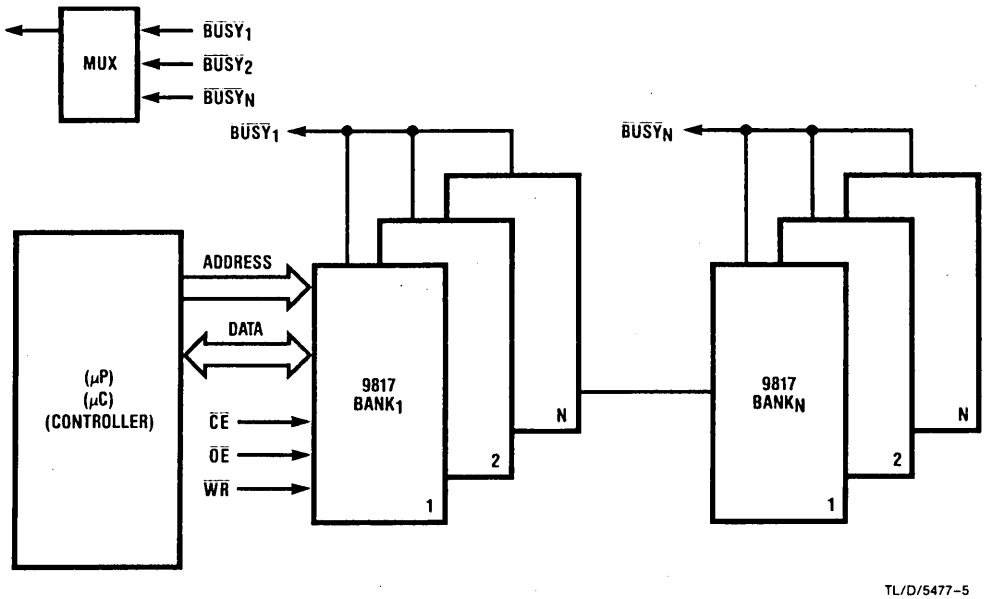


FIGURE 5. A Typical NMC9817 System

Section 8

Military/Aerospace

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Section Contents

Detailed Electrical Test and Burn-in information on the following MIL-STD-883, Class B tested memory devices may be found in Volume 2 of *The Reliability Handbook*. Screening is described in the brochure "883B/RETS™ Products from National Semiconductor," which follows.

MM2102AJ-L/883B	1024-bit (1024 × 1) static RAM (NMOS)
MM2102AJ-4/883B	1024-bit (1024 × 1) static RAM (NMOS)
MM2114MJ-3/883B	4096-bit (1024 × 4) static RAM (NMOS)
MM2716QM/883B	16,384-bit (2K × 8) UV erasable PROM (NMOS)
MM5290F-3/883B	16,384-bit (16K × 1) dynamic RAM (NMOS)
MM5290J-3/883B	16,384-bit (16K × 1) dynamic RAM (NMOS)
NMC2147HF-3/883B	4096-bit (4K × 1) static RAM (NMOS)
NMC2147HJ-3/883B	4096-bit (4K × 1) static RAM (NMOS)
NMC2147HJ/883B	4096-bit (4K × 1) static RAM (NMOS)
NMC27C16Q45/883B	16,384-bit (2K × 8) UV erasable PROM (CMOS)
NMC27C16Q55/883B	16,384-bit (2K × 8) UV erasable PROM (CMOS)
NMC27C16Q65/883B	16,384-bit (2K × 8) UV erasable PROM (CMOS)
NMC27C32Q45/883B	32,768-bit (4K × 8) UV erasable PROM (CMOS)
NMC27C32Q55/883B	32,768-bit (4K × 8) UV erasable PROM (CMOS)
NMC27C32Q65/883B	32,768-bit (4K × 8) UV erasable PROM (CMOS)
NMC2816ME-25/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC2816ME-35/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC2816ME-45/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC2816MJ-25/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC2816MJ-35/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC2816MJ-45/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC9716E-25/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC9716E-35/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC9716E-45/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC9716J-25/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC9716J-35/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC9716J-45/883B	16,384-bit (2K × 8) electrically erasable PROM (NMOS)
NMC9306J/883B	256-bit serial electrically erasable PROM (NMOS)
NMH2864D/MP	65,536-bit (8K × 8) E^2PROM module
NMH9764D/MP	65,536-bit (8K × 8) E^2PROM module

FUTURE MIL/AERO MEMORY PRODUCTS

As the following products become available, they will be submitted to our MIL-STD-883, Class B qualification program and will be offered as MIL-STD-883 Class B devices:

NMC27C64	65,536-bit (8K × 8) UV erasable PROM (CMOS)
NMC27C256	262,144-bit (32K × 8) UV erasable PROM (CMOS)
NMC3764	65,536-bit (64K × 1) dynamic RAM (NMOS)
NMC6164	65,536-bit (8K × 8) static RAM (CMOS with NMOS cells)
NMC9346	1024-bit (64 × 16) serial electrically erasable PROM (NMOS)
NMC9817	16,384-bit (2K × 8) electrically erasable PROM with 5V programming (NMOS)
NMC98C64	65,536-bit (8K × 8) electrically erasable PROM with 5V programming (NMOS)

National
Semiconductor

883B/RETS™ Products

from National Semiconductor

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National Semiconductor

883B/RETS™ Integrated Circuits From National

1.0 SCOPE

1.1 PURPOSE

This document establishes the requirements for screening, processing, qualification, and quality conformance testing of monolithic integrated circuits in accordance with Class B of MIL-STD-883.

1.2 INTENT

The program defined herein is intended to provide standardized, off-the-shelf integrated circuits manufactured and tested in full compliance with MIL-STD-883.

2.0 APPLICABLE DOCUMENTS

The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein. National Semiconductor reserves the right to change any or all of the requirements stated herein in order to update those requirements in accordance with changes in the applicable military specifications.

2.1 SPECIFICATIONS

MIL-M-38510 General Specification for Microcircuits
MIL-M-55565 Microcircuits, Packaging of
MIL-Q-9858 Quality System Requirements
MIL-C-45662 Calibration System Requirements

2.2 STANDARDS

MIL-STD-105 Sampling Procedures and Tables
MIL-STD-883 Test Methods and Procedures for Microelectronics
MIL-STD-977 Test Methods and Procedures for Line Certification

2.3 HANDBOOKS

MIL-HDBK-217 Reliability Prediction of Electronic Equipment
MIL-HDBK-263 Electrostatic Discharge Control Handbook

2.4 DETAIL SPECIFICATIONS

The applicable detail specification for a particular 883B/RETS microcircuit is the National Semiconductor RETS (Reliability Electrical Test Specification, see *Figure 1*) for that device. The RETS is a detailed listing of the parameters, test conditions, test limits, and applicable test temperatures which apply to electrical screening, Group A Quality Conformance Inspection, and electrical end points for other Quality Conformance Inspections. In addition, the RETS provides information relative to certain electrical characteristics which are of interest to the designer but are not directly measured.

2.5 ORDER OF PRECEDENCE

In the event of a conflict between this document and any of the references cited herein, the precedence in which requirements shall govern, in descending order, is as follows:

1. The applicable detail specification;
2. This document;
3. MIL-STD-883;
4. MIL-M-38510;
5. Other documents listed in 2.1 through 2.3;

except that all differences between processing done herein and that specified in MIL-STD-883 must be clearly noted either in this document or in the applicable detail specification (as applicable).

3.0 GENERAL REQUIREMENTS

Only integrated circuits which have met the screening, quality conformance and qualification procedures defined herein shall be shipped as 883B/RETS products.

3.1 TERMS, DEFINITIONS, AND SYMBOLS

All terms, definitions, and symbols shall be as specified in MIL-M-38510, except that the qualifying activity shall be National Semiconductor Corporation.

3.2 QUALIFICATION

Integrated circuits furnished under this document shall be products which have passed the qualification testing defined in Paragraph 6.0 herein.

3.3 LINE CERTIFICATION

Integrated circuits furnished under this document shall be produced exclusively on those lines certified by the National Quality Assurance Department for the manufacture and test of Military/Aerospace products. The MIL-M-38510 requirement that all devices be manufactured, assembled, and tested within the U.S. shall not apply.

3.4 SCREENING

Integrated Circuits furnished under this document shall have been subjected to and shall have passed all of the screening indicated in Paragraph 4.0 herein.

3.5 QUALITY CONFORMANCE INSPECTION

Integrated circuits furnished under this document shall come from lots which have been subjected to and have passed the Quality Conformance Inspection requirements defined in Paragraph 5.0 herein. The frequency of Quality Conformance Inspection shall be as defined in MIL-STD-883 and MIL-M-38510.

3.6 TRACEABILITY

Lot traceability shall be maintained in accordance with MIL-M-38510.

NOTES	RETS7835X REVISION 8C		TEST CONDITIONS (UNLESS OTHERWISE SPECIFIED) VCC		TEST #	TEST SYSTEM: TERADYNE J283 DC PARAMETERS SUBGRP 1 NOTE 6 25°C min	SUBGRP 1 NOTE 6 25°C max	SUBGRP 2 NOTE 6 +125°C min	SUBGRP 2 NOTE 6 +125°C max	SUBGRP 3 -55°C min	SUBGRP 3 -55°C max	OPTION DRIFT LIMITS (25°C)	UNITS
	Logical "1" Output Voltage	VOH	4.5V	IOH = -2mA, VB = VDR = 0, VD = VDD = 4V (Rcvr)	23,24	2.4		2.4		2.4			V
			4.5V	IBUS = -5.2mA, VD = .8V, VX = 0, VDR = 4V, VDD = 0 (Driver)	61,62, 65,66	2.4		2.4		2.4			V
	Logical "0" Output Voltage	VOL	4.5V	IOL = 16mA, VB = VDD = 4V, VDR = 0 (Rcvr)	22,25		.4		.4		.4		V
			4.5V	IBUS = 50mA, VD = 2V, VX = 0, VDR = 4V, VDD = 0	60,63, 64,67		.5		.5		.5		V
			4.5V	IOL = 2mA, VDD = .8V, VDR = 0, VD = 4V (Driver)	106		.4		.4		.4		V
			4.5V	IOL = 2mA, VDR = .8V, VDD = 4V, VB = 4V, VD = 0 (Rcvr)	105		.4		.4		.4		V
	Maximum Bus Current	IBUS	5.5V	VB = 4V, VD = 0, VDD = VDR = 4V	46,53		80		80		80		uA
			0V	VB = 4V, VD = VDD = VDR = 0	47,52		80		80		80		uA
			5.5V	VB = .4V, VDD = VDR = 4V	130		-40		-40		-40		uA
	Logical "1" Input Current	IIH1	5.5V	VIN = 2.4V, VDD = VDR = 0 (Driver)	71,76		40		40		40		uA
			5.5V	VIN = 2.4V (Disable)	101		40		40		40		uA
		IIH2	5.5V	VIN = 5.5V, VDD = VDR = 0 (Driver)	72,75		1		1		1		mA
			5.5V	VIN = 5.5V (Disable)	102		1		1		1		mA
	Logical "0" Input Current	IIL	5.5V	VIN = .4V, VDD = VDR = 0 (Driver)	70,77		-1.6		-1.6		-1.6		mA
			5.5V	VIN = .4V (Disable)	100		-1.6		-1.6		-1.6		mA
	Input Clamping Voltage	VIC	5.5V	IIN= -12mA, VDD = VDR = 4V (Bus)	50,51		-1.5		-1.5		-1.5		V
			5.5V	IIN= -12mA, VDD = VDR = 0 (Driver)	73,74		-1.5		-1.5		-1.5		V
			5.5V	IIN= -12mA (Disable)	103		-1.5		-1.5		-1.5		V
	Disabled Output Current	IOZH	4.5V	VDR = 2V, VDD = 4V, VB = 4V, VD = 0, VOUT = 3V (Rcvr)	104		80		80		80		uA
			4.5V	VDD = 2V, VDR = 0, VD = 4V, VOUT = 3V (Driver)	107		80		80		80		uA
			5.5V	VOUT = 2.4V, Disable inputs at 2V (Rcvr)	251		40		40		40		uA
		IOZL	5.5V	VOUT = .4V, Disable inputs at 2V (Rcvr)	250,253		-40		-40		-40		uA
	Short Circuit Current	IOS	5.5V	VOUT = 0, VB = VDR = 0, VD = VDD = 4V (Rcvr)	110,111, 114,115	-28	-70	-28	-70	-28	-70		mA
			5.5V	VOUT = 0, VD = 4V, VDD = VDR = 0 (Driver)	116,117, 122,123	-40	-120	-40	-120	-40	-120		mA

NOTE 6: Power dissipation must be externally controlled at elevated temperatures.

RETS7835X DEVICE: DS7835 FUNCTION: QUAD TRI-STATE BUS TRANSCEIVERS

RR0066
les

FIGURE 1. Sample RETS

3.7 DESIGN AND CONSTRUCTION

Design and Construction shall be in accordance with MIL-M-38510. Where differences exist, they shall be clearly noted in the applicable detail specification. Design documentation shall be maintained on file.

3.8 MARKING OF MICROCIRCUITS

All marking shall be legible, complete, and shall meet the resistance to solvents requirements of MIL-STD-883, Method 2015. If any additional marking is used, it shall not intefere with the marking required herein. The following marking shall be placed on each device:

a. Index point (see 3.8.1)
b. Part number (see 3.8.2)
c. Inspection lot identification code (see 3.8.3)
d. Manufacturer's identification (3.8.4)
e. Electrostatic discharge sensitivity identifier (see 3.8.5)
f. Radiation hardness indicator, where applicable (see 3.8.6)

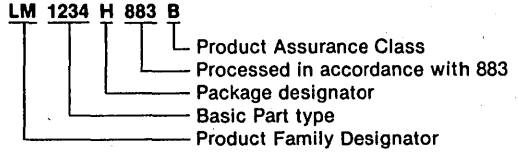
3.8.1 INDEX POINT

An index point, tab, or other marking shall be used to indicate the starting point for the numbering of leads or for mechanical orientation. It shall be so designed as to be visible from above when the microcircuit is installed in its normal mounting configuration. The electrostatic discharge sensitivity indicator (see 3.7.5) may also be used as the pin 1 identifier.

3.8.2 PART NUMBER

Each microcircuit shall be marked with the complete part number. The part number may be marked on more than one line, with "/883B" appearing on the second line. The part number shall be constructed as follows:

LM1234H/883B



3.8.3 INSPECTION LOT IDENTIFICATION CODE

Microcircuits shall be marked with a unique code to indicate the inspection lot from which they were taken. The basis for identification shall be the date of the first week in which devices from that inspection lot were sealed. The format shall be four (or five) digits, with the first two digits indicating the last two digits of the year, the next two digits indicating the week of seal (with a 0 prefix for weeks 1 through 9), and the final digit (where used) an alpha character to indicate the existence of more than one inspection lot bearing the same basic inspection lot code.

3.8.4 MANUFACTURER'S IDENTIFICATION

All devices shall be marked with the National Semiconductor logo, name, or trademark. The manufacturer's designating symbol (27014) need not be marked on the microcircuits.

3.8.5 ELECTROSTATIC DISCHARGE SENSITIVITY INDICATOR

Those microcircuits which are tested in accordance with Method 3015 of MIL-STD-883 and are found to be Category A devices, or those devices which are classified as Category A in lieu of testing, shall be marked with an isosceles triangle. (NOTE: MIL-M-38510 REQUIRES AN EQUILATERAL TRIANGLE.)

3.8.6 RADIATION HARDNESS ASSURANCE INDICATOR

Devices which have been tested in accordance with the radiation testing procedures defined in "Radiation Hardened Technologies from National Semiconductor" shall be marked with a -RX suffix, where the X shall indicate the radiation level to which the devices were tested (5 for $1x10^5$ rads (Si), 6 for $1x10^6$, 7 for $1x10^7$).

3.8.7 MARKING LOCATION AND SEQUENCE

Marking location and sequence shall be in accordance with MIL-M-38510.

3.8.8 MARKING ON CONTAINER

All of the markings indicated in 3.8 (except for the index point) shall be marked upon the microcircuit shipping container. In addition, the manufacturer's designating symbol (27014), the EIA-STD-RS-471 symbol for ESD sensitive devices, and (where applicable) the reinspection date code (see 3.9) shall also be marked on the shipping container.

3.9 PROCEDURE FOR LOTS HELD MORE THAN 36 MONTHS

Microcircuits held by the manufacturer or by authorized distributors for a period exceeding thirty-six (36) months following the date of the inspection lot identification code, shall be reinspected by the manufacturer for all specified Group A inspection requirements. The devices shall retain the original inspection lot identification code, but the date code of reinspection shall be marked on the shipping container and in the certifying documentation. Failure of any subgroup shall require 100% rescreening of the lot for the subgroup and removal from the lot of any device(s) failing the rescreening.

3.10 WORKMANSHIP AND REWORK PROVISIONS

Workmanship and rework provisions shall be in accordance with MIL-M-38510.

4.0 SCREENING

Each microcircuit shall have been subjected and passed all of the screening tests detailed in Method 5004 of MIL-STD-883 (see Table I) in order to be acceptable for delivery. Devices which fail any test criteria in the screening sequence shall be removed from the lot at the time of observation or immediately at the conclusion of the test in which the failure was observed. Once rejected and verified as a test failure, no device may be retested for acceptance.

4.1 ELECTRICAL TEST PARAMETERS

Electrical Test parameters for interim and final electrical testing (see Table I) shall be as defined in the applicable detail specification (RETS). Applicable test temperatures shall be 25°C, 125°C, and −55°C, unless otherwise specified in the applicable detail specification. Interim electrical test parameters are performed at the manufacturer's option.

4.2 PDA

All lots or sublots of microcircuits screened in accordance with this document shall be subject to a PDA (Percent Defective Allowable) for post-burn-in 25°C DC electrical test measurements. Lots failing PDA may be resubmitted to burn-in in accordance with 4.2.1. The applicable PDA shall be 5% for all devices.

4.2.1 LOTS RESUBMITTED FOR BURN-IN

Unless otherwise specified, lots and sublots may be resubmitted for burn-in one time only, provided the observed percent defective for 25°C DC measurements during the first submission does not exceed 20%. Resubmitted lots shall be kept separate from new lots, and shall be tested using a tightened inspection PDA of 3%.

5.0 QUALITY CONFORMANCE INSPECTION

Quality Conformance Inspection shall be conducted in accordance with the requirements of Groups A, B, C, and D of Method 5005. Inspection lot sampling shall be in accordance with Appendix B of MIL-M-38510. All lots submitted for quality conformance inspection shall have met the 100% screening requirements defined in 4.0 prior to submission (with the exception of those subgroups for which electrical rejects may be used as test samples).

5.1 GROUP A INSPECTION

Group A inspection shall be performed on each lot to the LTPD levels indicated in Table II and shall consist of the electrical parameter tests defined by the applicable detail specification or RETS. Where no parameters are indicated as tested for a given subgroup, that subgroup will not be performed. The manufacturer reserves the right to combine subgroups for test purposes, provided the LTPD for the combined subgroup is equal to or less than the lowest LTPD specified for any of the subgroups so combined. If a lot is composed of multiple sublots, each sublot must pass Group A inspection as specified.

TABLE I: 100% Screening

1. Internal visual External visual (Note 4)	2010, test condition B 2009	100% 100%
2. Stabilization bake	1008 24 hrs. @ condition C min	100%
3. Temperature cycling	1010, test condition C	100%
4. Constant acceleration	2001, test condition E (Note 6) Y_1 orientation only	100%
5. Visual inspection (Note 1)		100%
6. Initial (pre-burn-in) electrical parameters	Per applicable device specification	Op. at mfr's discretion
7. Burn-in test	1015 160 hrs @ 125°C min (or equivalent per Table I of Method 1015)	100%
8. Interim (post-burn-in) electrical parameters	Per applicable device specification	100%
9. Percent defective allowable (PDA) calculation	See 4.2	All lots
10. Final electrical test (a) Static tests (1) 25°C (subgroup 1, Table 2) (2) Maximum and minimum rated operating temp. (subgroups 2, 3, Table II) (b) Dynamic tests and switching tests 25°C (subgroups 4 and 9, Table 2) (c) Functional test 25°C (subgroup 7, Table 2)	Per applicable device specification (Note 5)	 100% 100% 100% 100%
11. Seal (a) Fine (b) Gross		100% (Note 2)
12. Qualification or quality conformance inspection test sample selection		(Note 3)

Note 1: At the manufacturer's option, visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages or lids off.

Note 2: The fine and gross seal tests shall be performed separately or together in any sequence or order between steps 5 and 11, and they shall be performed after all forming and shearing operations on the terminals.

Note 3: Samples shall be selected for testing in accordance with the requirements of paragraph 5.0 and Tables 2 through 5.

Note 4: External visual inspection shall be performed on the lot any time after step 11 and devices submitted to qualification and/or quality conformance testing shall undergo this testing prior to shipment.

Note 5: All devices whose lead finish is changed or reworked after final electrical testing shall be retested for subgroups 1 and 7 at a minimum.

Note 6: To-3 Devices use condition D instead.

5.2 GROUP B INSPECTION

Group B inspection shall consist of the mechanical and environmental tests specified in Table III. Group B inspection shall be performed on each package type and lead finish for each week of assembly per assembly location. Alternately, Group B may be performed on each inspection lot, per package type, lead finish, and detail specification. Testing of one device type sublot in any subgroup shall be considered as complying with the requirements for that subgroup for all device types covered by that Group B test. When Group B is performed per week of assembly, each sublot must be subjected to subgroup 4.

5.3 GROUP C INSPECTION

Group C inspection shall consist of the die-related tests specified in Table IV. Group C tests are required for each microcircuit group (see 5.3.1 and Table VI) and shall be performed on one device type or one inspection lot from each three months of production for each microcircuit group.

5.3.1 MICROCIRCUIT GROUP ASSIGNMENTS

A microcircuit group shall consist of devices utilizing a common fabrication technology to perform a similar circuit function, utilizing the same supply, bias and signal voltages, and assembled using the same die-attach and wire-bond methods. National's microcircuit group assignments as shown in Table VI.

5.3.2 GROUP C SAMPLE SELECTION

Samples for subgroups in Group C shall be randomly chosen from any inspection lot of a particular microcircuit group (see 5.3.1) which has been submitted to and

TABLE II: Group A Electrical Tests (Note 1)

Subgroup (Notes 2 and 3)	Class B LTPD (Note 4)
Subgroup 1 Static tests at 25°C	2
Subgroup 2 Static tests at maximum rated operating temperature	3
Subgroup 3 Static tests at minimum rated operating temperature	5
Subgroup 4 Dynamic tests at 25°C	2
Subgroup 5 Dynamic tests at maximum rated operating temperature	3
Subgroup 6 Dynamic tests at minimum rated operating temperature	5
Subgroup 7 Functional tests at 25°C	2
Subgroup 8 Functional tests at maximum and minimum operating temperatures	5
Subgroup 9 Switching tests at 25°C	2
Subgroup 10 Switching tests at maximum rated operating temperature	3
Subgroup 11 Switching tests at minimum rated operating temperature	5

Note 1: The specific parameters to be included for tests in each subgroup shall be as specified in the applicable detail specification. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

Note 2: A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100% inspection shall be allowed (see 30.2.5 of appendix B of MIL-M-38510).

Note 3: Group A testing by subgroup or within subgroups may be performed in any sequence unless otherwise specified.

Note 4: Maximum accept number allowed is 2.

has passed Group A quality conformance inspection. Testing of one device for each subgroup shall be considered as complying with the requirements for that subgroup for all devices within the applicable microcircuit group. The product which may be accepted for delivery based upon a successful completion of Group C testing shall be product within the tested microcircuit group with inspection lot identification codes of the 26 consecutive weeks beginning with the inspection lot identification code of the successful Group C sample.

5.4 GROUP D INSPECTION

Group D Inspection shall consist of the package related testing shown in Table V. Group D tests on each package type shall be performed on devices from each six months of production (based upon inspection lot identification codes). Where the package tested is provided with more than one lead finish, each additional lead finish shall be subjected to subgroups 3, 5, and 7 of Group D.

5.4.1. GROUP D SAMPLE SELECTION

Samples for subgroups in Group D shall be selected from any inspection lot containing the intended package and lead finish which has been submitted to and has passed Group A quality conformance inspection. The product which may be accepted for delivery based on a successful completion of Group D testing shall be product of the particular package type with inspection lot identification codes of the 36 consecutive weeks beginning with the inspection lot identification code of the successful Group D sample. Testing of a subgroup using a single device type enclosed in given package shall be considered as complying with the requirements of that subgroup for all device types utilizing that package and lead finish. Different device types may be used for each subgroup.

5.5 END POINT TESTS FOR GROUPS B, C, AND D

End point measurements and other specified post-test measurements shall be made for each microcircuit of the sample after completion of all other specified tests in each subgroup. The test limits for the end point measurements shall be the same as the limits for the respective Group A subgroup inspections.

5.6 RESUBMISSION OF FAILED LOTS

Procedures for resubmission of lots failing Group A, B, C, or D Quality Conformance Inspections shall be as specified in MIL-M-38510.

6.0 QUALIFICATION TESTING

Qualification of individual device types or groups of related device types shall be accomplished by subjecting them to and demonstrating that they meet all of the Group A, B, C, and D requirements of Method 5005 of MIL-STD-883. Qualification testing shall be performed on devices that have been screened in accordance with Paragraph 4.0.

6.1 END POINTS

Electrical end points shall be measured before starting and after completion of all tests in the subgroups of Groups B, C, and D for which electrical end point measurements are specified. Where no intervening tests have been performed, the final electrical measurements performed during 100% screening shall be considered as satisfying the requirement for testing prior to Group B, C, or D testing. End point measurements need not be recorded.

6.2 LOT SIZE

The inspection lot from which the qualification samples are to be selected shall contain a minimum of twice the number of devices required for the performance of the qualification testing.

6.3 QUALIFICATION STATUS

Two levels of qualifications shall exist. Level I and Level II. A Level I part shall be one which has successfully com-

TABLE III. Group B (Note 1)

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 1 (a) Physical dimensions (Note 2)	2016		2 devices (no failures)
Subgroup 2 (a) Resistance to solvents	2015		4 devices (no failures)
Subgroup 3 (a) Solderability (Note 5)	2022 or 2003	Soldering temperature of 245 ± 5°C	15
Subgroup 4 (a) Internal visual and mechanical (Note 7)	2014	Failure criteria from design and construction requirements of applicable procurement document	1 device (no failures)
Subgroup 5 (a) Bond strength (Note 4)	2011	Test condition C or D	15
Subgroup 6 (Note 3) (a) Internal water-vapor content	1018	1,000 ppm maximum water content at 100°C	3 devices (0 failure) or (Note 6) 5 devices (1 failure)
Subgroup 7 (Note 8) (a) Seal (1) Fine (2) Gross	1014	As applicable	5
Subgroup 8 (Note 9) (a) Electrical parameters (b) Electrostatic discharge sensitivity classification (c) Electrical parameters	3015	Group A, subgroup 1 Group A, subgroup 1	15(0)

Note 1: Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required, except devices being submitted to subgroup 7.

Note 2: Not required for qualification or quality conformance inspection where group D inspection is being performed on samples from the same inspection lot.

Note 3: Not required on National Products, since National does not use desiccants inside any packages.

Note 4: Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in method 5004, prior to sealing provided all other specifications requirements are satisfied (e.g. bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the LTPD sample size for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see method 2011).

Note 5: All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in. In the case of hot solder dip or fused tin lead finishes, the burn-in screen may precede the solder dip or tin fusing operation.The LTPD for solderability test applies to the number of leads inspected except in no case shall less than 3 devices be used to provide the number of lead required.

Note 6: Test three devices; if one fails, test two additional devices with no failures.

Note 7: Test samples for internal, visual and mechanical shall be selected at any point following the seal operation.

Note 8: This test is not required if either the 100% screen or sample seal test is performed between 3.1.16 and 3.1.20 of method 5004.

Note 9: Unless otherwise specified, test shall be performed for initial qualification and product redesign as a minimum. Alternately, devices may be classified as category A in lieu of testing.

TABLE IV. Group C (Die-Related Tests)

Test	MIL-STD-883		LTPD
	Method	Condition	
Subgroup 1			
(a) Steady state life test (Note 1)	1005	Test condition A, B, C, or D (1,000 hours at 125°C)	5
(b) End-point electrical parameters		Group A subgroup 1, 2 & 3 parameters per the applicable device specification	
Subgroup 2			
(a) Temperature cycling	1010	Test condition C	15
(b) Constant acceleration	2001	Test condition E min. (Note 3) Y_1 orientation only	
(c) Seal	1014	As applicable	
(1) Fine			
(2) Gross			
(d) Visual examination (Note 2)		Group A subgroup 1, 2 & 3 parameters per the applicable device specification	
(e) End-point electrical parameters			

Note 1: See 40.4 of Appendix B of MIL-M-38510.

Note 2: Visual examination shall be in accordance with method 1010 or 1011.

Note 3: TO-3 Packages shall be tested to Condition D.

pleted all of the Group A, B, C, and D inspections. Where a device type that has not completed Level I qualification falls within a microcircuit group for which other devices have been qualified, and is manufactured in a package which has been qualified, it will be considered qualified for Level II (and therefore shippable) once it has successfully completed Group A and B testing. No device may remain on Level II status for more than one year without successfully completing qualification testing.

6.4 QUALIFICATION BY EXTENSION

Qualification by die-related testing or qualification by extension, where applicable, shall be in accordance with the procedures defined in MIL-M-38510.

7.0 PACKAGING

Packing and Packaging shall be in accordance with MIL-M-38510. All devices classified as Category A for electrostatic discharge sensitivity and so marked (see 3.7.5) shall be packaged in conductive material or packaged in antistatic material with an external conductive field shielding barrier.

8.0 DATA

All 883B/RETS™ microcircuits shipped shall be accompanied by a Certificate of Conformance certifying their full compliance with the requirements of Methods 5004 and 5005 of MIL-STD-883 (as specified herein). Attributes data for the 100% screening and quality conformance inspection test data will not normally be provided but shall be retained on file for a period of three years from the date of the inspection lot identification code (or in the case of the quality conformance data the inspection lot identification code of the last lot whose quality conformance test requirements were met by that lot).

9.0 MIL-HDBK-217 QUALITY FACTORS

Devices processed in accordance with the requirements defined herein meet Quality Level B-1 of Table 2.1.5-1 of MIL-HDBK-217 for failure rate modeling in accordance with MIL-HDBK-217.

10.0 HYBRID MICROCIRCUITS

Hybrid microcircuits are not processed in accordance with this document. For Class B hybrid microcircuits refer to "883B/RETS™ Hybrid Microcircuits from National Semiconductor."

11.0 CLASS S MICROCIRCUITS

National Semiconductor Corporation also maintains a program for providing integrated circuits processed to the requirements of MIL-STD-883, Class S. These procedures are defined in the brochures "883S/RETS™ Integrated Circuits from National Semiconductor" and "883S/RETS™ Hybrid Microcircuits from National Semiconductor."

12.0 LEAD FINISH FOR TO-3 (K) PACKAGE

When TO-3 packages with solder-dipped leads are provided to this document, the leads will be dipped only to .100 ± .050 inches from the seating plane.

TABLE V. Group D (Package Related Tests)

Test	MIL-STD-883		Quantity/(Accept No.) or LTPD
	Method	Condition	
Subgroup 1 (Note 1) (a) Physical dimensions	2016		15
Subgroup 2 (Note 1) (a) Lead integrity (Note 7) (b) Seal (1) Fine (2) Gross	2004 1014	Test condition B_2 (lead fatigue) As applicable	15
Subgroup 3 (Note 3) (a) Thermal shock (b) Temperature cycling (c) Moisture resistance (Note 8) (d) Seal (1) Fine (2) Gross (e) Visual examination (f) End-point electrical parameters (Note 4)	1011 1010 1004 1014	Test condition B as a minimum, 15 cycles minimum Test condition C, 100 cycles minimum As applicable Per visual criteria of method 1004 and 1010 Group 8, subgroup 1, 2 & 3 parameters per the applicable device specification	15
Subgroup 4 (Note 3) (a) Mechanical shock (b) Vibration, variable frequency (c) Constant acceleration (d) Seal (1) Fine (2) Gross (e) Visual examination (Note 5) (f) End-point electrical parameters	2002 2007 2001 1014	Test condition B minimum Test condition A minimum Test condition E minimum (Note 11), Y_1 orientation only As applicable Group A, subgroup 1, 2 & 3 parameter, per the applicable device specification	15
Subgroup 5 (Note 1) (a) Salt atmosphere (b) Seal (1) Fine (2) Gross (c) Visual examination	1009 1014	Test condition A minimum As applicable Per visual criteria of method 1009	15
Subgroup 6 (Note 1) (a) Internal water-vapor content	1018	5,000 ppm maximum water content at 100°C	3 devices (0) failures or 5 devices (1 failure) (Note 6)
Subgroup 7 (Note 1) (a) Adhesion of lead finish (Notes 9 and 10)	2025		15
Subgroup 8 (a) Lid torque (Notes 1 and 2)	2024		5(0)

Note 1: Electrical reject devices from that same inspection lot may be used for samples.

Note 2: Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (i.e., wherever frit seal establishes hermeticity or package integrity).

Note 3: Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

Note 4: At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

Note 5: Visual examination shall be in accordance with method 1010 or 1011.

Note 6: Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample (i.e., 3 or 5 devices) fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes, the lot shall be accepted provided the devices and data from both submissions is submitted to the qualifying activity along with five additional devices from the same lot.

Note 7: For leadless chip carrier packages only, use test condition D.

Note 8: Lead bend stress. Initial conditioning is not required for leadless chip carrier packages.

Note 9: The adhesion of lead finish test shall not apply for leadless chip carrier packages.

Note 10: LTPD based upon number of leads.

Note 11: TO-3 Packages shall be tested to Condition D.

TABLE VI. Microcircuit Group Assignments

Microcircuit Group	Product
1	Standard TTL Logic
2	Schottky TTL Logic
3	Bipolar RAMs
4	Bipolar PROMs
5	Low Power TTL Logic
6	CMOS Logic
7	HC CMOS Logic
8	CMOS RAMs
9	CMOS EPROMs
10	MOS RAMs
11	MOS EPROMs
12	MOS E^2PROMS
13	Amplifiers
14	Comparators
15	Interface

Microcircuit Group	Product
16	Regulator, Reference
17	Other Linear
18	BiFET™ Amplifier
19	Other BiFET
20	Bipolar Microprocessor
21	CMOS Microprocessor
22	CMOS COPS
23	NMOS COPS
24	NMOS Microprocessors
25	Hybrid Switch
26	Hybrid Driver
27	Linear Hybrid
28	Not Assigned
29	CMOS E^2PROM
30	CMOS Gate Arrays

Section 9

Reliability

9

Section Contents

INTRODUCTION TO THE RELIABILITY MILITARY/AEROSPACE PROGRAMS

History

In the mid 1960's the various government agencies responsible for semiconductor reliability saw that screenable defects were resulting in an in-equipment failure rate of about 1% per thousand hours. In-depth failure analysis allowed them to determine what the predominate failure mechanisms were. The Solid State Applications Branch of the Air Force's Rome Air Development Center (RADC) was assigned the task of developing a screening procedure which would remove the infant mortality failures which had led to the high failure rate previously encountered. Working closely with other semiconductor reliability experts, the RADC staff developed MIL-STD-883, which was first issued in 1968. The objective of MIL-STD-883 was to create an economically feasible, standardized integrated circuit screening flow which would achieve an in-equipment failure rate of 0.08% per thousand hours for Class B and 0.004% per thousand hours for Class A (which was later superseded by Class S). Over the years this standard has grown and matured with a number of new test methods added as reliability information and failure analysis results became more detailed. These developments have led to one of the strongest and most comprehensive screening specs available, MIL-STD-883.

Purpose and Structure

MIL-STD-883 states: this standard establishes uniform methods and procedures for testing microelectronic devices, including basic environmental tests to determine resistance to deleterious effects of natural elements and conditions surrounding military and space operations, and physical and electrical tests. What does this mean to the semiconductor user? To understand this, one must subdivide MIL-STD-883 into two primary areas: 1) Detailed how-to specifications (methods 1001 through 4007) and 2) Screening and qualification and/or quality conformance testing requirements (methods 5001 through 5009). By examining each of these areas the thrust of MIL-STD-883 will become apparent.

Detailed How-to Specifications

MIL-STD-883 is a collection of environmental, mechanical, visual, and electrical test methods. These methods define tests which enable manufacturers and users to screen for specific reliability concerns. The tests covered include moisture resistance, high temperature storage, neutron irradiation, shock and acceleration tests, visual radiography, and dimensional tests, to mention only a few. In the electrical test section, there are tests to examine load conditions, power supplies, short circuit currents, and other tests. Each of these tests is designed to look at specific reliability and quality concerns that affect semiconductor products.

Screening Flows

The overall reliability requirements for a system depend upon a number of factors, including cost-effectiveness. For example, a deep space probe, where component replacement is impossible once the system is launched, requires very high reliability, despite the inherent cost of complex screening. On the other hand, a ground-based radio unit can use a less stringent reliability testing sequence, since a failed component can be easily replaced at moderate cost. In line with this range of needs, MIL-STD-883 established three distinct product assurance levels to provide reliability commensurate with the product's intended application. The three levels are Class S (intended for critical applications, such as space), Class B (intended for less critical applications, such as airborne or ground systems), and Class C (intended for easily replaceable systems, which has since been eliminated).

National and MIL-M-38510

A major thrust exists among integrated circuit users, suppliers, and the U.S. Government to avoid proliferation of military procurement specifications by turning instead to standardized high reliability microcircuits. National Semiconductor endorses and supports this trend.

One major program to which National is heavily committed is the JAN MIL-M-38510 IC program. This is a standardization program administered by the U.S. Defense Department which allows a user to purchase a broad line of standard products from a variety of qualified suppliers.

There is only one MIL-M-38510 program. National is committed to supplying only QPL devices, and discourages any "pseudo-38150" alternates.

There are two levels specified within MIL-M-38510 — Classes S and B. Class S is typically specified for space flight applications, while Class B is used for aircraft and ground systems.

MIL-M-38510

The Defense Electronic Supply Center (DESC) administers the integrated circuit standardization program known as MIL-M-38510 (sometimes referred to as the JAN IC Program). The specification set used to define the program consists of four documents: general specification MIL-M-38510, which is an overall definition of the processing and testing to be performed; detail specifications (referred to as "slash sheets"), each of which defines the performance parameters for a unique generic device or a family of devices; MIL-STD-883, which defines specific screening procedures; and MIL-STD-976, which defines line certification requirements.

When a user orders a MIL-M-38510 device, he is guaranteed that he will get a device fully conformant with the detail specification and which has also met all of the general testing and processing requirements. DESC requires semiconductor suppliers to become formally qualified under the MIL-M-38510 program and to be listed on the current Qualification Products List (QPL) before they are allowed to legally ship JAN devices.

Advantages to the User

The JAN 38510 program has numerous advantages for the integrated circuit user.

- A single explicit specification eliminates guesswork concerning device electrical characteristics or processing flow.
- The rigorous schedule of quality conformance testing that is a mandatory part of the MIL-M-38510 program assures the user of long-term stability.
- Since the electrical characteristics of the devices are at least as tight as the "standard industry data sheet" parameters, device performance will meet the vast majority of system design requirements. Additionally, min./max. limits replace many data sheet typicals, making circuit design and worst case design analysis decisions easier.
- The user is spared the expense of researching and preparing his own procurement document.
- The user is spared the expense of qualification testing. The QPL tells him which suppliers have qualified the device he requires.
- The QPL gives the user a choice of qualified suppliers for devices that are fully interchangeable. In addition, the presence of several sources guarantees competitive pricing that is typically lower than for devices to a user's own specifications.
- Since MIL-M-38510 is a standard program, procurement lead times will be shorter. With a large number of programs using JAN devices, distributors and manufacturers are able to establish inventories of JAN devices. National in particular is committed to maintaining finished goods and work-in-process inventories to support our customers' needs.
- Spare parts will be readily available without excessive minimum order requirements.
- Standard parts with volume requirements will remain in production longer.
- Device markings are consistent from one manufacturer to another.
- The program is extremely cost-effective. A user can purchase a few devices for engineering evaluation and prototyping and know that they will be identical to the devices he will get during production. When the cost factors associated with spec. writing, supplier qualification, maintaining voluminous parts control documentation, and the more intangible benefits of device availability are totaled, use of JAN ICs is overwhelmingly the most cost-effective approach.

Advantages to the Supplier

What motivates a supplier like National Semiconductor to be so heavily committed to the MIL-M-38510 program? National has the *broadest* range of reliability processed products available in the semiconductor industry. A program such as MIL-M-38510 helps to standardize the processing required and to minimize the number of individual user specifications. This allows National to concentrate more resources on this program, thereby improving product quality and availability.

The Most Frequently Asked Questions and Answers about MIL-M-38510

There are many questions which are frequently asked regarding the MIL-M-38510 program. We would like to answer some of them.

Q. WHAT MUST A MANUFACTURER DO TO GET HIS PARTS LISTED ON THE QPL?

A. There are two things which a manufacturer is required to do. First, he must get his facilities (including wafer fab, assembly, and rel processing areas) certified by DESC. This requires that each fab area used for QPL devices must be approved. Second, for each specific device and package combination listed on the QPL, the manufacturer must perform extensive qualification testing and provide detailed device information to DESC. This data is typically supplied in two phases.

In the first phase, the manufacturer must supply detailed information concerning the device construction and electrical characteristics. Once this data has been verified by DESC to confirm that the manufacturer's device meets the MIL-M-38510 requirements, the manufacturer is listed on Part II of the QPL. At this point the manufacturer is legally able to supply full JAN qualified devices meeting ALL of the MIL-M-38510 requirements. The manufacturer must then perform the full qualification testing of Method 5005 of MIL-STD-883 as specified in paragraph 4.4 of MIL-M-38510. Once this data has been reviewed and accepted by DESC, the manufacturer is listed on Part I of the QPL.

Q. IS THERE ANY DIFFERENCE IN DEVICES PRODUCED WHILE A MANUFACTURER IS LISTED ON PART II OF THE QPL AND THOSE PRODUCED AFTER PART I QUALIFICATION IS COMPLETED?

A. There is absolutely *no difference*. A supplier must meet all of the device screening and quality conformance requirements no matter what his QPL status.

Q. HOW DOES A USER KNOW WHAT DEVICES ARE COVERED BY SLASH SHEET SPECIFICATIONS?

A. Supplement 1 to MIL-M-38510 contains a listing of the slash sheet specifications and a cross reference to the generic part type. This is updated as new slash sheets are released. National's Reliability Handbook also contains a cross reference.

Q. HOW CAN A USER OBTAIN COPIES OF THE QPL, SUPPLEMENT 1 OF MIL-M-38510, MIL-M-38510 ITSELF, AND MIL-STD-883?

A. Copies of these and other related documents may be obtained from:

Naval Publications and Forms Center
5801 Tabor Avenue
Philadelphia, PA 19120
(212) 697-2179

Q. WHAT ABOUT THOSE DEVICES FOR WHICH NO DETAIL SPECIFICATION EXISTS?

A. The ultimate aim of a standardization program must be to furnish *all* parts. Requests for addition of a part to MIL-M-38510 should be made to DESC Directorate of Engineering, Dayton, Ohio 45444, indicating a need for slash sheets and/or suppliers to be qualified for the additional devices. National has a form (available through local sales offices) which may be used for this purpose. In addition, if only some parts are available, a user can still see significant savings on those that are available.

Q. HOW IS A JAN QPL DEVICE MARKED?

A. Tables I and II explain the details of the marking for JAN ICs.

TABLE I. MIL-M-38510 Part Marking

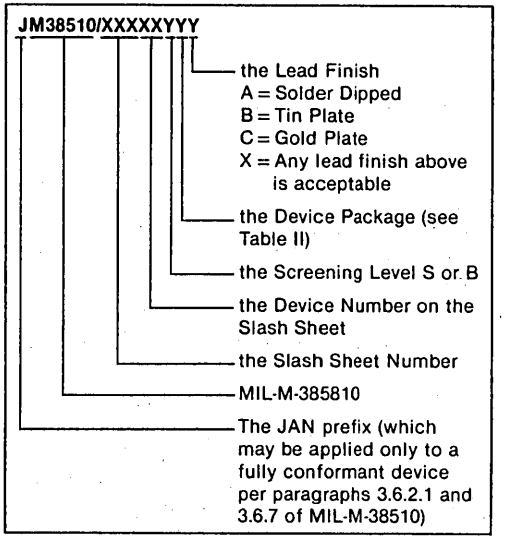


TABLE II. JAN Package Codes

38510 PACKAGE DESIGNATION	MICROCIRCUIT INDUSTRY DESCRIPTION
A	14-pin 1/4″ x 1/4″ (metal) flatpack
B	14-pin 3/16″ x 1/4″ flatpack
C	14-pin 1/4″ x 3/4″ dual-in-line
D	14-pin 1/4″ x 3/8″ (ceramic) flatpack
E	16-pin 1/4″ x 7/8″ dual-in-line
F	16-pin 1/4″ x 3/8″ (metal or ceramic) flatpack
G	8-pin TO-99 can or header
H	10-pin 1/4″ x 1/4″ (metal) flatpack
I	10-pin TO-100 can or header
J	24-pin 1/2″ x 1-1/4″ dual-in-line
K	24-pin 3/8″ x 5/8″ flatpack
M	12-pin TO-101 can or header
P	8-pin 1/4″ x 3/8″ dual-in-line
Q	40-pin 8/16″ x 2-1/16″ dual-in-line
R	26-pin 1/4″ x 1-1/16″ dual-in-line
S	20-pin 1/4″ x 1/2″ flatpack
V	18-pin 3/8″ x 1-15/16″ dual-in-line
W	22-pin 3/8″ x 1-1/8″ dual-in-line
X, Y, Z	Unassigned — Reserved for identifying special packages whose dimensions are carried in the detail specifications.

Q. ARE DEVICES CALLED "M38510, JAN PROCESSED, JAN EQUIVALENT, ETC." REALLY QPL PRODUCTS?

A. *Absolutely not.* There is only one QPL product — it is a JM38510 marked device. "JAN Equivalent" is expressly forbidden by para-

graphs 3.1 and 3.6.7 of MIL-M-38510. MIL-M-38510 does provide for the production of devices when no qualified sources exist, but this may be done only with prior DESC approval, and products produced under this provision must meet all requirements of MIL-M-38510 other than qualification.

Q. HOW LONG CAN A SUPPLIER REMAIN ON PART II OF THE QPL?

A. For Class B, a manufacturer can remain on Part II for two years or until 90 days after another supplier becomes qualified for the same device package, screening level, and lead finish combination on Part I of the QPL. Class S devices may remain on Part II for one year after another manufacturer reaches Part I.

Q. WHEN ANOTHER SUPPLIER OBTAINS PART I QUALIFICATION, ARE THE OTHER QUALIFIED SUPPLIERS REMOVED FROM PART II IMMEDIATELY?

A. No. The supplier is given 90 days before being removed from Part II for a Class B device and one year for a Class S device. During that time a supplier may legally accept orders for those devices. After the end of the 90-day or one year period, he may no longer accept orders but may complete and ship those orders received prior to that time, no matter how long it takes him to complete them.

Q. IS A SUPPLIER EVER REMOVED FROM PART I QUALIFICATION?

A. Generally not. As long as a supplier continues to manufacture the device, maintains appropriate facility approvals, and submits all required reports and information to DESC within stipulated time limits, he will retain QPL I listing. Violation of these requirements can be cause for removal from QPL.

Q. CAN AN AUTHORIZED DISTRIBUTOR SHIP JAN DEVICES FROM HIS SHELVES IF THE MANUFACTURER HAS LOST HIS QPL LISTING FOR THOSE DEVICES?

A. Yes. As long as those devices were ordered by the authorized distributor while the manufacturer had QPL listing for those devices, the distributor may subsequently ship those devices from his shelves.

Q. CAN A MANUFACTURER LEGALLY SHIP JAN QPL MATERIAL HE ASSEMBLED AND TESTED BEFORE HE RECEIVED A QPL LISTING?

A. Yes. The manufacturer must assemble and screen parts to prove his ability to comply with the specifications before he can be placed on QPL. As a result, his first lot of material, which is fully conformant to QPL product requirements, will have a date code that is earlier than the date he is placed on the QPL. However, the manufacturer may *not* begin to assemble and test unless he has a line certification and an approval to proceed with qualification.

Q. WHAT IS THE RELATIONSHIP BETWEEN MIL-M-38510 AND MIL-STD-883?

A. MIL-M-38510 defines complete program requirements and the detail device electrical performance parameters. The device processing requirements are specified in MIL-STD-883.

Q. SUPPOSE DEVICES ARE KEPT ON A MANUFACTURER'S OR DISTRIBUTOR'S SHELVES FOR A PERIOD OF TIME; MUST THEY EVER BE RETESTED TO VALIDATE THAT THEY STILL MEET SLASH SHEET CHARACTERISTICS?

A. Yes. Devices held by a manufacturer or by his authorized distributor which have a date code older than 24 months must be retested by the manufacturer in accordance with Group A sampling requirements prior to shipment to a customer or return to inventory.

Q. WHY SHOULD A USER SPECIFY "X" IN THE LEAD FINISH DESIGNATION FOR A PART TYPE?

A. A manufacturer who receives an order for a specific lead finish for which he is qualified but has no inventory at the time of order may not be able to fill the order in a timely manner, even though he might have substantial inventory of another lead finish. Unless a user has a specific reason for wanting a particular lead finish, he should allow his suppliers the flexibility of shipping whatever finish is available.

Q. WHAT DATA IS A MANUFACTURER REQUIRED TO SHIP WITH A JAN PART?

A. A certificate of conformance is all that is required. However, he must retain all data for three years.

Q. CAN A DEVICE FOR WHICH THERE IS NO SLASH SHEET BE PROCESSED TO MIL-M-38510?

A. Since MIL-M-38510 invokes a combination of the processing requirements of MIL-STD-883 and the detail device performance parameters contained in each individual slash sheet, the answer is obviously no. However, National's 883B/RETS™ program does provide parts which meet all of the screening requirements of the MIL-STD-883 specification and which have been subjected to all of the MIL-M-38510 controls (except for domestic assembly).

TABLE III. Sample MIL-M-38510 Listing

GOVERNMENT DESIGNATION				TEST REPORT NUMBER	MANUFACTURER'S NAME
DEVICE TYPE*	DEVICE CLASS	CASE OUTLINE	LEAD MATERIAL AND FINISH		
M38510/008					
01	S only	A	C	38510-953-81	National Semiconductor Corp.
01	B	C	A	38510-953-81	National Semiconductor Corp.
02		D	B	38510-30-7T	
03	B	C	A	38510-520-83	National Semiconductor Corp.
			B		

*"M38510" is the military designator for MIL-M-38510. The QPL shows this notation even though the parts are fully qualified devices and are marked JM38510/XXXXXYYY.

Q. WHAT DOES A QPL LISTING LOOK LIKE AND HOW DO YOU READ IT?

A. Sample QPL listings are shown in Table III.

JM38510/00801SAC
JM38510/00801BCA
JM38510/00801BCB
JM38510/00801BDA
JM38510/00801BDB
JM38510/00802BCA
JM38510/00802BCB
JM38510/00802BDA
JM38510/00802BDB
JM38510/00803BCA
JM38510/00803BCB

Q. WHAT QUALITY CONFORMANCE TESTS ARE CONDUCTED? ARE ALL DEVICES IN A GENERIC FAMILY EVENTUALLY SUBJECTED TO QUALITY CONFORMANCE TESTING?

A. For B level devices quality conformance tests must be conducted as follows:

Group A—Each inspection lot or sublot.

Group B—Each inspection lot for each package type and lead finish on each detail specification.

Group C—Periodically at 3-month intervals on one device type or one inspection lot from each mircocircuit group in which a manufacturer has qualified device types (die related tests).

Group D—Periodically at a 6-month interval for each package type for which a manufacturer holds qualifications (package related tests).

Different devices within a generic family are chosen for successive quality conformance tests until all of the devices have been subjected to testing. The sequence is then repeated. The manufacturer must submit attributes data to DESC for all quality conformance tests performed.

Q. HOW IS AN INSPECTION LOT DEFINED?

A. For Class B devices, each inspection lot shall consist of microcircuits of a single device type, in a single package type and lead finish, or may consist of inspection sublots of several different device types, in a single package type and lead finish, defined by a single detail specification. Each inspection lot shall be manufactured on the same production line(s) through final seal by the same production techniques, and to the same device design rules and case with the same material requirements, and sealed within the same period not exceeding 6 weeks.

Q. WHAT IS NATIONAL SEMICONDUCTOR'S COMMITMENT TO MIL-M-38510?

A. National Semiconductor is convinced that the level of standardization offered by a program like MIL-M-38510 is the key to long-term military component procurement viability. We have a corporate commitment to MIL-M-38510. We believe that the program will be of significant benefit in lessening the problem of product obsolescence, for the volume provided will help to keep many key devices in production. We believe that the program will make possible the procurement of devices in small quantities with reasonable lead times for long-term spares or field maintenance requirements.

National Semiconductor will continue to maintain a broad base of line certifications and an extensive list of Class B and Class S device qualifications. We will continue to work with the Department of Defense, concerned users, and other semiconductor manufacturers to update and redefine the applicable specifications. We feel that this level of support is essential if MIL-M-38510 is to remain the strongest standardization program available.

In addition, we will continue to add capacity and to build up substantial inventories of a large spectrum of products to ensure the

availability and the lead times that are needed for key military programs.

National Mil/Aero Standardization Programs

Your customer has imposed upon you requirements for product reliability that you must meet on every single component you buy. In most cases, these requirements mandate that you buy JAN MIL-M-38510 parts where they are available, and that all other devices must be as close to JAN as is achievable. We don't consider this unreasonable. In fact, we believe that this is the only reasonable and intelligent approach.

To meet this objective, we designed our 883B/RETS program around requirements that were already imposed for the MIL-M-38510 program.* We realize that there are many so-called standardization programs available in the marketplace which lack the compliance that you need. Our 883B/RETS program is totally compliant. We invite you to make this comparison between what we offer and what you need. Our screening flow, our 5% PDA, our quality conformance test frequency, and the other items that you consider important, match exactly the requirements defined in MIL-M-38510.** If they did not, we could not offer ***Total Standardization***.

Standardization provides the manufacturing efficiencies needed by the semiconductor manufacturers if they are to meet military semiconductor needs. To the user, standardization offers the highest guarantee of quality and reliability through production consistency and uniformity. The most significant benefit of standardization to the Department of Defense, however, is that it ensures the availability of component level spares to key programs with the pricing, delivery, and reliability needed for the field support and maintenance of our key defense electronics systems.

National's MIL-M-38510 Emphasis

To implement this view of standardization, we have based our entire approach to military screening upon the Class S and Class B requirements of MIL-M-38510. We are convinced that to do less than this would be to provide an inferior product, one that does not meet the true needs of the Department of Defense. Our 883B/RETS microcircuits are processed through the most comprehensive and compliant Class B screening program offered by any semiconductor manufacturer. We have tried to emulate MIL-M-38510 to the fullest extent possible, with the same production controls, calibration schedules, rework and resubmission procedures, operator certification requirements, and all of the other key elements of MIL-M-38510. The procedures that we employ in the production of MIL-M-38510 devices are used for all of the military devices we manufacture.

Our 883S/RETS microcircuits are processed through a screening flow that matches the MIL-M-38510 Class S flow exactly. Our commitment to MIL-M-38510 Class S is such that once qualified for a given device type we will sell that part only as a JAN Class S part. Class S QPL listing will result in the immediate removal from production of the 883S/RETS version of the device.

National's Commitment

But compliance flows are obviously meaningless unless the capacity is in place to support them. We have the industry's largest screening capacity. Over the past few years we have reinvested substantial sums in additional capital equipment in both buildings and the equipment with which to fill those buildings. Our Tucson, Arizona plant was the first plant in the entire industry to be totally dedicated to the production of military integrated circuits. We will continue to add capacity for military assembly and test, even during those periods when others turn away from the military marketplace in pursuit of what they view to be the more attractive commercial market. We feel that a commitment to the needs of the military/aerospace user community should not be based upon the conditions encountered in the commercial marketplace. We have no plans for other than a continued long-term commitment to military/aerospace component production and screening. And we will not deviate from the highest standards of quality and reliability in our execution of that commitment. There are no shortcuts to semiconductor reliability. It can only be achieved through rigid adherence to established standards.

However, we also acknowledge the quite obvious fact that through refinement and redefinition, standards are subject to change. As those changes occur, we will update our current procedures to reflect the changes that find their way into MIL-M-38510 and MIL-STD-883. We will, where our understanding of semiconductor reliability and screening indicates the need, actively pursue those changes that we feel will allow our industry to provide a better product to the systems manufacturers. We will also steadfastly resist those changes which we feel sacrifice reliability to the less important question of expediency.

*Requirements that were subsequently incorporated into MIL-STD-883

**and MIL-STD-883.

National's Standard Programs

MIL-M-38510 is the key military standardization program for ICs. National is equally committed to the support of the requirements of the space segment of the market for MIL-M-38510 Class S devices. To support these needs we have established dedicated Class S assembly and test facilities. The realization that users could not obtain all the device types they required through these programs led National's Military/Aerospace Products Group to the development of two of the strongest and most compliant in-house programs in the industry. National programs for 883B/RETS and 883S/RETS microcircuits provide the systems manufacturer with an easy mechanism for obtaining those devices not listed on the MIL-M-38510 QPL. In response to other user needs, National also developed a program for radiation hardened devices (both CMOS and linear), a comprehensive program for radiation susceptibility testing for Class S devices, and a program for the production of devices in leadless chip carriers (LCCs).

RETS and Burn-In

One of the primary advantages of MIL-M-38510 is its clear definition and standardization of electrical test and burn-in requirements. One of the major drawbacks seen in the standard reliability screening programs of most semiconductor manufacturers is that electrical testing is invariably performed to some document that is not available to the user. The user has the right to know what he is buying. At National that testing is never vague or undefined. Both in-house programs (883B/RETS and 883S/RETS) are based upon a document called the RETS (an acronym for Reliability Electrical Test Specification. The RETS is a simplified but complete description of the testing performed as part of National's standard Rel electrical test programs, and is controlled by our QA department. The burn-in circuits and electrical test parameters for the MIL-M-38510 Class S and Class B devices produced by National Semiconductor are defined by the applicable detail specification.

Ordering ICs from National

Ordering National Semiconductor High Reliability integrated circuits is very simple. National sales offices and sales representatives can provide price and delivery information on our entire line of JM38510 Class B, JM38510 Class S, 883B/RETS and 883S/RETS microcircuits. A large percentage of these devices are available from inventory at either the factory or at one of our many distributors.

Ordering to Control Specifications

We also acknowledge the fact that many military systems manufacturers must, for contractual purposes, maintain their own specifications for many of the devices that they purchase. We have no objection to the use of contractor prepared procurement specifications, for we have found that the majority of these documents are written in compliance with the requirements of MIL-M-38510. Where this is true, we have found that they are also totally compatible with our in-house standardization programs. Where drawings submitted to National differ from the requirements outlined in MIL-M-38510, we welcome the opportunity to work with our customers to develop specifications which do meet the intent of MIL-M-38510.

Where customer specifications and our 883B/RETS product specifications correspond, we have the ability to expedite delivery by adding the customer part number in addition to the basic 883B/RETS part number. Customers who understand our program and wish to use the program in their parts procurement may order by placing "M/O" after their part number on their purchase order, thus allowing us to mark their part number on our 883B/RETS devices without the lengthy delay normally required for a comprehensive specifications review cycle. We have tried to provide programs that offer the maximum level of flexibility within the constraints of standardization.

Standardization is the key to cost-effective procurement of high reliability semiconductor devices. National Semiconductor Corporation is committed to that standardization.

Military Processing: A Corporate Commitment

The National Semiconductor Military/Aerospace Products Division draws upon the total resources of National Semiconductor. National is one of the world's largest manufacturers of semiconductor products, offering the largest number of product types available from any single source in the industry. This product line is growing faster than that of any other worldwide semiconductor manufacturer. Each new product is carefully evaluated for possible military/aerospace usage potential, and new product designs must comply with the reliability and quality constraints required by that segment of the industry. All new product designs are targeted to full military temperature range operation.

In addition, a dedicated Reliability Engineering Department within the Military/Aerospace Prod-

ucts Division coordinates burn-in circuit design, test tape development, test fixturing, support documentation, and new product release paperwork to ensure the earliest possible introduction of fully compliant 883B/RETS versions of the new products introduced by the company.

We are able to do this well, for National is no newcomer to this business. Founded in Danbury, Connecticut in 1959, National acquired an entire new management team in 1967 and moved corporate headquarters to Santa Clara, California. The new management team focused its attention on the transistor product line, and rapidly made that line profitable. Then the company's talents were turned to the development of linear, digital, and MOS integrated circuits — the fastest-growing segments of the semiconductor marketplace. Finally, an OEM representative and distributor network was established to develop and service a broad customer base, and facilities were added around the world to provide competitive products to worldwide markets.

The Reliability Test Department was initially formed in 1968 and reported at that time to the Director of Quality Assurance. The Rel Department developed the same rapid growth rate that the company as a whole had shown. From a small staff occupying several thousand square feet in Santa Clara, these reliability test operations grew until today they employ over 3000 people worldwide. Well over 200,000 square feet are devoted to the testing and assembly of high reliability products. During 1981, the Military/ Aerospace Products Group became the Military/ Aerospace Products Division. The company is currently involved in a number of military research and development programs, including a Phase I VHSIC contract.

VHSIC involvement was natural since National's technological leadership has enabled the company to consistently be one of the major suppliers of military/aerospace semiconductors. Having continued to develop a high technology image through the development olf Megarad hardened CMOS and linear device types, and the development of TRI-CODE™ logic, National is now expanding technology frontiers in the areas of memory, microprocessor, and data acquisition products. As a result of all this innovation, National has become the only company in the entire semiconductor industry capable of providing high reliability devices from all of the following product lines:

linear
hybrid
CMOS logic
Megarad CMOS logic
bipolar memory
MOS RAMs
CMOS RAMs
MOS EPROMs
CMOS EPROMs
MOS EEPROMs
data acquisition devices
standard TTL
low power TTL
low power Schottky
standard Schottky
interface devices
bipolar microprocessors
MOS microprocessors
CMOS microprocessors
COPS™ microcontrollers
high-speed CMOS Schottky
advanced low power Schottky
advanced Schottky

National Semiconductor has wafer fabrication plants in Santa Clara, California; Salt Lake City, Utah; Arlington, Texas; and Danbury, Connecticut. Many of these fabrication plants, along with our assembly and test lines in Santa Clara, California and Tucson, Arizona, have been fully certified for the production of Class S and Class B MIL-M-38510 circuits.

To support the requirements of the Class S marketplace, we have our own SEM and radiation testing facilities. Our screening capabilities are backed up by one of the most extensive failure analysis labs in the industry.

National is the leader in the military/aerospace integrated circuit market. We have achieved that leadership by offering an unmatched combination of technology, product breadth, understanding, commitment and capacity.

883B/883S/RETS Screening Flows

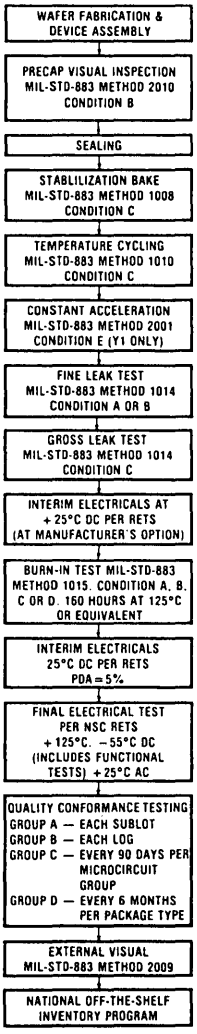
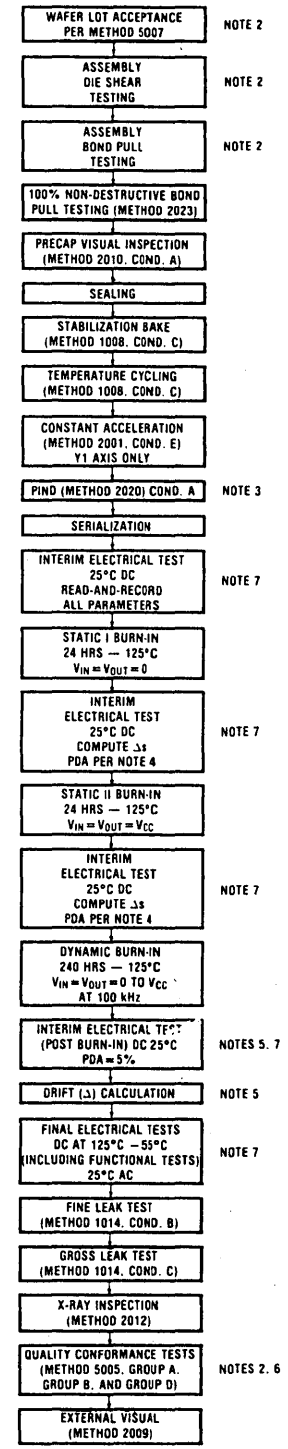


FIGURE 1. NATIONAL'S 883B/RETS CLASS B SCREENING FLOW



NOTES:
1. ALL METHODS REFERENCED ARE MIL-STD-883 TEST METHODS.
2. THESE TESTS ARE PERFORMED ON A SAMPLE BASIS. ALL OTHER TESTS ARE PERFORMED 100%.
3. ACCEPTANCE CRITERIA SHALL BE IN ACCORDANCE WITH MIL-M-38510.
4. THE PDA FOR STATIC I AND STATIC II BURN-IN SHALL BE 5% TOTAL.
5. THE PDA INCLUDES Δ FAILURES.
6. GROUP A AND BOND PULL AND DIE SHEAR TESTING OF GROUP B MAY BE PERFORMED ON-LINE.
7. ALL ELECTRICAL TESTING SHALL BE IN ACCORDANCE WITH THE APPLICABLE RETS OR THE APPLICABLE MIL-S-38510 DETAIL SPECIFICATION.

FIGURE 2. NATIONAL'S 883S/RETS CLASS S SCREENING FLOW

THE A+ RELIABILITY ENHANCEMENT PROGRAM

The quality and reliability of National Semiconductor's products have always stood among the best in the business.

But as the complexity of semiconductor devices increased over the years, many of our customers—especially those whose products were highly sensitive to warranty and repair considerations—began asking us for the benefits associated with additional processing.

So we set out to develop ways to provide the extra measure of quality and reliability needed for high-stress or difficult-to-service applications; to make these enhanced products available on an immediate-delivery basis; and to do it all for a cost low enough that our customers could remain competitive in their own markets.

This led to the A+ product reliability enhancement program which incorporates lot stress screening and testing beyond that which standard product receives.

HERE'S HOW WE DO IT

Quality—the measure of a component's conformance to specification—and reliability—the measure of the component's performance over time—both depend upon the tight control of materials; on precision design and fabrication techniques; and on the perfection of a component's assembly and packaging.

But quality and reliability also depend upon the kind of thorough testing that we do at National Semiconductor.

Using state-of-the-art, automated test equipment and handling methods, we test each and every A+ device under the most extreme conditions in which it might be used. We monitor test results, and feed those results to our special failure-analysis laboratory. And we do it all for only pennies a unit.

WEIGH THE ADVANTAGES

Our A+ program allows you:

- To minimize the need for incoming electrical inspection.
- To eliminate the need for (and cost of) using an independent testing laboratory and purchasing excess inventory to cover expected yield loss.
- A reduction in infant mortality rate.
- A reduction in the cost of reworking boards.
- A reduction in warranty and service costs.

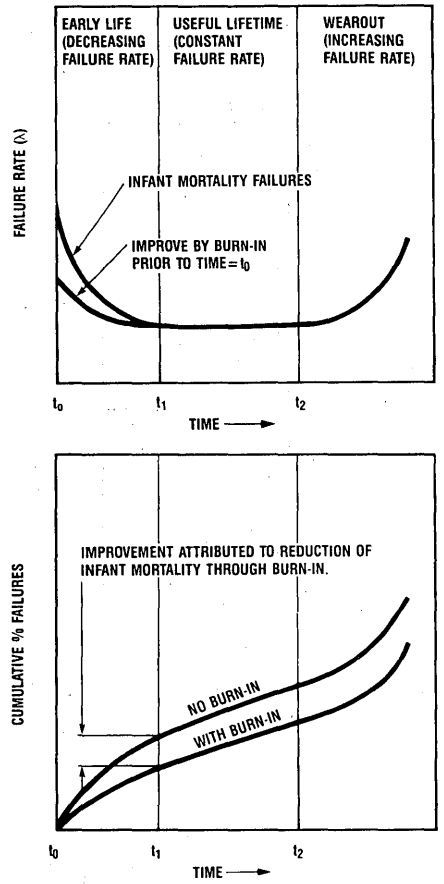
ABOUT A+ PRODUCT ENHANCEMENT

If your business is driven by the need to minimize electrical inspection, to cut down on board rework, and to gain a further reduction in infant mortality rate, National's A+ Product Enhancement is the program you should consider.

A+ incorporates the benefits of the multiple-pass and elevated temperture testing found in the B+ Program, along with an additional test—a combination of increased temperature and applied voltage known as "burn-in"—that in just hours can stress a device to the equivalent of years of normal operation.

The A+ Program gives you:

- High-temperature electrical testing at or above the commercial ambient limit.
- 100% multiple-pass electrical testing.
- A "burn-in" test combining increased temperature with applied voltage.
- Acceptable Quality Levels many times more stringent than the industry norm.



COMPONENT BURN-IN FEATURED IN THE A+ PROGRAM, REDUCES INFANT MORTALITY FAILURES AND TOTAL COMPONENT FAILURES OVER THE LIFE OF YOUR PRODUCTS.

THE A+ FLOW

- SEM: Randomly selected wafers are regularly taken from production and subjected to SEM analysis.
- Assembly and seal: All assembly processes are designed and monitored to produce products of the highest quality and reliability. Molded semiconductors are encapsulated with epoxy B.
- Six hour, 150°C bake. This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, eliminating marginal bonds and insuring an optimum plastic seal.
- Five temperature cycles (0°C to 100°C) based on Mil-STD-883 method 1011, condition A, exercising each device over a 100°C temperature range provides an additional die and package stress.
- Electrical test: Each device is electrically tested prior to submission to burn-in.
- Burn-in: Each device is burned-in for the equivalent of 160 hours at +125°C. The combination of elevated temperature and applied voltages places the die and package under severe stress.
- DC parametric and functional tests: These room temperature and high temperature functional and parametric tests are the comprehensive final tests through which all parts pass and are designed to guarantee compliance to data sheet parameters and functionality over the specified operating range.
- Tightened quality control inspection plans: Each lot is guaranteed to meet the AQL's listed in the following table:

Product Availability

The following MOS Memory Parts are currently available with A+ screening:

HMC2147H	4K NMOS Static RAM
HMC2148H	4K NMOS Static RAM
MM2716	16K NMOS EPROM
NMC27C16	16K CMOS EPROM
NMC27C32	32K CMOS EPROM

At National Semiconductor we turn out more than six million semiconductor products every day, and we build each one to standards that have been called the best in the business.

But if your business requires the benefits associated with additional processing, take a look at the A+ Product Enhancement Program from National Semiconductor.

You'll find a combination of state-of-the-art processing, manufacturing and testing facilities combined with quality and reliability monitoring that provides you with the broadest base of enhanced semiconductor products available in the market.

CALL US ON IT.

If you would like to know more about how our off-the-shelf product enhancement programs can benefit you, give us a call. We'd be happy to show you, in detail, how our A+ Programs can work for you.

When it comes to the many uses of semiconductor technology, National Semiconductor is making the most of a good thing.

MST™ Program
The System Environment Approach to Memory Component Testing

The Memory System Test (MST) program is designed to provide our customers with mainframe memory components that have already been through the test/temperature processing that the user normally implements at the board level.

This program assures memory components of significantly better quality and higher reliability than that achieved by the usual approach to memory component testing. MST processed components have experienced board level environmental testing over the temperature range of 25°C to 70°C.

Specifying MST processing offers you the following:

- Eliminates the need for additional burn-in and testing at independent test laboratories.
- Eliminates inventory throughput time at incoming test or at independent test laboratories.
- Simplifies system checkout and shortens card burn-in/test.
- Reduces board rework.
- Reduces field failures and equipment downtime.
- Provides soft error detection during component processing.
- Provides mobile ion drift detection during component processing.
- Increases reliability.
- Provides parts that have already operated in a system environment within system margins at maximum operating temperature.

The result is you get higher quality at lower cost.

THE MST SCREEN

The screening performed by National for MST products has a very significant improvement over standard product flows done by most dynamic RAM suppliers. National employs a Memory System Test (MST) which is a burn-in oven with added capability for driving components with various test patterns and monitoring component outputs for proper data. Parts are loaded in the MST oven and burned-in. They are then tested in the MST oven immediately after burn-in and are verified to operate properly over an extended test time at high and low temperatures.

MST parts are thus tested in a system environment with thousands of other RAMs operating in close proximity. This test more closely approximates a field environment than does a single insertion test.

Testing the parts in the burn-in chamber immediately following burn-in also weeds out mobile ion problems. During burn-in mobile ions migrate to the silicon-oxide interface where they are most likely to cause failures. Thus a test immediately after burn-in will detect mobile ions in a worst case condition.

The extended test time of MST parts at both high and low temperature will also detect intermittent failures. A single insertion test normally runs a pattern only once, whereas the MST will run all patterns over and over, giving an intermittent problem many opportunities to occur.

The MST also gives absolute knowledge of burn-in. If a part does not make total electrical contact when plugged into the burn-in socket, it will malfunction during MST and be classified as a reject. Thus the electrical stressing as well as the high temperature of burn-in are insured.

The MST screen detects the above possible defects, as well as accomplishing normal burn-in screen. The normal burn-in performs the early life operation at an accelerated rate and weeds out infant mortalities. The MST burn-in is done at 125°C minimum and at voltage levels above nominal for additional stress on the parts.

In addition to the above screening, MST parts are tested at high temperature and room temperature with heavy timing guardbands or critical parameters. Parts are tested with power supply voltages and input drivers guardbanded beyond the data sheet specifications. The parts are also tested to a very tight AQL at outgoing QA. Thus customers using MST products not only profit from excellent long term reliability, but they also experience fewer system incompatibility problems and have negligibly small incoming reject rates.

PRODUCT AVAILABILITY

National has shipped millions of MST screened parts and the program has been well received in the industry. Many users have seen board problems disappear and reject rates decrease by an order of magnitude after converting to MST.

All NMOS dynamic RAMs that National builds are available with MST screen.

OPERATING LIFE TEST RESULTS

The Biased Life Test at accelerated temperatures is the principal method of evaluating microcircuit reliability. This method is particularly useful because it provides a means of accelerating time-to-failure of temperature-sensitive failure mechanisms. By this method small sample tests can be used to predict actual field performance of the product lots sampled.

The nature of the operating stress selected differs for each unique circuit. Elevated ambient temperatures are used to accelerate thermally sensitive failure mechanisms. Voltage bias conditions are selected to approximate best the system bias conditions in normal design applications. Acceleration of bias or current stresses is not attempted.

Test ambient temperatures are selected to assure that junction temperatures do not exceed the critical molded thermal-expansion transition temperature of 140°C for Epoxy-B materials.

FAILURE RATE TREND AT $T_J \leq 140°C$

If a Weibul plot of failure-times were made, the Weibul parameter estimation of the rate of reliability improvement with life test (β) would be approximately equal to 0.50. The Weibul function is one which is commonly used to describe mathematically the failure rate of a solid state device as a function of time. It is also known as the Type III Extreme Value Distribution. Its probability density function may then be shown to be:

$$f(\tau-\gamma)=\frac{\beta}{\alpha}(\tau-\gamma)^{\beta-1}e^{-\left(\frac{\tau-\gamma}{\alpha}\right)}$$

γ (the location parameter) is assumed to be equal to 0 hours. β is the key parameter estimator for this product and may be used to tell when a failure rate is constant, increasing, or decreasing. In this instance, because the estimated value of β is less than 1.0, the interpretation is that the basic failure rate for these products improves with time.

A second approach to estimating failure distributions is to use the log-normal distribution. Using information from current product tests, Figure 1 was constructed to assist in estimating the effectivity of various burn-in time periods (based on 1,000-hour test results) by taking all failures occuring within 1,000 hours and plotting them as a normal density function with respect to the log of time. In Figure 1, the statistical fit with observed data is good. In that figure it is estimated that one-fourth of all failures occured within the first 70 hours of testing.

ESTIMATION OF USE-CONDITION FAILURE RATE

All National products are subjected to ongoing reliability evaluations. These evaluations employ various accelerated life tests, including dynamic high-temperature operating life, temperature-humidity life, temperature cycling, and thermal shock. A guide to the use of these tests in estimating equipment reliability is provided by accelerated life testing. The following discussion analyzes the effects of temperature and the use of the Arrhenius failure rate model in estimating failure rates at other temperatures.

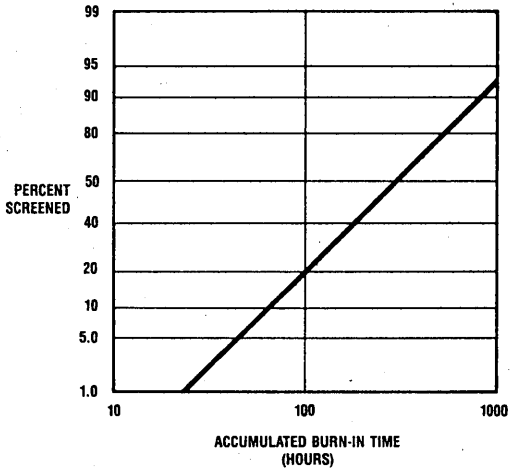
THE ARRHENIUS MODEL

The time and temperature dependence of virtually all long-term semiconductor failure mechanisms is a well established fact. The occurrence of this failure dependency can be represented by the Arrhenius Model. This model includes the effect of temperature and activation energy of the failure mechanism, permitting it to be used to characterize failure modes and predict reliability at normal operating temperatures based on tests performed at above-normal device junction temperatures.

Originally developed in the 1880s to describe chemical reaction rates, the Arrhenius Model was adapted to accelerated life testing for logical reasons. Faced with the critical need for full validation of accelerated life test data, researchers easily theorized that chemical processes were the cause of degradation of electronic parts. And, since temperature was commonly used in

SCREENING EFFICIENCY OF BURN-IN
PLOTS PERCENT OF LIFE TEST FAILURES EXPECTED TO BE SCREENED vs TIME ON BURN-IN

FIGURE 1. Screening Efficiency of Burn-In



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accelerated testing, the Arrhenius Model was applied and found to fit the data. The model was subsequently validated by years of reliability testing and found to be both a valuable design tool and a useful adjunct to the state of the art of accelerated life testing technology.

As applied to accelerated life testing of semiconductors, the Arrhenius Model assumes that degradation of a performance parameter is linear with time, with the MTBF a function of the temperature stress. The temperature dependence is taken to be the exponential function that defines the probability of occurrence, resulting in the following formula for defining the lifetime or MTBF at a given temperature stress level when knowing the MTBF at a second temperature stress level.

$$t_1 = t_2 \exp \frac{E}{K}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)$$

where: t_1 = MTBF at junction temperature T_1
t_2 = MTBF at junction temperature T_2
T = Junction temperature in °K (absolute)
E = Thermal activation energy in electron volts (eV)
K = Boltzman's constant (8.617×10^{-5} eV/°K)

Given the temperature and failure rate for a specific reliability test, the remaining unknown is the activation energy E. The value for E can be arrived at through experimentation or by assumption of the validity of the historical data.

The activation energy serves as a convenient means of characterizing the failure mechanisms. If the activation energy is known, or can be estimated, the acceleration factor can be determined, allowing field failure rate and useful life to be calculated from the accelerated life tests.

In calculating the field reliability of a semiconductor device, it is first necessary to calculate the junction temperature both for the reliability test and for actual field operating conditions. In general, the junction temperature will depend on the ambient temperature, cooling, package type, operating cycle times, supply voltage and current. In these terms, the junction temperature T_j is given as:

$$T_j = T_A + (I_{CC} \times V_{CC})(A_f)(JA)$$

where: T_j = Junction temperature
T_A = Ambient temperature
I_{CC} = Supply current
V_{CC} = Supply voltage
A_f = Air flow factor (0.75)
JA = Package thermal resistance

Now by estimating the failure rate at test temperature, converting the test temperature and use condition temperature to absolute temperatures (°K = °C + 273°), and by assuming an activation energy, the use condition failure rate can be estimated. This is the procedure performed in estimating the failure rates where the value for the activation energy was selected as 0.7eV.

TEMPERATURE AND HUMIDITY BIASED TEST RESULTS

For molded products, the most important test used to evaluate package resistance to external moisture contaminants has been the DC-biased low-power life test conducted in an ambient temperature of 85°C, with relative humidity constant at 85%. In this test, the package is placed in a chamber specially designed to assure that the density of water vapor in the vicinity of the device under test is constant for the duration of the test. By this means, comparing the respective rates of failure in humid and dry environments gives an indication of the permissivity of the package.

The principal failure mechanism expected to be induced by this "85/85" test is corrosion or one of its ancillary effects. However this test is most effective because it will also measure the long term potential for failure due to other failure mechanisms as well. Some other potential failure mechanisms include those induced by bias and temperature alone, by moisture induced changes in surface states resulting in changed electrical performance characteristics, and by those environmental stresses on package materials. Each such failure mechanism will have distinct failure characteristics that are a function of time on test. Each has its own characteristic probability density function.

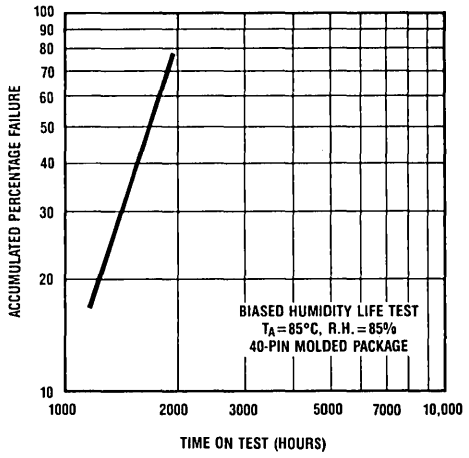
Numerous techniques are used to predict the acceleration of the failure mechanisms by stressing at $T_A = 85°C$ and RH = 85% under bias. While each technique arrives at the same general conclusions (i.e., the epoxy package is fully able to withstand normal earth-level environments such as those found in the vicinity of the Panama Canal), little agreement has yet been reached as to the exact method of extrapolation. National Semiconductor uses standard methods of calculating failure rates for 1,000 hours of testing, and combines temperature and relative humidity as independent variables in the reliability equation. Prediction of extrapolated failure-acceleration factors using this model then becomes the product of the estimated acceleration which is due to temperature times the estimated acceleration which is due to relative humidity.

TIME TO MEDIAN FAILURE

When time to median failure is of concern, this factor can be treated similarly.

Using the acceleration factor 208X provided by in-house experiments for correlation with $T_A = 30°C$ and RH = 85%, and recognizing an average internal system ambient temperature rise of 10°C, the time median failure is increased to 38.0 years. The ambient conditions of 30°C and 85% RH are seldom realized on an annual average basis in actual use conditions; except in those places with extreme climates, a more reasonable assumption of the annual average environment would be 30°C ambient temperature and 50% relative humidity. Under these more normal conditions, the time to median failure increases another 7 X.

FIGURE 2. Biased Humidity Life Test Summary



STORAGE LIFE TEST RESULTS

Storage at a maximum rated condition has long been used to test for atmospheric and chemical contaminants which are accelerated by temperature alone, and which can adversely affect microcircuit performance. The significance of this test has diminished as surface passivation technology has matured and as internal atmospheric control within hermetically sealed devices has effectively removed active ions from the die's presence. Its role for molded DIPs has been reduced to that of a test control only.

AUTOCLAVE OR "PRESSURE COOKER" TEST RESULTS

The autoclave test is performed as an accelerated moisture-resistance test for molded microcircuit packages. As the words "pressure cooker" imply, the test samples are supported above a well of water in a saturated atmosphere at an ambient temperature of approximately 121°C. At this temperature, two absolute atmospheres of pressure (1520 mm Hg) are maintained in the vessel, and the saturated water vapor density is 1.144 kg/m^3. While maintaining the relative humidity at 100%, the thermal activity of the water molecules is increased significantly, thus increasing the saturated water vapor pressure ninety-six times the normal 0.02156 kg/cm^2 at 30°C and 50% RH, or to 2.066 kg/cm^2 at 121°C, 100% RH.

It is this increased activity and density of the water molecules that provide the storage acceleration for this test. As in the "85/85" test, failure comes as a result of corrosion or its by-products.

TEMPERATURE CYCLING TEST RESULTS

Temperture cycling tests the thermal compatibility of the materials and metal used to make a microcircuit. In testing molded packages, a 2,000 cycle "fatigue" test is conducted to assure not only initial thermal compatibility, but comparative thermal compatibility throughout the life of the circuit.

Each cycle consists of a minimum of 10 minutes at the high temperature (T_A = 125°C), immediately followed by 10 minutes at the low temperature (T_A = 0°C). This cycling is repeated 2,000 times, with intermediate readings taken at the 1,000-cycle point.

Section 10

Physical Dimensions

10

PACKAGES

Dual-In-Line Packages

(N) Devices ordered with "N" suffix are supplied in plastic molded dual-in-line packages. Molding material is a highly reliable compound suitable for military as well as commercial temperature range applications. Lead material is copper or alloy 42 with a hot solder dipped surface to allow ease of solderability.

(J) Devices ordered with the "J" suffix are supplied in a CERDIP package (ceramic lid and base sealed with high temperature vitreous glass). Lead material is solder dipped alloy 42.

(D) Devices ordered with the "D" suffix are supplied in side brazed, multi-layer, ceramic dual-in-line packages. The leads are Kovar or alloy 42 and either tin-plated, gold-plated, or solder-plated.

(Q) Devices ordered with the "Q" suffix are supplied in either a "D" or "J" package, but with a UV window.

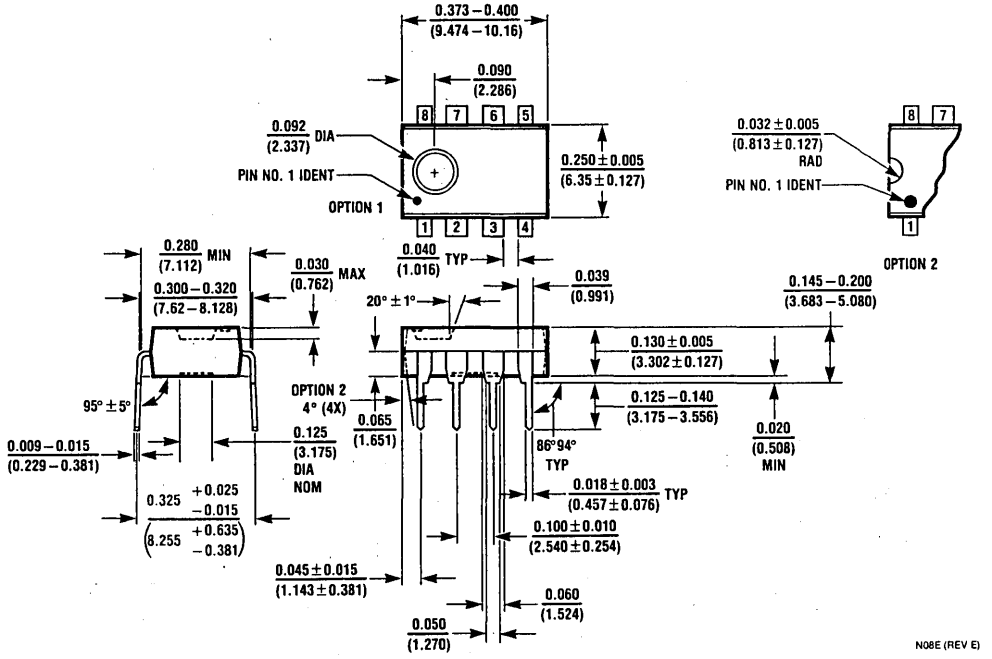
Metal Can Packages

(H) Devices ordered with the "H" suffix are supplied in a metal can package. The cap is nickel finish and the leads are gold-plated Kovar. Gold free construction using epoxy D/A is also available, with a tin-plated finish.

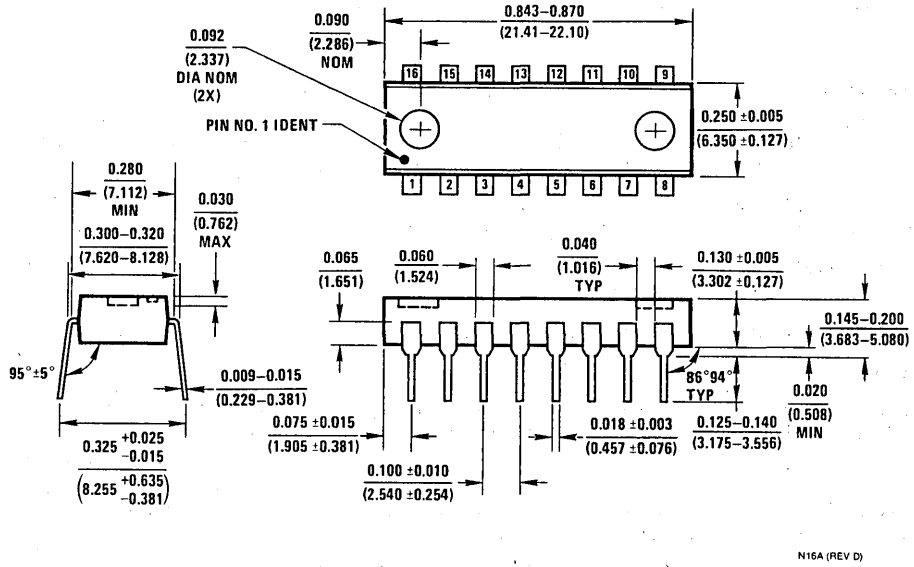
Flat Packages

(F) Devices ordered with the "F" suffix are supplied in a multi-layer, ceramic bottom brazed flat package. The lid is plated alloy 42, and leads are gold-plated, tin-plated, or solder-plated alloy 42 or Kovar.

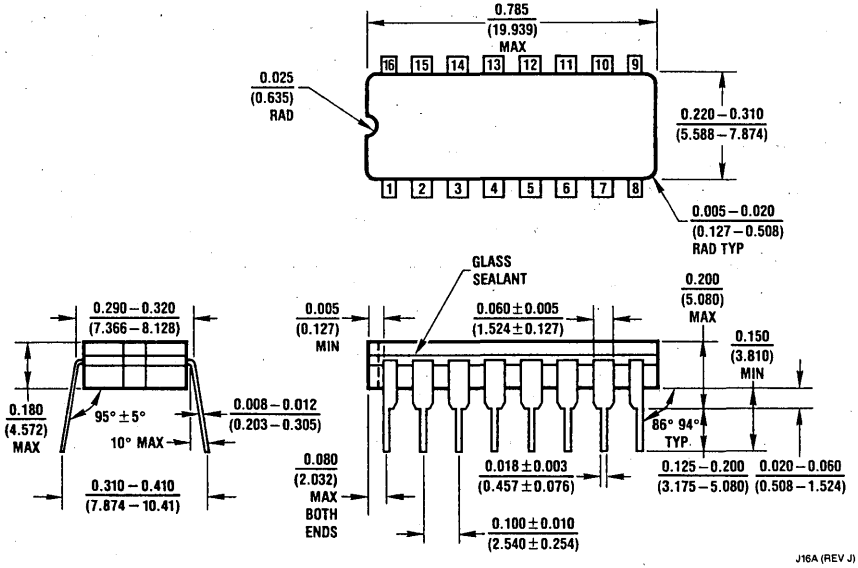
(W) Devices ordered with the "W" suffix are supplied in a low-temperature ceramic flat package.



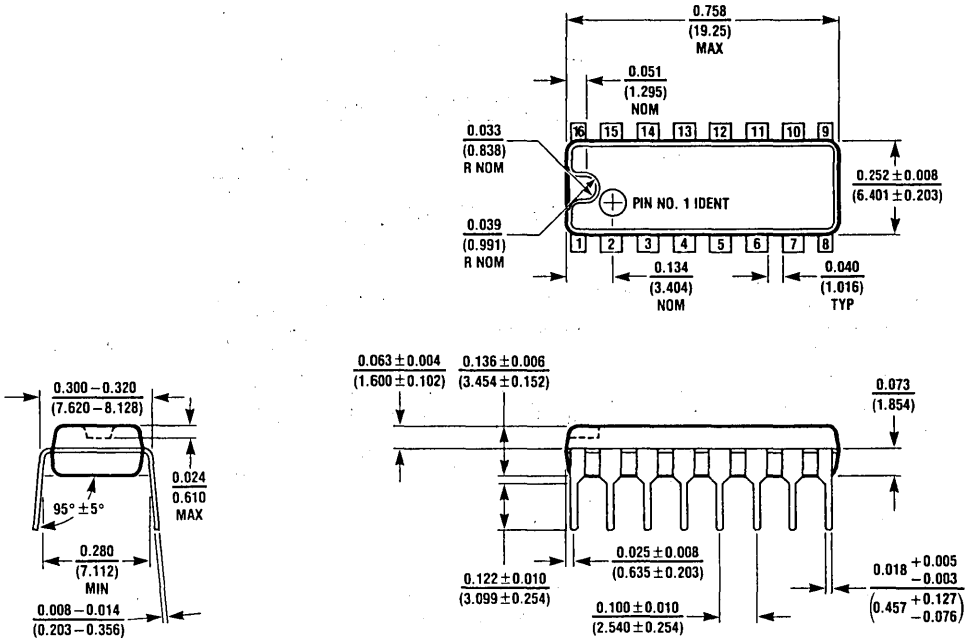
NS Package N08E
8-Lead Molded DIP (N)



NS Package N16A
16-Lead Molded DIP (N)

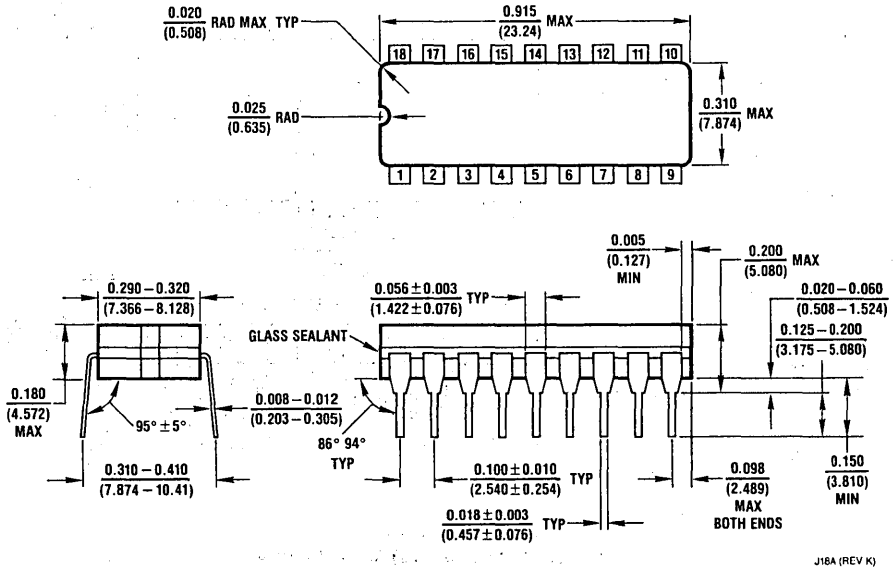


NS Package J16A
16-Lead Cerdip (J)



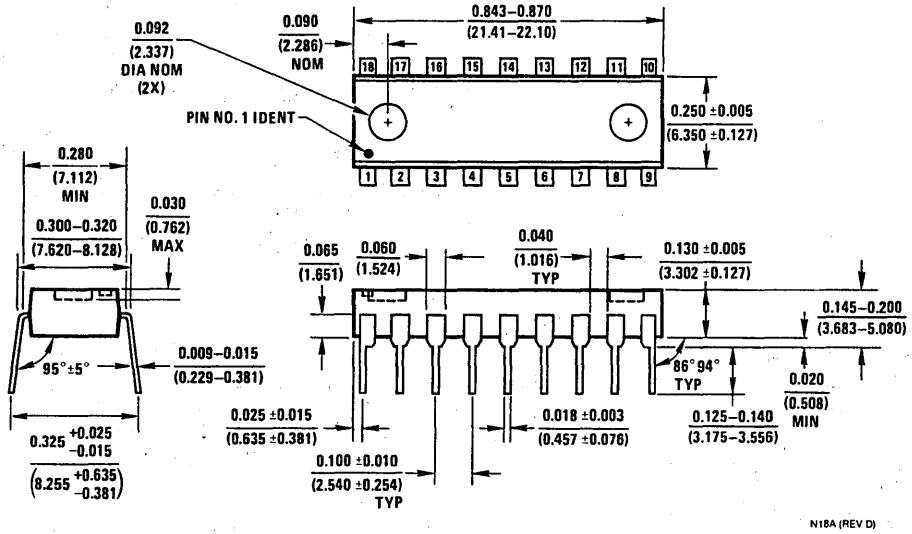
NS Package N16F
16-Lead Molded DIP (N)

N16F (REV C)

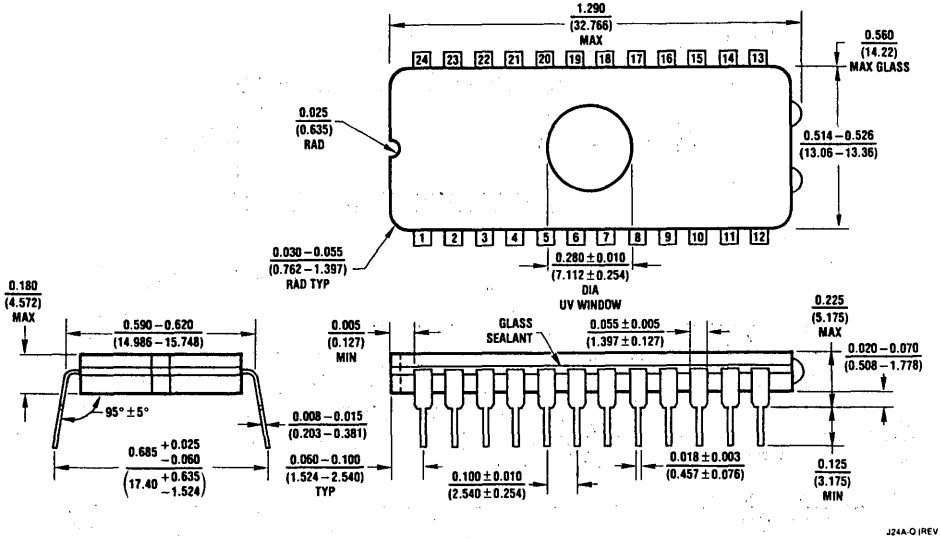


J18A (REV K)

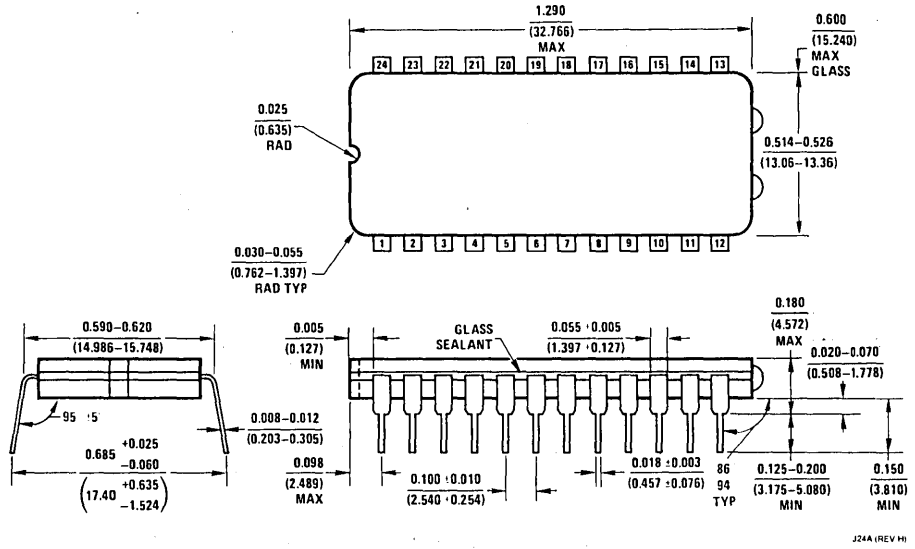
NS Package J18A
18-Lead Cerdip (J)



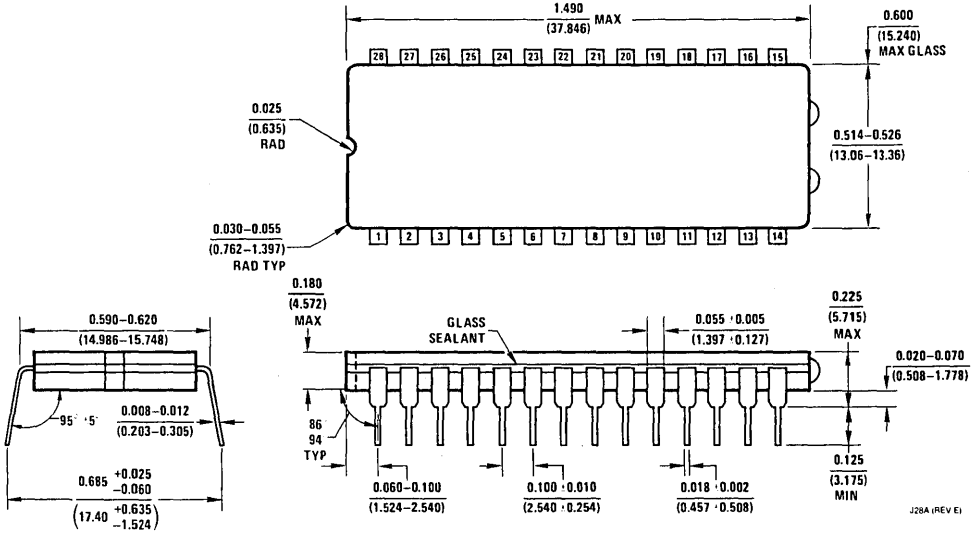
NS Package N18A
18-Lead Molded DIP (N)



NS Package J24A-Q
24-Lead EPROM Cerdip (JQ) Small Window

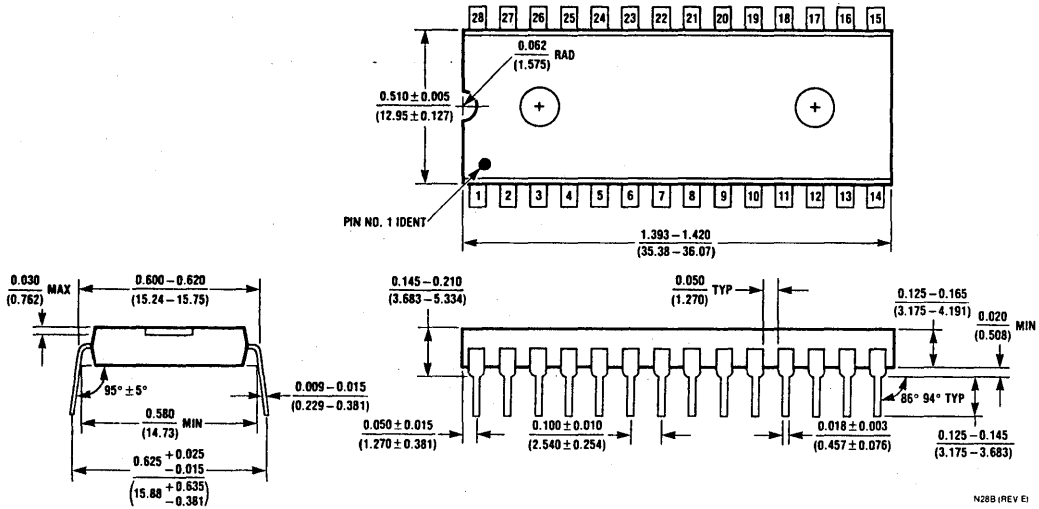


NS Package J24A
24-Lead Cerdip (J)



NS Package J28A
28-Lead Cerdip (J)

10



NS Package N28B
28-Lead Molded DIP (N)

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