400050

National Semiconductor Corporation

LS/S/TTL Logic Databook

For information on Advanced Schottky and Advanced Low Power Schottky devices see the ALS/AS Logic databook.

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Table of Contents

Section 1—Introduction to Bipolar Logic

Section 2—Low Power Schottky

Arithmetic Functions

Buffers/Drivers

Comparators

Counters

Table of Contents (Continued)

Table of Contents (Continued)

Section 3—Schottky

Table of Contents (Continued)

Table of Contents (Continued)

Table of Contents (Continued)

Table of Contents (Continued)

Section 5—Low Power

Counters

Flip-Flops

Gates/Inverters

Registers

Section 6—Appendices/Physical Dimensions

Alpha-Numeric Index

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

Alpha-Numeric Index (Continued)

Section 1

Introduction to Bipolar Logic

Section 1 Contents

Guide to Bipolar Logic Device Families

Since the introduction of the first saturating logic bipolar integrated circuit family (DM54/DM74), there have been many developments in the process and manufacturing technologies as well as circuit design techniques which have produced new generations (families) of bipolar logic devices. Each generation had advantages and disadvantages over the previous generations. Today National provides six bipolar logic families.

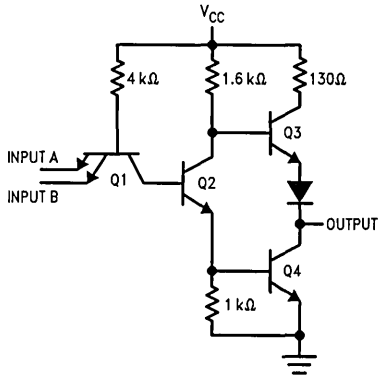
TTL	(DM54/DM74)
Low Power	(DM54L/DM74L)
Low Power Schottky	(DM54LS/DM74LS)
Advanced Low Power Schottky	(DM54ALS/DM74ALS)
Schottky	(DM54S/DM74S)
Advanced Schottky	(DM54AS/DM74AS)

TTL LOGIC (DM54/DM74)

TTL logic was the first saturating logic integrated circuit family introduced, thus setting the standard for all the future families. It offers a combination of speed, power consumption, output source and sink capabilities suitable for most applications. This family offers the greatest variety of logic functions. The basic gate (see *Figure 1*) features a multiple-emitter input configuration for fast switching speeds, active pull-up output to provide a low driving source impedance which also improves noise margin and device speed. Typical device power dissipation is 10 mW per gate and the typical propagation delay is 10 ns when driving a 15 pF/400Ω load.

LOW POWER (DM54L/DM74L)

The low power family has essentially the same circuit configuration as the TTL devices. The resistor values, however, are increased by nearly tenfold, which results in tremendous reduction of power dissipation to less than $1/10$ of the TTL family. Because of this reduction of power, the device speed is sacrificed. The propagation delays are increased threefold. These devices have a typical power dissipation of 1 mW per gate and typical propagation delay of 33 ns, making this family ideal for applications where power consumption and heat dissipation are the critical parameters.



TL/F/5534–1

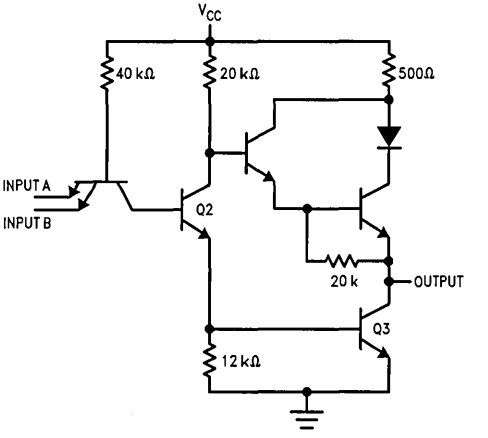
FIGURE 1. DM5400/DM7400

LOW POWER SCHOTTKY (DM54LS/DM74LS)

The low power Schottky family features a combined fivefold reduction in current and power when compared to the TTL family. Gold doping commonly used in the TTL devices reduces switching times at the expense of current gain. The LS process overcomes this limitation by using a surface barrier diode (Schottky diode) in the baker clamp configuration between the base and collector junction of the transistor. In this way, the transistor is never fully saturated and recovers quickly when base drive is interrupted. Using shallower diffusion and soft-saturating Schottky diode clamped transistors, higher current gains and faster turn-on times are obtained. The LS circuits do not use the multi-emitter inputs. They use diode-transistor inputs which are faster and give increased input breakdown voltage; the input threshold is ~0.1V lower than TTL. Another commonly used input is the vertical substrate PNP transistor. In addition to fast switching, it exhibits very high impedance at both the high and low input states, and the transistor's current gain (β) significantly reduces input loading and provides better output performance. The output structure is also modified with a Darlington transistor pair to increase speed and improve drive capability. An active pull-down transistor (Q3) is incorporated to yield a symmetrical transfer characteristic (squaring network). This family achieves circuit performance exceeding the standard TTL family at fractions of its power consumption. The typical device power dissipation is 2 mW per gate and typical propagation delay is 10 ns while driving a 15 pF/2 kΩ load.

SCHOTTKY (DM54S/DM74S)

This family features the high switching speed of unsaturated bipolar emitter-coupled logic, but consumes more power than standard TTL devices. To achieve this high speed, the Schottky barrier diode is incorporated as a clamp to divert the excess base current and to prevent the transistor from reaching deep saturation. The Schottky gate input and inter-



TL/F/5534–2

FIGURE 2. DM54L00/DM74L00

nal circuitry resemble the standard TTL gate except the resistor values are about one-half the TTL value. The output section has a Darlington transistor pair for pull-up and an active pull-down squaring network. This family has power dissipation of 20 mW per gate and propagation delays three times as fast as TTL devices with the average time of 3 ns while driving 15 pF/280Ω load.

ADVANCED LOW POWER SCHOTTKY (DM54ALS/DM74ALS)

The advanced low power Schottky family is one of the most advanced TTL families. It delivers twice the data handling efficiency and still provides up to 50% reduction in power consumption compared to the LS family. This is possible because of a new fabrication process where components are isolated by a selectively grown thick-oxide rather than the P-N junction used in conventional processes. This refined process, coupled with improved circuit design techniques, yields smaller component geometries, shallower diffusions, and lower junction capacitances. This enables the devices to have increased f_T in excess of 5 GHz and improved switching speeds by a factor of two, while offering much lower operating currents.

In addition to the pin-to-pin compatibility of the ALS family, a large number of MSI and LSI functions are introduced in the high density 24-pin 300 mil DIP. These devices offer the designers greater cost effectiveness with the advantages of reduced component count, reduced circuit board real-estate, increased functional capabilities per device and improved speed-power perfomance.

The basic ALS gate schematic is quite similar to the LS gate. It consists of either the PNP transistor or the diode inputs, Darlington transistor pair pull-up and active pull-down (squaring network) at the output. Since the shallower diffusions and thinner oxides will cause ALS devices to be more susceptible to damage from electro-static discharge, additional protection via a base-emitter shorted transistor is included at the input for rapid discharge of high voltage static electricity. Furthermore, the inputs and outputs are clamped by Schottky diodes to prevent them from swinging excessively below ground level. A buried N^+ guard ring around all input and output structures prevents crosstalk. The ALS family has a typical power dissipation of 1 mW per gate and typical propagation delay time of 4 ns into a 50 pF/2 kΩ load.

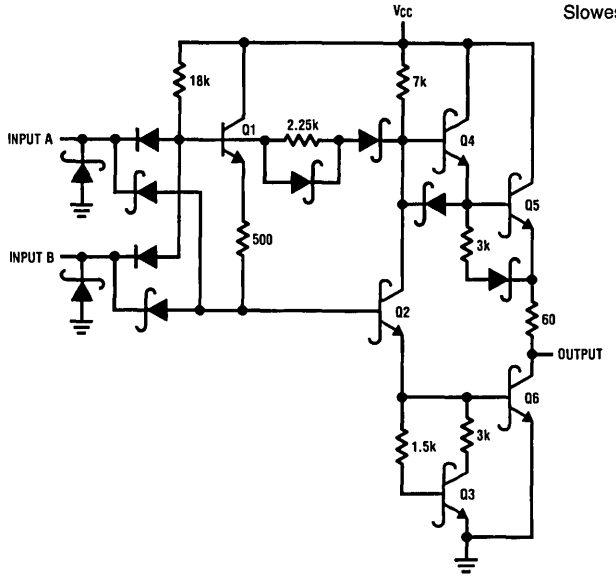
ADVANCED SCHOTTKY (DM54AS/DM74AS)

This family of devices is designed to meet the needs of the system designers who require the ultimate in speed. Utilizing Schottky barrier diode clamped transistors with shallower diffusions and advanced oxide-isolation fabrication techniques, the AS family achieves the fastest propagation delay that bipolar technology can offer. The AS family has virtually the same circuit configuration as the ALS family. It has PNP transistor or diode inputs with electrostatic protection base-emitter shorted transistors. The output totem-pole consists of a Darlington pair transistor pull-up and an active pull-down squaring network. The inputs and outputs are Schottky clamped to attenuate critical transmission line reflections. In addition, the circuit contains the "Miller Killer" network at the output section to improve output rise time and reduce power consumption during switching at high repetition rates. The AS family yields typical power dissipation of 7 mW per gate and propagation delay time of 1.5 ns when driving a 50 pF/2 kΩ load.

SELECTING A FAMILY

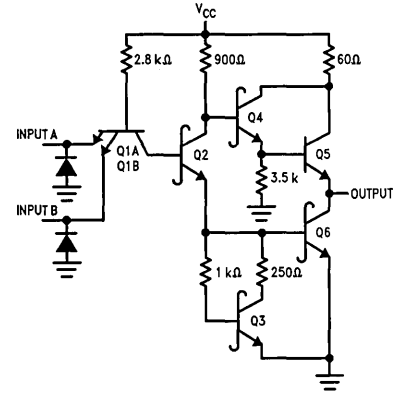
Two factors shoud be considered when choosing a logic family for application, speed and power consumption. New logic families were created to improve the speed or lower the power consumption of the previous families. The following tables rate each family.

Speed		Power Consumption	
Fastest	AS	Low	L
	S		ALS
	ALS		LS
↓	LS	↓	AS
	TTL		TTL
Slowest	L	High	S



TL/F/5534–3

FIGURE 3. DM54LS00/DM74LS00



TL/F/5534–4

FIGURE 4. DM54S00/DM74S00

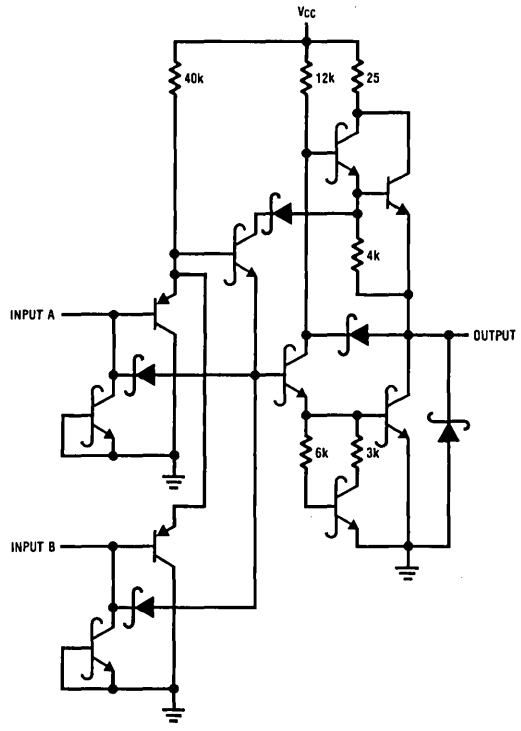


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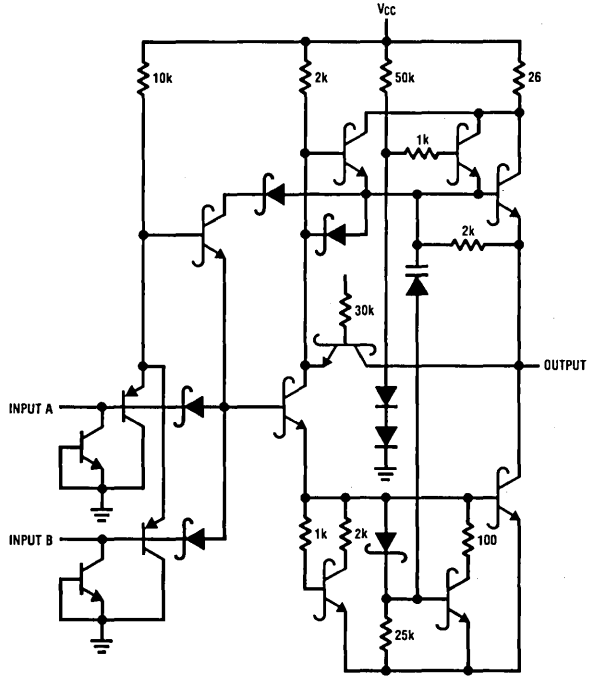
FIGURE 5. DM54ALS00/DM74ALS00



TL/F/5534–6

FIGURE 6. DM54AS00/DM74AS00

Bipolar Logic Family Electrical Characteristics Over Operating Temperatures

		TTL	L-TTL	LS	ALS	S	AS	Units
DM5400/DM7400								
2-Input NAND	t_{PLH}*	11	35	8	4	3	2.5	ns
	t_{PHL}*	7	31	8	4	3	1.5	ns
	t_r*	12	66	13	10	6	5	ns
	t_r*	5	30	3	6	3	3	ns
	I_{OH}	−400	−200	−400	−400	−1000	−2000	μA
Mil/Com	I_{OL}	16	2/3.6	4/8	4/8	20	20	mA
	I_{IH}	40	10	20	20	50	20	μA
	I_{IL}	−1.6	−0.18	−0.36	−0.20	−2	−0.50	mA
Min	I_{OS}	−20	−3	−20	−30	−40	−30	mA
Max	I_{OS}	−100	−15	−100	−112	−100	−112	mA
	I_{CCH}	8	0.8	1.6	0.85	16	3.2	mA
	I_{CCL}	22	2.04	4.4	3.0	36	16.1	mA
Mil	V_{OH}	2.4	2.4	2.5	$V_{CC}-2$	2.5	$V_{CC}-2$	V
Com	V_{OH}	2.4	2.4	2.7	$V_{CC}-2$	2.7	$V_{CC}-2$	V
Mil	V_{OL}	0.4	0.3	0.4	0.4	0.5	0.5	V
Com	V_{OL}	0.4	0.4	0.5	0.5	0.5	0.5	V
	V_{IH}	2	2	2	2	2	2	V
Mil	V_{IL}	0.8	0.7	0.7	0.8	0.8	0.8	V
Com	V_{IL}	0.8	0.7	0.8	0.8	0.8	0.8	V
	V_I	−1.5	N/A	−1.5	−1.5	−1.2	−1.2	V
Mil	NM-H	400	400	500	500	500	500	mV
Com	NM-H	400	400	700	700	700	700	mV
Mil	NM-L	400	400	300	400	400	300	mV
Com	NM-L	400	300	300	300	300	300	mV
Gate Power x Delay Product		100	20	20	4	60	30	pj
DM5474/DM7474								
D Flip-Flop	t_{PLH}*	14	50	17	5	8	6	ns
(CLK to Q)	t_{PHL}*	20	60	22	8	9	6	ns
(PS or	t_{PLH}*	14	40	17	7	6	4.5	ns
CLR to Q)	t_{PHL}*	20	60	22	10	12	6	ns
(CLK HI)	t_W	30	75	25	12	8	4	ns
(PS or CLR LOW)	t_W	30	75	20	15	9	4	ns
	t_{SET-UP}	20	50	25	15	3	3/2	ns
	t_{HOLD}	5	15	0	0	2	2/1	ns
	t_r*	13	64	9	17	4	5	ns
	t_r*	6	19	6	9	3	3	ns
	f_{MAX}*	25	11	33	34	95	125	MHz
	I_{OH}	−400	−200	−400	−400	−1000	−2000	μA
Mil/Com	I_{OL}	16	2/3.6	4/8	4/8	20	20	mA
(CLK/D)	I_{IH}	80/40	20/10	20	20	100/50	20	μA
(PS/CLR)	I_{IH}	40/120	20/30	40	40	100/150	40	μA
(CLK/D)	I_{IL}	−3.2/−1.6	−0.36/−0.18	−0.4	−0.2	−4/−2	−0.5	mA
(PS/CLR)	I_{IL}	−1.6/−3.2	−0.18/−0.36	−0.8	−0.4	−4/−6	−1.0	mA

Bipolar Logic Family Electrical Characteristics Over Operating Temperatures (Continued)

		TTL	L-TTL	LS	ALS	S	AS	Units
DM5474/DM7474 (Continued)								
Min	I_{OS}	−20/−18	−3	−20	−30	−40	−30	mA
Max	I_{OS}	−55	−15	−100	−112	−100	−112	mA
	I_{CC}	15	3	8	4	50	16	mA
Mil	V_{OH}	2.4	2.4	2.5	$V_{CC}-2$	2.5	$V_{CC}-2$	V
Com	V_{OH}	2.4	2.4	2.7	$V_{CC}-2$	2.7	$V_{CC}-2$	V
Mil	V_{OL}	0.4	0.3	0.4	0.4	0.5	0.5	V
Com	V_{OL}	0.4	0.4	0.5	0.5	0.5	0.5	V
	V_{IH}	2	2	2	2	2	2	V
Mil/Com	V_{IL}	0.8	0.7	0.7/0.8	0.8	0.8	0.8	V
	V_I	−1.5	N/A	−1.5	−1.5	−1.2	−1.2	V
Mil	NM-H	400	400	500	500	500	500	mV
Com	NM-H	400	400	700	700	700	700	mV
Mil	NM-L	400	400	400	400	300	300	mV
Com	NM-L	400	300	300	300	300	300	mV

Note: See Test Waveforms in this section for loading conditions, t_r and t_f are measured from 10% to 90% of waveform.

Note: NM-H is noise margin high. NM-L is noise margin low.

*Typical values. Other values are limit values.

Bipolar Logic Family Output Source/Sink Capability: 54/74 Families

Output			TTL	L-TTL	LS	ALS	S	AS	Units
Standard	Mil	I_{OH}	−0.4	−0.2	−0.4	−0.4	−1	−2	mA
	Com		−0.4	−0.2	−0.4	−0.4	−1	−2	mA
	Mil	I_{OL}	16	2	4	4	20	20	mA
	Com		16	3.6	8	8	20	20	mA
Buffered	Mil	I_{OH}	−0.8	−0.2	−0.4	−1	−1	−12	mA
	Com		−0.8	−0.2	−0.4	−2.6	−1	−15	mA
	Mil	I_{OL}	16	2	4	12	20	32	mA
	Com		16	3.6	8	24	20	48	mA
Bus Driver	Mil	I_{OH}	−2	N/A	−1	−12	−2	−48	mA
	Com		−5.2	N/A	−2.6	−15	−6.5	−48	mA
	Mil	I_{OL}	32	N/A	12	12	20	40	mA
	Com		32	N/A	24	24-48	20	48	mA

Fan-In and Fan-Out

	TTL	L-TTL	LS	ALS	S	AS	Units
Input Load: high	1	0.25	0.5	0.5	1.25	0.5	U.L.
Low	1	0.1125	0.225	0.125	1.25	0.3125	U.L.
Output Drive: High	10	2.25	5	5	12.5	12.5	U.L.
Low	10	5	10	10	25	50	U.L.

Note: UNIT LOAD (U.L.) Standard is referenced with respect to standard TTL device loading. It is defined as:

1 U.L. = 40 μA (HIGH STATE)

1 U.L. = 1.6 mA (LOW STATE)

IC Device Testing

Understanding the intent and practice of IC device testing is vital to insuring both the quality and proper usage of integrated circuits. All National Semiconductor data sheets list the AC and DC parameters with min and/or max limits, along with forcing functions. Understanding when a part fails the limit, and which forcing functions are really tighter, is critical when determining if an IC device is good or bad.

All of National's databook parameters are defined and guaranteed for "worst-case testing." Input loading currents (fan-in) are tested at the input and V_{CC} levels that most increase that loading, while the output drive capability (fan-out) is tested at the input and V_{CC} levels that most decrease that capability. I_{CC} is tested with the input conditions and V_{CC} level that yield the greatest I_{CC} value, and V_{CLAMP} is tested such that the negative voltage is maximized for the given clamp current. The fan-in and fan-out specs are contained in the I_{IH}, I_{OH}, I_{IL} and I_{OL} values. To guarantee these fan-in and fan-out limits at 10, the I_{OL} must be at least 10 times the I_{IL} and the I_{OH} must be at least 10 times the I_{IH}. Be aware that the fan-in and fan-out specifications are valid only within a given device family. The standard input loading and output drives are shown in Table I.

Notice that the I_{OL} is at least 10 times the I_{IL} and that the I_{OH} is greater than 10 times the I_{IH}. Also notice that these are "standard" drive and load currents for single sink outputs and inputs. Certain devices may have multiple load inputs where the input line goes to several input structures and has, say, 2 or 3 times the normal I_{IL} and I_{IH} loading. Certain other devices will have "triple sink" outputs that can drive 3 times the standard I_{OL} and I_{OH} currents. These devices are generally bus drivers, or drivers intended to drive highly capacitive loads. Finally, there are certain devices that have PNP inputs that reduce the I_{IL} loading to typically $-200\ \mu A$, thus allowing an increased DC fan-in of 20. One must therefore be careful when interfacing many different types of devices, even in the same family, and not simply go the "fan-out of 10" rule.

When dealing with any kind of device specification, it is important to note that there exists a *pair* of test conditions that define that test: the forcing function and the limit. Forcing functions appear under the column labeled "Conditions" and define the external operating constraints placed upon the device tested. The actual test limit defines how well the device responds to these constraints. For example, take the parameter $V_{OH(min)}$ for the DM74LS00. It is tested at $V_{CC(min)} = 4.75V$ commercial, using an $I_{OH} = -400\ \mu A$. If we required an $I_{OH} = -800\ \mu A$, this would be a "tighter" test, as the output voltage drops with increased I_{OH}. Hence, a device that would pass the $-800\ \mu A$ I_{OH} would also pass the $-400\ \mu A$ I_{OH}, but not necessarily the other way around. Futhermore, V_{OH} tracks with V_{CC}, which is why $V_{CC(min)}$ is the worst-case testing, and not $V_{CC(max)}$. Finally, forcing inputs to threshold represents the most difficult testing because this puts those inputs as close as possible to the actual switching point and guarantees that the device will meet the V_{IH}/V_{IL} spec.

TABLE I. Fan-In/Fan-Out

Device Family	Input Loading	Output Drive
TTL	$I_{IL} = -1.6$ mA $I_{IH} = 40\ \mu A$	$I_{OL} = 16$ mA $I_{OH} = -400\ \mu A$
Low Power Schottky	$I_{IL} = -400\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 4$ mA (Mil) $I_{OL} = 8$ mA (Com) $I_{OH} = -400\ \mu A$
Advanced Low Power Schottky	$I_{IL} = -100\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 4$ mA (Mil) $I_{OL} = 8$ mA (Com) $I_{OH} = -400\ \mu A$
Schottky	$I_{IL} = -2$ mA $I_{IH} = 50\ \mu A$	$I_{OL} = 20$ mA $I_{OH} = -1$ mA
Advanced Schottky	$I_{IL} = -500\ \mu A$ $I_{IH} = 20\ \mu A$	$I_{OL} = 20$ mA $I_{OH} = -2$ mA
Low Power	$I_{IL} = -180\ \mu A$ $I_{IH} = 10\ \mu A$	$I_{OL} = 2$ mA (Mil) $I_{OL} = 3.6$ mA (Com) $I_{OH} = -200\ \mu A$

Tables II and III show the "direction" of the looser/tighter testing for most common DC parameters. Notice that one can tighten either the forcing function or the limit, or both. Tightening either one is sufficient to insure a tighter test. Also notice the difference between max and min limits. For I_{OS} (double-ended limits), even though −20 mA is more positive than −100 mA, and is mathematically the max limit, the magnitude of the number is the determining factor when deciding which is the max limit. The negative sign simply implies the direction that the current is going, with a negative current leaving the device, and a positive current entering the device. Table II shows the direction of tighter forcing functions, while Table III shows the direction of tighter limits.

TABLE II. Looser/Tighter Forcing Functions Example: DM74LS00

Condition	Test	Looser	Nominal	Tighter	Units
I_{IK}	V_{IK}	−17	−18	−19	mA
I_{OH}	V_{OH}	−350	−400	−450	μA
I_{OL}	V_{OL}	3	4	5	mA
V_I	I_I	6.5	7	7.5	V
V_{IH}	I_{IH}	2.6	2.7	2.8	V
V_{IL}	I_{IL}	0.5	0.4	0.3	V
V_O	I_{OS}	0.1	0.0	−0.1	V
V_{CC}	I_{CC}	5.0	5.5	6.0	V

TABLE III. Looser/Tighter Test Limits Example: DM74LS00

Parameter	Looser	Nominal	Tighter	Units
$V_{IH(min)}$	2.1	2.0	1.9	V
$V_{IL(max)}$	0.7	0.8	0.9	V
$V_{IK(max)}$	−1.6	−1.5	−1.4	V
$V_{OH(min)}$	2.6	2.7	2.8	V
$V_{OL(max)}$	0.6	0.5	0.4	V
$I_{I(min)}$	6.5	7.0	7.5	V
$I_{IH(max)}$	50	40	30	μA
$I_{IL(max)}$	−450	−400	−390	μA
$I_{OS(max)}$	−110	−100	−90	mA
$I_{OS(min)}$	−10	−20	−30	mA
$I_{CCH(max)}$	1.7	1.6	1.5	mA
$I_{CCL(max)}$	4.5	4.4	4.3	mA

Following are the test set-ups that are used to test the DC parametrics. In each case, the gate connection, equivalent circuit schematic and resultant voltage/current plot are shown.

The indicated graphs are typical of LS products and are similiar to other bipolar logic families. The schematics shown are for single inversion devices and represent generalized circuits.

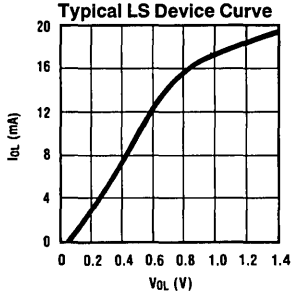
OUTPUT VOLTAGE LOW LEVEL (V_{OL})

Both inputs are connected to logic "1" values (assuming an inverting gate) and forced at the V_{IH} specs. V_{CC} minimum is used, and I_{OL} is forced on the output. The resulting V_{OL} is measured. For typical LS products, the military and commercial test points are indicated on the V_{OL} vs I_{OL} graph. In each case, the device must not exceed the V_{OL} spec when the I_{OL} current is being forced.

OUTPUT VOLTAGE HIGH LEVEL (V_{OH})

One input is tied high (any value above 2.0V) and the other input is forced at the V_{IL} threshold (assuming a single inversion gate). The minimum V_{CC} value is used. Each input is tested independently and the I_{OH} current is forced. The resulting V_{OH} is measured. The V_{OH} vs I_{OH} graph shows the military and commercial V_{OH}/I_{OH} test points for standard LS products.

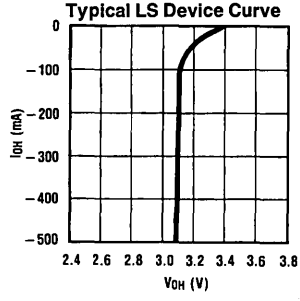
V_{OL} vs I_{OL}
Typical LS Device Curve



	I_{OL}	V_{OL}
Mil:	4.0 mA	0.40V
Com:	8.0 mA	0.50V

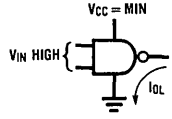
TL/F/6731–1

V_{OH} vs I_{OH}
Typical LS Device Curve

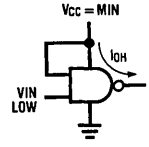


	I_{OH}	V_{OH}
Mil:	−400 μA	2.5V
Com:	−400 μA	2.7V

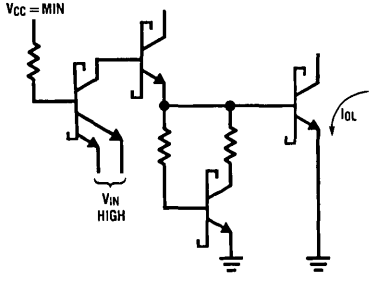
TL/F/6731–2



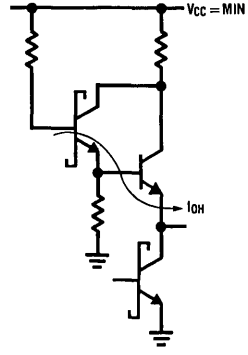
TL/F/6731–3



TL/F/6731–4



TL/F/6731–5



TL/F/6731–6

INPUT CURRENT HIGH LEVEL (I_{IH})

I_{IH} tests the input leakage in the high state. For MET, diode, and PNP input, the test set-up consists of all inputs except the one under test tied high (greater than V_{IH}). The remaining input has the V_{IH} value forced upon it, and the resultant I_{IH} is measured. This test checks for emitter-to-collector inverse transistor action for MET inputs, and reverse bias leakage for diode and PNP inputs.

For MET inputs, there is also an additional set-up for I_{IH} testing that checks for emitter-to-emitter transistor action. This is done with all the other inputs tied to ground.

MAXIMUM INPUT CURRENT (I_I)

I_I or BV_{IN} testing is the same as the emitter-to-collector leakage test (I_{IH}) and guarantees that the input will not pass more than the specified current at the stated specification (100 μA at 7V for LS).

INPUT CURRENT LOW LEVEL (I_{IL})

One input at a time is tested with the other inputs tied to a solid "1" value. V_{CC} is set to the maximum value and the V_{IL} value is forced. I_{IL} is then measured.

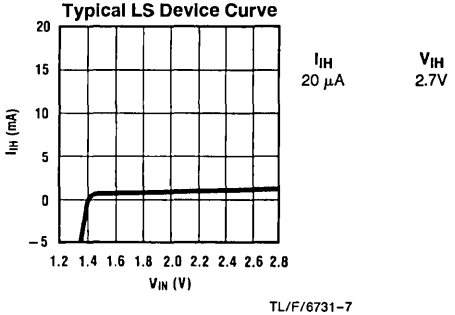
$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{BE})]}{R1} \quad \text{Standard Inputs}$$

$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{SH})]}{R1} \quad \text{Diode Inputs}$$

$$I_{IL} = \frac{[V_{CC} - (V_{IL} + V_{BE})]}{R1 \times \beta} \quad \text{PNP Inputs}$$

I_{IL} is intended to measure the value of the base pull-up resistor on the input, and to guarantee the maximum input load an IC presents.

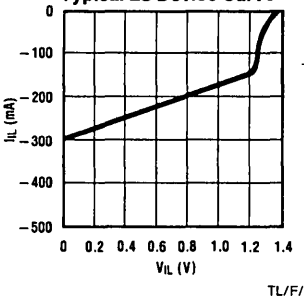
I_{IN} vs V_{IN} (High State)
Typical LS Device Curve



I_{IH} 20 μA V_{IH} 2.7V

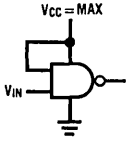
TL/F/6731–7

I_{IN} vs V_{IN} (Low State)
Typical LS Device Curve

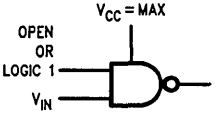


I_{IL} −400 μA V_{IL} 0.40V

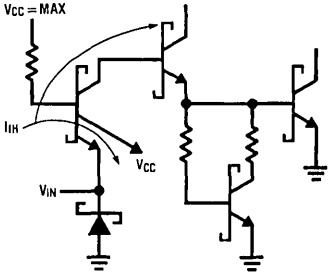
TL/F/6731–8



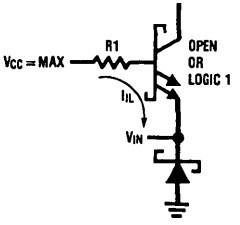
TL/F/6731–9



TL/F/6731–10



TL/F/6731–11



TL/F/6731–12

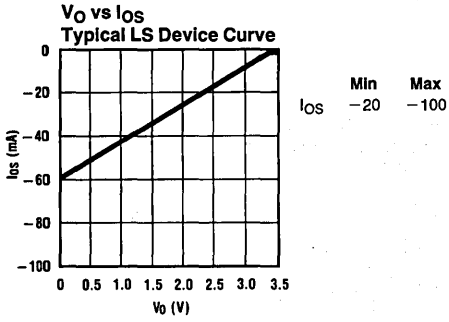
OUTPUT SHORT CIRCUIT CURRENT (I_{OS})

I_{OS} is measured with $V_{CC(max)}$ and the 0V forced on the output while it is in the high state. The resultant current is measured. The purpose of this is to check the I_{OS} resistor that forms the Darlington's collector pull-up. This parameter is important as it reflects both the maximum current the device will draw and the maximum drive it will provide when it is switching from low to high.

Caution must be taken when measuring TTL, LS and S outputs as the power dissipated on the die will be substantial. I_{OS} shorts should not be maintained in excess of one second or damage to the device may result.

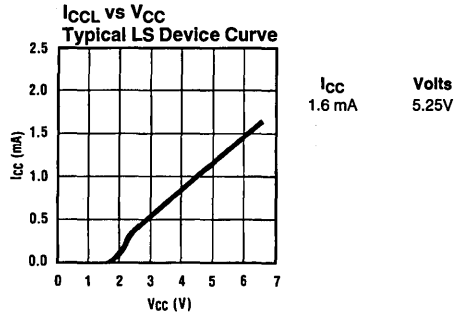
SUPPLY CURRENT HIGH LEVEL (I_{CCH}) AND SUPPLY CURRENT LOW LEVEL (I_{CCL})

Both I_{CCH} and I_{CCL} are tested using the V_{CC} maximum value. The inputs are set to the values necessary to achieve the output in the desired state. All outputs are left open, neither sourcing nor sinking current. The goal of this test is to guarantee the maximum quiescent operating power that the device will draw.



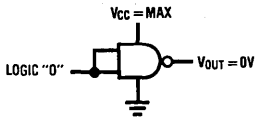
	Min	Max
I_{OS}	−20	−100

TL/F/6731–13

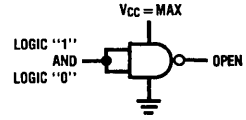


I_{CC}	Volts
1.6 mA	5.25V

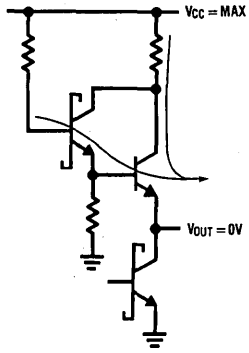
TL/F/6731–14



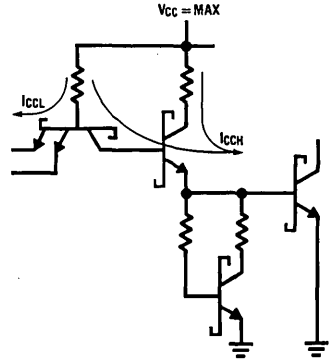
TL/F/6731–15



TL/F/6731–16



TL/F/6731–17



TL/F/6731–18

INPUT CLAMP VOLTAGE (V_{IC} OR V_{IK})

$V_{CLAMP}(V_{IK})$ is measured with all but one input tied high and the I_{IK} current forced on the remaining input. V_{CC} is set to the minimum and the V_{IK} voltage is measured.

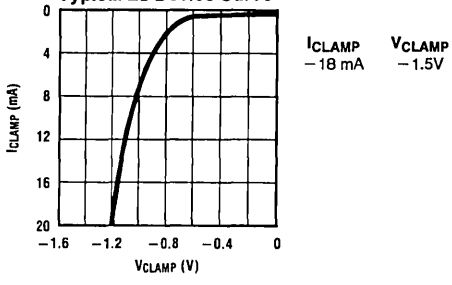
OUTPUT TRI-STATE CURRENT HIGH LEVEL (I_{OZH}) AND OUTPUT TRI-STATE CURRENT LOW LEVEL (I_{OZL})

TRI-STATE® I_{SINK} and I_{SOURCE} are measured with the output control input tied to the appropriate threshold value (usually V_{IL} = 0.8V) and with $V_{CC(max)}$. This is to insure that the output will have the greatest drive capability and the TRI-STATE control can effectively "turn off" the output under these conditions.

TRI-STATE I_{SINK}: Output is set in the high state and then TRI-STATE mode. V_{OZL} = 0.4V is then applied. The current drawn out of the device is then measured.

TRI-STATE I_{SOURCE}: Output is set in the low state and then TRI-STATE mode. V_{OZH} = 2.7V is then applied. The current drawn into the device is then measured.

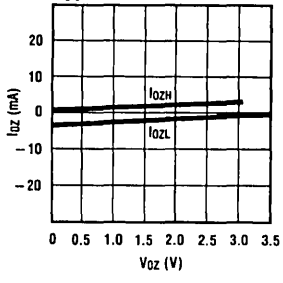
V_{CLAMP} vs I_{CLAMP}
Typical LS Device Curve



I_{CLAMP}	V_{CLAMP}
−18 mA	−1.5V

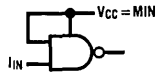
TL/F/6731–19

I_{OZH} vs V_{OZH}
(TRI-STATE I_{SOURCE}),
I_{OZL} vs V_{OZL}
(TRI-STATE I_{SINK})
Typical LS Device Curve



	I_{OZ}	V_{OZ}
I_{OZL}	−20 μA	0.4V
I_{OZH}	20 μA	2.7V

TL/F/6731–20



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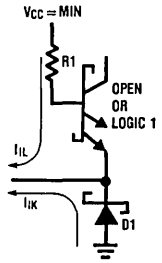

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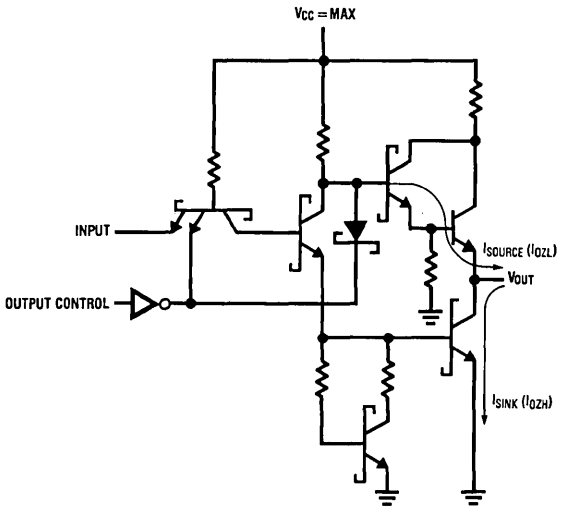
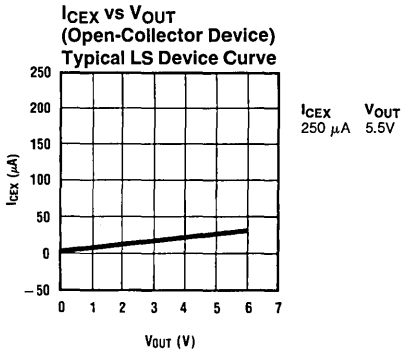


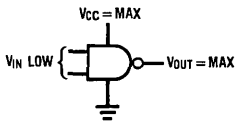
TL/F/6731–23

HIGH LEVEL OUTPUT CURRENT (OPEN-COLLECTOR DEVICES ONLY)

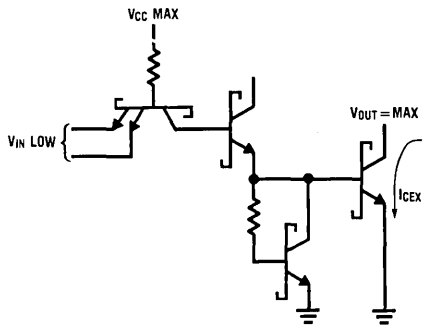
I_{CEX} is tested with the output in the high state. V_{CC} is set to 5.0V and the specified voltage (5.5V for LS) is applied to the output. The inputs are at the threshold values (0.8V and 2.0V, depending upon the logic to put output in the high state) and the resulting I_{CEX} leakage current is measured.



TL/F/6731–24



TL/F/6731–25



TL/F/6731–26

AC SWITCHING CHARACTERISTICS

The AC switching characteristics are generally measured in units of time (commonly in nanoseconds), and define how long it takes for the signal to propagate from the input to the output. The definitions used in determining the pass/fail status of each limit are not the same for AC as they are for DC. The distinction lies in the fact that for DC operation there exists one characteristic V-I curve on which the device must operate. Devices are good if they operate on the correct side of the limit, and bad if they operate on the wrong side of the limit. When dealing with certain AC parameters (f_{MAX}, $t_{SET\text{-}UP}$, t_{HOLD}, $t_{RELEASE}$, t_{PW}), the device can, and usually does, operate on both sides of the databook limit. The limit really implies a boundary that all devices are guaranteed to exceed. Depending upon the parameter, the device will either operate at all values above and some below the limit, or it will operate at all values below and some above the limit. In each case, the device is only guaranteed to operate for all values on one side of the limit. Although the device will also operate beyond the limit, it is not guaranteed to. Furthermore, device operation beyond the limit is not considered a failure. For instance, take the f_{MAX} parameter with a min limit of 25 MHz. All devices are guaranteed to operate at all frequencies below 25 MHz and will operate in excess of 25 MHz, although this is not guaranteed. Now, take the example of $t_{SET\text{-}UP}$ with a minimum limit of 25 ns. All of the devices are guaranteed to operate with a set-up time of 25 ns and longer, and will operate with set-up times below 25 ns, although this is not guaranteed either. Be aware that both of these specifications are listed in the minimum column in the databook, but the interpretation of what is failing differs significantly.

Propagation delays (called prop delays and denoted by the symbols t_{PHL} and t_{PLH}) are specified as maximum limits, and guarantee the maximum time one must wait to insure that the correct data has appeared at the device's output. Each propagation delay is specified from one input to one output only.

Input set-up and hold times (including $t_{RELEASE}$) specify how long one input must be stable at a particular logic level prior to an action occurring at another input. For example, take the DM54/74LS74 positive-edge-triggered D flip-flop. The "set-up 1" specification defines how long a logic "1" must be present *and* stable at the DATA input prior to the positive edge of the CLOCK to insure that the device will recognize that data as a "1". There also exists a "hold 1" specification which specifies how long a logic "1" must be held after the active edge of CLOCK for the device to recognize that logic "1". Both the set-up and hold times must always be met or the device will not necessarily bring in the proper data. Set-up times are generally positive, while hold

times may be either positive or negative, usually negative. The meaning of a negative hold time is that the data may be removed from the input prior to the active edge of CLOCK, and the CLOCK will still bring in the desired data. Set-up and hold times are specified as minimum values, since this defines the minimum time data must be stable prior to any change at the CLOCK input. Removing the data sooner than the minimum time may cause improper action on the part of the device.

$t_{RELEASE}$ is specified on devices where there is an input that must be set inactive prior to the active edge of CLOCK. Such inputs are usually overriding inputs like CLEAR and PRESET. With CLEAR active, it will prevent the device from switching on the CLOCK signal. $t_{RELEASE}$ is defined as the time it takes for the CLEAR input to "release" the device for clocking action, and is specified as a minimum. This represents the maximum delay required between CLEAR going inactive and the active edge of CLOCK to insure proper device operation.

All devices that have a CLOCK input also have a specification that defines the maximum speed that the CLOCK can be driven, called f_{MAX}. This specification is defined as a minimum specification and states that all of the devices will be able to operate at frequencies up to 25 MHz. For the DM54/74LS74 with an f_{MAX} of 25 MHz, all of the devices are guaranteed to operate at all clock frequencies, up to and including 25 MHz. Although no devices are guaranteed to operate above f_{MAX} (only below it), most devices will operate beyond the maximum specification. The minimum limit does *not* state that the device will not operate below f_{MAX} or that any devices that do are bad, but rather that all the devices will operate up to the limit.

Table IV shows the direction of the tighter testing for the more common AC parameters. All prop dealys (those AC parameters that have the symbols t_{PLH} or t_{PHL}) have simple min/max limits. The device is guaranteed to operate within the bounds of the min/max limits, and any operation outside these limits denotes a device failure. $t_{SET\text{-}UP}$, t_{HOLD}, f_{MAX}, and $t_{RELEASE}$ parameters have limits that denote guaranteed operation boundaries (i.e., the device is guaranteed to operate up to the boundary) but no guarantee is made concerning the device operation (or lack of it) beyond the boundary.

For detailed information on the AC waveforms, please see the test waveforms in this section.

TABLE IV. Looser/Tighter AC Test Limits Example: DM74LS74

Test	From	Looser	Nominal	Tighter	Units
$f_{max(min)}$		24	25	26	MHz
$t_{PLH(max)}$	CLR, PRE, CLK	26	25	24	ns
$t_{PHL(max)}$	CLR, PRE, CLK	31	30	29	ns
$t_{W(min)}$	CLOCK HIGH	21	20	19	ns
$t_{W(min)}$	PRE, CLR LOW	26	25	24	ns
$t_{SET\text{-}UP(min)}$	DATA HIGH	21	20	19	ns
$t_{SET\text{-}UP(min)}$	DATA LOW	21	20	19	ns
$t_{HOLD(min)}$	All DATA	1	0	−1	ns

Designing with TTL

National Semiconductor Corp.
Application Note 363
Walt Sirovy

54/74 series TTL has been used for more than a decade with excellent results, and continues to be a standard choice for design engineers because of the wide performance range and system optimization possible from the different families available. 54/74 logic comes in 7 different speed/power families (standard TTL, LS, S, ALS, AS, and L) that allow a design engineer to select device performance to suit his needs. Understanding the differences and the general limitations of all these families will go a long way toward insuring that a system will operate as intended with the minimum of corrections and redesigning.

FAMILY COMPATIBILITY: Intermixing Logic Types In One Design

Family interchangeability is a beneficial characteristic of the different TTL families and provides the designer with the ability to customize specific areas of his design in order to accomplish the task of achieving both high performance and the lowest power consumption possible. However, interchangeability is not simply a matter of replacing, say, an S00 for an LS00 to improve the speed and replacing an LS00 for an S00 for power savings. One must also look at the DC and AC characteristics to insure that the replacement device will be compatible with the existing circuit. The DC problems include input loading and compatible output drive capabilities. The AC problems include insuring that the new device speeds will be acceptable to the rest of the system. The different logic families also generate different amounts of noise and have different noise immunity. Finally, measure points for the AC parameters of the different families, although very similar, do vary some, and this will require attention.

SUPPLY RAILS: Why Not to Exceed the Specs

All bipolar logic (both junction and oxide isolated) is made up of selectively located regions of differently doped materials that form transistors, resistors, and diodes. Because of this, certain overall requirements are necessary to insure that the IC will be able to perform its task without interference from its environment. The first characteristic of bipolar devices is that the two power rails (V_{CC} and ground) represent the two voltage extremes that should be used in any system. Certain exceptions exist, primarily inputs and open-collector outputs that are pulled up to higher voltages than V_{CC}. However, while it is occasionally permissible to exceed the V_{CC} specification, it is never permissible to drive any input or output more than 0.5V below the ground reference. This limitation is due to the method used to electrically isolate the many circuit elements that are present on a bipolar IC. Oxide isolated devices use an oxide layer surrounding the various transistor and resistor tanks to provide an insulating barrier, while the original junction isolated devices use reverse biased PN junctions to provide that barrier. In both cases, the circuit is built on a P-type substrate that uses reverse biased PN junctions to separate the different circuit elements. The ground pin is electrically connected to the substrate and must be the most negative voltage on the device. When an input or output pin is taken below ground, the normally reverse biased isolation regions between the elements become forward biased and electrically connect these elements together, thus eliminating the integrity of the circuit. This may or may not result in actual damage to the device depending upon the magnitude of the violating signal and the specifics of the device being violated. This holds true for both junction and oxide isolated logic. Oxide isolated logic may provide more margin before failing (thereby "working" in some marginal designs), but it is nevertheless subject to the same kind of limitations as junction isolated logic.

IMPROPER GROUNDING: Noise Immunity, Floating Grounds

Bipolar logic uses the ground rail as the signal reference. Consequently, any modulation on the ground line will be directly added to the signal voltage. The logic "0" input noise margin is guaranteed as the difference between the V_{OL} and V_{IL} specification, and the logical "1" input noise margin is guaranteed as the difference between the V_{OH} and V_{IH} specification. This noise margin is intended to be protection against a reasonable amount of noise present. Insufficient grounding techniques can cause significant I_R and I_L drops on the ground line between two ICs and result in a "floating" ground line. This is due to the large currents that are present on ground and V_{CC} during high speed switching and means that the two devices are not using the same reference point. Any voltage drop in the ground line is added to the signal and ends up consuming some of the noise margin. Eventually, the mismatch caused by the floating ground will exceed the total noise margin and cause erroneous data to propagate through the system. The solutions to this problem are many and varied, but all of them revolve around improving the system grounding and include such ideas as providing separate signal and power grounds.

V_{CC} NOISE AND DECOUPLING: Providing Clean Power

The V_{CC} power rail is also susceptible to both I_R and I_L voltage drops. The problems that arise from the V_{CC} line are not the same as the problems that arise from the ground line. Since the V_{OH} level tracks the V_{CC} almost exactly, any voltage loss on the V_{CC} line is directly transferred to the V_{OH} level. However, the noise margin for the logic high state is typically 700 mV for commercial and 500 mV for military product, versus 400 mV and 300 mV for commercial and military product, respectively, for the logic low level. The main consequences of a drooping V_{CC} line now become I_{OL}/I_{OH} drive capability, and the AC performance in critical applications. Although bipolar devices are only guaranteed to operate over a given V_{CC} range (5V ± 10%), these devices typically function to V_{CC} values as low as 4V. Be aware that if the device does indeed function down to 4V, the AC and DC characteristics will be compromised, some quite severely.

Designing in a good power distribution system will insure that all the devices in the circuit will perform the same, regardless of their physical location. Properly decoupling the V_{CC} against both high and low frequency noise will help eliminate any problems with individual device operation. High frequency noise (100 MHz and above) comes primarily from two sources, while low frequency noise (less than 25 MHz) results from primarily one source.

SOURCES OF HIGH FREQUENCY NOISE ON THE V_{CC} LINE

1) High frequency noise results from the device rapidly switching logic levels. The bulk of the switching current from a low to high transitions shows up in I_{CC} current surges, while the bulk of the switching current from a high to low transition shows up in ground current surges.

2) Noise is transmitted through the changing magnetic fields that result from the changing electric fields in a switching line and are picked up on adjacent signal paths.

Note that the frequency causing the noise is not the signal's frequency, but the frequency of the signal's slew rate. For instance, in an S00 that is switching 0V to 3V at 1 MHz, the slew rate of the output is typically about 1 ns/V, which is a frequency of around 160 MHz. The faster the slew rate, the higher the frequency, until one has an ideal square wave with infinite frequency. It is this frequency component that gives rise to the strong magnetic fields associated with switching bipolar devices.

SOURCES OF LOW FREQUENCY NOISE ON THE V_{CC} LINE

1) Low frequency noise results from the change in the I_{CC} current demand as devices change state. For instance, gates, flip-flops, and registers will draw different I_{CC} currents, depending upon the state of the outputs.

The most commonly used method for countering these noise problems is to decouple the V_{CC} line. With this approach, capacitors are used to stabilize the V_{CC} line and filter out the unwanted frequency components. A small value capacitor (i.e., 0.1 μF) is used near the device to insure that the transient currents arising from device switching and magnetic coupling are minimized. A large value capacitor (i.e., 50 μF to 100 μF) is used on the board in general to accommodate the continually changing I_{CC} requirements of the total V_{CC} bus line. The following table shows a rough "rule of thumb" approach to determining how many capacitors to use for a given number if ICs. Be aware that the table is not a hard and fast rule, and that you must always evaluate your particular application to insure that there is sufficient V_{CC} decoupling. When using these guidelines, be sure that the devices are located near each other and near the capacitor. If the capacitor is too far away, I_R and I_L drops will diminish the capacitor's effect. All capacitors (especially the 0.01 μFs) must be high frequency RF capacitors. Disk ceramics are acceptable for this application. Keep in mind that, in synchronous systems, since a majority of the devices will be switching at once, alter your power distribution system accordingly.

Device Family	Number of Capacitors
AS, S, ALS, LS, H	1 Cap per 1 device
TTL, L	1 Cap per 2 devices

TYING ALL UNUSED INPUTS TO A SOLID LOGIC LEVEL

Unused inputs on TTL devices float at threshold, anywhere from 1.1V to 1.5V, depending upon the device and its family. While this usually simulates a "high", many application problems can be traced to open inputs. Inputs floating at threshold are very susceptible to induced noise (transmitted from other lines) and can easily switch the state of the device. A good design rule is to tie unused inputs to a solid logic level. Inputs are usually tied to V_{CC} through a 1 kΩ to 5 kΩ resistor, since tying them to ground means supplying the I_{IL} current instead of the I_{IH} current. I_{IL} is several orders of magnitude greater than I_{IH}. The resistor is recommended to protect the input against V_{CC} voltage surges and to protect the system against the possibility of the input shorting directly to ground. A single 1k resistor can handle up to 10 inputs.

TERMINATIONS: Why Terminate a Transmission Line?

Whenever signals change voltage levels, a wavefront is created that propagates according to the characteristics of the transmission line being used. If the overall length of the signal path is short compared with the signal's wavelength (1/frequency), then none of the complications of transmission lines are present. However, if the length of the signal path is long in comparison, then the wavefront will be significantly affected by the geometry and composition of that transmission line.

Fortunately, when dealing with a single board layout, the distances are usually short enough that one need not worry about the difficulties of terminating or impedance matching the line. However, if one is driving between boards or over long distances, he must be aware of the characteristics involved. When dealing with transmission lines it is necessary to know the impedance of the line. Every time the signal wavefront encounters a discontinuity (a point where the impedance changes, whether from a branch, junction or because of a change of environment), the opportunity for reflections and standing waves is present. These waves can easily cause the loss of the signal's integrity, having the ability to build voltages that are large enough to destroy an IC. Proper line termination will insure that the signal propagates down the line and is totally absorbed at the receiving end, thus preventing these waves from occurring.

Listed below is a guideline to the types of transmission lines to use when sending signals over various distances.

0" to 12" Single wire conductor OK. Use point-to-point routing and avoid parallel routing if possible. Ground plane recommended, but not mandatory. Space conductors as far apart as possible to reduce line to line capacitance.

12" to 6' Dense ground plane required with wire routed as closely as possible. Twisted-pair lines or coaxial cable mandatory for clock lines and recommended for all sensitive control lines.

Over 6' Use fully terminated transmission lines. Avoid the use of radially distributed lines and avoid sharp bends in the line. Be aware that transmission lines have complex impedances and are not simply resistive in nature.

BUS DRIVERS: On Board vs Off Board

Many of the TRI-STATE® buffers and flip-flops are intended to connect directly to the system bus and must be able to drive heavily capacitive loads. Keeping this in mind, all of National's LS TRI-STATE devices have "triple-sink" capability; that is, the I_{OL} and I_{OH} drive currents have been tripled. However, these devices are intended to drive single board buses. Driving off the board with these devices can easily lead to serious problems.

When using standard logic bus drivers on a single board, be aware that many of the octal and bus oriented devices have PNP inputs to reduce DC loading. PNP inputs on 54S/74S devices tend to be more capacitive than the corresponding diode or emitter inputs, and as such, compromise the AC loading of the bus. Careful attention must be given to both DC and AC loading when driving heavily loaded buses. PNP

inputs on LS/AS/ALS operate at significantly lower currents and do not significantly increase capacitive load.

It is strongly recommended that any time a bus line leaves a board, interface bus drivers be used. These devices (see National's 1986 Interface/Databook) are specifically designed to impedance match different kinds of transmission lines and have the necessary current drive to handle the job. Using an ordinary logic device will usually yield poor results. If one must drive a transmission line with a logic device, there are some guidelines that should be followed to minimize the problems that can result.

1) Take care to properly terminate the bus. Be aware that every time a signal passes through a different impedance, an interface is created and that any impedance mismatch will result in reflections.

2) Never drive off the board with a bistable element like a flip-flop or a latch. This is because those devices are very susceptible to reflected waves changing their state. By buffering the output of the latch with another device, the reflected wave can affect the output of the buffer, but not the latch. This means that when the wave finally dies out, the latch will still have the proper data and the buffer will "snap back" to the proper output.

3) Be sure to carry an adequate ground plan with the signals and to shield the bus. Carrying a good ground plan (use multiple ground lines spaced around the connector if possible) will reduce the problem of floating ground, and the shielding will help protect the signal lines for induced noise. Using twisted-pair transmission lines for critical signals helps to eliminate the capacitive coupling that can degrade signals, or even cause false signals.

4) It is best to buffer any clock or control lines that depend upon fast, clean switching. Buffering at both the sending and receiving end will go a long way toward insuring that the clock can accomplish its goals.

5) Use the devices with Schmitt inputs to add to the noise margin of the receiving device. This will help increase the noise rejection of the system. Decouple each receiver separately, connecting the capacitor directly between ground and V_{CC}. Make sure that the device ground is tied directly to the bus ground.

6) If using open-collector devices to drive the bus, add a pull-up resistor on the input to the receiving device if the I_{OL} current of the driving device can handle it. A resistance in the 300Ω range will significantly improve the signal's rise time.

AC LOADING: What Do AC Loads Look Like, and Why?

The standard AC load for all of the logic families, except ALS and AS, is built around a diode chain to ground and a pull-up resistor to V_{CC} with added capacitance. This load is designed to look like the standard logic circuit input structure, and to simulate the appearance of switching in an actual application. For ALS and AS, the load is built around a resistor to ground and added capacitance. This is primarily for the requirements of high speed device testing. There also exists a set of standardized military AC loads that were designed to approximate the input structure, while using no switches for the TRI-STATE parameters. Please see waveforms in this section. In the final analysis of these loads, it must be kept in mind that they represent a standard that can be used to determine the quality of an IC. No load will be able to predict exactly how a device will perform in a circuit or the speeds that a device can achieve in a good test jig with the spec load, as compared to the speeds that a device will produce in an application.

OPEN-COLLECTOR DEVICES: What They Are, How to Use Them

Open-collector devices are totem pole outputs where the upper output (usually a Darlington transistor) is left out of the circuit. As such, these devices have no active logic high drive and cannot be used to drive a line high. The advantage to open-collector devices is that a number of outputs can be directly tied together. If one were to tie two complete totem pole outputs together, then at some time one output would be driving high while the other output was driving low. The result is that one device will be dumping excessive current directly into the other device. The resulting power dissipation in both devices can easily degrade the lifetime of the device. Since open-collector devices only have active drive in one state, if two connected devices drive to opposite states, the low state will always predominate and there will be no degradation to either device. Open-collector specifications are obvious by the lack of a V_{OH} specification. The only V_{OH}/I_{OH} specification is the leakage limits, and these are specified at $V_{OH} = 5.5V$.

When dealing with open-collector devices, it must be noted that each output requires a resistive pull-up, usually tied to V_{CC}. (By using high voltage outputs, one can tie the resistor pull-up to a voltage higher than V_{CC}.) Designers often try to get away with tying the output to an input and relying on the I_{IL} current to pull up the output. This unwise, as it is just like leaving inputs floating: the input is very susceptible to noise and can easily give false signals. Shown below are two equations that can be used to determine the min/max range of the pull-up resistor.

$$R_{MAX} = \frac{(V_{CC(MIN)} - V_{OH})}{(N1 \bullet I_{OH} + N2 \bullet I_{IH})}$$

$$R_{MIN} = \frac{(V_{CC(MIN)} - V_{OL})}{(I_{OL} - N2 \bullet I_{IL})}$$

where: N1 = the number of open-collector devices tied together,

N2 = the number of inputs being driven on the line.

If the maximum resistance is exceeded, then it is possible for the total leakage currents from all of the inputs and outputs to pull the V_{OH} level below the spec value. Likewise, if the R_{MIN} value is exceeded, then the driving device may not be able to pull down the signal line to a solid V_{OL}. Either of these two cases can easily result in false logic levels being propagated through the system.

Designer's Encyclopedia of Bipolar One-Shots

National Semiconductor Corp.
Application Note 372
Kern Wong

INTRODUCTION

National Semiconductor manufacturers a broad variety of industrial bipolar monostable multivibrators (one-shots) in TTL and LS-TTL technologies to meet the stringent needs of systems designers for applications in the areas of pulse generation, pulse shaping, time delay, demodulation, and edge detection of waveforms. Features of the various device types include single and dual monostable parts, retriggerable and non-retriggerable devices, direct clearing input, and DC or pulse-triggered inputs. Furthermore, to provide the designer with complete flexibility in controlling the pulse width, some devices also have Schmitt trigger input, and/or contain internal timing components for added design convenience.

DESCRIPTION

One-shots are versatile devices in digital circuit design. They are actually quite easy to use and are best suited for applications to generate or to modify short timings ranging from several tens of nanoseconds to a few microseconds. However, difficulties are constantly being experienced by design and test engineers, and basically fall into the categories of either pulse width problems or triggering difficulties.

The purpose of this note is to present an overall view of what one-shots are, how they work, and how to use them properly. It is intended to give the reader comprehensive information which will serve as a designer's guide to bipolar one-shots.

Nearly all malfunctions and failures on one-shots are caused by misuse or misunderstanding of their fundamental operating rules, characteristic design equations, parameters, or more frequently by poor circuit layout, improper bypassing, and improper triggering signal.

In the following sections all bipolar one-shots manufactured by National Semiconductor are presented with features tables and design charts for comparisons. Operating rules are outlined for devices in general and for specific device types. Notes on unique differences per device and on special operating considerations are detailed. Finally, truth tables and connection diagrams are included for reference.

DEFINITION

A one-shot integrated circuit is a device that, when triggered, produces an output pulse width that is independent of the input pulse width, and can be programmed by an external Resistor-Capacitor network. The output pulse width will be a function of the RC time constant. There are various one-shots manufactured by National Semiconductor that have diverse features, although, all one-shots have the basic property of producing a programmable output pulse width. All National one-shots have True and Complementary outputs, and both positive and negative edge-triggered inputs.

OPERATING RULES

In all cases, R and C represented by the timing equations are the external resistor and capacitor, called R_{EXT} and C_{EXT}, respectively, in the data book. All the foregoing timing equations use C in pF, R in KΩ, and yield t_W in nanoseconds. For those one-shots that are not retriggerable, there is a duty cycle specification associated with them that

TTL AND LS-TTL ONE-SHOT FEATURES

Device Number	# Per IC Package	Re-trigger	Reset	Capacitor Min	Capacitor Max	Capacitor In μF	Resistor Min	Resistor Max	Resistor In KΩ	Timing Equation* for C_{EXT} > 1000 pF
DM54121	One	No	No	0	1000		1.4	30		$t_W = KRC\bullet(1 + 0.7/R)$
DM74121	One	No	No	0	1000		1.4	40		$K = 0.55$
DM54LS122	One	Yes	Yes	None			5	180		$t_W = KRC$
DM74LS122	One	Yes	Yes	None			5	260		$K = 0.45$
DM54123	Two	Yes	Yes	None			5	25		$t_W = KRC\bullet(1 + 0.7/R)$
DM74123	Two	Yes	Yes	None			5	50		$K = 0.34$
DM54LS123	Two	Yes	Yes	None			5	180		$t_W = KRC$
DM74LS123	Two	Yes	Yes	None			5	260		$K = 0.45$
DM54LS221	Two	No	Yes	0	1000		1.4	70		$t_W = KRC$
DM74LS221	Two	No	Yes	0	1000		1.4	100		$K = 0.7$
DM8601	One	Yes	No	None			5	25		$t_W = KRC\bullet(1 + 0.7/R)$
DM9601	One	Yes	No	None			5	50		$K = 0.32$
DM8602	Two	Yes	Yes	None			5	25		$t_W = KRC\bullet(1 + 1/R)$
DM9602	Two	Yes	Yes	None			5	50		$K = 0.31$

*The above timing equations hold for all combinations of R_{EXT} and C_{EXT} for all cases of C_{EXT} > 1000 pF within specified limits on the R_{EXT} and C_{EXT}.

defines the maximum trigger frequency as a function of the external resistor, R_{EXT}.

In all cases, an external (or internal) timing resistor (R_{EXT}) connects from V_{CC} or another voltage source to the "R_{EXT}/C_{EXT}" pin, and an external timing capacitor (C_{EXT}) connects between the "R_{EXT}/C_{EXT}", and "C_{EXT}" pins are required for proper operation. There are no other elements needed to program the output pulse width, though the value of the timing capacitor may vary from 0.0 to any necessary value.

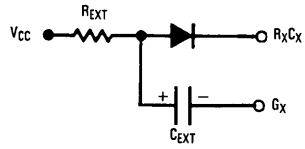
When connecting the R_{EXT} and C_{EXT} timing elements, care must be taken to put these components absolutely as close to the device pins as possible, electrically and physically. Any distance between the timing components and the device will cause time-out errors in the resulting pulse width, because the series impedance (both resistive and inductive) will result in a voltage difference between the capacitor and the one-shot. Since the one-shot is designed to discharge the capacitor to a specific fixed voltage, the series voltage will "fool" the one-shot into releasing the capacitor before the capacitor is fully discharged. This will result in a pulse width that appears much shorter than the programmed value. We have encountered users who have been frustrated by pulse width problems and had difficulty to perform correlations with commercial test equipment. The nature of such problems are usually related to the improper layout of the DUT adapter boards. (See *Figure 6* for a PC layout of an AC test adapter board.) It has been demonstrated that lead length greater than 3 cm from the timing component to the device pins can cause pulse width problems on some devices.

For precise timing, precision resistors with good temperature coefficient should be used. Similarly, the timing capacitor must have low leakage, good dielectric absorption characteristics, and a low temperature coefficient for stability. Please consult manufacturers to obtain the proper type of component for the application.

For small time constants, high-grade mica glass, polystyrene, polypropylene, or polycarbonate capacitor may be used. For large time constants, use a solid tantalum or special aluminum capacitor.

In general, if a small timing capacitor is used that has leakage approaching 100 nA or if the stray capacitance from either terminal to ground is greater than 50 pF, then the timing equations or design curves which predict the pulse width would not represent the programmed pulse width which the device generates.

When an electrolytic capacitor is used for C_{EXT}, a switching diode is often suggested for standard TTL one-shots to prevent high inverse leakage current *(Figure 1)*. In general, this switching diode is not required for LS-TTL devices; it is also not recommended with retriggerable applications.



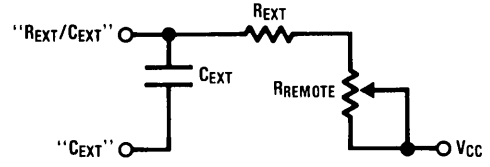
TL/F/7508–1

FIGURE 1

It is never a good practice to leave any unused inputs of a logic integrated circuit "floating". This is particularly true for one-shots. Floating uncommitted inputs or attempts to establish a logic HIGH level in this manner will result in malfunction of some devices.

Operating one-shots with values of the R_{EXT} outside the recommended limits is at the risk of the user. For some devices it will lead to complete inoperation, while for other devices it may result in either output pulse widths different from those values predicted by design charts or equations, or with modes of operation and performance quite different from known standard characterizations.

To obtain variable pulse width by remote trimmiing, the following circuit is recommended *(Figure 2)*. "R_{REMOTE}" should be placed as close to the one-shot as possible.

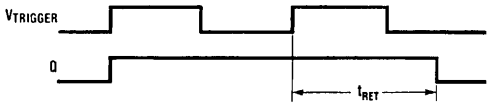


TL/F/7508–2

FIGURE 2

V_{CC} and ground wiring should conform to good high frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.001 μF to 0.1 μF bypass capacitor (disk or monolithic type) from the V_{CC} pin to ground is necessary on each device. Furthermore, the bypass capacitor shoud be located so as to provide as short an electrical path as possible between the V_{CC} and ground pins. In severe cases of supply-line noise, decoupling in the form of a local power supply voltage regulator is necessary.

For retriggerable devices the retrigger pulse width is calculated as follows for positive-edge triggering:



TL/F/7508–3

FIGURE 3

$$t_{RET} = t_W + t_{PLH} = K \bullet (R_{EXT})(C_{EXT}) + t_{PHL}$$

(See tables for exact expressions for K and t_W; K is unity on most HCMOS devices.)

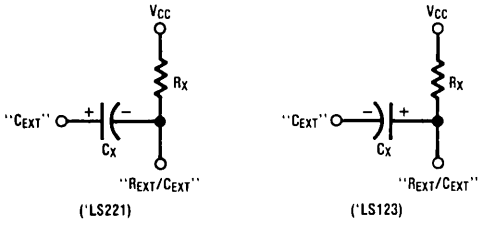
SPECIAL CONSIDERATIONS AND NOTES:

The 9601 is the single version of the dual 9602 one-shot. With the exception of an internal timing resistor, R_{INT}, the 'LS122 has performance characteristics virtually identical to the 'LS123. The design and characteristic curves for equivalent devices are not depicted individually, as they can be referenced from their parent device.

National's TTL-'123 dual retriggerable one-shot features a unique logic realization not implemented by other manufacturers. The "CLEAR" input does not trigger the device, a design tailored for applications where it is desired only to terminate or to reduce the timing pulse width.

The 'LS221, even though it has pin-outs identical to the 'LS123, is not functionally identical. It should be remembered that the 'LS221 is a non-retriggerable one-shot, while the 'LS123 is a retriggerable one. For the 'LS123 device, it is sometimes recommended to externally ground its "C_{EXT}" pin for improved system performance. The "C_{EXT}" pin on the 'LS221, however, is not an internal connection to the device ground. Hence, grounding this pin on the 'LS221 device will render the device inoperative.

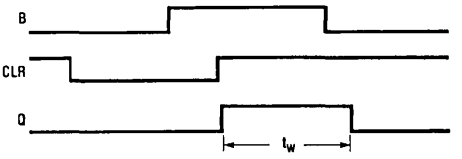
Furthermore, if a polarized timing capacitor is used on the 'LS221, the positive side of the capacitor should be connected to the "C_{EXT}" pin. For the 'LS123 part, it is the contrary, the negative terminal of the capacitor should be connected to the "C_{EXT}" pin of the device *(Figure 4)*.



TL/F/7508–4

FIGURE 4

The 'LS221 trigger on "CLEAR": This mode of trigger requires first the "B-Input" be set from a Low-to-High level while the "CLEAR" input is maintained at logic Low level. Then, with the "B" Input at logic High level, the "CLEAR" input, whose positive transition from LOW-to-HIGH will trigger an output pulse ("A input" is LOW).

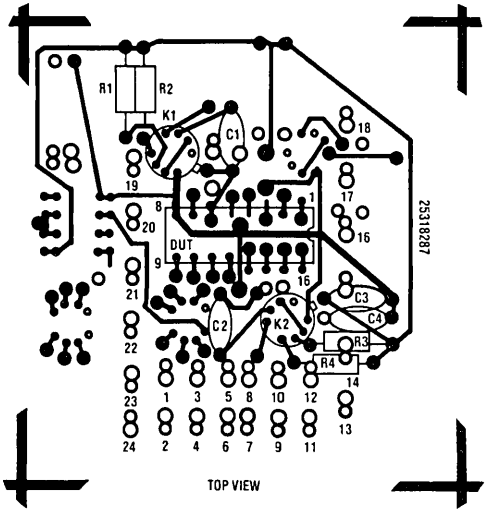


TL/F/7508–5

FIGURE 5

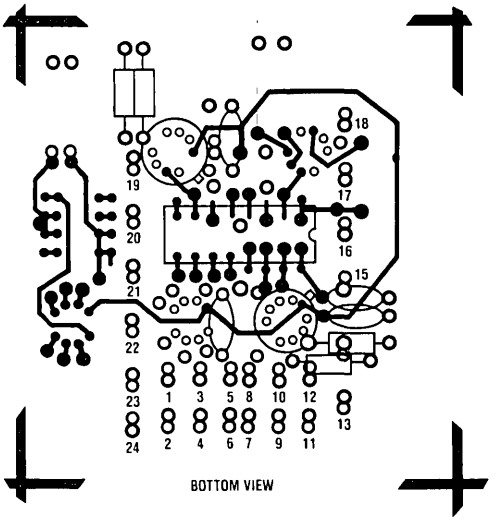
AC Test Adapter Board

The compact PC layout below is a universal one-shot test adapter board. By wiring different jumpers, it can be configured to accept all one-shots made by National Semiconductor. The configuration shown below is dedicated for the '123 device. It has been used successfully for functional and pulse width testing on all the '123 families of one-shots on the Teradyne AC test system.



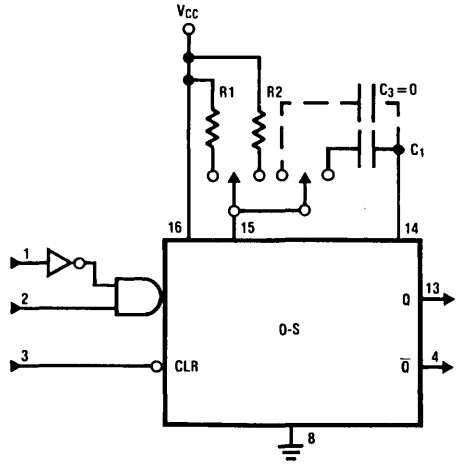
TL/F/7508–6

FIGURE 6a. AC Test Adapter



TL/F/7508–7

FIGURE 6b. AC Test Adapter

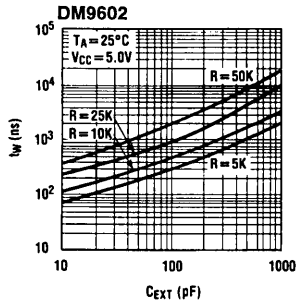


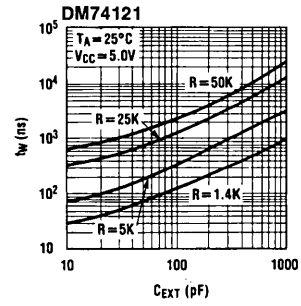
TL/F/7508–8

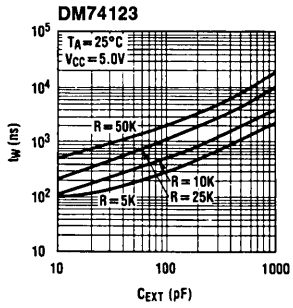
FIGURE 7a. Timing Components and I/O connections to D.U.T.

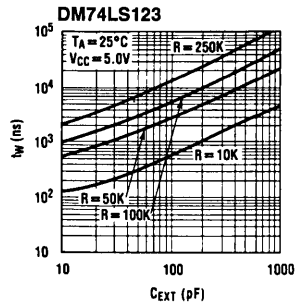
Typical Output Pulse Width vs Timing Components

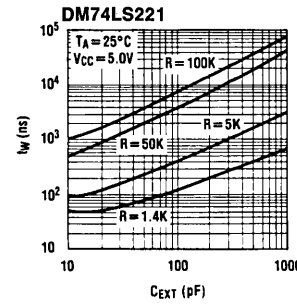
Timing equations listed in the features tables hold all combinations of R_{EXT} and C_{EXT} for all cases of $C_{EXT} >$ 1000 pF. For cases where the $C_{EXT} <$ 1000 pF, use graphs shown below.







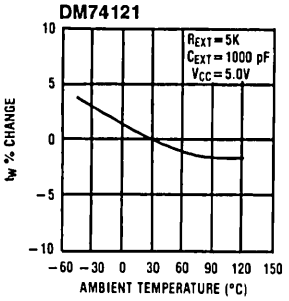


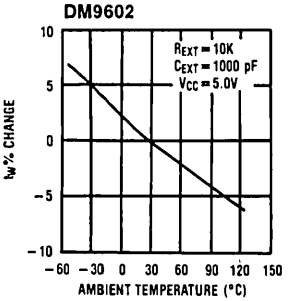


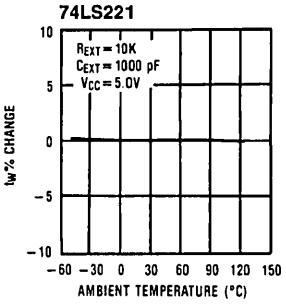
TL/F/7508–9

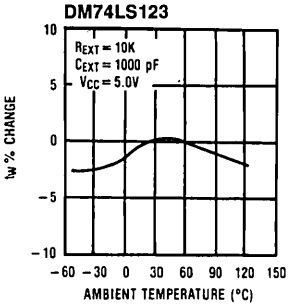
Typical Output Pulse Width Variation vs Ambient Temperature

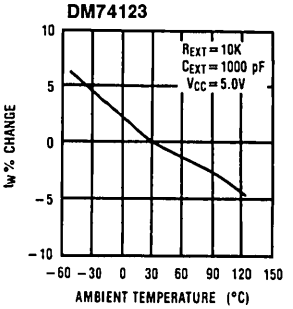
The graphs shown below demonstrate the typical shift in the device output pulse widths as a function of temperature. It should be noted that these graphs represent the temperature shift of the device after being corrected for any temperature shift in the timing components. Any shift in these components will result in a corresponding shift in the pulse width, as well as any shift due to the device itself.









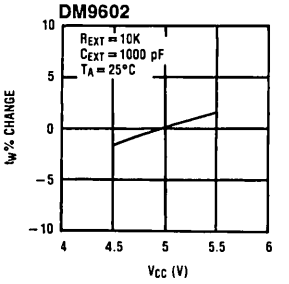


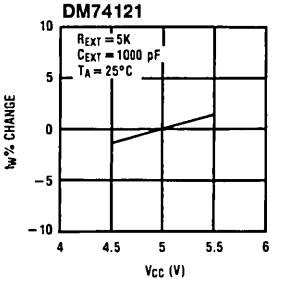
TL/F/7508–10

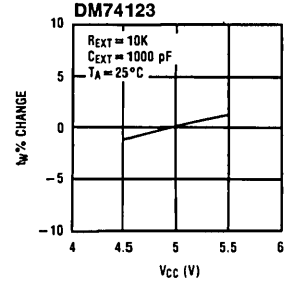
Typical Output Pulse Width Variation vs Supply Voltage

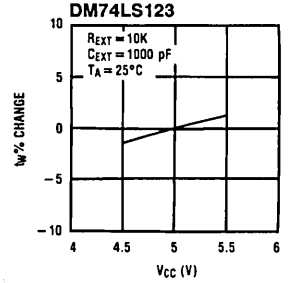
The following graphs show the dependence of the pulse width on V_{CC}.

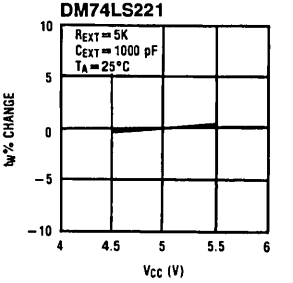
As with any IC applications, the device should be properly bypassed so that large transient switching currents can be easily supplied by the bypass capacitor. Capacitor values of 0.001 μF to 0.10 μF are generally used for the V_{CC} bypass capacitor.







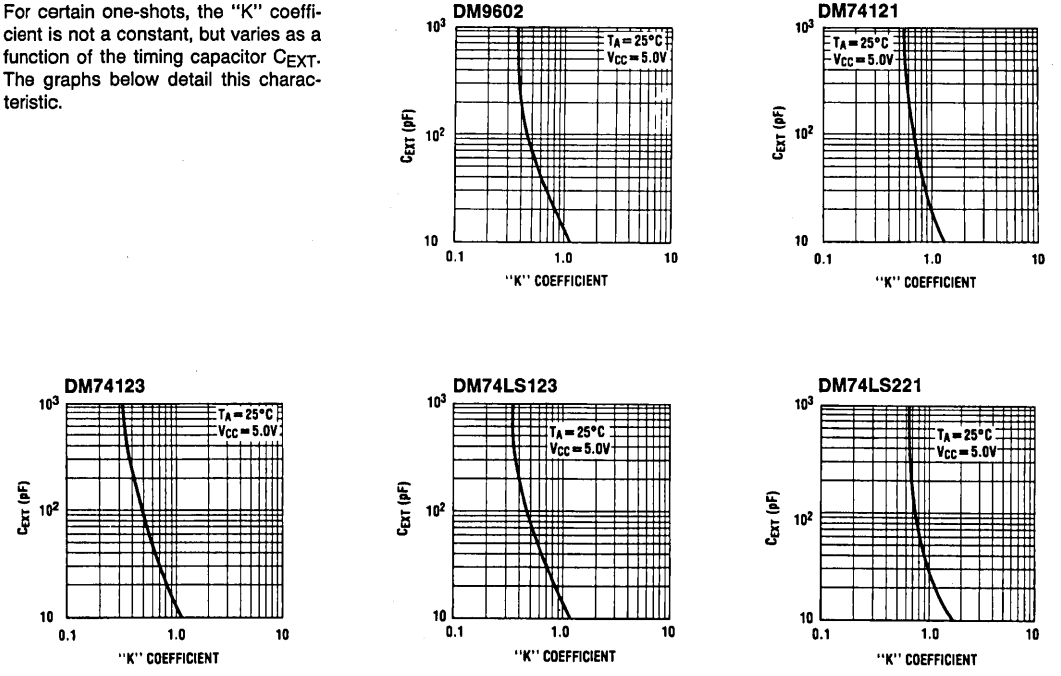




TL/F/7508–11

Typical "K" Coefficient Variation vs Timing Capacitance

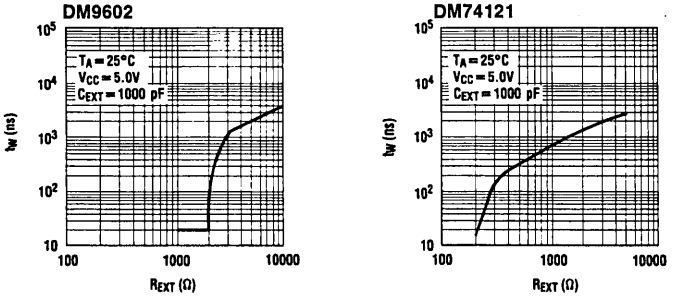
For certain one-shots, the "K" coefficient is not a constant, but varies as a function of the timing capacitor C_{EXT}. The graphs below detail this characteristic.



TL/F/7508–12

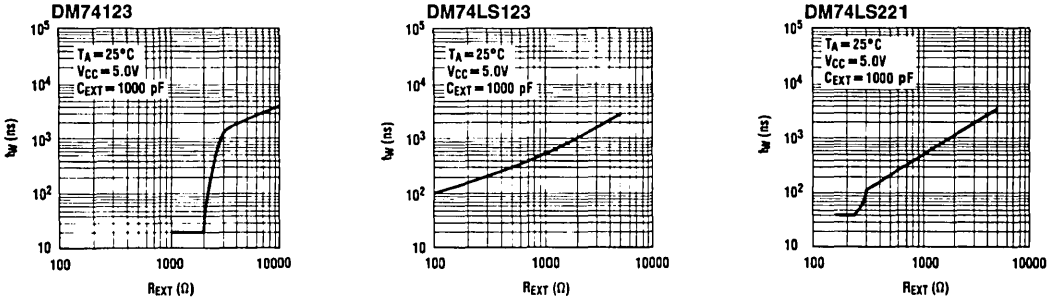
Typical Output Pulse Width vs Minimum Timing Resistance

The plots shown below demonstrate typical pulse widths and limiting values of the true output as a function of the external timing resistor, R_{EXT}. This information should evaporate those years of mysterious notions and numerous concerns about operating one-shots with lower that recommended minimum R_{EXT} values.



TL/F/7508–13

Typical Output Pulse Width vs Minimum Timing Resistance (Continued)



TL/F/7508–14

Function Tables

'121 One-Shots

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

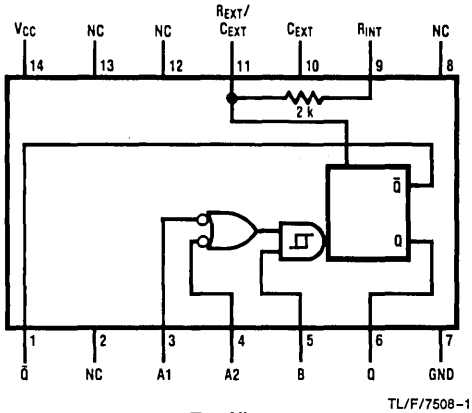
'122 Retriggerable One-Shots with Clear

Inputs					Outputs	
Clear	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
X	L	X	H	H	L	H
H	L	X	↑	H	⎍	⎎
H	L	X	H	↑	⎍	⎎
H	X	L	H	H	L	H
H	X	L	↑	H	⎍	⎎
H	X	L	H	↑	⎍	⎎
H	H	↓	H	H	⎍	⎎
H	↓	↓	H	H	⎍	⎎
H	↓	H	H	H	⎍	⎎
↑	L	X	H	H	⎍	⎎
↑	X	L	H	H	⎍	⎎

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Connection Diagrams

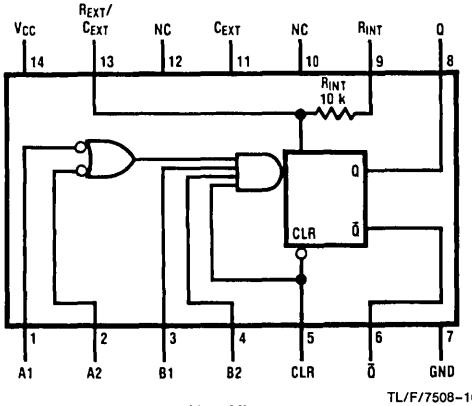
54121 (J, W); 74121 (N)



TL/F/7508–15

Top View

54LS122 (J, W); 74LS122 (N)



TL/F/7508–16

Top View

Function Tables (Continued)

'123 Dual Retriggerable One-Shots with Clear
'123

Inputs			Outputs	
A	A	Clear	Q	$\overline{Q}$
H	X	H	L	H
X	L	H	L	H
L	↑	H	⎍	⎎
↓	H	H	⎍	⎎
X	X	L	L	H

'LS123

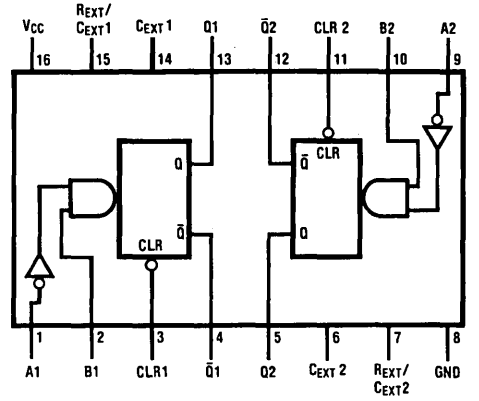
Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

8602

Pin Numbers			Operation
A	B	CLEAR	
↓	L	H	Trigger
H	↑	H	Trigger
X	X	L	Reset

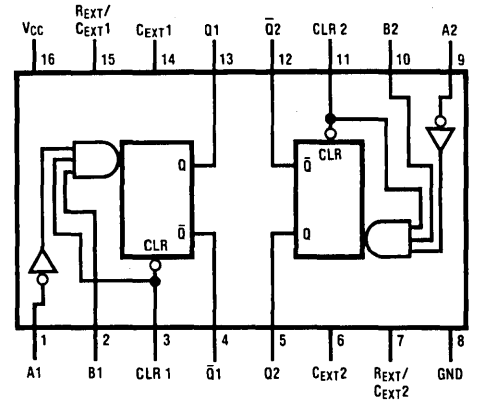
H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Connection Diagrams (Continued)



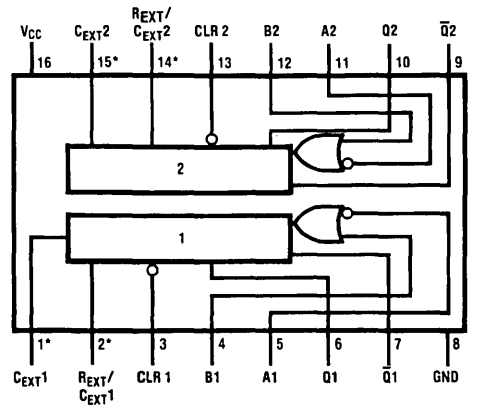
TL/F/7508–17

Top View
54LS123 (J, W); 74LS123 (N)



TL/F/7508–18

Top View
9602 (J, W); 8602 (N)



TL/F/7508–19

Top View

*Pins for external timing.

Function Tables (Continued)

'221 Dual One-Shots with Schmitt Trigger Inputs

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

8601

Inputs				Outputs	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎎
L	X	H	↑	⎍	⎎
X	L	H	H	L	H
X	L	↑	H	⎍	⎎
X	L	H	↑	⎍	⎎
H	↓	H	H	⎍	⎎
↓	↓	H	H	⎍	⎎
↓	H	H	H	⎍	⎎

H = HIGH Level
L = LOW Level
↑ = Transition from LOW-to-HIGH
↓ = Transition from HIGH-to-LOW
⎍ = One HIGH Level Pulse
⎎ = One LOW Level Pulse
X = Don't Care

Applications

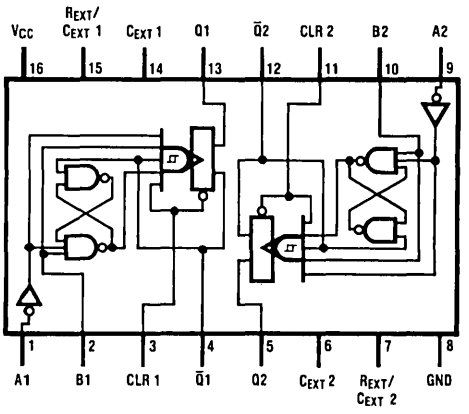
The following circuits are shown with generalized one-shot connection diagram.

NOISE DISCRIMINATOR *(Figure 8)*

The time constant of the one-shot (O-S) can be adjusted so that an input pulse width narrower than that determined by the time constant will be rejected by the circuit. Output at Q_2 will follow the desired input pulse, with the leading edge delayed by the predetermined time constant. The output pulse width is also reduced by the amount of the time constant from R_X and C_X.

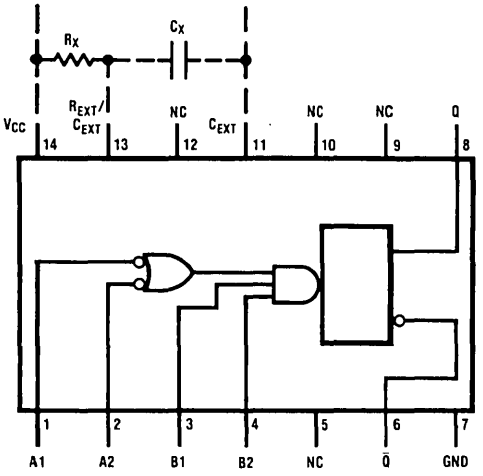
Connection Diagrams (Continued)

54LS221 (J, W); 74LS221 (N)

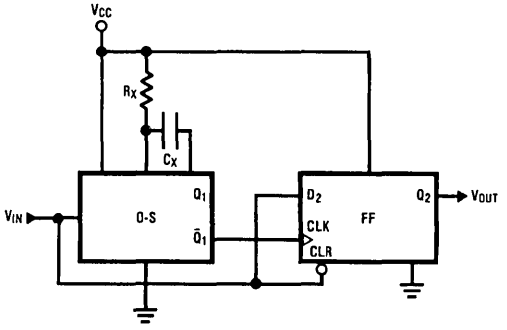


Top View TL/F/7508-20

9601 (J, W); 8601 (N)

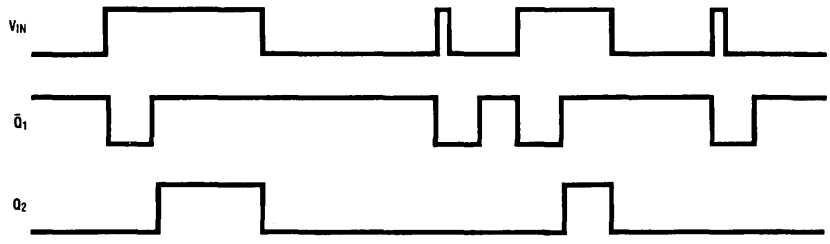


Top View TL/F/7508-21



TL/F/7508-22

FIGURE 8. Noise Discriminator

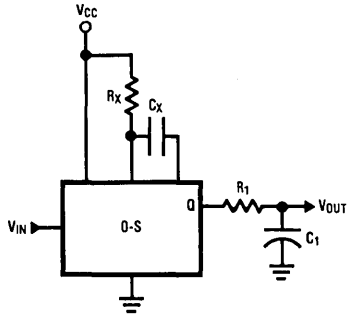


TL/F/7508–23

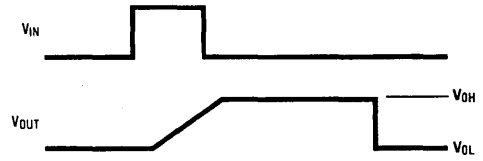
FIGURE 8. Noise Discriminator (Continued)

FREQUENCY DISCRIMINATOR ***(Figure 9)***

The circuit shown in *Figure 9* can be used as a frequency-to-voltage converter. For a pulse train of varying frequency applied to the input, the one-shot will produce a pulse constant width for each triggering transition on its input. The output pulse train is integrated by R_1 and C_1 to yield a waveform whose amplitude is proportional to the input frequency. (Retriggerable device required.)



TL/F/7508–24

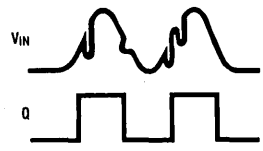


TL/F/7508–25

FIGURE 9. Frequency Discriminator

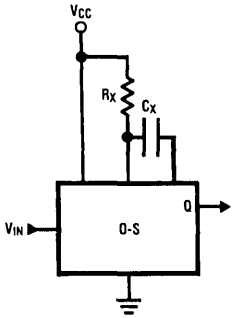
ENVELOPE DETECTOR ***(Figures 10a and 10b)***

An envelope detector can be made by using the one-shot's retrigger mode. The time constant of the device is selected to be slightly longer than the period of each cycle within the input pulse burst. Two distinct DC levels are present at the output for the duration of the input pulse burst and for its absence (see *Figure 10a*). The same circuit can also be employed for a specific frequency input as a Schmitt trigger to obviate input trigger problems associated with hysteresis and slow varying, noisy waveforms (see *Figure 10b*). (Retriggerable device required.)

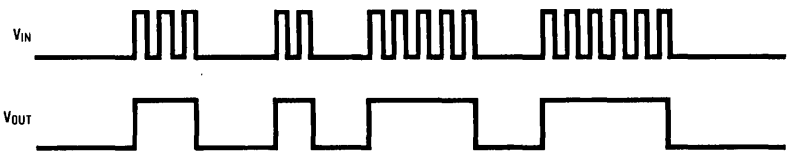


TL/F/7508–27

FIGURE 10b. Schmitt Trigger



TL/F/7508–26

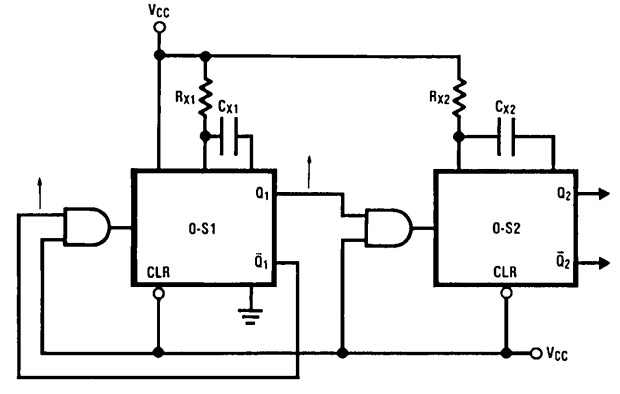


TL/F/7508–28

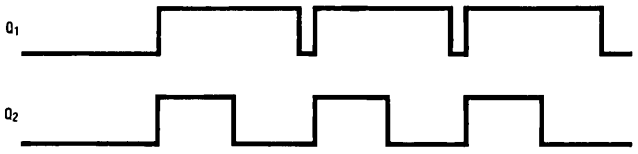
FIGURE 10a. Envelope Detector (Retriggerable Device Required)

PULSE GENERATOR *(Figure 11)*

Two one-shots can be connected together to form a pulse generator capable of variable frequency and independent duty cycle control. The R_{X1} and C_{X1} of O–S1 determine the frequency developed at output Q_1. R_{X2} and C_{X2} of O–S2 determine the output pulse width at Q_2. (Retriggerable device required.)



TL/F/7508–29



$$\text{DUTY CYCLE} = \frac{R_{X2}\,C_{X2}}{R_{X1}\,C_{X1}}$$

$$\text{FREQ} = \frac{1}{K\,R_{X1}\,C_{X1}}$$

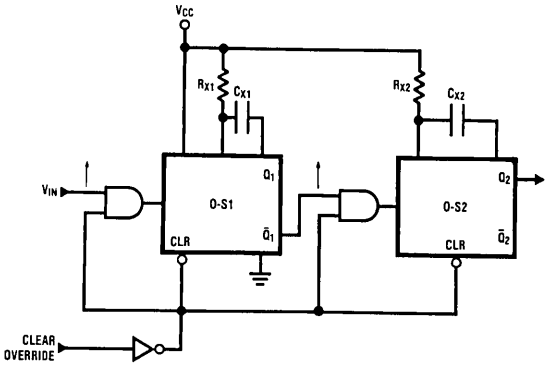
TL/F/7508–30

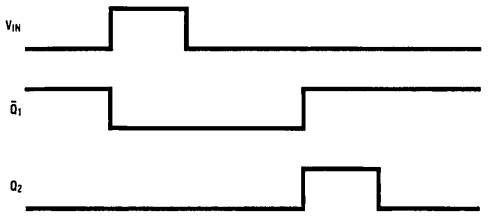
FIGURE 11. Pulse Generator (Retriggerable Device Required)

Note: K is the multiplication factor dependent of the device. Arrow indicates edge-trigger mode.

DELAYED PULSE GENERATOR WITH OVERRIDE TO TERMINATE OUTPUT PULSE *(Figure 12)*

An input pulse of a particular width can be delayed with the circuit shown in *Figure 12*. Preselected values of R_{X1} and C_{X1} determine the delay time via O–S1, while preselected values of R_{X2} and C_{X2} determine the output pulse width through O–S2. The override input can additionally serve to modify the output pulse width.





TL/F/7508–32

TL/F/7508–31

FIGURE 12. Delayed Pulse Generator with Override to Terminate Output Pulse

MISSING PULSE DETECTOR ***(Figure 13)***

By setting the time constant of O–S1 through R_{X1} and C_{X1} to be the least one full period of the incoming pulse period, the one-shot will be continuously retriggered as long as no missing pulse occurs. Hence, $\overline{Q}_1$ remains LOW until a pulse is missing in the incoming pulse train, which then triggers O–S2 and produces an indicating pulse at Q_2. (Retriggerable device required.)

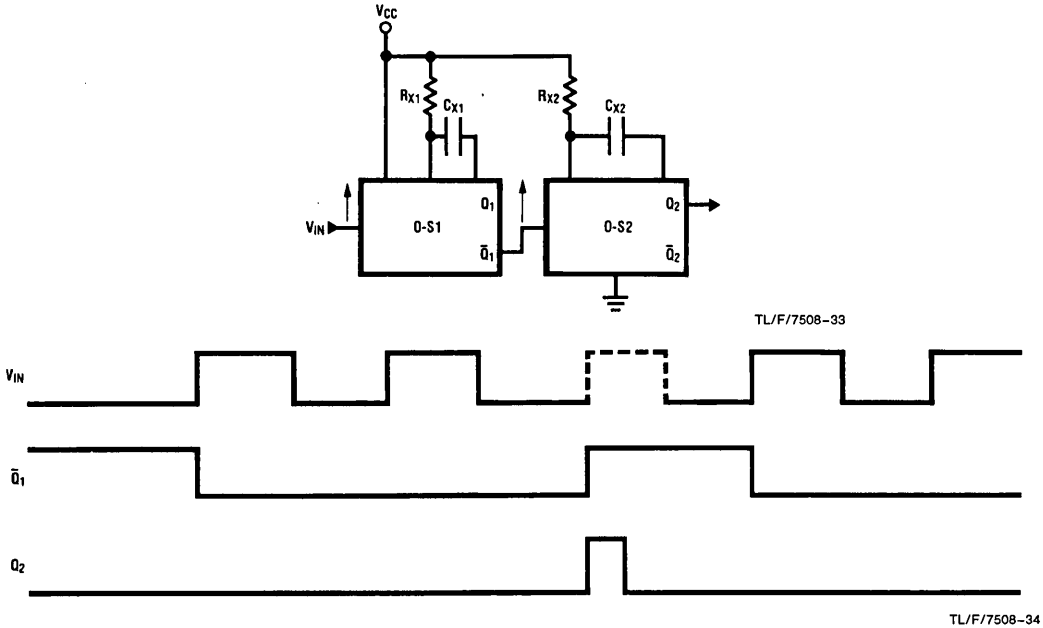


FIGURE 13. Missing Pulse Detector (Retriggerable Device Required)

PULSE WIDTH DETECTOR ***(Figure 14)***

The circuit of *Figure 14* produces an output pulse at V_{OUT} if the pulse width at V_{IN} is wider than the predetermined pulse width set by R_X and C_X.

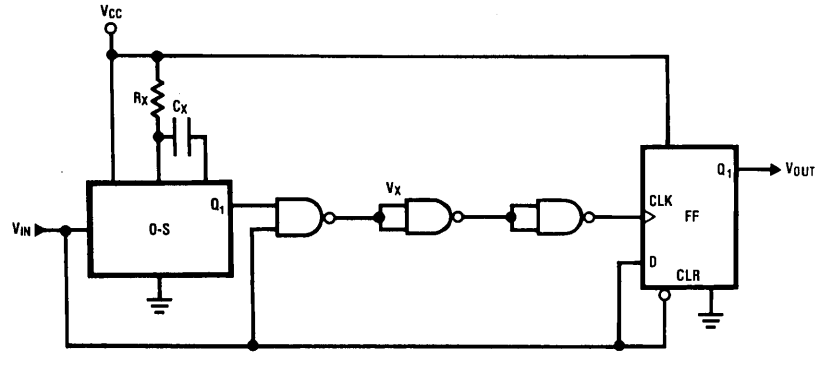
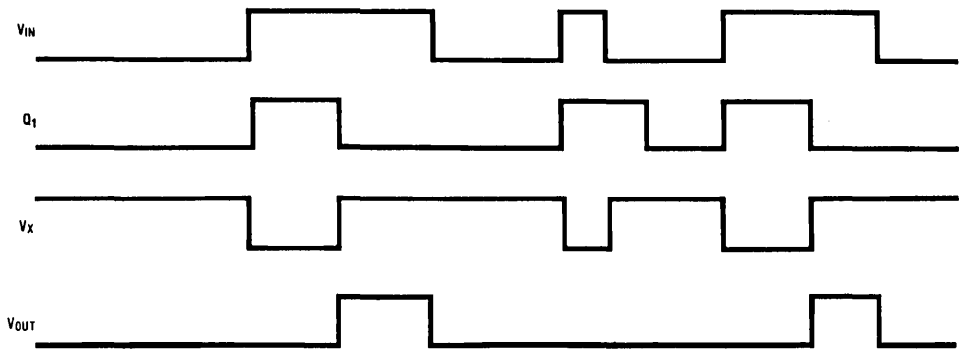


FIGURE 14. Pulse Width Detector

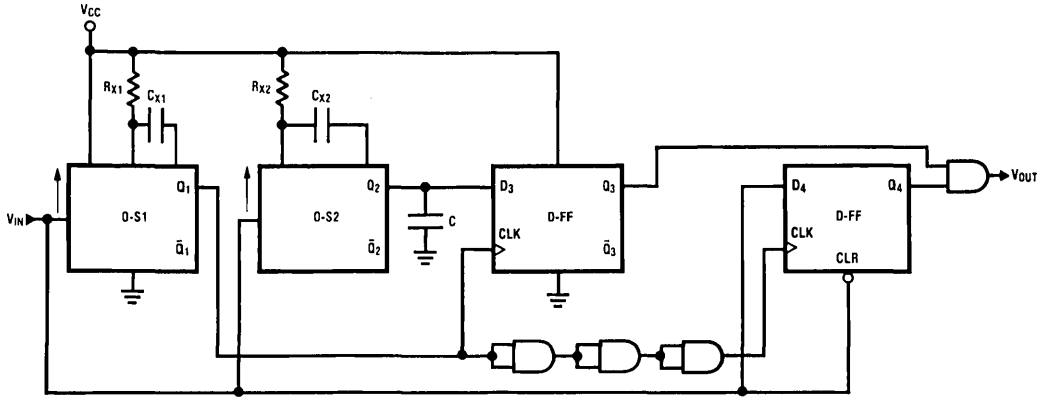


TL/F/7508–36

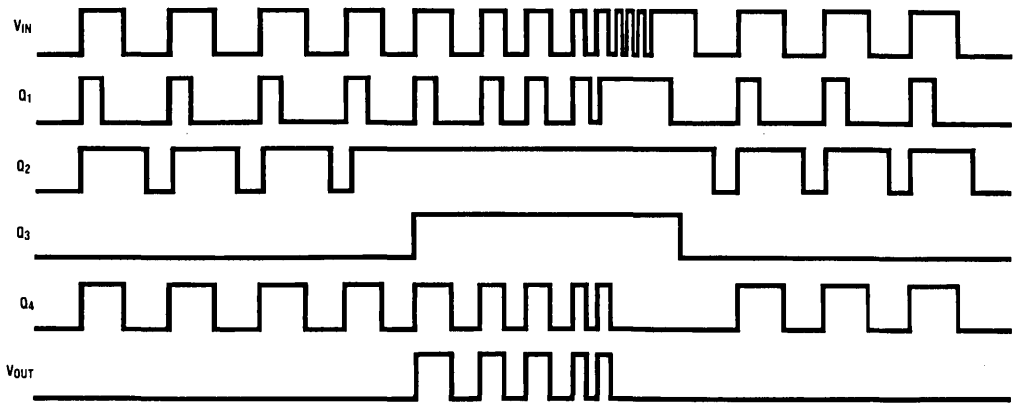
FIGURE 14. Pulse Width Detector (Continued)

BAND PASS FILTER ***(Figure 15)***

The band pass of the circuit is determined by the time constants of the two low-pass filters represented by O-S1 and O-S2. With the output at Q_2 delayed by C, the D-flip flop (D-FF) clocks HIGH only when the cutoff frequency of O-S2 has been exceeded. The output at Q_3 is gated with the delayed input pulse train at Q_4 to produce the desired output. (Retriggerable device required.)



TL/F/7508–37



TL/F/7508–38

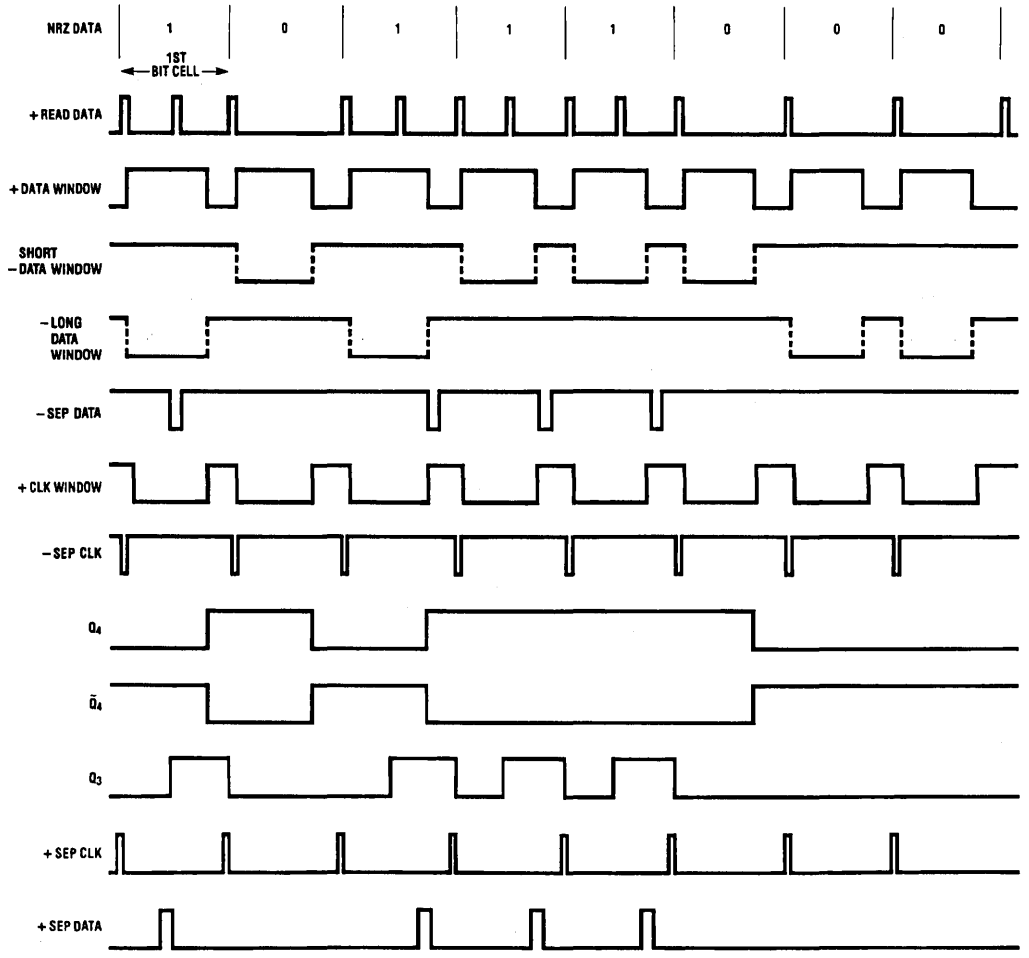
FIGURE 15. Band Pass Filter (Retriggerable Device Required)

FM DATA SEPARATOR ***(Figure 16)***

The data separator shown in *Figure 16* is a two-time constant separator that can be used on tape and disc drive memory storage systems. The clock and data pulses must fall within prespecified time windows. Both the clock and data windows are generated in this circuit. There are two data windows; the short window is used when the previous bit cell had a data pulse in it, while the long window is used when the previous bit cell had no data pulse.

If the data pulse initially falls into the data window, the —SEP DATA output returns to the NAND gate that generates the data window, to assure that the full data is allowed through before the window times out. The clock windows will take up the remainder of the bit cell time.

Assume all one-shots and flip-flops are reset initially and the +READ DATA has the data stream as indicated. With O–S1 and O–S2 inactive, +CLK WINDOW is active. The first +READ DATA pulse will be gated through the second AND gate, which becomes —SEP CLK for triggering of the R–S FF and the one-shots. With the D–FF off, O–S1 will remain reset. The —SEP CLK pulse will trigger O–S2, whose output is sent to the OR gate, and its output becomes +DATA WINDOW to enable the first AND gate. The next pulse on +READ DATA wil be allowed through the first AND gate to become —SEP DATA. This pulse sets the R–S FF, whose HIGH output becomes the data to the D–FF. The D–FF is clocked on by O–S2 timing out and +CLK WINDOW becoming active. $\overline{Q}_4$ will hold O–S2 reset and allow O–S1 to trigger on the next clock pulse.

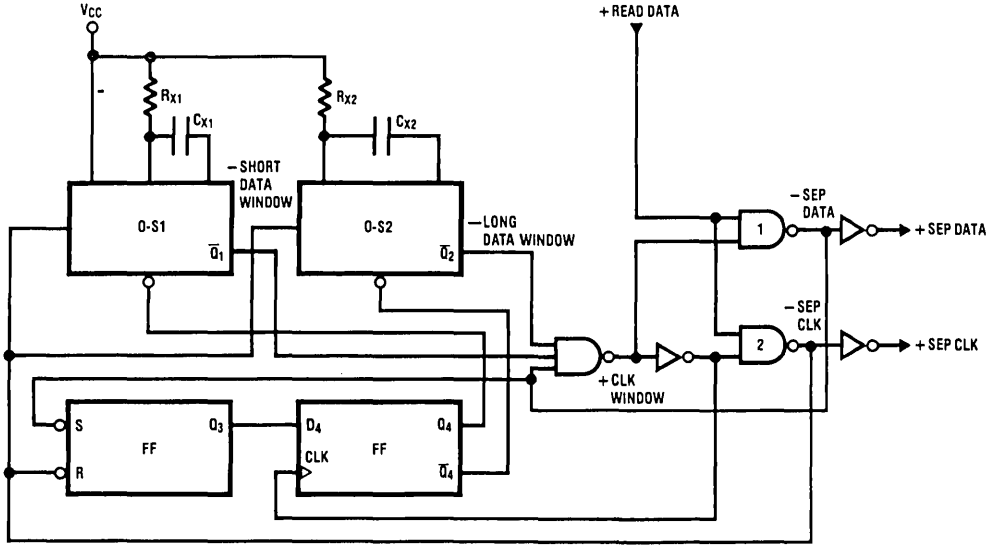


TL/F/7508–39

FIGURE 16. FM Data Separator

The next clock pulse (the second bit cell) is ANDed with +CLK WINDOW and becomes the next —SEP CLK, which will reset the R–S FF and trigger O–S1. As O–S1 becomes active, the +DATA WINDOW becomes active, enabling the first AND gate. With no data bit in the second bit cell, the R–S FF will remain reset, enabling the D–FF to be clocked off when +DATA WINDOW falls. When the D–FF is clocked off, Q_4 will hold O–S1 reset and allow O–S2 to be triggered.

The third clock pulse (bit cell 3) is ANDed with +CLK WINDOW and becomes —SEP CLK, which continues resetting the R–S FF and triggers O–S2. When O–S2 becomes active, +DATA WINDOW enables the first AND gate, allowing the data pulse in bit cell 3 to become —SEP DATA. This —SEP DATA will set the R–S FF, which enables the D–FF to be clocked on when +DATA WINDOW falls. When this happens, Q_4 will hold O–S2 reset and allow O–S1 to trigger. This procedure continues as long as there is clock and data pulse stream present on the +READ DATA line.



TL/F/7508–40

FIGURE 16. FM Data Separator (Continued)

PHASE-LOCKED LOOP VCO *(Figure 17)*

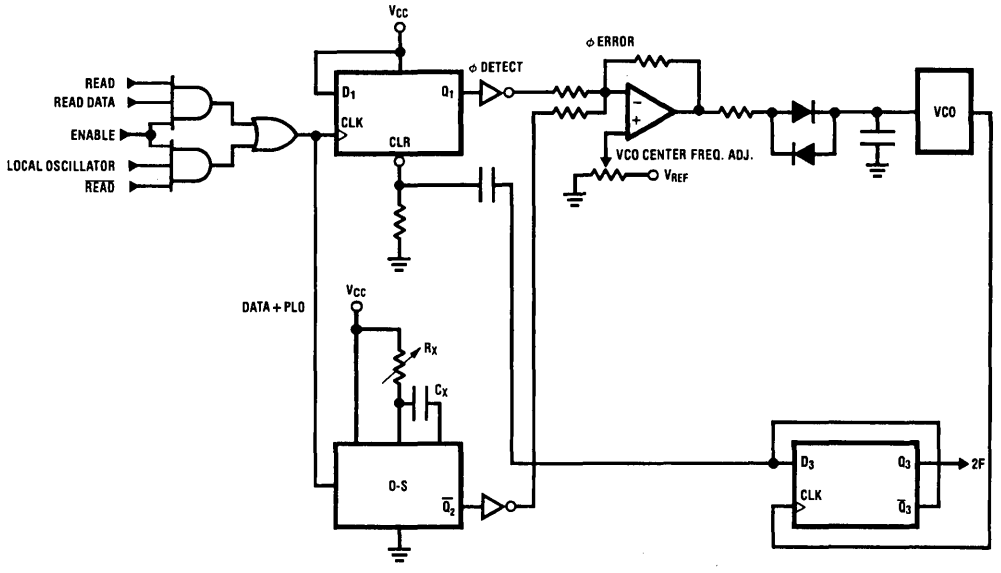
The circuit shown in *Figure 17* represents the VCO in the data separation part of a rotational memory storage system which generates the bit rate synchronous clocks for write data timing and for establishing the read data windows.

The op-amp that performs the phase-lock control operates by having its inverting input be driven by two sources that normally buck one another. One source is the one-shot, the other source is the phase detector flip-flop. When set, the one-shot, through an inverter, supplies a HIGH-level voltage to the summing node of the op-amp and the phase detector FF, also through an inverter, supplies a canceling LOW-level input.

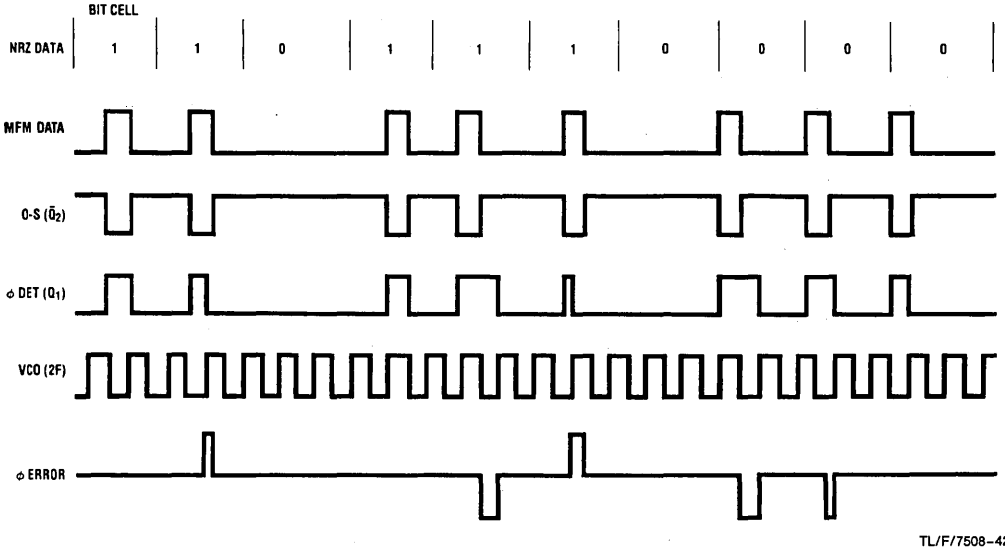
It is only when the two sources are out of phase with each other, that is one HIGH and the other LOW, that a positive- or negative-going phase error will be applied to the op-amp to effect a change in the VCO frequency. *Figure 17* illustrates the process of phase-error detection and correction when synchronizing to a data bit pattern. The rising edge of each pulse at DATA+PLO clocks the one-shot LOW and the phase detector FF HIGH. Since both outputs are still bucking each other, no change will be observed at the phase-error summing node. When the one-shot times out, if this occurs after the 2F clock has reset the phase detector FF to a LOW output, a positive pulse will be seen at the summing node until both the one-shot and the FF are reset. Any positive pulse will be reflected by a negative change in the op-amp output, which is integrated and reduces the positive control voltage at the VCO input in direct proportion to the duration of the phase-error pulse. A negative phase-error pulse occurs when the phase detector FF remains set longer than the one-shot.

Negative phase-error pulse causes the integrated control voltage to swing positive in direct proportion to the duration of the phase-error pulse. It is recommended that a clamping circuit be connected to the output of the op-amp to prevent the VCO control voltage from going negative or more positive than necessary. A back-to-back diode pair connected between the op-amp and the VCO is highly recommended, for it will present a high impedance to the VCO input during locked mode. This way, stable and smooth operation of the PLO circuit is assured.

2F Bit Rate Synchronous Read/Write Clock



TL/F/7508–41



TL/F/7508–42

FIGURE 17. Phase-Locked Loop Voltage Controlled Oscillator

A FINAL NOTE

It is hoped that this brief note will clarify many pertinent and subtle points on the use and testing of one-shots. We invite your comments to this application note and solicit your constructive criticism to help us improve our service to you.

ACKNOWLEDGEMENT

The author wishes to thank Stephen Wong, Bill Llewellyn, Walt Sirovy, Dennis Worden, Stephen Yuen, Weber Lau, Chris Henry and Michelle Fong for their help and guidance.

Functional Index/Selection Guide

*Several methods are used to represent typical values. For propagation delay typical values, the average of the typical values of the two delays are used.

$$\left[\frac{t_{PHL(TYP)} + t_{PLH(TYP)}}{2}\right]$$

For power dissipation, the average of the typical values of current for all states the outputs can achieve is used (I_{CCL}, I_{CCH}, I_{CCZ}.) This current value is multiplied by nominal supply voltage (5V), and in some cases divided by the number of gates, bits, etc. All other typical values are singular typicals.

Adders

Description	Device Type	Typ* Carry Time (ns)	Typ* Add Time (ns)	Typ* Power Diss./Bit (mW)	Package Availability		Page
					Mil	Com	
Single 4-Bit Full Adders	54/74LS283	12	15	24	J	N,M	2-208
	54/74S283	8.5	11	110	J	N	3-114
	54/74LS83A	12	15	24	J	N,WM	2-57

Arithmetic Logic Units, Carry Look-Ahead Generators

Description	Device Type	Typ* Carry Time (ns)	Typ* Add Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
					Mil	Com	
4-Bit ALU/ Function Generators	54/74AS181B	5	5	370	J	N	†
	54/74S181	7	14	600	J	N	3-74
	54/74181	12.5	18	455	J	N	4-177
	54/74S381	10	12	525	J	N	3-128
	54/74AS881B	5	5	370	J	N	†
Carry Look-Ahead Generator	54/74AS182	5	N/A	115	J	N	†
	54/74S182	9	N/A	345	J	N	3-83
	54/74AS264	6	N/A	140	J	N	†
	54/74AS282	6	N/A	130	J	N	†

Buffers/Clock Drivers with Totem-Pole Outputs

Description	Device Type	Low-Level Output Current (mA)	High-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Dual 4-Input NAND Buffers	54ALS40A	12	−1	4	3.5	J		†
	74ALS40A	24	−2.6	4	3.5		N,M	†
	54/74S40	60	−3	4	44	J	N	3-27
	54ALS1020A	12	−1	4	3.6	J		†
	74ALS1020A	24	−2.6	4	3.6		N,M	†
Quad 2-Input NAND Buffers	54ALS37A	12	−1	5	5	J		†
	74ALS37A	24	−2.6	5	5		N,M	†
	54LS37	12	−1.2	10	4.3	J		2-39
	74LS37	24	−1.2	10	4.3		N,M	2-39
	54/7437	48	−1.2	10.5	27	J	N	4-53
	54ALS1000A	12	−1	5	3.5	J		†
	74ALS1000A	24	−2.6	5	3.5		N,M	†
	54AS1000A	40	−40	2	8.5	J	N	†
	74AS1000A	48	−48	2	8.5	J	N	†

† Please see the ALS/AS Databook for this datasheet.

Buffers/Clock Drivers with Totem-Pole Outputs (Continued)

Description	Device Type	Low-Level Output Current (mA)	High-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Quad 2-Input NOR Buffers	54ALS28A	12	−1	3.7	4.5	J		†
	74ALS28A	24	−2.6	3.7	4.5		N,M	†
	54ALS1002A	12	−1	3.7	4.5	J		†
	74ALS1002A	24	−2.6	3.7	4.5		N,M	†
	54AS1036A	40	−40	2	9.7	J		†
	74AS1036A	48	−48	2	9.7		N	†
Quad 2-Input OR	54ALS1032A	12	−1	5.5	5.7	J		†
	74ALS1032A	24	−2.6	5.5	5.7		N,M	†
	54AS1032A	40	−40	2.5	14	J		†
	74AS1032A	48	−48	2.5	14		N	†
Quad 2-Input AND	54ALS1008A	12	−1	5.6	4.7	J		†
	74ALS1008A	24	−2.6	5.6	4.7		N,M	†
	54AS1008A	40	−40	2.5	12	J		†
	74AS1008A	48	−48	2.5	12		N	†
Triple 3-Input NAND	54ALS1010A	12	−1	4	3.6	J		†
	74ALS1010A	24	−2.6	4	3.6		N,M	†
Triple 3-Input AND	54ALS1011A	12	−1	6.4	4.75	J		†
	74ALS1011A	24	−2.6	6.4	4.75		N,M	†
Hex Buffers	54ALS1034	12	−12	4.5	4.6	J		†
	74ALS1034	24	−15	4.5	4.6		N,M	†
	54AS1034A	40	−40	2.5	11.9	J		†
	74AS1034A	48	−48	2.5	11.9		N	†
Hex Inverter Buffers	54ALS1004	12	−12	2.6	3.3	J		†
	74ALS1004	24	−15	2.6	3.3		N,M	†
	54AS1004A	40	−40	1.7	8.5	J		†
	74AS1004A	48	−48	1.7	8.5		N	†

Buffers/Clock Drivers with Open-Collector Outputs

Description	Device Type	High-Level Output Voltage V	Low-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Quad 2-Input NAND Buffers	54ALS38A	5.5	12	14.5	3.5	J		†
	74ALS38A	5.5	24	14.5	3.5		N,M	†
	54LS38	5.5	12	15	4.3	J		2-41
	74LS38	5.5	24	15	4.3		N,M	2-41
	54/7438	5.5	48	12.5	24.4	J	N,M	4-55
	54LS26	15	4	16	2	J		2-31
	74LS26	15	8	16	2		N,M	2-31
	54/7426	15	16	13.5	10	J	N	4-45
	54ALS1003A	5.5	12	14.5	3.5	J		†
	74ALS1003A	5.5	24	14.5	3.5		N,M	†

† Please see the ALS/AS Databook for this datasheet.

Buffers/Clock Drivers with Open-Collector Outputs (Continued)

Description	Device Type	High-Level Output Voltage (V)	Low-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Quad 2-Input NOR Buffers	54ALS33A	5.5	12	13.5	4.5	J		†
	74ALS33A	5.5	24	13.5	4.5		N,M	†
Hex Buffers/ Drivers	5407	30	30	13	21	J		4-28
	7407	30	40	13	21		N,M	4-28
	5417	15	30	13	21	J		4-41
	7417	15	40	13	21		N	4-41
	54ALS1035	5.5	12	12.5	4.6	J		†
	74ALS1035	5.5	24	12.5	4.6		N,M	†
Hex Inverter Buffers/ Drivers	5406	30	30	12.5	26	J		4-26
	7406	30	40	12.5	26		N,M	4-26
	5416	15	30	12.5	26	J		4-39
	7416	15	40	12.5	26		N	4-39
	54ALS1005	5.5	12	12.5	3.3	J		†
	74ALS1005	5.5	24	12.5	3.3		N, M	†

Buffer Gates with TRI-STATE® Totem-Pole Outputs

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Quad Buffers	54LS125A	−1	12	10	14.4	J		2-92
	74LS125A	−2.6	24	10	14.4		N,M	2-92
	54125	−2	16	11	40	J		4-114
	74125	−5.2	16	11	40		N	4-114
	54LS126A	−1	12	10	14.4	J		2-95
	74LS126A	−2.6	24	10	14.4		N,M	2-95
Hex Buffers	54LS365A	−1	12	10	10.8	J		2-223
	74LS365A	−2.6	24	10	10.8		N,M	2-223
	54365	−2	32	10.5	51.6	J		4-210
	74365	−5.2	32	10.5	51.6		N	4-210
	54LS367A	−1	12	10	10.8	J		2-229
	74LS367A	−2.6	24	10	10.8		N,M	2-229
	54367	−2	32	12	51.6	J		4-213
	74367	−5.2	32	12	51.6		N	4-213
Hex Inverter Buffers	54LS366A	−1	12	10	10.8	J		2-226
	74LS366A	−2.6	24	10	10.8		N,M	2-226
	54LS368A	−1	12	10	10.8	J		2-232
	74LS368A	−2.6	24	10	10.8		N,M	2-232
	54368	−2	32	10.5	51.6	J		4-216
	74368	−5.2	32	10.5	51.6		N	4-216

† Please see the ALS/AS Databook for this datasheet.

Buffer Gates with TRI-STATE® Totem-Pole Outputs (Continued)

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Octal Buffers	54ALS465A	−12	12	6.6	8.6	J		†
	74ALS465A	−15	24	6.6	8.6		N,M	†
	54LS465	−2.6	12	14.5	10	J		2-247
	74LS465	−5.2	24	14.5	10		N,M	2-247
	54ALS467A	−12	12	6.6	9.1	J		†
	74ALS467A	−15	24	6.6	9.1		N,M	†
	54LS467	−2.6	12	14.5	10	J		2-247
	74LS467	−5.2	24	14.5	10		N,M	2-247
	54ALS2541	−12	12	6	10.8	J		†
	74ALS2541	−15	24	6	10.8		N,M	†
	54ALS541	−12	12	6	10.8	J		†
	74ALS541	−15	24	6	10.8		N,M	†
Octal Inverter Buffers	54ALS466A	−12	12	4.8	7.5	J		†
	74ALS466A	−15	24	4.8	7.5		N,M	†
	54LS466	−2.6	12	9.5	8	J		2-247
	74LS466	−5.2	24	9.5	8		N,M	2-247
	54ALS468A	−12	12	4.7	7.5	J		†
	74ALS468A	−15	24	4.7	7.5		N,M	†
	54LS468	−2.6	12	9.5	8	J		2-247
	74LS468	−5.2	24	9.5	8		N,M	2-247
	54ALS540	−12	12	6.6	10.8	J		†
	74ALS540	−15	24	6.6	10.8		N,M	†
	54ALS5620	−12	12	6.6	18.3	J		†
	74ALS5620	−15	24	6.6	18.3		N,M	†
Quad Inverter Transceivers	54ALS242A	−12	12	5.6	16.3	J		†
	74ALS242A	−15	24	5.6	16.3		N,M	†
	54AS242	−12	48	3.5	33.8	J		†
	74AS242	−15	64	3.5	33.8		N	†
Quad Transceivers	54ALS243A	−12	12	6	23.3	J		†
	74ALS243A	−15	24	6	23.3		N,M	†
	54AS243	−12	48	4	45.8	J		†
	74AS243	−15	64	4	45.8		N	†
	54LS243	−15	12	12	34.5	J		2-182
	74LS243	−15	24	12	34.5		N,M	2-182
Octal Inverter Bus Buffers/ Drivers	54AS231	−12	40	3.5	18.5	J		†
	74AS231	−15	48	3.5	18.5		N	†
	54ALS240A	−12	12	2.6	6.5	J		†
	74ALS240A	−15	24	2.6	6.5		N,WM	†
	54AS240	−12	48	3.5	19.2	J		†
	74AS240	−15	64	3.5	19.2		N	†
	54LS240	−12	12	10	14.2	J		2-179
	74LS240	−15	24	10	14.2		N,WM	2-179
	54S240	−12	48	5	56.3	J		3-95
	74S240	−15	64	5	56.3		N,WM	3-95
	54S940	−12	48	5	56.3	J		3-132
	74S940	−15	64	5	56.3		N	3-132
	54ALS1240A	−12	8	9	5.9	J		†
	74ALS1240A	−15	16	9	5.9		N,WM	†

† Please see the ALS/AS Databook for this datasheet.

Buffer Gates with TRI-STATE® Totem-Pole Outputs (Continued)

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Octal Bus Buffers/ Drivers	54ALS241A	−12	12	4.3	8.6	J		†
	74ALS241A	−15	24	4.3	8.6		N,WM	†
	54AS241	−12	48	4	24.6	J		†
	74AS241	−15	64	4	24.6		N	†
	54LS241	−12	12	10	14.2	J		2-179
	74LS241	−15	24	10	14.2		N,WM	2-179
	54S241	−12	48	5	67.2	J		3-95
	74S241	−15	64	5	67.2		N	3-95
	54ALS244A	−12	12	4.3	8.5	J		†
	74ALS244A	−15	24	4.3	8.5		N,WM	†
	54AS244	−12	48	4	24.1	J		†
	74AS244	−15	64	4	24.1		N	†
	54LS244	−12	12	10	24.6	J		2-185
	74LS244	−15	24	10	24.6		N,WM	2-185
	54S244	−12	48	5	67.2	J		3-95
	74S244	−15	64	5	67.2		N	3-95
	54S941	−12	48	5	67.2	J		3-132
	74S941	−15	64	5	67.2		N,WM	3-132
	54ALS1241A	−12	12	9	5.9	J		†
	74ALS1241A	−15	24	9	5.9		N,WM	†
	54ALS1244A	−12	12	9	5.9	J		†
	74ALS1244A	−15	24	9	5.9		N,WM	†
Octal Transceivers	54ALS245A	−12	12	9	21.7	J		†
	74ALS245A	−15	24	9	21.7		N,WM	†
	54AS245	−12	32	5.5	49.1	J		†
	74AS245	−15	48	5.5	49.1		N	†
	54LS245	−12	12	8	36.3	J		2-188
	74LS245	−15	24	8	36.3		N,WM	2-188
	54ALS645A	−12	12	5	21.7	J		†
	74ALS645A	−15	24	5	21.7		N,WM	†
	54AS645	−12	48	5.5	49.2	J		†
	74AS645	−15	64	5.5	49.2		N	†
	54LS645	−12	12	8	36	J		2-251
	74LS645	−15	24	8	36		N,WM	2-251
	54ALS1243A	−12	8	7	19	J		†
	74ALS1243A	−15	16	7	19		N,WM	†
	54ALS1245A	−12	8	9	14	J	N,WM	†
	74ALS1245A	−15	16	9	14	J	N,WM	†
	54ALS1645A	−12	8	7.5	14.4	J		†
	74ALS1645A	−15	16	7.5	14.4		N,WM	†

† Please see the ALS/AS Databook for this datasheet.

Buffer Gates with TRI-STATE® Totem-Pole Outputs (Continued)

Description	Device Type	Max Source Current (mA)	Max Sink Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Octal Inverter Transceivers	54ALS620A	−12	12	8	14.6	J		†
	74ALS620A	−15	24	8	14.6		N,WM	†
	54AS620	−12	48	5.5	32.7	J		†
	74AS620	−15	64	5.5	32.7		N	†
	54ALS640A	−12	12	5	15.4	J		†
	74ALS640A	−15	24	5	15.4		N,WM	†
	54AS640	−12	48	4	32.9	J		†
	74AS640	−15	64	4	32.9		N	†
	54ALS1242A	−12	12	5	10.9	J		†
	74ALS1242A	−15	24	5	10.9		N,WM	†
Octal Transceivers with True and Inverting Outputs	54AS230	−12	48	3.5	20.8	J		†
	74AS230	−15	64	3.5	20.8		N	†
Octal Transceivers with Register Storage	54AS646	−12	32	5	93.8	J		†
	74AS646	−15	48	5	93.8		N	†
	54AS652	−12	32	5	93.8	J		†
	74AS652	−15	48	5	93.8		N	†
Octal Inverter Transceivers with Register Storage	54AS648	−12	32	6	81.3	J		†
	74AS648	−15	48	6	81.3		N	†
	54AS651	−12	32	6	81.3	J		†
	74AS651	−15	48	6	81.3		N	†
Octal Inverting Tranceivers/ MOS Drivers	54/74AS2620	−2	1	4.5	38.3	J	N	†
Octal Bus Transceivers/ MOS Drivers	54/74ALS2645A	TBD	TBD	TBD	TBD	J	N,WM	†
	54/74AS2645	−2	1	5.5	47	J	N	†

Code Converters

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
				Mil	Com	
6-Bit Binary to 6-Bit BCD Converters	54/74185A	25	280	J	N	4-185
	8899	31	350		N	4-243
6-Bit BCD to 6-Bit Binary or 4-Line to 4-Line BCD 9's/BCD 10's Converters	54/74184	25	280	J	N	4-185
	8898	31	350		N	4-243

† Please see the ALS/AS Databook for this datasheet.

Comparators

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
				Mil	Com	
4-Bit Magnitude Comparator	54/74LS85	20	52	J	N,M	2-61
	54/7485	21	275	J	N	4-83
6-Bit Magnitude Comparators	71/8131	20	250	J	N	4-224
	71/8136	20	250	J	N	4-227
	71/8160	21	205	J	N	4-230
8-Bit Identity Comparator	54/74ALS520	13.5	60	J	N,M	†
	54/74ALS521	13.5	60	J	N,M	†
8-Bit Identity Comparator with Open-Collector Outputs	54/74ALS518	18.2	55	J	N,M	†
	54/74ALS519	18	55	J	N,M	†
	54/74ALS522	19	45	J	N,M	†
	54/74ALS689	11	60	J	N,M	†
10-Bit Magnitude Comparators	71/8130	21	240	J	N	4-222

Counters, Asynchronous (Ripple Clock)/Negative-Edge-Triggered

Description	Device Type	Count Freq. (MHz)	Parallel Load	Clear	Typ* Power Diss. Total (mW)	Package Availability		Page
						Mil	Com	
4-Bit Binary	54/74LS93	32	None	High	39	J	N,M	2-68
	54/7493A	32	None	High	160	J	N	4-90
	54/74L93	6	None	High	20	J	N	5-22
	54/74LS293	32	None	High	45	J	N,M	2-216
Decade	54/74LS90	32	Set-to-9	High	40	J	N,M	2-68
	54/7490A	32	Set-to-9	High	160	J	N	4-90
	54/74LS290	32	None	High	45	J	N,M	2-212
Dual 4-Bit Decade	54/74LS390	25	None	High	75	J	N,M	2-240
Dual 4-Bit Binary	54/74LS393	25	None	High	75	J	N,M	2-244

† Please see the ALS/AS Databook for this datasheet.

Counters, Synchronous/Positive-Edge-Triggered

Description	Device Type	Count Freq. (MHz)	Parallel Load	Clear	Typ* Power Diss. Total (mW)	Package Availability		Page
						Mil	Com	
4-Bit Binary	54/74ALS161B	25	Sync	Async-L	60	J	N,M	†
	54/74AS161		Sync	Async-L	200	J	N	†
	54/74LS161A	25	Sync	Async-L	93	J	N,M	2-123
	54/74S161	40	Sync	Async-L	475	J	N	3-64
	54/74161A	25	Sync	Async-L	305	J	N	4-148
	54/74ALS163B	25	Sync	Sync-L	60	J	N,M	†
	54/74AS163		Sync	Sync-L	200	J	N	†
	54/74LS163A	25	Sync	Sync-L	93	J	N,M	2-123
	54/74S163	40	Sync	Sync-L	475	J	N	3-64
	54/74163A	25	Sync	Sync-L	93	J	N	4-148
	75/8556	25	Sync	Sync-L	375	J	N	4-232
	93/8316	25	Sync	Async-L	305	J	N	4-279
4-Bit Binary Up-Down	54/74ALS169B	25	Sync	None	75	J	N,M	†
	54/74AS169		Sync	None	230	J	N	†
	54/74LS169A	25	Async	None	100	J	N,M	2-141
	54/74ALS191	25	Async	None	60	J	N,M	†
	54/74LS191	20	Async	None	90	J	N,M	2-155
	54/74191	20	Async	None	325	J	N	4-193
	54/74ALS193	25	Async	Async-H	60	J	N,M	†
	54/74LS193	25	Async	Async-H	85	J	N,M	2-161
	54/74193	20	Async	Async-H	325	J	N	4-198
	75/85L63	6	Async	Async-H	40	J	N	5-30
Decade	54/74ALS160B	25	Sync	Async-L	60	J	N,M	†
	54/74AS160		Sync	Async-L	200	J	N	†
	54/74ALS162B	25	Sync	Sync-L	60	J	N,M	†
	54/74AS162		Sync	Sync-L	200	J	N	†
	54/74162A	25	Sync	Sync-L	305	J	N	4-148
	93/8310	25	Sync	Async-L	305	J	N	4-264
Decade Up/Down	54/74ALS168B	25	Sync	None	75	J	N,M	†
	54/74AS168		Sync	None	230	J	N	†
	54/74ALS190	20	Async	None	110	J	N,M	†
	54/74LS190	20	Async	None	100	J	N,M	2-155
	54/74ALS192	20	Async	Async-H	60	J	N,M	†
	75/85L60	6	Async	Async-H	40	J	N	5-30

† Please see the ALS/AS Databook for this datasheet.

Data Selectors/Multiplexers

Description	Device Type	Type of Output	Data Inver. Output	Typ* Prop. Delay Time (ns)		Typ* Power Diss. Total (mW)	Package Availability		Page
				Data to Out	From Enable		Mil	Com	
Quad 2 to 1 Line	54/74ALS157	Standard	N/A	4.3	6.3	39	J	N,M	†
	54/74AS157	Standard	N/A	3.5	5.5	95	J	N	†
	54/74LS157	Standard	N/A	9	14	49	J	N,M	2-119
	54/74S157	Standard	N/A	5	8	250	J	N	3-59
	54/74157	Standard	N/A	9	14	150	J	N	4-145
	54/74ALS257A	TRI-STATE	N/A	4.2	6	33	J	N,M	†
	54/74AS257	TRI-STATE	N/A	3.5	4	83	J	N	†
	54/74LS257B	TRI-STATE	N/A	12	12	50	J	N,M	2-197
	54/74S257	TRI-STATE	N/A	5	41	320	J	N	3-105
	93/8322	Standard	N/A	9	14	150	J	N	4-290
	71/8123	TRI-STATE	N/A	9.5	N/A	200	J	N	4-219
Quad 2 to 1 Line (Inverting)	54/74ALS158	Standard	4.2	N/A	6.1	11.5	J	N,M	†
	54/74AS158	Standard	2.5	N/A	4	78	J	N	†
	54/74LS158	Standard	7	N/A	12	24	J	N,M	2-119
	54/74S158	Standard	4	N/A	7	195	J	N	3-59
	54/74ALS258A	TRI-STATE	4.2	N/A	6	29.2	J	N,M	†
	54/73AS258	TRI-STATE	3	N/A	4.5	58.5	J	N	†
	54/74LS258B	TRI-STATE	12	N/A	12	35	J	N,M	2-197
	54/74S258	TRI-STATE	4	N/A	14	280	J	N	3-105
Dual 4 to 1 Line	54/74ALS153	Standard	N/A	16.5	14.5	37.5	J	N,M	†
	54/74LS153	Standard	N/A	14	22	31	J	N,M	2-109
	54/74S153	Standard	N/A	6	9.5	225	J	N	3-56
	54/74153	Standard	N/A	10.5	20	170	J	N	4-136
	54/74ALS253	TRI-STATE	N/A	8	4.5	35	J	N,M	†
	54/74LS253	TRI-STATE	N/A	15	25	38	J	N,M	2-194
	54/74S253	TRI-STATE	N/A	6	12	275	J	N	3-102
	93/8309	Standard	12	20	20	135	J	N	4-261
Dual 4 to 1 Line (Inverting)	54/74ALS352	Standard	6		4.5	32.5	J	N,M	†
	54/74LS352	Standard	15	N/A	18	31	J	N,M	2-220
	54/74ALS353	TRI-STATE	6	N/A	4.5	37.5	J	N,M	†
8 to 1 Line	54/74ALS151	Standard	9.3	7.8	11	37.5	J	N,M	†
	54/74AS151	Standard	2.8	3.5	5	130	J	N	†
	54/74S151	Standard	4.5	8	9	225	J	N	3-52
	54/74151A	Standard	8	16	22	145	J	N	4-130
	54/74ALS251	TRI-STATE	9.4	7.6	7	47	J	N,M	†
	54/74LS251	TRI-STATE	17	21	21	35	J	N,M	2-191
	54/74S251	TRI-STATE	4.5	8	14	275	J	N	3-98
	93/8312	Standard	9	16	17	135	J	N	4-275
16 to 1 Line	54/74150	Standard	11	N/A	18	200	J	N	4-130

† Please see the ALS/AS Databook for this datasheet.

Decoders/Demultiplexers

Description	Device Type	Type of Output	Typ* Select Time (ns)	Typ* Enable Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
						Mil	Com	
Dual 2 to 4 Line	54/74LS139	Totem	22	19	34	J	N,M	2-101
	54/74S139	Totem	7.5	6	300	J	N	3-46
	54/74LS155	Totem	18	15	30	J	N,M	2-115
	54/74155	Totem	21	16	250	J	N	4-142
	54/74LS156	Open-Collector	33	26	31	J	N,M	2-115
3 to 8 Line	54/74ALS138	Totem	8.5	9	25	J	N,M	†
	54/74LS138	Totem	22	21	31	J	N,M	2-101
	54/74S138	Totem	8	7	225	J	N	3-46
3 to 8 Line Decoder with Address Register	54/74ALS131	Totem	8.5	10	25	J	N,M	†
3 to 8 Line Decoder with Address Latch	54/74ALS137	Totem	11	10	25	J	N,M	†
4 to 10 Line	54/74LS42	Totem	17	N/A	35	J	N,M	2-43
BCD to	54/7442	Totem	17	N/A	140	J	N	4-60
Decimal	93/8301	Totem	20	N/A	125	J	N	4-258
4 to 16 Line	54/74LS154	Totem	23	19	45	J	N,WM	2-112
	54/74154	Totem	19.5	17.5	170	J	N	4-139
	93/8311	Totem	19.5	17.5	170	J	N	4-271
1 of 10 Decoder	93/8301	Totem	19.5	N/A	125	J	N	4-258

Decoder/Drivers, Display

Description	Device Type	Output Sink Current (mA)	Off-State Output Voltage (V)	Typ* Power Diss. Total (mW)	Blanking	Package Availability		Page
						Mil	Com	
BCD to	54/7446A	40	30	320	Ripple	J	N	4-66
7-Segment	54/7447A	40	15	320	Ripple	J	N	4-66
Decoder/Drivers								
BCD to	54/7442	16	5.5	140	Invalid	J	N	4-60
Decimal	54/7445	80	30	215	Invalid	J	N	4-63
Decoder/	54/74141	7	60	80	Invalid	J	N	4-120
Driver	54/74145	80	15	215	Invalid	J	N	4-123
Nixie Driver	54/7441A	7	70	105	None	J	N	4-57

Flip-Flops, Gated

Device Type	Clear	Preset	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
							Mil	Com	
54/74L72	Yes	Yes	20	0	0	3.8	J	N	5-13

† Please see the ALS/AS Databook for this datasheet.

Flip-Flops, Single and Dual J-K Edge Triggered

Device Type	Clear	Preset	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
							Mil	Com	
54/74LS73A	Yes	No	45	25	5	10	J	N,M	2-48
54/74LS107A	Yes	No	45	20	0	10	J	N,M	2-75
54/74AS109A	Yes	Yes	50	15	0	6	J	N,M	†
54/74AS109	Yes	Yes	125	3	1	28.8	J	N	†
54/74LS109A	Yes	Yes	33	25	0	10	J	N,M	2-78
54/74109	Yes	Yes	33	10	6	45	J	N	4-103
54/74AS112	Yes	Yes	200			95	J	N	†
54/74LS112A	Yes	Yes	45	20	0	10	J	N,M	2-81
54/74S112	Yes	Yes	125	6	0	75	J	N	3-38
54/74S113	No	Yes	125	6	0	75	J	N	3-41
90/8024	Yes	Yes	40	15	10	45	J	N	4-251

Flip-Flops, Dual D Edge Triggered with Preset and Clear

Device Type	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
					Mil	Com	
54/74ALS74A	30	15	0	6	J	N,M	†
54/74AS74	125	2	1	26.3	J	N	†
54/74LS74A	33	20	0	10	J	N,M	2-51
54/74S74	110	3	2	75	J	N	3-33
54/7474	25	20	5	43	J	N,M	4-74
54/74L74	6	50	15	4	J	N	5-19

Flip-Flop, Octal D Edge Triggered with TRI-STATE Outputs

Device Type	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
					Mil	Com	
54/74ALS374	50	10	4	10.8	J	N,WM	†
54/74AS374	200	3	3	50.3	J	N	†
54/74LS374	50	20	0	15.9	J	N,WM	2-235
54/74S374	100	5	2	60.9	J	N	3-123
54/74ALS534	50	10	0	10.4	J	N,WM	†
54/74AS534	200	3	2	50.3	J	N	†
54/74ALS564	50	15	4	8.5	J	N,WM	†
54/74ALS574A	50	15	4	8.5	J	N,WM	†
54/74AS574	200	3	3	50.4	J	N	†
54/74AS575	160	3	3	53	J	N	†
54/74ALS576A	50	15	4	8.5	J	N,WM	†
54/74AS576	160	3	3	52.5	J	N	†
54/74AS577	160	3	3	50.4	J	N	†
54/74ALS874A	50	15	4	10.8	J	N,WM	†
54/74AS874	160	2.5	1	62.5	J	N	†
54/74ALS876A	50	15	4	10.8	J	N,WM	†
54/74AS876	160	2.5	1	58	J	N	†
54/74AS878	160	3	3	62.5	J	N	†
54/74AS879	160	3	3	59	J	N	†

† Please see the ALS/AS Databook for this datasheet.

Flip-Flops, Single and Dual, Pulse Triggered

Device Type	Clear	Preset	Typ* f_{MAX} (MHz)	Data Setup Time (ns)	Data Hold Time (ns)	Typ* Power Diss. /FF (mW)	Package Availability		Page
							Mil	Com	
54/7473	No	Yes	35	0	0	50.0	J	N	4-71
54/74L73	No	Yes	11	0	0	3.8	J	N	5-16
54/7476	Yes	Yes	20	0	0	50.0	J	N	4-80
54/74107	No	Yes	20	0	0	50.0	J	N	4-100

Gates, AND with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Dual 4-Input	54/74ALS21	9	2.2	J	N,M	†
	54/74AS21	3.3	12.5	J	N	†
	54/74LS21	7.8	4.5	J	N,M	2-29
Triple 3-Input	54/74ALS11A	9	2.1	J	N,M	†
	54/74AS11	3.3	12.9	J	N	†
	54/74LS11	7.8	4.3	J	N,M	2-20
	54/74S11	4.8	31	J	N	3-19
Quad 2-Input	54/74ALS08	6.5	2.2	J	N,M	†
	54/74AS08	3.3	12.9	J	N	†
	54/74LS08	7.8	4.3	J	N,M	2-14
	54/74S08	4.8	31	J	N	3-13
	54/7408	15	19	J	N	4-30

Gates, AND with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Triple 3-Input	54/74ALS15	17	1.5	J	N,M	†
Quad 2-Input	54/74ALS09	17	2.2	J	N,M	†
	54/74LS09	19	4.3	J	N,M	2-16
	54/74S09	6.5	31	J	N	3-15
	54/7409	18.5	19.4	J	N	4-32

Gates, AND-OR-INVERT with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Dual 2-Wide 2-Input	54/74LS51	7.5	2.75	J	N,M	2-46
	54/74S51	3.5	28	J	N	3-29
4-Wide 4-2-3-2 Input	54/74S64	3.5	29	J	N	3-31

† Please see the ALS/AS Databook for this datasheet.

Gates, NAND and Inverters with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Dual 4-Input NAND Gates	54/74ALS22B	19	1.3	J	N,M	†
Triple 3-Input NAND Gates	54/74ALS12A	18	1.3	J	N,M	†
	54/74LS12	21	2	J	N,M	2-22
Quad 2-Input NAND Gates	54/74ALS01	17	1.3	J	N,M	†
	54/7401	32	10	J	N	4-16
	54/74ALS03B	17	1.3	J	N,M	†
	54/74LS03	22	2	J	N,M	2-8
	54/74S03	7	17.5	J	N	3-7
	54/7403	10	22	J	N	4-20
Hex Inverters	54/74ALS05A	18	1.5	J	N,M	†
	54/74LS05	21	2	J	N,M	2-12
	54/74S05	7	17.5	J	N,M	3-11
	54/7405	22	10	J	N	4-24

Gates, NAND and Inverters with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Dual 4-Input NAND Gates	54/74ALS20A	6.5	1.3	J	N,M	†
	54/74AS20	2	8.7	J	N	†
	54/74LS20	8	2	J	N,M	2-27
	54/74S20	4.5	19	J	N	3-21
	54/7420	10	10	J	N	4-43
	54/74L20	33	1	J	N	5-11
Triple 3-Input NAND Gates	54/74ALS10A	7	1.3	J	N,M	†
	54/74AS10	2	14	J	N	†
	54/74LS10	8	2	J	N,M	2-18
	54/74S10	4.5	19	J	N	3-17
	54/7410	10	10	J	N	4-34
	54/74L10	33	1	J	N	5-9
Quad 2-Input NAND Gates	54/74ALS00A	3.5	1.25	J	N,M	†
	54/74AS00	2	8	J	N	†
	54/74LS00	8	2	J	N,M	2-4
	54/74S00	4.5	19	J	N,M	3-3
	54/7400	10	10	J	N	4-14
	54/74L00	33	1	J	N	5-3
	9002C	10	11	J	N	4-249

† Please see the ALS/AS Databook for this datasheet.

Gates, NAND and Inverters with Totem-Pole Outputs (Continued)

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Hex Inverters	54/74ALS04A	3.5	1.5	J	N,M	†
	54/74AS04	2	7.1	J	N	†
	54/74LS04	8	2	J	N,M	2-10
	54/74S04	4.5	19	J	N,M	3-9
	54/7404	10	10	J	N,M	4-22
	54/74L04	33	1	J	N	5-7
	54/74ALS14	8	10	J	N,M	†
8-Input NAND Gates	54/74ALS30A	6.5	1.9	J	N,M	†
	54/74AS30	2	9.8	J	N	†
	54/74LS30	10	2.4	J	N,M	2-35
	54/74S30	4.5	19	J	N	3-23
	54/7420	10	10	J	N	4-43
13-Input NAND Gate	54/74ALS133	7	2	J	N,M	†
	54/74S133	6	19	J	N,M	3-44
Hex Non-Inverter	54/74AS34	4.5	12	J	N	†

Gates, Exclusive NOR, OR with Open-Collector Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Quad 2-Input Exclusive NOR Gates	54/74ALS811		9.1	J	N,M	†
	54/74AS811			J	N	†
Quad 2-Input Exclusive OR Gates	54/74ALS136			J	N,M	†
	54/74AS136			J	N	†

Gates, Exclusive NOR with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Quad 2-Input Exclusive NOR Gates	54/74ALS810	N/A	N/A	J	N,M	†
	54/74AS810	N/A	N/A	J	N	†

Gates, NOR with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Triple 3-Input NOR Gates	54/74ALS27	5.5	2.5	J	N,M	†
	54/74AS27	2	12.2	J	N	†
	54/74LS27	10	4.5	J	N,M	2-33
	54/7427	8.5	22	J	N	4-47
Quad 2-Input NOR Gates	54/74ALS02	5	1.9	J	N,M	†
	54/74AS02	2	10.1	J	N	†
	54/74LS02	10	2.75	J	N,M	2-6
	54/74S02	5	29	J	N	3-5
	54/7402	10	14	J	N	4-18
	54/74L02	33	1.5	J	N	5-5

† Please see the ALS/AS Databook for this datasheet.

Gates, OR with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
				Mil	Com	
Quad 2-Input OR Gates	54/74ALS32	5.5	2.8	J	N,M	†
	54/74AS32	3.5	14.9	J	N	†
	54/74LS32	10	5	J	N,M	2-37
	54/74S32	5	35	J	N	3-25
	54/7432	12	24	J	N	4-51
Quad 2-Input Exclusive OR Gates	54/74ALS86	7	3.75	J	N,M	†
	54/74AS86			J	N	†
	54/74LS86	10	7.5	J	N,M	2-65
	54/74S86	9	62.5	J	N	3-36
	54/7486	14	41	J	N	4-87

Latches

Description	Device Type	No. of Bits	Clear	Outputs	Typ.* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
							Mil	Com	
Addressable Latches	54/74LS259	8	Low	Q	17	110	J	N,WM	2-202
	54/74259	8	Low	Q	21	150	J	N	4-207
	93/8334	8	Low	Q	21	280	J	N	4-293
DG (Clocked) Latches	54/74LS75	4	None	Q,$\overline{Q}$	11	32	J	N,M	2-54
	54/7475	4	None	Q,$\overline{Q}$	15	160	J	N	4-77
$\overline{S}$,$\overline{R}$ Latches	54/74LS279	4	None	Q	12	19	J	N,M	2-205
Dual 4-Bit Latches	54/74ALS880A	4	None	$\overline{Q}$	9	88.3	J	N,M	†
	54/74AS880	4	None	$\overline{Q}$	6	391.5	J	N	†
Octal Latch	54/74ALS273	8	Low	Q	12	50	J	N,M	†
TRI-STATE Octal Latches	54/74ALS373	8	None	Q	10	70	J	N,WM	†
	54/74AS373	8	None	Q	6	300	J	N	†
	54/74LS373	8	None	Q	17	120	J	N,WM	2-235
	54/74S373	8	None	Q	12	525	J	N,WM	3-123
	54/74ALS573A	8	None	Q	9	68.3	J	N,WM	†
	54/74AS573	8	None	Q	4.5	293	J	N	†
TRI-STATE Inverting Octal Latches	54/74ALS533	8	None	$\overline{Q}$	10	75.8	J	N,WM	†
	54/74AS533	8	None	$\overline{Q}$	5	328	J	N	†
	54/74ALS563	8	None	$\overline{Q}$	13	68.3	J	N,WM	†
	54/74ALS580A	8	None	$\overline{Q}$	9	68.3	J	N,WM	†
	54/74AS580	8	None	$\overline{Q}$	4.5	330	J	N	†
Dual 4-Bit TRI-STATE Latches	54/74ALS873A	4	Low	Q	10	68.3	J	N,WM	†
	54/74AS873	4	Low	Q	4.5	330	J	N	†

† Please see the ALS/AS Databook for this datasheet.

Line Drivers

Description	Device Type	Low-Level Output Current (mA)	High-Level Output Current (mA)	Typ* Prop. Delay Time (ns)	Typ* Power Diss. /Gate (mW)	Package Availability		Page
						Mil	Com	
Dual 4-Input NAND	54/74S140	60	−40	4	43.8	J	N	3-50
Hex 2-Input NAND	54ALS804	12	−1	2.7	3.3	J		†
	74ALS804	24	−2.6	2.7	3.3		N,M	†
	54AS804B	40	−40	2	7.7	J		†
	74AS804B	48	−48	2	7.7		N	†
	54AS1804	40	−40	2	7.7	J		†
	74AS1804	48	−48	2	7.7		N	†
Hex 2-Input NOR	54ALS805	12	−12	3	4.1	J		†
	74ALS805	24	−15	3	4.1		N,M	†
	54AS805B	40	−40	1.6	9.6	J		†
	74AS805B	48	−48	1.6	9.6		N	†
	54AS1805	40	−40	1.6	9.6	J		†
	74AS1805	48	−48	1.6	9.6		N	†
Hex 2-Input AND	54ALS808	12	−12	4.3	4.6	J		†
	74ALS808	24	−15	4.3	4.6		N,M	†
	54AS808B	40	−40	3	10.6	J		†
	74AS808B	48	−48	3	10.6		N	†
	54AS1808	40	−40	3	10.6	J		†
	74AS1808	48	−48	3	10.6		N	†
Hex 2-Input OR	54ALS832	12	−12	4	5.6	J		†
	74ALS832	24	−15	4	5.6		N,M	†
	54AS832B	40	−40	2.5	12.9	J		†
	74AS832B	48	−48	2.5	12.9		N	†
	54AS1832	40	−40	2.5	12.9	J		†
	74AS1832	48	−48	2.5	12.9		N	†

Multipliers

Description	Device Type	Package Availability		Page
		Mil	Com	
4-Bit by 4-Bit Parallel Binary Multipliers	78/8875A	J	N	4-238
	78/8875B	J	N	4-238

† Please see the ALS/AS Databook for this datasheet.

One Shots, Retriggerable

Description	Device Type	No. of Inputs		Dir. Clear	Output Pulse Range (ns)	Typ* Total Power Diss. (mW)	Package Availability		Page
		Pos	Neg				Mil	Com	
Single	54/74LS122	2	2	Yes	45 ns–inf.	30	J	N,M	2-84
	96/8601	2	2	Yes	50 ns–inf.	90	J	N	4-297
Dual	54/74LS123	1	1	Yes	90 ns–inf.	60	J	N,M	2-88
	54/74123	1	1	Yes	45 ns–inf.	230	J	N	4-110
	96/8602	1	1	Yes	72 ns–inf.	195	J	N	4-301

One Shots with Schmitt-Trigger Inputs

Description	Device Type	No. of Inputs		Dir. Clear	Output Pulse Range (ns)	Typ* Total Power Diss. (mW)	Package Availability		Page
		Pos	Neg				Mil	Com	
Single	54/74121	1	2	Yes	40 ns–28s	90	J	N	4-106
Dual	54LS221	1	1	Yes	20 ns–49s	65	J		2-174
	74LS221	1	1		20 ns–49s	23		N,M	2-174

Parity Generators/Checkers

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
				Mil	Com	
8-Bit Odd/Even Parity Generators/Checkers	54/74180	35	170	J	N	4-174
9-Bit Odd/Even Parity Generators/Checkers	54/74S280	13	335	J	N,M	3-110
	54/74AS280	7.3	135	J	N	†
9-Bit Parity Generator/Checker with Bus Driver Parity I/O Port	54/74AS286	9.3	160	J	N	†

Priority Encoders

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ* Power Diss. Total (mW)	Package Availability		Page
				Mil	Com	
Cascadable Octal Priority Encoders	54/74148	12	190	J	N	4-126
	93/8318	12	190	J	N	4-286

Register Files

Description	Device Type	Typ* Address Time (ns)	Typ* Read Enable Time (ns)	Data Input Rate (MHz)	Typ* Power Diss. Total (mW)	Package Availability		Page
						Mil	Com	
4 Words of 4 Bits with TRI-STATE Outputs	54/74LS670	24	19	20	135	J	N,M	2-254

† Please see the ALS/AS Databook for this datasheet.

Registers, Other

Description	Device Type	Typ* Clock Freq. (MHz)	Asyn. Clear	Typ* Power Diss. Total (mW)	Package Availability		Page
					Mil	Com	
Quad Bus Buffer Registers	54/74LS173A	40	High	85	J	N,M	2-146
	54/74173	30	High	250	J	N	4-165
Quad D-Type Registers	54/74ALS175	60	Low	47.5	J	N,M	†
	54/74AS175	160	Low	395	J	N	†
	54/74LS175	40	Low	55	J	N,M	2-150
	54/74S175	90	Low	300	J	N	3-70
	54/74175	40	Low	150	J	N	4-169
Quad Multi-plexers with Storage	54/74L98	15	None	30	J	N	5-28
Hex D-Type Registers	54/74ALS174	60	Low	50	J	N,M	†
	54/74AS174	160	Low	395	J	N	†
	54/74LS174	40	Low	80	J	N,M	2-150
	54/74S174	90	Low	450	J	N	3-70
	54/74174	40	Low	225	J	N	4-169
8-Bit Universal Shift/Storage Registers	54/74S299	60	Low	700	J	N	3-118
Octal D-Type Registers	54/74ALS374	50	None	86	J	N,WM	†
	54/74AS374	200	None	402	J	N	†
	54/74LS374	50	None	128	J	N,WM	2-235
	54/74S374	100	None	487	J	N,WM	3-123
	54/74ALS534	50	None	83	J	N,WM	†
	54/74AS534	200	None	328	J	N	†
	54/74ALS574A	40	None	68	J	N,WM	†
	54/74AS574	160	None	403	J	N	†
	54/74AS575	160	None	383	J	N	†
	54/74ALS576A	50	None	68	J	N,WM	†
	54/74AS576	160	None	420	J	N	†
	54/74AS577	160	None	420	J	N	†
	54/74ALS874A	50	Low	87	J	N,WM	†
	54/74AS874	160	Low	500	J	N	†
	54/74ALS876A	50	None	87	J	N,WM	†
	54/74AS876	160	None	500	J	N	†
	54/74AS878	160	Low	500	J	N	†
	54/74AS879	160	Low	500	J	N	†
8-Bit Dual Rank Shift Register	54/74LS952	36	None	305	J	N,M	2-258
	54/74LS962	36	None	305	J	N,M	2-264
Successive Approximation Registers	2502C	21	None	325	J	N	4-4
	2503C	21	None	300	J	N	4-4
	2504C	21	None	450	J	N	4-4
Octal Bus Transceivers And 8-Bit Storage Register	54/74ALS646	40	None	255	J	N,WM	†
	54/74ALS648	40	None	260	J	N,WM	†
	54/74ALS652	40	None	255	J	N,WM	†

† Please see the ALS/AS Databook for this datasheet.

Registers, Shift

Description	Device Type	No. of Bits	Typ* Shift Freq. (MHz)	Ser. Data Input	Asyn. Clear	Modes				Typ* Power Diss. Total (mW)	Package Availability		Page
						S-R	S-L	Load	Hold		Mil	Com	
Parallel-In	54/74LS194A	4	25	D	Low	x	x	x	x	75	J	N,M	2-166
Parallel-Out	54/74S194	4	90	D	Low	x	x	x	x	450	J	N	3-87
(Bidirectional)	54/74194	4	36	D	Low	x	x	x	x	195	J	N	4-203
Parallel-In	54/7495	4	36	D	None	x	x	x	x	195	J	N	4-97
Parallel-	54/74L95	4	14	D	None	x	x	x	x	24	J	N	5-25
Out	54/74LS195A	4	39	J-$\overline{K}$	Low	x		x		70	J	N,M	2-170
	54/74S195	4	90	J-$\overline{K}$	Low	x		x		375	J	N	3-91
	93/8300	4	39	J-$\overline{K}$	Low	x		x	x	356	J	N	4-254
Parallel-In	76/86L90	8	14	D	None	x		x	x	30	J	N	5-37
Serial-Out	54/74LS165	8	30	D	None	x		x	x	125	J	N,WM	2-133
	54/74ALS165	8	60	D	None	x		x	x	80	J	N,WM	†
	54/74LS166	8	35	D	Low	x		x	x	110	J	N,WM	2-137
	54/74166	8	35	D	Low	x		x	x	360	J	N	4-161
	54/74ALS166	8	60	D	Low	x		x	x	80	J	N,WM	†
Serial-In Parallel-	54/74LS164	8	36	Gated D	Low	x				80	J	N,M	2-130
Out	54/74164	8	36	Gated D	Low	x				175	J	N	4-158

Schmitt-Triggers with Totem-Pole Outputs

Description	Device Type	Typ* Prop. Delay Time (ns)	Typ.* Hysteresis (V)	Package Availability		Page
				Mil	Com	
Dual 4-Input NAND Schmitt Triggers	54/74ALS13		0.8	J	N,M	†
Quad 2-Input	54/74LS132	15	0.8	J	N,M	2-98
NAND Schmitt	54/74132	15	0.8	J	N	4-117
Triggers	54/74ALS132		0.8	J	N,M	†
Hex Schmitt	54/74LS14	15	0.8	J	N,M	2-24
Trigger	54/7414	15	0.8	J	N	4-36
Inverters	54/74ALS14		0.8	J	N,M	†

† Please see the ALS/AS Databook for this datasheet.

Glossary of Terms

DC Operating Conditions and Characteristics

GENERAL DEFINITIONS

I: Current is the flow of electric charge from one potential to another through a conductor. The unit of measure is the Ampere, or Amp, abbreviated A. One Amp is equal to the current flowing through one ohm of resistance when one volt is applied across that resistance. Common units found in the semiconductor industry are the milliampere, abbreviated mA, equal to 0.001A and the microampere, abbreviated μA, equal to 0.000001A. Negative current is defined as current flowing out of a device terminal and positive current is defined as current flowing into a device terminal.

V: Voltage, or the electromotive force which causes current to flow through a conductor. One Ampere of current flowing through one ohm of resistance develops a potential difference of one volt across that resistance. The unit of measure is the Volt, abbreviated V, and a common unit is the millivolt, abbreviated mV, equal to 0.001V.

INPUT CURRENT PARAMETERS

I_I Maximum High Level Input Current: Current flowing into an input when that input has the maximum voltage specified for the family applied to it. This test is used to guarantee the minimum reverse breakdown voltage of the input structure.

I_{IH} High Level Input Current: The current flowing into an input when that input has a high level voltage equal to the minimum high level output voltage specified for the family. This test is used to check the emitter-to-emitter leakage and the inverse transistor action of a multi-emitter transistor input, the input leakage of a diode, PNP transistor, or C-B short type of input, and to guarantee the fan-in specified for the family.

I_{IK} Input Clamp Current: The current flowing out of an input when that input is pulled below ground. This test is used to guarantee the integrity of the input clamp diode. The input clamp diode is used to limit the voltage swings on the input by clamping the negative excursions to a level equal to one diode drop below ground. This serves to reduce ringing on an incoming signal. Pulling the input below ground for an extended length of time can cause parasitic transistor action to occur between adjacent tanks on the die which can cause erroneous data to occur on the outputs of the device. To prevent this, voltages on the inputs during operation (other than high speed ringing) should be limited to no more than 0.5V below ground at all times.

I_{IL} Low Level Input Current: The current flowing out of an input when a low level voltage equal to the maximum low level output voltage specified for the family is applied to the input. This test is used to check the input pullup resistor on an MET or a diode input and to guarantee the specified fan-in of the family.

I_T+ Current at Positive-Going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the positive going threshold voltage is applied to the input.

I_T- Current at Negative-Going Threshold Point: The current flowing out of a transition-operated (Schmitt trigger) input when a voltage equal to the negative going threshold voltage is applied to the input.

OUTPUT CURRENT PARAMETERS

I_{CEX} Output Leakage Current: The current flowing into an open collector output when input conditions have been applied that, according to the product specification, will cause the output to be in the logic high state. This test checks the reverse breakdown of the output transistor.

$I_{O(off)}$ Off-State Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This parameter is usually specified for open collector outputs intended to drive devices other than logic circuits, such as displays. Any leakage current applied to a display may cuase the display to be activated.

I_{OH} High Level Output Current: The current flowing out of an output with input conditions applied that, according to the product specification, will establish a logic high level at the output. This test guarantees the current sourcing (drive) capability of the output and the fan-out specified for the family.

I_{OL} Low Level Output Current: The current flowing into an output with input conditions applied that, according to the product specification, will establish a logic low level at the output. This test guarantees the current sinking capability of the output and the fan-out specified for the family.

I_{OS} Output Short-Circuit Current: The current out of an output when that output is shorted to ground, or another specified potential, with input conditions applied that, according to the product specification, will establish a logic high level at the output.

I_{OZ} High-Impedance State Output Current: These tests guarantee that the device will not excessively load a bus line when the device output is put into the TRI-STATE® mode.

I_{OZH} (or I_{SINK}): The current flowing into an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic low level at the output.

I_{OZL}(or I_{SOURCE}): The current flowing out of an output with input conditions applied to the output control pin such that the output is in the high impedance state and input conditions applied to the other inputs that, according to the product specification, will establish a logic high level at the output.

SUPPLY CURRENT PARAMETERS

I_{CCH} Supply Current (outputs in the high state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a logic high level at the output(s).

I_{CCL} Supply Current (outputs in the low state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a logic low level at the output(s).

DC Operating Conditions and Characteristics (Continued)

I_{CCZ} Supply Current (outputs in the high-impedance state): The current flowing into the V_{CC} terminal of a device with input conditions applied that, according to the product specification, will establish a high impedance state at the output.

INPUT VOLTAGE PARAMETERS

BV_{IN} Input Breakdown Voltage: The maximum voltage that the device is guaranteed to be able to withstand without exceeding the maximum input current specification.

V_F Input Forward Voltage: The voltage applied to the input of a device that causes the input structure to become forward biased; usually equal to the maximum output low voltage specified for the family.

V_{IH} High Level Input Voltage: The minimum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic high level.

V_{IK} Input Clamp Voltage: The input clamp voltage specification checks the quality of the input diode whose purpose is to damp out ringing. This is not intended to be an operating condition and if this voltage is allowed to persist for any length of time, parasitic transistor action will occur between adjacent geometry tanks and circuit performance will be degraded, in some cases to the point of failure.

V_{IL} Low Level Input Voltage: The maximum positive voltage level that can be applied to an input terminal of a device and be recognized as a logic low level.

V_R Input Reverse Voltage: The voltage applied to an input of a device that causes the input structure to become reverse biased; usually equal to the minimum high level output voltage specified for the family.

V_T+ Positive-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_T-.

V_T- Negative-Going Threshold Voltage: The voltage level at a transition-operated (Schmitt trigger) input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_T+.

OUTPUT VOLTAGE PARAMETERS

V_{OH} High Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a high level at the output.

V_{OL} Low Level Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will establish a low level at the output.

V_O(off) Off-State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the off state.

NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.

V_O(on) On-State Output Voltage: The voltage at an output terminal with input conditions applied that, according to the product specification, will cause the output switching element to be in the on state.

NOTE: This characteristic is usually specified only for outputs without internal pull-up elements intended for driving devices other than logic circuits.

AC Operating Conditions and Characteristics

INPUT PARAMETERS

f_{MAX} Maximum Clock Frequency: The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic levels at the output with input conditions established that should cause changes of output logic level in accordance with the specification. Unless otherwise specified, this test is performed with no restrictions on input rise and fall times or duty cycle.

NOTE: A minimum value is specified that is the highest frequency at which all devices are guaranteed to function correctly.

t_H Hold Time: The interval during which a signal must be maintained at a given data input after an active transition at another given input.

NOTE: A minimum value is specified that is the smallest time interval above which all devices are guaranteed to function correctly.

t_W Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of a pulse waveform.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_{REC} Recovery Time: The time interval needed to switch a memory-type device from a write mode to a read mode and to obtain valid data signals at the output.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the device is guaranteed.

t_{REL} Release Time: The time interval between one control input going inactive and another input going active after which the inactive input no longer has any influence on the device operation.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_S Set-Up Time: The time interval during which a stable signal must be maintained at a specified input terminal before an active transition at another specified input terminal.

NOTE: A minimum value is specified that is the smallest time interval at which correct operation of the logic element is guaranteed.

t_R Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude.

t_F Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from 90% of the signal amplitude to 10% of the signal amplitude.

OUTPUT PARAMETERS

t_{PZH} Output Enable Time to a High Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from a high impedance (off) state to the defined high state.

t_{PZL} Output Enable Time to a Low Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from a high impedance (off) state to the defined low state.

t_{PHZ} Output Disable Time from a High Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from the defined high state to the high impedance (off) state .

t_{PLZ} Output Disable Time from a Low Logic Level: The propagation delay time between the specified voltage reference points on the input and output waveforms with a TRI-STATE output changing from the defined low state to the high impedance (off) state .

t_{WOUT} Output Pulse Width: The time interval between specified voltage reference points on the leading and trailing edges of an output waveform.

NOTE: This is usually only specified for monostable elements.

t_{PLH} Propagation Time, Low to High: The time between the specified voltage reference points on the input and output waveforms with the output changing from a low logic level to a high logic level.

t_{PHL} Propagation Delay, High to Low: The time between the specified voltage reference points on the input and output waveforms with the output changing from a high logic level to a low logic level.

t_{TLH}, t_r Transition Time, or Rise Time: The time interval between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from a defined low level to a defined high level. Common defined levels are from 10% of the signal amplitude to 90% of the signal amplitude, or from 0.6V to 2.6V.

t_{THL}, t_f Transition Time, or Fall Time: The time interval between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from a defined high level to a defined low level. Common defined levels are from 90% of the signal amplitude to 10% of the signal amplitude, or from 2.6V to 0.6V.

EXPLANATION OF DEVICE FUNCTIONS

Circuit Complexity

SSI: Small Scale Integration; the lowest level of complexity in integrated circuits.

MSI: Medium Scale Integration; small subsystems integrated into a single microcircuit.

LSI: Large Scale Integration; large subsystems or small systems integrated into a single microcircuit.

FUNCTIONAL DESCRIPTIONS

Buffer: A logic gate with high output drive capability, or fan-out. Buffers are used where a single circuit must drive a large number of loads.

Comparator: A logic circuit that will compare two separate input signals and produce an output based on that comparison. A simple comparator is the Exclusive-NOR gate, which produces a high level output only when its two inputs are identical.

Counter: A logic circuit that counts the number of input pulses it receives. Counters can be used for frequency division, counting, and sequencing digital operations. Common counter configurations are Binary, where the device counts from 0 to 15 and Decade, where the device counts from 0 to 9.

AC Operating Conditions and Characteristics (Continued)

Data Selector/Multiplexer: A logic circuit that will select one of several input signals and feed that signal onto a common bus line. It can be thought of as a multipole, multiposition switch with each switch pole representing one output and each switch position representing one input.

Decoder/Demultiplexer: A logic circuit that is the complement of the Data Selector/Multiplexer; that is, this circuit takes an input signal and feeds it to any one of several output lines depending on the information placed on its steering, or control, inputs.

Driver: Same as Buffer, above.

Flip-Flop: A logic circuit that is used to store information. A flip-flop is called "bistable" since it has two stable states.

Gate: The basic building block of all logic circuits; an element whose output is a Boolean function of its inputs. The basic functions are the AND, OR, and NOT. By combining these functions, NAND, NOR, and Exclusive-OR and Exclusive-NOR gates are built.

Latch: A bistable element that latches, or holds, data which is present at its input at the time the Enable input goes to its inactive state. When the Enable input is active, the data, present at the input, is passed directly to the output, similar to the operation of a gate.

One-Shot: Monostable multivibrator; a flip-flop that only has one stable state. When triggered by an input transient, it flips to its unstable state for a time period determined by an external R-C network connected to its timing inputs, and then returns to its stable state.

Shift Register: A series of flip-flops in which the data signal is shifted out of one flip-flop and into the succeeding flip-flop during an active transition on the clock input.

Transceiver: A logic circuit that can transmit data onto a bus line and receive data off of the bus line using the same terminal as an input and output. The direction of signal flow is determined by logic levels present at a Direction Control input.

OTHER TERMS

Asynchronous: A mode of operation that does not require any specific timing relationship between different control inputs.

Open Collector: Output configuration that has no internal pullup. This configuration enables outputs that are connected together (wired-OR) to assume opposite states without incurring damage.

Schmitt Trigger: An input configuration that has a different threshold point depending on whether the input signal is rising or falling. This is especially useful in electrically noisy environments.

Synchronous: A mode of operation where specific timing requirements must be met between control inputs before an indicated action can occur.

Totem Pole: An output configuration that contains an internal pullup structure, usually a transistor pullup allowing higher output drive capability than is available with open collector outputs.

TRI-STATE: A registered trademark for a circuit configuration in which the device can be switched 'off' during which time the output presents a very high impedance to the bus it is connected to. This allows multiple outputs to be connected to a bus line while only one output drives the line, the other outputs being switched into their high impedance states.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in the function tables found in NSC data sheets:

H = high logic level (steady state)

L = low logic level (steady state)

↑ = transition from low to high logic level

↓ = transition from high to low logic level

X = irrelevant (any level, including transitions)

Z = off (high impedance) state of a TRI-STATE output

a . . . h = the level of steady state inputs at inputs A through H respectively

Q_0 = the level of Q before the indicated steady state input conditions were established

$\overline{Q}_0$ = complement of Q_0 or level of Q before the indicated steady state input conditons were established

Q_n = level of Q before the most recent active transition indicated by ↑ or ↓

⎍ = one high level pulse

⎾ = one low level pulse

toggle = each output changes to the complement of its previous level on each active transition indicated by ↑ or ↓

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ and/or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect on the output. If the output is shown as a pulse, ⎍ or ⎾, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.

Among the most complex function tables in this book are those of the shift registers. These embody most of the symbols used in any of the function tables, plus more. As an example, *Figure 1* is the function table for a 4-bit bidirectional universal shift register, similar to the DM54LS194.

The first line of the table represents "asynchronous" clearing of the register and indicates that if CLEAR is low, all four outputs will be reset low regardless of the states of the other inputs. In the succeeding lines, CLEAR is inactive (high) and consequently has no effect.

AC Operating Conditions and Characteristics (Continued)

The second line indicates that so long as the CLOCK input remains low (while CLEAR is high), no other input has any effect and the outputs maintain the levels they assumed before the steady-state combination of CLEAR high and CLOCK low was established. Since on all the other lines of the table only the rising edge of the CLOCK is shown to be active, the second line implicitly shows that no further change in the outputs will occur while the CLOCK remains high or on the high-to-low transition of the CLOCK.

The third line of the table represents "synchronous" parallel loading of the register and indicates that if S1 and S0 are both high, then regardless of the levels at the SERIAL inputs, the data present at A will transfer to QA, the data present at B will transfer to QB, and so forth, following a low-to-high transition on CLOCK.

The fourth and fifth lines represent the "synchronous" loading of high and low level data, respectively, from the SHIFT RIGHT SERIAL input and the shifting one bit to the right of previously entered data; data previously at QA is now at QB, data previously at QB and QC is now at QC and QD respectively, and the data previously at QD has been shifted out of the register. This entry of data and shifting takes place on the low-to-high level transition of CLOCK when S1 is low and S0 is high and as shown, the levels at the PARALLEL inputs, A through D, have no effect.

The sixth and seventh lines represent the "synchronous" loading of high and low level data respectively, from the SHIFT LEFT SERIAL input and the shifting one bit to the left of previously entered data; data previously at QD is now at QC, data previously at QC and QB is now at QB and QA respectively, and the data previously at QA has been shifted out of the register. This entry of serial data and shifting to the left takes place on the low-to-high level transition of CLOCK when S1 is high and S0 is low and as seen, the levels at the PARALLEL inputs, A through D, have no effect.

The last line indicates that so long as both MODE inputs are low, no other input has any effect and, as in the second line, the outputs maintain the levels they assumed before the steady state combination of CLEAR high and both MODE inputs low was established.

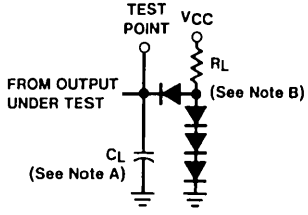
Clear	Mode		Inputs							Outputs			
			Clock	Serial		Parallel							
	S1	S0		Left	Right	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

FIGURE 1. Function Table

DM54/74, 54S/74S Test Waveforms

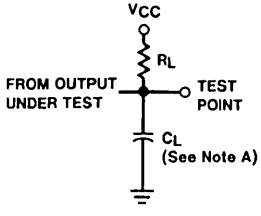
Parameter Measurement Information

Load Circuit for Bi-State Totem-Pole Outputs



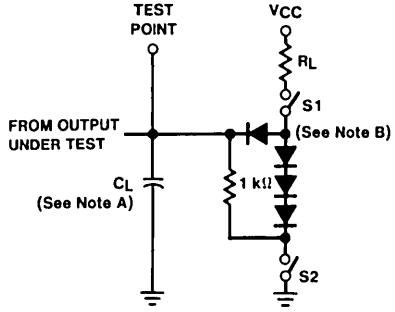
TL/X/0005-1

Load Circuit for Open-Collector Outputs



TL/X/0005-2

Load Circuit for TRI-STATE® Outputs

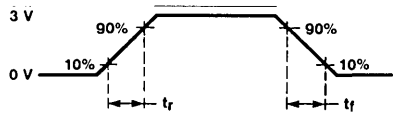


TL/X/0005-3

Note A: C_L includes probe and jig capacitance.

Note B: All diodes are 1N916 or 1N3064.

Input Waveform



TL/X/0005-4

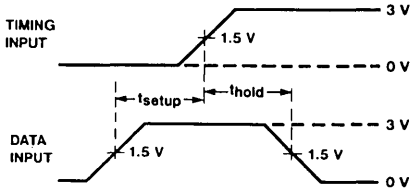
54/74 $t_r \leq 7$ ns; $t_f \leq 7$ ns

54S/74S $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns

Generator: $Z_{OUT} \approx 50\Omega$

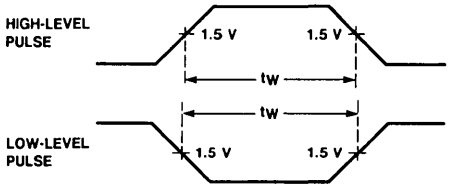
PRR $\leq$ 1 MHz

Voltage Waveforms Setup and Hold Times



TL/X/0005-5

Voltage Waveforms Pulse Widths

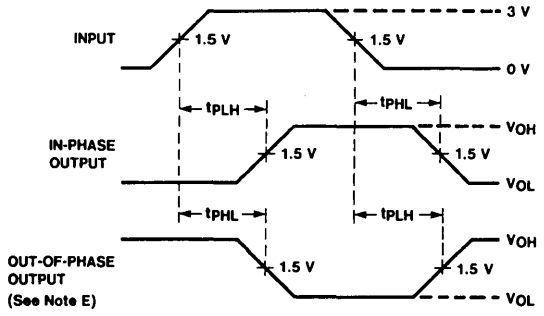


TL/X/0005-6

DM54/74, 54S/74S Test Waveforms (Continued)

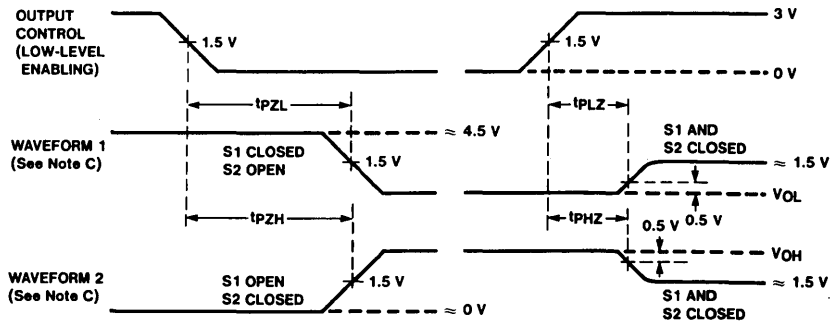
Parameter Measurement Information (Continued)

Voltage Waveforms Propagation Delay Times



TL/X/0005-7

Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs



TL/X/0005-8

Note C: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

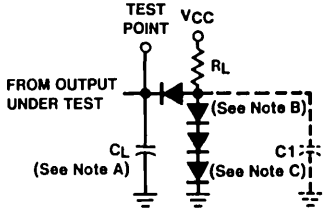
Note D: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note E: When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

DM54L/74L, 54LS/74LS Test Waveforms

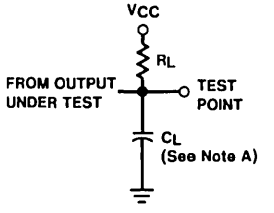
Parameter Measurement Information

Load Circuit for Bi-State Totem-Pole Outputs



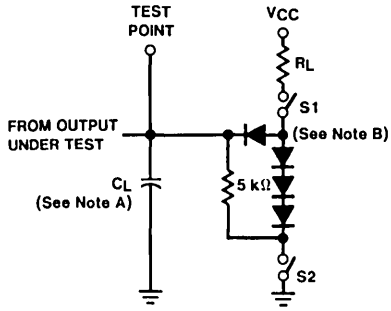
TL/X/0005-9

Load Circuit for Open-Collector Outputs



TL/X/0005-10

TRI-STATE Outputs



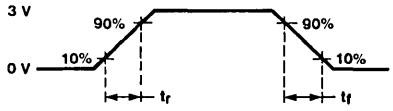
TL/X/0005-11

Note A: C_L includes probe and jig capacitance.

Note B: All diodes are 1N916 or 1N3064.

Note C: C1 (30 pF) is used for testing Series 54L/74L devices only.

Input Waveform



TL/X/0005-12

54LS/74LS: $t_r \leq 6$ ns, $t_f \leq 6$ ns

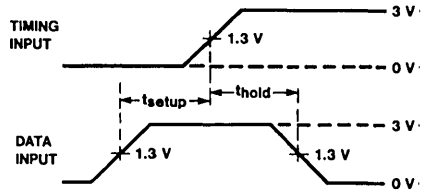
54L/74L gates and inverters: $t_r \leq 60$ ns, $t_f \leq 60$ ns

54L/74L flip-flops and MSI: $t_r \leq 25$ ns, $t_f \leq 25$ ns

Generator: $Z_{OUT} \approx 50\Omega$

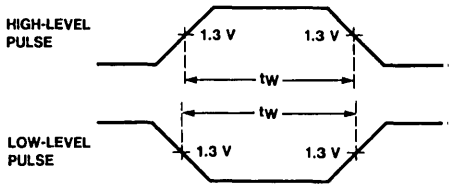
PRR $\leq$ 1 MHz

Voltage Waveforms Setup and Hold Times



TL/X/0005-13

Voltage Waveforms Pulse Widths

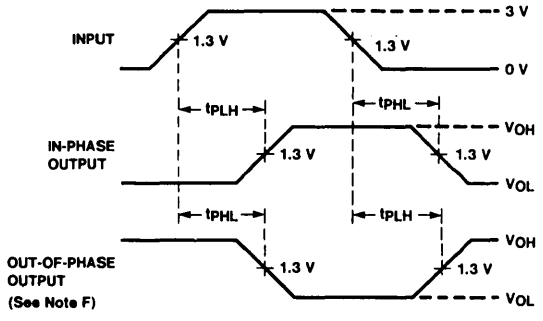


TL/X/0005-14

DM54L/74L, 54LS/74LS Test Waveforms (Continued)

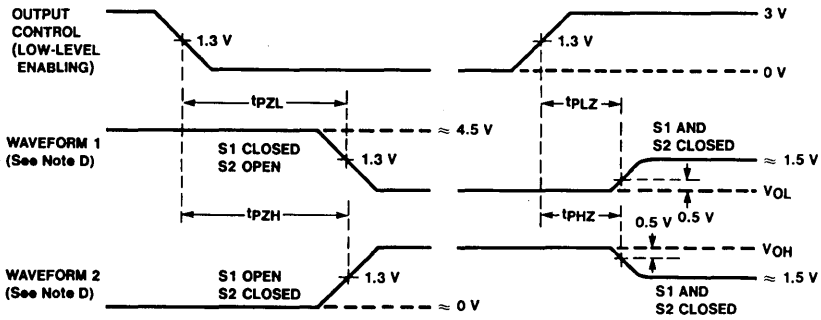
Parameter Measurement Information (Continued)

Voltage Waveforms Propagation Delay Times



TL/X/0005–15

Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs



TL/X/0005–16

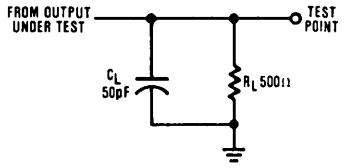
Note D: Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

Note E: In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.

Note F: When measuring propagation delay times of TRI-STATE outputs, switches S1 and S2 are closed.

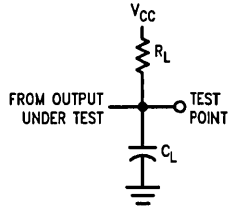
Test Waveforms DM54ALS/74ALS, 54AS/74AS

Load Circuit for Bi-State Totem-Pole Outputs



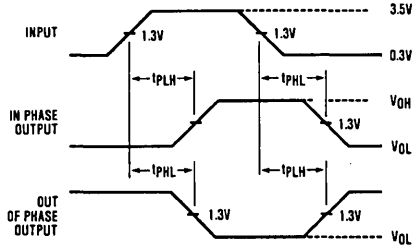
TL/X/0005-17

Load Circuit for Open-Collector Outputs



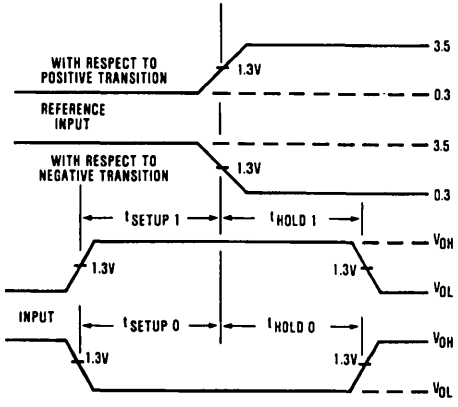
TL/X/0005-33

Voltage Waveforms Propagation Delay Times



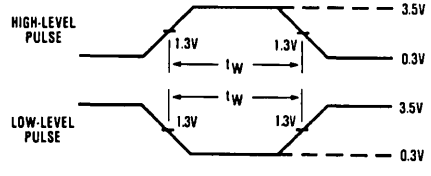
TL/X/0005-18

Voltage Waveforms Setup and Hold Times



TL/X/0005-19

Voltage Waveforms Pulse Widths

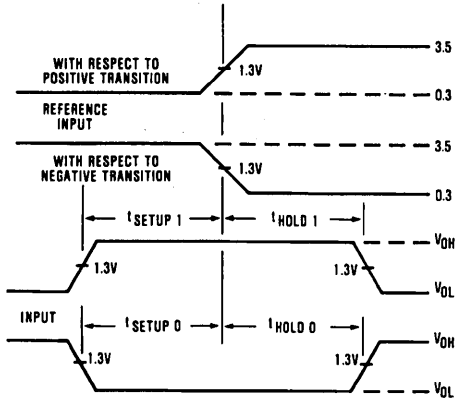


TL/X/0005-22

Note: All input pulses are supplied by generators having the following characteristics: frequency = 1 MHz, Z_{OUT} = 50Ω, $t_r = t_f$ = 2 ns.

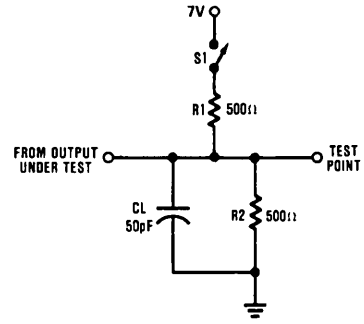
Test Waveforms DM54ALS/74ALS, 54AS/74AS (Continued)

Voltage Waveforms Setup and Hold Times



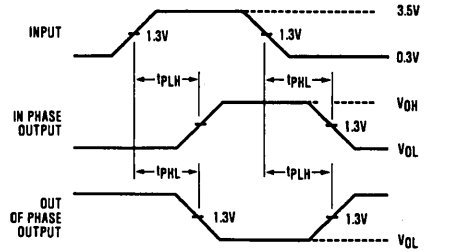
TL/X/0005–19

Load Circuit for TRI-STATE Outputs



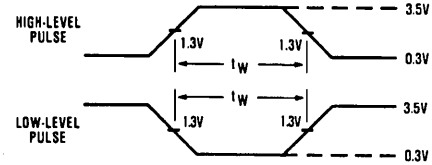
TL/X/0005–20

Voltage Waveforms Propagation Delay Times



TL/X/0005–21

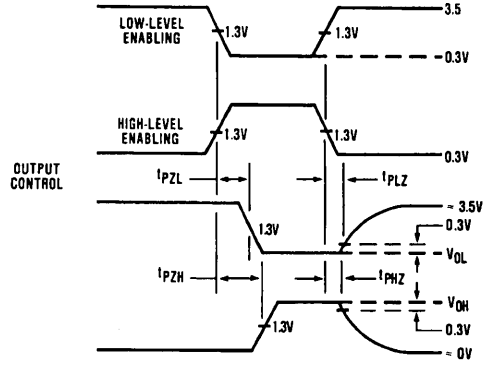
Voltage Waveforms Pulse Widths



TL/X/0005–22

Parameter	S1 Switch Position
T_{PLH}	OPEN
T_{PHL}	OPEN
T_{PHZ}	OPEN
T_{PZH}	OPEN
T_{PLZ}	CLOSED
T_{PZL}	CLOSED

Voltage Waveforms Enable and Disable Times, TRI-STATE Outputs



TL/X/0005–23

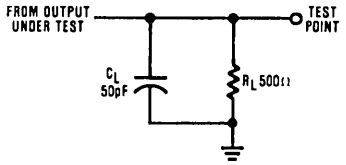
NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1 MHz, Z_{OUT} = 50Ω, t_r = t_f = 2 ns.

Group 4 Test Waveforms DM54ALS/74ALS, 54AS/74AS

54ALS74, 109, 112, 113, 114, 131, 137, 160, 161, 162, 163, 168, 169, 174, 175, 273

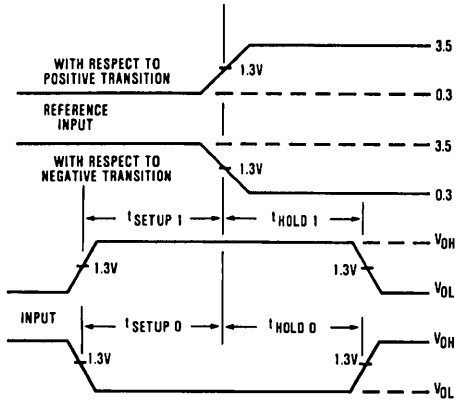
54AS74, 109, 112, 113, 114, 160, 161, 162, 163, 168, 169, 174, 175, 273

Load Circuit for Bi-State Totem-Pole Outputs



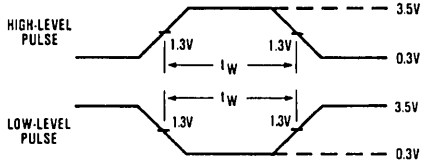
TL/X/0005-27

Voltage Waveforms Setup and Hold Times



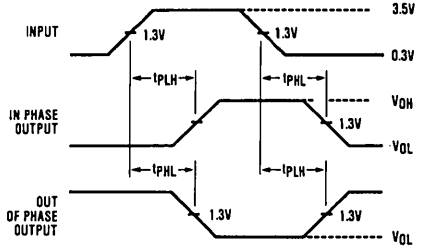
TL/X/0005-28

Voltage Waveforms Pulse Widths



TL/X/0005-29

Voltage Waveforms Propagation Delay Times



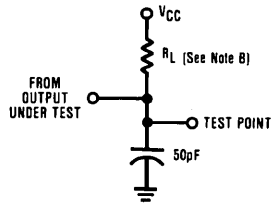
TL/X/0005-30

NOTE: All input pulses are supplied by generators having the following characteristics: frequency = 1 MHz, Z_{OUT} = 50Ω, t_r = t_f = 2 ns.

Group 5 Test Waveforms DM54ALS/74ALS, 54AS/74AS

54ALS01, 03, 05, 09, 12, 15, 22, 33, 38, 518, 519, 522, 689, 1003, 1005, 1035

Load Circuit for Open-Collector Outputs



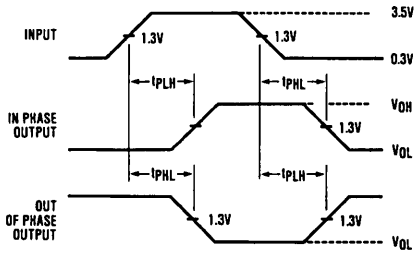
TL/X/0005–31

NOTES: A. C_L includes probe and jig capacitance

B. R_L = 2 kΩ for standard outputs

R_L = 667Ω for buffered outputs

Voltage Waveforms Propagation Delay Times



TL/X/0005–32

Note: All input pulses are supplied by generators having the following characteristics: frequency = 1 MHz, Z_{OUT} = 50Ω, $t_r = t_f$ = 2 ns.

Section 2

Low Power Schottky

Section 2 Contents

Section 2 Contents (Continued)

National Semiconductor Corporation

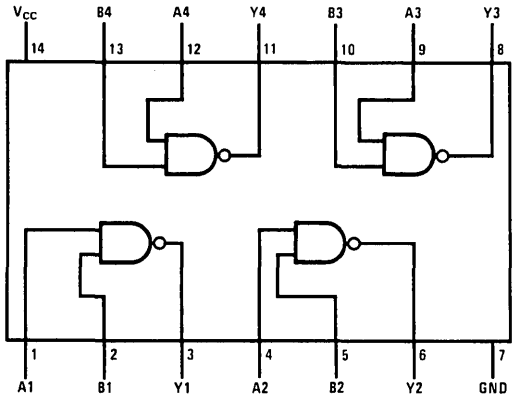
DM54LS00/DM74LS00 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6439–1

Order Number DM54LS00J, DM74LS00M or DM74LS00N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS00			DM74LS00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

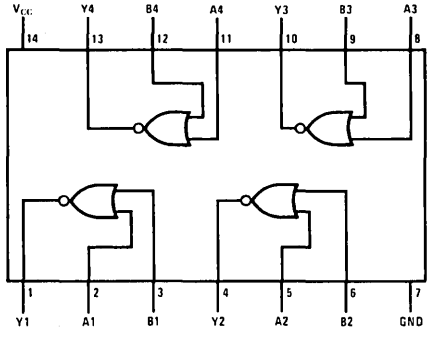
DM54LS02/DM74LS02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



TL/F/6441–1

Order Number DM54LS02J, DM74LS02M or DM74LS02N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS02			DM74LS02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.6	3.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.8	5.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	13	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54LS03/DM74LS03 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

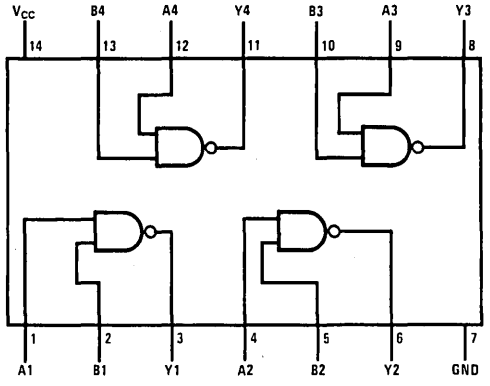
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6344–1

Order Number DM54LS03J, DM74LS03M or DM74LS03N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS03			DM74LS03			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

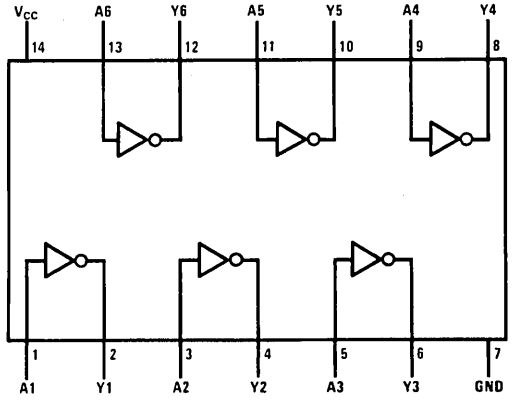
DM54LS04/DM74LS04 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

Connection Diagram

Dual-In-Line Package



TL/F/6345–1

Order Number DM54LS04J, DM74LS04M or DM74LS04N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS04			DM74LS04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.6	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54LS05/DM74LS05 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

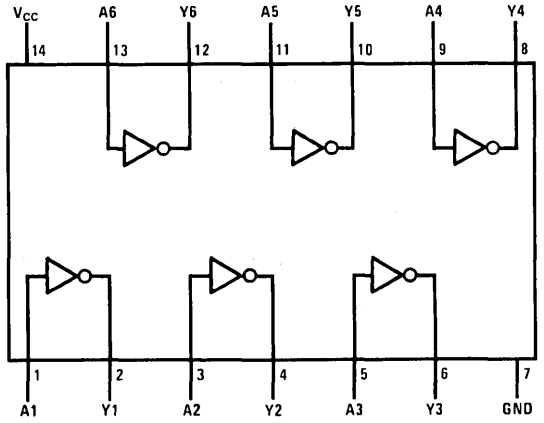
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6346–1

Order Number DM54LS05J, DM74LS05M or DM74LS05N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS05			DM74LS05			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.6	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

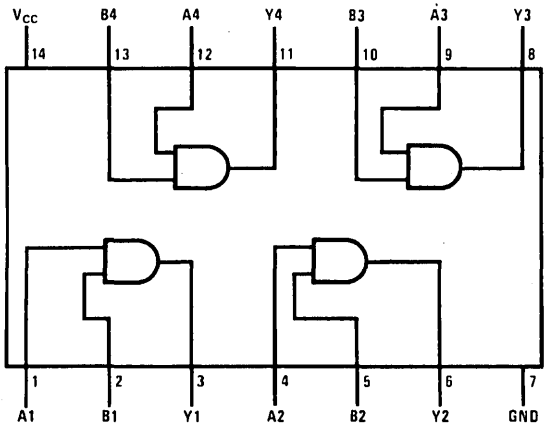
DM54LS08/DM74LS08 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

Connection Diagram

Dual-In-Line Package



TL/F/6347–1

Order Number DM54LS08J, DM74LS08M or DM74LS08N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS08			DM74LS08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54LS09/DM74LS09 Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

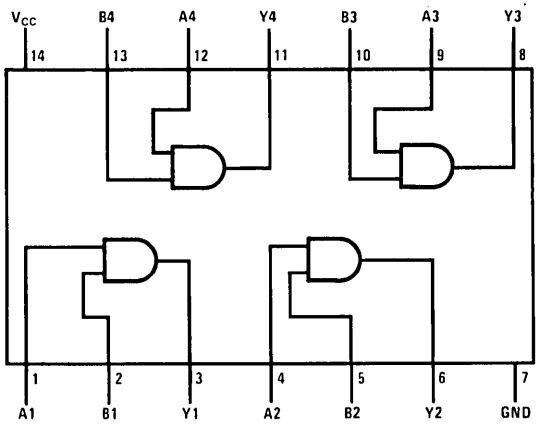
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6348–1

Order Number DM54LS09J, DM74LS09M or DM74LS09N
See NS Package Number J14A, M14A or N14A

Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS09			DM74LS09			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current With Outputs High	V_{CC} = Max			2.4	4.8	mA
I_{CCL}	Supply Current With Outputs Low	V_{CC} = Max			4.4	8.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	20	8	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	4	15	6	27	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

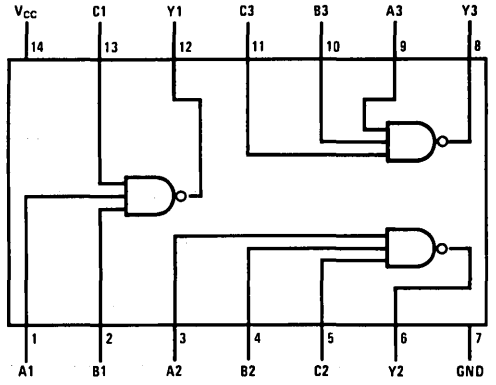
DM54LS10/DM74LS10 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6349–1

Order Number DM54LS10J, DM74LS10M or DM74LS10N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS10			DM74LS10			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.6	1.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.8	3.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

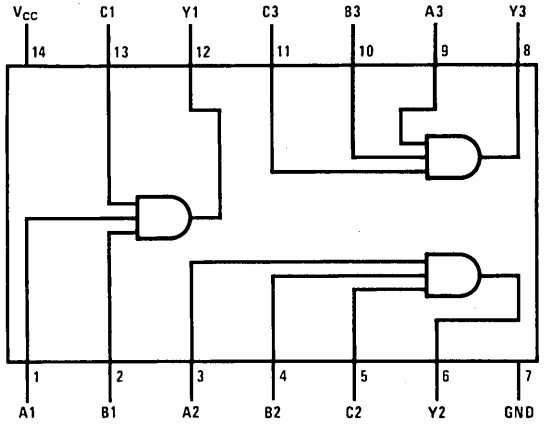
DM54LS11/DM74LS11 Triple 3-Input AND Gates

General Description

This device contains three independent gates each of which performs the logic AND function.

Connection Diagram

Dual-In-Line Package



TL/F/6350–1

Order Number DM54LS11J, DM74LS11M or DM74LS11N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = ABC$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS11			DM74LS11			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.8	3.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.3	6.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54LS12/DM74LS12 Triple 3-Input NAND Gates with Open-Collector Outputs

General Description

This device contains three independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

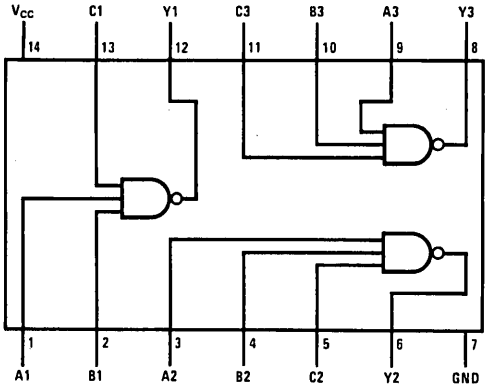
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6351–1

Order Number DM54LS12J, DM74LS12M or DM74LS12N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS12			DM74LS12			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5 V_{IL} = Max				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.7	1.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.8	3.3	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	6	20	20	45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

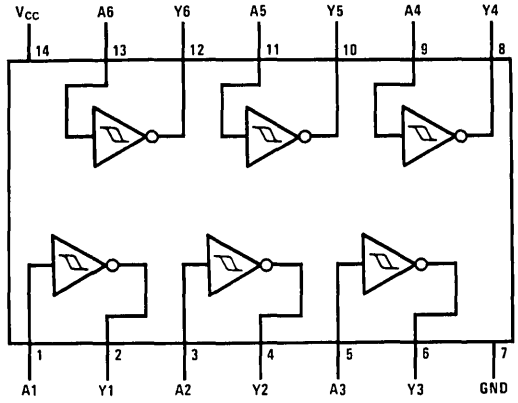
DM54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/6353–1

Order Number DM54LS14J, DM74LS14M or DM74LS14N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS14			DM74LS14			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.5	0.8	1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		V_{CC} = Min, I_{OL} = 4 mA	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8.6	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	21	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	22	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	5	22	10	33	ns

National Semiconductor Corporation

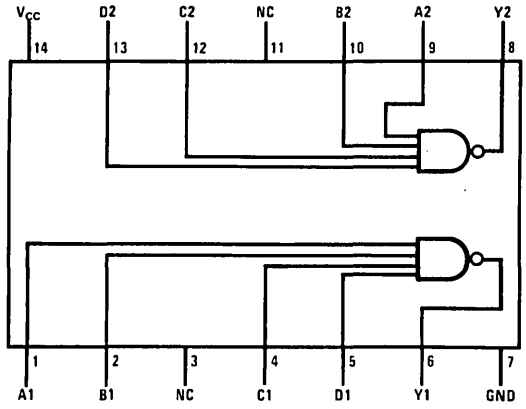
DM54LS20/DM74LS20 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6355–1

Order Number DM54LS20J, DM74LS20M or DM74LS20N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS20			DM74LS20			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.4	0.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.2	2.2	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

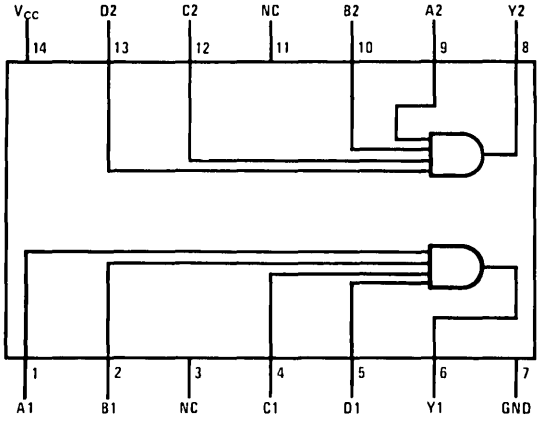
DM54LS21/DM74LS21 Dual 4-Input AND Gates

General Description

This device contains two independent gates each of which performs the logic AND function.

Connection Diagram

Dual-In-Line Package



TL/F/6356–1

Order Number DM54LS21J, DM74LS21M or DM74LS21N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = ABCD$

Inputs				Output
A	B	C	D	Y
X	X	X	L	L
X	X	L	X	L
X	L	X	X	L
L	X	X	X	L
H	H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS21			DM74LS21			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1.2	2.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.2	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	13	6	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	5	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54LS26/DM74LS26 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

These gates feature high-voltage output ratings (up to 15V) for interfacing with 12V systems. Although the outputs are rated for 15V, the device supply is still rated for 5V.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

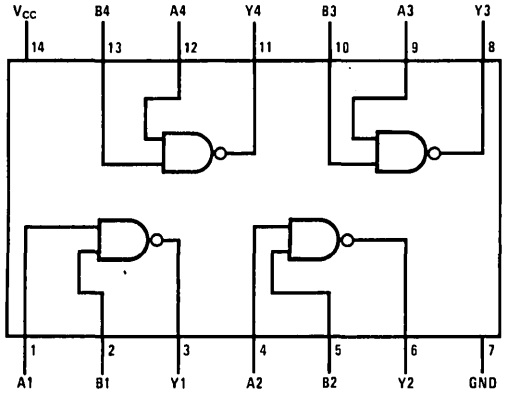
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6358–1

Order Number DM54LS26J, DM74LS26M or DM74LS26N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	15V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS26			DM74LS26			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_{IL} = Max	V_O = 15V			1000	μA
			V_O = 12V			50	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			2.4	4.4	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	R_L = 2 kΩ, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output			32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

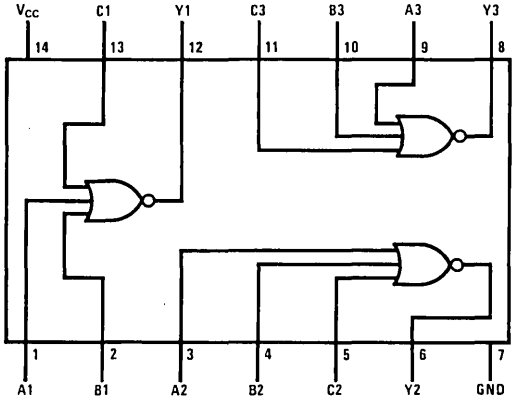
DM54LS27/DM74LS27 Triple 3-Input NOR Gates

General Description

This device contains three independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



TL/F/6359–1

Order Number DM54LS27J, DM74LS27M or DM74LS27N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS27			DM74LS27			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2	4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3.4	6.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	13	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

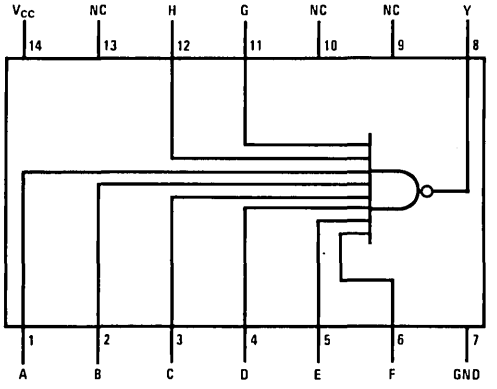
DM54LS30/DM74LS30 8-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6360–1

Order Number DM54LS30J, DM74LS30M or DM74LS30N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS30			DM74LS30			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.35	0.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			0.6	1.1	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	4	12	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	4	15	5	20	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

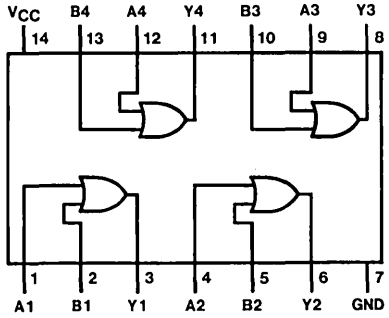
DM54LS32/DM74LS32 Quad 2-Input OR Gates

General Description

This device contains four independent gates each of which performs the logic OR function.

Connection Diagram

Dual-In-Line Package



TL/F/6361–1

Order Number DM54LS32J, DM74LS32M or DM74LS32N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS32			DM74LS32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3.1	6.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			4.9	9.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	11	4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	11	4	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

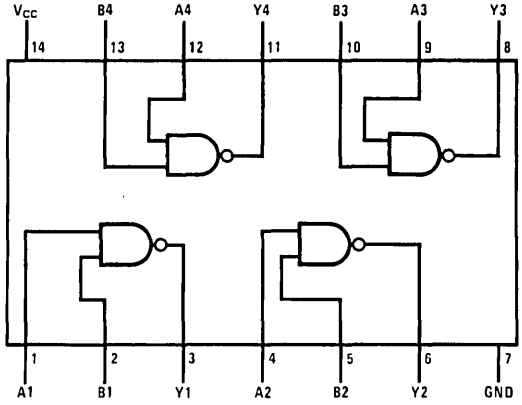
DM54LS37/DM74LS37 Quad 2-Input NAND Buffers

General Description

This device contains four independent buffer gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6362–1

Order Number DM54LS37J, DM74LS37M or DM74LS37N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS37			DM74LS37			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.9	2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			6	12	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 45 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	15	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	15	4	21	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54LS38/DM74LS38 Quad 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent gates, each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

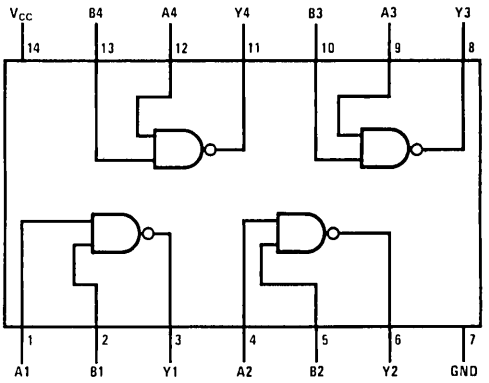
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6363–1

Order Number DM54LS38J, DM74LS38M or DM74LS38N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS38			DM74LS38			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V, V_{IL} = Max				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.9	2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			6	12	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 45 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		22		29	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

DM54LS42/DM74LS42 BCD/Decimal Decoders

General Description

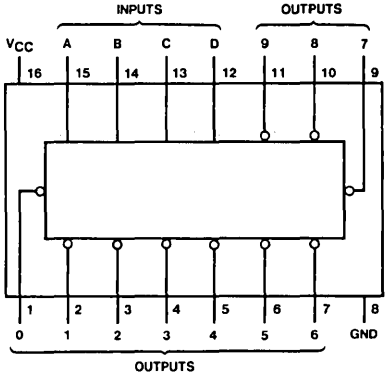
These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10–15) input conditions.

Features

- Diode clamped inputs
- Also for applications as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions

Connection Diagram

Dual-In-Line Package



TL/F/6365–1

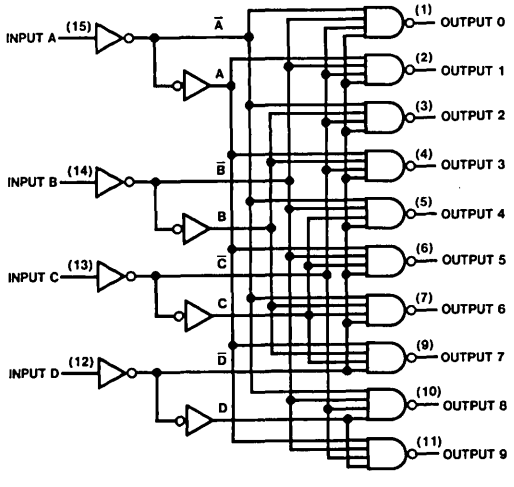
Order Number DM54LS42AJ, DM74LS42M or DM74LS42AN
See NS Package Number J16A, M16A or N16A

Function Table

No.	BCD Inputs				Decimal Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level
L = Low Level

Logic Diagram



TL/F/6365–2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS42			DM74LS42			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			7	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C, or D (2 Levels of Logic) to Output		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C, or D (3 Levels of Logic) to Output		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C, or D (2 Levels of Logic) to Output		25		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C, or D (3 Levels of Logic) to Output		30		35	ns

National Semiconductor Corporation

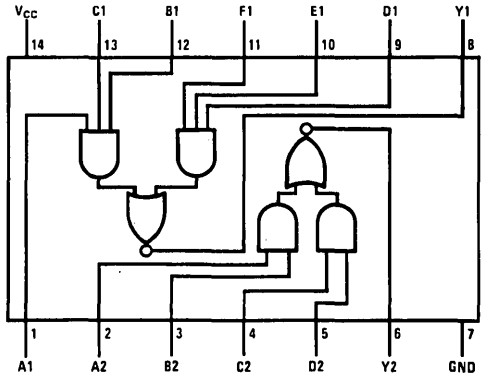
DM54LS51/DM74LS51 Dual 2-Wide 2-Input, 2-Wide 3-Input AND-OR-INVERT Gates

General Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function. Each package contains one 2-wide 2-input and one 2-wide 3-input AND-OR-INVERT gates.

Connection Diagram

Dual-In-Line Package



TL/F/6369–1

Order Number DM54LS51J, DM74LS51M or DM74LS51N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y1 = \overline{(A1)\,(B1)\,(C1) + (D1)\,(E1)\,(F1)}$$

Inputs						Output
A1	B1	C1	D1	E1	F1	Y1
H	H	H	X	X	X	L
X	X	X	H	H	H	L
Other Combinations						H

$$Y2 = \overline{((A2)\,(B2) + (C2)\,(D2))}$$

Inputs				Output
A2	B2	C2	D2	Y2
H	H	X	X	L
X	X	H	H	L
Other combinations				H

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS51			DM74LS51			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.4	2.8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	13	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	12	3	15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

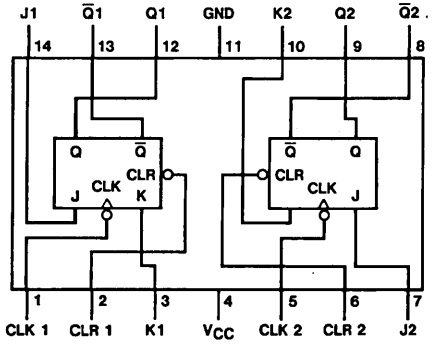
DM54LS73A/DM74LS73A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs is allowed to change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6372–1

Order Number DM54LS73AJ, DM74LS73AM or DM74LS73AN
See NS Package Number J14A, M14A or N14A

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative going edge of pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS73A			DM74LS73A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20 ↓			20 ↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25 ↓			25 ↓			ns
t_H	Hold Time (Notes 1 and 2)		0 ↓			0 ↓			ns
t_H	Hold Time (Notes 1 and 3)		5 ↓			5 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Clock			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state, an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

National Semiconductor Corporation

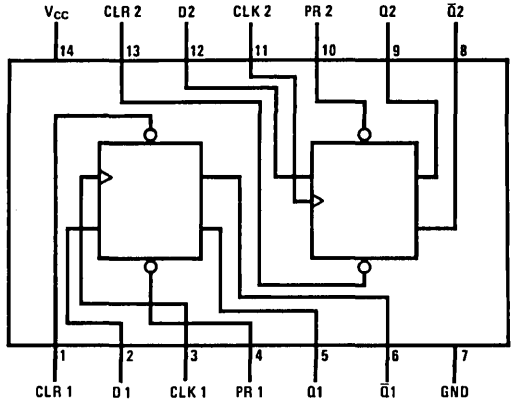
DM54LS74A/DM74LS74A Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6373–1

Order Number DM54LS74AJ, DM74LS74AM or DM74LS74AN
See NS Package Number J14A, M14A or N14A

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going Transition

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS74A			DM74LS74A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 2)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Setup Time (Notes 1 and 2)		20 ↑			20 ↑			ns
t_{SU}	Setup Time (Notes 1 and 3)		25 ↑			25 ↑			ns
t_H	Hold Time (Note 1 and 4)		0 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C, and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C, and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V	Data			0.1	mA
			Clock			0.1	
			Preset			0.2	
			Clear			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Data			20	μA
			Clock			20	
			Clear			40	
			Preset			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Data			−0.4	mA
			Clock			−0.4	
			Preset			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with CLOCK grounded after setting the Q and $\overline{Q}$ outputs high in turn.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30		35	ns

National Semiconductor Corporation

DM54LS75/DM74LS75 Quad Latches

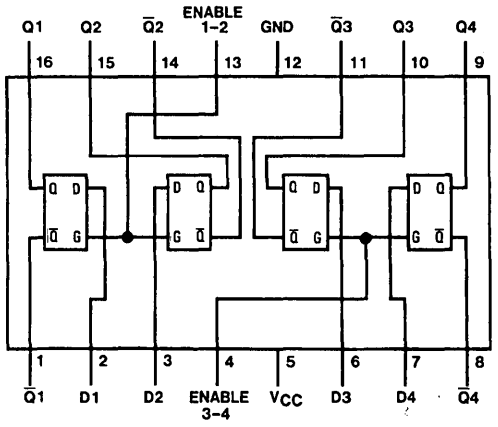
General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the enable is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occured) is retained at the Q output until the enable is permitted to go high.

These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and are available in 16-pin packages.

Connection Diagram

Dual-In-Line Package



TL/F/6374–1

Order Number DM54LS75J, DM74LS75M or DM74LS75N
See NS Package Number J16A, M16A or N16A

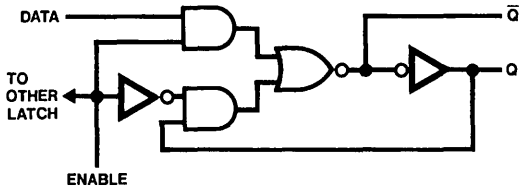
Function Table (Each Latch)

Inputs		Outputs	
D	Enable	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care

Q_0 = The Level of Q Before the High-to-Low Transition of ENABLE

Logic Diagram (Each Latch)



TL/F/6374–2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS75			DM74LS75			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
t_W	Enable Pulse Width (Note 4)	20			20			ns
t_{SU}	Setup Time (Note 4)	20			20			ns
t_H	Hold Time (Note 4)	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.5		V
			DM74	2.7	3.5		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	D			0.1	mA
			Enable			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D			20	μA
			Enable			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	D			−0.4	mA
			Enable			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Q		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Q		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		20		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		15		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Q		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Q		25		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to $\overline{Q}$		30		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to $\overline{Q}$		15		20	ns

National Semiconductor Corporation

DM54LS83A/DM74LS83A 4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

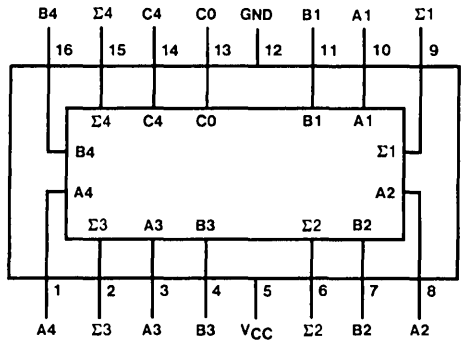
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  - Two 8-bit words 25 ns
  - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW

Connection Diagram

Dual-In-Line Package



TL/F/6378–1

Order Number DM54LS83AJ, DM74LS83AWM or DM74LS83AN
See NS Package Number J16A, M16B or N16A

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS83A			DM74LS83A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	A or B			0.2	mA
			C0			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A or B			40	μA
			C0			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A or B			−0.8	mA
			C0			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			19	34	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			22	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ1 or Σ2		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ1 or Σ2		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ3		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ3		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ4		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ4		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to Σ_i		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to Σ_i		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to C4		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to C4		17		26	ns

Truth Table

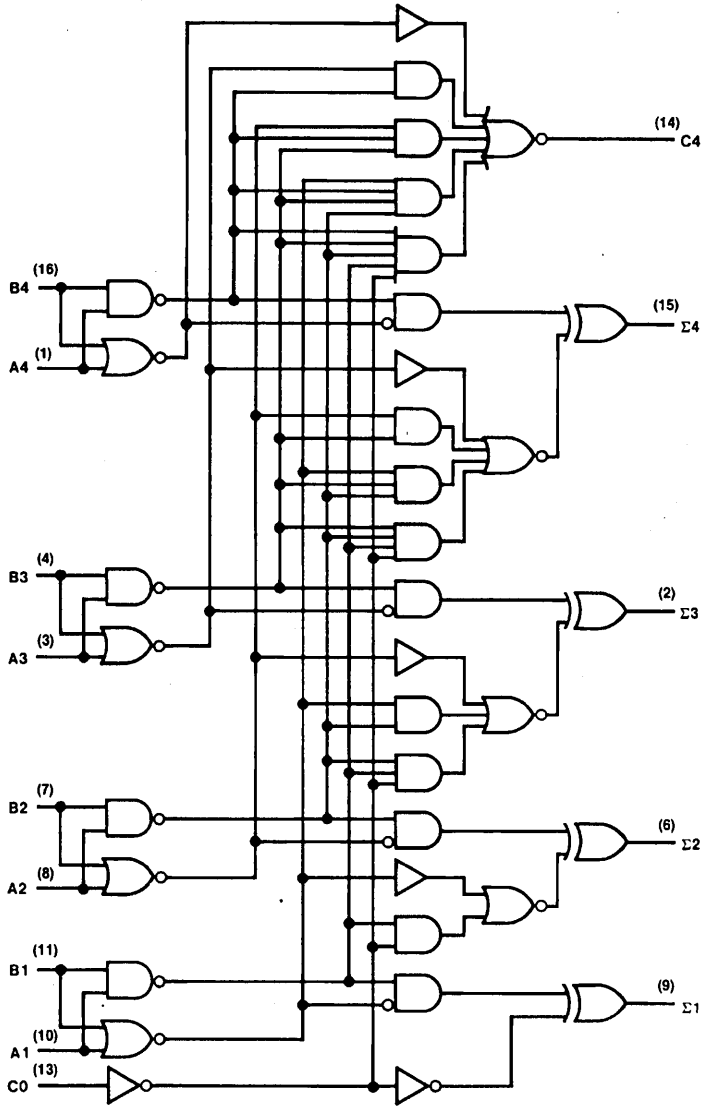
Inputs				Outputs					
				When C0 = L			When C0 = H		
				When C2 = L			When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

TL/F/6378–3

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Logic Diagram



TL/F/6378–2

National Semiconductor Corporation

DM54LS85/DM74LS85 4-Bit Magnitude Comparators

General Description

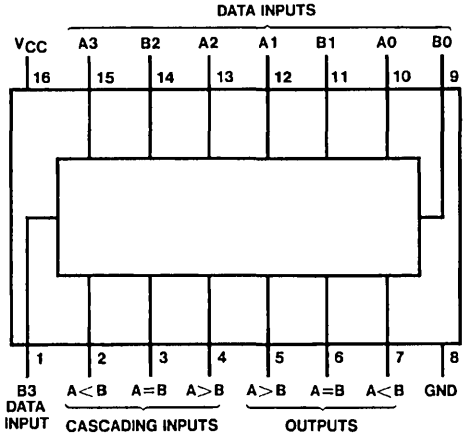
These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two, 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading path is implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

- Typical power dissipation 52 mW
- Typical delay (4-bit words) 24 ns

Connection Diagram

Dual-In-Line Package



TL/F/6379–1

Order Number DM54LS85J, DM74LS85M or DM74LS85N
See NS Package Number J14A, M14A or N14A

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS85			DM74LS85			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	A < B			0.1	mA
			A > B			0.1	
			Others			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A < B			20	μA
			A > B			20	
			Others			60	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A < B			−0.4	mA
			A > B			−0.4	
			Others			−1.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			10	20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

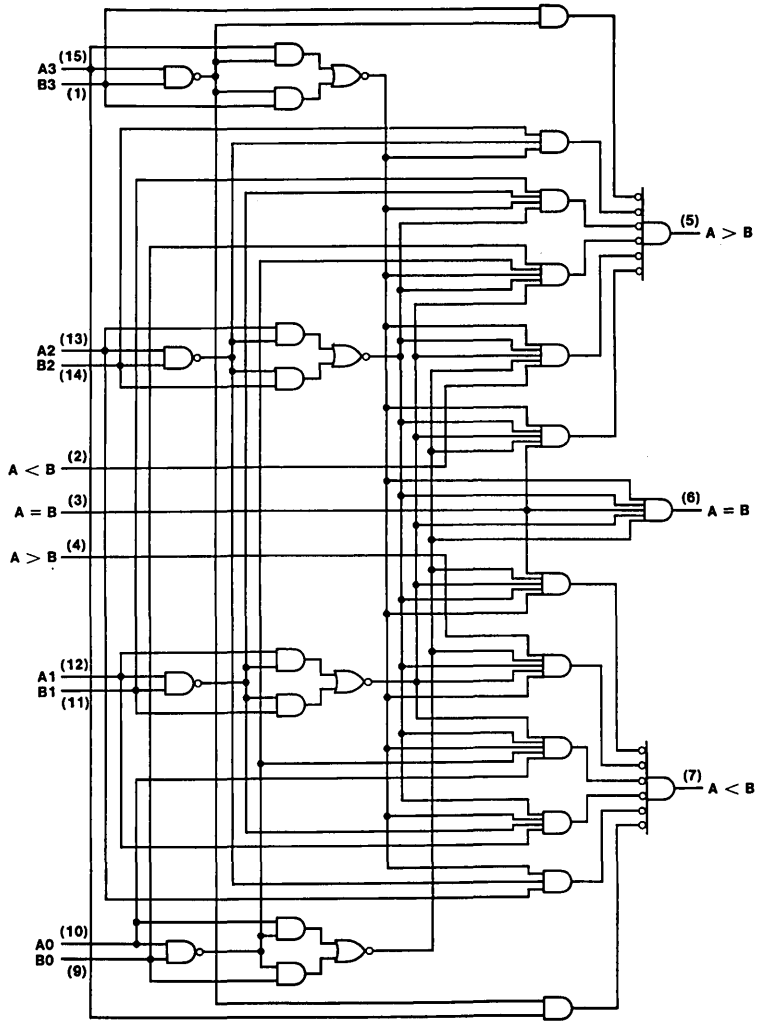
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, A = B grounded and all other inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From Input	To Output	Number of Gate Levels	R_L = 2 kΩ				Units
					C_L = 15 pF		C_L = 50 pF		
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B, A > B	3		36		42	ns
			A = B	4		40		40	
t_{PHL}	Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B, A > B	3		30		40	ns
			A = B	4		30		40	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A = B	A = B	2		20		25	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		17		26	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		22		26	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		17		26	ns

Logic Diagram



TL/F/6379-2

National Semiconductor Corporation

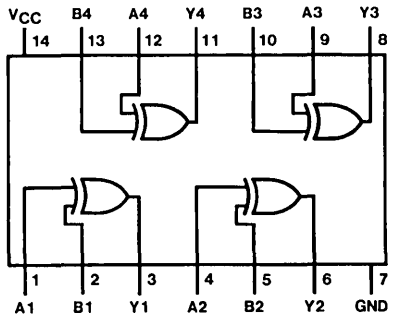
DM54LS86/DM74LS86 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

Connection Diagram

Dual-In-Line Package



TL/F/6380–1

Order Number DM54LS86J, DM74LS86M or DM74LS86N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS86			DM74LS86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			6.1	10	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with all outputs open, one input at each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low		18		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			17		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High		10		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			12		15	ns

National Semiconductor Corporation

DM54LS90/DM74LS90, DM54LS93/DM74LS93 Decade and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the LS90 and divide-by-eight for the LS93.

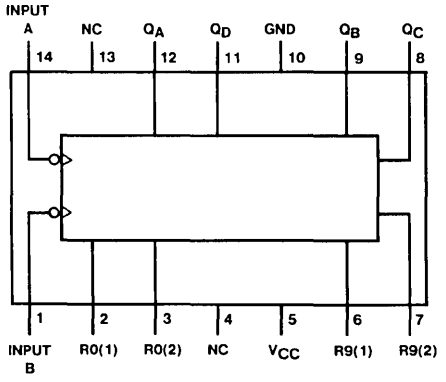
All of these counters have a gated zero reset and the LS90 also has gated set-to-nine inputs for use in BCD nine's complement applications.

To use their maximum count length (decade or four bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the LS90 counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

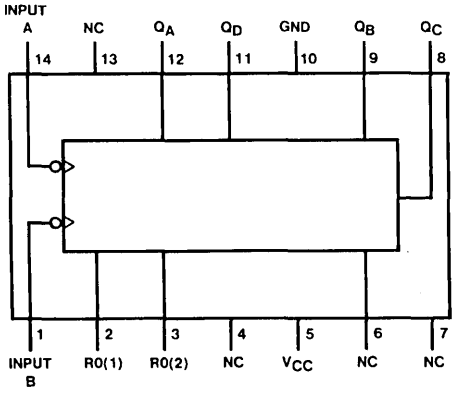
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagrams (Dual-In-Line Packages)



TL/F/6381–1

Order Number DM54LS90J, DM74LS90M or DM74LS90N
See NS Package Number J14A, M14A or N14A



TL/F/6381–2

Order Number DM54LS93J, DM74LS93M or DM74LS93N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage (Reset)	7V
Input Voltage (A or B)	5.5V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS90			DM74LS90			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	0		32	MHz
		B to Q_B	0		16	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	0		20	MHz
		B to Q_B	0		10	0		10	
t_W	Pulse Width (Note 1)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_W	Pulse Width (Note 2)	A	25			25			ns
		B	50			50			
		Reset	25			25			
t_{REL}	Reset Release Time (Note 1)		25			25			ns
t_{REL}	Reset Release Time (Note 2)		35			35			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

'LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
			B			0.4	

'LS90 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'LS90 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48		52	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50		60	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS93			DM74LS93			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	0		32	MHz
		B to Q_B	0		16	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	0		20	
		B to Q_B	0		10	0		10	
t_W	Pulse Width (Note 1)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_W	Pulse Width (Note 2)	A	25			25			ns
		B	50			50			
		Reset	25			25			
t_{REL}	Reset Release Time (Note 1)		25			25			ns
t_{REL}	Reset Release Time (Note 2)		35			35			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.
Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

'LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			80	

'LS93 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	15	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

'LS93 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70		85	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70		90	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51		70	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		52	ns

Function Tables

LS90
BCD Count Sequence
(See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

LS90
Bi-Quinary (5-2)
(See Note B)

Count	Output			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

LS93
Count Sequence
(See Note C)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

LS90
Reset/Count Truth Table

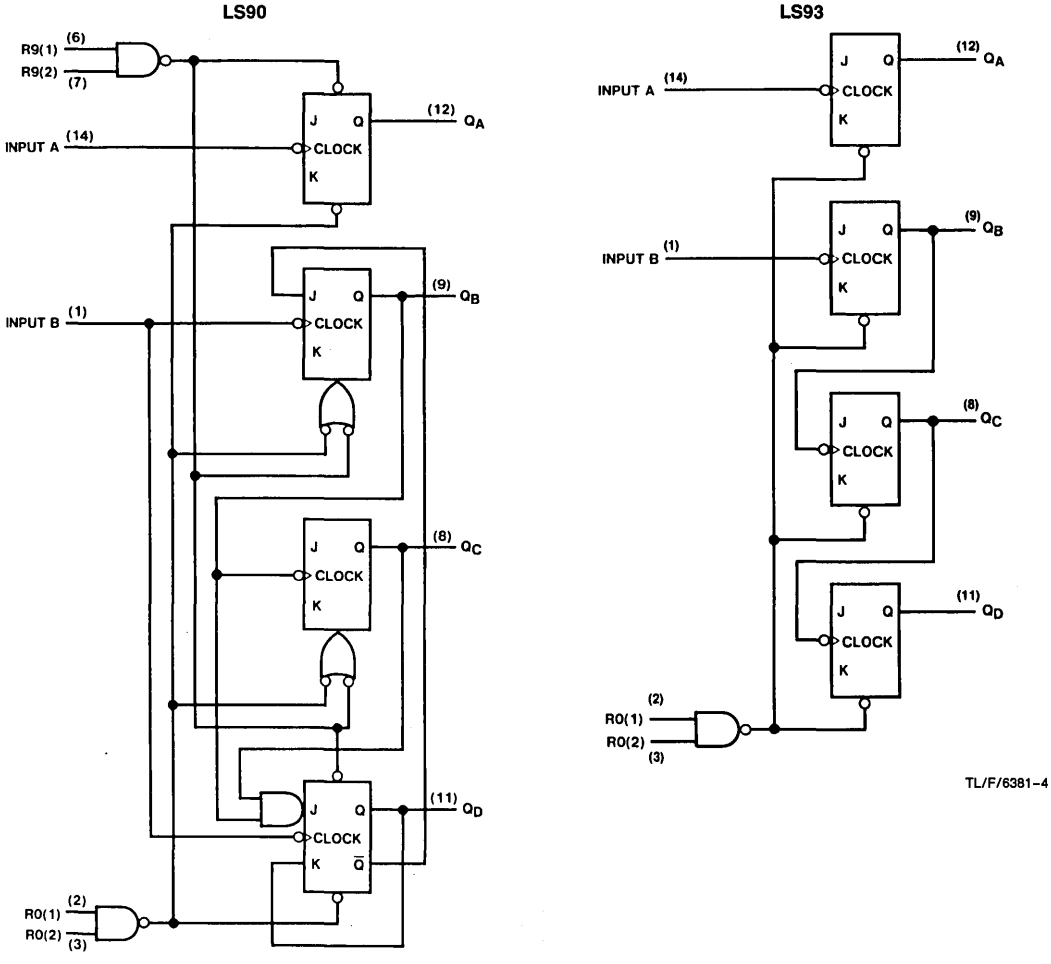
Reset Inputs				Output			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

LS93
Reset/Count Truth Table

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note A: Output Q_A is connected to input B for BCD count.
Note B: Output Q_D is connected to input A for bi-quinary count.
Note C: Output Q_A is connected to input B.
Note D: H = High Level, L = Low Level, X = Don't Care.

Logic Diagrams



The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor Corporation

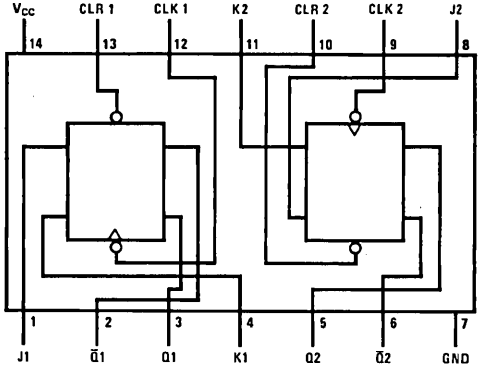
DM54LS107A/DM74LS107A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Clear, and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. The data on the J and K inputs may change while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the clear input will reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6367–1

Order Number DM54LS107AJ, DM74LS107AM or DM74LS107AN
See NS Package Number J14A, M14A or N14A

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS107A			DM74LS107A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 & 2)		20 ↓			20 ↓			ns
t_{SU}	Setup Time (Notes 1 & 3)		25 ↓			25 ↓			ns
t_H	Hold Time (Notes 1 & 2)		0 ↓			0 ↓			ns
t_H	Hold Time (Notes 1 & 3)		5 ↓			5 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Clock			0.4	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all inputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

National Semiconductor Corporation

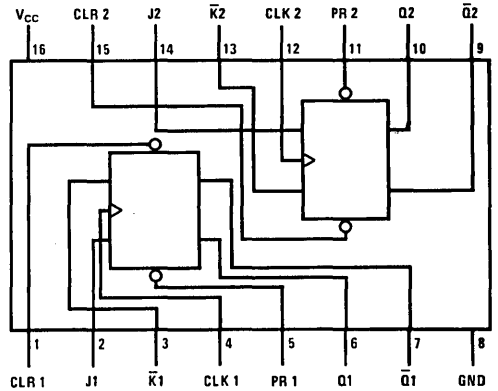
DM54LS109A/DM74LS109A Dual Positive-Edge-Triggered J-$\overline{K}$ Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered J-$\overline{K}$ flip-flops with complementary outputs. The J and $\overline{K}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and $\overline{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6368–1

Order Number DM54LS109AJ, DM74LS109AM or DM74LS109AN
See NS Package Number J16A, M16A or N16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↑ = Rising Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) state.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS109A			DM74LS109A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 2)	Clock High	18			18			ns
		Preset Low	15			15			
		Clear Low	15			15			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Setup Time (Notes 1 & 2)	Data High	30 ↑			30 ↑			ns
		Data Low	20 ↑			20 ↑			
t_{SU}	Setup Time (Notes 1 & 3)	Data High	35 ↑			35 ↑			ns
		Data Low	25 ↑			25 ↑			
t_H	Hold Time (Note 4)		0 ↑			0 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, $\overline{K}$			0.1	mA
			Clock			0.1	
			Preset			0.2	
			Clear			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J,$\overline{K}$			20	μA
			Clock			20	
			Preset			40	
			Clear			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, $\overline{K}$			−0.4	mA
			Clock			−0.4	
			Preset			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	8	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		30		35	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: I_{CC} is measured with all outputs open, with CLOCK grounded after setting the Q and $\overline{Q}$ outputs high in turn.

National Semiconductor Corporation

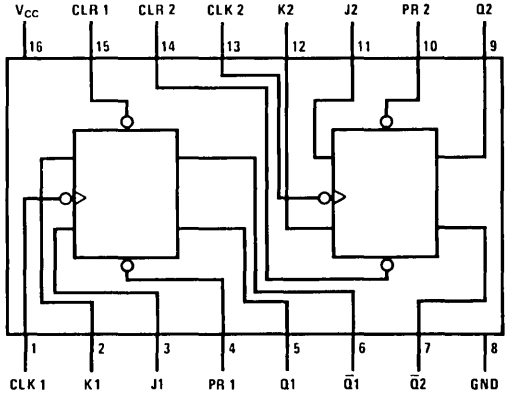
DM54LS112A/DM74LS112A Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the falling edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as the setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6382–1

Order Number DM54LS112AJ, DM74LS112AM or DM74LS112AN
See NS Package Number J16A, M16A or N16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

↓ = Negative Going Edge of Pulse

* = This configuration is nonstable; that is, it will not persist when preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS112A			DM74LS112A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 2)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 3)		0		25	0		25	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Preset Low	25			25			
		Clear Low	25			25			
t_W	Pulse Width (Note 3)	Clock High	25			25			ns
		Preset Low	30			30			
		Clear Low	30			30			
t_{SU}	Setup Time (Notes 1 and 2)		20 ↓			20 ↓			ns
t_{SU}	Setup Time (Notes 1 and 3)		25 ↓			25 ↓			ns
t_H	Hold Time (Notes 1 and 2)		0 ↓			0 ↓			ns
t_H	Hold Time (Notes 1 and 3)		5 ↓			5 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	J, K			0.1	mA
			Clear			0.3	
			Preset			0.3	
			Clock			0.4	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			20	μA
			Clear			60	
			Preset			60	
			Clock			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−0.4	mA
			Clear			−0.8	
			Preset			−0.8	
			Clock			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		20		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		20		28	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V_O = 2.25V and 2.125V for DM54 and DM74 series, respectively, with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

National Semiconductor Corporation

DM54LS122/DM74LS122 Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM54/74LS122 is a retriggerable monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal 10 kΩ timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. The 'LS122 has two active-low transition triggering inputs (A), two active-high transition triggering inputs (B), and a CLEAR input that terminates the output pulse width at a predetermined time independent of the timing components. The clear (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (⌝⌜). To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

Features

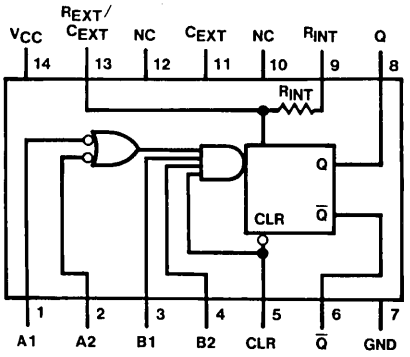
- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Over-riding clear terminates output pulse
- Internal 10 kΩ timing resistor
- TTL, DTL compatible
- Compensated for V_{CC} and temperature variations
- Input clamp diodes

Functional Description

The basic output pulse width is determined by selection of the internal resistor R_{INT} or an external resistor (R_X) and capacitor (C_X). Once triggered, the output pulse width may be extended by retriggering the gated active-low (A) transition inputs or the active-high transition (B) inputs or the CLEAR input. The output pulse width can be reduced or terminated by overriding it with the active-low CLEAR input.

Connection Diagram

Dual-In-Line Package



TL/F/6385–1

Order Number DM54LS122J, DM74LS122M or DM74LS122N
See NS Package Number J14A, M14A or N14A

Function Table

Inputs					Outputs	
CLEAR	A1	A2	B1	B2	Q	$\overline{Q}$
L	X	X	X	X	L	H
X	H	H	X	X	L	H
X	X	X	L	X	L	H
X	X	X	X	L	L	H
H	L	X	↑	H	⌝⌜	⌝⌜
H	L	X	H	↑	⌝⌜	⌝⌜
H	X	L	↑	H	⌝⌜	⌝⌜
H	X	L	H	↑	⌝⌜	⌝⌜
H	H	↓	H	H	⌝⌜	⌝⌜
H	↓	↓	H	H	⌝⌜	⌝⌜
H	↓	H	H	H	⌝⌜	⌝⌜
↑	L	X	H	H	⌝⌜	⌝⌜
↑	X	L	H	H	⌝⌜	⌝⌜

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⌝⌜ = A Positive Pulse
⌝⌜ = A Negative Pulse

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameters		DM54LS122			DM74LS122			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width (Note 6)	A or B High	40			40			ns
		A or B Low	40			40			
		Clear Low	40			40			
R_{EXT}	External Timing Resistor		5		180	5		260	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			No Restriction			μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal				50			50	pF
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Notes 3, 4 and 5)			6	11	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF, C_{EXT} = 0 pF, R_{EXT} = 5 kΩ		C_L = 15 pF, C_{EXT} = 1000 pF, R_{EXT} = 10 kΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q		33			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q		44			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		56			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		27			ns
$t_{WQ(Min)}$	Minimum Width of Pulse at Output Q	A or B to Q		200			ns
$t_{W(out)}$	Output Pulse Width	A or B to Q			4	5	μs

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 4: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to the clock.

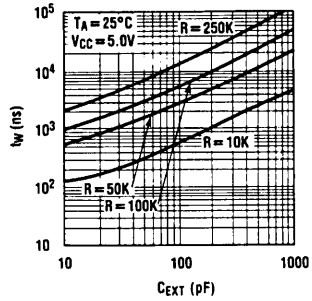
Note 6: T_A = 25°C and V_{CC} = 5V.

Operating Rules

1. To use the internal 10 kΩ timing resistor, connect the R_{INT} pin to V_{CC}.
2. An external resistor (R_X) or the internal resistor (10 kΩ) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
3. The pulse width is essentially determined by external timing components R_X and C_X. For C_X < 1000 pF see *Figure 1;* design curves on T_W as function of timing components value. For C_X >> 1000 pF the output is defined as:

$$T_W = KR_XC_X$$

where [R_X is in kΩ]
[C_X is in pF]
[T_W is in ns]
K ≈ 0.37

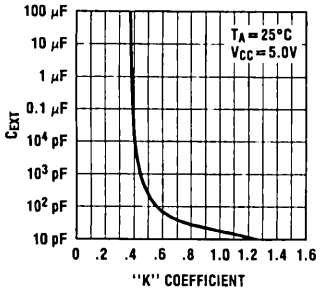


TL/F/6385–2

FIGURE 1

Operating Rules (Continued)

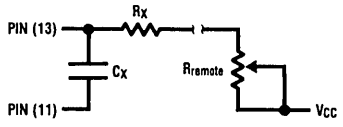
The K factor is not a constant, but, varies with C_X. See *Figure 2.*



TL/F/6385–3

FIGURE 2

4. The switching diode required for most TTL one-shots when using an electrolytic timing capacitor is not needed for the 'LS122 and should not be used.
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



TL/F/6385–4

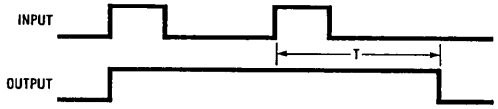
Note: "R_{remote}" should be as close to the device pins as possible.

FIGURE 3

6. The retriggerable pulse width is calculated as shown below:

$$T = T_W + t_{PLH} = 0.50 \times R_X \times C_X + T_{PLH}$$

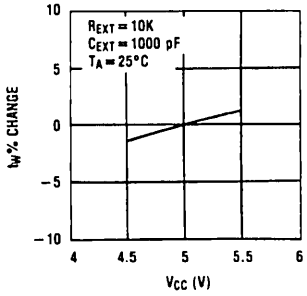
The retriggered pulse width is equal to the pulse width plus a delay time period *(Figure 4).*



TL/F/6385–5

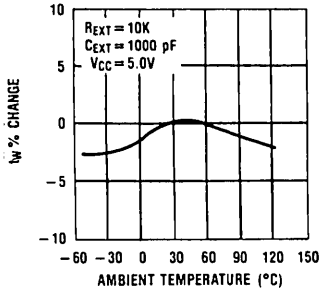
FIGURE 4

7. Output pulse width variation versus V_{CC} and operation temperatures: *Figure 5* depicts the relationship between pulse width variation versus V_{CC}; and *Figure 6* depicts pulse width variation versus temperatures.



TL/F/6385–6

FIGURE 5



TL/F/6385–7

FIGURE 6

8. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (13) and (11) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
9. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

***For further detailed device characteristics and output performance please refer to the NSC one-shot application note AN-366.**

2

National Semiconductor Corporation

DM54LS123/DM74LS123 Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM54/74LS123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading edge or trailing edge triggering. Pin (A) is an active-low transition trigger input and pin (B) is an active-high transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components. The clear input also serves as a trigger input when it is pulsed with a low level pulse transition (⎍⎍). To obtain the best trouble free operation from this device please read the operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

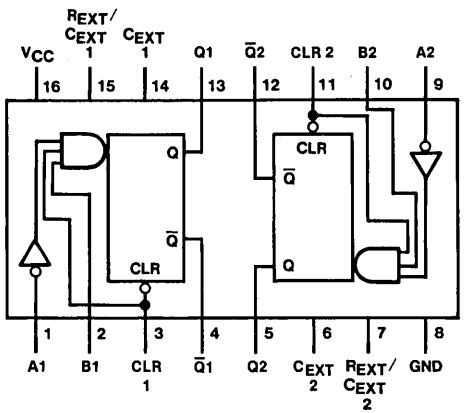
- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Compensated for V_{CC} and temperature variations
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-low transition or active-high transition inputs or be reduced by use of the active-low or CLEAR input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

Connection Diagram

Dual-In-Line Package



TL/F/6386–1

Order Number DM54LS123J, DM74LS123M or DM74LS123N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⎍ = A Positive Pulse
⎍ = A Negative Pulse

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS123			DM74LS123			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width (Note 6)	A or B High	40			40			ns
		A or B Low	40			40			
		Clear Low	40			40			
R_{EXT}	External Timing Resistor		5		180	5		260	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			No Restriction			μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal				50			50	pF
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Notes 3,4 and 5)			12	20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 4: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to the clock.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Symbol	Parameters	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15pF, C_{EXT} = 0 pF, R_{EXT} = 5 kΩ		C_L = 15pF, C_{EXT} = 1000 pF, R_{EXT} = 10 KΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q		33			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q		44			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		56			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		45			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		27			ns
$t_{WQ(Min)}$	Minimum Width of Pulse at Output Q	A or B to Q		200			ns
$t_{W(out)}$	Output Pulse Width	A or B to Q			4	5	μs

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the 'LS123 one-shot and should not be used. In general the use of the switching diode is not recommended with retriggerable operation.
3. For $C_X >> 1000$ pF the output pulse width (T_W) is defined as follows:

   $T_W = KR_X C_X$

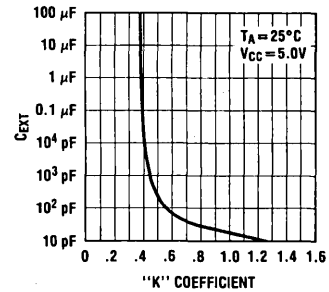
   where [R_X is in kΩ]

   [C_X is in pF]

   [T_W is in ns]

   $K \approx 0.37$

4. The multiplicative factor K is plotted as a function of C_X below for design considerations:

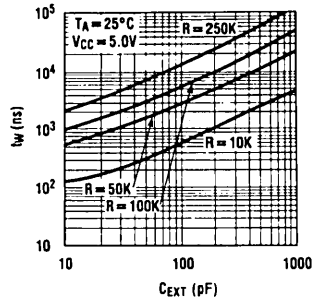


TL/F/6386–2

FIGURE 1

Operating Rules (Continued)

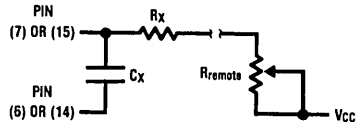
5. For C_X < 1000 pF see *Figure 2* for T_W vs C_X family curves with R_X as a parameter:



TL/F/6386–3

FIGURE 2

6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:



TL/F/6386–4

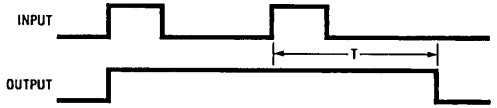
FIGURE 3

Note: "R_{remote}" should be as close to the device pin as possible.

7. The retriggerable pulse width is calculated as shown below:

$$T = T_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$$

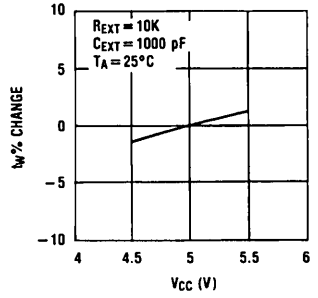
The retriggered pulse width is equal to the pulse width plus a delay time period *(Figure 4)*.



TL/F/6386–5

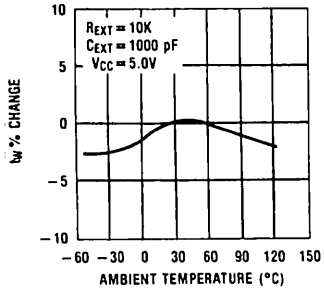
FIGURE 4

8. Output pulse width variation versus V_{CC} and temperatures: *Figure 5* depicts the relationship between pulse width variation versus V_{CC}, and *Figure 6* depicts pulse width variation versus temperatures.



TL/F/6386–6

FIGURE 5



TL/F/6386–7

FIGURE 6

9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
10. The C_{EXT} pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.
11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC}-pin as space permits.

For further detailed device characteristics and output performance please refer to the NSC one-shot application note AN-336.

2

National Semiconductor Corporation

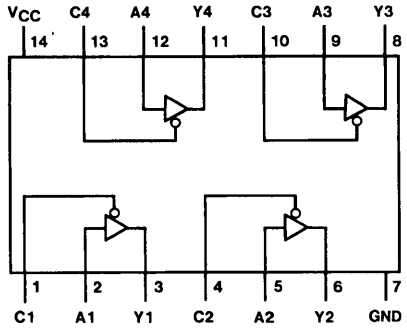
DM54LS125A/DM74LS125A Quad TRI-STATE® Buffers

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6387–1

Order Number DM54LS125AJ, DM74LS125AM or DM74LS125AN
See NS Package Number J14A, M14A or N14A

Function Table

$Y = A$

Inputs		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS125A			DM74LS125A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			11	20	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the data control (C) inputs at 4.5V and the data inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		22	ns
t_{PZH}	Output Enable Time to High Level Output		25		35	ns
t_{PZL}	Output Enable Time to Low Level Output		25		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)		20			ns

Note 1: C_L = 5pF.

National Semiconductor Corporation

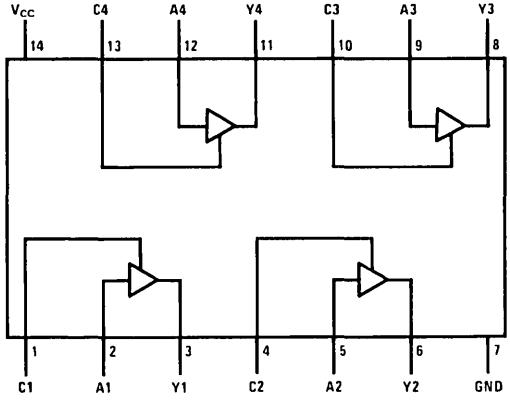
DM54LS126A/DM74LS126A Quad TRI-STATE® Buffers

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6388–1

Order Number DM54LS126AJ, DM74LS126AM or DM74LS126AN
See NS Package Number J14A, M14A or N14A

Function Table

$Y = A$

Inputs		Output
A	C	Y
L	H	L
H	H	H
X	L	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS126A			DM74LS126A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			12	22	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with both the output control and data inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		22	ns
t_{PZH}	Output Enable Time to High Level Output		30		36	ns
t_{PZL}	Output Enable Time to Low Level Output		30		42	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)		25			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)		25			ns

Note 1: C_L = 5pF.

National Semiconductor Corporation

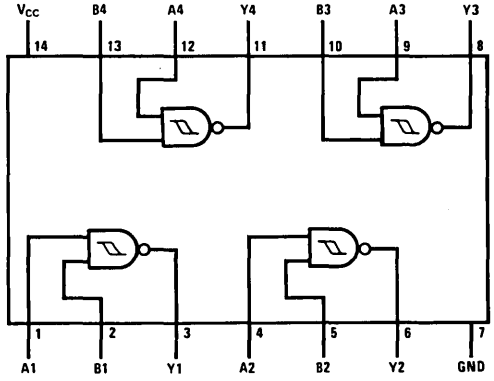
DM54LS132/DM74LS132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/6389–1

Order Number DM54LS132J, DM74LS132M or DM74LS132N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS132			DM74LS132			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.4	1.6	1.9	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.5	0.8	1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_I = V_{T-} Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_I = V_{T+} Max	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.14		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			5.9	11	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			8.2	14	mA

Note 1: V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	22	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	5	22	10	33	ns

National Semiconductor Corporation

DM54LS138/DM74LS138, DM54LS139/DM74LS139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

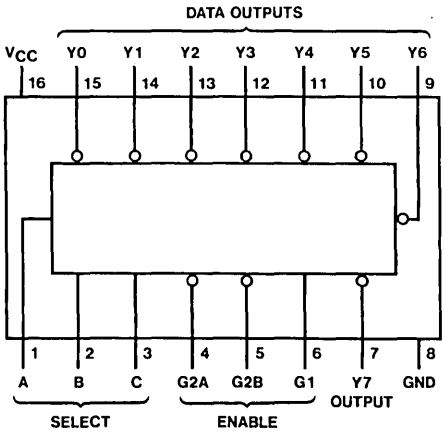
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - LS138 21 ns
  - LS139 21 ns
- Typical power dissipation
  - LS138 32 mW
  - LS139 34 mW

Connection Diagrams

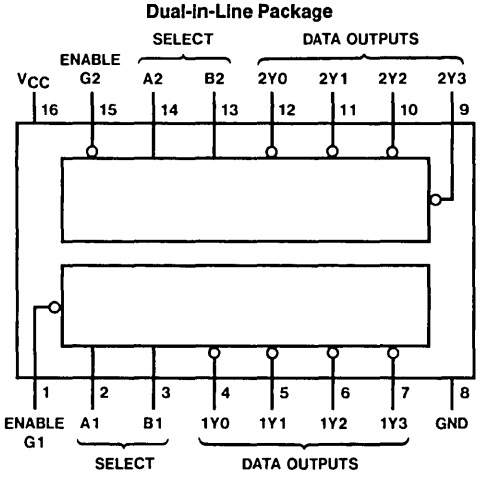
Dual-In-Line Package



TL/F/6391–1

Order Number DM54LS138J, DM74LS138M or DM74LS138N
See NS Package Number J16A, M16A or N16A

Dual-In-Line Package



TL/F/6391–2

Order Number DM54LS139J, DM74LS139M or DM74LS139N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS138			DM74LS138			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS138 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.3	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'LS138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Levels of Delay	R_L = 2 kΩ				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	2		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	3		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	2		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	2		24		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	3		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	3		28		40	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS139			DM74LS139			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS139 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.8	11	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'LS139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		40	ns

Function Tables

LS138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B

H = High Level, L = Low Level, X = Don't Care

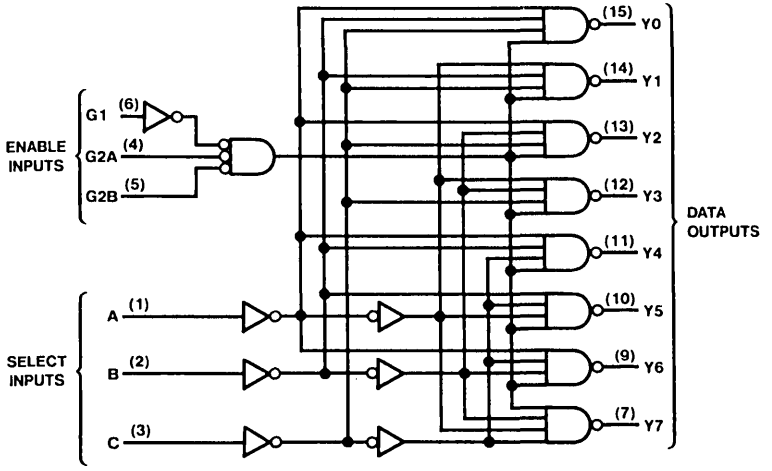
LS139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = High Level, L = Low Level, X = Don't Care

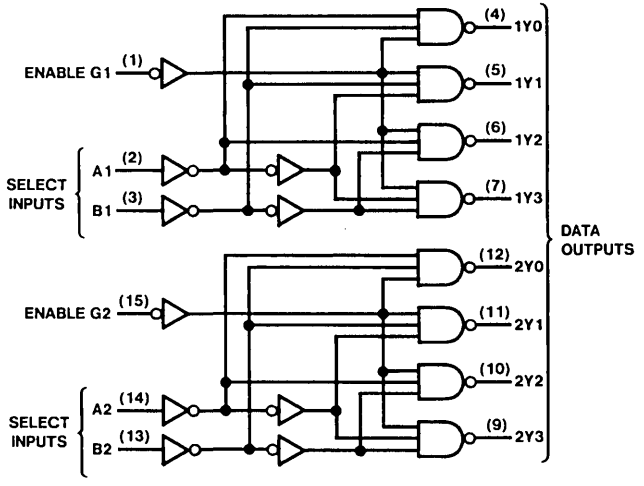
Logic Diagrams

LS138



TL/F/6391–3

LS139



TL/F/6391–4

2

National Semiconductor Corporation

DM54LS151/DM74LS151 Data Selector/Multiplexer

General Description

This data selector/multiplexer contains full on-chip decoding to select the desired data source. The LS151 selects one-of-eight data sources. The LS151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high, and the Y output low.

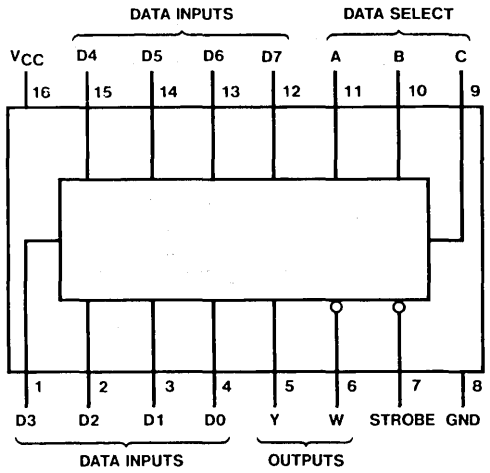
The LS151 features complementary W and Y outputs.

Features

- Select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time data input to W output 12.5 ns
- Typical power dissipation 30 mW

Connection Diagram

Dual-In-Line Package



TL/F/6392-1

Order Number DM54LS151J, DM74LS151M or DM74LS151N
See NS Package Number J16A, M16A or N16A

Truth Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

D0, D1...D7 = the level of the respective D input

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS151			DM74LS151			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

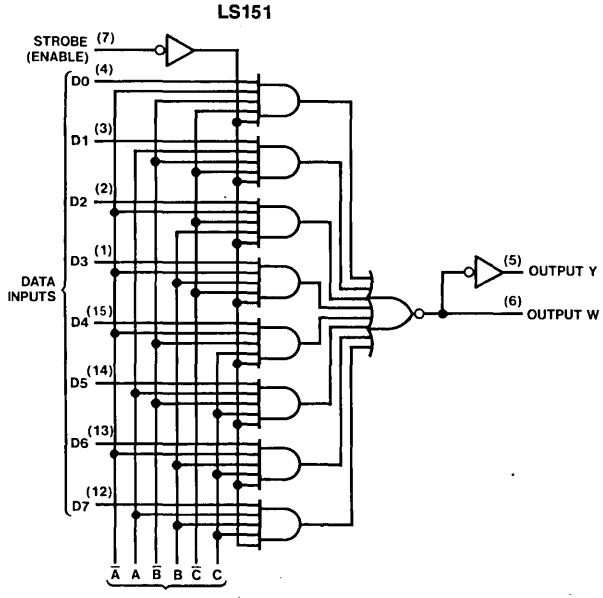
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, strobe and data select inputs at 4.5V, and all other inputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (4 Levels) to Y		43		46	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (4 Levels) to Y		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (3 Levels) to W		23		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (3 Levels) to W		32		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		42		44	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		32		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to W		24		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to W		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to Y		32		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to Y		26		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to W		21		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to W		20		27	ns

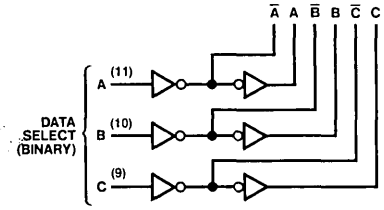
Logic Diagram



TL/F/6392-2

See Address Buffers to the Right

Address Buffers for 54LS151/74LS151



TL/F/6392-3

National Semiconductor Corporation

DM54LS153/DM74LS153 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

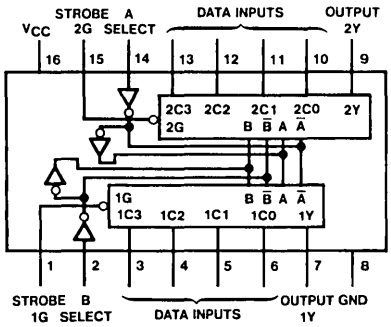
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Permits multiplexing from N lines to 1 line
- Performs at parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low impedance, totem pole outputs
- Typical average propagation delay times
  - — From data 14 ns
  - — From strobe 19 ns
  - — From select 22 ns
- Typical power dissipation 31 mW

Connection Diagram

Dual-In-Line Package



TL/F/6393-1

Order Number DM54LS153J, DM74LS153M or DM74LS153N
See NS Package Number J16A, M16A or N16A

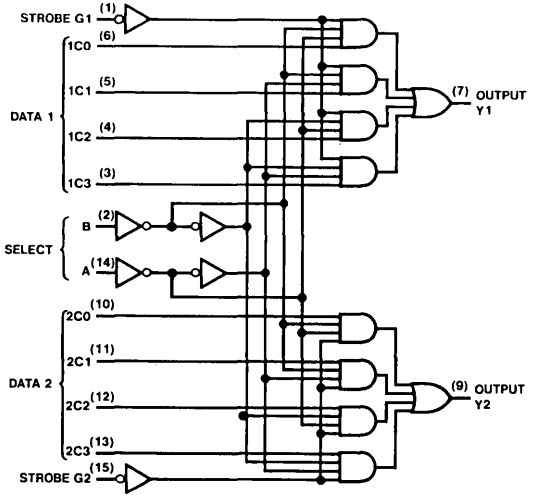
Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

Logic Diagram



TL/F/6393-2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS153			DM74LS153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.2	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		15		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		26		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		29		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		38		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		32		40	ns

National Semiconductor Corporation

DM54LS154/DM74LS154 4-Line to 16-Line Decoders/Demultiplexers

General Description

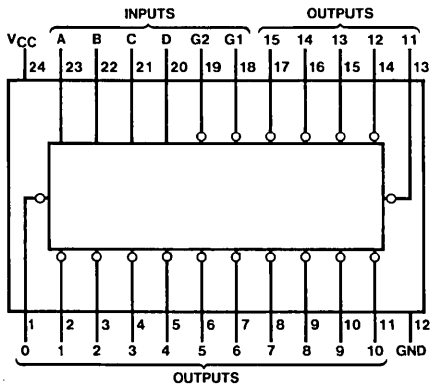
Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  3 levels of logic 23 ns
  Strobe 19 ns
- Typical power dissipation 45 mW

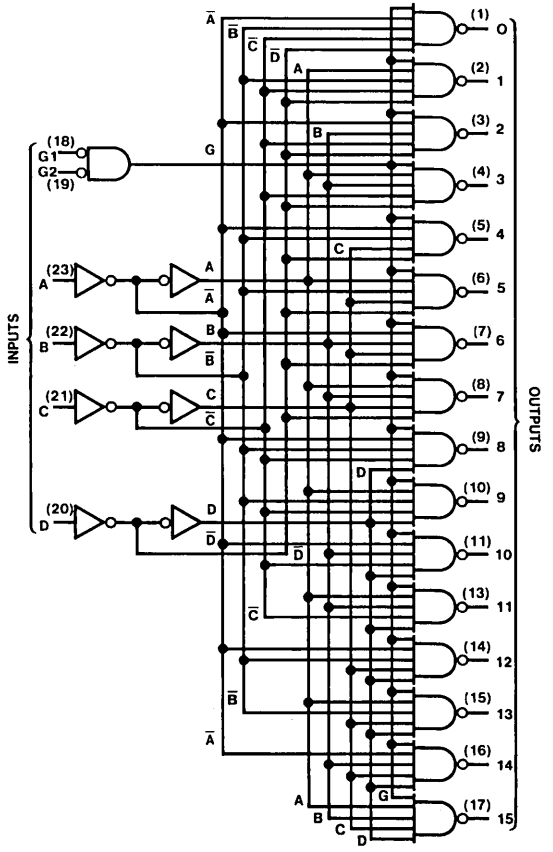
Connection and Logic Diagrams

Dual-In-Line Package



TL/F/6394–1

Order Number DM54LS154J,
DM74LS154WM or DM74LS154N
See NS Package Number J24A, M24B or N24A



TL/F/6394–2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS154			DM74LS154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		30		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		30		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		20		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		25		35	ns

Function Table

Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

National Semiconductor Corporation

DM54LS155/DM74LS155, DM54LS156/DM74LS156 Dual 2-Line to 4-Line Decoders/Demultiplexers

General Description

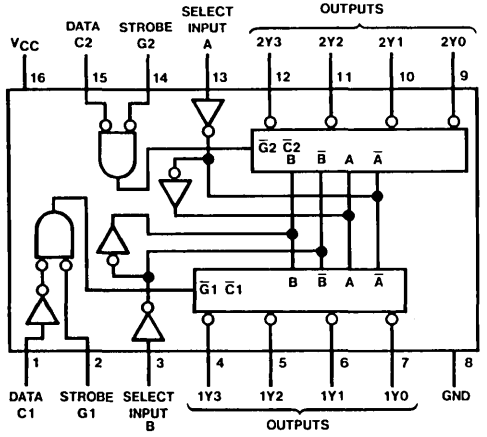
These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without external gating. Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

- Applications:
  Dual 2-to-4-line decoder
  Dual 1-to-4-line demultiplexer
  3-to-8-line decoder
  1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design
- Choice of outputs:
  Totem-pole (LS155)
  Open-collector (LS156)

Connection Diagram and Function Tables

Dual-In-Line Package



TL/F/6395–1

Order Number DM54LS155J, DM74LS155M, DM74LS155N, DM54LS156J, DM74LS156M or DM74LS156N
See NS Package Number J16A, M16A or N16A

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs C1 and C2 connected together
‡G = inputs G1 and G2 connected together
H = high level, L = low level, X = don't care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS155			DM74LS155			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS155 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.1	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open, A,B, and C1 inputs at 4.5V, and C2, G1, and G2 inputs grounded.

'LS155 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		18		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		27		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		18		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		27		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		27		35	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS156			DM74LS156			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS156 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.36	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			6.1	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

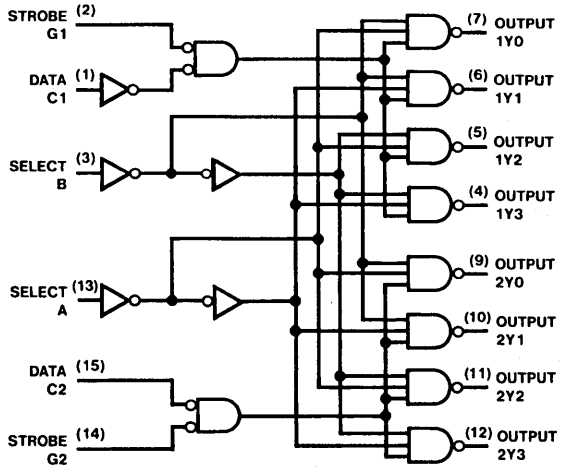
Note 2: I_{CC} is measured with all outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		33		43	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		33		43	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		28		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		34		43	ns

Logic Diagram



TL/F/6395–2

National Semiconductor Corporation

DM54LS157/DM74LS157, DM54LS158/DM74LS158 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The LS157 presents true data whereas the LS158 presents inverted data to minimize propagation delay time.

Applications

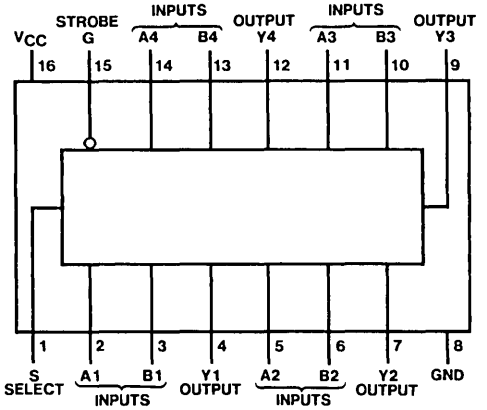
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

- Buffered inputs and outputs
- Typical Propagation Time
  LS157 9 ns
  LS158 7 ns
- Typical Power Dissipation
  LS157 49 mW
  LS158 24 mW

Connection Diagrams

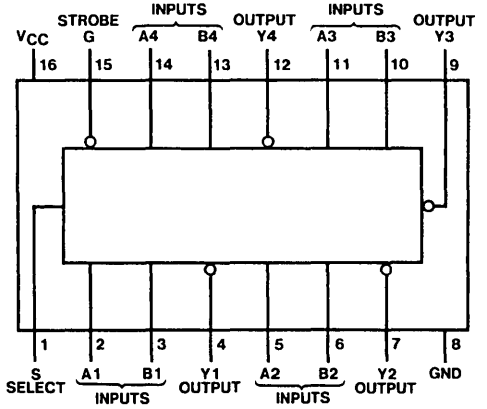
Dual-In-Line Package



TL/F/6396–1

Order Number DM54LS157J, DM74LS157M or DM74LS157N
See NS Package Number J16A, M16A or N16A

Dual-In-Line Package



TL/F/6396–2

Order Number DM54LS158J, DM74LS158M or DM74LS158N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs				Output Y	
Strobe	Select	A	B	LS157	LS158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS157			DM74LS157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS157 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	S or G			0.2	mA
			A or B			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	S or G			40	µA
			A or B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	S or G			−0.8	mA
			A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			9.7	16	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

'LS157 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		14		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		14		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		21		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		23		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		27		32	ns

Recommended Operating Conditions

Symbol	Parameter	DM54LS158			DM74LS158			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS158 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	S or G			0.2	mA
			A or B			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	S or G			40	μA
			A or B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	S or G			−0.8	mA
			A or B			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4.8	8	mA

'LS158 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		12		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		12		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		17		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		18		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		24		36	ns

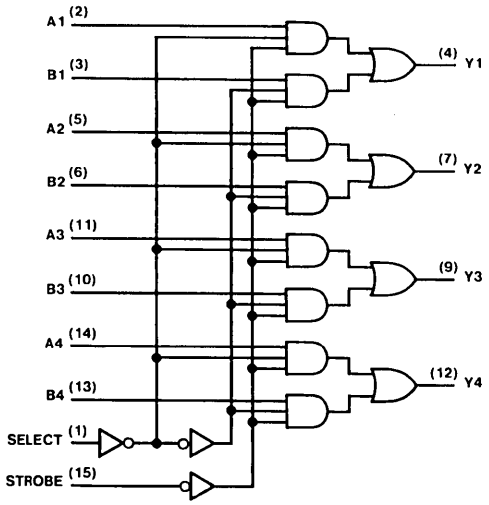
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Logic Diagrams

LS157



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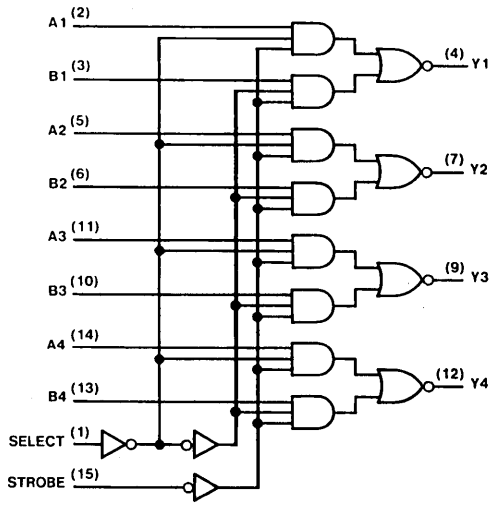
LS158



TL/F/6396–4

National Semiconductor Corporation

DM54LS161A/DM74LS161A, DM54LS163A/DM74LS163A Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The LS161A and LS163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the LS161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the LS163A is synchronous; and a low level at the clear inputs sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output.

Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur, regardless of the logic level of the clock.

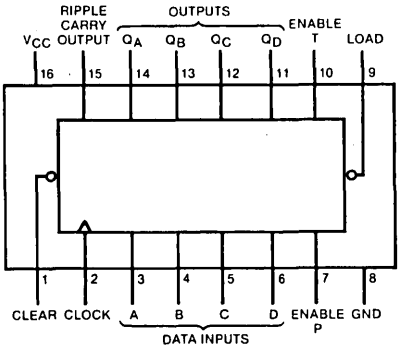
These counters feature a fully independent clock circuit. Changes made to control inputs (enable P or T or load) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable set-up and hold times.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical propagation time, clock to Q output 14 ns
- Typical clock frequency 32 MHz
- Typical power dissipation 93 mW

Connection Diagram

Dual-In-Line Package



TL/F/6397–1

Order Numbers DM54LS161AJ, DM54LS163AJ, DM74LS161AM, DM74LS163AM, DM74LS161AN or DM74LS163AN
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS161A			DM74LS161A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 1)	Clock	20	6		20	6		ns
		Clear	20	9		20	9		
	Pulse Width (Note 2)	Clock	25			25			ns
		Clear	25			25			
t_{SU}	Setup Time (Note 1)	Data	20	8		20	8		ns
		Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time (Note 2)	Data	20			20			ns
		Enable P	30			30			
		Load	30			30			
t_H	Hold Time (Note 1)	Data	0	−3		0	−3		ns
		Others	0	−3		0	−3		
	Hold Time (Note 2)	Data	5			5			ns
		Others	5			5			
t_{REL}	Clear Release Time (Note 1)		20			20			ns
	Clear Release Time (Note 2)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5.5V.

'LS161 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable T			0.2	mA
			Clock			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			40	μA
			Clock			40	
			Load			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−0.8	mA
			Clock			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			18	31	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			19	32	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

'LS161 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		22		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		27		38	ns

'LS161 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load) (Continued)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		29		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		35		45	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS163A			DM74LS163A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 1)	Clock	20	6		20	6		ns
		Clear	20	9		20	9		
	Pulse Width (Note 2)	Clock	25			25			ns
		Clear	25			25			
t_{SU}	Setup Time (Note 1)	Data	20	8		20	8		ns
		Enable P	25	17		25	17		
		Load	25	15		25	15		
	Setup Time (Note 2)	Data	20			20			ns
		Enable P	30			30			
		Load	30			30			
t_H	Hold Time (Note 1)	Data	0	−3		0	−3		ns
		Others	0	−3		0	−3		
	Hold Time (Note 2)	Data	5			5			ns
		Others	5			5			
t_{REL}	Clear Release Time (Note 1)		20			20			ns
	Clear Release Time (Note 2)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

'LS163 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable T			0.2	mA
			Clock, Clear			0.2	
			Load			0.2	
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable T			40	μA
			Load			40	
			Clock, Clear			40	
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable T			−0.8	mA
			Clock, Clear			−0.8	
			Load			−0.8	
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			18	31	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			18	32	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with the load high, then again with the load low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

'LS163 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		30		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load High)		22		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load High)		27		38	ns

'LS163 Switching Characteristics

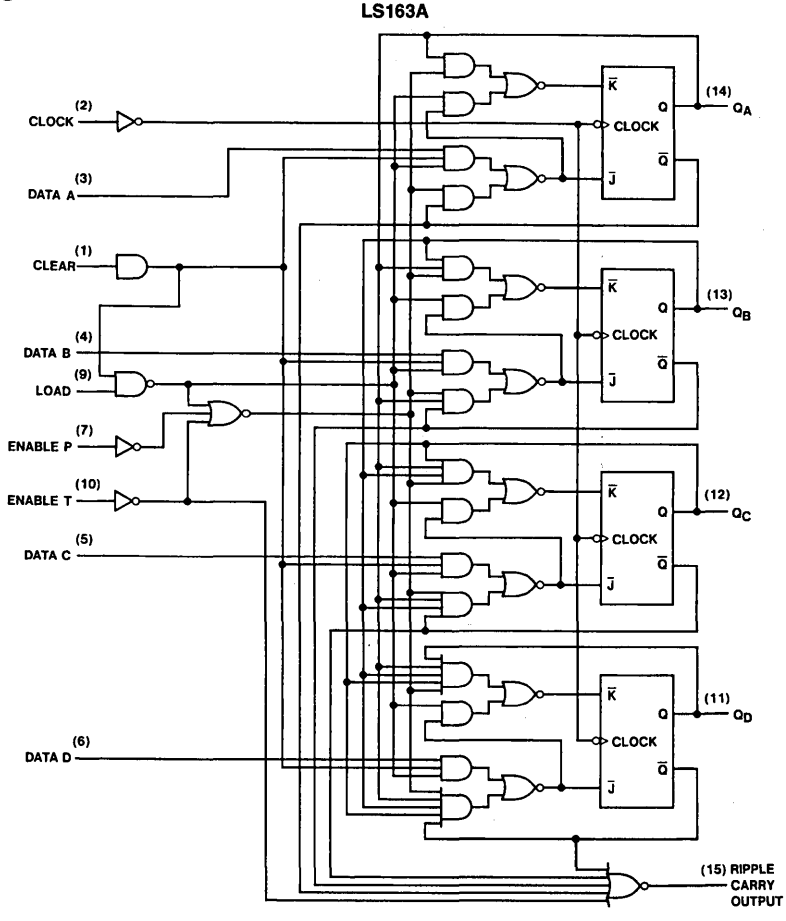
at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load) (Continued)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q (Load Low)		24		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q (Load Low)		29		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q (Note 1)		35		45	ns

Note 1: The propagation delay clear to output is measured from the clock input transition.

Logic Diagram

LS163A

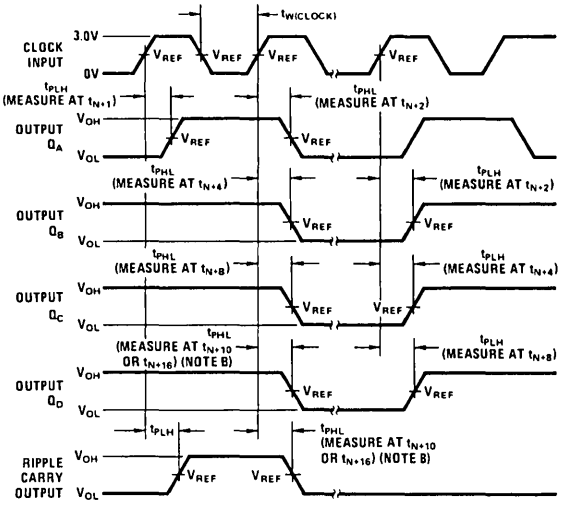


TL/F/6397–2

The LS161A is similar, however, the clear buffer is connected directly to the flip flops.

Parameter Measurement Information

Switching Time Waveforms



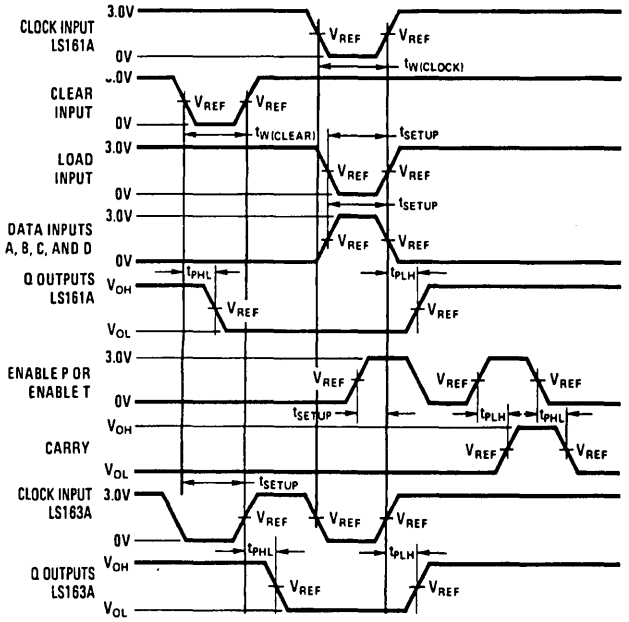
TL/F/6397–3

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+16} where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5V$.

Switching Time Waveforms



TL/F/6397–4

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at t_{n+0}.

Note C: $V_{REF} = 1.3V$.

National Semiconductor Corporation

DM54LS164/DM74LS164 8-Bit Serial In/Parallel Out Shift Registers

General Description

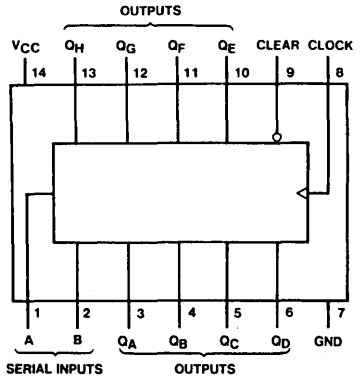
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 80 mW

Connection Diagram

Dual-In-Line Package



TL/F/6398–1

Order Number DM54LS164J, DM74LS164M or DM74LS164N
See NS Package Number J14A, M14A or N14A

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

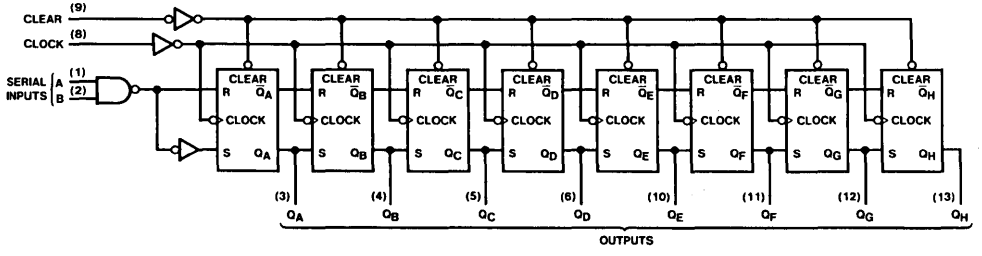
X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Logic Diagram



TL/F/6398–2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" tables will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS164			DM74LS164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		15			15			ns
t_H	Data Hold Time (Note 4)		5			5			ns
t_{REL}	Clear Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.4		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max	DM54		0.25	0.4	V
		V_{IL} = Max, V_{IH} = Min	DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			16	27	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

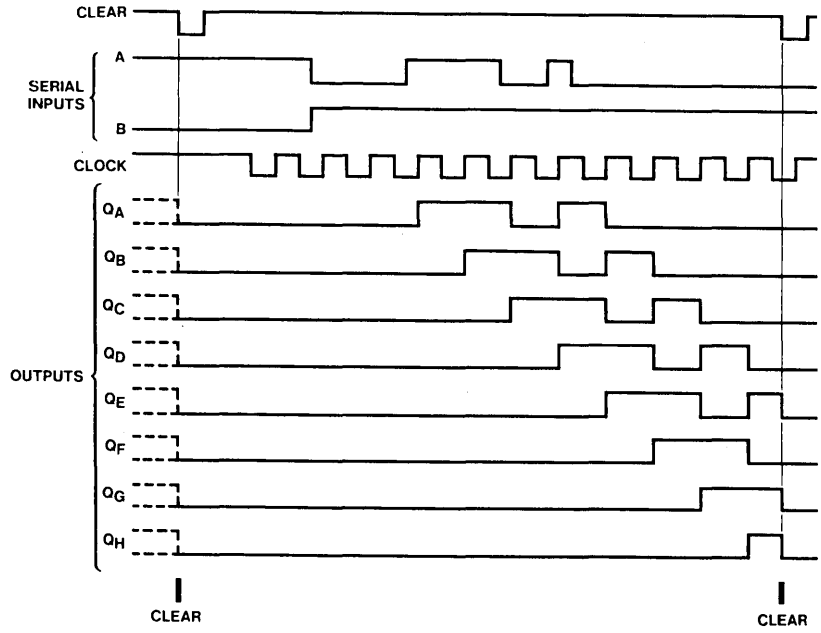
Note 3: I_{CC} is measured with all outputs open, the SERIAL input grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		32		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		36		45	ns

Timing Diagram



TL/F/6398–3

National Semiconductor Corporation

DM54LS165/DM74LS165 8-Bit Parallel In/Serial Output Shift Registers

General Description

This device is an 8-bit serial shift register which shifts data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high.

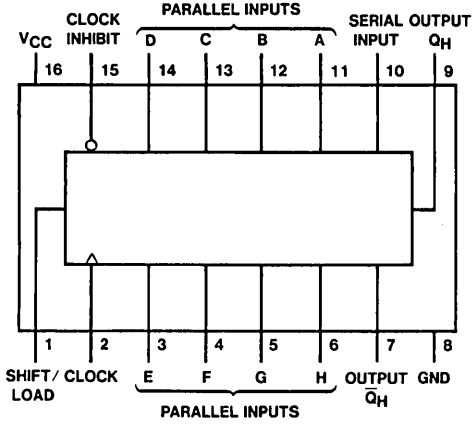
Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 35 MHz
- Typical power dissipation 105 mW

Connection Diagram

Dual-In-Line Package



TL/F/6399-1

Order Number DM54LS165J, DM74LS165WM or DM74LS165N
See NS Package Number J16A, M16B or N16A

Function Table

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	X	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low-to-high level

a...h = The level of steady-state input at inputs A through H, respectively.

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS165			DM74LS165			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 2)	Clock	25			25			ns
		Load	15			15			
t_{SU}	Setup Time (Note 6)	Parallel	10			10			ns
		Serial	20			20			
		Enable	30			30			
		Shift	45			45			
t_H	Hold Time (Note 6)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Shift/Load			0.3	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Shift/Load			60	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Shift/Load			−1.2	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			21	36	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V

Note 3: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open, clock inhibit and shift/load at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then again grounded.

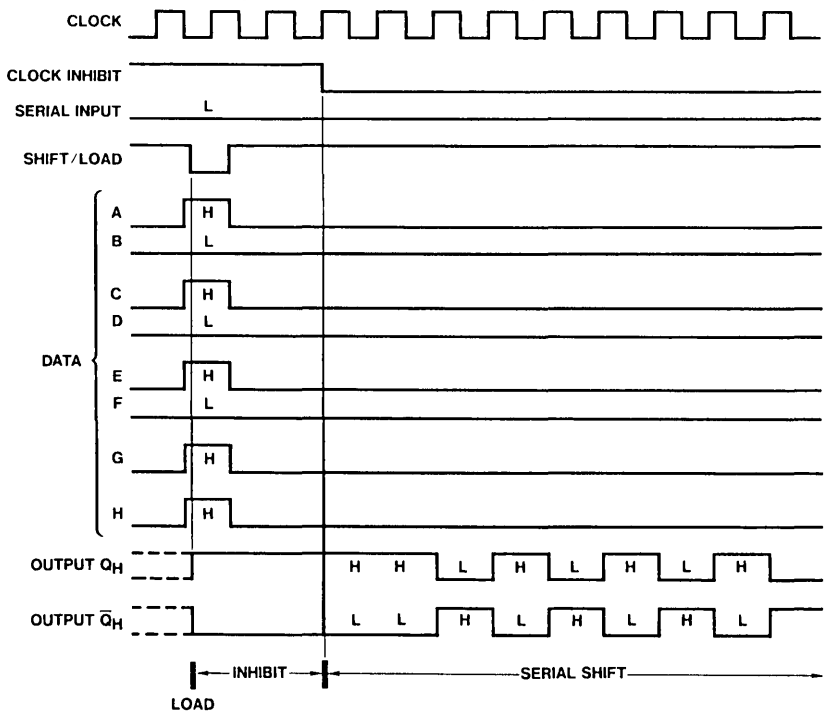
Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		35		37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		35		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		40		42	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		40		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to Q_H		25		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to Q_H		30		37	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to $\overline{Q}_H$		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to $\overline{Q}_H$		25		32	ns

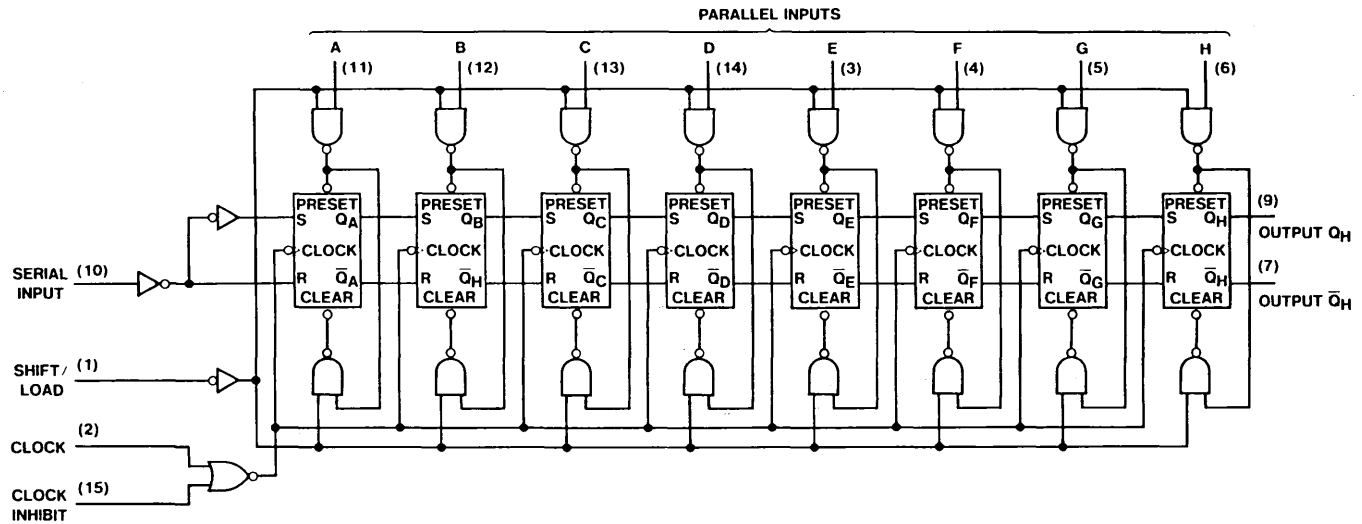
Timing Diagram

Typical Shift, Load, and Inhibit Sequences



TL/F/6399–3

Logic Diagram



TL/F/6399–2

National Semiconductor Corporation

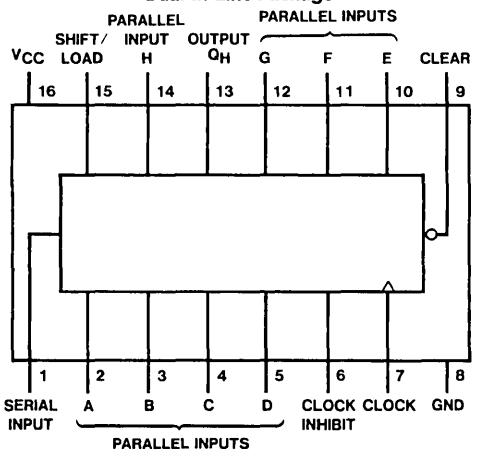
DM54LS166/DM74LS166 8-Bit Parallel-In/Serial-Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Connection Diagram

Dual-In-Line Package



TL/F/6400–1

Order Number DM54LS166J, DM74LS166WM or DM74LS166N
See NS Package Number J16A, M16B or N16A

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS166			DM74LS166			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 6)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 6)	Mode	30			30			ns
		Data	20			20			
t_H	Hold Time (Note 6)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			22	38	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open, 4.5V applied to the serial input, all other inputs except the CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V is applied to the CLOCK.

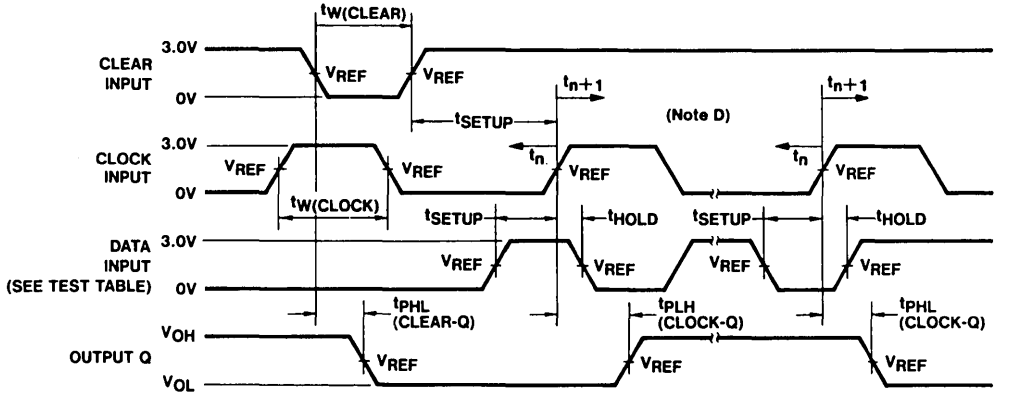
Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output	8	35		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output	8	35		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output	6	30		36	ns

Parameter Measurement Information

Voltage Waveforms



TL/F/6400–2

Test Table for Synchronous Inputs

Data Input for Test	Shift/Load	Output Tested (See Note C)
H	0V	Q_H at T_{N+1}
Serial Input	4.5V	Q_H at T_{N+8}

Note A: The clock pulse has the following characteristics: $t_{W(clock)} \geq$ 20 ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{W(clear)} \geq$ 20 ns and t_{HOLD} = 0 ns. When testing f_{MAX}, vary the clock PRR.

Note B: A clear pulse is applied prior to each test.

Note C: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+8} with a functional test.

Note D: t_n = bit time before clocking transition

t_{n+1} = bit time after one clocking transition

t_{n+8} = bit time after eight clocking transitions

Note E: V_{REF} = 1.3V.

Function Table

Inputs						Internal Outputs		Output Q_H
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

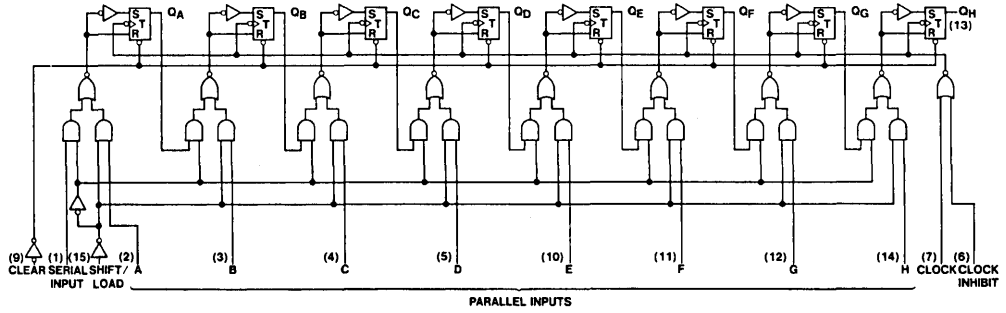
↑ = Transition from low to high level

a . . . h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn}, = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

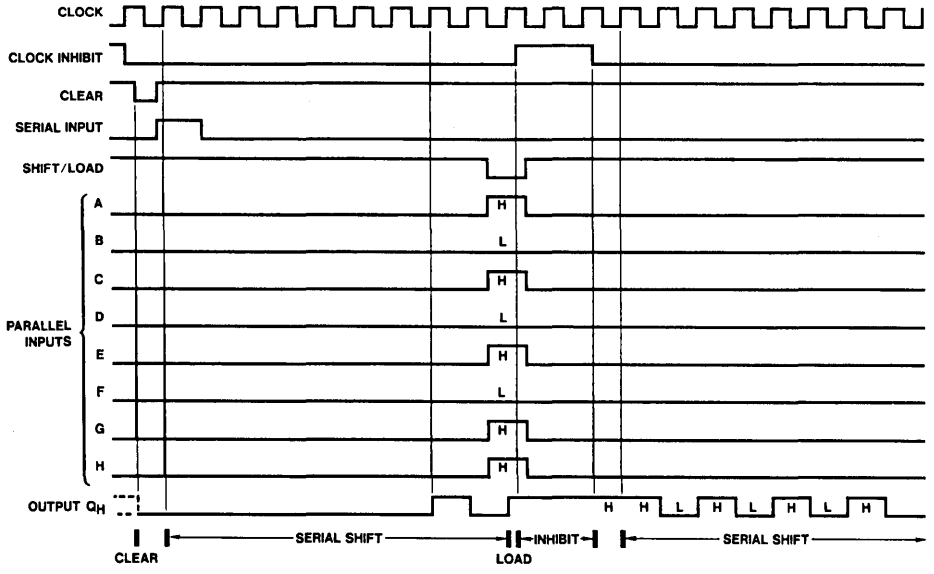
Logic Diagram



TL/F/6400–3

Timing Diagram

Typical Clear, Shift, Load, Inhibit and Shift Sequences



TL/F/6400–4

National Semiconductor Corporation

DM54LS169A/DM74LS169A Synchronous 4-Bit Up/Down Binary Counter

General Description

This synchronous presettable counter features an internal carry look-ahead for cascading in high-speed counting applications. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs all change at the same time when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising edge of the clock waveform.

This counter is fully programmable; that is, the outputs may each be preset either high or low. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry permits cascading counters for n-bit synchronous applications without additional gating. Both count-enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry outputs. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up, and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successively cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode clamped to minimize transmission-line effects, thereby simplifying system design.

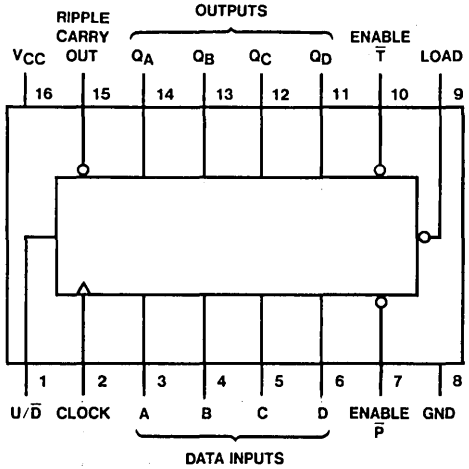
This counter features a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down), which modify the operating mode, have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

Features

- Fully synchronous operation for counting and programming.
- Internal look-ahead for fast counting.
- Carry output for n-bit cascading.
- Fully independent clock circuit

Connection Diagram

Dual-In-Line Package



TL/F/6401–1

Order Number DM54LS169AJ, DM74LS169AM or DM74LS169AN
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS169A			DM74LS169A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Clock Pulse Width (Note 3)		25			25			ns
t_{SU}	Setup Time (Note 3)	Data	20			20			ns
		Enable $\overline{T}$ or $\overline{P}$	20			20			
		Load	25			25			
		U/D	30			30			
t_H	Hold Time (Note 3)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable $\overline{T}$			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable $\overline{T}$			40	μA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable $\overline{T}$			−0.8	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			20	34	mA

Note 4: All typicals are at V_{CC} = 5V and T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

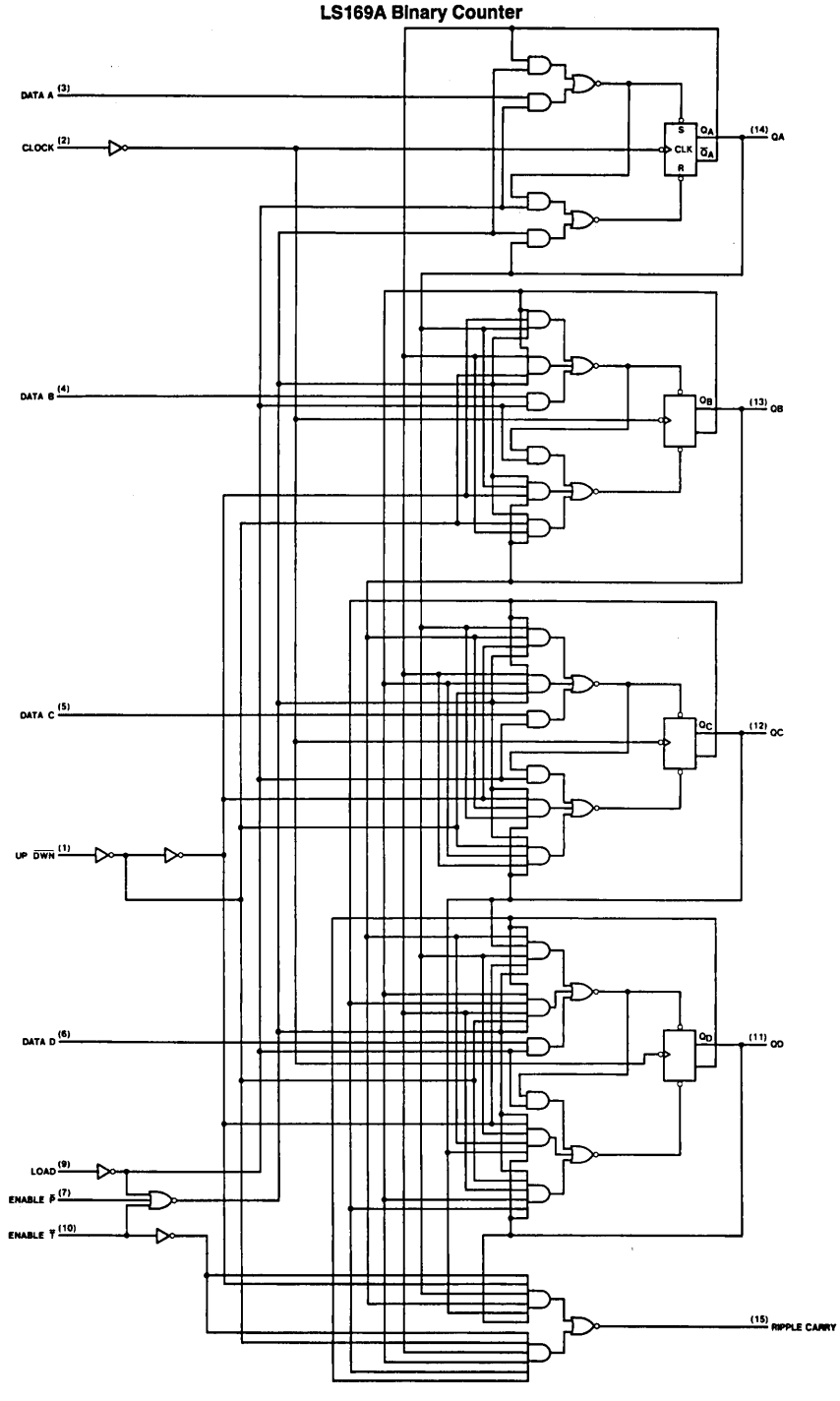
Note 6: I_{CC} is measured after a momentary 4.5V, then ground, is applied to the CLOCK with all other inputs grounded and all the outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		35		39	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		35		44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		23		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable $\overline{T}$ to Ripple Carry		18		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable $\overline{T}$ to Ripple Carry		18		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Up/Down to Ripple Carry (Note 1)		25		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Up/Down to Ripple Carry (Note 1)		29		38	ns

Note 1: The propagation delay from UP/DOWN to RIPPLE CARRY must be measured with the counter at either a minimum or a maximum count. As the logic level of the up/down input is changed, the ripple carry output will follow. If the count is minimum, the ripple carry output transition will be in phase. If the count is maximum, the ripple carry output will be out of phase.

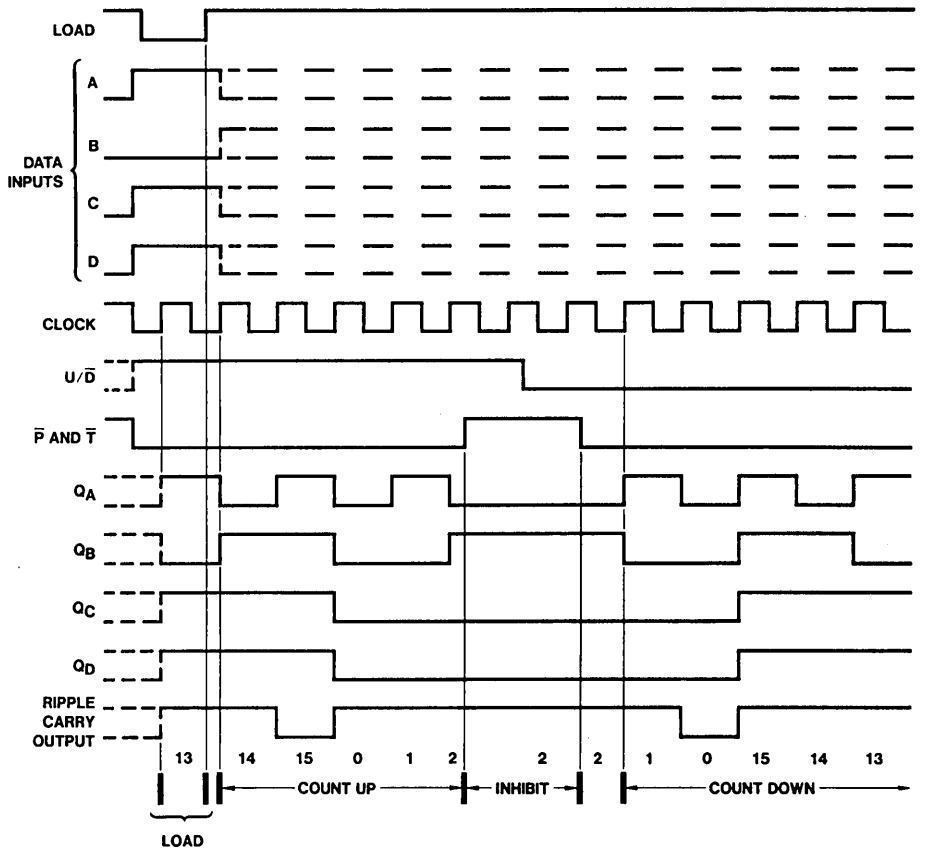
Logic Diagram



TL/F/6401–2

Timing Diagram

LS169A Binary Counters
Typical Load, Count, and Inhibit Sequences



TL/F/6401–3

National Semiconductor Corporation

DM54LS173A/DM74LS173A TRI-STATE® 4-Bit D-Type Register

General Description

This four-bit register contains D-type flip-flops with totem-pole TRI-STATE® outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the truth table.

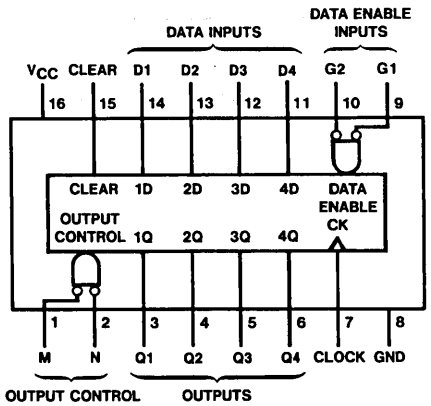
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers

Connection Diagram

Dual-In-Line Package



TL/F/6403–1

Order Number DM54LS173AJ, DM74LS173AM or DM74LS173AN
See NS Package Number J16A, M16A or N16A

Function Table

Inputs					Output Q
Clear	Clock	Data Enable		Data D	
		G1	G2		
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = High Level (Steady State)

L = Low Level (Steady State)

↑ = Low-to-High Level Transition

X = Don't Care (Any Input Including Transitions)

Q_0 = The Level of Q Before the Indicated Steady State Input Conditions Were Established.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS173A			DM74LS173A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 3)	Clock	17			17			ns
		Clear	17			17			
t_{SU}	Setup Time (Note 3)	Enable	17			17			ns
		Data	10			10			
t_H	Hold Time (Note 3)	Enable	0			0			ns
		Data	0			0			
t_{REL}	Clear Release Time		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 45 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.
Note 2: C_L = 150 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.
Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			17	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		20		ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		25		34	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		30		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		30		40	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control (M or N) to Any Q	7	21	9	34	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control (M or N) to Any Q	7	27	9	45	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 7)	Output Control (M or N) to Any Q	3	17			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 7)	Output Control (M or N) to Any Q	3	20			ns

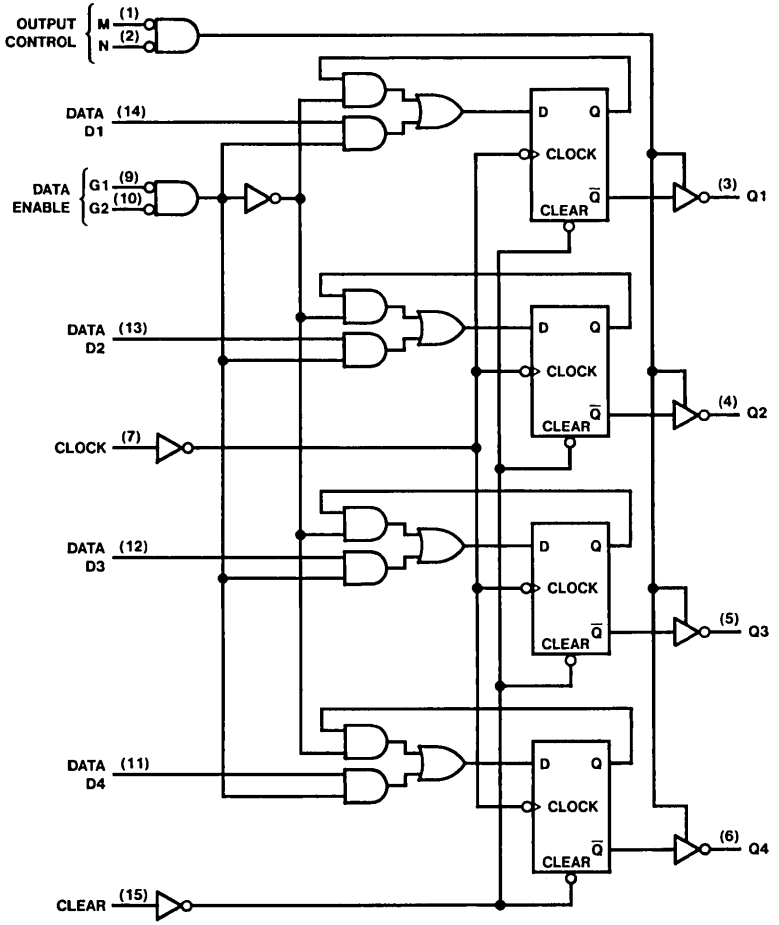
Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all outputs open: Clear grounded after a momentary 4.5V; N, G1, G2 and all data inputs grounded: and the CLOCK and M input at 4.5V.

Note 7: C_L = 5 pF.

Logic Diagram



TL/F/6403–2

National Semiconductor Corporation

DM54LS174/DM74LS174, DM54LS175/DM74LS175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

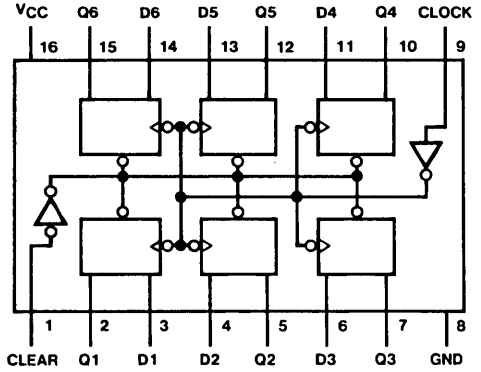
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- LS174 contains six flip-flops with single-rail outputs
- LS175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 14 mW

Connection Diagrams

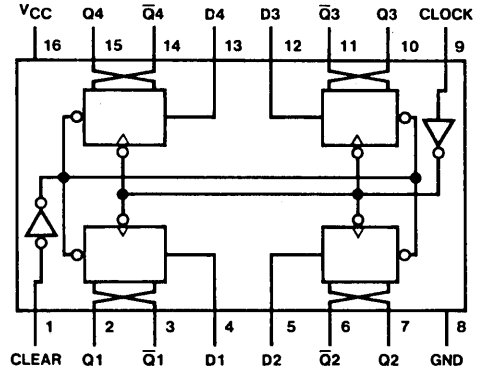
Dual-In-Line Package



TL/F/6404–1

Order Number DM54LS174J, DM74LS174M or DM74LS174N
See NS Package Number J16A, M16A or N16A

Dual-In-Line Package



TL/F/6404–2

Order Number DM54LS175J, DM74LS175M or DM74LS175N
See NS Package Number J16A, M16A or N16A

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$†**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)

L = Low Level (steady state)

X = Don't Care

↑ = Transition from low to high level

Q_0 = The level of Q before the indicated steady-state input conditions were established.

† = LS175 only

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS174			DM74LS174			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width (Note 6)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 6)		20			20			ns
t_H	Data Hold Time (Note 6)		0			0			ns
t_{REL}	Clear Release Time (Note 6)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'LS174 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock			−0.4	mA
			Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			16	26	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock.

Note 6: T_A = 25°C and V_{CC} = 5V.

'LS174 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		30		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		35		42	ns

Recommended Operating Conditions

Symbol	Parameter		DM54LS175			DM74LS175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
f_{CLK}	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width (Note 3)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 3)		20			20			ns
t_H	Data Hold Time (Note 3)		0			0			ns
t_{REL}	Clear Release Time (Note 3)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

'LS175 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current@Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock			−0.4	mA
			Clear			−0.4	
			Data			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			11	18	mA

'LS175 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		30		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		30		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		35		42	ns

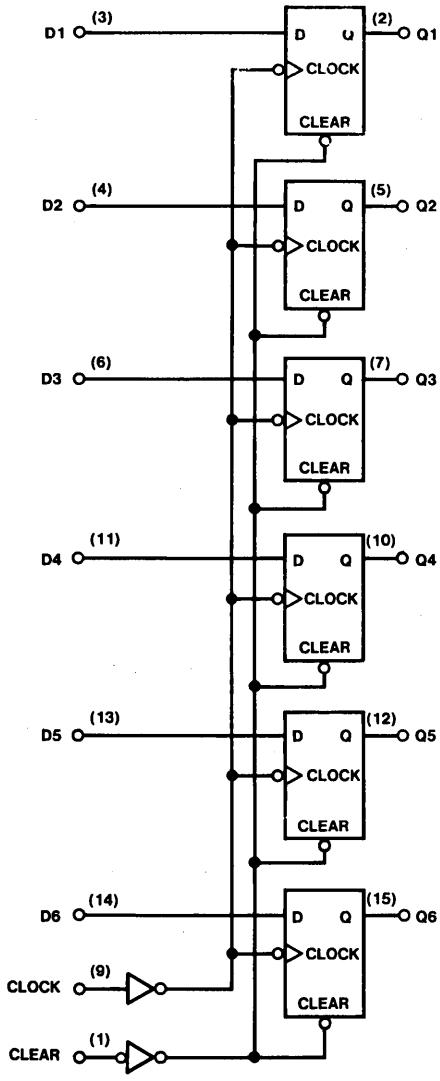
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the clock input.

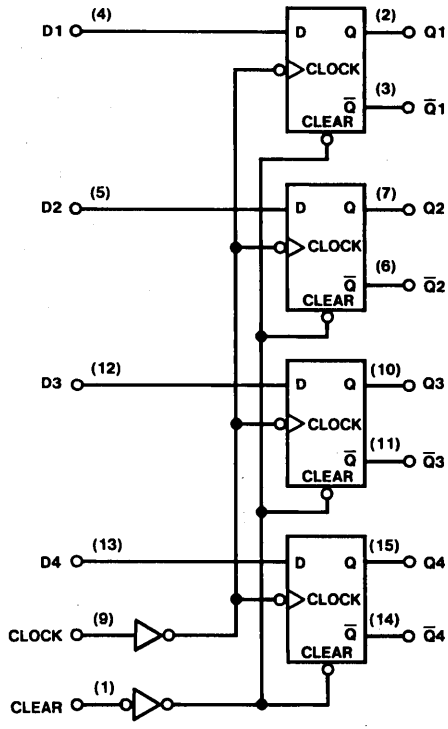
Logic Diagrams

LS174



TL/F/6404–3

LS175



TL/F/6404–4

National Semiconductor Corporation

DM54LS190/DM74LS190, DM54LS191/DM74LS191 Synchronous 4-Bit Up/Down Counters with Mode Control

General Description

These circuits are synchronous, reversible, up/down counters. The LS191 is a 4-bit binary counter and the LS190 is a BCD counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

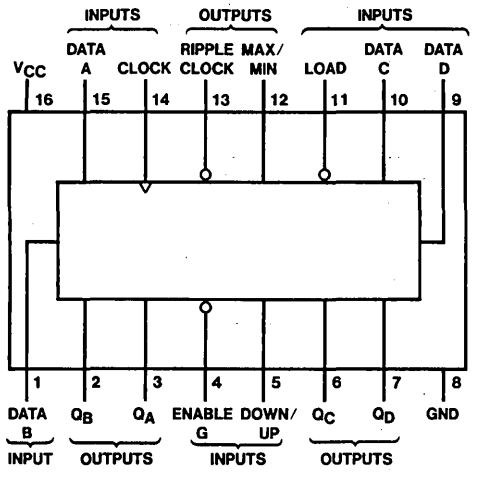
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Counts 8-4-2-1 BCD or binary
- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications
- Average propagation delay 20 ns
- Typical clock frequency 25 MHz
- Typical power dissipation 100 mW

Connection Diagram

Dual-In-Line-Package



TL/F/6405-1

Order Number DM54LS190J, DM54LS191J, DM74LS190M, DM74LS191M, DM74LS190N, or DM74LS191N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS190, LS191			DM74LS190, LS191			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 4)		0		20	0		20	MHz
t_W	Pulse Width (Note 4)	Clock	25			25			ns
		Load	35			35			
t_{SU}	Data Setup Time (Note 4)		20			20			ns
t_H	Data Hold Time (Note 4)		0			0			ns
t_{EN}	Enable Time to Clock (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'LS190 and 'LS191 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = − 18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Enable			0.3	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Enable			60	µA
			Others			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable			−1.08	mA
			Others			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			20	35	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: T_A = 25°C and V_{CC} = 5V.

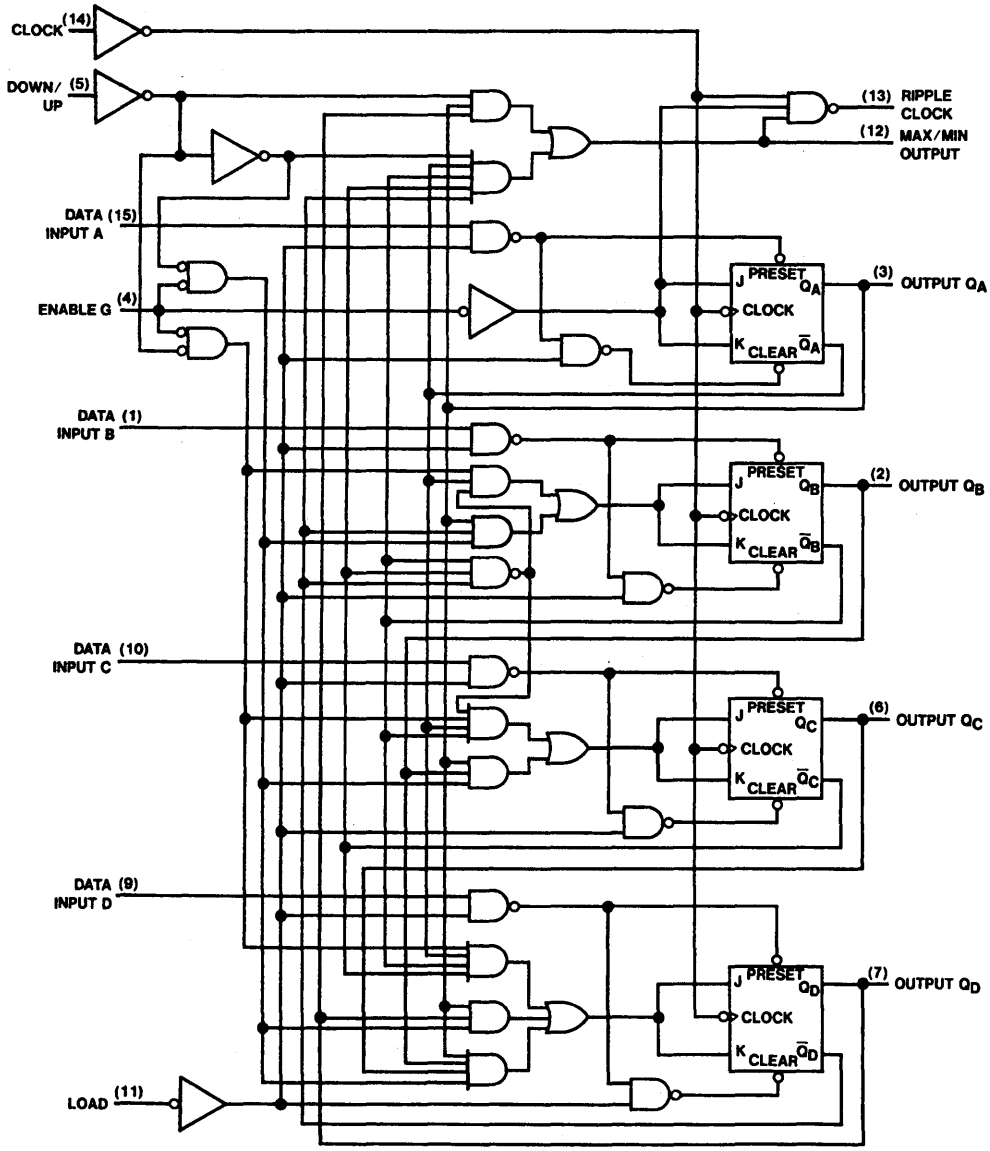
'LS190 and 'LS191 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		20		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		33		43	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		50		59	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Any Q		22		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Any Q		50		62	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Clock		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Clock		24		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		24		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		36		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Max/Min		42		47	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Max/Min		52		65	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Up/Down to Ripple Clock		45		50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Up/Down to Ripple Clock		45		54	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Down/Up to Max/Min		33		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Down/Up to Max/Min		33		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Ripple Clock		33		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Ripple Clock		33		42	ns

Logic Diagrams

LS190 Decade Counters

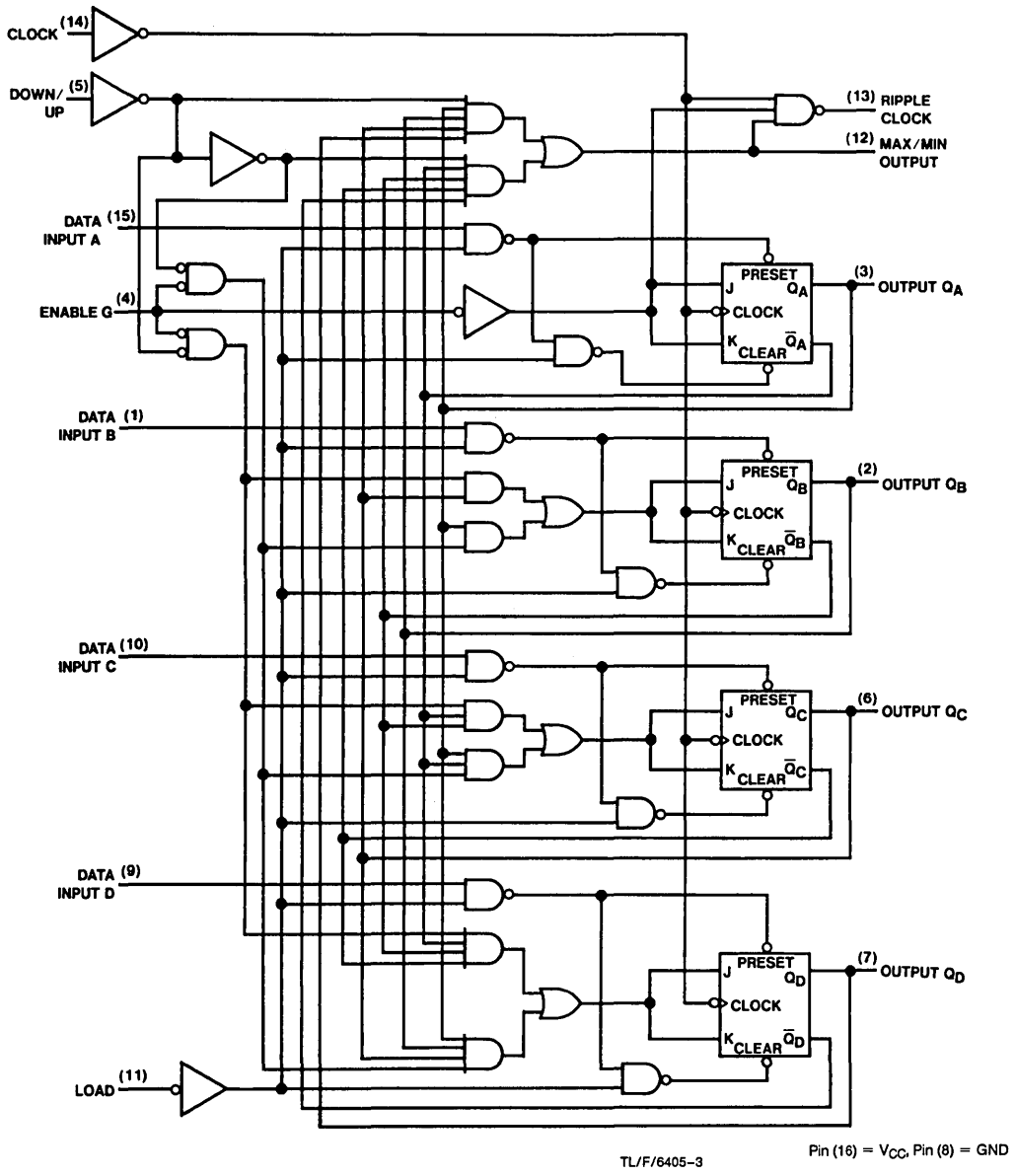


Pin (16) = V_{CC}, Pin (8) = GND

TL/F/6405–2

Logic Diagrams (Continued)

LS191 Binary Counters



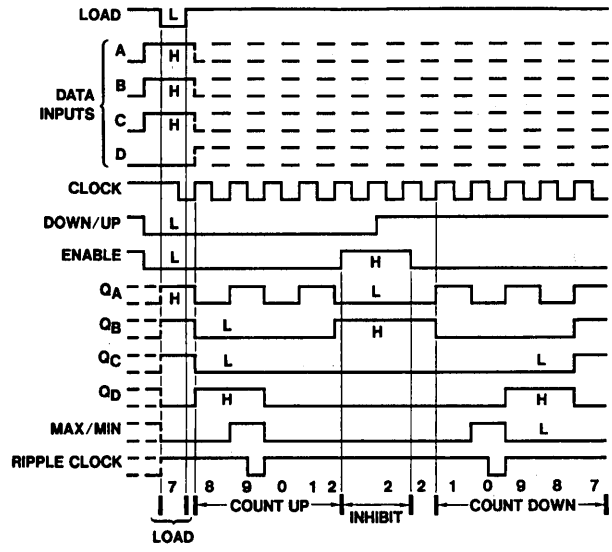
TL/F/6405–3

Pin (16) = V_{CC}, Pin (8) = GND

2

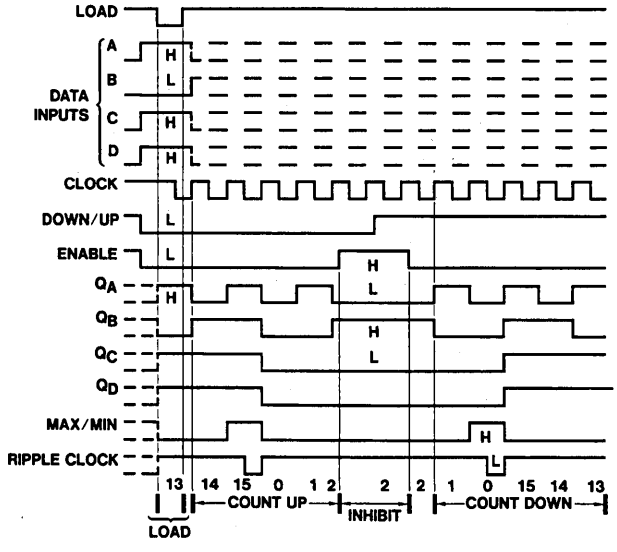
Timing Diagrams

LS190 Decade Counters
Typical Load, Count, and Inhibit Sequences



TL/F/6405–4

LS191 Binary Counters
Typical Load, Count, and Inhibit Sequences



TL/F/6405–5

National Semiconductor Corporation

DM54LS193/DM74LS193 Synchronous 4-Bit Up/Down Binary Counters with Dual Clock

General Description

This circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is held high.

The counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows.

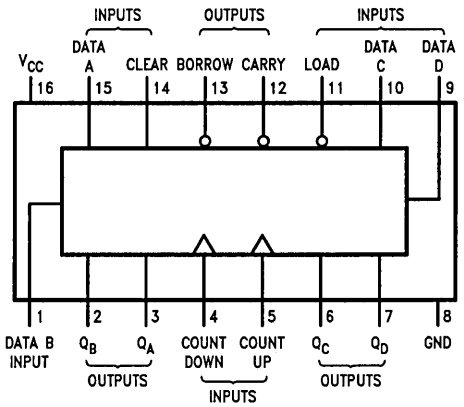
Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

Connection Diagram

Dual-In-Line Package



TL/F/6406–1

Order Number DM54LS193J, DM74LS193M or DM74LS193N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65° C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS193			DM74LS193			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
f_{CLK}	Clock Frequency (Note 1)	0		25	0		25	MHz
	Clock Frequency (Note 2)	0		20	0		20	MHz
t_W	Pulse Width of Any Input (Note 6)	20			20			ns
t_{SU}	Data Setup Time (Note 6)	20			20			ns
t_H	Data Hold Time (Note 6)	0			0			ns
t_{REL}	Release Time (Note 6)	40			40			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			19	34	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, I_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, I_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

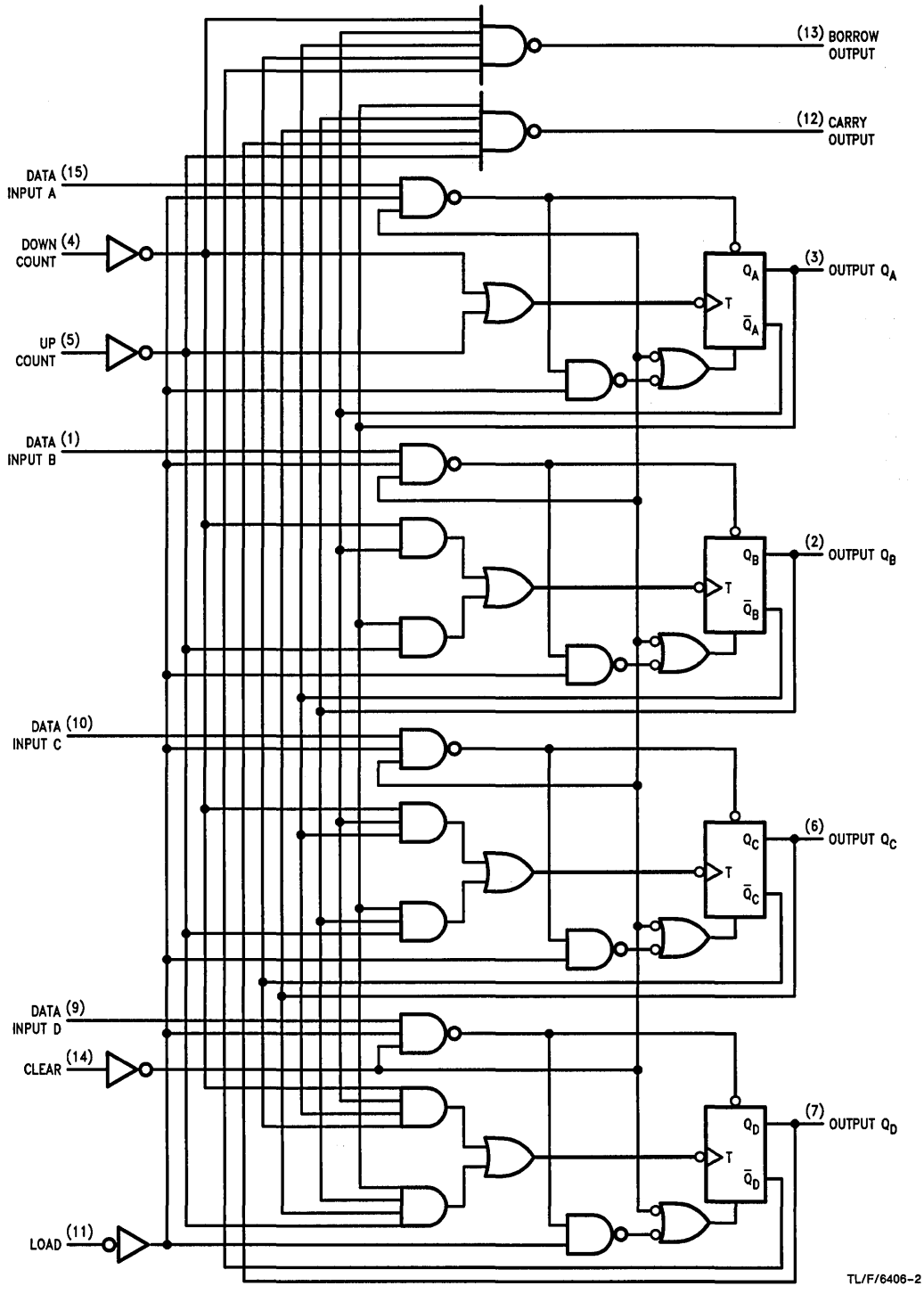
Note 5: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

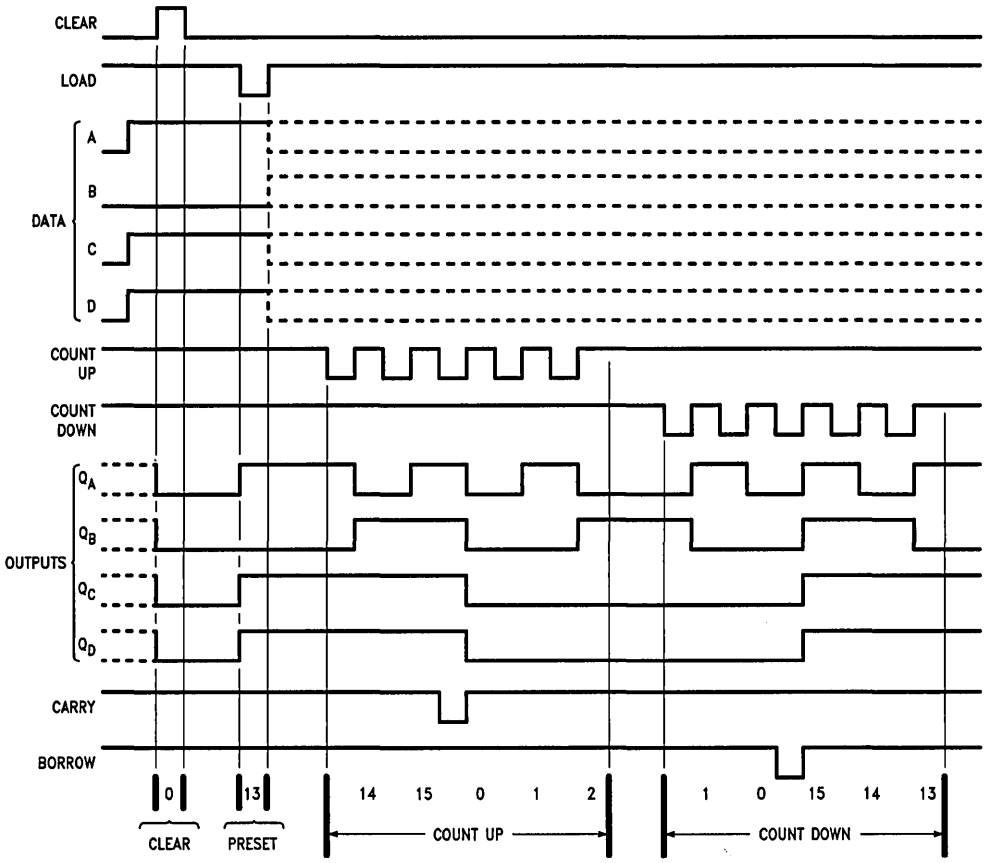
Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Up to Carry		26		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Up to Carry		24		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Down to Borrow		24		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Down to Borrow		24		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Either Count to Any Q		38		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Either Count to Any Q		47		54	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		40		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		40		47	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		35		44	ns

Logic Diagram



Timing Diagrams

Typical Clear, Load, and Count Sequences



TL/F/6406-3

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor Corporation

DM54LS194A/DM74LS194A 4-Bit Bidirectional Universal Shift Register

General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

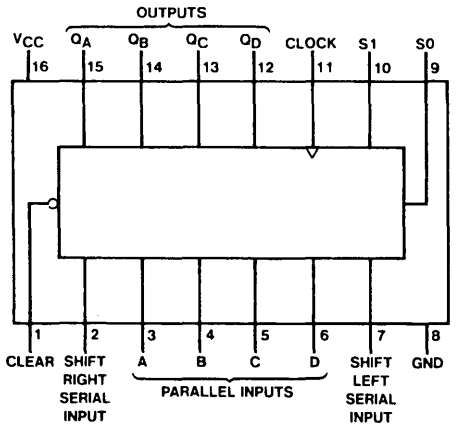
Clocking of the flip-flop is inhibited when both mode control inputs are low.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear

Connection Diagram

Dual-In-Line Package



TL/F/6407–1

Order Number DM54LS194AJ, DM74LS194AM or DM74LS194AN
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS194A			DM74LS194A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
	Clock Frequency (Note 2)		0		20	0		20	
t_W	Pulse Width (Note 3)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 3)	Mode	30			30			ns
		Data	20			20			
t_H	Hold Time (Note 3)		0			0			ns
t_{REL}	Clear Release Time (Note 3)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			15	23	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		22		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		22		35	ns
t_{PHL}	Propagation Delay Time High to Low Output	Clear to Any Q		30		38	ns

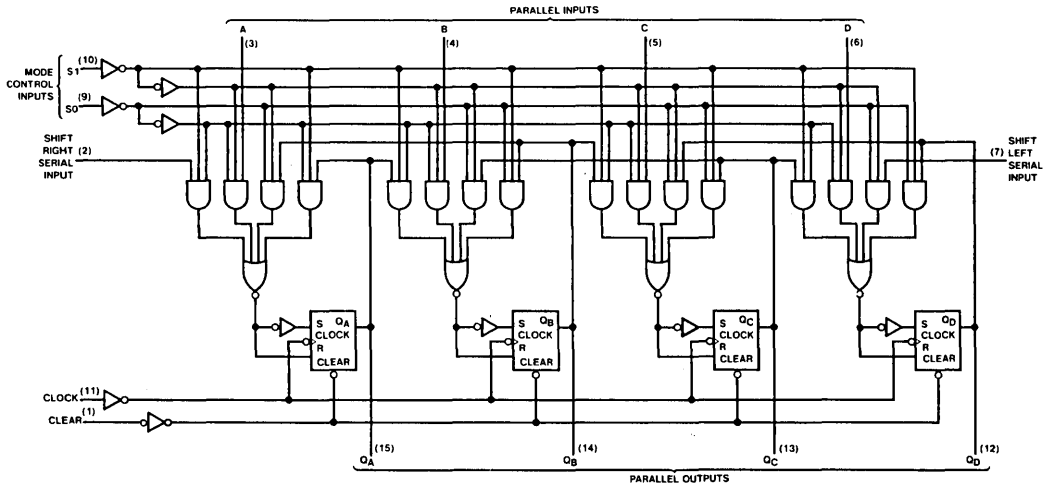
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the serial inputs, I_{CC} is tested with momentary ground, then 4.5V applied to CLOCK.

Logic Diagram

LS194A



TL/F/6407–2

Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

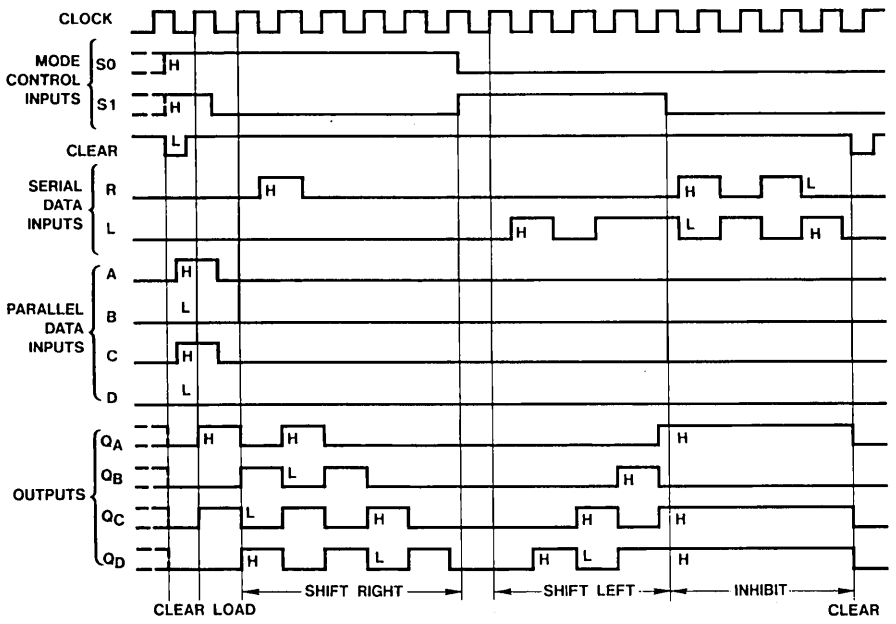
a, b, c, d = The level of steady state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most-recent ↑ transition of the clock.

Timing Diagram

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



TL/F/6407–3

National Semiconductor Corporation

DM54LS195A/DM74LS195A 4-Bit Parallel Access Shift Register

General Description

This 4-bit register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

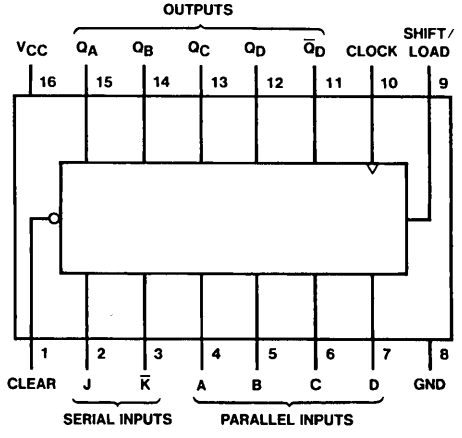
Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 39 MHz
- Typical power dissipation 70 mW

Connection Diagram

Dual-In-Line Package



TL/F/6408–1

Order Number DM54LS195AJ, DM74LS195AM or DM74LS195AN
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS195A			DM74LS195A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
	Clock Frequency (Note 2)		0		25	0		25	MHz
t_W	Pulse Width (Note 3)	Clock	16			16			ns
		Clear	12			12			
t_{SU}	Setup Time (Note 3)	Shift/Load	25			25			ns
		Data	15			15			
t_H	Hold Time (Note 3)		0			0			ns
t_{REL}	Shift/Load Release Time (Note 3)		10			10			ns
	Clear Release Time (Note 3)		25			25			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max, (Note 6)			14	21	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all inputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, then 4.5V to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		30		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		22		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		26		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		30		38	ns

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

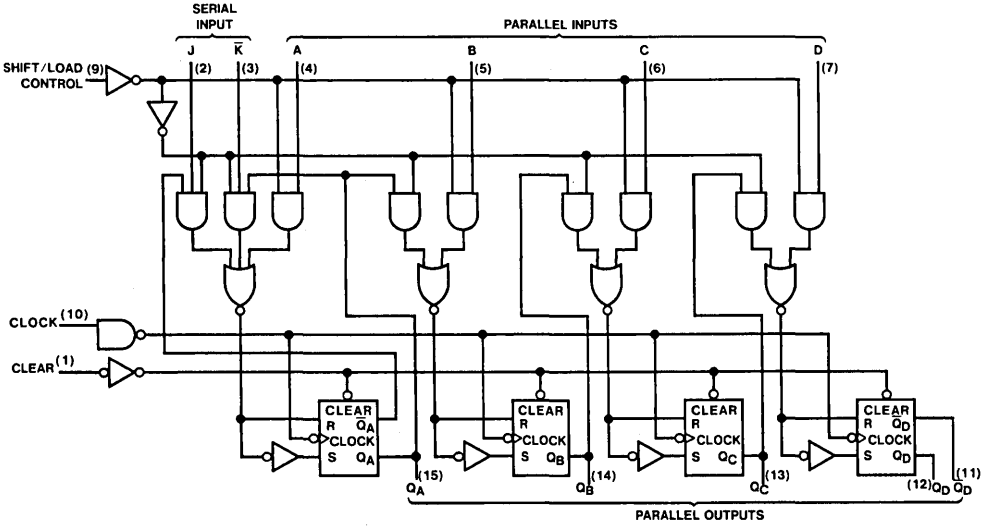
↑ = Transition from low to high level

a, b, c, d = The level of steady state input at A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

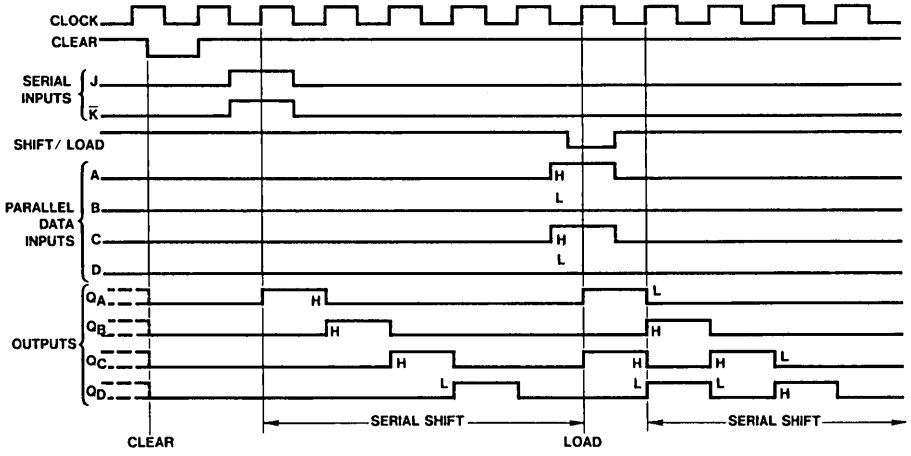
Logic Diagram



TL/F/6408–2

Timing Diagram

Typical Clear, Shift, and Load Sequences



TL/F/6408–3

National Semiconductor Corporation

DM54LS221/DM74LS221 Dual Non-Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM54/74LS221 is a dual monostable multivibrator with Schmitt-trigger input. Each device has three inputs permitting the choice of either leading-edge or trailing-edge triggering. Pin (A) is an active-low trigger transition input and pin (B) is an active-high transition Schmitt-trigger input that allows jitter free triggering for inputs with transition rates as slow as 1 volt/second. This provides the input with excellent noise immunity. Additionally an internal latching circuit at the input stage also provides a high immunity to V_{CC} noise. The clear (CLR) input can terminate the output pulse at a predetermined time independent of the timing components. This (CLR) input also serves as a trigger input when it is pulsed with a low level pulse transition (⌐⌙). To obtain the best and trouble free operation from this device please read operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

- A dual, highly stable one-shot
- Compensated for V_{CC} and temperature variations
- Pin-out identical to 'LS123 (Note 1)
- Output pulse width range from 30 ns to 70 seconds
- Hysteresis provided at (B) input for added noise immunity
- Direct reset terminates output pulse
- Triggerable from CLEAR input
- DTL, TTL compatible
- Input clamp diodes

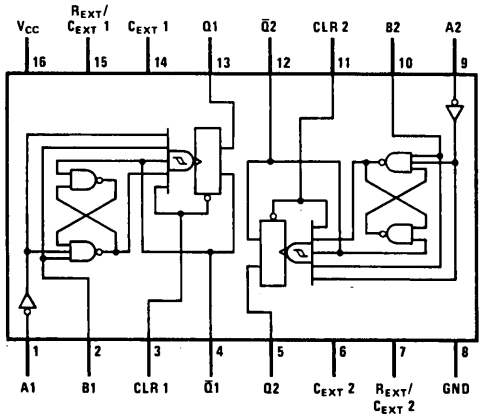
Note 1: The pin-out is identical to 'LS123 but, functionally it is not; refer to Operating Rules #10 in this datasheet.

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width is independent of further input transitions and is a function of the timing components, or it may be reduced or terminated by use of the active low CLEAR input. Stable output pulse width ranging from 30 ns to 70 seconds is readily obtainable.

Connection Diagram

Dual-In-Line Package



TL/F/6409–1

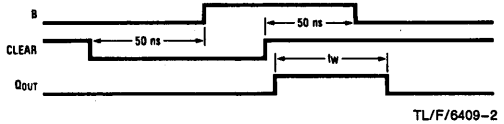
Order Number DM54LS221J, DM74LS221M or DM74LS221N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⌐⌙	⌙
H	↓	H	⌐⌙	⌙
* ↑	L	H	⌐⌙	⌙

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↑ = Negative Going Transition
⌐⌙ = A Positive Pulse
⌙ = A Negative Pulse

*This mode of triggering requires first the B input be set from a low to high level while the CLEAR input is maintained at logic low level. Then with the B input at logic high level, the CLEAR input whose positive transition from low to high will trigger an output pulse.



TL/F/6409–2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS221			DM74LS221			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage at the A Input (V_{CC} = Min)			1	2		1	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the A Input (V_{CC} = Min)		0.8	1		0.8	1		V
V_{T+}	Positive-Going Input Threshold Voltage at the B Input (V_{CC} = Min)			1	2		1	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the B Input (V_{CC} = Min)		0.8	0.9		0.8	0.9		V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width (Note 1)	Data	40			40			ns
		Clear	40			40			
t_{REL}	Clear Release Time (Note 1)		15			15			ns
$\frac{dV}{dt}$	Rate of Rise or Fall of Schmitt Input (B) (Note 1)				1			1	$\frac{V}{s}$
$\frac{dV}{dt}$	Rate of Rise or Fall of Logic Input (A) (Note 1)				1			1	$\frac{V}{\mu s}$
R_{EXT}	External Timing Resistor (Note 1)		1.4		70	1.4		100	kΩ
C_{EXT}	External Timing Capacitance (Note 1)		0		1000	0		1000	μF
DC	Duty Cycle (Note 1)	R_T = 2 kΩ			50			50	%
		$R_T = R_{EXT}$ (Max)			90			60	
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		V_{CC} = Min, I_{OL} = 4 mA	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A1, A2			−0.4	mA
			B			−0.8	
			Clear			−0.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		4.7	11	mA
			Triggered		19	27	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A1, A2 to Q	C_{EXT} = 80 pF, R_{EXT} = 2 kΩ, C_L = 15 pF, R_L = 2 kΩ		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q			55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A1, A2 to Q			80	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$			65	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$			65	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q			55	ns
$t_{W(out)}$	Output Pulse Width Using Zero Timing Capacitance	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 0, R_{EXT} = 2 kΩ, R_L = 2 kΩ, C_L = 15 pF	20	70	ns
$t_{W(out)}$	Output Pulse Width Using External Timing Resistor	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 100 pF, R_{EXT} = 10 kΩ, R_L = 2 kΩ, C_L = 15 pF	600	750	ns
			C_{EXT} = 1 μF, R_{EXT} = 10 kΩ, R_L = 2 kΩ, C_L = 15 pF	6	7.5	ms
			C_{EXT} = 80 pF, R_{EXT} = 2 kΩ, R_L = 2 kΩ, C_L = 15 pF	70	150	ns

Operating Rules

1. An external resistor (R_X) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to approximately 1000 μF. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitor may be used. For large time constants use tantalum or special aluminum capacitors. If timing capacitor has leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current. This switching diode is not needed for the 'LS221 one-shot and should not be used.
3. For $C_X >> 1000$ pF, the output pulse width (T_W) is defined as follows:

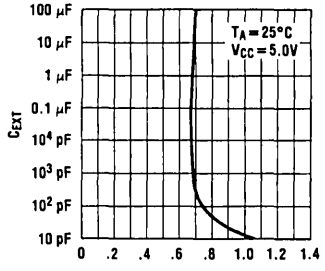
   $T_W = KR_X C_X$

   where $[R_X$ is in kΩ$]$

   $[C_X$ is in pF$]$

   $[T_W$ is in ns$]$

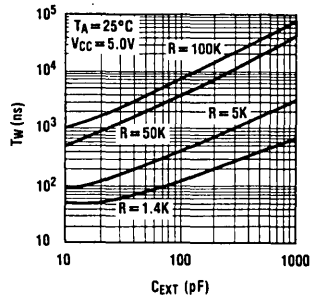
   $K \approx Ln2 = 0.70$
4. The multiplicative factor K is plotted as a function of C_X below for design considerations:



TL/F/6409-3

FIGURE 1

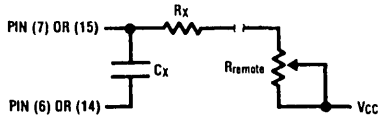
5. For $C_X < 1000$ pF see *Figure 2* for T_W vs C_X family curves with R_X as a parameter:



TL/F/6409-4

FIGURE 2

6. To obtain variable pulse widths by remote trimming, the following circuit is recommended:

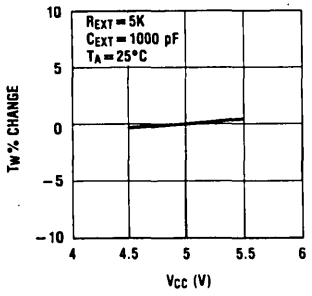


TL/F/6409-5

Note: "R_{remote}" should be as close to the one-shot as possible.

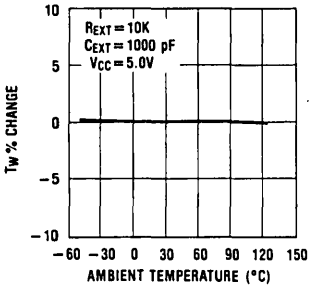
FIGURE 3

7. Output pulse width versus V_{CC} and temperatures: *Figure 4* depicts the relationship between pulse width variation versus V_{CC}. *Figure 5* depicts pulse width variation versus temperatures.



TL/F/6409-6

FIGURE 4



TL/F/6409-7

FIGURE 5

8. Duty cycle is defined as $T_W/T \times 100$ in percentage, if it goes above 50% the output pulse width will become shorter. If the duty cycle varies between low and high values, this causes output pulse width to vary, or jitter (a function of the R_{EXT} only). To reduce jitter , R_{EXT} should be as large as possible, for example, with $R_{EXT} = 100k$ jitter is not appreciable until the duty cycle approaches 90%.

Operating Rules (Continued)

9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I-R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
10. Although the 'LS221's pin-out is identical to the 'LS123 it should be remembered that they are not functionally identical. The 'LS123 is a retriggerable device such that the output is dependent upon the input transitions when its output "Q" is at the "High" state. Furthermore, it is recommended for the 'LS123 to externally ground the C_{EXT} pin for improved system performance. However, this pin on the 'LS221 is not an internal connection to the device ground. Hence, if substitution of an 'LS221 onto an 'LS123 design layout where the C_{EXT} pin is wired to the ground, the device will not function.
11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC}-pin as space permits.

For further detailed device characteristics and output performance, please refer to the NSC one-shot application note AN-366.

National Semiconductor Corporation

DM54LS240/DM74LS240, DM54LS241/DM74LS241 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

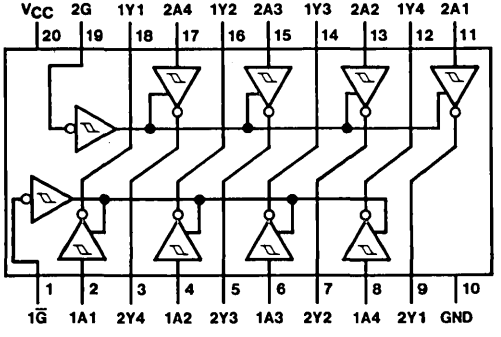
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- Typical I_{OH} (source current)
  - 54LS −12 mA
  - 74LS −15 mA
- Typical propagation delay times
  - Inverting 10.5 ns
  - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  - Inverting 130 mW
  - Noninverting 135 mW

Connection Diagrams

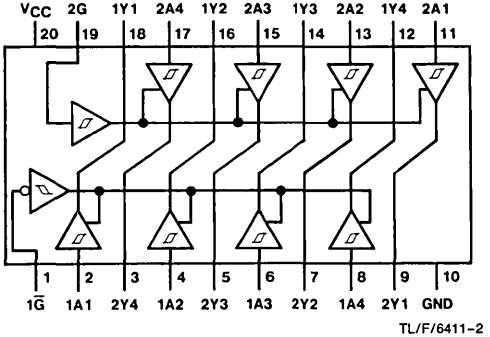
Dual-In-Line Package



TL/F/6411–1

Order Number DM54LS240J, DM74LS240WM or DM74LS240N
See NS Package Number J20A, M20B or N20A

Dual-In-Line Package



TL/F/6411–2

Order Number DM54LS241J, DM74LS241WM or DM74LS241N
See NS Package Number J20A, M20B or N20A

Function Tables

LS240

Inputs		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Z

LS241

Inputs				Outputs	
G	$\overline{G}$	1A	2A	1Y	2Y
X	L	L	X	L	
X	L	H	X	H	
X	H	X	X	Z	
H	X	X	L		L
H	X	X	H		H
L	X	X	X		Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS240, 241			DM74LS240, 241			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High	LS240, LS241		13	23	mA
			Outputs Low	LS240		26	44	
				LS241		27	46	
			Outputs Disabled	LS240		29	50	
				LS241		32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions		Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF, R_L = 667Ω	LS240	3	14	ns
			LS241	5	18	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF, R_L = 667Ω	LS240	5	18	ns
			LS241	7	18	
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF, R_L = 667Ω	LS240	10	30	ns
			LS241	10	30	
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF, R_L = 667Ω	LS240	5	23	ns
			LS241	10	23	
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF, R_L = 667Ω	LS240	7	25	ns
			LS241	8	25	
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 667Ω	LS240	5	18	ns
			LS241	5	18	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF, R_L = 667Ω	LS240	5	18	ns
			LS241	6	21	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF, R_L = 667Ω	LS240	6	22	ns
			LS241	6	22	
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF, R_L = 667Ω	LS240	12	33	ns
			LS241	12	33	
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF, R_L = 667Ω	LS240	6	26	ns
			LS241	11	26	

National Semiconductor Corporation

DM54LS243/DM74LS243 Quadruple Bus Transceiver

General Description

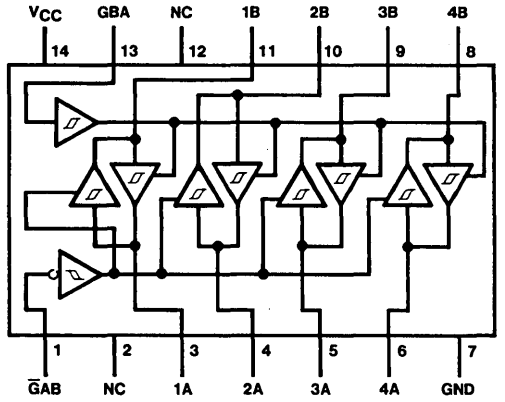
This four data line transceiver is designed for asynchronous two-way communications between data buses. It can be used to drive terminated lines down to 133Ω.

Features

- Two-way asynchronous communication between data buses
- P-N-P inputs reduce D-C loading
- Hysteresis (typically 400 mV) at inputs improves noise margin

Connection Diagram

Dual-In-Line Package



TL/F/6412–1

Order Number DM54LS243J, DM74LS243WM or DM74LS243N
See NS Package Number J14A, M14B or N14A

Function Table

Control Inputs		Data Port Status	
$\overline{G}AB$	GBA	A	B
H	H	O	I
L	H	*	*
H	L	ISOLATED	
L	L	I	O

*Possibly destructive oscillation may occur if the transceivers are enabled in both directions at once.

I = Input, O = Output.

H = High Logic Level, L = Low Logic Level.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	
Any G	7V
A or B	5.5V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS243			DM74LS243			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = −3 m		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min, V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = Max, V_{IH} = Min	V_O = 2.7V				40	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 5.5V	A or B			0.1	mA
			V_I = 7V	Any G			0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High			22	38	mA
			Outputs Low			29	50	
			Outputs Disabled			32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 667Ω	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF R_L = 667Ω	7	18	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF R_L = 667Ω	10	30	ns
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF R_L = 667Ω	10	23	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF R_L = 667Ω	8	25	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF R_L = 667Ω	5	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF R_L = 667Ω	6	21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF R_L = 667Ω	6	22	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF R_L = 667Ω	12	33	ns
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF R_L = 667Ω	11	26	ns

National Semiconductor Corporation

DM54LS244/DM74LS244 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

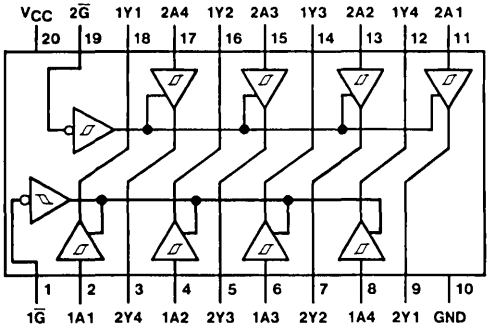
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- Typical I_{OH} (source current)
  - 54LS −12 mA
  - 74LS −15 mA
- Typical propagation delay times
  - Inverting 10.5 ns
  - Noninverting 12 ns
- Typical enable/disable time 18 ns
- Typical power dissipation (enabled)
  - Inverting 130 mW
  - Noninverting 135 mW

Connection Diagram

Dual-In-Line Package



TL/F/8442–1

Order Number DM54LS244J, DM74LS244WM or DM74LS244N
See NS Package Number J20A, M20B or N20A

Function Table

Inputs		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Z

L = Low Logic Level
H = High Logic Level
X = Either Low or High Logic Level
Z = High Impedance

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS244			DM74LS244			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−20	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max	V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.4V				−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	V_{CC} = Max, Outputs Open	Outputs High			13	23	mA
			Outputs Low			27	46	
			Outputs Disabled			32	54	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 667Ω	5	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF R_L = 667Ω	7	18	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF R_L = 667Ω	10	30	ns
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF R_L = 667Ω	10	23	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF R_L = 667Ω	8	25	ns
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF R_L = 667Ω	5	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF R_L = 667Ω	6	21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF R_L = 667Ω	6	22	ns
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF R_L = 667Ω	12	33	ns
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF R_L = 667Ω	11	26	ns

National Semiconductor Corporation

DM54LS245/DM74LS245 TRI-STATE® Octal Bus Transceiver

General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

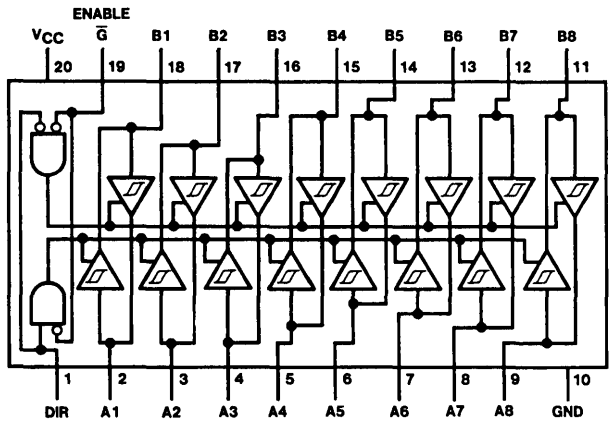
The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

- Bi-Directional bus transceiver in a high-density 20-pin package
- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at bus inputs improve noise margins
- Typical propagation delay times, port-to-port 8 ns
- Typical enable/disable times 17 ns
- I_{OL} (sink current)
  - 54LS 12 mA
  - 74LS 24 mA
- I_{OH} (source current)
  - 54LS −12 mA
  - 74LS −15 mA

Connection Diagram

Dual-In-Line Package



TL/F/6413–1

Order Number DM54LS245J, DM74LS245WM or DM74LS245N
See NS Package Number J20A, M20B or N20A

Function Table

Enable $\overline{G}$	Direction Control DIR	Operation
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High Level, L = Low Level, X = Irrelevant

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	
DIR or $\overline{G}$	7V
A or B	5.5V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS245			DM74LS245			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
HYS	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min			0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = Min V_{IL} = Max, I_{OH} = −1 mA		DM74	2.7			V
		V_{CC} = Min, V_{IL} = Min V_{IL} = Max, I_{OH} = −3 mA		DM54/DM74	2.4	3.4		
		V_{CC} = Min, V_{IH} = Min V_{IL} = 0.5V, I_{OH} = Max		DM54/DM74	2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min V_{IL} = Max V_{IH} = Min	I_{OL} = 12 mA	DM74			0.4	V
			I_{OL} = Max	DM54			0.4	
				DM74			0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = Max V_{IH} = Min	V_O = 2.7V				20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.4V				−200	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	A or B	V_I = 5.5V			0.1	mA
			DIR or $\overline{G}$	V_I = 7V			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V					−0.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)			−40		−225	mA
I_{CC}	Supply Current	Outputs High		V_{CC} = Max		48	70	mA
		Outputs Low				62	90	
		Outputs at Hi-Z				64	95	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, not to exceed one second duration

Switching Characteristics V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	DM54/74 LS245		Units
			Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 45 pF, R_L = 667Ω		12	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			12	ns
t_{PZL}	Output Enable Time to Low Level			40	ns
t_{PZH}	Output Enable Time to High Level			40	ns
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF, R_L = 667Ω		25	ns
t_{PHZ}	Output Disable Time from High Level			25	ns
t_{PLH}	Propagation Delay Time, Low-to-High-Level Output	C_L = 150 pF, R_L = 667Ω		16	ns
t_{PHL}	Propagation Delay Time, High-to-Low-Level Output			17	ns
t_{PZL}	Output Enable Time to Low Level			45	ns
t_{PZH}	Output Enable Time to High Level			45	ns

National Semiconductor Corporation

DM54LS251/DM74LS251 TRI-STATE® Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

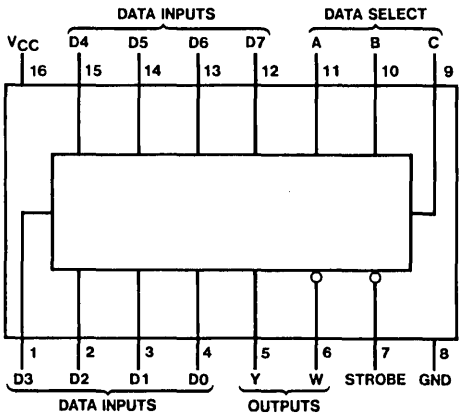
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE version of LS151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Maximum number of common outputs
  54LS 49
  74LS 129
- Typical propagation delay time (D to Y)
  54LS 17 ns
  74LS 17 ns
- Typical power dissipation
  54LS 35 mW
  74LS 35 mW

Connection Diagram

Dual-In-Line Package



TL/F/6415–1

Order Number DM54LS251J, DM74LS251M or DM74LS251N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level,
X = Don't Care, Z = High Impedance (Off)
D0, D1 ... D7 = The level of the respective D input

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS251			DM74LS251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			6.1	10	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			7.1	12	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with the outputs open, STROBE grounded, and all other inputs at 4.5V.

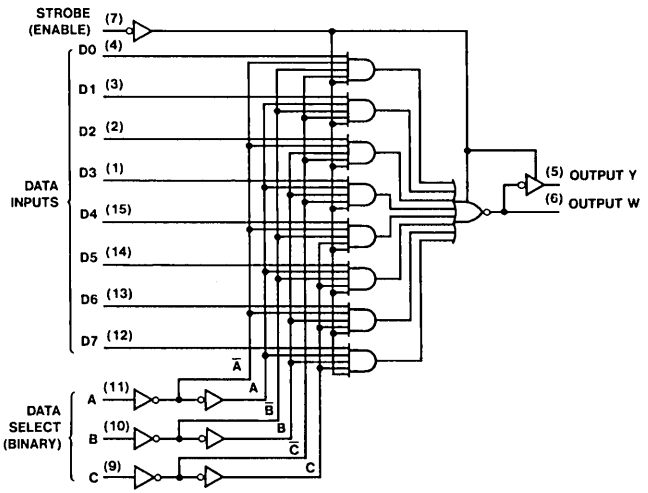
Note 4: I_{CC2} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C (4 Levels) to Y		45		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C (4 Levels) to Y		45		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C (3 Levels) to W		33		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C (3 Levels) to W		33		42	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Y		28		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Y		28		38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to W		15		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to W		15		25	ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to Y		45		60	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to Y		40		51	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Strobe to Y		45			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Strobe to Y		25			ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to W		27		40	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to W		40		47	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Strobe to W		55			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Strobe to W		25			ns

Note 1: C_L = 5 pF

Logic Diagram



TL/F/6415–2

National Semiconductor Corporation

DM54LS253/DM74LS253 TRI-STATE® Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

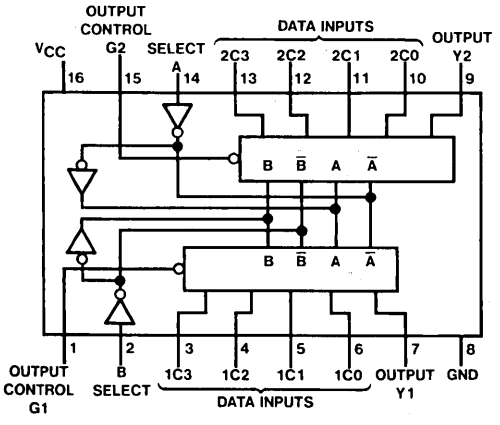
The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level.

Features

- TRI-STATE version of LS153 with same pinout
- Schottky-diode-clamped transistors
- Permit multiplexing from N-lines to one line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fanout totem-pole outputs
- Typical propagation delay
  - Data to output 12 ns
  - Select to output 21 ns
- Typical power dissipation 35 mW

Connection Diagram

Dual-In-Line Package



TL/F/6416–1

Order Number DM54LS253J, DM74LS253M or DM74LS253N
See NS Package Number J16A, M16A or N16A

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address Inputs A and B are common to both sections.
H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (off).

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS253			DM74LS253			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54			0.4	V
			DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			7	12	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			8.5	14	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, and all the inputs grounded.

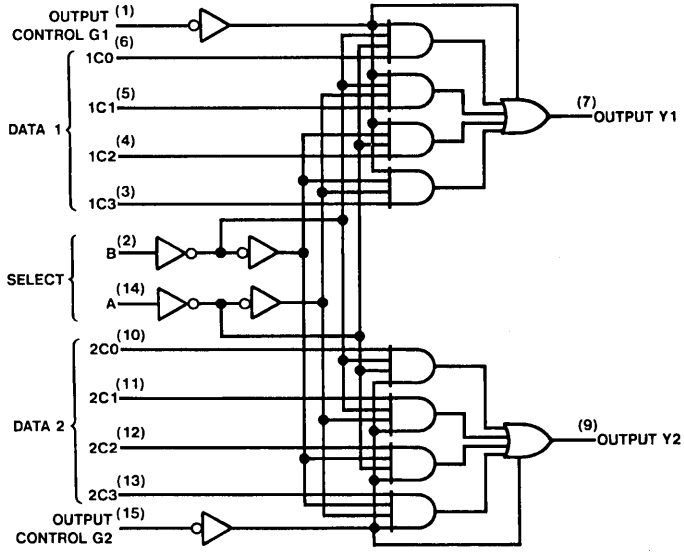
Note 4: I_{CC2} is measured with the outputs open, OUTPUT CONTROL at 4.5V and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		25		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		45		54	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		32		44	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		18		32	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		23		35	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Output Control to Y		41			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Output Control to Y		27			ns

Note 1: C_L = 5 pF.

Logic Diagram



TL/F/6416–2

National Semiconductor Corporation

DM54LS257B/DM74LS257B, DM54LS258B/DM74LS258B TRI-STATE® Quad 2-Data Selectors/Multiplexers

General Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

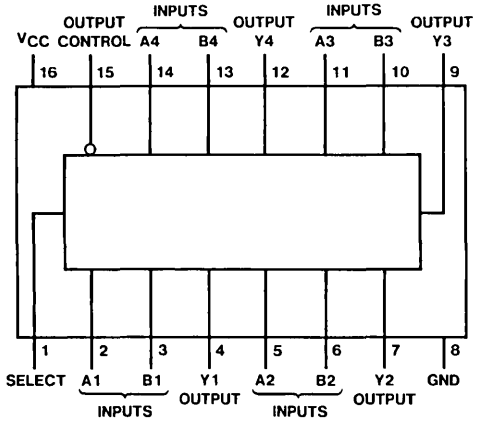
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- TRI-STATE versions LS157 and LS158 with same pinouts
- Schottky-clamped for significant improvement in A-C performance
- Provides bus interface from multiple sources in high-performance systems
- Average propagation delay from data input 12 ns
- Typical power dissipation
  LS257B 50 mW
  LS258B 35 mW

Connection Diagrams

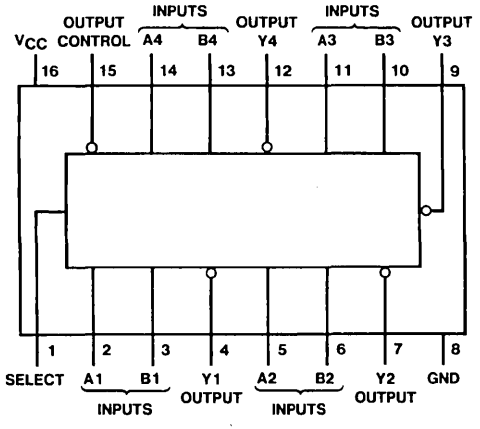
Dual-In-Line Package



TL/F/6417–1

Order Number DM54LS257BJ, DM74LS257BM or DM74LS257BN
See NS Package Number J16A, M16A or N16A

Dual-In-Line Package



TL/F/6417–2

Order Number DM54LS258BJ, DM74LS258BM or DM74LS258BN
See NS Package Number J16A, M16A or N16A

Function Table

Inputs				Output Y	
Output Control	Select	A	B	LS257	LS258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care,
Z = High Impedance (off)

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS257B			DM74LS257B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS257B Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Select			0.2	mA
			Other			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			40	μA
			Other			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Select			−0.8	mA
			Other			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			5.9	10	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			9.2	16	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			12	19	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'LS257B Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		28		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		35		42	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		15		27	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		28		38	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Output Control to Y		26			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Output Control to Y		25			ns

Note 1: C_L = 5 pF.

Recommended Operating Conditions

Symbol	Parameter	DM54LS258B			DM74LS258B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS258B Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Select			0.2	mA
			Other			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			40	μA
			Other			20	

'LS258B Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Select			−0.8	mA
			Other			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			4.1	7	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			9	14	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			12	19	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'LS258B Switching Characteristics

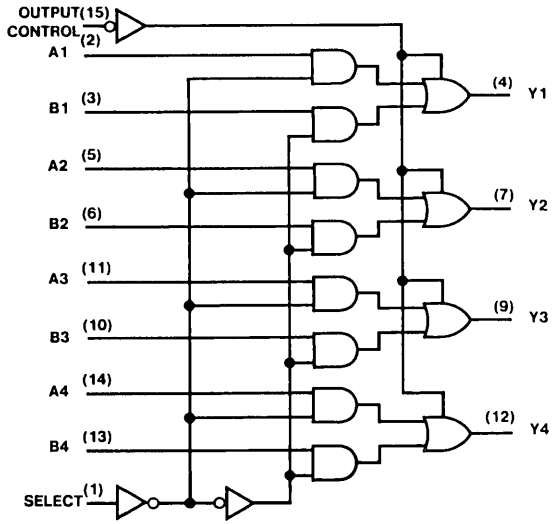
at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		18		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		28		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		35		42	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		15		27	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		28		38	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 4)	Output Control to Y		26			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 4)	Output Control to Y		25			ns

Note 4: C_L = 5 pF.

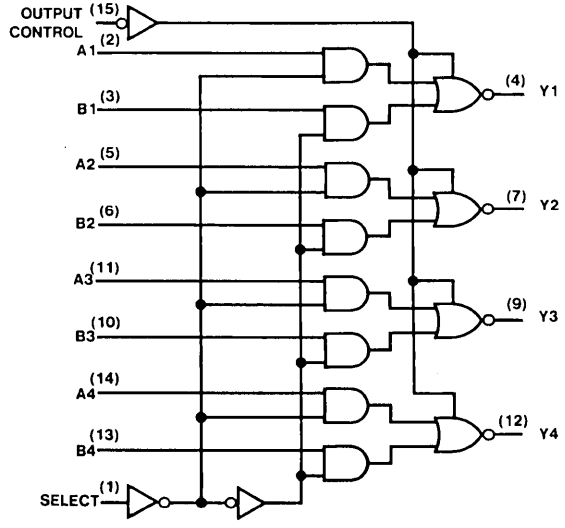
Logic Diagrams

LS257B



TL/F/6417–3

LS258



TL/F/6417–4

2

National Semiconductor Corporation

DM54LS259/DM74LS259 8-Bit Addressable Latches

General Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

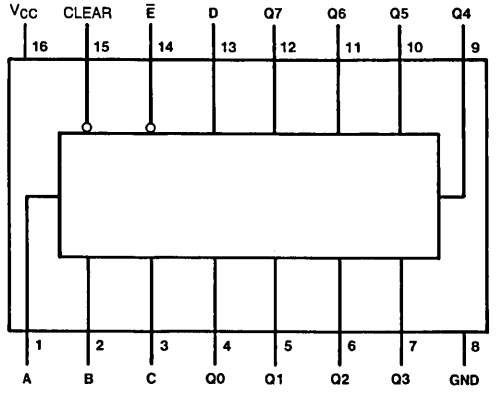
Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Features

- 8-Bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/disable input simplifies expansion
- Direct replacement for Fairchild 9334
- Expandable for N-bit applications
- Four distinct functional modes
- Typical propagation delay times:
  - Enable-to-output 18 ns
  - Data-to-output 16 ns
  - Address-to-output 21 ns
  - Clear-to-output 17 ns
- Fan-out
  - I_{OL} (sink current)
    - 54LS259 4 mA
    - 74LS259 8 mA
  - I_{OH} (source current) −0.4 mA
- Typical I_{CC} 22 mA

Connection Diagram

Dual-In-Line Package



TL/F/6418–1

Order Number DM54LS259J, DM74LS259WM or DM74LS259N
See NS Package Number J16A, M16B or N16A

Function Table

Inputs		Output of Addressed Latch	Each Other Output	Function
Clear	Ē			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = High Level, L = Low Level

D = the Level of the Data Input

Q_{i0} = the Level of Q_i (i = 0, 1, ... 7, as Appropriate) before the Indicated Steady-State Input Conditions Were Established.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS259			DM74LS259			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
t_W	Pulse Width (Note 7)	Enable	15			15			ns
		Clear	15			15			
t_{SU}	Setup Time (Notes 1, 2, 3 & 7)	Data	15 ↑			15 ↑			ns
		Select	15 ↓			15 ↓			
t_H	Hold Time (Notes 1, 2 & 7)	Data	0 ↑			0 ↑			ns
		Select	0 ↑			0 ↑			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			22	36	mA

Note 1: The symbols (↓, ↑) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: Setup and hold times are with reference to the enable input.

Note 3: The select-to-enable setup time is the time before the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: I_{CC} is measured with all inputs at 4.5V, and all outputs open.

Note 7: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		35		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		24		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		32		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		21		30	ns
t_{PHL}	Propagation Delay Time Low to High Level Output	Select to Output		38		41	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		29		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		27		36	ns

National Semiconductor Corporation

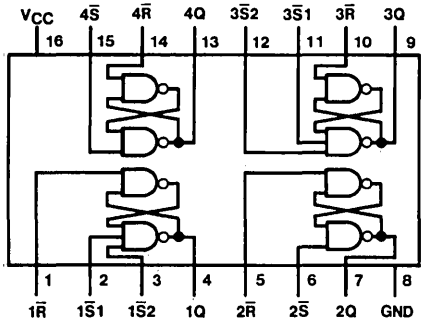
DM54LS279/DM74LS279 Quad $\overline{S}$-$\overline{R}$ Latches

General Description

This device consists of four individual and independent Set-Reset Latches with active low inputs. Two of the four latches have an additonal $\overline{S}$ input ANDed with the primary $\overline{S}$ input. A low on any $\overline{S}$ input while the $\overline{R}$ input is high will be stored in the latch and appear on the corresponding Q output as a high. A low on the $\overline{R}$ input while the $\overline{S}$ input is high will clear the Q output to a low. Simultaneous transistion of the $\overline{R}$ and $\overline{S}$ inputs from low to high will cause the Q output to be indeterminate. Both inputs are voltage level triggered and are not affected by transition time of the input data.

Connection Diagram

Dual-In-Line Package



TL/F/6420–1

Order Number DM54LS279J, DM74LS279M or DM74LS279N
See NS Package Number J16A, M16A or N16A

Function Table

Inputs		Output
$\overline{S}$(1)	$\overline{R}$	Q
L	L	H*
L	H	H
H	L	L
H	H	Q_0

H = High Level

L = Low Level

Q_0 = The Level of Q before the indicated input conditions were established.

*This output level is pseudo stable; that is, it may not persist when the $\overline{S}$ and $\overline{R}$ inputs return to their inactive (high) level.

Note 1: For latches with double $\overline{S}$ inputs:

H = both $\overline{S}$ inputs high

L = one or both $\overline{S}$ inputs low

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS279			DM74LS279			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max	DM54	2.5	3.5		V
		V_{IL} = Max, V_{IH} = Min	DM74	2.7	3.5		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			3.8	7	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all $\overline{R}$ inputs grounded, all $\overline{S}$ inputs at 4.5V and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	$\overline{S}$ to Q		22		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{S}$ to Q		15		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	$\overline{R}$ to Q		27		33	ns

National Semiconductor Corporation

DM54LS283/DM74LS283 4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

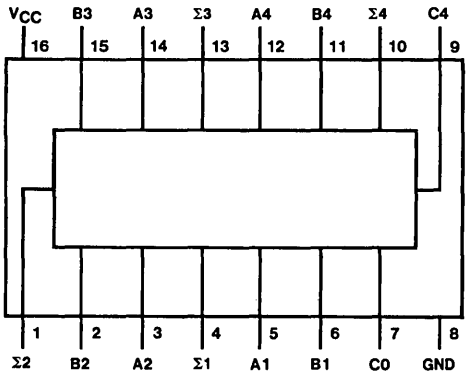
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  - Two 8-bit words 25 ns
  - Two 16-bit words 45 ns
- Typical power dissipation per 4-bit adder 95 mW

Connection Diagram

Dual-In-Line Package



TL/F/6421–1

Order Number DM54LS283J, DM74LS283M or DM74LS283N
See NS Package Number J16A, M16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS283			DM74LS283			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	A, B			0.2	mA
			C0			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A, B			40	μA
			C0			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A, B			−0.8	mA
			C0			−0.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			19	34	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			22	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V, or all inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ1, Σ2		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ1, Σ2		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ3		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ3		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ4		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ4		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to Σ_i		24		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to Σ_i		24		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to C4		17		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to C4		17		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to C4		17		26	ns

Function Table

Input				Outputs					
				When C0 = L			When C0 = H		
						When C2 = L			When C2 = H
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

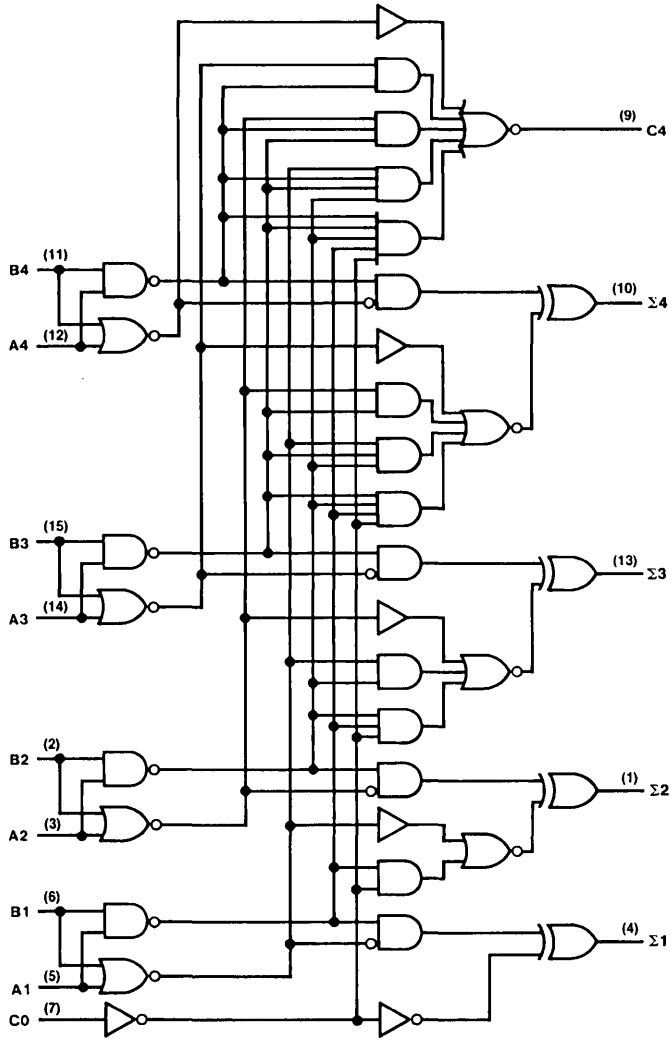
TL/F/6421–3

H = High Level, L = Low Level

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Logic Diagram

LS283



TL/F/6421–2

National Semiconductor Corporation

DM54LS290/DM74LS290 4-Bit Decade Counter

General Description

The DM54LS290/DM74LS290 counter is electrically and functionally identical to the DM54LS90/DM74LS90. Only the arrangement of the terminals has been changed for the 'LS290.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five.

This counter has a gated zero reset and gated set-to-nine inputs for use in BCD nine's complement applications.

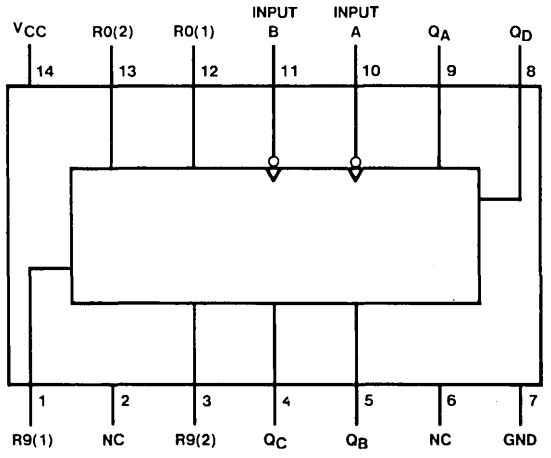
To use the maximum count length (decade) of this counter, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table. A symmetrical divide-by-ten count can be obtained from the 'LS290 counter by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- GND and V_{CC} on Corner Pins (Pins 7 and 14 respectively)
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6422–1

Order Number DM54LS290J, DM74LS290M or DM74LS290N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS290			DM74LS290			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Freq. (Note 1)	A to Q_A	0		32	0		32	MHz
		B to Q_B	0		16	0		16	
f_{CLK}	Clock Freq. (Note 2)	A to Q_A	0		20	0		20	MHz
		B to Q_B	0		10	0		10	
t_W	Pulse Width (Note 6)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time (Note 6)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
			A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	µA
			A			40	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			9	15	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50		68	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40		53	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		53	ns

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 6: T_A = 25°C and V_{CC} 5V.

Function Tables

BCD Count Sequence (See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Note A: Output Q_A is connected to input B for BCD count

H = High Logic Level

L = Low Logic Level

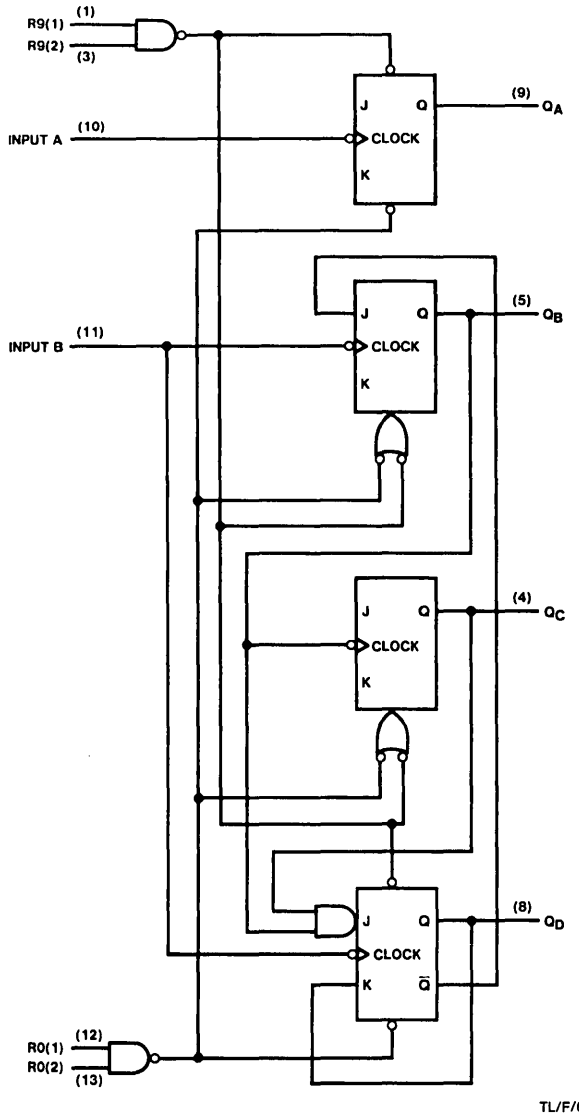
X = Either Low or High Logic Level

Bi-Quinary (5-2) (See Note B)

Count	Output			
	Q_A	Q_B	Q_C	Q_D
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note B: Output Q_D is connected to input A for bi-quinary count.

Logic Diagram



TL/F/6422-2

Reset/Count Truth Table

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

2

National Semiconductor Corporation

DM54LS293/DM74LS293 4-Bit Binary Counter

General Description

The DM54LS293/DM74LS293 counter is electrically and functionally identical to the DM54LS93/DM74LS93. Only the arrangement of the terminals has been changed for the 'LS293.

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

All of these counters have a gated zero reset.

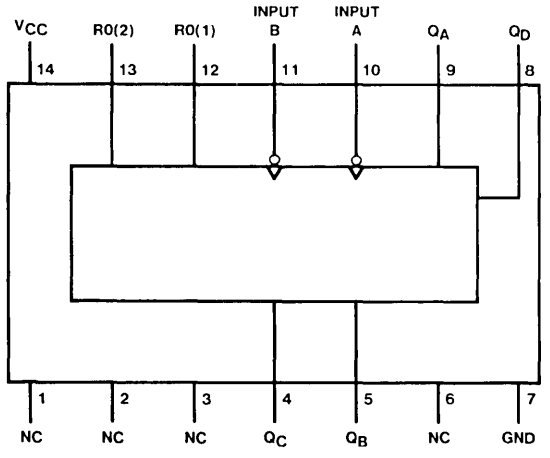
To use the maximum count length (four-bit binary) of these counters, the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate function table.

Features

- GND and V_{CC} on Corner Pins (Pins 7 and 14 respectively)
- Typical power dissipation 45 mW
- Count frequency 42 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6423–1

Order Number DM54LS293J, DM74LS293M or DM74LS293N
See NS Package Number J14A, M14A or N14A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS293			DM74LS293			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		32	0		32	MHz
		B to Q_B	0		16	0		16	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	0		20	MHz
		B to Q_B	0		10	0		10	
t_W	Pulse Width (Note 6)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time (Note 6)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Reset			0.1	mA
			A			0.2	
			B			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Reset			20	μA
			A			40	
			B			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Reset			−0.4	mA
			A			−2.4	
			B			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			9	15	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{MAX}	Maximum Clock Frequency	A to Q_A	32		20		MHz
		B to Q_B	16		10		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70		87	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70		93	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35		53	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51		71	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51		71	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40		53	ns

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 5: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 6: T_A = 25°C and V_{CC} = 5V.

Function Tables

Count Sequence (See Note C)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

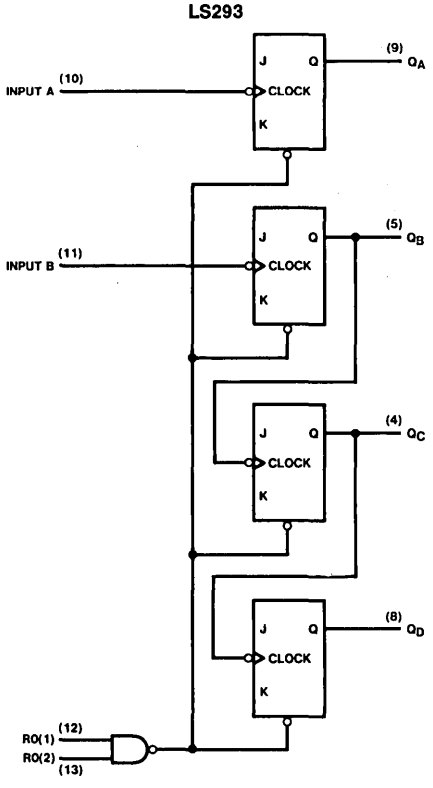
Note C: Output Q_A is connected to input B.

Reset/Count Truth Table

Reset Inputs		Outputs			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

H = High Level, L = Low Level, X = Don't Care.

Logic Diagram



TL/F/6423–2

Note: The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor Corporation

DM54LS352/DM74LS352 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

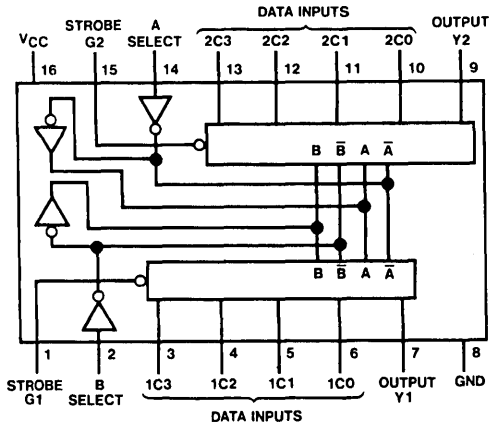
Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

- Inverting version of DM54/74LS153
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times
  - From data 15 ns
  - From strobe 19 ns
  - From select 22 ns
- Typical power dissipation 31 mW

Connection Diagram

Dual-In-Line Package



TL/F/6425–1

Order Number DM54LS352J, DM74LS352M or DM74S352N
See NS Package Number J16A, M16A or N16A

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	H
L	L	L	X	X	X	L	H
L	L	H	X	X	X	L	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	L	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	L	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	L	L

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55° C to +125°C
DM74LS	0° C to +70°C
Storage Temperature Range	−65° C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS352			DM74LS352			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			6.2	10	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

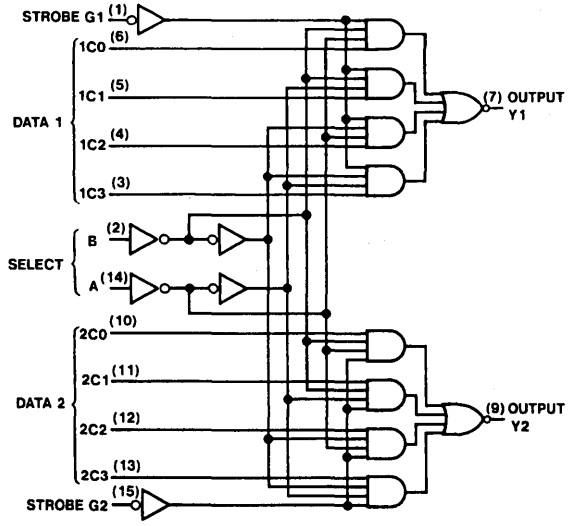
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all other inputs at ground.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		26		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		29		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		38		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		24		29	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		32		41	ns

Logic Diagram



TL/F/6425–2

National Semiconductor Corporation

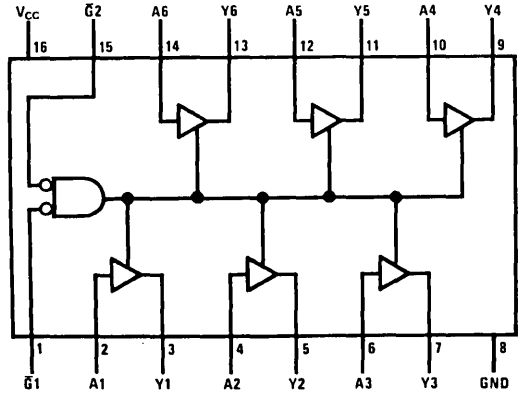
DM54LS365A/DM74LS365A Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6427–1

Order Number DM54LS365AJ, DM74LS365AM or DM74LS365AN
See NS Package Number J16A, M16A or N16A

Function Table

$Y = A$

Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	H
L	L	L	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS365A			DM74LS365A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max, V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			14	24	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		16		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		16		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		40	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)		20			ns

Note 6: C_L = 5 pF.

National Semiconductor Corporation

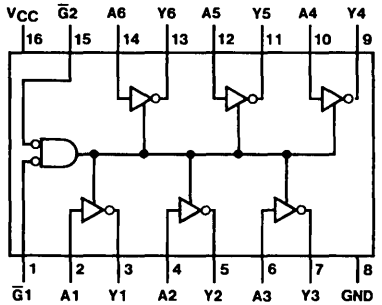
DM54LS366A/DM74LS366A Hex TRI-STATE® Inverting Buffers

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6428–1

Order Number DM54LS366AJ, DM74LS366AM or DM74LS366AN
See NS Package Number J16A, M16A or N16A

Function Table

$Y = \overline{A}$

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	L	H
L	L	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS366A			DM74LS366A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max, V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			12	21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		16		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		35	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)		20			ns

Note 6: C_L = 5pF.

National Semiconductor Corporation

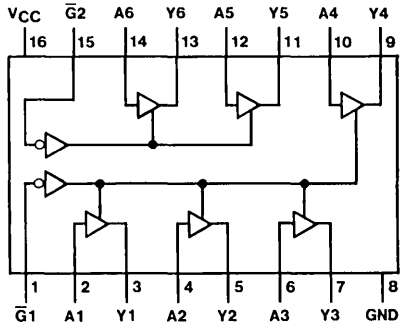
DM54LS367A/DM74LS367A Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6429–1

Order Number DM54LS367AJ, DM74LS367AM or DM74LS367AN
See NS Package Number J16A, M16A or N16A

Function Table

$Y = A$

Inputs		Output
A	$\overline{G}$	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS367A			DM74LS367A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max, V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			14	24	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		16		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		16		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		40	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)		20			ns

Note 6: C_L = 5pF.

National Semiconductor Corporation

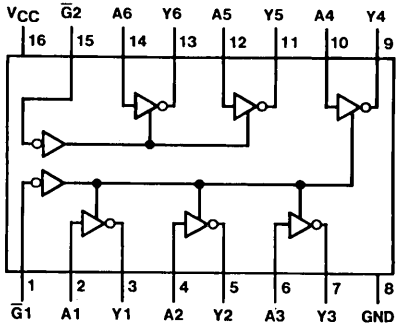
DM54LS368A/DM74LS368A Hex TRI-STATE® Inverting Buffers

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard LS output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6430–1

Order Number DM54LS368AJ, DM74LS368AM or DM74LS368AN
See NS Package Number J16A, M16A or N16A

Function Table

$Y = \overline{A}$

Inputs		Output
A	$\overline{G}$	Y
L	L	H
H	L	L
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS368A			DM74LS368A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−1			−2.6	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	A Input			−20	μA
		V_{CC} = Max, V_I = 0.4V (Note 5)	A Input			−0.4	mA
		V_{CC} = Max, V_I = 0.4V	$\overline{G}$ Input			−0.4	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			12	21	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the DATA inputs grounded and the OUTPUT CONTROLS at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		15		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		18		25	ns
t_{PZH}	Output Enable Time to High Level Output		30		35	ns
t_{PZL}	Output Enable Time to Low Level Output		30		40	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 6)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 6)		20			ns

Note 6: C_L = 5 pF.

National Semiconductor Corporation

DM54LS373/DM74LS373, DM54LS374/DM74LS374 TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

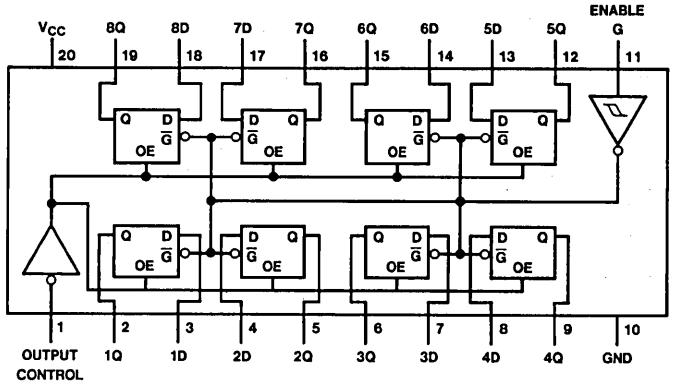
These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. (Continued)

Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- TRI-STATE bus-driving outputs
- Full parallel-access for loading
- Buffered control inputs
- Clock/Enable input has hysteresis to improve noise rejection
- P-N-P inputs reduce D-C loading on data lines

Connection Diagrams

Dual-In-Line Packages



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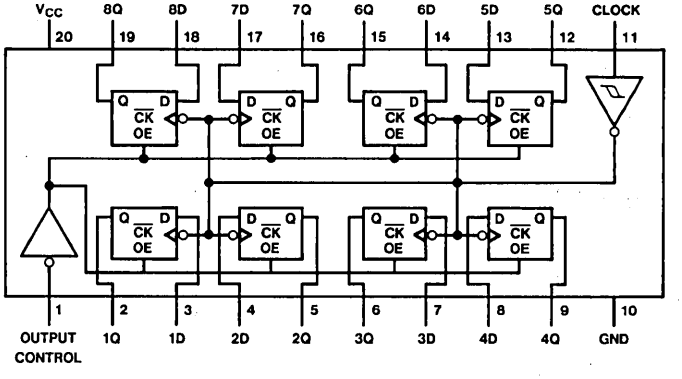


TL/F/6431–2

Order Number
DM54LS373J,
DM74LS373WM,
DM74LS373N,
DM54LS374J,
DM74LS374WM or
DM74LS374N
See NS Package Number
J20A, M20B or N20A

2

General Description (Continued)

The eight latches of the DM54/74LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM54/74LS374 are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as AC and DC noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Function Tables

DM54/74LS373

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

DM54/74LS374

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care

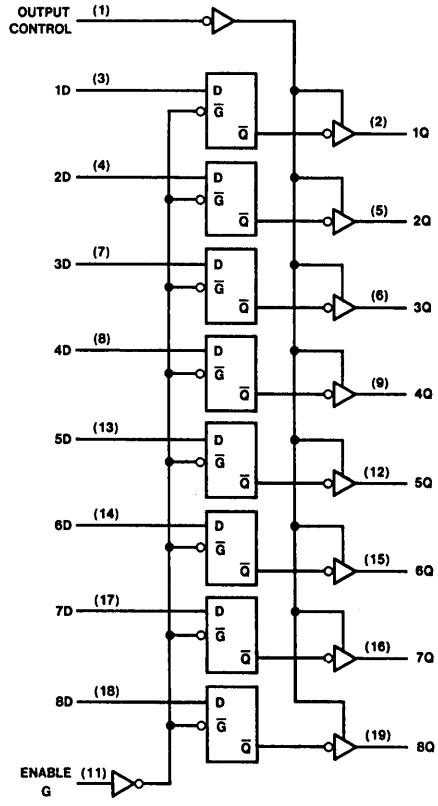
↑ = Transition from low-to-high level, Z = High Impedance State

Q_0 = The level of the output before steady-state input conditions were established.

Logic Diagrams

DM54/74LS373

Transparent Latches



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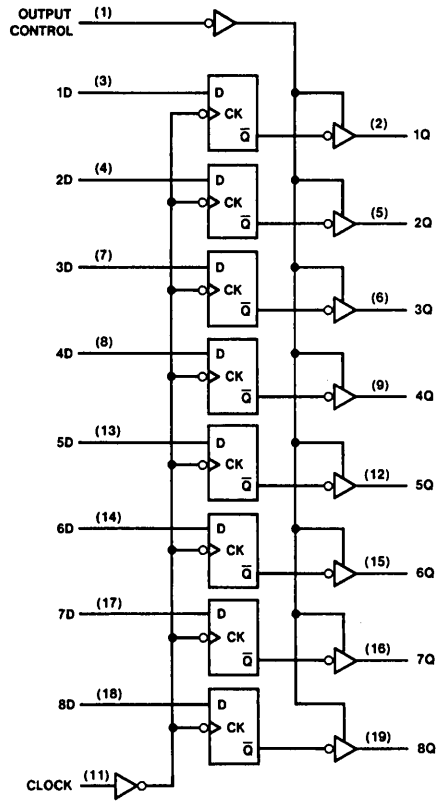
DM54/74LS374

Positive-Edge-Triggered Flip-Flops



TL/F/6431–4

Absolute Maximum Ratings (See Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS373			DM74LS373			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Votage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Pulse Width (Note 2)	Enable High	15			15			ns
		Enable Low	15			15			
t_{SU}	Data Setup Time (Notes 1 & 2)		5↓			5↓			ns
t_H	Data Hold Time (Notes 1 & 2)		20↓			20↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: T_A = 25°C and V_{CC} = 5V.

'LS373 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max			24	40	mA

'LS373 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Q		18		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Q		18		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Q		30		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Q		30		36	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Any Q		28		36	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Any Q		36		50	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 3)	Output Control to Any Q		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 3)	Output Control to Any Q		25			ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: C_L = 5 pF.

Recommended Operating Conditions

Symbol	Parameter		DM54LS374			DM74LS374			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
f_{CLK}	Clock Frequency (Note 2)		0		35	0		35	MHz
f_{CLK}	Clock Frequency (Note 3)		0		20	0		20	MHz
t_W	Pulse Width (Note 4)	Clock High	15			15			ns
		Clock Low	15			15			
t_{SU}	Data Setup Time (Notes 1 & 4)		20↑			20↑			ns
t_H	Data Hold Time (Notes 1 & 4)		0↑			0↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 45 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 150 pF, R_L = 667Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

'LS374 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.1		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 12 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−0.4	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max			27	45	mA

'LS374 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 45 pF		C_L = 150 pF		
		Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	35		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output		28		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		28		38	ns
t_{PZH}	Output Enable Time to High Level Output		28		44	ns
t_{PZL}	Output Enable Time to Low Level Output		28		44	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 3)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 3)		25			ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: C_L = 5 pF.

National Semiconductor Corporation

DM54LS390/DM74LS390 Dual 4-Bit Decade Counter

General Description

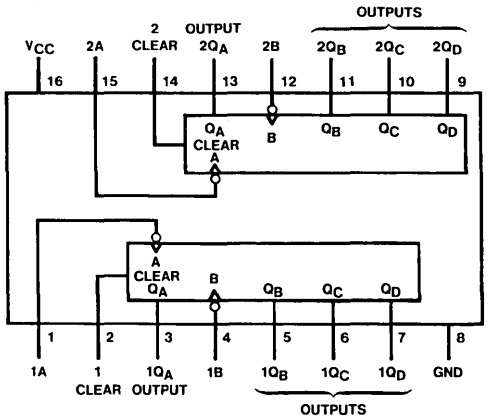
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and/or cumulative multiples of 2 and/or 5 up to divide-by-100. When connected as a bi-quinary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage. The 'LS390 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Features

- Dual version of the popular 'LS90
- 'LS390 . . . individual clocks for A and B flip-flops provide dual ÷ 2 and ÷ 5 counters
- Direct clear for each 4-bit counter
- Dual 4-bit version can significantly improve system densities by reducing counter package count by 50%
- Typical maximum count frequency . . . 35 MHz
- Buffered outputs reduce possibility of collector commutation

Connection Diagram

Dual-In-Line Package



TL/F/6433–1

Order Number DM54LS390J, DM74LS390M or DM74LS390N
See NS Package Number J16A, M16A or N16A

Function Tables

BCD Count Sequence (Each Counter) (See Note A)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-Quinary (5-2) (Each Counter) (See Note B)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

Note A: Output Q_A is connected to input B for BCD count.
Note B: Output Q_D is connected to input A for Bi-quinary count.
Note C: H = High Level, L = Low Level.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	
Clear	7V
A or B	5.5V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS390			DM74LS390			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)	A to Q_A	0		25	0		25	MHz
		B to Q_B	0		20	0		20	
f_{CLK}	Clock Frequency (Note 2)	A to Q_A	0		20	0		20	MHz
		B to Q_B	0		15	0		15	
t_W	Pulse Width (Note 1)	A	20			20			ns
		B	25			25			
		Clear High	20			20			
t_{REL}	Clear Release Time (Notes 3 & 4)		25 ↓			25 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: The symbol (↓) indicates the falling edge of the clear pulse is used for reference.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Clear			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
			B			0.4	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clear			20	μA
			A			40	
			B			80	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−0.4	mA
			A			−1.6	
			B			−2.4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			15	26	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

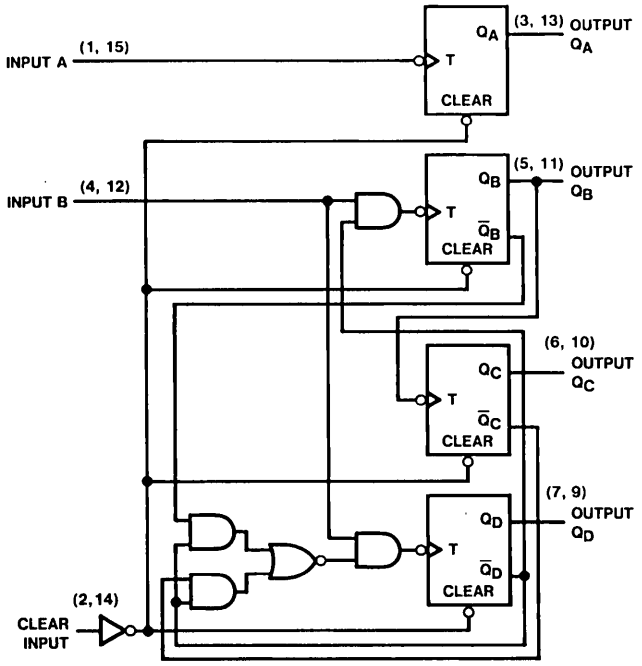
Note 3: I_{CC} is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5 and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	25		20		MHz
		B to Q_B	20		15		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_C		60		81	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_C		60		81	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		21		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		39		51	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		39		54	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		21		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		21		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		39		45	ns

Logic Diagram

'LS390



TL/F/6433–2

National Semiconductor Corporation

DM54LS393/DM74LS393 Dual 4-Bit Binary Counter

General Description

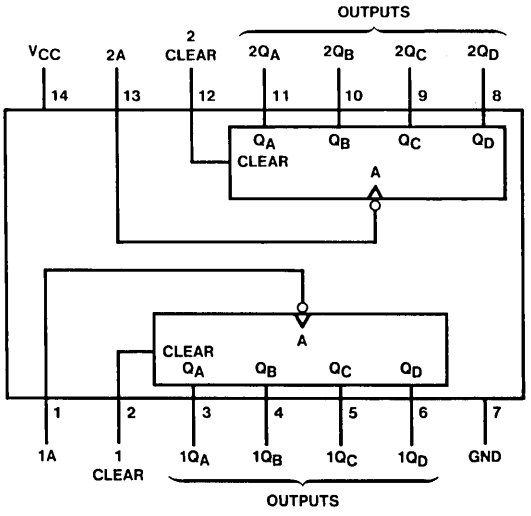
Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The 'LS393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The LS393 has parallel outputs from each counter stage so that any submultiple of the input count freqency is available for system-timing signals.

Features

- Dual version of the popular 'LS93
- 'LS393 dual 4-bit binary counter with individual clocks
- Direct clear for each 4-bit counter
- Dual 4-bit versions can significantly improve system densities by reducing counter package count by 50%
- Typical maximum count frequency 35 MHz
- Buffered outputs reduce possibility of collector commutation

Connection Diagram

Dual-In-Line Package



TL/F/6434–1

Order Number DM54LS393J, DM74LS393M or DM74LS393N
See NS Package Number J14A, M14A or N14A

Function Table

Count Sequence (Each Counter)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	
Clear	7V
A	5.5V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54LS393			DM74LS393			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				4			8	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
f_{CLK}	Clock Frequency (Note 2)		0		20	0		20	MHz
t_W	Pulse Width (Note 7)	A	20			20			ns
		Clear High	20			20			
t_{REL}	Clear Release Time (Notes 3 & 7)		25 ↓			25 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.35	0.5	
		I_{OL} = 4 mA, V_{CC} = Min	DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	Clear			0.1	mA
		V_{CC} = Max, V_I = 5.5V	A			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Clear			20	μA
			A			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clear			−0.4	mA
			A			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			15	26	mA

Note 1: C_L = 15 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 2 kΩ, T_A = 25°C and V_{CC} = 5V.

Note 3: The symbol (↓) indicates that the falling edge of the clear pulse is used for reference.

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

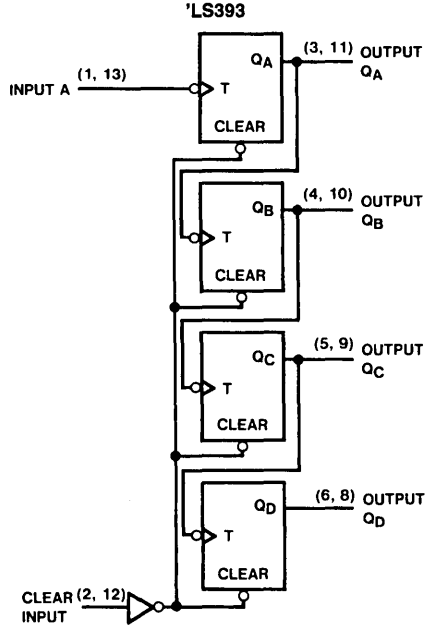
Note 6: I_{CC} is measured with all outputs open, both CLEAR inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Note 7: T_A = 25°C, and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 2 kΩ				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	25		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		20		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		20		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		60		87	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		60		87	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		39		45	ns

Logic Diagram



TL/F/6434–2

National Semiconductor Corporation

DM54LS465/DM74LS465, DM54LS466/DM74LS466, DM54LS467/DM74LS467, DM54LS468/DM74LS468 (DM71LS95A/DM81LS95A, DM71LS96A/DM81LS96A, DM71LS97A/DM81LS97A, DM71LS98A/DM81LS98A) TRI-STATE® Octal Buffers

General Description

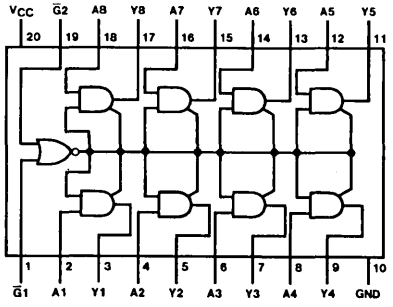
These devices provide eight, two-input buffers in each package. All employ the newest low-power-Schottky TTL technology. One of the two inputs to each buffer is used as a control line to gate the output into the high-impedance state, while the other input passes the data through the buffer. The LS465 and LS467 present true data at the outputs, while the LS466 and LS468 are inverting. On the LS465 and LS466 versions, all eight TRI-STATE enable lines are common, with access through a 2-input NOR gate. On the LS467 and LS468 versions, four buffers are enabled from one common line, and the other four buffers are enabled from another common line. In all cases the outputs are placed in the TRI-STATE condition by applying a high logic level to the enable pins. These devices represent octal, low power-Schottky versions of the very popular DM54/74365, 366, 367, and 368 (DM70/8095, 96, 97, and 98) TRI-STATE hex buffers.

Features

- Octal versions of popular DM54/74365, 366, 367, and 368 (DM70/8095, 96, 97 and 98)
- Typical power dissipation
  - DM54/74LS465, 467 80 mW
  - DM54/74LS466, 468 65 mW
- Typical propagation delay
  - DM54/74LS465, 467 15 ns
  - DM54/74LS466, 468 10 ns
- Low power-Schottky, TRI-STATE technology

Connection Diagrams

Dual-In-Line Packages



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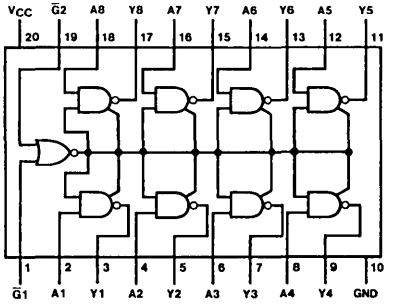

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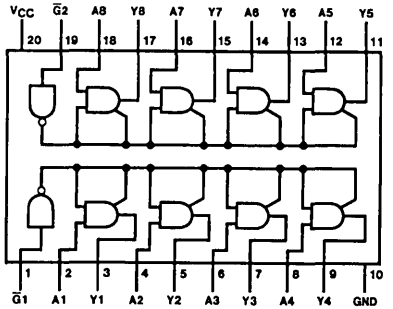

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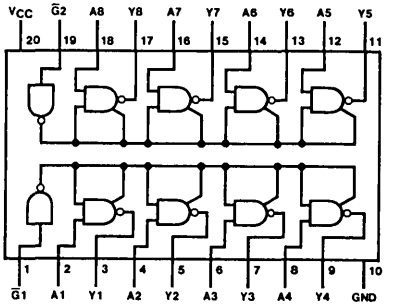


TL/F/6435-4

Order Numbers DM54LS465J, DM54LS466J, DM54LS467J, DM54LS468J, DM74LS465N, DM74LS465WM, DM74LS466N, DM74LS466WM, DM74LS467N, DM74LS467WM, DM74LS468N or DM74LS468WM. See NS Package Number J20A, M20B or N20A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. the parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS465, 466, 467, 468			DM74LS465, 466, 467, 468			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.8	V
I_{OH}	High Level Output Current			−2.6			−5.2	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'LS465 and 'LS467 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		DM54	2.5			V
				DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		DM54			0.4	V
				DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min		DM74			0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	µA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.5V	A (Note 3)			−20	µA
			V_I = 0.4V	A (Note 4)			−50	
				$\overline{G}$			−50	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max					20	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max					−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		DM54	−20		−100	mA
				DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				16	26	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Both $\overline{G}$ inputs are at 2V.

Note 4: Both $\overline{G}$ inputs are at 0.4V.

'LS465 and 'LS467 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		16		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		28		40	ns
t_{PZH}	Output Enable Time to High Level Output		25		30	ns
t_{PZL}	Output Enable Time to Low Level Output		30		42	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)		27			ns

Note 1: C_L = 5 pF.

'LS466 and 'LS468 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions			Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA					−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		DM54	2.5			V
				DM74	2.7			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min		DM54			0.4	V
				DM74			0.5	
		I_{OL} = 12 mA, V_{CC} = Min		DM74			0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 7V					0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V					20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	V_I = 0.5V	A (Note 4)			−20	μA
			V_I = 0.4V	A (Note 5)			−50	
				$\overline{G}$			−50	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max					20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max					−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)		DM54	−20		−100	mA
				DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)				13	21	mA

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

'LS466 and 'LS468 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 667Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		10		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		17		30	ns
t_{PZH}	Output Enable Time to High Level Output		15		30	ns
t_{PZL}	Output Enable Time to Low Level Output		35		45	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)		20			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)		27			ns

Note 1: C_L = 5 pF.

Function Tables

LS465

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	H
L	L	L	L

LS466

Inputs			Output
$\overline{G}1$	$\overline{G}2$	A	Y
H	X	X	Hi-Z
X	H	X	Hi-Z
L	L	H	L
L	L	L	H

LS467

Inputs		Output
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	H
L	L	L

LS468

Inputs		Output
$\overline{G}$	A	Y
H	X	Hi-Z
L	H	L
L	L	H

H = High Logic Level
L = Low Logic Level
X = Either High or Low Logic Level
Hi-Z = High Impedance (Off) State

National Semiconductor Corporation

DM54LS645/DM74LS645 Octal Bus Transceivers

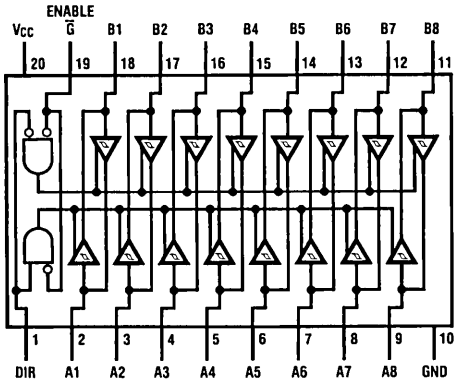
General Description

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The devices transmit data from the A bus to the B bus or from the B bus to the A bus depending upon the level at the direction control (DIR) input. The enable input ($\overline{G}$) can be used to disable the device so that the buses are effectively isolated.

Features

- Bi-directional bus transceivers in high-density 20-pin packages
- Hysteresis at bus inputs improves noise margins
- TRI-STATE® outputs

Connection Diagram



TL/F/9056–1

Order Number DM54LS645J or DM74LS645N, DM74LS645WM
See NS Package Number J20A, M20B or N20A

Function Table

Control Inputs		'LS645
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High Level
L = Low Level
X = Irrelevant

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−55°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS645			DM74LS645			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage (Note 1)	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.5			0.6	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			12			24	mA
T_A	Free Air Operating Temperature	−55		−125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 2)		DM54LS645			DM74LS645			Units
				Min	Typ (Note 3)	Max	Min	Typ (Note 3)	Max	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = 18 mA				−1.5			−1.5	V
H_{YS}	Hysteresis ($V_{T+} - V_{-}$) A or B Input	V_{CC} = Min		0.1	0.4		0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
			I_{OH} = Max	2			2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = Max	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, G at 2V, V_O = 2.7V				20			20	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = Max, G at 2V V_O = 0.4V				−400			−400	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max	A or B, V_I = 5.5V			0.1			0.1	mA
			DIR or G, V_I = 7V			0.1			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_{IH} = 2.7V				20			20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_{IL} = 0.4V				−0.4			−0.4	mA
I_{OS}	Short Circuit Output Current (Note 4)	V_{CC} = Max		−40		−225	−40		−225	mA
I_{CC}	Total Supply Current	Outputs High	V_{CC} = Max, Outputs Open		48	70		48	70	mA
		Outputs Low			62	90		62	90	
		Outputs at Hi-Z			64	95		64	95	

Note 1: Voltage values are with respect to the network ground terminal.

Note 2: For conditions shown as Min or Max, use the appropriate value specified under Recommended Operating Conditions.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 5 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to B		15			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to B		15			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to A		15			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to A		15			ns
t_{PZL}	Output Enable Time to Low Level	$\overline{G}$ to A		40			ns
t_{PZH}	Output Enable Time to High Level	$\overline{G}$ to A		40			ns
t_{PZL}	Output Enable Time to Low Level	$\overline{G}$ to B		40			ns
t_{PZH}	Output Enable Time to High Level	$\overline{G}$ to B		40			ns
t_{PLZ}	Output Disable Time to Low Level	$\overline{G}$ to A				25	ns
t_{PHZ}	Output Disable Time to High Level	$\overline{G}$ to A				25	ns
t_{PLZ}	Output Disable Time to Low Level	$\overline{G}$ to B				25	ns
t_{PHZ}	Output Disable Time to High Level	$\overline{G}$ to B				25	ns

National Semiconductor Corporation

DM54LS670/DM74LS670 TRI-STATE® 4-by-4 Register Files

General Description

These register files are organized as 4 words of 4 bits each, and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits writing into one location, and reading from another word location, simultaneously.

Four data inputs are available to supply the word to be stored. Location of the word is determined by the write select inputs A and B, in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high level signal is desired from the output, a high level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write-enable input, G_W, is high, the data inputs are inhibited and their levels can cause no change in the information stored in the internal latches. When the read-enable input, G_R, is high, the data outputs are inhibited and go into the high impedance state.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data entry addressing separate from data read addressing and individual sense line — eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (27 ns typical) and the read time (24 ns typical). The register file has a non-volatile readout in that data is not lost when addressed.

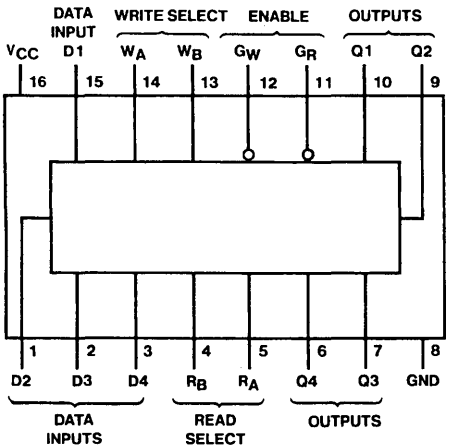
All inputs (except read enable and write enable) are buffered to lower the drive requirements to one normal Series 54LS/74LS load, and input clamping diodes minimize switching transients to simplify system design. High speed, double ended AND-OR-INVERT gates are employed for the read-address function and have high sink current, TRI-STATE outputs. Up to 128 of these outputs may be wire-AND connected for increasing the capacity up to 512 words. Any number of these registers may be paralleled to provide n-bit word length.

Features

- For use as:
  - Scratch pad memory
  - Buffer storage between processors
  - Bit storage in fast multiplication designs
- Separate read/write addressing permits simultaneous reading and writing
- Organized as 4 words of 4 bits
- Expandable to 512 words of n-bits
- TRI-STATE versions of DM54LS170/DM74LS170
- Fast access times 20 ns typ

Connection Diagram

Dual-In-Line Package



TL/F/6436–1

Order Number DM54LS670J, DM74LS670M or DM74LS670N
See NS Package Number J16A, M16A or N16A

Function Tables

WRITE TABLE (SEE NOTES A, B, AND C)

Write Inputs			Word			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_0	Q_0	Q_0
L	H	L	Q_0	Q = D	Q_0	Q_0
H	L	L	Q_0	Q_0	Q = D	Q_0
H	H	L	Q_0	Q_0	Q_0	Q = D
X	X	H	Q_0	Q_0	Q_0	Q_0

READ TABLE (SEE NOTES A AND D)

Read Inputs			Outputs			
R_B	R_A	G_R	Q1	Q2	Q3	Q4
L	L	L	WOB1	WOB2	WOB3	WOB4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

Note A: H = High Level, L = Low Level, X = Don't Care, Z = High Impedance (Off).

Note B: (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.

Note C: Q_0 = The level of Q before the indicated input conditions were established.

Note D: WOB1 = The first bit of word 0, etc.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54S670			DM74S670			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.8	V
I_{OH}	High Level Output Current				−1			−2.6	mA
I_{OL}	Low Level Output Current				12			24	mA
t_W	Write Enable Pulse Width (Note 3)		25			25			ns
t_{SU}	Setup Time (Notes 1 & 3)	Data	10			10			ns
		W_A, W_B	15			15			
t_H	Hold Time (Notes 1 & 3)	Data	15			15			ns
		W_A, W_B	5			5			
t_{LATCH}	Latch Time for New Data (Notes 2 & 3)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: Times are with respect to the Write-Enable input. Write-Select time will protect the data written into the previous address. If protection of data in the previous address, t_{SETUP} (W_A, W_B) can be ignored. As any address selection sustained for the final 30 ns of the Write-Enable pulse and during t_H (W_A, W_B) will result in data being written into that location. Depending on the duration of the input conditions, one or a number of previous addresses may have been written into.

Note 2: Latch time is the time allowed for the internal output of the latch to assume the state of new data. This is important only when attempting to read from a location immediately after that location has received new data.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, I_{OL} = Max, V_{IH} = Min	DM54		0.25	0.4	V
			DM74		0.34	0.5	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	D, R or W			0.1	mA
			G_W			0.2	
			G_R			0.3	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D, R or W			20	μA
			G_W			40	
			G_R			60	

Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	D, R, or W			−0.4	mA
			G_W			−0.8	
			G_R			−1.2	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max				20	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−20	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−100	mA
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	50	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 667Ω				Units
			C_L = 45 pF		C_L = 150 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Read Select to Q		40		50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Read Select to Q		45		55	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Write Enable to Q		45		55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Write Enable to Q		50		60	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Q		45		55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Q		40		50	ns
t_{PZH}	Output Enable Time to High Level Output	Read Enable to Any Q		35		45	ns
t_{PZL}	Output Enable Time to Low Level Output	Read Enable to Any Q		40		50	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 4)	Read Enable to Any Q		50			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 4)	Read Enable to Any Q		35			ns

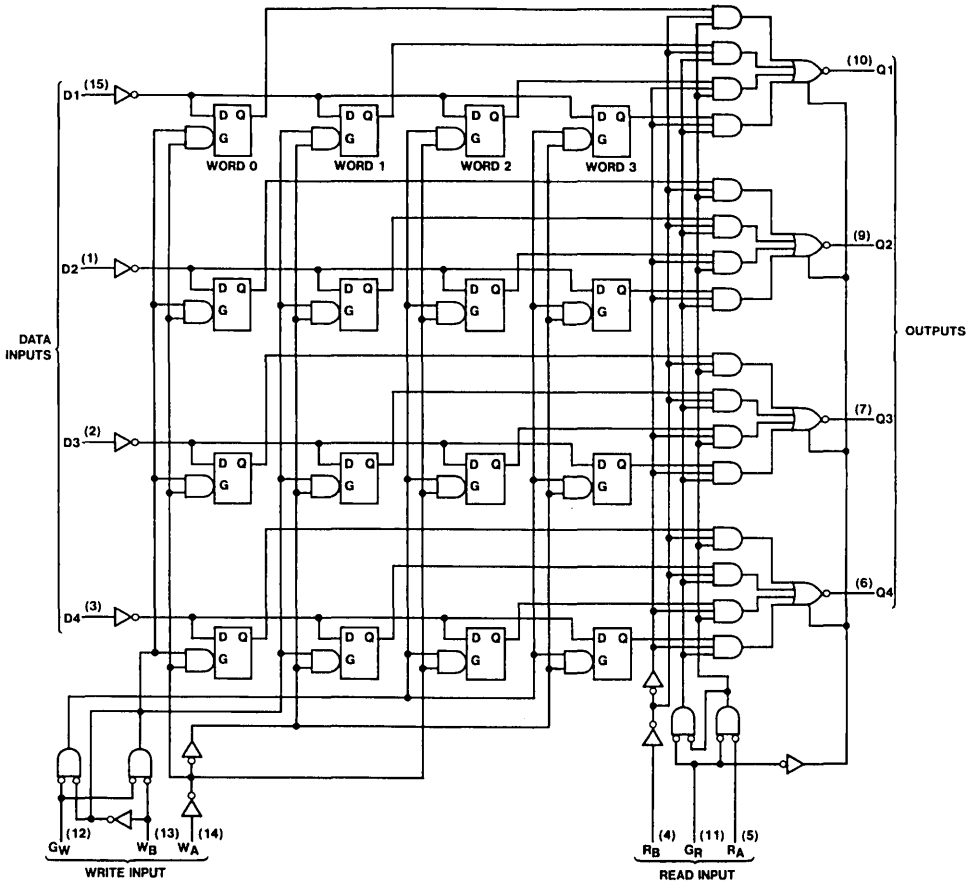
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with 4.5V applied to all DATA inputs and both ENABLE inputs, all ADDRESS inputs are grounded and all outputs are open.

Note 4: C_L = 5 pF.

Logic Diagram



TL/F/6436-2

National Semiconductor Corporation

DM54LS952/DM74LS952 Dual Rank 8-Bit TRI-STATE® Shift Registers

General Description

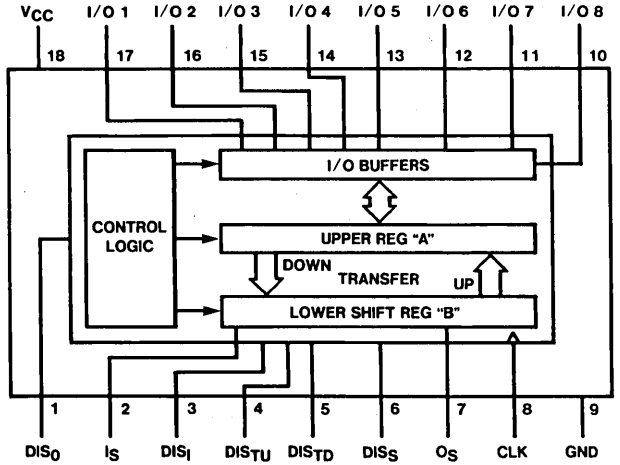
These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register "A", parallel transfer down from register "A" to serial shift register "B", parallel transfer up from shift register "B" to register "A", serial shift of register "B", synchronously clear. Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Features

- Registers are edge-triggered by the positive transition of the clock
- All inputs are PNP transistors
- Input disable dominates over output disable
- Output high impedance state does not impede any other mode of operation
- 8-bit I/O pins are TRI-STATE buffers
- Typical shift frequency is 36 MHz
- Typical power dissipation is 305 mW
- All control inputs are active when in an "L" logic state
- Devices can be cascaded into N-bit word

Connection Diagram

Dual-In-Line Package



TL/F/6437–1

Top View

Order Number DM54LS952J or DM74LS952N
See NS Package Number J18A or N18A

Pin Description

DIS_O—Output disable
I_S—Serial input
DIS_I—Input disable
DIS_{TU}—Transfer up disable
DIS_{TD}—Transfer down disable
DIS_S—Shift disable
O_S—Serial output
CLK—Clock
GND—Ground
I/O 1 . . . I/O 8—8-bit I/O pins
V_{CC}—Supply Voltage

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS952			DM74LS952			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-Level Input Voltage	2			2			V
V_{IL}	Low-Level Input Voltage			0.7			0.8	V
I_{OH}	High-Level Output Current			−2.6			−5.2	mA
I_{OL}	Low-Level Output Current			8			16	mA
f_{CLOCK}	Clock Frequency (Note 5)	0		25	0		25	MHz
Clock Pulse	High Pulse Width (Note 5)	25	17		25	17		ns
	Low Pulse Width (Note 5)	15	7		15	7		ns
t_{SET-UP}	Data Set-Up Time (Note 5)	10			10			ns
t_{HOLD}	Data Hold Time (Note 5)	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (1)		DM54LS952			DM74LS952			Units
				Min	Typ (2)	Max	Min	Typ (2)	Max	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = V_{IL} Max	I_{OH} = −2.6 mA	2.4						V
			I_{OH} = −5.2 mA				2.4			
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, V_{IL} = V_{IL} Max	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA					0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1			0.1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.7V				20			20	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V				−50			−50	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max (3)		−20		−100	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (4)			61	99		61	99	mA
I_{OFF}	TRI-STATE I/O Current	V_{CC} = Max, V_{IH} = 2V	V_O = 2.4V			20			20	μA
			V_O = 0.4V			−20			−20	μA

Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

Note 2: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

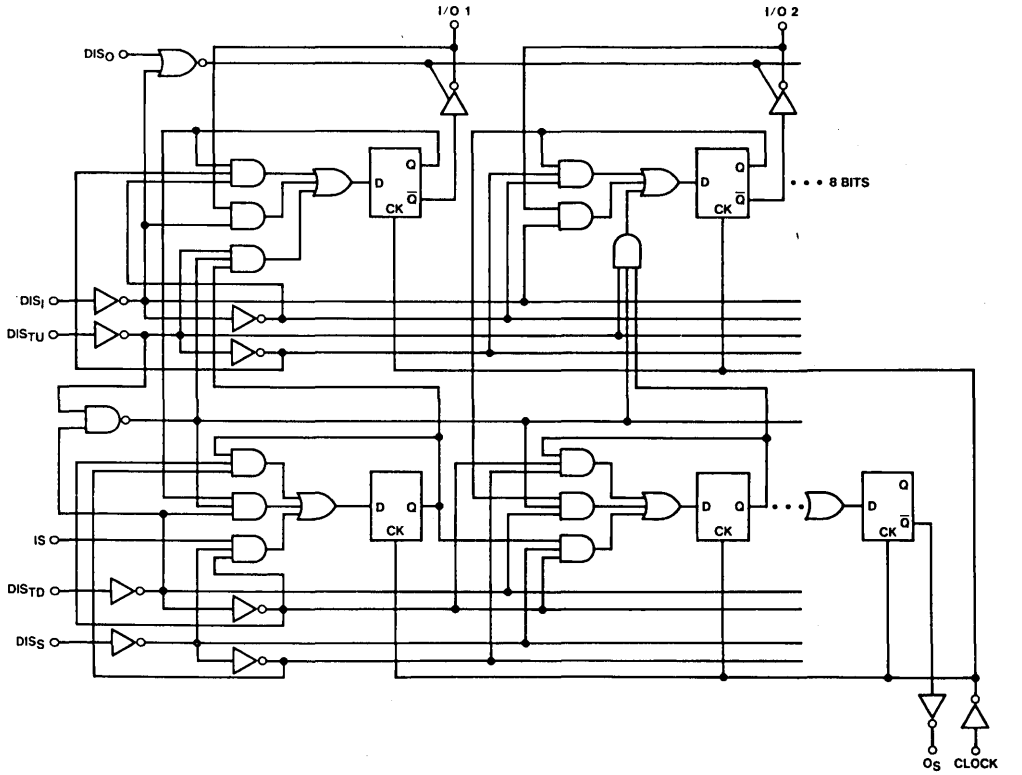
Note 4: I_{CC} is measured with serial output open, the clock and shift disable input at 2.4V. All other control inputs and I/O pins grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 1 kΩ	25		MHz
t_{PLH}	Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs		7	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level from Clock to Any Output		10	48	ns
t_{ENABLE}	Enable Time from Any Control Inputs		5	24	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		6	27	ns
t_{ZH}	Output Enable Time to High Level		5	23	ns
t_{ZL}	Output Enable to Low Level		4	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 1 kΩ	5	23	ns
t_{LZ}	Output Disable Time from Low Level		6	27	ns

Logic Diagram



TL/F/6437–2

Function Table

Table I

DIS_O	DIS_I	DIS_{TU}	DIS_{TD}	DIS_S	CLK	I_S	8-Bit I/O Pins	Content of Upper Reg. "A"								Content of Lower Serial Shift Reg. "B"								O_S	Comments
								A1	A2	A3	A4	A5	A6	A7	A8	B1	B2	B3	B4	B5	B6	B7	B8		
H	H	H	H	H	X	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Stable state
L	H	H	H	H	X	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	H	H	H	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Entering data from I/O to reg. "A"
H	H	L	H	H	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Transfer data up from reg. "B" to reg. "A"
L	H	L	H	H	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	L	H	H	↑	X	Input	←	←	←	DOR	→	→	→		b1	b2	b3	b4	b5	b6	b7	b8	b8	Reg. "A" will OR data from I/O to reg. "B"
H	H	H	L	X	↑	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Transfer data down from reg. "A" to reg. "B"
L	H	H	L	X	↑	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	
X	L	H	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Entering data and transfer down
H	H	L	L	X	↑	X	Hi-Z	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	(1) Synchronously clear both registers to
L	H	L	L	X	↑	X	Output	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	(2) logic "L" level
X	L	L	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	L	L	L	L	L	L	L	L	L	(3) Enter data to reg. "A" clear reg. "B"
H	H	H	H	L	↑	d	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	Serial shifting in the lower reg. "B"
L	H	H	H	L	↑	d	Output	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	H	H	L	↑	d	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	d	b1	b2	b3	b4	b5	b6	b7	b7	Entering data and serial shifting
H	H	L	H	L	↑	d	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	Transfer up and serial shifting
L	H	L	H	L	↑	d	Output	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	L	H	L	↑	d	Input	←	←	←	DOR	→	→	→		d	b1	b2	b3	b4	b5	b6	b7	b7	DOR function and serial shifting

X ≡ Don't Care

Hi-Z/Output/Input/ ≡ High impedance state/output state/input state

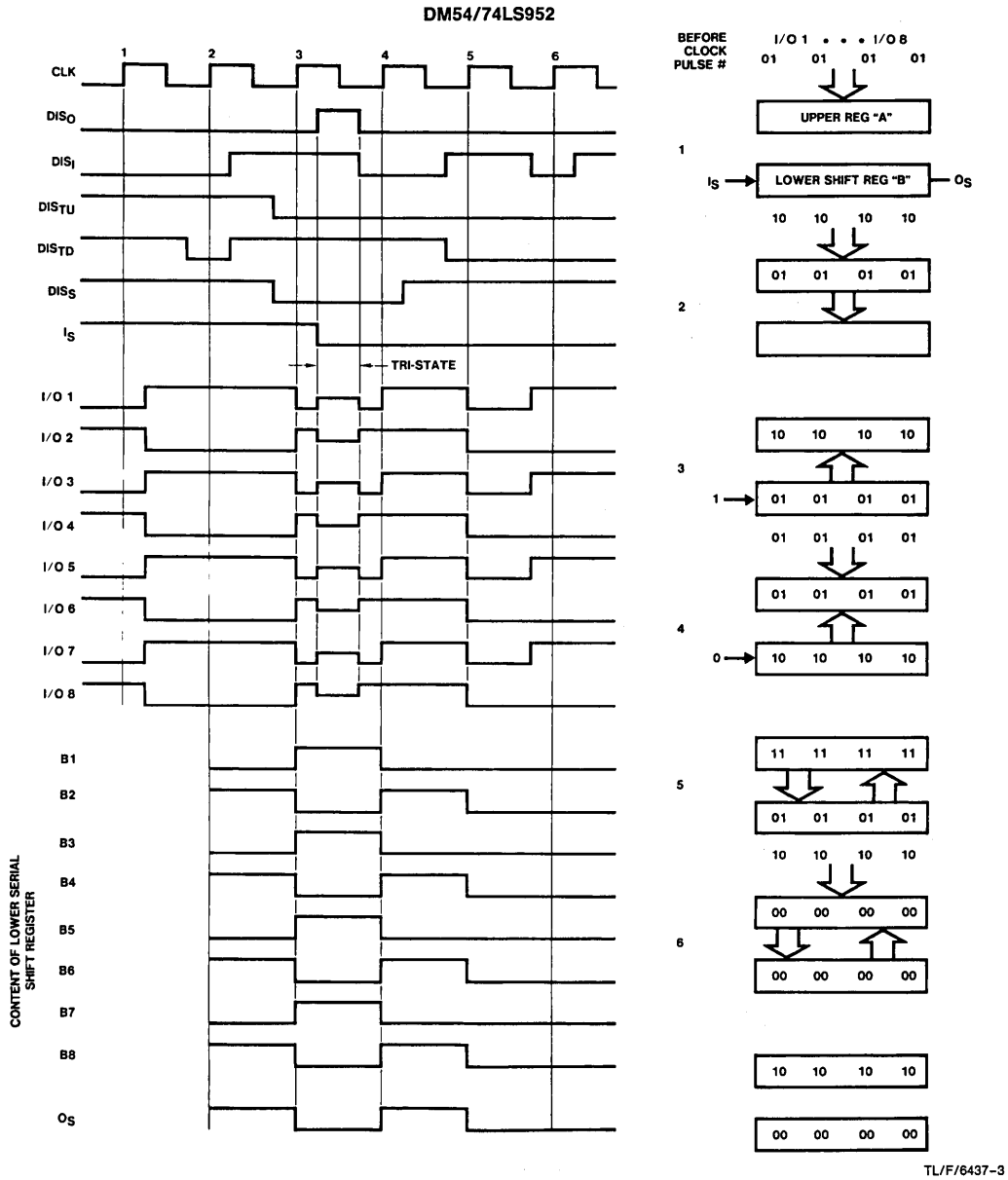
a1 ... a8/b1 ... b8 ≡ The content of the upper register "A"/the lower serial shift register "B" before the most recent ↑ transition of the clock

$I_1 \ldots I_8$ ≡ The level of steady state inputs of the I/O pins

DOR ≡ "Data ORing function" ORing data from both I/O pins and register "B", i.e., I_1 + b1, I_2 + b2, I_3 + b3 ... I_8 + b8

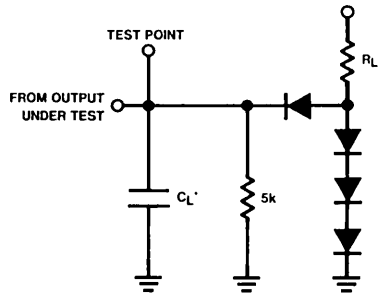
d ≡ Data of the serial input

Timing Diagram



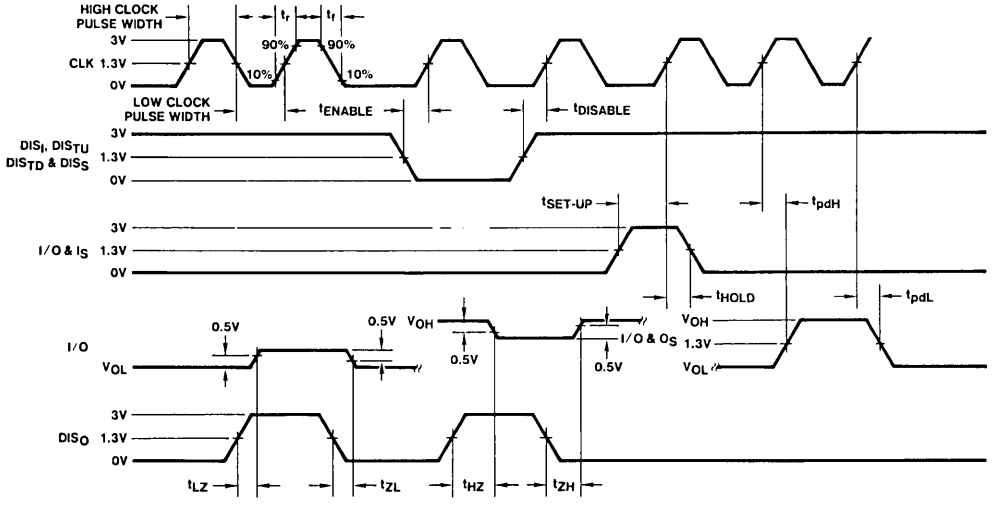
TL/F/6437–3

AC Test Circuit and Switching Time Waveforms



All diodes are 1N916 or 1N3064.
C_L includes probe and jig capacitance.

TL/F/6437–4

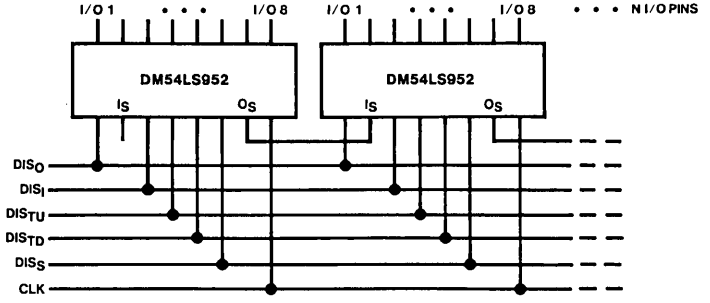


TL/F/6437–5

All input pulses are supplied by generators having $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR ≤ 1 MHz, $Z_{OUT} \approx 50\Omega$.

Cascading Packages

Cascading Packages for N-Bit Word



TL/F/6437–6

National Semiconductor Corporation

DM54LS962/DM74LS962 Dual Rank 8-Bit TRI-STATE® Shift Registers

General Description

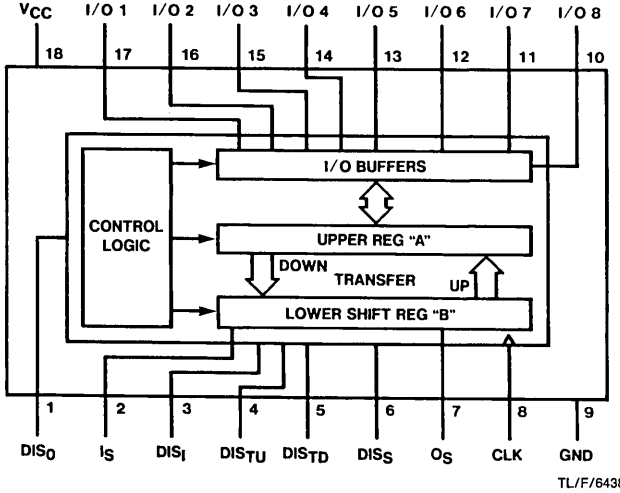
These circuits are TRI-STATE, edge-triggered, 8-bit I/O registers in parallel with 8-bit serial shift registers which are capable of operating in any of the following modes: parallel load from I/O pins to register "A", parallel transfer down from register "A" to serial shift register "B", parallel transfer up from shift register "B" to register "A", serial shift of register "B", or exchange data between register "A" and shift register "B". Since the registers are edge-triggered by the positive transition of the clock, the control lines which determine the mode or operation are completely independent of the logic level applied to the clock. Designed for bus-oriented systems, these circuits have their TRI-STATE inputs and outputs on the same pins.

Features

- Registers are edge-triggered by the positive transition of the clock
- All inputs are PNP transistors
- Input disable dominates over output disable
- Output high impedance state does not impede any other mode of operation
- 8-bit I/O pins are TRI-STATE buffers
- Typical shift frequency is 36 MHz
- Typical power dissipation is 305 mW
- All control inputs are active when in an "L" logic state
- Devices can be cascaded into N-bit word

Connection Diagram

Dual-In-Line Package



TL/F/6438–1

Top View

Order Number DM54LS962J or DM74LS962N
See NS Package Number J18A or N18A

Pin Description

DIS_O—Output disable
I_S—Serial input
DIS_I—Input disable
DIS_{TU}—Transfer up disable
DIS_{TD}—Transfer down disable
DIS_S—Shift disable
O_S—Serial output
CLK—Clock
GND—Ground
I/O 1 . . . I/O 8—8-bit I/O pins
V_{CC}—Supply Voltage

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
DM54LS	−55°C to +125°C
DM74LS	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54LS962			DM74LS962			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-Level Input Voltage	2			2			V
V_{IL}	Low-Level Input Voltage			0.8			0.8	V
I_{OH}	High-Level Output Current			−2.6			−5.2	mA
I_{OL}	Low-Level Output Current			8			16	mA
f_{CLOCK}	Clock Frequency (Note 5)	0		25	0		25	MHz
Clock Pulse	High Pulse Width (Note 5)	25	17		25	17		ns
	Low Pulse Width (Note 5)	15	7		15	7		ns
t_{SET-UP}	Data Set-Up Time (Note 5)	10			10			ns
t_{HOLD}	Data Hold Time (Note 5)	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (1)		DM54LS962			DM74LS962			Units
				Min	Typ (2)	Max	Min	Typ (2)	Max	
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = V_{IL} Max	I_{OH} = −2.6 mA	2.4						V
			I_{OH} = −5.2 mA				2.4			
V_{OL}	Low-Level Output Voltage	V_{CC} = Min, V_{IH} = 2 V, V_{IL} = V_{IL} Max	I_{OL} = 8 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 16 mA					0.35	0.5	
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1			0.1	mA
I_{IH}	High-Level Input Current	V_{CC} = Max, V_I = 2.7V				20			20	μA
I_{IL}	Low-Level Input Current	V_{CC} = Max, V_I = 0.4V				−50			−50	μA
I_{OS}	Short-Circuit Output Current	V_{CC} = Max (3)		−20		−100	−20		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (4)			61	99		61	99	mA
I_{OFF}	TRI-STATE I/O Current	V_{CC} = Max, V_{IH} = 2V	V_O = 2.4V			20			20	μA
			V_O = 0.4V			−20			−20	μA

Note 1: For conditions shown as min or max, use the appropriate value specified under recommended operating conditions.

Note 2: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

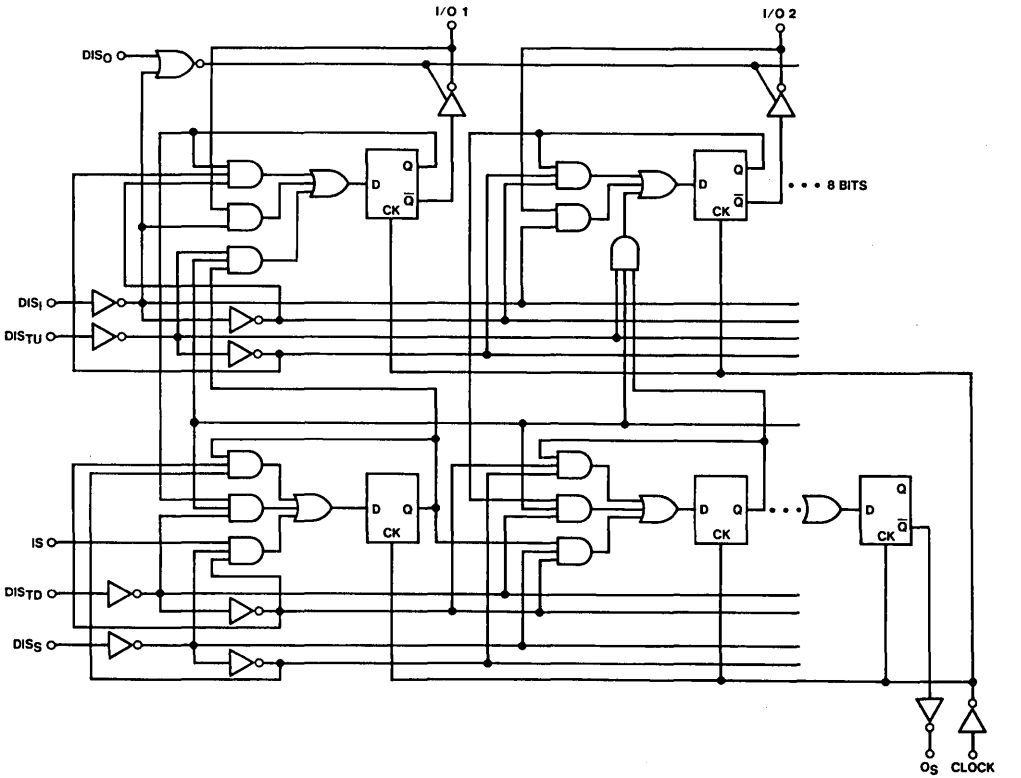
Note 4: I_{CC} is measured with serial output open, the clock and shift disable input at 2.4V. All other control inputs and I/O pins grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF, R_L = 1 kΩ	25		MHz
t_{PLH}	Propagation Delay Time, Low-to-High-Level from Clock to Any Outputs		7	33	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level from Clock to Any Outputs		10	48	ns
t_{ENABLE}	Enable Time from Any Control Inputs		5	24	ns
$t_{DISABLE}$	Disable Time from Any Control Inputs		6	27	ns
t_{ZH}	Output Enable Time to High Level		5	23	ns
t_{ZL}	Output Enable to Low Level		4	18	ns
t_{HZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 1 kΩ	5	23	ns
t_{LZ}	Output Disable Time from Low Level		6	27	ns

Logic Diagram



TL/F/6438–2

Function Table

Table I

DIS_O	DIS_I	DIS_{TU}	DIS_{TD}	DIS_S	CLK	I_S	8-Bit I/O Pins	Content of Upper Reg. "A"								Content of Lower Serial Shift Reg. "B"								O_S	Comments
								A1	A2	A3	A4	A5	A6	A7	A8	B1	B2	B3	B4	B5	B6	B7	B8		
H	H	H	H	H	X	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Stable state
L	H	H	H	H	X	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	H	H	H	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Entering data from I/O to reg. "A"
H	H	L	H	H	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	Transfer data up from reg. "B" to reg. "A"
L	H	L	H	H	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	b1	b2	b3	b4	b5	b6	b7	b8	b8	
X	L	L	H	H	↑	X	Input	←	←	←	DOR	→	→	→		b1	b2	b3	b4	b5	b6	b7	b8	b8	Reg. "A" will OR data from I/O to reg. "B"
H	H	H	L	X	↑	X	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Transfer data down from reg. "A" to reg. "B"
L	H	H	L	X	↑	X	Output	a1	a2	a3	a4	a5	a6	a7	a8	a1	a2	a3	a4	a5	a6	a7	a8	a8	
X	L	H	L	X	↑	X	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	a1	a2	a3	a4	a5	a6	a7	a8	a8	Entering data and transfer down
H	H	L	L	X	↑	X	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	a1	a2	a3	a4	a5	a6	a7	a8	a8	(1) Exchange data between registers
L	H	L	L	X	↑	X	Output	b1	b2	b3	b4	b5	b6	b7	b8	a1	a2	a3	a4	a5	a6	a7	a8	a8	(2) Beside data exchanging, reg. "A"
X	L	L	L	X	↑	X	Input	←	←	←	DOR	→	→	→		a1	a2	a3	a4	a5	a6	a7	a8	a8	(3) will "OR" data from I/O and reg. "B"
H	H	H	H	L	↑	d	Hi-Z	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	Serial shifting in the lower reg. "B"
L	H	H	H	L	↑	d	Output	a1	a2	a3	a4	a5	a6	a7	a8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	H	H	L	↑	d	Input	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	d	b1	b2	b3	b4	b5	b6	b7	b7	Entering data and serial shifting
H	H	L	H	L	↑	d	Hi-Z	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	Transfer up and serial shifting
L	H	L	H	L	↑	d	Output	b1	b2	b3	b4	b5	b6	b7	b8	d	b1	b2	b3	b4	b5	b6	b7	b7	
X	L	L	H	L	↑	d	Input	←	←	←	DOR	→	→	→		d	b1	b2	b3	b4	b5	b6	b7	b7	DOR function and serial shifting

X ≡ Don't Care

Hi-Z/Output/Input/ ≡ High impedance state/output state/input state

a1 ... a8/b1 ... b8 ≡ The content of the upper register "A"/the lower serial shift register "B" before the most recent ↑ transition of the clock

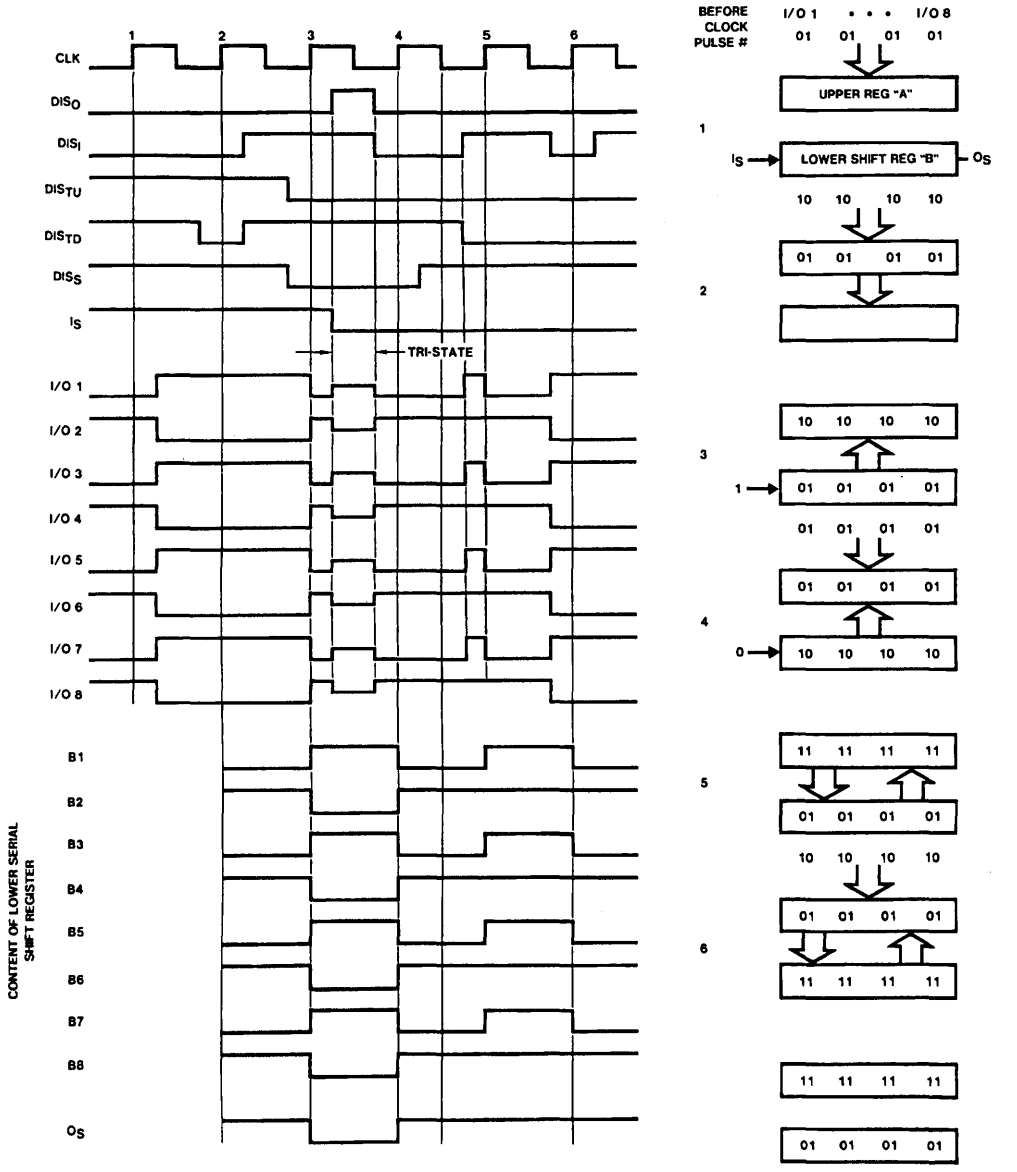
$I_1 \ldots I_8$ ≡ The level of steady state inputs of the I/O pins

DOR ≡ "Data ORing function" ORing data from both I/O pins and register "B", i.e., $I_1 + b1$, $I_2 + b2$, $I_3 + b3 \ldots I_8 + b8$

d ≡ Data of the serial input

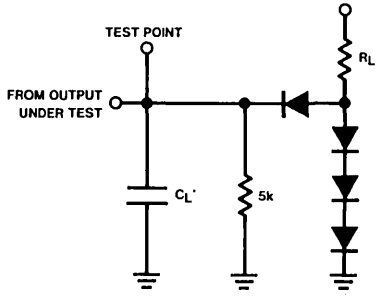
Timing Diagram

DM54/74LS962



TL/F/6438–3

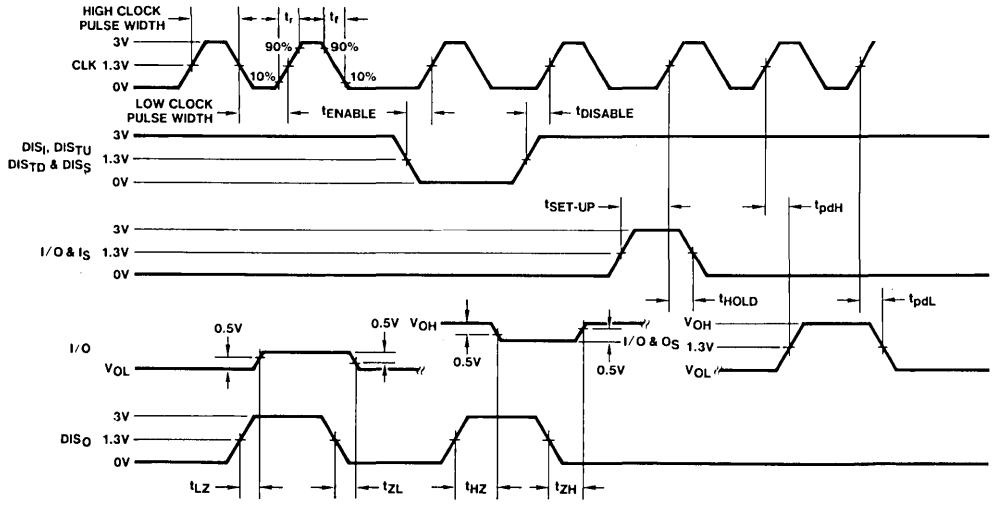
AC Test Circuit and Switching Time Waveforms



All diodes are 1N916 or 1N3064.

C_L includes probe and jig capacitance.

TL/F/6438–4

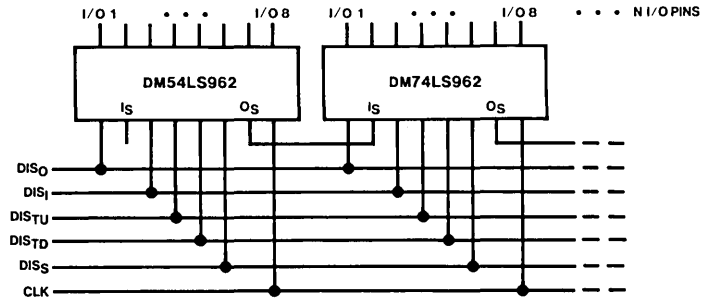


TL/F/6438–5

All input pulses are supplied by generators having $t_r \leq 15$ ns, $t_f \leq 6$ ns, PRR $\leq$ 1MHz, $Z_{OUT} \approx 50\Omega$.

Cascading Packages

Cascading Packages for N-Bit Word



TL/F/6438–6

Section 3

Schottky

Section 3 Contents

National Semiconductor Corporation

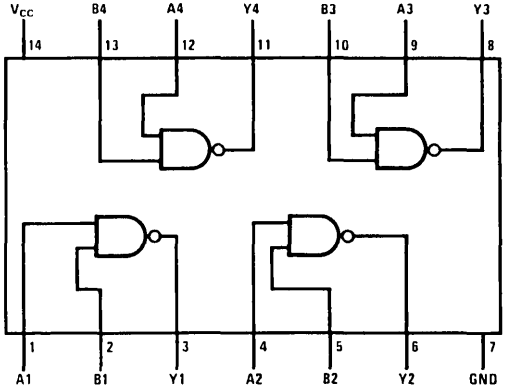
DM54S00/DM74S00 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6489–1

Order Number DM54S00J, DM74S00M or DM74S00N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S00			DM74S00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			10	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			20	36	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	4.5	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5	2	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time and the duration should not exceed one second.

National Semiconductor Corporation

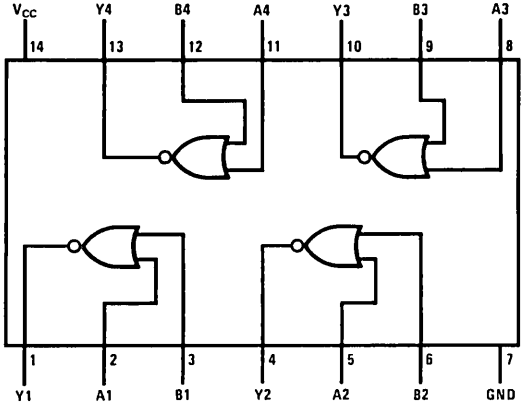
DM54S02/DM74S02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



TL/F/6490–1

Order Number DM54S02J or DM74S02N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S02			DM74S02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			17	29	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			26	45	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	1.5	5.5	2	7.5	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	1.5	5.5	2	7.5	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54S03/DM74S03 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

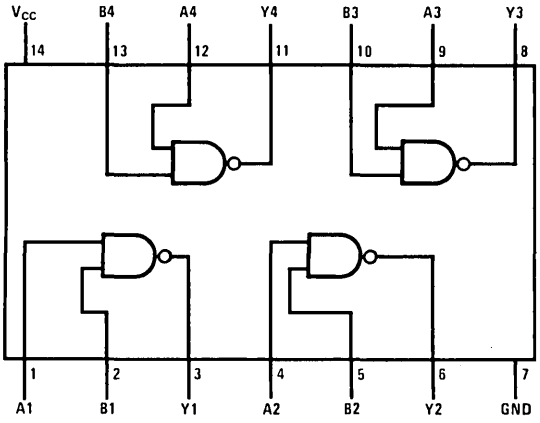
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6491–1

Order Number DM54S03J or DM74S03N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S03			DM74S03			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		6.0	13.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		20	36	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	7.5	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	3	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

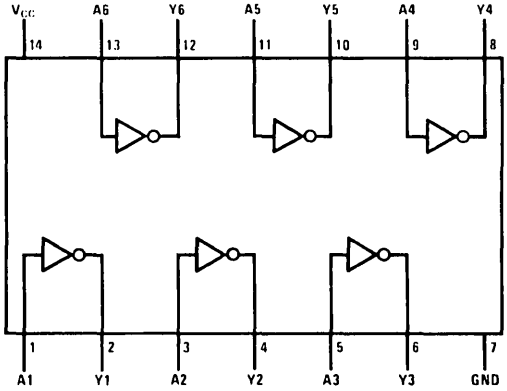
DM54S04/DM74S04 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

Connection Diagram

Dual-In-Line Package



TL/F/6442–1

Order Number DM54S04J, DM74S04M or DM74S04N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S04			DM74S04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			15	24	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			30	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	4.5	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5	2	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54S05/DM74S05 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

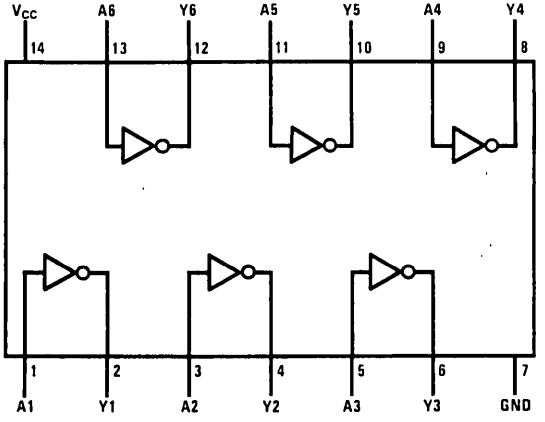
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6443–1

Order Number DM54S05J, DM74S05M or DM74S05N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S05			DM74S05			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		9	19.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		30	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	7.5	3	11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	3	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

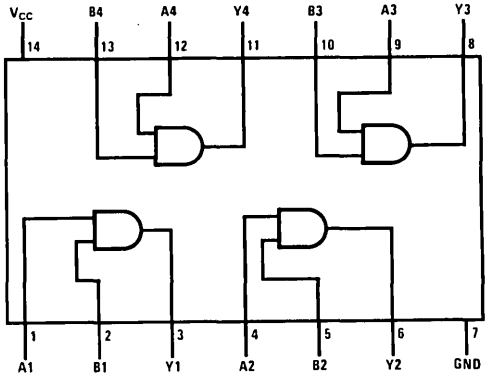
DM54S08/DM74S08 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

Connection Diagram

Dual-In-Line Package



TL/F/6444–1

Order Number DM54S08J or DM74S08N
See NS Package Number J14A or N14A

Function Table

Y = AB

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S08			DM74S08			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			18	32	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			32	57	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2.5	7	3	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2.5	7.5	3	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54S09/DM74S09 Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require an external pull-up resistor for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

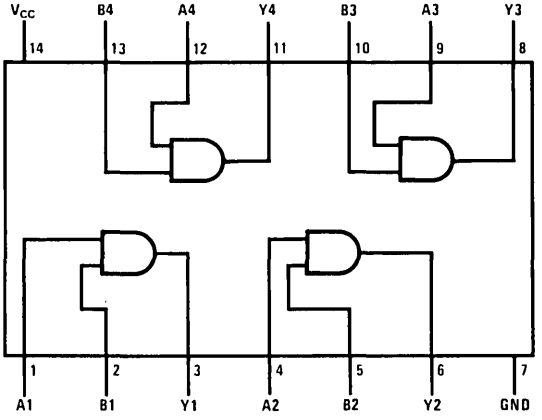
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6465–1

Order Number DM54S09J or DM74S09N
See NS Package Number J14A or N14A

Function Table

$$Y = AB$$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S09			DM74S09			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.2	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V			50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−2	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		18	32	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		32	57	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	3	10	4	18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	3	10	4	18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

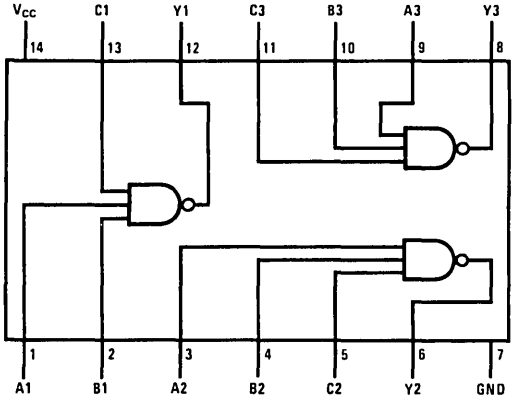
DM54S10/DM74S10 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6446–1

Order Number DM54S10J or DM74S10N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S10			DM74S10			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			7.5	12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			15	27	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	4.5	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5	2	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

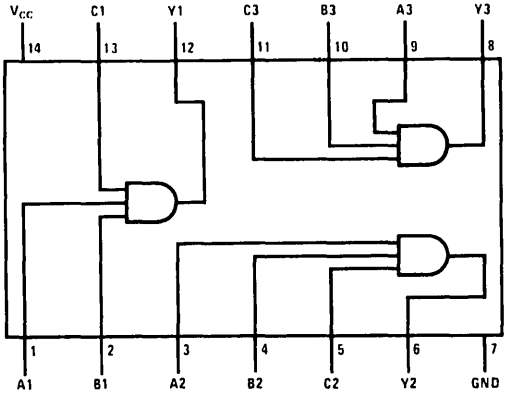
DM54S11/DM74S11 Triple 3-Input AND Gates

General Description

This device contains three independent gates each of which performs the logic AND function.

Connection Diagram

Dual-In-Line Package



TL/F/6447–1

Order Number DM54S11J or DM74S11N
See NS Package Number J14A or N14A

Function Table

$Y = ABC$

Inputs			Output
A	B	C	Y
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S11			DM74S11			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			13.5	24	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			24	42	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2.5	7	3	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2.5	7.5	3	11	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

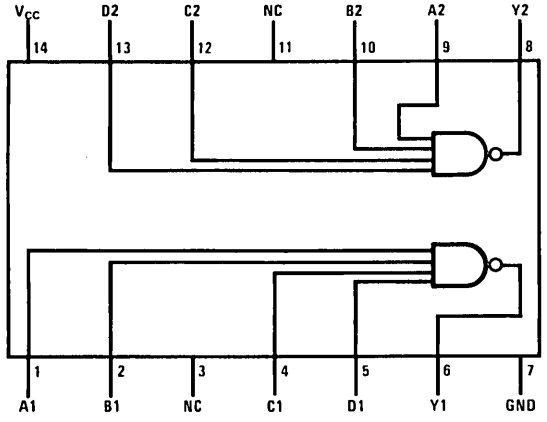
DM54S20/DM74S20 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6449–1

Order Number DM54S20J or DM74S20N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S20			DM74S20			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			5	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			10	18	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (see Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	4.5	2	7	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5	2	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

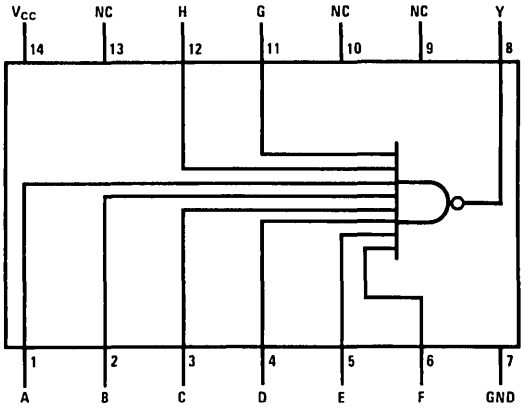
DM54S30/DM74S30 8-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6451–1

Order Number DM54S30J or DM74S30N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S30			DM74S30			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3	5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			5.5	10	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	6	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	3	10	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

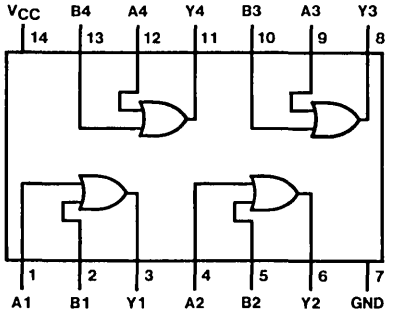
DM54S32/DM74S32 Quad 2-Input OR Gates

General Description

This device contains four independent gates each of which performs the logic OR function.

Connection Diagram

Dual-In-Line Package



TL/F/6452–1

Order Number DM54S32J or DM74S32N
See NS Package Number J14A or N14A

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S32			DM74S32			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			18	32	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			38	68	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	7	2	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	2	9	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

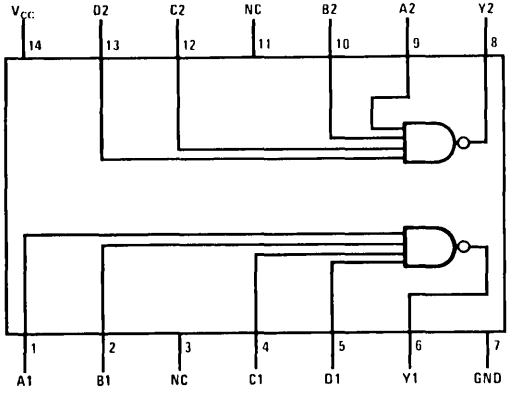
DM54S40/DM74S40 Dual 4-Input NAND Buffers

General Description

This device contains two independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6453–1

Order Number DM54S40J or DM74S40N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{ABCD}$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S40			DM74S40			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−3			−3	mA
I_{OL}	Low Level Output Current			60			60	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			10	18	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			25	44	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 93Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	6.5	3	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	6.5	3	9	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

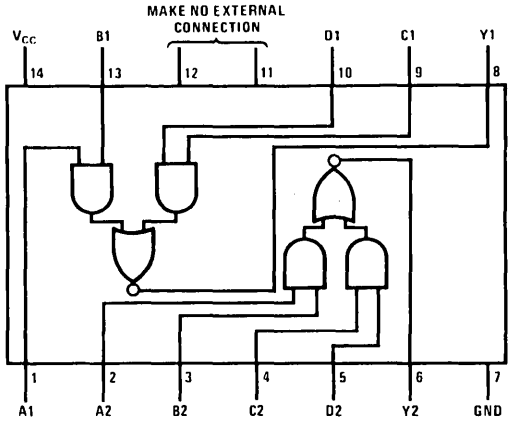
DM54S51/DM74S51 Dual 2-Wide 2-Input AND-OR-INVERT Gates

General Description

This device contains two independent combinations of gates each of which performs the logic AND-OR-INVERT function.

Connection Diagram

Dual-In-Line Package



TL/F/6454–1

Order Number DM54S51J or DM74S51N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{AB + CD}$$

Inputs				Output
A	B	C	D	Y
H	H	X	X	L
X	X	H	H	L
All other combinations				H

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S51			DM74S51			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8.2	17.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			14	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	5.5	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5.5	3	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

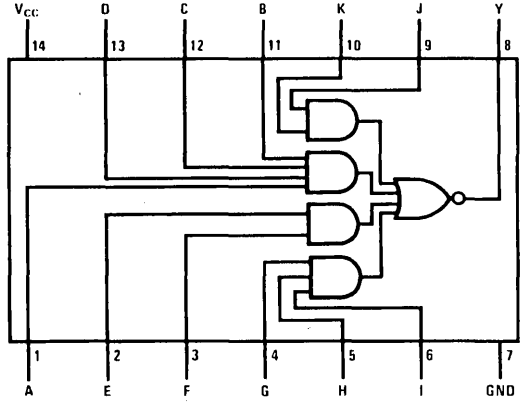
DM54S64/DM74S64 4-Wide AND-OR-INVERT Gates

General Description

This device contains a combination of gates which performs the logic AND-OR-INVERT function.

Connection Diagram

Dual-In-Line Package



TL/F/6455–1

Order Number DM54S64J or DM74S64N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{ABCD + EF + GHI + JK}$$

Inputs											Output
A	B	C	D	E	F	G	H	I	J	K	Y
H	H	H	H	X	X	X	X	X	X	X	L
X	X	X	X	H	H	X	X	X	X	X	L
X	X	X	X	X	X	H	H	H	X	X	L
X	X	X	X	X	X	X	X	X	H	H	L
All other combinations											H

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S64			DM74S64			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			7	12.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			8.5	16	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	5.5	3	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	5.5	3	8	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

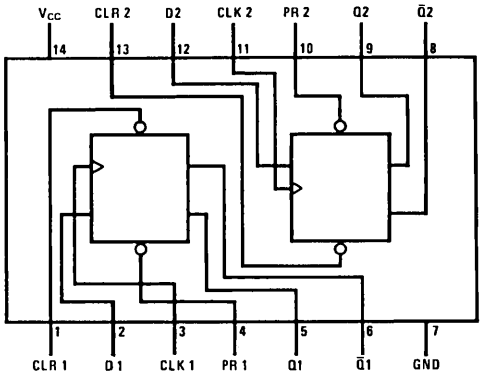
DM54S74/DM74S74
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6457–1

Order Number DM54S74J, DM74S74M or DM74S74N
See NS Package Number J14A, M14A or N14A

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↑ = Positive-going Transition
* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (high) level.
Q_0 = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S74			DM74S74			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	110	75	0	110	75	MHz
f_{CLK}	Clock Frequency (Note 3)		0	95	65	0	95	65	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	7.3			7.3			
		Clear Low	7			7			
		Preset Low	7			7			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	9			9			
		Clear Low	9			9			
		Preset Low	9			9			
t_{SU}	Setup Time (Notes 1 & 2)		3↑			3↑			ns
t_{SU}	Setup Time (Notes 1 & 3)		3↑			3↑			ns
t_H	Input Hold Time (Notes 1 & 2)		2↑			2↑			ns
t_H	Input Hold Time (Notes 1 & 3)		2↑			2↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge at the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	D			50	μA
			Clear			150	
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	D			−2	mA
			Clear			−6	
			Preset			−4	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		75		65		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		6		9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		6		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock High)	Preset to $\overline{Q}$		13.5		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock Low)	Preset to $\overline{Q}$		8		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock High)	Clear to Q		13.5		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Clock Low)	Clear to Q		8		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		9		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		9		13	ns

National Semiconductor Corporation

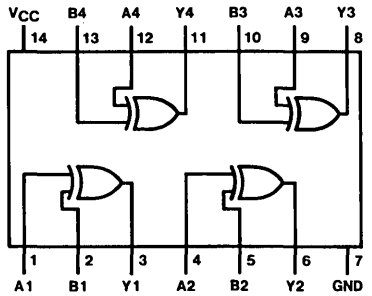
DM54S86/DM74S86 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic Exclusive-OR function.

Connection Diagram

Dual-In-Line Package



TL/F/6458–1

Order Number DM54S86J or DM74S86N
See NS Package Number J14A or N14A

Function Table

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S86			DM74S86			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			35	50	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			50	75	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		10.5		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			10		13	ns

National Semiconductor Corporation

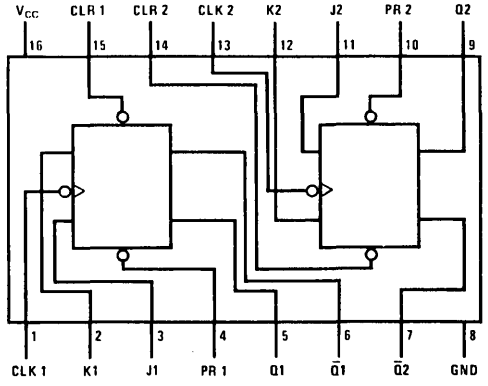
DM54S112/DM74S112 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs can be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6459–1

Order Number DM54S112J or DM74S112N
See NS Package Number J16A or N16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↓ = Negative going edge of pulse.

Q_0 = The output logic level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (high) level.

Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S112			DM74S112			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	125	80	0	125	80	MHz
f_{CLK}	Clock Frequency (Note 3)		0	80	60	0	80	60	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	6.5			6.5			
		Clear Low	8			8			
		Preset Low	8			8			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	8			8			
		Clear Low	10			10			
		Preset Low	10			10			
t_{SU}	Setup Time (Notes 1 & 4)		7↓			7↓			ns
t_H	Input Hold Time (Notes 1 & 4)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge at the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			50	μA
			Clear			100	
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V (Note 4)	J, K			−1.6	mA
			Clear			−7	
			Preset			−7	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Note 4: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		80		60		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		7		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		7		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		7		12	ns

National Semiconductor Corporation

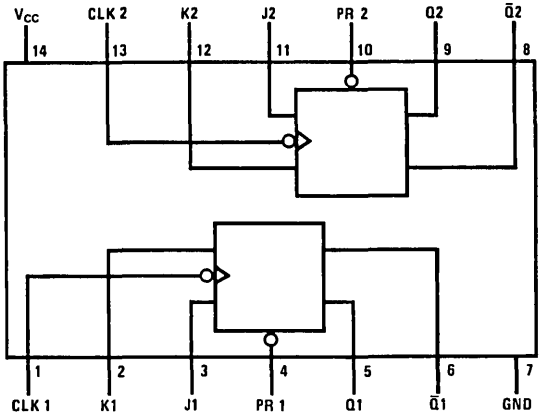
DM54S113/DM74S113 Dual Negative-Edge-Triggered Master-Slave J-K Flip-Flops with Preset and Complementary Outputs

General Description

This device contains two independent negative-edge-triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops on the falling edge of the clock pulse. The clock triggering occurs at a voltage level and is not directly related to the transition time of the negative going edge of the clock pulse. Data on the J and K inputs may be changed while the clock is high or low without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset input will set the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6460–1

Order Number DM54S113J or DM74S113N
See NS Package Number J14A or N14A

Function Table

Inputs				Outputs	
PR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	H	L
H	↓	L	L	Q_0	$\overline{Q}_0$
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	
H	H	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
↓ = Negative going edge of pulse.
Q_0 = The output logic level of Q before the indicated input conditions were established.
Toggle = Each output changes to the complement of its previous level on each falling edge of the clock pulse.

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S113			DM74S113			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	125	80	0	125	80	MHz
f_{CLK}	Clock Frequency (Note 3)		0	80	60	0	80	60	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	6.5			6.5			
		Preset Low	8			8			
t_W	Pulse Width (Note 3)	Clock High	8			8			ns
		Clock Low	8			8			
		Preset Low	10			10			
t_{SU}	Setup Time (Notes 1 & 4)		7↓			7↓			ns
t_H	Input Hold Time (Notes 1 & 4)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge at the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	J, K			50	μA
			Preset			100	
			Clock			100	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	J, K			−1.6	mA
			Preset			−7	
			Clock			−4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			30	50	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		80		60		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		7		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		7		12	ns

National Semiconductor Corporation

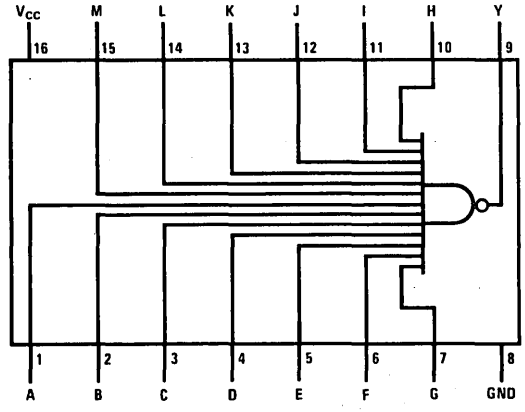
DM54S133/DM74S133 13-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6462–1

Order Number DM54S133J, DM74S133M or DM74S133N
See NS Package Number J16A, M14A or N16A

Function Table

$Y = \overline{ABCDEFGHIJKLM}$

Inputs	Output
A thru M	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S133			DM74S133			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3	5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			5.5	10	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 280Ω				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	6	2	8	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	7	3	10	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM54S138/DM74S138, DM54S139/DM74S139 Decoders/Demultiplexers

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The S138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The S139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

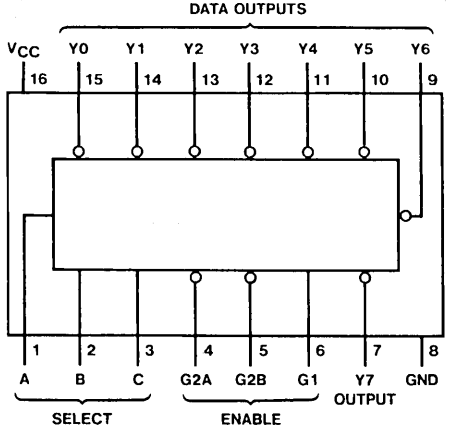
All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  Memory decoders
  Data transmission systems
- S138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- S139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay time (3 levels of logic)
  S138 8 ns
  S139 7.5 ns
- Typical power dissipation
  S138 245 mW
  S139 300 mW

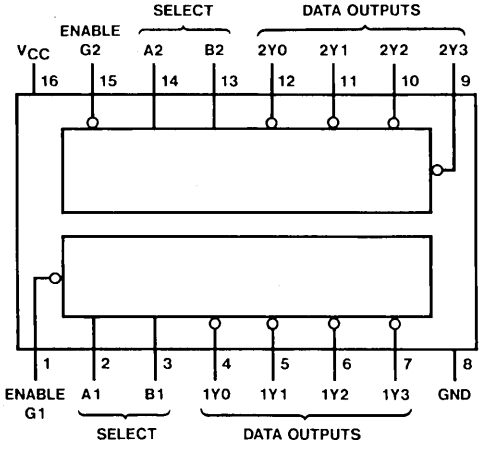
Connection Diagrams

Dual-in-Line Package



TL/F/6466–1

Dual-in-Line Package



TL/F/6466–2

Order Number DM54S138J, DM54S139J, DM74S138N or DM74S139N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55° C to +125°C
DM74S	0° C to +70°C
Storage Temperature Range	−65° C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S138,S139			DM74S138,S139			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current (S138)	V_{CC} = Max (Note 3)			49	74	mA
I_{CC}	Supply Current (S139)	V_{CC} = Max (Note 3)			60	90	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs enabled and open.

'S138 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	Levels of Delay	R_L = 280Ω				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	2		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	2		10.5		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	3		12		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	3		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	2		8		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	2		11		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	3		11		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	3		11		14	ns

'S139 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) to (Output)	Levels of Delay	R_L = 280Ω				Units
				C_L = 15 pF		C_L = 50 pF		
				Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	2		7.5		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	2		10		13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output	3		12		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output	3		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output	2		8		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output	2		10		13	ns

Function Tables

S138

Inputs					Outputs							
Enable		Select										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

* G2 = G2A + G2B

H = high level, L = low level, X = don't care (either low or high logic level)

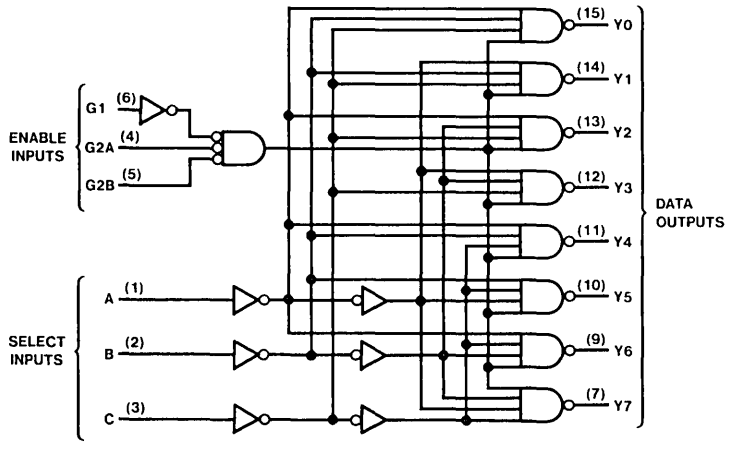
S139

Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = high level, L = low level, X = don't care (either low or high logic level)

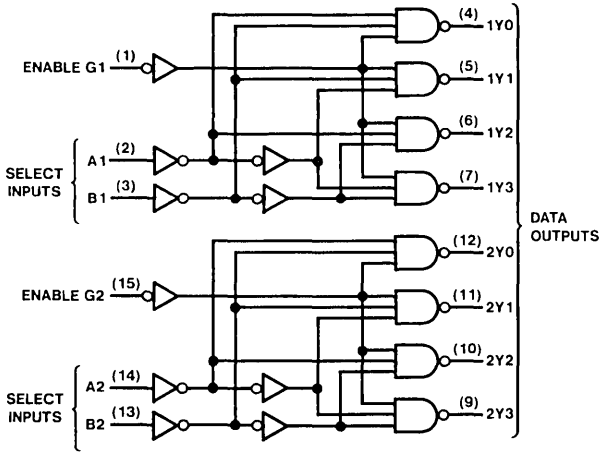
Logic Diagrams

S138



TL/F/6466–3

S139



TL/F/6466–4

3

National Semiconductor Corporation

DM54S140/DM74S140
Dual 4-Input NAND 50Ω Line Driver

General Description

This device contains two independent line driver gates each of which performs the logic NAND function.

Absolute Maximum Ratings (Note)

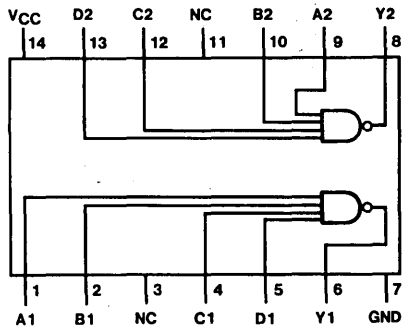
Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Connection Diagram

Dual-In-Line Package



TL/F/6487–1

Order Number DM54S140J or DM74S140N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54S140			DM74S140			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−40			−40	mA
I_{OL}	Low Level Output Current			60			60	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = Max, I_{OH} = Max	DM54	2.5	3.4		V
			DM74	2.7	3.4		
		V_{IL} = 0.5V, R_O = 50Ω to GND		2.0			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−50		−225	mA
			DM74	−50		−225	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			10	18	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			25	44	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 93Ω				Units
		C_L = 50 pF		C_L = 150 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	2	6.5	3	9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	2	6.5	3	9	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

3

National Semiconductor Corporation

DM54S151/DM74S151 1 of 8 Data Selector/Multiplexer with Complementary Outputs

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The S151 selects one-of-eight data sources. The S151 has a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the Y output low.

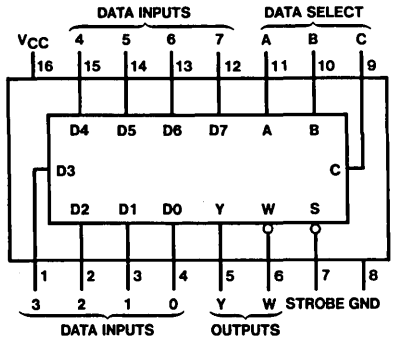
The S151 features complementary W and Y outputs.

Features

- Select one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output 4.5 ns
- Typical power dissipation 225 mW

Connection Diagram

Dual-In-Line Package



TL/F/6468–1

Order Number DM54S151J or DM74S151N
See NS Package Number J16A or N16A

Function Table

Inputs				Outputs	
Select			Strobe	Y	W
C	B	A	S		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = high level, L = low level, X = don't care

D0, D1 . . . D7 = the level of the respective D input

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S151			DM74S151			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

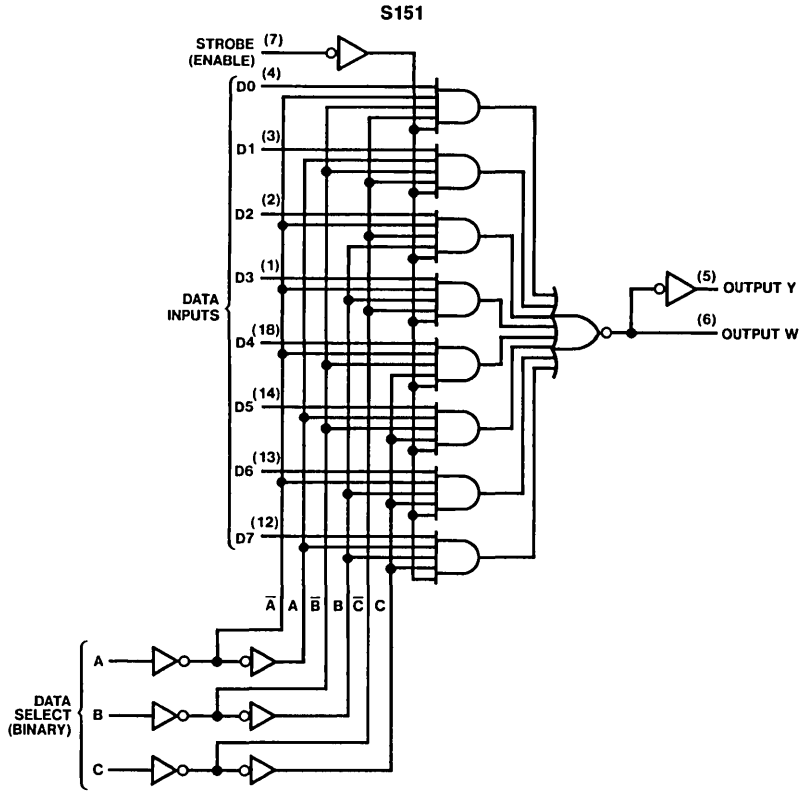
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y (4 Levels)		18		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y (4 Levels)		18		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to W (3 Levels)		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to W (3 Levels)		13.5		17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		16.5		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		18		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to W		13		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to W		12		16	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to Y		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to Y		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0 thru D7 to W		7		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0 thru D7 to W		7		10	ns

Logic Diagram



TL/F/6468–2

National Semiconductor Corporation

DM54S153/DM74S153 Dual 1 of 4 Line Data Selectors/Multiplexers

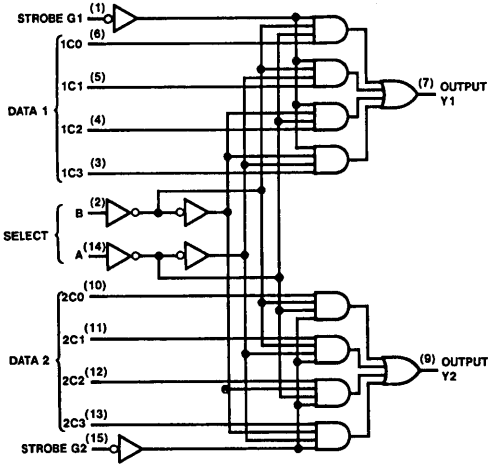
General Description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

Features

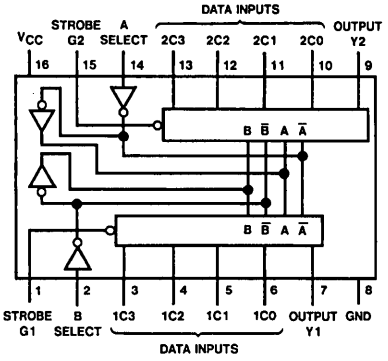
- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times
  - From data 6 ns
  - From strobe 9.5 ns
  - From select 12 ns
- Typical power dissipation 225 mW

Logic and Connection Diagrams



TL/F/6469–1

Dual-In-Line Package



TL/F/6469–2

Order Number DM54S153J or DM74S153N
See NS Package Number J16A or N16A

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperture Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S153			DM74S153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		9		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		9		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		18		21	ns
t_{PLH}	Propagtion Delay Time Low to High Level Output	Strobe to Y		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		13.5		17	ns

National Semiconductor Corporation

DM54S157/DM74S157, DM54S158/DM74S158 Quad 1 of 2 Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. The S157 presents true data whereas the S158 presents inverted data to minimize propagation delay time.

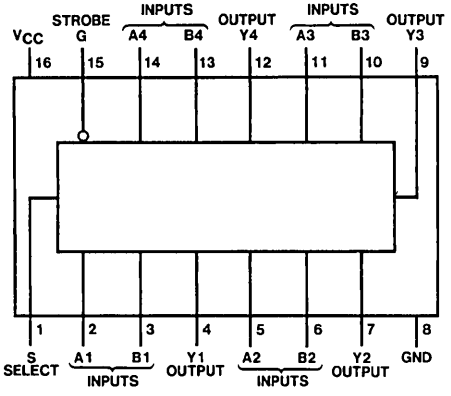
Features

- Buffered inputs and outputs
- Typical propagation time
  S157 5 ns
  S158 4 ns
- Typical power dissipation
  S157 250 mW
  S158 195 mW

Applications

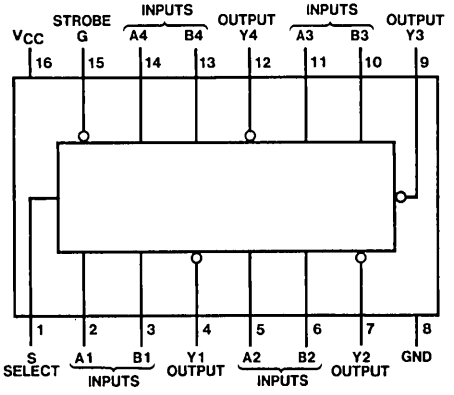
- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Connection Diagrams (Dual-In-Line Packages)



TL/F/6470–1

Order Number DM54S157J or DM74S157N
See NS Package Number J16A or N16A



TL/F/6470–2

Order Number DM54S158J or DM74S158N
See NS Package Number J16A or N16A

Function Table

Inputs				Output Y	
Strobe	Select	A	B	S157	S158
H	X	X	X	L	H
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S157			DM74S157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S157 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	S or G			100	µA
			A or B			50	
I_{IL}	High Level Input Current	V_{CC} = Max, V_I = 0.5V	S or G			−4	mA
			A or B			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	78	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured 4.5V applied to all inputs and all outputs open.

'S157 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		7.5		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		6.5		10	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		12.5		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		15		17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		15		17	ns

Recommended Operating Conditions

Symbol	Parameter	DM54S158			DM74S158			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S158 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	S or G			100	μA
			A or B			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	S or G			−4	mA
			A or B			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			39	61	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)				81	mA

'S158 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		6		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		6		9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		11.5		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		12		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		12		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

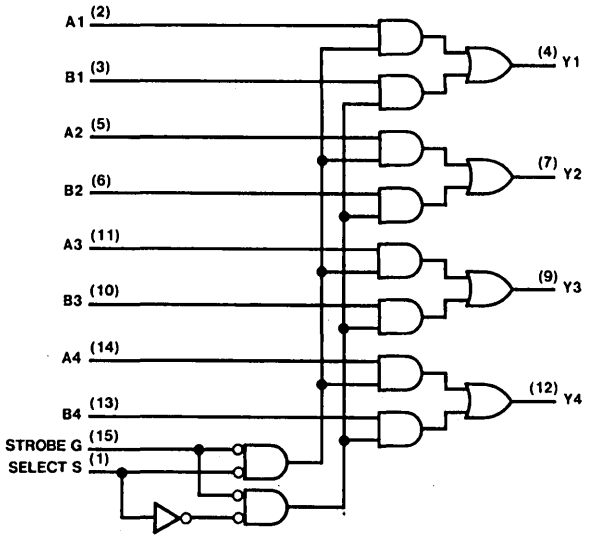
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open and all inputs at 4.5V.

Note 4: I_{CC2} is measured with B, G, and S inputs grounded, A inputs at 4.5V, and all outputs open.

Logic Diagrams

S157



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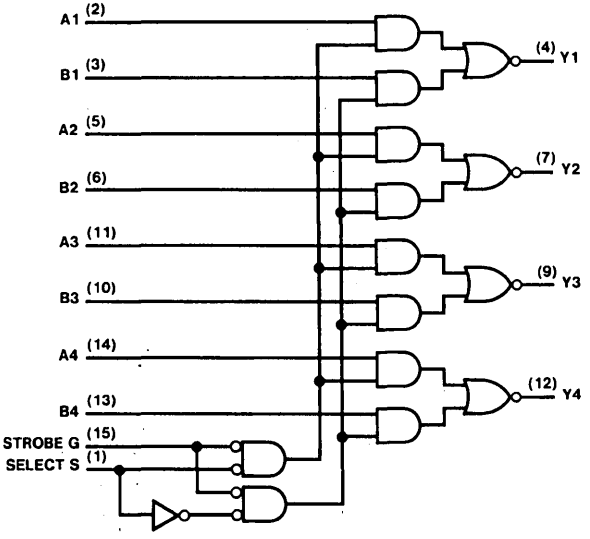
S158



TL/F/6470–4

3

National Semiconductor Corporation

DM54S161/DM74S161, DM54S163/DM74S163 Synchronous 4-Bit Binary Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. They are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input.

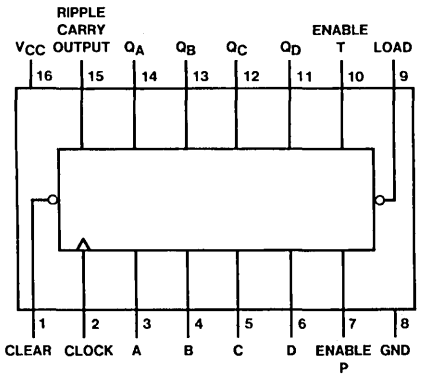
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

Connection Diagram

Dual-In-Line Package



TL/F/6471–1

Order Number DM54S161J, DM54S163J, DM74S161N, or DM74S163N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions See Section 1 for Test Waveforms and Output Load

Symbol	Parameter		DM54S161/163			DM74S161/163			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0		40	0		40	MHz
	Clock Frequency (Note 2)		0		35	0		35	
t_w	Pulse Width (Note 1)	Clock	10			10			ns
		Clear (Note 4)	10			10			
	Pulse Width (Note 2)	Clock	12			12			
		Clear (Note 4)	12			12			
t_{SU}	Setup Time (Note 1)	Data	4			4			ns
		Enable P or T	12			12			
		Load	14			14			
		Clear (Note 3)	14			14			
	Setup Time (Note 2)	Data	5			5			
		Enable P or T	14			14			
		Load	16			16			
		Clear (Note 3)	16			16			
t_H	Hold Time (Note 1)	Data	3			3			ns
		Others	0			0			
	Hold Time (Note 2)	Data	5			5			
		Others	2			2			
t_{REL}	Load or Clear Release Time (Note 1)		12			12			ns
	Load or Clear Release Time (Note 2)		14			14			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: Applies only to the 'S163 which has synchronous clear inputs.

Note 4: Applies only to the 'S161 which has asynchronous clear inputs.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	Low Level Input Current	V_{CC} = Max, V_I = 2.7V	CLK, Data			50	µA
			Others	−10		−200	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Enable T			−4	mA
			Others			−2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			95	160	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		40		35		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		25		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		25		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		15		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		15		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 3)	Clear to Any Q		20		24	ns

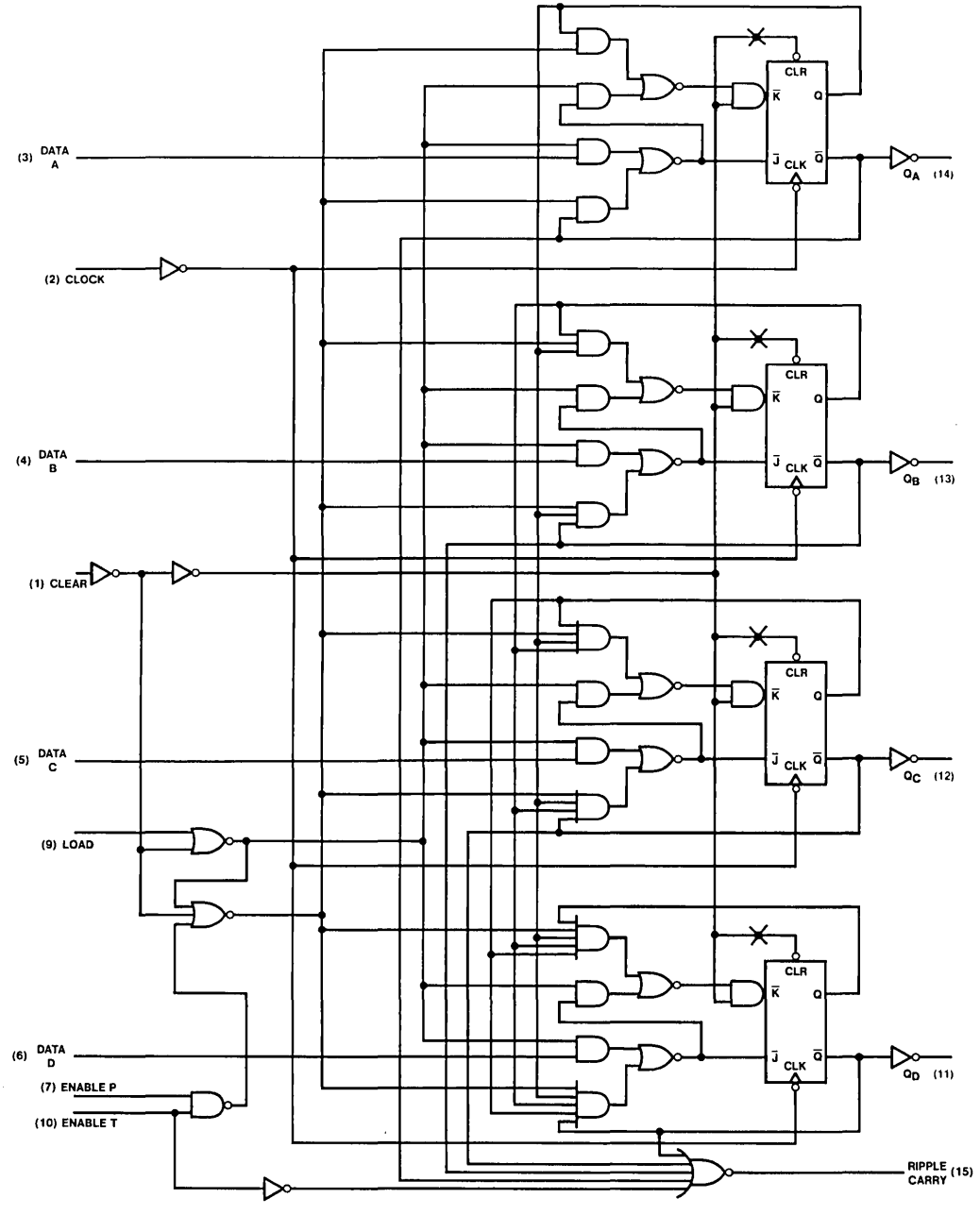
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: Propagation delay for clearing is measured from clear input for the 'S161 and from the clock input transition for the 'S163.

Logic Diagram

S161, S163

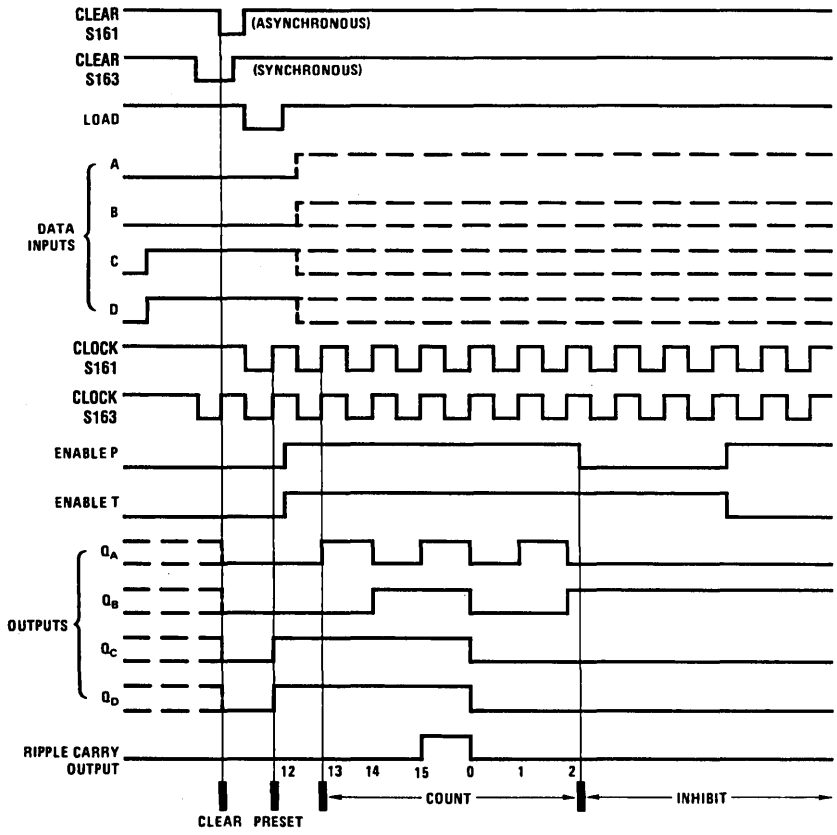


✕ S161 option

TL/F/6471–2

Timing Diagram

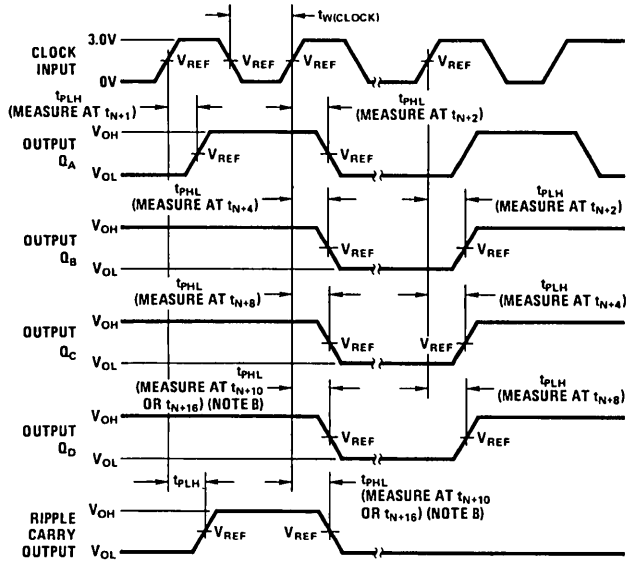
S161, S163 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



TL/F/6471–3

Parameter Measurement Information

Switching Time Waveforms



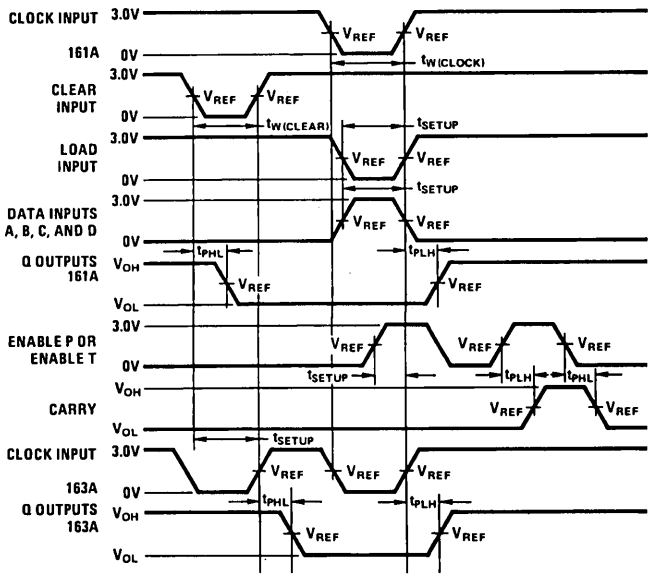
TL/F/6471–4

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For S161/163, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at $t_n + 16$ for S161, S163 where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5V$.

Switching Time Waveforms



TL/F/6471–5

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at $t_n + 0$.

Note C: $V_{REF} = 1.5V$.

National Semiconductor Corporation

DM54S174/DM74S174, DM54S175/DM74S175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) versions feature complementary outputs from each flip-flop.

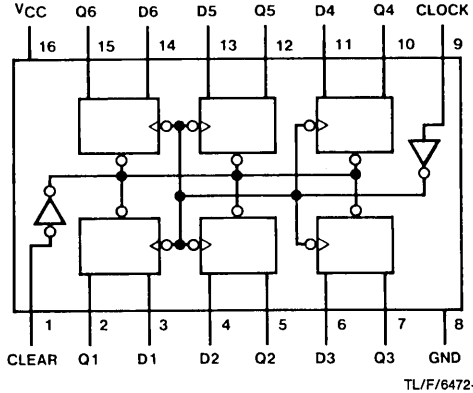
Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- S174 contain six flip-flops with single-rail outputs.
- S175 contain four flip-flops with double-rail outputs.
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 110 MHz
- Typical power dissipation per flip-flop 75mW

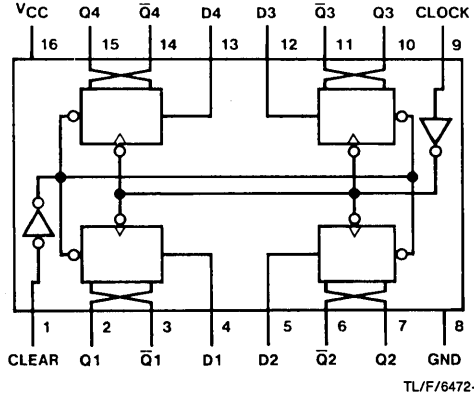
Connection Diagrams

Dual-In-Line Package



TL/F/6472–1

Dual-In-Line Package



TL/F/6472–2

Order Number DM54S174J, DM54S175J, DM74S174N or DM74S175N
See NS Package Number J16A or N16A

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = S175 only

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions See Section 1 for Test Waveforms and Output Load

Symbol	Parameter		DM54S174			DM74S175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0	110	75	0	110	75	MHz
f_{CLK}	Clock Frequency (Note 2)		0	90	65	0	90	65	MHz
t_w	Pulse Width (Note 1)	Clock	7			7			ns
		Clear	10			10			
	Pulse Width (Note 2)	Clock	9			9			
		Clear	12			12			
t_{SU}	Data Setup Time (Note 1)		5			5			ns
	Data Setup Time (Note 2)		7			7			
t_H	Data Hold Time (Note 1)		3			3			ns
	Data Hold Time (Note 2)		5			5			
t_{REL}	Clear Release Time (Note 1)		5			5			ns
	Clear Release Time (Note 2)		7			7			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current (S174)	V_{CC} = Max (Note 3)			90	144	mA
I_{CC}	Supply Current (S175)	V_{CC} = Max (Note 3)			60	96	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		75		65		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		17		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (S175 Only)	Clear to $\overline{Q}$		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		22		23	ns

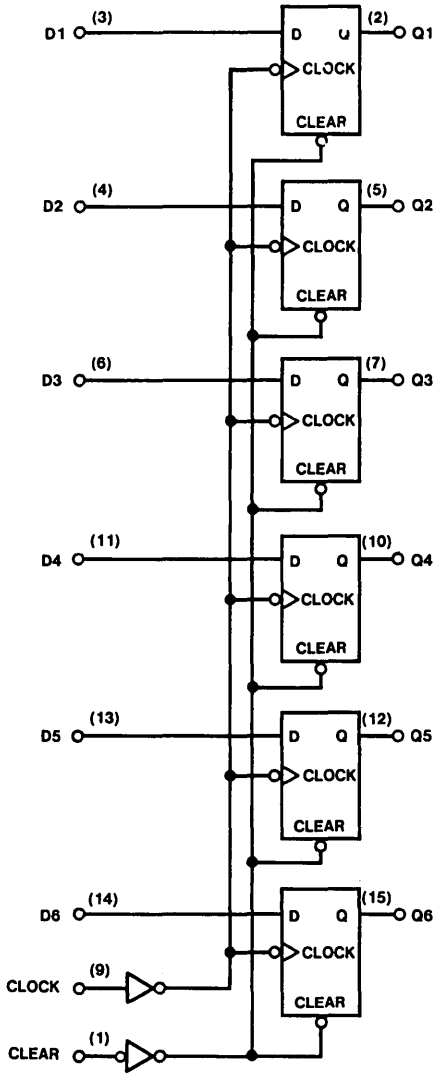
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: With all outputs open and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

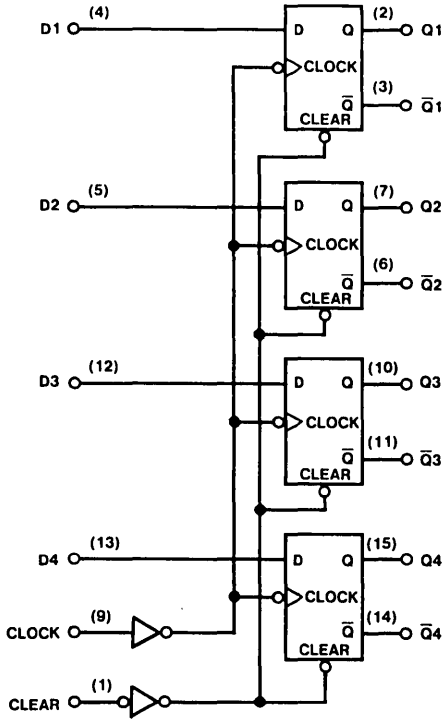
Logic Diagrams

S174



TL/F/6472-3

S175



TL/F/6472-4

National Semiconductor Corporation

DM54S181/DM74S181 Arithmetic Logic Unit/Function Generators

General Description

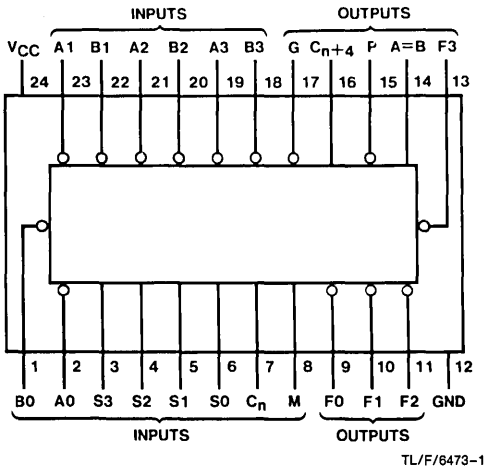
These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54S182/DM74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182/DM74S182. (Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words

Connection Diagram

Dual-In-Line Package



TL/F/6473–1

Order Number DM54S181J or DM74S181N
See NS Package Number J24A or N24A

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The S181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requriements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The DM54S181/DM74S181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

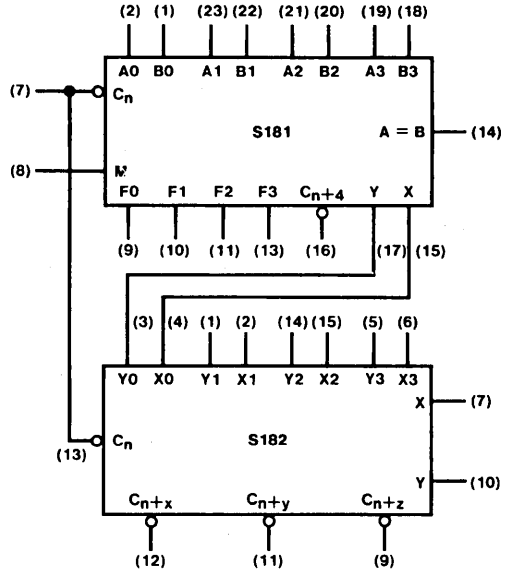
Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_n+4$	X	Y
Active-Low Data (Table II)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_n+4	$\overline{P}$	$\overline{G}$

Input C_n	Output C_n+4	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A ≤ B	A ≤ B
H	L	A ≤ B	A ≤ B
L	H	A ≤ B	A ≤ B
L	L	A ≤ B	A ≤ B

3

General Description (Continued)



TL/F/6473–2

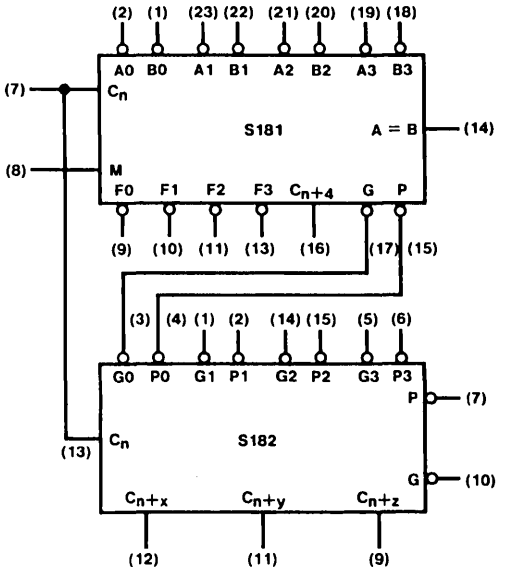
FIGURE 1

TABLE I

Selection				Active High Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	F = $\overline{A}$	F = A	F = A Plus 1
L	L	L	H	F = $\overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	F = $\overline{AB}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	F = $\overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	F = $\overline{A}$ + B	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	F = $\overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

General Description (Continued)



TL/F/6473–3

FIGURE 2

TABLE II

Selection				Active Low Data		
				M = H	M = L; Arithmetic Operations	
S3	S2	S1	S0	Logic Functions	C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A $\oplus$ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage (A = B Output)	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S181			DM74S181			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (A = B Output)			5.5			5.5	V
I_{OH}	High Level Output Current (All Except A = B)			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
I_{CEX}	High Level Output Current (A = B Output)	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OH}	High Level Output Voltage (All Except A = B)	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	Mode			50	μA
			A or B			150	
			S			200	
			Carry			250	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	Mode			−2	mA
			A or B			−6	
			S			−8	
			Carry			−10	
I_{OS}	Short Circuit Output Current (Any Output Except A = B)	V_{CC} = Max (Note 2)		−40		−100	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			120	220	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured for the following conditions: A. S0 through S3, M, and A inputs at 4.5V, all other inputs grounded and all outputs open. B. S0 through S3 and M inputs at 4.5V, all other inputs grounded and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	From (Input)	To (Output)	DM54/74 S181				Units
					R_L = 280Ω, C_L = 15 pF		R_L = 280Ω, C_L = 50 pF		
					Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output		C_n	C_n+4		10.5		14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					10.5		14	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any A or B	C_n+4		18.5		22	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					18.5		22	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	C_n+4		23		27	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					23		27	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ mode)	C_n	Any F		12		14	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12		14	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any A or B	G		12		15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12		15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	G		15		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					15		20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	Any A or B	P		12		15	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					12		15	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	P		15		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					15		20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)	A_i or B_i	F_i		16.5		20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					16.5		20	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	A_i or B_i	F_i		20		24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22		24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 4.5V (logic mode)	A_i or B_i	F_i		20		24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					22		24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)	Any A or B	A = B		23		26	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30		33	

Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase

$\overline{\text{SUM}}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

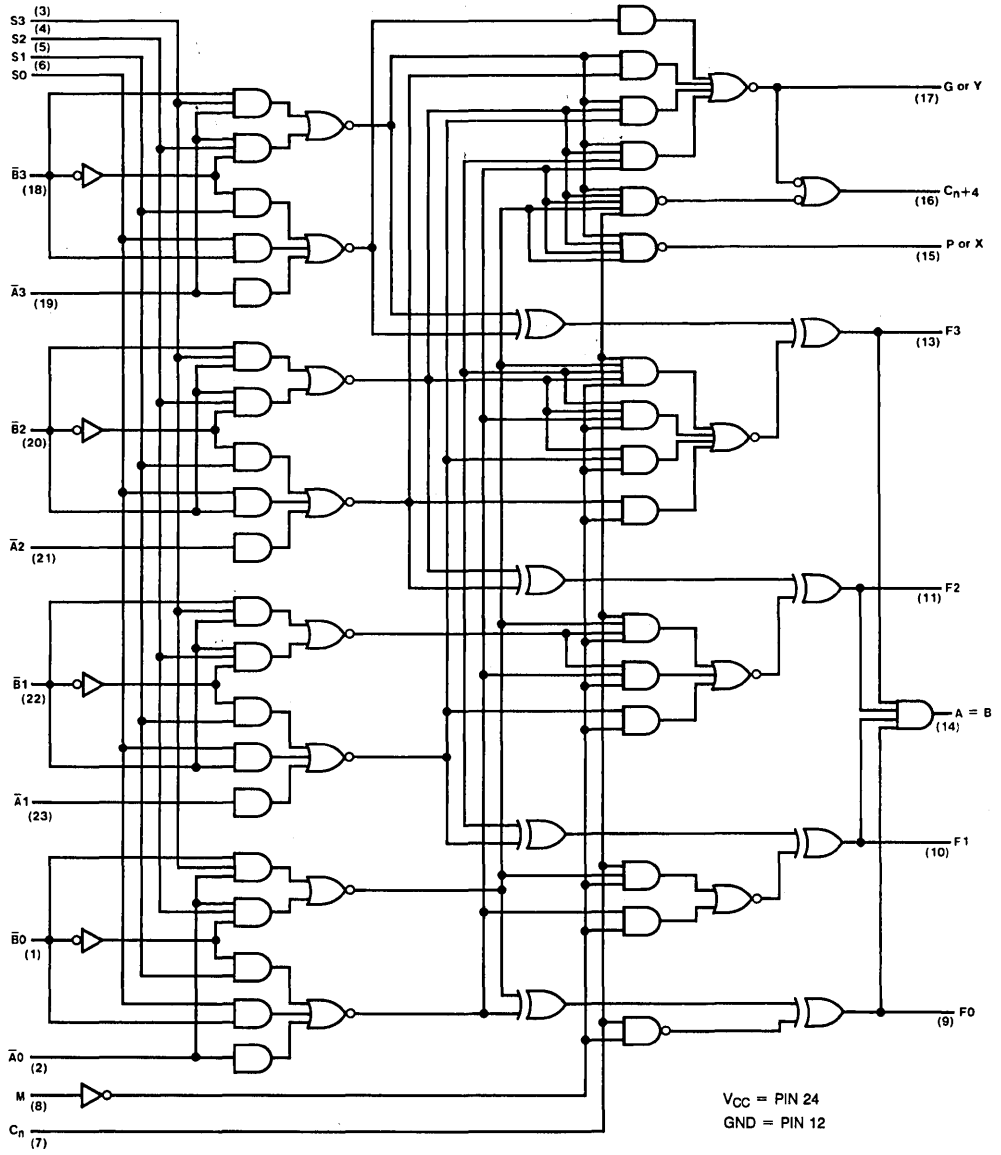
Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} / t_{PHL}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PLH} / t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

Parameter Measurement Information (Continued)

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A and B	None	C_n+4 or any F	In-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_n+4	In-Phase

Logic Diagram



TL/F/6473–4

National Semiconductor Corporation

DM54S182/DM74S182 Look-Ahead Carry Generators

General Description

These circuits are high-speed, look-ahead carry generators, capable of anticipating a carry across four binary adders or groups of adders. They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

When used in conjunction with the 181 arithmetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each S182 generates the look-ahead (anticipated carry) across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

Carry input and output of the ALU's are in their true form, and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry functions (inputs, outputs, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretations of carry functions, as explained on the 181 data sheet are also applicable to and compatible with the look-ahead generator. Positive logic equations for the S182 are:

$$C_{n+x} = \overline{G}0 + \overline{P}0\, C_n$$

$$C_{n+y} = \overline{G}1 + \overline{P}1\,\overline{G}0 + \overline{P}1\,\overline{P}0\, C_n$$

$$C_{n+z} = \overline{G}2 + \overline{P}2\,\overline{G}1 + \overline{P}2\,\overline{P}1\,\overline{G}0 + \overline{P}2\,\overline{P}1\,\overline{P}0\, C_n$$

$$\overline{G} = \overline{G}3\,(\overline{P}3 + \overline{G}2)\,(\overline{P}3 + \overline{P}2 + \overline{G}1)\,(\overline{P}3 + \overline{P}2 + \overline{P}1 + \overline{G}0)$$

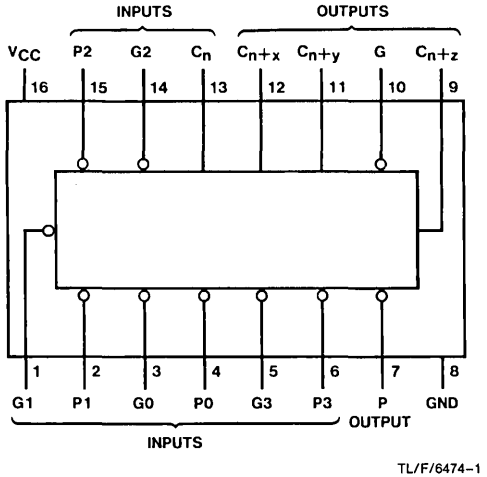
$$\overline{P} = \overline{P}3\,\overline{P}2\,\overline{P}1\,\overline{P}0$$

Features

- Typical propagation delay time 7 ns
- Typical power dissipation 260 mW

Connection Diagram

Dual-In-Line Package



TL/F/6474–1

Order Number DM54S182J or DM74S182N
See NS Package Number J16A or N16A

Pin Designations

Designation	Pin Nos.	Function
G0, G1, G2, G3	3, 1, 14, 5	Active Low Carry Generate Inputs
P0, P1, P2, P3	4, 2, 15, 6	Active Low Carry Propagate Inputs
C_n	13	Carry Input
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	Carry Outputs
G	10	Active Low Carry Generate Output
P	7	Active Low Carry Propagate Output
V_{CC}	16	Supply Voltage
GND	8	Ground

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S182			DM74S182			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	P0, P1 or G3			200	μA
			P3			100	
			P2			150	
			C_n			50	
			G0, G2			350	
			G1			400	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	P0, P1 or G3			−8	mA
			P3			−4	
			P2			−6	
			C_n			−2	
			G0, G2			−14	
			G1			−16	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54		39	55	mA
			DM74		39	55	
I_{CCL}	Supply Currents with Outputs Low	V_{CC} = Max (Note 4)	DM54		69	99	mA
			DM74		69	109	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

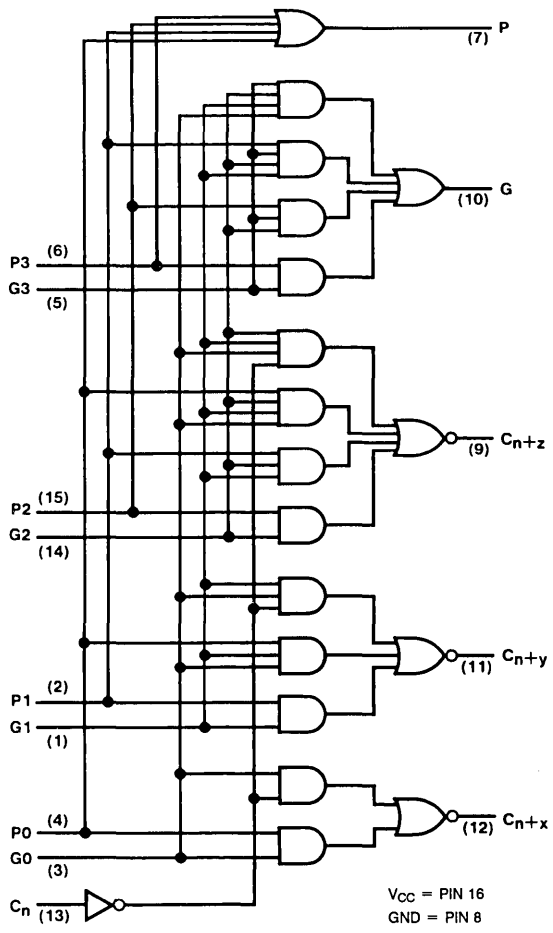
Note 3: I_{CCH} is measured with all outputs open, inputs P3 and G3 at 4.5V, and all other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open, inputs G0, G1, and G2 at 4.5V, and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Min	
t_{PLH}	Propagation Delay Time Low to High Level Output	GN or PN to $C_{n+x,y,z}$		7		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	GN or PN to $C_{n+x,y,z}$		7		11	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	GN or PN to G		7.5		11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	GN or PN to G		10.5		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	PN to P		6.5		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	PN to P		10		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C_n to to $C_{n+x,y,z}$		10		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C_n to to $C_{n+x,y,z}$		10.5		14	ns

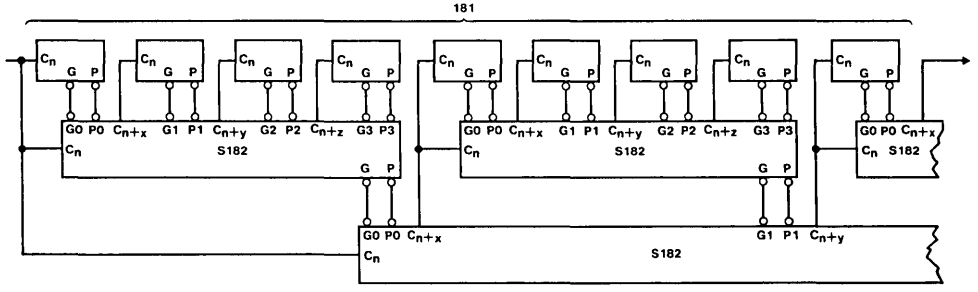
Logic Diagram



TL/F/6474-2

Typical Application

64-Bit ALU, Full-Carry Look Ahead in Three Levels



TL/F/6474-3

A and B inputs, and F outputs of 181 are not shown.

National Semiconductor Corporation

DM54S194/DM74S194
4-Bit Bidirectional Universal Shift Registers

General Description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register; they feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

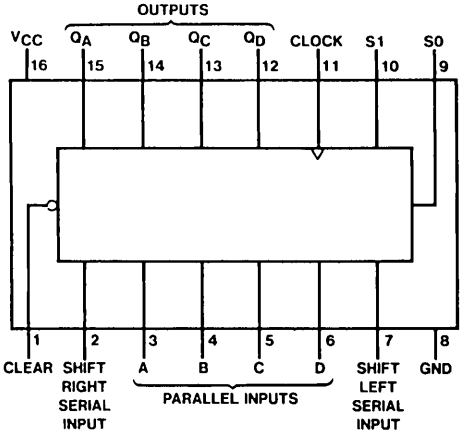
Clocking of the flip-flop is inhibited when both mode control inputs are low.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear
- Typical clock frequency 105 MHz
- Typical power dissipation 425 mW

Connection Diagram

Dual-In-Line Package



TL/F/6475–1

Order Number DM54S194J or DM74S194N
See NS Package Number J16A or N16A

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54S194			DM74S194			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0	105	70	0	105	70	MHz
f_{CLK}	Clock Frequency (Note 2)		0	90	60	0	90	60	MHz
t_W	Pulse Width (Note 3)	Clock	7			7			ns
		Clear	12			12			
t_{SU}	Setup Time (Note 3)	Mode	11			11			ns
		Data	5			5			
t_H	Hold Time (Note 3)		3			3			ns
t_{REL}	Clear Release Time (Note 3)		9			9			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			85	135	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR, and the SERIAL inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CLOCK.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		70		60		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		16.5		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		18.5		23	ns

Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state). L = Low Level (steady state). X = Don't Care (any input, including transitions).

↑ = Transition from low to high level.

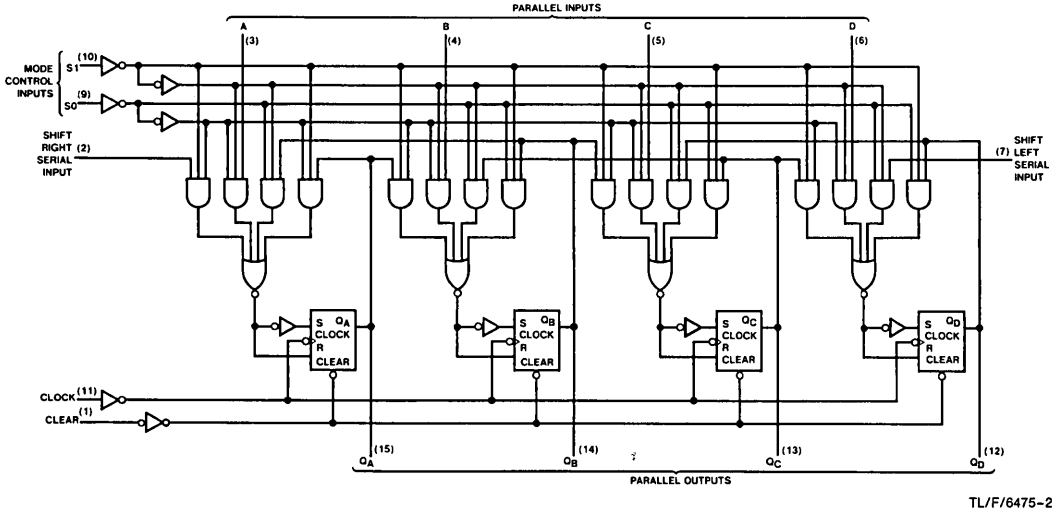
a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C respectively, before the most recent ↑ transition of the clock.

Logic Diagram

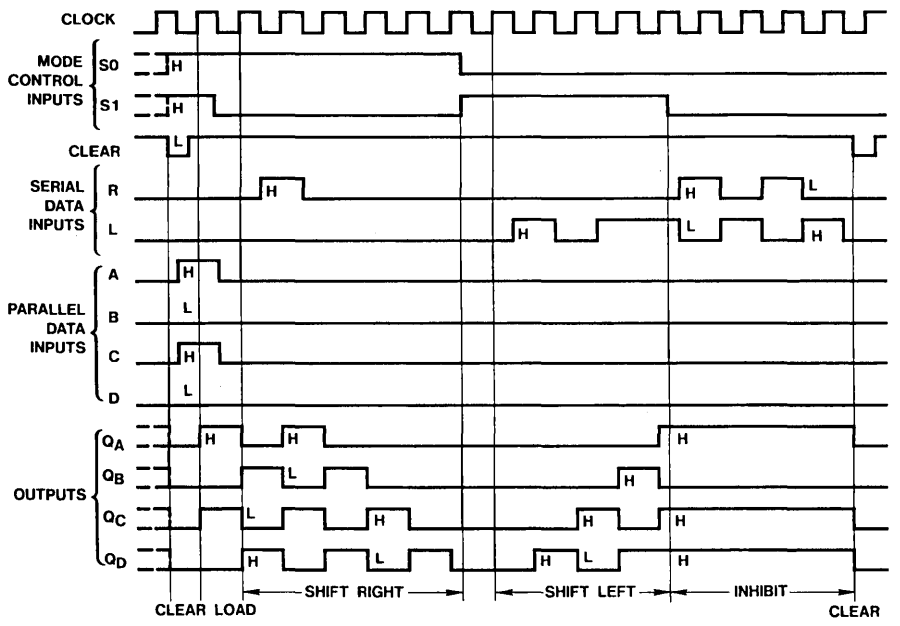
S194



TL/F/6475-2

Timing Diagram

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit, and Clear Sequences



TL/F/6475–3

National Semiconductor Corporation

DM54S195/DM74S195 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. All inputs are buffered to lower the input drive requirements. The registers have two modes of operation:

Parallel (broadside) load

Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D, or T-type flip-flop as shown in the truth table.

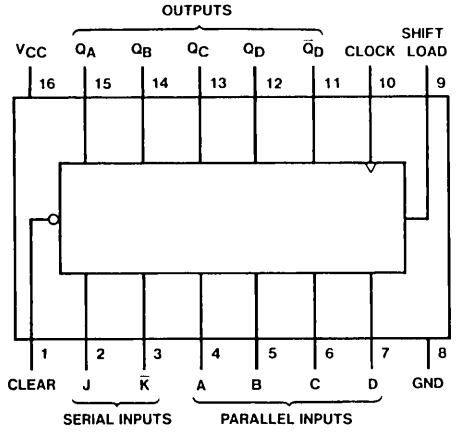
The high-performance S195, with a 105 MHz typical shift frequency, is particularly attractive for very high-speed data processing systems. In most cases existing systems can be upgraded merely by using this Schottky-clamped shift register.

Features

- Synchronous parallel load
- Positive-edge-triggered clocking
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- For use in high-performance:
  accumulators/processors
  serial-to-parallel, parallel-to-serial converters
- Typical clock frequency 105 MHz
- Typical power dissipation 350 mW

Connection Diagram

Dual-In-Line Package



TL/F/6476–1

Order Number DM54S195J or DM74S195N
See NS Package Number J16A or N16A

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54S195			DM74S195			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1			−1	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 1)		0	105	70	0	105	70	MHz
f_{CLK}	Clock Frequency (Note 2)		0	90	60	0	90	60	MHz
t_W	Pulse Width (Note 3)	Clock	7			7			ns
		Clear	12			12			
t_{SU}	Setup Time (Note 3)	Shift/Load	11			11			ns
		Data	5			5			
t_H	Data Hold Time (Note 3)		3			3			ns
t_{REL}	Shift/Load Release Time (Note 3)		6			6			ns
	Clear Release Time (Note 3)		9			9			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 2: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 6)			70	109	mA

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 6: With all inputs open, SHIFT/LOAD grounded, and 4.5V applied to the J, K, and data inputs, I_{CC} is measured by applying a momentary ground, then 4.5V to the CLEAR and then applying a momentary ground then 4.5V to the CLOCK.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		70		60		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		16.5		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		18.5		23	ns

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

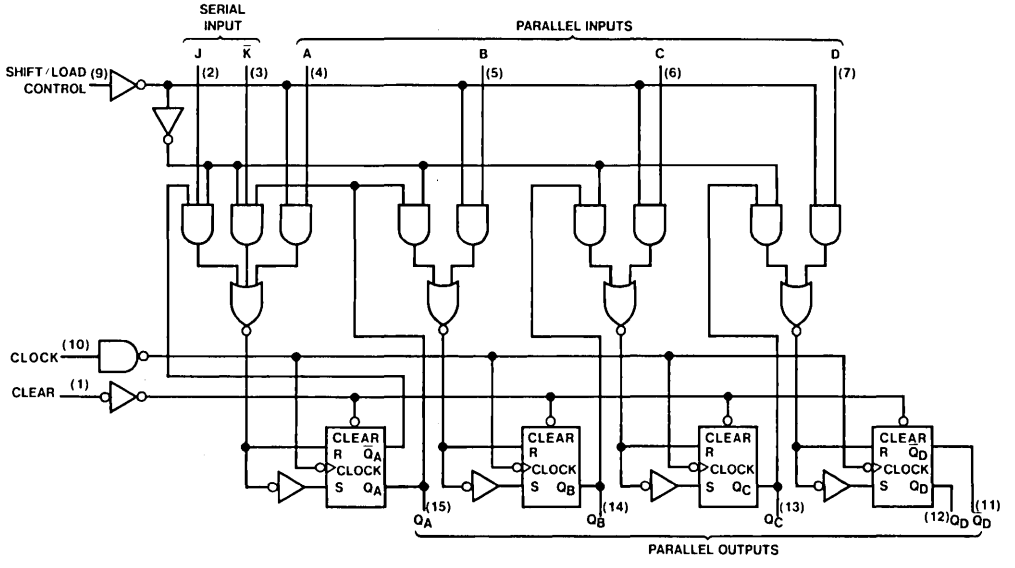
↑ = Transition from low to high level

a, b, c, d = The level of steady state input at A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent transition of the clock.

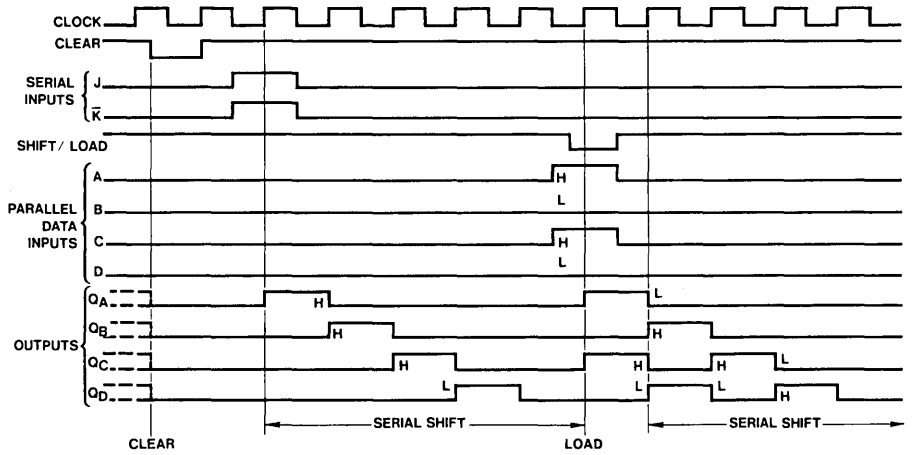
Logic Diagram



TL/F/6476–2

Timing Diagram

Typical Clear, Shift, and Load Sequences



TL/F/6476–3

National Semiconductor Corporation

DM54S240/DM74S240, DM54S241/DM74S241, DM54S244/DM74S244 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

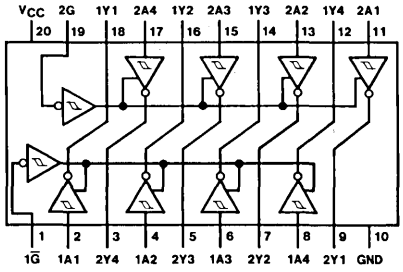
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  54S 48 mA
  74S 64 mA
- Typical I_{OH} (source current)
  54S −12 mA
  74S −15 mA
- Typical propagation delay times
  Inverting 4.5 ns
  Noninverting 6 ns
- Typical enable/disable times 9 ns
- Typical power dissipation (enabled)
  Inverting 450 mW
  Noninverting 538 mW

Connection Diagrams

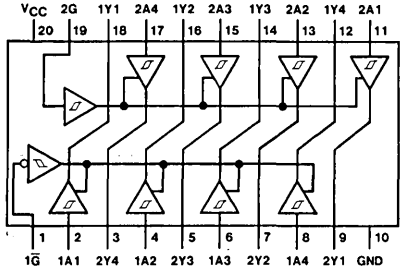
Dual-In-Line Package



TL/F/6478–1

Order Number DM54S240J, DM74S240WM or DM74S240N
See NS Package Number J20A, M14B or N20A

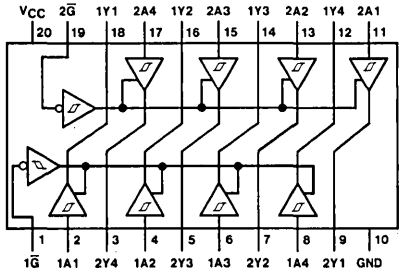
Dual-In-Line Package



TL/F/6478–2

Order Number DM54S241J or DM74S241N
See NS Package Number J20A or N20A

Dual-In-Line Package



TL/F/6478–3

Order Number DM54S244J, DM74S244WM or DM74S244N
See NS Package Number J20A, M14B or N20A

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S			DM74S			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.5	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			48			64	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
H_{ys}	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min		0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −1 mA	DM74	2.7			V
		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −3 mA		2.4	3.4		
		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.5V, I_{OH} = Max		2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = 0.8V, V_{IH} = 2V	DM54			0.55	V
			DM74			0.55	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V; V_O = 2.4V				50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied	V_{CC} = Max, V_{IL} = 0.8V, V_{IH} = 2V; V_O = 0.5V				−50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	Any A			−400	μA
			Any G			−2	mA

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−50		−225	mA
I_{CC}	Supply Current	Outputs High	DM54S240		80	123	mA
			DM74S240		80	135	
			DM54S241, 244		95	147	
			DM74S241, 244		95	160	
		Outputs Low	DM54S240		100	145	
			DM74S240		100	150	
			DM54S241, 244		120	170	
			DM74S241, 244		120	180	
		Outputs Disabled	DM54S240		100	145	
			DM74S240		100	150	
			DM54S241, 244		120	170	
			DM74S241, 244		120	180	

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time and duration should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions		Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF, R_L = 90Ω	DM54/74S240	2	7	ns
			DM54/74S241, 244	2	9	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF, R_L = 90Ω	DM54/74S240	2	7	ns
			DM54/74S241, 244	2	9	
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF, R_L = 90Ω	DM54/74S240	3	15	ns
			DM54/74S241, 244	3	15	
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF, R_L = 90Ω	DM54/74S240	2	10	ns
			DM54/74S241, 244	3	12	
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF, R_L = 90Ω	DM54/74S240	4	15	ns
			DM54/74S241, 244	2	15	
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 90Ω	DM54/74S240	2	9	ns
			DM54/74S241, 244	2	9	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF, R_L = 90Ω	DM54/74S240	3	10	ns
			DM54/74S241, 244	4	12	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF, R_L = 90Ω	DM54/74S240	3	10	ns
			DM54/74S241, 244	4	12	
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF, R_L = 90Ω	DM54/74S240	6	21	ns
			DM54/74S241, 244	6	21	
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF, R_L = 90Ω	DM54/74S240	4	12	ns
			DM54/74S241, 244	4	15	

National Semiconductor Corporation

DM54S251/DM74S251 TRI-STATE® 1 of 8 Line Data Selector/Multiplexer

General Description

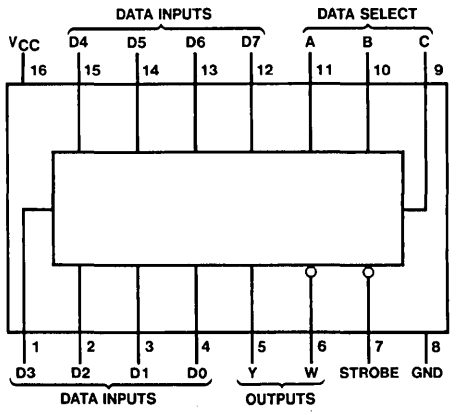
These data selectors/multiplexers contain full on-chip binary decoding to select one-of-eight data sources, and feature a strobe-controlled TRI-STATE output. The strobe must be at a low logic level to enable these devices. The TRI-STATE outputs permit direct connection to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

Features

- TRI-STATE version of S151
- Interface directly with system bus
- Perform parallel-to-serial conversion
- Permit multiplexing from N-lines to one line
- Complementary outputs provide true and inverted data
- Max no. of common outputs
  - 54S 39
  - 74S 129
- Typical propagation delay time (D to Y) 8 ns
- Typical power dissipation 275 mW

Connection Diagram



TL/F/6480–1

Order Number DM54S251J or DM74S251N
See NS Package Number J16A or N16A

Function Table

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Logic Level, L = Low Logic Level
X = Don't Care, Z = High Impedance (Off)
D0, D1 ... D7 = The Level of the respective D input

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S251			DM74S251			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			55	85	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

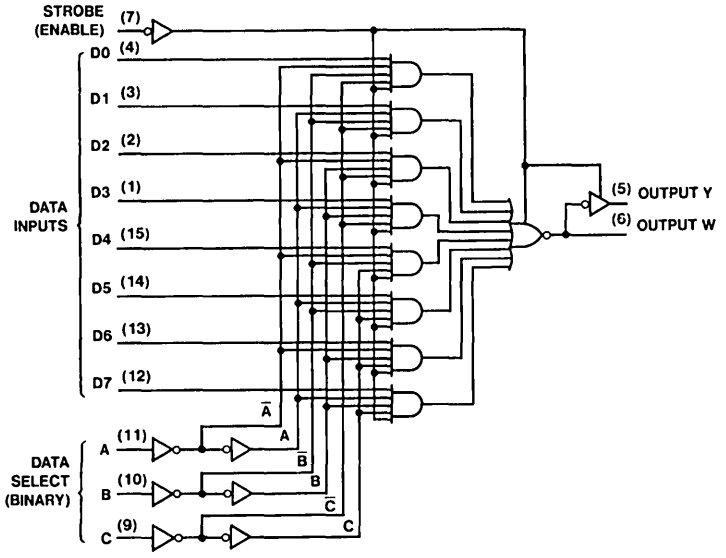
Note 3: I_{CC} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, or C (4 Levels) to Y		18		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, or C (4 Levels) to Y		19.5		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, or C (3 Levels) to W		15		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, or C (3 Levels) to W		13.5		17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Y		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Y		12		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to W		7		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to W		7		10	ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to Y				19.5	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to Y				21	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Strobe to Y		8.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Strobe to Y		14			ns
t_{PZH}	Output Enable Time to High Level Output	Strobe to W				19.5	ns
t_{PZL}	Output Enable Time to Low Level Output	Strobe to W				21	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Strobe to W		8.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Strobe to W		14			ns

Note 1: C_L = 5 pF.

Logic Diagram



TL/F/6480–2

National Semiconductor Corporation

DM54S253/DM74S253
Dual TRI-STATE® 1 of 4 Line Data Selectors/Multiplexers

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

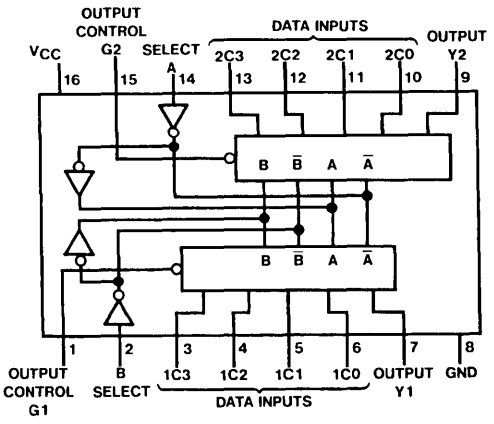
The TRI-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enable output will drive the bus line to a high or low logic level.

Features

- TRI-STATE version of S153 with same pin-out
- Schottky-diode-clamped transistors
- Permits multiplexing from N lines to 1 line
- Performs parallel-T-serial conversion
- Strobe/output control
- High fan-out totem-pole outputs
- Typical propagation delay
  - From data to output 6 ns
  - From select to output 12 ns
- Typical power dissipation 275 mW

Connection Diagram

Dual-In-Line Package



TL/F/6481–1

Order Number DM54S253J or DM74S253N
NS Package Number J16A or N16A

Function Table

Select Inputs		Data Inputs				Output Control	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S253			DM74S253			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			55	70	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

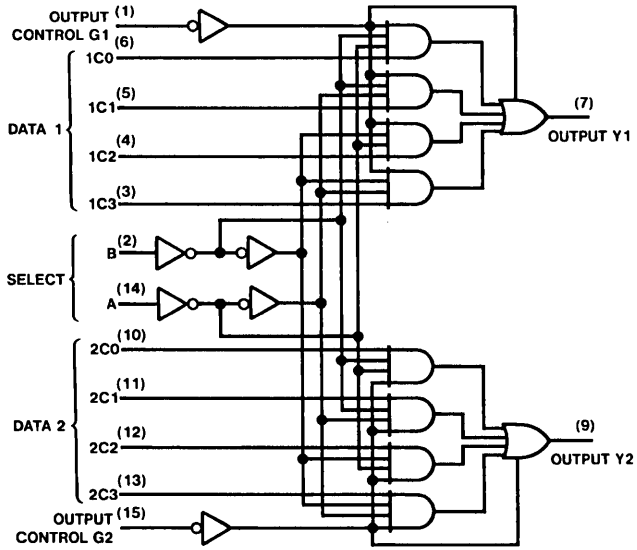
Note 3: I_{CC} is measured with all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		9		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		9		12	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		18		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		18		21	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		16.5		19.5	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		18		21	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Output Control to Y		9.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Output Control to Y		15			ns

Note 1: C_L = 5 pF.

Logic Diagram



TL/F/6481–2

National Semiconductor Corporation

DM54S257/DM74S257, DM54S258/DM74S258 TRI-STATE® Quad 1 of 2 Data Selectors/Multiplexers

General Description

These Schottky-clamped high-performance multiplexers feature TRI-STATE outputs that can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a high or low logic level. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output enable circuitry is designed such that the output disable times are shorter than the output enable times.

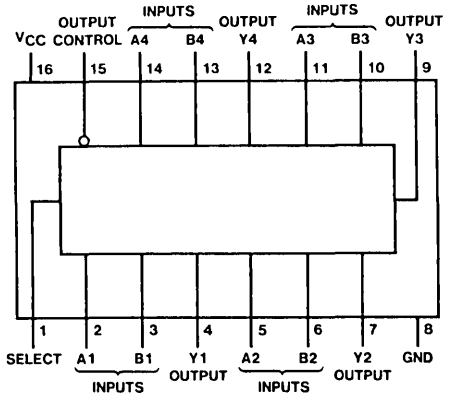
This TRI-STATE output feature means that n-bit (paralleled) data selectors with up to 258 sources can be implemented for data buses. It also permits the use of standard TTL registers for data retention throughout the system.

Features

- TRI-STATE versions S157, S158, with same pin-outs
- Schottky-clamped for significant improvement in A-C performance
- Provides bus interface from multiple sources in high-performance systems
- Average propagation delay from data input
  S257 4.8 ns
  S258 4 ns
- Typical power dissipation
  S257 320 mW
  S258 280 mW

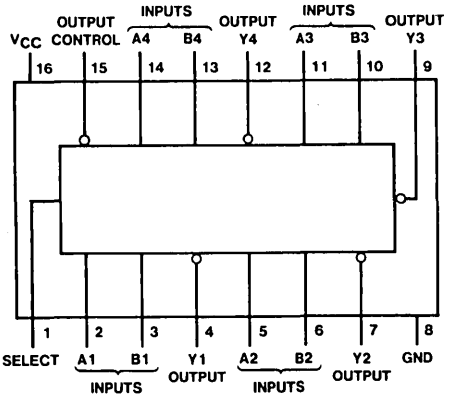
Connection Diagrams

Dual-In-Line Package



TL/F/6482–1

Dual-In-Line Package



TL/F/6482–2

Order Number DM54S258J or DM74S258N
See NS Package Number J16A or N16A

Function Table

Inputs				Output Y	
Output Control	Select	A	B	S257	S258
H	X	X	X	Z	Z
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

H = High Level, L = Low Level, X = Don't Care
Z = High Impedance (off)

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S257			DM74S257			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S257 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			100	µA
			Other			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Select			−4	mA
			Other			−2	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				50	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−50	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			44	68	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			60	93	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			64	99	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'S257 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		7.5		11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		6.5		10	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		15		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		15		16	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		19.5		23	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		21		24	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Output Control to Y		8.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Output Control to Y		14			ns

Note 1: C_L = 5 pF.

Recommended Operating Conditions

Symbol	Parameter	DM54S258			DM74S258			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−6.5	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'S258 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Select			100	μA
			Other			50	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Select			−4	mA
			Other			−2	

'S258 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)			36	56	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 3)			52	81	mA
I_{CCZ}	Supply Current with Outputs Disabled	V_{CC} = Max (Note 3)			56	87	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all outputs open and all possible inputs grounded, while achieving the stated output conditions.

'S258 Switching Characteristics

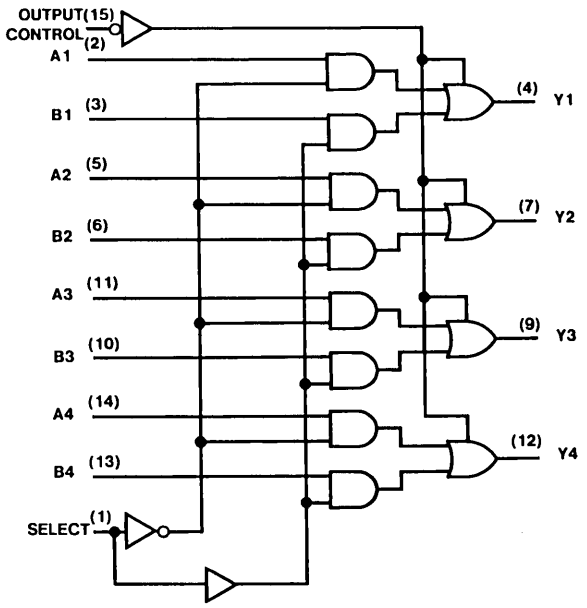
at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		6		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		6		9	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		12		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		12		15	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Y		19.5		23	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Y		21		24	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Output Control to Y		8.5			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Output Control to Y		14			ns

Note 1: C_L = 5 pF.

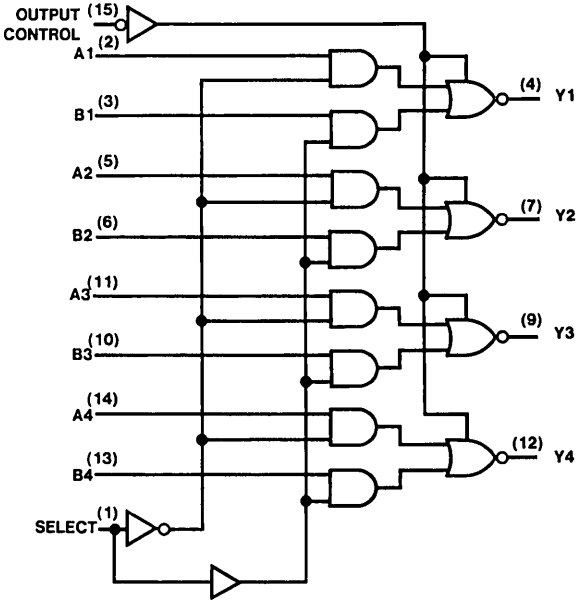
Logic Diagrams

S257



TL/F/6482–3

S258



TL/F/6482–4

National Semiconductor Corporation

DM54S280/DM74S280 9-Bit Parity Generators/Checkers

General Description

These universal, nine-bit parity generators/checkers utilize Schottky-clamped TTL high-performance circuitry, and feature odd/even outputs to facilitate operation of either odd or even parity applications. The word-length capability is easily expanded by cascading.

The S280 can be used to upgrade the performance of most systems utilizing the DM74180 parity generator/checker. Although the S280 is implemented without expander inputs, the corresponding function is provided by the availability of all input at pin 4, and no internal connection at pin 3. This permits the S280 to be substituted for the 180 in existing designs to produce an identical function, even if S280's are mixed with existing 180's.

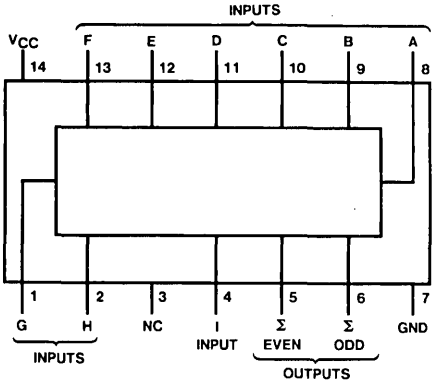
Input buffers are provided so that each input represents only one normal 74S load, and full fan-out to 10 normal Series 74S loads is available from each of the outputs at low logic levels. A fan-out to 20 normal Series 74S loads is provided at high logic levels, to facilitate connection of unused inputs to used inputs.

Features

- Generates either odd or even parity for nine data lines
- Cascadable for N-bits
- Can be used to upgrade existing systems using MSI parity circuits
- Typical data-to-output delay—14 ns

Connection Diagram

Dual-In-Line Package



TL/F/6483–1

Order Number DM54S280J, DM74S280M or DM74S280N
See NS Package Number J14A, M14A or N14A

Function Table

Number of Inputs (A Thru I) that are High	Outputs	
	Σ Even	Σ Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S280			DM74S280			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} Max (Note 3)			67	105	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

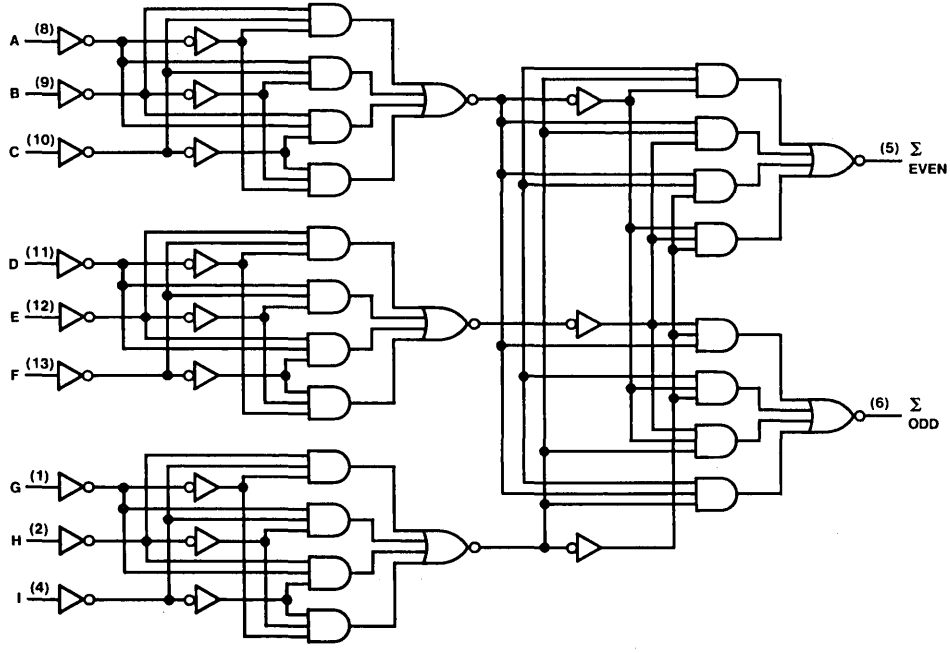
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω, C_L = 15 pF		R_L = 280Ω, C_L = 50 pF		Units
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Even		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Even		18		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Odd		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Odd		18		21	ns

Logic Diagram



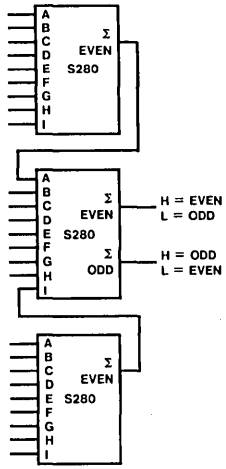
TL/F/6483–2

Typical Applications

Three S280's can be used to implement a 25-line parity generator/checker. This arrangement will provide parity in typically 25 ns. (See *Figure 1.*)

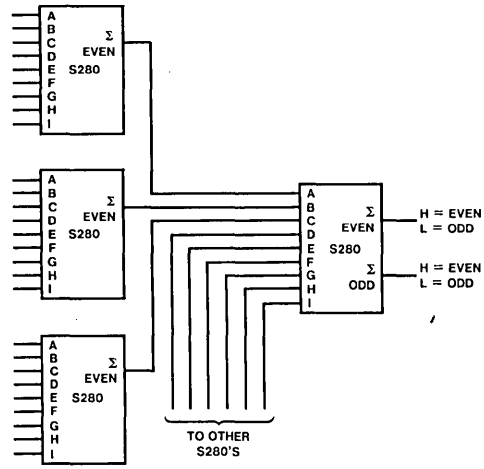
As an alternative, the outputs of two or three parity generators/checkers can be decoded with a 2-input (S86) or 3-input (S135) exclusive-OR gate for 18 or 27-line parity applications.

Longer word lengths can be implemented by cascading S280's. As shown in *Figure 2*, parity can be generated for word lengths up to 81 bits in typically 25 ns.



TL/F/6483–3

FIGURE 1. 25-Line Parity/Generator Checker



TL/F/6483–4

FIGURE 2. 81-Line Parity/Generator Checker

National Semiconductor Corporation

DM54S283/DM74S283 4-Bit Binary Adders with Fast Carry

General Description

These full adders perform the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit. These adders feature full internal look ahead across all four bits. This provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

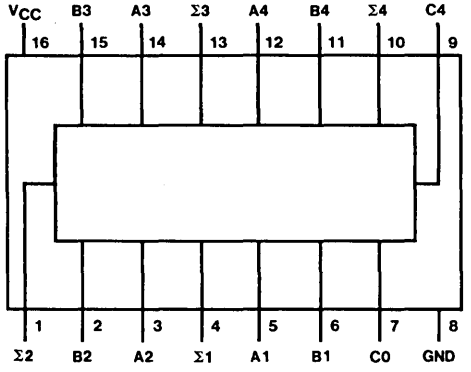
The adder logic, including the carry, is implemented in its true form meaning that the end-around carry can be accomplished without the need for logic or level inversion.

Features

- Full-carry look-ahead across the four bits
- Systems achieve partial look-ahead performance with the economy of ripple carry
- Typical add times
  - Two 8-bit words 15 ns
  - Two 16-bit words 30 ns
- Typical power dissipation 510 mW

Connection Diagram

Dual-In-Line Package



TL/F/6484–1

Order Number DM54S283J or DM74S283N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S283			DM74S283			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current (Output C4)			−0.5			−0.5	mA
	High Level Output Current (Other Outputs)			−1			−1	
I_{OL}	Low Level Output Current (Output C4)			10			10	mA
	Low Level Output Current (Other Outputs)			20			20	
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_L	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	C4 Output	−20		−100	mA
			Other Outputs	−40		−100	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			80	120	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			95	160	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC1} is measured with all outputs open, all B inputs low and all other inputs at 4.5V.

Note 4: I_{CC2} is measured with all outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ1 or Σ2		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ1 or Σ2		18		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ3		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ3		18		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C0 to Σ4		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C0 to Σ4		18		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i, B_i to S_i		18		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i, B_i to S_i		18		20	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 1)	C0 to Σ4		11		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 1)	C0 to Σ4		11		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 1)	A_i, B_i to C4		12		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 1)	A_i, B_i to C4		12		16	ns

Note 1: R_L = 560Ω.

Function Table

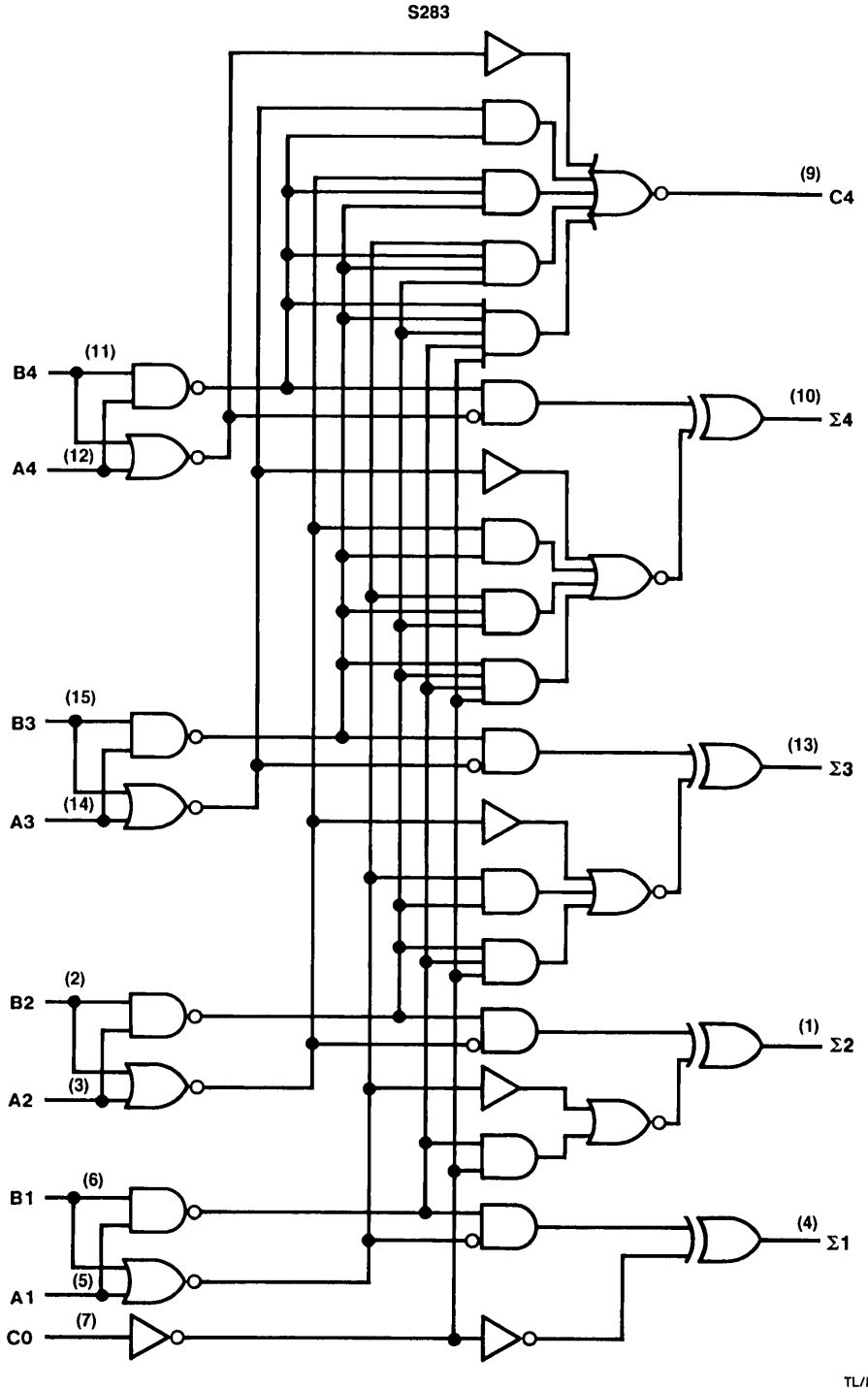
Input				Output					
				When CO = L			When CO = H		
				When C2 = L			When C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = High Level, L = Low Level

TL/F/6484–3

Note: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

Logic Diagram



TL/F/6484–2

National Semiconductor Corporation

DM54S299/DM74S299
TRI-STATE® 8-Bit Universal Shift/Storage Registers

Description

This Schottky TTL eight-bit universal register features multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

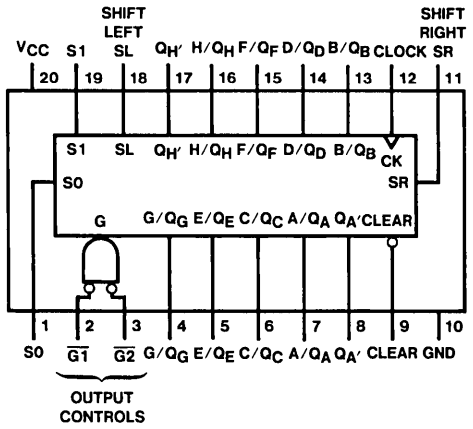
Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the TRI-STATE outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Features

- Multiplexed inputs/outputs provide improved bit density
- Four modes of operation:
  Hold (Store) Shift Left
  Shift Right Load Data
- TRI-STATE outputs drive bus lines directly
- Can be cascaded for N-bit word lengths
- Operates with outputs enabled or at high Z
- Guaranteed shift (clock) frequency 50 MHz
- Typical power dissipation 700 mW

Connection Diagram

Dual-In-Line Package



TL/F/6485–1

Order Number DM54S299J or DM74S299N
See NS Package Number J20A or N20A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S299			DM74S299			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current (Q_A thru Q_H)				−2			−6.5	mA
	High Level Output Current ($Q_{A'}$, $Q_{H'}$)				−0.5			−0.5	
I_{OL}	Low Level Output Current (Q_A thru Q_H)				20			20	mA
	High Level Output Current ($Q_{A'}$, $Q_{H'}$)				6			6	
f_{CLK}	Clock Frequency (Note 2)		0	70	50	0	70	50	MHz
f_{CLK}	Clock Frequency (Note 3)		0	60	40	0	60	40	MHz
t_W	Pulse Width (Note 5)	Clock High	10			10			ns
		Clock Low	10			10			
		Clear Low	10			10			
t_{SU}	Setup Time (Notes 4 & 5)	Select	15 ↑			15 ↑			ns
		Data High	7 ↑			7 ↑			
		Data Low	5 ↑			5 ↑			
t_H	Hold Time (Notes 4 & 5)		5 ↑			5 ↑			ns
t_{REL}	Clear Release Time (Note 5)		10 ↑			10 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: Data includes the two serial inputs and the eight input/output data lines.

Note 5: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	Q_A thru Q_H	2.4	3.2		V
			$Q_{A'}$, $Q_{H'}$	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	A thru H, S0, S1			100	μA
			Any Other			50	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Clock, Clear			−2	mA
			S0, S1			−0.5	
			Other			−0.25	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied (Q_A thru Q_H)	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				100	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied (Q_A thru Q_H)	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−250	μA
I_{OS}	Short Circuit Output Current (Q_A thru Q_H)	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
	Short Circuit Output Current ($Q_{A'}$, $Q_{H'}$)	V_{CC} = Max (Note 2)	DM54	−20		−100	
			DM74	−20		−100	
I_{CC}	Supply Current	V_{CC} = Max			140	225	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω (Note 2)				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency	(Note 3)	50		40		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 2)	Clock to $Q_{A'}$ or $Q_{H'}$		20		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 2)	Clock to $Q_{A'}$ or $Q_{H'}$		20		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q_A thru Q_H				21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q_A thru Q_H				21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 2)	Clear to $Q_{A'}$ or $Q_{H'}$		21		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q_A thru Q_H				24	ns
t_{PZH}	Output Enable Time to High Level Output	$\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H				18	ns
t_{PZL}	Output Enable Time to Low Level Output	$\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H				18	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	$\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H		12			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	$\overline{G1}$, $\overline{G2}$ to Q_A thru Q_H		12			ns

Note 1: C_L = 5 pF.

Note 2: R_L = 1KΩ for delays measured to $Q_{A'}$ and $Q_{H'}$.

Note 3: For testing f_{MAX} all outputs are loaded simultaneously.

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	$\overline{G1}$†	$\overline{G2}$†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected

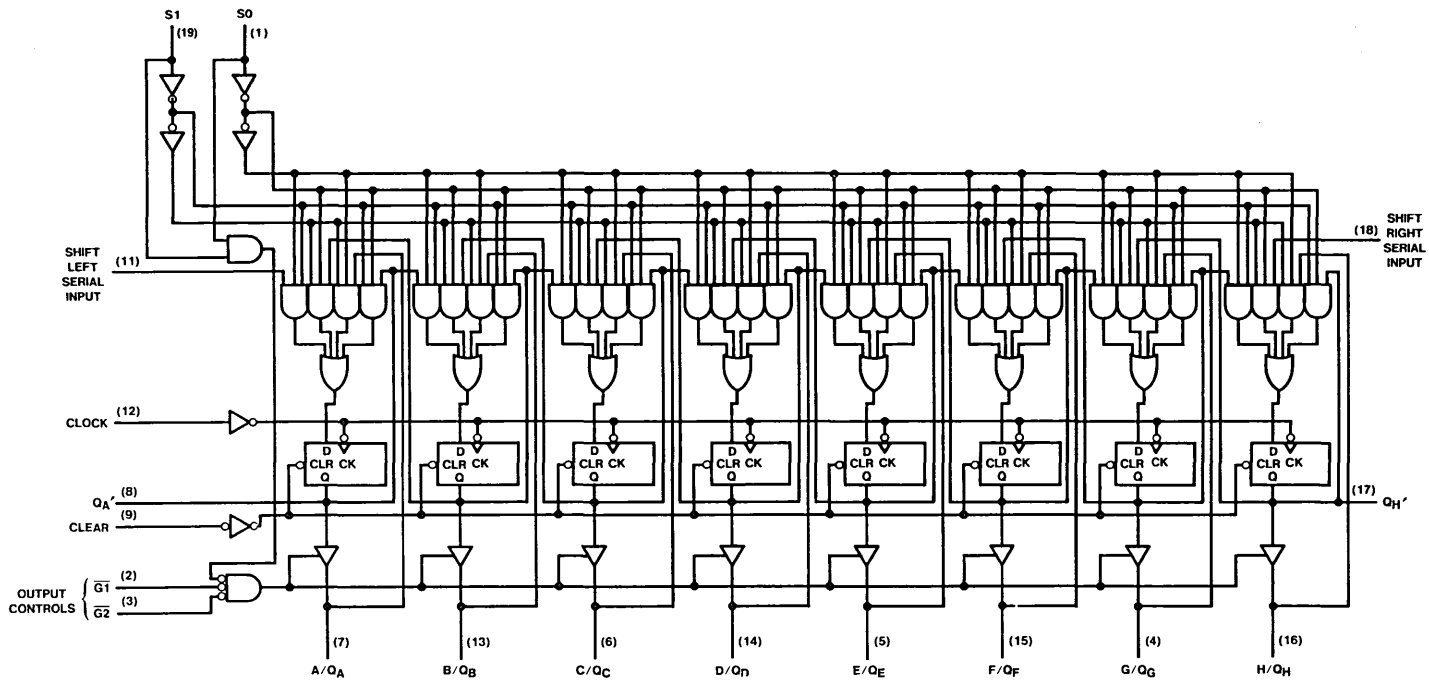
a...h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

$Q_{A0}...Q_{H0}$ = The output logic level of Q_X before the indicated input conditions were established.

H = high level, L = low logic level, X = either low or high logic level

$Q_{An}...Q_{Hn}$ = The output logic level before the active transition (↑) of the clock input.

Logic Diagram



TL/F/6485–2

National Semiconductor Corporation

DM54S373/DM74S373, DM54S374/DM74S374 TRI-STATE® Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

General Description

These 8-bit registers feature totem-pole TRI-STATE outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches of the DM54/74S373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was set up.

The eight flip-flops of the DM54/74S374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were set up at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as ac and dc noise rejection is improved by typically 400 mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

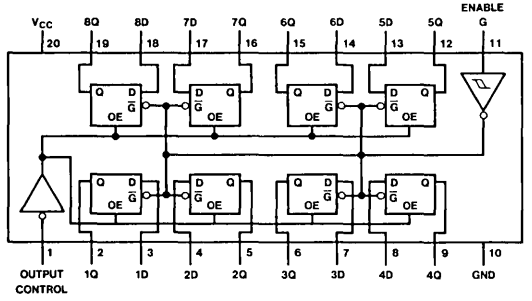
The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- TRI-STATE bus-driving outputs
- Full parallel-access for loading
- Buffered control inputs
- Clock/Enable input has hysteresis to improve noise rejection
- P-N-P input reduce D-C loading on data lines

Connection Diagrams

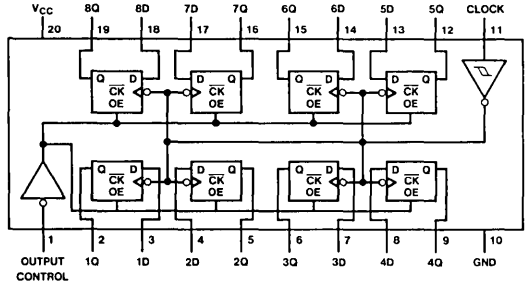
Dual-In-Line Package



Order Number DM54S373J, DM74S373WM or DM74S373N
See NS Package Number J20A, M20B or N20A

TL/F/6486–1

Dual-In-Line Package



Order Number DM54S374J, DM74S374WM or DM74S374N
See NS Package Number J20A, M20B or N20A

TL/F/6486–2

3

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Function Tables

DM54/74S373
Truth Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

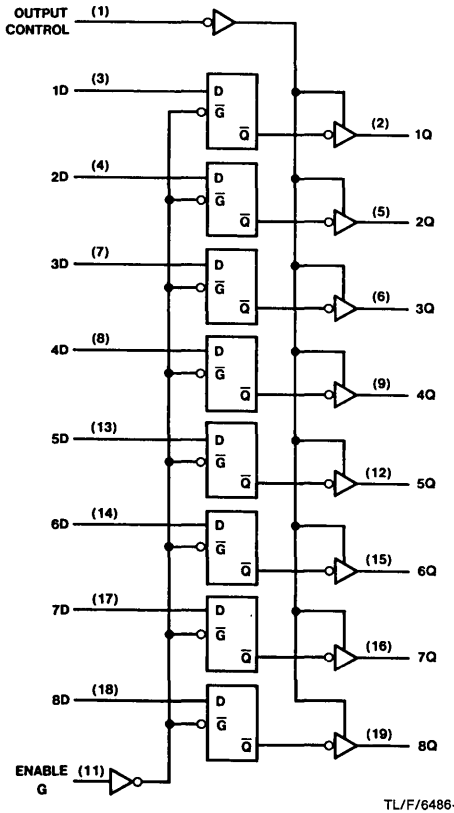
DM54/74S374
Truth Table

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care
↑ = Transition from low-to-high level, Z = High Impedance State
Q_0 = The level of the output before steady-state input conditions were established.

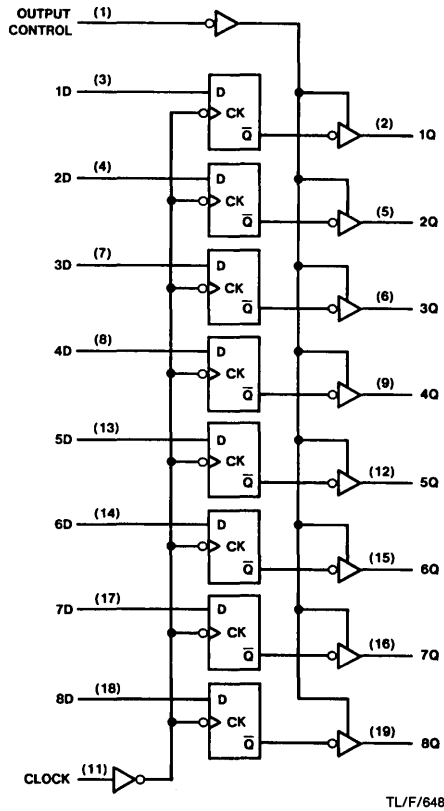
Logic Diagrams

DM54/74S373
Transparent Latches



TL/F/6486–3

DM54/74S374
Positive-Edge-Triggered Flip-Flops



TL/F/6486–4

'S373 Recommended Operating Conditions (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S373			DM74S373			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−6.5	mA
I_{OL}	Low Level Output Current				20			20	mA
t_W	Pulse Width (Note 2)	Enable High	6			6			ns
		Enable Low	7.3			7.3			
t_{SU}	Data Setup Time (Notes 1 and 3)		0 ↓			0 ↓			ns
t_H	Data Hold Time (Notes 1 and 3)		10 ↓			10 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↓) indicates the falling edge of the clock pulse is used for reference.

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: T_A = 25°C and V_{CC} = 5V.

'S373 Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−250	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZH}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 5)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max	Outputs High or Low		105	160	mA
			Outputs Disabled			190	

Note 4: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 5: Not more than one output should be shorted at a time, and the duration should not exceed one second.

'S373 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Any Q		12		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Any Q		12		16	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Any Q		14		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Any Q		18		21	ns
t_{PZH}	Enable Time to High Level Output	Output Control to Any Q		15		17	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Any Q		18		23	ns
t_{PHZ}	Output Disable Time to High Level Output (Note 1)	Output Control to Any Q		9			ns
t_{PLZ}	Output Disable Time to Low Level Output (Note 1)	Output Control to Any Q		12			ns

Note 1: C_L = 5 pF

'S374 Recommended Operating Conditions

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		DM54S374			DM74S374			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2						V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−6.5	mA
I_{OL}	Low Level Output Current				20			20	mA
f_{CLK}	Clock Frequency (Note 2)		0	100	75	0	100	75	MHz
f_{CLK}	Clock Frequency (Note 3)		0	100	75	0	100	75	MHz
t_W	Pulse Width (Note 2)	Clock High	6			6			ns
		Clock Low	7.3			7.3			
	Pulse Width (Note 3)	Clock High	15			15			
		Clock Low	15			15			
t_{SU}	Data Setup Time (Notes 1 and 4)		5↑			5↑			ns
t_H	Data Hold Time (Notes 1 and 4)		2↑			2↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.
Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.
Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.
Note 4: T_A = 25°C and V_{CC} = 5V.

'S374 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.4	3.2		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V				−250	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				50	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.5V, V_{IH} = Min, V_{IL} = Max				−50	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max	Outputs High			110	mA
			Outputs Low		90	140	
			Outputs Disabled			160	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

'S374 Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency			75		75	MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		15		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		17		20	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Any Q		15		17	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Any Q		18		23	ns
t_{PHZ}	Output Disable Time from High Level Output (Note 1)	Output Control to Any Q		9			ns
t_{PLZ}	Output Disable Time from Low Level Output (Note 1)	Output Control to Any Q		12			ns

Note 1: C_L = 5 pF

National Semiconductor Corporation

DM54S381/DM74S381 Arithmetic Logic Unit/Function Generator

General Description

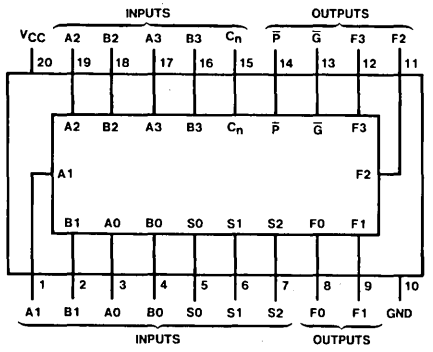
The 'S381 is a Schottky TTL arithmetic logic unit (ALU)/function generator that performs eight binary arithmetic/logic operations on two 4-bit words as shown in the function table. These operations are selected by the three function-select lines (S0, S1, S2). A full carry look-ahead circuit is provided for fast, simultaneous carry generation by means of two cascade outputs ($\overline{P}$ and $\overline{G}$) for the four bits in the package. The method of cascading 54S182/74S182 look-ahead carry generators with these ALU's to provide multi-level full carry look-ahead is illustated under typical applications data for the 'S182. The typical addition times shown illustrate the short delay time required for addition of longer words when full look-ahead is employed. The exclusive-OR, AND, or OR function of two Boolean variables is provided without the use of external circuitry. Also, the outputs can be either cleared (low) or preset (high) as desired.

Features

- A fully parallel 4-Bit ALU in 20-pin package for 0.300-inch row spacing
- Ideally suited for high-density economical processors
- Parallel inputs and outputs and full look-ahead provide system flexibility
- Arithmetic and logic operations selected specifically to simplify system implementation:
  - A minus B
  - B minus A
  - A plus B
  - and five other functions
- Schottky-clamped for high performance
  - 16-bit add time . . . 26 ns typ using look-ahead
  - 32-bit add time . . . 34 ns typ using look-ahead

Connection Diagram

Dual-In-Line Package



TL/F/6487–1

Order Number DM54S381J or DM74S381N
See NS Package Number J20A or N20A

Function Table

Selection			Arithmetic/Logic Operation
S2	S1	S0	
L	L	L	CLEAR
L	L	H	B MINUS A
L	H	L	A MINUS B
L	H	H	A PLUS B
H	L	L	A ⊕ B
H	L	H	A + B
H	H	L	AB
H	H	H	PRESET

H = high level, L = low level

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	17, 19, 1, 3	Word A Inputs
B3, B2, B1, B0	16, 18, 2, 4	Word B Inputs
S2, S1, S0	7, 6, 5	Function-Select Inputs
C_n	15	Carry Input for Addition, Inverted Carry Input for Subtraction
F3, F2, F1, F0	12, 11, 9, 8	Function Outputs
$\overline{P}$	14	Inverted Carry Propagate Output
$\overline{G}$	13	Inverted Carry Generated Output
V_{CC}	20	Supply Voltage
GND	10	Ground

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S381			DM74S381			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1			−1	mA
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM54	2.4	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V	Any S			50	μA
			Cn			250	
			Any Other			200	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V	Any S			−2	mA
			Cn			−8	
			Any Other			−6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−100	mA
			DM74	−40		−100	
I_{CC}	Supply Current	V_{CC} = Max			105	160	mA

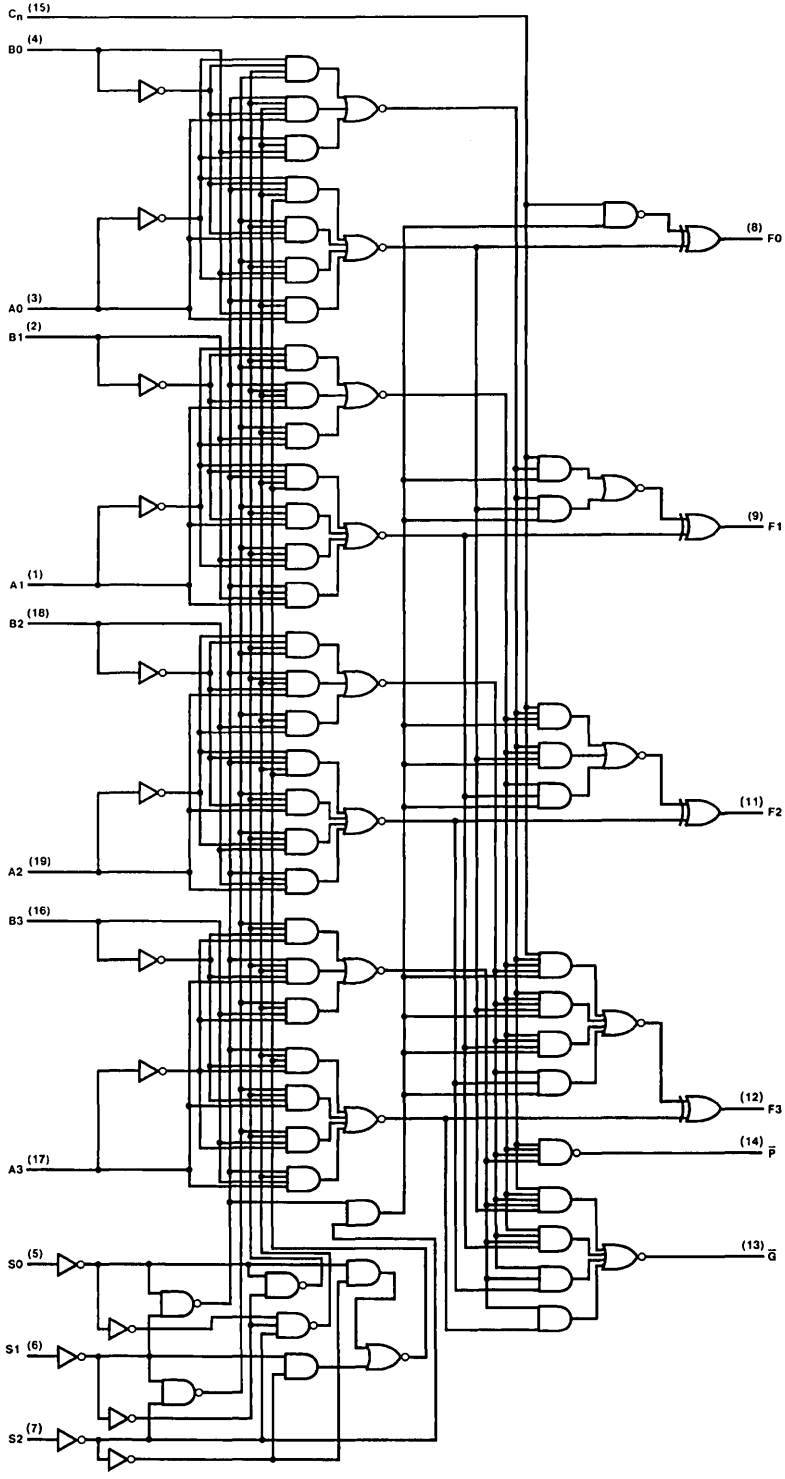
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Cn to Any F		17		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Cn to Any F		17		19	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to $\overline{G}$		20		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to $\overline{G}$		20		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to $\overline{P}$		18		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to $\overline{P}$		18		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A_i or B_i to F_i		27		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A_i or B_i to F_i		25		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	S to Any		30		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	S to Any		30		33	ns

Logic Diagram



TL/F/6487–2

National Semiconductor Corporation

DM54S940/DM74S940, DM54S941/DM74S941 Octal TRI-STATE® Buffers/Line Drivers/Line Receivers

General Description

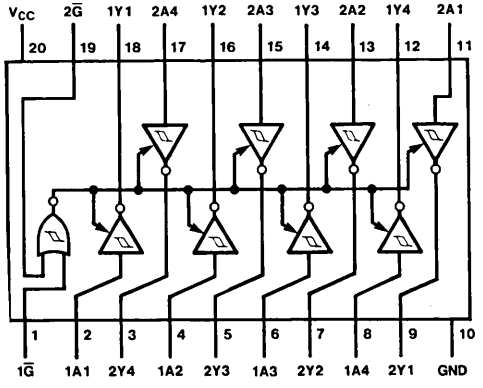
These buffers/line drivers are designed to improve both the performance and PC board density of TRI-STATE buffers/drivers employed as memory-address drivers, clock drivers, and bus-oriented transmitters/receivers. Featuring 400 mV of hysteresis at each low current PNP data line input, they provide improved noise rejection and high fanout outputs, and can be used to drive terminated lines down to 133Ω.

Features

- TRI-STATE outputs drive bus lines directly
- PNP inputs reduce DC loading on bus lines
- Hysteresis at inputs improves noise margins
- Typical I_{OL} (sink current)
  54S 48 mA
  74S 64 mA
- Typical I_{OH} (source current)
  54S −12 mA
  74S −15 mA
- Typical propagation delay times
  Inverting 4.5 ns
  Noninverting 6 ns
- Typical enable/disable times 9 ns
- Typical power dissipation (enabled)
  Inverting 450 mW
  Noninverting 538 mW

Connection Diagrams

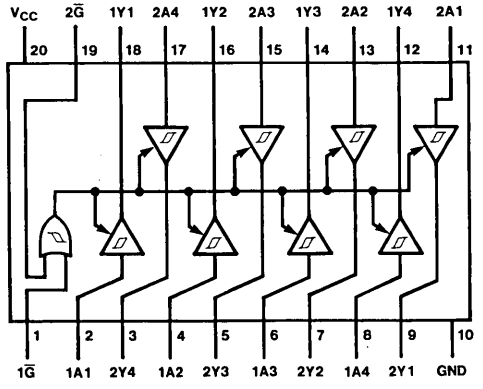
Dual-In-Line Package



TL/F/6488–1

Order Number DM54S940J or 74S940N
See NS Package Number J20A or N20A

Dual-In-Line Package



TL/F/6488–2

Order Number DM54S941J or 74S941N
See NS Package Number J20A or N20A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54S	−55°C to +125°C
DM74S	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absoulte Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54S			DM74S			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−12			−15	mA
I_{OL}	Low Level Output Current			48			64	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free-air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA				−1.2	V
Hys	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = Min		0.2	0.4		V
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −1 mA	DM74	2.7			V
		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = −3 mA		2.4	3.4		
		V_{CC} = Min, V_{IH} = 2V V_{IL} = 0.5V, I_{OH} = Max		2			
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = 0.8V V_{IH} = 2V	DM54			0.55	V
			DM74			0.55	
I_{OZH}	Off-State Output Current, High Level Voltage Applied	V_{CC} = Max V_{IL} = 0.8V V_{IH} = 2V	V_O = 2.4V			50	μA
I_{OZL}	Off-State Output Current, Low Level Voltage Applied		V_O = 0.5V			−50	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V	Any A			−400	μA
			Any G			−2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−50		−225	mA

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{CC}	Supply Current	Outputs High	DM54S940		80	123	mA
			DM74S940		80	135	
			DM54S941		95	147	
			DM74S941		95	160	
		Outputs Low	DM54S940		100	145	
			DM74S940		100	150	
			DM54S941		120	170	
			DM74S941		120	180	
		Outputs Disabled	DM54S940		100	145	
			DM74S940		100	150	
			DM54S941		120	170	
			DM74S941		120	180	

Note 1: All typical values are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time and duration should not exceed one second.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions		Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF, R_L = 90Ω	DM54/74S940	2	7	ns
			DM54/74S941	2	9	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 45 pF, R_L = 90Ω	DM54/74S940	2	7	ns
			DM54/74S941	2	9	
t_{PZL}	Output Enable Time to Low Level	C_L = 45 pF, R_L = 90Ω	DM54/74S940	3	15	ns
			DM54/74S941	3	15	
t_{PZH}	Output Enable Time to High Level	C_L = 45 pF, R_L = 90Ω	DM54/74S940	2	10	ns
			DM54/74S941	3	12	
t_{PLZ}	Output Disable Time from Low Level	C_L = 5 pF, R_L = 90Ω	DM54/74S940	4	15	ns
			DM54/74S941	2	15	
t_{PHZ}	Output Disable Time from High Level	C_L = 5 pF, R_L = 90Ω	DM54/74S940	2	9	ns
			DM54/74S941	2	9	
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 150 pF, R_L = 90Ω	DM54/74S940	3	10	ns
			DM54/74S941	4	12	
t_{PHL}	Propagation Delay Time High to Low Level Output	C_L = 150 pF, R_L = 90Ω	DM54/74S940	3	10	ns
			DM54/74S941	4	12	
t_{PZL}	Output Enable Time to Low Level	C_L = 150 pF, R_L = 90Ω	DM54/74S940	6	21	ns
			DM54/74S941	6	21	
t_{PZH}	Output Enable Time to High Level	C_L = 150 pF, R_L = 90Ω	DM54/74S940	4	12	ns
			DM54/74S941	4	15	

Section 4

TTL

Section 4 Contents

Section 4 Contents (Continued)

National Semiconductor Corporation

DM2502/DM2502C, DM2503/DM2503C, DM2504/DM2504C Successive Approximation Registers

General Description

The DM2502, DM2503 and DM2504 are 8-bit and 12-bit TTL registers designed for use in successive approximation A/D converters. These devices contain all the logic and control circuits necessary (in combination with a D/A converter) to perform successive approximation analog-to-digital conversions.

The DM2502 has 8 bits with serial capability and is not expandable.

The DM2503 has 8 bits and is expandable without serial capability.

The DM2504 has 12 bits with serial capability and expandability.

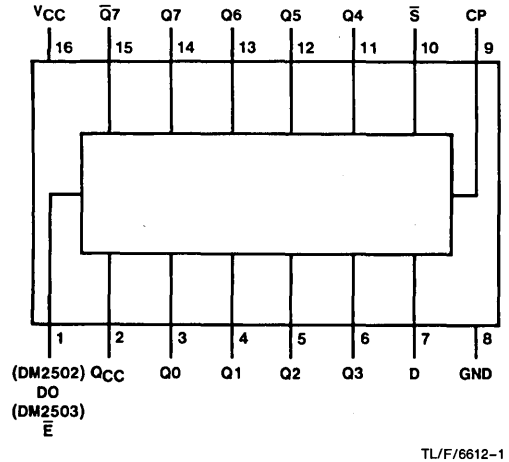
All three devices are available in ceramic DIP and molded Epoxy-B DIPs. The DM2502, DM2503 and DM2504 operate over −55°C to +125°C; the DM2502C, DM2503C and DM2504C operate over 0°C to +70°C.

Features

- Complete logic for successive approximation A/D converters
- 8-bit and 12-bit registers
- Capable of short cycle or expanded operation
- Continuous or start-stop operation
- Compatible with D/A converters using any logic code
- Active low or active high logic outputs
- Use as general purpose serial-to-parallel converter or ring counter

Connection Diagrams

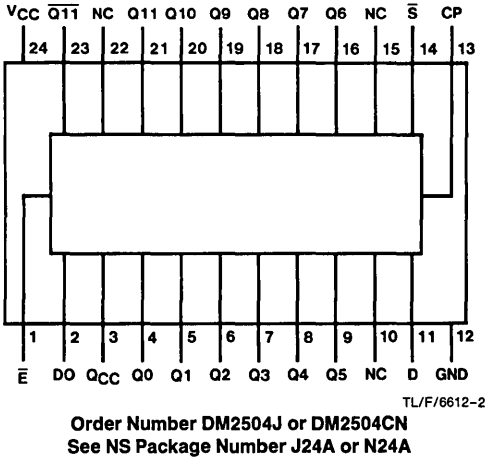
Dual-In-Line Package



TL/F/6612–1

Order Number DM2502J, DM2503J, DM2502CN or DM2503CN
See NS Package Number J16A or N16A

Dual-In-Line Package



TL/F/6612–2

Order Number DM2504J or DM2504CN
See NS Package Number J24A or N24A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
2502, 3, 4	−55°C to +125°C
2502C, 3C, 4C	0°C to +70°C
Storage Temperature Range	−65°C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM2502			DM2502C			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.48			−0.48	mA
I_{OL}	Low Level Output Current				9.6			9.6	mA
f_{CLK}	Clock Frequency (Note 3)		0		15	0		15	MHz
t_W	Pulse Width (Note 3)	Clock Low	42	30		42	30		ns
		Clock High	24	17		24	17		
t_{SU}	Setup Time (Note 3)	$\overline{S}$ Input	16	9		16	9		ns
		D Input	8	4		8	4		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

DM2502 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	CP Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	CP Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	2502	−10		−45	mA
			2502C	−10		−45	
I_{CC}	Supply Current	V_{CC} = Max	2502		65	85	mA
			2502C		65	95	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: T_A = 25°C and V_{CC} = 5V.

DM2502 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	CP to Output	10	38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CP to Output	10	28	ns

Recommended Operating Conditions

Symbol	Parameter		DM2503			DM2503C			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.48			−0.48	mA
I_{OL}	Low Level Output Current				9.6			9.6	mA
f_{CLK}	Clock Frequency (Note 1)		0		15	0		15	MHz
t_W	Pulse Width (Note 1)	CP Low	42	30		42	30		ns
		CP High	24	17		24	17		
t_{SU}	Setup Time (Note 1)	$\overline{S}$	16	9		16	9		ns
		D	8	4		8	4		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

DM2503 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	CP Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	CP Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	2503	−10		−45	mA
			2503C	−10		−45	
I_{CC}	Supply Current	V_{CC} = Max	2503		60	80	mA
			2503C		60	90	

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

DM2503 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	CP to Output	10	38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CP to Output	10	28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 1)	$\overline{E}$ to Q7		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 1)	$\overline{E}$ to Q7		24	ns

Note 1: CP = high logic level, $\overline{S}$ = low logic level.

Recommended Operating Conditions

Symbol	Parameter		DM2504			DM2504C			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.48			−0.48	mA
I_{OL}	Low Level Output Current				9.6			9.6	mA
f_{CLK}	Clock Frequency (Note 2)		0		15	0		15	MHz
t_W	Pulse Width (Note 2)	CP Low	42	30		42	30		ns
		CP High	24	17		24	17		
t_{SU}	Setup Time (Note 2)	$\overline{S}$	16	9		16	9		ns
		D	8	4		8	4		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 2: T_A = 25°C and V_{CC} = 5V.

DM2504 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	CP Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	CP Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	2504	−10		−45	mA
			2504C	−10		−45	
I_{CC}	Supply Current	V_{CC} = Max	2504		90	110	mA
			2504C		90	124	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

DM2504 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	CP to Output	10	38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	CP to Output	10	28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output (Note 3)	$\overline{E}$ to Q11		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output (Note 3)	$\overline{E}$ to Q11		24	ns

Note 3: CP = high logic level, $\overline{S}$ = low logic level.

Function Table

Time	Inputs			Outputs (4)									
t_n	D	$\overline{S}$	$\overline{E}$ (5)	D0 (6)	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	Q_{CC}
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D7	H	L	X	L	H	H	H	H	H	H	H	H
2	D6	H	L	D7	D7	L	H	H	H	H	H	H	H
3	D5	H	L	D6	D7	D6	L	H	H	H	H	H	H
4	D4	H	L	D5	D7	D6	D5	L	H	H	H	H	H
5	D3	H	L	D4	D7	D6	D5	D4	L	H	H	H	H
6	D2	H	L	D3	D7	D6	D5	D4	D3	L	H	H	H
7	D1	H	L	D2	D7	D6	D5	D4	D3	D2	L	H	H
8	D0	H	L	D1	D7	D6	D5	D4	D3	D2	D1	L	H
9	X	H	L	D0	D7	D6	D5	D4	D3	D2	D1	D0	L
10	X	X	L	X	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

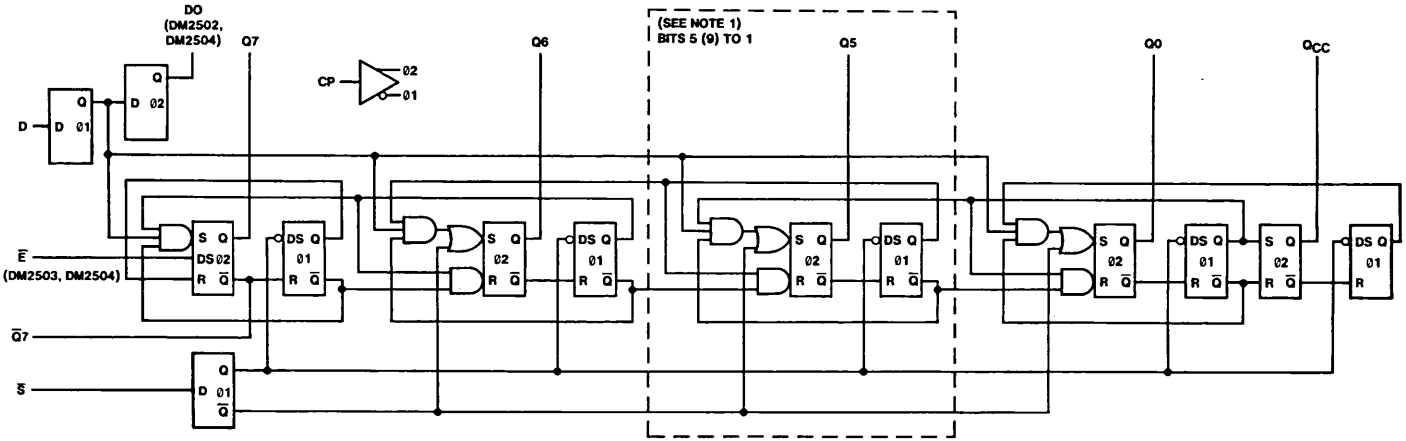
Note 4: Function table for DM2504 is extended to include 12 outputs.

Note 5: Function table for DM2502 does not include $\overline{E}$ column or last line in function table shown.

Note 6: Function table for DM2503 does not include D0 column.

H = High Level
L = Low Level
X = Don't Care
NC = No Change

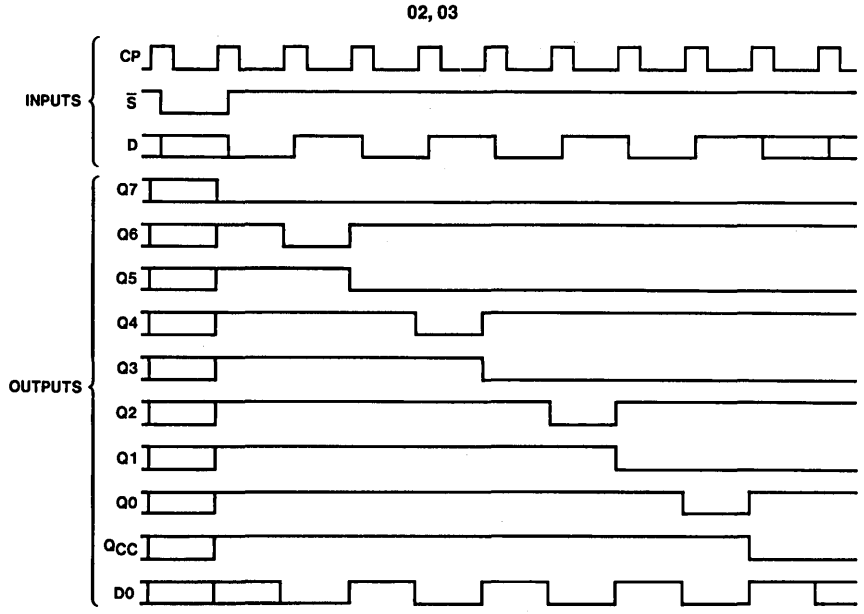
Logic Diagram



TL/F/6612–3

Note 1: Cell logic is repeated for register stages.
Q5 to Q1 DM2502, DM2503
Q9 to Q1 DM2504

Timing Diagram



TL/F/6612–4

Application Information

OPERATION

The registers consist of a set of master latches that act as the control elements in the device and change state on the input clock high-to-low transition and a set of slave latches that hold the register data and change on the input clock low-to-high transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the D0 output on the DM2502 and DM2504 when the clock goes from low-to-high. There are no restrictions on the data input; it can change state at any time except during a short interval centered about the clock low-to-high transition. At the same time that data enters the register bit the next less significant bit register is set to a low ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal low during the clock low-to-high transition. The register synchronously resets to the state Q7 (11) low, and all the remaining register outputs high. The Q_{CC} (Conversion Complete) signal is also set high at this time. The $\overline{S}$ signal should not be brought back high until after the clock low-to-high transition in order to guarantee correct resetting. After the clock has gone high resetting the register, the $\overline{S}$ must be removed. On the next clock low-to-high transition the data on the D input is set into the Q7 (11) register bit and the Q6 (10) register bit is set to a low ready for the next clock cycle. On the next clock low-to-high transition data enters the Q6 (10) register bit and Q5 (9) is set to a low. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q0, the Q_{CC} signal goes low, and the register is inhibited from further change until reset by a Start signal.

The DM2502, DM2503 and DM2504 have a specially tailored two-phase clock generator to provide non-overlapping two-phase clock pulses (i.e., the clock waveforms intersect below the thresholds of the gates they drive). Thus, even at very slow dV/dt rates at the clock input (such as from relatively weak comparator outputs), improper logic operation will not result.

LOGIC CODES

All three registers can be operated with various logic codes. Two's complement code is used by offsetting the comparator ½ full range + ½ LSB and using the complement of the MSB ($\overline{Q}$7 or $\overline{Q}$11) with a binary D/A converter. Offset binary is used in the same manner but with the MSB (Q7 or Q11). BCD D/A converters can be used with the addition of illegal code suppression logic.

ACTIVE HIGH OR ACTIVE LOW LOGIC

The register can be used with either D/A converters that require a low voltage level to turn on, or D/A converters that require a high voltage level to turn the switch on. If D/A converters are used which turn on with a low logic level, the resulting digital output from the register is active low. That is, a logic "1" is represented as a low voltage level. If D/A converters are used that turn on with a high logic level then the digital output is active high; a logic "1" is represented as a high voltage level.

EXPANDED OPERATION

An active low enable input, $\overline{E}$, on the DM2503 and DM2504 allows registers to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs in parallel and connecting the Q_{CC} output of one register to the $\overline{E}$ input of the next less significant register. When the start signal resets the register, the $\overline{E}$ signal goes high, forcing the Q7 (11) bit high and inhibiting the register from accepting data until the previous register is full and its Q_{CC} goes low. If only one register is used the $\overline{E}$ input should be held at a low logic level.

SHORT CYCLE

If all bits are not required, the register may be truncated and conversion time saved by using a register output going low rather than the Q_{CC} signal to indicate the end of conversion. If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power turn-on. This condition can be avoided by making the start input the OR function of Q_{CC} and the appropriate register output.

COMPARATOR BIAS

To minimize the digital error below ±½ LSB, the comparator must be biased. If a D/A converter is used which requires a low voltage level to turn on, the comparator should be biased +½ LSB. If the D/A converter requires a high logic level to turn on, the comparator must be biased −½ LSB.

Definition of Terms (See Timing Diagram)

CP: The clock input of the register.

D: The serial data input of the register.

D0: The serial data out. (The D input delayed one bit).

$\overline{E}$: The register enable. This input is used to expand the length of the register and when high forces the Q7 (11) register output high and inhibits conversion. When not used for expansion the enable is held at a low logic level (ground).

Q_I I = 7 (11) to 0: The outputs of the register.

Q_{CC}: The conversion complete output. This output remains high during a conversion and goes low when a conversion is complete.

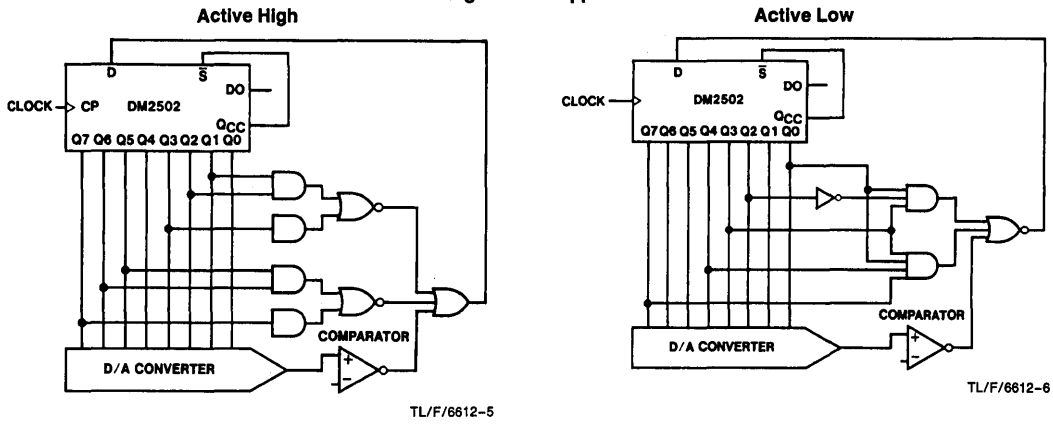
Q7 (11): The true output of the MSB of the register.

$\overline{Q}$7 (11): The complement output of the MSB of the register.

$\overline{S}$: The start input. If the start input is held low for at least a clock period the register will be reset to Q7 (11) low and all the remaining outputs high. A start pulse that is low for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

Typical Applications

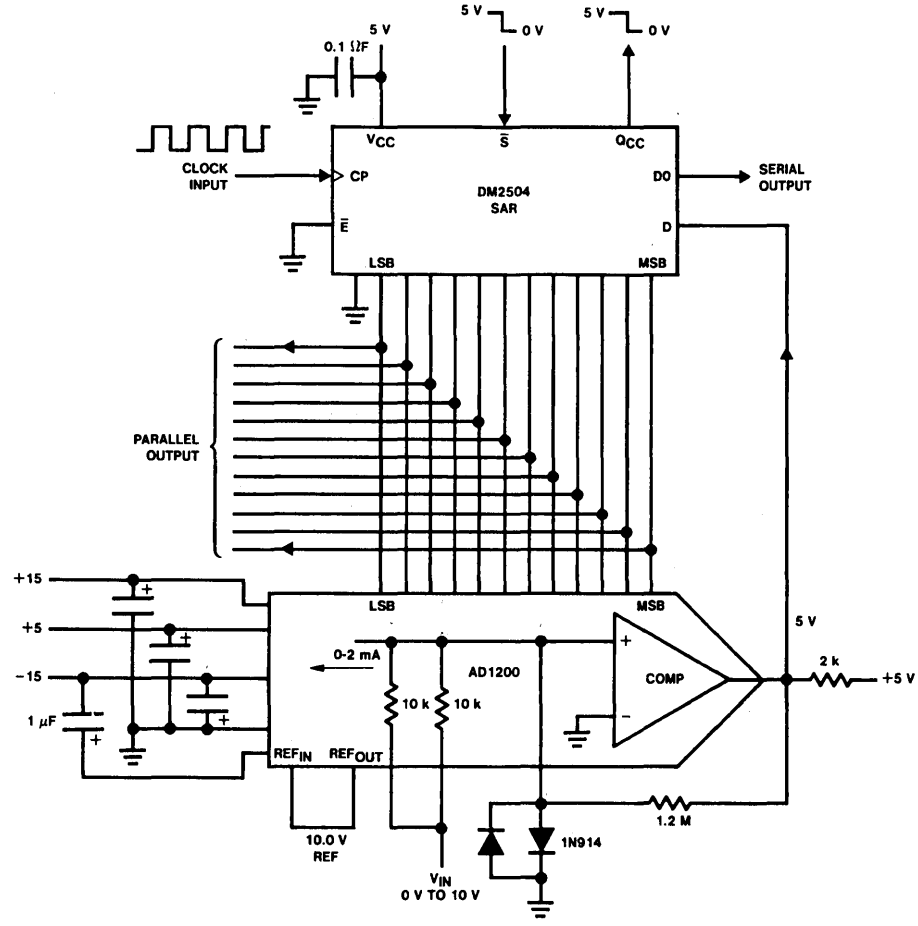
BCD Illegal Code Suppression



TL/F/6612-5

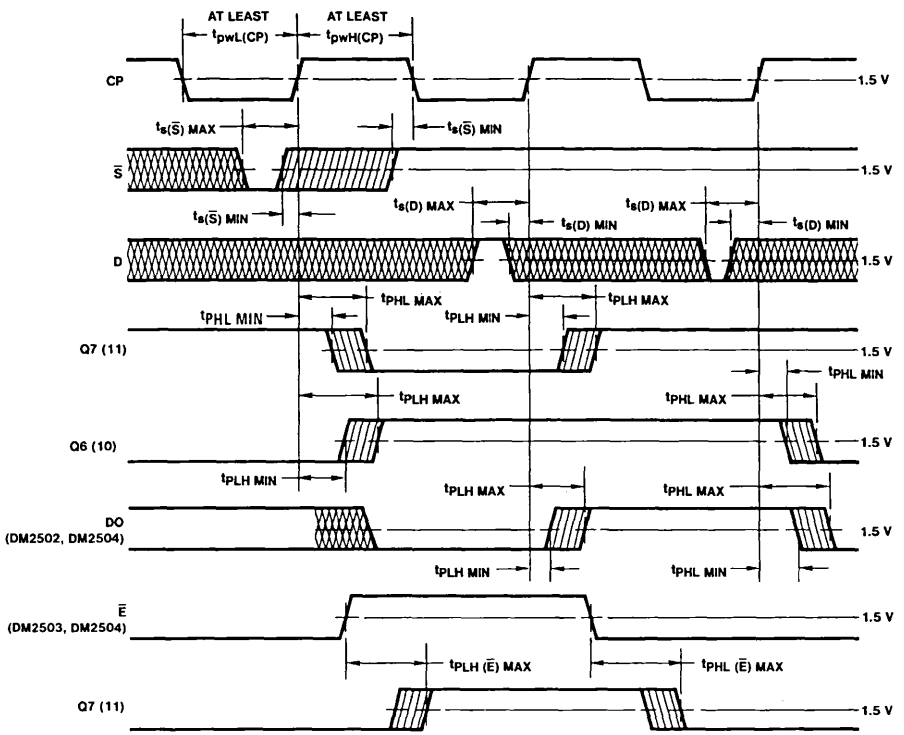
TL/F/6612-6

High Speed 12-BIT A/D Converter



TL/F/6612-7

Switching Time Waveforms



WAVEFORMS	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from H to L	Will be changing from H to L
	May change from L to H	Will be changing from L to H
	Don't care: any change permitted	Changing: state unknown

ENABLE TO Q7 (11)
CP = H
$\overline{S}$ = L

TL/F/6612–8

National Semiconductor Corporation

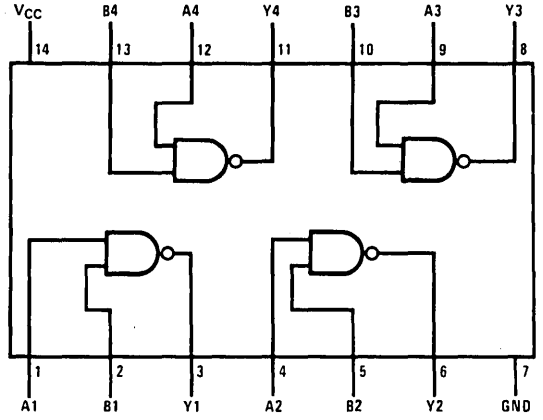
DM5400/DM7400 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6613–1

Order Number DM5400J or DM7400N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5400			DM7400			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

DM5401/DM7401 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

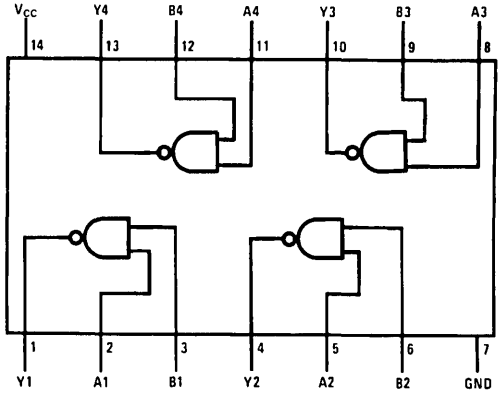
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6614–1

Order Number DM5401J or DM7401N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5401			DM7401			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		4	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 4 kΩ (t_{PLH}) R_L = 400Ω (t_{PHL})		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

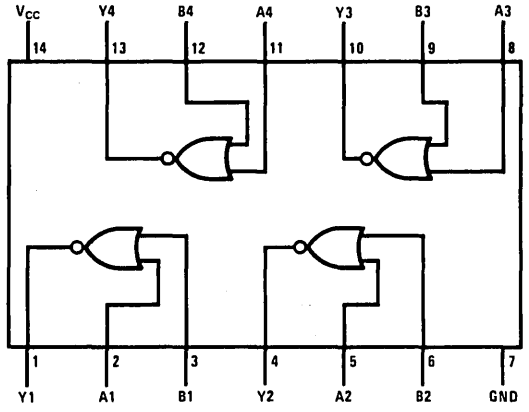
DM5402/DM7402 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



TL/F/6492–1

Order Number DM5402J or DM7402N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5402			DM7402			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			14	27	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

DM5403/DM7403 Quad 2-Input NAND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

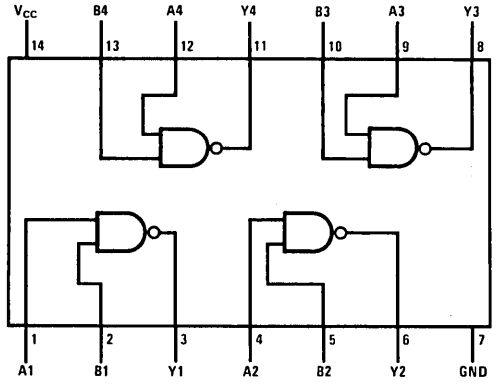
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6493–1

Order Number DM5403J or DM7403N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5403			DM7403			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		4	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 4 kΩ (t_{PLH}) R_L = 400Ω (t_{PHL})		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

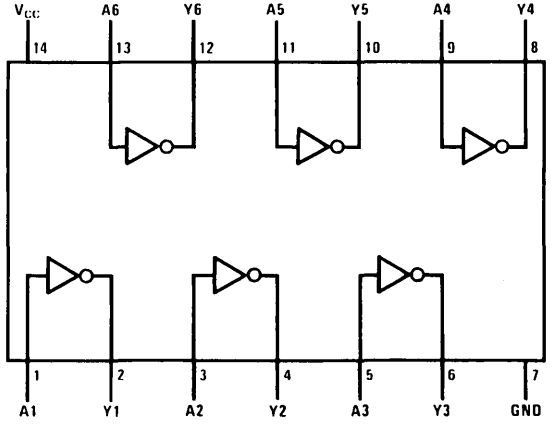
DM5404/DM7404 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

Connection Diagram

Dual-In-Line Package



TL/F/6494–1

Order Number DM5404J, DM7404M or DM7404N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = \overline{A}$

Inputs	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5404			DM7404			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			6	12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			18	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

DM5405/DM7405 Hex Inverters with Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

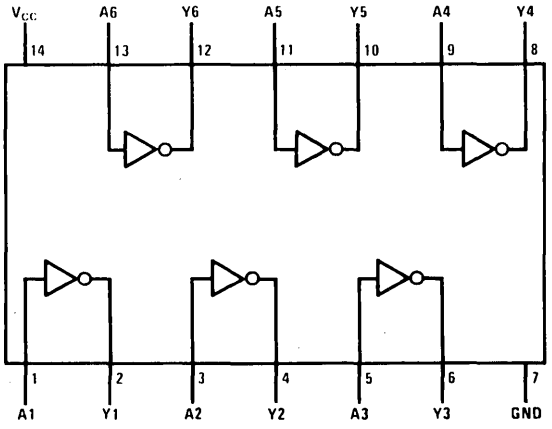
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6495–1

Order Number DM5405J or DM7405N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5405			DM7405			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		6	12	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		18	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 4 kΩ (t_{PLH}) R_L = 400Ω (t_{PHL})		55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

DM5406/DM7406 Hex Inverting Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent buffers each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

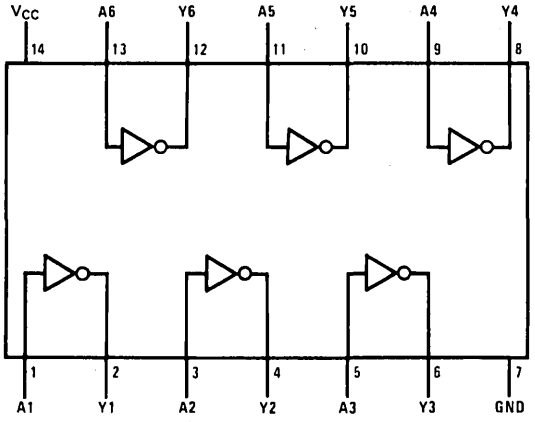
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6496–1

Order Number DM5406J, DM7406M or DM7406N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5406			DM7406			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		30	42	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		27	38	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 110Ω		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			23	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

DM5407/DM7407 Hex Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs a buffer function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

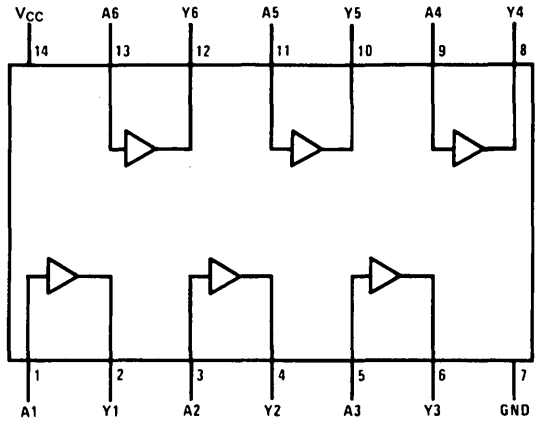
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6497–1

Order Number DM5407J, DM7407M or DM7407N
See NS Package Number J14A, M14A or N14A

Function Table

$Y = A$

Input	Output
A	Y
L	L
H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5407			DM7407			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		29	41	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		21	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 110Ω		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

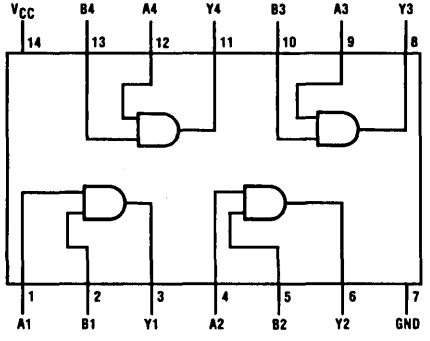
DM5408/DM7408 Quad 2-Input AND Gates

General Description

This device contains four independent gates each of which performs the logic AND function.

Connection Diagram

Dual-In-Line Package



TL/F/6498–1

Order Number DM5408J or DM7408N
See NS Package Number J14A or N14A

Function Table

$Y = AB$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5408			DM7408			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			11	21	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			20	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 400Ω		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			19	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

DM5409/DM7409 Quad 2-Input AND Gates with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic AND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

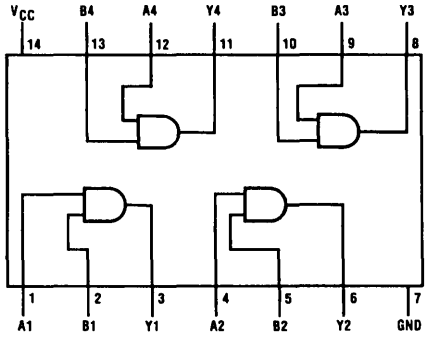
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6499–1

Order Number DM5409J or DM7409N
See NS Package Number J14A or N14A

Function Table

$$Y = AB$$

Inputs		Output
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5409			DM7409			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		11	21	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		20	33	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			24	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

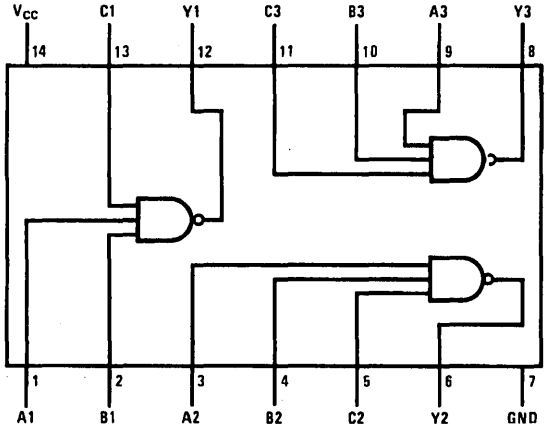
DM5410/DM7410 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6500–1

Order Number DM5410J or DM7410N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{ABC}$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5410			DM7410			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			3	6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			9	16.5	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

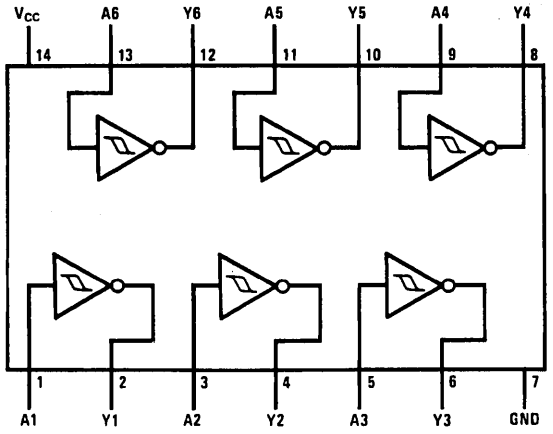
DM5414/DM7414 Hex Inverter with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package



TL/F/6503–1

Order Number DM5414J or DM7414N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5414			DM7414			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.7	2	1.5	1.7	2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.9	1.1	0.6	0.9	1.1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_I = V_{T-} Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_I = V_{T+} Max			0.2	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.43		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.56		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−18		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			22	36	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			39	60	mA

Note 1: V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			22	ns

National Semiconductor Corporation

DM5416/DM7416 Hex Inverting Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

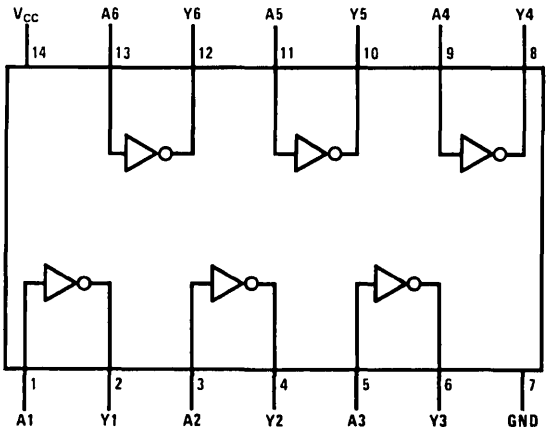
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6504–1

Order Number DM5416J or DM7416N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{A}$$

Input	Output
A	Y
L	H
H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	15V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5416			DM7416			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 15V, V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		30	42	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		27	38	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 110Ω		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			23	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

DM5417/DM7417 Hex Buffers with High Voltage Open-Collector Outputs

General Description

This device contains six independent gates each of which performs a buffer function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

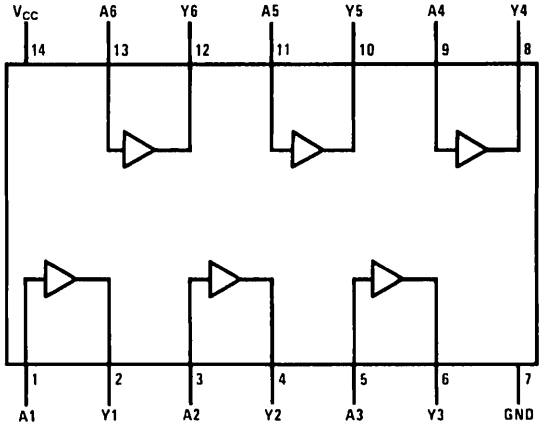
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6505–1

Order Number DM5417J or DM7417N
See NS Package Number J14A or N14A

Function Table

$Y = A$

Input	Output
A	Y
L	L
H	H

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	15V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5417			DM7417			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			30			40	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 15V V_{IH} = Min			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max			0.7	V
		I_{OL} = 16 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		29	41	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		21	30	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 110Ω		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

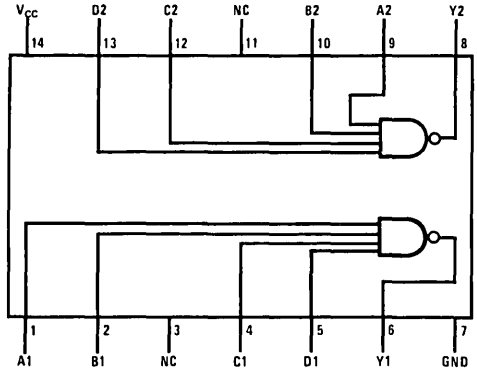
DM5420/DM7420 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6506–1

Order Number DM5420J or DM7420N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5402			DM7402			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			2	4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			6	11	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

DM5426/DM7426 Quad 2-Input NAND Gates with High Voltage Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_O\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_O\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

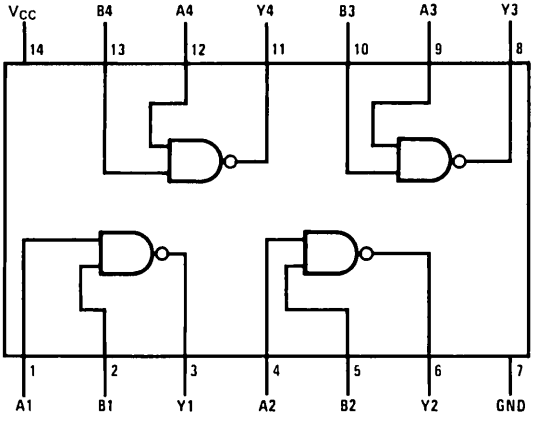
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6508–1

Order Number DM5426J or DM7426N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	15V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5426			DM7426			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_{IL} = Max	V_O = 15V			1000	μA
			V_O = 12V			50	
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			4	8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	22	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 1 kΩ (t_{PLH})		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			17	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

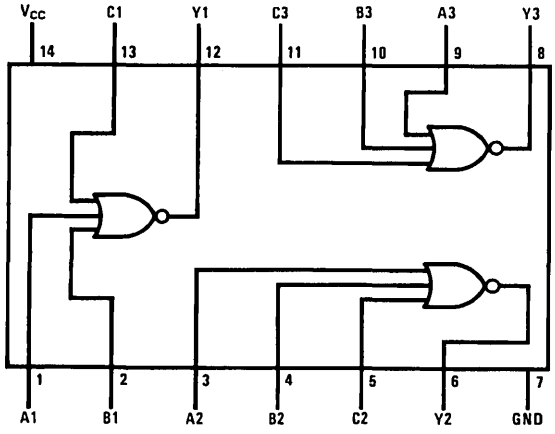
DM5427/DM7427 Triple 3-Input NOR Gates

General Description

This device contains three independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



TL/F/6509–1

Order Number DM5427J or DM7427N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{A + B + C}$$

Inputs			Output
A	B	C	Y
L	L	L	H
X	X	H	L
X	H	X	L
H	X	X	L

H = High Logic Level
L = Low Logic Level
X = Either High or Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5427			DM7427			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			10	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			16	26	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		11	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

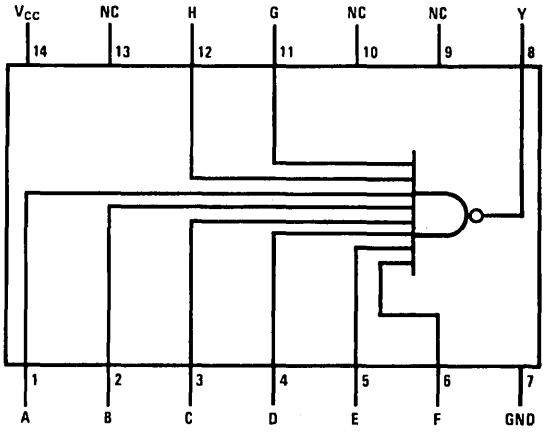
DM5430/DM7430 8-Input NAND Gate

General Description

This device contains a single gate which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6510–1

Order Number DM5430J or DM7430N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{ABCDEFGH}$$

Inputs	Output
A thru H	Y
All Inputs H	L
One or More Input L	H

H = High Logic Level
L = Low Logic Level

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5430			DM7430			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			1	2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			3	6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 400Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

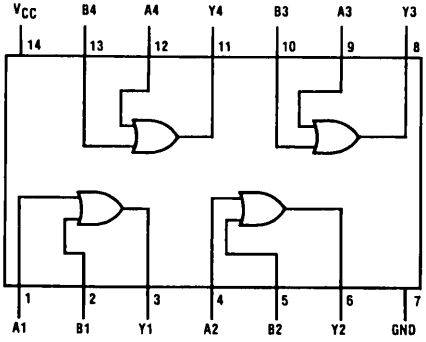
DM5432/DM7432 Quad 2-Input OR Gates

General Description

This device contains four independent gates each of which performs the logic OR function.

Connection Diagram

Dual-In-Line Package



TL/F/6511–1

Order Number DM5432J or DM7432N
See NS Package Number J14A or N14A

Function Table

$Y = A + B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5432			DM7432			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			15	22	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			23	38	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF, R_L = 400Ω		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			22	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

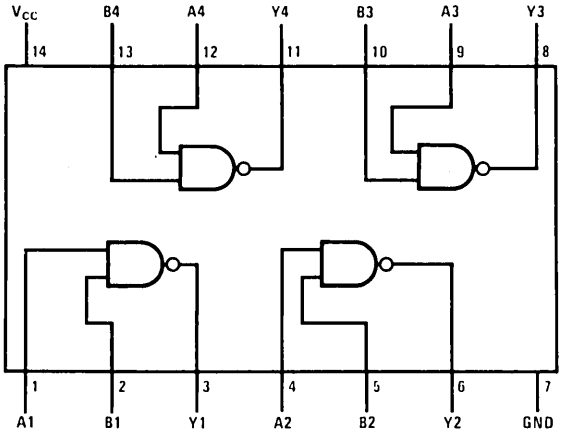
DM5437/DM7437 Quad 2-Input NAND Buffers

General Description

This device contains four independent gates each of which performs the logic NAND function.

Connection Diagram

Dual-In-Line Package



TL/F/6512–1

Order Number DM5437J or DM7437N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5437			DM7437			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−1.2			−1.2	mA
I_{OL}	Low Level Output Current			48			48	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−70	mA
			DM74	−18		−70	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			9	15.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			34	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF, R_L = 133Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

DM5438/DM7438 Quad 2-Input NAND Buffers with Open-Collector Outputs

General Description

This device contains four independent gates each of which performs the logic NAND function. The open-collector outputs require external pull-up resistors for proper logical operation.

Pull-Up Resistor Equations

$$R_{MAX} = \frac{V_{CC}\,(Min) - V_{OH}}{N_1\,(I_{OH}) + N_2\,(I_{IH})}$$

$$R_{MIN} = \frac{V_{CC}\,(Max) - V_{OL}}{I_{OL} - N_3\,(I_{IL})}$$

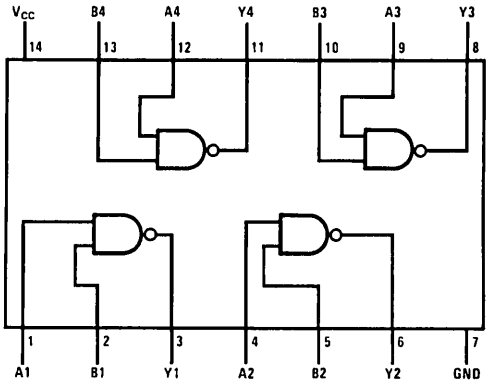
Where: $N_1\,(I_{OH})$ = total maximum output high current for all outputs tied to pull-up resistor

$N_2\,(I_{IH})$ = total maximum input high current for all inputs tied to pull-up resistor

$N_3\,(I_{IL})$ = total maximum input low current for all inputs tied to pull-up resistor

Connection Diagram

Dual-In-Line Package



TL/F/6513–1

Order Number DM5438J, DM7438M or DM7438N
See NS Package Number J14A, M14A or N14A

Function Table

$$Y = \overline{AB}$$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5438			DM7438			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			48			48	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min			0.4	V
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		5	8.5	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		34	54	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 45 pF R_L = 133Ω		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			18	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

National Semiconductor Corporation

DM5441A/DM7441A BCD to Decimal Decoders/Drivers

General Description

The DM5441A/DM7441A is a BCD-to-decimal decoder designed to drive gas-filled NIXIE tubes. The device is also capable of driving other types of low-current lamps and relays.

An over-range decoding feature provides that if binary numbers between 10 and 15 are applied to the input, the least significant bit (0-5) will be decoded on the output.

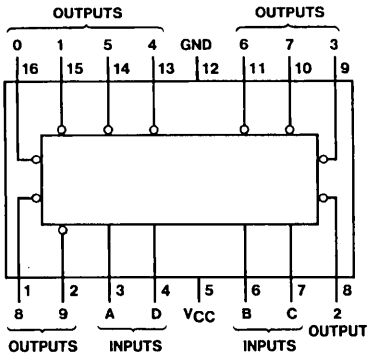
Input clamp diodes are also provided to clamp negative-voltage transitions in order to minimize transmission-line effects.

Features

- Drive cold-cathode, numeric indicator tubes directly
- Fully decoded inputs
- Low leakage current 1.8 μA @ 50V
- Low power dissipation 105 mW typical

Connection Diagram

Dual-In-Line Package



TL/F/6515–1

Order Number DM5441AJ or DM7441AN
See NS Package Number J16A or N16A

Function Table

5441A/7441A

Inputs				Output On*
D	C	B	A	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
(Over Range)				
H	L	H	L	0
H	L	H	H	1
H	H	L	L	2
H	H	L	H	3
H	H	H	L	4
H	H	H	H	5

H = High Level, L = Low Level

*All other outputs are off

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5441A			DM7441A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OL}	Low Level Output Current			7			7	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

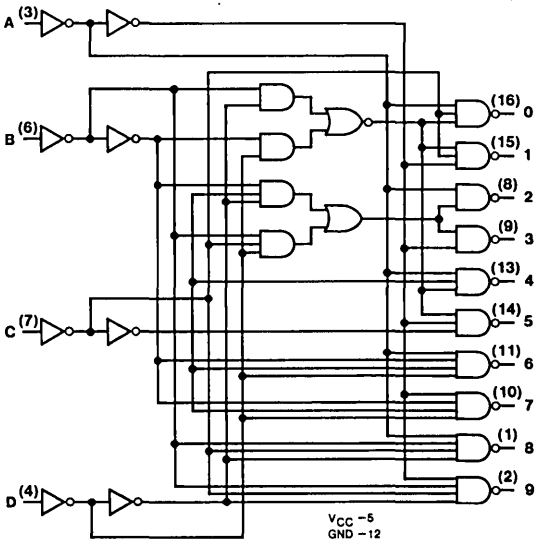
Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = 1 mA V_{IL} = Max, V_{IH} = Min		70			V
I_{OH}	Off-State Reverse Current	V_{CC} = Min V_O = 50V	T_A = 125°C			60	μA
			T_A = 70°C			40	
			T_A = −55 to 70°C			1.8	
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	T_A = − 55 to 70°C			2.5	V
			T_A = 125°C			3	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			21	36	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs grounded.

Logic Diagram

5441A/7441A



TL/F/6515-2

National Semiconductor Corporation

DM5442/DM7442 BCD to Decimal Decoders

General Description

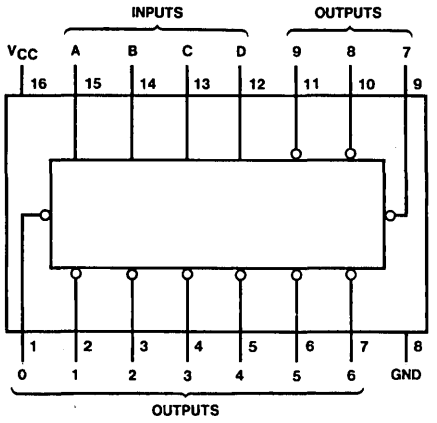
These BCD-to-decimal decoders consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of input logic ensures that all outputs remain off for all invalid (10–15) input conditions.

Features

- Diode clamped inputs
- Also for application as 4-line-to-16-line decoders; 3-line-to-8-line decoders
- All outputs are high for invalid input conditions
- Typical power dissipation 140 mW
- Typical propagation delay 17 ns

Connection Diagram

Dual-In-Line Package



TL/F/6516–1

Order Number DM5442J or DM7442N
See NS Package Number J16A or N16A

Function Table

No.	BCD Input				Decimal Output									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = High Level
L = Low Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5442			DM7442			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		28	41	mA
			DM74		28	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

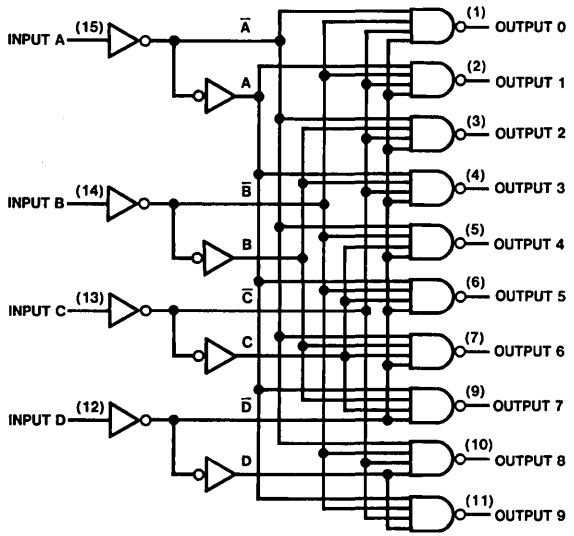
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PHL}	Propagation Delay Time High to Low Level Output from A, B, C or D through 2 Levels of Logic	C_L = 15 pF, R_L = 400Ω		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output from A, B, C or D through 3 Levels of Logic			30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output from A, B, C or D through 2 Levels of Logic			25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output from A, B, C or D through 3 Levels of Logic			30	ns

Logic Diagram



TI/F/6516–2

National Semiconductor Corporation

DM5445/DM7445 BCD to Decimal Decoders/Drivers

General Description

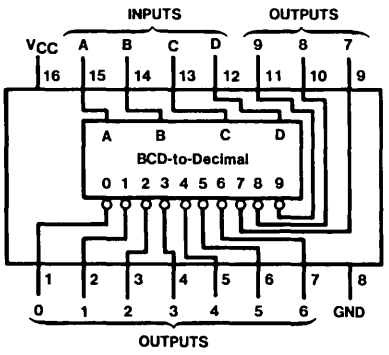
These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10–15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

Features

- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

Connection Diagram

Dual-In-Line Package



TL/F/6517–1

Order Number DM5445J or DM7445N
See NS Package Number J16A or N16A

Function Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = High Level (Off), L = Low Level (On)

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	30V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5445			DM7445			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			30			30	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 30V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
		I_{OL} = 80 mA V_{CC} = Min			0.5	0.9	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		43	62	mA
			DM74		43	70	

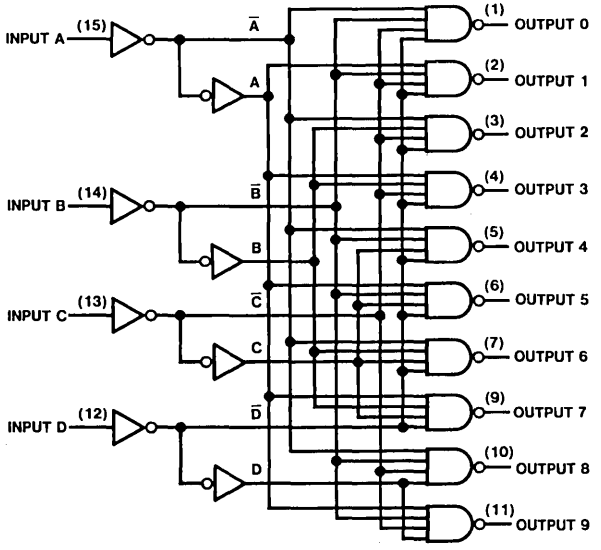
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 100Ω		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

Logic Diagram



TL/F/6517–2

National Semiconductor Corporation

DM5446A/DM7446A, DM5447A/DM7447A BCD to 7-Segment Decoders/Drivers

General Description

The 46A and 47A feature active-low outputs designed for driving common-anode LEDs or incandescent indicators directly. All of the circuits have full ripple-blanking input/output controls and a lamp test input. Segment identification and resultant displays are shown on a following page. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

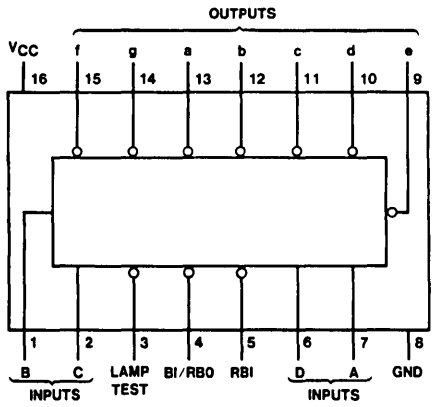
All of the circuits incorporate automatic leading and/or trailing-edge, zero-blanking control (RBI and RBO). Lamp test (LT) of these devices may be performed at any time when the BI/RBO node is at a high logic level. All types contain an overriding blanking input (BI) which can be used to control the lamp intensity (by pulsing) or to inhibit the outputs.

Features

- All circuit types feature lamp intensity modulation capability
- Open-collector outputs drive indicators directly
- Lamp-test provision
- Leading/trailing zero suppression

Connection Diagram

Dual-In-Line Package



TL/F/6518–1

Order Number DM5446AJ, DM5447AJ, DM7446AN or DM7447AN
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5446A			DM7446A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			30			30	V
I_{OH}	High Level Output Current (BI/RBO)			−0.2			−0.2	μA
I_{OL}	Low Level Output Current (a thru g)			40			40	mA
I_{OL}	Low Level Output Current (BI/RBO)			8			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'46A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage (BI/RBO)	V_{CC} = Min, I_{OH} = Max		2.4	3.7		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Max, V_O = 30V, V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V (Except BI/RBO)				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V (Except BI/RBO)				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	BI/RBO			−4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		60	85	mA
			DM74		60	103	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

'46A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 120Ω		100	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			100	ns

Recommended Operating Conditions

Symbol	Parameter	DM5447A			DM7447A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (a thru g)			15			15	V
I_{OH}	High Level Output Current (BI/RBO)			−0.2			−0.2	μA
I_{OL}	Low Level Output Current (a thru g)			40			40	mA
I_{OL}	Low Level Output Current (BI/RBO)			8			8	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'47A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage (BI/RBO)	V_{CC} = Min I_{OH} = Max		2.4	3.7		V
I_{CEX}	High Level Output Current (a thru g)	V_{CC} = Max, V_O = 15V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.3	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	BI/RBO			−4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (BI/RBO)				−4	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		60	85	mA
			DM74		60	103	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs at 4.5V.

'47A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 120Ω		100	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			100	ns

Function Table

46A, 47A

Decimal or Function	Inputs						BI/RBO (Note 1)	Outputs							Note
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	(2)
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
BI	X	X	X	X	X	X	L	H	H	H	H	H	H	H	(3)
RBI	H	L	L	L	L	L	L	H	H	H	H	H	H	H	(4)
LT	L	X	X	X	X	X	H	L	L	L	L	L	L	L	(5)

Note 1: BI/RBO is a wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

Note 2: The blanking input (BI) must be open or held at a high logic level when output functions 0 through 15 are desired. The ripple-blanking input (RBI) must be open or high if blanking of a decimal zero is not desired.

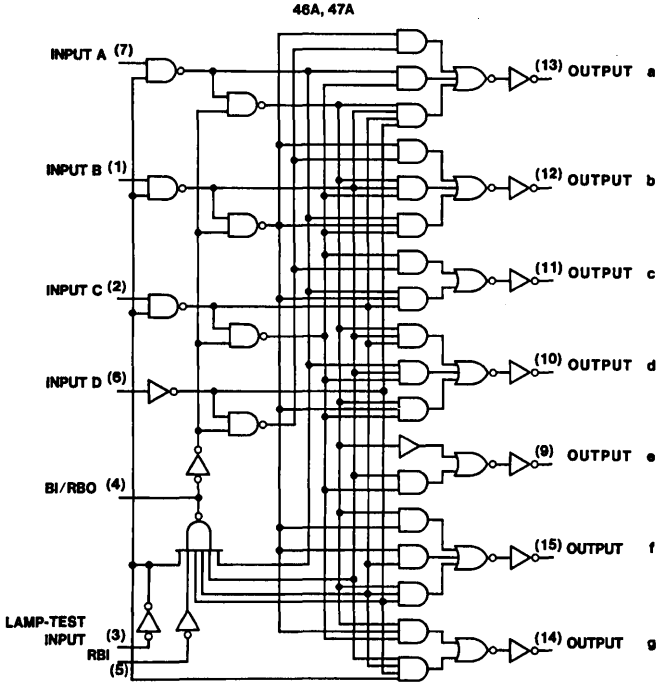
Note 3: When a low logic level is applied directly to the blanking input (BI), all segment outputs are high regardless of the level of any other input.

Note 4: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp test input high, all segment outputs go H and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 5: When the blanking input/ripple-blanking output (BI/RBO) is open or held high and a low is applied to the lamp-test input, all segment outputs are L.

H = High level, L = Low level, X = Don't Care

Logic Diagram



TL/F/6518–2

National Semiconductor Corporation

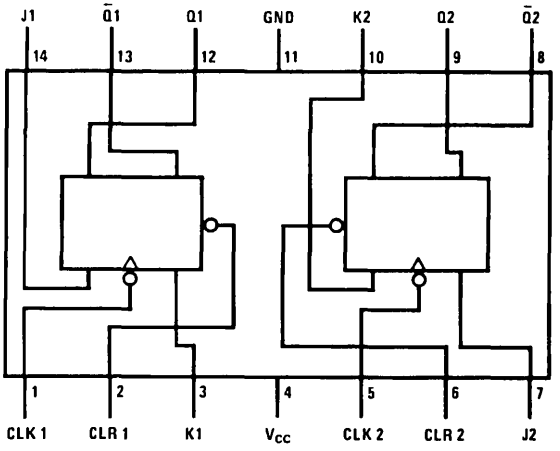
DM5473/DM7473 Dual Master-Slave J-K Flip-Flops with Clear, and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data transfers to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6525–1

Order Number DM5473J or DM7473N
See NS Package Number J14A or N14A

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

⎍ = Positive pulse data. the J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each high level clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM5473			DM7473			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)		0		15	0		15	MHz
t_W	Pulse Width (Note 5)	Clock High	20			20			ns
		Clock Low	47			47			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Note 1 & 5)		0 ↑			0 ↑			ns
t_H	Input Hold Time (Note 1 & 5)		0 ↓			0 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max, (Note 4)			18	34	mA

Note 1: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference: (↑) for rising edge, (↓) for falling edge.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns

National Semiconductor Corporation

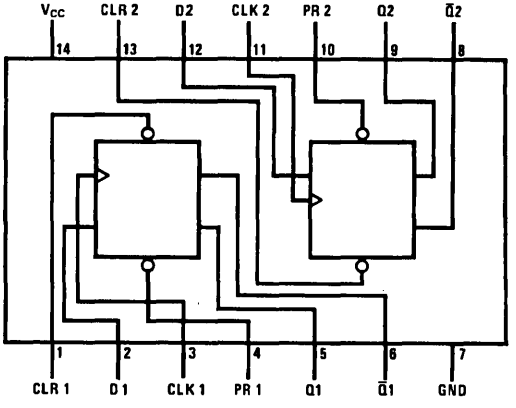
DM5474/DM7474 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6526–1

Order Number DM5474J, DM7474M or DM7474N
See NS Package Number J14A, M14A or N14A

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going transition of the clock.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM5474			DM7474			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 2)		0		15	0		15	MHz
t_W	Pulse Width (Note 2)	Clock High	30			30			ns
		Clock Low	37			37			
		Clear Low	30			30			
		Preset Low	30			30			
t_{SU}	Input Setup Time (Notes 1 & 2)		20↑			20↑			ns
t_H	Input Hold Time (Notes 1 & 2)		5↑			5↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	D			40	μA
			Clock			80	
			Clear			120	
			Preset			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V (Note 6)	D			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
			Preset			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)			17	30	mA

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time.

Note 5: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock is grounded.

Note 6: Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns

National Semiconductor Corporation

DM5475/DM7475 Quad Latches

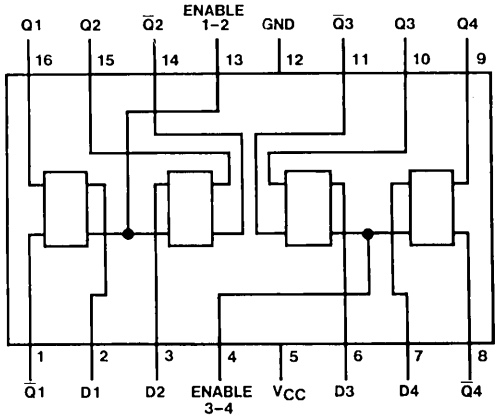
General Description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q input when the enable (G) is high, and the Q output will follow the data input as long as the enable remains high. When the enable goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the enable is permitted to go high.

These latches feature complementary Q and $\overline{Q}$ outputs from a 4-bit latch and are available in 16-pin packages.

Connection Diagram

Dual-In-Line Package



TL/F/6527–1

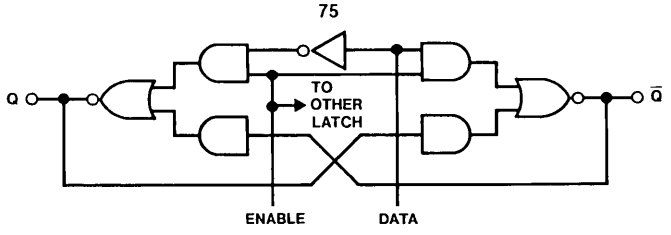
Order Number DM5475J or DM7475N
See NS Package Number J16A or N16A

Function Table (Each Latch)

Inputs		Outputs	
D	G	Q	$\overline{Q}$
L	H	L	H
H	H	H	L
X	L	Q_0	$\overline{Q}_0$

H = High Level, L = Low Level, X = Don't Care, Q_0 = The Level of Q Before the High-to-Low Transition of G

Logic Diagram (Each Latch)



TL/F/6527–2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5475			DM7475			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
t_W	Enable Pulse Width (Note 4)	20			20			ns
t_{SU}	Setup Time (Note 4)	20			20			ns
t_H	Hold Time (Note 4)	5			5			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		32	46	mA
			DM74		32	50	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PHL}	Propagation Delay Time High to Low Level Output	D to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to Q		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D to $\overline{Q}$		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D to $\overline{Q}$		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	G to Q		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	G to Q		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	G to $\overline{Q}$		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	G to $\overline{Q}$		30	ns

National Semiconductor Corporation

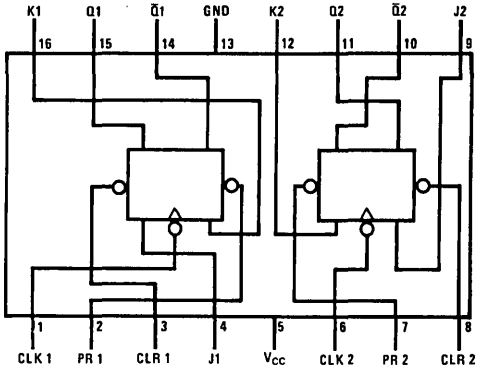
DM5476/DM7476 Dual Master-Slave J-K Flip-Flops with Clear, Preset, and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic state of J and K inputs must not be allowed to change while the clock is high. The data is transfered to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6528–1

Order Number DM5476J or DM7476N
See NS Package Number J16A or N16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

H = High Logic Level

L = Low Logic Level

X = Either Low or High Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transfered to the outputs on the falling edge of the clock pulse.

* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.

Q_0 = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete active high level clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM5476			DM7476			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 6)		0		15	0		15	MHz
t_W	Pulse Width (Note 6)	Clock High	20			20			ns
		Clock Low	47			47			
		Preset Low	25			25			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Notes 1 & 6)		0↑			0↑			ns
t_H	Input Hold Time (Notes 1 & 6)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
			Preset			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V (Note 5)	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
			Preset			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			18	34	mA

Note 1: The symbol (↑, ↓) indicates the edge of the clock pulse is used for reference (↑) for rising edge, (↓) for falling edge.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Note 5: Clear is measured with preset high and preset is measured with clear high.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns

National Semiconductor Corporation

DM5485/DM7485 4-Bit Magnitude Comparators

General Description

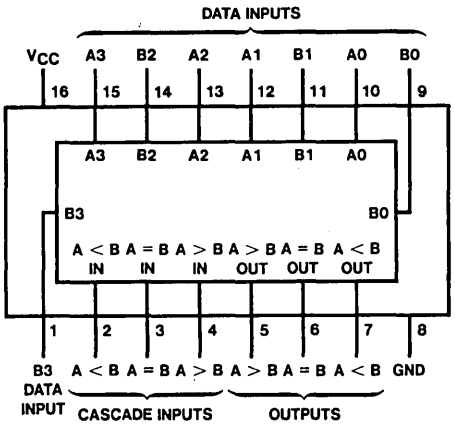
These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A = B input. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long words.

Features

- Typical power dissipation 275 mW
- Typical delay (4-bit words) 23 ns

Connection Diagram

Dual-In-Line Package



TL/F/6530–1

Order Number DM5485J or DM7485N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5485			DM7485			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	A < B			40	μA
			A > B			40	
			Others			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A < B			−1.6	mA
			A > B			−1.6	
			Others			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			55	88	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, A = B input grounded and all other inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

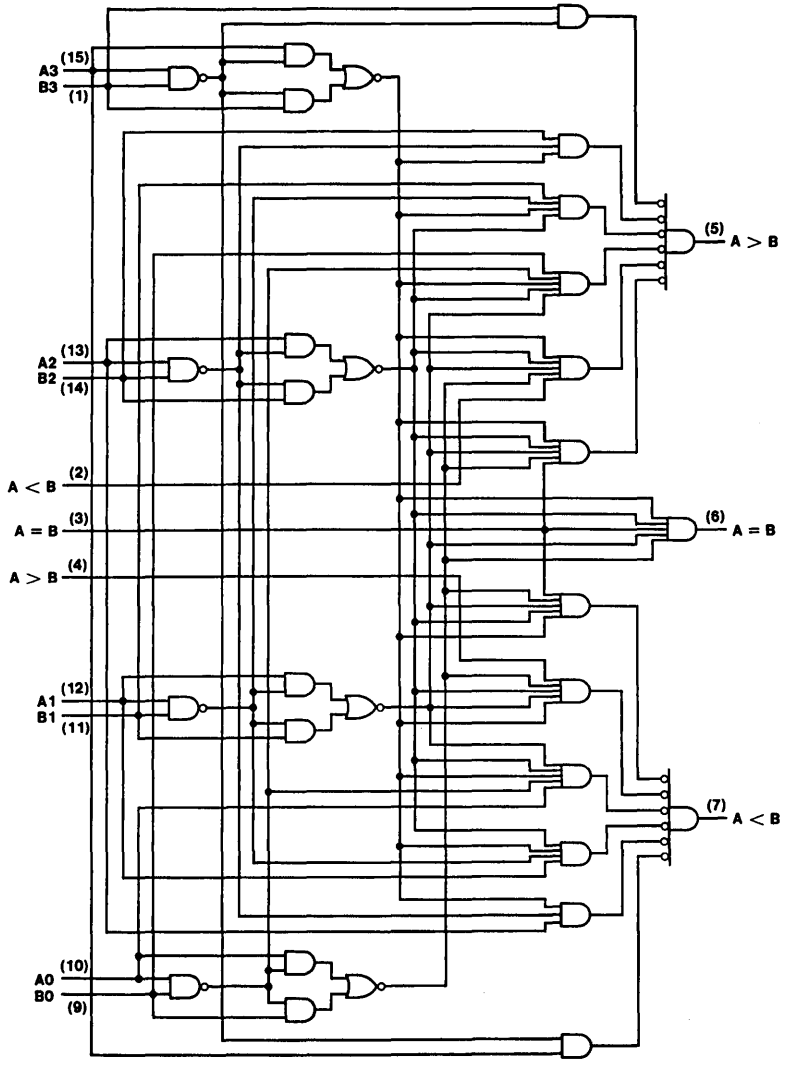
Symbol	Parameter	From Input	To Output	Number of Gate Levels	R_L = 400Ω, C_L = 15 pF		Units
					Min	Max	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	Any A or B Data Input	A < B, A > B	3		26	ns
			A = B	4		35	
t_{PHL}	Propagation Delay Time High-to-Low Level Output	Any A or B Data Input	A < B, A > B	3		30	ns
			A = B	4		30	
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A < B or A = B	A > B	1		11	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A < B or A = B	A > B	1		17	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A = B	A = B	2		20	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A = B	A = B	2		17	ns
t_{PLH}	Propagation Delay Time Low-to-High Level Output	A > B or A = B	A < B	1		11	ns
t_{PHL}	Propagation Delay Time High-to-Low Level Output	A > B or A = B	A < B	1		17	ns

Function Table

Comparing Inputs				Cascading Inputs			Outputs		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = High Level, L = Low Level, X = Don't Care

Logic Diagram



TL/F/6530–2

National Semiconductor Corporation

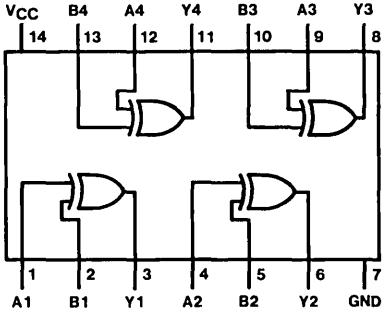
DM5486/DM7486 Quad 2-Input Exclusive-OR Gates

General Description

This device contains four independent gates each of which performs the logic exclusive-OR function.

Connection Diagram

Dual-In-Line Package



TL/F/6531–1

Order Number DM5486J or DM7486N
See NS Package Number J14A or N14A

Function Table

$Y = A \oplus B$

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM5486			DM7486			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54		30	43	mA
			DM74		30	50	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)			36	57	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with all outputs open, one input of each gate at 4.5V, and the other inputs grounded.

Note 4: I_{CCL} is measured with all outputs open, and all inputs at ground.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	C_L = 15 pF, R_L = 400Ω		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input Low		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			17	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Other Input High		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			22	ns

National Semiconductor Corporation

DM5490A/DM7490A, DM5493A/DM7493A Decade, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-five for the 90A and divide-by-eight for the 93A.

All of these counters have a gated zero reset and the 90A also has gated set-to-nine inputs for use in BCD nine's complement applications.

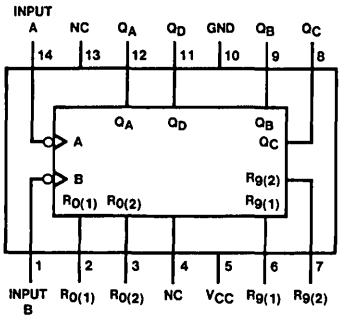
To use their maximum count length (decade or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table. A symmetrical divide-by-ten count can be obtained from the 90A counters by connecting the Q_D output to the A input and applying the input count to the B input which gives a divide-by-ten square wave at output Q_A.

Features

- Typical power dissipation
  - — 90A 145 mW
  - — 93A 130 mW
- Count frequency 42 MHz

Connection Diagrams

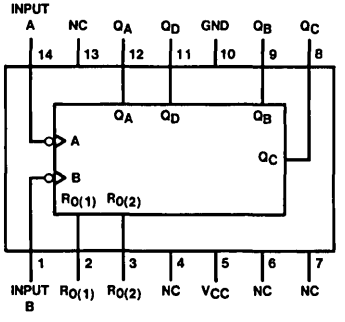
Dual-In-Line Package



TL/F/6533–1

Order Number DM5490AJ or DM7490AN
See NS Package Number J14A or N14A

Dual-In-Line Package



TL/F/6533–2

Order Number DM5493AJ or DM7493N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM5490A			DM7490A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)	A	0		32	0		32	MHz
		B	0		16	0		16	
t_W	Pulse Width (Note 5)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time (Note 5)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'90A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.7V	A			80	μA
			Reset			40	
			B			120	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	A			−3.2	mA
			Reset			−1.6	
			B			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			29	42	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both RO inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 5: T_A = 25°C and V_{CC} = 5V.

'90A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		MHz
		B to Q_B	16		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		50	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	SET-9 to Q_A, Q_D		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-9 to Q_B, Q_C		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 Any Q		40	ns

Recommended Operating Conditions

Symbol	Parameter		DM5493A			DM7493A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)	A	0		32	0		32	MHz
		B	0		16	0		16	
t_W	Pulse Width (Note 5)	A	15			15			ns
		B	30			30			
		Reset	15			15			
t_{REL}	Reset Release Time (Note 5)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'93A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max (Note 4)			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Reset			40	μA
			A			80	
			B			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Reset			−1.6	mA
			A			−3.2	
			B			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			26	39	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, both R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

Note 4: Q_A outputs are tested at I_{OL} = Max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 5: T_A = 25°C and V_{CC} = 5V.

'93A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	32		MHz
		B to Q_B	16		
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_A		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_A		18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		70	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_B		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_B		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_C		32	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_C		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q_D		51	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to Q_D		51	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	SET-0 to Any Q		40	ns

Function Tables (Note D)

90A
BCD Count Sequence
(See Note A)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

90A
BCD Bi-Quinary (5-2)
(See Note B)

Count	Outputs			
	Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

93A
Count Sequence
(See Note C)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

90A
Reset/Count Function Table

Reset Inputs				Outputs			
R0(1)	R0(2)	R9(1)	R9(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L		COUNT		
L	X	L	X		COUNT		
L	X	X	L		COUNT		
X	L	L	X		COUNT		

93A
Reset/Count Function Table

Reset Inputs		Outputs			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X		COUNT		
X	L		COUNT		

Note A: Output Q_A is connected to input B for BCD count.

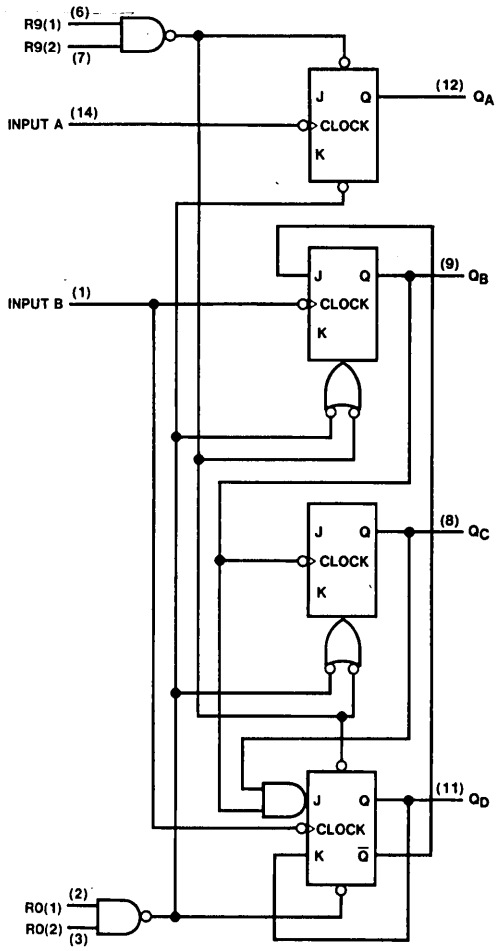
Note B: Output Q_D is connected to input A for bi-quinary count.

Note C: Output Q_A is connected to input B.

Note D: H = High Level, L = Low Level, X = Don't Care.

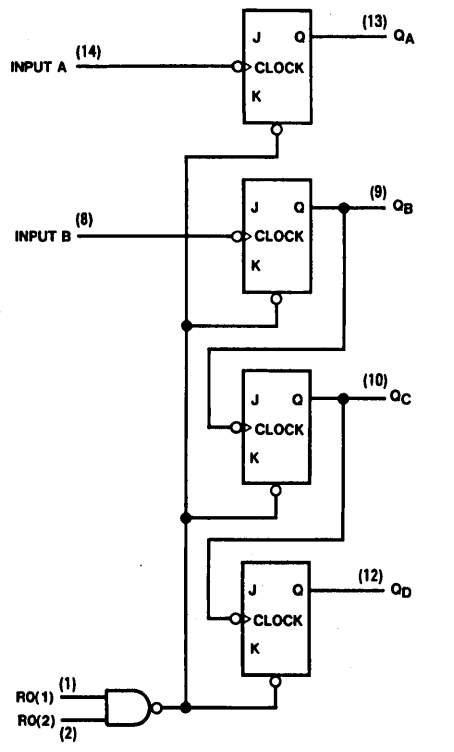
Logic Diagrams

90A



TL/F/6533–3

93A



TL/F/6533–4

The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor Corporation

DM5495/DM7495 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source.

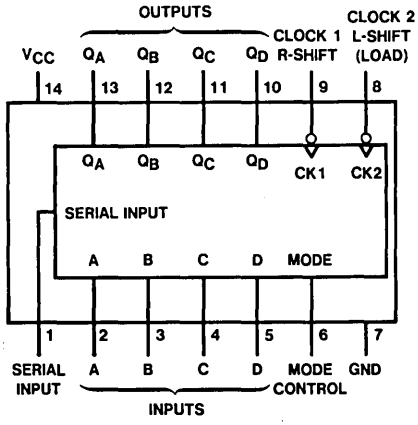
Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

Features

- Typical maximum clock frequency 36 MHz
- Typical power dissipation 250 mW

Connection Diagram

Dual-In-Line Package



TL/F/6534–1

Order Number DM5495J or DM7495N
See NS Package Number J14A or N14A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM5495			DM7495			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Clock Pulse Width (Note 4)		15	11		15			ns
t_{SU}	Data Setup Time (Note 4)		20	10		20	10		ns
t_{EN}	Time to Enable Clock (Note 4)	Clock 1	20			20			ns
		Clock 2	15			15			
t_H	Data Hold Time (Note 4)		0	−10		0	−10		ns
t_{IN}	Time to Inhibit Clock 1 or Clock 2 (Note 4)		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Mode			80	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Mode			−3.2	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−18		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	75	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded: Mode Control at 4.5V: and a momentary 3V, then ground, applied to both clock inputs.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		35	ns

Function Table

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2(L)	1(R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	$Q_{B\dagger}$	$Q_{C\dagger}$	$Q_{D\dagger}$	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

†Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.

H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions)

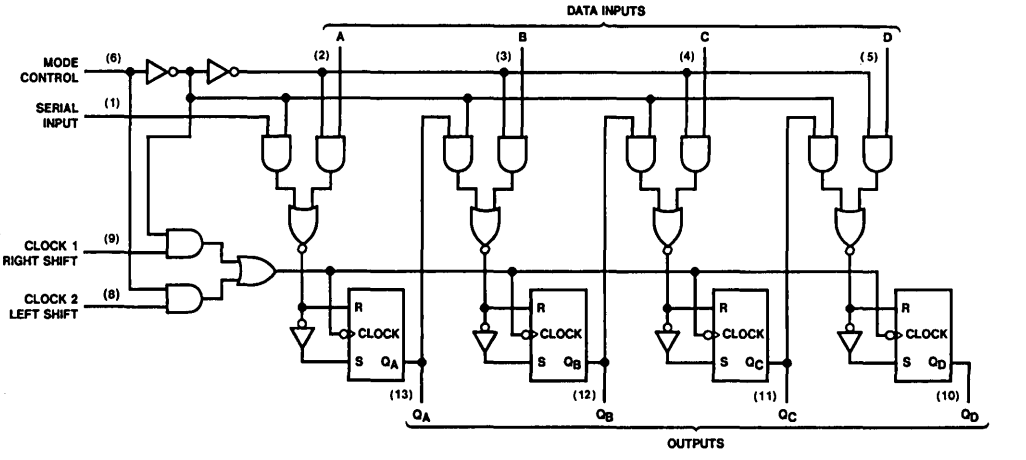
↓ = Transition from high to low level, ↑ = Transition from low to high level

a, b, c, d = The level of steady, state input at inputs A, B, C, or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, Q_D, respectively, before the most recent ↓ transition of the clock.

Logic Diagram



TL/F/6534-2

National Semiconductor Corporation

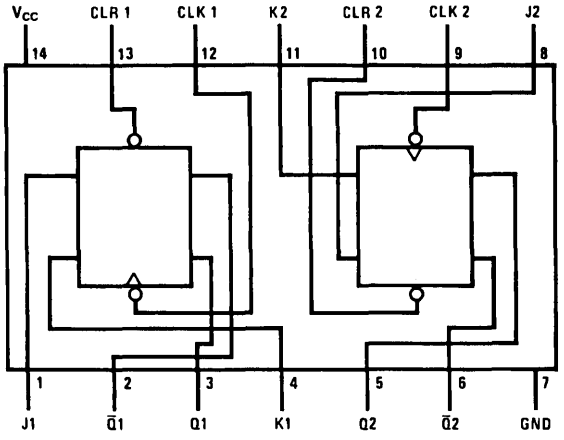
DM54107/DM74107 Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the output regardless of the logic states of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6536–1

Order Number DM54107J or DM74107N
See NS Package Number J14A or N14A

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\overline{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete positive clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54107			DM74107			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)		0	20	15	0	20	15	MHz
t_W	Pulse Width (Note 5)	Clock High	20			20			ns
		Clock Low	47			47			
		Clear Low	25			25			
t_{SU}	Input Setup Time (Notes 1 & 5)		0↑			0↑			ns
t_H	Input Hold Time (Notes 1 & 5)		0↓			0↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			40	μA
			Clock			80	
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	J, K			−1.6	mA
			Clock			−3.2	
			Clear			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max, (Note 4)			18	34	mA

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse is used for reference: (↑) for rising edge, (↓) for falling edge.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		15		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		25	ns

National Semiconductor Corporation

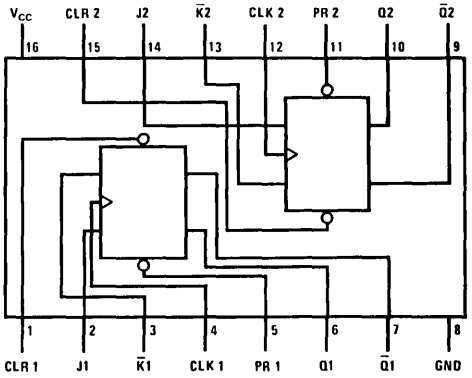
DM54109/DM74109 Dual Positive-Edge-Triggered J-$\overline{K}$ Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered J-$\overline{K}$ flip-flops with complementary outputs. The J and $\overline{K}$ data is accepted by the flip-flop on the rising edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the J and $\overline{K}$ inputs may be changed while the clock is high or low as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6537–1

Order Number DM54109J or DM74109N
See NS Package Number J16A or N16A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	Toggle	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = High Logic Level

L = Low Logic Level

↑ = Rising Edge of Pulse.

* = This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

Q_0 = The output logic level of Q before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each active transition of the clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54109			DM74109			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−1.2			−1.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 6)		0		30	0		30	MHz
t_W	Pulse Width (Note 6)	Clock High	20			20			ns
		Clock Low	20			20			
		Preset Low	20			20			
		Clear Low	20			20			
t_{SU}	Input Setup Time (Notes 1 & 6)		15 ↑			15 ↑			ns
t_H	Input Hold Time (Notes 1 & 6)		10 ↓			10 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, $\overline{K}$			40	μA
			Preset			80	
			Clock			80	
			Clear			160	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V (Note 5)	J, $\overline{K}$			−1.6	mA
			Preset			−3.2	
			Clock			−3.2	
			Clear			−4.8	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−30		−85	mA
			DM74	−30		−85	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			20	30	mA

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input grounded.

Note 5: Clear is tested with preset high and preset is tested with clear high.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		29	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$		28	ns

National Semiconductor Corporation

DM54121/DM74121 One-Shot with Clear and Complementary Outputs

General Description

The DM54/74121 is a monostable multivibrator featuring both positive and negative edge triggering with complementary outputs. An internal 2kΩ timing resistor is provided for design convenience minimizing component count and layout problems. This device can be used with a single external capacitor. Inputs (A) are active-low trigger transition inputs and input (B) is an active-high transition Schmitt-trigger input that allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second. A high immunity to V_{CC} noise of typically 1.5V is also provided by internal circuitry at the input stage.

To obtain optimum and trouble free operation please read operating rules and NSC one-shot application notes carefully and observe recommendations.

Features

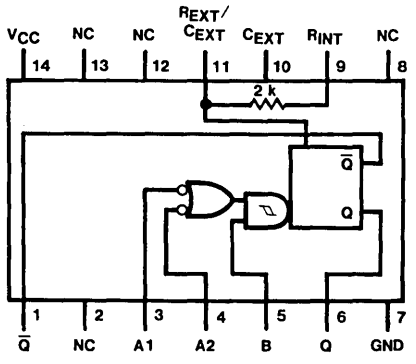
- Triggered from active-high transition or active-low transition inputs
- Variable pulse width from 30 ns to 28 seconds
- Jitter free Schmitt-trigger input
- Excellent noise immunity typically 1.2V
- Stable pulse width up to 90% duty cycle
- TTL, DTL compatible
- Compensated for V_{CC} and temperature variations
- Input clamp diodes

Functional Description

The basic output pulse width is determined by selection of an internal resistor R_{INT} or an external resistor (R_X) and capacitor (C_X). Once triggered the output pulse width is independent of further transitions of the inputs and is a function of the timing components. Pulse width can vary from a few nano-seconds to 28 seconds by choosing appropriate R_X and C_X combinations. There are three trigger inputs from the device, two negative edge-triggering (A) inputs, one positive edge Schmitt-triggering (B) input.

Connection Diagram

Dual-In-Line Package



TL/F/6538–1

Order Number DM54121J or DM74121N
See NS Package Number J14A or N14A

Function Table

Inputs			Outputs	
A1	A2	B	Q	$\overline{Q}$
L	X	H	L	H
X	L	H	L	H
X	X	L	L	H
H	H	X	L	H
H	↓	H	⎍	⎎
↓	H	H	⎍	⎎
↓	↓	H	⎍	⎎
L	X	↑	⎍	⎎
X	L	↑	⎍	⎎

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⎍ = A Positive Pulse
⎎ = A Negative Pulse

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54121			DM74121			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage at the A Input (V_{CC} = Min)		1.4	2		1.4	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the A Input (V_{CC} = Min)	0.8	1.4		0.8	1.4		V
V_{T+}	Positive-Going Input Threshold Voltage at the B Input (V_{CC} = Min)		1.5	2		1.5	2	V
V_{T-}	Negative-Going Input Threshold Voltage at the B Input (V_{CC} = Min)	0.8	1.3		0.8	1.3		V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
t_W	Input Pulse Width (Note 1)	50			50			ns
dV/dt	Rate of Rise or Fall of Schmidt Input (B) (Note 1)			1			1	V/s
dV/dt	Rate of Rise or Fall of Logic Input (A) (Note 1)			1			1	V/μs
R_{EXT}	External Timing Resistor (Note 1)	1.4		30	1.4		40	kΩ
C_{EXT}	External Timing Capacitance (Note 1)	0		1000	0		1000	μF
DC	Duty Cycle (Note 1) R_T = 2 kΩ			67			67	%
	Duty Cycle (Note 1) $R_T = R_{EXT}$ (Max)			90			90	%
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	A1, A2			40	μA
			B			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A1, A2			−1.6	mA
			B			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	mA
I_{CC}	Supply Current	V_{CC} = Max	Quiescent		13	25	mA
			Triggered		23	40	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Outout Load)

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	A1, A2 to Q	C_{EXT} = 80 pF, R_{INT} to V_{CC}, C_L = 15 pF, R_L = 400Ω		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q			55	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A1, A2 to $\overline{Q}$			80	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$			65	ns
$t_{W(OUT)}$	Output Pulse Width Using the Internal Timing Resistor	A1, A2 or B to Q, $\overline{Q}$	C_{EXT} = 80 pF, R_{INT} to V_{CC}, R_L = 400Ω, C_L = 15 pF	70	150	ns
$t_{W(OUT)}$	Output Pulse Width Using Zero Timing Capacitance	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 0 pF, R_{INT} to V_{CC}, R_L = 400Ω, C_L = 15 pF		50	ns
$t_{W(OUT)}$	Output Pulse Width Using External Timing Resistor	A1, A2 to Q, $\overline{Q}$	C_{EXT} = 100 pF, R_{INT} = 10 kΩ, R_L = 400Ω, C_L = 15 pF	600	800	ns
		A1, A2 to Q, $\overline{Q}$	C_{EXT} = 1 μF, R_{INT} = 10 kΩ, R_L = 400Ω, C_L = 15 pF	6	8	ms

Operating Rules

1. To use the internal 2 kΩ timing resistor, connect the R_{INT} pin to V_{CC}.
2. An external resistor (R_X) or the internal resistor (2 kΩ) and an external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants use high-quality mica, glass, polypropylene, polycarbonate, or polystyrene capacitors. For large time constants use solid tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
3. The pulse width is essentially determined by external timing components R_X and C_X. For C_X < 1000 pF see *Figure 1* design curves on T_W as function of timing components value. For C_X > 1000 pF the output is defined as:

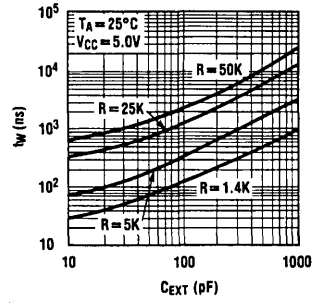
   $t_W = K R_X C_X$

   where [R_X is in Kilo-ohm]

   [C_X is in pico Farad]

   [T_W is in nano second]

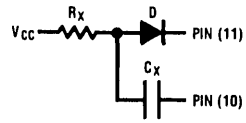
   [K ≈ 0.7]



TL/F/6538–2

FIGURE 1

4. If C_X is an electrolytic capacitor a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current *(Figure 2)*.

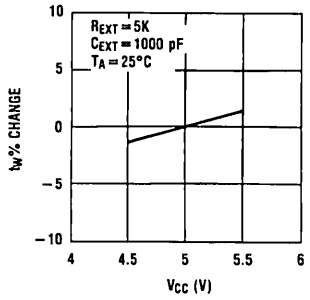


TL/F/6538–3

FIGURE 2

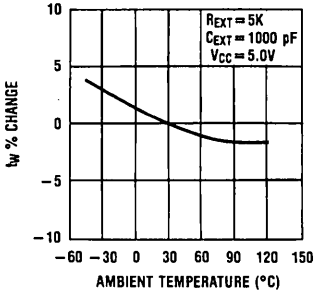
Operating Rules (Continued)

5. Output pulse width versus V_{CC} and operation temperatures: *Figure 3* depicts the relationship between pulse width variation versus V_{CC}. *Figure 4* depicts pulse width variation versus ambient temperature.



TL/F/6538–4

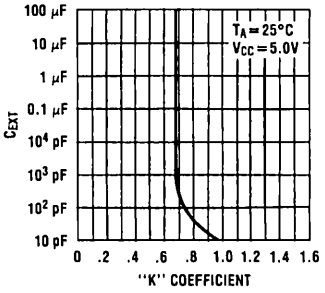
FIGURE 3



TL/F/6538–5

FIGURE 4

6. The "K" coefficient is not a constant, but varies as a function of the timing capacitor C_X. *Figure 5* details this characteristic.



TL/F/6538–6

FIGURE 5

7. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I × R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (10) and (11) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
8. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 µF to 0.10 µF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

For further detailed device characteristics and output performance please refer to the NSC one-shot application note, AN-366.

4

National Semiconductor Corporation

DM54123/DM74123 Dual Retriggerable One-Shot with Clear and Complementary Outputs

General Description

The DM54/74123 is a dual retriggerable monostable multivibrator capable of generating output pulses from a few nano-seconds to extremely long duration up to 100% duty cycle. Each device has three inputs permitting the choice of either leading-edge or trailing edge triggering. Pin (A) is an active-low transition trigger input and pin (B) is an active-high transition trigger input. The clear (CLR) input terminates the output pulse at a predetermined time independent of the timing components.

National's '123 device features a unique logic realization not implemented by other manufacturers. The "Clear" input will not trigger the device, a design tailored for applications where it shall only terminate or reduce a timing pulse.

To obtain the best and trouble free operation from this device please read the operating rules as well as the NSC one-shot application notes carefully and observe recommendations.

Features

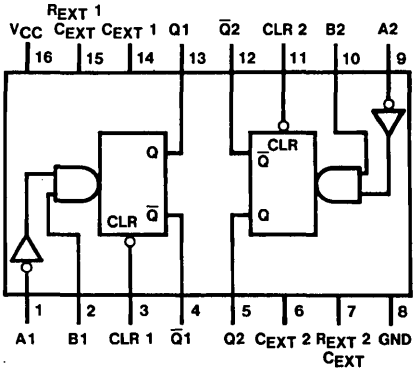
- DC triggered from active-high transition or active-low transition inputs
- Retriggerable to 100% duty cycle
- Direct reset terminates output pulse
- Compensated for V_{CC} and temperature variations
- DTL, TTL compatible
- Input clamp diodes

Functional Description

The basic output pulse width is determined by selection of an external resistor (R_X) and capacitor (C_X). Once triggered, the basic pulse width may be extended by retriggering the gated active-low transition or active-high transition inputs or be reduced by use of the active-low transition clear input. Retriggering to 100% duty cycle is possible by application of an input pulse train whose cycle time is shorter than the output cycle time such that a continuous "HIGH" logic state is maintained at the "Q" output.

Connection Diagram

Dual-In-Line Package



TL/F/6539–1

Order Number DM54123J or DM74123N
See NS Package Number J16A or N16A

Function Table

Inputs			Outputs	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
H	H	X	L	H
H	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H = High Logic Level
L = Low Logic Level
X = Can Be Either Low or High
↑ = Positive Going Transition
↓ = Negative Going Transition
⎍ = A Positive Pulse
⎎ = A Negative Pulse

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54123			DM74123			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	Pulse Width (Note 5)	A or B High	40			40			ns
		A or B Low	40			40			
		Clear Low	40			40			
T_{WQ} (Min)	Minimum Width of Pulse at Q (Note 5)	A or B			76			65	ns
R_{EXT}	External Timing Resistor		5		25	5		50	kΩ
C_{EXT}	External Timing Capacitance		No Restriction			No Restriction			μF
C_{WIRE}	Wiring Capacitance at R_{EXT}/C_{EXT} Terminal (Note 5)				50			50	pF
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.5	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Data			40	μA
			Clear			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−10		−40	mA
			DM74	−10		−40	
I_{CC}	Supply Current	V_{CC} = Max (Notes 3 and 4)			46	66	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: Quiescent I_{CC} is measured (after clearing) with 2.4V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 KΩ.

Note 4: I_{CC} is measured in the triggered state with 2.4V applied to all clear and B inputs, A inputs grounded, all outputs open, C_{EXT} = 0.02 μF, and R_{EXT} = 25 kΩ.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω				Units
			C_L = 15 pF, C_{EXT} = 0 pF, R_{EXT} = 5 kΩ		C_L = 15 pF, C_{EXT} = 1000 pF, R_{EXT} = 10 KΩ		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q		33			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	B to Q		28			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to $\overline{Q}$		40			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	B to $\overline{Q}$		36			ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		40			ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		27			ns
$t_{W(out)}$	Output Pulse Width	A or B to Q			3.08	3.76	μs

Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required for proper operation. The value of C_X may vary from 0 to any necessary value. For small time constants high-grade mica, glass, polypropylene, polycarbonate, or polystyrene material capacitors may be used. For large time constants use tantalum or special aluminum capacitors. If the timing capacitors have leakages approaching 100 nA or if stray capacitance from either terminal to ground is greater than 50 pF the timing equations may not represent the pulse width the device generates.
2. When an electrolytic capacitor is used for C_X a switching diode is often required for standard TTL one-shots to prevent high inverse leakage current *(Figure 2)*. However, its use in general is not recommended with retriggerable operation.
3. The output pulse width (T_W) for C_X > 1000 pF is defined as follows:

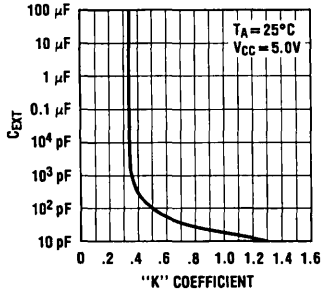
   $T_W = K R_X C_X (1 + 0.7/R_X)$

   where [R_X is in Kilo-ohm]

   [C_X is in pico Farad]

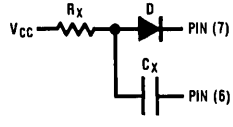
   [T_W is in nano second]

   [$K \approx 0.34$]
4. The multiplicative factor K is plotted as a function of C_X below for design considerations:



TL/F/6539–2

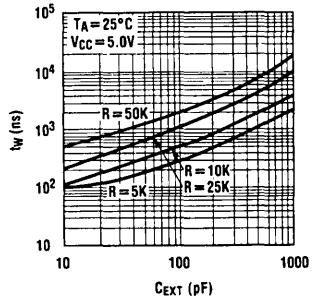
FIGURE 1



TL/F/6539–3

FIGURE 2

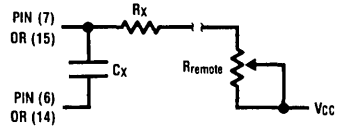
5. For C_X < 1000 pF see *Figure 3* for T_W vs C_X family curves with R_X as a parameter:



TL/F/6539–4

FIGURE 3

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



TL/F/6539–5

Note: "R_{remote}" should be as close to the one-shot as possible.

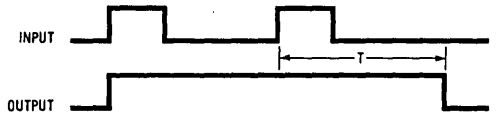
FIGURE 4

Operating Rules (Continued)

7. The retriggerable pulse width is calculated as shown below:

$$T = T_W + t_{PLH} = K \times R_X \times C_X + t_{PLH}$$

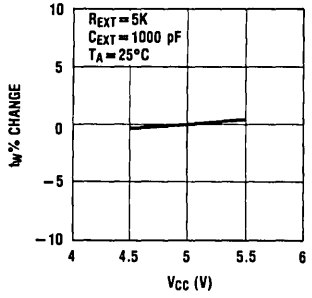
The retriggered pulse width is equal to the pulse width plus a delay time period *(Figure 5)*.



TL/F/6539–6

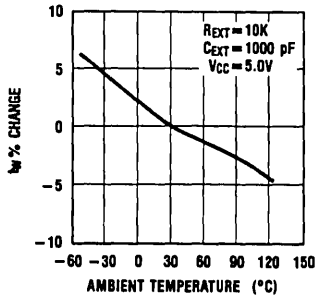
FIGURE 5

8. Output pulse width versus V_{CC} and Temperatures: *Figure 6* depicts the relationship between pulse width variation versus operating V_{CC}. *Figure 7* depicts pulse width variation versus ambient temperatures.



TL/F/6539–7

FIGURE 6



TL/F/6539–8

FIGURE 7

9. Under any operating condition C_X and R_X must be kept as close to the one-shot device pins as possible to minimize stray capacitance, to reduce noise pick-up, and to reduce I × R and Ldi/dt voltage developed along their connecting paths. If the lead length from C_X to pins (6) and (7) or pins (14) and (15) is greater than 3 cm, for example, the output pulse width might be quite different from values predicted from the appropriate equations. A non-inductive and low capacitive path is necessary to ensure complete discharge of C_X in each cycle of its operation so that the output pulse width will be accurate.
10. The C_{EXT} pins of this device are internally connected to the internal ground. For optimum system performance they should be hard wired to the system's return ground plane.
    * However, it should be noted that although the 74221 series one-shot is pin-for-pin compatiable with the '123 device, its C_{EXT} pin is not an internal connection to ground. Hence, if substitution of an '221 on to an '123 design layout whose C_{EXT} pin is wired to the ground is attempted, the '221 device will not function!
11. V_{CC} and ground wiring should conform to good high-frequency standards and practices so that switching transients on the V_{CC} and ground return leads do not cause interaction between one-shots. A 0.01 μF to 0.10 μF bypass capacitor (disk ceramic or monolithic type) from V_{CC} to ground is necessary on each device. Furthermore, the bypass capacitor should be located as close to the V_{CC} pin as space permits.

***For further detailed device characteristics and output performance please refer to the NSC one-shot application note, AN-366.**

National Semiconductor Corporation

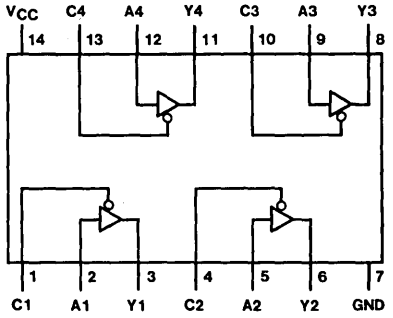
DM54125/DM74125 Quad TRI-STATE® Buffers

General Description

This device contains four independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability at the high Logic level to permit the driving of bus lines without external pull-up resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6540–1

Order Number DM54125J or DM74125N
See NS Package Number J14A or N14A

Function Table

$Y = A$

Inputs		Output
A	C	Y
L	L	L
H	L	H
X	H	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54125			DM74125			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{IZL}	Off-State Input Current with Low Level Input Voltage Applied	V_{CC} = Max, V_I = 0.4V				−40	μA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−30		−70	mA
			DM74	−28		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			36	54	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the output control (C) inputs at 4.5V, the data inputs grounded, and the outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				18	ns
t_{PZH}	Output Enable Time to High Level Output				18	ns
t_{PZL}	Output Enable Time to Low Level Output				25	ns
t_{PHZ}	Output Disable Time from High Level Output		8			ns
t_{PLZ}	Output Disable Time from Low Level Output		14			ns

National Semiconductor Corporation

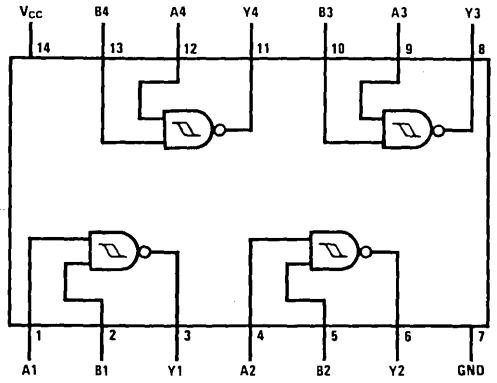
DM54132/DM74132 Quad 2-Input NAND Gates with Schmitt Trigger Inputs

General Description

This device contains four independent gates each of which performs the logic NAND function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter-free output.

Connection Diagram

Dual-In-Line Package



TL/F/6542–1

Order Number DM54132J or DM74132N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54132			DM74132			Units
		Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.7	2	1.5	1.7	2	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.9	1.1	0.6	0.9	1.1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_I = V_{T-}Min	DM54	2.4	3.4		V
			DM74	2.4	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_I = V_{T+}Max			0.2	0.4	V
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T+}			−0.43		mA
I_{T-}	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}			−0.56		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.8	−1.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−18		−55	mA
			DM74	−18		−55	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			15	24	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			26	40	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω, C_L = 15 pF		Units
		Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		22	ns

National Semiconductor Corporation

DM54141/DM74141 BCD to Decimal Decoders/Drivers

General Description

The DM54141/DM74141 is a BCD-to-decimal decoder designed to drive cold-cathode indicator tubes.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the DM54141/DM74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display.

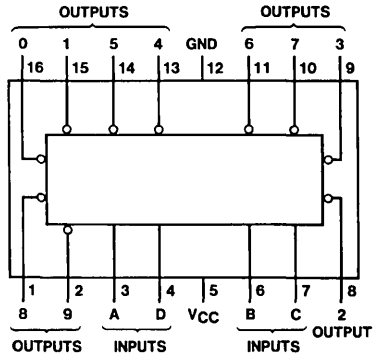
Input clamp diodes are also provided to clamp negative-voltage transitions in order to minimize transmission-line effects.

Features

- Drive cold-cathode, numeric indicator tubes directly
- Fully decoded inputs
- Low leakage current 50 μA @ 55V
- Low power dissipation 55 mW typical

Connection Diagram

Dual-In-Line Package



TL/F/6543–1

Order Number DM54141J or DM74141N
See NS Package Number J16A or N16A

Function Table

Inputs				Output
D	C	B	A	On*
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
(Over Range)				
H	L	H	L	None
H	L	H	H	None
H	H	L	L	None
H	H	L	H	None
H	H	H	L	None
H	H	H	H	None

H = High Level, L = Low Level

* All other outputs are off

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54141			DM74141			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OL}	Low Level Output Current			7			7	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = 0.5 mA		60			V
I_{OH}	Off-State Reverse Current for Input Counts 10–15	V_{CC} = Min, V_O = 30V	T_A = −55°C			5	μA
			T_A = 70°C			15	
I_{OH}	Off-State Reverse Current for Input Counts 0–9	V_{CC} = Min, V_O = 55V				50	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	T_A = −55°C to +70°C			2.5	V
			T_A = 125°C			3	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	A Input			40	μA
			B, C, D Inputs			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	A Input			−1.6	mA
			B, C, D Inputs			−3.2	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			11	25	mA

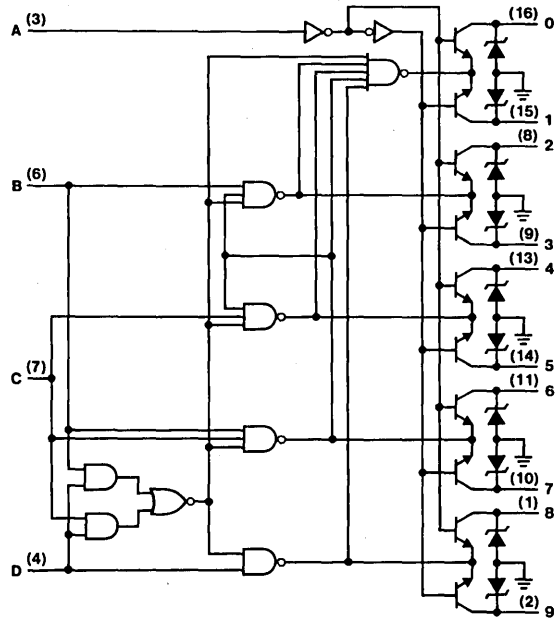
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

4

Logic Diagram

54141/74141



TL/F/6543–2

National Semiconductor Corporation

DM54145/DM74145 BCD to Decimal Decoders/Drivers

General Description

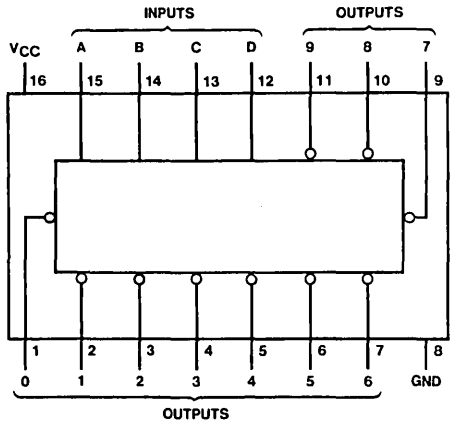
These BCD-to-decimal decoders/drivers consist of eight inverters and ten, four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of BCD input logic ensures that all outputs remain off for all invalid (10–15) binary input conditions. These decoders feature high-performance, NPN output transistors designed for use as indicator/relay drivers, or as open-collector logic-circuit drivers. The high-breakdown output transistors are compatible for interfacing with most MOS integrated circuits.

Features

- Full decoding of input logic
- 80 mA sink-current capability
- All outputs are off for invalid BCD input conditions

Connection Diagram

Dual-In-Line Package



TL/F/6544–1

Order Number DM54145J or DM74145N
See NS Package Number J16A or N16A

Function Table

No.	Inputs				Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

H = High Level (Off), L = Low Level (On)

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54145			DM74145			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			15			15	V
I_{OL}	Low Level Output Current			20			20	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_{OH} = Max V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
		I_{OL} = 80 mA V_{CC} = Min			0.5	0.9	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)	DM54		43	62	mA
			DM74		43	70	

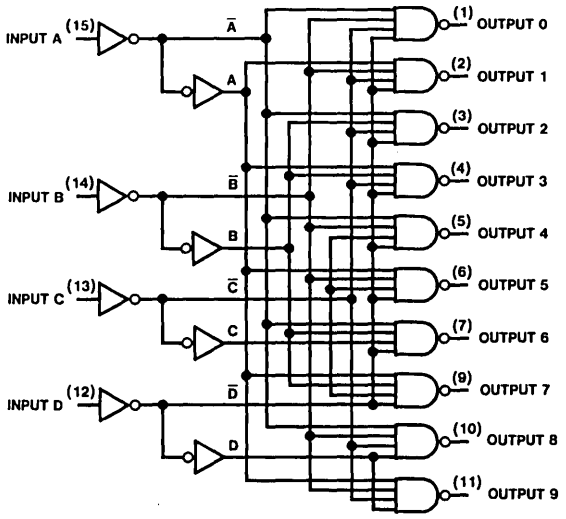
Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 100Ω		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs grounded.

Logic Diagram



TL/F/6544–2

National Semiconductor Corporation

DM54148/DM74148 Priority Encoders

General Description

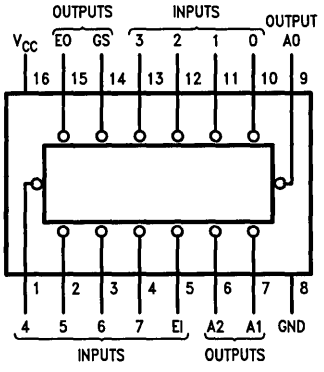
This TTL encoder features priority decoding of the input data to ensure that only the highest-order data line is encoded. The DM54148 and DM74148 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

Features

- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  N-bit encoding
  Code converters and generators

Connection Diagram

Dual-In-Line Package



TL/F/6545–1

Order Number DM54148J or DM74148N
See NS Package Number J16A or N16A

Function Table

54148/74148

Inputs									Outputs				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High Logic Level, L = Low Logic Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54148			DM74148			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	0 Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	0 Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−35		−85	mA
			DM74	−35		−85	
I_{CC1}	Supply Current	V_{CC} = Max (Note 3)			40	60	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 4)			35	55	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

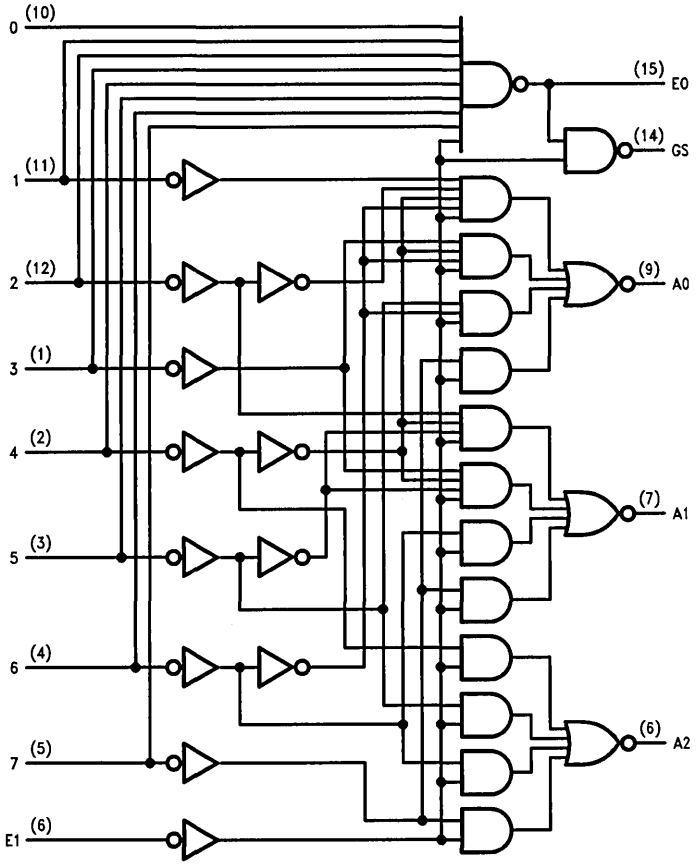
Note 3: I_{CC1} is measured with inputs E1 and 7 grounded, other inputs and outputs open.

Note 4: I_{CC2} is measured with all inputs and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Waveform	R_L = 400Ω, C_L = 15 pF		Units
				Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 9 to A0, 1, 2	In-Phase Output		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 9 to A0, 1, 2			14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 9 to A0, 1, 2	Out-of-Phase Output		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 9 to A0, 1, 2			19	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to E0	Out-of-Phase Output		10	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to E0			25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to GS	In-Phase Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to GS			25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	E1 to A0, 1, 2	In-Phase Output		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	E1 to A0, 1, 2			15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	E1 to GS	In-Phase Output		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	E1 to GS			15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	E1 to E0	In-Phase Output		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	E1 to E0			30	ns

Logic Diagram



TL/F/6545–2

National Semiconductor Corporation

DM54150/DM74150, DM54151A/DM74151A Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain full on-chip decoding to select the desired data source. The 150 selects one-of-sixteen data sources; the 151A selects one-of-eight data sources. The 150 and 151A have a strobe input which must be at a low logic level to enable these devices. A high level at the strobe forces the W output high and the Y output (as applicable) low.

The 151A features complementary W and Y outputs, whereas the 150 has an inverted (W) output only.

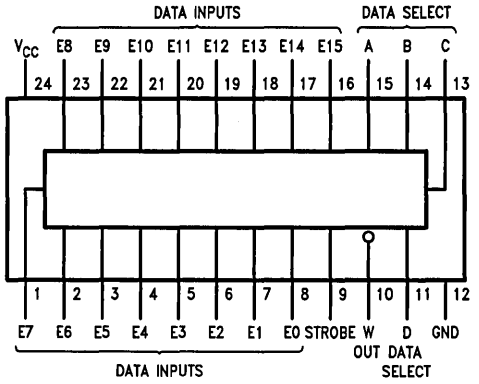
The 151A incorporates address buffers which have symmetrical propagation delay times through the complementary paths. This reduces the possibility of transients occurring at the output(s) due to changes made at the select inputs, even when the 151A outputs are enabled (i.e., strobe low).

Features

- 150 selects one-of-sixteen data lines
- 151A selects one-of-eight data lines
- Performs parallel-to-serial conversion
- Permits multiplexing from N lines to one line
- Also for use as Boolean function generator
- Typical average propagation delay time, data input to W output
  - 150 11 ns
  - 151A 9 ns
- Typical power dissipation
  - 150 200 mW
  - 151A 135 mW

Connection Diagrams

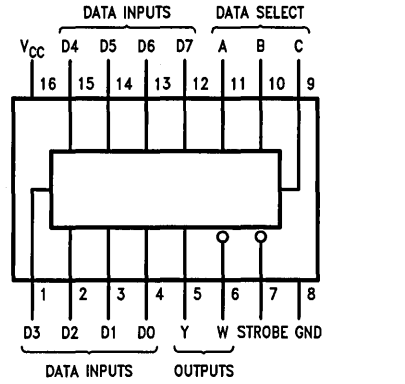
Dual-In-Line Package



TL/F/6546–1

Order Number DM54150J or DM74150N
See NS Package Number J24A or N24A

Dual-In-Line Package



TL/F/6546–2

Order Number DM54151AJ or DM74151AN
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54150			DM74150			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'150 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			40	68	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

'150 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to W		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to W		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to W		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to W		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	E0-E15 to W		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	E0-E15 to W		14	ns

Recommended Operating Conditions

Symbol	Parameter	DM54151A			DM74151A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'151A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			27	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the strobe and data select inputs at 4.5V, all other inputs and outputs open.

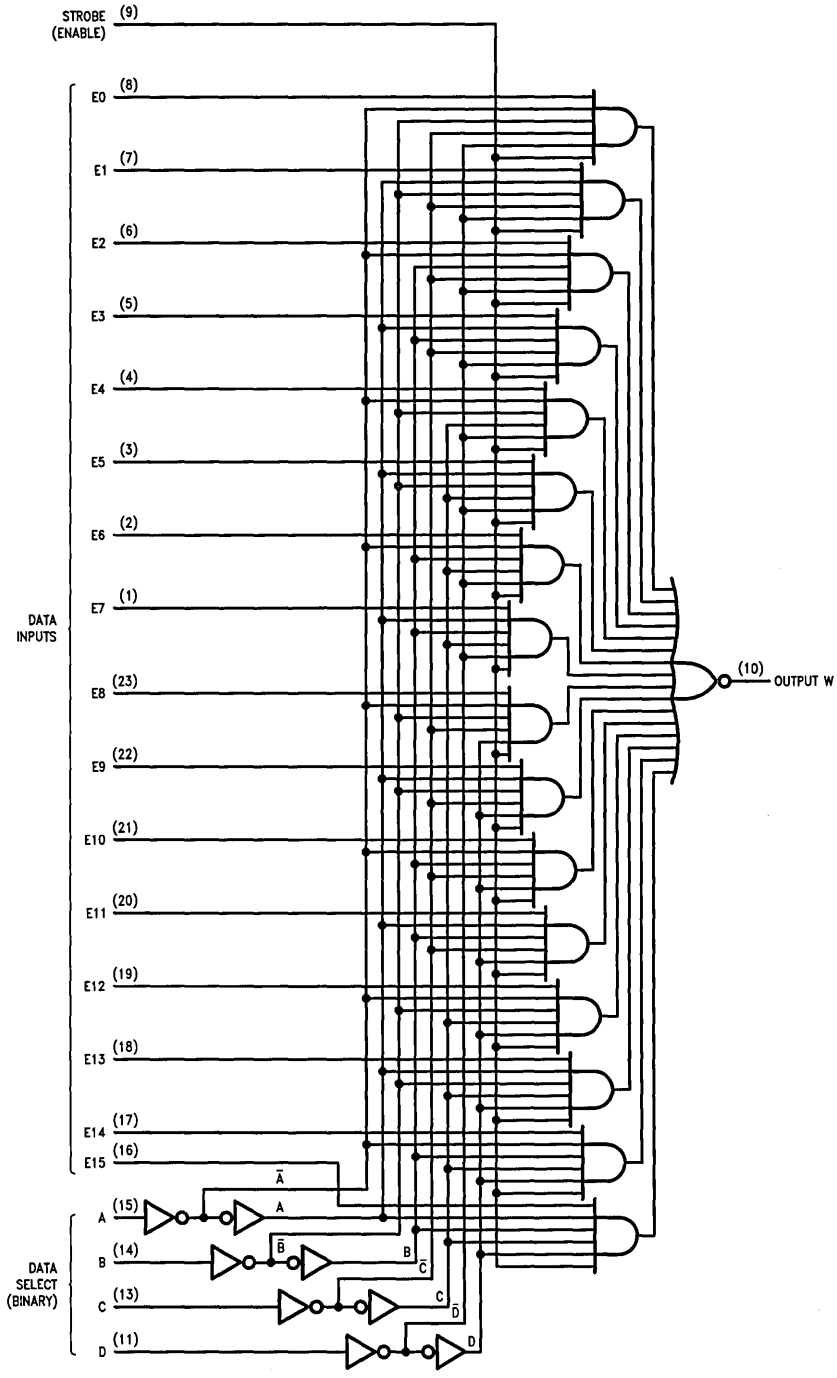
'151A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (4 Levels) to Y		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (4 Levels) to Y		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select (3 Levels) to W		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select (3 Levels) to W		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to W		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to W		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0-D7 to Y		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0-D7 to Y		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	D0-D7 to W		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	D0-D7 to W		14	ns

Logic Diagrams

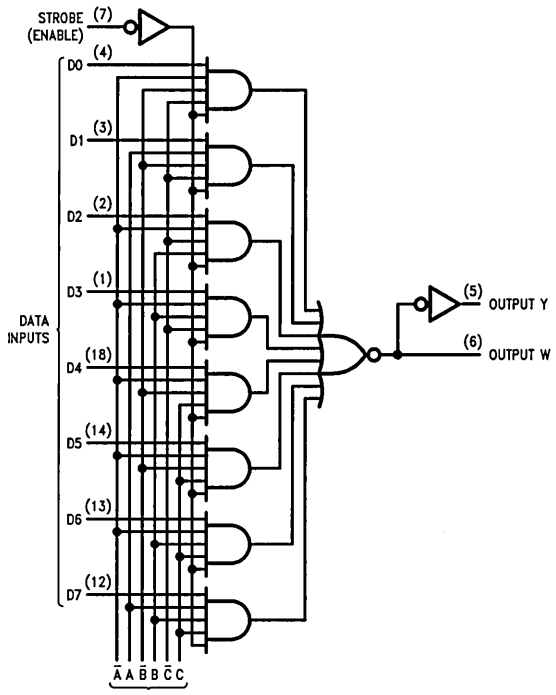
150



TL/F/6546–3

Logic Diagrams

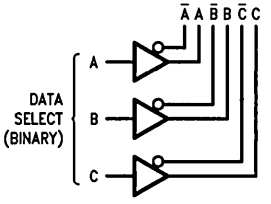
151A



TL/F/6546–4

See Address Buffers Below

Address Buffers for 54151A/74151A



TL/F/6546–5

Function Tables

54150/74150

Inputs					Outputs
Select				Strobe	
D	C	B	A	S	W
X	X	X	X	H	H
L	L	L	L	L	$\overline{E0}$
L	L	L	H	L	$\overline{E1}$
L	L	H	L	L	$\overline{E2}$
L	L	H	H	L	$\overline{E3}$
L	H	L	L	L	$\overline{E4}$
L	H	L	H	L	$\overline{E5}$
L	H	H	L	L	$\overline{E6}$
L	H	H	H	L	$\overline{E7}$
H	L	L	L	L	$\overline{E8}$
H	L	L	H	L	$\overline{E9}$
H	L	H	L	L	$\overline{E10}$
H	L	H	H	L	$\overline{E11}$
H	H	L	L	L	$\overline{E12}$
H	H	L	H	L	$\overline{E13}$
H	H	H	L	L	$\overline{E14}$
H	H	H	H	L	$\overline{E15}$

H = High Level, L = Low Level, X = Don't Care

$\overline{E0}$, $\overline{E1}$ . . . $\overline{E15}$ = the complement of the level of the respective E input

54151A/75151A

Inputs				Outputs	
Select			Strobe		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care

D0, D1 . . . D7 = the level of the respective D input

4

National Semiconductor Corporation

DM54153/DM74153 Dual 4-Line to 1-Line Data Selectors/Multiplexers

General Description

Each of these data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

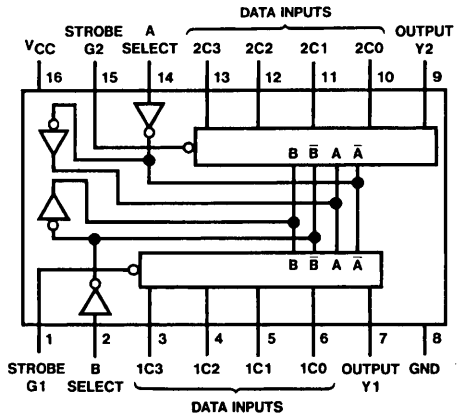
Features

- Permits multiplexing from N lines to 1 line
- Performs parallel-to-serial conversion
- Strobe (enable) line provided for cascading (N lines to n lines)
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times

  From data 11 ns
  From strobe 18 ns
  From select 20 ns
- Typical power dissipation 170 mW

Connection Diagram

Dual-In-Line Package



TL/F/6547–1

Order Number DM54153J or DM74153N
See NS Package Number J16A or N16A

Function Table

Select Inputs		Data Inputs				Strobe	Output
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54153			DM74153			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	52	mA
			DM74		34	60	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

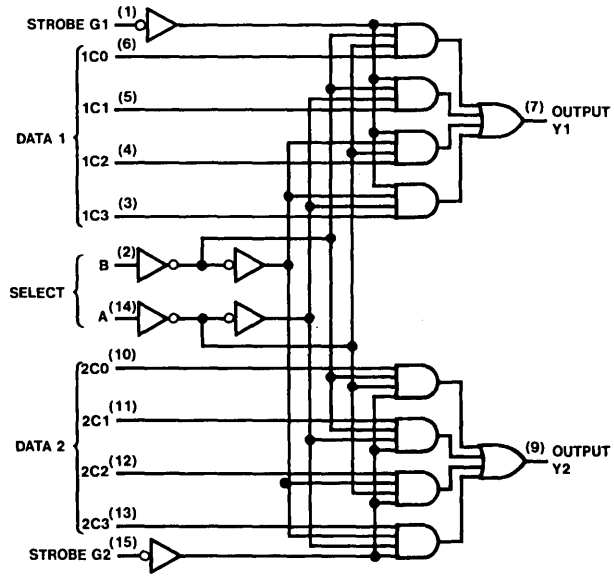
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 30 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		34	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		34	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		23	ns

Logic Diagram



TL/F/6547–2

National Semiconductor Corporation

DM54154/DM74154 4-Line to 16-Line Decoders/Demultiplexers

General Description

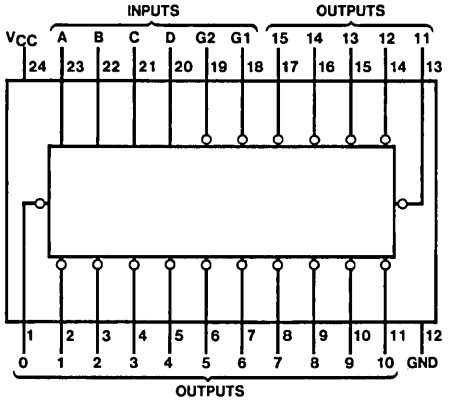
Each or these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay
  - 3 levels of logic 19 ns
  - Strobe 18 ns
- Typical power dissipation 170 mW

Connection Diagram

Dual-In-Line Package



TL/F/6548–1

Order Number DM54154J or DM74154N
See NS Package Number J24A or N24A

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54154			DM74154			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.25	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	49	mA
			DM74		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open and all inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

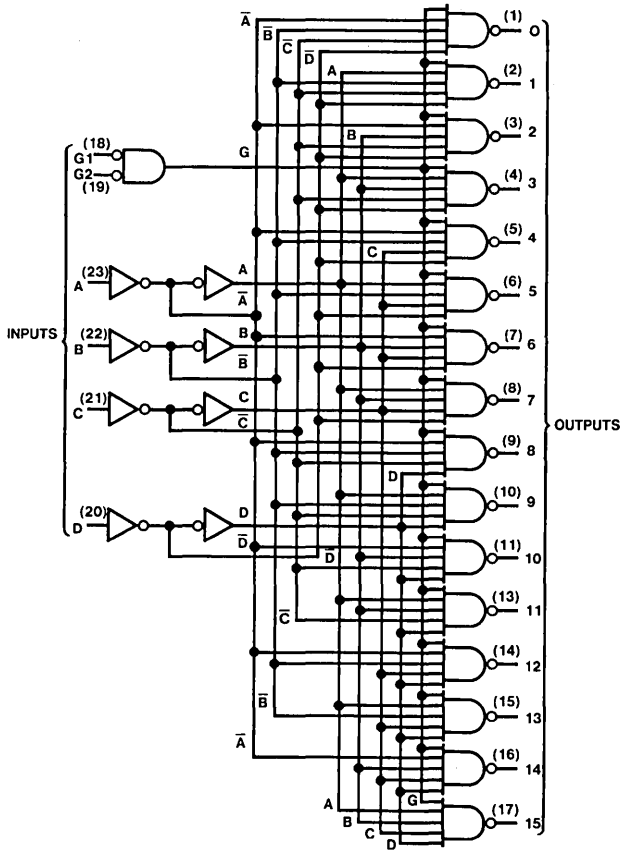
Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		36	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		27	ns

Function Table

Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Logic Diagram



TL/F/6548–2

National Semiconductor Corporation

DM54155/DM74155 Dual 2-Line to 4-Line Decoders/Demultiplexers

General Description

These TTL circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input C1 is inverted at its outputs and data applied at C2 is true through its outputs. The inverter following the C1 data input permits use as a 3-to-8-line decoder, or 1-to-8-line demultiplexer, without external gating.

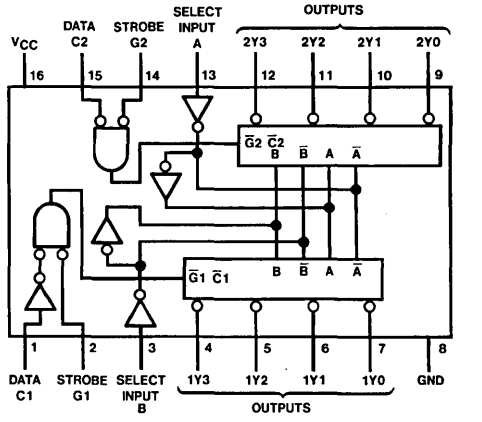
Input clamping diodes are provided on these circuits to minimize transmission-line effects and simplify system design.

Features

- Applications:
  Dual 2-to-4-line decoder
  Dual 1-to-4-line demultiplexer
  3-to-8-line decoder
  1-to-8-line demultiplexer
- Individual strobes simplify cascading for decoding or demultiplexing larger words
- Input clamping diodes simplify system design

Connection Diagram and Function Tables

Dual-In-Line Package



TL/F/6549–1

Order Number DM54155J or DM74155N
See NS Package Number J16A or N16A

2-Line-to-4-Line Decoder or 1-Line-to-4-Line Demultiplexer

Inputs				Outputs			
Select		Strobe	Data				
B	A	G1	C1	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

Inputs				Outputs			
Select		Strobe	Data				
B	A	G2	C2	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-Line-to-8-Line Decoder or 1-Line-to-8-Line Demultiplexer

Inputs				Outputs							
Select			Strobe Or Data	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs C1 and C2 connected together
‡G = inputs G1 and G2 connected together
H = high level, L = low level, X = don't care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54155			DM74155			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		25	35	mA
			DM74		25	40	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

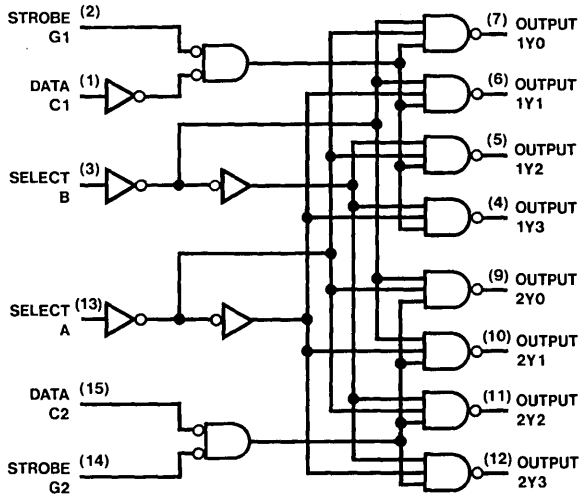
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs open, A, B, and C1 inputs at 4.5V, and C2, G1, and G2 inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	A, B, C2, G1 or G2 to Y		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A, B, C2, G1 or G2 to Y		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	A or B to Y		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A or B to Y		26	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	C1 to Y		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	C1 to Y		26	ns

Logic Diagram



TL/F/6549–2

National Semiconductor Corporation

DM54157/DM74157 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs.

Features

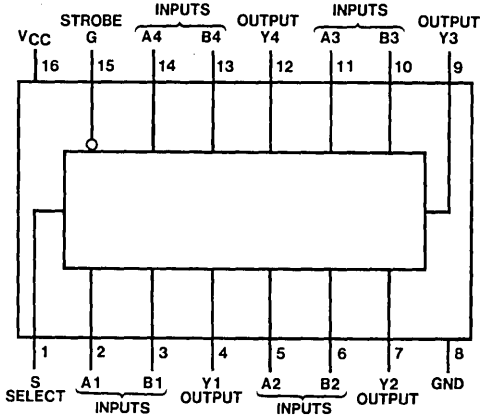
- Buffered inputs and outputs
- Typical propagation time 9 ns
- Typical power dissipation 150 mW

Applications

- Expand any data input point
- Multiplex dual data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Connection Diagram

Dual-In-Line Package



TL/F/6550–1

Order Number DM54157J or DM74157N
See NS Package Number J16A or N16A

Function Table

Inputs				Output Y
Strobe	Select	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54157			DM74157			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

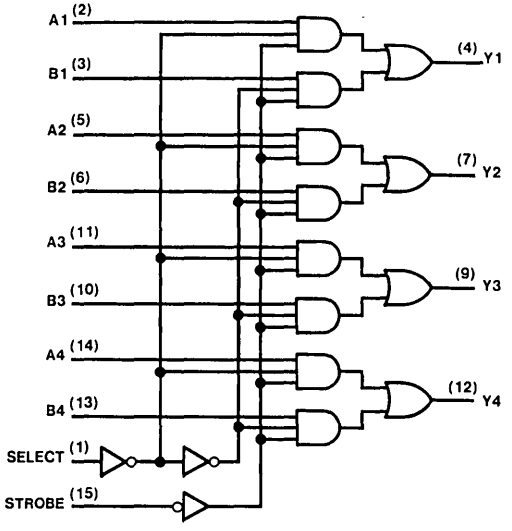
Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Seclect to Y		27	ns

Logic Diagram

157



TL/F/6550–2

National Semiconductor Corporation

DM54161A/DM74161A, DM54162A/DM74162A DM54163A/DM74163A Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The 162A is a decade counter and the 161A and 163A are 4-bit binary counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse, regardless of the levels of the enable input. Low-to-high transitions at the load input of the 161A through 163A are perfectly acceptable, regardless of the logic levels on the clock or enable inputs. The clear function for the 161A is asynchronous; and a low level at the clear input sets all four of the flip-flop outputs low, regardless of the levels of clock, load, or enable inputs. The clear function for the 162A and 163A is synchronous; and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily, as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to all low outputs. Low-to-high transitions at the clear input of the 162A and 163A are also permissible, regardless of the logic levels on the clock, enable, or load inputs.

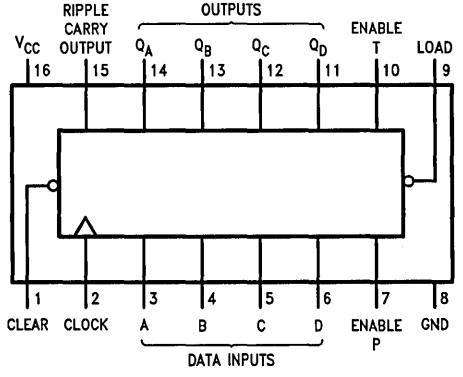
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs of the 161A through 163A may occur, regardless of the logic level on the clock.

Features

- Synchronously programmable
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs

Connection Diagram

Dual-In-Line Package



TL/F/6551–1

Order Number DM54161AJ, DM54162AJ or DM54163AJ, or DM74161AN, DM74162AN, or DM74163AN
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54161A thru 163A			DM74161A thru 163A			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 6)		0		25	0		25	MHz
t_W	Pulse Width (Note 6)	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 6)	Data	20			20			ns
		Enable P	34			34			
		Load	25			25			
		Clear (Note 5)	20			20			
t_H	Hold Time (Note 6)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Enable T			80	μA
			Clock			80	
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Enable T			−3.2	mA
			Clock			−3.2	
			Others			−1.6	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−20		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54		59	85	mA
			DM74		59	94	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)	DM54		63	91	mA
			DM74		63	101	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with the LOAD high, then again with the LOAD low, with all inputs high and all outputs open.

Note 4: I_{CCL} is measured with the CLOCK high, then again with the CLOCK input low, with all inputs low and all outputs open.

Note 5: Applies to '162A and '163A which have synchronous clear inputs.

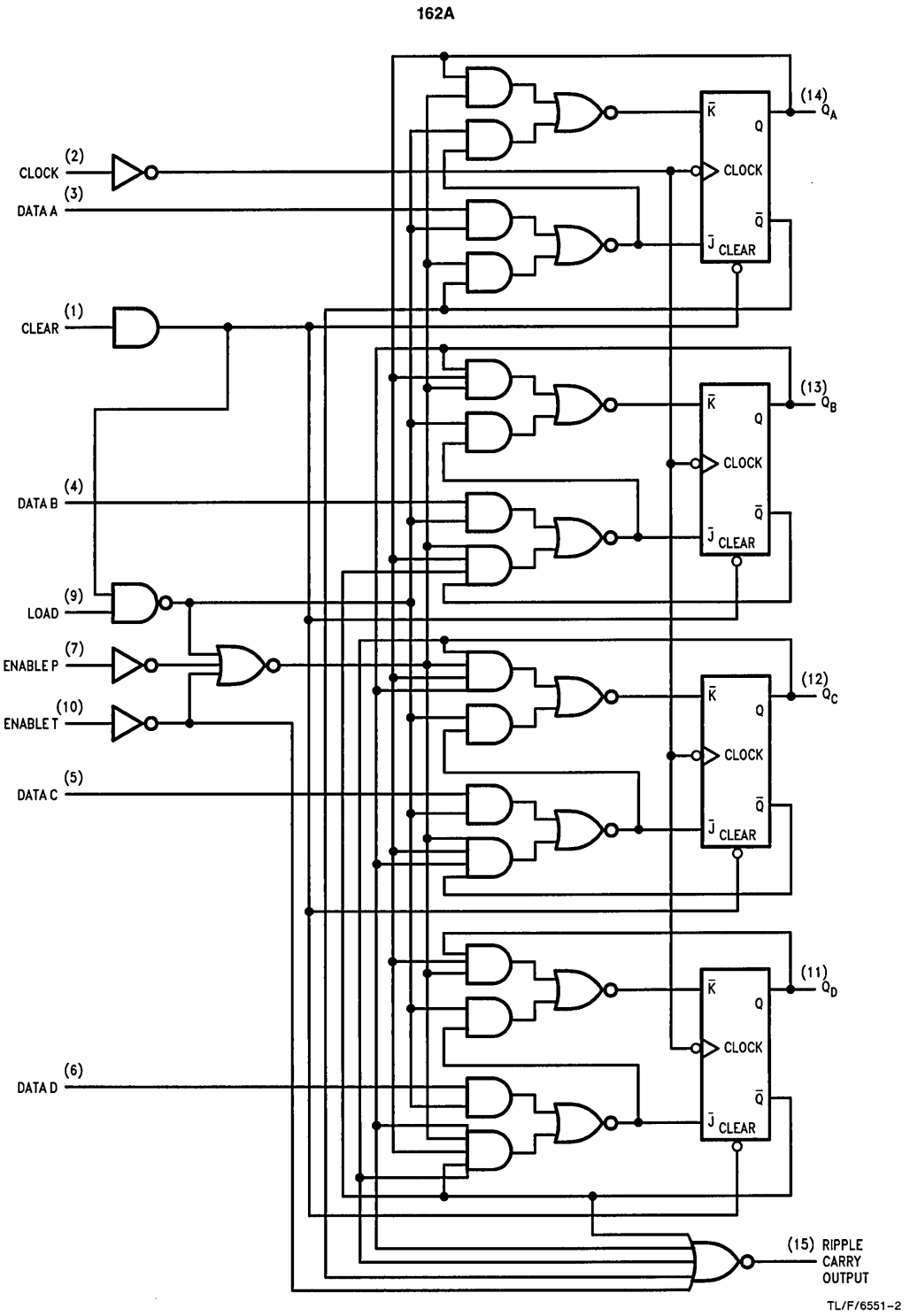
Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock (Load High) to Q		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock (Load High) to Q		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock (Load Low) to Q		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock (Load Low) to Q		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear (Note 7) to Q		36	ns

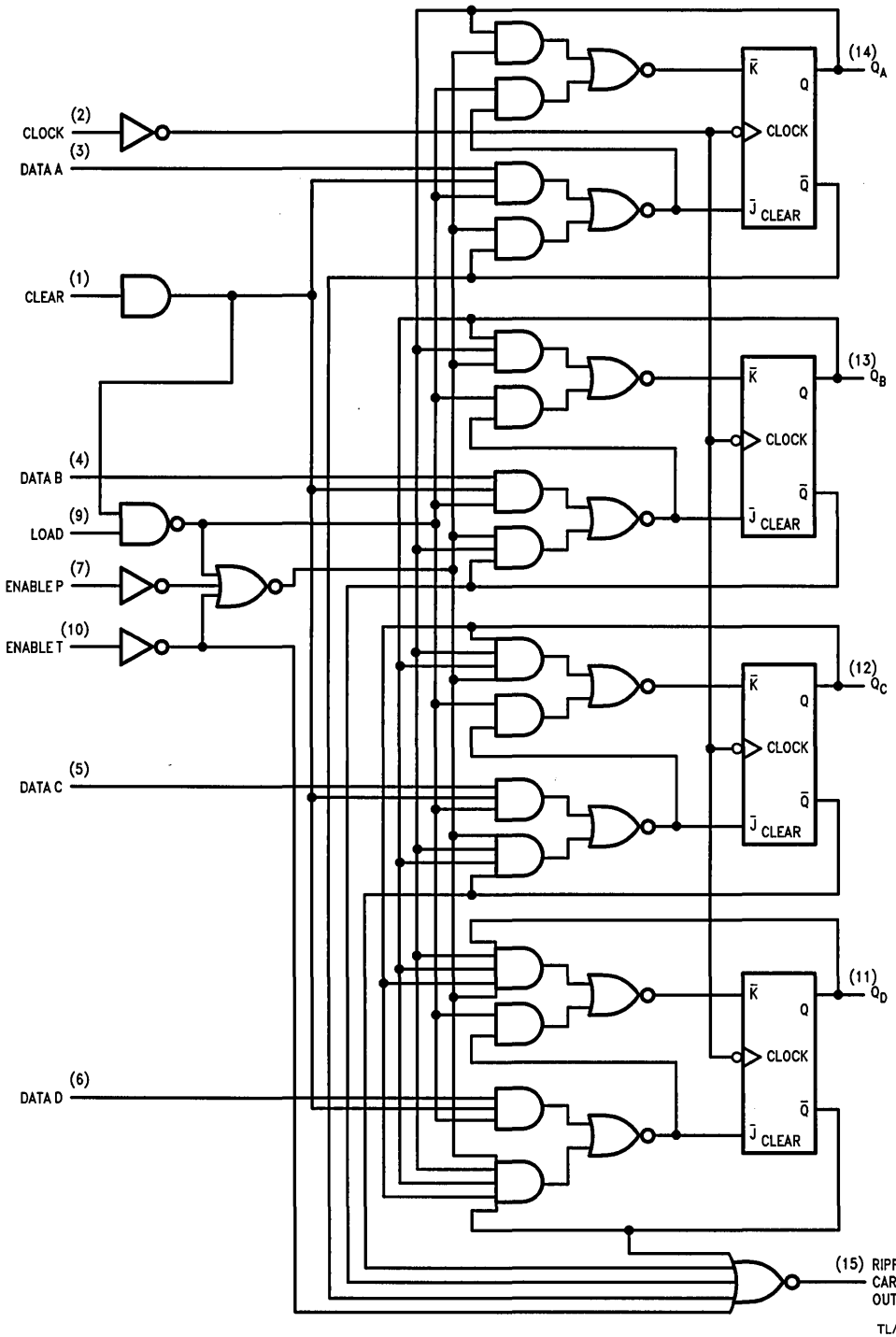
Note 7: Propagation delay for clearing is measured from the clear input for the 161A or from the clock input transition for the 162A and 163A.

Logic Diagrams



Logic Diagrams (Continued)

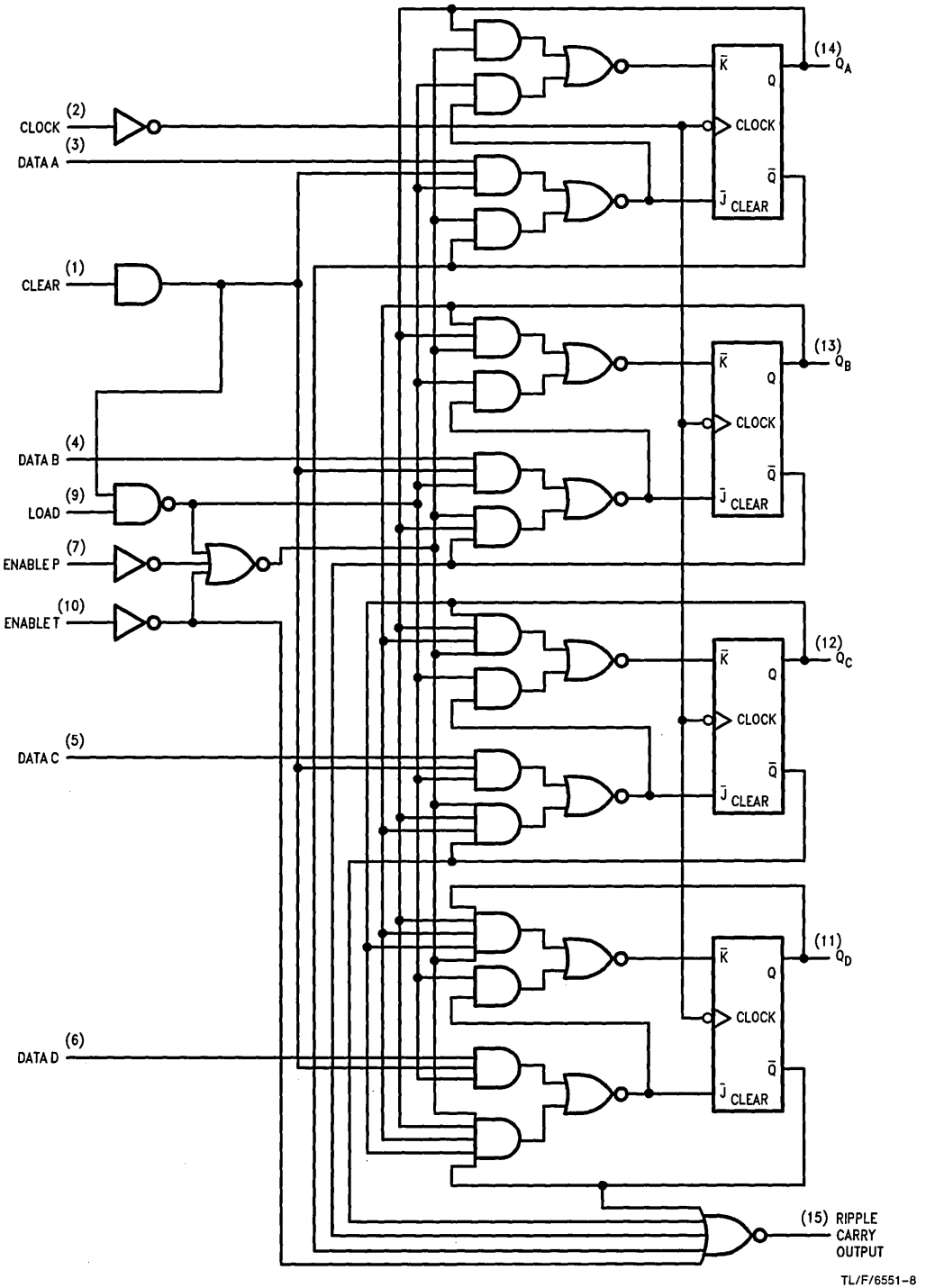
161A



TL/F/6551–3

Logic Diagrams (Continued)

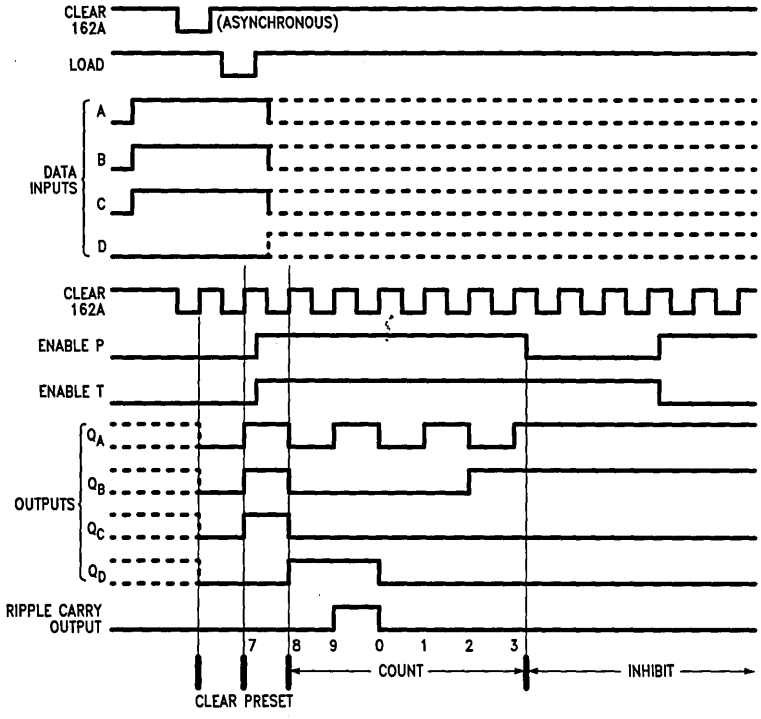
163A



TL/F/6551–8

Timing Diagrams

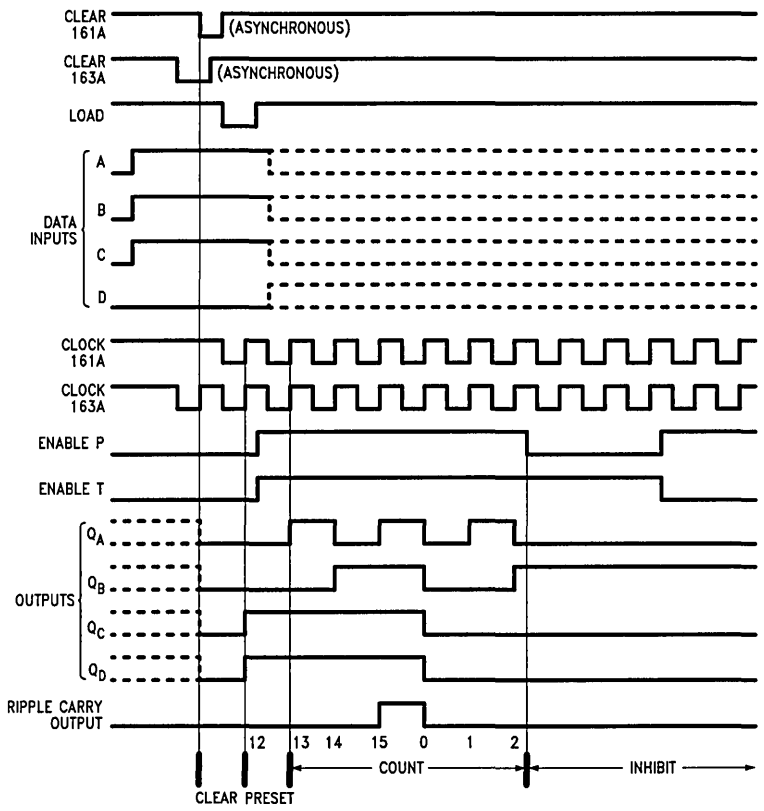
162A Synchronous Decade Counters
Typical Clear, Preset, Count and Inhibit Sequences



TL/F/6551–4

Timing Diagrams (Continued)

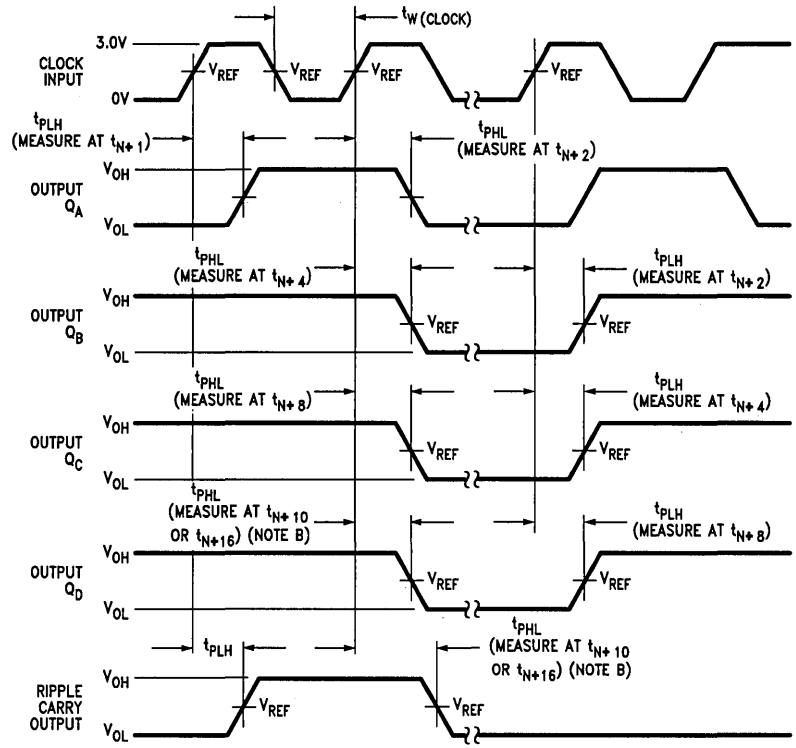
161A, 163A Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



TL/F/6551–5

Parameter Measurement Information

Switching Time Waveforms



TL/F/6551–6

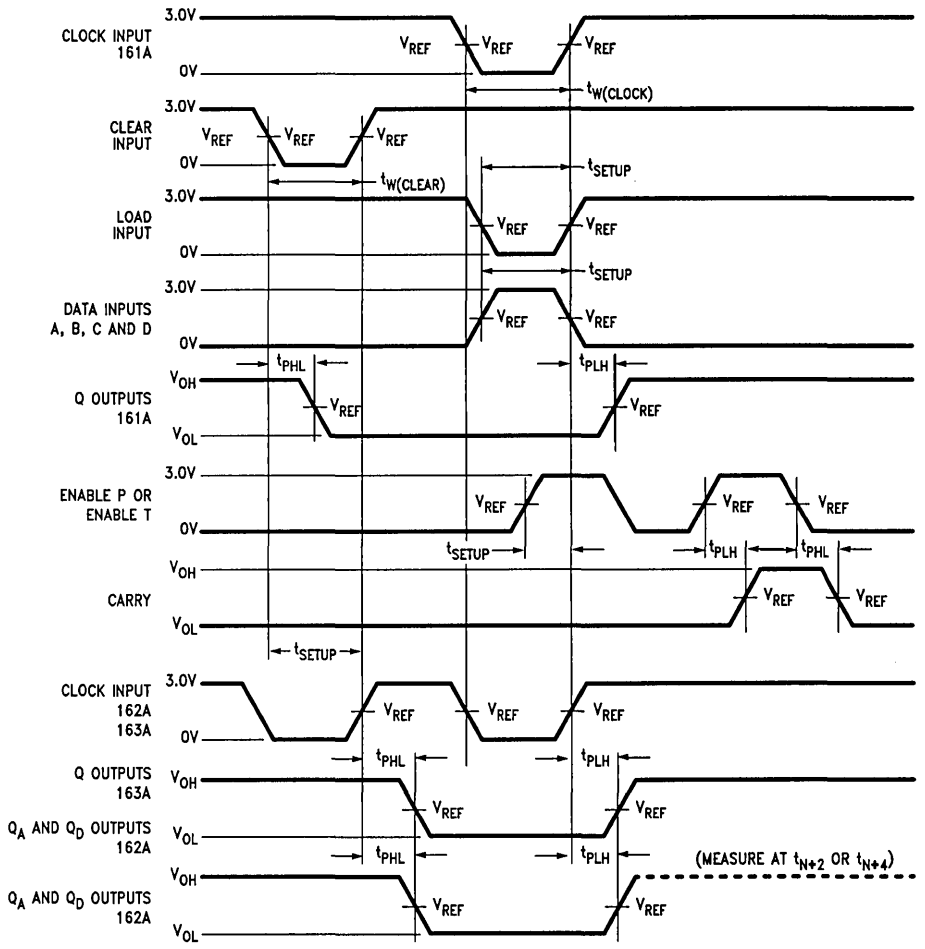
Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For 161A through 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+10} for 162A and at t_{n+16} for 161A, 163A where t_n is the bit time when all outputs are low.

Note C: For 161A through 163A, $V_{REF} = 1.5V$.

Parameter Measurement Information (Continued)

Switching Time Waveforms



TL/F/6551–7

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$. For 161A through 163A, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Enable P and enable T setup times are measured at t_{n+0}.

Note C: For 161A through 163A, $V_{REF} = 1.5V$.

National Semiconductor Corporation

DM54164/DM74164 8-Bit Serial In/Parallel Out Shift Registers

General Description

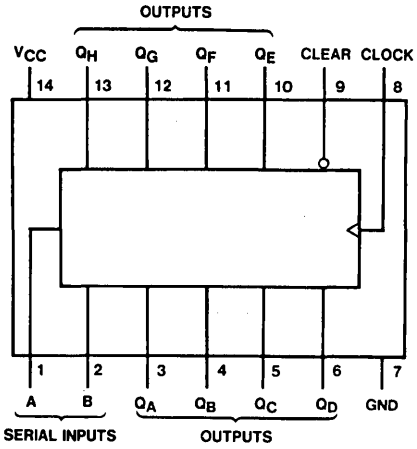
These 8-bit shift registers feature gated serial inputs and an asynchronous clear. A low logic level at either serial input inhibits entry of the new data, and resets the first flip-flop to the low level at the next clock pulse, thus providing complete control over incoming data. A high logic level on either input enables the other input, which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Clocking occurs on the low-to-high level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

Features

- Gated (enable/disable) serial inputs
- Fully buffered clock and serial inputs
- Asynchronous clear
- Typical clock frequency 36 MHz
- Typical power dissipation 185 mW

Connection Diagram

Dual-In-Line Package



TL/F/6552–1

Order Number DM54164J or DM74164N
See NS Package Number J14A or N14A

Function Table

Inputs				Outputs			
Clear	Clock	A	B	Q_A	Q_B	...	Q_H
L	X	X	X	L	L	...	L
H	L	X	X	Q_{A0}	Q_{B0}	...	Q_{H0}
H	↑	H	H	H	Q_{An}	...	Q_{Gn}
H	↑	L	X	L	Q_{An}	...	Q_{Gn}
H	↑	X	L	L	Q_{An}	...	Q_{Gn}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low to high level

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G before the most recent ↑ transition of the clock; indicates a one-bit shift.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54164			DM74164			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				8			8	mA
f_{CLK}	Clock Frequency (Note 4)		0	36	25	0	36	25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		15			15			ns
t_H	Data Hold Time (Note 4)		5			5			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.2		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−10		−27.5	mA
			DM74	−9		−27.5	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			37	54	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

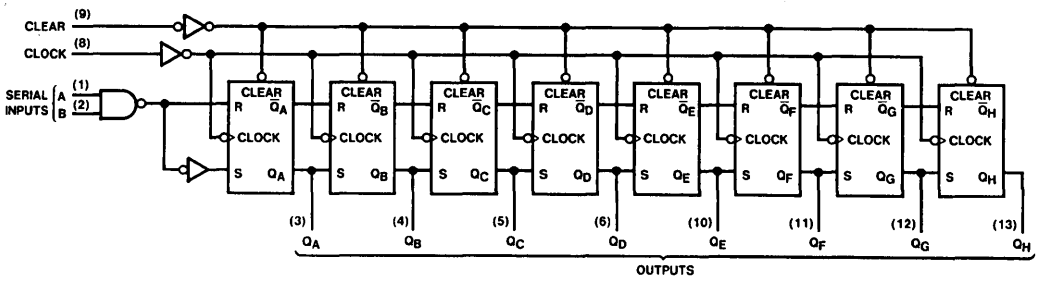
Note 3: I_{CC} is measured with all outputs open, SERIAL inputs grounded, the CLOCK input at 2.4V, and a momentary ground, then 4.5V, applied to the CLEAR input.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

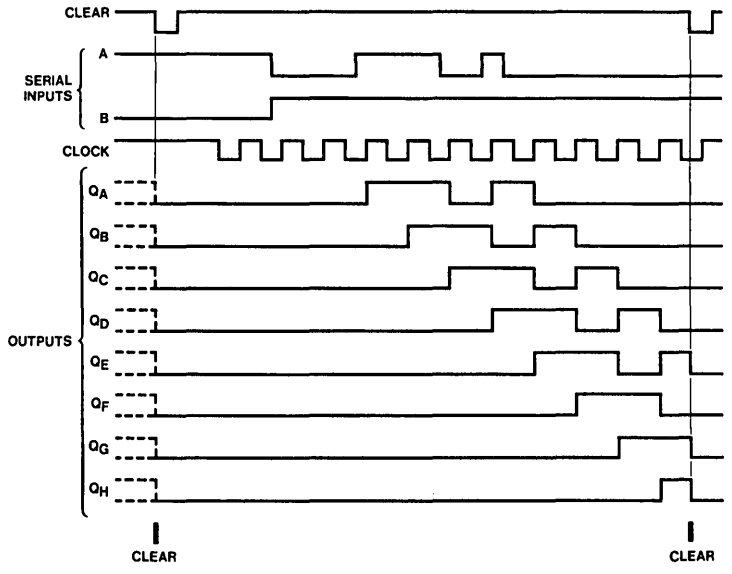
Symbol	Parameter	From (Input) To (Output)	R_L = 800Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		25				MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output	8	27	10	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output	10	32	10	37	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		36		42	ns

Logic Diagram



TL/F/6552–2

Timing Diagram



TL/F/6552–3

National Semiconductor Corporation

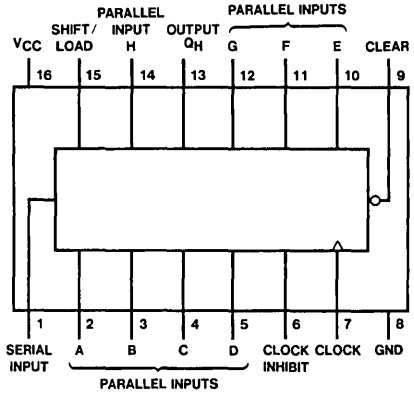
DM54166/DM74166 8-Bit Parallel In/Serial Out Shift Registers

General Description

These parallel-in or serial-in, serial-out shift registers feature gated clock inputs and an overriding clear input. All inputs are buffered to lower the drive requirements to one normalized load, and input clamping diodes minimize switching transients to simplify system design. The load mode is established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free-running, and the register can be stopped on command with the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock, and sets all flip-flops to zero.

Connection Diagram

Dual-In-Line Package



TL/F/6554–1

Order Number DM54166J or DM74166N
See NS Package Number J16A or N16A

Function Table

Inputs						Internal Outputs		Output
Clear	Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from Low to High Level

a . . . h = The level of stead-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, Q_H, respectively, before the indicated steady-state input conditions were established

Q_{An}, Q_{Gn} = The level of Q_A, Q_G, respectively, before the most recent ↑ transition of the clock

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54166			DM74166			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock	24			24			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 4)	Mode	30			30			ns
		Data	20			20			
t_H	Data Hold Time (Note 4)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		72	104	mA
			DM74		72	116	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

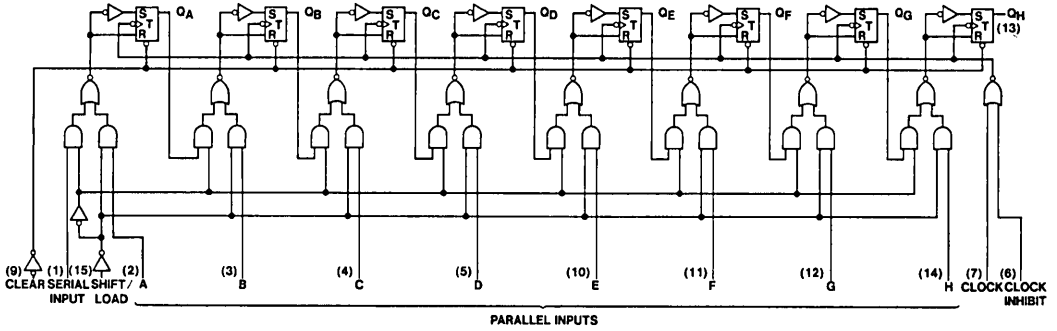
Note 3: With all outputs open, 4.5V applied to the SERIAL input, all other inputs except CLOCK grounded, I_{CC} is measured after a momentary ground, then 4.5V, is applied to the CLOCK.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output	8	26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output	8	30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		35	ns

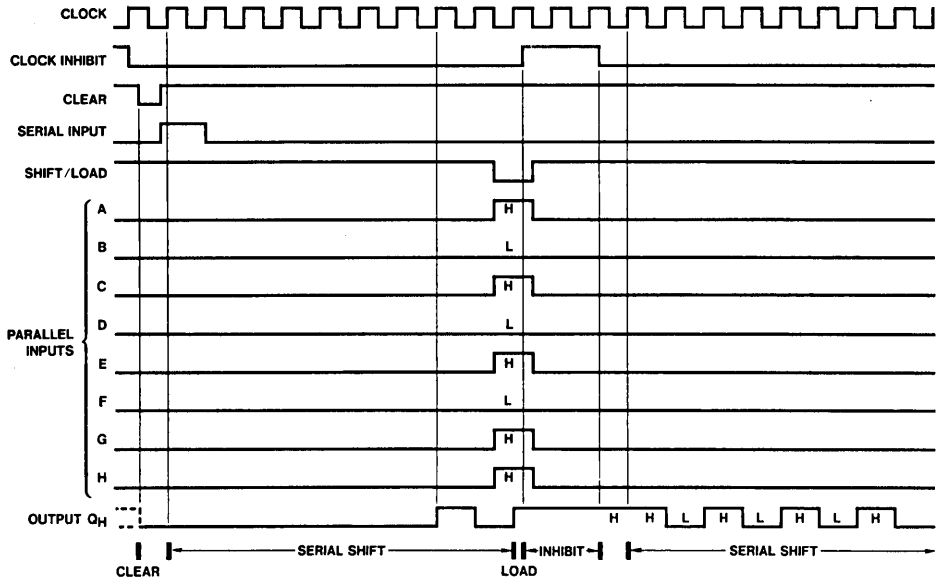
Logic Diagram



TL/F/6554–2

Timing Diagram

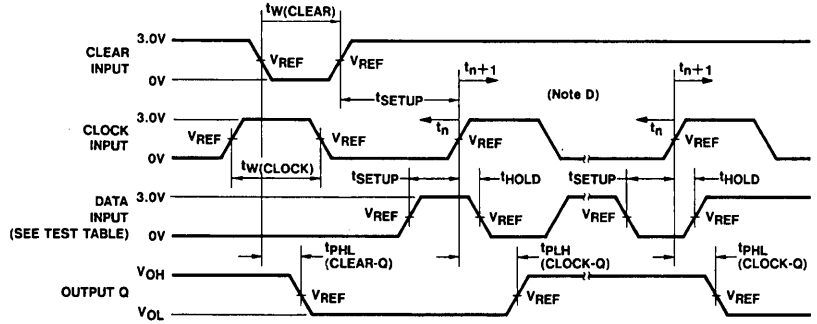
Typical Clear, Shift, Load, Inhibit, and Shift Sequences



TL/F/6554–3

Parameter Measurement Information

Voltage Waveforms



TL/F/6554–4

Test Table for Synchronous Inputs

Data Input For Test	Shift/Load	Output Tested (See Note C)
H	0V	Q_H at $T_N + 1$
Serial Input	4.5V	Q_H at $T_N + 8$

Note A: The clock pulse has the following characteristics:
$t_{W(clock)} \geq 20$ ns and PRR = 1 MHz.
The clear pulse has the following characteristics:
$t_{W(clear)} \geq 20$ ns and $t_{HOLD} = 0$ ns.
When testing f_{MAX}, vary the clock PRR.

Note B: A clear pulse is applied prior to each test.

Note C: Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}.
Proper shifting of data is verified at t_{n+8} with a functional test.

Note D: t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+8} = bit time after eight clocking transitions.

Note E: V_{REF} = 1.5V for 166.

National Semiconductor Corporation

DM54173/DM74173 TRI-STATE® Quad D Registers

General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

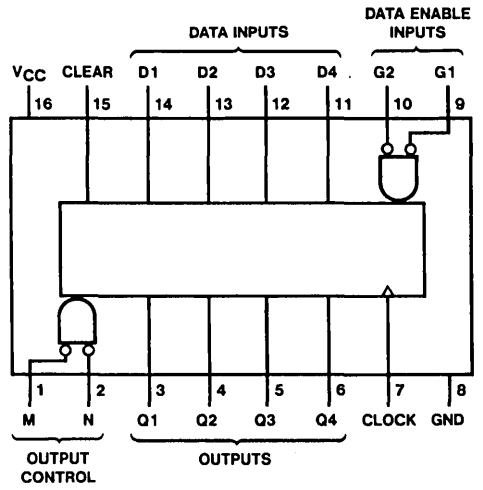
To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock elminates restrictions for operating in one of two modes:
  - Parallel load
  - Do nothing (hold)
- For application as bus buffer registers
- Typical propagation delay 18 ns
- Typical frequency 30 MHz
- Typical power dissipation 250 mW

Connection Diagram

Dual-In-Line Package



TL/F/6556–1

Order Number DM54173J or DM74173N
See NS Package Number J16A or N16A

Function Table

Inputs					Output Q
Clear	Clock	Data Enable G1	Data Enable G2	Data D	
H	X	X	X	X	L
L	L	X	X	X	Q_0
L	↑	H	X	X	Q_0
L	↑	X	H	X	Q_0
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)

L = low level (steady state)

↑ = low-to-high level transition

X = don't care (any input including transitions)

Q_0 = the level of Q before the indicated steady state input conditions were established

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54173			DM74173			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 4)	Enable	17			17			ns
		Data	10			10			
t_H	Hold Time (Note 4)	Enable	2			2			ns
		Data	10			10			
t_{REL}	Clear Release Time (Note 4)		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−30		−70	mA
			DM74	−30		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	72	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

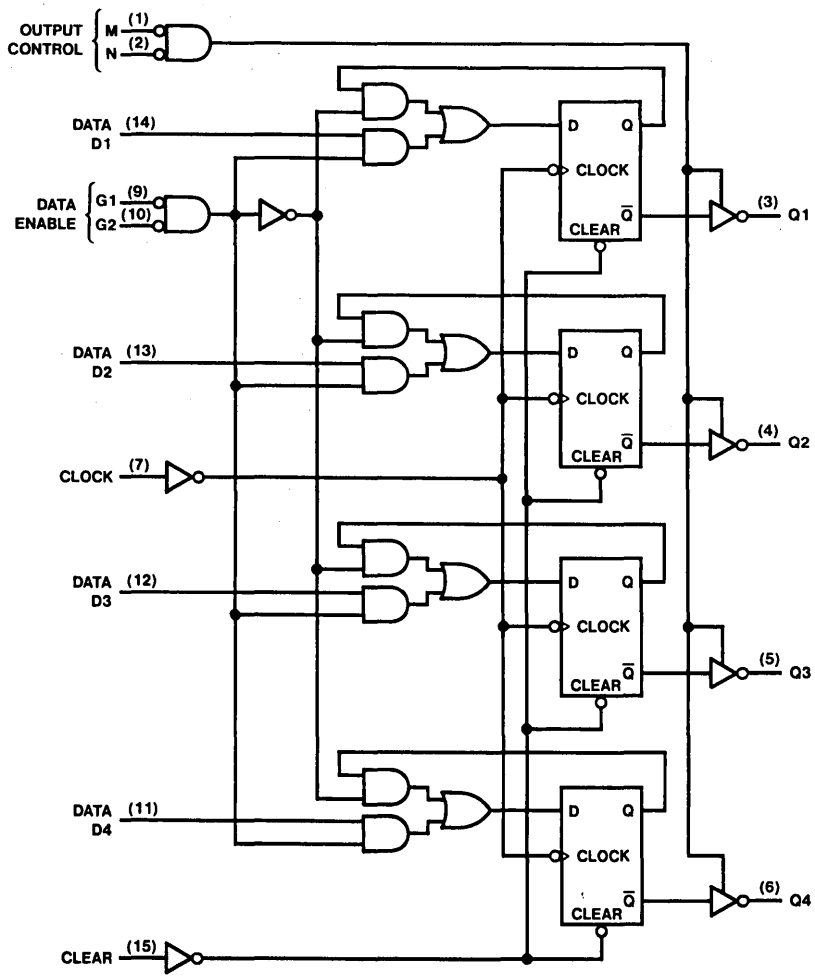
Note 3: I_{CC} is measured with all outputs open, CLEAR grounded after a momentary connection to 4.5V: N, G1, G2 and all DATA inputs grounded: and the CLOCK input and M input at 4.5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω				Units
			C_L = 5 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency				25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output				25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output				28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output				27	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Q			7	30	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Q			7	30	ns
t_{PHZ}	Output Disable Time from High Level Output	Output Control to Q	3	14			ns
t_{PLZ}	Output Disable Time from Low Level Output	Output Control to Q	3	20			ns

Logic Diagram



TL/F/6556–2

National Semiconductor Corporation

DM54174/DM74174, DM54175/DM74175 Hex/Quad D Flip-Flops with Clear

General Description

These positive-edge triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the quad (175) version features complementary outputs from each flip-flop.

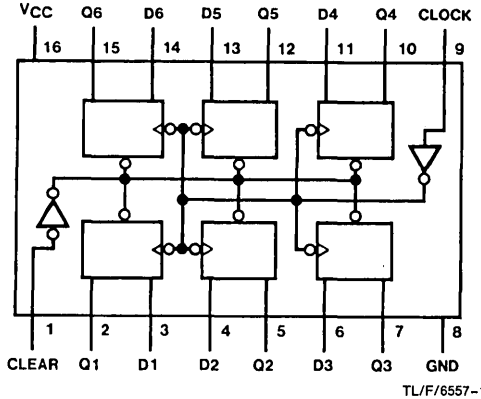
Information at the D inputs meeting the setup and hold time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

Features

- 174 contains six flip-flops with single-rail outputs
- 175 contains four flip-flops with double-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop
- Applications include:
  - Buffer/storage registers
  - Shift registers
  - Pattern generators
- Typical clock frequency 40 MHz
- Typical power dissipation per flip-flop 38 mW

Connection Diagrams

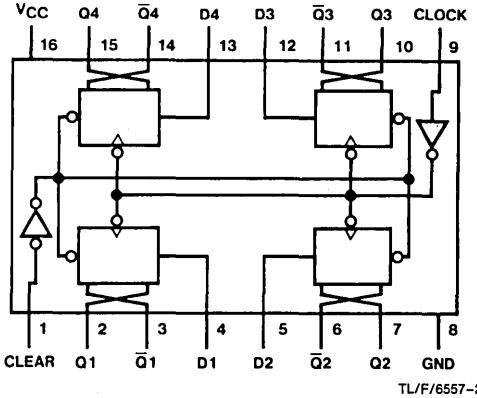
Dual-In-Line Package



TL/F/6557-1

Order Number DM54174J or DM74174N
See NS Package Number J16A or N16A

Dual-In-Line Package



TL/F/6557-2

Order Number DM54175J or DM74175N
See NS Package Number J16A or N16A

Function Table (Each Flip-Flop)

Inputs			Outputs	
Clear	**Clock**	**D**	**Q**	**$\overline{Q}$†**
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

H = High Level (steady state)
L = Low Level (steady state)
X = Don't Care
↑ = Transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established.
† = 175 only

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54174			DM74174			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		30	0		30	MHz
t_W	Pulse Width (Note 4)	Clock Low	25			25			ns
		Clock High	10			10			
		Clear	20			20			
t_{SU}	Data Setup Time (Note 4)		20			20			ns
t_H	Data Hold Time (Note 4)		0			0			ns
t_{REL}	Clear Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'174 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			45	65	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open and all DATA and CLEAR inputs at 4.5V, I_{CC} is measured after a momentary ground, then 4.5V applied to the CLOCK input.

Note 4: T_A = 25°C and V_{CC} = 5V.

'174 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		40	ns

Recommended Operating Conditions

Symbol	Parameter		DM54175			DM74175			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 1)		0		30	0		30	MHz
t_W	Pulse Width (Note 1)	Clock Low	25			25			ns
		Clock High	10			10			
		Clear	20			20			
t_{SU}	Data Setup Time (Note 1)		20			20			ns
t_H	Data Hold Time (Note 1)		0			0			ns
t_{REL}	Clear Release Time (Note 1)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

'175 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	45	mA

'175 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q or $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q or $\overline{Q}$		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to Any $\overline{Q}$		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Any Q		40	ns

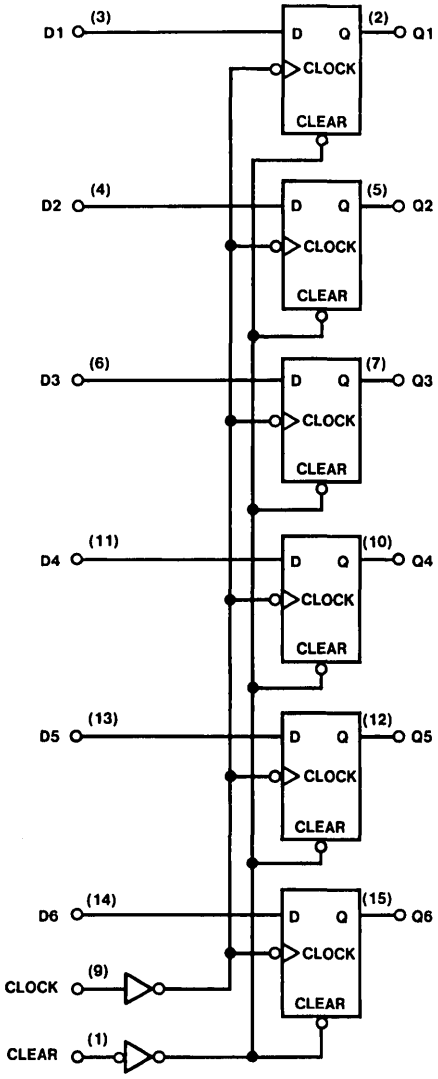
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open and 4.5V applied to all DATA and CLEAR inputs, I_{CC} is measured after a momentary ground then 4.5V applied to the CLOCK.

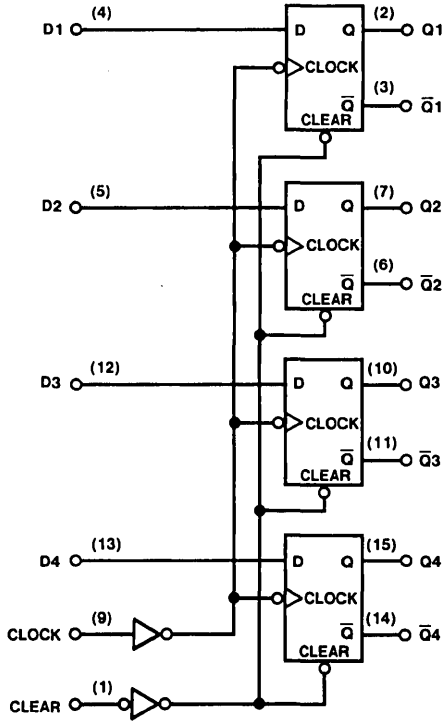
Logic Diagrams

174



TL/F/6557–3

175



TL/F/6557–4

National Semiconductor Corporation

PRELIMINARY

DM54180/DM74180 9-Bit Parity Generators/Checkers

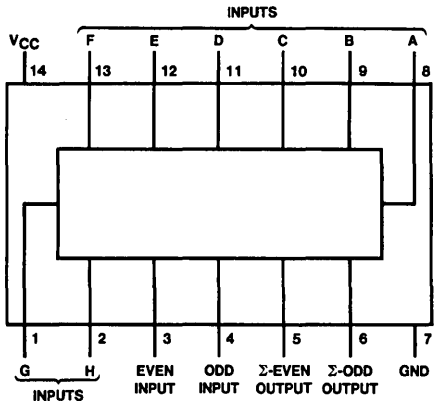
General Description

These universal 9-bit (8 data bits plus 1 parity bit) parity generators/checkers feature odd/even outputs and control inputs to facilitate operation in either odd or even parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd input can be utilized as the parity or 9th-bit input. The word-length capability is easily expanded by cascading.

Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs at a low logic level. A fan-out to 20 normalized loads is provided at a high logic level to facilitate the connection of unused inputs to used inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6559–1

Order Number DM54180J or DM74180N
See NS Package Number J14A or N14A

Function Table

Inputs			Outputs	
Σ of H's at A thru H	Even	Odd	Σ Even	Σ Odd
Even	H	L	H	L
Odd	H	L	L	H
Even	L	H	L	H
Odd	L	H	H	L
X	H	H	L	L
X	L	L	H	H

H = High Level, L = Low Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54180			DM74180			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Odd or Even			80	μA
			Data			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Odd or Even			−3.2	mA
			Data			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		34	49	mA
			DM74		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

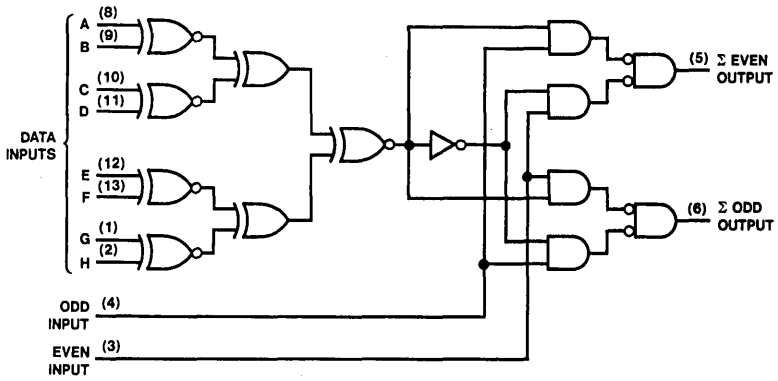
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with EVEN and ODD inputs at 4.5V, all other inputs and outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Even	C_L = 15 pF, R_L = 400Ω, Odd Input Low		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Even			68	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Odd			48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Odd			38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Even	C_L = 15 pF, R_L = 400Ω, Odd Input High		48	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Even			38	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Σ Odd			60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Σ Odd			68	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Even or Odd to Σ Even or Σ Odd	C_L = 15 pF, R_L = 400Ω		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Even or Odd to Σ Even or Σ Odd			10	ns

Logic Diagram



TL/F/6559–2

National Semiconductor Corporation

DM54181/DM74181 Arithmetic Logic Unit/Function Generators

General Description

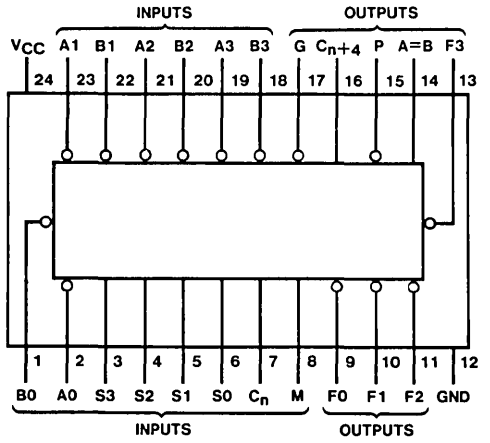
These arithmetic logic units (ALU)/function generators perform 16 binary arithmetic operations on two 4-bit words, as shown in Tables I and II. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (P and G) for the four bits in the package. When used in conjunction with the DM54S182/DM74S182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. The typical addition times shown below illustrate how little time is required for addition of longer words, when full carry look-ahead is employed. The method of cascading 182 circuits with these ALU's to provide multi-level full carry look-ahead is illustrated under typical applications data for the DM54S182/DM74S182. (Continued)

Features

- Arithmetic operating modes:
  - Addition
  - Subtraction
  - Shift operand A one position
  - Magnitude comparison
  - Plus twelve other arithmetic operations
- Logic function modes:
  - EXCLUSIVE-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus ten other logic operations
- Full look-ahead for high-speed operations on long words

Connection Diagram

Dual-In-Line Package



TL/F/6560–1

Order Number DM54181J or DM74181N
See NS Package Number J24A or N24A

Pin Designations

Designation	Pin Nos.	Function
A3, A2, A1, A0	19, 21, 23, 2	Word A Inputs
B3, B2, B1, B0	18, 20, 22, 1	Word B Inputs
S3, S2, S1, S0	3, 4, 5, 6	Function-Select Inputs
C_n	7	Inv. Carry Input
M	8	Mode Control Input
F3, F2, F1, F0	13, 11, 10, 9	Function Outputs
A = B	14	Comparator Output
P	15	Carry Propagate Output
C_n+4	16	Inv. Carry Output
G	17	Carry Generate Output
V_{CC}	24	Supply Voltage
GND	12	Ground

Number of Bits	Typical Addition Times	Package Count		Carry Method Between ALU's
		Arithmetic/ Logic Units	Look Ahead Carry Generators	
1 to 4	20 ns	1	0	None
5 to 8	30 ns	2	0	Ripple
9 to 16	30 ns	3 or 4	1	Full Look-Ahead
17 to 64	50 ns	5 to 16	2 to 5	Full Look-Ahead

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage (A = B Output)	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54181			DM74181			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage (A = B Output)			5.5			5.5	V
I_{OH}	High Level Output Current (All Except A = B)			−800			−800	μA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current (A = B Output)	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OH}	High Level Output Voltage (All Except A = B)	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Mode			40	μA
			A or B			120	
			S			160	
			Carry			200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	Mode			−1.6	mA
			A or B			−4.8	
			S			−6.4	
			Carry			−8	
I_{OS}	Short Circuit Output Current (All Except A = B)	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM54		88	127	mA
			DM74		88	140	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)	DM54		92	135	mA
			DM74		92	150	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with S0 through S3, M, and A inputs at 4.5V, all other inputs grounded and all outputs open.

Note 4: I_{CCL} is measured with S0 through S3 and M inputs at 4.5V, all other inputs grounded and all outputs open.

Switching Characteristics V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input)	To (Output)	Conditions	DM54/74 181 R_L = 400Ω, C_L = 15 pF		Units
					Min	Max	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	C_n+4			18	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					19	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_n+4	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)		30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					33	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	C_n+4	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					33	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	C_n	Any F	M = 0V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					18	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					19	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	G	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		20	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)		19	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	P	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		25	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					25	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0V, S0 = S3 = 4.5V S1 = S2 = 0V ($\overline{SUM}$ mode)		30	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		24	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					24	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	A_i or B_i	F_i	M = 4.5V (logic mode)		28	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					30	
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Any A or B	A = B	M = 0V, S0 = S3 = 0V S1 = S2 = 4.5V ($\overline{DIFF}$ mode)		40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output					40	

General Description (Continued)

If high speed is not important, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

These circuits will accommodate active-high or active-low data, if the pin designations are interpreted as shown below.

Subtraction is accomplished by 1's complement addition, where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1, which requires an end-around or forced carry to provide A—B.

The 181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1, S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

ALU SIGNAL DESIGNATIONS

The DM54181/DM74181 can be used with the signal designations of either *Figure 1* or *Figure 2*.

The logic functions and arithmetic operations obtained with signal designations as in *Figure 1* are given in Table I; those obtained with the signal designations of *Figure 2* are given in Table II.

Pin Number	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-High Data (Table I)	A0	B0	A1	B1	A2	B2	A3	B3	F0	F1	F2	F3	$\overline{C}_n$	$\overline{C}_n+4$	X	Y
Active-Low Data (Table II)	$\overline{A}0$	$\overline{B}0$	$\overline{A}1$	$\overline{B}1$	$\overline{A}2$	$\overline{B}2$	$\overline{A}3$	$\overline{B}3$	$\overline{F}0$	$\overline{F}1$	$\overline{F}2$	$\overline{F}3$	C_n	C_n+4	$\overline{P}$	$\overline{G}$

Input C_n	Output C_n+4	Active-High Data (Figure 1)	Active-Low Data (Figure 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

General Description (Continued)

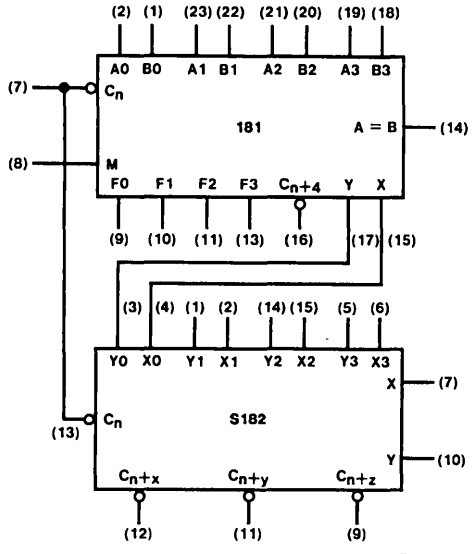


FIGURE 1

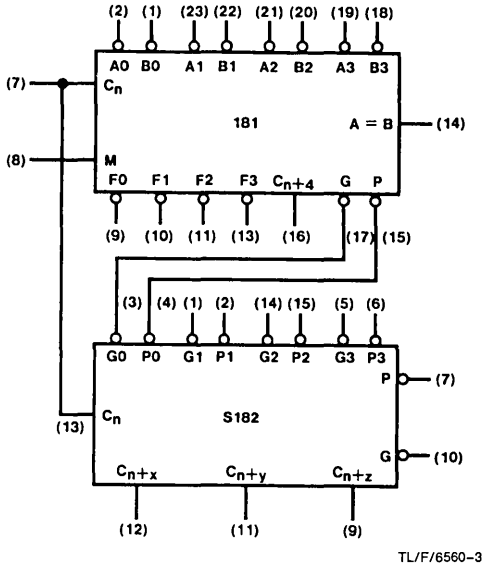


FIGURE 2

TABLE I

Selection				Active High Data		
				M = H	M = L; Arithmetic Operations	
				Logic		
S3	S2	S1	S0	Functions	C_n = H (no carry)	C_n = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A Plus 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) Plus 1
L	L	H	L	$F = \overline{A}B$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
L	L	H	H	F = 0	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	$F = \overline{AB}$	F = A Plus A$\overline{B}$	F = A Plus A$\overline{B}$ Plus 1
L	H	L	H	$F = \overline{B}$	F = (A + B) Plus A$\overline{B}$	F = (A + B) Plus A$\overline{B}$ Plus 1
L	H	H	L	F = A ⊕ B	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A$\overline{B}$	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A Plus AB	F = A Plus AB Plus 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) Plus AB	F = (A + $\overline{B}$) Plus AB Plus 1
H	L	H	H	F = AB	F = AB Minus 1	F = AB
H	H	L	L	F = 1	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A + $\overline{B}$	F = (A + B) Plus A	F = (A + B) Plus A Plus 1
H	H	H	L	F = A + B	F = (A + $\overline{B}$) Plus A	F = (A + $\overline{B}$) Plus A Plus 1
H	H	H	H	F = A	F = A Minus 1	F = A

*Each bit is shifted to the next more significant position.

4

General Description (Continued)

TABLE II

Selection				Active Low Data		
				M = H Logic Functions	M = L; Arithmetic Operations	
S3	S2	S1	S0		C_n = L (no carry)	C_n = H (with carry)
L	L	L	L	F = $\overline{A}$	F = A Minus 1	F = A
L	L	L	H	F = $\overline{AB}$	F = AB Minus 1	F = AB
L	L	H	L	F = $\overline{A}$ + B	F = A$\overline{B}$ Minus 1	F = A$\overline{B}$
L	L	H	H	F = 1	F = Minus 1 (2's Compl)	F = Zero
L	H	L	L	F = $\overline{A + B}$	F = A Plus (A + $\overline{B}$)	F = A Plus (A + $\overline{B}$) Plus 1
L	H	L	H	F = $\overline{B}$	F = AB Plus (A + B)	F = AB Plus (A + $\overline{B}$) Plus 1
L	H	H	L	F = $\overline{A \oplus B}$	F = A Minus B Minus 1	F = A Minus B
L	H	H	H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) Plus 1
H	L	L	L	F = $\overline{A}$B	F = A Plus (A + B)	F = A Plus (A + B) Plus 1
H	L	L	H	F = A $\oplus$ B	F = A Plus B	F = A Plus B Plus 1
H	L	H	L	F = B	F = A$\overline{B}$ Plus (A + B)	F = A$\overline{B}$ Plus (A + B) Plus 1
H	L	H	H	F = A + B	F = A + B	F = (A + B) Plus 1
H	H	L	L	F = 0	F = A Plus A*	F = A Plus A Plus 1
H	H	L	H	F = A$\overline{B}$	F = AB Plus A	F = AB Plus A Plus 1
H	H	H	L	F = AB	F = A$\overline{B}$ Plus A	F = A$\overline{B}$ Plus A Plus 1
H	H	H	H	F = A	F = A	F = A Plus 1

*Each bit is shifted to the next more significant position.

Parameter Measurement Information

Logic Mode Test Table
Function Inputs: S1 = S2 = M = 4.5V, S0 = S3 = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	F_i	Out-of-Phase

$\overline{SUM}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} / t_{PHL}	A_i	B_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	Remaining A and B	C_n	F_i	In-Phase
t_{PLH} / t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} / t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	In-Phase

Parameter Measurement Information (Continued)

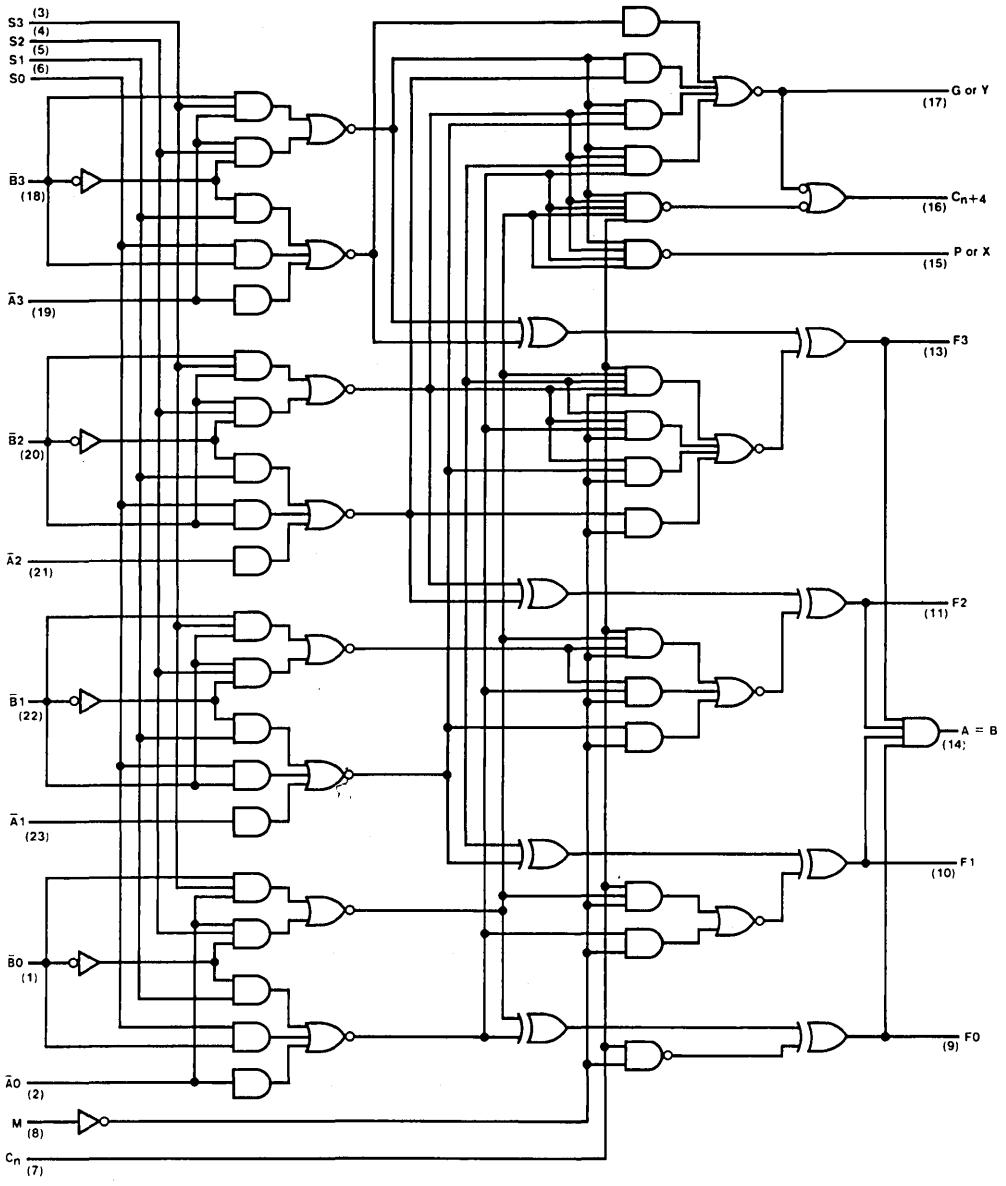
$\overline{\text{SUM}}$ Mode Test Table
Function Inputs: S0 = S3 = 4.5V, S1 = S2 = M = 0V (Continued)

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	G	In-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A	All B	Any F or C_n+4	In-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	Remaining B	Remaining A, C_n	C_n+4	Out-of-Phase

$\overline{\text{DIFF}}$ Mode Test Table
Function Inputs: S1 = S2 = 4.5V, S0 = S3 = M = 0V

Parameter	Input Under Test	Other Input Same Bit		Other Data Inputs		Output Under Test	Output Waveform
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND		
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	F_i	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	F_i	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	None	Remaining A and B, C_n	P	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	None	Remaining A and B, C_n	P	Out-of-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A and B, C_n	G	In-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A and B, C_n	G	Out-of-Phase
t_{PLH} t_{PHL}	A_i	None	B_i	Remaining A	Remaining B, C_n	A = B	In-Phase
t_{PLH} t_{PHL}	B_i	A_i	None	Remaining A	Remaining B, C_n	A = B	Out-of-Phase
t_{PLH} t_{PHL}	C_n	None	None	All A and B	None	C_n+4 or any F	In-Phase
t_{PLH} t_{PHL}	A_i	B_i	None	None	Remaining A, B, C_n	C_n+4	Out-of-Phase
t_{PLH} t_{PHL}	B_i	None	A_i	None	Remaining A, B, C_n	C_n+4	In-Phase

Logic Diagram



TL/F/6560–4

V_{CC} = PIN 24
GND = PIN 12

National Semiconductor Corporation

DM54184/DM74184, DM54185A/DM74185A BCD-to-Binary and Binary-to-BCD Converters

General Description

These monolithic converters are derived from the 256-bit read only memories, DM5488, and DM7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1, as shown in the function tables. These converters demonstrate the versatility of a read only memory in that an unlimited number of reference tables or conversion tables may be built into a system. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

An overriding enable input is provided on each converter which when taken high inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the 185A and all "don't care" conditions of the 184 are programmed high. The outputs are of the open-collector type.

DM54184 AND DM74184 BCD-TO-BINARY CONVERTERS

The 6-bit BCD-to-binary function of the DM54184 and DM74184 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.

b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the DM54184 and DM74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7 and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table when the devices are connected as shown.

DM54185A AND DM74185A BINARY-TO-BCD CONVERTERS

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

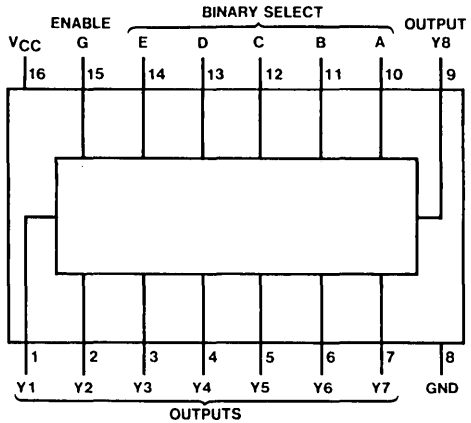
a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.

b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.

c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

(Continued)

Connection Diagram



TL/F/6561–1

Order Number DM54184J, DM54185AJ, DM74184N or DM74185AN
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Output Voltage	7V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54184, 185A			DM74184, 185A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			12			12	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

'184 and '185A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			25	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max		65	95	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max		80	99	mA

'184 and '185A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_{L1} = 400Ω, R_{L2} = 600Ω C_L = 15 pF (See Test Circuit)		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable G to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable G to Output		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Binary Select to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Binary Select to Output		35	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

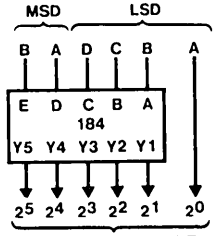
General Description (Continued)

DM54184 and DM74184 BCD-to-Binary

TABLE I. Package Count and Delay Times for BCD-to-Binary Conversion

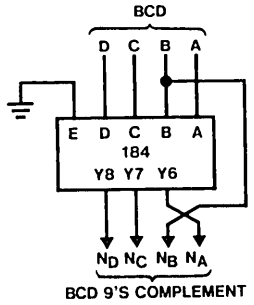
Input (Decades)	Packages Required	Total Delay Times (ns)	
		Typ	Max
2	2	56	80
3	6	140	200
4	12	196	280
5	19	280	400
6	28	364	520

6-Bit Converter



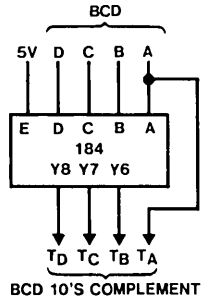
TL/F/6561-2

BCD 9's Complement Converter



TL/F/6561-3

BCD's 10's Complement Converter



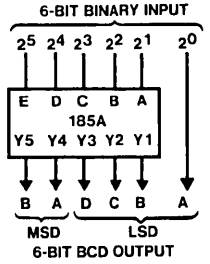
TL/F/6561-4

DM54185A and DM74185A Binary-to-BCD

TABLE II. Package Count and Delay Times for Binary-to-BCD Conversion

Input (Bits)	Packages Required	Total Delay Times (ns)	
		Typ	Max
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-Bit Converter



TL/F/6561-5

Function Tables

Binary Words		Inputs						Outputs							
		Binary Select					Enable								
		E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2	3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6	7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10	11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12	13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14	15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16	17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18	19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20	21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22	23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24	25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26	27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28	29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30	31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32	33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34	35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36	37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38	39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40	41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42	43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44	45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46	47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48	49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50	51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52	53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54	55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56	57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58	59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60	61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62	63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
All		X	X	X	X	X	H	H	H	H	H	H	H	H	H

Function Tables (Continued)

BCD-to-Binary Converter

BCD Words		Inputs (See Note A)					Outputs (See Note B)				
		E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	L	L	L	L	L
2	3	L	L	L	L	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	L	L	L	H	L
6	7	L	L	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	L	L	H	L	L
10	11	L	H	L	L	L	L	L	L	H	L	H
12	13	L	H	L	L	H	L	L	L	H	H	L
14	15	L	H	L	H	L	L	L	L	H	H	H
16	17	L	H	L	H	H	L	L	H	L	L	L
18	19	L	H	H	L	L	L	L	H	L	L	H
20	21	H	L	L	L	L	L	L	H	L	H	L
22	23	H	L	L	L	H	L	L	H	L	H	H
24	25	H	L	L	H	L	L	L	H	H	L	L
26	27	H	L	L	H	H	L	L	H	H	L	H
28	29	H	L	H	L	L	L	L	H	H	H	L
30	31	H	H	L	L	L	L	L	H	H	H	H
32	33	H	H	L	L	H	L	H	L	L	L	L
34	35	H	H	L	H	L	L	H	L	L	L	H
36	37	H	H	L	H	H	L	H	L	L	H	L
38	39	H	H	H	L	L	L	H	L	L	H	H
Any		X	X	X	X	X	H	H	H	H	H	H

BCD 9's or BCD 10's Complement Converter

BCD Word	Inputs (See Note C)						Outputs (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
Any	X	X	X	X	X	H	H	H	H

H = High Level, L = Low Level, X = Don't Care

Note A: Input Conditions other than those shown produce highs at outputs Y1 through Y5.

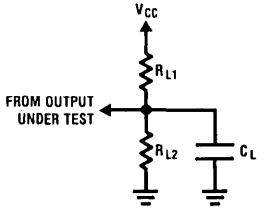
Note B: Output Y6, Y7, and Y8 are not used for BCD-to-Binary conversion.

Note C: Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

Note D: Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

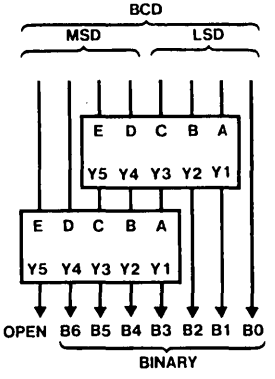
Test Circuit



TL/F/6561–6

C_L includes probe and jig capacitance

Typical Applications

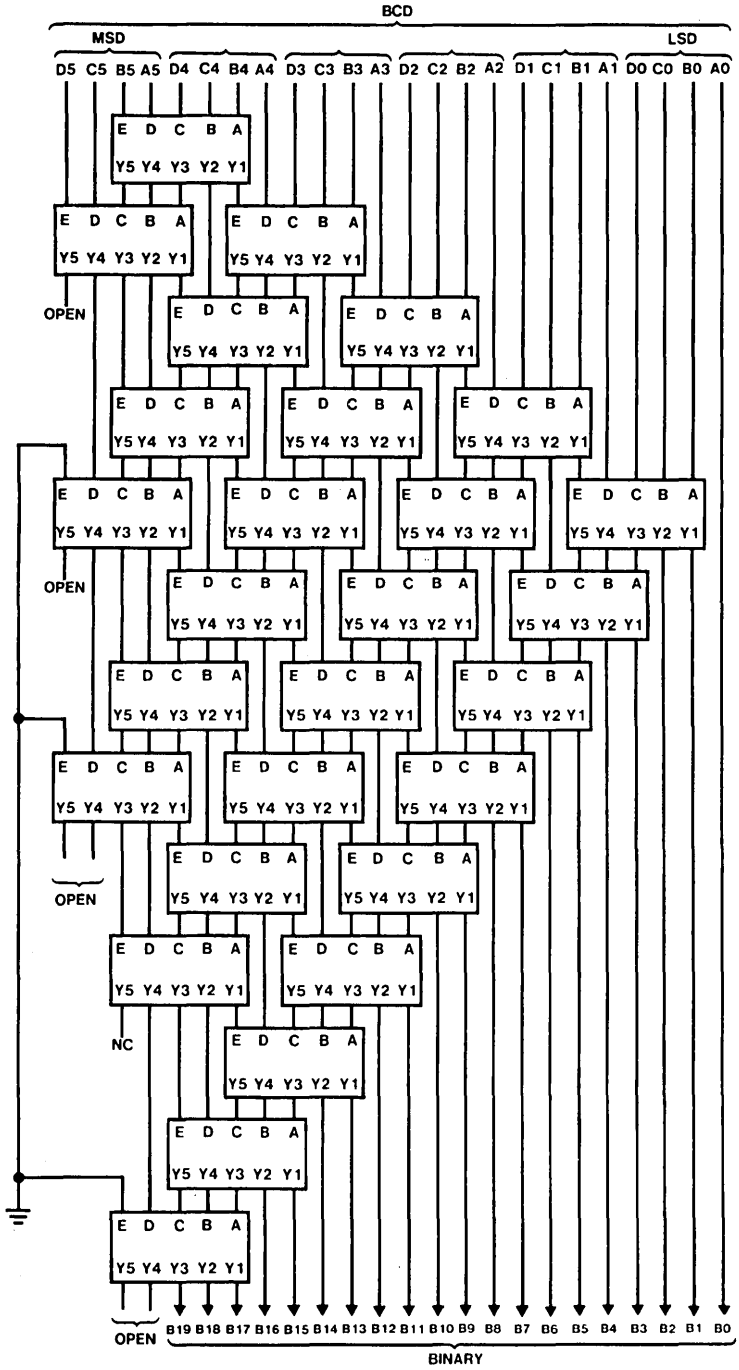


TL/F/6561–7

FIGURE 1. BCD-to-Binary Converter for Two BCD Decades

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents a DM54184 or DM74184

Typical Applications (Continued)

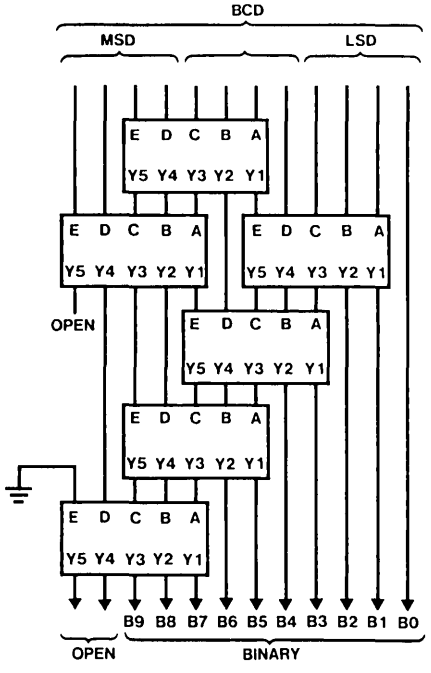


TL/F/6561–9

FIGURE 2. BCD-to-Binary Converter for Six BCD Decades

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents a DM54184 or DM74184

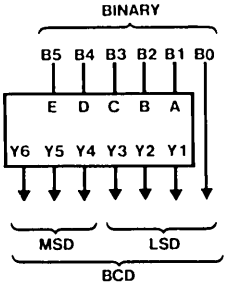
Typical Applications (Continued)



TL/F/6561–8

FIGURE 3. BCD-to-Binary Converter for Three BCD Decades

MSD—Most significant decade
LSD—Least significant decade
Each rectangle represents a DM54184 or DM74184



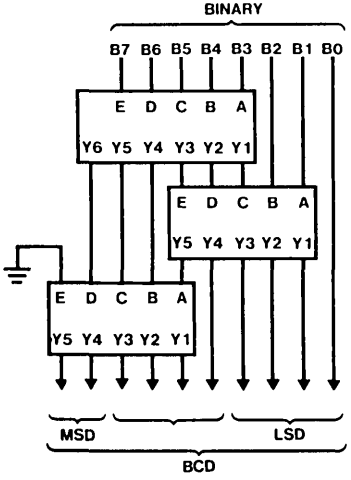
TL/F/6561–10

FIGURE 4. 6-Bit Binary-to-BCD Converter

MSD—Most significant decade
LSD—Least significant decade

Note A: Each rectangle represents a DM54185A or a DM74185A.

Note B: All unused E inputs are grounded.



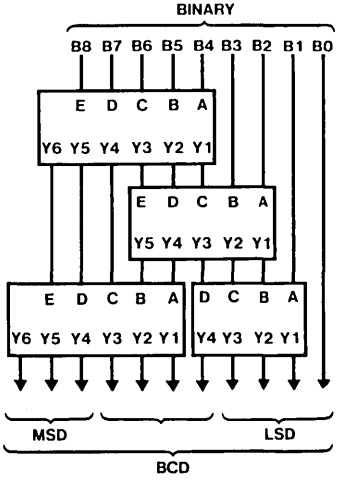
TL/F/6561–11

FIGURE 5. 8-Bit Binary-to-BCD Converter

MSD—Most significant decade
LSD—Least significant decade

Note A: Each rectangle represents a DM54185A or a DM74185A.

Note B: All unused E inputs are grounded.



TL/F/6561–12

FIGURE 6. 9-Bit Binary-to-BCD Converter

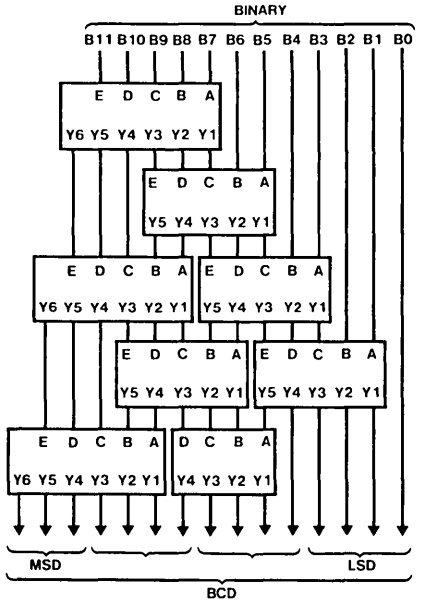
MSD—Most significant decade
LSD—Least significant decade

Note A: Each rectangle represents a DM54185A or a DM74185A.

Note B: All unused E inputs are grounded.

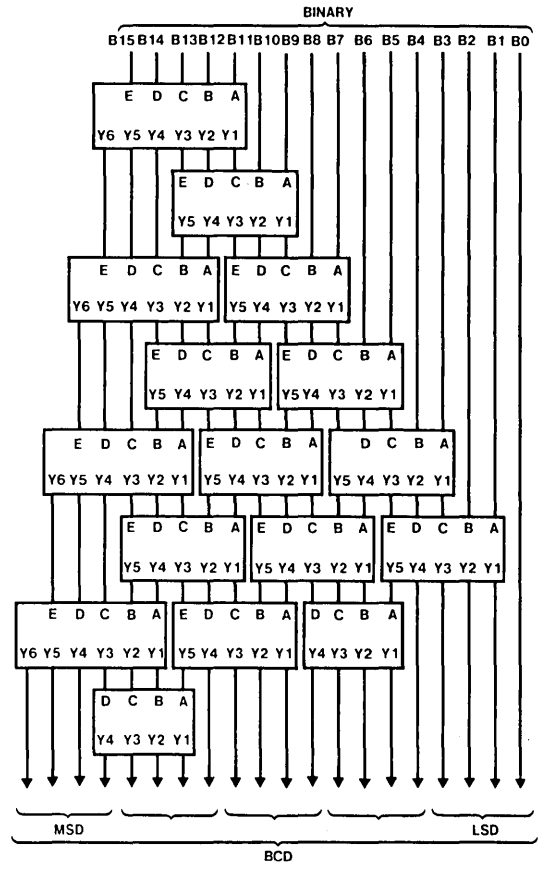
4

Typical Applications (Continued)



TL/F/6561–13

FIGURE 7. 12-Bit Binary-to-BCD Converter (See Note B)



TL/F/6561–14

FIGURE 8. 16-Bit Binary-to-BCD Converter (See Note B)

MSD—Most significant decade

LSD—Least significant decade

Note A: Each rectangle represents a DM54185A or a DM74185A.

Note B: All unused E inputs are grounded.

National Semiconductor Corporation

DM54191/DM74191 Synchronous Up/Down 4-Bit Binary Counter with Mode Control

General Description

This circuit is a synchronous, reversible, up/down counter. The 191 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. Level changes at either the enable input or the down/up input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

This counter is fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

The clock, down/up, and load inputs are buffered to lower the drive requirement; which significantly reduces the number of clock drivers, etc., required for long parallel words.

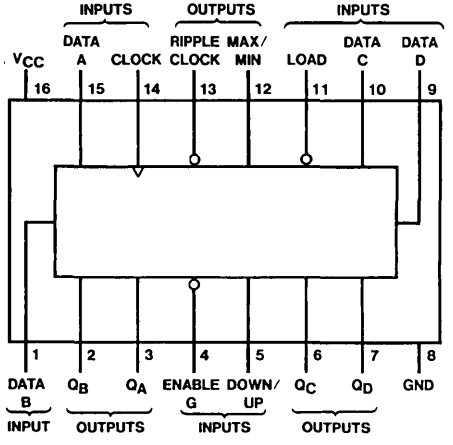
Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Features

- Single down/up count control line
- Count enable control input
- Ripple clock output for cascading
- Asynchronously presettable with load control
- Parallel outputs
- Cascadable for n-bit applications

Connection Diagram

Dual-In-Line Package



TL/F/6562–1

Order Number DM54191J or DM74191N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54191			DM74191			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0		20	0		20	MHz
t_W	Pulse Width (Note 4)	Clock	25			25			ns
		Load	35			35			
t_{SU}	Data Setup Time (Note 4)		28			28			ns
t_H	Hold Time (Note 4)		0			0			ns
t_{REL}	Load Release Time (Note 4)		30			30			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Enable			120	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Enable			−4.8	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−65	mA
			DM74	−18		−65	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		65	99	mA
			DM74		65	105	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

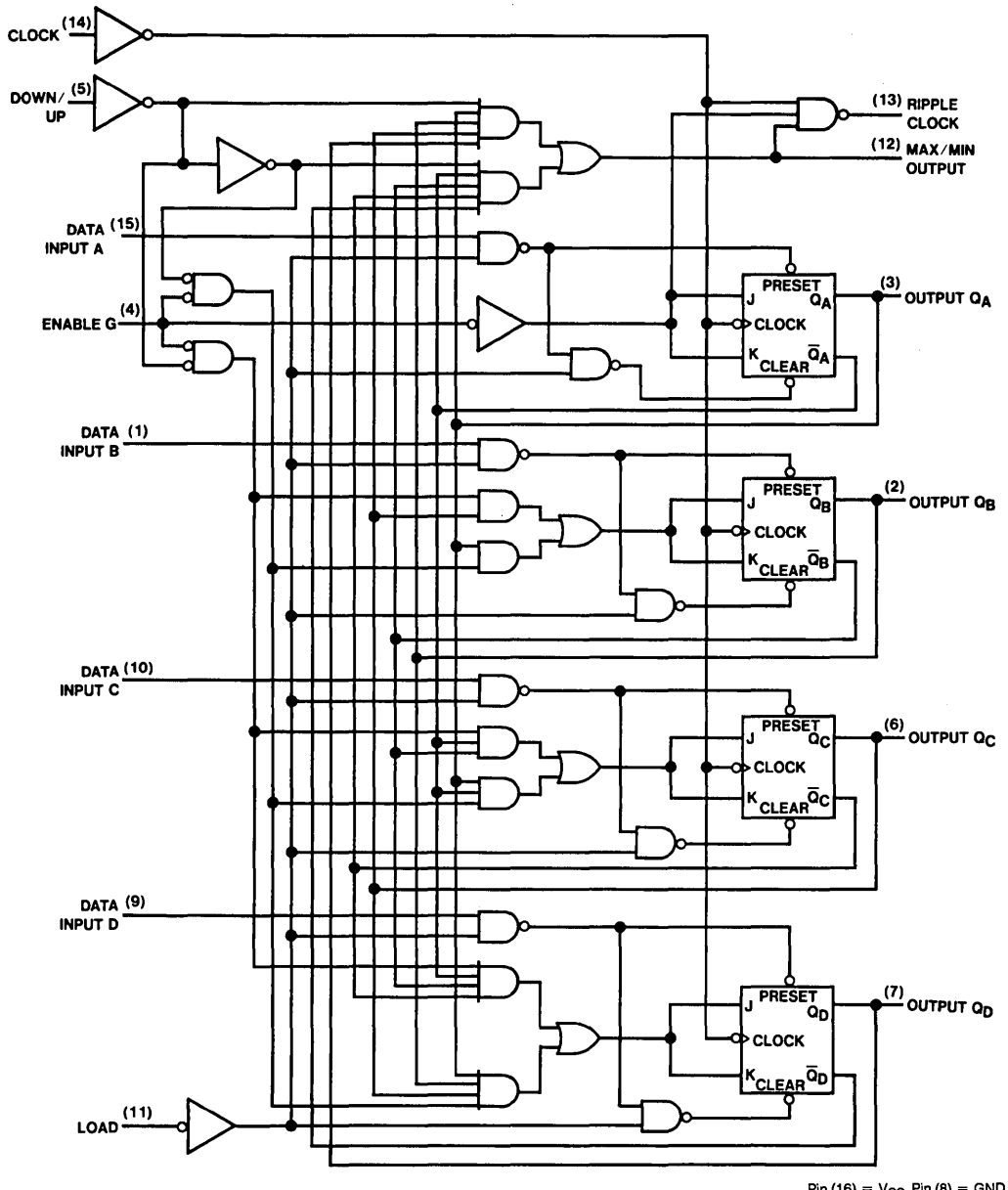
Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Any Q		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Any Q		70	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Max/Min		42	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Max/Min		52	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Down/Up to Ripple Carry		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Down/Up to Ripple Carry		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Down/Up to Max/Min		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Down/Up to Max/Min		33	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable G to Ripple Carry		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable G to Ripple Carry		24	ns

Logic Diagram

191 Binary Counter

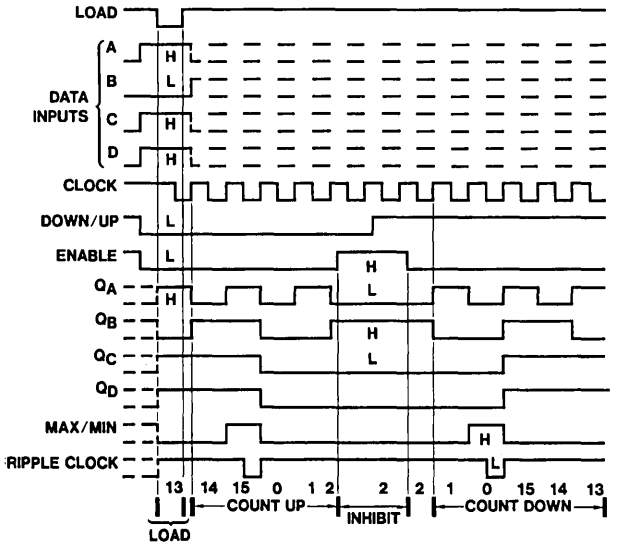


TL/F/6562-2

Pin (16) = V_{CC}, Pin (8) = GND

Timing Diagrams

191 Decade Counter
Typical Load, Count, and Inhibit Sequences



TL/F/6562–3

National Semiconductor Corporation

DM54193/DM74193 Synchronous Up/Down 4-Bit Binary Counter with Dual Clock

General Description

This circuit is a synchronous up/down 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously, so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

This counter is fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counter to be used as modulo-N divider by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

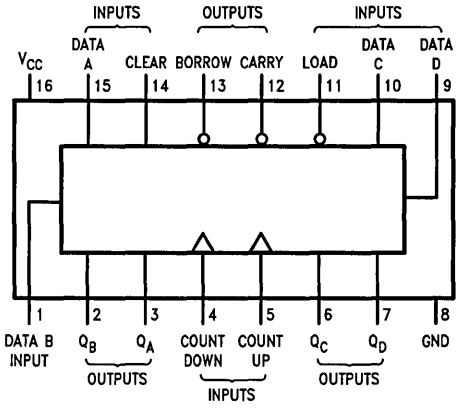
This counter was designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count up input when an overflow condition exists. The counter can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop

Connection Diagram

Dual-In-Line Package



TL/F/6563–1

Order Number DM54193J or DM74193N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54193			DM74193			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0	25	20	0	25	20	MHz
t_W	Pulse Width (Note 4)	Clock Low	30			30			ns
		Clock, Clear High Load Low	20			20			
t_{SU}	Data Setup Time (Note 4)		20			20			ns
t_H	Hold Time (Note 4)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		65	89	mA
			DM74		65	102	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25° C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

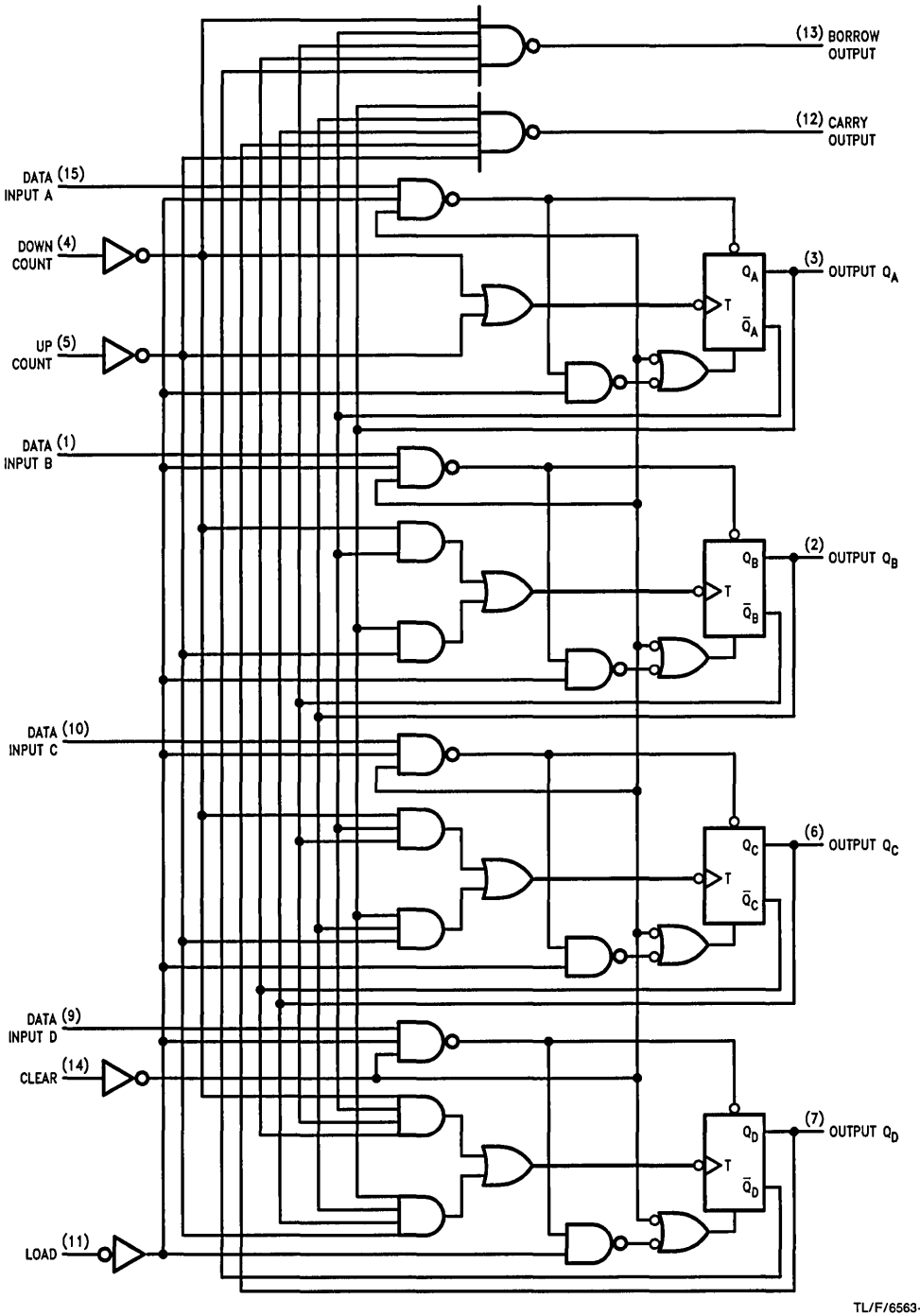
Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		20		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Up to Carry		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Up to Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Count Down to Borrow		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Count Down to Borrow		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Either Count to Q		38	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Either Count to Q		47	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Q		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Q		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		35	ns

Logic Diagrams

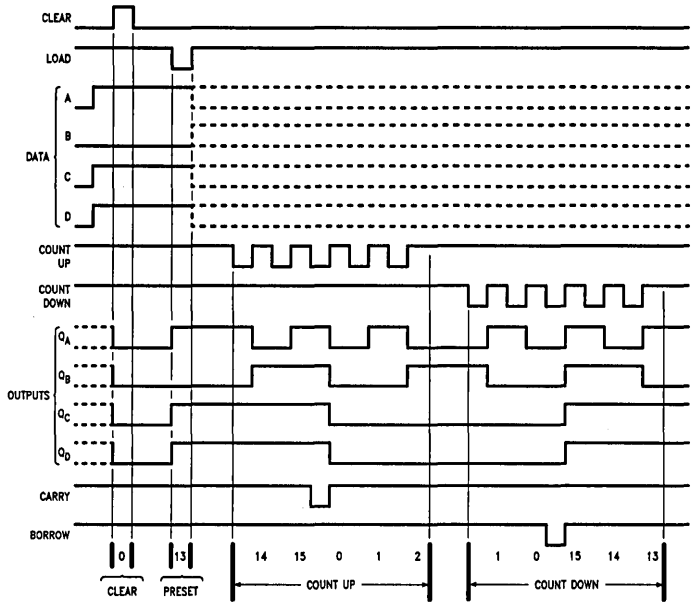
193



TL/F/6563–2

Timing Diagram

193 Binary Counter
Typical Clear, Load, and Count Sequences



TL/F/6563–3

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high, when counting down, count-up input must be high.

National Semiconductor Corporation

DM54194/DM74194 4-Bit Bidirectional Universal Shift Registers

General Description

This bidirectional shift register is designed to incorporate virtually all of the features a system designer may want in a shift register; it features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

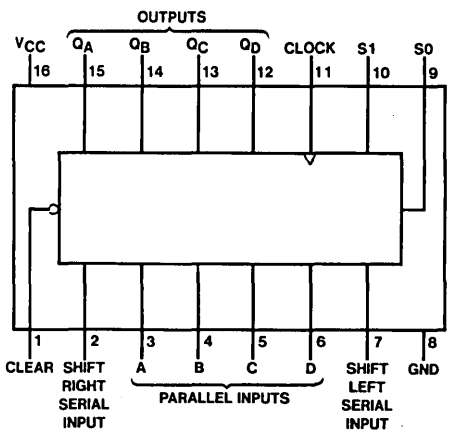
Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls of the DM54194/DM74194 should be changed only while the clock input is high.

Features

- Parallel inputs and outputs
- Four operating modes:
  - Synchronous parallel load
  - Right shift
  - Left shift
  - Do nothing
- Positive edge-triggered clocking
- Direct overriding clear
- Typical clock frequency 36 MHz
- Typical power dissipation 195 mW

Connection Diagram

Dual-In-Line Package



TL/F/6564–1

Order Number DM54194J or DM74194N
See NS Package Number J16A or N16A

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54194			DM74194			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 4)		0	36	25	0	36	25	MHz
t_W	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 4)	Mode	30			30			ns
		Data	20			20			
t_H	Hold Time (Note 4)		0			0			ns
t_{REL}	Clear Release Time (Note 4)		25			25			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−57	mA
			DM74	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			39	63	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: With all outputs open, inputs A through D grounded, and 4.5V applied to S0, S1, CLEAR and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5V applied to CLOCK.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		30	ns

Function Table

Inputs										Outputs			
Clear	Mode		Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D
	S1	S0		Left	Right	A	B	C	D				
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

H = High Level (steady state), L = Low Level (steady state), X = Don't Care (any input, including transitions)

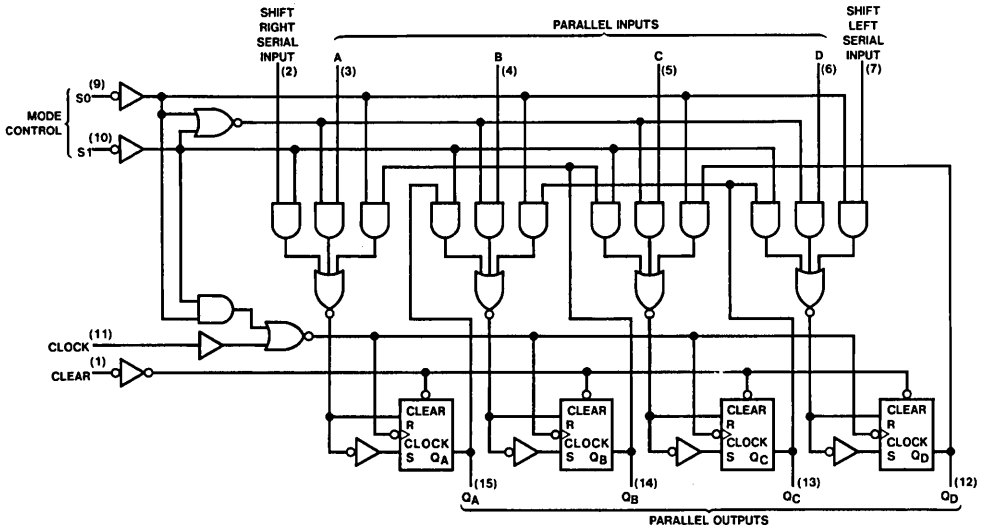
↑ = Transition from low to high level; a, b, c, d = The level of steady state input at inputs A, B, C, or D, respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock.

Logic Diagram

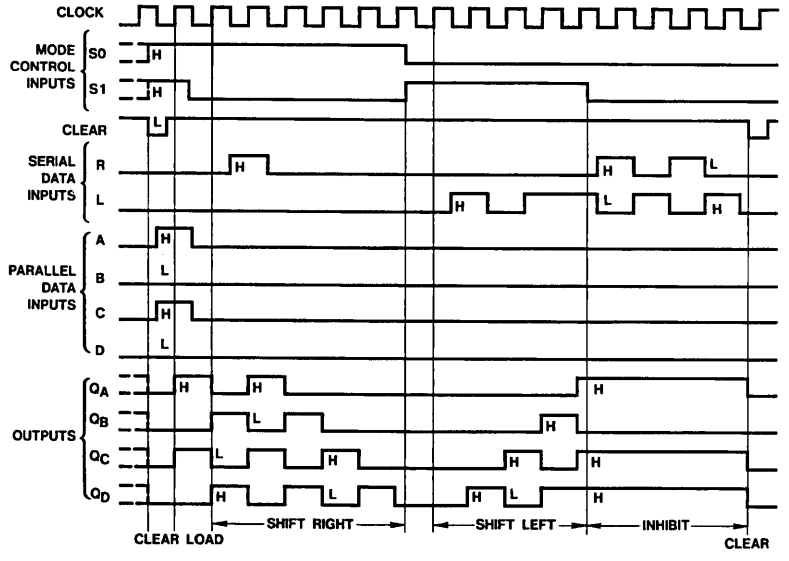
194



TL/F/6564–2

Timing Diagram

Typical Clear, Load, Right-Shift, Left-Shift, Inhibit and Clear Sequences



TL/F/6564–3

National Semiconductor Corporation

DM54259/DM74259 8-Bit Addressable Latches

General Description

These 8-bit addressable latches are designed for general purpose storage applications in digital systems. Specific uses include working registers, serial-holding registers, and active-high decoders or demultiplexers. They are multifunctional devices capable of storing single-line data in eight addressable latches, and being a 1-of-8 decoder or demultiplexer with active-high outputs.

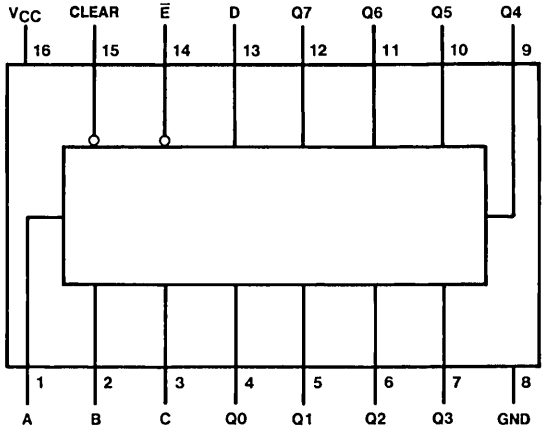
Four distinct modes of operation are selectable by controlling the clear and enable inputs as enumerated in the function table. In the addressable-latch mode, data at the data-in terminal is written into the addressed latch. The addressed latch will follow the data input with all unaddressed latches remaining in their previous states. In the memory mode, all latches remain in their previous states and are unaffected by the data or address inputs. To eliminate the possibility of entering erroneous data in the latches, the enable should be held high (inactive) while the address lines are changing. In the 1-of-8 decoding or demultiplexing mode, the addressed output will follow the level of the D input with all other outputs low. In the clear mode, all outputs are low and unaffected by the address and data inputs.

Features

- 8-bit parallel-out storage register performs serial-to-parallel conversion with storage
- Asynchronous parallel clear
- Active high decoder
- Enable/disable input simplifies expansion
- Direct replacement for Fairchild 9334
- Expandable for N-bit applications
- Four distinct functional modes
- Typical propagation delay times:
  - Enable-to-output 18 ns
  - Data-to-output 21 ns
  - Address-to-output 22 ns
  - Clear-to-output 21 ns
- Fan-Out
  - I_{OL} (sink current) 16 mA
  - I_{OH} (source current) −0.8 mA
- Typical I_{CC} 60 mA

Connection Diagram

Dual-In-Line Package



TL/F/6569–1

Order Number DM54259J or DM74259N
See NS Package Number J16A or N16A

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54259			DM74259			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	Pulse Width (Note 6)	Enable	19	13		19	13		ns
		Clear	19	13		19	13		
t_{SU}	Setup Time (Notes 1, 2, 3 & 6)	Data	20	13		20	13		ns
		Select	10	5		10	5		
t_H	Hold Time (Notes 1 & 6)	Data	0	−10		0	−10		ns
		Select	0	−13		0	−13		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 3)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 4)	DM54	−20		−55	mA
			DM74	−20		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 5)				90	mA

Note 1: Setup and hold times are with reference to the enable input.

Note 2: The select-to-enable setup time is the time before the High-to-Low enable transition that the select must be stable so that the correct latch is selected and the others not affected.

Note 3: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 4: Not more than one output should be shorted at a time.

Note 5: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		31	ns

Function Tables

Inputs		Output of Addressed Latch	Each Other Output	Function
Clear	$\overline{E}$			
H	L	D	Q_{i0}	Addressable Latch
H	H	Q_{i0}	Q_{i0}	Memory
L	L	D	L	8-Line Demultiplexer
L	H	L	L	Clear

Latch Selection Table

Select Inputs			Latch Addressed
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

H = High Level, L = Low Level

D = The level of the data input

Q_{i0} = The level of Q_i (i = 0, 1, . . . 7, as appropriate) before the indicated steady-state input conditions were established.

National Semiconductor Corporation

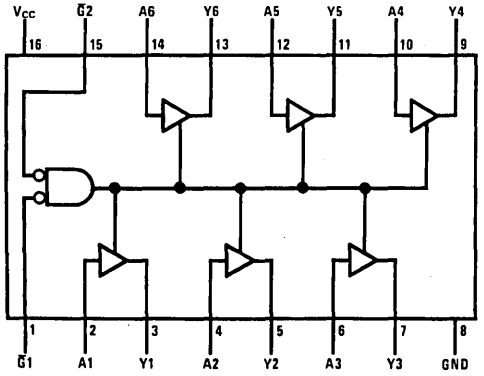
DM54365/DM74365 Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6570–1

Order Number DM54365J or DM74365N
See NS Package Number J16A or N16A

Function Table

$Y = A$

Input			Output
$\overline{G}1$	$\overline{G}2$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Hi-Z
X	H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54365			DM74365			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			32			32	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	µA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	µA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−115	mA
			DM74	−40		−115	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			59	85	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the data inputs grounded, and the output controls at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				22	ns
t_{PZH}	Output Enable Time to High Level Output				35	ns
t_{PZL}	Output Enable Time to Low Level Output				37	ns
t_{PHZ}	Output Disable Time from High Level Output		11			ns
t_{PLZ}	Output Disable Time from Low Level Output		27			ns

National Semiconductor Corporation

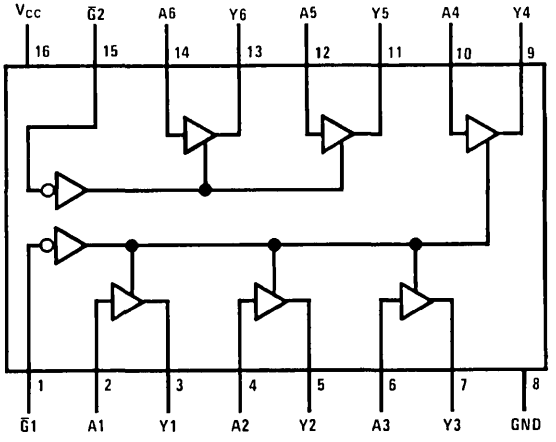
DM54367/DM74367 Hex TRI-STATE® Buffers

General Description

This device contains six independent gates each of which performs a non-inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a signficant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6572–1

Order Number DM54367J or DM74367N
See NS Package Number J16A or N16A

Function Table

$Y = A$

Input		Output
$\overline{G}$	A	Y
L	L	L
L	H	H
H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54367			DM74367			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			32			32	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−115	mA
			DM74	−40		−115	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			65	85	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the data inputs grounded and the output controls at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				22	ns
t_{PZH}	Output Enable Time to High Level Output				35	ns
t_{PZL}	Output Enable Time to Low Level Output				37	ns
t_{PHZ}	Output Disable Time from High Level Output		11			ns
t_{PLZ}	Output Disable Time from Low Level Output		27			ns

National Semiconductor Corporation

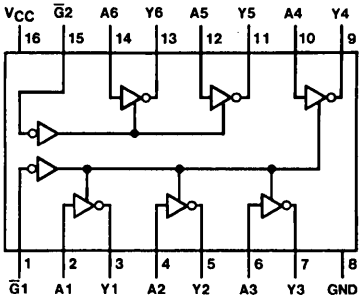
DM54368/DM74368 Hex TRI-STATE® Inverting Buffers

General Description

This device contains six independent gates each of which performs an inverting buffer function. The outputs have the TRI-STATE feature. When enabled, the outputs exhibit the low impedance characteristics of a standard TTL output with additional drive capability to permit the driving of bus lines without external resistors. When disabled, both the output transistors are turned off presenting a high-impedance state to the bus line. Thus the output will act neither as a significant load nor as a driver. To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the disable time is shorter than the enable time of the outputs.

Connection Diagram

Dual-In-Line Package



TL/F/6573–1

Order Number DM54368J or DM74368N
See NS Package Number J16A or N16A

Function Table

$Y = \overline{A}$

Inputs		Output
$\overline{G}$	A	Y
L	L	H
L	H	L
H	X	Hi-Z

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54	−55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54368			DM74368			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			32			32	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.5V (Note 4)	A			−40	mA
		V_{CC} = Max V_I = 0.4V (Note 5)	A			−1.6	
		V_{CC} = Max V_I = 0.4V	$\overline{G}$			−1.6	
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−40		−115	mA
			DM74	−40		−115	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			59	77	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the data inputs grounded, and the output controls at 4.5V.

Note 4: Both $\overline{G}$ inputs are at 2V.

Note 5: Both $\overline{G}$ inputs are at 0.4V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				17	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				16	ns
t_{PZH}	Output Enable Time to High Level Output				35	ns
t_{PZL}	Output Enable Time to Low Level Output				37	ns
t_{PHZ}	Output Disable Time from High Level Output		11			ns
t_{PLZ}	Output Disable Time from Low Level Output		27			ns

National Semiconductor Corporation

DM7123/DM8123 Quad 2-Input Data Selectors/Multiplexers

General Description

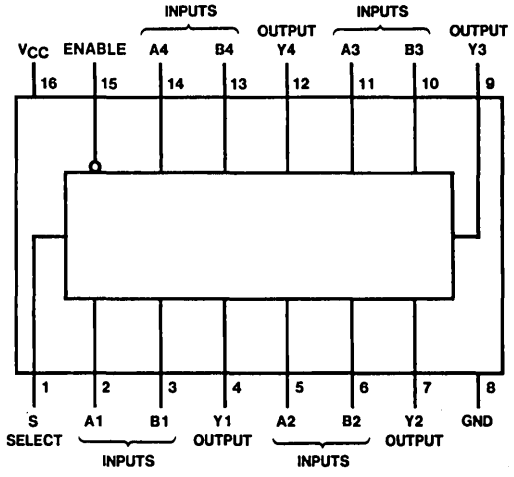
This device contains four 2-input multiplexers with common input select logic and common output disable circuitry. The DM7123/8123 provides TRI-STATE® outputs. When the enable/strobe input is at a low logic level, the outputs of all devices are conventional TTL. However, when the enable/strobe input is raised to a high logic level, the outputs of the DM7123/8123 go to the high-impedance third state. This device provides the designer with TRI-STATE and/or low power pin/pin replacements for the popular 9322 and 54/74157 multiplexers.

Features

- Pin equivalents popular 9322 and 54/74157 multiplexers
- Both conventional TTL and TRI-STATE outputs available
- Typical propagation delay 9.5 ns
- Typical power dissipation 200 mW

Connection Diagram

Dual-In-Line Package



TL/F/6574–1

Order Number DM7123J or DM8123N
See NS Package Number J16A or N16A

Function Table

Enable	Select	Inputs		Outputs
		A	B	Y
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H
H	X	X	X	Hi-Z

L = Low Logic Level, H = High Logic Level
X = Either Low or High Logic Level
Hi-Z = TRI-STATE (Outputs are disabled)

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM71	−55°C to +125°C
DM81	0°C to +70°C
Storage Temperature Range	−65°C to +150° C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7123			DM8123			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	DM71	2.4			V
			DM81	2.4			
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V, V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V, V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM71	−30		−70	mA
			DM81	−30		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			40	51	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

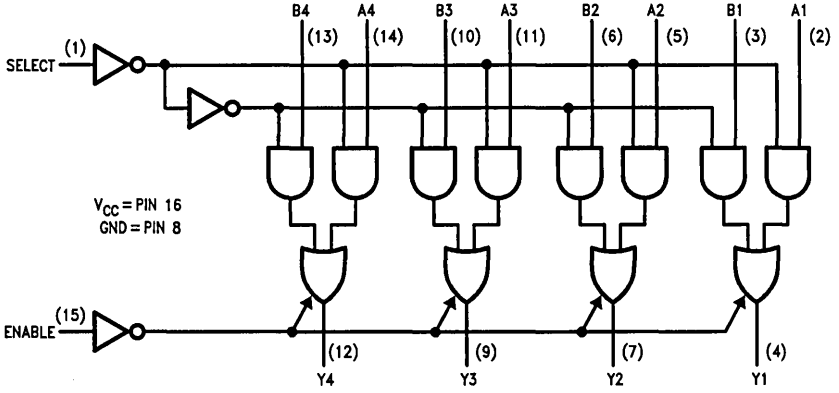
Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with the inputs grounded, and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω				Units
			C_L = 5 pF		C_L = 50 pF		
			Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output			4	15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output			5	18	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output			5	23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output			8	24	ns
t_{PZH}	Output Enable Time to High Level Output	Enable to Q			9	25	ns
t_{PZL}	Output Enable Time to Low Level Output	Enable to Q			10	30	ns
t_{PHZ}	Output Disable Time from High Level Output	Enable to Q	4	11			ns
t_{PLZ}	Output Disable Time from Low Level Output	Enable to Q	9	27			ns

Logic Diagram



TL/F/6574–2

National Semiconductor Corporation

DM7130/DM8130 Magnitude Comparators

General Description

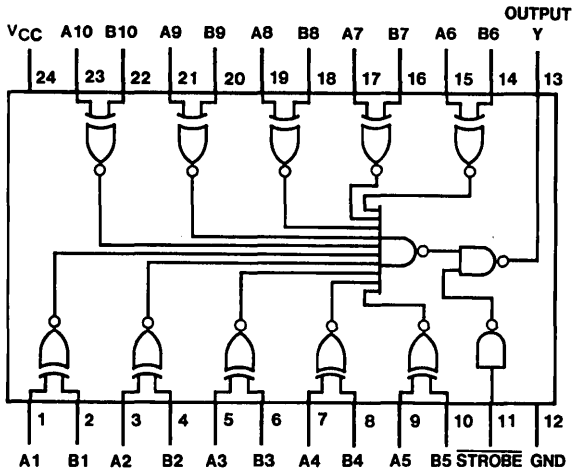
This device offers comparisons to determine equality between two binary words. The DM7130/DM8130 compares two ten-bit words. A strobe override is provided. When the strobe is taken to a high logic level, the output is forced to a high logic level. The device also features open collector outputs for expansion.

Features

- Typical propagation delay 21 ns
- Typical power dissipation 240 mW
- Open-collector outputs for expansion

Connection Diagram

Dual-In-Line Package



TL/F/6575–1

Order Number DM7130J or DM8130N
See NS Package Number J24A or N24A

Function Table

Condition	$\overline{\text{STROBE}}$ S	Output Y
A = B, A ≠ B	H	H
A = B	L	H
A ≠ B	L	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM71	−55°C to +125°C
DM81	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7130			DM8130			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IH} = Min			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)		48	70	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

National Semiconductor Corporation

DM7131/DM8131 6-Bit Unified Bus Comparator

General Description

The DM7131/DM8131 compares two binary words of two-to-six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65V typical hysteresis, which provides 1.4V noise immunity. The DM7131/DM8131 has active pull-up outputs and goes to the low state upon equality. The device has an output latch which is strobe controlled.

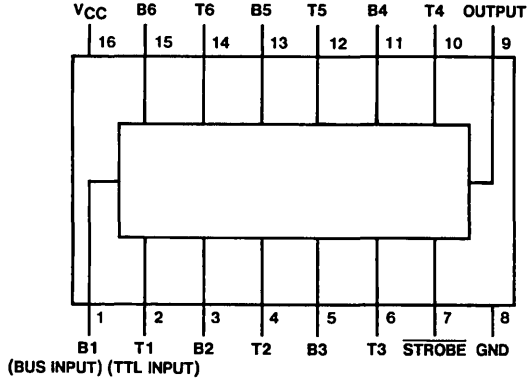
The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to a logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

Features

- Low bus input current 15 μA typ
- High bus input noise immunity 1.4V typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

Connection Diagram

Dual-In-Line Package



TL/F/6576–1

Order Number DM7131J or DM8131N
See NS Package Number J16A or N16A

Function Table

Condition	$\overline{\text{STROBE}}$	Output
		DM71/8131
T = B, T ≠ B	H	Q_{N-1}*
T = B	L	L
T ≠ B	L	H

*Latched in a previous state.
H = High Logic Level.
L = Low Logic Level.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM71	−55°C to +125°C
DM81	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7131			DM8131			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage for Bus Inputs (Note 1)	1.4	1.75	2	1.45	1.75	1.95	V
V_{T-}	Negative-Going Input Threshold Voltage for Bus Inputs (Note 1)	0.9	1.1	1.35	0.95	1.1	1.3	V
V_{IH}	High Level Input Voltage for Strobe and TTL Inputs	2			2			V
V_{IL}	Low Level Input Voltage for Strobe and TTL Inputs			0.8			0.8	V
I_{OH}	High Level Output Current			−0.4			−0.4	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V	TTL			1	mA
			Strobe			2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	TTL			40	μA
			Strobe			80	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	TTL			−1.6	mA
			Strobe			−2.4	
I_{IN}	Bus Input Current	V_I = 4V	V_{CC} = Max		15	50	μA
			V_{CC} = 0V		1	50	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM71	−18		−55	mA
			DM81	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)			50	74	mA

Note 1: V_{CC} = 5V

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

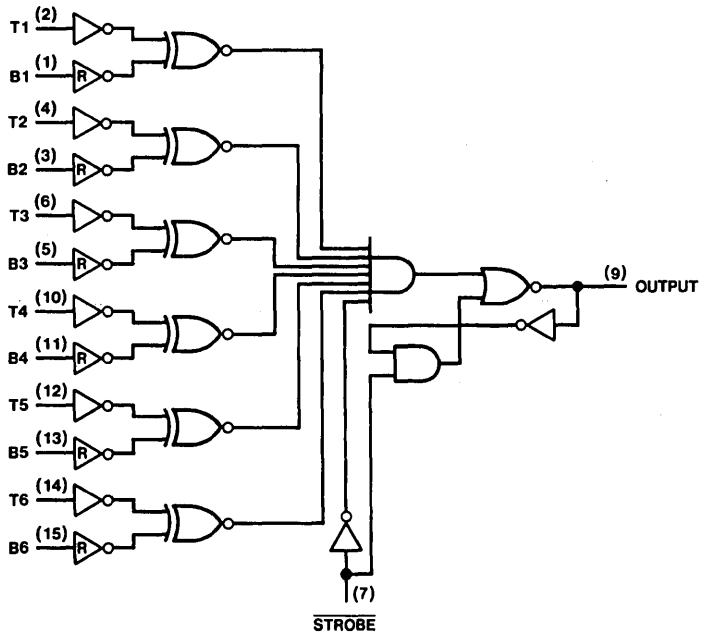
Note 4: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	TTL to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	TTL to Output		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Bus to Output		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Bus to Output		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		30	ns

Logic Diagram

DM71/8131



TL/F/6576–2

R = High Impedance Bus Receiver

National Semiconductor Corporation

DM7136/DM8136 6-Bit Unified Bus Comparator with Open-Collector Outputs

General Description

The DM7136/DM8136 compares two binary words of two-to-six bits in length and indicates matching (bit-for-bit) of the two words. Inputs for one word are 54/74 series-compatible TTL inputs, whereas those of the second word are high-impedance receivers driven by a terminated data bus. These bus inputs include 0.65V typical hysteresis which provides 1.4V noise immunity. The DM7136/DM8136 has open-collector outputs which go to the high state upon equality and is expandable to n bits by collector-ORing. The device has an output latch which is strobe controlled.

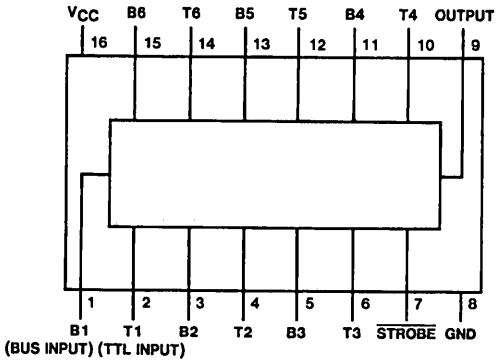
The transfer of information to the output occurs when the $\overline{\text{STROBE}}$ input goes from a logic "1" to a logic "0" state. Inputs may be changed while the $\overline{\text{STROBE}}$ is at the logic "1" level, without affecting the state of the output. These devices are useful as address comparators in computer systems utilizing unified data bus organization.

Features

- Low bus input current 15 μA typ
- High bus input noise immunity 1.4V typ
- Bus inputs comply with IEEE 488-1975
- TTL-compatible output
- Output latch provision

Connection Diagram

Dual-In-Line Package



TL/F/6577–1

Order Number DM7136J or DM8136N
See NS Package Number J16A or N16A

Function Table

Condition	$\overline{\text{STROBE}}$	Output
		DM71/8136
T = B, T ≠ B	H	Q_{N-1}*
T = B	L	H
T ≠ B	L	L

*Latched in previous state.

H = High Logic Level

L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM71	−55°C to +125°C
DM81	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7136			DM8136			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage for Bus Inputs (Note 1)	1.4	1.75	2	1.45	1.75	1.95	V
V_{T-}	Negative-Going Input Threshold Voltage for Bus Inputs (Note 1)	0.9	1.1	1.35	0.95	1.1	1.3	V
V_{IH}	High Level Input Voltage for TTL and Strobe Inputs	2			2			V
V_{IL}	Low Level Input Voltage for TTL and Strobe Inputs			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max, V_{IH} = Min				250	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	TTL			1	mA
			Strobe			2	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	TTL			40	μA
			Strobe			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	TTL			−1.6	mA
			Strobe			−2.4	
I_{IN}	Bus Input Current	V_I = 4V	V_{CC} = Max		15	50	μA
			V_{CC} = 0V		1	50	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			50	74	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

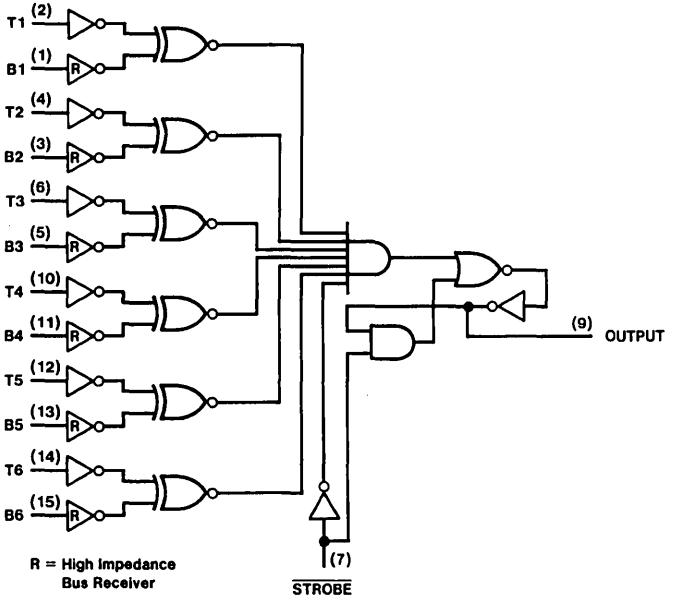
Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	TTL to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	TTL to Output		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Bus to Output		45	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Bus to Output		45	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		30	ns

Logic Diagram

DM71/8136



TL/F/6577–2

National Semiconductor Corporation

DM7160/DM8160 Magnitude Comparators

General Description

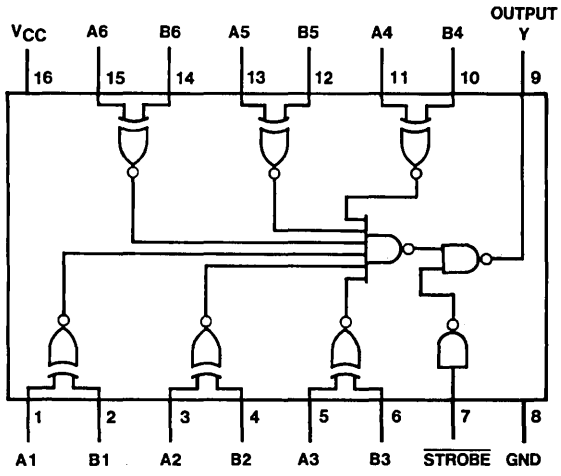
This device offers comparisons to determine equality between two binary words. The DM7160/DM8160 compares two six-bit words. A strobe override is provided. When the strobe is taken to a high logic level, the output is forced to a high logic level. The device also features open-collector outputs for expansion.

Features

- Typical propagation delay 21 ns
- Typical power dissipation 205 mW
- Open-collector outputs for expansion

Connection Diagram

Dual-In-Line Package



TL/F/6578–1

Order Number DM7160J or DM8160N
See NS Package Number J16A or N16A

Function Table

Condition	$\overline{\text{STROBE}}$ S	Output Y
A = B, A ≠ B	H	H
A = B	L	H
A ≠ B	L	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM71	−55°C to +125°C
DM81	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7160			DM8160			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
V_{OH}	High Level Output Voltage			5.5			5.5	V
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
I_{CEX}	High Level Output Current	V_{CC} = Min, V_O = 5.5V V_{IL} = Max			100	μA
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min		0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{CC}	Supply Current	V_{CC} = Max (Note 2)		41	60	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		40	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		30	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all inputs grounded and all outputs open.

National Semiconductor Corporation

DM7556/DM8556 TRI-STATE® Programmable Binary Counters

General Description

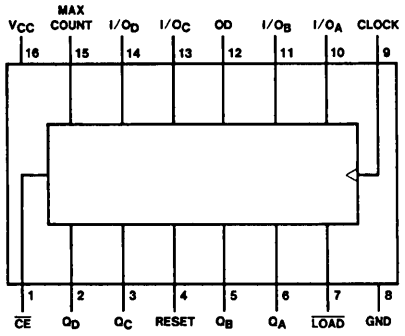
These circuits are synchronous, edge-sensitive, fully-programmable 4-bit counters. The counters feature both conventional totem-pole and TRI-STATE outputs; such that when the outputs are in the high impedance mode, they can be used to enter data from the bus lines. In addition, the clear input operates completely independent of all other inputs. During the programming operation, data is loaded into the flip-flops on the positive-going edge of the clock pulse. To facilitate cascading of these counters, the MAX COUNT output can be tied directly into the count enable input of the next counter.

Features

- Typical clock frequency 35 MHz
- TRI-STATE outputs
- Fully independent clear
- Synchronous loading
- Cascading circuitry provided internally

Connection Diagram

Dual-In-Line Package



TL/F/6588–1

Order Number DM7556J or DM8556N
See NS Package Number J16A or N16A

Function Table

Control Inputs					I/O Ports				Active Outputs			
$\overline{LOAD}$	$\overline{CE}$	CLK	OD	Reset	I/O_A	I/O_B	I/O_C	I/O_D	Q_A	Q_B	Q_C	Q_D
H	X	X	L	H	L	L	L	L	L	L	L	L
H	X	X	H	H	Z	Z	Z	Z	L	L	L	L
H	X	L	L	L	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	X	L	H	L	Z	Z	Z	Z	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	H	↑	L	L	a	b	c	d	A	B	C	D
H	L	↑	L	L		COUNT				COUNT		
H	L	↑	H	L	Z	Z	Z	Z		COUNT		

The I/O pins are used as inputs when they are TRI-STATED, and the $\overline{LOAD}$ input is Low. They are outputs and active when $\overline{LOAD}$ input is High and OD is Low.

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care including transitions

a, b, c, d = The level of the steady state input at inputs A, B, C, D respectively

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, Q_D respectively, before the indicated steady state input conditions were established.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM75	−55°C to +125°C
DM85	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM7556			DM8556			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−2			−5.2	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 1)		0		25	0		25	MHz
t_W	Pulse Width (Note 1)	Clock	25			25			ns
		Clear	20			20			
		Load	30			30			
$t_{\overline{CE}}$	Count Enable Time (Note 1)	Setup	30			30			ns
		Hold	−10			−10			
$t_{SETUP(1)}$	Setup Time High Logic Level (Note 1)	Data	25			25			ns
		Load	30			30			
$t_{HOLD(1)}$	Hold Time High Logic Level (Note 1)	Data	5			5			ns
		Load	−10			−10			
$t_{SETUP(0)}$	Setup Time Low Logic Level (Note 1)	Data	30			30			ns
		Load	25			25			
$t_{HOLD(0)}$	Hold Time Low Logic Level (Note 1)	Data	5			5			ns
		Load	−10			−10			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−25		−70	mA
			DM85	−25		−70	
I_{CC}	Supply Current	V_{CC} = Max			75	100	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

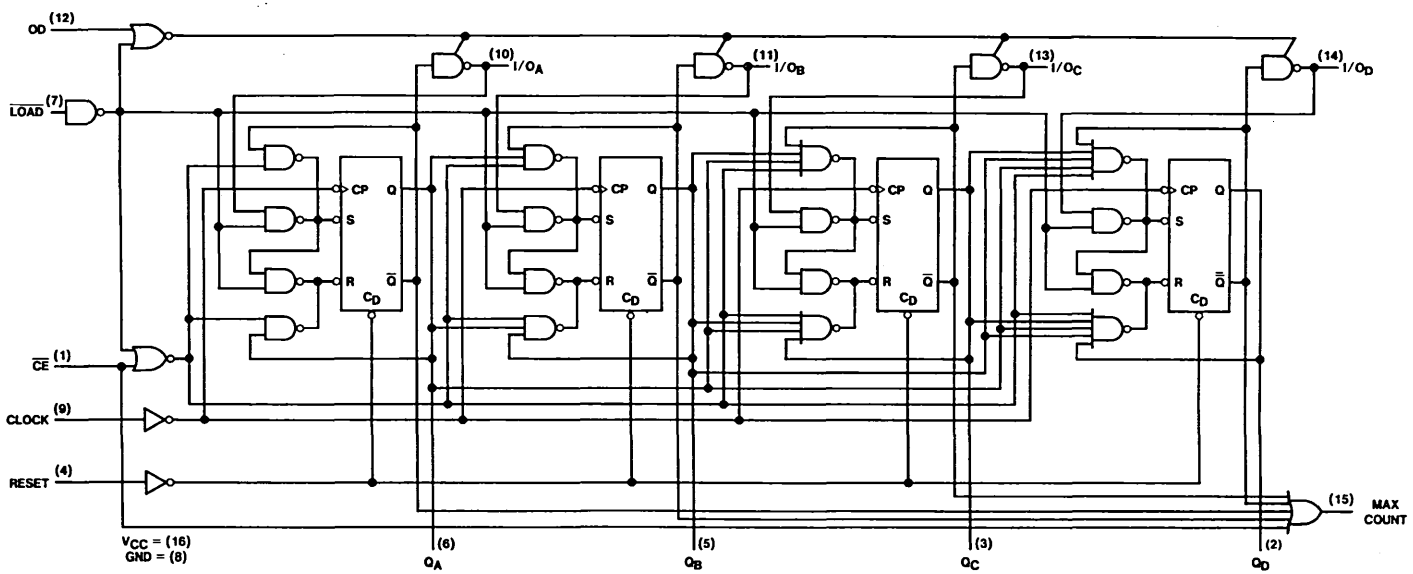
Note 2: Not more than one output should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω				Units
			C_L = 5 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency				25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output				22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output				44	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to MAX-CNT				33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to MAX-CNT				33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Reset to Output				44	ns
t_{PZH}	Output Enable Time to High Level Output	Output Disable to Q				20	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Disable to Q				20	ns
t_{PHZ}	Output Disable Time from High Level Output	Output Disable to Q		12			ns
t_{PLZ}	Output Disable Time from Low Level Output	Output Disable to Q		20			ns

Logic Diagram

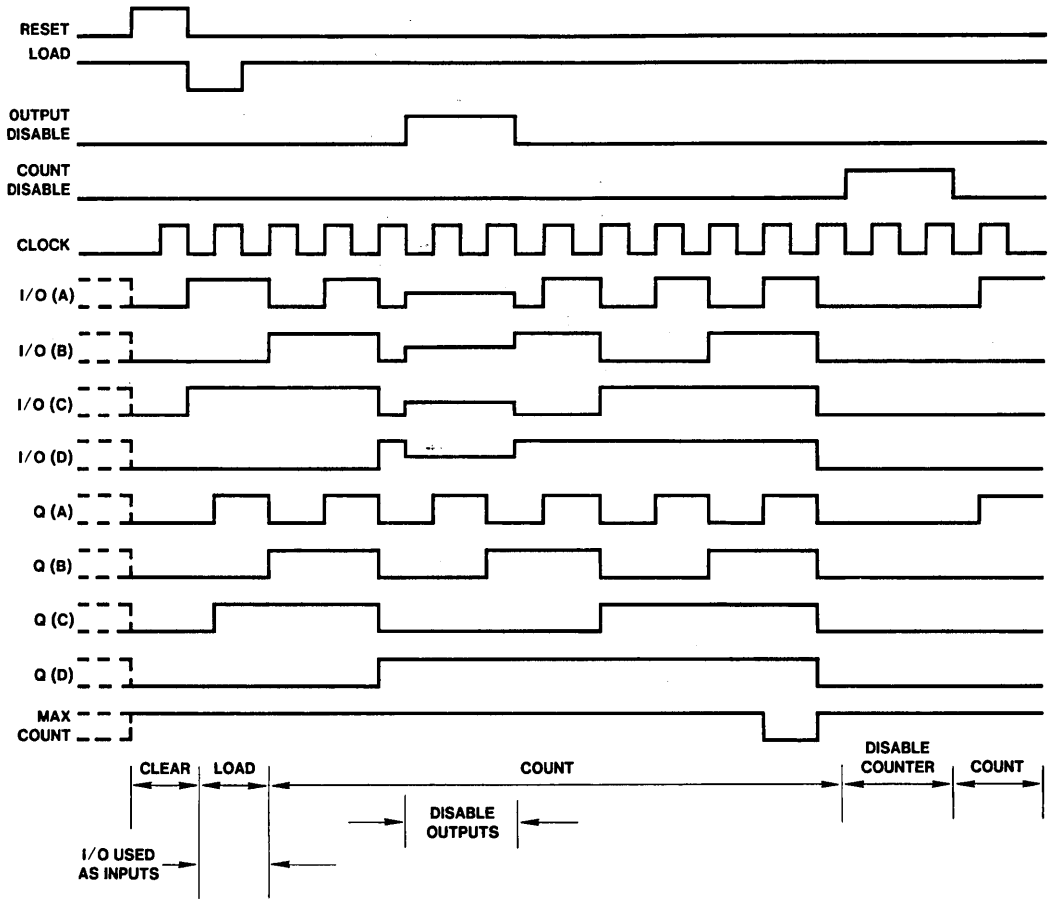
75/8556



TL/F/6588–2

Timing Diagram

75/8556 Typical Clear, Preset, Count, Inhibit Sequence



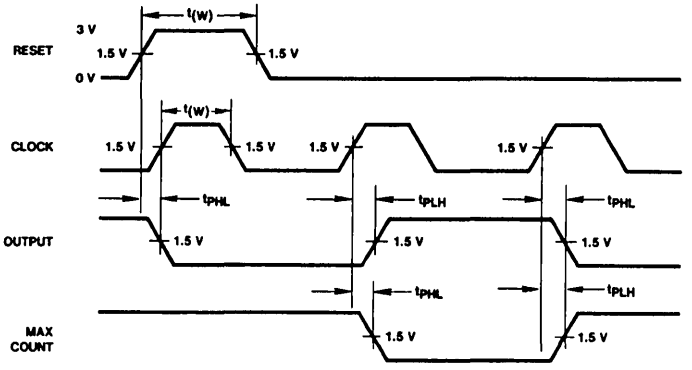
TL/F/6588–3

Sequence

(1) Clear to zero.
(2) Load binary five.
(3) Count six, seven, eight, nine, ten, eleven, twelve, thirteen, fourteen, fifteen, zero.
(4) Disable TRI-STATE outputs.
(5) Disable counter.
(6) Count to one.

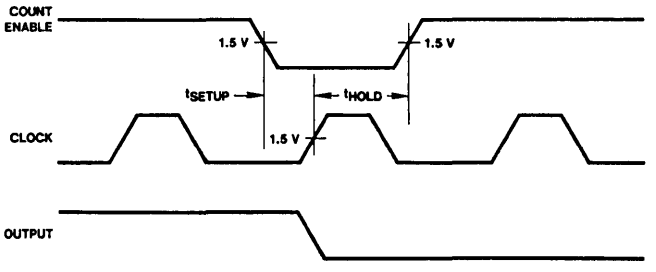
Switching Time Waveforms

Clock and Reset Voltage



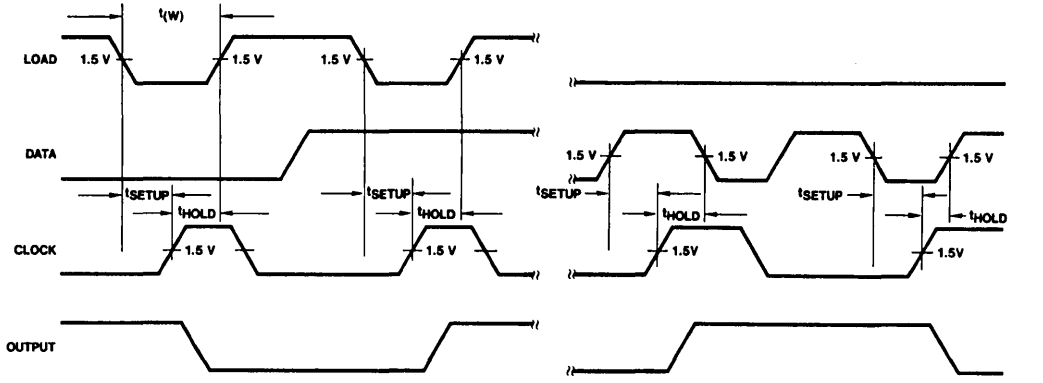
TL/F/6588–4

Count Enable and Clock



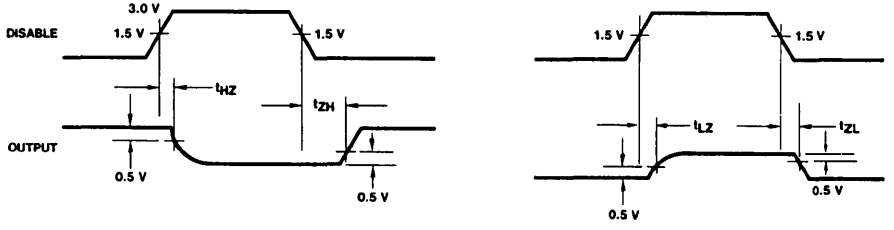
TL/F/6588–5

Load, Data and Clock



TL/F/6588–6

Output Disable



TL/F/6588–7

National Semiconductor Corporation

DM7875A/DM8875A, DM7875B/DM8875B TRI-STATE® 4-Bit Parallel Binary Multipliers

General Description

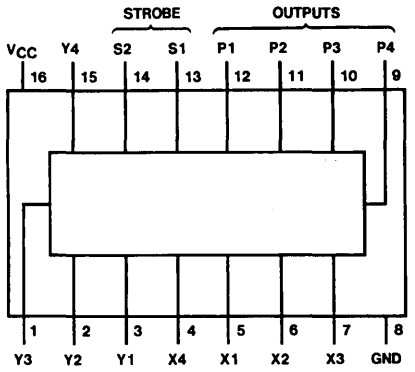
These circuits are capable of multiplying together two 4-bit binary numbers when used together in pairs. The DM7875A/8875A provides the most significant four bits, and the DM7875B/8875B provides the least significant four bits. Since the largest number that can be obtained by multiplying two 4-bit numbers is 225 (15 × 15), the eight output pins (four from each package) are sufficient to produce this number. Both the multiplier and the multiplicand must be connected to the eight input pins of each device. These devices are pin compatible with the SN54284/74284, and SN54285/74285; but have the advantage that these circuits provide either standard totem-pole TTL or TRI-STATE outputs. A gated two-input strobe control is provided. When either one, or both, of the strobe inputs is raised to a high logic level the outputs are forced into the high-impedance state. Thus, multiple devices may be connected to a common bus line.

Features

- Pin compatible replacements for
  SN54284/74284 (DM7875A/8875A)
  SN54285/74285 (DM7875B/8875B)
- TRI-STATE outputs
- Typical propagation delay 35 ns

Connection Diagram

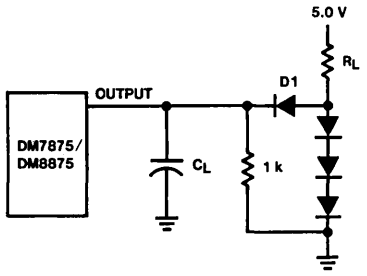
Dual-In-Line Package



TL/F/6592–1

Order Number DM7875AJ, DM7875BJ, DM8875AN or DM8875BN
See NS Package Number J16A or N16A

AC Test Circuit



TL/F/6592–2

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM78	−55°C to +125°C
DM88	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM7875A			DM8875A			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

DM78/8875A Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM78	−20		−70	mA
			DM88	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max			75	110	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded.

DM78/8875A Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				60	ns
t_{PZH}	Output Enable Time to High Level Output				30	ns
t_{PZL}	Output Enable Time to Low Level Output				30	ns
t_{PHZ}	Output Disable Time from High Level Output		30			ns
t_{PLZ}	Output Disable Time from Low Level Output		30			ns

Recommended Operating Conditions

Symbol	Parameter	DM7875B			DM8875B			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−2			−5.2	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

DM78/8875B Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max				40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max				−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM78	−20		−70	mA
			DM88	−20		−70	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			75	110	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

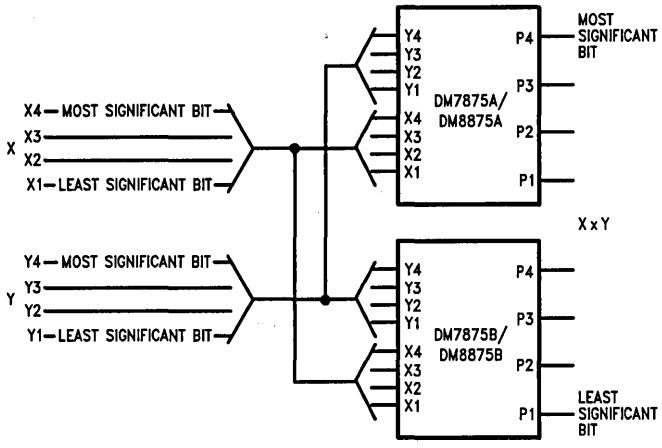
Note 3: I_{CC} is measured with all inputs grounded.

DM78/8875B Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

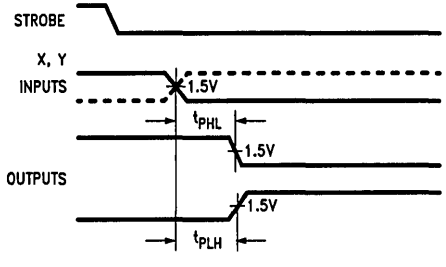
Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				60	ns
t_{PZH}	Output Enable Time to High Level Output				30	ns
t_{PZL}	Output Enable Time to Low Level Output				30	ns
t_{PHZ}	Output Disable Time from High Level Output		30			ns
t_{PLZ}	Output Disable Time from Low Level Output		30			ns

Typical Application



TL/F/6592-3

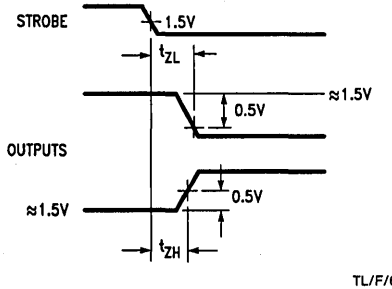
Switching Time Waveforms



TL/F/6592-4

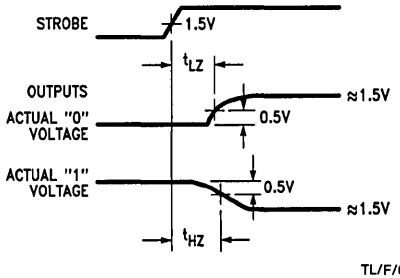
Input Pulses: $t_r = t_f \leq 10$ ns, f = 1 MHz

t_{ZL} & t_{ZH}



TL/F/6592-5

t_{LZ} & t_{HZ}



TL/F/6592-6

National Semiconductor Corporation

DM8898/DM8899 TRI-STATE® BCD to Binary/Binary to BCD Converters

General Description

These circuits are the TRI-STATE versions of the popular BCD to binary and binary to BCD converters, DM74184 and DM74185A respectively. They are derived from the 256-bit ROM, DM8598. Emitter connections are made to provide direct read out of converted codes at outputs Y8 through Y1, as shown in the truth tables. Both converters comprehend the fact that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter. Thus a 6-bit converter is produced in each case, and both devices are cascadable.

An overriding enable input is provided on each converter which, when taken high, inhibits the function, causing all outputs to go into the high-impedance state. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the 185A and all "don't care" conditions of the 184 are programmed high.

DM8898 BCD-TO-BINARY CONVERTERS

The 6-bit BCD-to-binary function of the DM8898 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.

b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

In addition to BCD-to-binary conversion, the DM8898 is programmed to generate BCD 9's complement or BCD 10's complement. In each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7 and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the function table when the devices are connected as shown.

DM8899A BINARY-TO-BCD CONVERTERS

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.

b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.

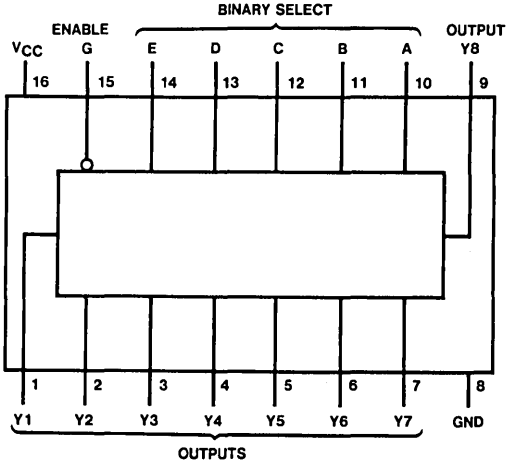
c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

Features

- TRI-STATE versions of DM74184, DM74185A
- Typical propagation delay 30 ns

Connection Diagram

Dual-In-Line Package



TL/F/6593–1

Order Number DM8898N or DM8899N
See NS Package Number N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range DM88	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM8898			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−5.2	mA
I_{OL}	Low Level Output Current			12	mA
T_A	Free Air Operating Temperature	0		70	°C

DM8898 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max		70	99	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

DM8898 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				50	ns
t_{PZH}	Output Enable Time to High Level Output				25	ns
t_{PZL}	Output Enable Time to Low Level Output				40	ns
t_{PHZ}	Output Disable Time from High Level Output		20			ns
t_{PLZ}	Output Disable Time from Low Level Output		36			ns

Recommended Operating Conditions

Symbol	Parameter	DM8899			Units
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{IH}	High Level Input Voltage	2			V
V_{IL}	Low Level Input Voltage			0.8	V
I_{OH}	High Level Output Current			−5.2	mA
I_{OL}	Low Level Output Current			12	mA
T_A	Free Air Operating Temperature	0		70	°C

DM8899 Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA			−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min	2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V			1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V			−1.6	mA
I_{OZH}	Off-State Output Current with High Level Output Voltage Applied	V_{CC} = Max, V_O = 2.4V V_{IH} = Min, V_{IL} = Max			40	μA
I_{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4V V_{IH} = Min, V_{IL} = Max			−40	μA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	−20		−70	mA
I_{CC}	Supply Current	V_{CC} = Max		70	99	mA

DM8899 Switching Characteristics

at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 400Ω				Units
		C_L = 5 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output				50	ns
t_{PHL}	Propagation Delay Time High to Low Level Output				50	ns
t_{PZH}	Output Enable Time to High Level Output				25	ns
t_{PZL}	Output Enable Time to Low Level Output				40	ns
t_{PHZ}	Output Disable Time from High Level Output		20			ns
t_{PLZ}	Output Disable Time from Low Level Output		36			ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Function Tables

BCD-to-Binary Converter

BCD Words		Inputs (See Note A)						Outputs (See Note B)				
		E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	L	L	L	L	L
2	3	L	L	L	L	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	L	L	L	H	L
6	7	L	L	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	L	L	H	L	L
10	11	L	H	L	L	L	L	L	L	H	L	H
12	13	L	H	L	L	H	L	L	L	H	H	L
14	15	L	H	L	H	L	L	L	L	H	H	H
16	17	L	H	L	H	H	L	L	H	L	L	L
18	19	L	H	H	L	L	L	L	H	L	L	H
20	21	H	L	L	L	L	L	L	H	L	H	L
22	23	H	L	L	L	H	L	L	H	L	H	H
24	25	H	L	L	H	L	L	L	H	H	L	L
26	27	H	L	L	H	H	L	L	H	H	L	H
28	29	H	L	H	L	L	L	L	H	H	H	L
30	31	H	H	L	L	L	L	L	H	H	H	H
32	33	H	H	L	L	H	L	H	L	L	L	L
34	35	H	H	L	H	L	L	H	L	L	L	H
36	37	H	H	L	H	H	L	H	L	L	H	L
38	39	H	H	H	L	L	L	H	L	L	H	H
Any		X	X	X	X	X	H	Z	Z	Z	Z	Z

BCD 9's or BCD 10's Complement Converter

BCD Word	Inputs (See Note C)						Outputs (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
Any	X	X	X	X	X	H	Z	Z	Z

H = High Level, L = Low Level, Z = High Impedance

Note A: Input conditions other than those shown produce highs at outputs Y1 through Y5.

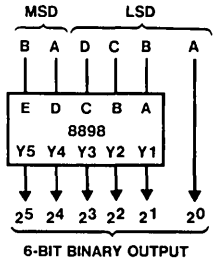
Note B: Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

Note C: Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.

Note D: Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

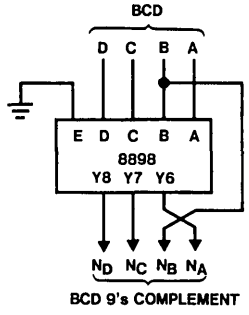
†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

6-Bit Converter



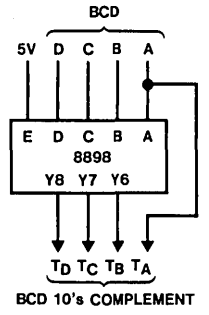
TL/F/6593–2

BCD 9's Complement Converter



TL/F/6593–3

BCD 10's Complement Converter



TL/F/6593–4

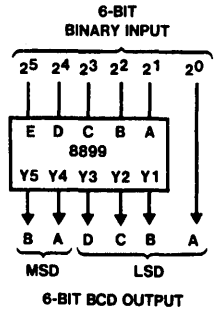
4

Function Tables (Continued)

Binary Words		Inputs						Outputs							
		Binary Select					Enable								
		E	D	C	B	A	G	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0	1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2	3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4	5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6	7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8	9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10	11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12	13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14	15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16	17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18	19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20	21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22	23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24	25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26	27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28	29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30	31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32	33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34	35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36	37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38	39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40	41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42	43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44	45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46	47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48	49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50	51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52	53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54	55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56	57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58	59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60	61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62	63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
All		X	X	X	X	X	H	Z	Z	Z	Z	Z	Z	Z	Z

H = High Level, L = Low Level, X = Don't Care, Z = High Impedance

6-Bit Converter



TL/F/6593–5

National Semiconductor Corporation

DM9002C Quad 2-Input NAND Gates

General Description

The DM9002C device is designed to be used in existing systems as replacements for Fairchild 9000-type circuits. The DM9002C circuit offers several significant advantages over 9000 type circuits, some of which are:

- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.
- Power-dissipation of DM9002C circuit is in most cases lower than that for the equivalent 9002 type.

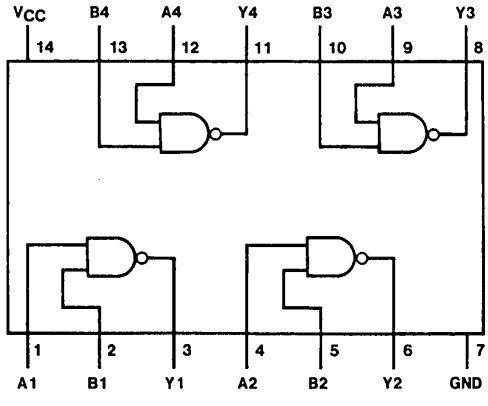
The DM9002C circuit is characterized for operation over the industrial temperature range of 0°C to 75°C.

For the new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Series 54/74 pin-for-pin equivalent is available for the following SSI type:

DM9000C Series	Equivalent Series 74
DM9002C	DM7400

Connection Diagrams

Dual-In-Line Package



TL/F/6594–1

Order Number DM9002CN
See NS Package Number N14A

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +75°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM9002C			Units
			Min	Nom	Max	
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	High Level Input Voltage	0°C	1.9			V
		25°C	1.8			
		75°C	1.6			
V_{IL}	Low Level Input Voltage				0.85	V
I_{OH}	High Level Output Current				−1.2	mA
I_{OL}	Low Level Output Current				50	mA
T_A	Free Air Operating Temperature		0		75	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Max, I_{OL} = 16 mA V_{IH} = Min				0.45	V
		I_{OL} = 14.1 mA, V_{CC} = Min				0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V Other Input at 0V				60	μA
I_{IL}	Low Level Input Current	V_I = 4.5V	V_{CC} = 5.25V			−1.6	mA
			V_{CC} = 4.75V			−1.41	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)		−18		−55	mA
I_{CCH}	Supply Current with Outputs High	V_{CC} = 5V				1.7	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = 5V				6.1	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω	3		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output		3		15	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

National Semiconductor Corporation

DM9024/DM8024 Dual J-K Flip-Flops with Preset and Clear

General Description

The DM9024 series device is designed to be used in existing systems as replacements for Fairchild 9000-type circuits. These DM9024 circuits offer several significant advantages over 9024 type circuits, some of which are:

- Input clamp diodes
- Output short-circuit current specified to guarantee the high-level impedance.

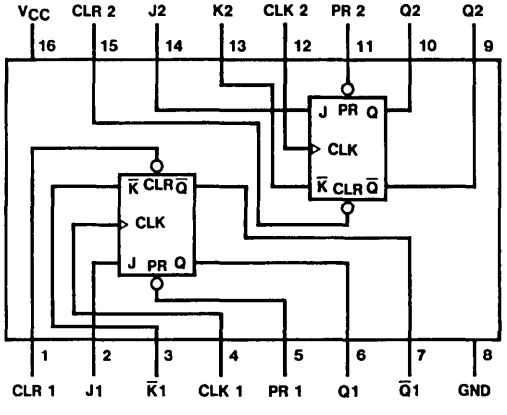
The DM9024 circuit is characterized for operation over the industrial temperature range of 0°C to 75°C.

For the new designs, the 54/74 families of TTL circuits offer the industry's broadest choice of high-performance digital circuits. Series 54/74 pin-for-pin equivalents are available for the following SSI types:

DM9000 Series	Equivalent Series 74
DM9024	DM74109

Connection Diagram

Dual-In-Line Package



TL/F/6599–1

Order Number DM9024J or DM8024N
See NS Package Number J16A or N16A

Function Table

24

Inputs					Outputs	
Preset	Clear	Clock	J	$\overline{K}$	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

H = High Level (Steady State), L = Low Level (Steady State).

X = Don't Care

↑ = Transition from low to high level

Q_0 = The level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.

*This configuration is nonstable. That is, it will not persist when preset and clear inputs return to their inactive (high) level.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM90	−55°C to +125°C
DM80	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM9024			DM8024			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5.0	5.5	4.75	5.0	5.25	V
V_{IH}	High Level Input Voltage	T_A = Min	2.0			1.9			V
		T_A = 25°C	1.7			1.8			
		T_A = Max	1.4			1.6			
V_{IL}	Low Level Input Voltage				0.9			0.85	V
I_{OH}	High Level Output Current				−1.2			−1.2	mA
I_{OL}	Low Level Output Current				12.4			14.1	mA
f_{CLK}	Clock Frequency (Note 2)		0	40	30	0	40	30	MHz
t_W	Pulse Width (Note 2)	Clock High	20			20			ns
		Clock Low	20			20			
		PR, CLR Low	20			20			
t_{SU}	Setup Time (Notes 1 & 2)		15↑			15↑			ns
T_H	Hold Time (Notes 1 & 2)		10↑			10↑			ns
T_A	Free Air Operating Temperature		−55		125	0		75	°C

Note 1: The symbol (↑) indicates rising edge of clock pulse is used for reference.

Note 2: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM90			0.4	V
			DM80			0.45	
		I_{OL} = 16 mA V_{CC} = Max	DM90			0.4	
			DM80			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 4.5V Other Inputs at Ground	J, K			60	μA
			Clock			120	
			Preset			120	
			Clear			240	

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted) (Continued)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.40V (DM90), V_I = 0.45V (DM80), Other Inputs at 4.5V	J, K			−1.6	mA
			Clock			−3.2	
			Preset			−3.2	
			Clear			−4.8	
		V_{CC} = Min, V_I = 0.40V (DM90), Other Inputs at 4.5V	J, K			−1.24	
			Clock			−2.48	
			Preset			−2.48	
			Clear			−3.72	
		V_{CC} = Min, V_I = 0.40V (DM80), Other Inputs at 4.5V	J, K			−1.41	
			Clock			−2.82	
			Preset			−2.82	
			Clear			−4.23	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM90	−30		−85	mA
			DM80	−30		−85	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				28	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 3: I_{CC} is measured with all inputs open, first with PRESET at 4.5V and all other inputs grounded, then with CLEAR at 4.5V and all other inputs grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		29	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q, $\overline{Q}$		18	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q, $\overline{Q}$		28	ns

National Semiconductor Corporation

DM9300/DM8300 4-Bit Parallel-Access Shift Registers

General Description

These 4-bit registers feature parallel inputs, parallel outputs, $J\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation: parallel (broadside) load and shift (in direction Q_A toward Q_D).

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops, and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the $J\overline{K}$ inputs. These inputs permit the first stage to perform as a $J\overline{K}$, D or T-type flip-flop as shown in the function table.

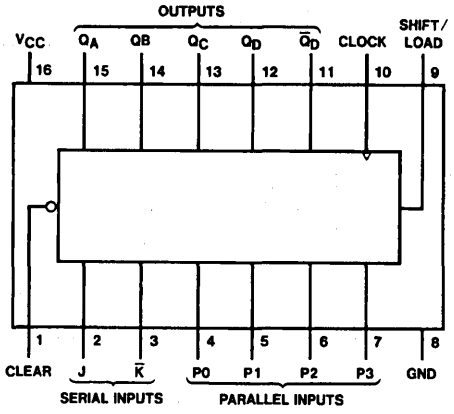
These shift registers are fully compatible with most other TTL and DTL families. All inputs, including the clock, are buffered to lower the drive requirements to one normalized Series 54/74 load.

Features

- Direct replacement for Fairchild 9300
- Fully buffered inputs
- Direct overriding clear
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Positive edge-triggered clocking
- J and $\overline{K}$ inputs to first stage
- Typical shift frequency—39 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6600–1

Order Number DM9300J or DM8300N
See NS Package Number J16A or N16A

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel				Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
			J	$\overline{K}$	P0	P1	P2	P3					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Bn}	$\overline{Q}_{Cn}$

H = High Level (Steady State)

L = Low Level (Steady State)

X = Don't Care

↑ = Transition from low-to-high level

a, b, c, d, = The level of steady state input at P0, P1, P2, or P3 respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = The level of Q_A, Q_B, Q_C, or Q_D, respectively before the indicated steady state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn} = The level of Q_A, Q_B, Q_C, respectively, before the most recent ↑ transition of the clock.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM9300			DM8300			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)		0		30	0		30	MHz
t_W	Pulse Width (Note 5)	Clock	16	11		16	11		ns
		Clear	30	15		30	15		
t_{SU}	Setup Time (Note 5)	S/L	30	13		30	13		ns
		Data	20	13		20	13		
		Clear	30	13		30	13		
t_H	Data Hold Time (Note 5)		0	−11		0	−11		ns
t_{REL}	S/L Release Time (Notes 1 and 5)		10			10			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM93	−18		−55	mA
			DM83	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 4)	DM93			86	mA
			DM83			92	

Note 1: RELEASE TIME: $t_{RELEASE}$ is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) *not* to respond.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

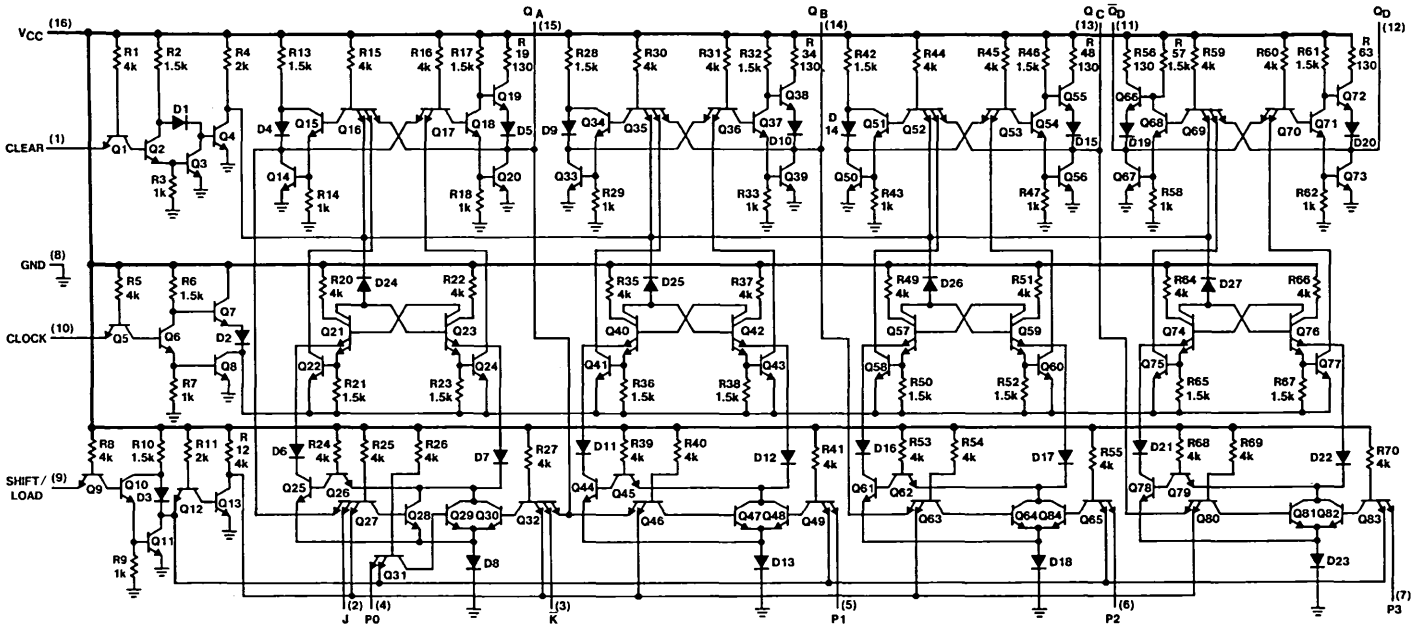
Note 4: With all outputs open, SHIFT/LOAD grounded, and 4.5V applied to J, K, and data inputs, I_{CC} is measured by applying momentary ground, then 4.5V to CLEAR, and then to CLOCK.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		30		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		22	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		26	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output		30	ns

DM93/8300



TL/F/6600-2

National Semiconductor Corporation

DM9301/DM8301 1 of 10 Decoders

General Description

These BCD-to-decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain "OFF" for all invalid input conditions.

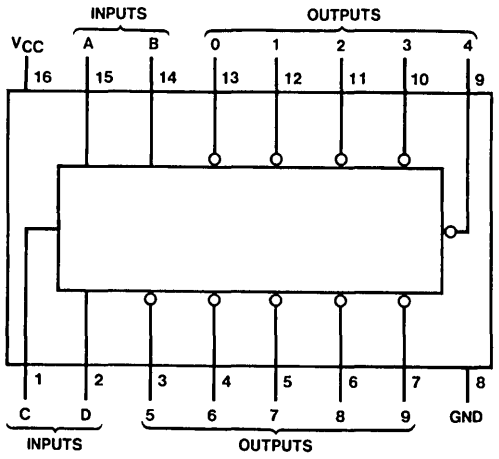
These circuits provide familiar TTL inputs and outputs which are compatible for use with other TTL and DTL circuits. DC noise margins are typically 1V and power dissipation is typically 125 mW. The diode-clamped, buffered inputs represent only one normalized Series 54/74 load.

Features

- Direct replacement for Fairchild 9301 and Signetics 8252
- Diode-clamped inputs
- All outputs are high for invalid BCD input conditions
- Typical power dissipation 125 mW
- Typical propagation delay 20 ns

Connection Diagram

Dual-In-Line Package



TL/F/6601–1

Order Number DM9301J or DM8301N
See NS Package Number J16A or N16A

Function Table

No.	BCD Inputs				Decimal Outputs									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
I	H	L	H	L	H	H	H	H	H	H	H	H	H	H
N	H	L	H	H	H	H	H	H	H	H	H	H	H	H
V	H	H	L	L	H	H	H	H	H	H	H	H	H	H
A	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	L	H	H	H	H	H	H	H	H	H	H
I	H	H	H	H	H	H	H	H	H	H	H	H	H	H
D														

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to 70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM9301			DM8301			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−20		−55	mA
			DM83	−20		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			25	41	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	C_L = 15 pF R_L = 400Ω		30	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			30	ns

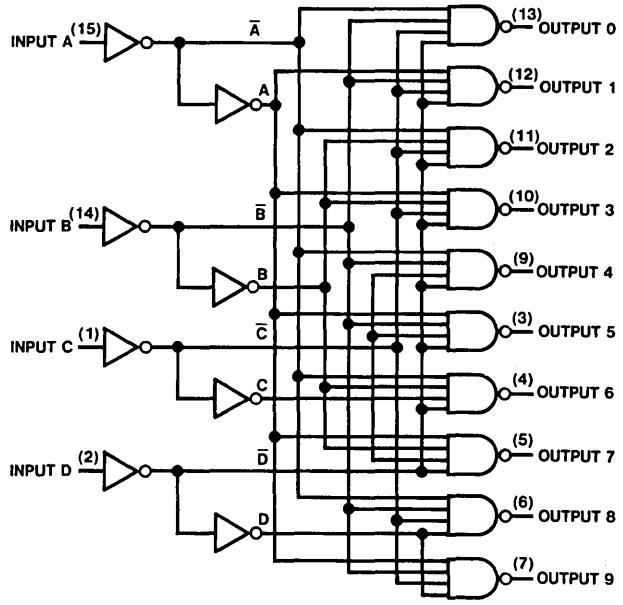
Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with the outputs open and all inputs grounded.

Logic Diagram

DM93/8301



TL/F/6601–2

National Semiconductor Corporation

DM9309/DM8309 Dual 4-Bit Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection.

The DM9309/8309 contains two separate 4-bit multiplexers with complementary Y and $\overline{Y}$ outputs; however, the two sections have common address select inputs.

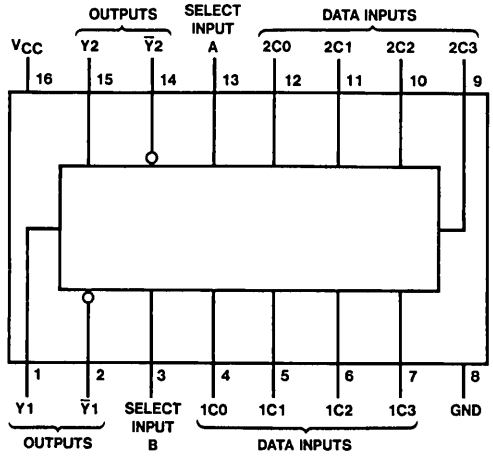
Features

DM9309/8309

- Direct replacement for Fairchild 9309
- Complementary outputs
- Dual one-of-four data selectors

Connection Diagram

Dual-In-Line Package



TL/F/6602–1

Order Number DM9309J or DM8309N
See NS Package Number J16A or N16A

Function Table

Inputs						Outputs	
Select		Data				Y	$\overline{Y}$
B	A	C0	C1	C2	C3		
L	L	L	X	X	X	L	H
L	L	H	X	X	X	H	L
L	H	X	L	X	X	L	H
L	H	X	H	X	X	H	L
H	L	X	X	L	X	L	H
H	L	X	X	H	X	H	L
H	H	X	X	X	L	L	H
H	H	X	X	X	H	H	L

Select inputs A and B are common to both sections.

H = High Level, L = Low Level, X = Don't Care.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM9309			DM8309			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−30		−85	mA
			DM83	−30		−85	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			27	44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

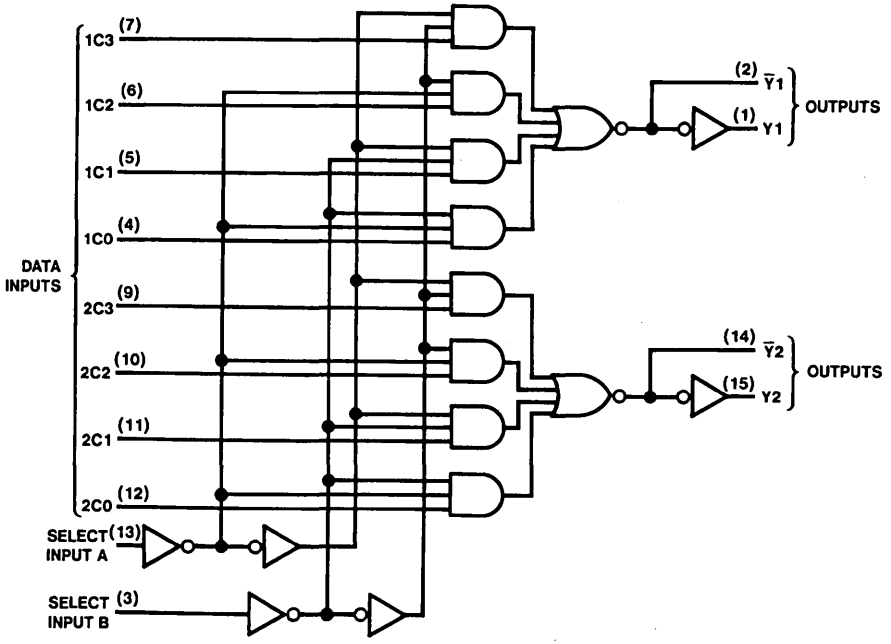
Note 3: I_{CC} is measured with the outputs open and all inputs at 4.5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		36	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to $\overline{Y}$		24	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to $\overline{Y}$		29	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		34	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to $\overline{Y}$		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to $\overline{Y}$		13	ns

Logic Diagram

DM93/8309



TL/F/6602–2

National Semiconductor Corporation

DM9310/DM8310 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM9310/DM8310 are decade counters. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

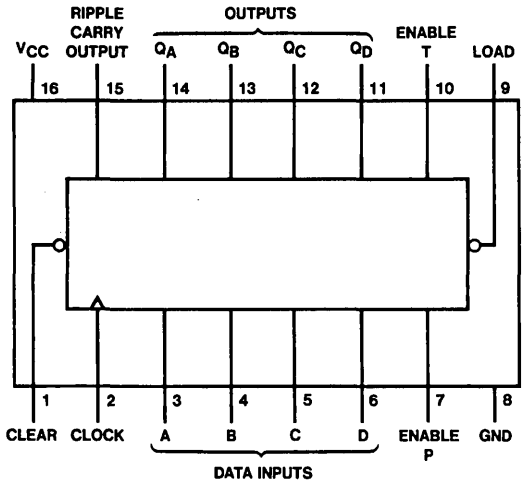
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

FEATURES

- Direct replacement for Fairchild 9310
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters 9310—54160A/74160A (decade)

Connection Diagram

Dual-In-Line Package



TL/F/6603–1

Order Number DM9310J or DM8310N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM9310			DM8310			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 5)		0		25	0		25	MHz
t_W	Pulse Width (Note 5)	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 5)	Data	20			20			ns
		Enable P	20			20			
		Load	25			25			
		Clear	20			20			
t_H	Any Hold Time (Notes 1 & 5)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The minimum HOLD time is as specified or as long as the CLOCK input takes to rise from 0.8V to 2V, whichever is longer.

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	CLK, EN T			80	μA
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	CLK, EN T			−3.2	mA
			Other			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−20		−57	mA
			DM83	−18		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 3)	DM93		59	85	mA
			DM83		59	94	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 4)	DM93		63	91	mA
			DM83		63	101	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CCH} is measured with the LOAD input high, then again with the LOAD input low, with all other inputs high and all outputs open.

Note 4: I_{CCL} is measured with the CLOCK input high, then again with the CLOCK input low, with all other inputs low and all outputs open.

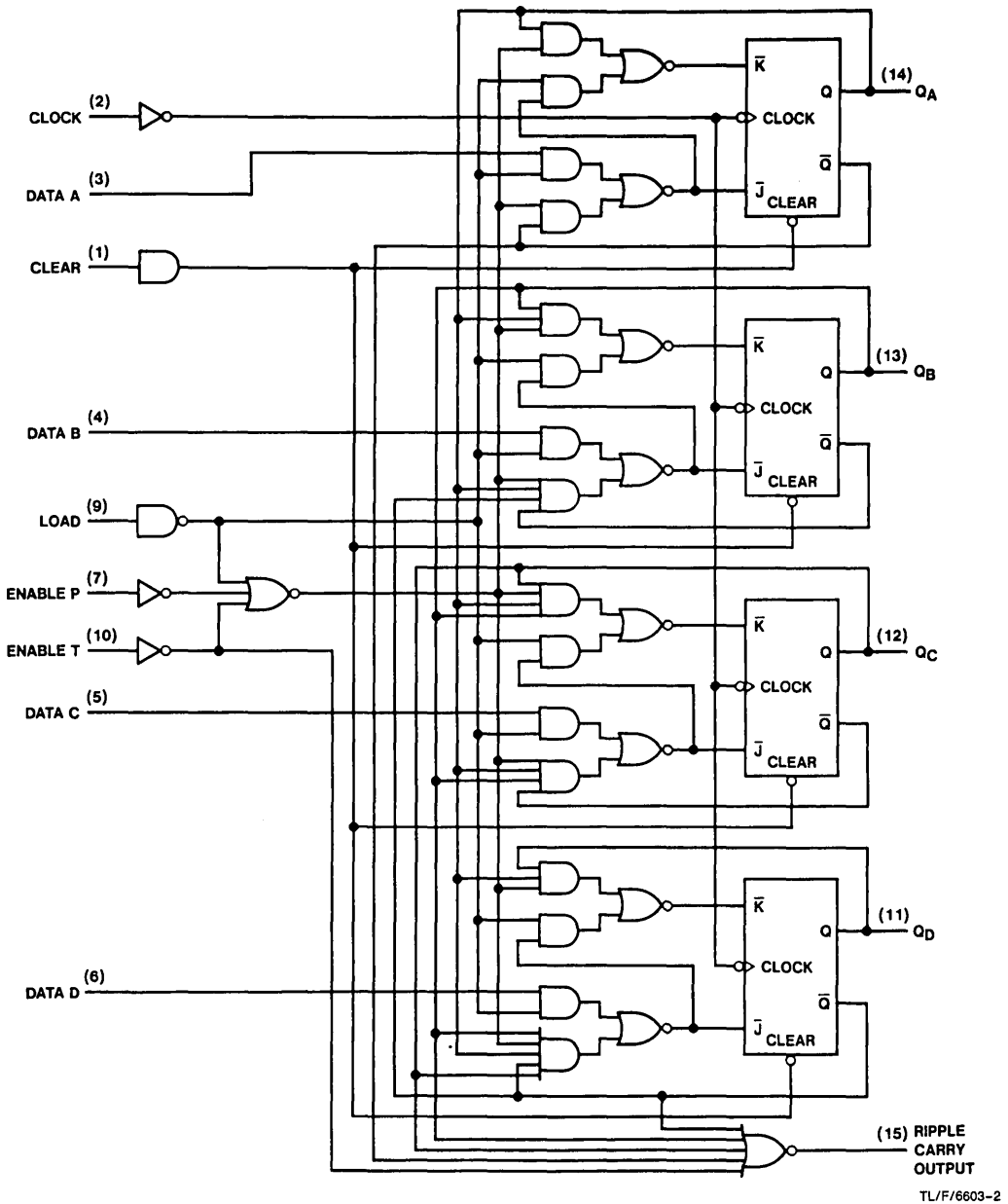
Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Ripple Carry		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Ripple Carry		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable T to Ripple Carry		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable T to Ripple Carry		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		36	ns

Logic Diagram

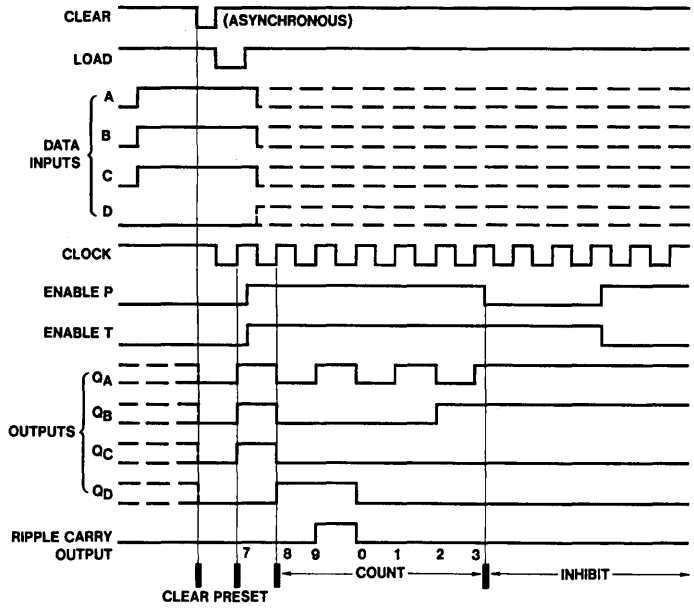
DM93/8310



TL/F/6603–2

Timing Diagram

9310/8310 Synchronous Decade Counters
Typical Clear, Preset, Count and Inhibit Sequence



TL/F/6603–3

Sequence:

(1) Clear outputs to zero.

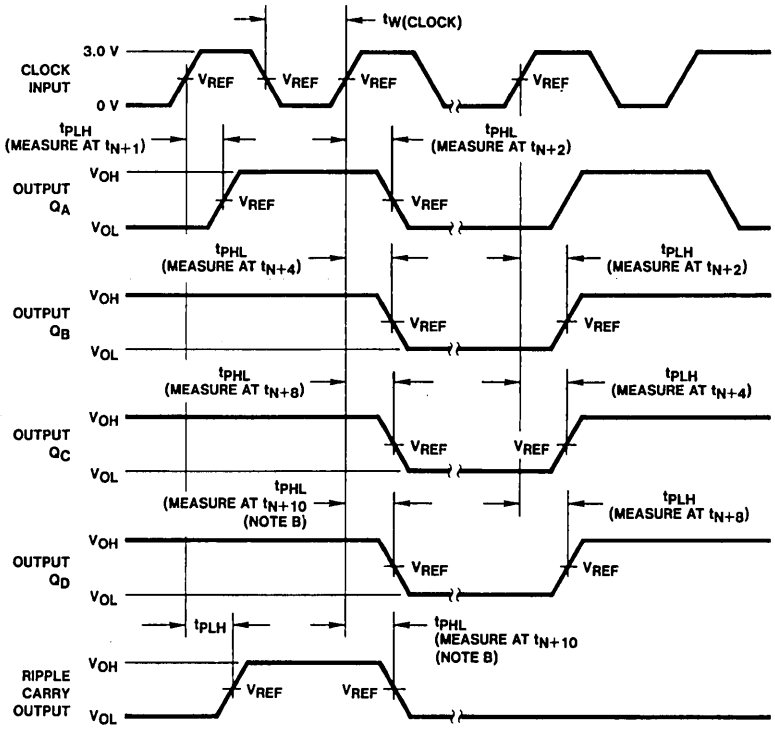
(2) Preset to BCD seven.

(3) Count to eight, nine, zero, one, two, and three.

(4) Inhibit

Parameter Measurement Information

Switching Time Waveforms



TL/F/6603–4

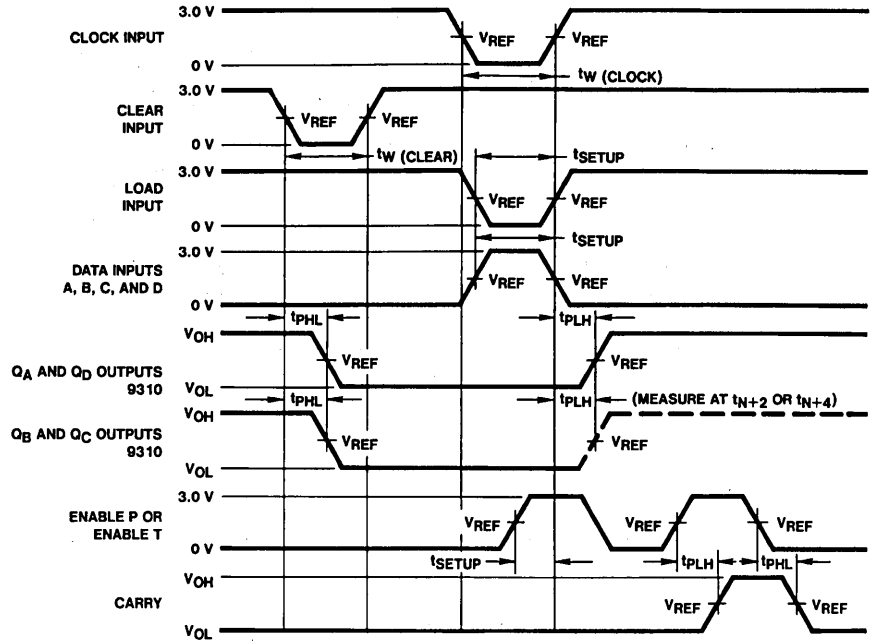
Note A: The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+10} for 9310/8310, where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5V$.

Parameter Measurement Information (Continued)

Switching Time Waveforms



TL/F/6603–5

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note B: Enable P and enable T setup times are measured at t_{n+10} for 8310/9310.

Note C: $V_{REF} = 1.5V$.

National Semiconductor Corporation

DM9311/DM8311 4-Line to 16-Line Decoders/Demultiplexers

General Description

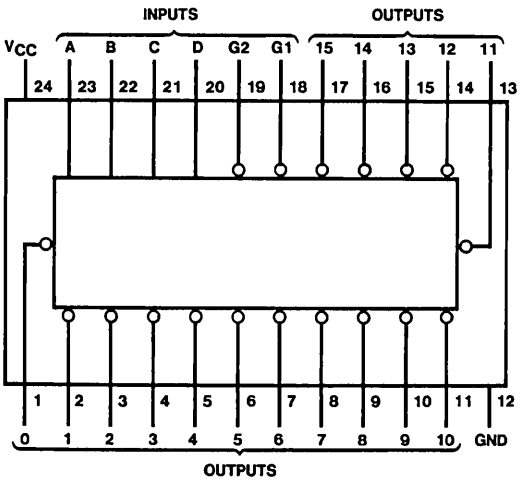
Each of these 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high. These demultiplexers are ideally suited for implementing high-performance memory decoders. All inputs are buffered and input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design.

Features

- Direct replacement for Fairchild 9311
- Pin for pin with popular DM54154/74154
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical propagation delay 19 ns
- Typical power dissipation 170 mW

Connection Diagram

Dual-In-Line Package



TL/F/6604–1

Order Number DM9311J or DM8311N
See NS Package Number J24A or N24A

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM9311			DM8311			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.25	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−20		−55	mA
			DM83	−18		−57	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM93		34	49	mA
			DM83		34	56	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all inputs grounded and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		30	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		27	ns

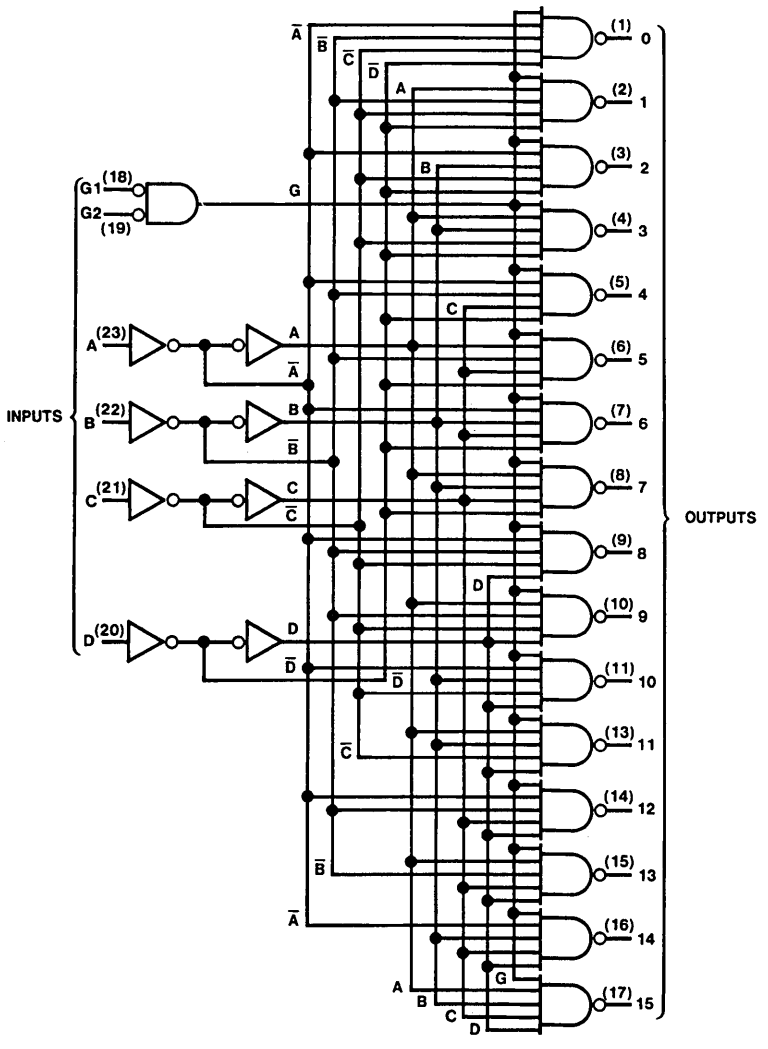
Function Table

Inputs						Outputs														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = High Level, L = Low Level, X = Don't Care.

Logic Diagram

DM93/8311



TL/F/6604–2

National Semiconductor Corporation

DM9312/DM8312 One of Eight Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverter/drivers to supply full complementary, on-chip, binary decoded data selection.

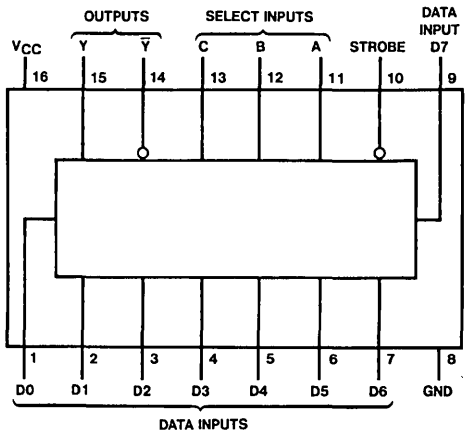
The DM9312/8312 is a single 8-bit multiplexer with complementary outputs and a strobe control. When the strobe is low, the function is enabled. When a high logic level is applied to the strobe, the output is forced to the logic zero state regardless of the logic level of the data inputs.

Features

- Direct replacement for Fairchild 9312
- Selects one-of-eight data sources
- Performs parallel to serial conversion
- Strobe controlled outputs
- Complementary outputs

Connection Diagram

Dual-In-Line Package



TL/F/6605–1

Order Number DM9312J or DM8312N
See NS Package Number J16A or N16A

Function Table

DM93/8312

Inputs				Outputs	
Select			Strobe	Y	$\overline{Y}$
C	B	A	G		
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care.

D0, D1 . . . D7 = The level of the respective D input.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM9312			DM8312			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−30		−85	mA
			DM83	−30		−85	
I_{CC}	Supply Current	V_{CC} = Max, (Note 3)			27	44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

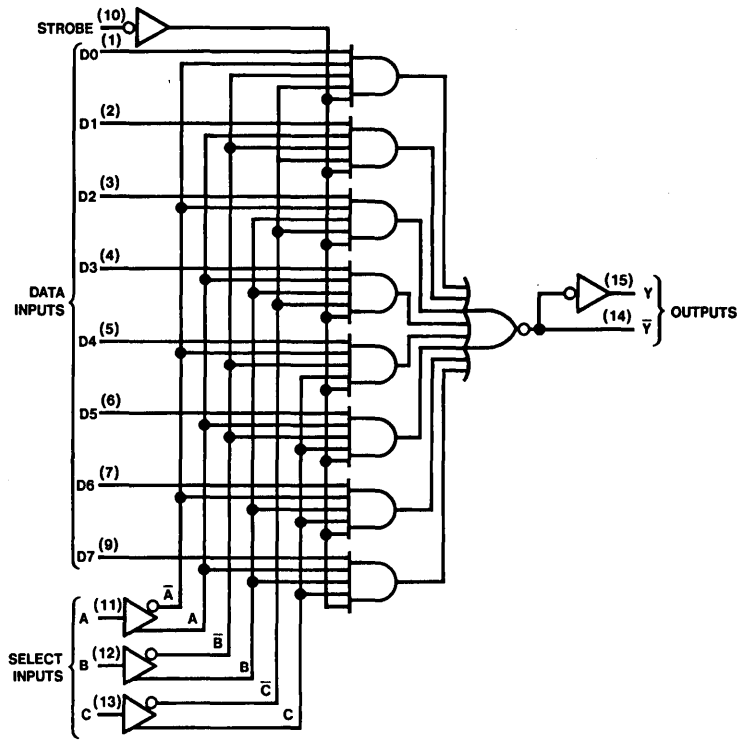
Note 3: I_{CC} is measured with the STROBE and DATA SELECT inputs 4.5V and all other inputs and outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Y		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Y		35	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to $\overline{Y}$		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to $\overline{Y}$		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Y		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Y		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to $\overline{Y}$		13	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to $\overline{Y}$		13	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Y		33	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Y		32	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to $\overline{Y}$		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to $\overline{Y}$		21	ns

Logic Diagram

DM93/8312



TL/F/6605–2

National Semiconductor Corporation

DM9316/DM8316 Synchronous 4-Bit Counters

General Description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting designs. The DM9316/DM8316 is a 4-bit binary counter. The carry output is decoded by means of a NOR gate, thus preventing spikes during the normal counting mode of operation. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enables inputs and internal gating. This mode of operating eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable input. Low-to-high transitions at the load input are perfectly acceptable regardless of the logic levels on the clock or enable inputs. The clear function is asynchronous and a low level at the clear input sets of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs.

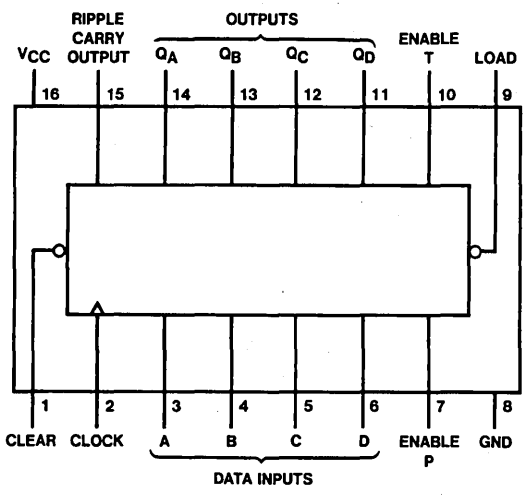
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed-forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low level transitions at the enable P or T inputs may occur regardless of the logic level in the clock.

Features

- Direct replacement for Fairchild 9316
- Internal look-ahead for fast counting
- Carry output for n-bit cascading
- Synchronous counting
- Load control line
- Diode-clamped inputs
- Typical clock frequency 35 MHz
- Pin-for-pin replacements popular 54/74 counters 9316—5416A/7416A (binary)

Connection Diagram

Dual-In-Line Package



TL/F/6606–1

Order Number DM9316J or DM8316N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM9316			DM8316			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency (Note 6)		0		25	0		25	MHz
t_W	Pulse Width (Note 6)	Clock	25			25			ns
		Clear	20			20			
t_{SU}	Setup Time (Note 6)	Data	20			20			ns
		Enable P	20			20			
		Load	25			25			
		Clear	20			20			
t_H	Any Hold Time (Notes 1 & 6)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4 V	Clock			80	µA
			Enable $\overline{T}$			80	
			Other			40	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V	Clock			−3.2	µA
			Enable $\overline{T}$			−3.2	
			Other			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM93	−20		−57	mA
			DM83	−18		−57	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max (Note 4)	DM93		59	85	mA
			DM84		59	94	
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max (Note 5)	DM93		63	91	mA
			DM83		63	101	

Note 1: The minimum HOLD time is as specified or as long as the CLOCK input takes to rise from 0.8V to 2V, whichever is longer.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time.

Note 4: I_{CCH} is measured with the LOAD input high, then again with the LOAD input low, with all other inputs high and all outputs open.

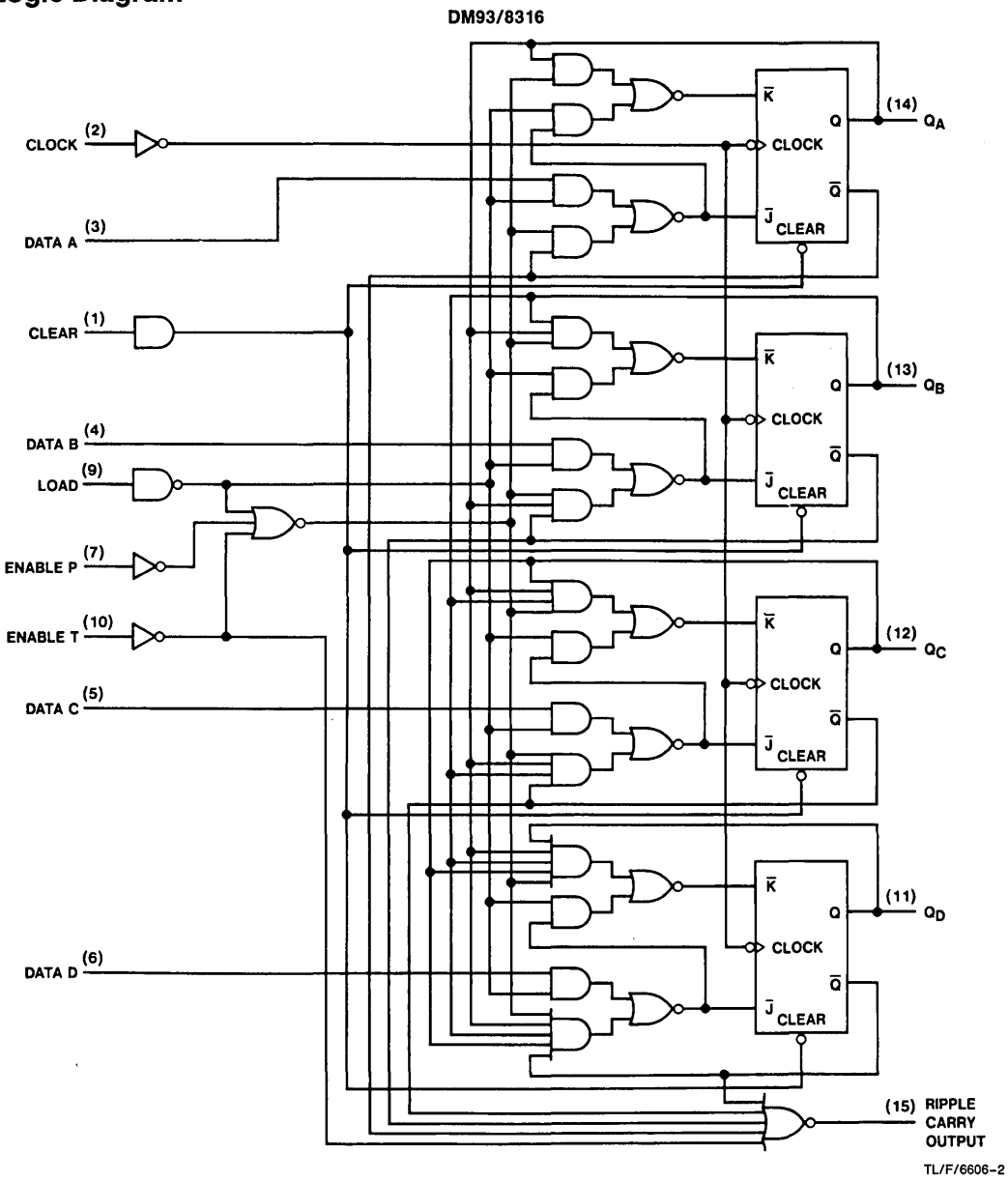
Note 5: I_{CCL} is measured with the CLOCK input high, then again with the CLOCK input low, with all other inputs low and all outputs open.

Note 6: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

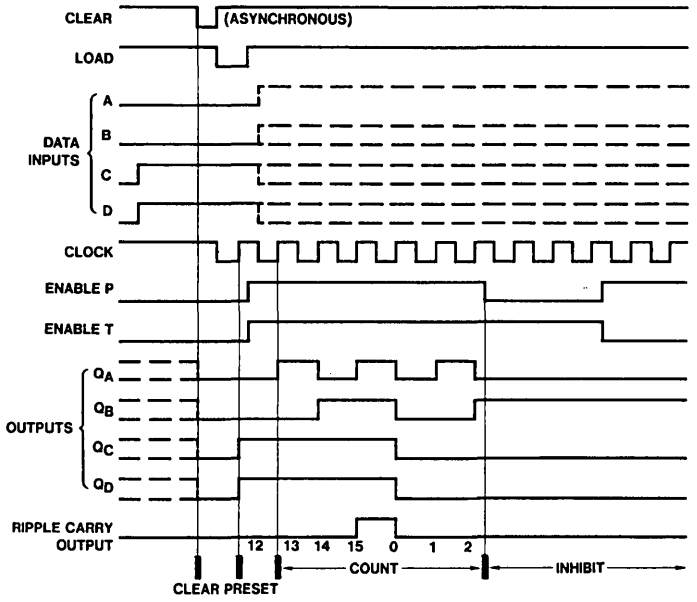
Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to RC		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to RC		24	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		23	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q		21	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q		25	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	ENT to RC		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	ENT to RC		16	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		36	ns

Logic Diagram



Timing Diagram

9316/8316 Synchronous Binary Counters
Typical Clear, Preset, Count and Inhibit Sequences



TL/F/6606–3

Sequence:

(1) Clear outputs to zero.

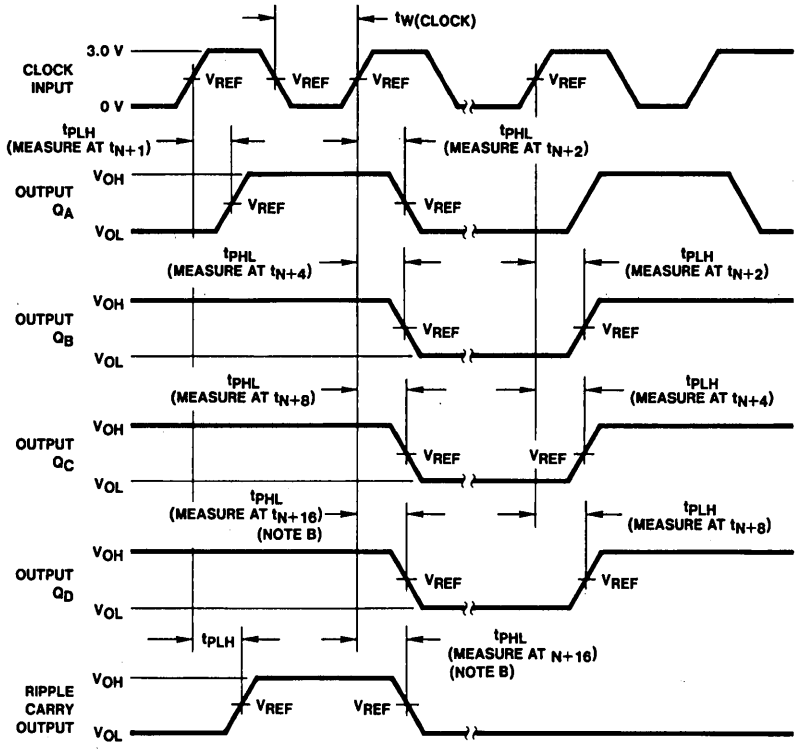
(2) Preset to binary twelve.

(3) Count to thirteen, fourteen, fifteen, zero, one, and two.

(4) Inhibit

Parameter Measurement Information

Switching Time Waveforms



TL/F/6606–4

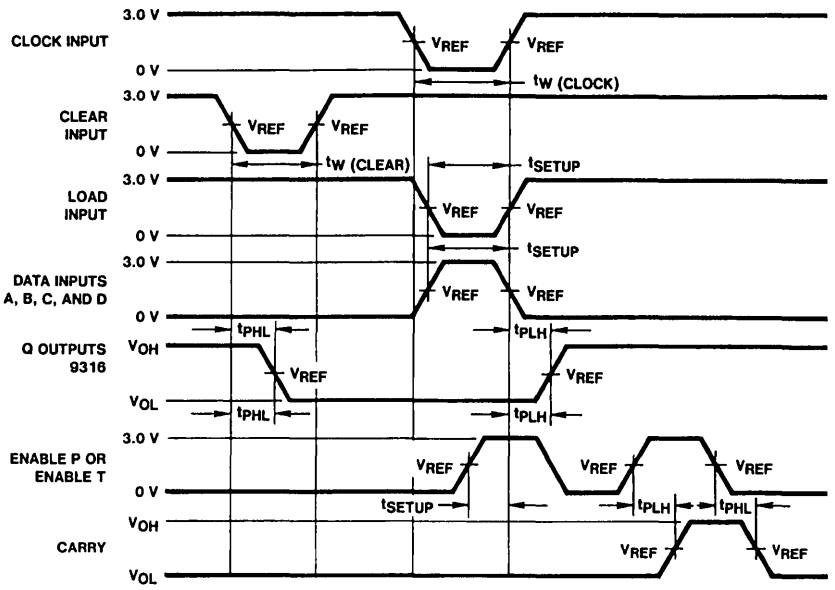
Note A: The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns. Vary PRR to measure f_{MAX}.

Note B: Outputs Q_D and carry are tested at t_{n+16} for 9316/8316, where t_n is the bit time when all outputs are low.

Note C: $V_{REF} = 1.5V$.

Parameter Measurement Information (Continued)

Switching Time Waveforms



TL/F/6606–5

Note A: The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, $Z_{OUT} \approx 50\Omega$, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Note B: Enable P and Enable T setup times are measured at t_{n+16} for 8316/9316.

Note C: $V_{REF} = 1.5V$.

National Semiconductor Corporation

DM9318/DM8318 Priority Encoders

General Description

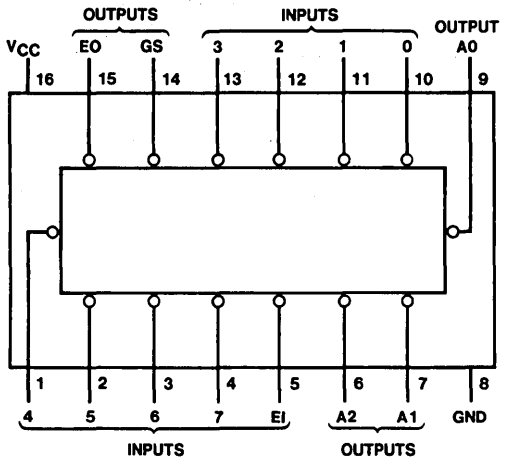
These TTL encoders feature priority decoding of the input data to ensure that only the highest-order data line is encoded. All inputs are buffered to represent one normalized Series 54/74 load. The DM9318 and DM8318 encode eight data lines to three-line (4-2-1) binary (octal). Cascading circuitry (enable input E1 and enable output E0) has been provided to allow octal expansion without the need for external circuitry. For all types, data inputs and outputs are active at the low logic level.

Features

- Direct replacement for Fairchild 9318
- Pin for pin with popular DM54148/74148
- Encodes 8 data lines to 3-line binary (octal)
- Applications include:
  - N-bit encoding
  - Code converters and generators
- Typical data delay 10 ns
- Typical power dissipation 190 mW

Connection Diagram

Dual-In-Line Package



TL/F/6607–1

Order Number DM9318J or DM8318N
See NS Package Number J16A or N16A

Function Table

Inputs									Outputs				
E1	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H

H = High Logic Level, L = Low Logic Level, X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM9318			DM8318			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	0 Input			40	μA
			Others			80	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	0 Input			−1.6	mA
			Others			−3.2	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−35		−85	mA
			DM83	−35		−85	
I_{CC1}	Supply Current Condition 1	V_{CC} = Max, (Note 3)			35	55	mA
I_{CC2}	Supply Current Condition 2	V_{CC} = Max, (Note 4)			40	60	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC1} is measured with all inputs and outputs open.

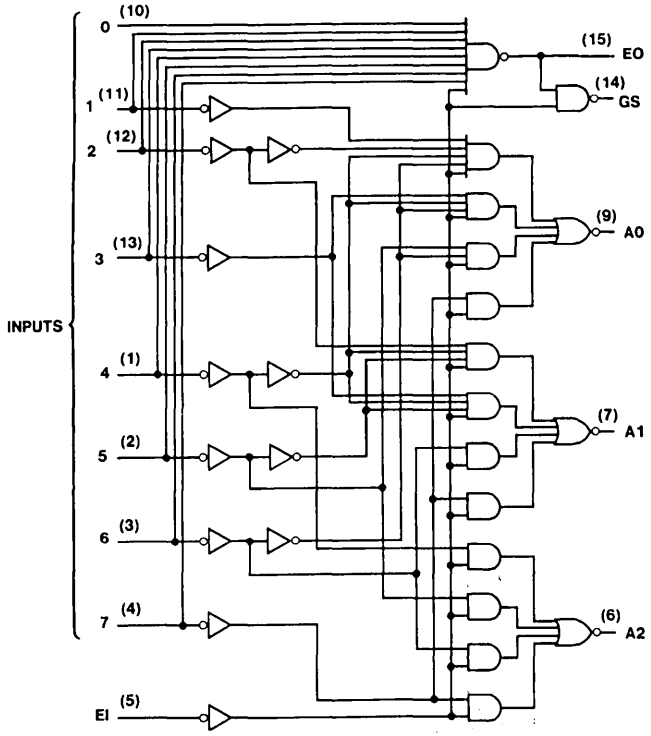
Note 4: I_{CC2} is measured with inputs 7 and EI grounded and outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to ABCD In Phase		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to ABCD In Phase		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to ABCD Out of Phase		19	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to ABCD Out of Phase		19	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to E0 Out of Phase		9	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to E0 Out of Phase		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	0 thru 7 to GS In Phase		27	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	0 thru 7 to GS In Phase		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	EI to A0, 1, 2 In Phase		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	EI to A0, 1, 2 In Phase		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	EI to GS In Phase		12	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	EI to GS In Phase		15	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	EI to E0 In Phase		15	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	EI to E0 In Phase		26	ns

Logic Diagram

DM93/8318



TL/F/6607–2

National Semiconductor Corporation

DM9322/DM8322 Quad 2-Line to 1-Line Data Selectors/Multiplexers

General Description

These data selectors/multiplexers contain inverters and drivers to supply full on-chip data selection to the four output gates. A separate strobe input is provided. A 4-bit word is selected from one of two sources and is routed to the four outputs. True data is presented at the outputs.

Applications

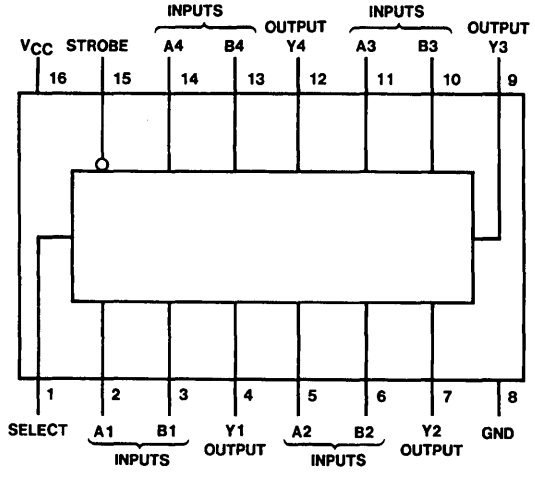
- Expand any data input point
- Multiplex dual-data buses
- Generate four functions of two variables (one variable is common)
- Source programmable counters

Features

- Direct replacement for Fairchild 9322
- Pin-for-pin with popular DM54157/74157
- Buffered inputs and outputs

Connection Diagram

Dual-In-Line Package



TL/F/6608–1

Order Number DM9322J or DM8322N
See NS Package Number J16A or N16A

Function Table

Inputs				Output
Strobe	Select	A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = High Level, L = Low Level, X = Don't Care.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM9322			DM8322			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.8			0.8	V
I_{OH}	High Level Output Current			−0.8			−0.8	mA
I_{OL}	Low Level Output Current			16			16	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM93	−20		−55	mA
			DM83	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			30	48	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

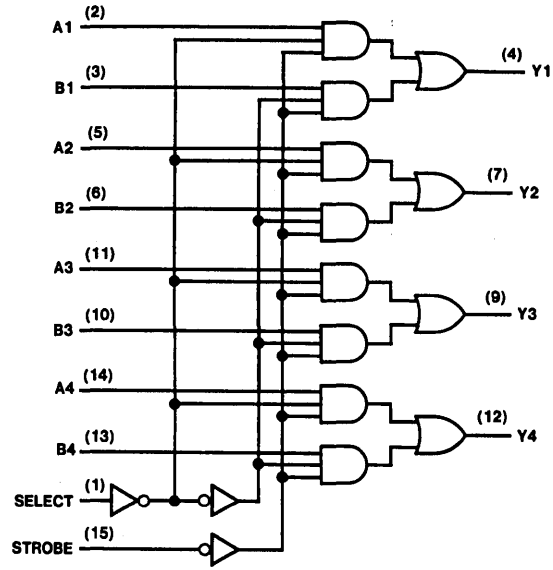
Note 3: I_{CC} is measured with 4.5V applied to all inputs and all outputs open.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output		14	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output		14	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Strobe to Output		20	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Strobe to Output		21	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Select to Output		23	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Select to Output		27	ns

Logic Diagram

DM93/8322



TL/F/6608–2

National Semiconductor Corporation

DM9334/DM8334 8-Bit Addressable Latches

General Description

The DM9334/DM8334 is a high speed 8-bit Addressable Latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and being a one-of-eight decoder and demultiplexer with active level high outputs. The device also incorporates an active level low common clear for resetting all latches, as well as an active level low enable.

The DM9334/DM8334 has four modes of operation which are shown in the mode selection table. In the addressable latch mode, data on the data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states. In the memory mode, all latches remain in their previous state and are unaffected by the data or address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other inputs in the low state. In the clear mode all outputs are low and unaffected by the address and data inputs.

When operating the device as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode.

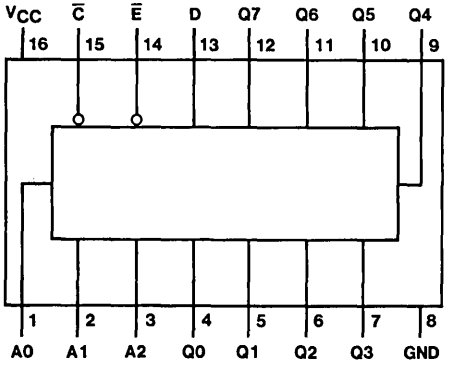
The function tables summarize the operation of the product.

Features

- Direct replacement for Fairchild 9334
- Common clear
- Easily expandable
- Random (addressable) data entry
- Serial to parallel capability
- 8 bits of storage/output of each bit available
- Active high demultiplexing/decoding capability

Connection Diagram

Dual-In-Line Package



TL/F/6609–1

Order Number DM9334J or DM8334N
See NS Package Number J16A or N16N

4

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM93	−55°C to +125°C
DM83	0° to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM9334			DM8334			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
t_W	ENABLE Pulse Width (Fig. 1) (Note 4)		19	13		19	13		ns
t_{SU}	Setup Time (Note 4)	Data 1 (Fig. 4)	20	13		20	13		ns
		Data 0 (Fig. 4)	20	14		20	14		
		Address (Fig. 6) (Note 1)	10	5		10	5		
t_H	Hold Time (Note 4)	Data 1 (Fig. 4)	0	−10		0	−10		ns
		Data 0 (Fig. 4)	0	−13		0	−13		
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.6		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max			0.2	0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	$\overline{E}$ Input			60	μA
			Others			40	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.4V	$\overline{E}$ Input			−2.4	mA
			Others			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM93	−30		−100	mA
			DM83	−30		−100	
I_{CC}	Supply Current	V_{CC} = Max			56	86	mA

Note 1: The ADDRESS setup time is the time before the negative ENABLE transition that the ADDRESS must be stable so that the correct latch is addressed without affecting the other latches.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 400Ω, C_L = 15 pF		Units
			Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	Enable to Output, Fig. 1		28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Enable to Output, Fig. 1		27	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Data to Output, Fig. 2		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Data to Output, Fig. 2		28	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Address to Output, Fig. 3		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Address to Output, Fig. 3		35	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output, Fig. 5		31	ns

Function Tables

$\overline{E}$	$\overline{C}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active High Eight Channel Demultiplexer
H	L	Clear

Inputs						Present Output States								Mode
$\overline{C}$	$\overline{E}$	D	A0	A1	A2	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7	
L	H	X	X	X	X	L	L	L	L	L	L	L	L	Clear
L	L	L	L	L	L	L	L	L	L	L	L	L	L	
L	L	H	L	L	L	H	L	L	L	L	L	L	L	
L	L	L	H	L	L	L	L	L	L	L	L	L	L	
L	L	H	H	L	L	L	H	L	L	L	L	L	L	
•	•	•		•					•					Demultiplex
•	•	•		•					•					
•	•	•		•					•					
L	L	H	H	H	H	L	L	L	L	L	L	L	H	
H	H	X	X	X	X	Q_{N-1}								Memory
H	L	L	L	L	L	L	Q_{N-1}	Q_{N-1}	Q_{N-1}					
H	L	H	L	L	L	H	Q_{N-1}	Q_{N-1}						
H	L	L	H	L	L	Q_{N-1}	L	Q_{N-1}						
H	L	H	H	L	L	Q_{N-1}	H	Q_{N-1}						Addressable Latch
•	•	•		•				•						
•	•	•		•				•						
•	•	•		•				•						
H	L	L	H	H	H	Q_{N-1}						Q_{N-1}	L	
H	L	H	H	H	H	Q_{N-1}						Q_{N-1}	H	

X = Don't Care Condition

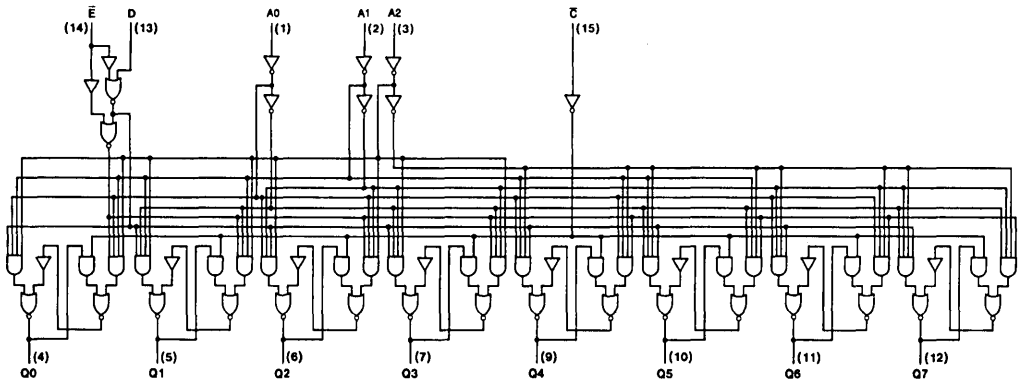
L = Low Voltage Level

H = High Voltage Level

Q_{N-1} = Previous Output State

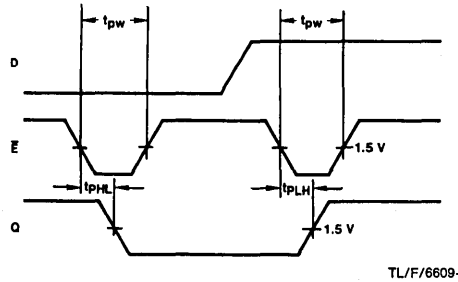
Logic Diagram

DM93/8334



TL/F/6609-2

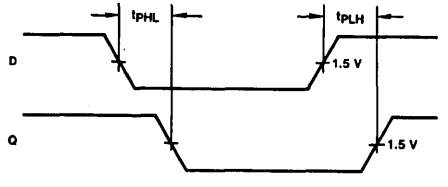
Switching Time Waveforms



TL/F/6609-3

Other Conditions: C = H, A = Stable

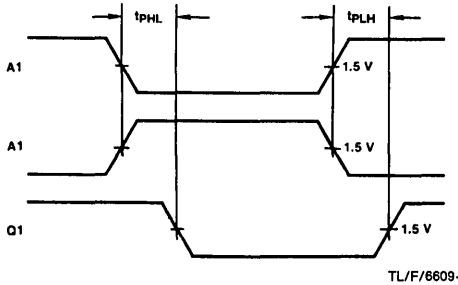
Figure 1



TL/F/6609-4

Other Conditions: $\overline{E}$ = L, $\overline{C}$ = H, A = Stable

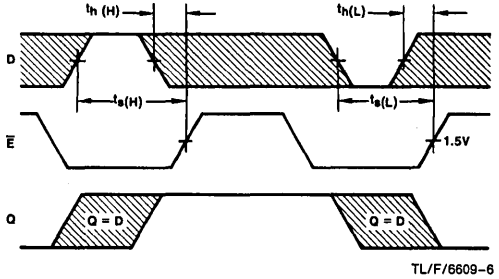
Figure 2



TL/F/6609-5

Other Conditions: $\overline{E}$ = L, $\overline{C}$ = L, D = H

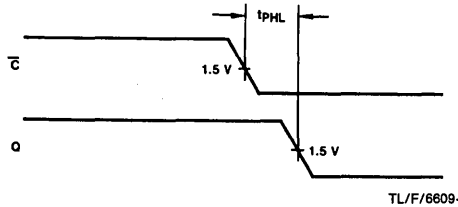
Figure 3



TL/F/6609-6

Other Conditions: C = H, A = Stable

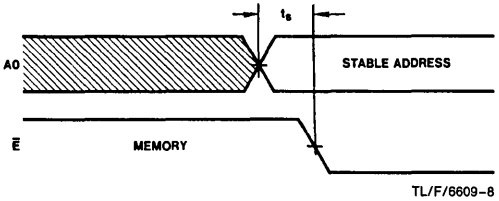
Figure 4



TL/F/6609-7

Other Conditons: $\overline{E}$ = H

Figure 5



TL/F/6609-8

Other Conditions: $\overline{C}$ = H

Figure 6

Note: The shaded areas indicate when the inputs are permitted to change for predictable output performance.

National Semiconductor Corporation

DM9601/DM8601 Retriggerable One Shots

General Description

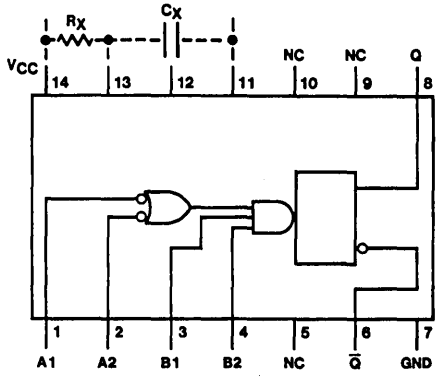
These retriggerable one shots provide the designer with four inputs; two active high and two active low. This permits a choice of either leading-edge or trailing-edge triggering, independent of input transition times. When input conditons for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge again. The retriggerable feature allows for output pulse widths to be expanded. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. Retriggering may be inhibited by tying the $\overline{Q}$ output to an active low input.

Features

- High speed operation—input repetition rate > 10 MHz
- Flexibility of operation—optional retriggering/lock-out capability
- Output pulse width range—50 ns to ∞
- Leading or trailing edge triggering
- Complementary outputs/inputs
- Input clamping diodes
- DTL/TTL compatible logic levels

Connection Diagram

Dual-In-Line Package



TL/F/6610–1

Order Number DM9601J or DM8601N
See NS Package Number J14A or N14A

Function Table

Inputs				Outputs	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎏
L	X	H	↑	⎍	⎏
X	L	H	H	L	H
X	L	↑	H	⎍	⎏
X	L	H	↑	⎍	⎏
H	↓	H	H	⎍	⎏
↓	↓	H	H	⎍	⎏
↓	H	H	H	⎍	⎏

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level
↑ = Low to High Level Transition
↓ = High to Low Level Transition
⎍ = Positive Pulse
⎏ = Negative Pulse

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM96	−55°C to +125°C
DM86	0° to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM9601			DM8601			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	$T_A = -55°C$	2						V
		$T_A = 0°C$				1.9			
		$T_A = 25°C$	1.7			1.8			
		$T_A = 75°C$				1.6			
		$T_A = 125°C$	1.5						
V_{IL}	Low Level Input Voltage	$T_A = -55°C$			0.85				V
		$T_A = 0°C$						0.85	
		$T_A = 25°C$			0.9			0.85	
		$T_A = 75°C$						0.85	
		$T_A = 125°C$			0.85				
I_{OH}	High Level Output Current				−0.72			−0.96	mA
I_{OL}	Low Level Output Current				10			12.8	mA
T_A	Free Air Operating Temperature		−55		125	0		75	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min, (Note 4)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IL} = Max, V_{IH} = Min (Note 4)	DM96			0.4	V
			DM86			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V				60	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	DM96 V_{IN} = 0.40V			−1.6	mA
			DM96 V_{IN} = 0.45V			−1.6	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Notes 2 and 4)	DM96	−10		−40	mA
			DM86	−10		−40	
I_{CC}	Supply Current	V_{CC} = Max				25	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: Unless otherwise noted, R_X = 10k between PIN 13 and V_{CC} on all tests.

Note 4: Ground PIN 11 for V_{OL} test on PIN 6, V_{OH} and I_{OS} tests on PIN 8. Open PIN 11 for V_{OL} test on PIN 8, V_{OH} and I_{OS} tests on PIN 6.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	Negative Trigger Input to True Output	C_L = 15 pF, C_X = 0, R_X = 5 kΩ		40	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Negative Trigger Input to Complement Output			40	ns
$t_{PW(MIN)}$	Minimum True Output Pulse Width				65	ns
t_{PW}	Pulse Width		R_X = 10 kΩ, C_X = 1000 pF	3.08	3.76	μs
C_{STRAY}	Maximum Allowable Wiring Capacitance		Pin 13 to GND		50	pF
R_X	External Timing Resistor		DM96		25	kΩ
R_X	External Timing Resistor		DM86		50	kΩ

Operating Rules

1. An external resistor R_X and an external capacitor C_X are required for operation. The value of R_X can vary between the limits shown in switching characteristics. The value of C_X is optional and may be adjusted to achieve the required output pulse width.
2. Output pulse width t_{PW} may be calculated as follows:

$$t_{PW} = K R_X C_X \left[1 + \frac{0.7}{R_X}\right] \text{ (for } C_X > 10^3 \text{ pF)}$$

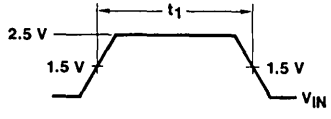
$K \approx 0.34$

R_X in kΩ, C_X in pF and t_{PW} in ns.

(For $C_X < 10^3$ pF, see curve.)

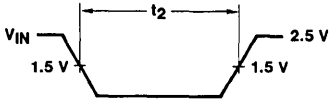
3. R_X and C_X must be kept as close as possible to the circuit in order to minimize stray capacitance and noise pickup. If remote trimming is required, R_X may be split up such that at least $R_{X(MIN)}$ must be as close as possible to the circuit and the remote portion of the trimming resistor $R < R_{X(MAX)} - R_X$.
4. Set-up time (t_1) for input trigger pulse must be > 40 ns. (See *Figure 1*).

   Release time (t_2) for input trigger pulse must be > 40 ns. (See *Figure 2*).



TL/F/6610-2

FIGURE 1



TL/F/6610-3

FIGURE 2

5. Retrigger pulse width (see *Figure 3*) is calculated as follows:

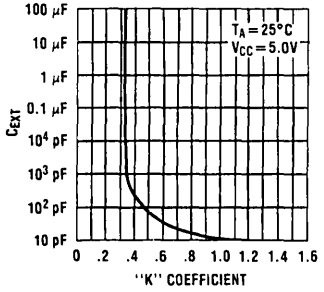
$$t_W = t_{PW} + t_{PLH} = K R_X C_X \left[1 + \frac{0.7}{R_X}\right] + t_{PLH}$$

TL/F/6610-4

FIGURE 3

Typical "K" Coefficient Variation vs Timing Capacitance

The multiplicative factor "K" varies as a function of the timing capacitor, C_X. The graph below details this characteristic:

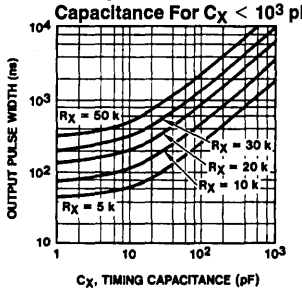


TL/F/6610-5

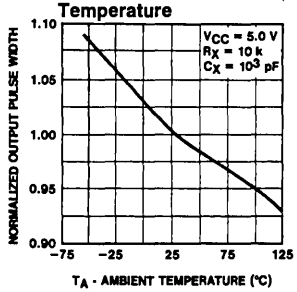
*For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.

Typical Performance Characteristics

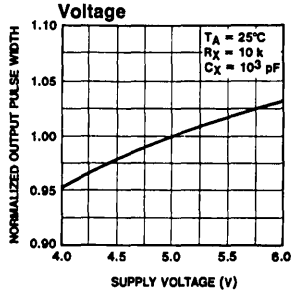
Output Pulse Width vs Timing Resistance And Capacitance For $C_X < 10^3$ pF



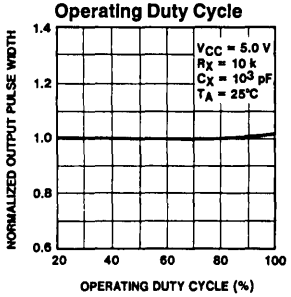
Normalized Output Pulse Width vs Ambient Temperature



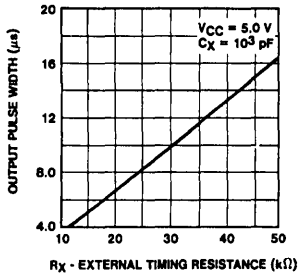
Normalized Output Pulse Width vs Supply Voltage



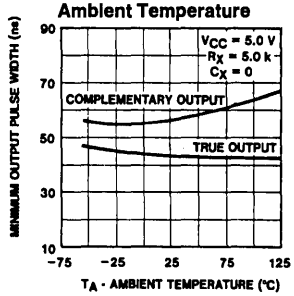
Normalized Output Pulse Width vs Operating Duty Cycle



Pulse Width vs Timing Resistance

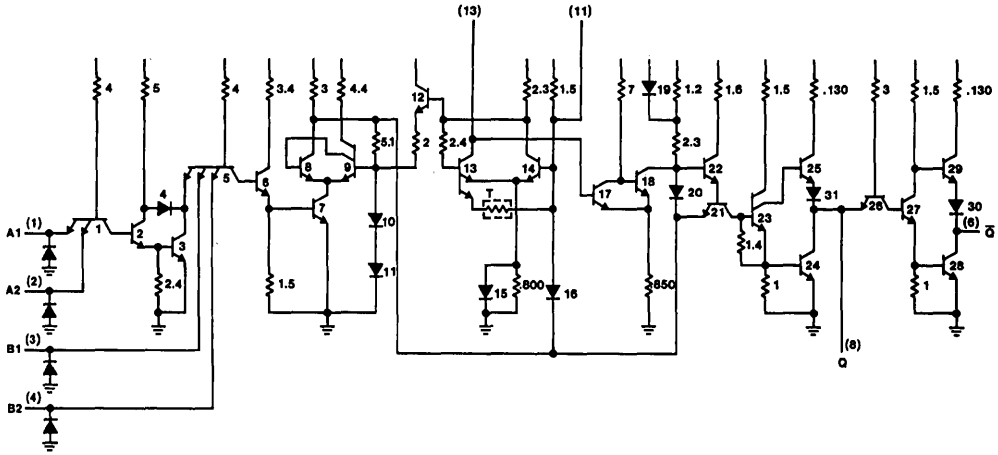


Output Pulse Width vs Ambient Temperature



TL/F/6610–6

Schematic Diagram



TL/F/6610–7

National Semiconductor Corporation

DM9602/DM8602 Dual Retriggerable, Resettable One Shots

General Description

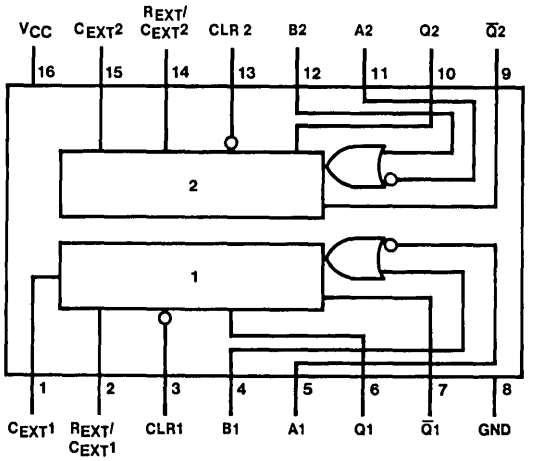
These dual resettable, retriggerable one shots have two inputs per function; one which is active high, and one which is active low. This allows the designer to employ either leading-edge or trailing-edge triggering, which is independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is allowed to rapidly discharge and then charge again. The retriggerable feature permits output pulse widths to be extended. In fact a continuous true output can be maintained by having an input cycle time which is shorter than the output cycle time. The output pulse may then be terminated at any time by applying a low logic level to the RESET pin. Retriggering may be inhibited by either connecting the Q output to an active high input, or the $\overline{Q}$ output to an active low input.

Features

- 70 ns to ∞ output width range
- Resettable and retriggerable—0% to 100% duty cycle
- TTL input gating—leading or trailing edge triggering
- Complementary TTL outputs
- Optional retrigger lock-out capability
- Pulse width compensated for V_{CC} and temperature variations

Connection Diagram

Dual-In-Line Package



TL/F/6611–1

Order Number DM9602J or DM8602N
See NS Package Number J16A or N16A

Function Table

Pin No's.			Operation
A	B	CLR	
H → L	L	H	Trigger
H	L → H	H	Trigger
X	X	L	Reset

H = High Voltage Level
L = Low Voltage Level
X = Don't Care

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM96	−55°C to +125°C
DM86	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM9602			DM8602			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	$T_A = -55°C$	2						V
		$T_A = 0°C$				1.9			
		$T_A = 25°C$	1.7			1.8			
		$T_A = 75°C$				1.65			
		$T_A = 125°C$	1.5						
V_{IL}	Low Level Input Voltage	$T_A = -55°C$			0.85				V
		$T_A = 0°C$						0.85	
		$T_A = 25°C$			0.9			0.85	
		$T_A = 75°C$						0.85	
		$T_A = 125°C$			0.85				
I_{OH}	High Level Output Current				−0.8			−0.8	mA
I_{OL}	Low Level Output Current				16			16	mA
T_A	Free Air Operating Temperature		−55		125	0		75	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions (Note 3)		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM96			0.4	V
			DM86			0.45	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 4.5V				60	μA
I_{IL}	Low Level Input Current	V_{CC} = Max	DM96 V_I = 0.40V			−1.6	mA
			DM86 V_I = 0.45V			−1.6	
		V_{CC} = Min	DM96 V_I = 0.40V			−1.24	
			DM86 V_I = 0.45V			−1.41	
I_{OS}	Short Circuit Output Current	V_{CC} = Max, V_{OUT} = 1V (Notes 2 and 4)	DM96			−25	mA
			DM86			−35	
I_{CC}	Supply Current	V_{CC} = Max	DM96		39	45	mA
			DM86		39	50	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

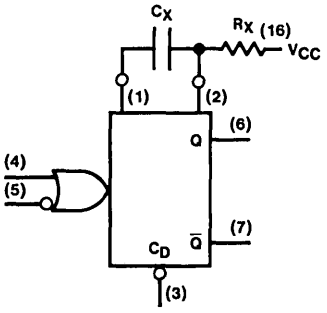
Note 3: Unless otherwise noted, R_X = 10k for all tests.

Note 4: Ground PIN 1(15) for V_{OL} on PIN 7(9) or V_{OH} and I_{OS} on PIN 6(10) and apply momentary ground to PIN 4(12). Open PIN 1(15) for V_{OL} on PIN 6(10) or V_{OH} and I_{OS} on PIN 7(9).

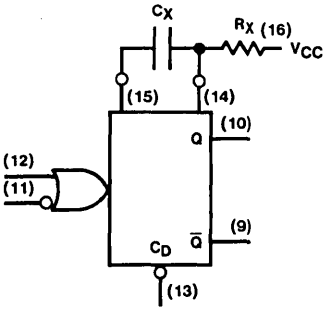
Switching Characteristics V_{CC} = 5V, T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter		Conditions	DM96 02 Min	DM96 02 Max	DM86 02 Min	DM86 02 Max	Units
t_{PLH}	Propagation Delay Time, Low-to-High Level Output	Negative Trigger Input to True Output	C_L = 15 pF, C_X = 0, R_X = 5 kΩ		35		40	ns
t_{PHL}	Propagation Delay Time, High-to-Low Level Output	Negative Trigger Input To Complement Output			43		48	ns
t_{PW}(MIN)	Minimum True Output Pulse Width				90		100	ns
	Minimum Complement Pulse Width				100		110	
t_{PW}	Pulse Width		R_X = 10 kΩ, C_X = 1000 pF	3.08	3.76	3.08	3.76	μs
C_{STRAY}	Maximum Allowable Wiring Capacitance		Pins 2, 14 to GND		50		50	pF
R_X	External Timing Resistor			5	25	5	50	kΩ

Logic Diagrams



TL/F/6611–2



TL/F/6611–3

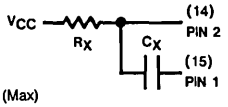
Operating Rules

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
3. The output pulse with (t) is defined as follows:

$$t = K R_X C_X \left[1 + \frac{1}{R_X}\right] \quad \text{for } C_X > 10^3 \text{ pF}, \; K \approx 0.34$$

where: R_X is in kΩ, C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see *Figure 1.*
for K vs C_X see *Figure 6.*

4. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0V is less than 3 μA, and the inverse capacitor leakage at 1.0V is less than 5 μA over the operational temperature range.



$R < 0.6\ R_X$ (Max)

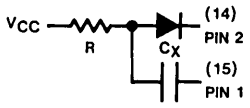
TL/F/6611–4

Operating Rules (Continued)

B. Use with high inverse leakage current electrolytic capacitors:

The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.

$$t \approx 0.3\, RC_X$$



TL/F/6611–5

C. Use to obtain extended pulse widths:

This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.

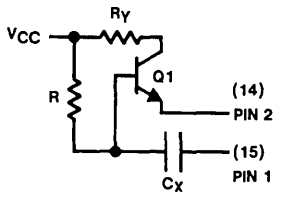
$R < R_X$ (0.7) (h_{FE} Q1) or < 2.5 MΩ, whichever is the lesser

R_X (min) < R_Y < R_X (max)

(5 kΩ ≤ R_Y ≤ 10 kΩ is recommended)

Q1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962.

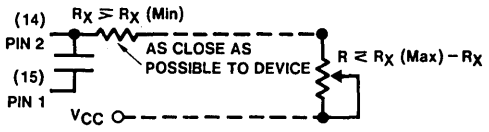
$$t \approx 0.3\, RC_X$$



TL/F/6611–6

This configuration is not recommended with retriggerable operation.

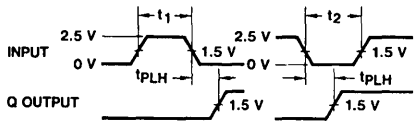
5. To obtain variable pulse width by remote trimming, the following circuit is recommended:



TL/F/6611–7

6. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

7. Input Trigger Pulse Rules (See Triggering Truth Table)



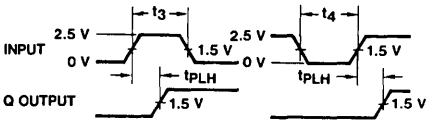
TL/F/6611–8

Input to Pin 5(11), (Pin 3(13) = HIGH)

Pin 4(12) = LOW

t_1, t_3 = Min. Positive Input Pulse Width > 40 ns

t_2, t_4 = Min. Negative Input Pulse Width > 40 ns



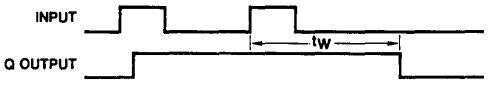
TL/F/6611–9

Input to Pin 4(12) (Pin 3(13) = HIGH)

Pin 5(11) = HIGH

8. The retriggerable pulse width is calculated as shown below:

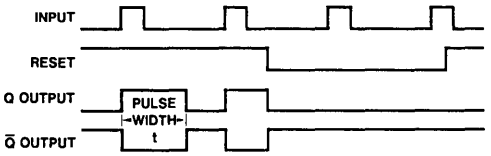
$$t_W = t + t_{PLH} = K\, R_X\, C_X \left(1 + \frac{1}{R_X}\right) + t_{PLH}$$



TL/F/6611–10

The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X (ns) after the initial trigger pulse (i.e., during the discharge cycle).

9. Reset Operation—An overriding clear (active LOW level) is provided on each one shot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.

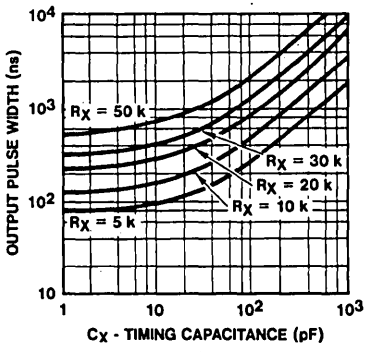


TL/F/6611–11

10. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the DM9602/DM8602 is recommended.

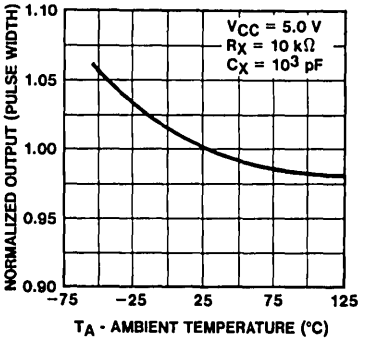
*For further detailed device characteristics and output performance, please refer to the NSC one-shot application note, AN-366.

Typical Performance Characteristics



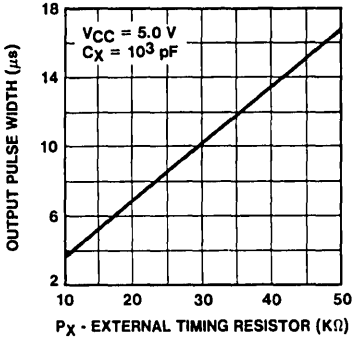
TL/F/6611–12

FIGURE 1. Output Pulse Width vs Timing Resistance and Capacitance for $C_X < 10^3$ pF



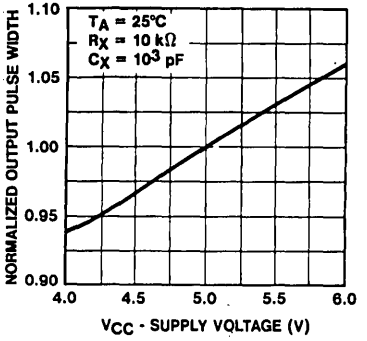
TL/F/6611–13

FIGURE 2. Normalized Output Pulse Width vs Ambient Temperature



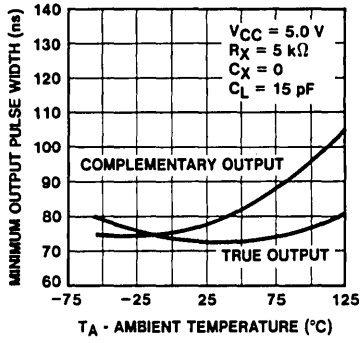
TL/F/6611–14

FIGURE 3. Pulse Width vs Timing Resistor



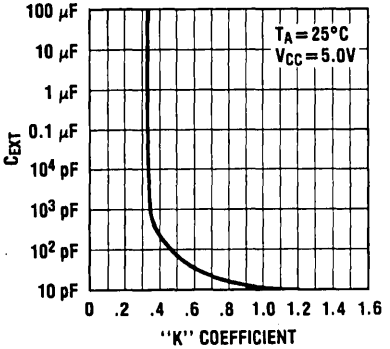
TL/F/6611–15

FIGURE 4. Normalized Output Pulse Width vs Supply Voltage



TL/F/6611–16

FIGURE 5. Minimum Output Pulse Width vs Ambient Temperature



TL/F/6611–17

FIGURE 6. Typical "K" Coefficient Variation vs Timing Capacitance

4

Section 5

Low Power

Section 5 Contents

National Semiconductor Corporation

DM54L00/DM74L00 Quad 2-Input NAND Gates

General Description

This device contains four independent gates each of which performs the logic NAND function.

Absolute Maximum Ratings (Note)

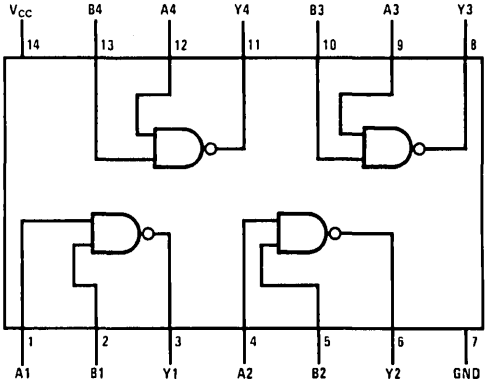
Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM57L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Connection Diagram

Dual-In-Line Package



TL/F/6654–1

Order Number DM54L00J or DM74L00N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{AB}$

Inputs		Output
A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

H = High Logic Level
L = Low Logic Level

5

Recommended Operating Conditions

Symbol	Parameter	DM54L00			DM74L00			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Ouput Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Voltage Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.44	0.8	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.16	2.04	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one should be shorted at a time.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Low to High Level Output	R_L = 4 kΩ C_L = 50 pF		60	ns
t_{PHL}	Propagation Delay High to Low Level Output			60	ns

National Semiconductor Corporation

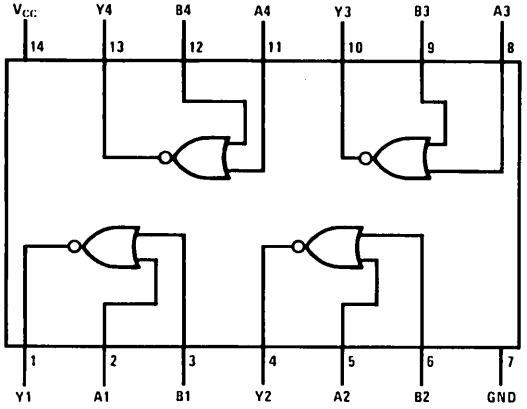
DM54L02/DM74L02 Quad 2-Input NOR Gates

General Description

This device contains four independent gates each of which performs the logic NOR function.

Connection Diagram

Dual-In-Line Package



TL/F/6656–1

Order Number DM54L02J or DM74L02N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{A + B}$$

Inputs		Output
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM54L02			DM74L02			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.8	1.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.4	2.6	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	R_L = 4 kΩ, C_L = 50 pF		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

DM54L04/DM74L04 Hex Inverting Gates

General Description

This device contains six independent gates each of which performs the logic INVERT function.

Absolute Maximum Ratings (Note)

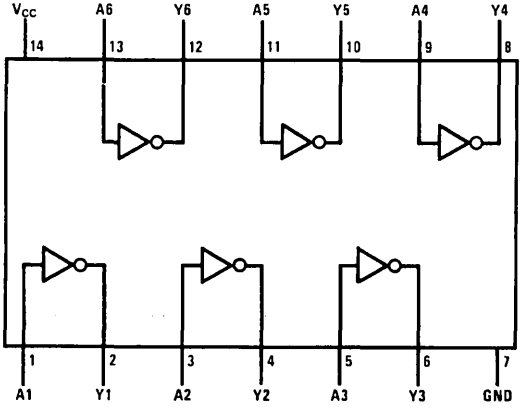
Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Connection Diagram

Dual-In-Line Package



TL/F/6616–1

Order Number DM54L04J or DM74L04N
See NS Package Number J14A or N14A

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

5

Recommended Operating Conditions

Symbol	Parameter	DM54L04			DM74L04			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.6	1.2	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			1.7	3.06	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	R_L = 4 kΩ, C_L = 50 pF		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

DM54L10/DM74L10 Triple 3-Input NAND Gates

General Description

This device contains three independent gates each of which performs the logic NAND function.

Absolute Maximum Ratings (Note)

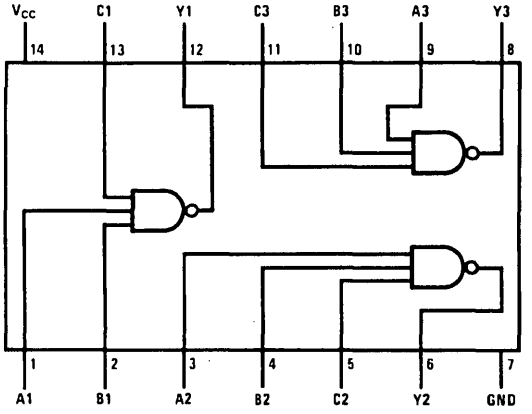
Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Connection Diagram

Dual-In-Line Package



TL/F/6619–1

Order Number DM54L10J or DM74L10N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{ABC}$$

Inputs			Output
A	B	C	Y
X	X	L	H
X	L	X	H
L	X	X	H
H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

Recommended Operating Conditions

Symbol	Parameter	DM54L10			DM74L10			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.33	0.6	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			0.87	1.53	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	R_L = 4 kΩ, C_L = 50 pF		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

DM54L20/DM74L20 Dual 4-Input NAND Gates

General Description

This device contains two independent gates each of which performs the logic NAND function.

Absolute Maximum Ratings (Note)

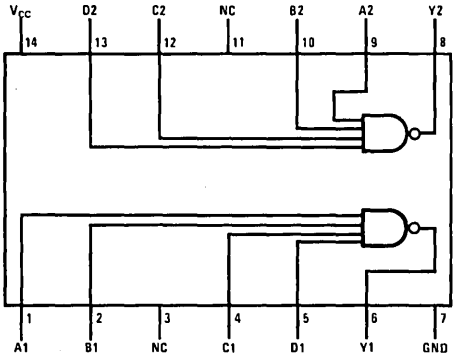
Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Connection Diagram

Dual-In-Line Package



TL/F/6621–1

Order Number DM54L20J or DM74L20N
See NS Package Number J14A or N14A

Function Table

$$Y = \overline{ABCD}$$

Inputs				Output
A	B	C	D	Y
X	X	X	L	H
X	X	L	X	H
X	L	X	X	H
L	X	X	X	H
H	H	H	H	L

H = High Logic Level
L = Low Logic Level
X = Either Low or High Logic Level

5

Recommended Operating Conditions

Symbol	Parameter	DM54L20			DM74L20			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Ouput Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max		2.4	3.3		V
V_{OL}	Low Voltage Output Voltage	V_{CC} = Min I_{OL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			0.22	0.4	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			0.58	1.02	mA

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	Conditions	Min	Max	Units
t_{PLH}	Propagation Delay Time Low to High Level Output	R_L = 4 kΩ, C_L = 50 pF		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output			60	ns

Note 1: All typicals are at V_{CC} = 5V, T_A 25°C.

Note 2: Not more than one output should be shorted at a time.

National Semiconductor Corporation

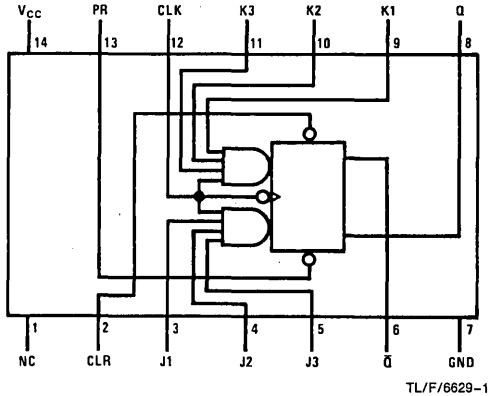
DM54L72/DM74L72 AND-Gated Master-Slave J-K Flip-Flop with Preset, Clear and Complementary Outputs

General Description

This device contains a positive pulse triggered master-slave J-K flip-flop with complementary outputs. Multiple J and K inputs are ANDed together to produce the internal J and K function for the flip-flop. The J and K data is processed by the flip-flop after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the AND gates is transferred to the master. While the clock is high the AND gate inputs are disabled. On the negative transition of the clock the data from the master is transferred to the slave. The logic state of the J and K inputs must not be allowed to change while the clock is in the high state. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the preset or clear inputs sets or resets the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6629–1

Order Number DM54L72J or DM74L72N
See NS Package Number J14A or NJ14A

Function Table

Inputs					Outputs	
PR	CLR	CLK	J (Note 1)	K (Note 1)	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	⎍	L	L	Q_0	$\overline{Q}_0$
H	H	⎍	H	L	H	L
H	H	⎍	L	H	L	H
H	H	⎍	H	H	Toggle	

Note 1: J = (J1)(J2)(J3), K = (K1)(K2)(K3)

H = High Logic Level
X = Either Low or High Logic Level
L = Low Logic Level
⎍ = Positive pulse. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.
Q_0 = The output logic level before the indicated input conditions were established.
* = This configuration is nonstable; that is, it will not persist when the preset and/or clear inputs return to their inactive (high) level.
Toggle = Each output changes to the complement of its previous level on each complete high level clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guarateed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L72			DM74L72			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage	Clock			0.6			0.6	V
		Others			0.7			0.7	
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency (Note 2)		0		6	0		6	MHz
t_W	Pulse Width (Note 2)	Clock High	100			100			ns
		Clock Low	100			100			
		Preset Low	100			100			
		Clear Low	100			100			
t_{SU}	Input Setup Time (Notes 1 & 2)		0 ↑			0 ↑			ns
t_H	Input Hold Time (Notes 1 & 2)		0 ↓			0 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	J, K			100	μA
			Clear			200	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			10	μA
			Clear			20	
			Preset			20	
			Clock			−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	J, K			−0.18	mA
			Clear			−0.36	
			Preset			−0.36	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			0.76	1.44	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		150	ns
t_{PLH}	Propagation Delay Level Output Low to High Level Output	Clear to $\overline{Q}$		75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		150	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	150	ns

National Semiconductor Corporation

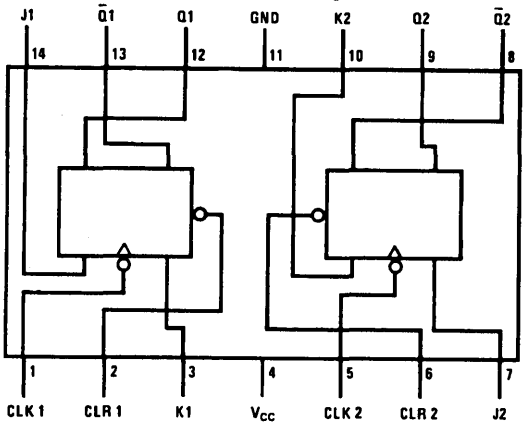
DM54L73/DM74L73 Dual Master-Slave J-K Flip-Flops with Clear and Complementary Outputs

General Description

This device contains two independent positive pulse triggered J-K flip-flops with complementary outputs. The J and K data is processed by the flip-flops after a complete clock pulse. While the clock is low the slave is isolated from the master. On the positive transition of the clock, the data from the J and K inputs is transferred to the master. While the clock is high, the data from the J and K inputs are disabled. On the negative transition of the clock, the data from the master is transferred to the slave. The logic states of the J and K inputs must not be allowed to change while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse. A low logic level on the clear input will reset the outputs regardless of the logic states of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6630–1

Order Number DM54L73J or DM74L73N
See NS Package Number J14A or N14A

Function Table

Inputs				Outputs	
CLR	CLK	J	K	Q	$\overline{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_O	$\overline{Q}_O$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	Toggle	

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

⎍ = Positive pulse data. The J and K inputs must be held constant while the clock is high. Data is transferred to the outputs on the falling edge of the clock pulse.

Q_O = The output logic level before the indicated input conditions were established.

Toggle = Each output changes to the complement of its previous level on each complete high level clock pulse.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L73			DM74L73			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage	Clock			0.6			0.6	V
		Others			0.7			0.7	
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency (Note 2)		0		6	0		6	MHz
t_W	Pulse Width (Note 2)	Clock High	100			100			ns
		Clock Low	100			100			
		Clear Low	100			100			
t_{SU}	Input Setup Time (Notes 1 & 2)		0 ↑			0 ↑			ns
t_H	Input Hold Time (Notes 1 & 2)		0 ↓			0 ↓			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbols (↑, ↓) indicate the edge of the clock pulse used for reference: ↑ for rising edge, ↓ for falling edge.

Note 2: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Voltage Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	J, K			100	μA
			Clear			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	J, K			10	μA
			Clear			20	
			Clock			−200	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	J, K			−0.18	mA
			Clear			−0.36	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			1.5	2.88	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock is grounded.

Switching Characteristics V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		150	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		75	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	75	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	150	ns

National Semiconductor Corporation

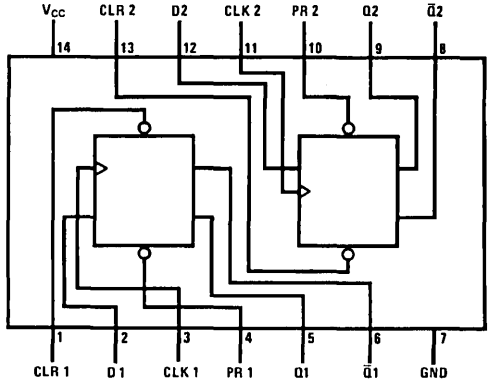
DM54L74/DM74L74 Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is low or high without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Connection Diagram

Dual-In-Line Package



TL/F/6631–1

Order Number DM54L74J or DM74L74N
See NS Package Number J14A or N14A

Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_O	$\overline{Q}_O$

H = High Logic Level

X = Either Low or High Logic Level

L = Low Logic Level

↑ = Positive-going transition.

Q_O = The output logic level of Q before the indicated input conditions were established.

* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs returned to their inactive (high) level.

5

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L74			DM74L74			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency (Note 2)		0		6	0		6	MHz
t_W	Pulse Width (Note 2)	Clock High	75			75			ns
		Clock Low	75			75			
		Preset Low	75			75			
		Clear Low	75			75			
t_{SU}	Input Setup Time (Notes 1 & 2)		50 ↑			50 ↑			ns
t_H	Input Hold Time (Notes 1 & 2)		15 ↑			15 ↑			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: The symbol (↑) indicates the rising edge of the clock pulse is used for reference.

Note 2: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max V_I = 5.5V	D			100	μA
			Clear			300	
			Preset			200	
			Clock			200	
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	D			10	μA
			Clear			30	
			Preset			20	
			Clock			20	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	D			−0.18	mA
			Clear			−0.36	
			Preset			−0.18	
			Clock			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			1.6	3	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Preset to Q		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Preset to $\overline{Q}$		120	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clear to $\overline{Q}$		60	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Q		120	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Q or $\overline{Q}$	10	90	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Q or $\overline{Q}$	10	120	ns

National Semiconductor Corporation

DM54L93/DM74L93 Decade, Divide-by-12, and Binary Counters

General Description

Each of these monolithic counters contains four master-slave flip-flops and additional gating to provide a divide-by-two counter and a three-stage binary counter for which the count cycle length is divide-by-eight.

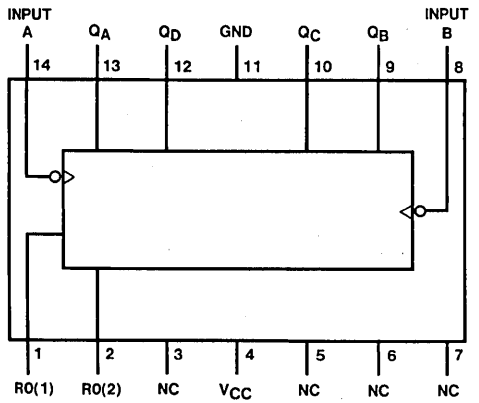
To use their maximum count length (decade, divide-by-twelve, or four-bit binary), the B input is connected to the Q_A output. The input count pulses are applied to input A and the outputs are as described in the appropriate truth table.

Features

- Typical power dissipation 16 mW
- Count frequency 15 MHz

Connection Diagram

Dual-In-Line Package



TL/F/6637–1

Order Number DM54L93J or DM74L93N
See NS Package Number J14A or N14A

Function Tables

COUNT SEQUENCE (See Note A)

Count	Output			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

RESET/COUNT TRUTH TABLE (Note B)

Reset Inputs		Output			
R0(1)	R0(2)	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

Note A: Output Q_A is connected to input B

Note B: H = High Level, L = Low Level, X = Don't Care.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L93			DM74L93			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency (Note 5)		0		6	0		6	MHz
t_W	Pulse Width (Note 5)	A	90			90			ns
		B	90			90			
		Reset	200			200			
t_{REL}	Reset Release time (Note 5)		200			200			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.4		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min (Note 4)	DM54		0.15	0.3	V
			DM74		0.25	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V	Reset			0.1	mA
			A			0.2	
			B			0.2	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Reset			10	μA
			A			20	
			B			20	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Reset			−0.18	mA
			A			−0.36	
			B			−0.36	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				5.5	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, R0 inputs grounded following momentary connection to 4.5V and all other inputs grounded.

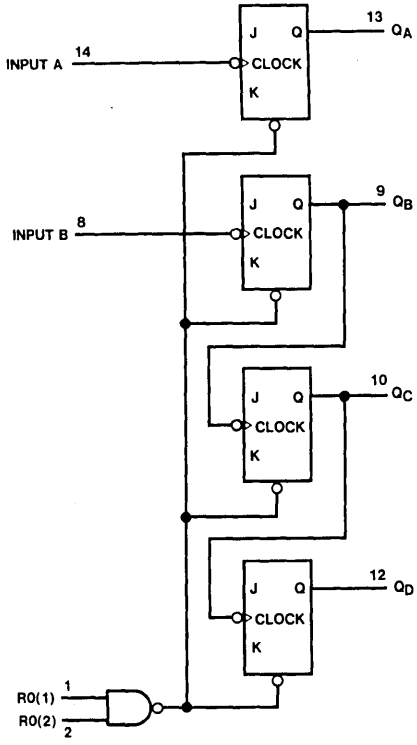
Note 4: Q_A outputs are tested at I_{OL} = max plus the limit value of I_{IL} for the B input. This permits driving the B input while maintaining full fan-out capability.

Note 5: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency	A to Q_A	6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	A to Q_D		400	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	A to Q_D		400	ns

Logic Diagram



TL/F/6637–2

The J and K inputs shown without connection are for reference only and are functionally at a high level.

National Semiconductor Corporation

DM54L95/DM74L95 4-Bit Parallel Access Shift Registers

General Description

These 4-bit registers feature parallel and serial inputs, parallel output, mode control, and two clock inputs. The registers have three modes of operation.

Parallel (broadside) load
Shift right (the direction Q_A toward Q_D)
Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied simultaneously to clock 1 and clock 2 if both modes can be clocked from the same source.

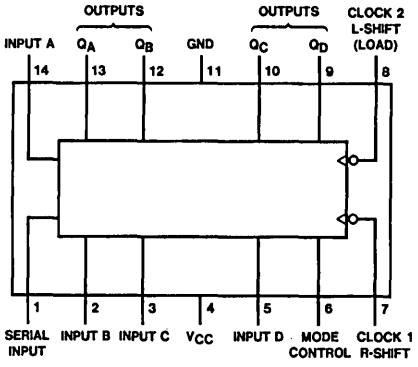
Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the truth table will also ensure that register contents are protected.

Features

- Typical maximum clock frequency 14 MHz
- Typical power dissipation mW

Connection Diagram

Dual-In-Line Package



TL/F/6638–1

Order Number DM54L95J or DM74L95N
See NS Package Number J14A or N14A

Function Table

Inputs								Outputs			
Mode Control	Clocks		Serial	Parallel				Q_A	Q_B	Q_C	Q_D
	2 (L)	1 (R)		A	B	C	D				
H	H	X	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{AO}	Q_{Bn}	Q_{CO}	Q_{DO}
↓	L	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↓	L	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	L	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}
↑	H	H	X	X	X	X	X	Q_{AO}	Q_{BO}	Q_{CO}	Q_{DO}

†Shifting left requires external connection of Q_B to A, Q_C to B, Q_D to C. Serial data is entered at input D.
H = High Level (Steady State), L = Low Level (Steady State), X = Don't Care (Any input, including transitions).
↓ = Transition from high to low level. ↑ = Transition from low to high level.
a, b, c, d, = The level of steady state input at inputs A, B, C, or D, respectively.
Q_{AO}, Q_{BO}, Q_{CO}, Q_{DO} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady state input conditions were established.
Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = The level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most recent ↓ transition of the clock.

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter		DM54L95			DM74L95			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency (Note 1)		0		6	0		6	MHz
$t_{W(CLK)}$	Pulse Width of Clock (Note 1)		90			90			ns
t_{SU}	Data Setup Time (Note 1)		50			50			ns
t_{EN}	Time to Enable Clock (Note 1)	Clock 1	120			120			ns
		Clock 2	100			100			ns
t_H	Data Hold Time (Note 1)		0			0			ns
t_{IN}	Time to Inhibit Clock 1 or Clock 2 (Note 1)		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Note 1: T_A = 25°C and V_{CC} = 5V.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min		2.4	3.1		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.13	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V	Mode			0.2	mA
			Others			0.1	
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V	Mode			20	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V	Mode			−0.36	mA
			Others			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			4.8	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A 25°C

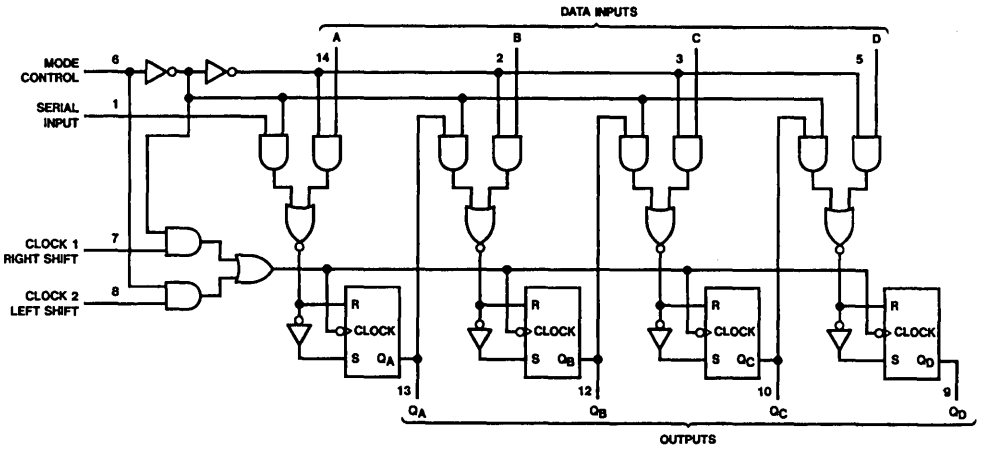
Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5V; and a momentary 3V, then ground, applied to both clock inputs.

Switching Characteristics at V_{CC} = 5V and T_A 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4Ω, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		90	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		90	ns

Logic Diagram



TL/F/6638–2

National Semiconductor Corporation

DM54L98/DM74L98 4-Bit Storage Registers

General Description

These data selectors/storage registers are composed of four S-R master-slave flip-flops, four AND-OR INVERT gates, one buffer, and six inverter/drivers.

When the word select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high level input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is shifted to the output terminals on the negative-going edge of the clock pulse.

Typical clock frequency is 12 MHz.

Absolute Maximum Ratings (Note)

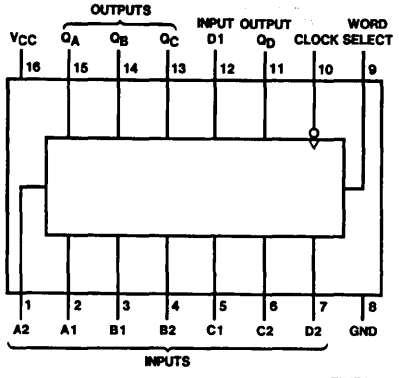
Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Connection Diagram

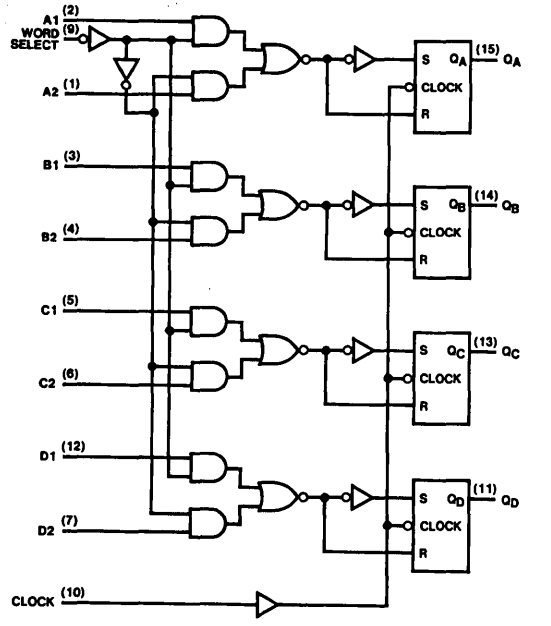
Dual-In-Line-Package



TL/F/6639–1

Order Number DM54L98J or DM74L98N
See NS Package Number J16A or N16A

Logic Diagram



TL/F/6639–2

Recommended Operating Conditions

Symbol	Parameter		DM54L98			DM74L98			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.7			0.7	V
I_{OH}	High Level Output Current				−0.2			−0.2	mA
I_{OL}	Low Level Output Current				2			3.6	mA
f_{CLK}	Clock Frequency (Note 4)		0		6	0		6	MHz
t_W	Clock Pulse Width (Note 4)		100	65		100	65		ns
t_{SU}	Setup Time (Note 4)	Data High	100			100			ns
		Data Low	120			120			
		Select High	150			150			
		Select Low	100			100			
T_A	Free Air Operating Temperature		−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min	DM54		0.15	0.3	V
			DM74		0.2	0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	DM54	−3		−15	mA
			DM74	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 2)			6	8	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: I_{CC} is measured with all outputs open and all inputs grounded.

Note 3: Not more than one output should be shorted at a time.

Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output		80	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output		100	ns

National Semiconductor Corporation

DM75L60/DM85L60, DM75L63/DM85L63 Synchronous 4-Bit Up/Down Decade/Binary Counters

General Description

These circuits are synchronous up/down counters; the L60 circuit is a BCD counter and the L63 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

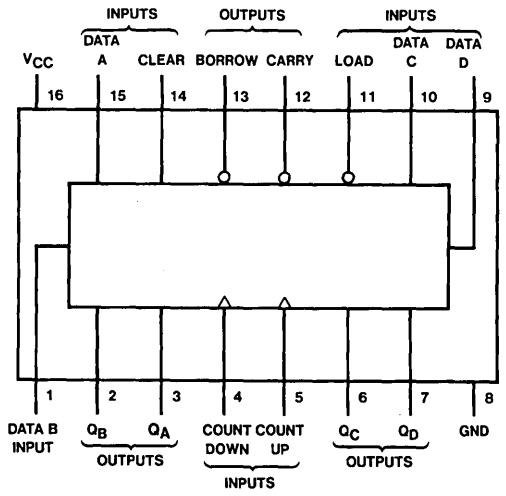
A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset for each flip-flop
- Typical count frequency 12 MHz
- Typical power dissipation 40 mW

Connection Diagram

Dual-In-Line Package



TL/F/6649–1

Order Numbers DM75L60J, DM75L63J, DM85L60N, or DM85L63N
See NS Package Number J16A or N16A

Absolute Maximum Ratings (Note)

Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Storage Temperature Range	−65°C to +150°C
Operating Free Air Temperature Range	
DM75L	−55°C to +125°C
DM85L	0°C to +70°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	DM75L60, L63			DM85L60, L63			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
f_{CLK}	Clock Frequency (Note 4)	0		6	0		6	MHz
t_W	Pulse Width of Any Input (Note 4)	70			70			ns
t_{SU}	Data Setup Time (Note 4)	30			30			ns
t_H	Data Hold Time (Note 4)	0			0			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM75		0.15	0.3	V
			DM85		0.2	0.4	
I_I	Input Current @Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				10	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.3V				−0.18	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM75	−3		−15	mA
			DM85	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)			8	13	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

Note 4: T_A = 25°C and V_{CC} = 5V.

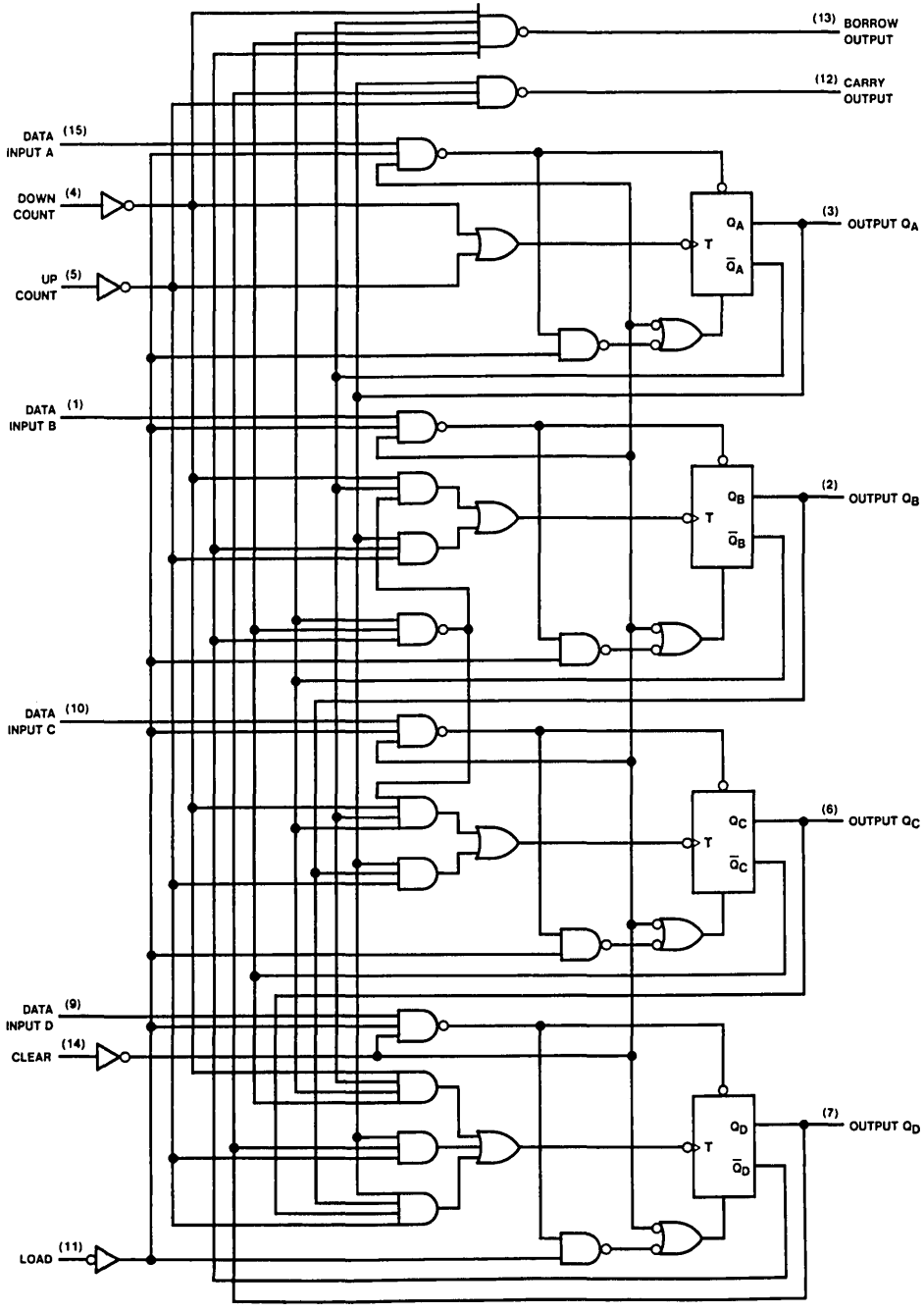
Switching Characteristics at V_{CC} = 5V and T_A = 25°C

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
		Min	Max	
f_{MAX} Maximum Clock Frequency		6		ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Up to Carry		60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Up to Carry		120	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Down to Borrow		60	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Down to Borrow		100	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Either Count to Q		90	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Either Count to Q		150	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Q		110	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Q		200	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		190	ns

Logic Diagrams

L60

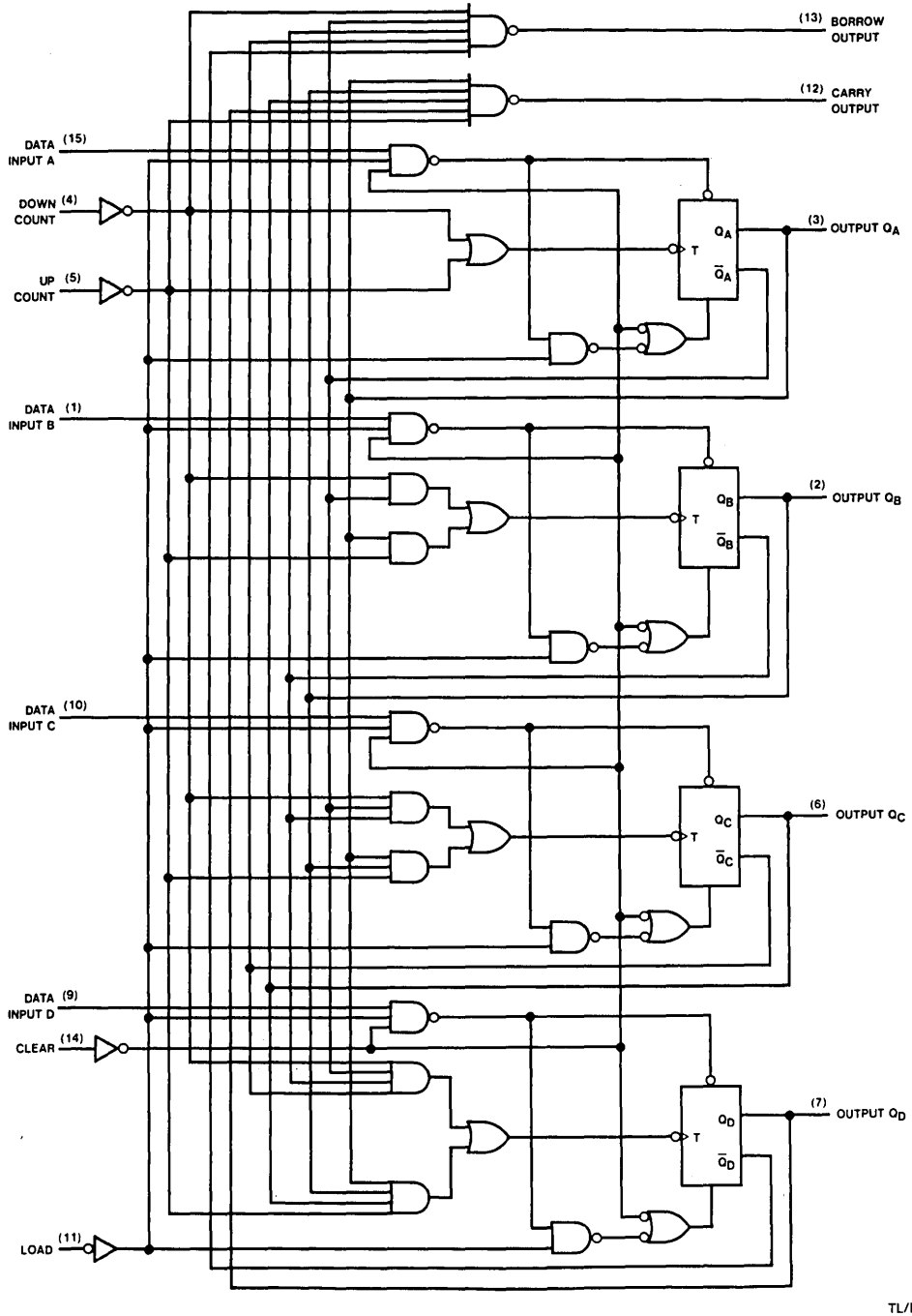


TL/F/6649–2

5

Logic Diagrams (Continued)

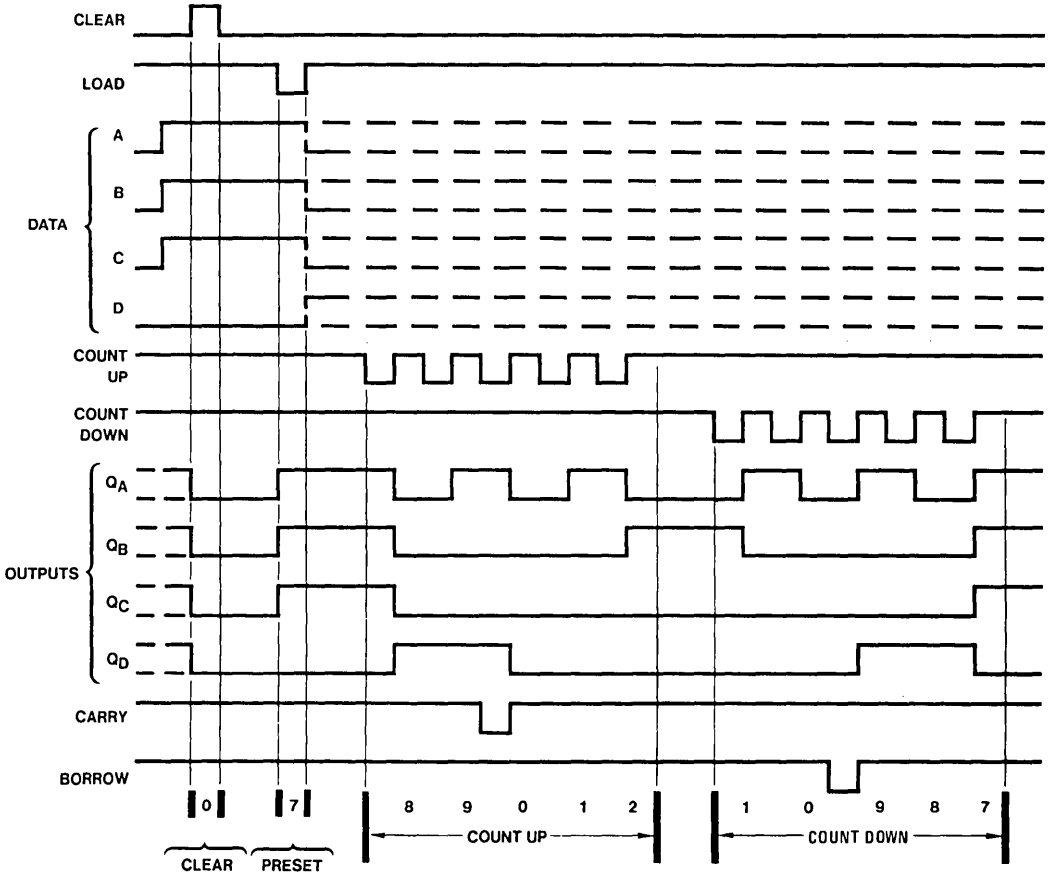
L63



TL/F/6649–3

Timing Diagrams

L60 Decade Counters
Typical Clear, Load and Count Sequences



TL/F/6649–4

Sequence:

(1) Clear outputs to zero.

(2) Load (preset) to BCD seven.

(3) Count up to eight, nine, carry, zero, one, and two.

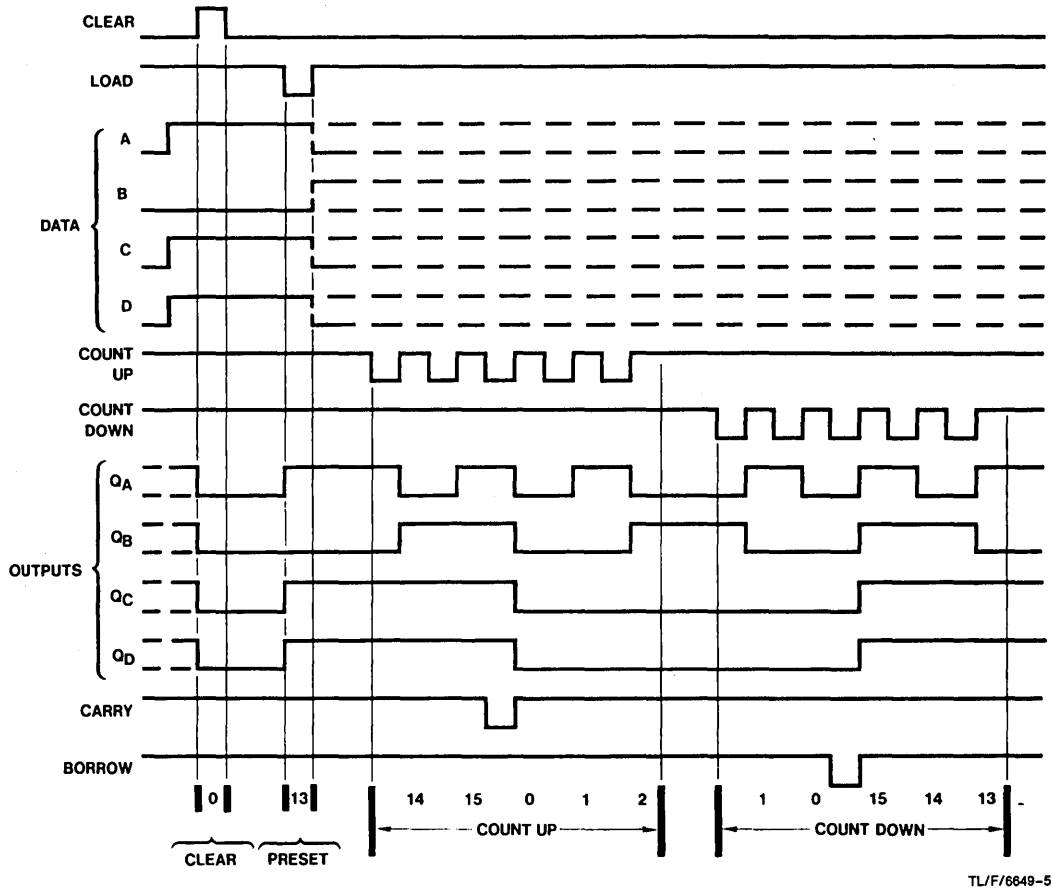
(4) Count down to one, zero, borrow, nine, eight, and seven.

Note A: Clear overrides, load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high

Timing Diagrams (Continued)

L63 Binary Counters
Typical Clear, Load and Count Sequences



TL/F/6649–5

Sequence:

(1) Clear outputs to zero.

(2) Load (preset) to binary thirteen.

(3) Count up to fourteen, fifteen, carry, zero, one, and two.

(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load, data, and count inputs.

Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

National Semiconductor Corporation

DM76L90/DM86L90 8-Bit Parallel In/Serial Out Shift Registers

General Description

These are 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access is made available by eight individual direct data inputs, which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift/load input, regardless of the logic levels on the clock, clock inhibit, or serial inputs.

Features

- Complementary outputs
- Direct overriding load (data) inputs
- Gated clock inputs
- Parallel-to-serial data conversion
- Typical frequency 14 MHz
- Typical power dissipation 80 mW

Absolute Maximum Ratings (Note)

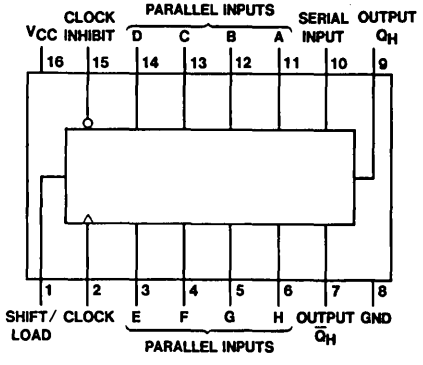
Specifications for Military/Aerospace products are not contained in this datasheet. Refer to the associated reliability electrical test specifications document.

Supply Voltage	8V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54L	−55°C to +125°C
DM74L	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Connection Diagram

Dual-In-Line Package



TL/F/6652–1

Order Number DM76L90J or DM86L90N
See NS Package Number J16A or N16A

Function Table

Inputs					Internal Outputs		Output
Shift/ Load	Clock Inhibit	Clock	Serial	Parallel A...H	Q_A	Q_B	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = High Level (steady state), L = Low Level (steady state)

X = Don't Care (any input, including transitions)

↑ = Transition from low-to-high level

a ... h = The level of steady-state input at inputs A through H, respectively

Q_{A0}, Q_{B0}, Q_{H0} = The level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Gn} = The level of Q_A or Q_G, respectively, before the most recent ↑ transition of the clock.

5

Recommended Operating Conditions

Symbol	Parameter	DM76L90			DM86L90			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage	2			2			V
V_{IL}	Low Level Input Voltage			0.7			0.7	V
I_{OH}	High Level Output Current			−0.2			−0.2	mA
I_{OL}	Low Level Output Current			2			3.6	mA
f_{CLK}	Clock Frequency (Note 1)	0		6	0		6	MHz
t_W	Pulse Width (Clock, Load)(Note 1)	100			100			ns
t_{SU}	Data Setup Time (Note 1)	44	22		44	22		ns
t_H	Data Hold Time (Note 1)	10			10			ns
T_A	Free Air Operating Temperature	−55		125	0		70	°C

Note 1: $T_A = 25°C$ and $V_{CC} = 5V$.

Electrical Characteristics over recommended operating free air temperature (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min I_{OL} = Max V_{IL} = Max V_{IH} = Min	DM76			0.3	V
			DM86			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				0.1	mA
I_{IH}	High Level Input Current	V_{CC} = Max V_I = 2.4V	Load			30	μA
			Others			10	
I_{IL}	Low Level Input Current	V_{CC} = Max V_I = 0.3V	Load			−0.54	mA
			Others			−0.18	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM76	−3		−15	mA
			DM86	−3		−15	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)				9.5	mA

Note 1: All typicals are at $V_{CC} = 5V$, $T_A = 25°C$.

Note 2: Not more than one output should be shorted at a time.

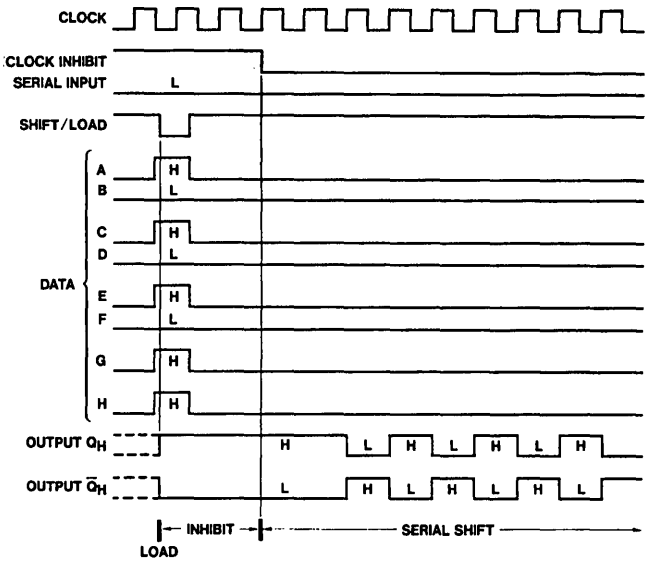
Note 3: With the outputs open, CLOCK INHIBIT and SHIFT/LOAD at 4.5V, and a clock pulse applied to the CLOCK input, I_{CC} is measured first with the parallel inputs at 4.5V, then with them at 0V.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	R_L = 4 kΩ, C_L = 50 pF		Units
			Min	Max	
f_{MAX}	Maximum Clock Frequency		6		ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Load to Any Q		88	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Load to Any Q		124	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Any Q		70	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Any Q		100	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to Q_H		66	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to Q_H		112	ns
t_{PLH}	Propagation Delay Time Low to High Level Output	H to $\overline{Q}_H$		66	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	H to $\overline{Q}_H$		112	ns

Timing Diagram

Typical Shift, Load and Inhibit Sequences



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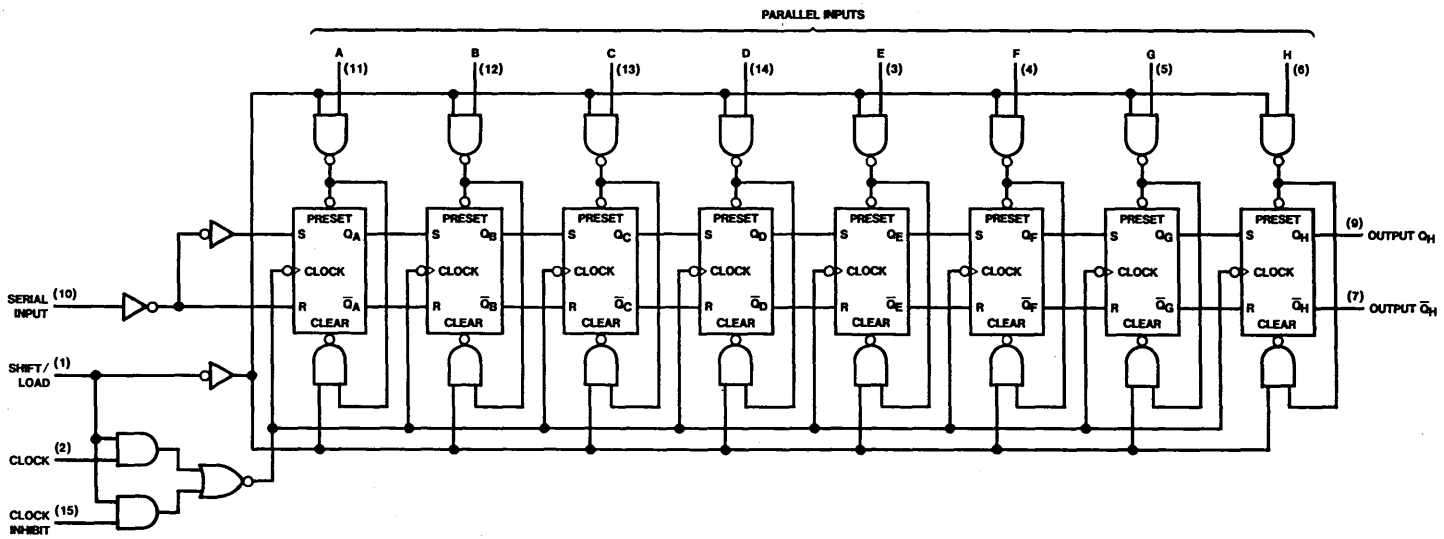
5

Logic Diagram



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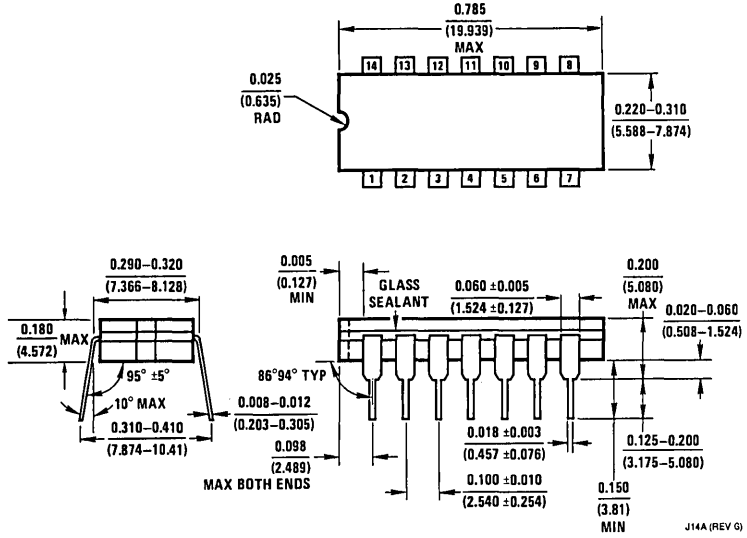
Section 6

Physical Dimensions/ Appendices

Section 6 Contents



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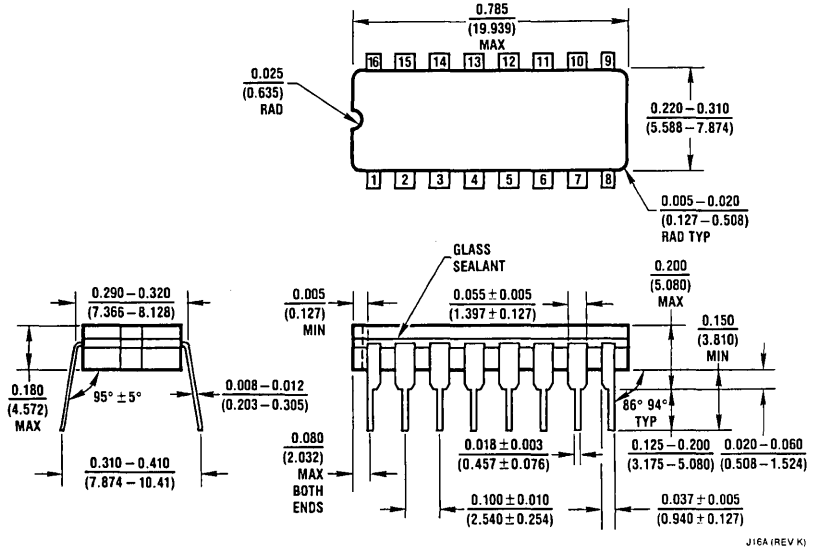

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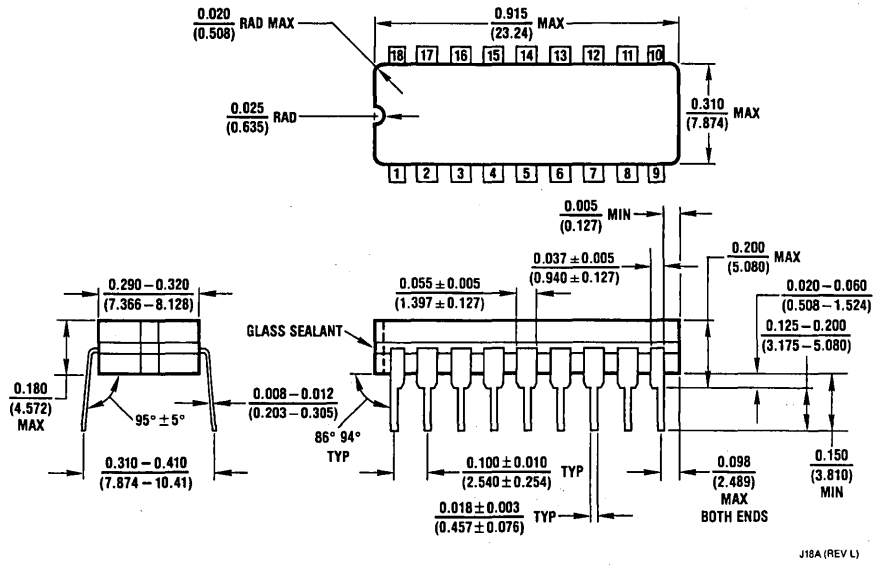

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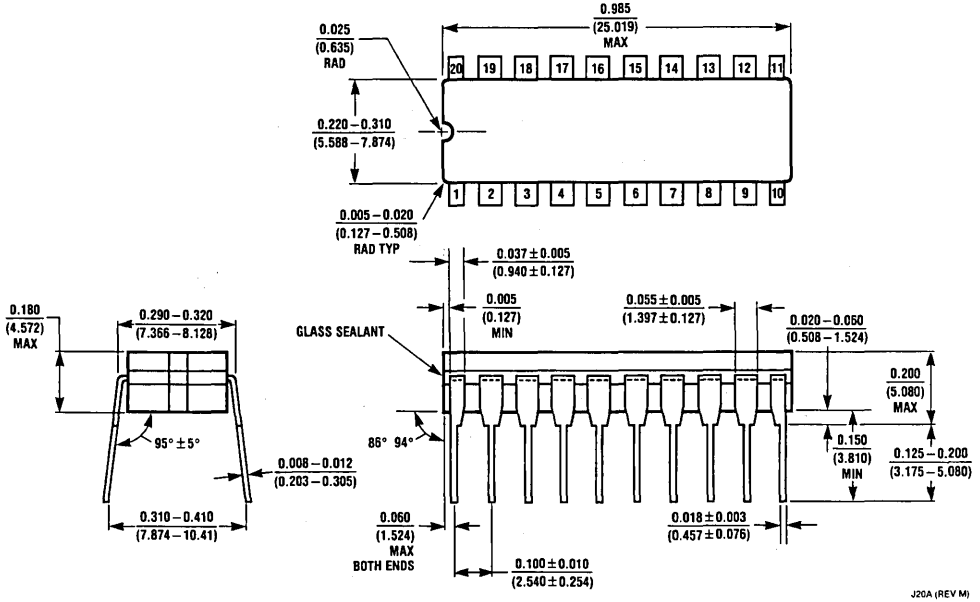

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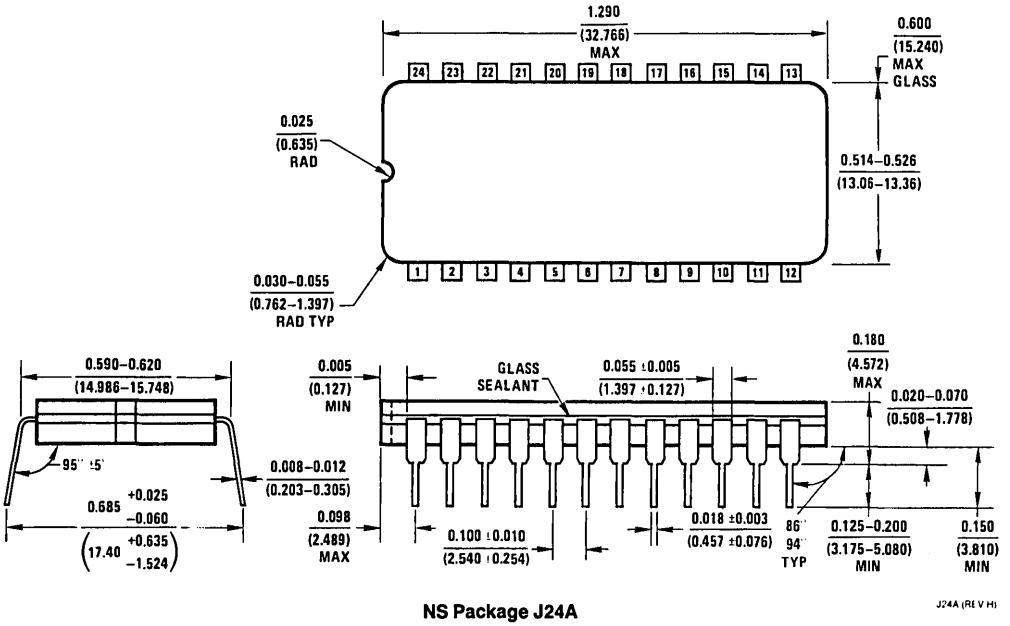

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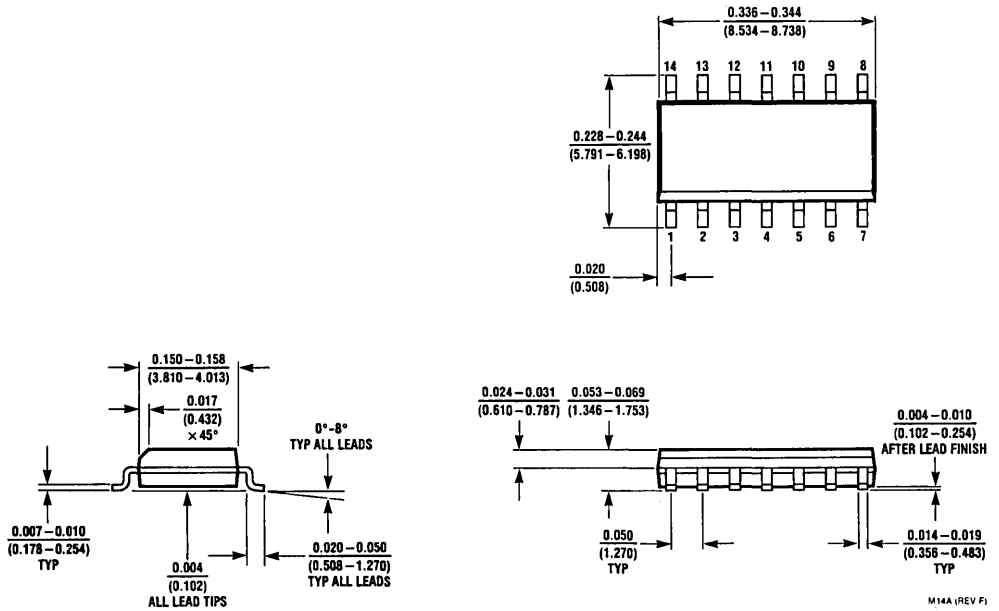

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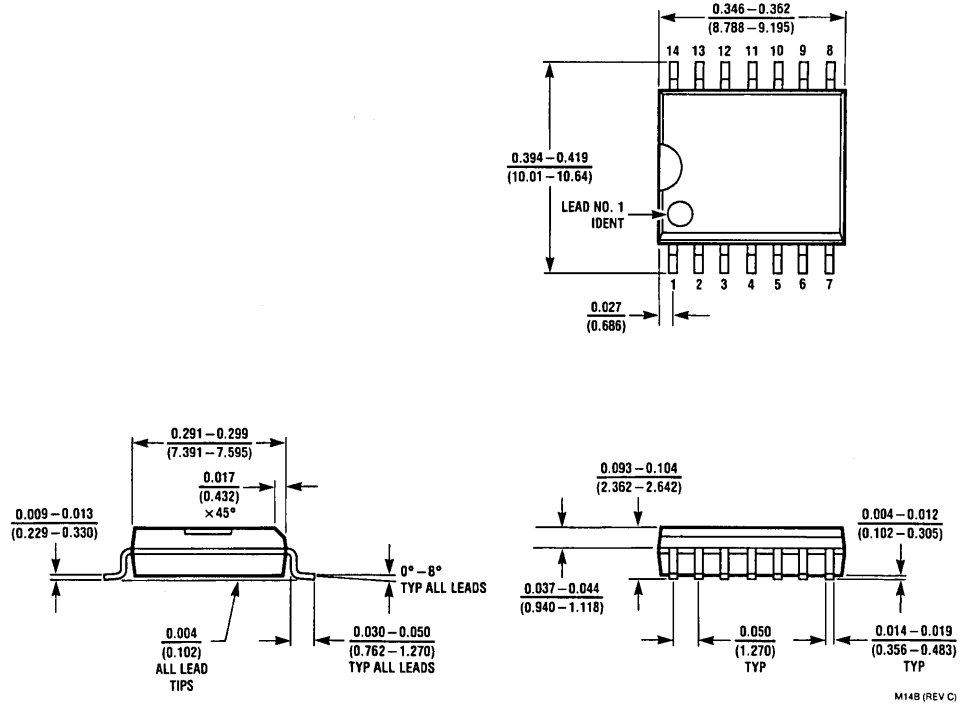

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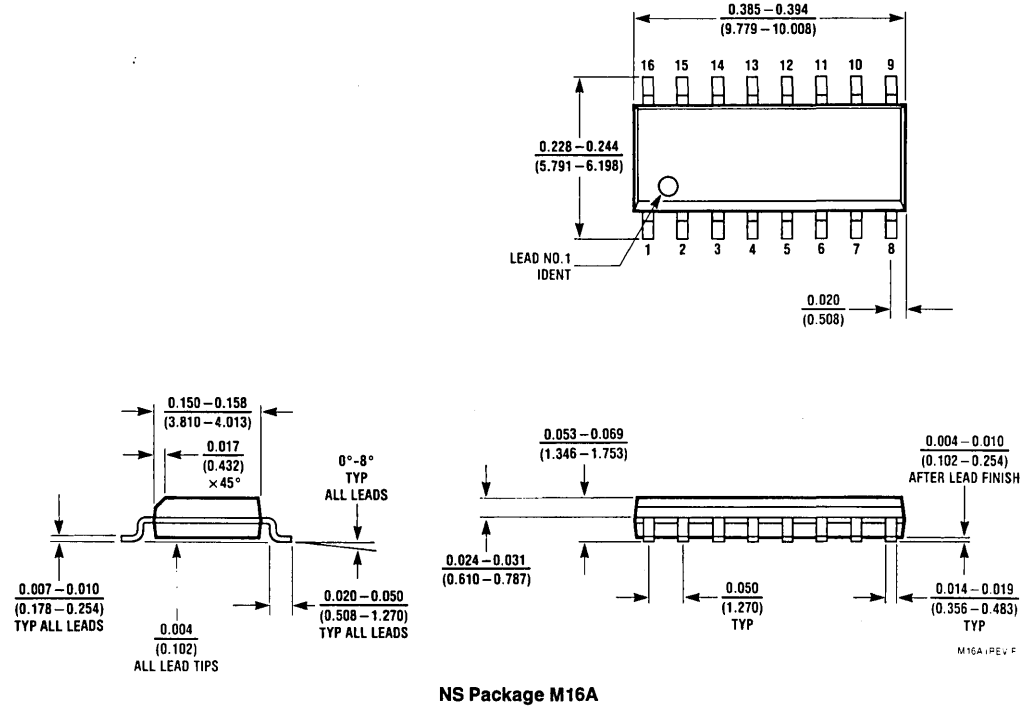

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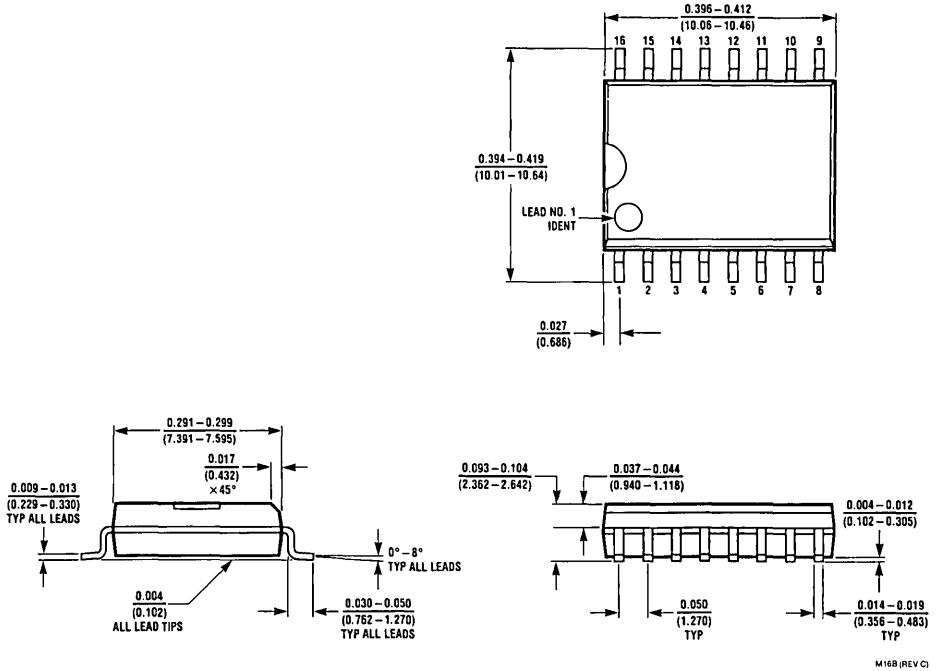

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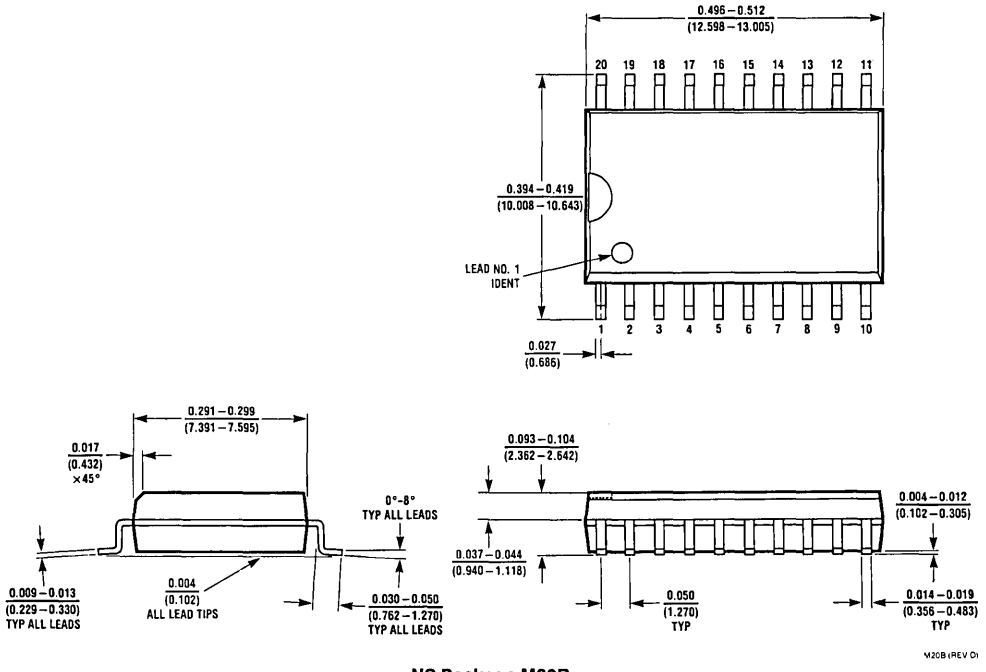

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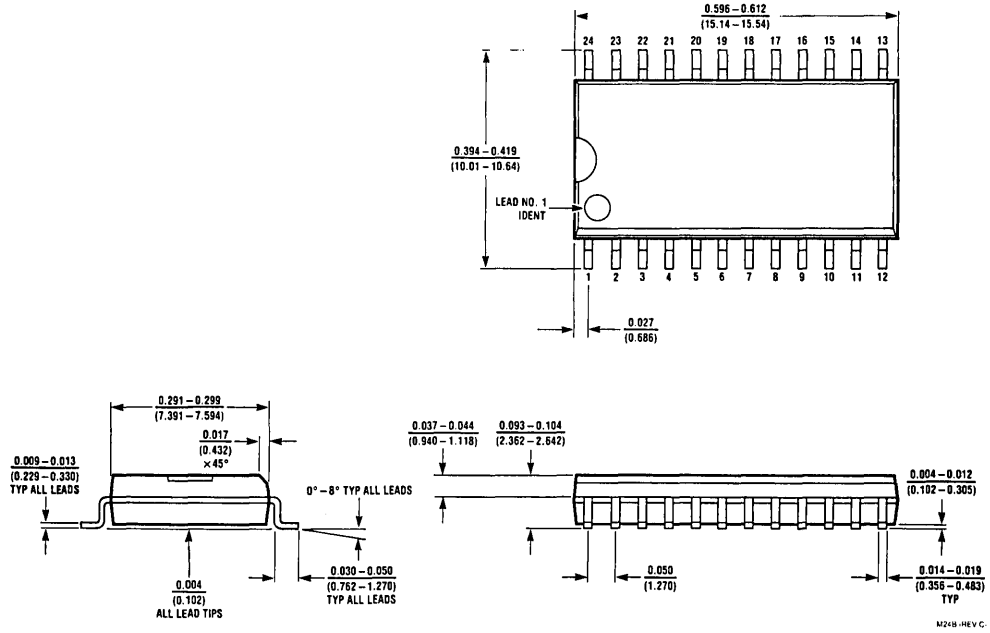

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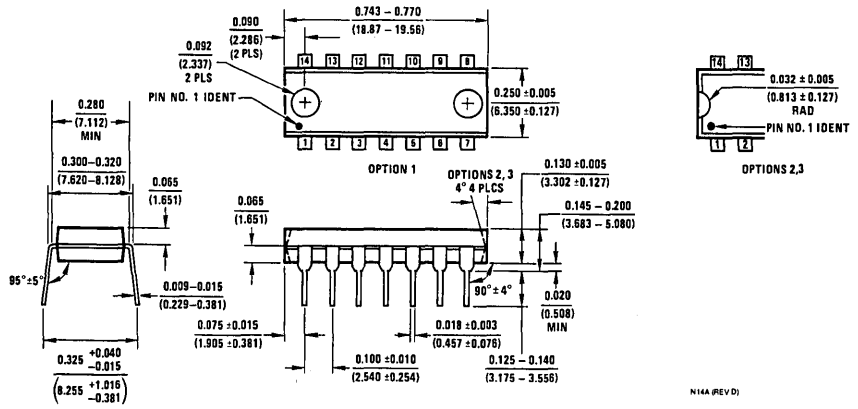

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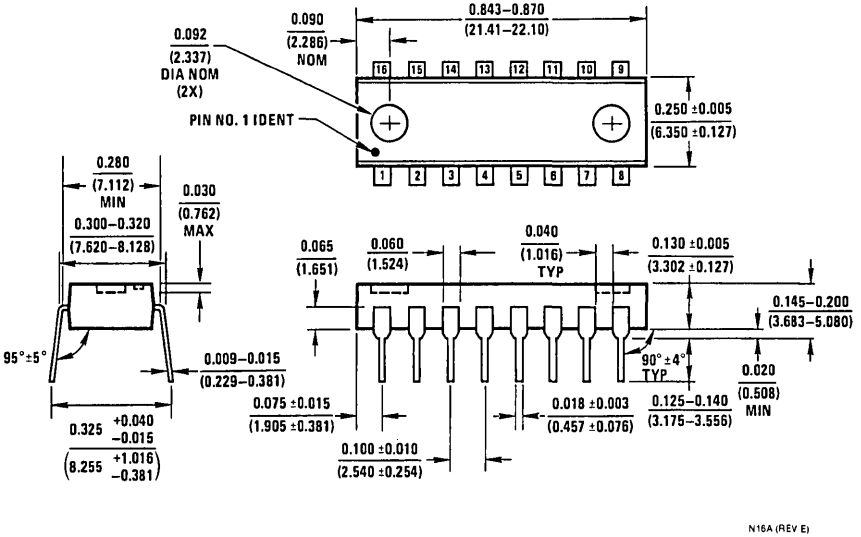

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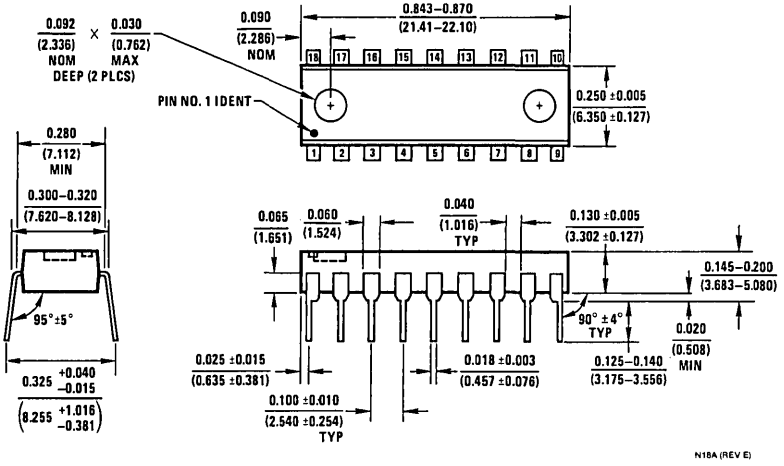

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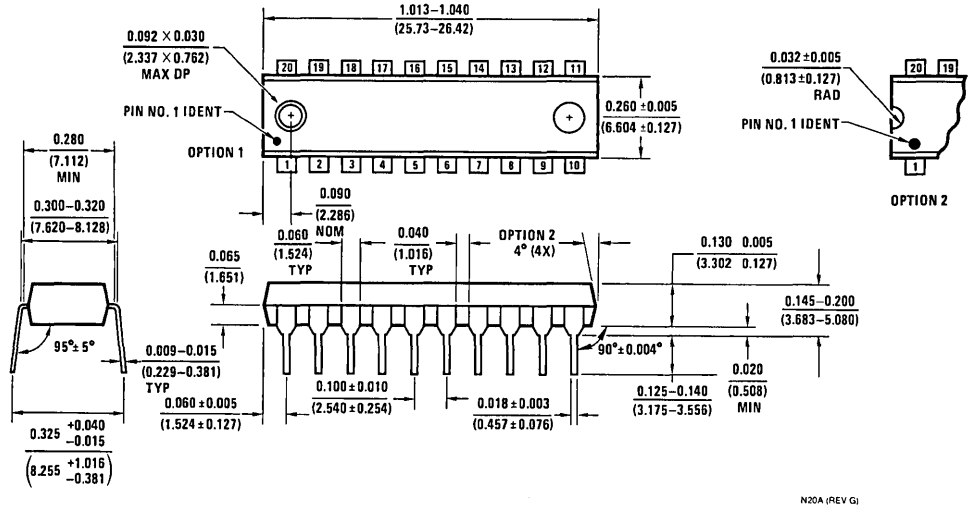

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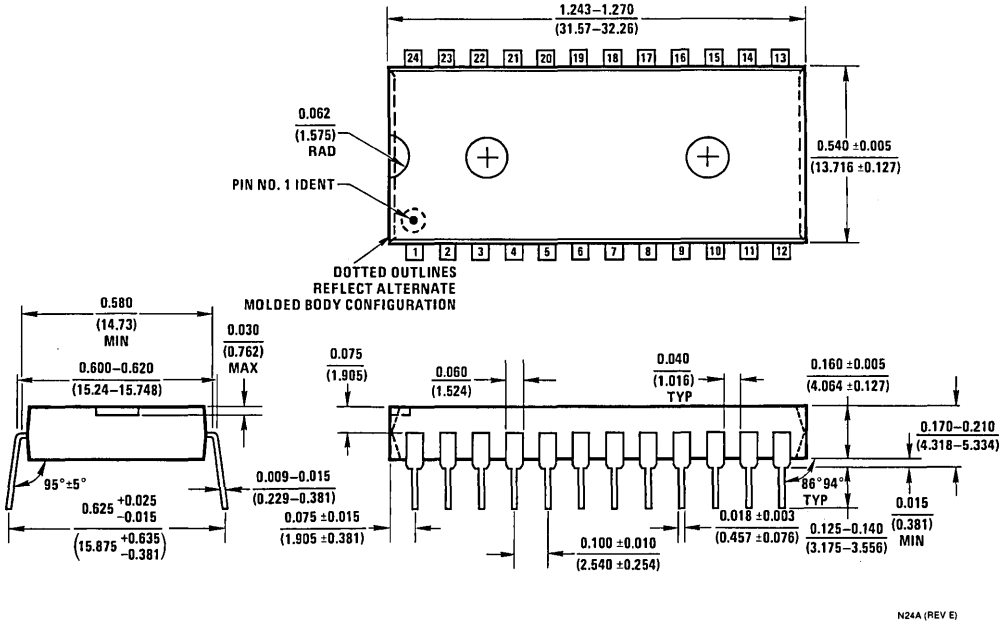

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