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National Semiconductor

Telecommunications Databook

1990
Telecommunications Databook
National Semiconductor

TELECOMMUNICATIONS
DATABOOK

1990 Edition

Line Card Components 1

ISDN Components 2

Analog Telephone Components 3

Application Notes 4

Physical Dimensions/Appendices 5

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Introduction

Welcome to the 1990 Telecommunications Databook. This book is almost twice the size of the previous edition. New products have been added to the line, and the datasheets are more extensive as a result of increasing complexity of the devices. As more system functions are incorporated onto chips and modules, such as those in this databook, more information is required and has been provided in the datasheets as well as in new applications notes to assist the system designer.

For the first time, the Databook includes information on National's Subscriber Line Interface Module, or SLIM™. This module is a masterpiece of linecard design and packaging expertise. It incorporates National's industry-standard CODEC/Filter (COMBO®), a complete SLIC (Subscriber Line Interface Circuit), as well as most of the peripheral and protection circuitry to make a complete subscriber line function. The SLIM, a small 1" x 2" module, has been used as the basis for design of some of the highest performance, most reliable transformerless linecards in the world. Three versions of SLIM are described in this Databook. Additional SLIM modules are in development for different market and customer requirements.

Also new to this databook is the TP3410 "U" Interface device for ISDN applications. This device, a single-chip CMOS implementation of the 2B1Q U Interface Echo Canceller, may be used in any ISDN-related application: linecards, repeaters, network terminators and test equipment. The U Interface is a milestone device in the completion of ISDN networks, and in making end-to-end digital connectivity a reality. The TP3410 may also be used in analog-loop applications such as pairgain, where a high-performance long range transceiver is required.

Starting with the world's first commercially available integrated CMOS CODEC, National has invested for many years in the development of high performance, cost effective solutions for the telecommunications designer. These devices have gone on to become standards in the industry. National has shipped over 50 million CODEC/Filter silicon solutions to telecommunications customers, including over 14 million of the world's first single chip CMOS CODEC/filter, the COMBO, in the past year alone.

With unique experience in mixed mode analog/digital design, standards group participation, sophisticated laboratories and access to a full spectrum of leading edge processes, National's designers will continue to design silicon solutions that meet the needs of telecommunications systems designers all over the world. Customers can count on National's demonstrated track record of quality and reliability for their telecommunications silicon requirements.

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Product Status Definitions

Definition of Terms

Data Sheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data, and supplementary data will be published at a later date. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full Production	This data sheet contains final specifications. National Semiconductor Corporation reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Table of Contents

Alphanumeric Index ix

Section 1 Line Card Components

TP3020, TP3020-1, TP3021, TP3021-1 Monolithic PCM CODECs 1-3
TP3040, TP3040-1, TP3040A, TP3040A-1 PCM Monolithic Filter 1-11
TP3051, TP3056 Parallel Interface CODEC/Filter COMBO 1-19
TP3052, TP3053, TP3054, TP3054-1, TP3057, TP3057-1 "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-29
TP3052-X, TP3054-X, TP3057-X Extended Temperature "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-43
TP3058, TP3059 Microprocessor Compatible COMBO 1-56
TP3064, TP3067 Monolithic Serial Interface CMOS CODEC/Filter COMBO 1-67
TP3068, TP3069 Monolithic Serial Interface CMOS CODEC/Filter COMBO 1-81
TP3070A, TP3071A, TP3070A-X, TP3071A-X COMBO II Programmable PCM CODEC/Filter 1-94
TP3075A, TP3076A COMBO II Programmable PCM CODEC/Filter for ISDN and Digital Phone Applications 1-111
TP3155 Time Slot Assignment Circuit 1-127
TP3200, TP3204 SLIC-MC Magnetic Compensation SLICs 1-135
TP3210 SLIM Subscriber Line Interface Module 1-143
TP3211 SLIM Subscriber Line Interface Module 1-163
TP3212 SLIM Subscriber Line Interface Module 1-181
TP5116A, TP5116A-1, TP5156A, TP5156A-1 Monolithic CODECs 1-202

Section 2 ISDN Components

Introduction to National Semiconductor Basic Access I.C. Set 2-3
TP3401, TP3402, TP3403 DASL Digital Adapter for Subscriber Loops 2-8
TP3410 ISDN Basic Access Echo-Cancelling 2B1Q U Transceiver 2-21
TP3420 ISDN S/T Interface Device 2-51
TP3421 ISDN S/T Interface Device with GCI (General Circuit Interface) 2-69
TP3451 ISDN HDLC and GCI Controller 2-87
TP3460 ISDN R Interface Device USART 2-113
TP34XX MICROWIRE Interface Device (MID) 2-128
HPC16400E High-Performance Communications microController 2-129

Section 3 Analog Telephone Components

TP5088 DTMF Generator for Binary Data 3-3
TP5089 DTMF (Touch-Tone) Generator 3-7
TP5700A Telephone Speech Circuit 3-11

Section 4 Application Notes

AN-336 Understanding Integrated Circuit Package Power Capabilities 4-3
AN-370 Techniques for Designing with CODEC/Filter COMBO Circuits 4-8
AN-439 TP3200 MC-SLIC Application Guide 4-11
AN-466 Improving the Performance of a High Speed PBX Backplane 4-21
AN-492 "Intuitive ISDN"—An ISDN Tutorial 4-26
AN-509 Using the TP3401, TP3402, TP3403 ISDN PBX Transceivers 4-31
AN-520 Building an ISDN Terminal/Terminal Adapter 4-44
AN-614 COMBO II Programmable PCM CODEC/Filter Family Application Guide 4-52
AN-639 High Voltage Protection Techniques with TP3210 Subscriber Line Interface Module 4-69
AN-664 ISDN Basic Rate Interface Terminal Equipment (TE) System Design Guide 4-78
AN-665 TP3420, TP3421 S Interface Device (SID) User's Guide 4-87
Definitions and Timing Conventions 4-129

Table of Contents (Continued)

Section 4 Application Notes (Continued)
ISDN Basic Rate Interface Software for the HPC16400 High Performance Data Communications Microcontroller 4-132
ISDN Glossary of Terms 4-143
Section 5 Physical Dimensions/Appendices
Physical Dimensions 5-3
Bookshelf
Distributors

Alpha-Numeric Index

AN-336 Understanding Integrated Circuit Package Power Capabilities 4-3
AN-370 Techniques for Designing with CODEC/Filter COMBO Circuits 4-8
AN-439 TP3200 MC-SLIC Application Guide 4-11
AN-466 Improving the Performance of a High Speed PBX Backplane 4-21
AN-492 "Intuitive ISDN"—An ISDN Tutorial 4-26
AN-509 Using the TP3401, TP3402, TP3403 ISDN PBX Transceivers 4-31
AN-520 Building an ISDN Terminal/Terminal Adapter 4-44
AN-614 COMBO II Programmable PCM CODEC/Filter Family Application Guide 4-52
AN-639 High Voltage Protection Techniques with TP3210 Subscriber Line Interface Module 4-69
AN-664 ISDN Basic Rate Interface Terminal Equipment (TE) System Design Guide 4-78
AN-665 TP3420, TP3421 S Interface Device (SID) User's Guide 4-87
Definitions and Timing Conventions 4-129
HPC16400E High-Performance Communications microController 2-129
ISDN Basic Rate Interface Software for the HPC16400 High Performance Data Communications Microcontroller 4-132
ISDN Glossary of Terms 4-143
TP34XX MICROWIRE Interface Device (MID) 2-128
TP3020 Monolithic PCM CODEC 1-3
TP3020-1 Monolithic PCM CODEC 1-3
TP3021 Monolithic PCM CODEC 1-3
TP3021-1 Monolithic PCM CODEC 1-3
TP3040 PCM Monolithic Filter 1-11
TP3040-1 PCM Monolithic Filter 1-11
TP3040A PCM Monolithic Filter 1-11
TP3040A-1 PCM Monolithic Filter 1-11
TP3051 Parallel Interface CODEC/Filter COMBO 1-19
TP3052 "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-29
TP3052-X Extended Temperature "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-43
TP3053 "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-29
TP3054 "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-29
TP3054-1 "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-29
TP3054-X Extended Temperature "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-43
TP3056 Parallel Interface CODEC/Filter COMBO 1-19
TP3057 "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-29
TP3057-1 "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-29
TP3057-X Extended Temperature "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-43
TP3058 Microprocessor Compatible COMBO 1-56
TP3059 Microprocessor Compatible COMBO 1-56
TP3064 Monolithic Serial Interface CMOS CODEC/Filter COMBO 1-67
TP3067 Monolithic Serial Interface CMOS CODEC/Filter COMBO 1-67
TP3068 Monolithic Serial Interface CMOS CODEC/Filter COMBO 1-81
TP3069 Monolithic Serial Interface CMOS CODEC/Filter COMBO 1-81
TP3070A COMBO II Programmable PCM CODEC/Filter 1-94
TP3070A-X COMBO II Programmable PCM CODEC/Filter 1-94
TP3071A COMBO II Programmable PCM CODEC/Filter 1-94
TP3071A-X COMBO II Programmable PCM CODEC/Filter 1-94
TP3075A COMBO II Programmable PCM CODEC/Filter for ISDN and Digital Phone Applications .. 1-111
TP3076A COMBO II Programmable PCM CODEC/Filter for ISDN and Digital Phone Applications .. 1-111
TP3155 Time Slot Assignment Circuit 1-127
TP3200 SLIC-MC Magnetic Compensation SLIC 1-135
TP3204 SLIC-MC Magnetic Compensation SLIC 1-135

Alpha-Numeric Index (Continued)

TP3210 SLIM Subscriber Line Interface Module 1-143
TP3211 SLIM Subscriber Line Interface Module 1-163
TP3212 SLIM Subscriber Line Interface Module 1-181
TP3401 DASL Digital Adapter for Subscriber Loops 2-8
TP3402 DASL Digital Adapter for Subscriber Loops 2-8
TP3403 DASL Digital Adapter for Subscriber Loops 2-8
TP3410 ISDN Basic Access Echo-Cancelling 2B1Q U Transceiver 2-21
TP3420 ISDN S/T Interface Device 2-51
TP3421 ISDN S/T Interface Device with GCI (General Circuit Interface) 2-69
TP3451 ISDN HDLC and GCI Controller 2-87
TP3460 ISDN R Interface Device USART 2-113
TP5088 DTMF Generator for Binary Data 3-3
TP5089 DTMF (Touch-Tone) Generator 3-7
TP5116A Monolithic CODEC 1-202
TP5116A-1 Monolithic CODEC 1-202
TP5156A Monolithic CODEC 1-202
TP5156A-1 Monolithic CODEC 1-202
TP5700A Telephone Speech Circuit 3-11

Section 1

Line Card Components

Section 1 Contents

TP3020, TP3020-1, TP3021, TP3021-1 Monolithic PCM CODECs 1-3
TP3040, TP3040-1, TP3040A, TP3040A-1 PCM Monolithic Filter 1-11
TP3051, TP3056 Parallel Interface CODEC/Filter COMBO 1-19
TP3052, TP3053, TP3054, TP3054-1, TP3057, TP3057-1 "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-29
TP3052-X, TP3054-X, TP3057-X Extended Temperature "Ruggedized" Serial Interface CODEC/Filter COMBO Family 1-43
TP3058, TP3059 Microprocessor Compatible COMBO 1-56
TP3064, TP3067 Monolithic Serial Interface CMOS CODEC/Filter COMBO 1-67
TP3068, TP3069 Monolithic Serial Interface CMOS CODEC/Filter COMBO 1-81
TP3070A, TP3071A, TP3070A-X, TP3071A-X COMBO II Programmable PCM CODEC/Filter . 1-94
TP3075A, TP3076A COMBO II Programmable PCM CODEC/Filter for ISDN and Digital Phone Applications 1-111
TP3155 Time Slot Assignment Circuit 1-127
TP3200, TP3204 SLIC-MC Magnetic Compensation SLICs 1-135
TP3210 SLIM Subscriber Line Interface Module 1-143
TP3211 SLIM Subscriber Line Interface Module 1-163
TP3212 SLIM Subscriber Line Interface Module 1-181
TP5116A, TP5116A-1, TP5156A, TP5156A-1 Monolithic CODECs 1-202

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TP3020, TP3020-1, TP3021, TP3021-1 Monolithic CODECs

General Description

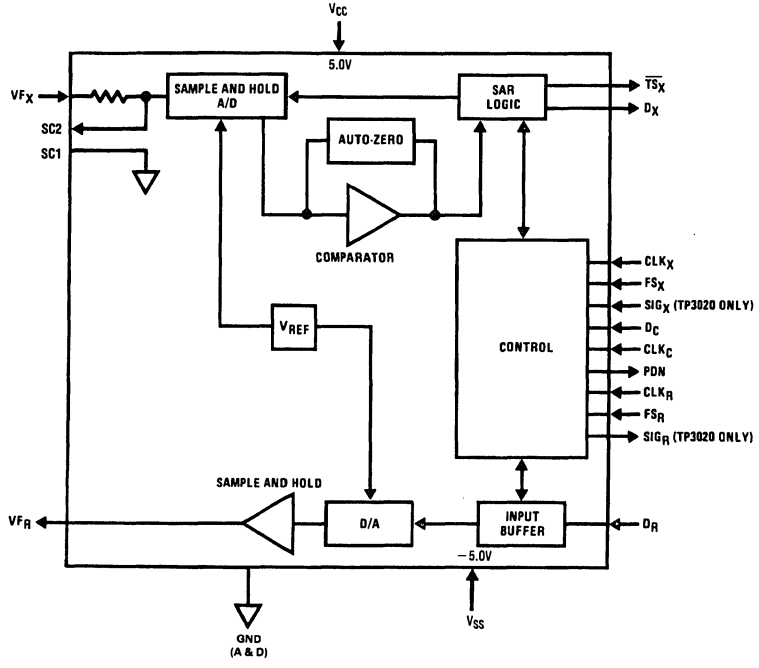
The TP3020 and TP3021 are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP3020 is intended for μ-law applications and contains logic for μ-law signaling insertion and extraction. The TP3021 is intended for A-law applications.

Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the TP3020/TP3021 may be operated in a fixed time slot mode. Both devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- Low operation power—45 mW typical
- Low standby power—1 mW typical
- ±5V operation
- TTL compatible digital interface
- Time slot assignment or alternate fixed time slot modes
- Internal precision reference
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP3020—μ-law coding with signaling capabilities
- TP3021—A-law coding
- Synchronous or asynchronous operation

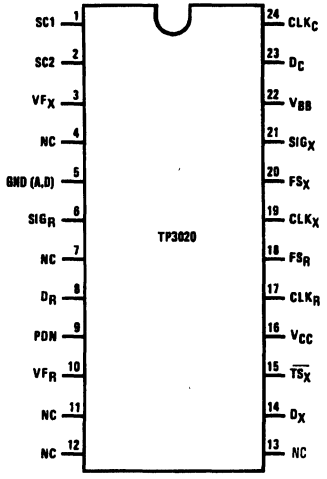
Simplified Block Diagram



TL/H/5538–1

Connection Diagrams

Dual-In-Line Package

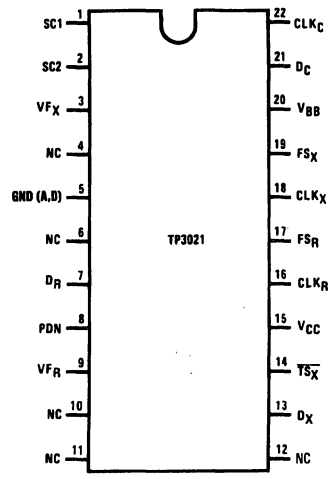


TL/H/5538–3

Top View

Order Number TP3020J or TP3020J-1
See NS Package Number J24A

Dual-In-Line Package



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Top View

Order Number TP3021J or TP3021J-1
See NS Package Number J22A

Description of Pin Functions

Symbol	Function
SC1	Internally connected to GNDA.
SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatibility.
VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
GND	Analog and digital ground. All analog and digital signals are referenced to this pin.
SIG_R	Receive signaling bit output. During receive signaling frames the least significant (last) bit shifted into D_R is internally latched and appears at this output—SIG_R will then remain valid until changed during a subsequent receive signaling frame or reset by a power-down command.
D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel.
VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μS after the end of the decode time slot.

Symbol	Function
NC	Unused
D_X	Serial PCM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
V_{CC}	5V (±5%) Power Supply.
CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MH_z, 1.544 MH_z or 2048 MHz. May be asynchronous with CLK_X or CLK_C.
FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.

Description of Pin Functions (Continued)

Symbol	Function
SIG_X	Transmit signaling input. During a transmit signaling frame, the signal at SIG_X is shifted out of D_X in place of the least significant (last) bit of PCM data.
V_{BB}	−5V (±5%) input.
D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3020/TP3021 into the fixed time slot mode.

Absolute Maximum Ratings

Operating Temperature	−25°C to + 125°C
Storage Temperature	−65°C to + 150°C
V_{CC} with Respect to GND	7V
V_{BB} with Respect to GND	−7V
ESD rating is to be determined.	
Voltage at Any Analog Input or Output	V_{BB} −0.3V to V_{CC} + 0.3V
Voltage at Any Digital Input or Output	GND −0.3V to V_{CC} + 0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V and T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0<V_{IN}<V_{CC}$	**−10**		**10**	μA
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_{OL}=4.0 mA			**0.4**	V
		SIG_R, I_{OL}=0.5 mA			**0.4**	V
		$\overline{TS}_X$, I_{OL}=3.2 mA, Open Drain			**0.4**	V
		PDN, I_{OL}=1.6 mA			**0.4**	V
V_{OH}	Output High Voltage	D_X, I_{OH}=6 mA	**2.4**			V
		SIG_R, I_{OH}=0.6 mA	**2.4**			V
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2.0			kΩ
Z_O	Output Impedance at VF_R	$-3.1V<VF_R<3.1V$		10	20	Ω
V_{OS}	Output Offset Voltage at VF_R	D_R=PCM Zero Code (TP3020) or Alternating ± 1 Code (TP3021)	**−25**		**25**	mV
I_{IN}	Analog Input Bias Current	V_{IN}=0V	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				160	kΩ
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}			0.1	**0.4**	mA
I_{BB0}	Standby Current, V_{BB}			0.03	**0.1**	mA
I_{CC1}	Operating Current, V_{CC}			4.5	**8.0**	mA
I_{BB1}	Operating Current, V_{BB}			4.5	**8.0**	mA

AC Electrical Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected. Limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP3020 and TP3021 are 1.520 Vrms and 1.525 Vrms respectively. The resulting nominal overload level is 3.096V peak for both devices. All gain measurements for the encode and decode portions of the TP3020/TP3021 are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute TP3020, TP3021 TP3020-1, TP3021-1	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	 **−0.125** **−0.175**		 **0.125** **0.175**	 dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%	**−0.07**		**0.07**	dB
G_{XA}	Transmit Gain, Absolute TP3020, TP3021 TP3020-1, TP3021-1	T = 25°C, V_{CC} = 5V, V_{BB} = −5V	 **−0.325** **−0.375**		 **−0.075** **−0.025**	 dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T = 0°C to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%	**−0.07**		**0.07**	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−1.0**		 **0.3** **0.2** **0.4** **1.0**	 dB dB dB dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−1.0**		 **0.3** **0.2** **0.4** **1.0**	 dB dB dB dB
S/D_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBc dBc dBc
S/D_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBc dBc dBc
N_R	Receive Idle Channel Noise	D_R = Steady State PCM Code			**6**	dBrnc0
N_X	Transmit Idle Channel Noise	TP3020, (No Signaling) TP3021 (Note 1)			**13** **−66***	dBrnc0 dBn0p
HD_R	Receive Harmonic Distortion	2nd or 3rd Harmonic			**−47**	dB
HD_X	Transmit Harmonic Distortion	2nd or 3rd Harmonic			**−47**	dB
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, V_{CC} = 5.0 V_{DC} +300 mVrms, f = 1.02 kHz	**50**			dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0 level.

AC Electrical Characteristics (Continued)

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected. Limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{CC} = 5.0 V_{DC} + 300 mVrms, F = 1.02 kHz	**40**			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**50**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = = 1.02 kHz	**45**			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			**−75**	dB
CT_{RX}	Receive to Transmit Crosstalk	Transmit Input Level = 0V TP3020 TP3021			**−70** **−65** (Note 2)	dB dB

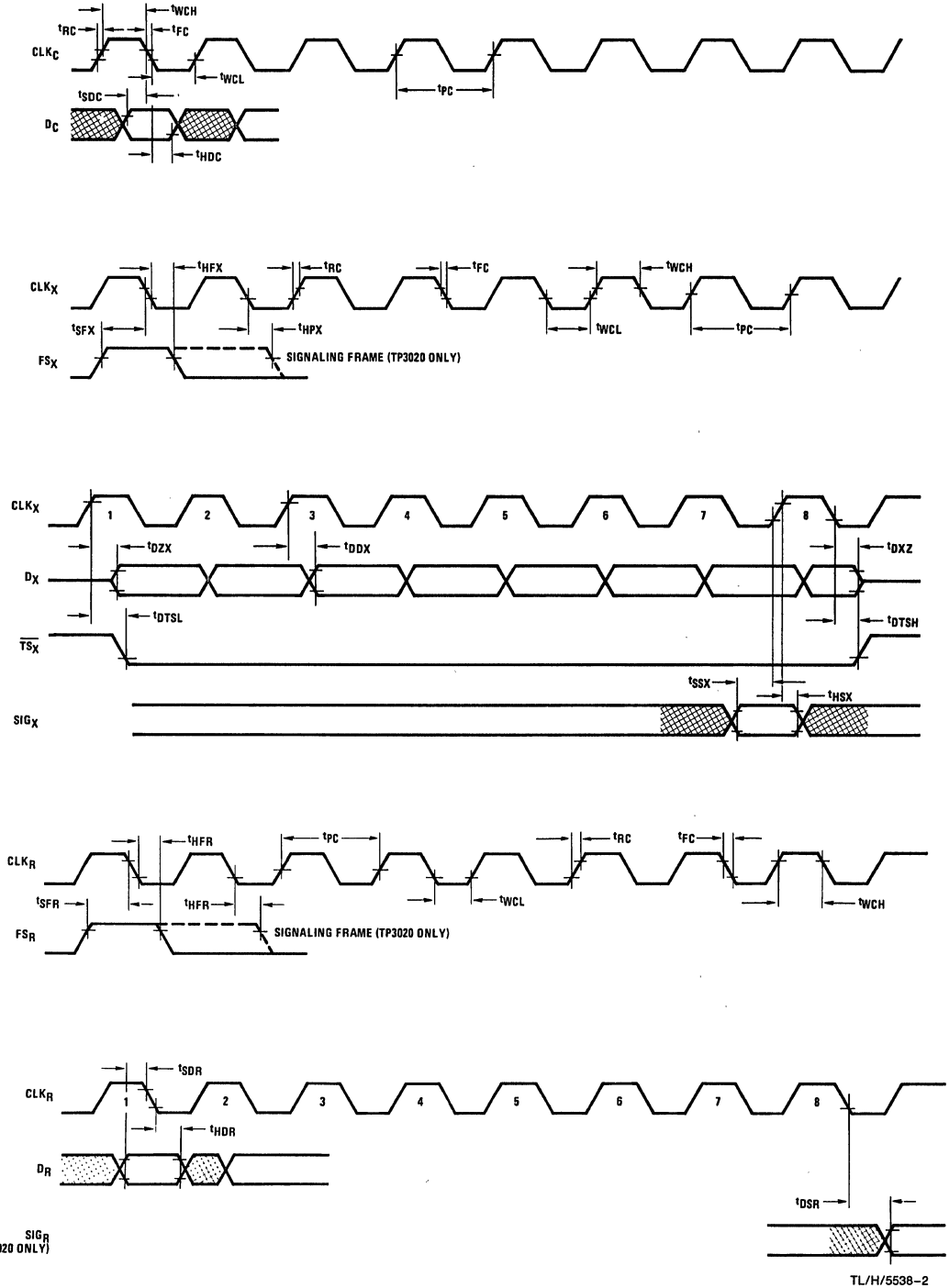
Note 2: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Timing Specification

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All digital signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PC}	Period of Clock	CLK_C, CLK_R, CLK_X	**485**			ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	CLK_C, CLK_R, CLK_X			30	ns
t_{WCH}	Width of Clock High	CLK_C, CLK_R, CLK_X	**165**			ns
t_{WCL}	Width of Clock Low	CLK_C, CLK_R, CLK_X	**165**			ns
$t_{A/D}$	A/D Conversion Time	From End of Encoder Time Slot to Completion of Conversion			**16**	Time Slots
$t_{D/A}$	D/A Conversion Time	From End of Decoder Time Slot to Transition of VF_R			**2**	Time Slots
t_{SDC}	Set-Up Time, D_C to CLK_C		**100**			ns
t_{HDC}	Hold Time, CLK_C to DC		**100**			ns
t_{SFX}	Set-Up Time, FS_X to CLK_X		**100**			ns
t_{HFX}	Hold Time, CLK_X to FS_X		**100**			ns
t_{DZX}	Delay Time to Enable D_X on TS Entry	C_L = 150 pF	25		125	ns
t_{DDX}	Delay Time, CLK_X to D_X	C_L = 150 pF			**125**	ns
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	C_L = 0 pF	50		165	ns
t_{DTSL}	Delay to $\overline{TS}_X$ Low	0 ≤ C_L ≤ 150 pF	30		185	ns
t_{DTSH}	Delay to $\overline{TS}_X$ Off	C_L = 0 pF	30		185	ns
t_{SSX}	Set-Up Time, SIG_X to CLK_X		**100**			ns
t_{HSX}	Hold Time, CLK_X to SIG_X		**100**			ns
t_{SFR}	Set-Up Time, FS_R to CLK_R		**100**			ns
t_{HFR}	Hold Time, CLK_R to FS_R		**100**			ns
t_{SDR}	Set-Up Time, D_R to CLK_R		**40**			ns
t_{HDR}	Hold Time, CLK_R to D_R		**30**			ns
t_{DSR}	Delay Time, CLK_R to SIG_R	C_L = 100 pF			300	ns

Timing Waveforms



TL/H/5538–2

Functional Description

POWER-UP

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or −5V is required. In the power-down mode, all non-essential circuits are deactivated, the TRI-STATE PCM data output D_X is placed in the high impedance state and the receive signaling output of the TP3020, SIG_R, is reset to logical zero. Once in the power-down mode, the method of activating the TP3020/TP3021 depends on the chosen mode of operation, time slot assignment or fixed time slot.

TIME SLOT ASSIGNMENT MODE

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μS or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequent control bits B3−B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputted during the previously assigned time slot which may now be assigned to another CODEC.

FIXED TIME SLOT MODE

There are several ways in which the TP3020/TP3021 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

SERIAL CONTROL PORT

When the TP3020/TP3021 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	Action
0	0	Assign time slot to encoder and decoder
0	1	Assign time slot to encoder
1	0	Assign time slot to decoder
1	1	Power-down CODEC

B3	B4	B5	B6	B7	B8	Time Slot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

SIGNALING

The TP3020 μ-law CODEC contains circuitry to insert and extract signaling information for the PCM data. The transmit signaling frame is signified by widening the FS_X pulse from one cycle of CLK_X to two or more cycles.

When this occurs, the data present on the SIG_X input at the eighth clock pulse of the encode time slot is inserted into the last bit of the PCM data stream. A receive signaling frame is indicated in a similar fashion by widening the FS_R pulse to two or more cycles of CLK_R.

During a receive signaling frame, the last PCM bit shifted in is latched into a flip-flop and appears at the SIG_R output. This output will remain unchanged until the next signaling frame, until a power-down is executed or until power is removed from the device. Since the least significant bit of the PCM data is lost during a signaling frame, the decoder interprets the bit as a "½" (i.e., half way between a "0" and a "1"). This minimizes the noise and distortion due to the signaling.

Functional Description (Continued)

ENCODING DELAY

The encoding process begins at the start of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μS later, resulting in an encoding delay of 125 μS. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz clock, the FS rate could be increased to 15 kHz reducing the delay from 125 μS to 67 μS.

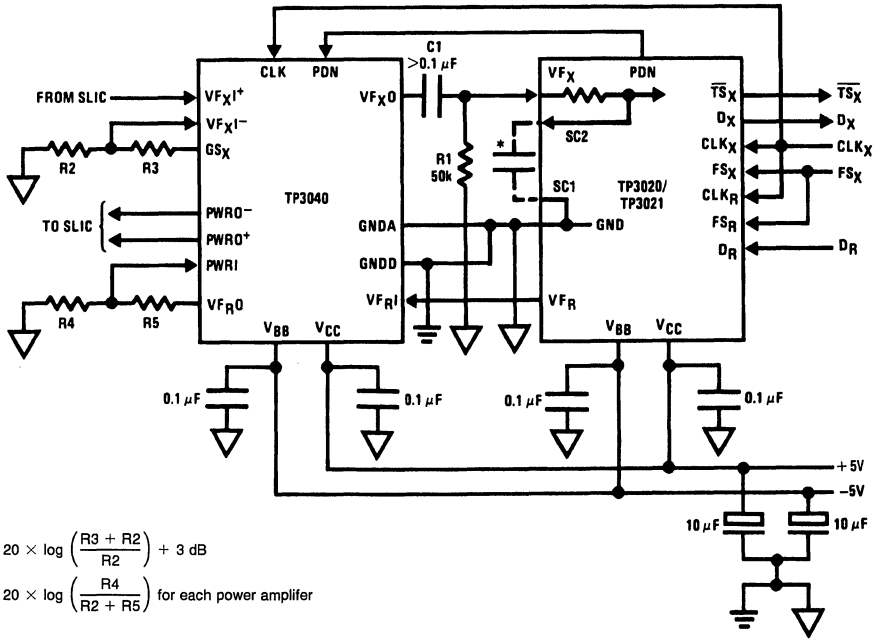
DECODING DELAY

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81 μS for a 1.544 MHz system with an 8 kHz frame rate or 76 μS for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

TYPICAL APPLICATION

A typical application of the TP3020/TP3021 used in conjunction with the TP3040 PCM filter is shown. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should not exceed 160 kΩ, and the product R1 × C1 should exceed 4 rms. 0.1 μf power supply bypass capacitors should be used and placed as close to the device as possible.

Typical Application



$$\text{XMT gain} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\ \text{dB}$$

$$\text{RCV gain} = 20 \times \log\left(\frac{R4}{R2 + R5}\right) \text{ for each power amplifer}$$

TL/H/5538–5

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of the TP3020/TP3021/TP3040, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

*The external sample/hold capacitor required for use with pin-compatible NMOS CODECs introduces attenuation due to the capacitive divider formed with C1. The SC pin connects VF_X to this sample/hold capacitor (via a 300Ω resistor) to ensure gain compatibility. The TP3020/TP3021 itself does not require an external sample/hold capacitor.

National Semiconductor

TP3040, TP3040-1, TP3040A, TP3040A-1 PCM Monolithic Filter

General Description

The TP3040/TP3040-1/TP3040A/TP3040A-1 filter is a monolithic circuit containing both transmit and receive filters specifically designed for PCM CODEC filtering applications in 8 kHz sampled systems.

The filter is manufactured using microCMOS technology and switched capacitor integrators are used to simulate classical LC ladder filters which exhibit low component sensitivity.

TRANSMIT FILTER STAGE

The transmit filter is a fifth order elliptic low pass filter in series with a fourth order Chebyshev high pass filter. It provides a flat response in the passband and rejection of signals below 200 Hz and above 3.4 kHz.

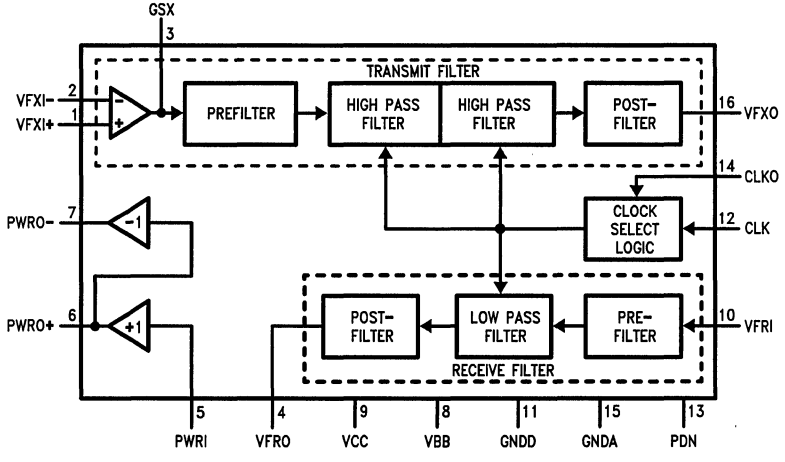
RECEIVE FILTER STAGE

The receive filter is a fifth order elliptic low pass filter designed to reconstruct the voice signal from the decoded/demultiplexed signal which, as a result of the sampling process, is a stair-step signal having the inherent sin x/x frequency response. The receive filter approximates the function required to compensate for the degraded frequency response and restore the flat passband response.

Features

- Exceeds all D3/D4 and CCITT specifications
- +5V, −5V power supplies
- Low power consumption:
  45 mW (0 dBm0 into 600Ω)
  30 mW (power amps disabled)
- Power down mode: 0.5 mW
- 20 dB gain adjust range
- No external anti-aliasing components
- Sin x/x correction in receive filter
- 50/60 Hz rejection in transmit filter
- TTL and CMOS compatible logic
- All inputs protected against static discharge due to handling

Block Diagram



TL/H/6660–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltages	±7V
Power Dissipation	1 W/Package
Input Voltage	±7V
Voltage at Any Input or Output	V_{CC} + 0.3V to V_{BBV} − 0.3V
Output Short-Circuit Duration	Continuous
Operating Temperature Range	−25°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating to be determined	

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C. Clock frequency is 2.048 MHz. Digital interface voltages measured with respect to digital ground, GNDD. Analog voltages measured with respect to analog ground, GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION						
I_{CC0}	V_{CC} Standby Current	V_{CC} = 5.25V, V_{BB} = −5.25V, CLK0 and PWRI = −5.25V (Note 6) All other pins at GND (0V)				
		TP3040, TP3040A		50	**100**	µA
		TP3040-1, TP3040A-1			**400**	µA
I_{BB0}	V_{BB} Standby Current	V_{CC} = 5.25V, V_{BB} = −5.25V, CLK0 and PWRI = −5.25V (Note 6) All other pins at GND (0V)				
		TP3040, TP3040A		50	**100**	µA
		TP3040-1, TP3040A-1			**400**	µA
I_{CC1}	V_{CC} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	**4.0**	mA
I_{BB1}	V_{BB} Operating Current	PWRI = V_{BB}, Power Amp Inactive		3.0	**4.0**	mA
I_{CC2}	V_{CC} Operating Current	(Note 1)		4.6	**6.4**	mA
I_{BB2}	V_{BB} Operating Current	(Note 1)		4.6	**6.4**	mA
DIGITAL INTERFACE						
I_{INC}	Input Current, CLK	$V_{BB} \le V_{IN} \le V_{CC}$	**−10**		**10**	µA
I_{INP}	Input Current, PDN	$V_{BB} \le V_{IN} \le V_{CC}$	**−100**			µA
I_{IN0}	Input Current, CLK0	$V_{BB} \le V_{IN} \le V_{CC}$ − 0.5V	**−10**		**−0.1**	µA
V_{IL}	Input Low Voltage, CLK, PDN		0		**0.8**	V
V_{IH}	Input High Voltage, CLK, PDN		**2.2**		V_{CC}	V
V_{IL0}	Input Low Voltage, CLK0		V_{BB}		V_{BB}+0.5	V
V_{II0}	Input Intermediate Voltage, CLK0		−0.8		0.8	V
V_{IH0}	Input High Voltage, CLK0		V_{CC}−0.5		V_{CC}	V
TRANSMIT INPUT OP AMP						
$IB_X I$	Input Leakage Current, $VF_X I$	−3.2V ≤ V_{IN} ≤ +3.2V	**−100**		**100**	nA
$RI_X I$	Input Resistance, $VF_X I$	$V_{BB} \le VF_X I \le V_{CC}$	10			MΩ
$VOS_X I$	Input Offset Voltage, $VF_X I$	−2.5V ≤ V_{IN} ≤ +2.5V	**−20**		**20**	mV
V_{CM}	Common-Mode Range, $VF_X I$		**−2.5**		**2.5**	V
CMRR	Common-Mode Rejection Ratio	−2.5V ≤ V_{IN} ≤ 2.5V	**60**			dB
PSRR	Power Supply Rejection of V_{CC} or V_{BB}		**60**			dB
R_{OL}	Open Loop Output Resistance, GS_X			1		kΩ
R_L	Minimum Load Resistance, GS_X		10			kΩ
C_L	Maximum Load Capacitance, GS_X				100	pF
$VO_X I$	Output Voltage Swing, GS_X	$R_L \ge$ 10k	**±2.5**			V
A_{VOL}	Open Loop Voltage Gain, GS_X	$R_L \ge$ 10k	**5,000**			V/V
F_C	Open Loop Unity Gain Bandwidth, GS_X			2		MHz

AC Electrical Characteristics

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. Limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMIT FILTER (Transmit filter input op amp set to the non-inverting unity gain mode, with $VF_xI = 1.09$ Vrms unless otherwise noted.)						
RL_x	Minimum Load Resistance, VF_xO	$-2.5V < V_{OUT} < 2.5V$ $-3.2V < V_{OUT} < 3.2V$	3 10			kΩ kΩ
CL_x	Load Capacitance, VF_xO				100	pF
RO_x	Output Resistance, VF_xO			1	**3**	Ω
PSRR1	V_{CC} Power Supply Rejection, VF_xO	f = 1 kHz, $VF_xI+ = 0$ Vrms	**30**			dB
PSRR2	V_{BB} Power Supply Rejection, VF_xO	Same as Above	**35**			dB
GA_x	Absolute Gain	f = 1 kHz (TP3040A, TP3040A-1) f = 1 kHz (TP3040, TP3040-1)	**2.9** **2.875**	3.0 3.0	**3.1** **3.125**	dB dB
GR_x	Gain Relative to GA_x	Below 50 Hz 50 Hz 60 Hz 200 Hz (TP3040A, TP3040A-1) 200 Hz (TP3040, TP3040-1) 300 Hz to 3 kHz (TP3040A, TP3040A-1) 300 Hz to 3 kHz (TP3040, TP3040-1) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 **−1.5** **−1.5** **−0.125** **−0.15** **−0.35** **−0.70**	 −41 −35 −15	−35 **−35** **−30** **0** **0.05** **0.125** **0.15** **0.03** **−0.1** **−14** **−32**	dB dB dB dB dB dB dB dB dB dB dB
DA_x	Absolute Delay at 1 kHz				250	μs
DD_x	Differential Envelope Delay from 1 kHz to 2.6 kHz				60	μs
DP_x1	Single Frequency Distortion Products				**−48**	dB
DP_x2	Distortion at Maximum Signal Level	0.16 Vrms, 1 kHz Signal Applied to VF_xI+, Gain = 20 dB, $R_L = 10k$			−45	dB
NC_x1	Total C Message Noise at VF_xO	TP3040, TP3040A TP3040-1, TP3040A-1		2	**5** **6**	dBrnc0 dBrnc0
NC_x2	Total C Message Noise at VF_xO	Gain Setting Op Amp at 20 dB, Non-Inverting (Note 3) $T_A = 0°C$ to $70°C$ TP3040, TP3040A TP3040-1, TP3040A-1		 3	 **6** **7**	 dBrnc0 dBrnc0
GA_xT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_xS	Supply Voltage Coefficient of 1 kHz Gain	$V_{CC} = 5.0V \pm 5\%$ $V_{BB} = -5.0V \pm 5\%$		0.01		dB/V
CT_{RX}	Crosstalk, Receive to Transmit $20 \log \frac{VF_xO}{VF_RO}$	Receive Filter Output = 2.2 Vrms $VF_xI+ = 0$ Vrms, f = 0.2 kHz to 3.4 kHz Measure VF_xO			**−70**	dB
GR_xL	Gaintracking Relative to GA_x	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0	**−0.1** **−0.05** **−0.1**		**0.1** **0.05** **0.1**	dB dB dB

1

AC Electrical Characteristics (Continued)

Unless otherwise specified, $T_A = 25°C$. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. Limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE FILTER (Unless otherwise noted, the receive filter is preceded by a sin x/x filter with an input signal level of 1.54 Vrms.)						
IB_R	Input Leakage Current, VF_RI	$-3.2V \le V_{IN} \le 3.2V$	**−100**		**100**	nA
RI_R	Input Resistance, VF_RI		10			MΩ
RO_R	Output Resistance, VF_RO			1	**3**	Ω
CL_R	Load Capacitance, VF_RO				100	pF
RL_R	Load Resistance, VF_RO		10			kΩ
PSRR3	Power Supply Rejection of V_{CC} or V_{BB}, VF_RO	VF_RI Connected to GNDA f = 1 kHz	**35**			dB
VOS_RO	Output DC Offset, VF_RO	VF_RI Connected to GNDA	**−200**		**200**	mV
GA_R	Absolute Gain	f = 1 kHz (TP3040A, TP3040A-1) f = 1 kHz (TP3040, TP3040-1)	**−0.1** **−0.125**	0 0	**0.1** **0.125**	dB dB
GR_R	Gain Relative to Gain at 1 kHz	Below 300 Hz 300 Hz to 3.0 kHz (TP3040A, TP3040A-1) 300 Hz to 3.0 kHz (TP3040, TP3040-1) 3.3 kHz 3.4 kHz 4.0 kHz 4.6 kHz and Above	 **−0.125** **−0.15** **−0.35** **−0.7**		**0.125** **0.125** **0.15** **0.03** **−0.1** **−14** **−32**	dB dB dB dB dB dB dB
DA_R	Absolute Delay at 1 kHz				140	μs
DD_R	Differential Envelope Delay 1 kHz to 2.6 kHz				100	μs
DP_R1	Single Frequency Distortion Products	f = 1 kHz			**−48**	dB
DP_R2	Distortion at Maximum Signal Level	2.2 Vrms Input to Sin x/x Filter, f = 1 kHz, $R_L = 10k$			−45	dB
NC_R	Total C-Message Noise at VF_RO	TP3040, TP3040A TP3040-1, TP3040A-1		3	**5** **6**	dBrnc0 dBrnc0
GA_RT	Temperature Coefficient of 1 kHz Gain			0.0004		dB/°C
GA_RS	Supply Voltage Coefficient of 1 kHz Gain			0.01		dB/V
CT_{XR}	Crosstalk, Transmit to Receive $20 \log \frac{VF_RO}{VF_XO}$	Transmit Filter Output = 2.2 Vrms $VF_RI = 0$ Vrms, f = 0.3 kHz to 3.4 kHz Measure VF_RO			**−70**	dB
GR_RL	Gaintracking Relative to GA_R	Output Level = +3 dBm0 +2 dBm0 to −40 dBm0 −40 dBm0 to −55 dBm0 (Note 5)	**−0.1** **−0.05** **−0.1**		**0.1** **0.05** **0.1**	dB dB dB

AC Electrical Characteristics (Continued)

Unless otherwise specified, T_A = 25°C. All parameters are specified for a signal level of 0 dBm0 at 1 kHz. The 0 dBm0 level is assumed to be 1.54 Vrms measured at the output of the transmit or receive filter. Limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE OUTPUT POWER AMPLIFIER						
IBP	Input Leakage Current, PWRI	−3.2V ≤ V_{IN} ≤ 3.2V	**0.1**		**3**	μA
RIP	Input Resistance, PWRI		10			MΩ
ROP1	Output Resistance, PWRO+, PWRO−	Amplifiers Active		1		Ω
CLP	Load Capacitance, PWRO+, PWRO−				500	pF
GA_p+ GA_p−	Gain, PWRI to PWRO+ Gain, PWRI to PWRO−	R_L=600Ω Connected Between PWRO+ and PWRO−, Input Level=0 dBm0 (Note 4)		1 −1		V/V V/V
GR_pL	Gaintracking Relative to 0 dBm0 Output Level, Including Receive Filter	V=2.05 Vrms, R_L=600Ω (Notes 4, 5) V=1.75 Vrms, R_L=300Ω	**−0.1** −0.1		**0.1** 0.1	dB dB
S/D_p	Signal/Distortion	V=2.05 Vrms, R_L=600Ω (Notes 4, 5) V=1.75 Vrms, R_L=300Ω			**−45** −45	dB dB
VOSP	Output DC Offset, PWRO+, PWRO−	PWRI Connected to GNDA	**−50**		**50**	mV
PSRR5	Power Supply Rejection of V_{CC} or V_{BB}	PWRI Connected to GNDA	**45**			dB

Note 1: Maximum power consumption will depend on the load impedance connected to the power amplifier. This specification listed assumes 0 dBm is delivered to 600Ω connected from PWRO+ to PWRO−.

Note 2: Voltage input to receive filter at 0V, VF_RO connected to PWRI, 600Ω from PWRO+ to PWRO−. Output measured from PWRO+ to PWRO−.

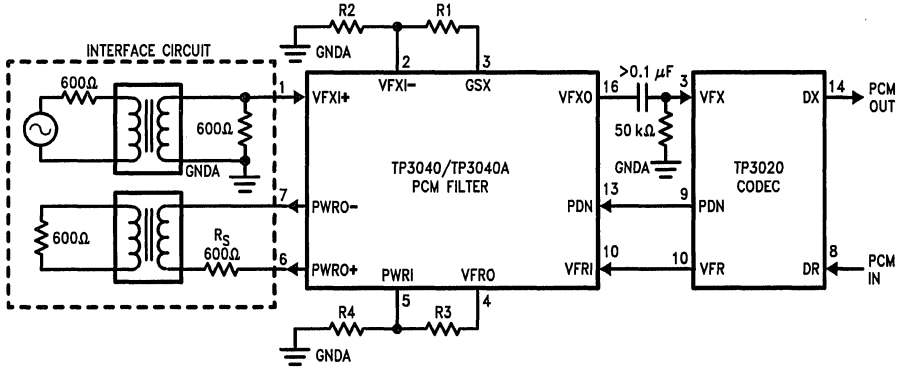
Note 3: The 0 dBm0 level for the filter is assumed to be 1.54 Vrms measured at the output of the XMT or RCV filter.

Note 4: The 0 dBm0 level for the power amplifiers is load dependent. For R_L=600Ω to GNDA, the 0 dBm0 level is 1.43 Vrms measured at the amplifier output. For R_L=300Ω the 0 dBm0 level is 1.22 Vrms.

Note 5: VF_RO connected to PWRI, input signal applied to VF_RI.

Note 6: Previous revisions of the datasheet did not clearly indicate this specification requires power amps in powerdown (PWRI = −5.25V).

Typical Application



TL/H/6660-2

Note 1: Transmit voltage gain = $\frac{R1+R2}{R2} \times \sqrt{2}$ (The filter itself introduces a 3 dB gain), (R1 + R2 ≥ 10k)

Note 2: Receive gain = $\frac{R4}{R3+R4}$

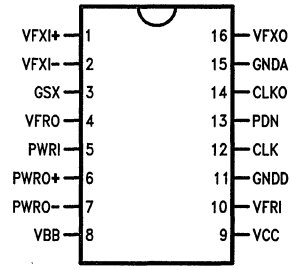
(R3 + R4 ≥ 10k)

Note: In the configuration shown, the receive filter power amplifiers will drive a 600Ω T to R termination to a maximum signal level of 8.5 dBm. An alternative arrangement, using a transformer winding ratio equivalent to 1.414:1 and 300Ω resistor, R_S, will provide a maximum signal level of 10.1 dBm across a 600Ω termination impedance.

FIGURE 2

Connection Diagram

Dual-In-Line Package

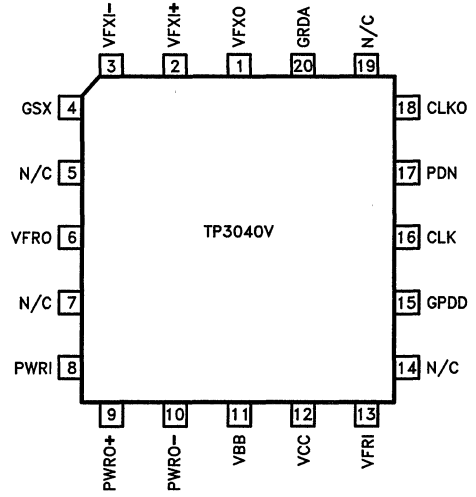


TL/H/6660–3

Top View

Order Number TP3040J or TP3040AJ
or TP3040J-1 or TP3040AJ-1
See NS Package J16A

Plastic Lead Chip Carrier



TL/H/6660–4

Order Number TP3040V or TP3040AV
or TP3040V-1 or TP3040AV-1
See NS Package V20A

Description of Pin Functions

Symbol	Function
VF_XI+	The non-inverting input to the transmit filter stage.
VF_XI-	The inverting input to the transmit filter stage.
GS_X	The output used for gain adjustments of the transmit filter.
VF_RO	The low power receive filter output. This pin can directly drive the receive port of an electronic hybrid.
PWRI	The input to the receive filter differential power amplifier.
PWRO+	The non-inverting output of the receive filter power amplifier. This output can directly interface conventional transformer hybrids.
PWRO−	The inverting output of the receive filter power amplifier. This output can be used with PWRO+ to differentially drive a transformer hybrid.
V_{BB}	The negative power supply pin. Recommended input is −5V.
V_{CC}	The positive power supply pin. The recommended input is 5V.
VF_RI	The input pin for the receive filter stage.

Symbol	Function
GNDD	Digital ground input pin. All digital signals are referenced to this pin.
CLK	Master input clock. Input frequency can be selected as 2.048 MHz, 1.544 MHz or 1.536 MHz.
PDN	The input pin used to power down the TP3040/TP3040A during idle periods. Logic 1 (V_{CC}) input voltage causes a power down condition. An internal pull-up is provided.
CLK0	This input pin selects internal counters in accordance with the CLK input clock frequency:

CLK	Connect CLK0 to:
2048 kHz	V_{CC}
1544 kHz	GNDD
1536 kHz	V_{BB}

An internal pull-up is provided.

GNDA	Analog ground input pin. All analog signals are referenced to this pin. Not internally connected to GNDD.
VF_XO	The output of the transmit filter stage.

Functional Description

The TP3040/TP3040A monolithic filter contains four main sections; Transmit Filter, Receive Filter, Receive Filter Power Amplifier, and Frequency Divider/Select Logic (*Figure 1*). A brief description of the circuit operation for each section is provided below.

TRANSMIT FILTER

The input stage of the transmit filter is a CMOS operational amplifier which provides an input resistance of greater than 10 MΩ, a voltage gain of greater than 5,000, low power consumption (less than 3 mW), high power supply rejection, and is capable of driving a 10 kΩ load in parallel with up to 25 pF. The inputs and output of the amplifier are accessible for added flexibility. Non-inverting mode, inverting mode, or differential amplifier mode operation can be implemented with external resistors. It can also be connected to provide a gain of up to 20 dB without degrading the overall filter performance.

The input stage is followed by a prefilter which is a two-pole RC active low pass filter designed to attenuate high frequency noise before the input signal enters the switched-capacitor high pass and low pass filters.

A high pass filter is provided to reject 200 Hz or lower noise which may exist in the signal path. The low pass portion of the switched-capacitor filter provides stopband attenuation which exceeds the D3 and D4 specifications as well as the CCITT G712 recommendations.

The output stage of the transmit filter, the postfilter, is also a two-pole RC active low pass filter which attenuates clock frequency noise by at least 40 dB. The output of the transmit filter is capable of driving a ±3.2V peak to peak signal into a 10 kΩ load in parallel with up to 25 pF.

RECEIVE FILTER

The input stage of the receive filter is a prefilter which is similar to the transmit prefilter. The prefilter attenuates high frequency noise that may be present on the receive input signal. A switched capacitor low pass filter follows the prefilter to provide the necessary passband flatness, stopband rejection and sin x/x gain correction. A postfilter which is similar to the transmit postfilter follows the low pass stage. It attenuates clock frequency noise and provides a low output impedance capable of directly driving an electronic subscriber-line-interface circuit.

RECEIVE FILTER POWER AMPLIFIERS

Two power amplifiers are also provided to interface to transformer coupled line circuits. These two amplifiers are driven by the output of the receive postfilter through gain setting resistors, R3, R4 (*Figure 2*). The power amplifiers can be deactivated, when not required, by connecting the power amplifier input (pin 5) to the negative power supply V_{BB}. This reduces the total filter power consumption by approximately 10 mW–20 mW depending on output signal amplitude.

POWER DOWN CONTROL

A power down mode is also provided. A logic 1 power down command applied on the PDN pin (pin 13) will reduce the total filter power consumption to less than 1 mW. Connect PDN to GNDD for normal operation.

FREQUENCY DIVIDER AND SELECT LOGIC CIRCUIT

This circuit divides the external clock frequency down to the switching frequency of the low pass and high pass switched capacitor filters. The divider also contains a TTL-CMOS interface circuit which converts the external TTL clock level to the CMOS logic level required for the divider logic. This interface circuit can also be directly driven by CMOS logic. A frequency select circuit is provided to allow the filter to operate with 2.048 MHz, 1.544 MHz or 1.536 MHz clock frequencies. By connecting the frequency select pin CLK0 (pin 14) to V_{CC}, a 2.048 MHz clock input frequency is selected. Digital ground selects 1.544 MHz and V_{BB} selects 1.536 MHz.

Applications Information

GAIN ADJUST

Figure 2 shows the signal path interconnections between the TP3040/TP3040A and the TP3020 signal-channel CODEC. The transmit RC coupling components have been chosen both for minimum passband droop and to present the correct impedance to the CODEC during sampling.

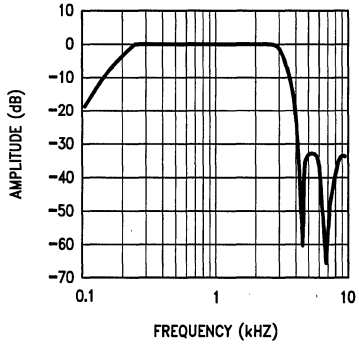
Optimum noise and distortion performance will be obtained from the TP3040/TP3040A filter when operated with system peak overload voltages of ±2.5V to ±3.2V at VF_XO and VF_RO. When interfacing to a PCM CODEC with a peak overload voltage outside this range, further gain or attenuation may be required.

BOARD LAYOUT

Care must be taken in PCB layout to minimize power supply and ground noise. Analog ground (GNDA) of each filter should be connected to digital ground (GNDD) at a single point, which should be bypassed to both power supplies. Further power supply decoupling adjacent to each filter and CODEC is recommended. Ground loops should be avoided, both between GNDA and GNDD and between the GNDA traces of adjacent filters and CODECs.

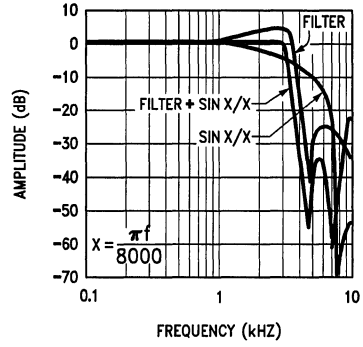
Typical Performance Characteristics

Transmit Filter Stage



TL/H/6660–5

Receive Filter Stage



TL/H/6660–6

National Semiconductor

TP3051, TP3056 Parallel Interface CODEC/Filter COMBO®

General Description

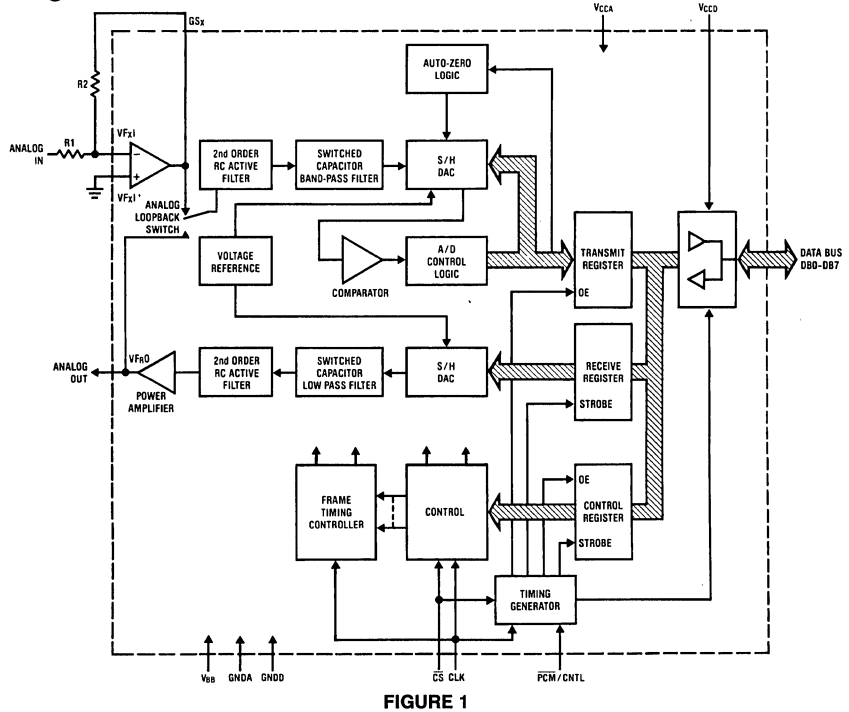
The TP3051, TP3056 family consists of a μ-law and A-law monolithic PCM CODEC/filter set utilizing the A/D and D/A conversion architecture shown in *Figure 1* and a parallel I/O data bus interface. The devices are fabricated using National's advanced double poly microCMOS process.

The transmit section consists of an input gain adjust amplifier, an active RC pre-filter, and a switched-capacitor bandpass filter that rejects signals below 200 Hz and above 3400 Hz. A compressing coder samples the filtered signal and encodes it in the μ-255 law or A-law PCM format. Autozero circuitry is included on-chip. The receive section consists of an expanding decoder which reconstructs the analog signal from the compressed μ-law or A-law code, and a low pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The receive output is a single-ended power amplifier capable of driving low impedance loads. The TP3051 μ-law and TP3056 A-law devices are pin compatible parallel interface COMBOs for bus-oriented systems.

Features

- Complete CODEC and filtering system including:
  - — Transmit high pass and low pass filtering
  - — Receive low pass filter with sin x/x correction
  - — Receive power amplifier
  - — Active RC noise filters
  - — μ-255 law COder and DECoder—TP3051
  - — A-law COder and DECoder—TP3056
  - — Internal precision voltage reference
  - — Internal auto-zero circuitry
- Meets or exceeds all LSSGR and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- High speed TRI-STATE® data bus
- 2 loopback test modes

Block Diagram

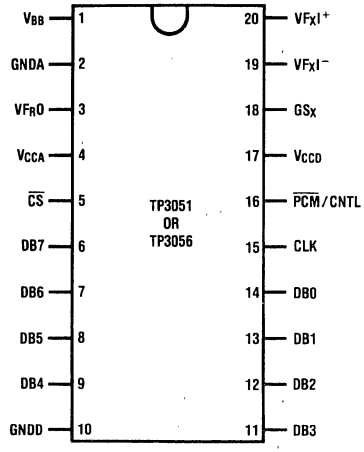


TL/H/8834–1

FIGURE 1

Connection Diagrams

Dual-In-Line Package



TL/H/8834–3

Top View

Order Number TP3051J or TP3056J
See NS Package Number J20A

Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
GNDA	Analog ground. All analog signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier. This output can drive a 600Ω load to ±2.5V.
V_{CCA}	Positive power supply voltage pin for the analog circuitry. $V_{CCA} = 5V \pm 5\%$. Must be connected to V_{CCD}.
$\overline{CS}$	Device chip select input which controls READ, WRITE and TRI-STATE® operations on the data bus. $\overline{CS}$ does not control the state of any analog functions.
DB7	Bit 7 I/O on the data bus. The PCM LSB.
DB6	Bit 6 I/O on the data bus.
DB5	Bit 5 I/O on the data bus.
DB4	Bit 4 I/O on the data bus.
GNDD	Digital ground. All digital signals are referenced to this pin.
DB3	Bit 3 I/O on the data bus.
DB2	Bit 2 I/O on the data bus.
DB1	Bit 1 I/O on the data bus.
DB0	Bit 0 I/O on the data bus. This is the PCM sign bit.
CLK	The clock input for the switched-capacitor filters and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the system clock input.
$\overline{PCM}$/CNTL	This control input determines whether the information on the data bus is PCM data or control data.
V_{CCD}	Positive power supply pin for the bus drivers. $V_{CCD} = 5V \pm 5\%$. Must be connected to V_{CCA}.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

CLOCK AND DATA BUS CONTROL

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table I and must be correctly selected by control bits C0 and C1.

CLK also functions as a READ/$\overline{WRITE}$ control signal, with the device reading the data bus on a positive half-clock cycle and writing the bus on a negative half-clock cycle, as shown in *Figures 4a* and *4b*.

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0–DB7, and receive power amplifier output, VF_RO, are in high impedance states.

The TP3051, TP3056 is powered-up via a command to the control register (see Control Register Functions). This sets

Functional Description (Continued)

the device in the standby mode with all circuitry activated, but encoding and decoding do not begin until PCM READ and PCM WRITE chip selects occur.

TABLE I. Control Bit Functions

Control Bits	Function
C0, C1	Select Clock Frequency **C0** **C1** **Frequency** 0 X 1.024 MHz 1 0 0.768 MHz or 0.772 MHz 1 1 1.28 MHz
C2, C3	Digital and Analog Loopback **C2** **C3** **Mode** 1 X digital loopback 0 1 analog loopback 0 0 normal
C4	Power-Down/Power-Up (Note 1) 1 = power-down 0 = power-up
C5	TP3051—Don't care (Note 1) TP3056 1 = Not implemented. Do not use. 0 = A-law with even bit inversion
C6–C7	Don't Care (Note 1)

Note 1: These bits are always set to logical "1" when reading back the control register.

DATA BUS NOMENCLATURE

The normal order for serial PCM transmission is sign bit first, whereas the normal order for serial data is LSB first. The parallel data bus is defined as follows:

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

READING THE BUS

If CLK is low when $\overline{CS}$ goes low, bus data is gated in during the next positive half-clock cycle of CLK and latched on the negative-going transition. If $\overline{PCM}$/CNTL is low during the falling $\overline{CS}$ transition, then the bus data is defined as PCM voice data, which is latched into the receive register. This also functions as an internal receive frame synchronization pulse to start a decode cycle and must occur once per receive frame, i.e., at an 8 kHz rate.

If $\overline{PCM}$/CNTL is high during the falling $\overline{CS}$ transition, the bus data is latched into the control register. This does not affect frame synchronization.

WRITING THE BUS

If CLK is high when $\overline{CS}$ goes low, at the next falling transition of CLK, the bus drivers are enabled and either the PCM transmit data or the contents of the control register are gated onto the bus, depending on the level of $\overline{PCM}$/CNTL at the $\overline{CS}$ transition. If $\overline{PCM}$/CNTL is low during the $\overline{CS}$ falling transition, the transmit register data is written to the bus.

An internal transmit frame synchronization pulse is also generated to start an encode cycle, and this must occur once per transmit frame; i.e., at an 8 kHz rate.

If $\overline{PCM}$/CNTL is high during the $\overline{CS}$ falling transition, the control register data is written to the bus. This does not affect frame synchronization.

The receive register contents may also be written back to the bus, as described in the Digital Loopback section.

Except during a WRITE cycle, the bus drivers are in TRI-STATE mode.

CONTROL REGISTER FUNCTIONS

Writing to the control register allows the user to set the various operating states of the TP3051 and TP3056. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. CLK Select

   Since one of three distinct clock frequencies may be used, the actual frequency must be known by the device for proper operation of the switched-capacitor filters. This is achieved by writing control register bits C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

2. Digital Loopback

   In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in the TP3051 or TP3056 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back onto the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination at VF_RO.

3. Analog Loopback

   In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is entered by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.

4. Power-Down/Power-Up

   The TP3051 or TP3056 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, setting bit C4 to 0 powers-up the device.

TRANSMIT FILTER AND ENCODE SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 2*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2nd order RC active pre-filter, followed by an 8th order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-255 law (TP3051) or A-law (TP3056) coding schemes. A precision voltage reference is trimmed in manufacturing

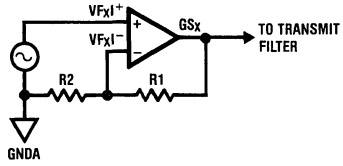
Functional Description (Continued)

to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

The total encoding delay referenced to a PCM WRITE chip select will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs.

DECODER AND RECEIVE FILTER SECTION

The receive section consists of an expanding DAC which drives a 5th order switched-capacitor low pass filter clocked at 256 kHz. The decoder is of A-law (TP3056) or μ-law (TP3051) coding law and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter. The power amplifier output stage is capable of driving a 600Ω load to a level of 7.2 dBm. See *Figure 3.* The receive section has unity-gain. Following a PCM READ chip select, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

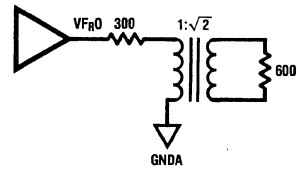


TL/H/8834–4

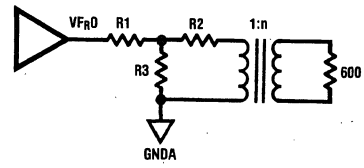
Non-inverting transmit gain = $20 \log_{10} \left(\frac{R1 + R2}{R2} \right)$

Set gain to provide peak overload level = t_{MAX} at GS_X (see Transmission Characteristics)

FIGURE 2. Transmit Gain Adjustment



Maximum output power = 7.2 dBm total, 4.2 dBm to the load.



TL/H/8834–5

See Applications information for attenuator design guide.

FIGURE 3. Receive Gain Adjustment

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

GNDD to GNDA	±0.3V
V_{CCA} or V_{CCD} to GNDD or GNDA	7V
V_{BB} to GNDD or GNDA	−7V
Voltage at Any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at Any Digital Input or Output	V_{CC} + 0.3V to GNDD − 0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD (Human Body Model)	1000V

Electrical Characteristics

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, T_A = 0°C to 70°C; typical characteristics specified at nominal supply voltages, T_A = 25°C; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; T_A = 0°C to 70°C by correlation with 100% Electrical testing at T_A = 25°C. All other limits are assured by correlation with other production test and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	DB0–DB7, I_L = 2.5 mA			**0.4**	V
V_{OH}	Output High Voltage	DB0–DB7, I_H = −2.5 mA	**2.4**			V
I_{IL}	Input Low Current	GNDD ≤ V_{IN} ≤ V_{IL}	**−3**		**3**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−3**		**3**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	DB0–DB7, GNDD ≤ V_O ≤ V_{CC}	**−3**		**3**	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER						
I_IXA	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance, GS_X	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance, GS_X		10			kΩ
C_LXA	Load Capacitance, GS_X				50	pF
V_OXA	Output Dynamic Range, GS_X	R_L = 10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	**−2.5**		**2.5**	V
CMRRXA	Common-Mode Rejection Ratio	D.C. Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	D.C. Test	**60**			dB
RECEIVE POWER AMPLIFIER						
R_ORF	Output Resistance, VF_RO			1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	600			Ω
C_LRF	Load Capacitance				50	pF
VOS_RO	Output DC Offset Voltage		**−200**		**200**	mV
POWER DISSIPATION						
I_{CC0}	Power-Down Current	No Load (Note 1)		0.5	**1.5**	mA
I_{BB0}	Power-Down Current	No Load (Note 1)		0.05	**0.3**	mA
I_{CC1}	Active Current	No Load		6.0	**9.0**	mA
I_{BB1}	Active Current	No Load		6.0	**9.0**	mA

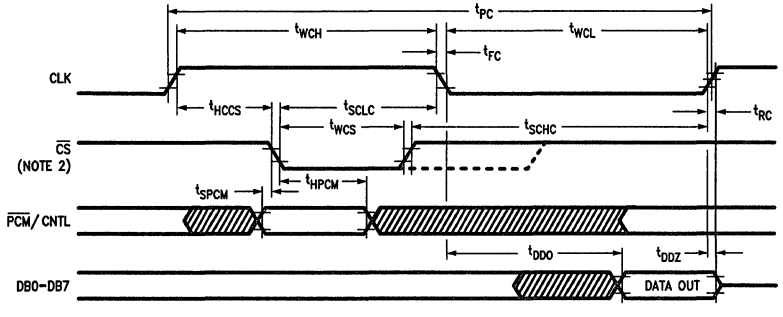
Note 1: I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

Timing Specifications

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, $T_A = 0°C$ to $70°C$; typical characteristics specified at nominal supply voltages, $T_A = 25°C$; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% Electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production test and/or product design and characteristics. All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$. See Definitions and Timing Conventions section for test method information.

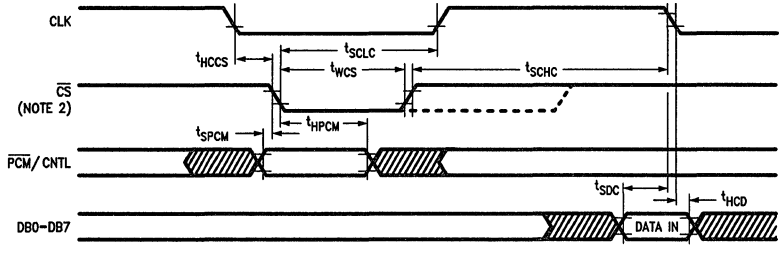
Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock		760		ns
t_{WCH}	Width of Clock High		**330**		ns
t_{WCL}	Width of Clock Low		330		ns
t_{RC}	Rise Time of Clock			50	ns
t_{FC}	Fall Time of Clock			50	ns
t_{HCCS}	Hold Time from CLK to $\overline{CS}$ Low		**100**		ns
t_{SCLC}	Set-Up Time of $\overline{CS}$ Low to CLK		**100**		ns
t_{SCHC}	Set-Up Time from $\overline{CS}$ High to Second CLK Edge		**0**		ns
t_{WCS}	Width of Chip Select		**100**		ns
t_{SPCM}	Set-Up Time of $\overline{PCM}$/CNTL to $\overline{CS}$		**0**		ns
t_{HPCM}	Hold Time from $\overline{CS}$ to $\overline{PCM}$/CNTL		**100**		ns
t_{SDC}	Set-Up Time of Data In to CLK		**50**		ns
t_{HCD}	Hold Time from CLK to Data In		20		ns
t_{DDO}	Delay Time to Data Out Valid	$C_L = 0$ pF to 200 pF	**90**	**260**	ns
t_{DDZ}	Delay Time to Data Output Disabled	$C_L = 0$ pF to 200 pF	20	80	ns

Switching Time Waveforms



TL/H/8834-6

FIGURE 4a. Timing Waveforms for COMBO Writing to the Bus



TL/H/8834-7

FIGURE 4b. Timing Waveforms for COMBO Reading from the Bus

Note 2: READ and WRITE $\overline{CS}$ pulses must each occur at an 8 kHz rate, and may occur on consecutive half-cycles of CLK if required, although this is not a restriction.

Transmission Characteristics

Unless otherwise specified: T_A = 0°C to +70°C, V_{CCA} = V_{CCD} = 5V ±5%, V_{BB} = −5V ±5%, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for V_{CCA} = V_{CCD} = 5.0V ±5% and V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω)				
	0 dBm0	TP3051 TP3056		1.2276 1.2276		Vrms Vrms
t_{MAX}	Maximum Overload Level	TP3051 (+3.17 dBm0) TP3056 (+3.14 dBm0)		2.501 2.492		V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, V_{CCA} = V_{CCD} = 5.0V, V_{BB} = −5.0V Input at GS_X = 0 dBm0 at 1020 Hz	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz f = 50 Hz f = 60 Hz f = 200 Hz f = 300 Hz–3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−1.8** **−0.15** **−0.35** **−0.7** 		−40 −30 **−26** **−0.1** **0.15** **0.1** **0** **−14** **−32**	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variation with Level	Sinusoidal Method Reference Level = −10 dBm0 VF_XI^+ = −40 dBm0 to +3 dBm0 VF_XI^+ = −50 dBm0 to −40 dBm0 VF_XI^+ = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A = 25°C, V_{CCA} = V_{CCD} = 5V, V_{BB} = −5V Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	**−0.15**		**0.15**	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz f = 3300 Hz f = 3400 Hz f = 4000 Hz	**−0.15** **−0.35** **−0.7** 		**0.15** **0.05** **0** **−14**	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variation with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded −10 dBm0 Signal PCM Level = −40 dBm0 to +3 dBm0 PCM Level = −50 dBm0 to −40 dBm0 PCM Level = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
V_{RO}	Receive Output Drive Level	R_L = 600Ω	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise specified: T_A = 0°C to +70°C, V_{CCA} = V_{CCD} = 5V ±5%, V_{BB} = −5V ±5%, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for V_{CCA} = V_{CCD} = 5.0V ±5% and V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	μs
		f = 600 Hz–800 Hz		120	145	μs
		f = 800 Hz–1000 Hz		50	75	μs
		f = 1000 Hz–1600 Hz		20	40	μs
		f = 1600 Hz–2600 Hz		55	75	μs
		f = 2600 Hz–2800 Hz		80	105	μs
		f = 2800 Hz–3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		μs
		f = 1000 Hz–1600 Hz	−30	−20		μs
		f = 1600 Hz–2600 Hz		70	90	μs
		f = 2600 Hz–2800 Hz		100	125	μs
		f = 2800 Hz–3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3051, (Note 3)		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3056, VF_XI^+ = 0V (Note 3)		−74	**−69**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3051, PCM Code Equals Alternating Positive and Negative Zero		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3056, PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0V			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI^+ = 0V, V_{CCA} = V_{CCD} = 5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 4)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI^+ = 0 Vrms, V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz–50 kHz (Note 4)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3051 and TP3056 V_{CC} = 5.0 V_{DC} + 100 mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dBc
		f = 25 kHz–50 kHz	**36**			dBc
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3051 and TP3056 V_{BB} = −5.0 V_{DC} + 100 mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dBc
		f = 25 kHz–50 kHz	**36**			dBc
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz–3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO				
		4600 Hz–7600 Hz			**−32**	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			**−32**	dB

Transmission Characteristics (Continued)

Unless otherwise specified: T_A = 0°C to +70°C, V_{CCA} = V_{CCD} = 5V ±5%, V_{BB} = −5V ±5%, GNDD = GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for V_{CCA} = V_{CCD} = 5.0V ±5% and V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characteristics.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 5) Level = 3.0 dBm0 = 0 dBm0 to −30 dBm0 = −40 dBm0 XMT RCV = −55 dBm0 XMT RCV	 **33** **36** **29** **30** **14** **15**			 dB dB dB dB dB dB
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz at 0 dBm0 Transmit Level Steady PCM Receive Code		−90	**−70**	dB
CT_{R-X}	Receive to Transmit Crosstalk 0 dBm0 Receive Level	f = 300 Hz–3400 Hz at 0 dBm0 (Note 2)		−90	**−70**	dB

Note 3: Measured by extrapolation from the distortion test result at −50 dB m0.

Note 4: CT_{R-X}, $PPSR_X$, and $NPSR_X$ are measured with a −50 dBm0 activation signal applied at VF_XI^+.

Note 5: Devices are measured using C message weighted filter for μ-law and psophometric weighted filter for A-law.

Encoding Format at Data Bus Output

	TP3051 μ-Law								TP3056 True A-Law, C5 = 0 (Includes Even Bit Inversion)							
	MSB							LSB	MSB							LSB
V_{IN} = + Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = +0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
V_{IN} = − 0V	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = − Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Applications Information

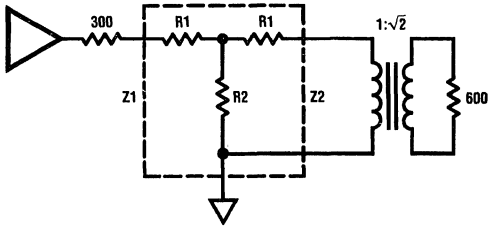
POWER SUPPLIES

While the pins of the TP3051/6 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used. GNDA and GNDD MUST be connected together adjacent to each COMBO not on the connector or backplane wiring.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CCA} and V_{BB}.

For best performance, the ground point of each COMBO on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

T-Pad Attenuator



TL/H/8834–8

$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

Where: $N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$

and

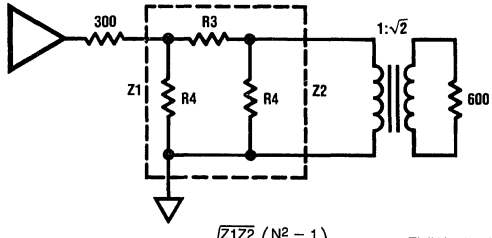
$$S = \sqrt{\frac{Z1}{Z2}}$$

Also: $Z = \sqrt{Z_{SC}\,Z_{OC}}$

Where Z_{SC} = Impedance with short circuit termination

and Z_{OC} = Impedance with open circuit termination

π-Pad Attenuator



TL/H/8834–9

$$R3 = \sqrt{\frac{Z1Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R4 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

FIGURE 5. T-Pad and π-Pad Attenuator Models

The positive power supply to the bus drivers, V_{CCD}, is provided on a separate pin from the positive supply for the CODEC and filter circuits to minimize noise injection when driving the bus. V_{CCA} and V_{CCD} MUST be connected together close to the CODEC/filter at the point where the 0.1 μF decoupling capacitor is connected.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family COMBO receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. (See *Figure 5.*) Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closer practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Note: See Application Note 370 for further details.

National Semiconductor

TP3052, TP3053, TP3054 TP3054-1, TP3057, TP3057-1 "Ruggedized" Serial Interface CODEC/Filter COMBO® Family

General Description

The TP3052, TP3053, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (micro-CMOS).

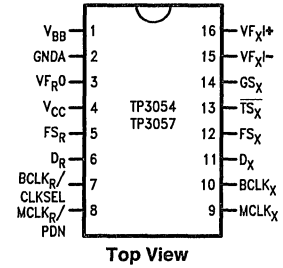
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- Complete CODEC and filtering system (COMBO) including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
- μ-law with signaling, TP3020 or TP5116A timing—TP3052
- μ-law with signaling, TP5116A family timing—TP3053
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density
- Dual-In-Line or PCC surface mount packages

Connection Diagrams

Dual-In-Line Package

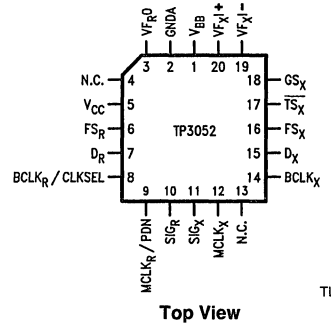


TL/H/5510-1

Top View

Order Number TP3054J, TP3054J-1, TP3057J or TP3057J-1
See NS Package Number J16A

Plastic Chip Carriers



TL/H/5510-10

Top View

Order Number TP3052V*
See NS Package Number V20A

*Available mid 1990

1

Block Diagram

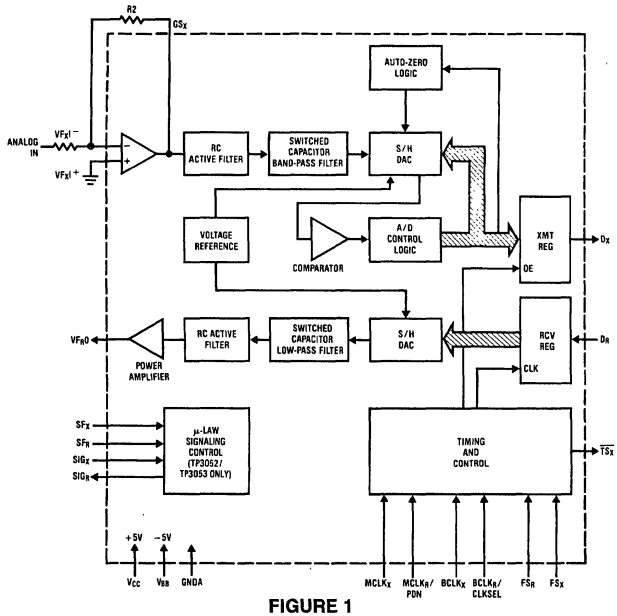


FIGURE 1 TL/H/5510–2

Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
GNDA	Analog ground. All signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1).
$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
SF_R	When high during FS_R, this input indicates a receive signal frame.
SIG_R	The eighth bit of the PCM data appears at this output after each receive signalling frame.
SIG_X	Signal data input. Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
SF_X	When high during FS_X, this input indicates a transmit signaling frame.
$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into a power-down state. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3057	TP3052 TP3053 TP3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3052, 53, 54, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table 1 are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the TP5116A/56A long frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

SIGNALING

The TP3052 and TP3053 μ-law COMBOs contain circuitry to insert and extract signaling information in the PCM data stream. The TP3052 is intended for short frame sync applications, and the TP3053 for long frame sync applications, although the TP3053 may also be used in short frame sync applications. The TP3054 and TP3057 have no provision for signaling.

Functional Description (Continued)

Signaling for the TP3052 is accomplished by applying a frame sync pulse two bit clock periods long, as shown in *Figure 2*. With FS_X two bit clock periods long, the data present at SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With FS_R two bit clock periods long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as "½" to minimize noise and distortion. This short frame signaling may also be implemented using the TP3053, providing SF_R and SF_X are left open circuit or tied low. The TP3052 is not capable of inserting or extracting signaling information in the long frame mode.

Signaling for the TP3053 may be accomplished in either short or long frame sync mode. The short mode signaling is the same as the TP3052. For long frame signaling, two additional frame sync pulses are required, SF_X and SF_R, which indicate transmit and receive signaling frames, respectively. With an SF_X signaling frame sync, the data present at the SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With an SF_R signaling frame sync, the LSB of the PCM data at D_R will be latched and appear on the SIG_R output pin until the next signaling frame. The decoder will also do the "½" step interpretation to compensate for the loss of the LSB.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3052, TP3053, TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ-law (TP3052, TP3053, TP3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifer capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at any Digital Input or Output	V_{CC} + 0.3V to GNDA − 0.3V
Operating Temperature Range	−25°C to + 125°C
Storage Temperature Range	−65°C to + 150°C
Lead Temperature (Soldering, 10 seconds)	300°C
ESD (Human Body Model)	2000V
Latch-Up Immunity = 100 mA on any Pin	

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

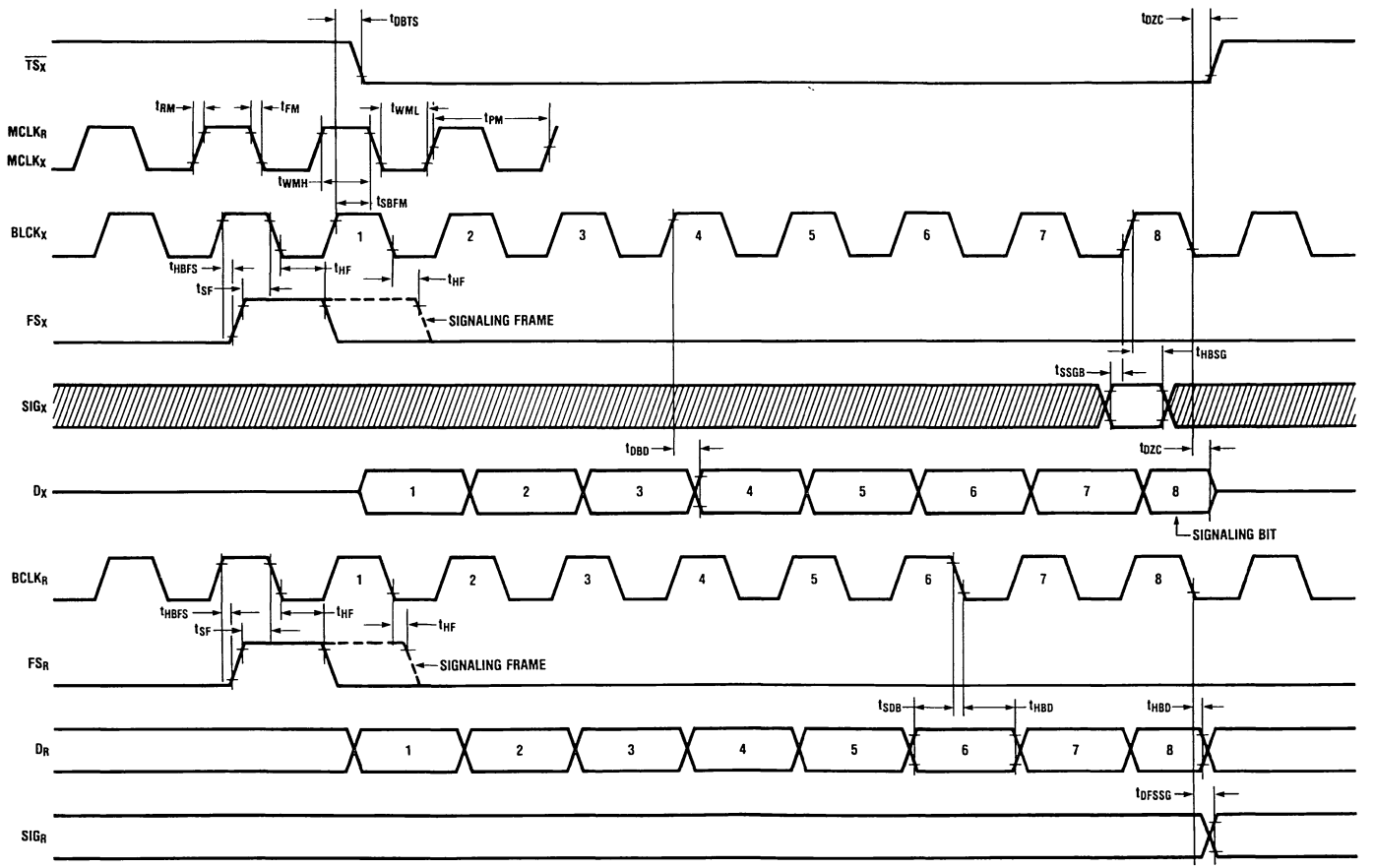
Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA SIG_R, I_L = 1.0 mA $\overline{TS}_X$, I_L = 3.2 mA, Open Drain			**0.4** **0.4** **0.4**	V V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA SIG_R, I_H = −1.0 mA	**2.4** **2.4**			V V
I_{IL}	Input Low Current	GNDA ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	**−10**		**10**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA ≤ V_O ≤ V_{CC}	**−10**		**10**	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VF_XI+ or VF_XI-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V ≤ V ≤ +2.5V, VF_XI+ or VF_XI-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, R_L ≥ 10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI+ to GS_X	**5000**			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		−200		200	mV
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current	No Load (Note)		0.5	**1.5**	mA
$I_{BB}0$	Power-Down Current	No Load (Note)		0.05	**0.3**	mA
$I_{CC}1$	Power-Up Active Current	No Load		6.0	**9.0**	mA
$I_{BB}1$	Power-Up Active Current	No Load		6.0	**9.0**	mA

Note: I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

Timing Specifications

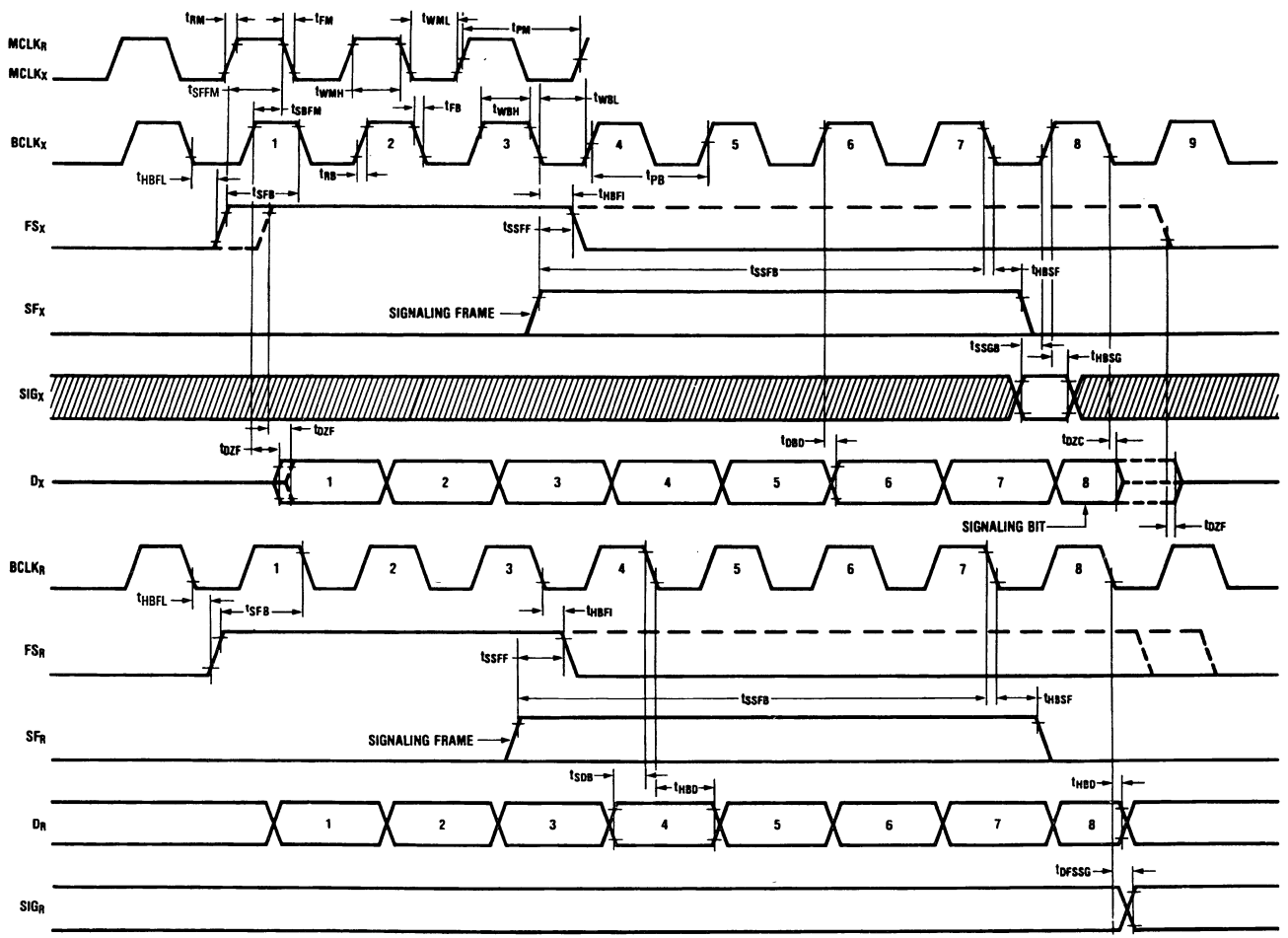
Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V. See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 2.048		MHz MHz MHz
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock		485	**488**	15725	ns
t_{RB}	Rise Time of Bit Clock	$BCLK_X$ and $BCLK_R$			50	ns
t_{FB}	Fall Time of Bit Clock	$BCLK_X$ and $BCLK_R$			50	ns
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	**100**			ns
t_{SFFM}	Set-Up Time from FS_X High to $MCLK_X$ Falling Edge	Long Frame Only	**100**			ns
t_{WBH}	Width of Bit Clock High	V_{IH} = 2.2V	**160**			ns
t_{WBL}	Width of Bit Clock Low	V_{IL} = 0.6V	**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	**80**			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	C_L = 0 pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C_L = 0 pF to 150 pF	20		165	ns
t_{SSFF}	Set-Up Time from $SF_{X/R}$ High to $FS_{X/R}$	TP3053 Only	**60**			ns
t_{SSFB}	Set-Up Time from Signal Frame Sync High to $BCLK_{X/R}$ Clock	TP3053 Only	**60**			ns
t_{SSGB}	Set-Up Time from SIG_X to $BCLK_X$	TP3052 and TP3053	**100**			ns
t_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	TP3052 and TP3053	**50**			ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		**50**			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		**50**			ns
t_{HBSF}	Hold Time from $BCLK_{X/R}$ Low to Signaling Frame Sync	TP3053 Only	**100**			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	**160**			ns



TL/H/5510–3

FIGURE 2. Short Frame Sync Timing



TL/H/5510–4

FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		 1.2276		 Vrms
t_{MAX}		Max Overload Level TP3052, TP3053, TP3054 (3.17 dBm0) TP3057 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input at GS_X=0 dBm0 at 1020 Hz TP3052/53/54/57 TP3054-1/57-1	 **−0.15** **−0.20**		 **0.15** **0.20**	 dB dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16 Hz f=50 Hz f=60 Hz (TP3054-1/57-1) f=60 Hz (TP3054/57) f=200 Hz f=300 Hz−3000 Hz f=3300 Hz f=3400 Hz (TP3052/53/54/57) f=3400 Hz (TP3054-1/57-1) f=4000 Hz f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−1.8** **−0.15** **−0.35** **−0.7** **−0.95**		−40 −30 **−22** **−26** **−0.1** **0.15** **0.05** **0** **0.05** **−14** **−32**	dB dB dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level=−10 dBm0 VF_XI^+=−40 dBm0 to +3 dBm0 VF_XI^+=−50 dBm0 to −40 dBm0 VF_XI^+=−55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz TP3052/53/54/57 TP3054-1/57-1	 **−0.15** **−0.20**		 **0.15** **0.20**	 dB dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0 Hz to 3000 Hz f=3300 Hz f=3400 Hz f=4000 Hz	**−0.15** **−0.35** **−0.7**		**0.15** **0.05** **0** **−14**	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level =−40 dBm0 to +3 dBm0 =−40 dBm0 to +3 dBm0 (TP3054-1/57-1 only) =−50 dBm0 to −40 dBm0 =−55 dBm0 to −50 dBm0	 **−0.2** **−0.25** **−0.4** **−1.2**		 **0.2** **0.25** **0.4** **1.2**	 dB dB dB dB
V_{RO}	Receive Output Drive Level	R_L=600Ω	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	μs
		f = 600 Hz–800 Hz		120	145	μs
		f = 800 Hz–1000 Hz		50	75	μs
		f = 1000 Hz–1600 Hz		20	40	μs
		f = 1600 Hz–2600 Hz		55	75	μs
		f = 2600 Hz–2800 Hz		80	105	μs
		f = 2800 Hz–3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		μs
		f = 1000 Hz–1600 Hz	−30	−20		μs
		f = 1600 Hz–2600 Hz		70	90	μs
		f = 2600 Hz–2800 Hz		100	125	μs
		f = 2800 Hz–3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3052, TP3053, TP3054		12	**15**	dBrnC0
		TP3054-1 (Note 1)			**16**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3057		−74	**−67**	dBm0p
		TP3057-1 (Note 1)			**−66**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	PCM Code is Alternating Positive and Negative Zero —				
		TP3052/53/54		8	**11**	dBrnC0
		TP3054-1			**13**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3057 PCM Code Equals Positive Zero —				
		TP3057-1		−82	**−79**	dBm0p
					−77	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI^+ = −50 dBm0				
		V_{CC} = 5.0 V_{DC} + 100 mVrms				
		f = 0 kHz–50 kHz (Note 2)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI^+ = −50 dBm0				
		V_{BB} = −5.0 V_{DC} + 100 mVrms				
		f = 0 kHz–50 kHz (Note 2)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero				
		V_{CC} = 5.0 V_{DC} + 100 mVrms				
		Measure VF_R0				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dB
		f = 25 kHz–50 kHz	**36**			dB
		f = 0–4 kHz (TP3054-1/57-1)	**38**			dBC
		f = 4–50 kHz (TP3054-1/57-1)	**35**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero				
		V_{BB} = −5.0 V_{DC} + 100 mVrms				
		Measure VF_R0				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dB
		f = 25 kHz–50 kHz	**36**			dB

Transmission Characteristics (Continued) Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = 5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R.			−30	dB
		4600 Hz–7600 Hz			−30	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			−30	dB
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3)				
		Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to −30 dBm0	**36**			dBC
		= −40 dBm0 XMT	**29**			dBC
		RCV	**30**			dBC
		= −55 dBm0 XMT	**14**			dBC
		RCV	**15**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_X+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz, D_R = Quiet PCM Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz, VF_XI = Multitone (Note 2)		−90	**−70**	dB

ENCODING FORMAT AT D_X OUTPUT

	TP3052, TP3053, TP3054 μ-Law								TP3057 A-Law (Includes Even Bit Inversion)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI+.

Note 3: Devices are measured using C message weighted filter for μ-Law and psophometric weighted filter for A-Law.

Applications Information

POWER SUPPLIES

While the pins of the TP3050A family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to the device as possible.

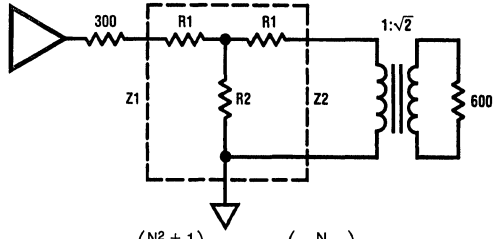
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050A family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

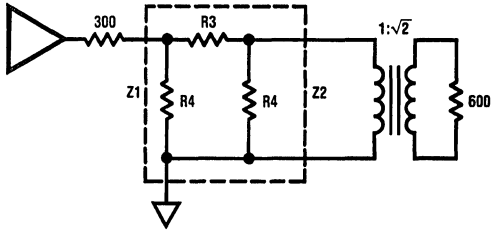
$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{SC} \bullet Z_{OC}}$$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination

π-Pad Attenuator



TL/H/5510–5

$$R3 = \sqrt{\frac{Z1 \cdot Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

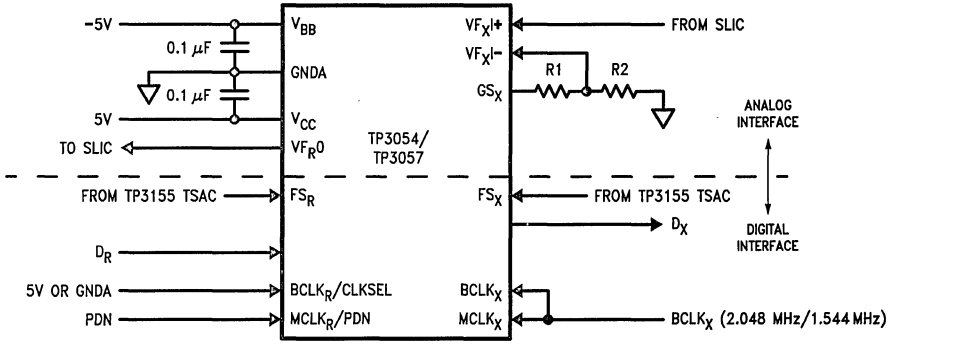
Note: See Application Note 370 for further details.

Applications Information (Continued)

TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6l	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



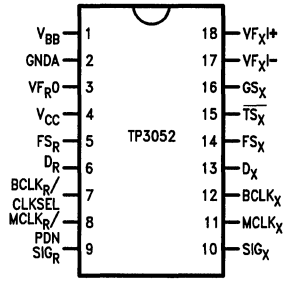
TL/H/5510–6

Note 1: XMIT gain = $20 \times \log \left(\frac{R1+R2}{R2} \right)$ where (R1 + R2) > 10 KΩ.

FIGURE 4

Connection Diagrams (Continued)

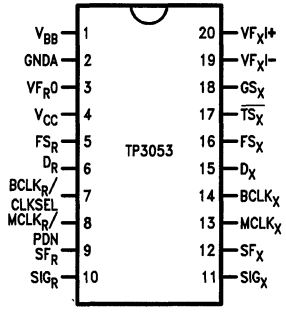
Dual-In-Line Package



TL/H/5510–8

Top View
Order Number TP3052J
See NS Package Number J18A

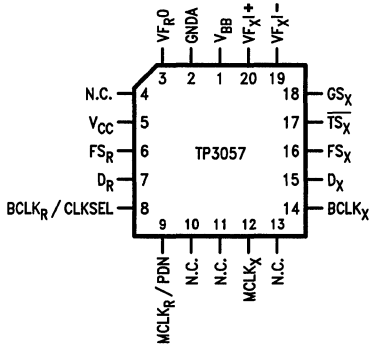
Dual-In-Line Package



TL/H/5510–9

Top View
Order Number TP3053J
See NS Package Number J20A

Plastic Chip Carrier



TL/H/5510–7

Top View
Order Number TP3057V*
See NS Package Number V20A
*Available mid 1990

National Semiconductor

PRELIMINARY

TP3052-X, TP3054-X, TP3057-X Extended Temperature "Ruggedized" Serial Interface CODEC/Filter COMBO® Family

General Description

The TP3052, TP3054, TP3057 family consists of μ-law and A-law monolithic PCM CODEC/filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

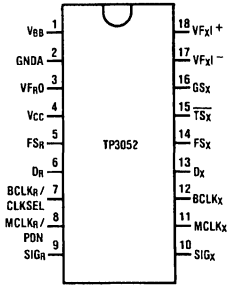
The encode portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are auto-zero circuitry and a companding coder which samples the filtered signal and encodes it in the companded μ-law or A-law PCM format. The decode portion of each device consists of an expanding decoder, which reconstructs the analog signal from the companded μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous; transmit and receive bit clocks, which may vary from 64 kHz to 2.048 MHz; and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- −40°C to +80°C operation
- Complete CODEC and filtering system (COMBO) including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
- μ-law with signaling, TP3020 or TP5116A timing—TP3052
- μ-law without signaling, 16-pin—TP3054
- A-law, 16-pin—TP3057
- Meets or exceeds all D3/D4 and CCITT specifications
- ±5V operation
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density
- Dual-In-Line or PCC surface mount packages

Connection Diagrams

Dual-In-Line Package

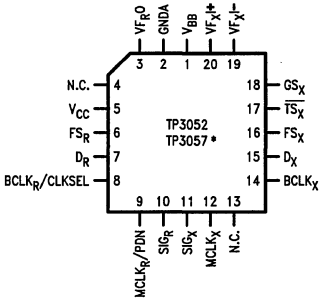


TL/H/8674–7

Top View

Order Number TP3052J-X
NS Package Number J18A

Plastic Chip Carriers



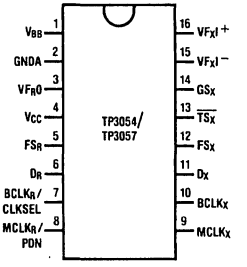
TL/H/8674–8

Top View

Order Number TP3052V-X or TP3057V-X
NS Package Number V20A

*TP3057 does not have SIG_R or SIG_X signalling features.

Dual-In-Line Package



TL/H/8674–1

Top View

Order Number TP3054J-X or TP3057J-X
NS Package Number J16A

Block Diagram

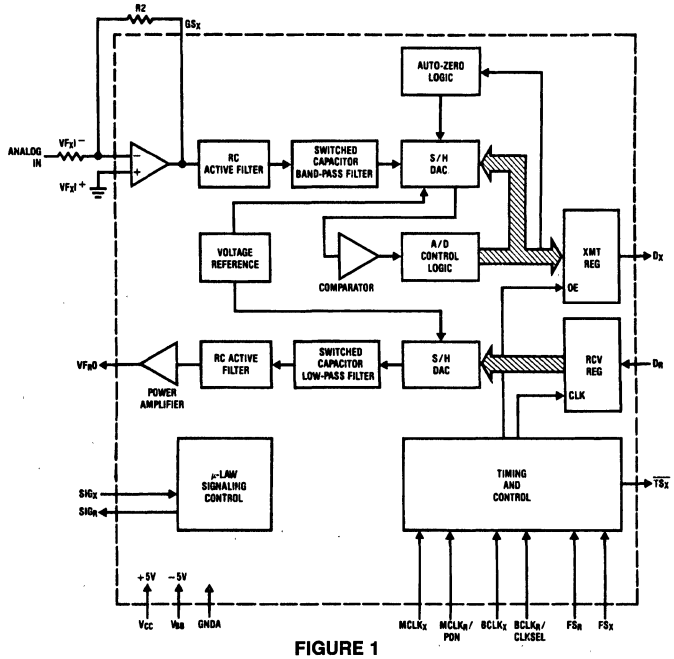


FIGURE 1

TL/H/8674–2

Pin Description

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.
GNDA	Analog ground. All signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table 1).
$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.

Symbol	Function
SIG_R	The eighth bit of the PCM data appears at this output after each receive signalling frame.
SIG_X	Signal data input. Data at this input is inserted into the 8th bit of the PCM word during transmit signaling frames.
$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and places it into a power-down state. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table I indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3057	TP3052 TP3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3057, or 1.536 MHz, 1.544 MHz for the TP3052, 54, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table I are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All four devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A/56A) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$ ($BCLK_X$ in synchronous mode). All four devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

SIGNALING

The TP3052 μ-law COMBOs contains circuitry to insert and extract signaling information in the PCM data stream. The TP3052 is intended for short frame sync applications. The TP3054 and TP3057 have no provision for signaling.

Functional Description (Continued)

Signaling for the TP3052 is accomplished by applying a frame sync pulse two bit clock periods long, as shown in *Figure 2*. With FS_X two bit clock periods long, the data present at SIG_X input will be inserted as the LSB in the PCM data transmitted during that frame. With FS_R two bit clock periods long, the LSB of the PCM data read into the D_R input will be latched and appear on the SIG_R output pin until updated following the next signaling frame. The decoder will then interpret the lost LSB as "½" to minimize noise and distortion. The TP3052 is not capable of inserting or extracting signaling information in the long frame mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3052, TP3054) or A-law (TP3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3057) or μ-law (TP3052, TP3054) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter/power amplifer capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is $\sim$ 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at any Digital Input or Output	V_{CC} + 0.3V to GNDA − 0.3V
Operating Temperature Range	−55°C to + 125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA SIG_R, I_L = 1.0 mA $\overline{TS_X}$, I_L = 3.2 mA, Open Drain			**0.4** **0.4** **0.4**	V V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA SIG_R, I_H = −1.0 mA	**2.4** **2.4**			V V
I_{IL}	Input Low Current	GNDA ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	**−10**		**10**	µA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−10**		**10**	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA ≤ V_O ≤ V_{CC}	**−10**		**10**	µA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, R_L ≥ 10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	60			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		−200		200	mV
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current	No Load (Note)		0.65	**2.0**	mA
$I_{BB}0$	Power-Down Current	No Load (Note)		0.01	**0.33**	mA
$I_{CC}1$	Power-Up (Active) Current	No Load		7.0	**11.0**	mA
$I_{BB}1$	Power-Up (Active) Current	No Load		7.0	**11.0**	mA

Note: I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

1

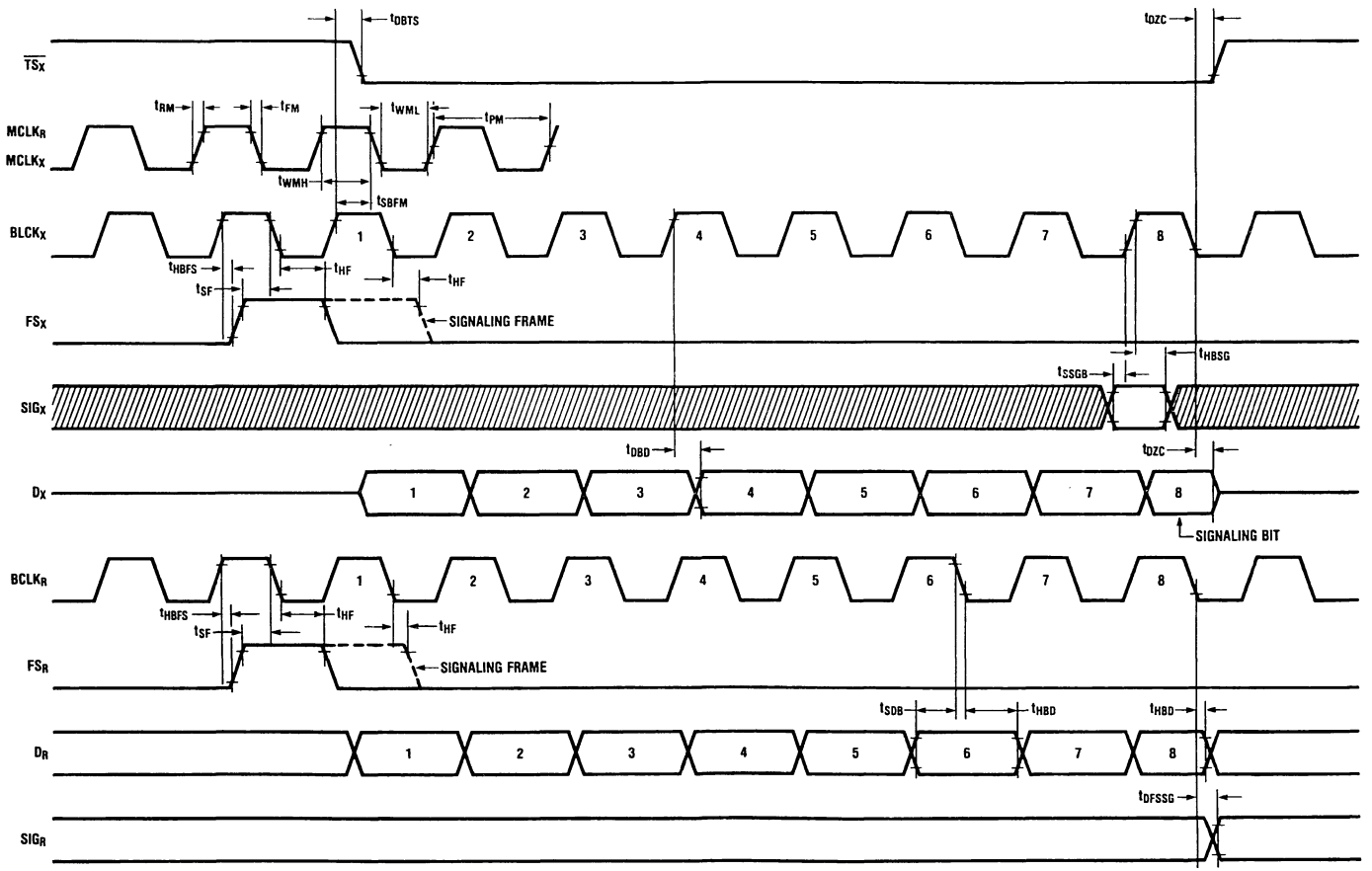
Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = 5.0V, T_A = 25°C.

All timing parameters are assured at V_{OH} = 2.0V and V_{OL} = 0.7V.

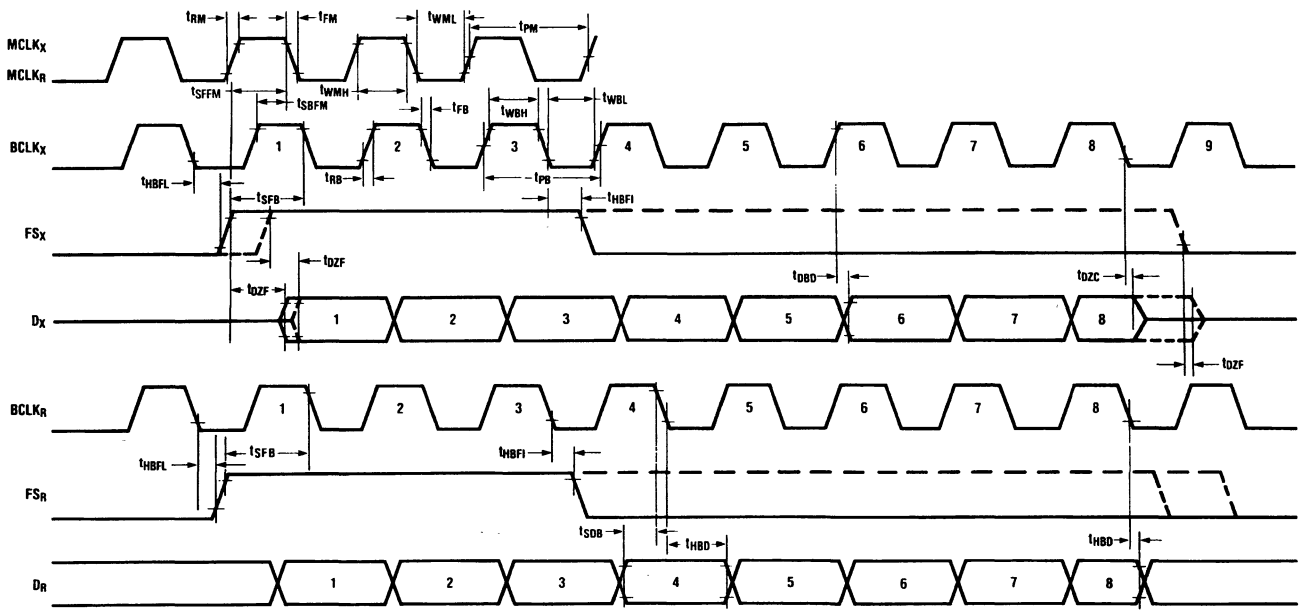
See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin. $MCLK_X$ and $MCLK_R$		1.536 1.544 **2.048**		MHz MHz MHz
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock		485	**488**	15725	ns
t_{RB}	Rise Time of Bit Clock	$BCLK_X$ and $BCLK_R$			50	ns
t_{FB}	Fall Time of Bit Clock	$BCLK_X$ and $BCLK_R$			50	ns
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X — Short Frame Long Frame	**100** **125**			ns
t_{SFFM}	Setup Time from FS_X High to $MCLK_X$ Falling Edge	Long Frame Only	**100**			ns
t_{WBH}	Width of Bit Clock High	V_{IH}=2.2V	**160**			ns
t_{WBL}	Width of Bit Clock Low	V_{IL}=0.6V	**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	**115**			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load=150 pF plus 2 LSTTL Loads	0		140	ns
t_{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load=150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled	C_L=0 pF to 150 pF	50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C_L=0 pF to 150 pF	20		165	ns
t_{SSGB}	Set-Up Time from SIG_X to $BCLK_X$	TP3052	**100**			ns
t_{HBSG}	Hold Time from $BCLK_X$ High to SIG_X	TP3052	**50**			ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		**50**			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		**50**			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	**160**			ns



TL/H/8674–3

FIGURE 2. Short Frame Sync Timing



TL/H/8674–9

FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of Nominal Gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		 1.2276		 Vrms
t_{MAX}		Max Overload Level TP3052, TP3054 (3.17 dBm0) TP3057 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input at GS_X=0 dBm0 at 1020 Hz	**−0.20**		**0.20**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16 Hz f=50 Hz f=60 Hz f=200 Hz f=300 Hz−3000 Hz f=3152 Hz f=3300 Hz f=3400 Hz f=4000 Hz f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−1.8** **−0.15** **−0.15** **−0.35** **−0.7**		−40 −30 **−26** **−0.1** **0.15** **0.20** **0.1** **0** **−14** **−32**	dB dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.15		0.15	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level=−10 dBm0 VF_XI+=−40 dBm0 to +3 dBm0 VF_XI+=−50 dBm0 to −40 dBm0 VF_XI+=−55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	 **−0.20**		 **0.20**	 dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0 Hz to 3000 Hz f=3300 Hz f=3400 Hz f=4000 Hz	**−0.15** **−0.35** **−0.7**		**0.15** **0.1** **0** **−14**	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.15		0.15	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Reletive to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded PCM Level=−40 dBm0 to +3 dBm0 PCM Level=−50 dBm0 to −40 dBm0 PCM Level=−55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
V_{RO}	Receive Output Drive Level	R_L=600Ω	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f=1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f=500 Hz–600 Hz		195	220	μs
		f=600 Hz–800 Hz		120	145	μs
		f=800 Hz–1000 Hz		50	75	μs
		f=1000 Hz–1600 Hz		20	40	μs
		f=1600 Hz–2600 Hz		55	75	μs
		f=2600 Hz–2800 Hz		80	105	μs
		f=2800 Hz–3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f=1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f=500 Hz–1000 Hz	−40	−25		μs
		f=1000 Hz–1600 Hz	−30	−20		μs
		f=1600 Hz–2600 Hz		70	90	μs
		f=2600 Hz–2800 Hz		100	125	μs
		f=2800 Hz–3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3052, TP3054 (Note 1)		12	**16**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3057 (Note 1)		−74	**−67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	PCM Code is Alternating Positive and Negative Zero — TP3052/54		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3057 PCM Code Equals Positive Zero —		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f=0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC}=5.0 V_{DC}+100 mVrms f=0 kHz–50 kHz (Note 2)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB}=−5.0 V_{DC}+100 mVrms f=0 kHz–50 kHz (Note 2)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC}=5.0 V_{DC}+100 mVrms Measure VF_R0				
		f=0 Hz–4000 Hz	**38**			dBC
		f=4 kHz–25 kHz	**38**			dB
		f=25 kHz–50 kHz	**35**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB}=−5.0 V_{DC}+100 mVrms Measure VF_R0				
		f=0 Hz–4000 Hz	**38**			dBC
		f=4 kHz–25 kHz	**38**			dB
		f=25 kHz–50 kHz	**35**			dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = −40°C to +85°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dBm0, transmit input amplifier connected for unity gain non inverting. Typicals are specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SOS	Spurious Out-of-Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R.			−30	dB
		4600 Hz–7600 Hz			−30	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			−30	dB
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3)				
		Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to −30 dBm0	**36**			dBC
		= −40 dBm0 XMT	**28**			dBC
		RCV	**29**			dBC
		= −55 dBm0 XMT	**13**			dBC
		RCV	**14**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−43**	dB
SFD_R	Single Frequency Distortion, Receive				**−43**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_X+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Quiet PCM Code (Note 4)		−90	**−70**	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz, VF_XI = Multitone (Note 2)		−90	**−70**	dB

ENCODING FORMAT AT D_X OUTPUT

	TP3052, TP3054 μ-Law								TP3057 A-Law (Includes Even Bit Inversion)							
V_{IN} (at GS_X) = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X) = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X) = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI^+.

Note 3: TP3052/54/57 are measured using C message weighted filter for μ-law and psophometric weighted filter for A-law.

Note 4: CT_{X-R} @ 1.544 MHz $MCLK_X$ freq. is −70 dB max. 50% ±5% $BCLK_X$ duty cycle.

Applications Information

POWER SUPPLIES

While the pins of the TP3050 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to device pins as possible.

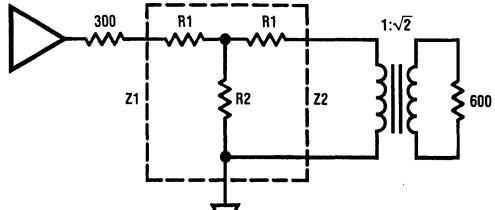
For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus.

This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1 \cdot Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

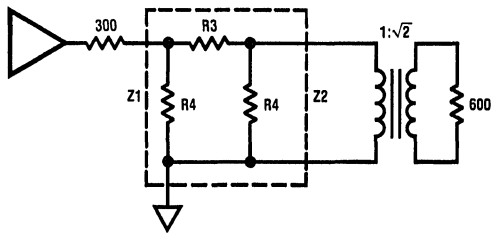
$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{SC} \bullet Z_{OC}}$$

Where Z_{SC} = impedance with short circuit termination

and Z_{OC} = impedance with open circuit termination

π-Pad Attenuator



TL/H/8674–5

$$R3 = \sqrt{\frac{Z1 \cdot Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

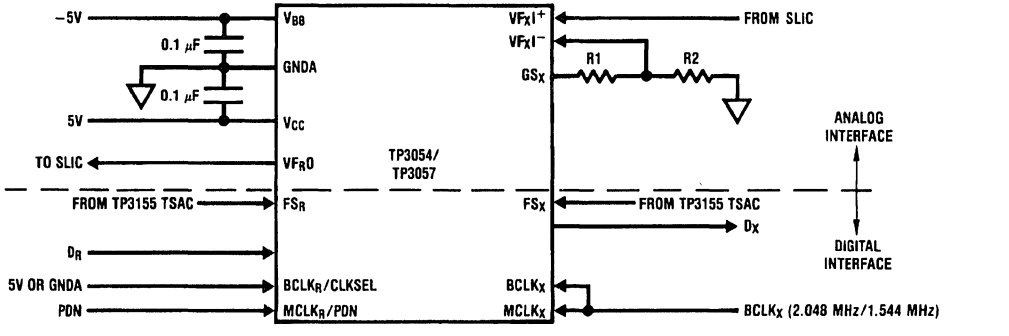
Note: See Application Note 370 for further details.

Applications Information (Continued)

TABLE II. Attentuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6l	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



TL/H/8674–6

Note 1: XMIT gain = $20 \times \log \left(\frac{R1+R2}{R2} \right)$, (R1 + R2) > 10 KΩ.

FIGURE 4

National Semiconductor

TP3058, TP3059 Microprocessor Compatible COMBO®

General Description

The TP3058, TP3059 family consists of a μ-law and A-law monolithic PCM COMBO set utilizing the A/D and D/A conversion architecture shown in *Figure 1* and a parallel I/O microprocessor bus interface. The devices are fabricated using National's advanced double poly microCMOS process.

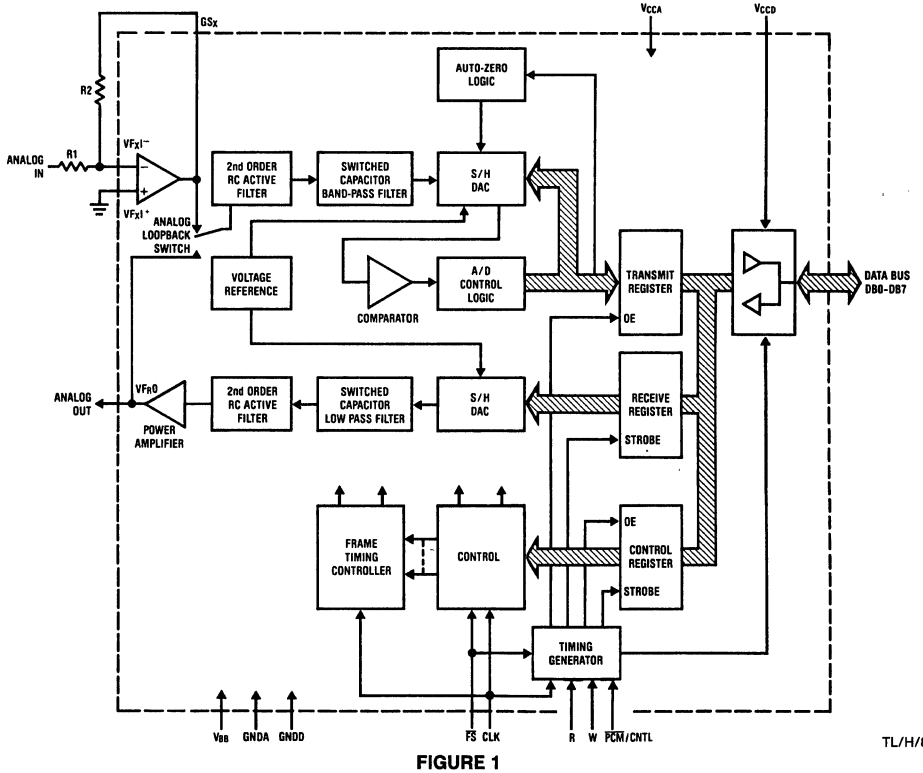
The transmit section consists of an input gain adjust amplifier, an active RC pre-filter, and a switched-capacitor bandpass filter that rejects signals below 200 Hz and above 3400 Hz. A compressing coder samples the filtered signal and encodes it in the μ-225 law or A-law PCM format. Autozero circuitry is included on-chip. The receive section consists of an expanding decoder which reconstructs the analog signal from the compressed μ-law or A-law code, and a low pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz. The receive output is a single-ended power amplifier capable of driving low impedance loads.

The TP3058 μ-law and TP3059 A-law devices are pin compatible parallel interface CODEC/filters for microprocessor and digital signal processor systems.

Features

- Complete CODEC and filtering system including:
  - — Transmit high pass and low pass filtering
  - — Receive low pass filter with sin x/x correction
  - — Receive power amplifier
  - — Active RC noise filters
  - — μ-255 law COder and DECoder—TP3058
  - — A-law COder and DECoder—TP3059
  - — Internal precision voltage reference
  - — Internal auto-zero circuitry
- Meets or exceeds all LSSGR and CCITT specifications
- Microprocessor interface independant of frame sync
- Low operating power—typically 60 mW
- Power-down standby mode—typically 3 mW
- 2 loopback test modes

Block Diagram

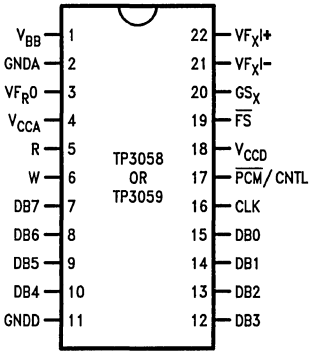


TL/H/8833–1

FIGURE 1

Connection Diagram

Dual-In-Line Package



TL/H/8833–2

Top View

Order Number TP3058J or TP3059J
See NS Package Number J22A

Pin Descriptions

Symbol	Function
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$
GNDA	Analog ground. All analog signals are referenced to this pin.
VF_RO	Analog output of the receive power amplifier. This output can drive a 600Ω load to ±2.5V.
V_{CCA}	Positive power supply voltage pin for the analog circuitry. $V_{CCA} = 5V \pm 5\%$. Must be connected to V_{CCD}.
DB7	Bit 7 I/O on the data bus. The PCM LSB.
DB6	Bit 6 I/O on the data bus.
DB5	Bit 5 I/O on the data bus
DB4	Bit 4 I/O on the data bus.
GNDD	Digital ground. All digital signals are referenced to this pin.
DB3	Bit 3 I/O on the data bus.
DB2	Bit 2 I/O on the data bus.
DB1	Bit 1 I/O on the data bus.
DB0	Bit 0 I/O on the data bus. This is the PCM sign bit.

Symbol	Function
CLK	The clock input for the switched-capacitor filters and CODEC. Clock frequency must be 768 kHz, 772 kHz, 1.024 MHz or 1.28 MHz and must be synchronous with the μC system clock.
$\overline{FS}$	Frame sync input, which starts a new Encode and Decode cycle. Must occur at an 8 kHz rate to meet CCITT and LSSGR specifications.
R	Input from the Microprocessor READ signal, which enables the COMBO bus drivers. May be asynchronous with $\overline{FS}$.
W	Input from the Microprocessor WRITE signal, which enables the COMBO bus receivers. May be asynchronous with $\overline{FS}$.
$\overline{PCM}$/ CNTL	This control input determines whether the information on the data bus is PCM data or control data.
V_{CCD}	Positive power supply pin for the bus drivers. $V_{CCD} = 5V \pm 5\%$. Must be connected to V_{CCA}.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO and sets it in the power-down mode. All non-essential circuits are deactivated and the data bus outputs, DB0–DB7, and receive power amplifier output, VF_RO, are in high impedance states.

The TP3058 and TP3059 are powered-up via a command to the control register (see Control Register Functions). This sets the device in the standby mode with all circuitry activated, but encoding and decoding do not begin until PCM READ and PCM WRITE chip selects occur.

TABLE I. Control Bit Functions

Control Bits	Function
C0, C1	Select Clock Frequency **C0** **C1** **Frequency** 0 X 1.024 MHz 1 0 0.768 MHz or 0.772 MHz 1 1 1.28 MHz
C2, C3	Digital and Analog Loopback **C2** **C3** **Mode** 1 X digital loopback 0 1 analog loopback 0 0 normal
C4	Power-Down/Power-Up 1 = power-down 0 = power-up
C5	TP3058—Don't care (Note 1) TP3059 1 = Not implemented. Do not use 0 = A-law with even bit inversion
C6–C7	Don't Care (Note 1)

Note 1: These bits are always set to "1" when reading back the control register.

DATA BUS NOMENCLATURE

The order of the data bus is as follows:

Data Type	DB0	DB7
PCM	Sign Bit	LSB
Control Data	C0	C7

MICROPROCESSOR WRITING THE BUS

The microprocessor may write to either the Control Register or PCM Receive Register by first setting up the $\overline{PCM}$/CNTL address bit during a WRITE cycle. A CNTL WRITE may take place at any time without restriction, during either the powered-up or powered-down state.

A PCM WRITE cycle normally occurs once per frame, and may occur any time in the frame except during the $\overline{FS}$ falling edge. PCM data is held in a register and will not update the DAC until the next $\overline{FS}$ pulse starts a new decoding cycle.

MICROPROCESSOR READING THE BUS

The microprocessor may read either the Control Register, to verify the status of the device, or the PCM Transmit Register. Selection is again by means of the $\overline{PCM}$/CNTL address input. A CNTL READ may take place at any time without restriction, during either the powered-up or powered-down state. A PCM READ cycle normally occurs once per frame, and may occur any time in the frame except during the $\overline{FS}$ falling edge.

COMBO TIMING

The CLK input signal provides timing for the encode and decode logic and the switched-capacitor filters. It must be one of the frequencies listed in Table I and must be correctly selected by control bits C0 and C1. $\overline{FS}$ is a sync input which starts both the Encode and Decode cycles. It must be an integer sub-multiple of CLK, and must occur at an 8 kHz rate to meet CCITT and LSSGR transmission specifications.

CONTROL REGISTER FUNCTIONS

Writing to the control register (see Table I) allows the user to set the various operating states of the TP3058 and TP3059. The control register can also be read back via the data bus to verify the current operating mode of the device.

1. CLK Select

   Since one of three distinct clock frequencies may be used, the actual frequency must be known by the device for proper operation of the switched-capacitor filters. This is achieved by writing control register bits C0 and C1, normally in the same WRITE cycle that powers-up the device, and before any PCM data transfers take place.

2. Digital Lookback

   In order to establish that a valid path has been selected through a network, it is sometimes desirable to be able to send data through the network to its destination, then loop it back through the network return path to the originating source where the data can be verified. This loopback function can be performed in the TP3058 and TP3059 by setting control register bit C2 to 1. With C2 set, the PCM data in the receive register will be written back onto the data bus during the next PCM WRITE cycle. In the digital loopback mode, the receive section is set to an idle channel condition in order to maintain a low impedance termination at VF_RO.

3. Analog Loopback

   In the analog loopback mode, the transmit filter input is switched from the gain adjust amplifier to the receive power amplifier output, forming a unity-gain loop from the receive register back to the transmit register. This mode is entered by setting control register bits C2 to 0 and C3 to 1. The receive power amplifier continues to drive the load in this mode.

4. Power-Down/Power-Up

   The TP3058, TP3059 may be put in the power-down mode by setting control register bit C4 to 1. Conversely, settng bit C4 to 0 powers-up the device.

Functional Description (Continued)

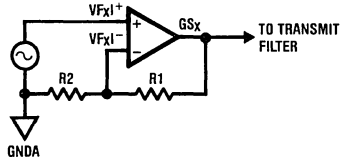
TRANSMIT FILTER AND ENCODE SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 2*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of a 2nd order RC active pre-filter, followed by an 8th order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-255 law (TP3058) or A-law (TP3059) coding schemes. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see table of Transmission Characteristics). Any offset voltage due to the filters or comparator is cancelled by sign bit integration in the auto-zero circuit.

The total encoding delay referenced to a frame sync input select will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs.

TRANSMIT GAIN ADJUSTMENT

Figure 2 shows the connections for setting the Transmit input amplifier in non-inverting mode. Gains in excess of 20 dB can be obtained with this amplifier without significantly impairing the transmission performance of the device.



TL/H/8833-3

$$\text{Non-inverting transmit gain} = 20 \log_{10}\left(\frac{R1 + R2}{R2}\right)$$

Set gain to provide peak overload level = t_{MAX} at GS_X (see Transmission Characteristics)

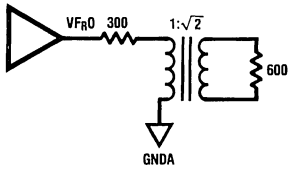
FIGURE 2. Transmit Gain Adjustment

DECODER AND RECEIVE FILTER SECTION

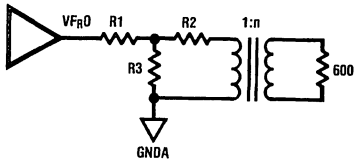
The receive section consists of an expanding DAC which drives a 5th order switched-capacitor low pass filter clocked at 256 kHz. The decoder is of A-law (TP3059) or μ-law (TP3058) coding law and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter. The power amplifier output stage is capable of driving a 600Ω load to a level of 7.2 dBm. The receive section has unity-gain. Each decoding cycle begins just prior to a $\overline{FS}$ pulse. The total decoder delay is 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 170 μs, relative to the $\overline{FS}$ pulse following the microprocessor PCM WRITE cycle.

RECEIVE GAIN ADJUSTMENT

Receive gain adjustments with a high impedance load can be implemented with a simple 2-resistor potentiometer. Gain adjustments requiring matching to a transformer should use the equations given in the Applications section.



Maximum output power = 7.2 dBm total, 4.2 dBm to the load.



TL/H/8833-8

See Applications information for attenuator design guide.

FIGURE 3. Receive Gain Adjustment

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

GNDD to GNDA	±0.3V
V_{CCA} or V_{CCD} to GNDD or GNDA	7V
V_{BB} to GNDD or GNDA	−7V
Voltage at Any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at Any Digital Input or Output	V_{CC} + 0.3V to GNDD − 0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Electrical Characteristics

Unless otherwise noted: $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, T_A = 0°C to 70°C; typical characteristics specified at nominal supply voltages, T_A = 25°C; all digital signals are referenced to GNDD, all analog signals are referenced to GNDA. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design characterizations.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	DB0–DB7, I_L = 2.5 mA			**0.4**	V
V_{OH}	Output High Voltage	DB0–DB7, I_H = 2.5 mA	**2.4**			V
I_{IL}	Input Low Current	GNDD ≤ V_{IN} ≤ V_{IL}	**−3**		**3**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−3**		**3**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE®)	DB0–DB7, GNDD ≤ V_O ≤ V_{CC}	**−3**		**3**	μA
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER						
I_IXA	Input Leakage Current	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	−2.5V ≤ V ≤ +2.5V, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance, GS_X	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance, GS_X		10			kΩ
C_LXA	Load Capacitance, GS_X				50	pF
V_OXA	Output Dynamic Range, GS_X	R_L = 10 kΩ	**−2.8**		**2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	**−2.5**		**2.5**	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	**60**			dB
RECEIVE POWER AMPLIFIER						
R_ORF	Output Resistance, VF_RO			1	3	Ω
R_LRF	Load Resistance	VF_RO = ±2.5V	600			Ω
C_LRF	Load Capacitance				50	pF
VOS_RO	Output DC Offset Voltage		**−200**		**200**	mV
POWER DISSIPATION						
I_{CC0}	Power-Down Current	No Load (Note †)		0.5	**1.5**	mA
I_{BB0}	Power-Down Current	No Load (Note †)		0.05	**0.3**	mA
I_{CC1}	Active Current	No Load		6.0	**9.0**	mA
I_{BB1}	Active Current	No Load		6.0	**9.0**	mA

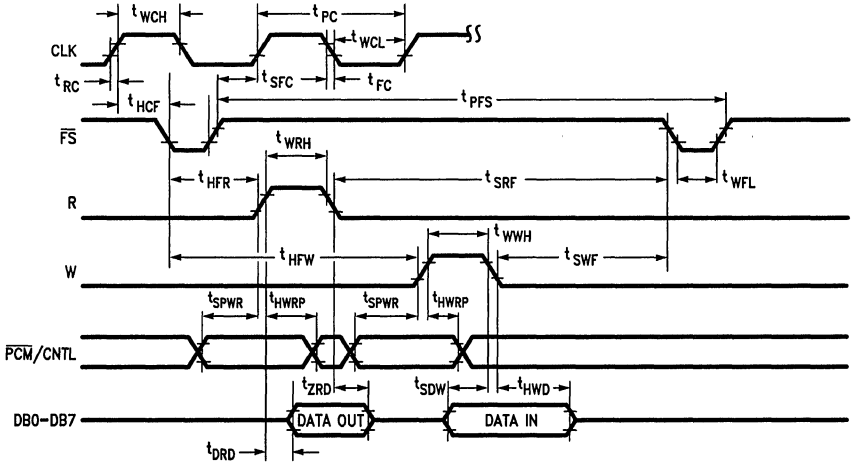
† I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

Timing Specifications

Unless otherwise noted, $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$, GNDA = 0V, $T_A = 0°C$ to 70°C; typical characteristics specified at $V_{CCA} = V_{CCD} = 5.0V$, $V_{BB} = -5.0V$, $T_A = 25°C$; all signals are referenced to GNDA. Timing specifications are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to 70°C by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design characterizations. See Definitions and Timing Conventions for test methods information.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock		760		ns
t_{WCH}	Width of Clock High		**330**		ns
t_{WCL}	Width of Clock Low		330		ns
t_{RC}	Rise Time of Clock			50	ns
t_{FC}	Fall Time of Clock			50	ns
t_{WFL}	Width of $\overline{FS}$ Low		200	 100	ns µs
t_{HFR}	Hold Time, $\overline{FS}$ Low to R	PCM READ Only	100		ns
t_{SRF}	Set-Up Time, R Low to $\overline{FS}$	PCM READ Only	100		ns
t_{HFW}	Hold Time, $\overline{FS}$ Low to W	PCM WRITE Only	100		ns
t_{SWF}	Set-Up Time, W Low to $\overline{FS}$	PCM WRITE Only	100		ns
t_{WRH}	Width of R High		75		ns
t_{WWH}	Width of W High		125		ns
t_{DRD}	Delay Time, R to Data Valid	$C_L = 100$ pF		65	ns
t_{ZRD}	Float Delay, R Low to DB High-Z		0	80	ns
t_{SDW}	Set-Up Time, DB to W Low		75		ns
t_{HWD}	Hold Time, W Low to DB		25		ns
t_{SPWR}	Set-Up Time, $\overline{PCM}$/CNTL to R or W		**20**		ns
t_{HWRP}	Hold-Time, W or R to $\overline{PCM}$/CNTL		100		ns
t_{HCF}	Hold-Time, $\overline{FS}$ Low after CLK High		100		ns
t_{SFC}	Set-Up Time, $\overline{FS}$ High to CLK High		100		ns
t_{PFS}	Period of $\overline{FS}$ (Note 4)	CLK = 1.024 MHz	70		µs

Timing Diagram



TL/H/8833–4

Transmission Characteristics

Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% testing at $T_A = 25°C$. All other limits are assured by correlation with production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	Nominal 0 dBm0 Level is 4 dBm (600Ω)				
	0 dBm0	TP3058		1.2276		Vrms
		TP3059		1.2276		Vrms
t_{MAX}	Maximum Overload Level	TP3058 (+3.17 dBm0)		2.501		V_{PK}
		TP3059 (+3.14 dBm0)		2.492		V_{PK}
G_{XA}	Transmit Gain, Absolute	$T_A = 25°C$, $V_{CCA} = V_{CCD} = 5.0V$, $V_{BB} = -5.0V$ Input at GS_X = 0 dBm0 at 1020 Hz	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f = 16 Hz			**−40**	dB
		f = 50 Hz			**−30**	dB
		f = 60 Hz			**−26**	dB
		f = 200 Hz	**−1.8**		**−0.1**	dB
		f = 300 Hz–3000 Hz	**−0.15**		**0.15**	dB
		f = 3300 Hz	**−0.35**		**0.1**	dB
		f = 3400 Hz	**−0.7**		**0**	dB
		f = 4000 Hz			**−14**	dB
		f = 4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz			**−32**	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variation with Level	Sinusoidal Test Method				
		Reference Level = −10 dBm0				
		$VF_{XI}+$ = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		$VF_{XI}+$ = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		$VF_{XI}+$ = −55 dBm0 to −50 dBm0	**1.2**		**1.2**	dB
G_{RA}	Receive Gain, Absolute	$T_A = 25°C$, $V_{CCA} = V_{CCD} = 5V$, $V_{BB} = -5V$ Input = Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	**−0.15**		**0.15**	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f = 0 Hz to 3000 Hz	**−0.15**		**0.15**	dB
		f = 3300 Hz	**−0.35**		**0.05**	dB
		f = 3400 Hz	**−0.7**		**0**	dB
		f = 4000 Hz			**−14**	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variation with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded				
		PCM Level = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		= −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		= −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
V_{RO}	Receive Output Drive Level	$R_L = 600Ω$	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for $V_{CCA} = V_{CCD} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% testing at $T_A = 25°C$. All other limits are assured by correlation with production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz–600 Hz		195	220	μs
		f = 600 Hz–800 Hz		120	145	μs
		f = 800 Hz–1000 Hz		50	75	μs
		f = 1000 Hz–1600 Hz		20	40	μs
		f = 1600 Hz–2600 Hz		55	75	μs
		f = 2600 Hz–2800 Hz		80	105	μs
		f = 2800 Hz–3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz–1000 Hz	−40	−25		μs
		f = 1000 Hz–1600 Hz	−30	−20		μs
		f = 1600 Hz–2600 Hz		70	90	μs
		f = 2600 Hz–2800 Hz		100	125	μs
		f = 2800 Hz–3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3058, (Note 1)		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted	TP3059, (Note 1)		−74	**−69**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	TP3058, PCM Code Equals Alternating Positive and Negative Zero		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted	TP3059, PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, $VF_XI+ = 0V$			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	$V_{CCA} = V_{CCD} = 5.0\ V_{DC} + 100$ mVrms f = 0 kHz–50 kHz (Note 2)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	$V_{BB} = -5.0\ V_{DC} + 100$ mVrms f = 0 kHz–50 kHz (Note 2)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3058 and TP3059 $V_{CC} = 5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dB
		f = 25 kHz–50 kHz	**36**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero for TP3058 and TP3059 $V_{BB} = -5.0\ V_{DC} + 100$ mVrms				
		f = 0 Hz–4000 Hz	**40**			dBC
		f = 4 kHz–25 kHz	**40**			dB
		f = 25 kHz–50 kHz	**36**			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz–3400 Hz Input Applied to VF_XI+, Measure Individual Image Signals at VF_RO				
		4600 Hz–7600 Hz			**−32**	dB
		7600 Hz–8400 Hz			−40	dB
		8400 Hz–100,000 Hz			**−32**	dB

Transmission Characteristics (Continued)

(All Devices) Unless otherwise specified: $T_A = 0°C$ to $70°C$, $V_{CCA} = V_{CCD} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, GNDD = GNDA = 0V, f = 1.02 kHz, $V_{IN} = 0$ dBm0, transmit input amplifier connected for unity-gain non-inverting. Limits printed in **BOLD** characters are guaranteed for $V_{CC} = 5.0V \pm 5\%$ and $V_{BB} = -5.0V \pm 5\%$; $T_A = 0°C$ to $70°C$ by correlation with 100% testing at $T_A = 25°C$. All other limits are assured by correlation with production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3) Level = 3.0 dBm0 = 0 dBm0 to −30 dBm0 = −40 dBm0 XMT RCV = −55 dBm0 XMT RCV	 **33** **36** **29** **30** **14** **15**			 dB dB dB dB dB dB
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk 0 dBm0 Transmit Level	f = 300 Hz–3000 Hz at 0 dBm0 Transmission Level Steady PCM Receive Code		−90	**−70**	dB
CT_{R-X}	Receive to Transmit Crosstalk 0 dBm0 Receive Level	f = 300 Hz–3000 Hz at 0dBm0 Transmit Level (Note 2)		−90	**−70**	dB

Note 1: Measured by extrapolation from the distortion test result. At −50 dBm0

Note 2: CT_{R-X}, $PPSR_X$, and $NPSR_X$ are measured with a −50 dBm0 activation signal applied at VF_XI^+.

Note 3: Using C message weighted filter.

Note 4: Must be 125 μs to meet CCITT and LSSGR specifications.

Encoding Format At Data Bus Output

	TP3058 μ-Law								TP3059 True A-Law, C5 = 0 (Includes Even Bit Inversion)							
	MSB							LSB	MSB							LSB
V_{IN} = + Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = − Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Applications Information

POWER SUPPLIES

While the pins of the TP3058/9 family are well protected against electrical misuse, however, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used. GNDA and GNDD MUST be connected together adjacent to each COMBO, not on the connector or backplane wiring.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CCA} and V_{BB}.

For best performance, the ground point of each COMBO on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

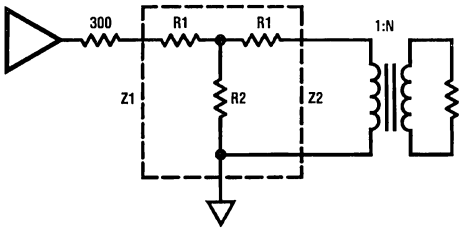
The positive power supply to the bus drivers, V_{CCD}, is provided on a separate pin from the positive supply for the COMBO circuits to minimize noise injection when driving the bus. V_{CCA} and V_{CCD} MUST be connected together close to the COMBO at the point where the 0.1 μF decoupling capacitor is connected.

Application Note AN370 provides further guidance on board layout techniques.

RECEIVE GAIN ADJUSTMENT

For applications where a TP3050 family CODEC/filter receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output as shown in *Figure 4*. Table II lists the required resistor values for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors. It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



TL/H/8833–5

$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1Z2}\left(\frac{N}{N^2-1}\right)$$

$$\text{Where: } N = \sqrt{\frac{\text{POWER IN}}{\text{POWER OUT}}}$$

and

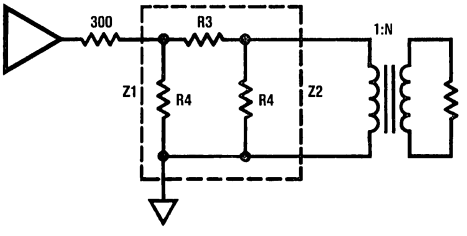
$$S = \sqrt{\frac{Z1}{Z2}}$$

$$\text{Also: } Z = \sqrt{Z_{SC}\,Z_{OC}}$$

Where Z_{SC} = Impedance with short circuit termination

and Z_{OC} = Impedance with open circuit termination

π-Pad Attenuator



TL/H/8833–6

$$R3 = \sqrt{\frac{Z1Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

$$R4 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

FIGURE 4. Receive Gain Adjustment for Matched Loads

Applications Information (Continued)

TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω (All Values in Ω)

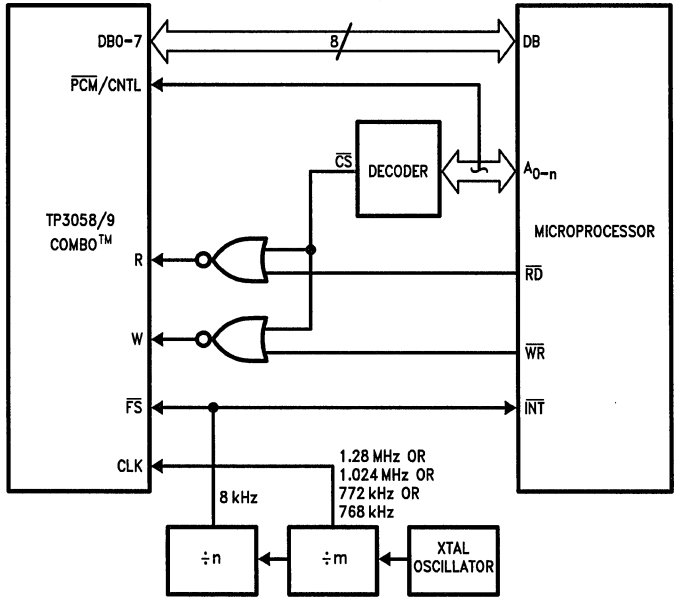
dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	8.7k	10.4	17.4k
0.4	6.9	6.5k	13.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.7	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900

TABLE II. Attenuator Tables for Z1 = Z2 = 300Ω (All Values in Ω) (Continued)

dB	R1	R2	R3	R4
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	816	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Application

Figure 5 shows a typical application of the TP3058/9 with a microprocessor having non-multiplexed address and data ports. The COMBO clocks, CLK and $\overline{FS}$, are derived from a crystal-controlled counter chain. The 8 kHz $\overline{FS}$ signal is also used as an Interrupt to the processor, prompting it to generate a PCM READ and PCM WRITE cycle sometime during the next frame period.



TL/H/8833–7

FIGURE 5. Typical Application

National Semiconductor

TP3064, TP3067
Monolithic Serial Interface CMOS CODEC/Filter COMBO®

General Description

The TP3064 (μ-law) and TP3067 (A-law) are monolithic PCM CODEC/Filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

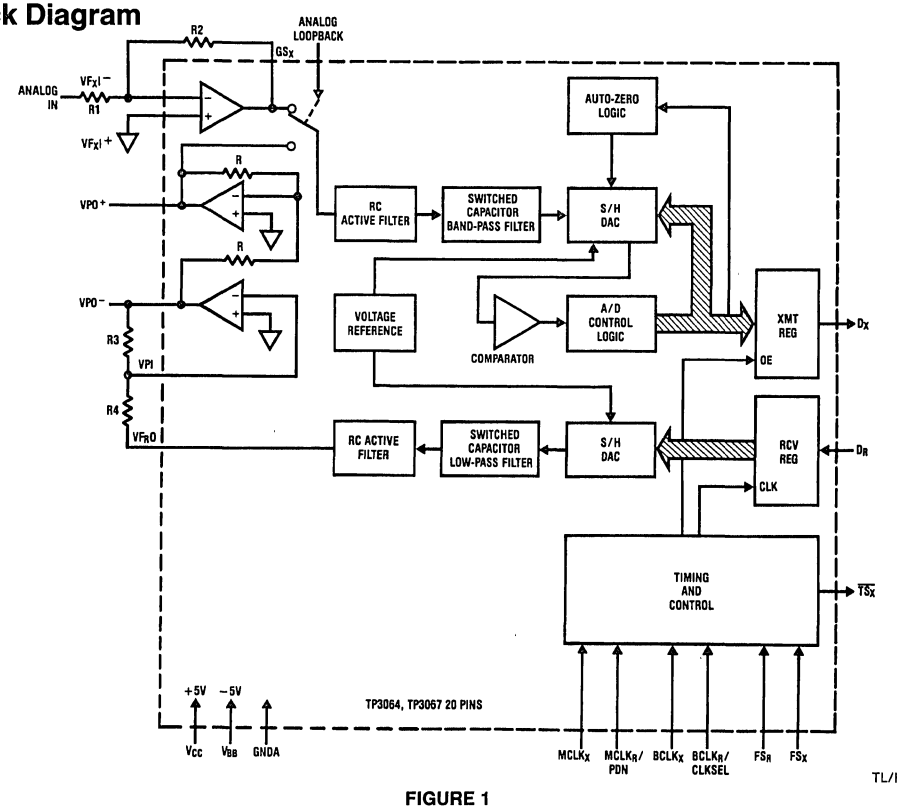
Similar to the TP3050 family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ± 6.6V across a balanced 600Ω load.

Also included is an Analog Loopback switch and a $\overline{TS_X}$ output.

Features

- Complete CODEC and filtering system including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
  - — Receive push-pull power amplifiers
- μ-law—TP3064
- A-law—TP3067
- Meets or exceeds all D3/D4 and CCITT specifications
- ± 5V operation
- Low operating power—typically 70 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

Block Diagram

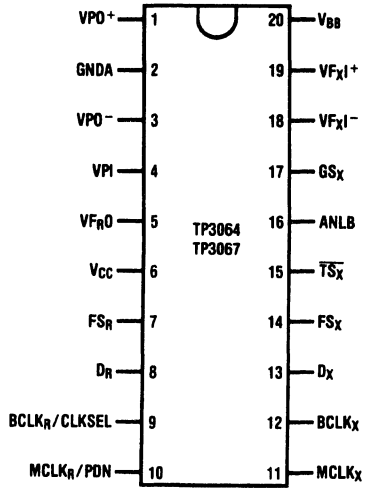


TL/H/5070–1

FIGURE 1

Connection Diagrams

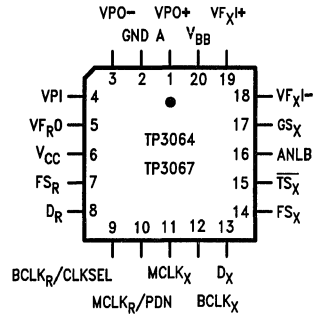
Dual-In-Line Package



TL/H/5070-2

Top View

Plastic Chip Carrier



TL/H/5070-6

Top View

Order Number TP3064V, TP3064V-1 or TP3067V or TP3067V-1
See NS Package V20A

Order Number TP3064J, TP3067J
See NS Package J20A

Pin Description

Symbol	Function
VPO^+	The non-inverted output of the receive power amplifier.
GNDA	Analog ground. All signals are referenced to this pin.
VPO^-	The inverted output of the receive power amplifier.
VPI	Inverting input to the receive power amplifier.
VF_RO	Analog output of the receive filter.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table I).
$MCLK_R$/ PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
ANLB	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the VPO^+ output of the receive power amplifier.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
VF_XI^-	Inverting input of the transmit input amplifier.
VF_XI^+	Non-inverting input of the transmit input amplifier.
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO™ and places it into a power-down state. All non-essential circuits are deactivated and the D_X, VF_RO, VPO^- and VPO^+ outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BLCK_X$ will be selected as the bit clock for both the transmit and receive directions. Table I indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3067	TP3064
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3067, or 1.536 MHZ, 1.544 MHz for the TP3064, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table I are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A/56 CODECs) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$($BCLK_X$ in synchronous mode). All devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3064) or A-law (TP3067) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see

Functional Description (Continued)

table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3067) or μ-law (TP3064) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at VF_RO. The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5V peak output signal from the receive filter up to ±3.3V peak into an unbalanced 300Ω load, or ±4.0V into an unbalanced 15 kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$:1 turns ratio, as shown in *Figure 4*. A total peak power of 15.6 dBm can be delivered to the load plus termination.

ENCODING FORMAT AT D_X OUTPUT

	TP3064 μ-Law								TP3067 A-Law (Includes Even Bit Inversion)							
V_{IN} = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	$V_{CC}+0.3V$ to $V_{BB}-0.3V$
Voltage at any Digital Input or Output	$V_{CC}+0.3V$ to GNDA−0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current	(Note)		0.5	**1.5**	mA
$I_{BB}0$	Power-Down Current	(Note)		0.05	**0.3**	mA
$I_{CC}1$	Active Current	VPI = 0V; VF_RO, VPO+ and VPO− unloaded		7.0	**10.0**	mA
$I_{BB}1$	Active Current	VPI = 0V; VF_RO, VPO+ and VPO− unloaded		7.0	**10.0**	mA
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA $\overline{TS_X}$, I_L = 3.2 mA, Open Drain			**0.4** **0.4**	V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA	**2.4**			V
I_{IL}	Input Low Current	GNDA ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	**−10**		**10**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA ≤ V_O ≤ V_{CC}	**−10**		**10**	μA

Note: I_{CC0} and I_{BB0} are measured after first achieving a power-up state.

Electrical Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V±5%, V_{BB} = −5.0V±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

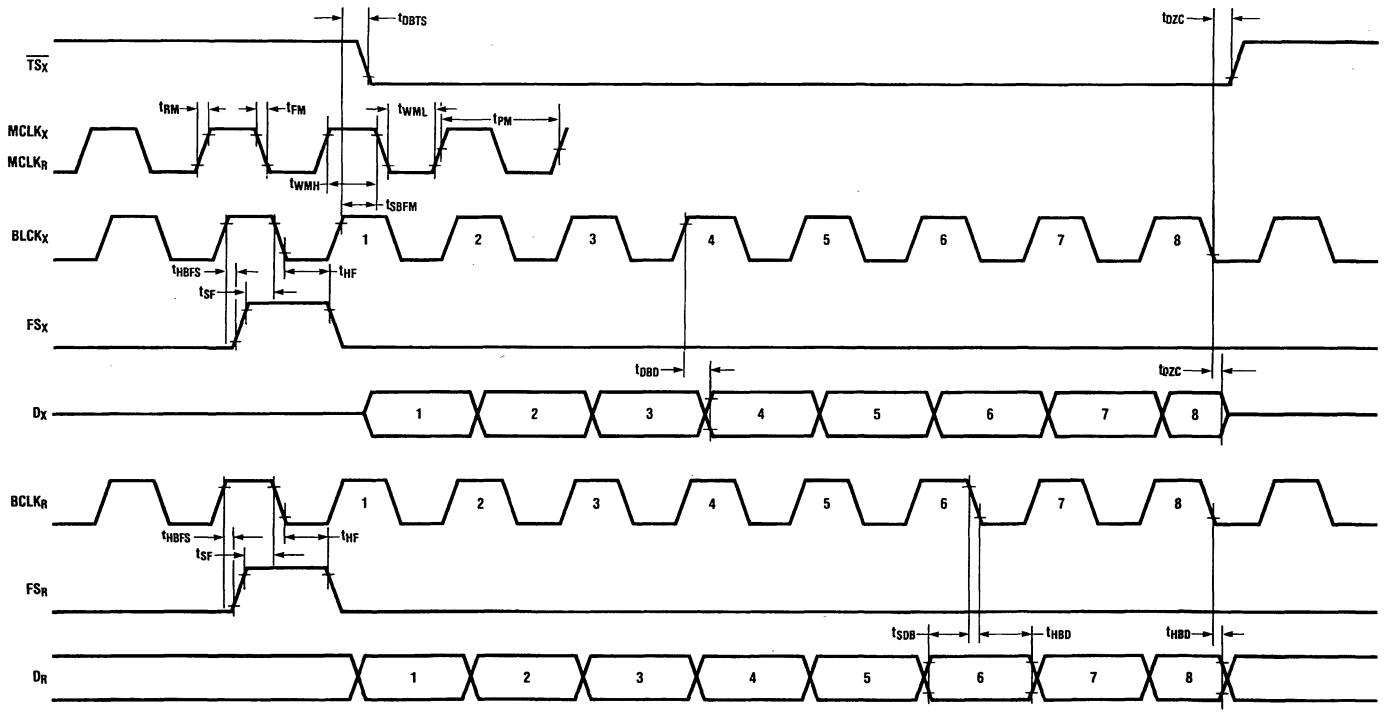
Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L \ge 10$ kΩ	**−2.8**		**+2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	**−2.5**		**2.5**	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	**60**			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	$VF_RO = \pm 2.5V$	10			kΩ
C_LRF	Load Capacitance	Connect from VF_RO to GNDA			25	pF
VOS_RO	Output DC Offset Voltage	Measure from VF_RO to GNDA	**−200**		**200**	mV
ANALOG INTERFACE WITH POWER AMPLIFIERS (ALL DEVICES)						
IPI	Input Leakage Current	$-1.0V \le VPI \le 1.0V$	**−100**		**100**	nA
RIPI	Input Resistance	$-1.0V \le VPI \le 1.0V$	10			MΩ
VIOS	Input Offset Voltage		**−25**		**25**	mV
ROP	Output Resistance	Inverting Unity-Gain at VPO^+ or VPO^-		1		Ω
F_C	Unity-Gain Bandwidth	Open Loop (VPO^-)		400		kHz
C_LP	Load Capacitance				100	pF
GA_P^+	Gain from VPO^- to VPO^+	$R_L = 600\Omega$ VPO^+ to VPO^- Level at $VPO^- = 1.77$ Vrms		−1		V/V
$PSRR_P$	Power Supply Rejection of V_{CC} or V_{BB}	VPO^- Connected to VPI 0 kHz−4 kHz 4 kHz−50 kHz	 60 36			 dB dB
R_LP	Load Resistance	Connect from VPO^+ to VPO^-	600			Ω

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%, T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals are referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	MCLK$_X$ and MCLK$_R$		1.536 **1.544** **2.048**		MHz MHz MHz
t_{RM}	Rise Time of Master Clock	MCLK$_X$ and MCLK$_R$			50	ns
t_{FM}	Fall Time of Master Clock	MCLK$_X$ and MCLK$_R$			50	ns
t_{PB}	Period Bit of Clock		485	**488**	15725	ns
t_{RB}	Rise Time of Bit Clock	BCLK$_X$ and BCLK$_R$			50	ns
t_{FB}	Fall Time of Bit Clock	BCLK$_X$ and BCLK$_R$			50	ns
t_{WMH}	Width of Master Clock High	MCLK$_X$ and MCLK$_R$	**160**			ns
t_{WML}	Width of Master Clock Low	MCLK$_X$ and MCLK$_R$	**160**			ns
t_{SBFM}	Set-Up Time from BCLK$_X$ High to MCLK$_X$ Falling Edge		**100**			ns
t_{SFFM}	Set-Up Time from FS$_X$ High to MCLK$_X$ Falling Edge	Long Frame Only	**100**			ns
t_{WBH}	Width of Bit Clock High		**160**			ns
t_{WBL}	Width of Bit Clock Low		**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time for Frame Sync to Bit Clock Low	Long Frame Only	**80**			ns
t_{DBD}	Delay Time from BCLK$_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	**0**		**180**	ns
t_{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from BCLK$_X$ Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS$_X$ or BCLK$_X$, Whichever Comes Later	C_L = 0 pF to 150 pF	20		165	ns
t_{SDB}	Set-Up Time from D_R Valid to BCLK$_{R/X}$ Low		**50**			ns
t_{HBD}	Hold Time from BCLK$_{R/X}$ Low to D_R Invalid		**50**			ns
t_{SF}	Set-Up Time from FS$_{X/R}$ to BCLK$_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from BCLK$_{X/R}$ Low to FS$_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS$_X$ or FS$_R$)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	**160**			ns



TL/H/5070–3

FIGURE 2. Short Frame Sync Timing

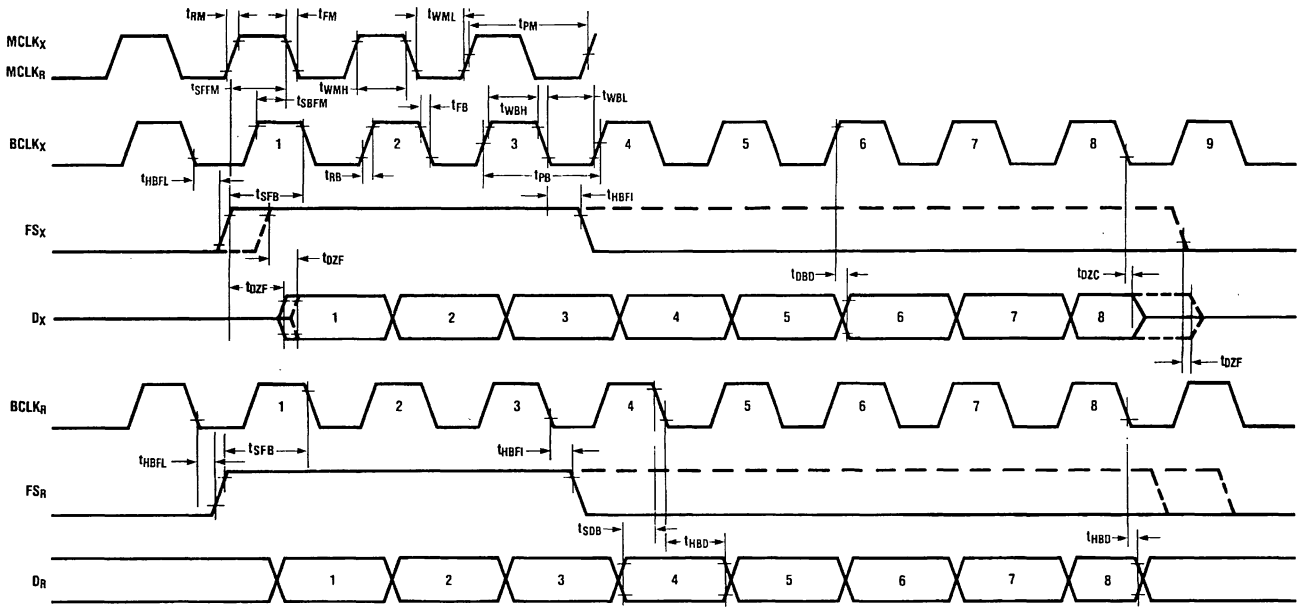


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FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of nominal gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		1.2276		Vrms
t_{MAX}		Max Transmit Overload Level TP3064 (3.17 dBm0) TP3067 (3.14 dBm0)		2.501 2.492		V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16 Hz			−40	dB
		f=50 Hz			−30	dB
		f=60 Hz			**−26**	dB
		f=200 Hz	**−1.8**		**−0.1**	dB
		f=300 Hz-3000 Hz	**−0.15**		**0.15**	dB
		f=3300 Hz	**−0.35**		**0.05**	dB
		f=3400 Hz	**−0.7**		**0**	dB
		f=4000 Hz			**−14**	dB
		f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz			**−32**	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level = −10 dBm0				
		VF_XI^+ = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		VF_XI^+ = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		VF_XI^+ = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
G_{RA}	Receive Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal	**−0.15**		**0.15**	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0 Hz to 3000 Hz	**−0.15**		**0.15**	dB
		f=3300 Hz	**−0.35**		**0.05**	dB
		f=3400 Hz	**−0.7**		**0**	dB
		f=4000 Hz			**−14**	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded − 10 dBm0 Signal				
		PCM Level = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		PCM Level = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		PCM Level = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
V_{RO}	Receive Filter Output at VF_RO	RL=10 kΩ	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz − 600 Hz		195	220	μs
		f = 600 Hz − 800 Hz		120	145	μs
		f = 800 Hz − 1000 Hz		50	75	μs
		f = 1000 Hz − 1600 Hz		20	40	μs
		f = 1600 Hz − 2600 Hz		55	75	μs
		f = 2600 Hz − 2800 Hz		80	105	μs
		f = 2800 Hz − 3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz − 1000 Hz	−40	−25		μs
		f = 1000 Hz − 1600 Hz	−30	−20		μs
		f = 1600 Hz − 2600 Hz		70	90	μs
		f = 2600 Hz − 2800 Hz		100	125	μs
		f = 2800 Hz − 3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3064 (Note 1)		12	**15**	dBrnC0
N_{XP}	Transmit Noise, Psophometric Weighted	TP3067 (Note 1)		−74	**−67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	PCM Code Equals Alternating Positive and Negative Zero				
		TP3064		8	**11**	dBrnCO
N_{RP}	Receive Noise, Psophometric Weighted	PCM Code Equals Positive Zero				
		TP3067		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 100 mVrms f = 0 kHz − 50 kHz (Note 2)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz − 50 kHz (Note 2)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz − 4000 Hz	**38**			dBC
		f = 4 kHz − 50 kHz	**25**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB} = −5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz − 4000 Hz	**40**			dBC
		f = 4 kHz − 25 kHz	**40**			dB
		f = 25 kHz − 50 kHz	**36**			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz − 3400 Hz Input PCM Code Applied at DR Measure Individual Image Signals at VF_RO				
		4600 Hz − 7600 Hz			**−32**	dB
		7600 Hz − 8400 Hz			−40	dB
		8400 Hz − 100,000 Hz			**−32**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X, STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3)				
		Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to −30 dBm0	**36**			dBC
		= −40 dBm0 XMT	**29**			dBC
		RCV	**30**			dBC
		= −55 dBm0 XMT	**14**			dBC
		RCV	**15**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz−3400 Hz			−41	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk	f = 300 Hz−3000 Hz, D_R = Quiet PCM Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk	f = 300 Hz−3000 Hz, VF_XI = 0V (Note 2)		−90	**−70**	dB
POWER AMPLIFIERS						
V_OPA	Maximum 0 dBm0 Level (Better than ±0.1 dB Linearity over the Range −10 dBm0 to +3 dBm0)	Balanced Load, R_L Connected Between VPO^+ and VPO^-.				
		R_L = 600Ω	**3.3**			Vrms
		R_L = 1200Ω	3.5			Vrms
S/D_P	Signal/Distortion	R_L = 600Ω	50			dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI^+.

Note 3: TP3064 is measured using C message weighted filter. TP3067 is measured using psophometric weighted filter.

Applications Information

POWER SUPPLIES

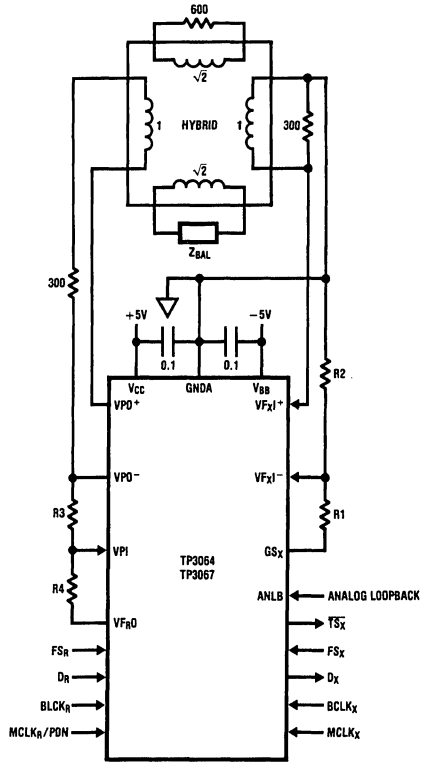
While the pins of the TP3060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in "STAR" formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

Note: See Application Note 370 for further details

Typical Asynchronous Application



TL/H/5070–5

Note 1: Transmit gain = $20 \times \log \left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10\ k\Omega$

Note 2: Receive gain = $20 \times \log \left(\frac{2 \times R3}{R4}\right)$, $R4 \geq 10\ k\Omega$

FIGURE 4

Definitions and Timing Conventions

DEFINITIONS

V_{IH}	V_{IH} is the d.c. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device
V_{IL}	V_{IL} is the d.c. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device.
V_{OH}	V_{OH} is the minimum d.c. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum d.c. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between V_{IL} and V_{IH}.
Valid Signal	A signal is Valid if it is in one of the valid logic states, (i.e. above V_{IH} or below V_{IL}). In timing specifiations, a signal is deemed valid at the instant it enters a valid state.
Invalid Signal	A signal is Invalid if it is not in a valid logic state, i.e. when it is in in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purposes of this timing specification, the following conventions apply:

Input Signals	All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ ns.
Period	The period of clock signal is designated as t_{Pxx} where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse width is designated as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as t_{Hxxww}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as t_{Dxxyy} Hi to Low, where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this data sheet.

National Semiconductor

TP3068, TP3069 Monolithic Serial Interface CMOS CODEC/Filter COMBO®

General Description

The TP3068 (μ-law) and TP3069 (A-law) are monolithic PCM CODEC/Filters utilizing the A/D and D/A conversion architecture shown in *Figure 1*, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

Similar to the TP3050 family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to ± 6.6V across a balanced 600Ω load.

Also included is an Analog Loopback switch and a $\overline{TS_X}$ output.

Features

- Complete CODEC and filtering system including:
  - — Transmit high-pass and low-pass filtering
  - — Receive low-pass filter with sin x/x correction
  - — Active RC noise filters
  - — μ-law or A-law compatible COder and DECoder
  - — Internal precision voltage reference
  - — Serial I/O interface
  - — Internal auto-zero circuitry
  - — Receive push-pull power amplifiers
- μ-law—TP3068
- A-law—TP3069
- Meets or exceeds all D3/D4 and CCITT specifications
- ± 5V operation
- Low operating power—typically 70 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

Block Diagram

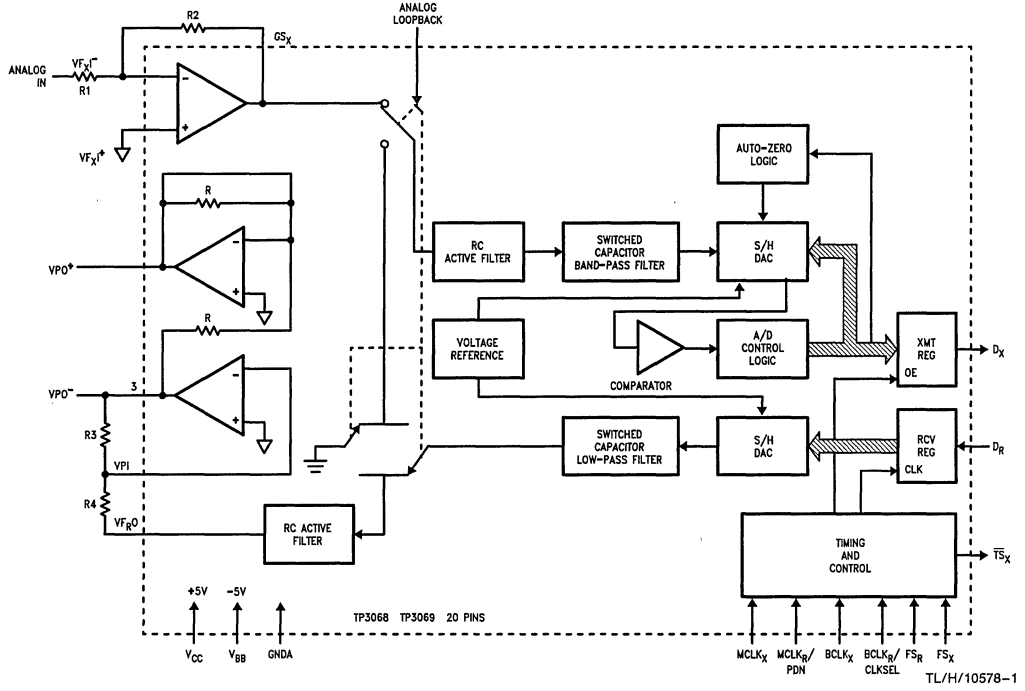
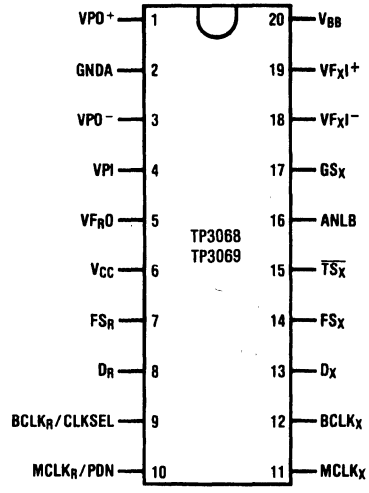


FIGURE 1

Connection Diagrams

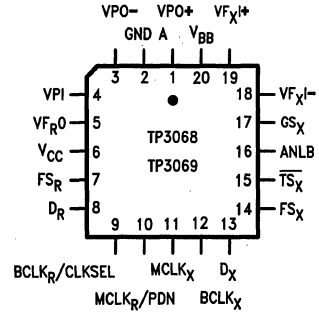
Dual-In-Line Package



TL/H/10578–2

Top View

Plastic Chip Carrier



TL/H/10578–3

Top View

Order Number TP3068V, TP3068V-1 or TP3069V or TP3069V-1
See NS Package V20A

Order Number TP3068J, TP3069J
See NS Package J20A

Pin Description

Symbol	Function
VPO^+	The non-inverted output of the receive power amplifier.
GNDA	Analog ground. All signals are referenced to this pin.
VPO^-	The inverted output of the receive power amplifier.
VPI	Inverting input to the receive power amplifier.
VF_RO	Analog output of the receive filter.
V_{CC}	Positive power supply pin. $V_{CC} = +5V \pm 5\%$.
FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 kHz pulse train. See *Figures 2* and *3* for timing details.
D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
$BCLK_R$/ CLKSEL	The bit clock which shifts data into D_R after the FS_R leading edge. May vary from 64 kHz to 2.048 MHz. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (see Table I).
$MCLK_R$/ PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_X$, but should be synchronous with $MCLK_X$ for best performance. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for all internal timing. When $MCLK_R$ is connected continuously high, the device is powered down.
$MCLK_X$	Transmit master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$. Best performance is realized from synchronous operation.
$BCLK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
D_X	The TRI-STATE® PCM data output which is enabled by FS_X.
FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 kHz pulse train, see *Figures 2* and *3* for timing details.
$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
ANLB	Analog Loopback control input. Must be set to logic '0' for normal operation. When pulled to logic '1', the transmit filter input is disconnected from the output of the transmit preamplifier and connected to the output of the receive switched capacitor low-pass filter and the input to the receive RC active filter is connected to ground. This results in the VFRO output being at ground level during analog loopback operation.
GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
$VFXI^-$	Inverting input of the transmit input amplifier.
$VFXI^+$	Non-inverting input of the transmit input amplifier.
V_{BB}	Negative power supply pin. $V_{BB} = -5V \pm 5\%$.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the COMBO™ and places it into a power-down state. All non-essential circuits are deactivated and the D_X, VF_RO, VPO^- and VPO^+ outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin *and* FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FS_X and FS_R inputs continuously low—the device will power-down approximately 2 ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The TRI-STATE PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

With a fixed level on the $BCLK_R$/CLKSEL pin, $BLCK_X$ will be selected as the bit clock for both the transmit and receive directions. Table I indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$/CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 kHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the TRI-STATE D_X output is returned to a high impedance state. With an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

TABLE I. Selection of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	TP3069	TP3068
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the TP3069, or 1.536 MHZ, 1.544 MHz for the TP3068, and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by applying only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$. FS_R starts each decoding cycle and must be synchronous with $BCLK_R$. $BCLK_R$ must be a clock, the logic levels shown in Table I are not valid in asynchronous mode. $BCLK_X$ and $BCLK_R$ may operate from 64 kHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The COMBO can utilize either a short frame sync pulse (the same as the TP3020/21 CODECs) or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in *Figure 2*. With FS_X high during a falling edge of $BCLK_X$, the next rising edge of $BCLK_X$ enables the D_X TRI-STATE output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. All devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

To use the long (TP5116A/56 CODECs) frame mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in *Figure 3*. Based on the transmit frame sync, FS_X, the COMBO will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edges of $BCLK_R$($BCLK_X$ in synchronous mode). All devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see *Figure 4*. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 kHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of companding type according to μ-law (TP3068) or A-law (TP3069) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) of nominally 2.5V peak (see

Functional Description (Continued)

table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which totals 290 μs. Any offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive section consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 kHz. The decoder is A-law (TP3069) or μ-law (TP3068) and the 5th order low pass filter corrects for the sin x/x attenuation due to the 8 kHz sample/hold. The filter is then followed by a 2nd order RC active post-filter with its output at VF_RO. The receive section is unity-gain, but gain can be added by using the power amplifiers. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is ~10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs (½ frame), which gives approximately 180 μs.

RECEIVE POWER AMPLIFIERS

Two inverting mode power amplifiers are provided for directly driving a matched line interface transformer. The gain of the first power amplifier can be adjusted to boost the ±2.5V peak output signal from the receive filter up to ±3.3V peak into an unbalanced 300Ω load, or ±4.0V into an unbalanced 15 kΩ load. The second power amplifier is internally connected in unity-gain inverting mode to give 6 dB of signal gain for balanced loads.

Maximum power transfer to a 600Ω subscriber line termination is obtained by differentially driving a balanced transformer with a $\sqrt{2}$:1 turns ratio, as shown in *Figure 4*. A total peak power of 15.6 dBm can be delivered to the load plus termination.

ENCODING FORMAT AT D_X OUTPUT

	TP3068 μ-Law								TP3069 A-Law (Includes Even Bit Inversion)							
V_{IN} = +Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} = −Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GNDA	7V
V_{BB} to GNDA	−7V
Voltage at any Analog Input or Output	V_{CC} + 0.3V to V_{BB} − 0.3V
Voltage at any Digital Input or Output	V_{CC} + 0.3V to GNDA − 0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 sec.)	300°C
ESD rating to be determined.	

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (ALL DEVICES)						
$I_{CC}0$	Power-Down Current	(Note †)		0.5	**1.5**	mA
$I_{BB}0$	Power-Down Current	(Note †)		0.05	**0.3**	mA
$I_{CC}1$	Active Current	VPI = 0V; VF_RO, VPO+ and VPO− unloaded		7.0	**10.0**	mA
$I_{BB}1$	Active Current	VPI = 0V; VF_RO, VPO+ and VPO− unloaded		7.0	**10.0**	mA
DIGITAL INTERFACE						
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	D_X, I_L = 3.2 mA $\overline{TS_X}$, I_L = 3.2 mA, Open Drain			**0.4** **0.4**	V V
V_{OH}	Output High Voltage	D_X, I_H = −3.2 mA	**2.4**			V
I_{IL}	Input Low Current	GNDA ≤ V_{IN} ≤ V_{IL}, All Digital Inputs	**−10**		**10**	μA
I_{IH}	Input High Current	V_{IH} ≤ V_{IN} ≤ V_{CC}	**−10**		**10**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X, GNDA ≤ V_O ≤ V_{CC}	**−10**		**10**	μA

Note †: I_{CC0} and I_{BB0} are measured after first acheiving a power-up state.

Electrical Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V±5%, V_{BB} = −5.0V±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

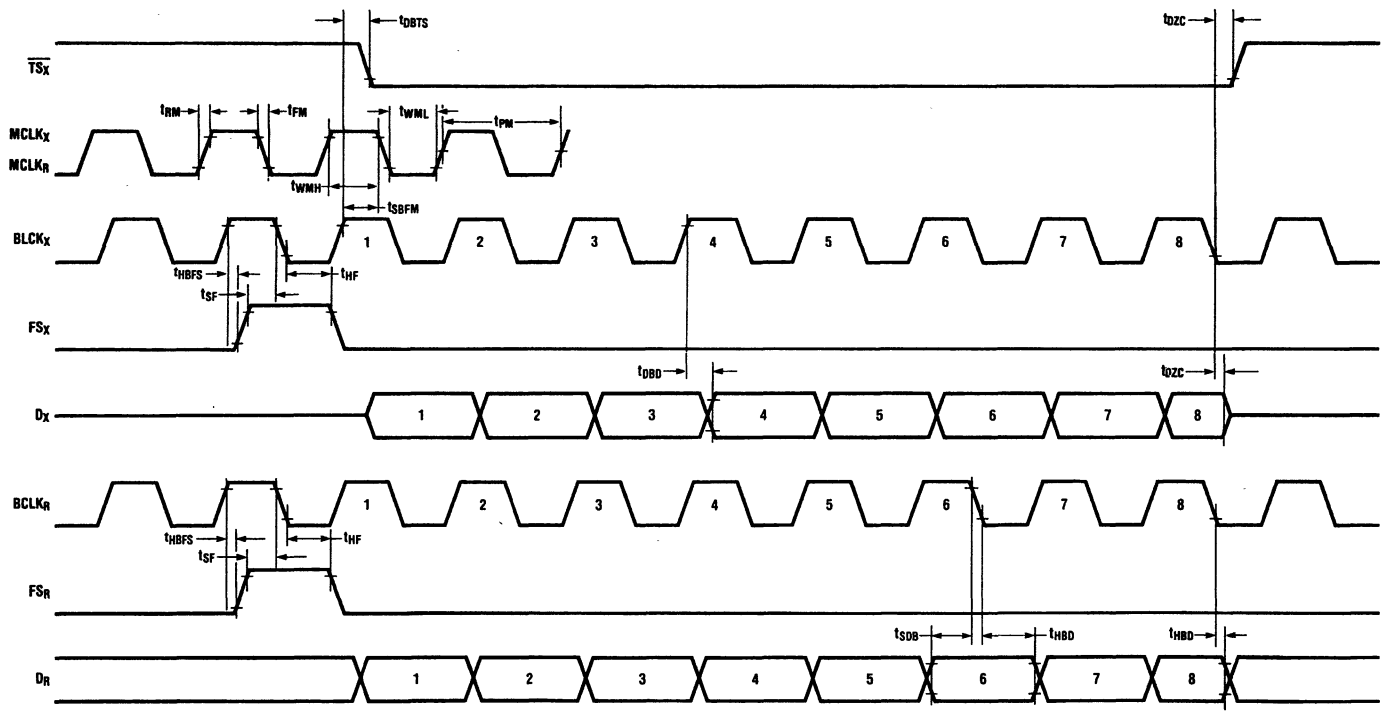
Symbol	Parameter	Conditions	Min	Typ	Max	Units
ANALOG INTERFACE WITH TRANSMIT INPUT AMPLIFIER (ALL DEVICES)						
I_IXA	Input Leakage Current	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	**−200**		**200**	nA
R_IXA	Input Resistance	$-2.5V \le V \le +2.5V$, VF_XI^+ or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			kΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L \ge 10$ kΩ	**−2.8**		**+2.8**	V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	**5000**			V/V
F_UXA	Unity-Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		**−20**		**20**	mV
$V_{CM}XA$	Common-Mode Voltage	CMRRXA > 60 dB	**−2.5**		**2.5**	V
CMRRXA	Common-Mode Rejection Ratio	DC Test	**60**			dB
PSRRXA	Power Supply Rejection Ratio	DC Test	**60**			dB
ANALOG INTERFACE WITH RECEIVE FILTER (ALL DEVICES)						
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	$VF_RO = \pm 2.5V$	10			kΩ
C_LRF	Load Capacitance	Connect from VF_RO to GNDA			25	pF
VOS_RO	Output DC Offset Voltage	Measure from VF_RO to GNDA	**−200**		**200**	mV
ANALOG INTERFACE WITH POWER AMPLIFIERS (ALL DEVICES)						
IPI	Input Leakage Current	$-1.0V \le VPI \le 1.0V$	**−100**		**100**	nA
RIPI	Input Resistance	$-1.0V \le VPI \le 1.0V$	10			MΩ
VIOS	Input Offset Voltage		**−25**		**25**	mV
ROP	Output Resistance	Inverting Unity-Gain at VPO^+ or VPO^-		1		Ω
F_C	Unity-Gain Bandwidth	Open Loop (VPO^-)		400		kHz
C_LP	Load Capacitance				100	pF
GA_P^+	Gain from VPO^- to VPO^+	$R_L = 600\Omega$ VPO^+ to VPO^- Level at $VPO^- = 1.77$ Vrms		−1		V/V
$PSRR_P$	Power Supply Rejection of V_{CC} or V_{BB}	VPO^- Connected to VPI 0 kHz−4 kHz 4 kHz−50 kHz	 60 36			 dB dB
R_LP	Load Resistance	Connect from VPO^+ to VPO^-	600			Ω

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%, T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals are referenced to GNDA. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

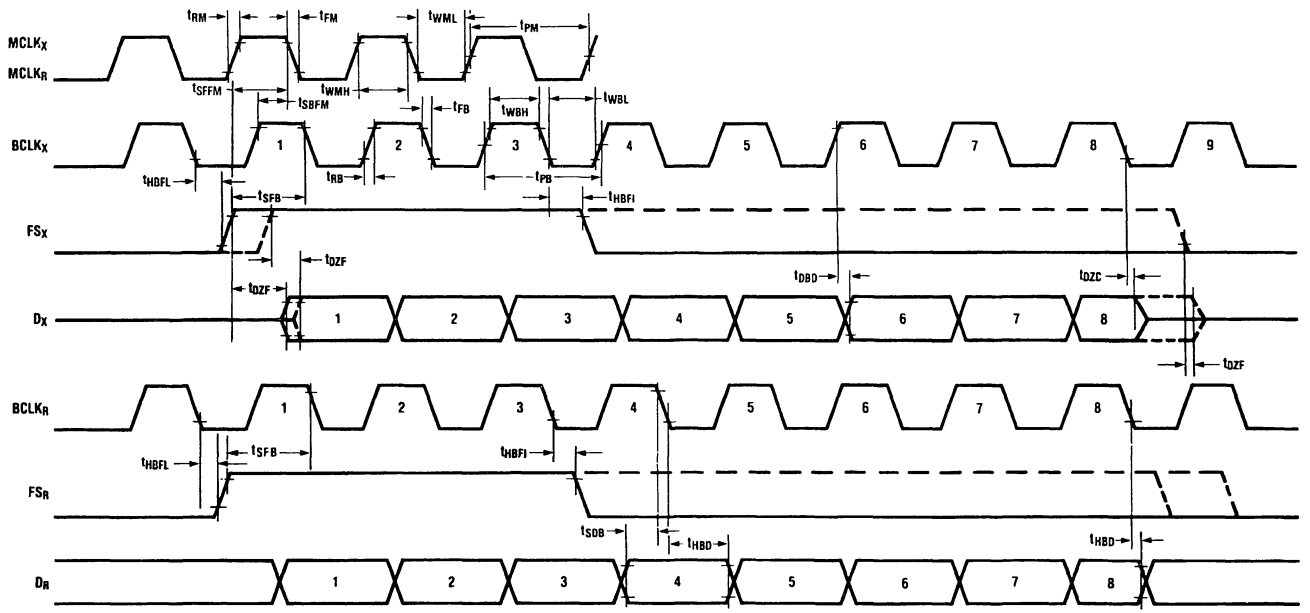
See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$1/t_{PM}$	Frequency of Master Clock	 $MCLK_X$ and $MCLK_R$		1.536 **1.544** **2.048**		MHz MHz MHz
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{PB}	Period of Bit Clock		485	**488**	15725	ns
t_{RB}	Rise Time of Bit Clock	$BCLK_X$ and $BCLK_R$			50	ns
t_{FB}	Fall Time of Bit Clock	$BCLK_X$ and $BCLK_R$			50	ns
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	**160**			ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	**100**			ns
t_{WBH}	Width of Bit Clock High		**160**			ns
t_{WBL}	Width of Bit Clock Low		**160**			ns
t_{HBFL}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	**0**			ns
t_{HBFS}	Holding Time from Bit Clock High to Frame Sync	Short Frame Only	**0**			ns
t_{SFB}	Set-Up Time for Frame Sync to Bit Clock Low	Long Frame Only	**80**			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load = 150 pF plus 2 LSTTL Loads	**0**		**180**	ns
t_{DBTS}	Delay Time to $\overline{TS_X}$ Low	Load = 150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C_L = 0 pF to 150 pF	20		165	ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		**50**			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		**50**			ns
t_{SF}	Set-Up Time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**50**			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$ Low	Short Frame Sync Pulse (1 Bit Clock Period Long)	**100**			ns
t_{HBFI}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Bit Clock Periods Long)	**100**			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	160			ns
t_{SFFM}	Set-Up Time from FS_X High to $MCLK_X$ Falling Edge	Long Frame Only	100			ns



TL/H/10578–4

FIGURE 2. Short Frame Sync Timing



TL/H/10578–5

FIGURE 3. Long Frame Sync Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels (Definition of nominal gain)	Nominal 0 dBm0 Level is 4 dBm (600Ω) 0 dBm0		 1.2276		 Vrms
t_{MAX}		Max Transmit Overload Level TP3068 (3.17 dBm0) TP3069 (3.14 dBm0)		 2.501 2.492		 V_{PK} V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V	**−0.15**		**0.15**	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16 Hz f=50 Hz f=60 Hz f=200 Hz f=300 Hz-3000 Hz f=3300 Hz f=3400 Hz f=4000 Hz f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz	 **−1.8** **−0.15** **−0.35** **−0.7**		−40 −30 **−26** **−0.1** **0.15** **0.05** **0** **−14** **−32**	dB dB dB dB dB dB dB dB dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	Relative to G_{XA}	−0.1		0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	Relative to G_{XA}	**−0.05**		**0.05**	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test Method Reference Level=−10 dBm0 VF_XI^+ = −40 dBm0 to +3 dBm0 VF_XI^+ = −50 dBm0 to −40 dBm0 VF_XI^+ = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
G_{RA}	Receive Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal	 **−0.15**		 **0.15**	 dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0 Hz to 3000 Hz f=3300 Hz f=3400 Hz f=4000 Hz	**−0.15** **−0.35** **−0.7**		**0.15** **0.05** **0** **−14**	dB dB dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	Relative to G_{RA}	−0.1		0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	Relative to G_{RA}	**−0.05**		**0.05**	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded − 10 dBm0 Signal PCM Level=−40 dBm0 to +3 dBm0 PCM Level=−50 dBm0 to −40 dBm0 PCM Level=−55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB
V_{RO}	Receive Filter Output at VF_RO	RL=10 kΩ	−2.5		2.5	V

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Transmit Delay, Absolute	f = 1600 Hz		290	315	μs
D_{XR}	Transmit Delay, Relative to D_{XA}	f = 500 Hz − 600 Hz		195	220	μs
		f = 600 Hz − 800 Hz		120	145	μs
		f = 800 Hz − 1000 Hz		50	75	μs
		f = 1000 Hz − 1600 Hz		20	40	μs
		f = 1600 Hz − 2600 Hz		55	75	μs
		f = 2600 Hz − 2800 Hz		80	105	μs
		f = 2800 Hz − 3000 Hz		130	155	μs
D_{RA}	Receive Delay, Absolute	f = 1600 Hz		180	200	μs
D_{RR}	Receive Delay, Relative to D_{RA}	f = 500 Hz − 1000 Hz	−40	−25		μs
		f = 1000 Hz − 1600 Hz	−30	−20		μs
		f = 1600 Hz − 2600 Hz		70	90	μs
		f = 2600 Hz − 2800 Hz		100	125	μs
		f = 2800 Hz − 3000 Hz		145	175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted	TP3068 (Note 1)		12	**15**	dBrnC0
N_{XP}	Transmit Noise, Psophometric Weighted	TP3069 (Note 1)		−74	**−67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted	PCM Code Equals Alternating Positive and Negative Zero				
		TP3068		8	**11**	dBrnC0
N_{RP}	Receive Noise, Psophometric Weighted	PCM Code Equals Positive Zero				
		TP3069		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI^+ = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 100 mVrms f = 0 kHz − 50 kHz (Note 2)	**40**			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB} = −5.0 V_{DC} + 100 mVrms f = 0 kHz − 50 kHz (Note 2)	**40**			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz − 4000 Hz	**38**			dBC
		f = 4 kHz − 50 kHz	**25**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB} = −5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz − 4000 Hz	**40**			dBC
		f = 4 kHz − 25 kHz	**40**			dB
		f = 25 kHz − 50 kHz	**36**			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz − 3400 Hz Input PCM Code Applied at DR Measure Individual Image Signals at VF_RO				
		4600 Hz − 7600 Hz			**−32**	dB
		7600 Hz − 8400 Hz			−40	dB
		8400 Hz − 100,000 Hz			**−32**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5.0V ±5%, V_{BB} = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. GNDA = 0V, f = 1.02 kHz, V_{IN} = 0 dbm0, transmit input amplifier connected for unity gain non-inverting. Typicals specified at V_{CC} = +5.0V, V_{BB} = −5.0V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X, STD_R	Signal to Total Distortion Transmit or Receive Half-Channel	Sinusoidal Test Method (Note 3)				
		Level = 3.0 dBm0	**33**			dBC
		= 0 dBm0 to −30 dBm0	**36**			dBC
		= −40 dBm0 XMT	**29**			dBC
		RCV	**30**			dBC
		= −55 dBm0 XMT	**14**			dBC
		RCV	**15**			dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_XI^+ = −4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz−3400 Hz			−41	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk	f = 300 Hz−3000 Hz, D_R = Quiet PCM Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk	f = 300 Hz−3000 Hz, VF_XI = 0V (Note 2)		−90	**−70**	dB
POWER AMPLIFIERS						
V_OPA	Maximum 0 dBm0 Level (Better than ±0.1 dB Linearity over the Range −10 dBm0 to +3 dBm0)	Balanced Load, R_L Connected Between VPO^+ and VPO^-.				
		R_L = 600Ω	**3.3**			Vrms
		R_L = 1200Ω	3.5			Vrms
S/D_P	Signal/Distortion	R_L = 600Ω	50			dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI^+.

Note 3: TP3068 is measured using C message weighted filter. TP3069 is measured using psophometric weighted filter.

Applications Information

POWER SUPPLIES

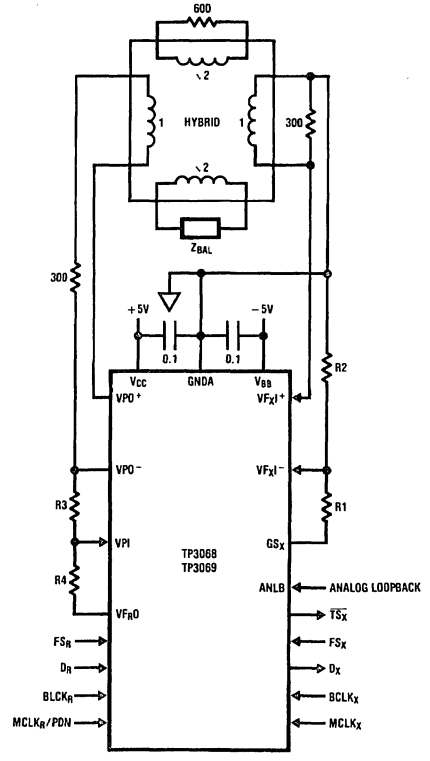
While the pins of the TP3060 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be plugged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

All ground connections to each device should meet at a common point as close as possible to the GNDA pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1 μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}, as close to the device as possible.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in "STAR" formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10 μF capacitors.

Note: See Application Note 370 for further details

Typical Asynchronous Application



TL/H/10578–6

Note 1: Transmit gain = $20 \times \log \left(\frac{R1 + R2}{R2}\right)$, $(R1 + R2) \geq 10\ k\Omega$

Note 2: Receive gain = $20 \times \log \left(\frac{2 \times R3}{R4}\right)$, $R4 \geq 10\ k\Omega$

FIGURE 4

National Semiconductor

TP3070A, TP3071A and TP3070A-X, TP3071A-X COMBO II™ Programmable PCM CODEC/Filter

General Description

The TP3070A and TP3071A are second-generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber line and trunk cards. Using advanced switched capacitor techniques, COMBO II combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

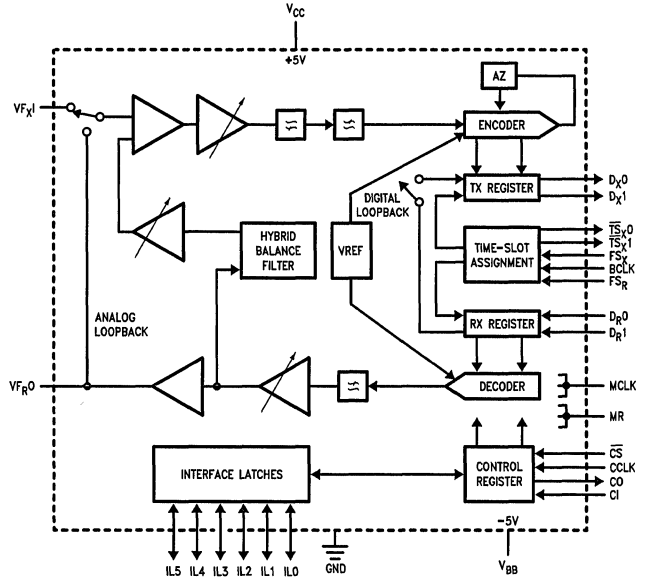
Channel gains are programmable over a 25.4 dB range in each direction, and a programmable filter is included to enable Hybrid Balancing to be adjusted to suit a wide range of loop impedance conditions. Both transformer and active SLIC interface circuits with real or complex termination impedances can be balanced by this filter, with cancellation in excess of 30 dB being readily achievable when measured across the passband against standard test termination networks.

To enable COMBO II to interface to the SLIC control leads, a number of programmable latches are included; each may be configured as either an input or an output. The TP3070A provides 6 latches and the TP3071A 5 latches.

Features

- Complete CODEC and FILTER system including:
  - — Transmit and receive PCM channel filters
  - — μ-law or A-law companding encoder and decoder
  - — Receive power amplifier drives 300Ω
  - — 4.096 MHz serial PCM data (max)
- Programmable Functions:
  - — Transmit gain: 25.4 dB range, 0.1 dB steps
  - — Receive gain: 25.4 dB range, 0.1 dB steps
  - — Hybrid balance cancellation filter
  - — Time-slot assignment; up to 64 slots/frame
  - — 2 port assignment (TP3070A)
  - — 6 interface latches (TP3070A)
  - — A or μ-law
  - — Analog loopback
  - — Digital loopback
- Direct interface to solid-state SLICs
- Simplifies transformer SLIC; single winding secondary
- Standard serial control interface
- 80 mW operating power (typ)
- 1.5 mW standby power (typ)
- Meets or exceeds all CCITT and LSSGR specifications
- TTL and CMOS compatible digital interfaces
- Extended temperature versions available for −40°C to +85°C (TP3070AJ-X, TP3070AV-X, TP3071AJ-X)

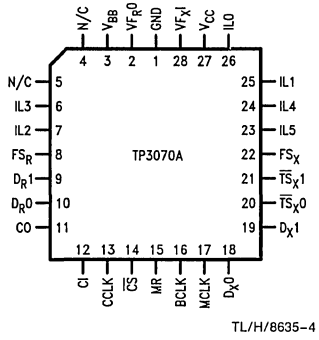
Block Diagram



TL/H/8635–1

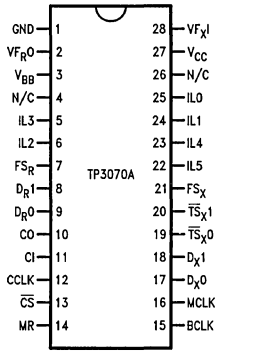
FIGURE 1

Connection Diagrams



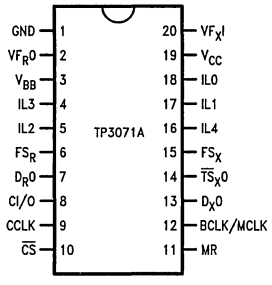
TL/H/8635-4

Order Number TP3070AV
(0°C to +70°C)
Order Number TP3070AV-X
(−40°C to +85°C)
See NS Package Number V28A



TL/H/8635-3

Order Number TP3070AJ
(0°C to +70°C)
Order Number TP3070AJ-X
(−40°C to +85°C)
See NS Package Number J28A



TL/H/8635-2

Order Number TP3071AJ
(0°C to +70°C)
Order Number TP3071AJ-X
(−40°C to +85°C)
See NS Package Number J20A

Pin Descriptions

Pin	Description
V_{CC}	+5V ±5% power supply.
V_{BB}	−5V ±5% power supply.
GND	Ground. All analog and digital signals are referenced to this pin.
FS_X	Transmit Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the transmit time slot assigned to this device (non-delayed data timing mode), or the start of the transmit frame (delayed data timing mode using the internal time-slot assignment counter).
FS_R	Receive Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the receive time slot assigned to this device (non-delayed data timing mode), or the start of the receive frame (delayed data timing mode using the internal time-slot assignment counter).
BCLK	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK.
VF_XI	The Transmit analog high-impedance input. Voice frequency signals present on this input are encoded as an A-law or μ-law PCM bit stream and shifted out on the selected D_X pin.
VF_RO	The Receive analog power amplifier output, capable of driving load impedances as low as 300Ω (depending on the peak overload level required). PCM data received on the assigned D_R pin is decoded and appears at this output as voice frequency signals.
D_X0	D_X1 is available on the TP3070A only; D_X0 is available on all devices. These Transmit Data TRI-STATE® outputs remain in the high impedance state except during the assigned transmit time slot on the assigned port, during which the transmit PCM data byte is shifted out on the rising edges of BCLK.
$\overline{TS}_X0$ $\overline{TS}_X1$	$\overline{TS}_X1$ is available on the TP3070A only; $\overline{TS}_X0$ is available on all devices. Normally these open-drain outputs are floating in a high impedance state except when a time-slot is active on one of the D_X outputs, when the appropriate $\overline{TS}_X$ output pulls low to enable a backplane line-driver.
D_R0 D_R1	D_R1 is available on the TP3070A only; D_R0 is available on all devices. These receive data inputs are inactive except during the assigned receive time slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.
CCLK	Control Clock input. This clock shifts serial control information into or out from CI/O or CI and CO when the $\overline{CS}$ input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI/O	This is the Control Data I/O pin which is provided on the TP3071A. Serial control information is shifted to or read from COMBO II on this pin when $\overline{CS}$ is low. The direction of the data is determined by the current instruction as defined in Table I.
CI	This is a separate Control Input, available only on the TP3070A. It can be connected to CO if required.
CO	This is a separate Control Output, available only on the TP3070A. It can be connected to CI if required.
$\overline{CS}$	Chip Select input. When this pin is low, control information can be written to or read from COMBO II via the CI/O pin (or CI and CO).
IL5–IL0	IL5 through IL0 are available on the TP3070A. IL4 through IL0 are available on the TP3071A.

Pin Descriptions (Continued)

Pin	Description
	Each Interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to COMBO II, while $\overline{CS}$ is low, and the information is shifted out on the CO (or CI/O) pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.
MR	This logic input must be pulled low for normal operation of COMBO II. When pulled momentarily high (at least 1 μsec.), all programmable registers in the device are reset to the states specified under "Power-On Initialization".
NC	No Connection. Do not connect to this pin. Do not route traces through this pin.

Functional Description

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes the COMBO II and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed to OFF (00000000), the hybrid balance circuit is turned off, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CI/O pin is set as an input ready for the first control byte of the initialization sequence. Other initial states in the Control Register are indicated in Section 2.0.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high. This may be done either when powered-up or down. For normal operation this pin must be pulled low. If not used, MR should be hardwired to ground.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing any of the control instructions into the serial control port with the "P" bit set to "1" as indicated in Table I. It is recommended that the chip be powered down before writing any additional instructions. In the power-down state, all non-essential circuitry is de-activated and the D_X0 (and D_X1) outputs are in the high impedance TRI-STATE condition.

The coefficients stored in the Hybrid Balance circuit and the Gain Control registers, the data in the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains active. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control the SLIC.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI, is a high impedance summing input which is used as the differencing point for the internal hybrid balance cancellation signal. No external components are necessary to set the gain. Following this circuit is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active pre-filter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or μ255 coding laws, which must be selected by a control instruction during initialization (see Tables I and II). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is canceled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Transmit Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_X0 or D_X1 during the selected time slot on eight rising edges of BCLK.

DECODER AND RECEIVE FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R0 or D_R1 pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or μ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Power Amplifier capable of driving a 300Ω load to ±3.5V, a 600Ω load to ±3.8V or a 15 kΩ load to ±4.0V at peak overload.

A decode cycle begins immediately after the assigned receive time-slot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (½ frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK HIGH to one MCLK period LOW. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see Table II). Non-delayed data mode is similar to long-frame timing on the TP3050/60 series of devices (COMBO™); time-slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode, which is similar to short-frame sync timing on COMBO, in which each FS input must be high at least a half-cycle of BCLK earlier than the time-slot. The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing.

When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters.

Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles. During each assigned Transmit time-slot, the selected $D_X0/1$ output shifts data out from the PCM register on the rising edges of BCLK. $\overline{TS}_X0$ (or $\overline{TS}_X1$ as appropriate) also pulls low for the first 7½ bit times of the time-slot to control the TRI-STATE Enable of a backplane line-driver. Serial PCM data is shifted into the selected $D_R0/1$ input during each assigned Receive time-slot on the falling edges of BCLK. D_X0 or D_X1 and D_R0 or D_R1 are selectable on the TP3070A only, see Section 6.

Functional Description (Continued)

TABLE I. Programmable Register Instructions

Function	Byte 1 (Note 1) 7	6	5	4	3	2	1	0	Byte 2 (Note 1) 7	6	5	4	3	2	1	0
Single Byte Power-Up/Down	P	X	X	X	X	X	0	X	None							
Write Control Register	P	0	0	0	0	0	1	X	See Table II							
Read-Back Control Register	P	0	0	0	0	1	1	X	See Table II							
Write to Interface Latch Register	P	0	0	0	1	0	1	X	See Table V							
Read Interface Latch Register	P	0	0	0	1	1	1	X	See Table V							
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table IV							
Read Latch Direction Register	P	0	0	1	0	1	1	X	See Table IV							
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table VIII							
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table VIII							
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table VII							
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table VII							
Write Receive Time-Slot/Port	P	1	0	0	1	0	1	X	See Table VI							
Read-Back Receive Time-Slot/Port	P	1	0	0	1	1	1	X	See Table VI							
Write Transmit Time-Slot/Port	P	1	0	1	0	0	1	X	See Table VI							
Read-Back Transmit Time-Slot/Port	P	1	0	1	0	1	1	X	See Table VI							

Note 1: Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI, CO or CI/O pin. X = don't care.

Note 2: "P" is the power-up/down control bit, see "Power-Up/Down Control" section. ("0" = Power Up, "1" = Power Down)

Note 3: Three additional registers are provided for the Hybrid Balance Filter, see Section 9.0. Other register address codes are invalid and should not be used.

SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO II via the serial control port consisting of the control clock CCLK, the serial data input/output CI/O, (or separate input, CI, and output, CO, on the TP3070A only), and the Chip Select input, $\overline{CS}$. All control instructions require 2 bytes, as listed in Table I, with the exception of a single byte power-up/down command. The byte 1 bits are used as follows: bit 7 specifies power up or power down; bits 6, 5, 4 and 3 specify the register address; bit 2 specifies whether the instruction is read or write; bit 1 specifies a one or two byte instruction; and bit 0 is not used.

To shift control data into COMBO II, CCLK must be pulsed 8 times while $\overline{CS}$ is low. Data on the CI/O (or CI) input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first contiguously, i.e. it is not mandatory for $\overline{CS}$ to return high between the first and second control bytes. At the end of CCLK8 in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However, $\overline{CS}$ should be set high when no data transfers are in progress.

To readback Interface Latch data or status information from COMBO II, the first byte of the appropriate instruction is strobed in during the first $\overline{CS}$ pulse, as defined in Table I. $\overline{CS}$ must then be taken low for a further 8 CCLK cycles, during which the data is shifted onto the CO or CI/O pin on the rising edges of CCLK. When $\overline{CS}$ is high the CO or CI/O pin is in the high-impedance TRI-STATE, enabling the CI/O pins of many devices to be multiplexed together.

Programmable Functions

1.0 POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in Table I into COMBO II with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down by setting the "P" bit as indicated. When the power-up or down control is entered as a single byte instruction, bit one (1) must be reset to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), D_X0 (and D_X1), will remain in the high impedance state until the second FS_X pulse after power-up.

2.0 CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in Table I. The second byte has the following bit functions:

TABLE II. Control Register Byte 2 Functions

Bit Number and Name 7	6	5	4	3	2	1	0	Function
F_1	F_0	MA	IA	DN	DL	AL	PP	
0	0							MCLK = 512 kHz
0	1							MCLK = 1.536 or 1.544 MHz
1	0							MCLK = 2.048 MHz*
1	1							MCLK = 4.096 MHz
		0	X					Select μ-255 law*
		1	0					A-law, Including Even Bit Inversion
		1	1					A-law, No Even Bit Inversion
				0				Delayed Data Timing
				1				Non-Delayed Data Timing*
					0	0		Normal Operation*
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN*

* = State at power-on initialization. (Bit 4 = 0)

Programmable Functions (Continued)

TABLE III. Coding Law Conventions

	μ255 law MSB LSB	True A-law with even bit inversion MSB LSB	A-law without even bit inversion MSB LSB
V_{IN} = +Full Scale	10000000	10101010	11111111
V_{IN} = 0V	11111111 01111111	11010101 01010101	10000000 00000000
V_{IN} = −Full Scale	00000000	00101010	01111111

Note 1: The MSB is always the first PCM bit shifted in or out of COMBO II.

2.1 Master Clock Frequency Selection

A Master clock must be provided to COMBO II for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F_1 and F_0 (see Table II) must be set during initialization to select the correct internal divider.

2.2 Coding Law Selection

Bits "MA" and "IA" in Table II permit the selection of μ255 coding or A-law coding, with or without even bit inversion.

2.3 Analog Loopback

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop. Hybrid balance must be disabled for meaningful analog loopback function.

2.4 Digital Loopback

Digital Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at $D_X0/1$. In digital loopback, the decoder will remain functional and output a signal at VF_RO. If this is undesirable, the receive output can be turned off by programming the receive gain register to all zeros.

3.0 INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see Tables I and IV. For minimum power dissipation, unconnected latch pins should be programmed as outputs. For the TP3071A, L5 should always be programmed as an output.

Bits L_5–L_0 must be set by writing the specified instruction to the LDR with the L bits in the second byte set as follows:

TABLE IV. Byte 2 Functions of Latch Direction Register

Byte 2 Bit Number							
7	6	5	4	3	2	1	0
L_0	L_1	L_2	L_3	L_4	L_5	X	X

L_n Bit	IL Direction
0	Input
1	Output

X = don't care

4.0 INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Interface Latch Register (ILR) as shown in Tables I and V. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR.

It is recommended that during initialization, the state of IL pins to be configured as outputs should be programmed first, followed immediately by the Latch Direction Register.

TABLE V. Interface Latch Data Bit Order

Bit Number							
7	6	5	4	3	2	1	0
D_0	D_1	D_2	D_3	D_4	D_5	X	X

5.0 TIME-SLOT ASSIGNMENT

COMBO II can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_R. Time-Slot Assignment may only be used with Delayed Data timing; see *Figure 6*. FS_X and FS_R may have any phase relationship with each other in BCLK period increments.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A

Programmable Functions (Continued)

TABLE VI. Time-Slot and Port Assignment Instruction

Bit Number and Name								Function
7 EN	6 PS (Note 1)	5 T_5 (Note 2)	4 T_4	3 T_3	2 T_2	1 T_1	0 T_0	
0	0	X	X	X	X	X	X	Disable D_X0 Output (Transmit Instruction) Disable D_R0 Input (Receive Instruction)
0	1	X	X	X	X	X	X	Disable D_X1 Output (Transmit Instruction) Disable D_R1 Input (Receive Instruction)
1	0	Assign One Binary Coded Time-Slot from 0–63 Assign One Binary Coded Time-Slot from 0–63						Enable D_X0 Output (Transmit Instruction) Enable D_R0 Input (Receive Instruction)
1	1	Assign One Binary Coded Time-Slot from 0–63 Assign One Binary Coded Time-Slot from 0–63						Enable D_X1 Output (Transmit Instruction) Enable D_R1 Input (Receive Instruction)

Note 1: The "PS" bit MUST always be set to 0 for the TP3071A.

Note 2: T5 is the MSB of the Time-slot assignment bit field. Time slot bits should be set to "000000" for both transmit and receive when operating in non-delayed data timing mode.

time-slot is assigned by a 2-byte instruction as shown in Tables I and VI. The last 6 bits of the second byte indicate the selected time-slot from 0–63 using straight binary notation. A new assignment becomes active on the second frame following the end of the Chip-Select for the second control byte. The "EN" bit allows the PCM inputs, $D_R0/1$, or outputs, $D_X0/1$, as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the FS_X and FS_R pulses must conform to the delayed data timing format shown in *Figure 6.*

6.0 PORT SELECTION

On the TP3070A only, an additional capability is available; 2 Transmit serial PCM ports, D_X0 and D_X1, and 2 Receive serial PCM ports, D_R0 and D_R1, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instruction using the "PS" bit in the second byte.

On the TP3071A, only ports D_X0 and D_R0 are available, therefore the "PS" bit MUST always be set to 0 for these devices.

Table VI shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

7.0 TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in Tables I and VII. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.619 Vrms and 0.087 Vrms (equivalent to +6.4 dBm to −19.0 dBm in 600Ω).

To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.08595)$$

and convert to the binary equivalent. Some examples are given in Table VII.

It should be noted that the Transmit (idle channel) Noise and Transmit Signal to Total Distortion are both specified with transmit gain set to 0 dB. At high transmit gains there will be some degradation in noise performance for these parameters. See Application Note AN-614 for more information on this subject.

TABLE VII. Byte 2 of Transmit Gain Instruction

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_XI
0 0 0 0 0 0 0 0	No Output
0 0 0 0 0 0 0 1	0.087
0 0 0 0 0 0 1 0	0.088
—	—
1 1 1 1 1 1 1 0	1.600
1 1 1 1 1 1 1 1	1.619

8.0 RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in Tables I and VIII. Note the following restrictions on output drive capability:

a) 0 dBm0 levels ≤ 1.96 Vrms at VF_RO may be driven into a load of ≥ 15 kΩ to GND; receive gain set to 0 dB

b) 0 dBm0 levels ≤ 1.85 Vrms at VF_RO may be driven into a load of ≥ 600Ω to GND; receive gain set to −0.5 dB

c) 0 dBm0 levels ≤ 1.71 Vrms at VF_RO may be driven into a load of ≥ 300Ω to GND; receive gain set to −1.2 dB

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.1043)$$

and convert to the binary equivalent. Some examples are given in Table VIII.

TABLE VIII. Byte 2 of Receive Gain Instruction

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_RO
0 0 0 0 0 0 0 0	No Output (Low Z to GND)
0 0 0 0 0 0 0 1	0.105
0 0 0 0 0 0 1 0	0.107
—	—
1 1 1 1 1 1 1 0	1.941
1 1 1 1 1 1 1 1	1.964

Programmable Functions (Continued)

9.0 HYBRID BALANCE FILTER

The Hybrid Balance Filter on COMBO II is a programmable filter consisting of a second-order section, Hybal1, followed by a first-order section, Hybal2, and a programmable attenuator. Either of the filter sections can be bypassed if only one is required to achieve good cancellation. A selectable 180 degree inverting stage is included to compensate for interface circuits which also invert the transmit input relative to the receive output signal. The 2nd order section is intended mainly to balance low frequency signals across a transformer SLIC, and the first order section to balance midrange to higher audio frequency signals.

As a 2nd order section, Hybal1 has a pair of low frequency zeroes and a pair of complex conjugate poles. When configuring Hybal1, matching the phase of the hybrid at low to mid-band frequencies is most critical. Once the echo path is correctly balanced in phase, the magnitude of the cancellation signal can be corrected by the programmable attenuator.

The 2nd order mode of Hybal1 is most suitable for balancing interfaces with transformers having high inductance of 1.5 Henries or more. An alternative configuration for smaller transformers is available by converting Hybal1 to a simple first-order section with a single real low-frequency pole and zero. In this mode, the pole/zero frequency may be programmed.

Many line interfaces can be adequately balanced by use of the Hybal1 section only, in which case the Hybal2 filter should be de-selected to bypass it.

Hybal2, the higher frequency first-order section, is provided for balancing an electronic SLIC, and is also helpful with a transformer SLIC in providing additional phase correction for mid and high-band frequencies, typically 1 kHz to 3.4 kHz. Such a correction is particularly useful if the test balance impedance includes a capacitor of 100 nF or less, such as the loaded and non-loaded loop test networks in the United States. Independent placement of the pole and zero location is provided.

Figure 2 shows a simplified diagram of the local echo path for a typical application with a transformer interface. The magnitude and phase of the local echo signal, measured at VF_XI, are a function of the termination impedance Z_T, the line transformer and the impedance of the 2W loop, Z_L. If the impedance reflected back into the transformer primary is expressed as Z_L' then the echo path transfer function from VF_RO to VF_XI is:

$$H(w) = Z_L'/(Z_T + Z_L') \quad (1)$$

9.1 PROGRAMMING THE FILTER

On initial power-up, the Hybrid Balance filter is disabled. Before the hybrid balance filter can be programmed it is necessary to design the transformer and termination impedance in order to meet system 2W input return loss specifications, which are normally measured against a fixed test impedance (600 or 900Ω in most countries). Only then can the echo path be modeled and the hybrid balance filter programmed. Hybrid balancing is also measured against a fixed test impedance, specified by each national Telecom administration to provide adequate control of talker and listener echo over the majority of their network connections. This test impedance is Z_L in *Figure 2*. The echo signal and the degree of transhybrid loss obtained by the programmable filter must be measured from the PCM digital input, D_RO, to the PCM digital output, D_XO, either by digital test signal analysis or by conversion back to analog by a PCM CODEC/Filter.

Three registers must be programmed in COMBO II to fully configure the Hybrid Balance Filter as follows:

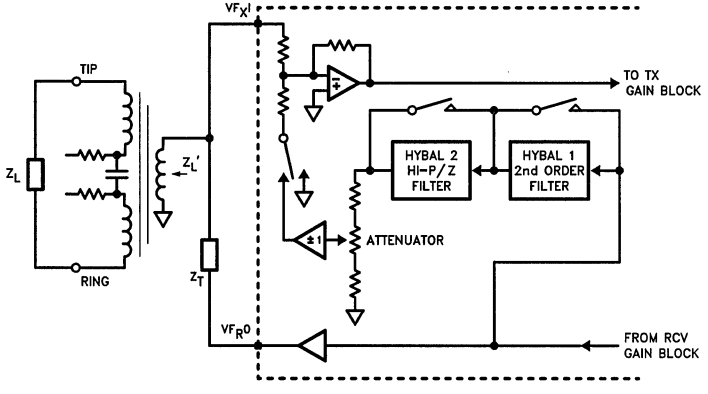
Register 1: select/de-select Hybrid Balance Filter;
invert/non-invert cancellation signal;
select/de-select Hybal2 filter section;
attenuator setting.

Register 2: select/de-select Hybal1 filter;
set Hybal1 to 2nd order or 1st order;
pole and zero frequency selection.

Register 3: program pole frequency in Hybal2 filter;
program zero frequency in Hybal2 filter.

Standard filter design techniques may be used to model the echo path (see Equation 1) and design a matching hybrid balance filter configuration. Alternatively, the frequency response of the echo path can be measured and the hybrid balance filter designed to replicate it.

A Hybrid Balance filter design guide and software optimization program are available under license from National Semiconductor Corporation; order TP3077SW.



TL/H/8635–5

FIGURE 2. Simplified Diagram of Hybrid Balance Circuit

Applications Information

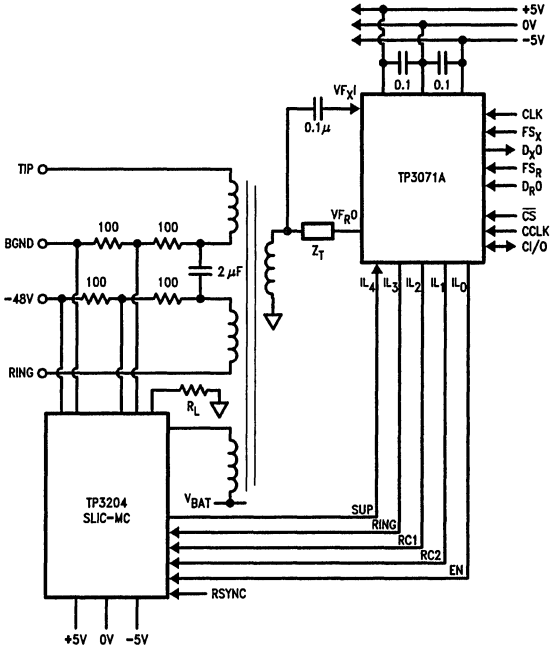
Figure 3 shows a typical application of the TP3071A together with a transformer-based SLIC using the TP3204 Magnetic Compensation device. Four of the IL latches are configured as outputs to control the relay drivers on the SLIC, while IL4 is an input for the Supervision signal. *Figure 4* shows a similar arrangement with a monolithic SLIC.

POWER SUPPLIES

While the pins of the TP3070A COMBO II devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, extra long pins on the connector should be used for ground and V_{BB}. In addition, a Schottky diode should be connected between V_{BB} and ground.

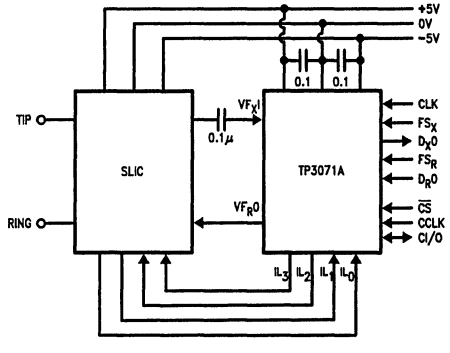
To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the device GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 μF should be connected from this common device ground point to V_{CC} and V_{BB} as close to the device pins as possible. V_{CC} and V_{BB} should also be decoupled with Low Effective Series Resistance Capacitors of at least 10 μF located near the card edge connector.

Further guidelines on PCB layout techniques are provided in Application Note AN-614, "COMBO II™ Programmable PCM CODEC/Filter Family Application Guide".



TL/H/8635-6

FIGURE 3. Typical Application with Transformer SLIC



TL/H/8635-7

FIGURE 4. Typical Application with Monolithic SLIC

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at VF_XI	V_{CC} + 0.5V to V_{BB} − 0.5V
Voltage at any Digital Input	V_{CC} + 0.5V to GND − 0.5V
Storage Temperature Range	−65°C to + 150°C
V_{BB} to GND	−7V
Current at VF_RO	±100 mA
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C (−40°C to +85°C for TP3070A/71A-X) by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs (DC Meas.)*			**0.7**	V
V_{IH}	Input High Voltage	All Digital Inputs (DC Meas.)*	**2.0**			V
V_{OL}	Output Low Voltage	D_X0, D_X1, $\overline{TS}_X0$, $\overline{TS}_X1$ and CO, I_L = 3.2 mA, All Other Digital Outputs, I_L = 1 mA			**0.4**	V
V_{OH}	Output High Voltage	D_X0, D_X1 and CO, I_L = −3.2 mA, All Other Digital Outputs (except $\overline{TS}_X$), I_L = −1 mA All Digital Outputs, I_L = −100 μA	**2.4** V_{CC} − 0.5			V V
I_{IL}	Input Low Current	Any Digital Input, GND < V_{IN} < V_{IL}	**−10**		**10**	μA
I_{IH}	Input High Current	Any Digital Input except MR, V_{IH} < V_{IN} < V_{CC}	**−10**		**10**	μA
		MR Only	**−10**		**100**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	D_X0, D_X1, CO and CI/O (as an Output) IL5–IL0 When Selected as Inputs GND < V_{OUT} < V_{CC} −40°C to +85°C (TP3070A/71A-X)	**−10** −30		**10** 30	μA μA
ANALOG INTERFACES						
I_{VFXI}	Input Current, VF_XI	−3.3V < VF_XI < 3.3V	**−10.0**		**10.0**	μA
R_{VFXI}	Input Resistance	−3.3V < VF_XI < 3.3V	**390**	620		kΩ
VOS_X	Input Offset Voltage Applied at VF_XI	Transmit Gain = 0 dB Transmit Gain = 25.4 dB			200 10	mV mV
RL_{VFRO}	Load Resistance	Receive Gain = 0 dB Receive Gain = −0.5 dB Receive Gain = −1.2 dB	15k 600 **300**			Ω
CL_{VFRO}	Load Capacitance	RL_{VFRO} ≥ 300Ω CL_{VFRO} from VF_RO to GND			**200**	pF
RO_{VFRO}	Output Resistance	Steady Zero PCM Code Applied to D_R0 or D_R1		1.0	3.0	Ω
VOS_R	Output Offset Voltage at V_{FRO}	Alternating ± Zero PCM Code Applied to D_R0 or D_R1, Maximum Receive Gain	**−200**		**200**	mV
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	CCLK, CI/O, CI, CO, = 0.4V, $\overline{CS}$ = 2.4V Interface Latches Set as Outputs with No Load, All Other Inputs Active, Power Amp Disabled		0.1	**0.6**	mA
$I_{BB}0$	Power Down Current	As Above −40°C to +85°C (TP3070A/71A-X)		−0.1	**−0.3** −0.4	mA mA
$I_{CC}1$	Power Up Current	CCLK, CI/O, CI, CO = 0.4V, $\overline{CS}$ = 2.4V No Load on Power Amp Interface Latches Set as Outputs with No Load −40°C to +85°C (TP3070A/71A-X)		8.0	**11.0** 13.0	mA mA
$I_{BB}1$	Power Up Current	As Above −40°C to +85°C (TP3070A/71A-X)		−8.0	**−11.0** −13.0	mA mA
$I_{CC}2$	Power Down Current	Power Amp Enabled −40°C to +85°C (TP3070A/71A-X)		2.0	**3.0** 4.0	mA mA
$I_{BB}2$	Power Down Current	Power Amp Enabled −40°C to +85°C (TP3070A/71A-X)		−2.0	**−3.0** −4.0	mA mA

Note *: See definitions and timing conventions section.

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ ($-40°C$ to $+85°C$ for TP3070A/71A-X) by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER CLOCK TIMING						
f_{MCLK}	Frequency of MCLK	Selection of Frequency is Programmable (See Table III)		512 1536 1544 2048 **4096**		kHz kHz kHz kHz kHz
t_{WMH}	Period of MCLK High	Measured from V_{IH} to V_{IH} (See Note)	**80**			ns
t_{WML}	Period of MCLK Low	Measured from V_{IL} to V_{IL} (See Note)	**80**			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBM}	HOLD Time, BCLK LOW to MCLK HIGH	TP3070A Only	**50**			ns
t_{WFL}	Period of F_{SX} or F_{SR} Low	Measured from V_{IL} to V_{IL}	1			MCLK Period
PCM INTERFACE TIMING						
f_{BCLK}	Frequency of BCLK	May Vary from 64 kHz to 4096 kHz in 8 kHz Increments	**64**		**4096**	kHz
t_{WBH}	Period of BCLK High	Measured from V_{IH} to V_{IH}	**80**			ns
t_{WBL}	Period of BCLK Low	Measured from V_{IL} to V_{IL}	**80**			ns
t_{RB}	Rise Time of BCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FB}	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low		**30**			ns
t_{SFB}	Setup Time, $FS_{X/R}$ High to BCLK Low		**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads $-40°C$ to $+85°C$ (TP3070A/71A-X)			**80** 90	ns ns
t_{DBZ}	Delay Time, BCLK Low to $D_X0/1$ Disabled if FS_X Low, FS_X Low to $D_X0/1$ disabled if 8th BCLK Low, or BCLK High to $D_X0/1$ Disabled if FS_X High	 $-40°C$ to $+85°C$ (TP3070A/71A-X)	**15** 15		**80** 100	ns ns
t_{DBT}	Delay Time, BCLK High to $\overline{TS}_X$ Low if FS_X High, or FS_X High to $\overline{TS}_X$ Low if BCLK High	Load = 100 pF Plus 2 LSTTL Loads			60	ns
t_{ZBT}	TRI-STATE Time, BCLK Low to $\overline{TS}_X$ High if FS_X Low, FS_X Low to $\overline{TS}_X$ High if 8th BCLK Low, or BCLK High to $\overline{TS}_X$ High if FS_X High		15		60	ns
t_{DFD}	Delay Time, $FS_{X/R}$ High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads, Applies if $FS_{X/R}$ Rises Later than BCLK Rising Edge in Non-Delayed Data Mode Only $-40°C$ to $+85°C$ (TP3070A/71A-X)			**80** 90	ns ns
t_{SDB}	Setup Time, $D_R0/1$ Valid to BCLK Low		**30**			ns
t_{HBD}	Hold Time, BCLK Low to $D_R0/1$ Invalid	 $-40°C$ to $+85°C$ (TP3070A/71A-X)	**20** 25			ns ns

Note: Applies only to MCLK Frequencies ≥ 1.536 MHz. At 512 kHz a 50:50 ±2% Duty Cycle must be used.

Timing Specifications (Continued)

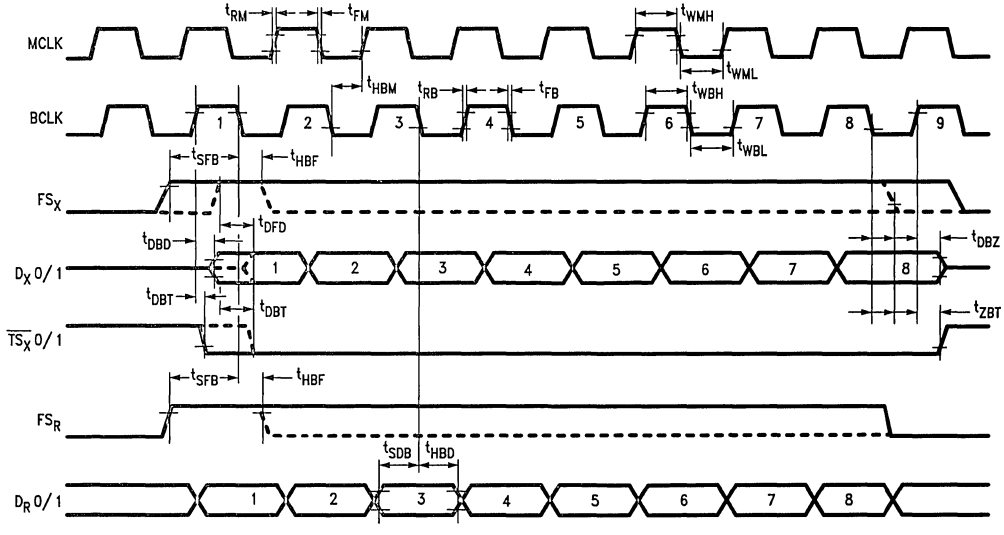
Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C (−40°C to +85°C for TP3070A/71A-X) by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL CONTROL PORT TIMING						
f_{CCLK}	Frequency of CCLK				**2048**	kHz
t_{WCH}	Period of CCLK High	Measured from V_{IH} to V_{IH}	**160**			ns
t_{WCL}	Period of CCLK Low	Measured from V_{IL} to V_{IL}	**160**			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured from V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low	CCLK1	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High	CCLK 8	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low		**60**			ns
t_{SSCO}	Setup Time, $\overline{CS}$ Transition to CCLK High		50			ns
t_{SDC}	Setup Time, CI (CI/O) Data In to CCLK Low		**50**			ns
t_{HCD}	Hold Time, CCLK Low to CI/O Invalid		50			ns
t_{DCD}	Delay Time, CCLK High to CI/O Data Out Valid	Load = 100 pF plus 2 LSTTL Loads −40°C to +85°C (TP3070A/71A-X)			**80** 100	ns ns
t_{DSD}	Delay Time, $\overline{CS}$ Low to CO (CI/O) Valid	Applies Only if Separate $\overline{CS}$ used for Byte 2 −40°C to +85°C (TP3070A/71A-X)			**80** 100	ns ns
t_{DDZ}	Delay Time, $\overline{CS}$ or 9th CCLK High to CO (CI/O) High Impedance	Applies to Earlier of $\overline{CS}$ High or 9th CCLK High	15		80	ns
INTERFACE LATCH TIMING						
t_{SLC}	Setup Time, IL to CCLK 8 of Byte 1	Interface Latch Inputs Only	**100**			ns
t_{HCL}	Hold Time, IL Valid from 8th CCLK Low (Byte 1)		50			ns
t_{DCL}	Delay Time CCLK 8 of Byte 2 to IL	Interface Latch Outputs Only C_L = 50 pF			200	ns
MASTER RESET PIN						
t_{WMR}	Duration of Master Reset High		1			µs

Timing Diagrams



TL/H/8635-8

FIGURE 5. Non Delayed Data Timing Mode

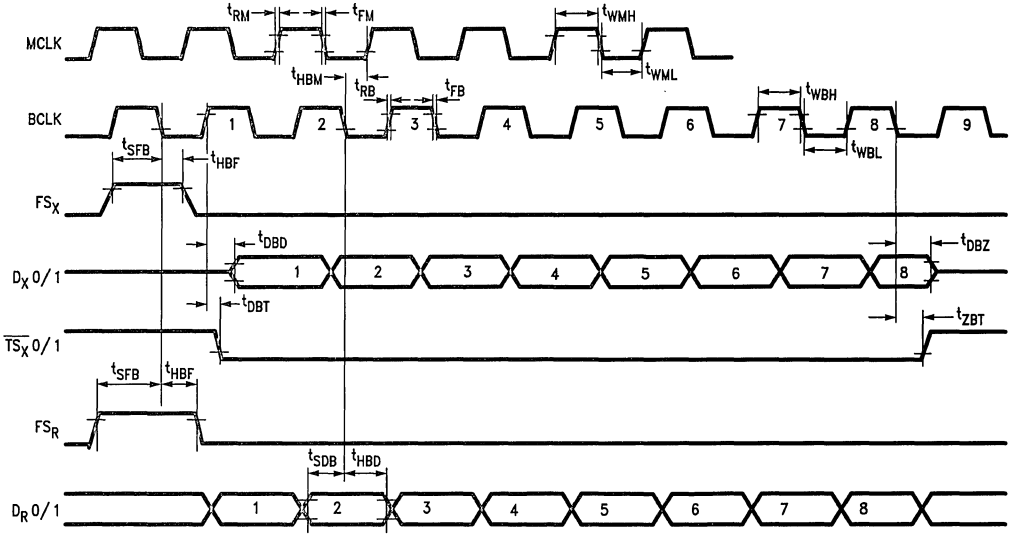


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FIGURE 6. Delayed Data Timing Mode (Time Slot Zero Only)

1

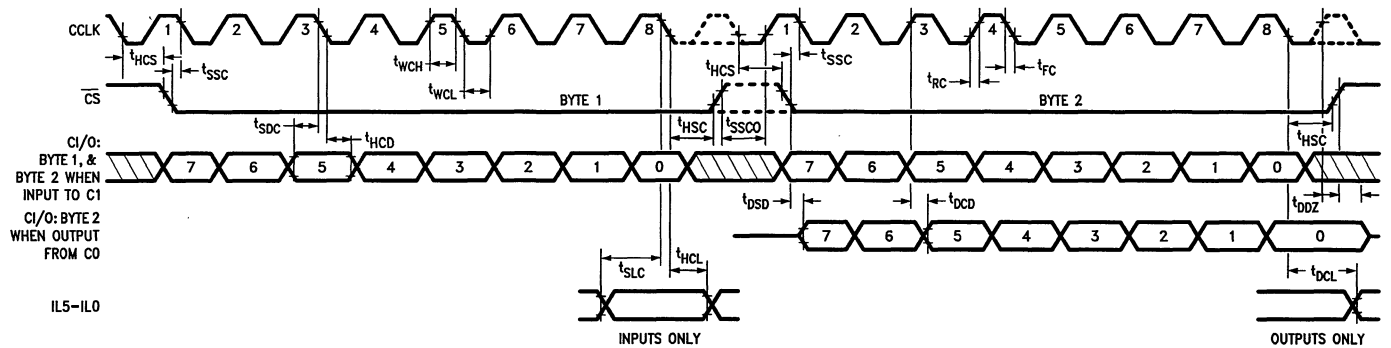

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FIGURE 7. Control Port Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C (−40°C to +85°C for TP3070A/71A-X) by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	The Maximum 0 dBm0 Levels are:				
		VF_XI		1.619		Vrms
		VF_RO (15 kΩ Load)		1.964		Vrms
		The Minimum 0 dBm0 Levels are:				
		VF_XI		87.0		mVrms
		VF_RO (Any Load ≥ 300Ω)		105.0		mVrms
		Overload Levels are 3.17 dBm0 (μLaw) and 3.14 dBm0 (A-Law)				
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for Maximum 0 dBm0 Test Level. (All 1's in gain register) Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at $D_X0/1$. T_A = 25°C	**−0.15**		**0.15**	dB
G_{XAG}	Transmit Gain Variation with Programmed Gain	Measure Transmit Gain Over the Range from Maximum to Minimum. Calculate the Deviation from the Programmed Gain Relative to G_{XA}, i.e., $G_{XAG} = G_{actual} - G_{prog} - G_{XA}$. T_A = 25°C, V_{CC} = 5V, V_{BB} = 5V	**−0.1**		**0.1**	dB
G_{XAF}	Transmit Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4) Minimum Gain < G_X < Maximum Gain				
		f = 60 Hz			−26	dB
		f = 200 Hz	−1.8		−0.1	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 4000 Hz			−14	dB
		f ≥ 4600 Hz. Measure Response at Alias Frequency from 0 kHz to 4 kHz. G_X = 0 dB, VF_XI = 1.619 Vrms			−32	dB
		Relative to 1015.625 Hz				
		f = 62.5 Hz			**−24.9**	dB
		f = 203.125 Hz	**−1.7**		**−0.1**	dB
		f = 343.75 Hz	**−0.15**		**0.15**	dB
		f = 515.625 Hz	**−0.15**		**0.15**	dB
		f = 2140.625 Hz	**−0.15**		**0.15**	dB
		f = 3156.25 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.74**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
		Relative to 1062.5 Hz (Note 4)				
		f = 5250 Hz, Measure 2750 Hz			**−32**	dB
		f = 11750 Hz, Measure 3750 Hz			**−32**	dB
		f = 49750 Hz, Measure 1750 Hz			**−32**	dB
G_{XAT}	Transmit Gain Variation with Temperature	Measured Relative to G_{XA}, V_{CC} = 5V, V_{BB} = −5V, Minimum gain < G_X < Maximum Gain	−0.1		0.1	dB
		−40°C to +85°C (TP3070A/71-X)	−0.15		0.15	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C (−40°C to +85°C for TP3070A/71A-X) by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE (Continued)						
G_{XAL}	Transmit Gain Variation with Signal Level	Sinusoidal Test Method. Reference Level = 0 dBm0.				
		VF_XI = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		VF_XI = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		VF_XI = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
G_{RA}	Receive Gain Absolute Accuracy	Receive Gain Programmed for Maximum 0 dBm0 Test Level (All 1's in Gain Register). Apply 0 dBm0 PCM Code to D_R0 or D_R1. Measure VF_RO. T_A = 25°C	**−0.15**		**0.15**	dB
G_{RAG}	Receive Gain Variation with Programmed Gain	Measure Receive Gain Over the Range from Maximum to Minimum Setting. Calculate the Deviation from the Programmed Gain Relative to G_{RA}, i.e. $G_{RAG} = G_{actual} - G_{prog} - G_{RA}$. T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V	**−0.1**		**0.1**	dB
G_{RAT}	Receive Gain Variation with Temperature	Measured Relative to G_{RA}.				
		V_{CC} = 5V, V_{BB} = −5V.	−0.1		0.1	dB
		Minimum Gain < G_R < Maximum Gain				
		−40°C to +85°C (TP3070A/71-X)	−0.15		0.15	dB
G_{RAF}	Receive Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4) D_R0 or D_R1 = 0 dBm0 code. Minimum Gain < G_R < Maximum Gain				
		f = 200 Hz	−0.25		0.15	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 4000 Hz			−14	dB
		G_R = 0 dB, D_R0 = 0 dBm0 Code, G_X = 0 dB (Note 4)				
		f = 296.875 Hz	**−0.15**		**0.15**	dB
		f = 1875.00 Hz	**−0.15**		**0.15**	dB
		f = 2906.25 Hz	**−0.15**		**0.15**	dB
		f = 2984.375 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.74**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
G_{RAL}	Receive Gain Variation with Signal Level	Sinusoidal Test Method. Reference Level = 0 dBm0.				
		D_R0 = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		D_R0 = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		D_R0 = −55 dBm0 to − 50 dBm0	**−1.2**		**1.2**	dB
		D_R0 = 3.1 dBm0				
		R_L = 600Ω, G_R = −0.5 dB	−0.2		0.2	dB
		R_L = 300Ω, G_R = −1.2 dB	**−0.2**		**0.2**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C (−40°C to +85°C for TP3070A/71A-X) by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Tx Delay, Absolute	f = 1600 Hz			315	μs
D_{XR}	Tx Delay, Relative to D_{XA}	f = 500–600 Hz			220	μs
		f = 600–800 Hz			145	μs
		f = 800–1000 Hz			75	μs
		f = 1000–1600 Hz			40	μs
		f = 1600–2600 Hz			75	μs
		f = 2600–2800 Hz			105	μs
		f = 2800–3000 Hz			155	μs
D_{RA}	Rx Delay, Absolute	f = 1600 Hz			200	μs
D_{RR}	Rx Delay, Relative to D_{RA}	f = 500–1000 Hz	−40			μs
		f = 1000–1600 Hz	−30			μs
		f = 1600–2600 Hz			90	μs
		f = 2600–2800 Hz			125	μs
		f = 2800–3000 Hz			175	μs
NOISE						
N_{XC}	Transmit Noise, C Message Weighted, μ-law Selected	(Note 1) All '1's in Gain Register		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted, A-law Selected	(Note 1) All '1's in Gain Register		−74	**−67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted, μ-law Selected	PCM Code is Alternating Positive and Negative Zero		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted, A-law Selected	PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 100 mVrms				
		f = 0 kHz–4 kHz (Note 2)	**36**			dBC
		f = 4 kHz–50 kHz	30			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB} = −5.0 V_{DC} + 100 mVrms				
		f = 0 kHz–4 kHz (Note 2)	**36**			dBC
		f = 4 kHz–50 kHz	30			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz–4000 Hz	**36**			dBC
		f = 4 kHz–25 kHz	40			dB
		f = 25 kHz–50 kHz	36			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB} = −5.0 V_{DC} + 100 mVrms Measure VF_RO				
		f = 0 Hz–4000 Hz	**36**			dBC
		f = 4 kHz–25kHz	40			dB
		f = 25 kHz–50 kHz	36			dB
SOS	Spurious Out-of-Band Signals at the Channel Output	0 dBm0, 300 Hz to 3400 Hz Input PCM Code Applied at D_R0 (or D_R1)				
		4600 Hz–7600 Hz			**−30**	dB
		7600 Hz–8400 Hz			**−40**	dB
		8400 Hz–50,000 Hz			**−30**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C (−40°C to +85°C for TP3070A/71A-X) by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB gain), hybrid balance filter disabled. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel, μ-law Selected	Sinusoidal Test Method Level = 3.0 dBm0 = 0 dBm0 to − 30 dBm0 = −40 dBm0 = −45 dBm0	 **33** **36** **30** **25**			 dBC dBC dBC dBC
STD_{RL}	Signal to Total Distortion Receive with Resistive Load	Sinusoidal Test Method Level = +3.1 dBm0 R_L = 600Ω, G_R = −0.5 dB R_L = 300Ω, G_R = −1.2 dB	 33 **33**			 dBC dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Transmit or Receive Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Idle Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz (Note 2)		−90	**−70**	dB

Note 1: Measured by grounded input at VF_XI.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI.

Note 3: A signal is Valid if it is above V_{IH} or below V_{IL} and Invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification the following conditions apply:

a) All input signals are defined as: V_{IL} = 0.4V, V_{IH} = 2.7V, t_R < 10 ns, t_F < 10 ns.

b) t_R is measured from V_{IL} to V_{IH}. t_F is measured from V_{IH} to V_{IL}.

c) Delay Times are measured from the input signal Valid to the output signal Valid.

d) Setup Times are measured from the data input Valid to the clock input Invalid.

e) Hold Times are measured from the clock signal Valid to the data input Invalid.

f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}.

Note 4: A multi-tone test technique is used.

National Semiconductor

TP3075A, TP3076A COMBO II™ Programmable PCM CODEC/Filter for ISDN and Digital Phone Applications

General Description

The TP3075A and TP3076A are second-generation combined PCM CODEC and Filter devices optimized for digital switching applications on subscriber line and trunk cards and digital phone applications. Using advanced switched capacitor techniques, COMBO II combines transmit bandpass and receive lowpass channel filters with a companding PCM encoder and decoder. The devices are A-law and μ-law selectable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions may be controlled via a serial control port.

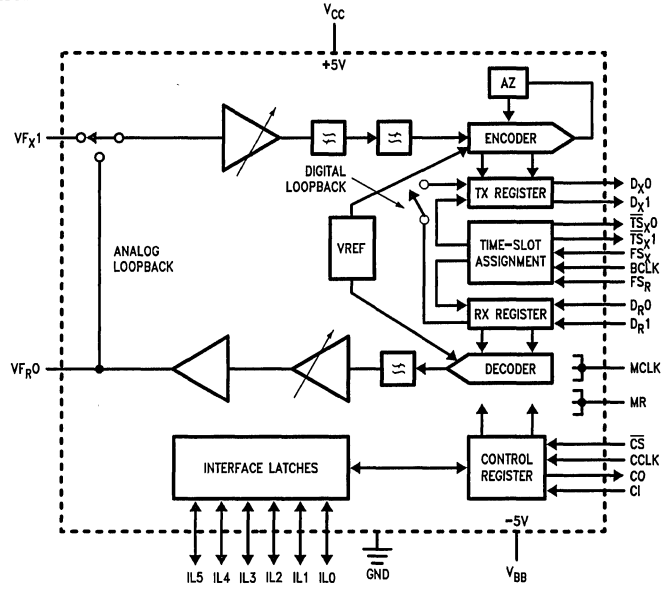
Channel gains are programmable over a 25.4 dB range in each direction.

To enable COMBO II to interface to the SLIC control leads, a number of programmable latches are included; each may be configured as either an input or an output. The TP3075A provides 6 latches and the TP3076A 4 latches.

Features

- Complete CODEC and Filter system including:
  - — Transmit and receive PCM channel filters
  - — μ-law or A-law companding coder and decoder
  - — Receive power amplifier drives 300Ω
  - — 4.096 MHz serial PCM data (max)
- Programmable functions:
  - — Transmit gain: 25.4 dB range, 0.1 dB steps
  - — Receive gain: 25.4 dB range, 0.1 dB steps
  - — Time-slot assignment; up to 64 slots/frame
  - — 2 port assignment (TP3075A)
  - — 6 interface latches (TP3075A), 4 latches (TP3076A)
  - — A or μ-law
  - — Analog loopback
  - — Digital loopback
- Direct interface to solid-state SLICs
- Standard serial control interface
- 80 mW operating power (typ)
- 1.5 mW standby power (typ)
- Meets or exceeds all CCITT and LSSGR specifications
- TTL and CMOS compatible digital interfaces

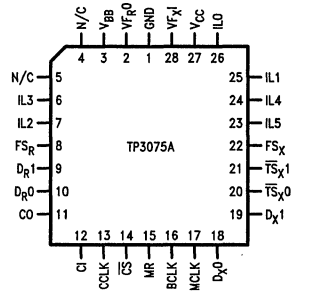
Block Diagram



TL/H/9758-1

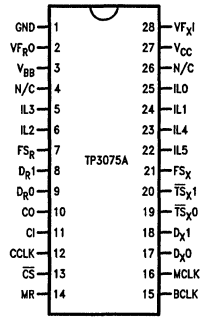
FIGURE 1

Connection Diagrams



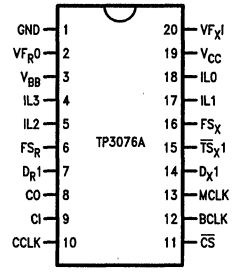
TL/H/9758-2

Order Number TP3075AV
See NS Package Number V28A



TL/H/9758-3

Order Number TP3075AJ
See NS Package Number J28A



TL/H/9758-4

Order Number TP3076AJ
See NS Package Number J20A

Pin Descriptions

Pin	Description
V_{CC}	+5V ±5% power supply.
V_{BB}	−5V ±5% power supply.
GND	Ground. All analog and digital signals are referenced to this pin.
FS_X	Transmit Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the transmit time slot assigned to this device (non-delayed data timing mode), or the start of the transmit frame (delayed data timing mode using the internal time-slot assignment counter).
FS_R	Receive Frame Sync input. Normally a pulse or squarewave with an 8 kHz repetition rate is applied to this input to define the start of the receive time slot assigned to this device (non-delayed data timing mode), or the start of the receive frame (delayed data timing mode using the internal time-slot assignment counter).
BCLK	Bit clock input used to shift PCM data into and out of the D_R and D_X pins. BCLK may vary from 64 kHz to 4.096 MHz in 8 kHz increments, and must be synchronous with MCLK.
MCLK	Master clock input used by the switched capacitor filters and the encoder and decoder sequencing logic. Must be 512 kHz, 1.536/1.544 MHz, 2.048 MHz or 4.096 MHz and synchronous with BCLK.
VF_XI	The Transmit analog high-impedance input. Voice frequency signals present on this input are encoded as an A-law or μ-law PCM bit stream and shifted out on the selected D_X pin.
VF_RO	The Receive analog power amplifier output, capable of driving load impedances as low as 300Ω (depending on the peak overload level required). PCM data received on the assigned D_R pin is decoded and appears at this output as voice frequency signals.
D_X0 D_X1	D_X0 is available on the TP3075A only; D_X1 is available on all devices. These Transmit Data TRI-STATE® outputs remain in the high impedance state except during the assigned transmit time slot on the assigned port, during which the transmit PCM data byte is shifted out on the rising edges of BCLK.

Pin	Description
$\overline{TS}_X0$ $\overline{TS}_X1$	$\overline{TS}_X0$ is available on the TP3075A only; $\overline{TS}_X1$ is available on all devices. Normally these open drain outputs are floating in a high impedance state except when a time-slot is active on one of the D_X outputs, when the appropriate $\overline{TS}_X$ output pulls low to enable a backplane line-driver.
D_R0 D_R1	D_R0 is available on the TP3075A only; D_R1 is available on all devices. These receive data input(s) are inactive except during the assigned receive time slot of the assigned port when the receive PCM data is shifted in on the falling edges of BCLK.
CCLK	Control Clock input. This clock shifts serial control information into CI or out from CO when the $\overline{CS}$ input is low, depending on the current instruction. CCLK may be asynchronous with the other system clocks.
CI	Control Data Input pin. Serial control information is shifted into COMBO II on this pin when $\overline{CS}$ is low. Byte 1 of control information is always written into COMBO II, while the direction of byte 2 data is determined by bit 2 of byte 1, as defined in Table I.
CO	Control Data Output pin. Serial control or status information is shifted out of COMBO II on this pin when $\overline{CS}$ is low.
$\overline{CS}$	Chip Select input. When this pin is low, control information can be written to or read from COMBO II via CI or CO.
IL5–IL0	IL5 through IL0 are available on the TP3075A. IL3 through IL0 are available on the TP3076A. Each Interface Latch I/O pin may be individually programmed as an input or an output determined by the state of the corresponding bit in the Latch Direction Register (LDR). For pins configured as inputs, the logic state sensed on each input is latched into the Interface Latch Register (ILR) whenever control data is written to COMBO II, while $\overline{CS}$ is low, and the information is shifted out on the CO pin. When configured as outputs, control data written into the ILR appears at the corresponding IL pins.

Pin Descriptions (Continued)

Pin	Description
MR	MR is available on the TP3075A only. This logic input must be pulled low for normal operation of COMBO II. When pulled momentarily high (at least 1 μs), all programmable registers in the device are reset to the states specified under "Power-On Initialization".

Functional Description

POWER-ON INITIALIZATION

When power is first applied, power-on reset circuitry initializes the COMBO II and puts it into the power-down state. The gain control registers for the transmit and receive gain sections are programmed for no output, the power amp is disabled and the device is in the non-delayed timing mode. The Latch Direction Register (LDR) is pre-set with all IL pins programmed as inputs, placing the SLIC interface pins in a high impedance state. The CO pin is in TRI-STATE condition. Other initial states in the Control Register are indicated in Section 2.0.

A reset to these same initial conditions may also be forced by driving the MR pin momentarily high (TP3075A only). This may be done either when powered-up or down. For normal operation this pin must be pulled low. If not used, MR should be hardwired to ground.

The desired modes for all programmable functions may be initialized via the control port prior to a Power-up command.

POWER-DOWN STATE

Following a period of activity in the powered-up state the power-down state may be re-entered by writing any of the control instructions into the serial control port with the "P" bit set to "1" as indicated in Table I. It is recommended that the chip be powered down before writing any additional instructions. In the power-down state, all non-essential circuitry is de-activated and the D_XO (and D_X1) outputs are in the high impedance TRI-STATE condition.

The data stored in the Gain Control registers, the LDR and ILR, and all control bits remain unchanged in the power-down state unless changed by writing new data via the serial control port, which remains active. The outputs of the Interface Latches also remain active, maintaining the ability to monitor and control the SLIC.

TRANSMIT FILTER AND ENCODER

The Transmit section input, VF_XI, is a high impedance input. No external components are necessary to set the gain. Following this is a programmable gain/attenuation amplifier which is controlled by the contents of the Transmit Gain Register (see Programmable Functions section). An active pre-filter then precedes the 3rd order high-pass and 5th order low-pass switched capacitor filters. The A/D converter has a compressing characteristic according to the standard CCITT A or μ255 coding laws, which must be selected by a control instruction during initialization (see Tables I and II). A precision on-chip voltage reference ensures accurate and highly stable transmission levels. Any offset voltage arising in the gain-set amplifier, the filters or the comparator is canceled by an internal auto-zero circuit.

Each encode cycle begins immediately following the assigned Transmit time-slot. The total signal delay referenced to the start of the time-slot is approximately 165 μs (due to the Transmit Filter) plus 125 μs (due to encoding delay), which totals 290 μs. Data is shifted out on D_X0 or D_X1 during the selected time slot on eight rising edges of BCLK.

DECODER AND RECEIVER FILTER

PCM data is shifted into the Decoder's Receive PCM Register via the D_R0 or D_R1 pin during the selected time-slot on the 8 falling edges of BCLK. The Decoder consists of an expanding DAC with either A or μ255 law decoding characteristic, which is selected by the same control instruction used to select the Encode law during initialization. Following the Decoder is a 5th order low-pass switched capacitor filter with integral Sin x/x correction for the 8 kHz sample and hold. A programmable gain amplifier, which must be set by writing to the Receive Gain Register, is included, and finally a Power Amplifier capable of driving a 300Ω load to ±3.5V, a 600Ω load to ±3.8V or a 15 kΩ load to ±4.0V at peak overload.

TABLE I. Programmable Register Instructions

Function	Byte 1 (Notes 1, 2, 3)								Byte 2 (Note 1)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Single Byte Power-Up/Down	P	X	X	X	X	X	0	X	None							
Write Control Register	P	0	0	0	0	0	1	X	See Table II							
Read-Back Control Register	P	0	0	0	0	1	1	X	See Table II							
Write to Interface Latch Register	P	0	0	0	1	0	1	X	See Table V							
Read Interface Latch Register	P	0	0	0	1	1	1	X	See Table V							
Write Latch Direction Register	P	0	0	1	0	0	1	X	See Table IV							
Read Latch Direction Register	P	0	0	1	0	1	1	X	See Table IV							
Write Receive Gain Register	P	0	1	0	0	0	1	X	See Table VIII							
Read Receive Gain Register	P	0	1	0	0	1	1	X	See Table VIII							
Write Transmit Gain Register	P	0	1	0	1	0	1	X	See Table VII							
Read Transmit Gain Register	P	0	1	0	1	1	1	X	See Table VII							
Write Receive Time-Slot/Port	P	1	0	0	1	0	1	X	See Table VI							
Read-Back Receive Time-Slot/Port	P	1	0	0	1	1	1	X	See Table VI							
Write Transmit Time-Slot/Port	P	1	0	1	0	0	1	X	See Table VI							
Read-Back Transmit Time-Slot/Port	P	1	0	1	0	1	1	X	See Table VI							

Note 1: Bit 7 of bytes 1 and 2 is always the first bit clocked into or out from the CI or CO pin. X = don't care.

Note 2: "P" is the power-up/down control bit, see Power-up/Down Control section. ("0" = Power Up, "1" = Power Down)

Note 3: Other register address codes are invalid and should not be used.

Functional Description (Continued)

A decode cycle begins immediately after the assigned receive timeslot, and 10 μs later the Decoder DAC output is updated. The total signal delay is 10 μs plus 120 μs (filter delay) plus 62.5 μs (½ frame) which gives approximately 190 μs.

PCM INTERFACE

The FS_X and FS_R frame sync inputs determine the beginning of the 8-bit transmit and receive time-slots respectively. They may have any duration from a single cycle of BCLK HIGH to one MCLK period LOW. Two different relationships may be established between the frame sync inputs and the actual time-slots on the PCM busses by setting bit 3 in the Control Register (see Table II). Non-delayed data mode is similar to long-frame timing on the TP3050/60 series of devices (COMBO®); time-slots begin nominally coincident with the rising edge of the appropriate FS input. The alternative is to use Delayed Data mode, which is similar to shortframe sync timing on COMBO, in which each FS input must be high at least a half-cycle of BCLK earlier than the timeslot. The Time-Slot Assignment circuit on the device can only be used with Delayed Data timing.

When using Time-Slot Assignment, the beginning of the first time-slot in a frame is identified by the appropriate FS input. The actual transmit and receive time-slots are then determined by the internal Time-Slot Assignment counters.

Transmit and Receive frames and time-slots may be skewed from each other by any number of BCLK cycles. During each assigned Transmit time-slot, the selected $D_X0/1$ output shifts data out from the PCM register on the rising edges of BCLK. $\overline{TS}_X0$ (or $\overline{TS}_X1$ as appropriate) also pulls low for the first 7½ bit times of the time-slot to control the TRI-STATE Enable of a backplane line-driver. Serial PCM data is shifted into the selected $D_R0/1$ input during each assigned Receive time-slot on the falling edges of BCLK. D_X0 or D_X1 and D_R0 or D_R1 are selectable on the TP3075A only, see Section 6.

SERIAL CONTROL PORT

Control information and data are written into or read-back from COMBO II via the serial control port consisting of the control clock CCLK, the serial data input, CI, and output, CO, and the Chip Select input, $\overline{CS}$. All control instructions require 2 bytes, as listed Table I, with the exception of a single byte power-up/down command. The Byte 1 bits are used as follows: bit 7 specifies power up or power down; bits 6, 5, 4 and 3 specify the register address, bit 2 specifies whether the instruction is read or write; bit 1 specifies a one or two byte instruction; and bit 0 is not used.

To shift control data into COMBO II, CCLK must be pulsed high 8 times while $\overline{CS}$ is low. Data on the CI input is shifted into the serial input register on the falling edge of each CCLK pulse. After all data is shifted in, the contents of the input shift register are decoded, and may indicate that a 2nd byte of control data will follow. This second byte may either be defined by a second byte-wide $\overline{CS}$ pulse or may follow the first contiguously, i.e, it is not mandatory for $\overline{CS}$ to return high between the first and second control bytes. At the end of CCLK8 in the 2nd control byte the data is loaded into the appropriate programmable register. $\overline{CS}$ may remain low continuously when programming successive registers, if desired. However, $\overline{CS}$ must be set high when no data transfers are in progress.

To readback Interface Latch data or status information from COMBO II, the first byte of the appropriate instruction is strobed in during the first $\overline{CS}$ pulse, as defined in Table I. $\overline{CS}$ must then be taken low for a further 8 CCLK cycles, during which the data is shifted onto the CO pin on the rising edges of CCLK. When $\overline{CS}$ is high the CO pin is in the high-impedance TRI-STATE, enabling the CI and CO pins of many devices to be multiplexed together.

Programmable Functions

1.0 POWER-UP/DOWN CONTROL

Following power-on initialization, power-up and power-down control may be accomplished by writing any of the control instructions listed in Table I into COMBO II with the "P" bit set to "0" for power-up or "1" for power-down. Normally it is recommended that all programmable functions be initially programmed while the device is powered down. Power state control can then be included with the last programming instruction or the separate single-byte instruction. Any of the programmable registers may also be modified while the device is powered-up or down by setting the "P" bit as indicated. When the power-up or down control is entered as a single byte instruction, bit one (1) must be reset to a 0.

When a power-up command is given, all de-activated circuits are activated, but the TRI-STATE PCM output(s), D_X0 (and D_X1), will remain in the high impedance state until the second FS_X pulse after power-up.

2.0 CONTROL REGISTER INSTRUCTION

The first byte of a READ or WRITE instruction to the Control Register is as shown in Table I. The second byte has the following bit functions:

TABLE II. Control Register Byte 2 Functions

Bit Number and Name								Function
7	6	5	4	3	2	1	0	
F_1	F_0	MA	IA	DN	DL	AL	PP	
0	0							MCLK = 512 kHz
0	1							MCLK = 1.536 MHz or 1.544 MHz
1	0							MCLK = 2.048 MHz*
1	1							MCLK = 4.096 MHz
		0	X					Select μ255 Law*
		1	0					A-Law, Including Even Bit Inversion
		1	1					A-Law, No Even Bit Inversion
				0				Delay Data Timing
				1				Non-Delayed Data Timing*
					0	0		Normal Operation*
					1	X		Digital Loopback
					0	1		Analog Loopback
							0	Power Amp Enabled in PDN
							1	Power Amp Disabled in PDN*

* = state at power-on initialization.

2.1 Master Clock Frequency Selection

A Master clock must be provided to COMBO II for operation of the filter and coding/decoding functions. The MCLK frequency must be either 512 kHz, 1.536 MHz, 1.544 MHz, 2.048 MHz, or 4.096 MHz and must be synchronous with BCLK. Bits F_1 and F_0 (see Table II) must be set during initialization to select the correct internal divider.

Programmable Functions (Continued)

TABLE III. Coding Law Conventions

	μ255 Law		True A-Law with Even Bit Inversion		A-Law without Even Bit Inversion	
	MSB	LSB	MSB	LSB	MSB	LSB
V_{IN} = +Full Scale	10000000		10101010		111111111	
V_{IN} = 0V	11111111		11010101		100000000	
	11111111		01010101		000000000	
V_{IN} = −Full Scale	00000000		00101010		011111111	

Note 1: The MSB is always the first PCM bit shifted in or out of COMBO II.

2.2 Coding Law Selection

Bits "MA" and "IA" in Table II permit the selection of μ255 coding or A-law coding, with or without even bit inversion.

2.3 Analog Loopback

Analog Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. In the analog loopback mode, the Transmit input VF_XI is isolated from the input pin and internally connected to the VF_RO output, forming a loop from the Receive PCM Register back to the Transmit PCM Register. The VF_RO pin remains active, and the programmed settings of the Transmit and Receive gains remain unchanged, thus care must be taken to ensure that overload levels are not exceeded anywhere in the loop.

2.4 Digital Loopback

Digital Loopback mode is entered by setting the "AL" and "DL" bits in the Control Register as shown in Table II. This mode provides another stage of path verification by enabling data written into the Receive PCM Register to be read back from that register in any Transmit time-slot at $D_X0/1$. PCM decoding continues and analog output appears at VF_R0. The output can be disabled by programming 'No Output' in the Receive Gain Register (see Table VIII).

3.0 INTERFACE LATCH DIRECTIONS

Immediately following power-on, all Interface Latches assume they are inputs, and therefore all IL pins are in a high impedance state. Each IL pin may be individually programmed as a logic input or output by writing the appropriate instruction to the LDR, see Tables I and IV. For minimum power dissipation, unconnected latch pins should be programmed as outputs. For the TP3076A, L4 and L5 should always be programmed as outputs.

Bits L_5–L_0 must be set by writing the specific instruction to the LDR with the L bits in the second byte set as follows:

TABLE IV. Byte 2 Functions of Latch Direction Register

Byte 2 Bit Number							
7	6	5	4	3	2	1	0
L_0	L_1	L_2	L_3	L_4	L_5	X	X

L_n Bit	IL Direction
0	Input
1	Output

X = Don't Care

4.0 INTERFACE LATCH STATES

Interface Latches configured as outputs assume the state determined by the appropriate data bit in the 2-byte instruction written to the Interface Latch Register (ILR) as shown in Tables I and V. Latches configured as inputs will sense the state applied by an external source, such as the Off-Hook detect output of a SLIC. All bits of the ILR, i.e. sensed inputs and the programmed state of outputs, can be read back in the 2nd byte of a READ from the ILR.

It is recommended that during initialization, the state of IL pins to be configured as outputs should be programmed first followed immediately by the Latch Direction Register.

TABLE V. Interface Latch Data Bit Order

Bit Number							
7	6	5	4	3	2	1	0
D_0	D_1	D_2	D_3	D_4	D_5	X	X

5.0 TIME-SLOT ASSIGNMENT

COMBO II can operate in either fixed time-slot or time-slot assignment mode for selecting the Transmit and Receive PCM time-slots. Following power-on, the device is automatically in Non-Delayed Timing mode, in which the time-slot always begins with the leading (rising) edge of frame sync inputs FS_X and FS_R. Time-Slot Assignment may only be used with Delay Data timing; see *Figure 4*. FS_X and FS_R may have any phase relationship with each other in BCLK period increments.

Alternatively, the internal time-slot assignment counters and comparators can be used to access any time-slot in a frame, using the frame sync inputs as marker pulses for the beginning of transmit and receive time-slot 0. In this mode, a frame may consist of up to 64 time-slots of 8 bits each. A time-slot is assigned by a 2-byte instruction as shown in Tables I and VI. The last 6 bits of the second byte indicate the selected time-slot from 0–63 using straight binary notation. A new assignment becomes active on the second frame following the end of the Chip-Select for the second control byte. The "EN" bit allows the PCM inputs, $D_R0/1$, or outputs, $D_X0/1$, as appropriate, to be enabled or disabled.

Time-Slot Assignment mode requires that the FS_X and FS_R pulses conform to the delayed data timing format shown in *Figure 4*.

6.0 PORT SELECTION

On the TP3075A only, an additional capability is available; 2 Transmit serial PCM ports, D_X0 and D_X1, and 2 Receive serial PCM ports, D_R0 and D_R1, are provided to enable two-way space switching to be implemented. Port selections for transmit and receive are made within the appropriate time-slot assignment instructions using the "PS" bit in the second byte.

On the TP3076A, only ports D_X1 and D_R1 are available, therefore the "PS" bit MUST always be set to 1 for these devices.

Table VI shows the format for the second byte of both transmit and receive time-slot and port assignment instructions.

Programmable Functions (Continued)

TABLE VI. Time-Slot and Port Assignment Instruction

Bit Number and Name								Function
7 EN	6 PS (Note 1)	5 T_5 (Note 2)	4 T_4	3 T_3	2 T_2	1 T_1	0 T_0	
0	0	X	X	X	X	X	X	Disable D_X0 Output (Transmit Instruction) Disable D_R0 Input (Receive Instruction)
0	1	X	X	X	X	X	X	Disable D_X1 Output (Transmit Instruction) Disable D_R1 Input (Receive Instruction)
1	0	Assign One Binary Coded Time-Slot from 0–63 Assign One Binary Coded Time-Slot from 0–63						Enable D_X0 Output (Transmit Instruction) Enable D_R0 Input (Transmit Instruction)
1	1	Assign One Binary Coded Time-Slot from 0–63 Assign One Binary Coded Time-Slot from 0–63						Enable D_X1 Output (Transmit Instruction) Enable D_R1 Input (Transmit Instruction)

Note 1: The "PS" bit MUST be set to "1" for both transmit and receive for the TP3076A.

Note 2: T5 is the MSB of the time-slot assignment bit field. Time-slot bits should be set to "000000" for both transmit and receive when operating in non-delayed data timing mode.

7.0 TRANSMIT GAIN INSTRUCTION BYTE 2

The transmit gain can be programmed in 0.1 dB steps by writing to the Transmit Gain Register as defined in Tables I and VII. This corresponds to a range of 0 dBm0 levels at VF_XI between 1.375 Vrms and 0.074 Vrms (equivalent to +5.0 dBm to −20.4 dBm in 600Ω).

To calculate the binary code for byte 2 of this instruction for any desired input 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.07299)$$

and convert to the binary equivalent. Some examples are given in Table VII.

It should be noted that the Transmit (idle channel) Noise and Transmit Signal to Total Distortion are both specified with transmit gain set to 0 dB. At high transmit gains there will be some degradation in noise performance for these parameters. See Application Note AN-614 for more information on this subject.

TABLE VII. Byte 2 of Transmit Gain Instruction

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_XI
0 0 0 0 0 0 0 0	No Output
0 0 0 0 0 0 0 1	0.074
0 0 0 0 0 0 1 0	0.075
—	—
1 1 1 1 1 1 1 0	1.359
1 1 1 1 1 1 1 1	1.375

8.0 RECEIVE GAIN INSTRUCTION BYTE 2

The receive gain can be programmed in 0.1 dB steps by writing to the Receive Gain Register as defined in Tables I and VIII. Note the following restrictions on output drive capability:

a. 0 dBm0 levels ≤ 1.96 Vrms at VF_RO may be driven into a load of ≥ 15 kΩ to GND; Receive Gain set to 0 dB.

b. 0 dBm0 levels ≤ 1.85 Vrms at VF_RO may be driven into a load of ≥ 600Ω to GND; Receive Gain set to 0.5 dB.

c. 0 dBm0 levels ≤ 1.71 Vrms at VF_RO may be driven into a load of ≥ 300 Ω to GND. Receive Gain set to −1.2 dB.

To calculate the binary code for byte 2 of this instruction for any desired output 0 dBm0 level in Vrms, take the nearest integer to the decimal number given by:

$$200 \times \log_{10} (V/0.1043)$$

and convert to the binary equivalent. Some examples are given in Table VIII.

TABLE VIII. Byte 2 of Receive Gain Instruction

Bit Number 7 6 5 4 3 2 1 0	0 dBm0 Test Level (Vrms) at VF_RO
0 0 0 0 0 0 0 0	No Output (Low Z to GND)
0 0 0 0 0 0 0 1	0.105
0 0 0 0 0 0 1 0	0.107
—	—
1 1 1 1 1 1 1 0	1.941
1 1 1 1 1 1 1 1	1.964

Applications Information

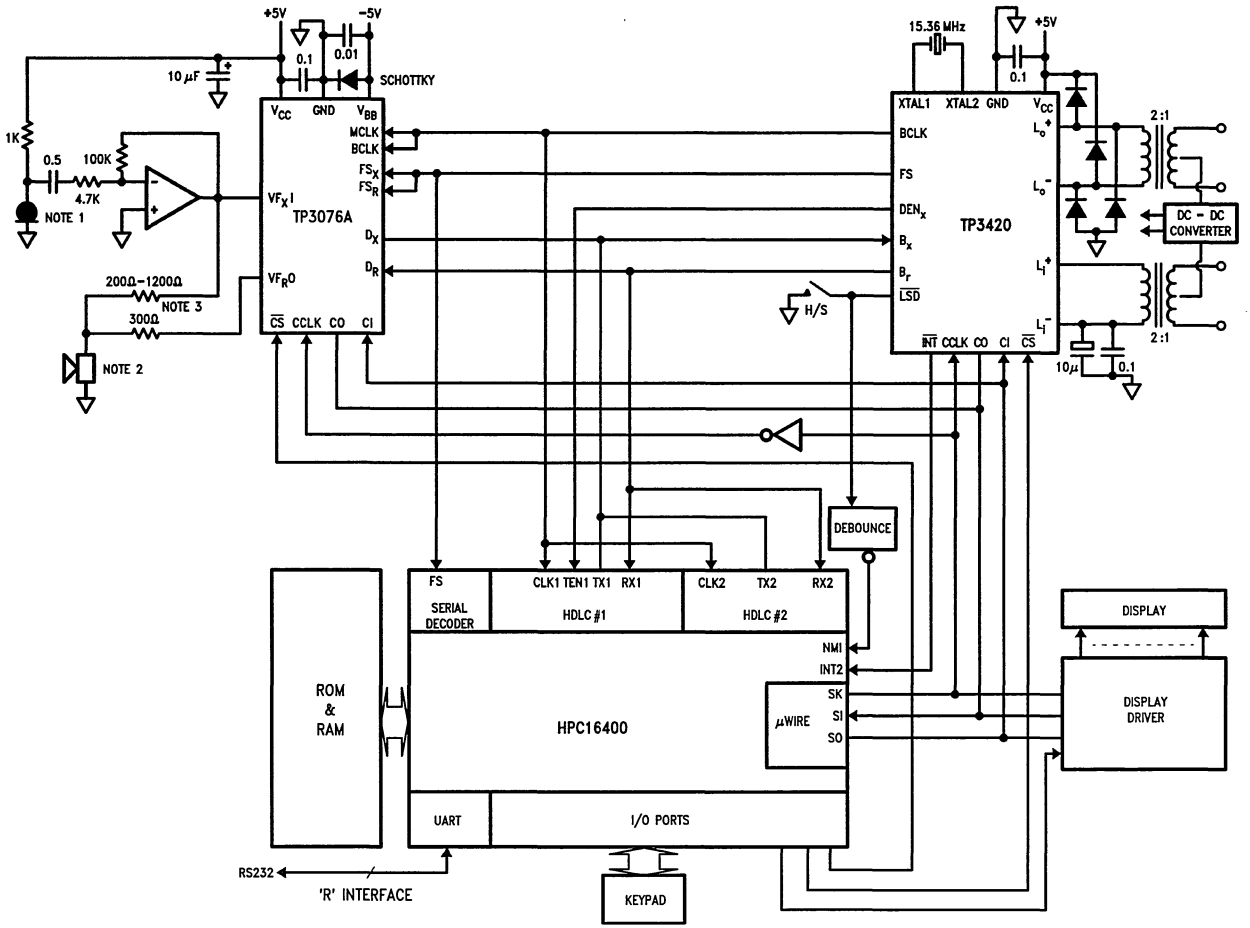
Figure 2 shows a typical ISDN phone application of the TP3076A together with a TP3420 ISDN Transceiver "S" Interface Device and HPC16400 High-Performance Microcontroller with HDLC Controller. The TP3076A device is programmed over its serial control interface via the HPC16400 MICROWIRE/PLUS™ serial I/O port.

POWER SUPPLIES

While the pins of the TP3075A and TP3076A COMBO II devices are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used and a Schottky diode connected between V_{BB} and GND.

To minimize noise sources all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. Power supply decoupling capacitors of 0.1 μF should be connected from this common point to V_{CC} and V_{BB} as close to the device pins as possible.

Further guidelines on PCB layout techniques are provided in Application Note AN-614, "COMBO II™ Programmable PCM CODEC/Filter Family Application Guide".



TL/H/9758–5

Note 1: Primotype EM80–PMI2 or similar.

Note 2: Primotype DH31 or similar.

Note 3: Sidetone ≅ −9.2 dB for 200Ω,
Sidetone ≅ −21.5 dB for 1200Ω.

FIGURE 2. Typical Application in an ISDN Phone

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at VF_XI	V_{CC} +0.5V to V_{BB} −0.5V
Voltage at Any Digital Input	V_{CC} +0.5V to GND −0.5V
Storage Temperature Range	−65°C to +150°C
V_{BB} to GND	−7V
Current at VF_RO	±100 mA
Current at Any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs (DC Meas.)			**0.7**	V
V_{IH}	Input High Voltage	All Digital Inputs (DC Meas.)*	**2.0**			V
V_{OL}	Output Low Voltage	D_X0, D_X1, $\overline{TS}_X0$, $\overline{TS}_X1$, and CO, I_L = 3.2 mA, All Other Digital Outputs, I_L = 1 mA			**0.4**	V
V_{OH}	Output High Voltage	D_X0, D_X1 and CO, I_L = −3.2 mA, All Other Digital Outputs (except $\overline{TS}_X$), I_L = −1 mA All Digital Outputs, I_L = −100 μA	**2.4** V_{CC} − 0.5			V V
I_{IL}	Input Low Current	Any Digital Input, GND < V_{IN} < V_{IL}	**−10**		**10**	μA
I_{IH}	Input High Current	Any Digital Input, except MR, V_{IH} < V_{IN} < V_{CC} MR Only	**−10** **−10**		**10** **100**	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE®)	D_X0, D_X1 and CO IL5–IL0 when Selected as Inputs GND < V_{OUT} < V_{CC}	**−10**		**10**	μA
ANALOG INTERFACES						
I_{VFXI}	Input Current, VF_XI	−3.3V < VF_XI < 3.3V	**−1.0**		**1.0**	μA
R_{VFXI}	Input Resistance	−3.3V < VF_XI < 3.3V	**1.0**			MΩ
VOS_X	Input Offset Voltage Applied at VF_XI	Transmit Gain = 0 dB Transmit Gain = 25.40 dB			200 10	mV mV
RL_{VFRO}	Load Resistance	Receive Gain = 0 dB Receive Gain = −0.5 dB Receive Gain = −1.2 dB	15k 600 **300**			Ω
CL_{VFRO}	Load Capacitance	RL_{VFRO} ≤ 300Ω CL_{VFRO} from VF_RO to GND			**200**	pF
RO_{VFRO}	Output Resistance	Steady Zero PCM Code Applied to D_R0 or D_R1		1.0	3.0	Ω
VOS_R	Output Offset Voltage at V_{FRO}	Alternating ± Zero PCM Code Applied D_{R0} or D_R1, Maximum Receive Gain	**−200**		**200**	mV
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	CCLK, CI, CO = 0.4V, $\overline{CS}$ = 2.4V Interface Latches Set as Outputs with No Load, All Other Inputs Active, Power Amp Disabled		0.1	**0.6**	mA
$I_{BB}0$	Power Down Current	As Above		−0.1	**−0.3**	mA
$I_{CC}1$	Power Up Current	CCLK, CI, CO = 0.4V, $\overline{CS}$ = 2.4V No Load on Power Amp Interface Latches Set as Outputs with No Load		8.0	**11.0**	mA
$I_{BB}1$	Power Up Current	As Above		−8.0	**−11.0**	mA
$I_{CC}2$	Power Down Current	As Above, Power Amp Enabled		2.0	**3.0**	mA
$I_{BB}2$	Power Down Current	As Above, Power Amp Enabled		−2.0	**−3.0**	mA

*See definitions and timing conventions section.

Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER CLOCK TIMING						
f_{MCLK}	Frequency of MCLK	Selection of Frequency is Programmable (See Table III)		512 1536 1544 2048 **4096**		kHz kHz kHz kHz kHz
t_{WMH}	Period of MCLK High	Measured from V_{IH} to V_{IH} (See Note)	**80**			ns
t_{WML}	Period of MCLK Low	Measured from V_{IL} to V_{IL} (See Note)	**80**			ns
t_{RM}	Rise Time of MCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FM}	Fall Time of MCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBM}	HOLD Time, BCLK LOW to MCLK HIGH		**50**			ns
t_{WFL}	Period of FS_X or FS_R Low	Measured from V_{IL} to V_{IL}	1			MCLK Period
PCM INTERFACE TIMING						
f_{BCLK}	Frequency of BCLK	May Vary from 64 kHz to 4096 kHz in 8 kHz Increments	**64**		**4096**	kHz
t_{WBH}	Period of BCLK High	Measured from V_{IH} to V_{IH}	**80**			ns
t_{WBL}	Period of BCLK Low	Measured from V_{IL} to V_{IL}	**80**			ns
t_{RB}	Rise Time of BCLK	Measured from V_{IL} to V_{IH}			30	ns
t_{FB}	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			30	ns
t_{HBF}	Hold Time, BCLK Low to $FS_{X/R}$ High or Low		**30**			ns
t_{SFB}	Setup Time, $FS_{X/R}$ High to BCLK Low		**30**			ns
t_{DBD}	Delay Time, BCLK High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads			**80**	ns
t_{DBZ}	Delay Time, BCLK Low to $D_X0/1$ Disabled if FS_X Low, FS_X Low to $D_X0/1$ disabled if 8th BCLK Low, or BCLK High to $D_X0/1$ Disabled if FS_X High		**15**		**80**	ns
t_{DBT}	Delay Time, BCLK High to $\overline{TS}_X$ Low if FS_X High, or FS_X High to $\overline{TS}_X$ Low if BCLK High	Load = 100 pF Plus 2 LSTTL Loads			60	ns
t_{ZBT}	TRI-STATE Time, BCLK Low to $\overline{TS}_X$ High if FS_X Low, FS_X Low to $\overline{TS}_X$ High if 8th BCLK Low, or BCLK High to $\overline{TS}_X$ High if FS_X High		15		60	ns
t_{DFD}	Delay Time, $FS_{X/R}$ High to Data Valid	Load = 100 pF Plus 2 LSTTL Loads, Applies if $FS_{X/R}$ Rises Later Than BCLK Rising Edge in Non-Delayed Data Mode Only			**80**	ns
t_{SDB}	Setup Time, $D_R0/1$ Valid to BCLK Low		**30**			ns
t_{HBD}	Hold Time, BCLK Low to $D_R0/1$ Invalid		**20**			ns

Note: Applies only to MCLK Frequencies ≥ 1.536 MHz. At 512 kHz a 50:50 ±2% Duty Cycle must be used.

Timing Specifications (Continued)

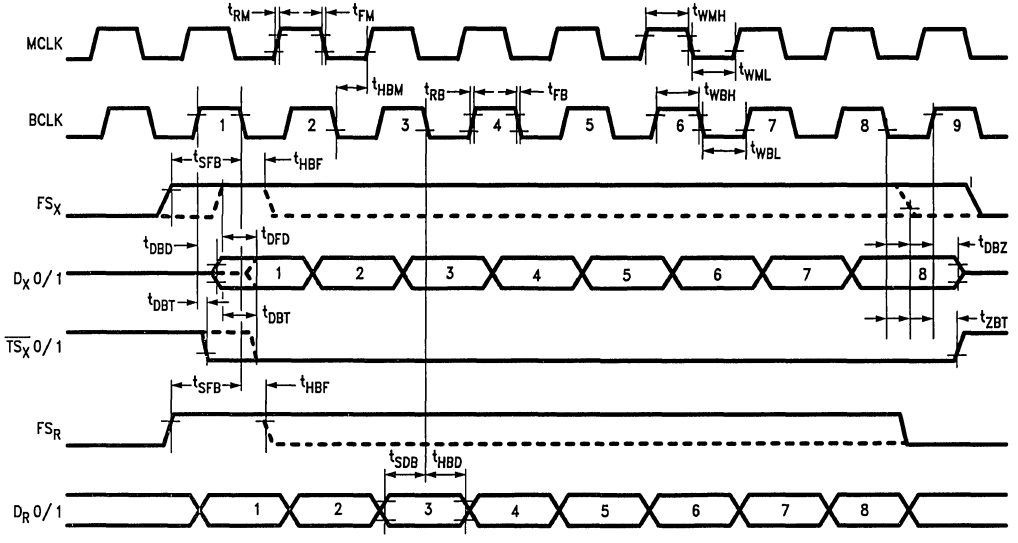
Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$; $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

All timing parameters are measured at $V_{OH} = 2.0V$ and $V_{OL} = 0.7V$.

See Definitions and Timing Conventions section for test methods information.

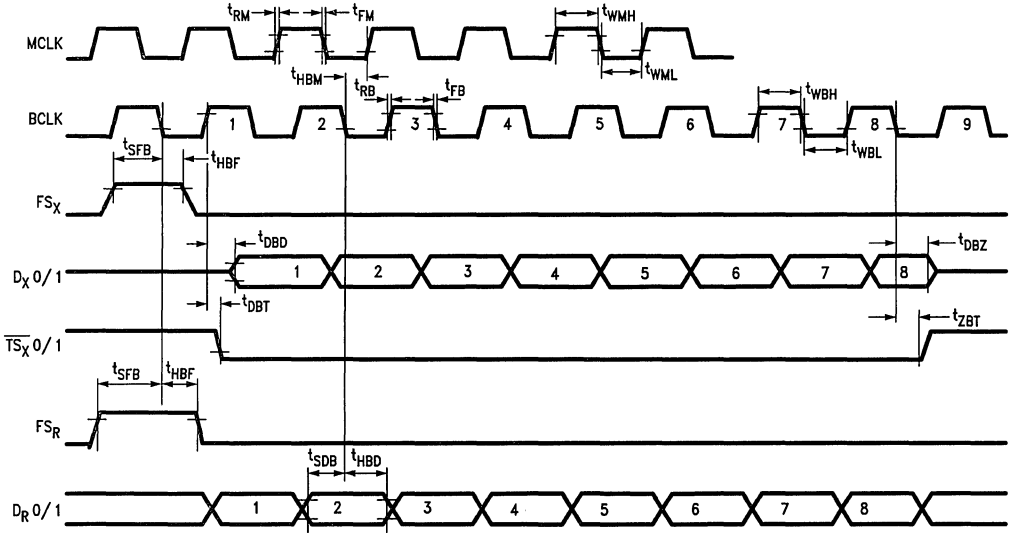
Symbol	Parameter	Conditions	Min	Typ	Max	Units
SERIAL CONTROL PORT TIMING						
f_{CCLK}	Frequency of CCLK				**2048**	kHz
t_{WCH}	Period of CCLK High	Measured from V_{IH} to V_{IH}	**160**			ns
t_{WCL}	Period of CCLK Low	Measured from V_{IL} to V_{IH}	**160**			ns
t_{RC}	Rise Time of CCLK	Measured from V_{IL} to V_{IH}			50	ns
t_{FC}	Fall Time of CCLK	Measured of V_{IH} to V_{IL}			50	ns
t_{HCS}	Hold Time, CCLK Low to $\overline{CS}$ Low	CCLK1	**10**			ns
t_{HSC}	Hold Time, CCLK Low to $\overline{CS}$ High	CCLK8	**100**			ns
t_{SSC}	Setup Time, $\overline{CS}$ Transition to CCLK Low		**60**			ns
t_{SSCO}	Setup Time, $\overline{CS}$ Transition to CCLK High	To Insure CO is Not Enabled for Single Byte	60			ns
t_{SDC}	Setup Time, CI Data In to CCLK Low		**50**			ns
t_{HCD}	Hold Time, CCLK Low to CO Invalid		50			ns
t_{DCD}	Delay Time, CCLK High to CO Data Out Valid	Load = 100 pF Plus 2 LSTTL Loads			**80**	ns
t_{DSD}	Delay Time, $\overline{CS}$ Low to CO Valid	Applies Only if Separate $\overline{CS}$ Used for Byte 2			**80**	ns
t_{DDZ}	Delay Time, $\overline{CS}$ or 9th CCLK High to CO High Impedance	Applies to Earlier of $\overline{CS}$ High or 9th CCLK High	15		80	ns
INTERFACE LATCH TIMING						
t_{SLC}	Setup Time, IL to CCLK 8 of Byte 1	Interface Latch Inputs Only	**100**			ns
t_{HCL}	Hold Tme, IL Valid from 8th CCLK Low (Byte 1)		50			ns
t_{DCL}	Delay Time CCLK8 of Byte 2 to IL	Interface Latch Outputs Only $C_L = 50$ pF			200	ns
MASTER RESET PIN						
t_{WMR}	Duration of Master Reset High	TP3075A Only	1			μs

Timing Diagrams



TL/H/9758–6

FIGURE 3. Non-Delayed Data Timing Mode



TL/H/9758–7

FIGURE 4. Delayed Data Timing Mode

Timing Diagrams (Continued)

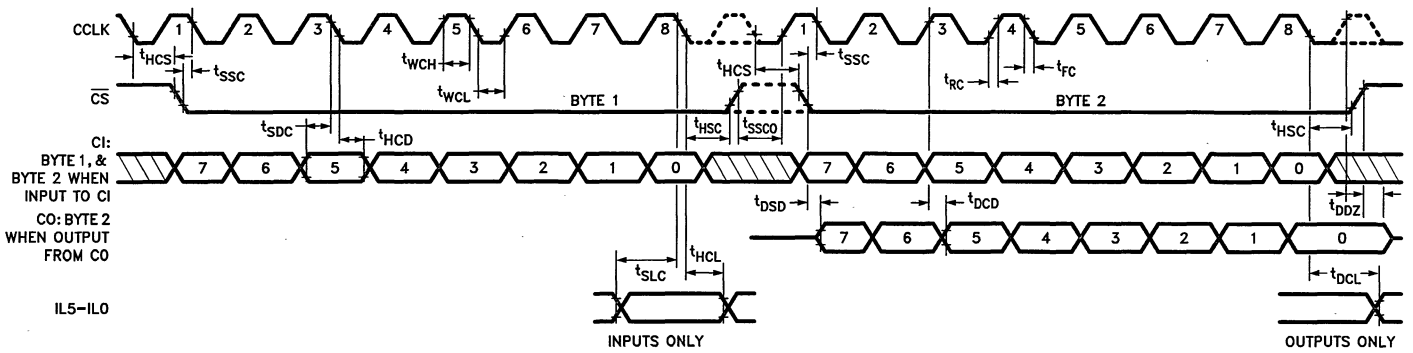


FIGURE 5. Control Port Timing

Transmission Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels. All other limits are assured by correlation with other production tests and/or product design and characterization (0 dB Gain). All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE						
	Absolute Levels	The Maximum 0 dBm0 Levels Are: VF_XI VF_RO (15 kΩ Load)		 1.375 1.964		 Vrms Vrms
		The Minimum 0 dBm0 Levels are: VF_XI VF_RO (Any Load ≥ 300Ω)		 73.8 105.0		 mVrms mVrms
G_{XA}	Transmit Gain Absolute Accuracy	Transmit Gain Programmed for Maximum 0 dBm0 Test Level. Measure Deviation of Digital Code from Ideal 0 dBm0 PCM Code at $D_X0/1$. T_A = 25°C	**−0.15**		**0.15**	dB
G_{XAG}	Transmit Gain Variation with Programmed Gain	Measure Transmit Gain Over the Range from Maximum to Minimum. Calculate the Deviation from the Programmed Gain Relative to G_{XA}, i.e., $G_{XAG} = G_{actual} - G_{prog} - G_{XA}$. T_A = 25°C, V_{CC} = 5V, V_{BB} = 5V	**−0.1**		**0.1**	dB
G_{XAF}	Transmit Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4) Minimum Gain < G_X < Maximum Gain f = 60 Hz f = 200 Hz f = 300 Hz to 3000 Hz f = 3400 Hz f = 400 Hz f ≥ 4600 Hz. Measure Response at Alias Frequency from 0 kHz to 4 kHz	 −1.8 −0.15 −0.7		 −26 −0.1 0.15 0.0 −14 −32	 dB dB dB dB dB dB
		G_X = 0.0 dB, VF_XI = 1.375 Vrms Relative to 1015.625 Hz f = 62.5 Hz f = 203.125 Hz f = 343.75 Hz f = 515.625 Hz f = 2140.625 Hz f = 3156.25 Hz f = 3406.250 Hz f = 3984.375 Hz Relative to 1062.5 Hz (Note 4) f = 5250 Hz, Measure 2750 Hz f = 11750 Hz, Measure 3750 Hz f = 49750 Hz, Measure 1750 Hz	 **−1.7** **−0.15** **−0.15** **−0.15** **−0.15** **−0.74** 		 **−24.9** **−0.1** **0.15** **0.15** **0.15** **0.15** **0.0** **−13.5** **−32** **−32** **−32**	 dB dB dB dB dB dB dB dB dB dB dB
G_{XAT}	Transmit Gain Variation with Temperature	Measured Relative to G_{XA}, V_{CC} = 5V, V_{BB} = −5V, Minimum gain < G_X < Maximum Gain	−0.1		0.1	dB
G_{XAL}	Transmit Gain Variation with Signal Level	Sinusoidal Test Method. Reference Level = 0 dBm0 VF_XI = −40 dBm0 to +3 dBm0 VF_XI = −50 dBm0 to −40 dBm0 VF_XI = −55 dBm0 to −50 dBm0	 **−0.2** **−0.4** **−1.2**		 **0.2** **0.4** **1.2**	 dB dB dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AMPLITUDE RESPONSE (Continued)						
G_{RA}	Receive Gain Absolute Accuracy	Receive Gain Programmed for Maximum 0 dBm0 Test Level. Apply 0 dBm0 PCM Code to D_R0 or D_R1. Measure VF_R0. T_A = 25°C	**−0.15**		**0.15**	dB
G_{RAG}	Receive Gain Variation with Programmed Gain	Measure Receive Gain Over the Range from Maximum to Minimum Setting. Calculate the Deviation from the Programmed Gain Relative to G_{RA}, i.e., $G_{RAG} = G_{actual} - G_{prog} - G_{RA}$. T_A = 25°C, V_{CC} = 5V, V_{BB} = −5V	**−0.1**		**0.1**	dB
G_{RAT}	Receive Gain Variation with Temperature	Measured Relative to G_{RA}. V_{CC} = 5V, V_{BB} = −5V. Minimum Gain < G_R < Maximum Gain	−0.1		0.1	dB
G_{RAF}	Receive Gain Variation with Frequency	Relative to 1015.625 Hz, (Note 4) D_R0 or D_R1 = 0 dBm0 Code. Minimum Gain < G_R < Maximum Gain				
		f = 200 Hz	−0.25		0.15	dB
		f = 300 Hz to 3000 Hz	−0.15		0.15	dB
		f = 3400 Hz	−0.7		0.0	dB
		f = 4000 Hz			−14	dB
		G_R = 0 dB, D_R0 or D_R1 = 0 dBm0 Code, G_X = 0 dB (Note 4)				
		f = 296.875 Hz	**−0.15**		**0.15**	dB
		f = 1875.00 Hz	**−0.15**		**0.15**	dB
		f = 2906.25 Hz	**−0.15**		**0.15**	dB
		f = 2984.375 Hz	**−0.15**		**0.15**	dB
		f = 3406.250 Hz	**−0.74**		**0.0**	dB
		f = 3984.375 Hz			**−13.5**	dB
G_{RAL}	Receive Gain Variation with Signal Level	Sinusoidal Test Method. Reference Level = 0 dBm0.				
		D_R0 = −40 dBm0 to +3 dBm0	**−0.2**		**0.2**	dB
		D_R0 = −50 dBm0 to −40 dBm0	**−0.4**		**0.4**	dB
		D_R0 = −55 dBm0 to −50 dBm0	**−1.2**		**1.2**	dB
		D_R0 or DR_1 = 3.1 dBm0 −0.5				
		R_L = 600Ω, G_R = −0.5 dB	−0.2		0.2	dB
		R_L = 300Ω, G_R = 1.2 dB	−0.2		0.2	dB
ENVELOPE DELAY DISTORTION WITH FREQUENCY						
D_{XA}	Tx Delay, Absolute	f = 1600 Hz			315	μs
D_{XR}	Tx Delay, Relative to DXA	f = 500 Hz–600 Hz			220	μs
		f = 600 Hz–800 Hz			145	μs
		f = 800 Hz–1000 Hz			75	μs
		f = 1000 Hz–1600 Hz			40	μs
		f = 1600 Hz–2600 Hz			75	μs
		f = 2600 Hz–2800 Hz			105	μs
		f = 2800 Hz–3000 Hz			155	μs
D_{RA}	Rx Delay, Absolute	f = 1600 Hz			200	μs
D_{RR}	Rx Delay, Relative to DRA	f = 500 Hz–1000 Hz	−40			μs
		f = 1000 Hz–1600 Hz	−30			μs
		f = 1600 Hz–2600 Hz			90	μs
		f = 2600 Hz–2800 Hz			125	μs
		f = 2800 Hz–3000 Hz			175	μs

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = +5V ±5%, V_{BB} = −5V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. f = 1015.625 Hz, VF_XI = 0 dBm0, D_R0 or D_R1 = 0 dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at V_{CC} = +5V, V_{BB} = −5V, T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
NOISE						
N_{XC}	Transmit Noise, C Message Weighted, μ-Law Selected	(Note 1) 11111111 in Gain Register		12	**15**	dBrnC0
N_{XP}	Transmit Noise, P Message Weighted, A-Law Selected	(Note 1) 11111111 in Gain Register		−74	**−67**	dBm0p
N_{RC}	Receive Noise, C Message Weighted, μ-Law Selected	PCM Code is Alternating Positive		8	**11**	dBrnC0
N_{RP}	Receive Noise, P Message Weighted, A-Law Selected	PCM Code Equals Positive Zero		−82	**−79**	dBm0p
N_{RS}	Noise, Single Frequency	f = 0 kHz to 100 kHz, Loop Around Measurement, VF_XI = 0 Vrms			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 100 mVrms f = 0 kHz–4 kHz (Note 2) f = 4 kHz–50 kHz	**36** 30			dBC dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	V_{BB} = −5.0 V_{DC} +100 mVrms f = 0 kHz–4 kHz (Note 2) f = 4 kHz–50 kHz	**36** 30			dBC dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC} = 5.0 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz–4000 Hz f = 4 kHz–25 kHz f = 25 kHz–50 kHz	 **36** 40 36			 dBC dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB} = −5.0 V_{DC} + 100 mVrms Measure VF_RO f = 0 Hz–4000 Hz f = 4 kHz–25 kHz f = 25 kHz–50 kHz	 **36** 40 36			 dBC dB dB
SOS	Spurous Out-of-Band Signals Applied at the Channel Output	0 dBm0 300 Hz to 3400 Hz Input PCM Code at D_R0 (or D_R1) 4600 Hz–7600 Hz 7600 Hz–8400 Hz 8400 Hz–50,000 Hz			 **−30** **−40** **−30**	 dB dB dB
DISTORTION						
STD_X STD_R	Signal to Total Distortion Transmit or Receive Half-Channel, μ-Law Selected	Sinusoidal Test Method Level = 3.0 dBm0 = 0 dBm0 to −30 dBm0 = −40 dBm0 = −45 dBm0	 **33** **36** **30** **25**			 dBC dBC dBC dBC
STD_{RL}	Single to Total Distortion Receive with Resistive Load	Sinusoidal Test Method Level = +3.1 dBm0 R_L = 600Ω, G_R = −0.5 dB R_L = 300Ω, G_R = −1.2 dB	 **33** **33**			 dBC dBC
SFD_X	Single Frequency Distortion, Transmit				**−46**	dB
SFD_R	Single Frequency Distortion, Receive				**−46**	dB
IMD	Intermodulation Distortion	Transmit or Receive Two Frequencies in the Range 300 Hz–3400 Hz			**−41**	dB

Transmission Characteristics (Continued)

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$; $T_A = 0°C$ to $+70°C$ by correlation with 100% electrical testing at $T_A = 25°C$. f = 1015.625 Hz, $VF_XI = 0$ dBm0, D_R0 or $D_R1 = 0$ dBm0 PCM code. Transmit and receive gains programmed for maximum 0 dBm0 test levels (0 dB Gain). All other limits are assured by correlation with other production tests and/or product design and characterization. All signals referenced to GND. Typicals specified at $V_{CC} = +5V$, $V_{BB} = -5V$, $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CROSSTALK						
CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f = 300 Hz–3400 Hz D_R = Idle Code		−90	**−75**	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f = 300 Hz–3400 Hz (Note 2)		−90	**−70**	dB

Note 1: Measured by grounded input at V_{FXI}.

Note 2: $PPSR_X$, $NPSR_X$, and CT_{R-X} are measured with a −50 dBm0 activation signal applied to VF_XI.

Note 3: A signal is Valid if it is above V_{IH} or below V_{IL} and Invalid if it is between V_{IL} and V_{IH}. For the purposes of this specification the following conditions apply:

a) All input signals are defined as: $V_{IL} = 0.4V$, $V_{IH} = 2.7V$, $t_R < 10$ ns, $t_F < 10$ ns.

b) t_R is measured from V_{IL} to V_{IH}. t_F is measured from V_{IH} to V_{IL}.

c) Delay Times are measured from the input signal Valid to the output signal Valid.

d) Setup Times are measured from the data input Valid to the clock input Invalid.

e) Hold Times are measured from the clock signal Valid to the data input Invalid.

f) Pulse widths are measured from V_{IL} to V_{IL} or from V_{IH} to V_{IH}.

Note 4: A multi-tone test technique is used.

National Semiconductor

TP3155 Time Slot Assignment Circuit

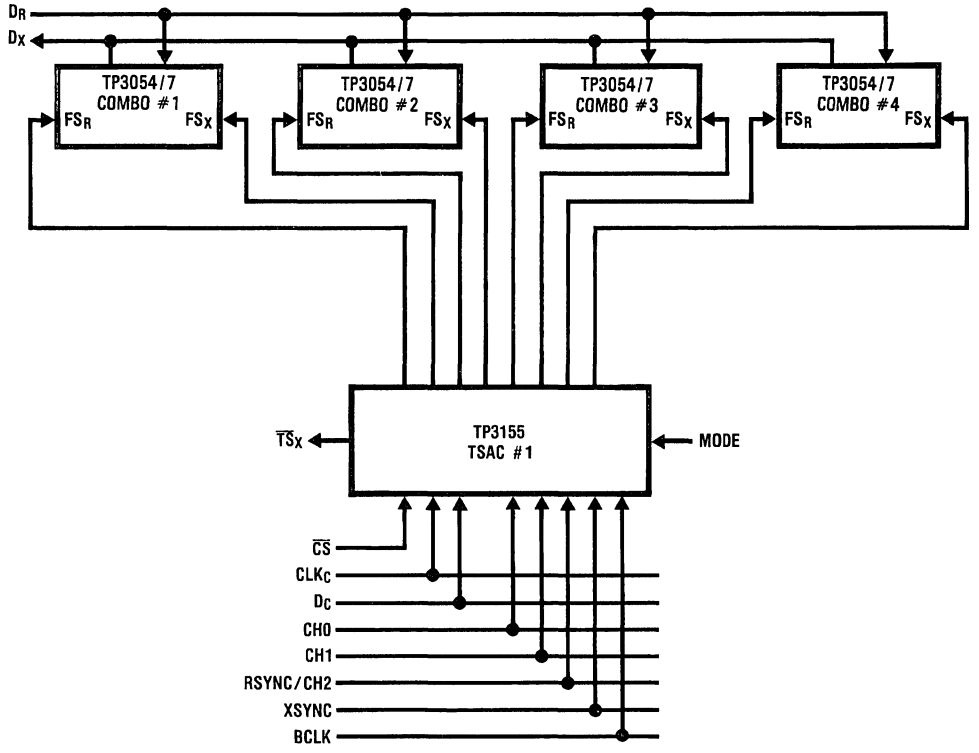
General Description

The TP3155 is a monolithic CMOS logic circuit designed to generate transmit and receive frame synchronization pulses for up to 8 COMBO™ CODEC/Filters. Each frame sync pulse may be independently assigned to a time slot in a frame of up to 32 time slots. Assignments are controlled by loading in an 8-bit word via a simple serial interface port. This control interface is compatible with that used on the TP3020/TP3021 and 2910/2911 CODECs, enabling an easy upgrade to COMBO CODEC/Filters to be made.

Features

- Controls up to 8 COMBO CODEC/Filters
- Independent transmit and receive time slot assignments
- 8-channel unidirectional mode
- Up to 32 time slots per frame
- Serial control interface compatible with TP3020/TP3021 CODECs
- LS TTL and CMOS compatible inputs
- 5 mW, 5V operation

Typical Application



TL/H/5118–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} Relative to GND	7V
Voltage at Any Input or Output	V_{CC} + 0.3V to GND −0.3V
Operating Temperature Range (Ambient)	−25°C to +125°C
Storage Temperature Range (Ambient)	−65°C to +150°C
Maximum Lead Temperature (Soldering, 10 seconds)	300°C

ESD rating to be determined.

DC Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%; T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at V_{CC} = 5.0V, T_A = 25°C.

Parameter	Conditions	Min	Typ	Max	Units
Input Voltage Levels					
V_{IH}, Logic High		**2.0**			V
V_{IL}, Logic Low				**0.7**	V
Input Currents					
All Inputs Except MODE	$V_{IL} < V_{IN} < V_{IH}$	**−1**		**1**	μA
MODE	V_{IN} = 0V	**−100**			μA
Output Voltage Levels					
V_{OH}, Logic High	FS_X and FS_R Outputs, I_{OH} = 3 mA	2.4			V
V_{OL}, Logic Low	FS_X and FS_R Outputs, I_{OL} = 5 mA			0.4	V
	TS_X Output, I_{OL} = 5 mA			**0.4**	V
Power Dissipation Operating Current	BCLK = 2.048 MHz, All Outputs Open-Circuit		1	**1.5**	mA

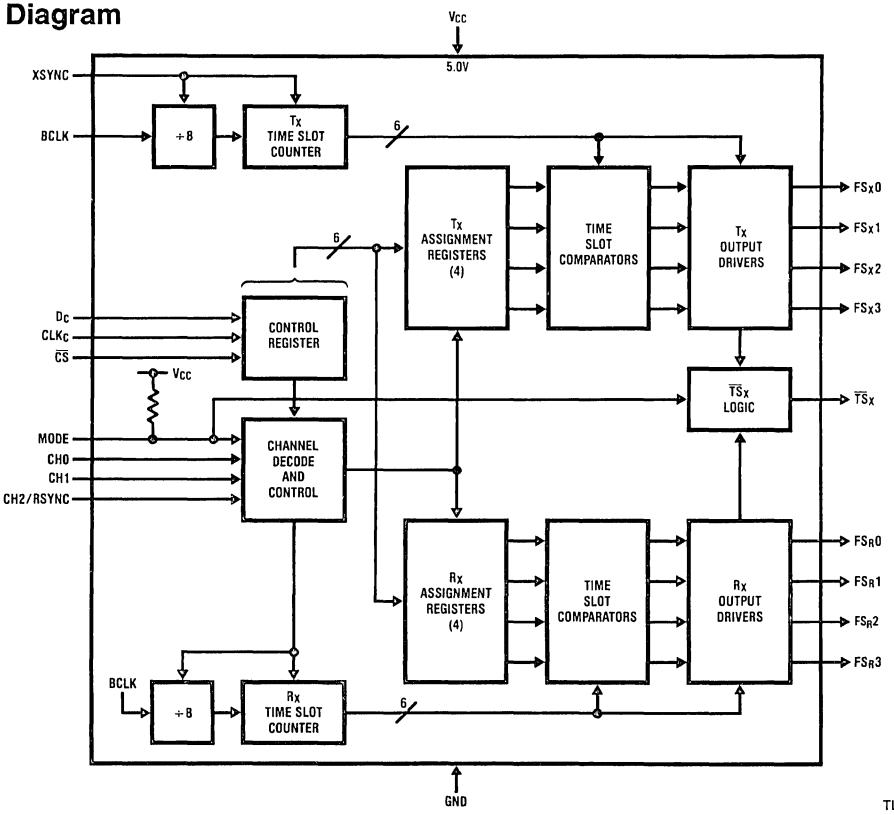
Timing Specifications

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{CC} = 5.0V ±5%, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typicals specified at V_{CC} = 5.0V, T_A = 25°C. All timing parameters are measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

See Definitions and Timing Conventions section for test methods information.

Symbol	Parameter	Conditions	Min	Max	Units
t_{PC}	Period of Clock	BCLK, CLK_C	**480**		ns
t_{WCH}	Width of Clock High	BCLK, CLK_C	**160**		ns
t_{WCL}	Width of Clock Low	BCLK, CLK_C	**160**		ns
t_{SDC}	Set-Up Time from D_C to CLK_C		**50**		ns
t_{HCD}	Hold Time from CLK_C to D_C		**50**		ns
t_{SCC}	Set-Up Time from $\overline{CS}$ to CLK_C		**30**		ns
t_{HCC}	Hold Time from CLK_C to $\overline{CS}$		**100**		ns
t_{SCHC}	Set-Up Time from Channel Select to CLK_C		**50**		ns
t_{HCHC}	Hold Time from Channel Select to CLK_C		**50**		ns
t_{DBF}	Delay Time from BCLK Low to $FS_{X/R}$ 0–3 High or Low	C_L = 50 pF		**100**	ns
t_{HSYNC}	Hold Time from BCLK to Frame Sync		**50**		ns
t_{SSYNC}	Set-Up Time from Frame Sync to BCLK		**100**		ns
t_{DTL}	Delay to $\overline{TS_X}$ Low	C_L = 50 pF		**140**	ns
t_{DTH}	Delay to $\overline{TS_X}$ High	R_L = 1k to V_{CC}	**30**	**140**	ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	BCLK, CLK_C		50	ns

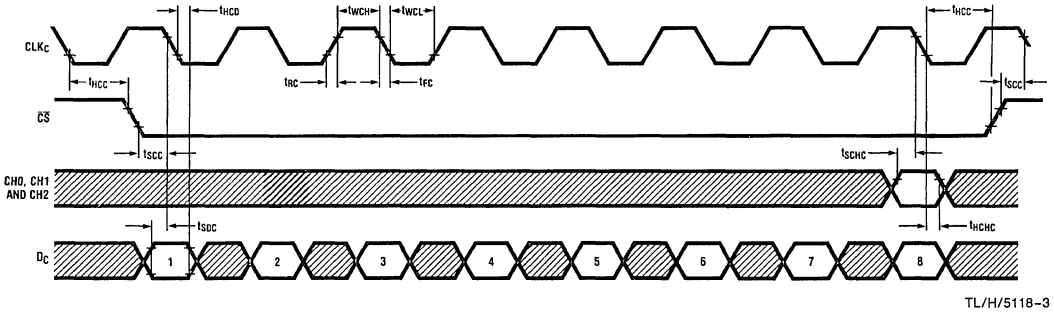
Block Diagram



TL/H/5118–2

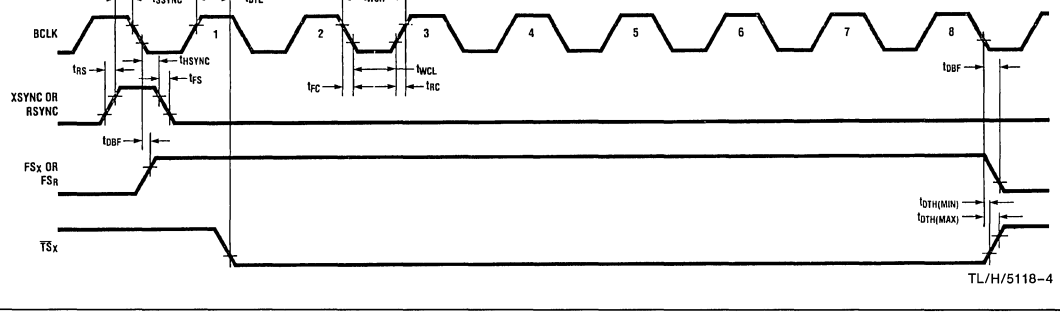
Timing Diagrams

Control Interface



TL/H/5118–3

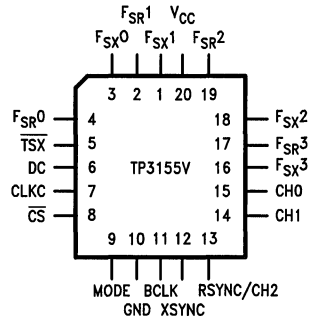
Output



TL/H/5118–4

Connection Diagrams

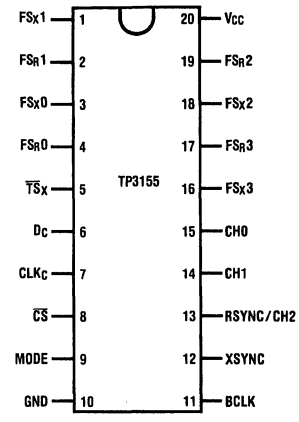
Plastic Chip Carrier (PCC) Package



TL/H/5118–5

Order Number TP3155V
See NS Package Number V20A

Dual-In-Line Package



TL/H/5118–6

Top View

Order Number TP3155J or TP3155N
See NS Package Numbers J20A, N20A

Pin Descriptions

Symbol	Description
FS_X1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid transmit time slot assignment is made.
FS_R1	A conventional CMOS frame sync output which is normally low, and goes active-high for 8 cycles of BCLK when a valid receive time slot assignment is made.
FS_X0	A transmit frame sync output similar to pin 1.
FS_R0	A receive frame sync output similar to pin 2.
$\overline{TS}_X$	An open-drain N-channel output which is normally high impedance but pulls low during any active transmit time slot.
D_C	The input for an 8-bit serial control word. $\overline{X}$ is the first bit clocked in.
CLK_C	The clock input for the control interface.
$\overline{CS}$	The active-low chip select for the control interface.
MODE	The mode select input. When left open-circuit or connected to V_{CC}, mode 1 is selected, and when connected to GND, mode 2 is selected.
GND	The 0V ground connection to the device.

Symbol	Description
BCLK	The bit clock input, which should run at the same rate as that for the COMBO CODEC/ Filter COMBO.
XSYNC	The transmit TS0 sync pulse input. Must be synchronous with BCLK.
RSYNC/CH2	The function of this input is determined by the MODE input (pin 9). In mode 1 this is the receive TS0 sync pulse, RSYNC, which must be synchronous with BCLK. In mode 2 this is the CH2 input for the MSB of the channel select word.
CH1	The input for the next significant bit of the channel select word.
CH0	The input for the LSB of the channel select word, which defines the frame sync output affected by the following control word.
FS_X3	A transmit frame sync output similar to pin 1.
FS_R3	A receive frame sync output similar to pin 2.
FS_X2	A transmit frame sync output similar to pin 1.
FS_R2	A receive frame sync output similar to pin 2.
V_{CC}	The positive supply to the device. 5V ±5%.

Functional Description

OPERATING MODES

The TP3155 control interface requires an 8-bit serial control word which is compatible with the TP3020/TP3021 and 2910/2911 CODECs. Two bits, $\overline{X}$ and $\overline{R}$, define which of the two groups of frame sync outputs, FS_X0 to FS_X3 or FS_R0 to FS_R3, is affected by the control word, and a 6-bit assignment field specifies the selected time slot, from 0 to 31. A frame sync output is active-high for one time slot, which is always 8 cycles of BCLK. A frame may consist of any number of time slots up to 32. If a timeslot is assigned which is beyond the number of time slots in a frame, the FS_X or FS_R output to which it was assigned will remain inactive.

Two modes of operation are available. Mode 1 is for systems requiring different time slot assignments for the transmit and receive direction of each channel. Mode 1 is selected by leaving pin 9 (MODE) open-circuit or connecting it to V_{CC}. In this case, Pin 13 is the RSYNC input which defines the start of each receive frame, and the four outputs, FS_R0–FS_R3, are assigned with respect to RSYNC. The XSYNC input defines the start of each transmit frame and outputs FS_X0–FS_X3 are assigned with respect to XSYNC. XSYNC may have any phase relationship with RSYNC. Inputs CH0 and CH1 select the channel, from 0 to 3 (see Table Ia).

Mode 2 provides the option of assigning all 8 frame sync outputs with respect to the XSYNC input. Mode 2 is selected by connecting pin 9 (MODE) to GND. This makes the TP3155 TSAC useful for either an 8-channel undirectional controller or for systems in which the transmit and receive directions of each channel are always assigned to the same time slot as the other, i.e., the FS_X and FS_R inputs on the COMBO CODEC/Filter are hard-wired together. In this case, logical selection of the channel to be assigned is made via inputs CH0, CH1 and CH2 (see Table Ib).

POWER-UP INITIALIZATION

During power-up, all frame sync outputs, FS_X0–FS_X3 and FS_R0–FS_R3, are inhibited and held low. No outputs will go active until a valid time slot assignment is made.

LOADING CONTROL DATA

During the loading of control data, the binary code for the selected channel must be set on inputs CH0 and CH1 (and CH2 in mode 2), see Tables Ia and Ib.

Control data is clocked into the D_C input on the falling edges of CLK_C while $\overline{CS}$ is low.

A new time slot assignment is transferred to the selected assignment register on the high going transition of $\overline{CS}$. The new assignment is re-synchronized to the system clock such that the new FS output pulses will start at the next complete valid time slot after the rising edge of $\overline{CS}$.

TIME SLOT COUNTER OPERATION

At the start of TS0 of each transmit frame, defined by the first falling edge of BCLK after XSYNC goes high, the transmit time slot counter is reset to 000000 and begins to increment once every 8 cycles of BCLK. Each count is compared with the 4 transmit assignment registers and, on finding a match, a frame sync pulse is generated at that FS_X output.

Similarly, the first falling edge of BCLK after RSYNC goes high defines the start of receive TS0, and outputs FS_R0–FS_R3 are generated with respect to TS0 when the receive time slot counter matches the appropriate receive assignment register.

$\overline{TS_X}$ OUTPUT

In mode 1 (separate transmit and receive assignments), this output pulls low whenever any FS_X output pulse is being generated. In mode 2, this output pulls low whenever any FS_X or FS_R output is being generated. At all other times it is open-circuit, allowing the $\overline{TS_X}$ outputs of a number of TSACS to be wire-ANDed together with a common pull-up resistor. This signal can be used to control the TRI-STATE® enable input of a line driver to buffer the transmit PCM bus from the CODEC/Filters to the backplane.

TABLE Ia. Control Mode 1 (TP3020/TP3021 Compatible)

$\overline{X}$	$\overline{R}$	T5	T4	T3	T2	T1	T0

$\overline{X}$ *is the first bit clocked into the* D_C *input.*

Control Data Format

T5	T4	T3	T2	T1	T0	Time Slot
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
						:
0	1	1	1	1	0	30
0	1	1	1	1	1	31
1	X	X	X	X	X	(Note 1)

CH1	CH0	Channel Selected
0	0	Assign to FS_X0 and/or FS_R0
0	1	Assign to FS_X1 and/or FS_R1
1	0	Assign to FS_X2 and/or FS_R2
1	1	Assign to FS_X3 and/or FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to both selected FS_X and FS_R
0	1	Assign time slot to selected FS_X only
1	0	Assign time slot to selected FS_R only
1	1	Disable both selected FS_X and FS_R

TABLE Ib. Control Mode 2

CH2	CH1	CH0	Channel Selected
0	0	0	Assign to FS_X0
0	0	1	Assign to FS_X1
0	1	0	Assign to FS_X2
0	1	1	Assign to FS_X3
1	0	0	Assign to FS_R0
1	0	1	Assign to FS_R1
1	1	0	Assign to FS_R2
1	1	1	Assign to FS_R3

$\overline{X}$	$\overline{R}$	Action
0	0	Assign time slot to selected output
0	1	
1	0	
1	1	Disable selected output

Note 1: When T5 = 1, then the appropriate FS_X or FS_R output is inactive.

Definitions and Timing Conventions

DEFINITIONS

V_{IH}	V_{IH} is the d.c. input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum setup and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device.
V_{IL}	V_{IL} is the d.c. input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device.
V_{OH}	V_{OH} is the minimum d.c. output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current.
V_{OL}	V_{OL} is the maximum d.c. output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current.
Threshold Region	The threshold region is the range of input voltages between V_{IL} and V_{IH}.
Valid Signal	A signal is Valid if it is in one of the valid logic states, (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.
Invalid Signal	A signal is Invalid if it is not in a valid logic state, i.e. when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purposes of this timing specification the following conventions apply:

Input Signals	All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ns.
Period	The period of clock signal is designated as t_{Pxx} where xx represents the mnemonic of the clock signal being specified.
Rise Time	Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}.
Fall Time	Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}.
Pulse Width High	The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}.
Pulse Width Low	The low pulse width is designated as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}.
Setup Time	Setup times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose setup time is being specified relative to a clock or strobe input represented by mnemonic xx. Setup times are measured from the ww Valid to xx Invalid.
Hold Time	Hold times are designated as t_{Hxxww}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by mnemonic xx. Hold times are measured from xx Valid to ww Invalid.
Delay Time	Delay times are designated as $t_{Dxxyy[\ \|H\|L]}$, where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of this data sheet.

Applications Information

A combination of the TP3155 TSAC and any CODEC/Filter COMBO from the TP3052/3/4/7 or TP3064/7 series will result in data timing as shown in *Figure 1*. Although the FS_X output pulse goes high before BCLK goes high, the D_X output of the combo remains in the TRI-STATE mode until both are high. The eight bit period is shortened to prevent a bus clash, just as it is on the TP3020/1 CODECs.

Alternatively, eight full-length bits can be obtained by inverting the BCLK to the combo devices, thereby aligning rising edges of BCLK and $FS_{X/R}$.

Figure 2 shows typical timing for the control data interface.

Figure 3 shows the digital interconnections of a typical line card application.

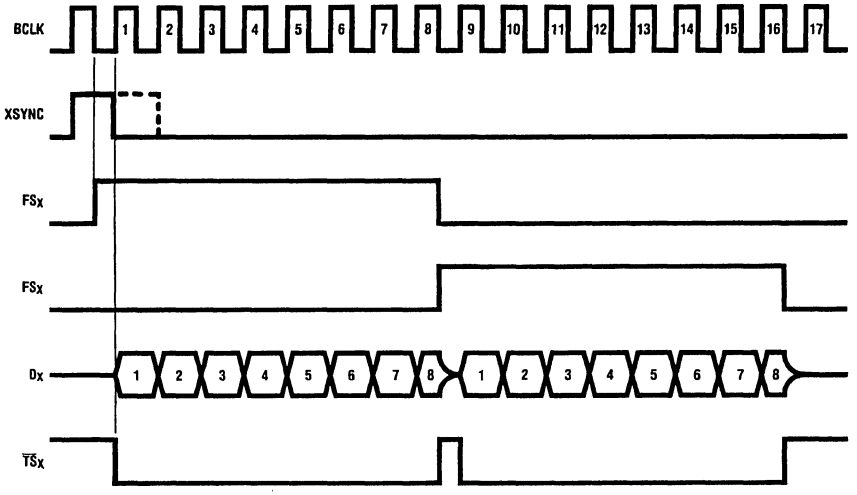


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FIGURE 1. Transmit Data Timing

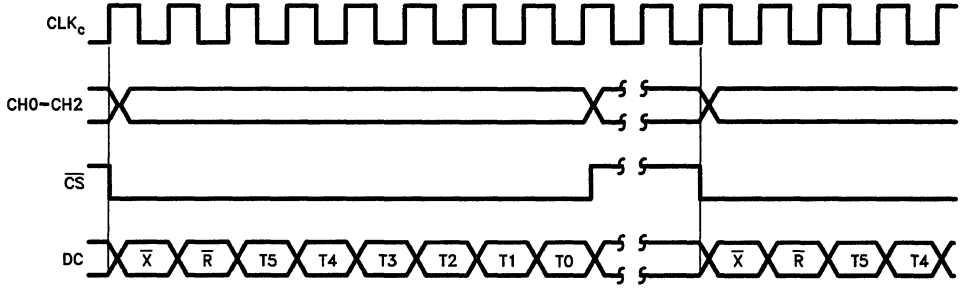

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FIGURE 2. Control Data Timing

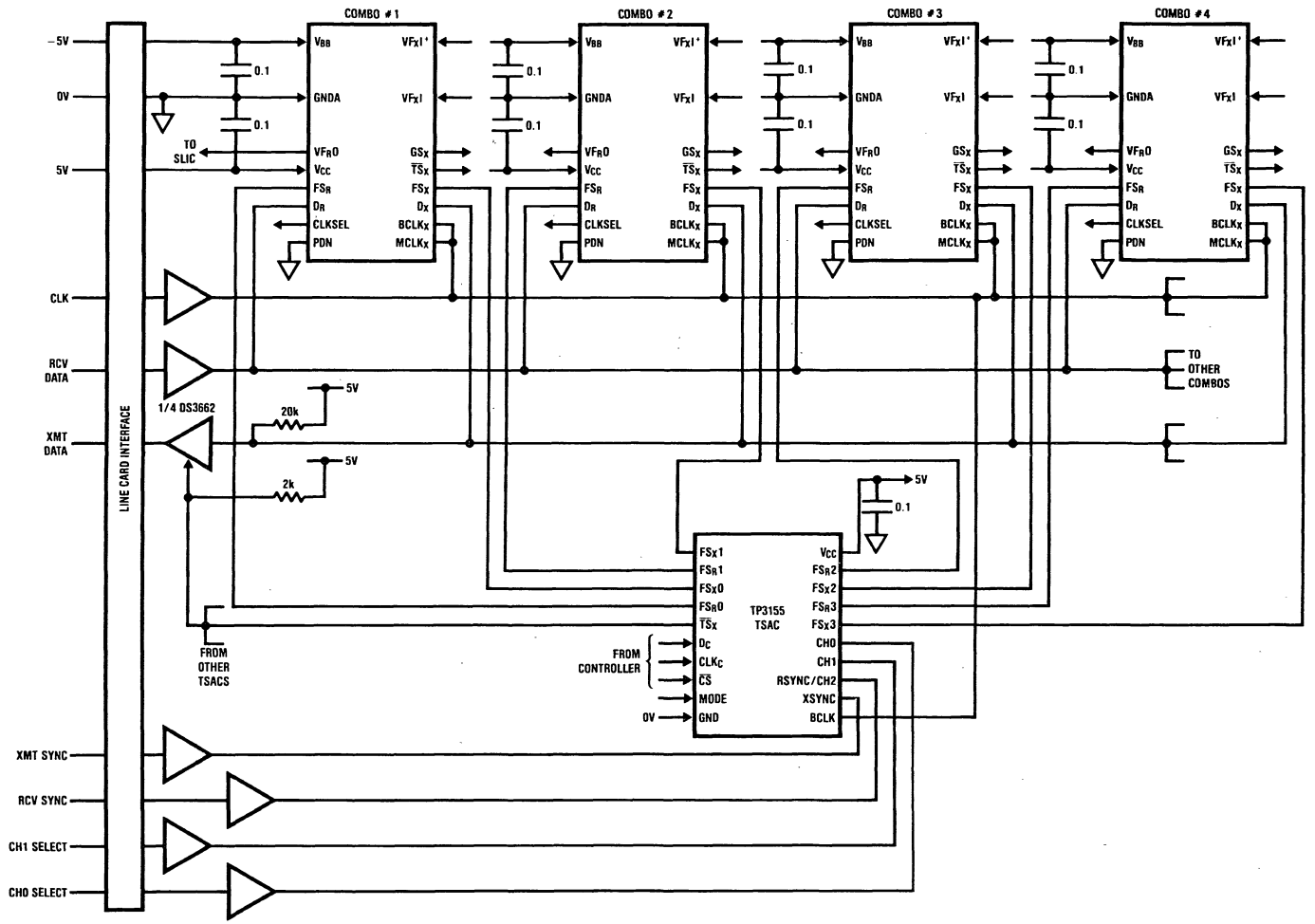

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FIGURE 3. Digital Interconnections on a Typical Synchronous Line Card

National Semiconductor

TP3200, TP3204 SLIC–MC Magnetic Compensation SLICs

General Description

The TP3200 and TP3204 are monolithic Bipolar integrated circuits intended for use on subscriber and trunk interface cards of digital PABX and central office equipment. Each device contains a magnetic compensation circuit, a supervision circuit and three relay drivers with latched inputs.

The magnetic compensation circuit allows the use of a small, low cost line transformer by measuring the loop current, and producing an output current proportional to the d.c. value of the loop current. This output current is passed through a winding of the line transformer in such a way as to cancel the d.c. component of the magnetic flux. Thus the transformer may be wound on a small ferrite core without an air gap.

The supervision output is used to detect off-hook, replicate dial pulses and terminate ringing on detection of ring-trip.

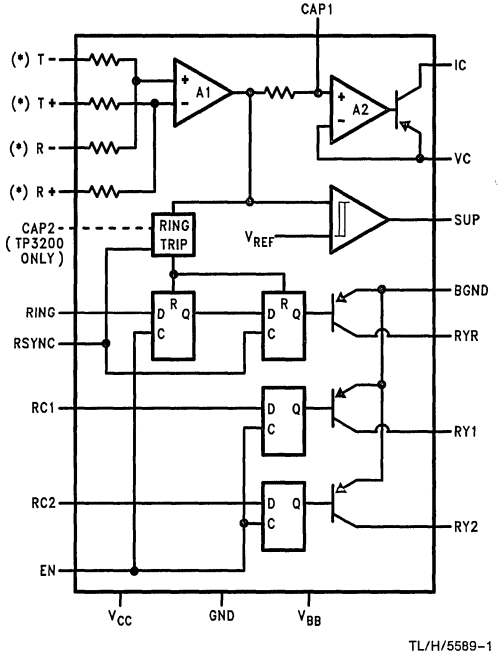
One of the three relay drivers is dedicated to the ring function, the other two are general purpose. TP3200 has PNP relay drivers, while the TP3204 has NPN relay drivers.

Features

- Magnetic Compensation Circuit allows the use of low cost ferrite core transformers
- Supervision Circuitry provides hook-switch detect, ring-trip detect and dial pulse replication
- Ring relay driver synchronized to zero-crossings
- Automatic ring-trip circuit—TP3200, TP3204
- Three Latched relay drivers
- −48 Volt relay drivers—TP3200
- +5 Volt relay drivers—TP3204
- Requires only ±5V supplies
- Thermal shutdown protection
- Power-Up reset on relay driver latches

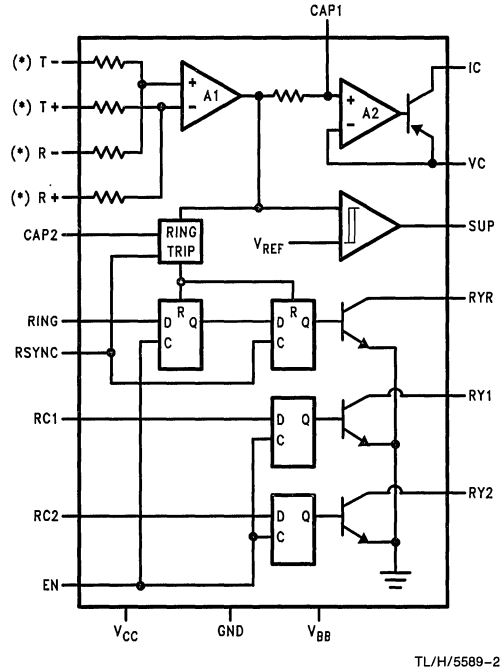
Simplified Block Diagrams

TP3200



TL/H/5589–1

TP3204



TL/H/5589–2

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Operating Temperature	−25°C to +85°C
Storage Temperature	−65°C to +150°C
V_{CC} w.r.t. GND	7V
V_{BB} w.r.t. GND	−7V
V_{CC} w.r.t. V_{BB}	14V
V_{IC} w.r.t. GND	−70V
V_{RY} w.r.t. GND (TP3200)	−70V
V_{RY} w.r.t. GND (TP3204)	20V
Voltage at Sensing Inputs T+, T−, R+, R−, w.r.t. GND	300 V_{peak} (continuous)
T+, T−, R+, R− (FCC 68,302/d)	1000V (surge)
I_{RY} (TP3200)	−50 mA
I_{RY} (TP3204)	120 mA
Power Dissipation (Note 1)	1.5W
ESD (Note 2)	2 kV

Electrical Characteristics

Unless otherwise specified, Limits printed in bold characters are guaranteed for V_{CC} = +5.0V, V_{BB} = −5.0V ±5% and T_A = 0°C to 70°C by correlation with 100% production testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at V_{CC} = +5.0V, V_{BB} = −5.0V, and T_A = 25°C.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
COMPENSATION CIRCUIT						
R_{IN}	Input Resistance	T+, T−, R+, R−		200		KΩ
V_{OS}	Offset Voltage at V_C	I_{LOOP} = 0 mA, R_S = 100Ω V_{BAT} = −48V, VC Open.	**−30**		**+30**	mV
A_V	Differential Voltage Gain	R_L = 150Ω, R_S = 100, Measure from T+, T−, R+ and R− to VC, I_{LOOP} = 10–100 mA	**0.147**		**0.153**	V/V
I_C	Maximum Compensation Current	The Output Current is Nominally Given by V_C/R_L, Where R_L is Connected from VC to GND.			25	mA
R_O	Output Resistance	Measure at CAP1	**80**	100	**120**	KΩ
VIC_{Sat}	Saturation Voltage at IC	I_C = 20 mA. Measure from VC to IC.		−0.3	**−1.5**	V
R_{IC}	IC Output Impedance	R_L = 150Ω, f = 1 kHz, I_C = 10 mA I_C = 20 mA		2 300		MΩ KΩ
N	Idle Noise	IC = 20 mA, R_L = 150Ω Connect 1500Ω from IC to V_{BAT}, Measure at IC.		0	**10**	dBrnC
SUPERVISION CIRCUITRY						
I_O	Ring-Trip Current Source	At CAP2		10		μA
I_R	Ring-Trip Threshhold	CAP2 = 0.1 μF, f = 20 Hz, R_S = 100Ω		12		mA
I+	Off-hook Positive Threshold	R_S = 100. Increase Loop Current until SUP Switches low.	**11**	13	**15**	mA
H	Off-hook Hysteresis	R_S = 100. Decrease Loop Current from I+ until SUP Switches High.		2		mA
RELAY DRIVERS						
VRY_{sat}	Relay Driver Saturation Voltage	TP3200, IRY = 30 mA TP3204, IRY = 80 mA			**−2.2** **1**	V V
DIGITAL INTERFACE (SUP, EN, RC1, RC2, RING, RSYNC)						
V_{OL}	Output Low Level	I_{OL} = 1.6 mA			**0.4**	V
V_{OH}	Output High Level	I_{OH} = 0.1 mA	**4**			V
V_{IL}	Input Low Level				**0.7**	V
V_{IH}	Input High Level		**2**			V
I_I	Input Current	0.7 < V_{IN} < 2.0	−0.1		0.1	mA
POWER DISSIPATION						
$I_{CC}0$	V_{CC} Supply I_{DLE} Current	R_L = 150Ω, R_S = 100Ω I_{LOOP} = 0 mA, All Relays Off		3	**4.5**	mA
$I_{BB}0$	V_{BB} Supply I_{DLE} Current	R_L = 150Ω, R_S = 100Ω, I_{LOOP} = 0 mA All Relays Off.		2.5	**4**	mA
$I_{CC}1$	V_{CC} Supply Active Current	R_L = 150Ω, R_S = 100Ω I_{LOOP} = 40 mA, I_{RY} = 10 mA		3	**4.7**	mA
$I_{BB}1$	V_{BB} Supply Active Current	R_L = 150Ω, R_S = 100Ω I_{LOOP} = 40 mA, I_{RY} = 10 mA		2.5	**4.2**	mA
PSRR+	Power Supply Rejection Ratio	$\Delta V_C/\Delta V_{CC}$, f = 1 kHz, CAP1 = 1 μF	**−60**	−80		dB
PSRR−		$\Delta V_C/\Delta V_{BB}$, f = 1 kHz, CAP1 = 1 μF	**−38**	−50		dB

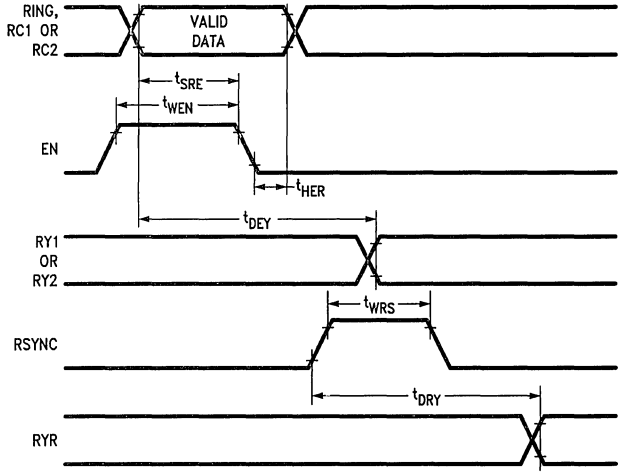
Electrical Characteristics Unless otherwise specified, Limits printed in bold characters are guaranteed for $V_{CC} = +5.0V$, $V_{BB} = -5.0V \pm 5\%$ and $T_A = 0°C$ to $70°C$ by correlation with 100% production testing at $T_A = 25°C$. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical values are measured at $V_{CC} = +5.0V$, $V_{BB} = -5.0V$, and $T_A = 25°C$.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TIMING (SEE DEFINITIONS AND TIMING CONVENTIONS FOR TEST METHOD INFORMATION)						
t_{SRE}	Set-up Time	Measure from RING, or RC1, RC2 Valid to EN Falling Edge.	**1**			μs
t_{HER}	Hold Time	Measure from EN Falling Edge to RING, RC1, or RC2 Invalid.	**1**			μs
t_{WEN} t_{WRS}	Input Pulse Width EN RSYNC	Active High	**2** **3**			μs μs
t_{DEY}	RY1, RY2 Drivers Delay Time	Measure from En Active and RC1, RC2, Valid to RY1, RY2 On or Off. $I_{RY\ (on)} = 10$ mA, $I_{RY\ (off)} = 0.1$ mA			20	μs
t_{DRY}	RYR Driver Delay Time	Measure from RSYNC Rising Edge to RYR On or Off. $I_{RYR\ (on)} = 10$ mA, $I_{RYR\ (off)} = 0.1$ mA			20	μs
t_{HS}	Off-Hook Detection Time	Measure from $I_{LOOP} = 20$ mA to SUP Transition from High to Low.		2.5		μs
t_R	Ring-Trip Detection Time	Measure from $I_{LOOP} = 20$ mA to, RYR Off, CAP2 = 0.1 μF, f = 20 Hz, $I_{RYR\ (on)} = 10$ mA, $I_{RYR\ (off)} = 0.1$ mA			150	ms

Note 1: Derate based on 150°C maximum junction temperature and thermal resistance of 80°C/W, junction to ambient.

Note 2: Device pins T+, T−, R+, R− are not guaranteed to meet the NSC standard requirement for ESD protection of 2000V. The functional requirements in the intended application prohibit the use of any additional components on chip for ESD protection. Maximum surge voltage for these pins is greater than 1000V, measured in accordance with FCC 68, 302/d.

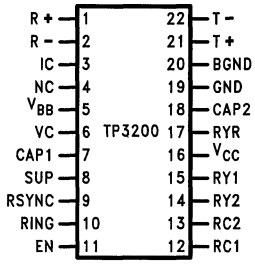
Timing Diagram



TL/H/5589–17

Connection Diagrams

Dual-In-Line



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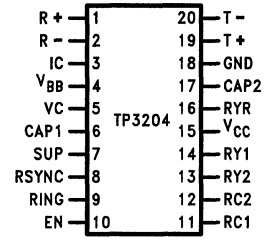
Top View

Order Number TP3200N
See NS Package Number N22A

Dual-In-Line



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Top View

Order Number TP3204N
See NS Package Number N20A

Description of Pin Functions

Name	Function
T+	Tip positive voltage sense input connected to the positive (GND) side of the Tip current sense resistor.
T−	Tip negative voltage sense input connected to the negative (line) side of the Tip current sense resistor.
BGND	Battery ground return for the relay drivers. This ground should be connected in such a way as to minimize noise due to relay switching and also to avoid large voltage transients in the presence of lightning. Preferably it should be connected to GND on the backplane.
R−	Ring negative voltage sense input connected to the negative (V_{BAT}) side of the Ring current sense resistor.
R+	Ring positive voltage sense input connected to the positive (line) side of the Ring current sense resistor.
V_{BB}	−5 volts ±5%
IC	Compensation current output. The current sourced by this output is proportional to the d.c. loop current flowing through the line transformer. By passing this current through an auxiliary winding of appropriate winding ratio, the average magnetic flux in the transformer core can be cancelled.
CAP1	External capacitor input required to filter voice frequency components from the loop current.
CAP2	External capacitor input required to perform charging and discharging by I_O for one cycle of ring frequency in order to perform the ring-trip function.
VC	Compensation voltage output. The output voltage at this pin is proportional to the d.c. loop current flowing through the line transformer. An external resistor R_L connected from VC to GND causes a current to flow from IC which is in turn proportional to the d.c. loop current.
GND	Analog ground.
V_{CC}	+5 volts ±5%
SUP	Supervision output indicating off-hook, Dial Pulse and Ring Trip status.
EN	Enable input. The RING, RC1 and RC2 inputs are gated in during the high state of EN and latched on the falling edge.
RC1	General purpose relay control input 1, used to turn on or off relay driver 1 (RY1) when enabled by EN.
RC2	General purpose relay control input 2 used to turn on or off relay driver 2 (RY2) when enabled by EN.
RING	Ring command input used to turn on or off the ring relay driver when enabled by EN.

Description of Pin Functions (Continued)

Name	Function
RSYNC	Ring Synchronization input used to synchronize the opening and closing of the ring relay with zero crossings of the ring signal, i.e., the minimum voltage across the relay contacts. RSYNC should nominally be a square wave generated by a zero crossing detector from the ringing signal, and should have the same frequency as the ringing signal.
RYR	Ring relay driver output.
RY1	General purpose relay driver output 1.
RY2	General purpose relay driver output 2.

Functional Description

MAGNETIC COMPENSATION CIRCUIT *(Figure 1)*

The magnetic compensation circuit measures the loop current by sensing the voltage across two matched battery feed resistors, R_S, using a high impedance thin film resistor bridge, and produces a voltage proportional to the instantaneous loop current at the output of the OpAmp, A1. This voltage is filtered by the external capacitor CAP1. The output voltage follower A2 and output transistor Q1 then reproduce this voltage at the VC output. Capacitor CAP1 is selected such that the voice frequency components of the loop current are attenuated enough to prevent the compensation current from affecting the subscriber circuit output impedance. A resistor R_L connected from VC to GND causes a current V_C/R_L to flow from the IC output. This output is connected to an auxiliary winding on the line transformer. By proper selection of resistor ratios and transformer winding ratios, the current I_C can exactly cancel the flux produced by the d.c. component of the loop current. The equation relating these parameters is:

$$NP/NC = A_V R_S/R_L$$

SUPERVISION CIRCUIT *(Figure 2)*

The supervision circuit consists of a loop current comparator with built-in hysteresis. The input of the supervision circuit is taken from the output of the Op Amp A1. The voltage at this point represents the instantaneous loop current. The output is the SUP output. During on-hook operation SUP is high. When the loop current increases beyond approximately 13 mA the SUP output goes low, indicating off-hook. When the loop current falls below approximately 11 mA SUP will go high indicating on-hook. In the presence of dial pulses, SUP will produce a square-wave replication of the dial pulses. During ringing, the comparator will detect the instantaneous ringing current through the loop, causing SUP to produce a square-wave with a mark-to-space ratio larger than 50% during the on-hook condition. When the telephone goes off-hook, the resultant dc loop current causes the mark-to-space ratio to decrease until the threshhold is reached when the duty cycle of SUP output is exactly 50%. This change in duty cycle can easily be detected digitally and the ringing terminated. This is the most flexible form of ring trip since it is frequency independent and is compatible with multi-frequency ringing. A second method of ring trip is described in the next section.

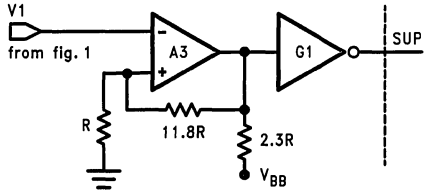

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FIGURE 2. Supervision Circuit

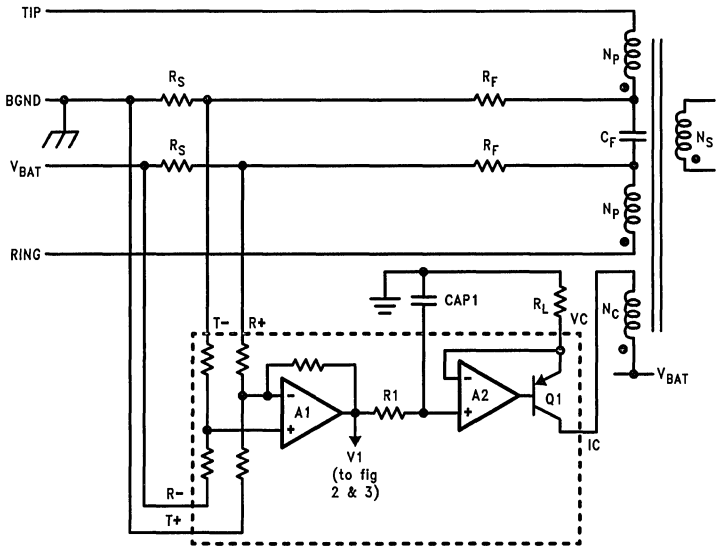

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FIGURE 1. Magnetic Compensation Circuit—Simplified Diagram

Functional Description (Continued)

RING TRIP CIRCUIT *(Figure 3)*

The ring trip circuit takes its input from the output of A1, which represents the combination of instantaneous ringing current and DC off-hook loop current, if any. A1 output voltage is compared against a reference voltage at A4. Depending on the polarity of the comparator's output, current source I_O either sources or sinks 10 μA into CAP2. This results in the charging and discharging of CAP2. Each positive transition of RSYNC enables comparator A5 for approximately 20 μs through the one-shot circuit, after which CAP2 is discharged via Q2. Thus, the resulting voltage on CAP2 after one ring cycle indicates the average DC component of the loop current. When the threshold of approximately 12 mA is reached, comparator A5 generates a pulse output at RT which is used to reset the ring driver flip-flop at approximately the zero crossing of the ringing signal.

If multiple ring frequencies must be used on the same line, then a compromise capacitor value for CAP2 must be used. A 0.1 μF value is recommended for ringing frequencies of 16 Hz to 40 Hz, and 0.033 μF for 30 Hz to 70 Hz. Alternately, if SUP output is used to perform ring trip detect externally, CAP2 input should be grounded.

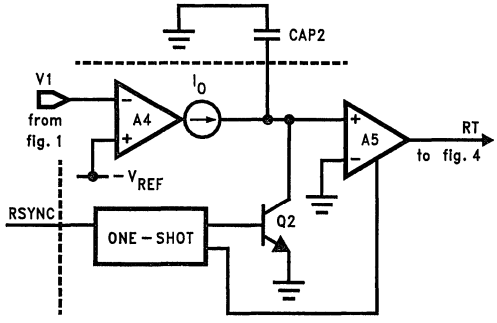


FIGURE 3. Ring Trip Circuit

RING RELAY DRIVER *(Figure 4)*

The ring relay driver consists of the ring trip latch, a ring relay flip-flop and a relay driver output transistor. Based on the state of the ring input, the ring-trip latch is set or cleared when EN is active high, and latched on the falling edge of EN. It is also cleared by the ring trip circuit. Based on the output of the ring-trip latch, the ring relay flip-flop is set or cleared on the positive transition of RSYNC, insuring that the ring relay is turned on or off near the zero crossing of the ring signal to minimize relay contact wear. After the ring relay driver is turned on, the RING and/or EN inputs should be kept at logic low in order to prevent relay chattering.

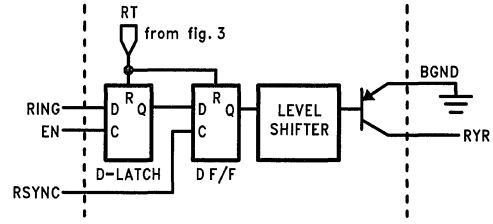


FIGURE 4. Ring Trip Relay Driver (PNP-type)

GENERAL PURPOSE RELAY DRIVERS *(Figure 5)*

The general purpose relay drivers consist of a relay driver latch and relay driver output transistor. Depending on the state of the appropriate input RC1 or RC2, the relay driver latches are set or cleared when EN is active high, and latched on the falling edge of EN. On the TP3200 the relay driver pnp transistors operate between BGND and a negative supply as high as −70 volts, with relay currents as high as 30 mA. On the TP3204, the relay driver npn transistors operate with a positive supply voltage up to 20 volts.

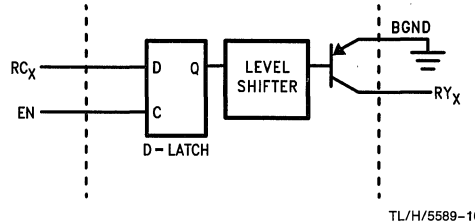
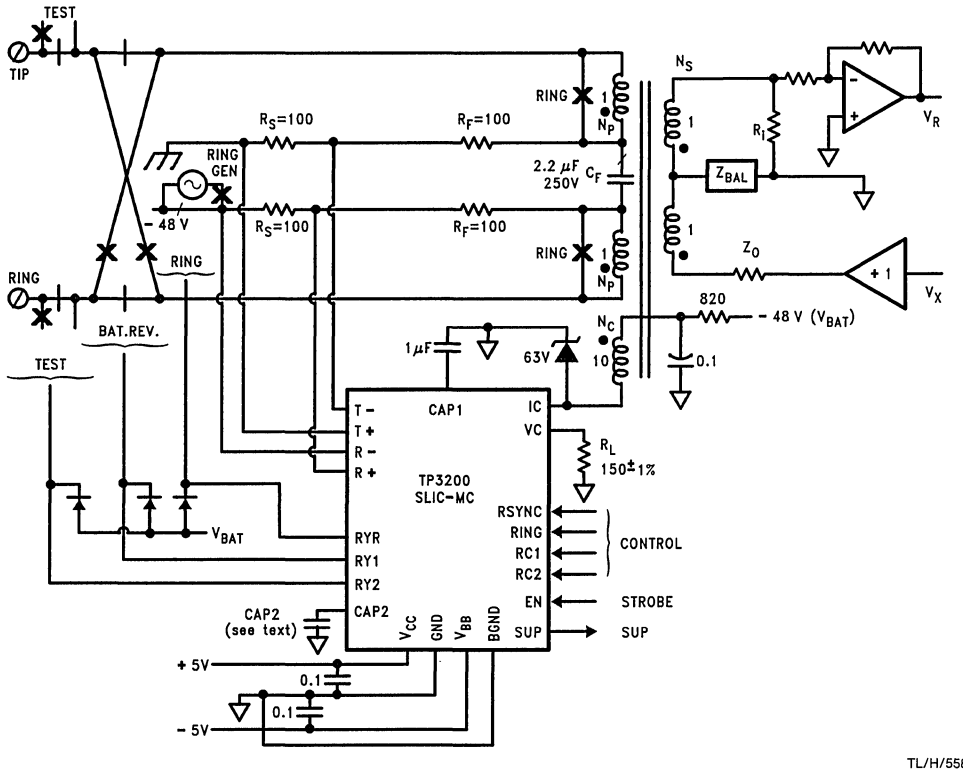


FIGURE 5. Relay Drivers RY1 and RY2, (PNP-type)



TL/H/5589-11

FIGURE 6. Typical Applications Schematic

Note 1: Resistors R_S, R_F are matched to within ±0.1% to achieve 60 dB longitudinal balance.

Note 2: Transformer specifications for 600Ω Line Impedance, 5:1 cancellation ratio, $Z_O = R_i = 300\Omega$.

primary windings	N_P	210T	AWG 36
secondary windings	N_S	2x220T	AWG 38
compensation winding	N_C	2100T	AWG 42

Siemens Type RM 8-T35 core (A_L = 8400 nH/T²)

Applications Information

Figure 6 illustrates the use of the TP3200/02/04 in one of many possible configurations. In this application, 200 ohm feed resistors ($R_S + R_F$) are used with a fixed −48 volt battery feed. 100 ohm current sense resistors in series with additional 100 ohm resistors insure that the T and R sense inputs of the device never see more than one half of any line transient voltages. The two general purpose relay drivers are used to operate a line test relay and a battery reversal relay. The a.c. line termination impedance is set by resistors R_i and Z_o (which should be equal to properly balance the hybrid), and the square of the turns ratio of the transformer, $(2N_p/N_S)^2$. The two amplifiers on the secondary side of the transformer are normally part of the PCM filter such as the TP3040, or the TP3050, TP3060, or TP3070 series of COMBO™ Codec/Filters. Z_{bal} represents the line circuit balance network. It is recommended that the IC pin be connected to the finish of the compensation winding in order to reduce the effective loading of the line impedance as well as Z_{bal} due to the reflected capacitance from the compensation winding at IC.

Ring voltage insertion is accomplished by breaking the battery feed path and superimposing the a.c. voltage upon the battery voltage. To prevent the feed decoupling capacitor from shunting ring current, a break contact is placed in series with C_F. To prevent the line transformer primary windings from attenuating the ring voltage or introducing distortion, make contacts are connected in shunt with the transformer primary.

Each relay driver output must be protected by a diode connected close to the relay coil. The IC pin must also be protected against line transients coupled through the transformer. Standard secondary transient suppression must also be connected from Tip to GND and Ring to GND.

In order to minimize errors in flux cancellation, the ratio of resistors R_S and R_L must be carefully controlled. Normally, all would reside on a common hybrid circuit. The two resistors, R_S, must be very accurately matched as must the two resistors, R_F, although R_F need not match R_S.

Application Information (Continued)

The a.c. loop voltage will appear at IC, amplified by the ratio $N_C/(2N_p)$. A d.c. bias voltage must be provided which is sufficiently negative to prevent the compensation transistor from saturating without producing excessive power dissipation in the integrated circuit. This bias voltage can be an intermediate supply voltage or may be generated by the compensation current flowing through a resistance. The resistance may be made up of the transformer winding resistance and discrete resistances such as the filter resistor shown in *Figure 6.* If the bias voltage is generated by an IR drop, a higher supply voltage or lower compensation current ratio will be required to allow for large variations in loop current, resulting in higher circuit power dissipation.

Design Example

Assuming a 0 TLP on the line of 0 dBm into 600Ω, a 3 dB overload corresponds to a peak signal level of 1.55 volts. The peak a.c. voltage at IC is therefore 1.55N, where $N=N_C/(2N_P)$. At minimum loop current, the d.c. bias at IC must be sufficiently positive of the zener voltage to allow negative swings without clipping. Allowing for the winding resistance and reactance, a safe limit is:

$$R_C \bullet I_{LOOP}\,(\text{min})/N > 1.55N - V_{Z\,min} + |V_{BAT}|_{max} \quad (1)$$

where V_Z is the zener voltage, R_C is the total resistance from IC to V_{BAT}.

At the opposite extreme, the compensation transistor must not saturate with maximum loop current and positive peak swings. This corresponds to a voltage at IC of not less than

$$-VIC_{sat} + VC = 1.5 + I_{LOOP}\,(\text{max}) \bullet 2R_S \bullet A_V.$$

Thus we require:

$$|V_{BAT}|\,(\text{min}) > R_C \bullet I_{LOOP}\,(\text{max})/N + 1.55N - VIC_{SAT} + I_{LOOP}(\text{max}) \bullet 2R_S \bullet A_V \quad (2)$$

Substituting for R_C,

$$|V_{BAT}|(\text{min}) > (1.55N - V_{Zmin} + |V_{BAT}|_{max}) \bullet I_{LOOP}(\text{max})/I_{LOOP}(\text{min}) + 1.55N + 1.5 + 30I_{LOOP}(\text{max})$$

Thus for a minimum loop current of 20 mA and a maximum of 100 mA, with a minimum zener voltage of 58 volts, and battery voltage from −42V to −54V, the maximum compensation current ratio is 6.18:1.

If N = 5 is chosen, i.e. N_C = 10 Np, the allowable range for R_C can then be calculated. From 1), R_C > 938Ω, and from 2), R_C < 1487Ω. Since the resistance of the compensation winding may typically be 600Ω, an additional 820Ω can safely be added in series to form a high frequency filter on the battery supply.

Finally, from $Np/Nc = A_V \bullet R_S/R_L$, R_L = 150Ω.

Further Information

For additional information on design of suitable transformers see National Semiconductor Application Note AN-439.

For information on the design of matched attenuators suitable for setting Receive TLP levels, see the data sheet "TP3052 Family of COMBO™ Devices".

National Semiconductor

PRELIMINARY

TP3210 SLIM™ Subscriber Line Interface Module

General Description

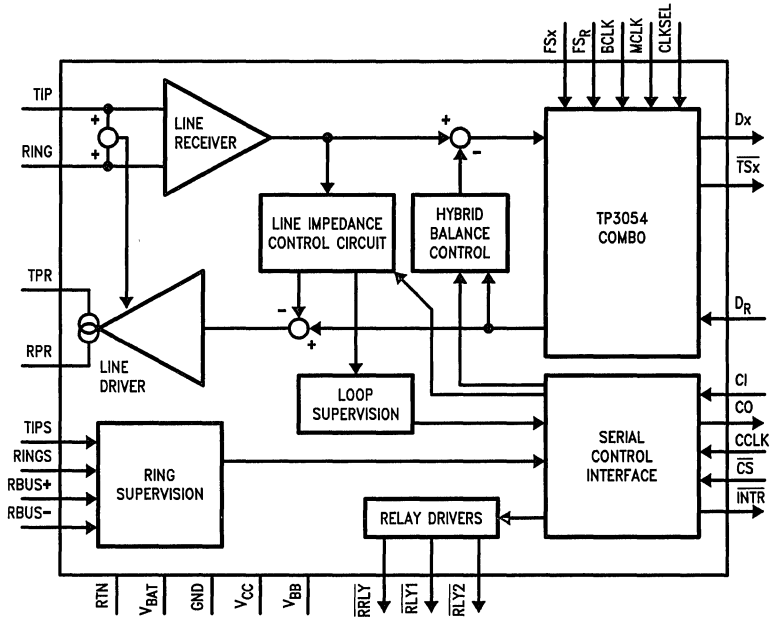
The TP3210 is a complete electronic SLIC and PCM COMBO® CODEC/Filter module intended to interface the analog subscriber line to a PCM highway. It is designed to meet the requirements for U.S. central office and remote switching applications. When used in conjunction with a simple, non-critical, external protection network, two resistors and a ring relay, the TP3210 forms a complete line circuit, handling all the BORSCHT functions.

The TP3210 module consists of a line driver, a line receiver, a line impedance control circuit, a hybrid balance circuit, a line supervision circuit, a ring supervision circuit, three positive relay drivers, a TP3054 μ-Law COMBO CODEC/Filter and a serial control interface. Any changes in the status of the subscriber loop generate an interrupt, allowing the device to be used in either polled or interrupt driven applications.

Features

- Complete COMBO CODEC/Filter and SLIC functions
- Exceeds LSSGR central office specifications
- In-band on-hook transmission capability
- Resistive loop feed with current limit
- Power denial mode
- Compatible with loop start and ground start signalling
- Automatic ring trip compatible with all U.S ringing conditions
- Four selectable hybrid balance networks
- Three relay drivers
- Thermal overload protection
- Compatible with inexpensive protection networks
- Withstands 500V RTN to GND surge
- Compatible with standard PCM highway
- Small physical size and minimal external components

Simplified Block Diagram

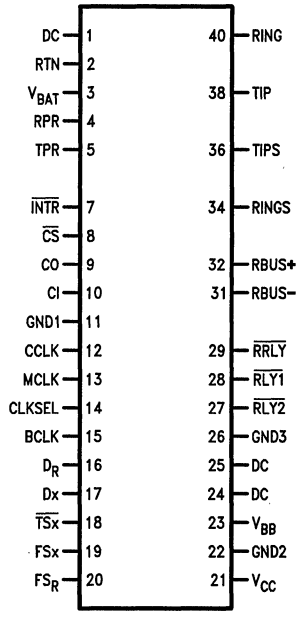


TL/H/9422–1

FIGURE 1. Simplified Block Diagram

Connection Diagram

Top View



TL/H/9422–2

Order Number TP3210J
NS Package Number HY40C

Pin Descriptions

Pin	Description
TIP	Normally positive side of the subscriber line.
RING	Normally negative side of the subscriber line.
TPR	High voltage line driver output. Connects to TIP via an external protection network.
RPR	High voltage line driver output. Connects to RING via an external protection network.
TIPS	Positive ring sensing input. Connected to the positive side of the subscriber loop during ringing.
RINGS	Negative ring sensing input. Connected to the negative side of the subscriber loop during ringing.
RBUS+	Positive ring bus sensing input. Connected to the positive side of the ring bus.
RBUS−	Negative ring bus sensing input. Connected to the negative side of the ring bus.
BCLK	Bit Clock used to shift PCM information into D_R and out of Dx. May vary from 64 kHz to 2.048 MHz in 8 kHz increments.
MCLK	Master Clock. Must be 1.536, 1.544 or 2.048 MHz.
CLKSEL	Master Clock Select Input. Must be connected high for 1.536 or 1.544 MHz operation. Must be connected low for 2.048 MHz operation.
FSx	Transmit frame synchronization pulse input which enables BCLK to shift the PCM information out of Dx. FSx is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
Dx	The TRI-STATE® PCM data output which is enabled by FSx.
$\overline{TSx}$	Open drain output which pulses low during the period when the Dx output is enabled.
FS_R	Receive frame synchronization pulse input which enables BCLK to shift the PCM information into D_R. FS_R is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
D_R	Receive data input. PCM data is shifted into D_R during the receive timeslot determined by FS_R.
CCLK	Control clock used to shift control data into CI and out of CO during $\overline{CS}$ low.
$\overline{CS}$	Chip select input. Must be low to enable the shifting of control data into CI and out of CO.
CI	The serial control data input used to set the operating state of the module.
CO	The serial status output used to monitor the operating state of the module. CO is TRI-STATE when $\overline{CS}$ is high. See *Figure 3* for timing diagram.
$\overline{INTR}$	Open drain interrupt output. A logic low indicates a change in the status of the subscriber loop, or a change in thermal shutdown.
V_{BB}	Negative power supply. $V_{BB} = 5V \pm 5\%$. Decoupled by internal 0.047 μF to ground.
V_{CC}	Positive power supply. $V_{CC} = 5V \pm 5\%$. Decoupled by internal 0.047 μF to ground.
$\overline{RRLY}$	Ring Relay Driver. Controlled by State Control Data Word bit D4 (see Table I). It is automatically turned off when ring trip is detected.
$\overline{RLY1}$	General purpose relay driver controlled by State Control Data Word bit D5.
$\overline{RLY2}$	General purpose relay driver controlled by State Control Data Word bit D6.
GND1 GND2 GND3	Low Voltage Ground. V_{BB}, V_{CC} and all digital signals are referenced to these pins. GND1, GND2 and GND3 should be externally connected together close to the module. Collectively referenced as GND in electrical specifications.
V_{BAT}	Negative high voltage supply. $V_{BAT} = -55V$ to $-59V$.
RTN	High voltage ground return. V_{BAT} and all analog signals are referenced to this pin.
DC	Don't connect. Do not make external connections to these pins.

Functional Block Description

Functional Block	Description
Line Driver	The Line Driver is a differential output transconductance amplifier which provides the d.c. power and balanced a.c. signals to the subscriber line. The d.c. power is determined by the d.c. Loop Impedance Control circuit. The a.c. signal applied to the line is controlled by the a.c. Loop Impedance Control and the analog signal generated by the TP3054 COMBO CODEC/Filter from the received PCM information. Feedback from the TIP and RING lines produces an effective longitudinal input impedance of about 150Ω from TIP and RING to RTN (75Ω total). In the presence of large longitudinal currents, each output of the Line Driver is capable of sourcing or sinking current to limit the longitudinal voltage.
Line Receiver	The Line Receiver monitors the metallic (differential) voltage on the line in the presence of large longitudinal (common mode) voltages.
Loop Impedance Control	The Loop Impedance Control feeds back the line voltage to produce a resistive/inductive d.c. feed impedance for longer loops and a constant current d.c. feed for shorter loops while maintaining an a.c. 2-wire input impedance of 900Ω + 2.16 μF over the voice band, easily meeting the 2-wire return loss requirements.
Hybrid Balance Control	The Hybrid Balance Control circuit consists of four software selectable networks, assuring that the 4-wire return loss requirements are met for a variety of conditions.
Loop Supervision	The Loop Supervision circuit monitors the d.c. current flow in the subscriber loop under non-ringing state and detects on-hook, off-hook and replicates dial pulses.
Ring Supervision	The Ring Supervision circuit monitors the d.c. current flow in the subscriber loop during the ringing state. This circuit is capable of detecting an off-hook condition in less than 200 ms in the presence of large a.c. ringing signals. It operates on loops with ringing superimposed on TIP or RING or with balanced ringing. It supports bridged ringers, ringers to ground on either TIP or RING and with superimposed ringers.
Relay Drivers	The three NPN relay drivers are capable of driving +5V or +12V relays directly. $\overline{\text{RRLY}}$ is dedicated to the ring relay and is automatically turned off when ring trip is detected by the Ring Supervision circuit. $\overline{\text{RLY1}}$ and $\overline{\text{RLY2}}$ are general purpose. Relay current will be returned to GND3 at pin 26.
COMBO	The COMBO provides the PCM filtering, encoding and decoding functions necessary to interface the PCM highway to the analog signals on the subscriber loop. This function is identical to the industry standard TP3054 COMBO CODEC/Filter (see the TP3054 datasheet for full details).
Control Interface	The Control Interface circuit provides easy control and monitoring of the state of the TP3210 via a simple serial interface. Via this circuit the user can program the operating mode of the module, and monitor the line status (see Table I for details).

Functional Description

Power-On

When power is first applied, the power-on reset circuitry initializes the TP3210 and places it in a standby mode. The State Control Data Word is cleared to "0". All unnecessary circuitry is powered down. The serial control interface and the loop supervision circuitry remain fully functional. The device is now ready for activation, either by the user programming it into the ring mode by writing into the State Control Data Word or by the subscriber going off-hook, powering-up the device automatically.

The State Control Data Word

The State Control Data word is a single eight-bit word as shown in Table I. Bits D0–D7 of the control word program the operating state of the device. The module can override the control bits D2 and D3 to activate the power denial mode in order to protect itself from damage under a thermal overload condition.

Status Word

The eight-bit Status Word indicates the status of the TP3210 at the instant a read operation is performed. Table IV shows the definitions of the status word. A logic high indicates that the state or function is enabled, a low indicatse that it is disabled.

The Control Interface

The Control Interface consists of a single eight-bit shift register and a buffer register. The shift register is written via the serial input CI, under the control of $\overline{\text{CS}}$ and CCLK, to program the device's operating state. Several bits of the shift register may be altered by the device itself in response to changes in the subscriber loop status. These changes in state may be read via the serial output CO. The S2 and S3 status bits are over-written by the occurrence of a thermal overload, forcing the device into the Power-Denial mode. S7 is the hook-switch status bit. A logic "0" for S7 indicates an Off-Hook or Ring-Trip condition exists at the instant of access and a logic "1" indicates on-hook. Any changes in line status, or thermal shutdown condition will generate an interrupt at $\overline{\text{INTR}}$ output.

Functional Description (Continued)

TABLE I. State Control Data Word

Control Bit	Description
D7	Don't Care. This bit is overwritten by the line supervision circuitry.
D6	A logic "1" turns on $\overline{RLY2}$.
D5	A logic "1" turns on $\overline{RLY1}$.
D4	A logic "1" enables Ring mode, turns on $\overline{RRLY}$ and Ring Supervision circuit. Status Bit S7 indicates ring-trip. Logic "0" at D4 enables the normal non-ringing mode.
D3	Used with D2 to select Power Denial, Battery Reversal and On-Hook Transmission modes. See Table II. Under Power Denial mode, the Line Driver is disabled, denying power to the subscriber loop. It can be set or cleared by a write operation. Under a thermal overload condition, D2 is forced to "0" and D3 is forced to "1" in order to protect the device from damage. As long as the thermal overload condition exists, the Power Denial mode cannot be cleared by a write operation.
D2	Used with D3 to select Power Denial, Battery Reversal and On-Hook Transmission modes. See Table II.
D1	Used with D0 to select hybrid balance network. See Table III.
D0	Used with D1 to select hybrid balance network. See Table III.

TABLE II. Operating Modes of TP3210

D4	D3	D2	Mode
0	**0**	**0**	Normal
0	0	1	Reverse Battery
0	1	0	Power Denial
0	1	1	On-Hook Transmission
1	X	X	Ring

TABLE III. Hybrid Balance Test Networks

D1	D0	Reference Test Network
0	**0**	900Ω
0	1	1650Ω‖(100Ω + 0.005 μF)
1	0	800Ω‖(100Ω + 0.05 μF)
1	1	900Ω + 2.16 μF

There are several ways of accessing the serial control interface. They are:

a. Write/Read

b. Read/Write

c. Quick Status Read

In the Write/Read operation, the objective is to change the state of the device. While shifting the new state control data into CI, the previous status information is shifted out of CO. This data should be compared with the previous status information to determine if a change had occurred since the last access.

In the Read/Write operation, the objective is to monitor the state of the module. While the current status is shifted out at CO, the last known state of the device is shifted into CI externally. If a thermal overload condition has occurred since the last access, the device will automatically set itself to the power denial mode (S2 bit will be forced to "0" and S3 bit will be forced to "1") prior to the access and will be reset by writing the previous state. This has no detrimental effect, however, since the power-denial mode will immediately be set again and the device will remain in the Power-Denial mode as long as the thermal overload continues to exist. If ring trip has occurred or the hook switch status has changed since the last access, the S7 bit will also be altered by the device. The timing for the Write/Read or Read/Write modes is shown in *Figure 2*.

The Quick Status Read operation allows a fast read of the S7 status bit, which indicates if a Ring-Trip or Off-Hook condition exists. It does not cause the shift register to shift, thus no control data is required. *Figure 3* is the timing diagram for the Quick Status Read Mode.

Functional Description (Continued)

TABLE IV. Status Information Word

Status Bit	Description
S7	Indicates switch hook status. S7 is a "1" if the subscriber is on-hook. If D4 is programmed to be "0" for normal mode, a logic "0" at S7 indicates off-hook. If the device is in the Ring mode (D4 = "1"), a logic "0" at S7 indicates ring-trip.
S6	A logic "1" indicates that $\overline{RLY2}$ is on.
S5	A logic "1" indicates that $\overline{RLY1}$ is on.
S4	A logic "1" indicates Ring mode is on. $\overline{RRLY}$ is turned on, and the Ring Supervision circuit is activated. A logic "0" at S7 indicates that a ring trip has occurred, forcing $\overline{RRLY}$ to be de-activated. D4 should be cleared to "0" by a write/read operation in order to program the device into the normal mode.
S3	S2 and S3 indicate Power-Denial, Battery Reversal and On-Hook Transmission modes. See Table II. When an overload condition exists which raises the junction temperature to exceed about 170°C, the TP3210 will automatically initialize a power denial mode (S2 forced to "0" and S3 forced to "1") to protect itself from damage. The device will not go back to the normal mode even if the thermal overload ceased to exist. The system can determine if the thermal overload condition has cleared itself by programming the TP3210 into the desired operating mode and read back status bits S2 and S3. If the overload still exists, the power denial mode will be activated again as long as the device's junction temperature exceeds approximately 170°C.
S2	S2 and S3 indicate Power-Denial, Battery Reversal and On-Hook Transmission modes. See Table II.
S1	S0 and S1 indicate the selected hybrid balance test network. See Table III.
S0	S0 and S1 indicate the selected hybrid balance test network. See Table III.

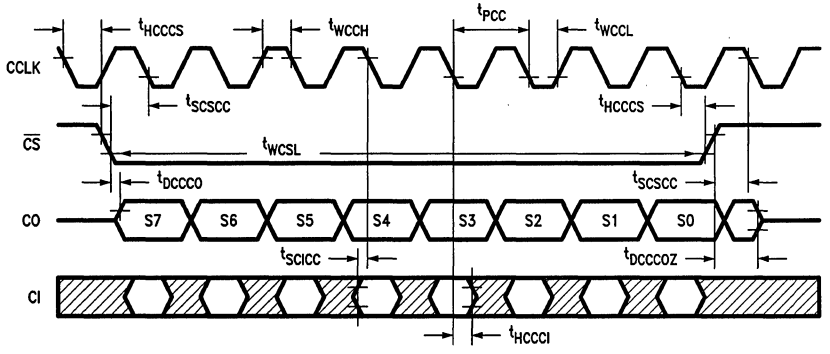


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FIGURE 2. Control Interface Timing—Write/Read or Read/Write Modes

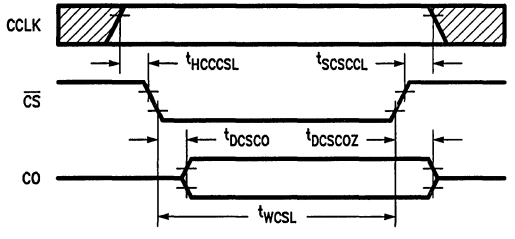

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FIGURE 3. Control Interface Timing—Quick Status Read Mode

Functional Description (Continued)

Battery Feed

The apparent battery voltage across the line is approximately 0.86 × V_{BAT}. With V_{BAT} = −56V, the TP3210 provides a nominal apparent battery voltage of −48V across TIP and RING. The module provides a resistive/inductive feed at longer loops. The d.c. current feed has been designed to guarantee 21 mA into a 1900Ω loop at nominal battery. At shorter loops, the d.c. feed is current-limited to nominally 43 mA in order to conserve power. At normal battery polarity (D2=0 and D3=0), TIP is more positive than RING. The current feed characteristic is shown in *Figure 4.*

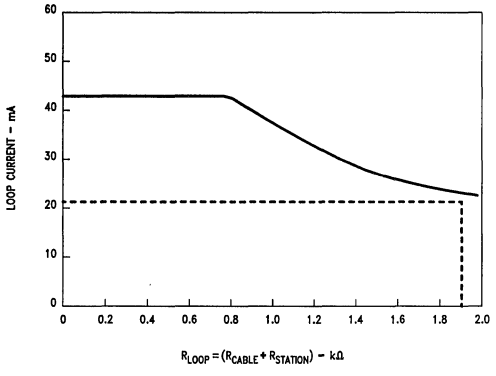

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FIGURE 4. DC Feed Characteristics

2-Wire Impedance

The nominal 2-wire input impedance is 900Ω + 2.16 μF. This is shunted by a feed inductance which is nominally 26 Henries on long loops, and approaches infinity on short loops.

Transmission Level

The 0 TLP is referenced at the PCM interface of the four wire ports. The TP3210 has 0.1 dB loss for both transmit and receive signals. On the 2-wire analog interface, the transmit is +0.1 TLP and the receive is −0.1 TLP. 0 TLP is defined as 0 dBm into 900Ω.

Hybrid Balance

The Hybrid Balance Control circuit contains four selectable balance networks which are selected by programming State Control Word bits D0 and D1. The balance networks are intended to be used with the corresponding reference test networks for hybrid balance as shown in Table III.

Longitudinal Balance and Longitudinal Current Capability

The 2-wire input of the device exhibits a longitudinal impedance of 150Ω from TIP to ground and from RING to ground. These impedances are extremely well matched and are not strongly dependent on impedance matching in the external protection network. The longitudinal voltage is sensed on the loop side of the protection network and fed back to the Line Driver, thus any component variations external to the device can be corrected by the feedback loop. The Line Driver is capable of handling 20 mA_{rms} of longitudinal current in each of the TIP and RING leads.

Loop Supervision

The Loop Supervision circuit operates in the normal (non-ringing) state. At normal battery polarity, off-hook is indicated when loop current exceeds nominally 8.5 mA and on-hook indicated when the current falls below nominally 6.5 mA, providing a 2 mA hysteresis. The Loop Supervision has been designed to maintain the dial pulse make interval greater than 25 ms regardless of the distortion introduced by the loop characteristics. At reversed battery polarity, off-hook is detected when loop current exceeds nominally 12 mA and on-hook indicated when current falls below nominally 10 mA. A logic "1" at status bit S7 indicates on-hook, while a logic "0" indicates off-hook. For Ground Start Signalling, TIP is opened with an external relay. Off-hook is indicated when the current from RING to ground exceeds nominally 17 mA and on-hook when the current falls below nominally 13 mA.

A typical example of hook switch timing is illustrated in *Figure 5.* While in the standby mode, all unnecessary circuitry is powered down. When Loop Supervision detects off-hook, the module is powered up, $\overline{INTR}$ goes low and status bit S7 is cleared (A). The $\overline{INTR}$ remains active until $\overline{CS}$ goes low and status is read, at which time the status of the switch hook is latched, clearing $\overline{INTR}$ (B). When the Loop Supervision detects on-hook, all unnecessary circuitry is again powered down, status bit S7 is set and $\overline{INTR}$ is again set low (C). When the status information is read, the present switch hook status is latched, clearing the interrupt, and $\overline{INTR}$ goes high (D). In the case of either on-hook or off-hook, if the system fails to read the status before the switch hook reverts to its previous state, the interrupt will clear itself (E). If the device's control interface is being accessed when off-hook occurs, i.e., $\overline{CS}$ is low, $\overline{INTR}$ is set low immediately (F) but S7 is cleared only after $\overline{CS}$ returns high (G). On the next Read/Write access, S7 is latched.

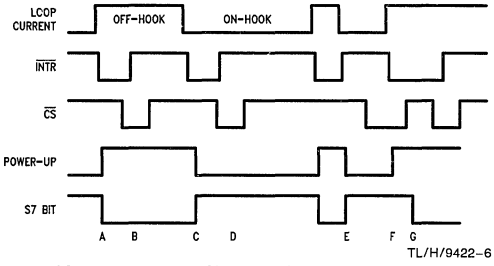

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FIGURE 5. Typical Hook Switch Detect Timing

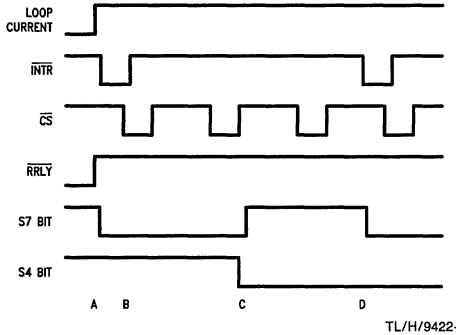
Ring Supervision

The Ring Supervision circuit measures the loop current across two 360Ω ring sensing resistors with a 1 MΩ internal resistive bridge (see *Figure 10*). The voltage at the output of the bridge is filtered, then algebraically added and subtracted from a voltage corresponding to a loop current of about 11 mAdc. Each of the resulting voltages are integrated over one period of the ring frequency and compared to zero. If either of the resulting voltages is less than zero for two consecutive cycles, ring-trip is detected. $\overline{RRLY}$ is de-activated, status bit S7 is cleared to "0" indicating ring trip, and an interrupt is also generated. Control bit D4 is not automatically reset to "0", it has to be cleared to "0" by a write/read operation after a ring trip is detected. If the MCLK is interrupted and stays continuously high or low for more than 200 μs, the ring relay driver will be turned off.

Functional Description (Continued)

The ring supervision circuit works with zero to five bridged ringers (1 ringer = 7 kΩ at 20 Hz),with ring frequencies from 16 Hz to 67 Hz, with ring voltages from 90 Vrms to 155 Vrms applied to either TIP or RING, superimposed on positive or negative battery voltages of from 42V to 56V on loops up to 1700Ω. Furthermore, it operates with up to five ringers connected from TIP or RING to ground or with up to three superimposed ringers connected from TIP to ground and three from RING to ground with a battery voltage of ±38 ±2V. The ring sensing inputs at TIPS, RINGS, RBUS+ and RBUS− when connected as shown in *Figure 10*, will present an effective load of about 500 kΩ across the ring bus.

A typical example of ring trip timing is illustrated in *Figure 6*. When the Ring Supervision circuit detects a ring trip, the device immediately turns off $\overline{RRLY}$, clears S7 and sets $\overline{INTR}$ low (A). The interrupt remains active until $\overline{CS}$ goes low and the status is read, at which time the status of the switch hook is latched, clearing $\overline{INTR}$ (B). Status bit S7 will remain a zero until the D4 bit is written to a zero, removing the device from the Ring mode (C). At this time, the S7 bit will indicate the switch hook status. Even though the station equipment is normally off-hook at this time, S7 will generally return to a "1" for several milliseconds (C) after D4 is cleared. This is because the Loop Supervision circuit was disconnected from the loop during ringing mode (D4 = 1), and it takes several milliseconds to detect the off-hook at which time S7 will be cleared and $\overline{INTR}$ will be set low (D). At this point the device is in the normal (non-ringing) mode, all necessary circuitry is powered up.



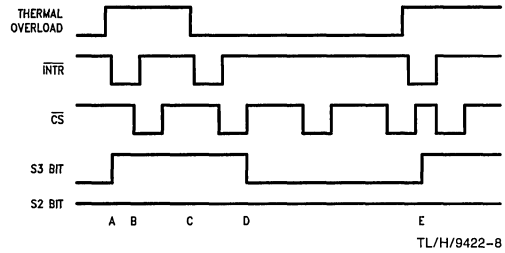
TL/H/9422–7

FIGURE 6. Typical Ring Trip Detect Timing

Thermal Overload

The Line Driver incorporates a built-in thermal overload detection circuitry. In the event of a fault on the subscriber line which causes the Line Driver to reach an internal junction temperature of approximately 170°C, the Line Driver will protect itself by forcing the device into the power-denial mode (S2 is forced to "0" and S3 is forced to "1"). The device will remain in power-denial mode even though the thermal overload ceases to exist. After the line fault has been cleared, the device can be put back into service under system control (see Table IV).

A typical example of thermal overload detection timing is illustrated in *Figure 7*. When a thermal overload is detected, S2 is set low and S3 is set high (A), forcing the device into the Power-Denial mode, and $\overline{INTR}$ is set low. The interrupt remains active until $\overline{CS}$ goes low, clearing $\overline{INTR}$ (B). As long as the thermal overload condition exists, the power denial mode cannot be reset by a write operation (B). When the thermal overload condition clears, the $\overline{INTR}$ will again be set low, but the device continues to remain at power denial mode (C). Thus the device does not automatically reapply power to the line since the fault that originally caused the failure may still exist and would simply cause the overload to reoccur. In this example, the Power-Denial mode is cleared by a control write to normal mode, clearing S2 and S3 to "0" (D). If the device is being accessed at the instant the thermal shutdown indication occurs, $\overline{INTR}$ is set low immediately, but S2 will be set low and S3 will be set high only after $\overline{CS}$ returns high (E).



TL/H/9422–8

FIGURE 7. Typical Thermal Overload Detection Timing

On-Hook Transmission Mode

The device is in the on-hook transmission mode when bit D3 and D2 of the State Control Data Word is set to the logic "1" and the loop is under "on-hook". In this mode, the line drivers operate in a reduced power state but all circuitry is active. This enables the system to communicate with a subscriber terminal or the subscriber to communicate through the network or to a terminal in the central office to provide alarm and telemetry services. When the loop goes off-hook, the loop supervision circuitry behaves normally and causes the line drivers to power up. Bit S7 of the Status Information Word is cleared and an interrupt is initiated. This enables the system to terminate any transmissions and handle the call initiation in the normal manner.

PCM Interface

The PCM interface consists of inputs MCLK, BCLK, FSx, FS_R and D_R, and outputs Dx and $\overline{TSx}$. MCLK controls the internal operation of the COMBO Codec/Filter's encoder and decoder, and must be 1.536 MHz or 1.544 MHZ if CLKSEL is connected high and 2.048 MHz if CLKSEL is connected low. BCLK shifts the PCM data out of Dx on its rising edge and latches the PCM data into D_R on its falling edge. It must be synchronous with MCLK and may be any integer multiple of 8 kHz from 64 kHz to 2.048 MHz. FSx and FS_R are 8 kHz pulse waveforms which determine the beginning of the PCM data transfer out of Dx and into D_R respectively. Both must be synchronous with MCLK but may have any phase relationship with each other. $\overline{TSx}$ is an open drain output which pulses low for the duration of the data transfer out of Dx. It is intended to be wire-ORed with the $\overline{TSx}$ outputs of other subscriber line interface modules to provide an enable signal for external TRI-STATE drivers buffering the PCM transmit data from a line card onto the backplane.

Short Frame Sync Operation

The TP3210 Subscribe Line Interface Module can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, the frame sync pulses applied to both FSx and FS_R must be one BCLK period long and with timing relationships as specified in *Figure 8*. With FSx high during a

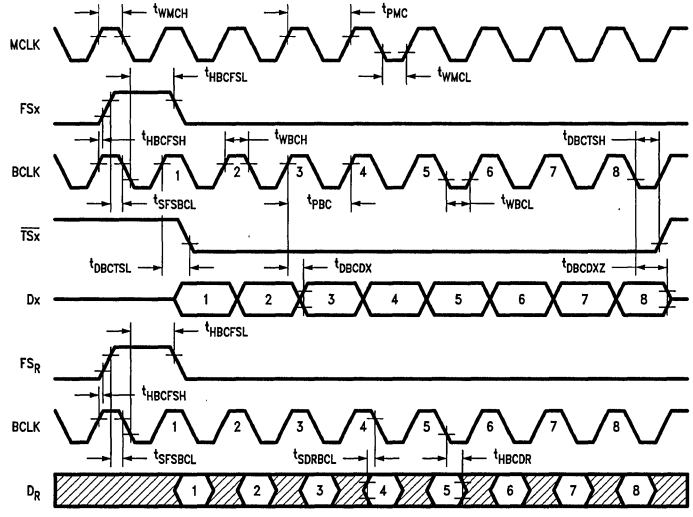
Functional Description (Continued)

falling edge of BCLK, the next rising edge of BCLK enables the Dx TRI-STATE output buffer, which will output the PCM sign bit. The following seven rising edges of the bit clock shifts out the remaining seven bits of PCM data, MSB first. The next falling edge disables the Dx output. With FS_R high during a falling edge of BCLK, the next falling edge latches the PCM sign bit into D_R. The next seven falling edges latch the remaining seven bits, MSB first.

Long Frame Sync Operation

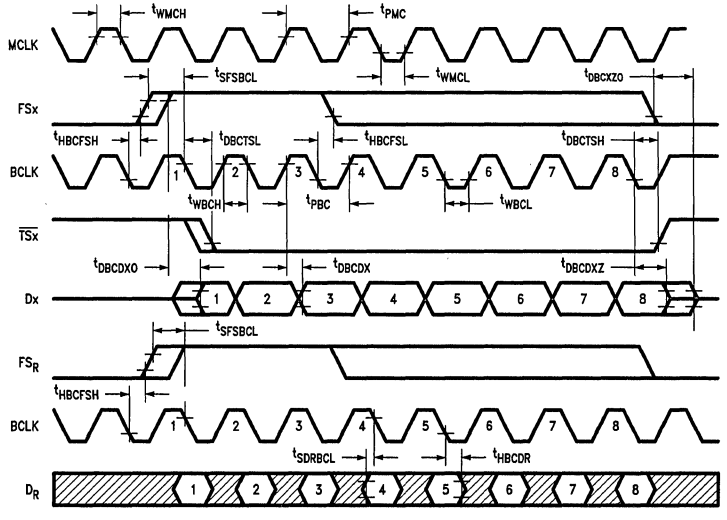
To use the long frame sync mode, the frame sync pulses applied to both FSx and FS_R must be three or more bit periods long, with timing relationships as specified in *Figure 9.*

Based on the transmit frame sync pulse, the device will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The Dx TRI-STATE output buffer is enabled with the rising edge of FSx or the rising edge of BCLK, whichever comes later, and the first bit clocked out is the PCM sign bit. The following seven rising edges of BCLK shift out the remaining seven bits, MSB first. The Dx output is disabled by the falling edge of BCLK following the eighth rising edge or by FSx going low, whichever comes later. A rising edge of the receive frame sync will cause PCM data at D_R to be latched in on the next eight falling edges of BCLK.



TL/H/9422–9

FIGURE 8. Timing Diagram for Short Frame Mode



TL/H/9422–10

FIGURE 9. Timing Diagram for Long Frame Mode

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	−0.5V to +7V
V_{BB} to GND	+0.5V to −7V
V_{BAT} to RTN	+0.5V to −70V
RTN to GND	±500V, 10 μs/50 μs Pulse
Voltage at Any Digital Input or Output	V_{CC} + 0.3V to GND − 0.3V
TPR, RPR to RTN	+2V to −85V (50 ms)
TIP, RING, TIPS, RINGS RBUS+, RBUS− to RTN	±1000V, 10 μs/1000 μs Pulse
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec)	300°C
Maximum Junction Temperature	150°C

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (Normal Mode: D2=0, D3=0)						
I_{BAT0}	V_{BAT} Idle Current	I_{Loop} = 0 mA, V_{BAT} = −57V		2.1	**3.2**	mA
I_{BB0}	V_{BB} Idle Current	I_{Loop} = 0 mA		1.9	**3.5**	mA
I_{CC0}	V_{CC} Idle Current	I_{Loop} = 0 mA		2.9	**4.5**	mA
I_{BAT1}	V_{BAT} Active Current	I_{Loop} = 20 mA, V_{BAT} = −57V		23	**25**	mA
I_{BB1}	V_{BB} Active Current	I_{Loop} = 20 mA		8.9	**15.2**	mA
I_{CC1}	V_{CC} Active Current	I_{Loop} = 20 mA		11.8	**15.2**	mA
POWER DISSIPATION (On-Hook Transmission Mode: D2=1, D3=1)						
I_{BAT0H}	V_{BAT} Idle Current	I_{Loop} = 0 mA, V_{BAT} = −57V		2.1	**3.2**	mA
I_{BB0H}	V_{BB} Idle Current	I_{Loop} = 0 mA		8.9	**15.2**	mA
I_{CC0H}	V_{CC} Idle Current	I_{Loop} = 0 mA		11.8	**15.2**	mA
DIGITAL INTERFACE (Note 1)						
V_{IL}	Input Low Level				**0.7**	V
V_{IH}	Input High Level	All Digital Inputs except CLKSEL CLKSEL	**2** **4**			V V
V_{OL}	Output Low Level	Dx, $\overline{TSx}$, CO, I_L = 3.2 mA $\overline{INTR}$, I_L = 2.0 mA			**0.4** **0.4**	V V
V_{OH}	Output High Level	Dx, CO, I_H = −3.2 mA	**2.4**			V
I_{IL}	Input Low Current	GND < V_{IN} < V_{IL}, All Digital Inputs	**−100**		**100**	μA
I_{IH}	Input High Current	V_{IH} < V_{IN} < V_{CC}, All Digital Inputs	**−100**		**100**	μA
I_{OH}	Output High Current	$\overline{TSx}$ and $\overline{INTR}$, V_{OH} < V_{OUT} < V_{CC}	**−100**		**100**	μA
I_{OZ}	Output Current in the High Impedance State (TRI-STATE)	CO, Dx	**−100**		**100**	μA

Note 1: See Appendix I for the definition of digital interface parameters.

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BATTERY FEED						
I_{Loop+}	Loop Current	R_{Loop} = 1900Ω, V_{BAT} = −55V R_{Loop} = 1300Ω, V_{BAT} = −57V R_{Loop} = 200Ω, V_{BAT} = −59V V_{BB} = −5V ±5%	**21** **27** **40**	 43	**24** **33** **46**	mA mA mA
I_{Loop-}	Reverse Loop Current	R_{Loop} = 1900Ω, V_{BAT} = −55V R_{Loop} = 1300Ω, V_{BAT} = −57V R_{Loop} = 200Ω, V_{BAT} = −59V V_{BB} = −5V ±5%	**20** **26** **38**	 43	**25** **34** **46**	mA mA mA
I_{PD}	Power Denial Loop Current	R_{Loop} = 200Ω		0.1	**2**	mA
V_{Loop}	Loop Voltage	R_{Loop} = 10 kΩ		−46.8		V
LOOP SUPERVISION						
Roffhk0	Loop Resistance to Produce an Off-Hook Indication at Loop Start	Roffhk0 Connected from TIP to RING, V_{BAT} = −55V			**2400**	Ω
Ronhk0	Loop Resistance to Produce an On-Hook Indication at Loop Start	Ronhk0 Connected from TIP to RING, V_{BAT} = −59V	**9**			kΩ
Roffhk1	Loop Resistance to Produce an Off-Hook Indication at Ground Start	Roffhk1 Connected from RING to RTN, TIP Open V_{BAT} = −55V			**2450**	Ω
Ronhk1	Loop Resistance to Produce an On-Hook Indication at Ground Start	Ronhk1 Connected from RING to RTN, TIP Open V_{BAT} = −59V	**9**			kΩ
DPD	Dial Pulse Distortion	R_{Leak} = 10 kΩ ‖ (5 kΩ + 2.16 μF) R_{Loop} = 200Ω, 12 pps, Break = 64% R_{Loop} = 1900Ω, 12 pps, Break = 64% $\overline{CS}$ High, Measure Width of Make Period at $\overline{INTR}$	 **25** **25**		 **58** **58**	 ms ms
RING SUPERVISION						
RNGTRP1	Ring Trip Detect, Normal Ringing	RBUS+ = 0V, RBUS− = −48V TIPS = −4.70V, RINGS = −43.3V, Must Detect Ring-Trip within the Specified Time	**50**		**180**	ms
RNGTRP2	Ring Trip Detect, Reverse Ringing	RBUS+ = −48V, RBUS− = 0V, TIPS = −43.3V, RINGS = −4.7V, Must Detect Ring-Trip within the Specified Time	**50**		**180**	ms

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RING SUPERVISION (Continued)						
RNGTRP3	Ring Trip Non-Detect Normal Ringing	RBUS+ = 0V, RBUS− = −48V, TIPS = −3.25V, RINGS = −44.75V, Must Not Detect Ring-Trip within the Specified Time (Note 2)	**0**		**180**	ms
RNGTRP4	Ring Trip Non-Detect Reverse Ringing	RBUS+ = −48V, RBUS− = 0V, TIPS = −44.75V, RINGS = −3.25V, Must Not Detect Ring-Trip within the Specified Time (Note 2)	**0**		**180**	ms
RNGTRP5	Ring Trip Detect, Normal Ringing	TIPS, RBUS− = −4.7V, RINGS, RBUS+ = 17 Vrms, f = 20 Hz, Must Detect Ring-Trip within the Specified Time	**100**		**190**	ms
RNGTRP6	Ring Trip Detect Reverse Ringing	TIPS, RBUS− = 17 Vrms, RINGS, RBUS+ = −4.7V, f = 20 Hz, Must Detect Ring-Trip within the Specified Time	**100**		**190**	ms
RNGTRP7	Ring Trip Non-Detect Normal Ringing	TIPS, RBUS− = −3.25V, RINGS, RBUS+ = 17 Vrms, f = 20 Hz, Must Not Detect Ring-Trip within the Specified Time (Note 2)	**0**		**190**	ms
RNGTRP8	Ring Trip Non-Detect Reverse Ringing	TIPS, RBUS− = 17 Vrms, RINGS, RBUS+ = −3.25V, f = 20 Hz, Must not Detect Ring-Trip within the Specified Time (Note 2)	**0**		**190**	ms
HYBRID BALANCE Unless otherwise specified, I_{Loop} = 20 mA, D2=0, D3=0						
ECHO1	4-Wire Return Loss	Z_{REF} = 900Ω across Tip-Ring D1 = 0, D0 = 0 f = 203.125 Hz = 484.375 Hz = 1015.625 Hz = 2500 Hz = 3406.25 Hz	 **21** **26** **26** **26** **21**	 40 	 	 dB dB dB dB dB
ECHO2	4-Wire Return Loss	Z_{REF} = 1650Ω ‖ (100Ω + 0.005 μF) D1 = 0, D0 = 1 f = 203.125 Hz = 484.375 Hz = 1015.625 Hz = 2500 Hz = 3406.25 Hz	 **21** **26** **26** **26** **21**	 40 	 	 dB dB dB dB dB
ECHO3	4-Wire Return Loss	Z_{REF} = 800Ω ‖ (100Ω +0.05 μF) D1 = 1, D0 = 0 f = 203.125 Hz = 484.375 Hz = 1015.625 Hz = 2500 Hz = 3406.25 Hz	 **21** **26** **26** **26** **21**	 40 	 	 dB dB dB dB dB

Note 2: The intent of Ring Trip Non-Detect tests are to ensure that ring does not occur under the specified conditions even after an essentially infinite period of time. For practical purposes of cost effectively testing the SLIM Subscriber Line Interface Module, the wait time to determine that a false ring trip has not occurred has necessarily been limited to a value which has been determined through characterization to ensure that false ring trip never occurs.

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
HYBRID BALANCE (Continued)						
ECHO4	4-Wire Return Loss	Z_{REF} = 900Ω + 2.16 μF D1 = 1, D0 = 1				
		f = 203.125 Hz	**21**			dB
		= 484.375 Hz	**26**			dB
		= 1015.625 Hz	**26**	40		dB
		= 2500 Hz	**26**			dB
		= 3406.25 Hz	**21**			dB
TRANSMISSION Unless Otherwise Noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{Loop} = 20 mA, D2 = 0, D3 = 0						
RTNLOSS	2-Wire Return Loss	f = 203.125 Hz	**21**			dB
		= 484.375 Hz	**27**			dB
		= 1015.625 Hz	**27**	40		dB
		= 2500 Hz	**27**			dB
		= 3406.25 Hz	**27**			dB
0 dBmO	The Absolute 2-Wire Reference Level	The Absolute Reference Level at at the 2-Wire Interface is Defined as 0 dBm into 900Ω.		0.949		Vrms
GRA	Absolute Receive Gain	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −56V, f = 1015.625 Hz, T_A = +25°C, Input = Digital Code for 0 dBm0 at D_R, Measure Voltage across TIP-RING.	**−0.35**	−0.1	**0.15**	dB
GXA	Absolute Transmit Gain	V_{CC} = 5V, V_{BB} = −5V V_{BAT} = −56V, f = 1015.625 Hz, T_A = +25°C, Input = 0 dBm0 at 2-Wire Port, Measure Digital Code at Dx.	**−0.35**	−0.1	**0.15**	dB
GRA0H	Absolute Receive Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V V_{BAT} = −56V, T_A = +25°C, Z_{REF} = 900Ω + 2.16 μF I_{Loop} = 0 mA, D2=1, D3=1	**−1.1**	−0.1	**0.9**	dB
GXA0H	Absolute Transmit Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V V_{BAT} = −56V, T_A = +25°C, I_{Loop} = 0 mA, D2=1, D3=1	**−1.1**	−0.1	**0.9**	dB
GRAV	Absolute Receive Gain over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5% V_{BAT} = −55V to −59V, f = 1015.625 Hz	**−0.4**	−0.1	**0.2**	dB
GXAV	Absolute Transmit Gain over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5% V_{BAT} = −55V to −59V, f = 1015.625 Hz	**−0.4**	−0.1	**0.2**	dB
GRT	Receive Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −56V, f = 1015.625 Hz Reference to GRA	−0.1		0.1	dB
GXT	Transmit Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −56V, f = 1015.625 Hz Reference to GXA	−0.1		0.1	dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless Otherwise Noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{Loop} = 20 mA, D2=0, D3=0 (Continued)						
GRF	Receive Frequency Response	Measure Relative to GRA,				
		f = 203.125 Hz	**−1.9**		**0**	dB
		= 296.875 Hz	**−0.4**		**0.25**	dB
		= 484.375 Hz	**−0.25**		**0.25**	dB
		= 2015.625 Hz	**−0.25**		**0.25**	dB
		= 2703.125 Hz	**−0.25**		**0.25**	dB
		= 3015.625 Hz	**−0.25**		**0.25**	dB
		= 3203.125 Hz	**−0.25**		**0.25**	dB
		= 3390.625 Hz	**−1.2**		**0**	dB
		= 3984.375 Hz			**−14**	dB
SOS	Spurious Out of Band Signals (Alias Tones)	Measure Relative to GRA,				
		f = 4796.75 Hz			**−30**	dB
		= 6703.125 Hz			**−30**	dB
		= 11390.625 Hz			**−30**	dB
GXF	Transmit Frequency Response	Measure Relative to GXA,				
		f = 62.500 Hz			**−21**	dB
		= 203.125 Hz	**−2.5**		**0**	dB
		= 296.875 Hz	**−0.4**		**0.25**	dB
		= 484.375 Hz	**−0.25**		**0.25**	dB
		= 2015.625 Hz	**−0.25**		**0.25**	dB
		= 2703.125 Hz	**−0.25**		**0.25**	dB
		= 3015.625 Hz	**−0.25**		**0.25**	dB
		= 3203.125 Hz	**−0.25**		**0.25**	dB
		= 3390.625 Hz	**−1.2**		**0**	dB
		= 3984.375 Hz			**−14**	dB
		= 5046.875 Hz			**−32**	dB
		= 11890.625 Hz			**−32**	dB
GRL	Receive Gain Variation with Signal Level	Measure Relative to GRA PCM Level				
		= 3.1 dBmO	**−0.25**		**0.25**	dB
		= −2.3 dBmO	**−0.25**		**0.25**	dB
		= −11.4 dBmO	**−0.25**		**0.25**	dB
		= −17.6 dBmO	**−0.25**		**0.25**	dB
		= −23.9 dBmO	**−0.25**		**0.25**	dB
		= −29.9 dBmO	**−0.25**		**0.25**	dB
		= −37.8 dBmO	**−0.25**		**0.25**	dB
		= −47.1 dBmO	**−0.45**		**0.45**	dB
		= −55.7 dBmO	**−1.3**		**1.3**	dB
GXL	Transmit Gain Variation with Signal Level	Measure Relative to GXA PCM Level				
		= 3.1 dBmO	**−0.25**		**0.25**	dB
		= −2.3 dBmO	**−0.25**		**0.25**	dB
		= −11.4 dBmO	**−0.25**		**0.25**	dB
		= −17.6 dBmO	**−0.25**		**0.25**	dB
		= −23.9 dBmO	**−0.25**		**0.25**	dB
		= −29.9 dBmO	**−0.25**		**0.25**	dB
		= −37.8 dBmO	**−0.25**		**0.25**	dB
		= −47.1 dBmO	**−0.45**		**0.45**	dB
		= −55.7 dBmO	**−1.3**		**1.3**	dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless Otherwise Noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{Loop} = 20 mA, D2=0, D3=0 (Continued)						
STDR	Receive Signal to Total Distortion	Measure through C Message Filter f = 1015.625 Hz, PCM Level				
		= 3.1 dBmO	**33**			dBC
		= 0.0 dBmO	**36**			dBC
		= −2.3 dBmO	**36**			dBC
		= −11.4 dBmO	**36**			dBC
		= −17.6 dBmO	**36**			dBC
		= −23.9 dBmO	**36**			dBC
		= −29.9 dBmO	**35**			dBC
		= −37.8 dBmO	**31**			dBC
		= −40.0 dBmO	**29**			dBC
		= −45.0 dBmO	**25**			dBC
		= −47.1 dBmO	**23**			dBC
		= −55.7 dBmO	**14**			dBC
STDX	Transmit Signal to Total Distortion	Measure through C Message Filter f = 1015.625 Hz, PCM Level				
		= 3.1 dBmO	**33**			dBC
		= 0.0 dBmO	**36**			dBC
		= −2.3 dBmO	**36**			dBC
		= −11.4 dBmO	**36**			dBC
		= −17.6 dBmO	**36**			dBC
		= −23.9 dBmO	**36**			dBC
		= −29.9 dBmO	**35**			dBC
		= −37.8 dBmO	**31**			dBC
		= −40.0 dBmO	**29**			dBC
		= −45.0 dBmO	**25**			dBC
		= −47.1 dBmO	**22**			dBC
		= −55.7 dBmO	**13**			dBC
DRA	Absolute Receive Delay	f = 1600 Hz		190		μs
DRR	Receive Delay Distortion	Measure Relative to DRA, f = 500 Hz		−2		μs
		= 1000 Hz		−10		μs
		= 2600 Hz		70		μs
		= 2800 Hz		100		μs
		= 3000 Hz		150		μs
DXA	Absolute Transmit Delay	f = 1600 Hz		300		μs
DXR	Transmit Delay Distortion	Measure Relative to DXA, f = 500 Hz		250		μs
		= 600 Hz		150		μs
		= 800 Hz		65		μs
		= 1000 Hz		30		μs
		= 2600 Hz		60		μs
		= 2800 Hz		80		μs
		= 3000 Hz		140		μs

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
NOISE Z_{REF} = 900Ω + 2.16 μF, I_{Loop} = 20 mA, D2=0, D3=0						
NRC	Receive C Message Weighted Idle Channel Noise	PCM Code is Alternating Positive and Negative Zeroes		9	**13**	dBrnC0
NXC	Transmit C Message Weighted Idle Channel Noise	Measured by Extrapolation from Signal to Distortion Measurements at −50 dBmO		13	**16**	dBrnC0
POWER SUPPLY REJECTION RATIO Unless Otherwise Specified, Z_{REF} = 900Ω + 2.16 μF, I_{Loop} = 20 mA, D2=0, D3=0						
$PPSR_R$	V_{CC} Power Supply Rejection, Receive	f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	**30** **30** **30**			dB dB dB
$VPSR_R$	V_{BAT} Power Supply Rejection, Receive	f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	**30** **40** **40**			dB dB dB
PPSRx	V_{CC} Power Supply Rejection, Transmit	f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	**30** **30** **30**			dB dB dB
VPSRx	V_{BAT} Power Supply Rejection, Transmit	f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	**30** **40** **40**			dB dB dB
LONGITUDINAL BALANCE AND CAPABILITY						
I_{LLS1}	Longitudinal Current Capability, Loop Start	I_{Loop} = 5 mA, f = 60 Hz, Inject I_{LLS1} into TIP and RING. Device Must Not Detect Off-Hook. Triangular Waveform	**21**			mArms
I_{LLS2}	Longitudinal Current Capability, Loop Start	I_{Loop} = 21 mA, f = 60 Hz, Inject I_{LLS2} into TIP and RING. Device Must Not Detect On-Hook. Triangular Waveform	**21**			mArms
I_{LGS1}	Longitudinal Current Capability, Ground Start	f = 60 Hz, I_{Ground} = 0 mA Triangular Waveform. Inject I_{LGS1} into RING, TIP Open. Device Must Not Detect Off-Hook	**8.5**			mArms
I_{LGS2}	Longitudinal Current Capability, Ground Start	I_{Ground} = 50 mA, f = 60 Hz. Inject I_{LGS2} into RING, TIP Open. Device Must Not Detect On-Hook. Triangular Waveform	50			mArms
BAL2W	2-Wire Longitudinal Balance	IEEE Method 455-1976, I_{Loop} = 20 mA, $I_{Longitudinal}$ = 20 mArms/leg, Measure $V_{metallic}$ across TIP-RING f = 62.5 Hz = 203.125 Hz = 1015.625 Hz = 2015.625 Hz = 2703.125 Hz = 3000 Hz = 3406.25 Hz	 **61** **61** **61** **61** **56** **54** **51**	 64 64 59		 dB dB dB dB dB dB dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RELAY DRIVERS						
V_{Ron}	Driver On Voltage	I_L = 80 mA			**1**	V
I_{Roff}	Leakage Current	V_{Relay} = 40V, Relay Off			**100**	μA
DIGITAL TIMING, PCM INTERFACE (See *Figures 8* and *9*, Notes 4 and 5)						
$1/t_{PMC}$	MCLK Frequency	Clock Frequency Accuracy < ±100 ppm		1.536 1.544 **2.048**		MHz MHz MHz
t_{WMCH}	Width of MCLK High		**160**			ns
t_{WMCL}	Width of MCLK Low		**160**			ns
$1/t_{PBC}$	BCLK Frequency				**2.048**	MHz
t_{WBCH}	Width of BCLK High		**160**			ns
t_{WBCL}	Width of BCLK Low		**160**			ns
SHORT FRAME SYNC MODE *(Figure 8)*						
t_{SFSBCL}	Setup Time from FS High to BCLK Low		**50**			ns
t_{HBCFSL}	Hold Time from BCLK Low to FS Low		**100**			ns
t_{HBCFSH}	Hold Time from BCLK Low to FS High		**0**			ns
t_{DBCDX1}	Delay Time from Bit Clock to Dx Data Valid	C_L = 150 pF Plus 2 LSTLL Loads	**0**		**140**	ns
t_{DBCDXz}	Delay Time from BCLK to Dx Disabled	C_L = 50 pF	**50**		**165**	ns
t_{DBCTSL}	Delay Time from BCLK to $\overline{TSx}$ Low	C_L = 150 pF Plus 2 LSTTL Loads			**140**	ns
t_{SDRBCL}	Setup Time from Dr to BCLK Low		**50**			ns
t_{HBCDR}	Hold Time from BCLK Low to D_R Valid		**50**			ns

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LONG FRAME SYNC MODE *(Figure 9)*						
t_{HBCFSH}	Hold Time from BCLK Low to FS		**0**			ns
t_{SFSBC0}	Setup Time from FS to BCLK Low		**80**			ns
t_{WFSL}	Width of FS Low		**160**			ns
t_{DBCDX0}	Delay Time from BCLK or FS, Whichever Comes Later to Dx Valid	C_L = 150 pF Plus 2 LSTTL Loads	**20**		**165**	ns
t_{DBCDX}	Delay Time from BCLK to Dx Valid	C_L = 150 pF Plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBCDXz}	Delay Time from BCLK to Dx Disabled	C_L = 50 pF	**50**		**165**	ns
$t_{DBCDXz0}$	Delay Time from BCLK or FS, Whichever Comes Later, to Dx Disabled	C_L = 50 pF	**20**		**165**	ns
t_{SDRBC}	Setup Time from D_R to BCLK Low		**50**			ns
t_{HBCDR}	Hold Time from BCLK Low to D_R Valid		**50**			ns
DIGITAL TIMING, SERIAL CONTROL INTERFACE (See *Figures 2* and *3*, Notes 4 and 5)						
$1/t_{PCC}$	CCLK Frequency	Frequency Accuracy < ±100 ppm	0.08		**2.048**	MHz
t_{WCCH}	Width of CCLK High		**200**			ns
t_{WCCL}	Width of CCLK Low		**200**			ns
t_{WCSL}	Width of $\overline{CS}$ Low				**100**	μs
READ/WRITE, WRITE READ MODES *(Figure 2)*						
t_{HCCCS}	Hold Time from CCLK to $\overline{CS}$		**100**			ns
t_{SCSCC}	Setup Time from $\overline{CS}$ to CCLK		**100**			ns
t_{DCCCO}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Valid	C_L = 150 pF Plus 2 LSTTL Loads			**150**	ns
t_{DCCCOZ}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Disabled				**150**	ns

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −55V to −59V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −56V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
READ/WRITE, WRITE READ MODES *(Figure 2)* (Continued)						
t_{SCCCI}	Setup Time from CI to CCLK		**100**			ns
t_{HCICC}	Hold Time from CCLK to CI		**100**			ns
t_{DCSIN}	Delay Time from $\overline{CS}$ Low to $\overline{INTR}$ High	R_L = 1 kΩ from $\overline{INTR}$ to V_{CC}			**200**	ns
QUICK STATUS READ MODE *(Figure 3)*						
t_{HCCCSL}	Hold Time from CCLK to $\overline{CS}$ Low		**100**			ns
t_{SCSCCL}	Setup Time from $\overline{CS}$ to CCLK Low		**100**			ns
t_{DCSCO}	Delay Time from $\overline{CS}$ to CO Valid	C_L = 150 pF Plus 2 LSTLL Loads			**150**	ns
t_{DCSCOZ}	Delay Time from $\overline{CS}$ to CO Disabled				**150**	ns

Note 4: See Appendix I for the definition and naming conventions used for digital timing parameters.

Note 5: See Table V for the definition of the mneumonics used for the digital timing parameters.

TABLE V. Timing Parameter Mneumonics

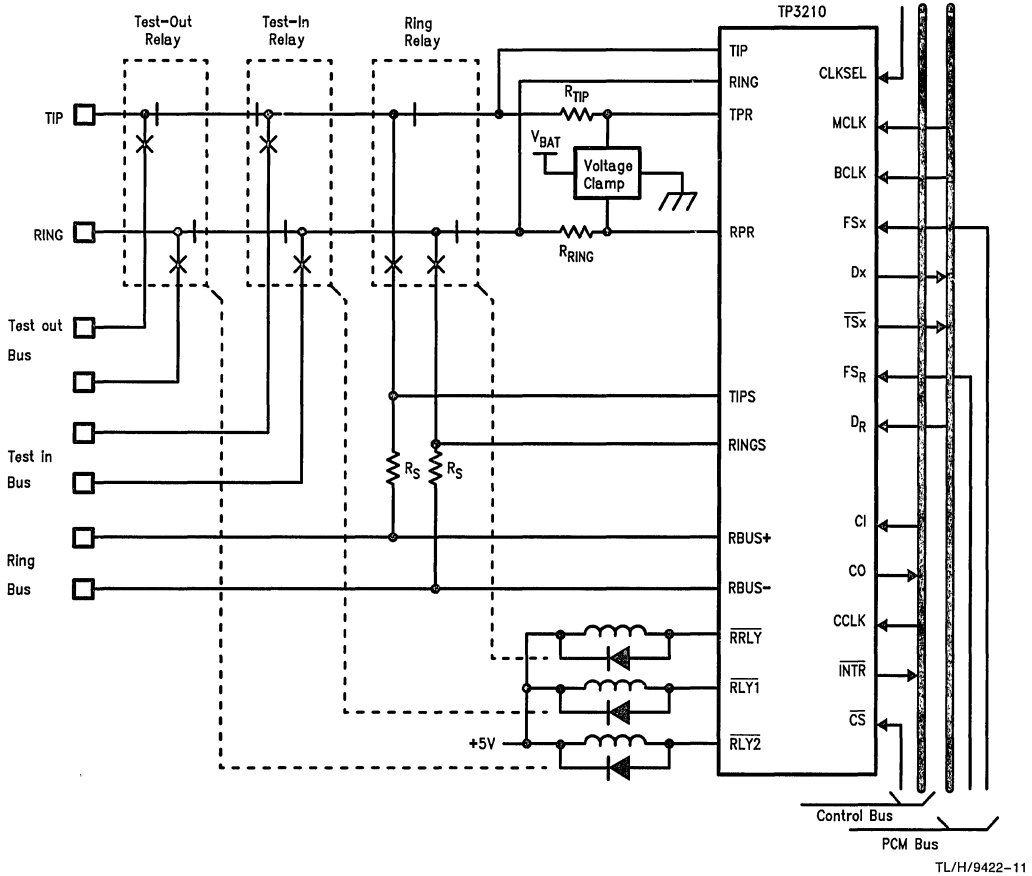
Pin Name	Mneumonic
$\overline{INTR}$	IN
$\overline{CS}$	CS
CO	CO
CI	CI
CCLK	CC
MCLK	MC
BCLK	BC
D_R	DR
Dx	DX
$\overline{TSx}$	TS
FS_R	FS
FSx	FS

Applications Information

Typical Line Circuit

Relatively few external components are required to implement a full featured central office line circuit. As shown in *Figure 10*, a complete line circuit is implemented using TP3210 with an external protection network consisting of fuse resistors R_{TIP} and R_{RING}, and a voltage clamp device, two 360Ω ring sensing resistors, a ring relay and two test relays. It should be noted that no supply decoupling capacitors are required for each line circuit at ±5V supplies, although the use of one larger electrolytic capacitor may be advisable for each power supply near the point at which it enters the line card.

Protection resistors R_{TIP} and R_{RING} should be nominally 100Ω matched to within ±1%. The selection of these protection resistors is important because they are fundamental to the ability of the line circuit to meet lightning and power cross requirements. R_{TIP} and R_{RING} should be designed such that they can withstand level one lightning and power cross requirements, while fusing open when over-stressed by level two lightning and power cross. TPR and RPR are protected by an external voltage clamp device to limit the voltage at these two pins to within +2 to −85V. The ring sensing resistors, R_S are 360Ω which sets the ring trip threshold to about 11 mAdC. The heavy relay current will be returned to GND3 at pin 26.



TL/H/9422–11

FIGURE 10. Complete Central Office Line Circuit

Applications Information (Continued)

Secondary Protection

The surge protection network in *Figure 10* consists of resistors R_{TIP}, R_{RING} and a voltage limiting circuit which limits the voltage at TPR and RPR. A number of low cost possibilities for this voltage limit are shown in *Figure 11*. The lowest cost solution is a simple full wave rectifier diode bridge used to clamp the voltage to no more than one or two volts above RTN or below V_{BAT}, provided that the V_{BAT} supply is capable to absorb the power surges. The TIP and RING input terminals of the TP3210 are internally connected in series to two 300 kΩ thick film resistors, which are capable to withstand power cross and surges.

Typical Line Card

A complete N-channel line card is illustrated in *Figure 12*. The backplane control interfaces vary greatly in different applications, and this example illustrates a possible arrangement.

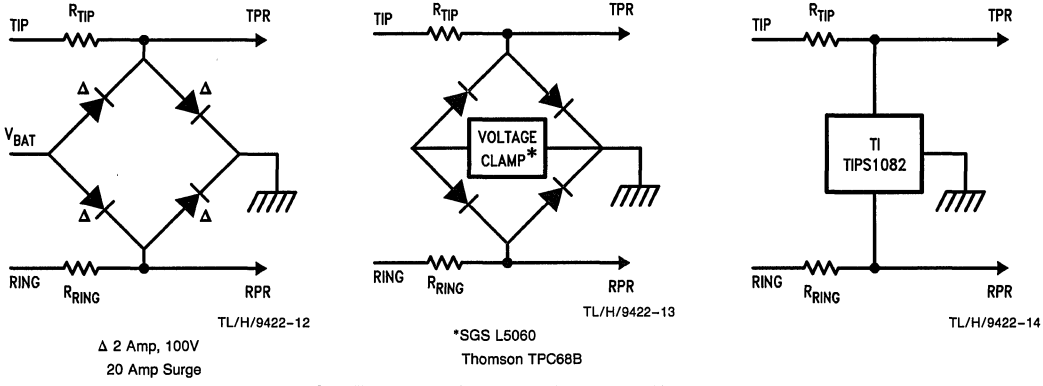


FIGURE 11. Some Secondary Protection Networks

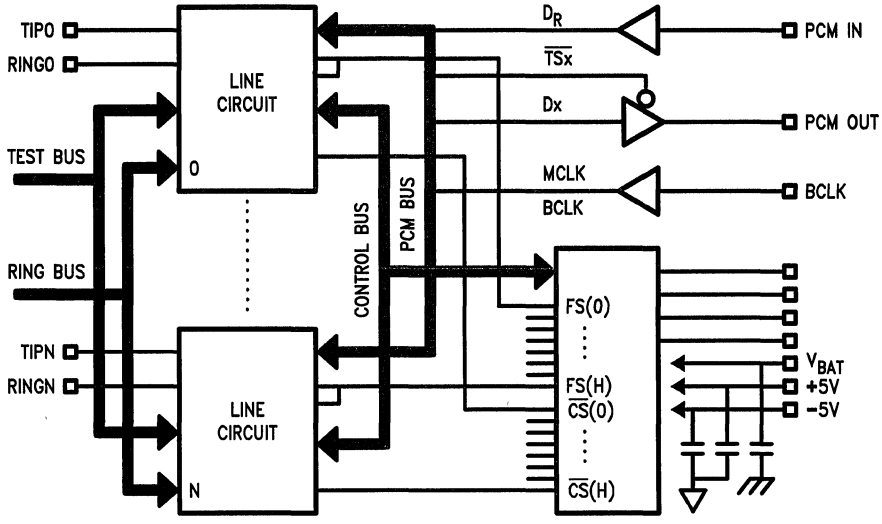


FIGURE 12. Typical N-Channel Linecard

National Semiconductor

PRELIMINARY

TP3211 SLIM™ Subscriber Line Interface Module

General Description

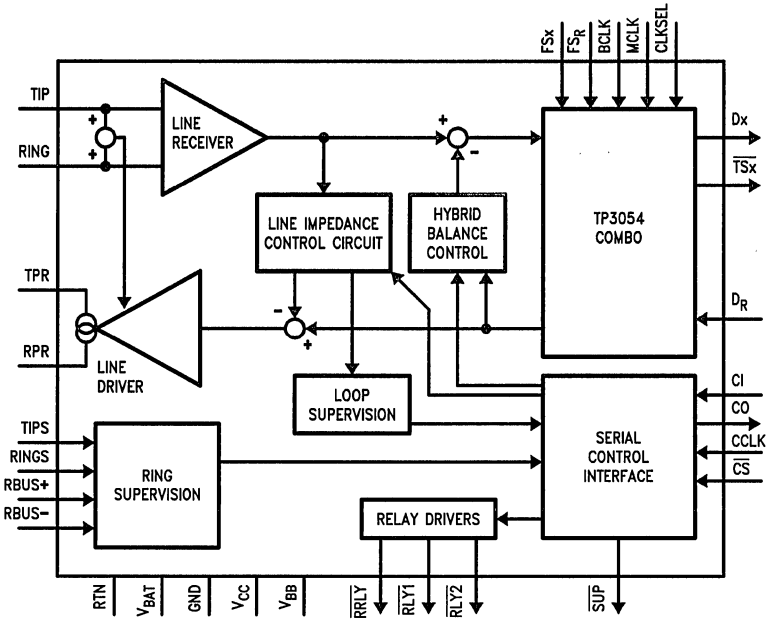
The TP3211 is a complete electronic SLIC and PCM COMBO® CODEC/Filter module intended to interface the analog subscriber line to a PCM highway. It is designed to meet the requirements for central office, Digital Loop Carrier and remote switching applications which require a 2-wire impedance of 600Ω. When used in conjunction with a simple, noncritical, external protection network, two resistors and a ring relay, the TP3211 forms a complete line circuit, handling all the BORSCHT functions.

The TP3211 module consists of a line driver, a line receiver, a line impedance control circuit, a hybrid balance circuit, a line supervision circuit, a ring supervision circuit, three positive relay drivers, a TP3054 μ-Law COMBO CODEC/Filter and a simple serial control interface circuit which is used to program and monitor the operating states of the device.

Features

- Complete COMBO CODEC/Filter and SLIC functions
- In-band on-hook transmission capability
- 600Ω two-wire line impedance
- 600Ω hybrid balance networks
- 2 x 200Ω resistive loop feed with current limit
- Power denial and battery reversal modes
- Compatible with loop start signalling
- Automatic ring trip
- Three positive relay drivers
- Thermal overload protection
- Transmission performance independent of external protection network
- Withstands 500V RTN to GND surge
- Compatible with standard PCM highway
- Small physical size and minimal external components

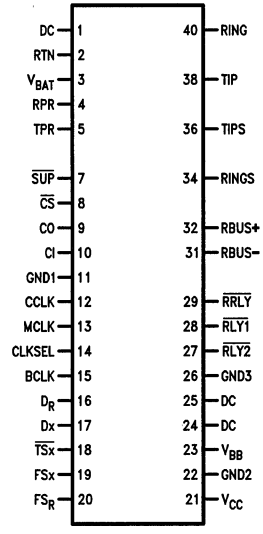
Simplified Block Diagram



TL/H/10718–1

FIGURE 1. Simplified Block Diagram

Connection Diagram



TL/H/10718–2

Top View

Order Number TP3211J
See NS Package Number HY40C

Pin Descriptions

Pin	Description
TIP	Normally positive side of the subscriber line.
RING	Normally negative side of the subscriber line.
TPR	High voltage line driver output. Connects to TIP via an external protection network.
RPR	High voltage line driver output. Connects to RING via an external protection network.
TIPS	Positive ring sensing input. Connected to the positive side of the subscriber loop during ringing.
RINGS	Negative ring sensing input. Connected to the negative side of the subscriber loop during ringing.
RBUS+	Positive ring bus sensing input. Connected to the positive side of the ring bus.
RBUS−	Negative ring bus sensing input. Connected to the negative side of the ring bus.
BCLK	Bit Clock used to shift PCM information into D_R and out of Dx. May vary from 64 kHz to 2.048 MHz in 8 kHz increments.
MCLK	Master Clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz.
CLKSEL	Master Clock select input. Must be connected high for 1.536 MHz or 1.544 MHz operation. Must be connected low for 2.048 MHz operation.
FSx	Transmit frame synchronization pulse input which enables BCLK to shift the PCM information out of Dx. FSx is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
Dx	The TRI-STATE® PCM data output which is enabled by FSx.
$\overline{TSx}$	Open drain output which pulses low during the period when the Dx output is enabled.
FS_R	Receive frame synchronization pulse input which enables BCLK to shift the PCM information into D_R. FS_R is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
D_R	Receive data input. PCM data is shifted into D_R during the receive timeslot determined by FS_R.
CCLK	Control clock used to shift control data into CI and out of CO during $\overline{CS}$ low.
$\overline{CS}$	Chip select input. Must be pulsed low to enable the shifting of control data into CI and out of CO.
CI	The serial control data input used to set the operating state of the module.
CO	The serial status output used to monitor the operating state of the module. CO is TRI-STATE when $\overline{CS}$ is high. See *Figure 3* for timing diagram.
$\overline{SUP}$	Open drain output which pulses high during on-hook, and pulses low to indicate off-hook or that the module is in ring mode.
V_{BB}	Negative power supply. Decoupled by internal 0.047 μF to ground. $V_{BB} = -5V \pm 5\%$
V_{CC}	Positive power supply. Decoupled by internal 0.047 μF to ground. $V_{CC} = 5V \pm 5\%$
$\overline{RRLY}$	Ring Relay Driver. Controlled by State Control Data Word bit D4 (see Table I). It is automatically turned off when ring trip is detected.
$\overline{RLY1}$	General purpose relay driver controlled by State Control Data Word bit D5.
$\overline{RLY2}$	General purpose relay driver controlled by State Control Data Word bit D6.

Pin Descriptions (Continued)

Pin	Description
GND1 GND2 GND3	Low voltage ground. V_{BB}, V_{CC} and all digital signals are referenced to these pins. GND1, GND2 and GND3 should be externally connected together close to the module. Collectively referenced as GND in electrical specifications.
V_{BAT}	Negative high voltage supply. $V_{BAT} = -44V$ to $-54V$
RTN	High voltage ground return. V_{BAT} and all analog signals are referenced to this pin.
DC	Don't connect. Do not make external connections to these pins.

Functional Block Description

Functional Block	Description
Line Driver	The Line Driver is a differential output transconductance amplifier which provides the d.c.power and balanced a.c. signals to the subscriber line. The d.c. power is determined by the d.c. Loop Impedance Control circuit. The a.c. signal applied to the line is controlled by the a.c. Loop Impedance Control and the analog signal generated by the TP3054 COMBO CODEC/Filter from the received PCM information. Feedback from the TIP and RING lines produces an effective longitudinal input impedance of about 200Ω from TIP and RING to RTN (100Ω total). In the presence of large longitudinal currents, each output of the Line Driver is capable of sourcing or sinking current to limit the longitudinal voltage.
Line Receiver	The Line Receiver monitors the metallic (differential) voltage on the line in the presence of large longitudinal (common mode) voltages.
Loop Impedance Control	The Loop Impedance Control feeds back the line voltage to produce a resistive/inductive d.c. feed impedance for longer loops and a constant current feed for shorter loops while maintaining an a.c. 2-wire line impedance of 600Ω over the voice band, easily meeting the 2-wire return loss requirements.
Hybrid Balance Control	The Hybrid Balance Control circuit is designed to meet the 4-wire return loss requirements for 600Ω hybrid balance testing network.
Loop Supervision	The Loop Supervision circuit monitors the d.c. current flow in the subscriber loop under non-ringing state and detects on-hook, off-hook and replicates dial pulses.
Ring Supervision	The Ring Supervision circuit monitors the d.c. current flow in the subscriber loop during the ringing state. This circuit is capable of detecting an off-hook condition in less than 200 ms in the presence of large a.c. ringing signals. It operates on loops with ringing superimposed on TIP or RING, or with balanced ringing. It supports bridged ringers, and ringers to ground on either TIP or RING.
Relay Drivers	The three relay drivers are capable of driving +5V or +12V relays directly. $\overline{RRLY}$ is dedicated to the ring relay and is automatically turned off when ring trip is detected by the Ring Supervision circuit. $\overline{RLY1}$ and $\overline{RLY2}$ are general purpose. Relay current will be returned to GND3 at pin 26.
COMBO	The COMBO provides the PCM filtering, encoding and decoding functions necessary to interface the PCM highway to the analog signals on the subscriber loop. This function is identical to the industry standard TP3054 COMBO CODEC/Filter (see the TP3054 datasheet for full details).
Control Interface	The Control Interface circuit provides easy control and monitoring of the state of the TP3211 via a simple serial interface. Via this circuit the user can program the operating mode of the module, and monitor the line status (See Table I for details).

Functional Description

Power-On

When power is first applied, the power-on reset circuitry initializes the TP3211 and places it in a standby mode. The State Control Data Word is cleared to "0". All unnecessary circuitry is powered down. The serial control interface and the loop supervision circuitry remain fully functional. The device is now ready for activation, either by the user programming it into the ring mode by writing into the State Control Data Word or by the subscriber going off-hook, powering-up the device automatically.

The State Control Data Word

The State Control Data Word is a single 8-bit word as shown in Table I. Bits D0–D7 of the control word program the operating state of the device. The module can override the control bits D2 and D3 to activate the power denial mode in order to protect itself from damage under a thermal overload condition.

Status Word

The 8-bit Status Word indicates the status of the TP3211 at the instant a read operation is performed. Table IV shows the definitions of the status word. A logic high indicates that the state or function is enabled, a low indicates that it is disabled.

The Control Interface

The Control Interface consists of a single 8-bit shift register and a buffer register. The shift register is written via the serial input CI, under the control of $\overline{CS}$ and CCLK, to program the device's operating state. Several bits of the shift register may be altered by the device itself in response to changes in the subscriber loop status. These changes in state may be read via the serial output CO. The S2 and S3 status bits are overwritten by the occurrence of a thermal overload, forcing the device into the Power-Denial mode. S7 is the hook-switch status bit. A logic "0" for S7 indicates an Off-Hook or Ring-Trip condition exists at the instant of access and a logic "1" indicates on-hook.

TABLE I. State Control Data Word

Control Bit	Description
D7	Must be programmed to logic "0". This bit is overwritten by the line supervision circuitry.
D6	Logical "1" turns on $\overline{RLY2}$.
D5	Logical "1" turns on $\overline{RLY1}$.
D4	Logical "1" enables Ring mode, turns on $\overline{RRLY}$ and Ring Supervision circuit. Status Bit S7 indicates ring trip. $\overline{SUP}$ pulses low to indicate ring mode. Logical "0" enables the normal non-ringing mode.
D3	Used with D2 to select Power Denial, Battery Reversal and On-Hook Transmission modes. See Table II. Under Power Denial mode, the Line Driver is disabled denying power to the subscriber loop. It can be set or cleared by a write operation. Under a thermal overload condition, the device will overwrite D2 to "0" and D3 to "1" in order to protect the device from damage. As long as the thermal overload condition exists, the Power Denial mode cannot be cleared by a write operation.
D2	Used with D3 to select Power Denial, Battery Reversal, and On-Hook Transmission modes. See Table II.
D1	Used with D0 to select hybrid balance network. See Table III.
D0	Used with D1 to select hybrid balance network. See Table III.

TABLE II. Operating Modes of TP3211

D4	D3	D2	Mode
0	**0**	**0**	Normal
0	0	1	Reverse Battery
0	1	0	Power Denial
0	1	1	On-Hook Transmission
1	X	X	Ring

TABLE III. Hybrid Balance Test Networks

D1	D0	Reference Test Network
0	**0**	600Ω
0	1	105Ω + (460Ω//25.5 nF)
1	0	Invalid
1	1	Invalid

Functional Description (Continued)

There are several ways to access the serial control interface. They are:

a) Write/Read

b) Read/Write

c) Quick Status Read

In the Write/Read operation, the objective is to change the state of the device. While shifting the new state control data into CI, the previous status information is shifted out of CO. This data should be compared with the previous status information to determine if a change had occurred since the last access.

In the Read/Write operation, the objective is to monitor the state of the module. While the current status is shifted out at CO, the last known state of the device is shifted into CI externally. If a thermal overload condition has occurred since the last access, the device will automatically set itself to the power-denial mode (S2 bit will be forced to "0" and S3 bit will be forced to "1") prior to the access and will be reset by writing the previous state. This has no detrimental effect, however, since the power-denial mode will immediately be set again and the device will remain in the Power-Denial mode as long as the thermal overload continues to exist. If ring trip has occurred or the hook switch status has changed since the last access, the S7 bit will also be altered by the device. The timing for the Read/Write or Write/Read modes is shown in *Figure 2*.

The Quick Status Read operation allows a fast read of the S7 status bit, which indicates if a Ring-Trip or Off-Hook condition exists. It does not cause the shift register to shift, thus no control data is required. *Figure 3* is the timing diagram for the Quick Status Read Mode.

TABLE IV. Status Information Word

Status Bit	Description
S7	Indicates switch hook status. S7 is a "1" if the subscriber is on-hook. If D4 is programmed to be "0" for normal mode, a logic "0" at S7 indicates off-hook. If the device is in the Ring mode (D4 = "1") a logic "0" at S7 indicates ring-trip.
S6	A logic "1" indicates that $\overline{\text{RLY2}}$ is on.
S5	A logic "1" indicates that $\overline{\text{RLY1}}$ is on.
S4	A logic "1" indicates Ring mode is on. $\overline{\text{RRLY}}$ is turned on, and the Ring Supervision circuit is activated. A logic "0" at S7 indicates that a ring trip has occurred, forcing $\overline{\text{RRLY}}$ to be deactivated. D4 should be cleared to "0" by a write/read operation in order to program the device into the normal mode.
S3	S2 and S3 indicate Power-Denial, Battery Reversal and On-Hook Transmission modes. See Table II. When an overload condition exists which raises the junction temperature to exceed about 170°C, the TP3211 will automatically initialize a power denial mode (S2 forced to "0" and S3 forced to "1") to protect itself from damage. The device will not go back to the normal mode even if the thermal overload ceased to exist. The system can determine if the thermal overload condition has cleared itself by programming the TP3211 into the desired operating mode and read back status bits S2 and S3. If the overload still exists, the power denial mode will be activated again as long as the device's junction temperature exceeds approximately 170°C.
S2	S2 and S3 indicate Power-Denial, Battery Reversal and On-Hook Transmission modes. See Table II.
S1	S0 and S1 indicate the selected hybrid balance test network. See Table III.
S0	S0 and S1 indicate the selected hybrid balance test network. See Table III.

Functional Description (Continued)

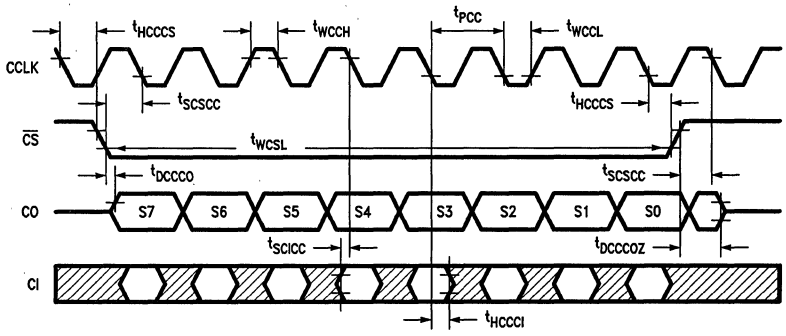


FIGURE 2. Control Interface Timing—Read/Write, Write/Read Modes

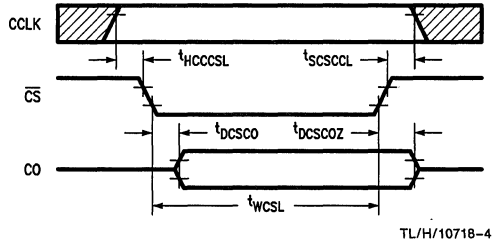


FIGURE 3. Control Interface Timing—Quick Status Read Mode

Battery Feed

With V_{BAT} = −48V, the TP3211 provides a nominal apparent battery voltage of −40V across TIP and RING. The module provides a 2 x 200Ω resistive feed at longer loops. The d.c. current feed has been designed to guarantee at least 15 mA into an 1800Ω loop. At short loops, the d.c. feed is current-limited to nominally 60 mA. The DC feed characteristic is shown in *Figure 4*. In normal battery mode (D2 = 0 and D3 = 0), TIP is more positive than RING.

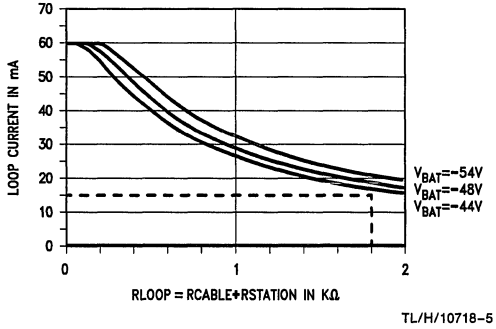


FIGURE 4. DC Feed Characteristics

2-Wire Impedance

The TP3211 module simulates a 2-wire input impedance of 600Ω across TIP and RING. This is shunted by the feeding inductance which is nominally 35 Henries on long loops, and approaches infinity on short loops. The 2-wire impedance is independent of the external protection resistors.

Transmission Level

The TLP on the 2-wire analog interface is 0, that is, 0 dB is 1 mW into 600Ω for both transmit and receive signals.

Hybrid Balance

The TP3211 contains two selectable hybrid balance circuits which are selected by programming control bits D0 and D1 (see Table III). The hybrid balance circuits are intended to be used with the corresponding reference testing networks terminating TIP and RING.

Longitudinal Balance and Longitudinal Current Capability

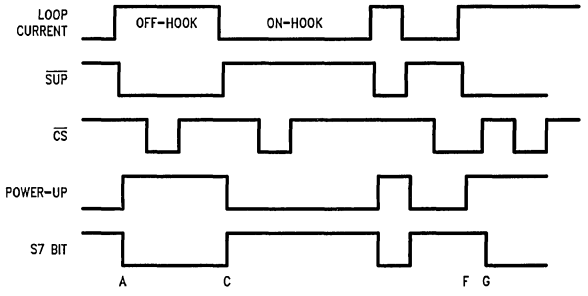
The 2-wire input of the device exhibits a longitudinal impedance of 200Ω from TIP to ground and from RING to ground. These impedances are extremely well matched and are not strongly dependent on impedance matching in the external protection network. The longitudinal voltage is sensed on the loop side of the protection network and fed back to the Line Driver, thus any component variations external to the device can be corrected by the feedback loop. The Line Driver is capable of handling 21 mA_{rms} of longitudinal current in each of the TIP and RING leads.

Loop Supervision

The Loop Supervision circuit operates in the normal (nonringing) state. Control bit D7 must be programmed to logic "0". Off-hook is indicated when the loop current exceeds nominally 13 mA and on-hook indicated when the current falls below nominally 11 mA, providing 2 mA hysteresis. The loop supervision has been designed to operate with loop-start signalling and to maintain the dial pulse make interval greater than 16 ms or break interval greater than 32 ms regardless of the distortion introduced by the loop characteristics. A logic "1" at status bit S7 indicates on-hook, while a logic "0" indicates off-hook.

A typical example of hook switch timing is illustrated in *Figure 5*. While in the standby mode, all unnecessary circuitry is powered down. When Loop Supervision detects off-hook, the module is powered up, $\overline{SUP}$ goes low and status bit S7 is cleared (A). When the Loop Supervision detects on-hook, all unnecessary circuitry is again powered down, status bit S7 is set and $\overline{SUP}$ is again set high (C). If the device's control interface is being accessed when off-hook occurs, i.e., $\overline{CS}$ is low, $\overline{SUP}$ is set low immediately (F) but S7 is cleared only after $\overline{CS}$ returns high (G). On the next Read/Write access, S7 is latched.

Functional Description (Continued)



TL/H/10718-6

FIGURE 5. Typical Hook Switch Detect Timing

Ring Supervision

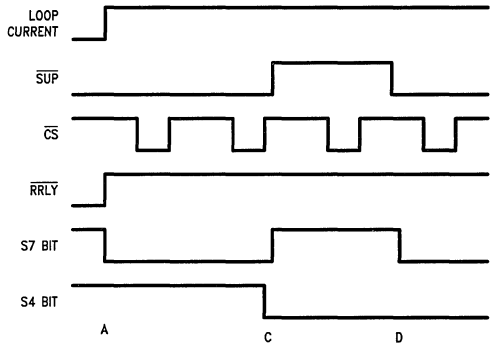
The Ring Supervision circuit measures the loop current across two 360Ω ring sensing resistors with a 1 MΩ internal precision bridge (see *Figure 10*). The voltage at the output of the bridge is filtered, then algebraically added and subtracted from a voltage corresponding to a loop current of about 11 mAdc. Each of the resulting voltages are integrated over one period of the ring frequency and compared to zero. If either of the resulting voltages is less than zero for two consecutive cycles, Ring-Trip is detected. $\overline{\text{RRLY}}$ is deactivated, and status bit S7 is cleared to "0" indicating ring trip. Control bit D4 is not automatically reset to "0", it has to be cleared to "0" by a write/read operation after a ring trip is detected. If the MCLK is interrupted and stays continuously high or low for more than 200 μs, the ring relay driver will be turned off.

The ring supervision circuit works with zero to three bridged ringers (1 ringer = 4 kΩ at 20 Hz), with ring frequencies from 16 Hz to 67 Hz, with ring voltages up to 155 Vrms applied to either TIP or RING, superimposed on positive or negative battery voltages of from 42V to 56V on loops up to 1700Ω. Furthermore, it operates with up to three ringers connected from TIP or RING to ground. The ring sensing inputs, TIPS, RINGS, RBUS+ and RBUS−, when connected as shown in *Figure 10*, will present an effective load of about 500 kΩ across the ring bus.

A typical example of ring trip timing is illustrated in *Figure 6*. During ring mode when D4 is set to "1", $\overline{\text{SUP}}$ pulses low indicating ring mode. When the Ring Supervision circuit detects a ring trip, the device immediately turns off $\overline{\text{RRLY}}$ and clears S7 (A). Status bit S7 will remain a zero until the D4 bit is written to a zero, removing the device from the Ring mode (C). At this time, the S7 bit and $\overline{\text{SUP}}$ will indicate the switch hook status. Even though the station equipment is normally off-hook at this time, S7 and $\overline{\text{SUP}}$ wll generally return to a "1" for several milliseconds (C) after D4 is cleared. This is because the Loop Supervision circuit was disconnected from the loop during ringing mode (D4 = 1), and it takes several milliseconds to detect the off hook at which time S7 wll be cleared and $\overline{\text{SUP}}$ will be set low (D). At this point the device is in the normal (non-ringing) mode, all necessary circuitry is powered up.

Thermal Overload

The Line Driver incorporates a built-in thermal overload detection circuitry. In the event of a fault on the subscriber line which causes the Line Driver to reach an internal junction temperature of approximately 170°C, the Line Driver will protect itself by forcing the device into the power-denial mode (D2 is forced to "0" and D3 is forced to "1"). The device will remain at the power denial mode even though the thermal overload ceases to exist. After the line fault has been corrected, the device can be put back into service under system control (see Table IV).



TL/H/10718-7

FIGURE 6. Typical Ring Trip Detect Timing

Functional Description (Continued)

A typical example of thermal overload detection timing is illustrated in *Figure 7*. When a thermal overload is detected, S2 is set low and S3 is set high (A), forcing the device into the Power-Denial mode. As long as the thermal overload condition exists, the power denial mode cannot be reset by a write operation (B). When the thermal overload condition clears, the device continue to remain at power denial mode (C). Thus the device does not automatically reapply power to the line since the fault that originally caused the failure may still exist and would simply cause the overload to reoccur. In this example, the power-denial mode is cleared by a control write to normal mode, clearing S2 to "0" and S3 to "0" (D). If the device is being accessed at the instant the thermal shutdown occurs, S2 will be set low and S3 will be set high only after $\overline{CS}$ returns high (E).

On-Hook Transmission Mode

The device is in the on-hook transmission mode when bits D3 and D2 of the State Control Data Word are set to the logic "1" and the loop is under "on-hook". In this mode, the line drivers operate in a reduced power state but all circuitry is active. This enables the system to communicate with a subscriber terminal or the subscriber to communicate through the network or to a terminal in the central office to provide alarm and telemetry services. When the loop goes off-hook, the loop supervision circuitry behaves normally and causes the line drivers to power up. Bit S7 of the Status Information Word is cleared and $\overline{SUP}$ pulses low. This enables the system to terminate any transmissions and handle the call initiation in the normal manner.

PCM Interface

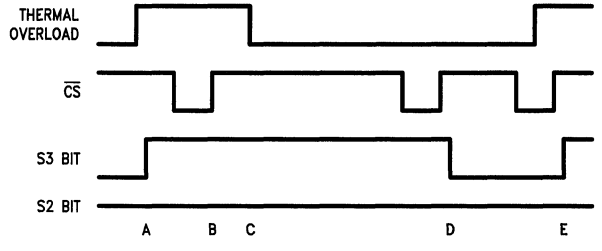
The PCM interface consists of inputs MCLK, BCLK, FSx, FS_R and D_R, and outputs Dx and $\overline{TSx}$. MCLK controls the internal operation of the COMBO CODEC/Filter's encoder and decoder, and must be 1.536 MHz or 1.544 MHz if CLKSEL is connected high and 2.048 MHz if CLKSEL is connected low. BCLK shifts the PCM data out of Dx on its rising edge and latches the PCM data into D_R on its falling edge. It must be synchronous with MCLK and may be any integer multiple of 8 kHz from 64 kHz to 2.048 MHz. FSx and FS_R are 8 kHz pulse waveforms which determine the beginning of the PCM data transfer out of Dx and into D_R respectively. Both must be synchronous with MCLK but may have any phase relationship with each other. $\overline{TSx}$ is an open drain output which pulses low for the duration of the data transfer out of Dx. It is intended to be wire-ORed with the $\overline{TSx}$ outputs of other subscriber line interface modules to provide an enable signal for external TRI-STATE drivers buffering the PCM transmit data from a line card onto the backplane.

Short Frame Sync Operation

The TP3211 Subscriber Line Interface Module can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, the frame sync pulses applied to both FSx and FS_R must be one BCLK period long and with timing relationships as specified in *Figure 8*. With FSx high during a falling edge of BCLK, the next rising edge of BCLK enables the Dx TRI-STATE output buffer, which will output the PCM sign bit. The following seven rising edges of the bit clock shifts out the remaining seven bits of PCM data, MSB first. The next falling edge disables the Dx output. With FS_R high during a falling edge of BCLK, the next falling edge latches the PCM sign bit into D_R. The next seven falling edges latch the remaining seven bits, MSB first.

Long Frame Sync Operation

To use the long frame sync mode, the frame sync pulses applied to both FSx and FS_R must be three or more bit periods long, with timing relationships as specified in *Figure 9*. Based on the transmit frame sync pulse, the device will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The Dx TRI-STATE output buffer is enabled with the rising edge of FSx or the rising edge of BCLK, whichever comes later, and the first bit clocked out is the PCM sign bit. The following seven rising edges of BCLK shift out the remaining seven bits, MSB first. The Dx output is disabled by the falling edge of BCLK following the eighth rising edge or by FSx going low, whichever comes later. A rising edge of the receive frame sync will cause PCM data at D_R to be latched in on the next eight falling edges of BCLK.



TL/H/10718–8

FIGURE 7. Typical Thermal Overload Detection Timing

Functional Description (Continued)

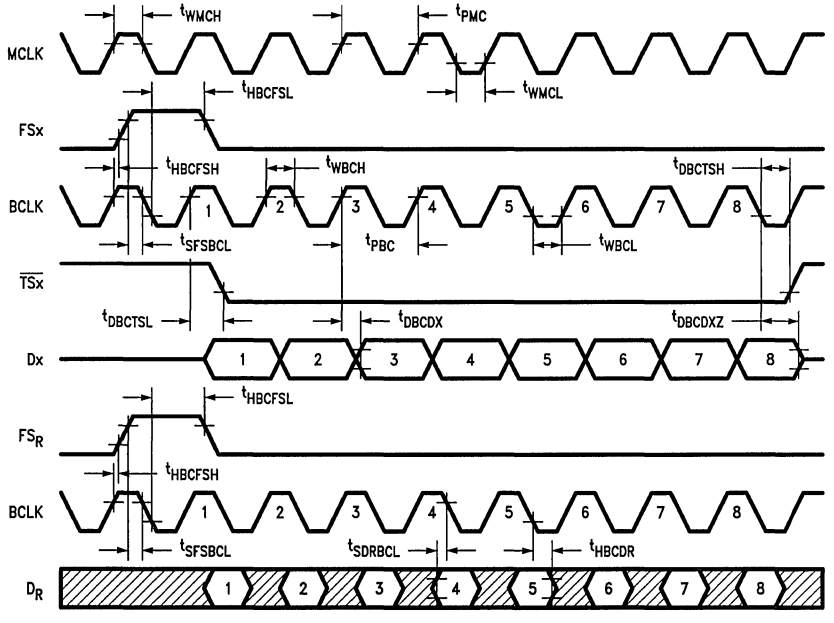


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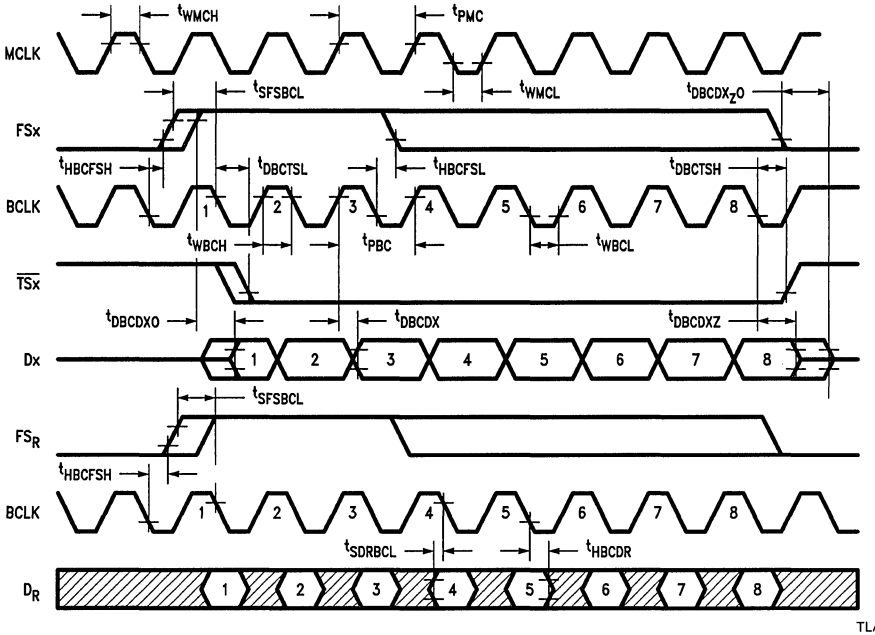
FIGURE 8. Timing Diagram for Short Frame Mode



TL/H/10718–10

FIGURE 9. Timing Diagram for Long Frame Mode

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	−0.5V to 7V
V_{BB} to GND	+0.5V to −7V
V_{BAT} to RTN	+0.5V to −70V
RTN to GND	±500V, 10 μs/50 μs Pulse
Voltage at Any Digital Input or Output	V_{CC} + 0.3V to GND − 0.3V
TPR, RPR to RTN	2V to −85V (50 ms)
TIP, RING, TIPS, RINGS, RBUS+, RBUS−, to RTN	±1000V, 10 μs/1000 μs Pulse
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 Sec.)	300°C
Maximum Junction Temperature	150°C

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −44V to −54V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −48V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (Normal Mode: D2 = 0, D3 = 0)						
I_{BAT0}	V_{BAT} Idle Current	I_{Loop} = 0 mA, V_{BAT} = −48V		2.1	**3.5**	mA
I_{BB0}	V_{BB} Idle Current	I_{Loop} = 0 mA		1.5	**3.5**	mA
I_{CC0}	V_{CC} Idle Current	I_{Loop} = 0 mA		2.5	**4.5**	mA
I_{BAT1}	V_{BAT} Active Current	I_{Loop} = 20 mA, V_{BAT} = −48V		23	**25**	mA
I_{BB1}	V_{BB} Active Current	I_{Loop} = 20 mA		8.9	**15.2**	mA
I_{CC1}	V_{CC} Active Current	I_{Loop} = 20 mA		11.8	**15.2**	mA
POWER DISSIPATION (On-Hook Transmission Mode: D2 = 1, D3 = 1)						
I_{BAT0H}	V_{BAT} Idle Current	I_{Loop} = 0 mA, V_{BAT} = −48V		2.1	**3.5**	mA
I_{BB0H}	V_{BB} Idle Current	I_{Loop} = 0 mA		8.9	**15.2**	mA
I_{CC0H}	V_{CC} Idle Current	I_{Loop} = 0 mA		11.8	**15.2**	mA
DIGITAL INTERFACE (Note 1)						
V_{IL}	Input Low Level				**0.7**	V
V_{IH}	Input High Level	All Digital Input except CLKSEL CLKSEL	**2** **4**			V V
V_{OL}	Output Low Level	Dx, $\overline{TSx}$, CO, I_L = 3.2 mA $\overline{SUP}$, I_L = 2.0 mA			**0.4** **0.4**	V V
V_{OH}	Output High Level	Dx, CO, I_H = −3.2 mA	**2.4**			V
I_{IL}	Input Low Current	GND < V_{IN} < V_{IL}, All Digital Inputs	**−100**		**100**	μA
I_{IH}	Input High Current	V_{IH} < V_{IN} < V_{CC}, All Digital Inputs	**−100**		**100**	μA
I_{OH}	Output High Current	$\overline{TSx}$ and $\overline{SUP}$, V_{OH} < V_{OUT} < V_{CC}	**−100**		**100**	μA
I_{OZ}	Leakage Current in the High Impedance State	CO, Dx	**−100**		**100**	μA

Note 1: See Appendix I for the definition of digital interface parameters.

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −44V to −54V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −48V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BATTERY FEED						
I_{Loop+}	Loop Current	R_{Loop} = 1800Ω R_{Loop} = 1200Ω R_{Loop} = 200Ω	**15** **50**	18.1 25 60	**25** **65**	mA mA mA
I_{Loop-}	Battery Reversal Loop Current	R_{Loop} = 1800Ω R_{Loop} = 1200Ω R_{Loop} = 200Ω	**15** **50**	18.1 25 60	**25** **65**	mA mA mA
I_{PD}	Power Denial Loop Current	R_{Loop} = 200Ω		0.1	**2**	mA
V_{Loop}	Loop Voltage	R_{Loop} = 10 kΩ		−38.4		V
LOOP SUPERVISION						
R_{offhk0}	Loop Resistance to Produce an Off-Hook Indication	R_{offhk0} Connected from TIP to RING			**2200**	Ω
R_{onhk0}	Loop Resistance to Produce an On-Hook Indication	R_{onhk0} Connected from TIP to RING	**9**			kΩ
DPD	Dial Pulse Distortion	D7 = 0, R_{Leak} = 20 kΩ ‖ 2 μF, R_{Loop} = 200Ω, 12 pps, Break = 50% R_{Loop} = 1800Ω, 12 pps, Break = 75% $\overline{CS}$ High, Measure width of $\overline{SUP}$ pulse low	 **18** **18**		 **49.3** **49.3**	 ms ms
RING SUPERVISION						
RNGTRP1	Ring Trip Detect, Normal Ringing	RBUS+ = 0V, RBUS− = −48V, TIPS = −5V, RINGS = −43V, Must Detect Ring-Trip within Specified Time	**50**		**180**	ms
RNGTRP3	Ring Trip Non-Detect Normal Ringing	RBUS+ = 0V, RBUS− = −48V TIPS = −3V, RINGS = −45V, Must Not Detect Ring Trip within the Specified Time (Note 2)	**0**		**180**	ms
RNGTRP5	Ring Trip Detect, Normal Ringing	TIPS, RBUS− = −5V, RINGS, RBUS+ = 26 Vrms, f = 20 Hz. Must Detect Ring-Trip within the Specified Time	**100**		**190**	ms
RNGTRP7	Ring Trip Non-Detect Normal Ringing	TIPS, RBUS− = −3V, RINGS, RBUS+ = 26 Vrms. f = 20 Hz. Must Not Detect Ring-Trip within the Specified Time (Note 2)	**0**		**190**	ms
HYBRID BALANCE Unless Otherwise Specified, I_{Loop} = 20 mA, D2 = 0, D3 = 0						
ECH01	4-Wire Return Loss	Z_{REF} = 600Ω Across Tip-Ring I_{Loop} = 20 mA, D1 = 0, D0 = 0 f = 296.875 Hz = 484.375 Hz = 1015.625 Hz = 2500 Hz = 3406.25 Hz	 **20** **26** **26** **26** **20**	 40 	 	 dB dB dB dB dB
ECH02	4-Wire Return Loss	Z_{REF} = 105Ω + (460Ω//25.5 nF) Across Tip-Ring I_{Loop} = 20 mA, D1 = 0, D0 = 1 f = 296.875 Hz = 484.375 Hz = 1015.625 Hz = 2500 Hz = 3406.25 Hz	 **20** **26** **26** **26** **20**	 40 	 	 dB dB dB dB dB

Note 2: The intent of Ring-Trip Non-Detect tests are to insure that ring-trip does not occur under the specified conditions even after an essentially infinite period of time. For practical purposes of cost effectively testing the SLIM Subscriber Line Interface Module, the wait time to determine that a false ring-trip has not occurred has necessarily been limited to a value which has been determined through characterization to insure that false ring-trip never occurs.

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −44V to −54V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −48V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless Otherwise Noted, Z_{REF} = 600Ω, f = 1015.625 Hz, I_{Loop} = 20 mA, D2 = 0, D3 = 0						
RTNLOSS	2-Wire Return Loss	f = 296.875 Hz = 484.375 Hz = 1015.625 Hz = 2500 Hz = 3406.25 Hz	**20** **26** **26** **26** **26**	 40 	 	dB dB dB dB dB
0 dBmO	The Absolute 2-Wire Reference Level	The Absolute Reference Level at the 2-Wire Interface is Defined as 0dBm into 600Ω		0.775		Vrms
GRA	Absolute Receive Gain	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −48V from D_R to 2-Wire Analog Interface, T_A = 25°C, Input = Digital Code for 0dBmO at D_R, Measure Voltage across TIP-RING	**−0.25**	0	**0.25**	dB
GXA	Absolute Transmit Gain	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −48V from 2-Wire Analog Interface to Dx, T_A = 25°C, Input = 0dBmO at 2-Wire Port, Measure Digital Code at Dx	**−0.25**	0	**0.25**	dB
GRA0H	Absolute Receive Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −48V T_A = 25°C, Z_{REF} = 600Ω I_{Loop} = 0 mA, D2 = 1, D3 = 1	**−1**	0	**1**	dB
GXA0H	Absolute Transmit Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −48V T_A = 25°C, I_{Loop} = 0 mA, D2 = 1, D3 = 1	**−1**	0	**1**	dB
GRAV	Absolute Receive Gain over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%, V_{BAT} = −44V to −54V	**−0.3**	0	**0.3**	dB
GXAV	Absolute Transmit Gain over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%, V_{BAT} = −44V to −54V	**−0.3**	0	**0.3**	dB
GRT	Receive Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −48V Reference to GRA	−0.1		0.1	dB
GXT	Transmit Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −48V, Reference to GXA	−0.1		0.1	dB
GRF	Receive Frequency Response	Measure Relative to GRA, f = 203.125 Hz = 296.875 Hz = 484.375 Hz = 2015.625 Hz = 2703.125 Hz = 3015.625 Hz = 3203.125 Hz = 3390.625 Hz = 3984.375 Hz	 **−1.9** **−0.6** **−0.25** **−0.25** **−0.25** **−0.25** **−0.25** **−1.2**		 **0** **0.25** **0.25** **0.25** **0.25** **0.25** **0.25** **0** **−14**	 dB dB dB dB dB dB dB dB dB
SOS	Spurious Out of Band Signals (Alias Tones)	Measure Relative to GRA, f = 4796.875 Hz = 6703.125 Hz = 11390.625 Hz			 **−30** **−30** **−30**	 dB dB dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −44V to −54V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −48V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless Otherwise Noted, Z_{REF} = 600Ω, f = 1015.625 Hz, I_{Loop} = 20 mA, D2 = 0, D3 = 0 (Continued)						
GXF	Transmit Frequency Response	Measure Relative to GXA, f = 62.500 Hz			**−22**	dB
		= 203.125 Hz	**−2.5**		**0**	dB
		= 296.875 Hz	**−0.4**		**0.25**	dB
		= 484.375 Hz	**−0.25**		**0.25**	dB
		= 2015.625 Hz	**−0.25**		**0.25**	dB
		= 2703.125 Hz	**−0.25**		**0.25**	dB
		= 3015.625 Hz	**−0.25**		**0.25**	dB
		= 3203.125 Hz	**−0.25**		**0.25**	dB
		= 3390.625 Hz	**−1.2**		**0**	dB
		= 3984.375 Hz			**−14**	dB
		= 5046.875 Hz			**−32**	dB
		= 11890.625 Hz			**−32**	dB
GRL	Receive Gain Variation with Signal Level	Measure Relative to GRA PCM Level = 3.1 dBmO	**−0.25**		**0.25**	dB
		= −2.3 dBmO	**−0.25**		**0.25**	dB
		= −11.4 dBmO	**−0.25**		**0.25**	dB
		= −17.6 dBmO	**−0.25**		**0.25**	dB
		= −23.9 dBmO	**−0.25**		**0.25**	dB
		= −29.9 dBmO	**−0.25**		**0.25**	dB
		= −37.8 dBmO	**−0.25**		**0.25**	dB
		= −47.1 dBmO	**−0.45**		**0.45**	dB
		= −55.7 dBmO	**−1.3**		**1.3**	dB
GXL	Transmit Gain Variation with Signal Level	Measure Relative to GXA PCM Level = 3.1 dBmO	**−0.25**		**0.25**	dB
		= −2.3 dBmO	**−0.25**		**0.25**	dB
		= −11.4 dBmO	**−0.25**		**0.25**	dB
		= −17.6 dBmO	**−0.25**		**0.25**	dB
		= −23.9 dBmO	**−0.25**		**0.25**	dB
		= −29.9 dBmO	**−0.25**		**0.25**	dB
		= −37.8 dBmO	**−0.25**		**0.25**	dB
		= −47.1 dBmO	**−0.45**		**0.45**	dB
		= −55.7 dBmO	**−1.3**		**1.3**	dB
STDR	Receive Signal to Total Distortion	Measure through C Message Filter, PCM Level = 3.1 dBmO	**33**			dBC
		= 0 dBmO	**36**			dBC
		= −11.4 dBmO	**36**			dBC
		= −17.6 dBmO	**36**			dBC
		= −29.9 dBmO	**35**			dBC
		= −40.0 dBmO	**29**			dBC
		= −45.0 dBmO	**25**			dBC
		= −55.7 dBmO	**14**			dBC
STDX	Transmit Signal to Total Distortion	Measure through C Message Filter, PCM Level = 3.1 dBmO	**33**			dBC
		= 0 dBmO	**36**			dBC
		= −11.4 dBmO	**36**			dBC
		= −17.6 dBmO	**36**			dBC
		= −29.9 dBmO	**35**			dBC
		= −40.0 dBmO	**29**			dBC
		= −45.0 dBmO	**25**			dBC
		= −55.7 dBmO	**13**			dBC

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −44V to −54V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −48V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless Otherwise Noted, Z_{REF} = 600Ω, f = 1015.625 Hz, I_{Loop} = 20 mA, D2 = 0, D3 = 0 (Continued)						
DRA	Absolute Receive Delay	f = 1600 Hz		190		μs
DRR	Receive Delay Distortion	Measure Relative to DRA, f = 500 Hz = 1000 Hz = 2600 Hz = 2800 Hz = 3000 Hz		 −2 −10 70 100 150		 μs μs μs μs μs
DXA	Absolute Transmit Delay	f = 1600 Hz		300		μs
DXR	Transmit Delay Distortion	Measure Relative to DXA, f = 500 Hz = 600 Hz = 800 Hz = 1000 Hz = 2600 Hz = 2800 Hz = 3000 Hz		 250 150 65 30 60 80 140		 μs μs μs μs μs μs μs
NOISE Z_{REF} = 600Ω, I_{Loop} = 20 mA, D2 = 0, D3 = 0						
NRC	Receive C Message Weighted Idle Channel Noise	PCM Code is Alternating Positive and Negative Zeroes			**15**	dBrnC0
NXC	Transmit C Message Weighted Idle Channel Noise	Measured by Extrapolation from Signal to Distortion Measurements about −50 dBmO			**20**	dBrnC0
LONGITUDINAL BALANCE AND CAPABILITY						
I_{LLS1}	Longitudinal Current Capability	Z_{Loop} = 20 kΩ ‖ 2 μF, f = 60 Hz, D7 = 0 Inject I_{LLS1} into TIP and RING. Device must not detect off-hook.	**21**			mArms
I_{LLS2}	Longitudinal Current Capability	Z_{Loop} = 1.8 kΩ, f = 60 Hz, D7 = 0 Inject I_{LLS2} into TIP and RING. Device must not detect off-hook.	**21**			mArms
BAL2W	2-Wire Longitudinal Balance	IEEE Method 455-1976, I_{Loop} = 20 mA $I_{Longitudinal}$ = 20 mArms/leg, Measure $V_{Metallic}$ across TIP-RING f = 62.5 Hz = 296.875 Hz = 1015.625 Hz = 3000 Hz = 3406.25 Hz	 **61** **61** **61** **54** **51**	 64 59 		 dB dB dB dB dB
POWER SUPPLY REJECTION RATIO Unless Otherwise Specified, Z_{REF} = 600Ω, I_{LOOP} = 20 mA, D2 = 0, D3 = 0						
$PPSR_R$	V_{CC} Power Supply Rejection, Receive	V_{CC} = 5.0 V_{DC} + 164 mVrms f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	 **30** **30** **30**			 dB dB dB
$VPSR_R$	V_{BAT} Power Supply Rejection, Receive	V_{BAT} = −48.0 V_{DC} + 424 mVrms f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	 **30** **40** **40**			 dB dB dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −44V to −54V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −48V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER SUPPLY REJECTION RATIO Unless Otherwise Specified, Z_{REF} = 600Ω, I_{LOOP} = 20 mA, D2 = 0, D3 = 0 (Continued)						
PPSRx	V_{CC} Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 164 mVrms f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	 **30** **30** **30**			 dB dB dB
VPSRx	V_{BAT} Power Supply Rejection, Transmit	V_{BAT} = −48.0 V_{DC} + 424 mVrms f = 328.125 Hz f = 1078.125 Hz f = 3328.125 Hz	 **30** **40** **40**			 dB dB dB
RELAY DRIVERS						
V_{RON}	Driver On Voltage	I_L = 80 mA			**1.0**	V
I_{Roff}	Leakage Current	V_{RELAY} = 40V, Relay Off			**100**	μA
DIGITAL TIMING, PCM INTERFACE (See *Figures 8* and *9*, Notes 4 and 5)						
$1/t_{PMC}$	MCLK Frequency	Clock Frequency Accuracy < ±100 ppm		1.536 1.544 **2.048**		MHz MHz MHz
t_{WMCH}	Width of MCLK High		**160**			ns
t_{WMCL}	Width of MCLK Low		**160**			ns
$1/t_{PBC}$	BCLK Frequency				**2.048**	MHz
t_{WBCH}	Width of BCLK High		**160**			ns
t_{WBCL}	Width of BCLK Low		**160**			ns
SHORT FRAME SYNC MODE *(Figure 8)*						
t_{SFSBCL}	Setup Time from FS High to BCLK Low		**50**			ns
t_{HBCFSL}	Hold Time from BCLK Low to FS Low		**100**			ns
t_{HBCFSH}	Hold Time from BCLK Low to FS High		**0**			ns
t_{DBCDX1}	Delay Time from Bit Clock to Dx Data Value	C_L = 150 pF Plus 2 LSTLL Loads	**0**		**140**	ns
t_{DBCDXz}	Delay Time from BCLK to Dx Disable	C_L = 50 pF	**50**		**165**	ns
t_{DBCTSL}	Delay Time from BCLK to $\overline{TSx}$ Low	C_L = 150 pF Plus 2 LSTTL Loads			**140**	ns
t_{SDRBCL}	Setup Time from D_R to BCLK Low		**50**			ns
t_{HBCDR}	Hold Time from BCLK Low to D_R Valid		**50**			ns
LONG FRAME SYNC MODE *(Figure 9)*						
t_{HBCFSH}	Hold Time from BCLK Low to FS		**0**			ns
t_{SFSBC0}	Setup Time from FS to BCLK Low		**80**			ns
t_{WFSL}	Width of FS Low		**160**			ns

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −44V to −54V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −48V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LONG FRAME SYNC MODE *(Figure 9)* (Continued)						
t_{DBCDX0}	Delay Time from BCLK or FS, Whichever Comes Later to Dx Valid	C_L = 150 pF Plus 2 LSTTL Loads	**20**		**165**	ns
t_{DBCDX}	Delay Time from BCLK to Dx Valid	C_L = 150 pF Plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBCDXz}	Delay Time from BCLK to Dx Disabled	C_L = 50 pF	**50**		**165**	ns
$t_{DBCDXz0}$	Delay Time from BCLK or FS, Whichever Comes Later, to Dx Disabled	C_L = 50 pF	**20**		**165**	ns
t_{SDRBC}	Setup Time from D_R to BCLK Low		**50**			ns
t_{HBCDR}	Hold Time from BCLK Low to D_R Valid		**50**			ns
DIGITAL TIMING, CONTROL INTERFACE (See *Figures 2* and *3*, Notes 4 and 5)						
$1/t_{PCC}$	CCLK Frequency	Frequency Accuracy < ±100 ppm	0.08		**2.048**	MHz
t_{WCCH}	Width of CCLK High		**200**			ns
t_{WCCL}	Width of CCLK Low		**200**			ns
t_{WCSL}	Width of $\overline{CS}$ Low				**100**	µs
READ/WRITE, WRITE READ MODES *(Figure 2)*						
t_{HCCCS}	Hold Time from CCLK to $\overline{CS}$		**100**			ns
t_{SCSCC}	Setup Time from $\overline{CS}$ to CCLK		**100**			ns
t_{DCCCO}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Valid	C_L = 150 pF Plus 2 LSTTL Loads			**150**	ns
t_{DCCCOZ}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Disabled				**150**	ns
t_{SCICC}	Setup Time from CI to CCLK		**100**			ns
t_{HCCCI}	Hold Time from CCLK to CI		**100**			ns
QUICK STATUS READ MODE *(Figure 3)*						
t_{HCCCSL}	Hold Time from CCLK to $\overline{CS}$ Low		**100**			ns
t_{SCSCCL}	Setup Time from $\overline{CS}$ to CCLK Low		**100**			ns
t_{DCSCO}	Delay Time from $\overline{CS}$ to CO	C_L = 150 pF Plus 2 LSTTL Loads			**150**	ns
t_{DCSCOZ}	Delay Time from $\overline{CS}$ to CO Disabled				**150**	ns

Note 4: See Appendix I for the definition and naming conventions used for digital timing parameters.

Note 5: See Table IV for the definition of the mneumonics used for the digital timing parameters.

TABLE IV. Timing Parameter Mneumonics

Pin Name	Mneumonic
$\overline{CS}$	CS
CO	CO
CI	CI
CCLK	CC
MCLK	MC
BCLK	BC
D_R	DR
Dx	DX
$\overline{TSx}$	TS
FS_R	FS
FSx	FS

Applications Information

Typical Line Circuit

Relatively few external components are required to implement a full featured central office line circuit. As shown in *Figure 10*, a complete line circuit is implemented using TP3211 with an external protection network consisting of fuse resistors R_{TIP} and R_{RING}, and a voltage clamp device, two 360Ω ring sensing resistors, a ring relay and two test relays. It should be noted that no supply decoupling capacitors are required for each line circuit, although the use of one larger electrolytic capacitor may be advisable for each power supply near the point at which it enters the line card.

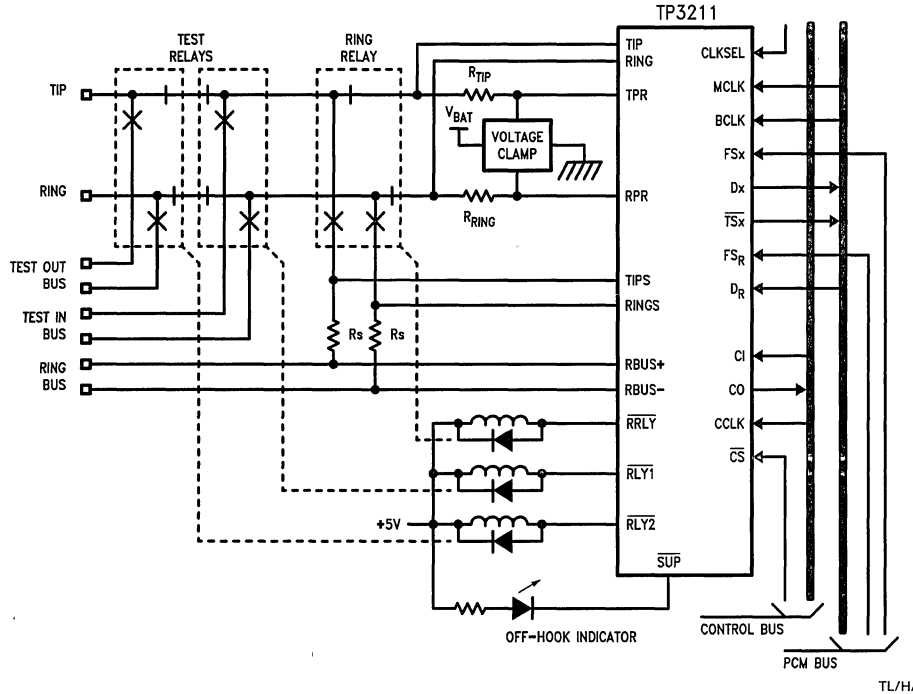
Protection fuse resistors R_{TIP} and R_{RING} should be nominally 150Ω. Mismatch of R_{TIP} and R_{RING} to within ±1% will not cause degradation in longitudinal balance. The selection of these fuse resistors is important because they are fundamental to the ability of the line circuit to meet lightning and power cross requirements. R_{TIP} and R_{RING} should be designed such that they can withstand level one lightning and power cross requirements, while fusing open when overstressed by level two lightning and power cross. The ring sensing resistors, R_S, are 360Ω which sets the ring trip threshold to about 11 mAdc. The heavy relay current will be returned to GND3 at pin 26. The $\overline{SUP}$ is capable to sink 2 mA nominal and can be used to drive a high efficient LED as a hook-switch indicator.

Secondary Protection

The surge protection network in *Figure 10* consists of resistors R_{TIP}, R_{RING} and a voltage limiting circuit which limits the voltage at TPR and RPR to within +2V to −85V. A number of low cost possibilities for this voltage limit are shown in *Figure 11*. The lowest cost solution is a simple full wave rectifier diode bridge used to clamp the voltage to no more than one or two volts above RTN or below V_{BAT}, provided that the V_{BAT} supply is capable to absorb the power surges. The TIP and RING input terminals of the TP3211 are internally connected in series to two 300 kΩ thick film resistors, which are capable to withstand power cross and surges.

Typical Line Card

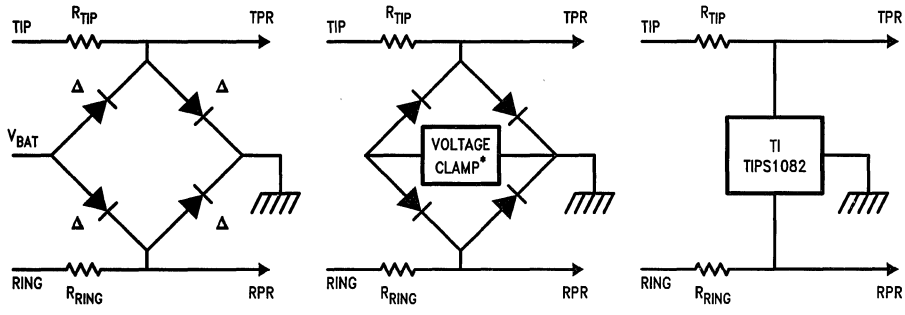
A complete n-channel line card is illustrated in *Figure 12*. The backplane control interfaces vary greatly in different applications, and this example illustrates a possible arrangement.



TL/H/10718–11

FIGURE 10. Complete Central Office Line Circuit

Applications Information (Continued)



Δ2A, 100V
20A Surge

*SGS L5060
Thomson TPC68B

FIGURE 11. Some Secondary Protection Networks

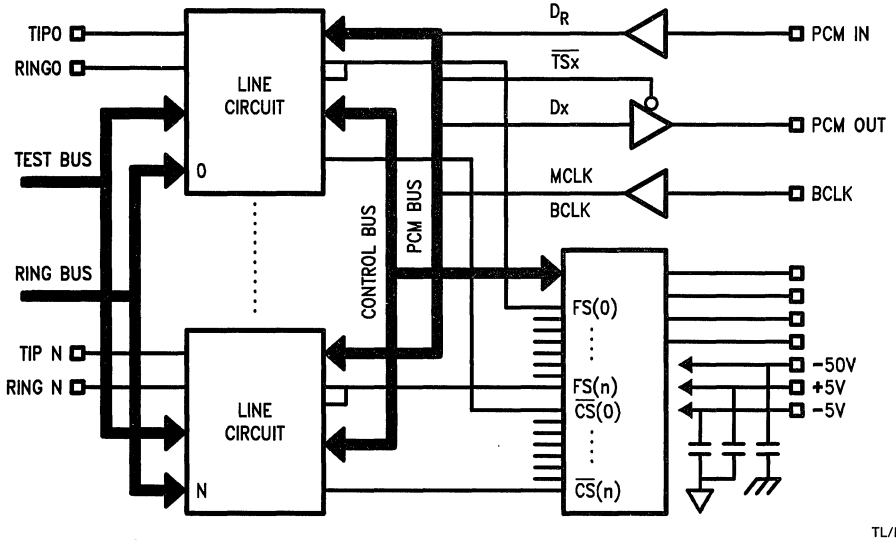


FIGURE 12. Typical n-Line Central Office Linecard

National Semiconductor

PRELIMINARY

TP3212 SLIM™ Subscriber Line Interface Module

General Description

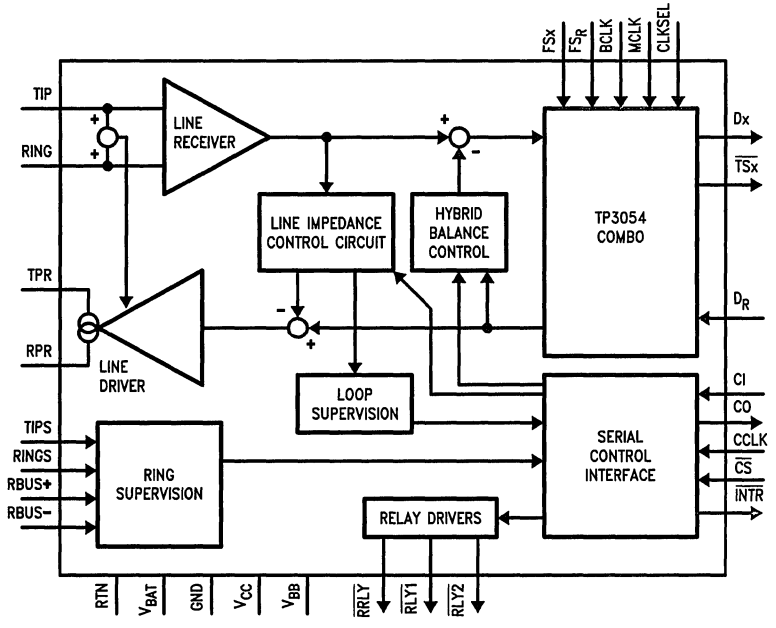
The TP3212 is a complete electronic SLIC and PCM COMBO® CODEC/Filter module intended to interface the analog subscriber line to a PCM highway. It is designed to meet the requirements for POTS (Plain Old Telephone Service) lines in U.S. Digital Loop Carrier applications as specified in TR-TSY-000057. It has the capability to perform in-band on-hook transmission. When used in conjuction with a simple, non-critical, external protection network, two resistors and a ring relay, the TP3212 forms a complete line circuit, handling all the BORSCHT functions.

The TP3212 module consists of a line driver, a line receiver, a line impedance control circuit, a hybrid balance circuit, a loop supervision circuit, a ring supervision circuit, three positive relay drivers, a TP3054 COMBO CODEC/Filter and a serial control interface. Any changes in the status of the subscriber loop generate an interrupt, allowing the device to be used in either polled or interrupt driven applications.

Features

- Complete COMBO CODEC/Filter and SLIC functions
- Exceeds TR-TSY-000057 DLC specifications for POTS lines
- On-hook transmission capability
- Resistive loop feed with current limit
- Power denial mode
- Compatible with loop start and ground start signalling
- Automatic ring trip
- Four selectable balance networks
- Three positive relay drivers
- Thermal overload protection
- Compatible with inexpensive protection networks
- Withstands 500V RTN to GND surge
- Compatible with standard PCM highway
- Small physical size and minimal external components

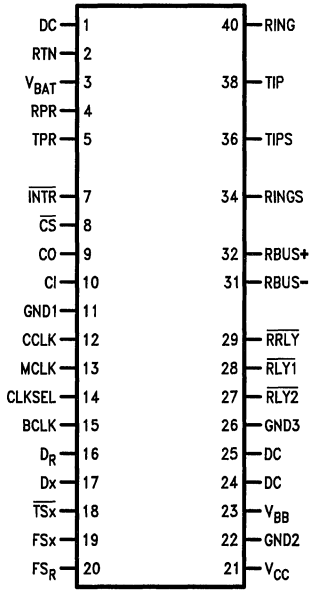
Simplified Block Diagram



TL/H/10736–1

FIGURE 1. Simplified Block Diagram

Connection Diagram



TL/H/10736–2

Order Number TP3212J
Refer To NSC Package Type HY40C

Pin Descriptions

Pin	Pin Descriptions
TIP	Normally positive side of the subscriber line.
RING	Normally negative side of the subscriber line.
TPR	High voltage line driver output. Connects to TIP via an external protection network.
RPR	High voltage line driver output. Connects to RING via an external protection network.
TIPS	Positive ring sensing input. Connected to the positive side of the subscriber loop during ringing.
RINGS	Negative ring sensing input. Connected to the negative side of the subscriber loop during ringing.
RBUS+	Positive ring bus sensing input. Connected to the positive side of the ring bus.
RBUS−	Negative ring bus sensing input. Connected to the negative side of the ring bus.
BCLK	Bit Clock used to shift PCM information into D_R and out of Dx. May vary from 64 kHz to 2.048 MHz in 8 kHz increments.
MCLK	Master clock. Must be 1.536, 1.544 or 2.048 MHz.

Pin	Pin Descriptions
CLKSEL	Master clock select input. Must be connected high for 1.536 or 1.544 MHz operation. Must be connected low for 2.048 MHz operation.
FSx	Transmit frame synchronization pulse input which enables BCLK to shift the PCM information out of Dx. FSx is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
Dx	The TRI-STATE® PCM data output which is enabled by FSx.
$\overline{TSx}$	Open drain output which pulses low during the period when the Dx output is enabled.
FS_R	Receive frame synchronization pulse input which enables BCLK to shift the PCM information into D_R. FS_R is an 8 kHz pulse train. See *Figures 8* and *9* for timing details.
D_R	Receive data input. PCM data is shifted into D_R during the receive timeslot determined by FS_R.
CCLK	Control clock used to shift control data into CI and out of CO during $\overline{CS}$ low.
$\overline{CS}$	Chip select input. Must be low to enable the shifting of control data into CI and out of CO.
CI	The serial control data input used to set the operating state of the module.
CO	The serial status output used to monitor the operating state of the module. CO is TRI-STATE when $\overline{CS}$ is high. See *Figure 3* for timing diagram.
$\overline{INTR}$	Open drain interrupt output. A logic low indicates a change in the status of the subscriber loop, or a change in thermal shutdown.
V_{BB}	Negative power supply. $V_{BB} = -5V \pm 5\%$. Decoupled by internal 0.047 μF to ground.
V_{CC}	Positive power supply. $V_{CC} = 5V \pm 5\%$. Decoupled by 0.047 μF to ground.
$\overline{RRLY}$	Ring Relay Driver. Controlled by State Control Data Word bit D4 (see Table I). It is automatically turned off when ring trip is detected.
$\overline{RLY1}$	General purpose relay driver controlled by State Control Data Word bit D5.
$\overline{RLY2}$	General purpose relay driver controlled by State Control Data Word bit D6.
GND1 GND2 GND3	Low voltage ground. V_{BB}, V_{CC} and all digital signals are referenced to these pins. These pins must be externally connected together close to the module. Collectively referenced as GND in electrical specifications.
V_{BAT}	Negative high voltage supply. $V_{BAT} = -42.5V$ to $-56V$.
RTN	High voltage ground return. V_{BAT} and all analog signals are referenced to this pin.
DC	Don't connect. Do not make external connections to these pins.

Functional Block Description

Functional Block	Description
Line Driver	The Line Driver is a differential output transconductance amplifier which provides the d.c. power and balanced a.c. signals to the subscriber line. The d.c. power is determined by the DC Loop Impedance Control circuit. The a.c. signal applied to the line is controlled by the AC Loop Impedance Control and the analog signal generated by the TP3054 COMBO CODEC/Filter from the received PCM information. Feedback from the Tip and Ring lines produces an effective longitudinal input impedance of about 150Ω from TIP and RING to RTN (75Ω total). In the presence of large longitudinal current, each output of the Line Driver is capable of sourcing or sinking current to limit the longitudinal voltage.
Line Receiver	The Line Receiver monitors the metallic (differential) voltage on the line in the presence of large longitudinal (common mode) voltages.
Loop Impedance Control	The Loop Impedance Control feeds back the line voltage to produce a resistive/inductive d.c. feed impedance for longer loops and a constant current d.c. feed for shorter loops while maintaining an a.c. 2-wire input impedance of 900Ω + 2.16 μF over the voice band, easily meeting the 2-wire return loss requirements.
Hybrid Balance Control	The Hybrid Balance Control circuit consists of four software selectable networks, assuring that the 4-wire return loss requirements are met for a variety of conditions.
Loop Supervision	The Loop Supervision circuit monitors the d.c. current flow in the subscriber loop under non-ringing state and detects on-hook, off-hook and replicates dial pulses.
Ring Supervision	The Ring Supervision circuit monitors the d.c. current flow in the subscriber loop during the ringing state. This circuit is capable of detecting an off-hook condition in less than 200 ms in the presence of large a.c. ringing signals. It operates on loops with ringing superimposed on TIP or RING, or with balanced ringing. This supports bridged ringers, ringers to ground on either TIP or RING and with superimposed ringers.
Relay Drivers	The three relay drivers are capable of driving +5V or +12V relays directly. $\overline{RRLY}$ is dedicated to the ring relay and is automatically turned off when ring trip is detected by the Ring Supervision circuit. $\overline{RLY1}$ and $\overline{RLY2}$ are general purpose. Relay current is returned to GND3 at pin 26.
COMBO	The COMBO CODEC/Filter provides the PCM filtering, encoding and decoding functions necessary to interface the PCM highway to the analog signals on the subscriber loop. This function is identical to the industry standard TP3054 COMBO CODEC/Filter (see the TP3054 datasheet for full details).
Control Interface	The Control Interface circuit provides easy control and monitoring of the state of the TP3212 via a simple serial interface. Through this circuit the user can program the operating mode of the module, and monitor the line status (see Table I for details).

Functional Description

POWER-ON

When power is first applied, the power-on reset circuitry initializes the TP3212 and places it in a standby mode. The State Control Data Word is cleared to "0". All unnecessary circuitry is powered down. The serial control interface and the loop supervision circuitry remain fully functional. The device is now ready for activation, either by the user programming it into the ring mode by writing into the State Control Data Word or by the subscriber going off-hook, powering-up the device automatically.

THE STATE CONTROL DATA WORD

The State Control Data word is a single eight-bit word as shown in Table I. Bits D0–D7 of the control word program the operating state of the device. The module can initialize the power denial mode by itself in order to protect itself from damage under a thermal overload condition.

STATUS WORD

The eight-bit Status Word indicates the status of the TP3212 at the instant a read operation is performed. Table IV shows the definitions of the status word. A logic high indicates that the state or function is enabled, a low indicates that it is disabled.

THE CONTROL INTERFACE

The Control Interface consists of a single eight-bit shift register and a buffer register. The shift register is written via the serial input CI, under the control of $\overline{CS}$ and CCLK, to program the device's operating state. Several bits of the shift register may be altered by the device itself in response to changes in the subscriber loop status. These changes in

Functional Description (Continued)

state may be read via the serial output CO. The S2 and S3 status bits are over-written by the occurrence of a thermal overload, forcing the device into the Power-Denial mode. S7 is the hook-switch status bit. A logic "0" for S7 indicates an Off-Hook at normal mode or Ring-Trip at ring mode at the instant of accessing the control interface and a logic "1" indicates on-hook. Any changes in line status, or thermal shutdown condition will generate an interrupt at $\overline{INTR}$ output.

TABLE I. State Control Data Word

Control Bit	Description
D7	Selects loop detector's thresholds. Must be programmed to "0" for loop start and "1" for ground start. This bit is overwritten by the line supervision circuitry.
D6	Logical "1" enables $\overline{RLY2}$.
D5	Logical "1" enables $\overline{RLY1}$.
D4	Logical "1" enables Ring mode, turns on $\overline{RRLY}$ and Ring Supervision circuit. Status Bit S7 indicates ring-trip. Logical "0" enables the normal mode.
D3	Used with D2 to select Power denial, Battery Reversal or On-Hook Transmission modes. See Table II. Under Power Denial mode, the Line Drivers are disabled, denying power to the subscriber loop. It can be set or cleared by a write operation. Under a thermal overload condition, D3 is forced to "1" and D2 is forced to "0" in order to protect the device from damage. As long as the thermal overload condition exists, the Power Denial mode cannot be cleared by a write operation.
D2	Used with D3 to select Power denial, Battery Reversal or On-Hook Transmission modes. See Table II.
D1	Used with D0 to select hybrid balance network. See Table III.
D0	Used with D1 to select hybrid balance network. See Table III.

TABLE II. Operating Modes of TP3212

D4	D3	D2	Mode
0	**0**	**0**	Normal
0	0	1	Reverse Battery
0	1	0	Power Denial
0	1	1	On-Hook Transmission
1	x	x	Ring

TABLE III. Hybrid Balance Test Networks

D1	D0	Reference Test Network
0	**0**	900Ω
0	1	1650Ω//(100Ω + 0.005 μF)
1	0	800Ω//(100Ω + 0.05 μF)
1	1	900Ω + 2.16 μF

There are several ways of accessing the serial control interface. They are:

a) Write/Read
b) Read/Write
c) Quick Status Read

In the Write/Read operation, the objective is to change the state of the device. While shifting the new state control data into CI, the previous status information is shifted out of CO. This data should be compared with the previous status information to determine if a change had occurred since the last access.

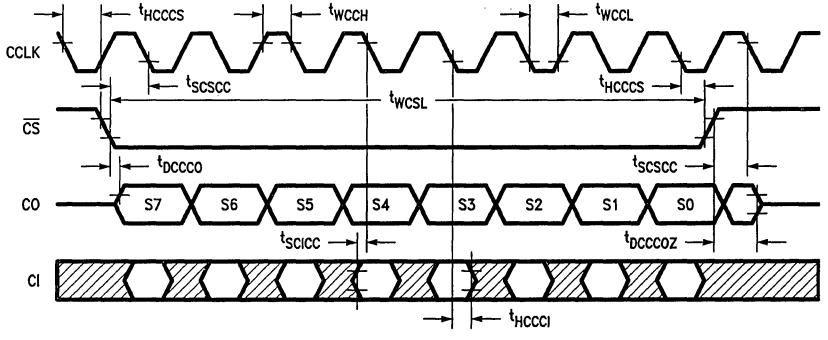
In the Read/Write operation, the objective is to monitor the state of the module. While the current status is shifted out at CO, the last known state of the device is shifted into CI externally. If a thermal overload condition has occurred since the last access, the device will automatically set itself to the power denial mode (S3 bit will be forced to "1" and S2 will be forced to "0") prior to the access and will be reset by writing the previous state. This has no detrimental effect, however, since the power-denial mode will immediately be set again and the device will remain in the Power-Denial mode as long as the thermal overload continues to exist. If ring trip has occurred or the hook switch status has changed since the last access, the S7 bit will also be altered by the device. The timing for the Write/Read or Read/Write modes is shown in *Figure 2.*

The Quick Status Read operation allows a fast read of the S7 status bit, which indicates if a Ring-Trip or Off-Hook condition exists. It does not cause the shift register to shift, thus no control data is required. *Figure 3* is the timing diagram for the Quick Status Read Mode.

Functional Description (Continued)

TABLE IV. Status Information Word

Status Bit	Description
S7	Indicates switch hook status. S7 is a "1" if the subscriber is on-hook. If D4 is programmed to be "0" for normal mode, a logic "0" at S7 indicates off-hook. If the device is in the Ring mode (D4 = "1"), a logic "0" at S7 indicates ring-trip.
S6	A logic "1" indicates that $\overline{RLY2}$ is on.
S5	A logic "1" indicates that $\overline{RLY1}$ is on.
S4	A logic "1" indicates Ring mode is on. $\overline{RRLY}$ is turned on, and the Ring Supervision circuit is activated. A logic "0" at S7 indicates that a ring trip has occurred, forcing $\overline{RRLY}$ to be de-activated. D4 should be cleared to "0" by a write/read operation in order to program the device into the non-ringing mode.
S3	S2 and S3 indicate Power Denial, Battery Reversal, or On-Hook Transmission mode (see Table II). When an overload condition exists which raises the junction temperature to exceed about 170°C, the TP3212 will automatically initiate a power denial mode (S3 forced to "1" and S2 forced to "0") to protect itself from damage. The device will not go back to the normal mode even if the thermal overload ceases to exist. The system can determine if the thermal overload condition has cleared itself by programming the TP3212 into the desired operating mode and read back status bits S2 and S3. If the overload still exists, the power denial mode will be activated again as long as the device's junction temperature exceeds approximately 170°C.
S2	S2 and S3 indicate Power Denial, Battery Reversal, or On-Hook Transmission mode (see Table II).
S1	Indicates the selected hybrid balance test network as shown in Table III.
S0	Indicates the selected hybrid balance test network as shown in Table III.



TL/H/10736–3

FIGURE 2. Control Interface Timing—Write/Read or Read/Write Modes

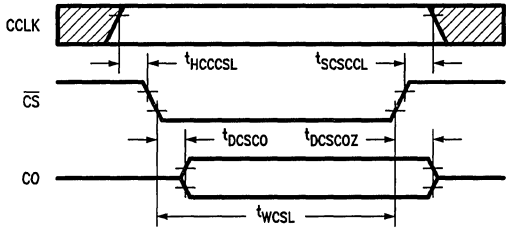


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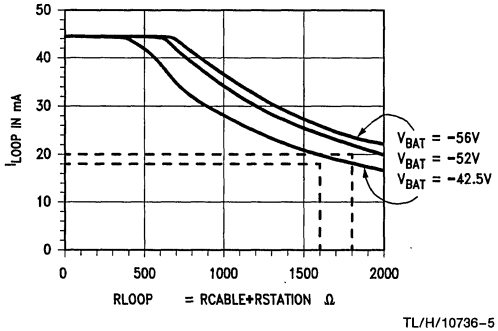
FIGURE 3. Control Interface Timing—Quick Status Read Mode

Functional Description (Continued)

BATTERY FEED

With $V_{BAT} = -52V$, the TP3212 provides a nominal apparent battery voltage of $-44.9V$ across TIP and RING. The module provides a resistive/inductive feed at longer loops. The d.c. current feed has been designed to guarantee 20 mA into an 1800Ω loop at nominal battery, and 18 mA into a 1600Ω loop at minimum battery of $-42.5V$. At shorter loops, the d.c. feed is current-limited to nominally 43 mA in order to conserve power. At normal battery polarity (D3 = 0 and D2 = 0), TIP is more positive than RING. The current feed characterisitc is shown in *Figure 4.*



TL/H/10736–5

FIGURE 4. d.c. Feed Characteristics

2-WIRE IMPEDANCE

The nominal 2-wire input impedance is 900Ω + 2.16 μF. This is shunted by the feeding inductance which is nominally 26 Henries on long loops, and approaches infinity on short loops.

TRANSMISSION LEVEL

The 0 TLP is referenced at the PCM interface of the four wire ports. The TP3212 module has 2 dB loss for both transmit and receive signals. On the 2-wire analog interface, the transmit is +2 TLP and the receive is −2 TLP. TLP is defined as 0 dBm into 900Ω.

HYBRID BALANCE

The Hybrid Balance Control circuit contains four selectable balance networks which are selected by programming State Control Word bits D0 and D1. The balance networks are intended to be used with the corresponding reference test networks for hybrid balance as shown in Table III.

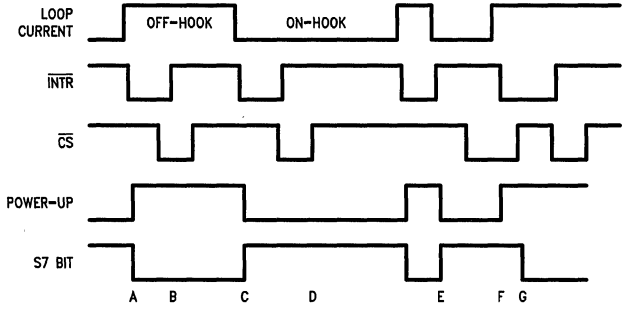
LONGITUDINAL BALANCE AND LONGITUDINAL CURRENT CAPABILITY

The 2-wire input of the device exhibits a longitudinal impedance of 150Ω from TIP to ground and from RING to ground. These impedances are extremely well matched and are not strongly dependent on impedance matching in the external protection network. The longitudinal voltage is sensed on the loop side of the protection network and fed back to the Line Driver, thus any component variations external to the device can be corrected by the feedback loop. The Line Driver is capable of handling 21 mA_{rms} of longitudinal current in each of the TIP and RING leads.

LOOP SUPERVISION

The Loop Supervision circuit operates in the normal (nonringing) state. When control bit D7 is programmed to logic 0, it enables loop start signalling and a dynamic threshold comparator in order to maintain the dial pulse break interval within 46% to 74% regardless of the distortion introduced by the loop characteristics. The output of the Loop Impedance Control is monitored and off-hook indicated when the loop current exceeds nominally 13 mA and on-hook indicated when the current falls below nominally 11 mA, providing a 2 mA hysteresis. A logic "1" at status bit S7 indicates on-hook, while a logic "0" indicates off-hook. When control bit D7 is programmed to logic "1", it adjusts the loop comparator's thresholds for ground start signalling. Off-hook is indicated when the current from RING to Ground (with TIP open) exceeds nominally 17 mA and on-hook when the current falls below nominally 13 mA.

A typical example of hook switch timing is illustrated in *Figure 5.* While in the standby mode, all unnecessary circuitry is powered down. When Loop Supervision detects off-hook, the module is powered up, $\overline{INTR}$ goes low and status bit S7 is cleared (A). The $\overline{INTR}$ remains active until $\overline{CS}$ goes low and status is read, at which time the status of the switch hook is latched, clearing $\overline{INTR}$ (B). When the Loop Supervision detects on-hook, all unnecessary circuitry is again powered down, status bit S7 is set and $\overline{INTR}$ is again set low (C). When the status information is read, the present switch hook status is latched, clearing the interrupt, and $\overline{INTR}$ goes high (D). In the case of either on-hook or off-hook, if the system fails to read the status before the switch hook reverts to its previous state, the interrupt will clear itself (E). If the device's control interface is being accessed when off-hook occurs, i.e., $\overline{CS}$ is low, $\overline{INTR}$ is set low immediately (F) but S7 is cleared only after $\overline{CS}$ returns high (G). On the next Read/Write access, S7 is latched.



TL/H/10736–6

FIGURE 5. Typical Hook Switch Detect Timing

Functional Description (Continued)

RING SUPERVISION

The Ring Supervision circuit measures the loop current across two 360Ω ring sensing resistors with a 1 MΩ internal resistive bridge (see *Figure 10*). The voltage at the output of the bridge is filtered, then algebraically added and subtracted from a voltage corresponding to a loop current of about 11 mAdc. Each of the resulting voltages are integrated over one period of the ring frequency and compared to zero. If either of the resulting voltages is less than zero for two consecutive cycles, ring-trip is detected. $\overline{RRLY}$ is de-activated, status bit S7 is cleared to "0" indicating ring trip, and an interrupt is also generated. Control bit D4 (RING) is not automatically reset to "0", it has to be cleared to "0" by a write/read operation after a ring trip is detected. If the MCLK is interrupted and stays continuously high or low for more than 200 μs, the ring relay driver will be turned off.

The ring supervision circuit works with zero to five bridged ringers (1 ringer = 7 kΩ at 20 Hz), with ring frequencies from 16 to 67 Hz, with ring voltages from 90 to 155 Vrms applied to either TIP or RING, superimposed on positive or negative battery voltages of from 42 to 56 volts on loops up to 1700Ω. Furthermore, it operates with up to five ringers connected from TIP or RING to ground or with up to three superimposed ringers connected from TIP to ground and three from RING to ground with a battery voltage of ±38 ±2V. The ring sensing inputs at TIPS, RINGS, RBUS+ and RBUS− when connected as shown in *Figure 10*, will present an effective load of about 500 kΩ across the ring bus.

A typical example of ring trip timing is illustrated in *Figure 6*. When the Ring Supervision circuit detects a ring trip, the device immediately turns off $\overline{RRLY}$, clears S7 and sets $\overline{INTR}$ low (A). The interrupt remains active until $\overline{CS}$ goes low and the status is read, at which time the status of the switch hook is latched, clearing $\overline{INTR}$ (B). Status bit S7 will remain a zero until the D4 bit is written to a zero, removing the device from the RING mode (C). At this time, the S7 bit will indicate the switch hook status. Even though the station equipment is normally off-hook at this time, S7 will generally return to a "1" (C) for several milliseconds after D4 is cleared. This is because the Loop Supervision circuit was disconnected from the loop during ringing mode (D4 = 1), and it takes several milliseconds to detect the off hook at which time S7 will be cleared and $\overline{INTR}$ will be set low (D). At this point the device is in the normal (non-ringing) mode, all necessary circuitry is powered up.

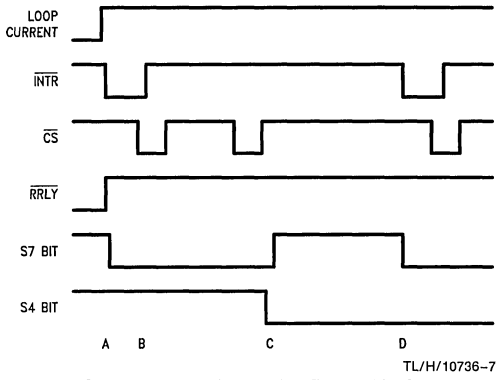


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FIGURE 6. Typical Ring Trip Detect Timing

THERMAL OVERLOAD

The Line Driver incorporates a built-in thermal overload detection circuitry. In the event of a fault on the subscriber line which causes the Line Driver to reach an internal junction temperature of approximately 170°C, the Line Driver will protect itself by forcing the device into the power-denial mode, S3 is forced to "1" and S2 is forced to "0". The device will remain at the power denial mode even though the thermal overload ceases to exist. After the line fault has been corrected, the device can be put back into service under system control (see Table IV).

A typical example of thermal overload detection timing is illustrated in *Figure 7*. When a thermal overload is detected, S3 is set high and S2 is set low (A), forcing the device into the Power-Denial mode, and $\overline{INTR}$ is set low. The interrupt remains active until $\overline{CS}$ goes low, clearing $\overline{INTR}$ (B). As long as the thermal overload condition exists, the power denial mode cannot be reset by a write operation (B). When the thermal overload condition clears, the $\overline{INTR}$ will again be set low, but the device continued to remain at power denial mode (C). Thus the device does not automatically re-apply power to the line since the fault that originally caused the failure may still exist and would simply cause the overload to re-occur. In this example, the power denial mode is cleared by a control write to normal mode, clearing S2 and S3 to "0" (D). If the device is being accessed at the instant the thermal shutdown indication occurs, $\overline{INTR}$ is set low immediately, but S3 will be set high and S2 will be set low only after $\overline{CS}$ returns high (E).

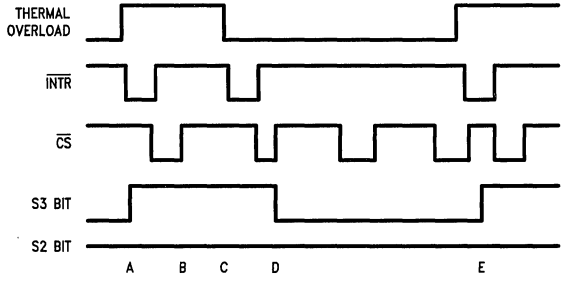

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FIGURE 7. Typical Thermal Overload Detection Timing

Functional Description (Continued)

ON-HOOK TRANSMISSION MODE

The device is in the on-hook transmission mode when bit D3 and D2 of the State Control Data Word is set to the logic "1" and the loop is under "on-hook". In this mode, the line drivers operate in a reduced power state but all circuitry is active. This enables the system to communicate with a subscriber terminal or the subscriber to communicate through the network or to a terminal in the central office to provide alarm and telemetry services. When the loop goes off-hook, the loop supervision circuitry behaves normally and causes the line drivers to power up. Bit S7 of the Status Information Word is cleared and an interrupt is initiated. This enables the system to terminate any transmissions and handle the call initiation in the normal manner.

PCM INTERFACE

The PCM interface consists of inputs MCLK, BCLK, FSx, FS_R and D_R, and outputs Dx and $\overline{TSx}$. MCLK controls the internal operation of the COMBO CODEC/Filter's encoder and decoder, and must be 1.536 or 1.544 MHz if CLKSEL is connected high and 2.048 MHz if CLKSEL is connected low. BCLK shifts the PCM data out of Dx on its rising edge and latches the PCM data into D_R on its falling edge. It must be synchronous with MCLK and may be any integer multiple of 8 kHz from 64 kHz to 2.048 MHz. FSx and FS_R are 8 kHz pulse waveforms which determine the beginning of the PCM data transfer out of Dx and into D_R respectively. Both must be synchronous with MCLK but may have any phase relationship with each other. $\overline{TSx}$ is an open drain output which pulses low for the duration of the data transfer out of Dx. It is intended to be wire-ORed with the $\overline{TSx}$ outputs of other subscriber line interface modules to provide an enable signal for external TRI-STATE drivers buffering the PCM transmit data from a line card onto the backplane.

Short Frame Sync Operation

The TP3212 Subscriber Line Interface Module can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, the frame sync pulses applied to both FSx and FS_R must be one BCLK period long and with timing relationships as specified in *Figure 8*. With FSx high during a falling edge of BCLK, the next rising edge of BCLK enables the Dx TRI-STATE output buffer, which will output the PCM sign bit. The following seven rising edges of the bit clock shifts out the remaining seven bits of PCM data, MSB first. The next falling edge disables the Dx output. With FS_R high during a falling edge of BCLK, the next falling edge latches the PCM sign bit into D_R. The next seven falling edges latch the remaining seven bits, MSB first.

Long Frame Sync Operation

To use the long frame sync mode, the frame sync pulses applied to both FSx and FS_R must be three or more bit periods long, with timing relationships as specified in *Figure 9*. Based on the transmit frame sync pulse, the device will sense whether short or long frame sync pulses are being used. For 64 kHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The Dx TRI-STATE output buffer is enabled with the rising edge of FSx or the rising edge of BCLK, whichever comes later, and the first bit clocked out is the PCM sign bit. The following seven rising edges of BCLK shift out the remaining seven bits, MSB first. The Dx output is disabled by the falling edge of BCLK following the eighth rising edge or by FSx going low, whichever comes later. A rising edge of the receive frame sync will cause PCM data at D_R to be latched in on the next eight falling edges of BCLK.

Functional Description (Continued)

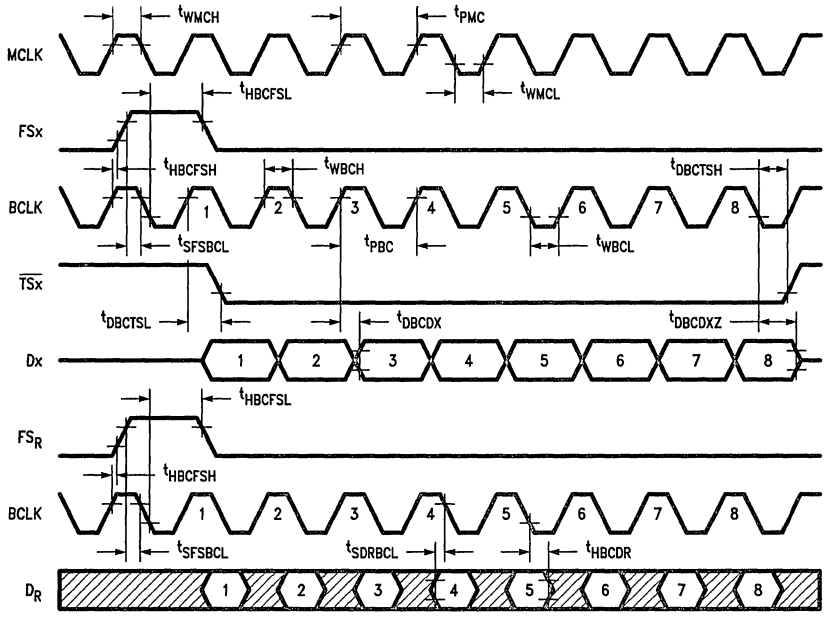

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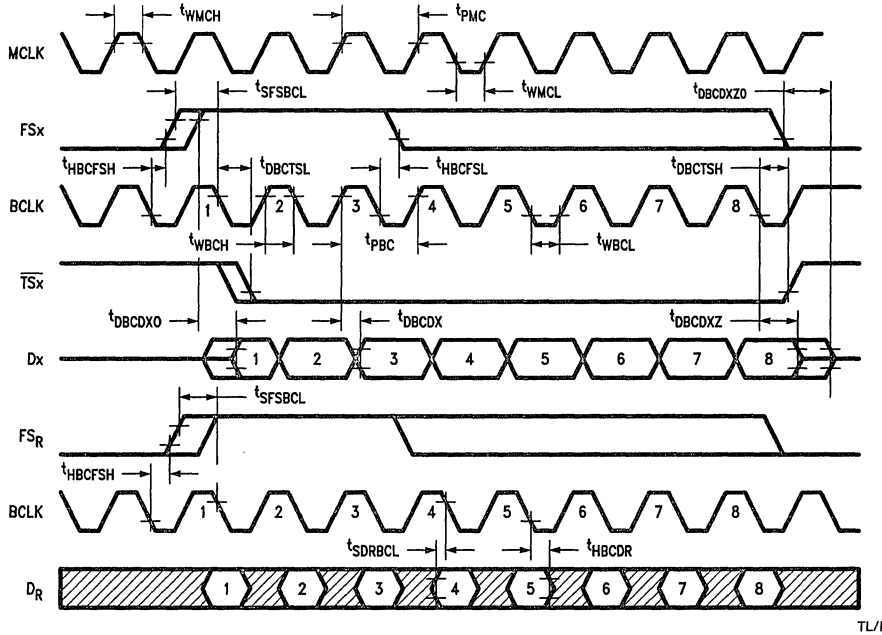
FIGURE 8. Timing Diagram for Short Frame Mode



TL/H/10736–10

FIGURE 9. Timing Diagram for Long Frame Mode

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	−0.5V to 7V
V_{BB} to GND	0.5V to −7V
V_{BAT} to RTN	0.5V to −70V
RTN to GND	±500V, 10 μs/50 μs Pulse
Voltage at any digital input or output	V_{CC} + 0.3V to GND − 0.3V
TPR, RPR to RTN	2V to −85V (50 ms)
TIP, RING, TIPS, RINGS, RBUS+, RBUS− to RTN	±1000V, 10 μs/1000 μs Pulse
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
Maximum Junction Temperature	150°C

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
POWER DISSIPATION (Normal Mode: D2 = 0, D3 = 0)						
$I_{BAT}0$	V_{BAT} Idle Current	I_{LOOP} = 0 mA, V_{BAT} = −52V		2.1	**4.0**	mA
$I_{BB}0$	V_{BB} Idle Current	I_{LOOP} = 0 mA		1.9	**3.6**	mA
$I_{CC}0$	V_{CC} Idle Current	I_{LOOP} = 0 mA		2.9	**5**	mA
$I_{BAT}1$	V_{BAT} Active Current	I_{LOOP} = 20 mA, V_{BAT} = −52V		23	**25**	mA
$I_{BB}1$	V_{BB} Active Current	I_{LOOP} = 20 mA		8.9	**17.2**	mA
$I_{CC}1$	V_{CC} Active Current	I_{LOOP} = 20 mA		11.8	**17.2**	mA
POWER DISSIPATION (On-Hook Transmission Mode: D2 = 1, D3 = 1)						
$I_{BAT}OH$	V_{BAT} Idle Current	I_{LOOP} = 0 mA, V_{BAT} = −52V		2.1	**4.0**	mA
$I_{BB}OH$	V_{BB} Idle Current	I_{LOOP} = 0 mA		8.9	**17.2**	mA
$I_{CC}OH$	V_{CC} Idle Current	I_{LOOP} = 0 mA		11.8	**17.2**	mA
DIGITAL INTERFACE (Note 1)						
V_{IL}	Input Low Level	All Digital Inputs			**0.7**	V
V_{IH}	Input High Level	All Digital Inputs except CLKSEL CLKSEL	**2** **4**			V V
V_{OL}	Output Low Level	Dx, $\overline{TSx}$, CO, I_L = 3.2 mA $\overline{INTR}$, I_L = 2.0 mA			**0.4** **0.4**	V V
V_{OH}	Output High Level	Dx, CO, I_H = −3.2 mA	**2.4**			V
I_{IL}	Input Low Current	GND < V_{IN} < V_{IL}, All Digital Inputs	**−100**		**100**	μA
I_{IH}	Input High Current	V_{IH} < V_{IN} < V_{CC}, All Digital Inputs	**−100**		**100**	μA
I_{OH}	Output High Current	$\overline{TSx}$ and $\overline{INTR}$, V_{OH} < V_{OUT} < V_{CC}	**−100**		**100**	μA
I_{OZ}	Output Current in the High Impedance State	CO, Dx	**−100**		**100**	μA

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BATTERY FEED						
I_{LOOP+}	Loop Current Normal Battery	R_{LOOP} = 1800Ω, V_{BAT} = −52V R_{LOOP} = 1600Ω, V_{BAT} = −42.5V R_{LOOP} = 100Ω, V_{BB} = −4.75V (Note 2)	**20** **18** 40	21.3 19.2 43	**24** **22** 46	mA mA mA
I_{LOOP-}	Loop Current Reverse Battery	R_{LOOP} = 1800Ω, V_{BAT} = −52V R_{LOOP} = 1600Ω, V_{BAT} = −42.5V R_{LOOP} = 100Ω, V_{BB} = −4.75V (Note 2)	**20** **18** 40	21.3 19.2 43	**24** **22** 46	mA mA mA
I_{PD}	Power Denial Loop Current	R_{LOOP} = 100Ω		0.1	**2**	mA
V_{LOOP}	Loop Voltage	R_{LOOP} = 10 kΩ, V_{BAT} = −52V		−43.4		V
LOOP SUPERVISION						
$R_{OFFHK}0$	Loop Resistance to Produce an Off-Hook Indication at Loop Start	$R_{OFFHK}0$ Connected from TIP to RING V_{BAT} = −42.5V D7 = 0			**2000**	Ω
$R_{ONHK}0$	Loop Resistance to Produce an On-Hook Indication at Loop Start	$R_{ONHK}0$ Connected from TIP to RING V_{BAT} = −56V D7 = 0	**9**			kΩ
$R_{OFFHK}1$	Loop Resistance to Produce an Off-Hook Indication at Ground Start	$R_{OFFHK}1$ Connected from RING to RTN, TIP Open V_{BAT} = −42.5V D7 = 1			**1330**	Ω
$R_{ONHK}1$	Loop Resistance to Produce an On-Hook Indication at Ground Start	$R_{ONHK}1$ Connected from RING to RTN, TIP Open V_{BAT} = −56V D7 = 1	**9**			kΩ
DPD	Dial Pulse Distortion	D7 = 0, R_{LEAK} = 15 kΩ R_{LOOP} = 100Ω, 12 pps, Break = 58% R_{LOOP} = 1800Ω, 12 pps, Break = 64%, $\overline{CS}$ High, Measure Width of Break Period at $\overline{INTR}$	38.4 **38.4**		61.5 **61.5**	ms ms
RING SUPERVISION						
RNGTRP1	Ring Trip Detect, Normal Ringing	RBUS+ = 0V, RBUS− = −48V, TIPS = −5V, RINGS = −43V, Must Detect Ring-Trip within the Specified Time	**50**		**180**	ms
RNGTRP2	Ring Trip Detect, Reverse Ringing	RBUS+ = −48V, RBUS− = 0V, TIPS = −43V, RINGS = −5V, Must Detect Ring-Trip within the Specified Time	**50**		**180**	ms
RNGTRP3	Ring Trip Non-Detect, Normal Ringing	RBUS+ = 0V, RBUS− = −48V, TIPS = −3V, RINGS = −45V, Must Not Detect Ring Trip within the Specified Time (Note 3)	**0**		**180**	ms

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RING SUPERVISION (Continued)						
RNGTRP4	Ring Trip Non-Detect, Reverse Ringing	RBUS+ = −48V, RBUS− = 0V, TIPS = −45V, RINGS = −3V, Must Not Detect Ring-Trip within the Specified Time (Note 3)	**0**		**180**	ms
RNGTRP5	Ring Trip Detect, Normal Ringing	TIPS, RBUS− = −5V, RINGS, RBUS+ = 26 Vrms, f = 20 Hz Must Detect Ring-Trip within the Specified Time	**100**		**190**	ms
RNGTRP6	Ring Trip Detect, Reverse Ringing	TIPS, RBUS− = 26 Vrms, RINGS, RBUS+ = −5V, f = 20 Hz Must Detect Ring-Trip within the Specified Time	**100**		**190**	ms
RNGTRP7	Ring Trip Non-Detect, Normal Ringing	TIPS, RBUS− = −3V, RINGS, RBUS+ = 26 Vrms, f = 20 Hz Must Not Detect Ring-Trip within the Specified Time (Note 3)	**0**		**190**	ms
RNGTRP8	Ring Trip Non-Detect, Reverse Ringing	TIPS, RBUS− = 26 Vrms, RINGS, RBUS+ = −3V, f = 20 Hz Must Not Detect Ring-Trip within the Specified Time (Note 3)	**0**		**190**	ms
HYBRID BALANCE Unless otherwise specified, I_{LOOP} = 20 mA, D2 = 0, D3 = 0						
ECHO1	4-Wire Return Loss	Z_{REF} = 900Ω across Tip-Ring D1 = 0, D0 = 0				
		f = 203.125 Hz	**21**			dB
		f = 484.375 Hz	**26**			dB
		f = 1015.625 Hz	**26**	40		dB
		f = 2500 Hz	**26**			dB
		f = 3406.25 Hz	**21**			dB
ECHO2	4-Wire Return Loss	Z_{REF} = 1650Ω//(100Ω + 0.005 μF) D1 = 0, D0 = 1				
		f = 203.125 Hz	**21**			dB
		f = 484.375 Hz	**26**			dB
		f = 1015.625 Hz	**26**	40		dB
		f = 2500 Hz	**26**			dB
		f = 3406.25 Hz	**21**			dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
HYBRID BALANCE Unless otherwise specified, I_{LOOP} = 20 mA, D2 = 0, D3 = 0 (Continued)						
ECHO3	4-Wire Return Loss	Z_{REF} = 800Ω//(100Ω + 0.05 μF) D1 = 1, D0 = 0				
		f = 203.125 Hz	**21**			dB
		f = 484.375 Hz	**26**			dB
		f = 1015.625 Hz	**26**	40		dB
		f = 2500 Hz	**26**			dB
		f = 3406.25 Hz	**21**			dB
ECHO4	4-Wire Return Loss	Z_{REF} = 900Ω + 2.16 μF D1 = 1, D0 = 1				
		f = 203.125 Hz	**21**			dB
		f = 484.375 Hz	**26**			dB
		f = 1015.625 Hz	**26**	40		dB
		f = 2500 Hz	**26**			dB
		f = 3406.25 Hz	**21**			dB
TRANSMISSION Unless otherwise noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{LOOP} = 20 mA, D2 = 0, D3 = 0						
RTNLOSS	2-Wire Return Loss	f = 203.125 Hz	**21**			dB
		f = 484.375 Hz	**27**			dB
		f = 1015.625 Hz	**27**	40		dB
		f = 2500 Hz	**27**			dB
		f = 3406.25 Hz	**27**			dB
0 dBm0	The Absolute 2-Wire Reference Level	The Absolute Reference Level at the Two Wire Interface is +2 dBm/900Ω for Transmit, and −2 dBm/900Ω for Receive. Transmit (2-Wire to Dx) Receive (D_R to 2-Wire)		 1.194 0.754		 Vrms Vrms
G_{RA}	Absolute Receive Gain	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V T_A = 25°C, D_R to 2-Wire Port, Input = Digital Code for 0 dBm0 at D_R, Measure Voltage across TIP-RING	**−0.25**		**0.25**	dB
G_{XA}	Absolute Transmit Gain	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V T_A = 25°C, 2-Wire Port to Dx, Input = 0 dBm0 at 2-Wire Port, Measure Digital Code at Dx	**−0.25**		**0.25**	dB
G_{RAOH}	Absolute Receive Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V Z_{REF} = 900Ω + 2.16 μF D3 = 1, D2 = 1, I_{LOOP} = 0 mA D_R to 2-Wire	**−1**		**1**	dB
G_{XAOH}	Absolute Transmit Gain at On-Hook Transmission Mode	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V from 2-Wire Analog Interface to Dx D3 = 1, D2 = 1, I_{LOOP} = 0 mA	**−1**		**1**	dB
G_{RAV}	Absolute Receive Gain Over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%, V_{BAT} = −42.5V to −56V	**−0.3**		**0.3**	dB
G_{XAV}	Absolute Transmit Gain Over Supply Range	V_{CC} = 5V ±5%, V_{BB} = −5V ±5%, V_{BAT} = −42.5V to −56V	**−0.3**		**0.3**	dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless otherwise noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{LOOP} = 20 mA, D2 = 0, D3 = 0 (Continued)						
G_{RT}	Receive Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V Reference to G_{RA}	−0.15		0.15	dB
G_{XT}	Transmit Gain Variation over Temperature	V_{CC} = 5V, V_{BB} = −5V, V_{BAT} = −52V Reference to G_{XA}	−0.15		0.15	dB
G_{RF}	Receive Frequency Response	Measure Relative to G_{RA}				
		f = 203.125 Hz	**−1.9**		**0**	dB
		f = 296.875 Hz	**−0.4**		**0.25**	dB
		f = 484.375 Hz	**−0.25**		**0.25**	dB
		f = 2015.625 Hz	**−0.25**		**0.25**	dB
		f = 2703.125 Hz	**−0.25**		**0.25**	dB
		f = 3015.625 Hz	**−0.25**		**0.25**	dB
		f = 3203.125 Hz	**−0.25**		**0.25**	dB
		f = 3390.625 Hz	**−1.2**		**0**	dB
		f = 3984.375 Hz			**−14**	dB
SOS	Spurious Out of Band Signals (Alias Tones)	Measure Relative to G_{RA}				
		f = 4796.875 Hz			**−30**	dB
		f = 6703.125 Hz			**−30**	dB
		f = 11390.625 Hz			**−30**	dB
G_{XF}	Transmit Frequency Response	Measure Relative to G_{XA}				
		f = 62.500 Hz			**−21**	dB
		f = 203.125 Hz	**−2.5**		**0**	dB
		f = 296.875 Hz	**−0.4**		**0.25**	dB
		f = 484.375 Hz	**−0.25**		**0.25**	dB
		f = 2015.625 Hz	**−0.25**		**0.25**	dB
		f = 2703.125 Hz	**−0.25**		**0.25**	dB
		f = 3015.625 Hz	**−0.25**		**0.25**	dB
		f = 3202.125 Hz	**−0.25**		**0.25**	dB
		f = 3390.625 Hz	**−1.2**		**0**	dB
		f = 3984.375 Hz			**−14**	dB
		f = 5046.875 Hz			**−32**	dB
		f = 11890.625 Hz			**−32**	dB
G_{RL}	Receive Gain Variation with Signal Level	Measure Relative to G_{RA} PCM Level				
		= 3.1 dBm0	**−0.25**		**0.25**	dB
		= −2.3 dBm0	**−0.25**		**0.25**	dB
		= −11.4 dBm0	**−0.25**		**0.25**	dB
		= −17.6 dBm0	**−0.25**		**0.25**	dB
		= −23.9 dBm0	**−0.25**		**0.25**	dB
		= −29.9 dBm0	**−0.25**		**0.25**	dB
		= −37.8 dBm0	**−0.25**		**0.25**	dB
		= −47.1 dBm0	**−0.45**		**0.45**	dB
		= −55.7 dBm0	**−1.3**		**1.3**	dB

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless otherwise noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{LOOP} = 20 mA, D2 = 0, D3 = 0 (Continued)						
G_{XL}	Transmit Gain Variation with Signal Level	Measure Relative to G_{XA} PCM Level				
		= 3.1 dBm0	**−0.25**		**0.25**	dB
		= −2.3 dBm0	**−0.25**		**0.25**	dB
		= −11.4 dBm0	**−0.25**		**0.25**	dB
		= −17.6 dBm0	**−0.25**		**0.25**	dB
		= −23.9 dBm0	**−0.25**		**0.25**	dB
		= −29.9 dBm0	**−0.25**		**0.25**	dB
		= −37.8 dBm0	**−0.25**		**0.25**	dB
		= −47.1 dBm0	**−0.45**		**0.45**	dB
		= −55.7 dBm0	**−1.3**		**1.3**	dB
STD_R	Receive Signal to Total Distortion	Measure through C Message Filter PCM Level				
		= 3.1 dBm0	**33**			dBC
		= 0.0 dBm0	**36**			dBC
		= −2.3 dBm0	**36**			dBC
		= −11.4 dBm0	**36**			dBC
		= −17.6 dBm0	**36**			dBC
		= −23.9 dBm0	**36**			dBC
		= −29.9 dBm0	**35**			dBC
		= −37.8 dBm0	**30**			dBC
		= −40.0 dBm0	**28**			dBC
		= −45.0 dBm0	**24**			dBC
		= −47.1 dBm0	**22**			dBC
		= −55.7 dBm0	**13**			dBC
STD_X	Transmit Signal to Total Distortion	Measure through C Message Filter PCM Level				
		= 3.1 dBm0	**33**			dBC
		= 0.0 dBm0	**36**			dBC
		= −2.3 dBm0	**36**			dBC
		= −11.4 dBm0	**36**			dBC
		= −17.6 dBm0	**36**			dBC
		= −23.9 dBm0	**36**			dBC
		= −29.9 dBm0	**35**			dBC
		= −37.8 dBm0	**30**			dBC
		= −40.0 dBm0	**28**			dBC
		= −45.0 dBm0	**24**			dBC
		= −47.1 dBm0	**21**			dBC
		= −55.7 dBm0	**12**			dBC
D_{RA}	Absolute Receive Delay	f = 1600 Hz		190		μs

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRANSMISSION Unless otherwise noted, Z_{REF} = 900Ω + 2.16 μF, f = 1015.625 Hz, I_{LOOP} = 20 mA, D2 = 0, D3 = 0 (Continued)						
D_{RR}	Receive Delay Distortion	Measure Relative to D_{RA}				
		f = 500 Hz		−2		μs
		f = 1000 Hz		−10		μs
		f = 2600 Hz		70		μs
		f = 2800 Hz		100		μs
		f = 3000 Hz		150		μs
D_{XA}	Absolute Transmit Delay	f = 1600 Hz		300		μs
D_{XR}	Transmit Delay Distortion	Measure Relative to D_{XA}				
		f = 500 Hz		250		μs
		f = 600 Hz		150		μs
		f = 800 Hz		65		μs
		f = 1000 Hz		30		μs
		f = 2600 Hz		60		μs
		f = 2800 Hz		80		μs
		f = 3000 Hz		140		μs
NOISE Z_{REF} = 900Ω + 2.16 μF, I_{LOOP} = 20 mA, D2 = 0, D3 = 0						
N_{RC}	Receive C Message Weighted Idle Channel Noise	PCM Code is Alternating Positive and Negative Zeroes		9	**13**	dBrnC
N_{XC}	Transmit C Message Weighted Idle Channel Noise	Measured by Extrapolation from Signal to Distortion Measurements about −50 dBm0		13	**17**	dBrnC
LONGITUDINAL BALANCE AND CAPABILITY						
$I_{LLS}1$	Longitudinal Current Capability, Loop Start	I_{LOOP} = 5 mA, D7 = 0, f = 60 Hz, Inject $I_{LLS}1$ into TIP and RING. Device Must Not Detect Off-Hook. Triangular Waveform	**21**			mArms
$I_{LLS}2$	Longitudinal Current Capability, Loop Start	I_{LOOP} = 21 mA, D7 = 0, f = 60 Hz, Inject $I_{LLS}2$ into TIP and RING. Device Must Not Detect On-Hook. Triangular Waveform	**21**			mArms
$I_{LGS}1$	Longitudinal Current Capability, Ground Start	f = 60 Hz, I_{GROUND} = 0 mA, D7 = 1 Triangular Waveform. Inject $I_{LGS}1$ into RING, TIP Open. Device Must Not Detect Off-Hook	**8.5**			mArms
$I_{LGS}2$	Longitudinal Current Capability, Ground Start	I_{GROUND} = 50 mA, f = 60 Hz. Inject $I_{LGS}2$ into RING, TIP Open. Device Must Not Detect On-Hook. Triangular Waveform, D7 = 1	50			mArms

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
LONGITUDINAL BALANCE AND CAPABILITY (Continued)						
BAL2W	2-Wire Longitudinal Balance	IEEE Method 455-1976, I_{LOOP} = 20 mA $I_{LONGITUDINAL}$ = 20 mArms/leg, Measure $V_{METALLIC}$ across TIP-RING				
		f = 62.5 Hz	**61**			dB
		f = 203.125 Hz	**61**	64		dB
		f = 1015.625 Hz	**61**	64		dB
		f = 2015.625 Hz	**61**			dB
		f = 2703.125 Hz	**56**			dB
		f = 3000 Hz	**54**	59		dB
		f = 3406.25 Hz	**51**			dB
POWER SUPPLY REJECTION RATIO						
Unless otherwise specified, Z_{REF} = 900 + 2.16 µF, I_{LOOP} = 20 mA, D2 = 0, D3 = 0						
$PPSR_R$	V_{CC} Power Supply Rejection, Receive	V_{CC} = 5.0 V_{DC} + 164 mVrms				
		f = 328.125 Hz	**30**			dB
		f = 1078.125 Hz	**30**			dB
		f = 3328.125 Hz	**30**			dB
$VPSR_R$	V_{BAT} Power Supply Rejection, Receive	V_{BAT} = −52.0 V_{DC} + 424 mVrms				
		f = 328.125 Hz	**30**			dB
		f = 1078.125 Hz	**40**			dB
		f = 3328.125 Hz	**40**			dB
$PPSR_X$	V_{CC} Power Supply Rejection, Transmit	V_{CC} = 5.0 V_{DC} + 164 mVrms				
		f = 328.125 Hz	**30**			dB
		f = 1078.125 Hz	**30**			dB
		f = 3328.125 Hz	**30**			dB
$VPSR_X$	V_{BAT} Power Supply Rejection, Transmit	V_{BAT} = −52.0 V_{DC} + 424 mVrms				
		f = 328.125 Hz	**30**			dB
		f = 1078.125 Hz	**40**			dB
		f = 3328.125 Hz	**40**			dB
RELAY DRIVERS						
VR_{ON}	Driver On Voltage	I_L = 80 mA			**1**	V
IR_{OFF}	Leakage Current	V_{RELAY} = 40V, Relay Off			**100**	µA
DIGITAL TIMING, PCM INTERFACE (See *Figures 8* and *9*, Notes 4 and 5)						
$1/t_{PMC}$	MCLK Frequency	Clock Frequency Accuracy < ±100 ppm		1.536 1.544 2.048		MHz MHz MHz
t_{WMCH}	Width of MCLK High		**160**			ns
t_{WMCL}	Width of MCLK Low		**160**			ns
$1/t_{PBC}$	BCLK Frequency				**2.048**	MHz
t_{WBCH}	Width of BCLK High		**160**			ns
t_{WBCL}	Width of BCLK Low		**160**			ns

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} = 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SHORT FRAME SYNC MODE *(Figure 8)*						
t_{SFSBCL}	Setup Time from FS High to BCLK Low		**50**			ns
t_{HBCFSL}	Hold Time from BCLK Low to FS Low		**100**			ns
t_{HBCFSH}	Hold Time from BCLK Low to FS High		**0**			ns
t_{DBCDX1}	Delay Time from Bit Clock to Dx Data Valid	C_L = 150 pF plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBCDXz}	Delay Time from BCLK to Dx Disabled	C_L = 50 pF	**50**		**165**	ns
t_{DBCTSL}	Delay Time from BCLK to $\overline{TSx}$ Low	C_L = 150 pF plus 2 LSTTL Loads			**140**	ns
t_{SDRBCL}	Setup Time from D_R to BCLK Low		**50**			ns
t_{HBCDR}	Hold Time from BCLK Low to D_R Valid		**50**			ns
LONG FRAME SYNC MODE *(Figure 9)*						
t_{HBCFSH}	Hold Time from BCLK Low to FS		**0**			ns
t_{SFSBC0}	Setup Time from FS to BCLK Low		**95**			ns
t_{WFSL}	Width of FS Low		**160**			ns
t_{DBCDX0}	Delay Time from BCLK or FS, Whichever Comes Later, to Dx Valid	C_L = 150 pF plus 2 LSTTL Loads	**20**		**165**	ns
t_{DBCDX}	Delay Time from BCLK to Dx Valid	C_L = 150 pF plus 2 LSTTL Loads	**0**		**140**	ns
t_{DBCDXz}	Delay Time from BCLK to Dx Disabled	C_L = 50 pF	**50**		**165**	ns
$t_{DBCDXz0}$	Delay Time from BCLK or FS, Whichever Comes Later, to Dx Disabled	C_L = 50 pF	**20**		**165**	ns
t_{SDRBC}	Setup Time from D_R to BCLK Low		**50**			ns
t_{HBCDR}	Hold Time from BCLK Low to D_R Valid		**50**			ns
DIGITAL TIMING, SERIAL CONTROL INTERFACE (See *Figures 2* and *3*, Notes 4 and 5)						
$1/t_{PCC}$	CCLK Frequency	Frequency Accuracy < ±100 ppm	0.08		**2.048**	MHz
t_{WCCH}	Width of CCLK High		**200**			ns
t_{WCCL}	Width of CCLK Low		**200**			ns
t_{WCSL}	Width of $\overline{CS}$ Low				**100**	µs

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are guaranteed for V_{CC} = 5.0V ±5%, V_{BB} = −5.0V ±5%, V_{BAT} = −42.5V to −56V, T_A = −40°C to +75°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. Typical characteristics are specified at V_{CC} 5.0V, V_{BB} = −5.0V, V_{BAT} = −52V, T_A = 25°C. All digital signals are referenced to GND, all analog signals are referenced to RTN. (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
READ/WRITE, WRITE/READ MODES *(Figure 2)*						
t_{HCCCS}	Hold Time from CCLK to $\overline{CS}$		**100**			ns
t_{SCSCC}	Setup Time from $\overline{CS}$ to CCLK		**100**			ns
t_{DCCCO}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Valid	C_L = 150 pF plus 2 LSTTL Loads			**150**	ns
t_{DCCCOZ}	Delay Time from CCLK or $\overline{CS}$, Whichever Comes Later, to CO Disabled				**150**	ns
t_{SCCCI}	Setup Time from CI to CCLK		**100**			ns
t_{HCICC}	Hold Time from CCLK to CI		**100**			ns
t_{DCSIN}	Delay Time from $\overline{CS}$ Low to $\overline{INTR}$ High	R_L = 1 kΩ from $\overline{INTR}$ to V_{CC}			**200**	ns
QUICK STATUS READ MODE *(Figure 3)*						
t_{HCCCSL}	Hold Time from CCLK to $\overline{CS}$ Low		**100**			ns
t_{SCSCCL}	Setup Time from $\overline{CS}$ to CCLK Low		**100**			ns
t_{DCSCO}	Delay Time from $\overline{CS}$ to CO Valid	C_L = 150 pF plus 2 LSTTL Loads			**150**	ns
t_{DCSCOZ}	Delay Time from $\overline{CS}$ to CO Disabled				**150**	ns

Note 1: See Appendix I for the definition of digital interface parameters.

Note 2: Derate based on T_{JMAX} = 150°C, thermal resistance from junction of bipolar IC to heat spreader = 27°C/W, thermal resistance from heat spreader to ambient is 18°C/W at still air, and 11.5°C/W at 120 ft/min of air velocity.

Note 3: The intent of Ring Trip Non-Detect tests are to insure that ring trip does not occur under the specified conditions even after an essentially infinite period of time. For practical purposes of cost effectively testing the SLIM Subscriber Line Interface Module, the wait time to determine that a false ring trip has not occurred has necessarily been limited to a value which has been determined through characterization to insure that false ring trip never occurs.

Note 4: See Appendix I for the definition and naming conventions used for digital timing parameters.

Note 5: See Table V for the definition of the mneumonics used for the digital timing parameters.

TABLE V. Timing Parameter Mneumonics

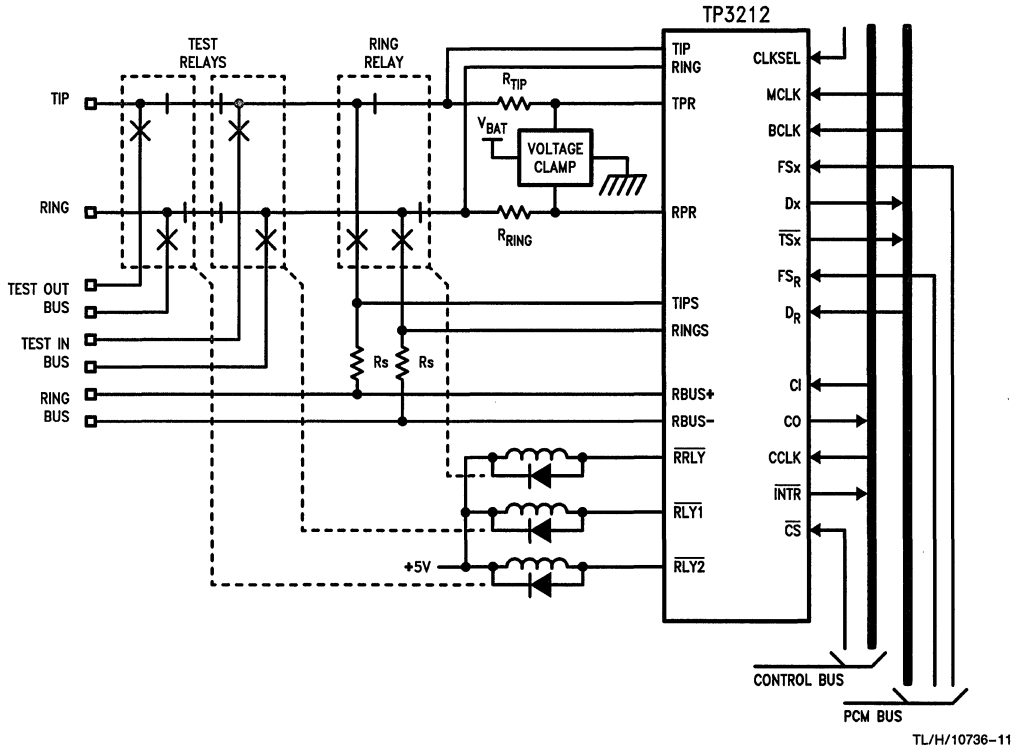
Pin Name	Mneumonic
$\overline{INTR}$	IN
$\overline{CS}$	CS
CO	CO
CI	CI
CCLK	CC
MCLK	MC
BCLK	BC
D_R	DR
Dx	DX
$\overline{TSx}$	TS
FS_R	FS
FSx	FS

Applications Information

TYPICAL LINE CIRCUIT

Relatively few external components are required to implement a DLC POTS line circuit. As shown in *Figure 10*, a complete line circuit is implemented using TP3212 with an external protection network consisting of fuse resistors R_{TIP} and R_{RING}, and a voltage clamp device, two 360Ω ring sensing resistors, ring relay and two test relays. It should be noted that no supply decoupling capacitors are required for each line circuit from ±5V to ground, although the use of one larger electrolytic capacitor may be advisable for each power supply near the point at which it enters the line card.

Protection resistors R_{TIP} and R_{RING} should be nominally 100Ω with matching better than 1%. The selection of R_{TIP} and R_{RING} is important because they are fundamental to the ability of the line circuit to meet lightning and power cross requirements. R_{TIP} and R_{RING} should be designed such that they can withstand level one lightning and power cross requirement, while fusing open when overstressed by level two lightning and power cross. TPR and RPR are protected by the external voltage clamp device to limit the voltage at these two pins to within +2 to −85V. The ring sensing resistors, R_S, are 360Ω which sets the ring trip threshold to about 11 mAdc. The heavy relay current will be returned to GND3 at pin 26.



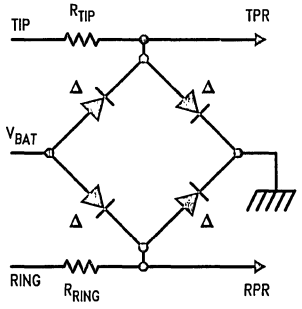
TL/H/10736–11

FIGURE 10. Complete DLC POTS Line Circuit Using TP3212

Applications Information (Continued)

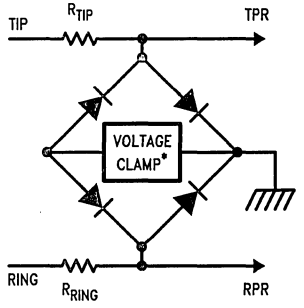
SECONDARY PROTECTION

The high voltage protection network in *Figure 10* consists of resistors R_{TIP}, R_{RING} and a voltage limiting circuit which limits the voltage at TPR and RPR. A number of low cost possibilities for this voltage limit are shown in *Figure 11*. The lowest cost solution is a simple full wave rectifier diode bridge used to clamp the voltage to no more than one or two volts above RTN or below V_{BAT}, provided that the V_{BAT} supply is capable to absorb the power surges. The TIP and RING input terminals of the TP3212 is internally connected in series to two 300 kΩ thick film resistors, which are capable of withstanding power cross and surges.



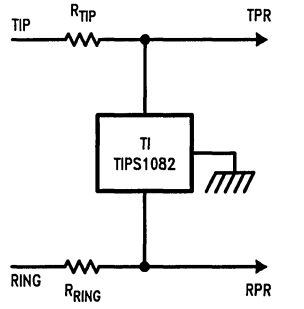
TL/H/10736–12

Δ20 Amp, 100V
20 Amp Surge



TL/H/10736–13

*SGS L5060
Thomson TPC68B

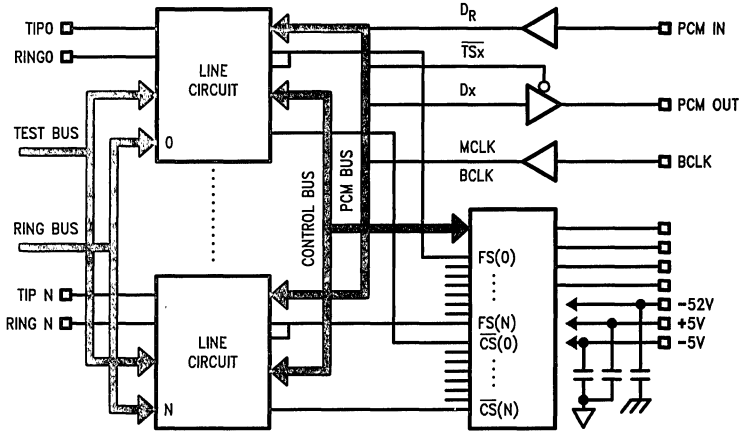


TL/H/10736–14

FIGURE 11. Recommended Secondary Protection Networks

TYPICAL LINE CARD

A complete N-channel line card is illustrated in *Figure 12*. The backplane control interfaces vary greatly in different applications, and this example illustrates a possible arrangement.



TL/H/10736–15

FIGURE 12. Typical N-Channel Linecard

National Semiconductor

TP5116A, TP5116A-1, TP5156A, TP5156A-1 Monolithic CODECs

General Description

The TP5116A and TP5156A are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP5116A is intended for μ-law applications and the TP5156A is for A-law applications.

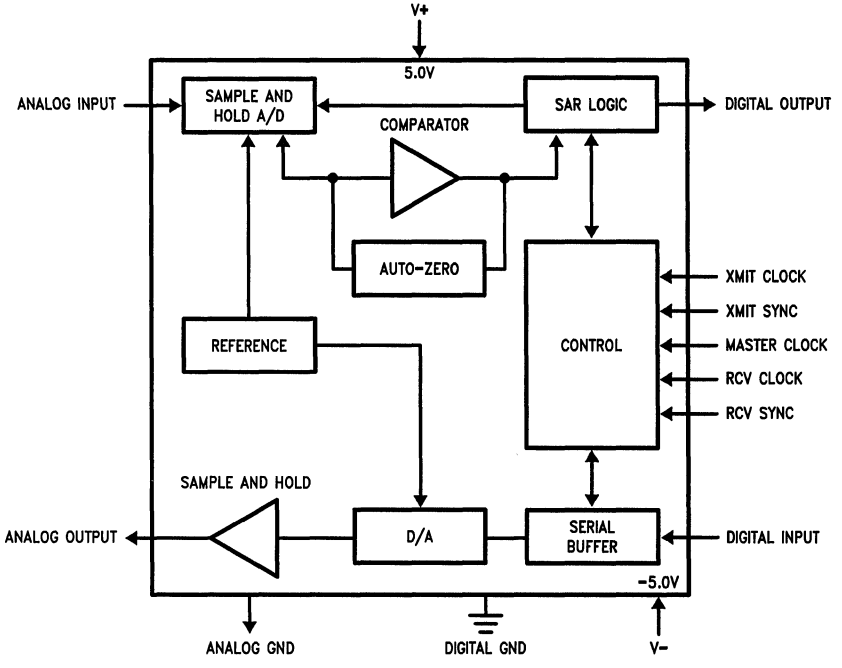
Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, and internal auto-zero circuits. Each device also contains a precision internal voltage reference, eliminating the need for an external reference. There are no internal connections to pins 15 or 16, making them directly interchangeable with CODECs using external reference components.

All devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder, smooths the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- TP5116A—μ-law coding (sign plus magnitude format)
- TP5156A—A-law coding
- Synchronous or asynchronous operation
- Precision voltage reference on-chip
- Internal sample-and-hold capacitors
- Internal auto-zero circuit
- Low operation power—40 mW typical
- ±5V operation
- TTL compatible digital interface

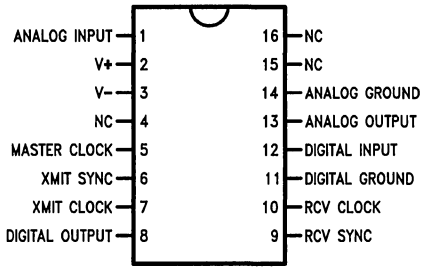
Simplified Block Diagram



TL/H/6663–1

Connection Diagram

Dual-In-Line Package



TL/H/6663–2

Top View

Order Number TP5116AJ or TP5156AJ
See NS Package Number J16A

Description of Pin Functions

Symbol	Function
ANALOG INPUT	ANALOG INPUT to the encoder. This signal will be sampled at the beginning of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
V^+	5V(±5%) Power Supply.
V^-	−5V(±5%) Power Supply.
NC	Unused.
MASTER CLOCK	MASTER CLOCK input used to operate the internal encode and decode sequencers. Should be 1.536 MHz, 1.544 MHz or 2.048 MHz.
XMIT SYNC	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight XMIT CLOCK cycles wide.
XMIT CLOCK	Transmit bit clock input used to shift out the PCM data on DIGITAL OUTPUT. May operate from 64 kHz to 2.048 MHz. May be asynchronous with RCV CLOCK.
DIGITAL OUTPUT	Serial PCM TRI-STATE output from encoder. During the encoder time slot, the PCM code for the previous sample of ANALOG INPUT is shifted out, most significant bit first, on the rising edge of XMIT CLOCK.
RCV SYNC	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally eight RCV CLOCK cycles wide.
RCV CLOCK	Receive bit clock input used to shift in the PCM data on DIGITAL INPUT. May operate from 64 kHz to 2.048 MHz. May be asynchronous with XMIT CLOCK.
DIGITAL GROUND	All digital levels referenced to the DIGITAL GROUND pin.
DIGITAL INPUT	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into DIGITAL INPUT, most significant bit first, on the rising edge of RCV CLOCK.
ANALOG OUTPUT	ANALOG OUTPUT from the decoder. The decoder sample and hold amplifier is updated approximately 15 μs after the end of the decode time slot.
ANALOG GROUND	All analog signals are referenced to the ANALOG GROUND pin.

ENCODING FORMAT AT DIGITAL OUTPUT

	TP5116A Sign + Magnitude								TP5156A A-Law (Includes Even Bit Inversion)							
V_{IN} = +Full-Scale	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1	0
V_{IN} = 0V	1	0	0	0	0	0	0	0	1	1	0	1	0	1	0	1
	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1
V_{IN} = −Full-Scale	0	1	1	1	1	1	1	1	0	0	1	0	1	0	1	0

Functional Description

Approximately 4 μs after the rising edge of the XMIT SYNC pulse, the voltage present on the ANALOG INPUT is sampled and the process of encoding that sample into a PCM code is begun. Simultaneously, the 8-bit PCM code corresponding to the previous sample is shifted out of the DIGITAL OUTPUT, MSB first, on the rising edge of the next eight cycles of the XMIT CLOCK. When XMIT SYNC (which is normally eight XMIT CLOCK cycles long) goes low, the TRI-STATE DIGITAL OUTPUT is returned to the high impedance state. On the TP5116A, the PCM code is in a μ-law sign plus magnitude format. The TP5156A uses the standard A-law coding.

An 8-bit PCM code is shifted into DIGITAL INPUT on the rising edge of the first eight RCV CLOCK pulses after RCV SYNC goes high. RCV SYNC is nominally eight RCV CLOCK cycles wide. Approximately 15 μs after RCV SYNC goes low, the ANALOG OUTPUT is updated to the voltage corresponding to the PCM input code.

All encoding and decoding operations are run from the MASTER CLOCK. MASTER CLOCK should be in the range of 1.536 MHz to 2.048 MHz and must be synchronous with XMIT CLOCK. The XMIT and RCV CLOCK may vary from 64 kHz to 2.048 MHz.

ENCODING DELAY

The encoding process begins immediately at the beginning of the encode time slot and is concluded no later than 18 time slots later. In normal applications, the PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125 μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz MASTER CLOCK, the FS rate could be increased to 15 kHz, reducing the delay from 125 μs to 67 μs.

DECODING DELAY

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 MASTER CLOCK cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or, 81 μs for a 1.544 MHz system with an 8 kHz frame rate or, 76 μs for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

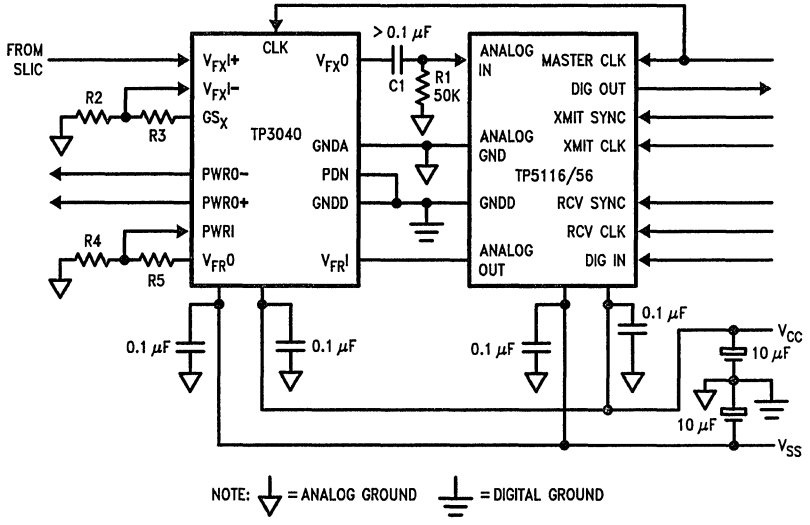
Typical Application

A typical application of these CODECs used in conjunction with the TP3040 PCM filter is shown below. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should be less than 50 kΩ, and the product R1×C1 should exceed 4 ms.

$$\text{XMIT GAIN} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\ \text{dB}$$

$$\text{RCV GAIN} = 20 \times \log\left(\frac{R4}{R4 + R5}\right)$$

The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of these CODECs, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines. For card insertion into a hot connector, care should be taken to insure that GNDA and GNDD are contacted prior to V_{CC} and V_{BB}.



TL/H/6663–5

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Operating Temperature	−25°C to +125°C
Storage Temperature	−65°C to +150°C
V^+ with Respect to DIGITAL GROUND	7V
V^- with Respect to DIGITAL GROUND	−7V
Voltage at Any Analog Input or Output	V^- −0.3V to V^+ +0.3V
Voltage at Any Digital Input or Output	GNDD −0.3V to V^+ + 0.3V
Lead Temperature (Solderdip 10 sec.)	300°C
ESD rating to be determined.	

DC Electrical Characteristics

Unless otherwise noted T_A = 0°C to 70°C, V^+ = 5.0V ±5%, V^- = −5.0V ±5%. Typical characteristics are specified at V^+ = 5.0V,V^- = −5.0V and T_A = 25°C. All digital signals are referenced to DIGITAL GROUND. All analog signals are referenced to ANALOG GROUND. Limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0V < V_{IN} < V^+$	**−10**		**10**	μA
V_{IL}	Input Low Voltage				**0.6**	V
V_{IH}	Input High Voltage		**2.2**			V
V_{OL}	Output Low Voltage	I_{OL} = 3.2 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = 6 mA	2.4			V
ANALOG INTERFACE						
Z_I	Analog Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2			kΩ
Z_O	Output Impedance at Analog Output			10	20	Ω
I_{IN}	Analog Input Bias Current	V_{IN} = 0V	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				50	kΩ
POWER DISSIPATION						
I_{CC1}	Operating Current, V_{CC}			3.5	**8.0**	mA
I_{BB1}	Operating Current, V_{BB}			3.5	**8.0**	mA

AC Electrical Characteristics

Unless otherwise noted, T_A = 25°C, V^+ =5.0V,V^- = −5.0V. The analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL INPUT is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected, limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP5116A is 1.227 Vrms and 1.231 Vrms for the TP5156A. The resulting nominal overload level is 2.5V peak for all devices. All gain measurements for the encode and decode portions of the devices are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute	T_A = 25°C, V^+ = 5V, V^- = −5V TP5116A, TP5156A TP5116A-1, TP5156A-1	 **−0.125** **−0.175**		 **0.125** **0.175**	 dB dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	T_A = 0°C to 70°C	−0.05		0.05	dB

AC Electrical Characteristics (Continued)

Unless otherwise noted, T_A = 25°C, V^+ = 5.0V, V^- = −5.0V. The analog input is a 0 dBm0, 1.02 kHz sine wave. The DIGITAL INPUT is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected. Limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V^+ = 5V ±5%, V^- = −5V±5%	−0.07		0.07	dB
G_{XA}	Transmit Gain, Absolute	T_A = 25°C, V^+ = 5V, V^- = −5V TP5116A, TP5156A TP5116A-1, TP5156A-1	 **−0.125** **−0.175**		 **0.125** **0.175**	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T_A = 0°C to 70°C	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V^+ = 5V ±5%, V^- = −5V ±5%	−0.07		0.07	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−1.0**		 **0.3** **0.2** **0.4** **1.0**	 dB dB dB dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0 0 dBm0 to 3 dBm0 −40 dBm0 to 0 dBm0 −50 dBm0 to −40 dBm0 TP5116A, TP5156A TP5116A-1, TP5156A-1 −55 dBm0 to −50 dBm0	 **−0.3** **−0.2** **−0.4** **−0.475** **−1.0**		 **0.3** **0.2** **0.4** **0.475** **1.0**	 dB dB dB dB dB
STD_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBC dBC dBC
STD_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level −30 dBm0 to 0 dBm0 −40 dBm0 −45 dBm0	 **35** **29** **25**			 dBC dBC dBC
N_R	Receive Idle Channel Noise	D_R = Idle Code			**8**	dBrnC0
N_X	Transmit Idle Channel Noise	TP5116A, VF_X = 0V TP5156A, VF_x = 0V			**13** **−66**	dBrnC0 dBm0p
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, V_{CC} = 5.0 V_{DC} +300 mVrms, f = 1.02 kHz	**50**			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Idle Code V_{CC} = 5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**40**			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, V_{BB} = −5.0 V_{DC} +300 mVrms, f = 1.02 kHz	**50**			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{BB} = −5.0 V_{DC} + 300 mVrms, f = 1.02 kHz	**45**			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			**−75**	dB
CT_{RX}	Receive to Transmit Crosswalk	Transmit Input Level = 0V TP5116A TP5156A			 **−70** **−65** (Note 2)	 dB dB

Note 1: Measured by extrapolation from the distortion test result at −50 dBm0 level.

Note 2: Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Timing Specifications

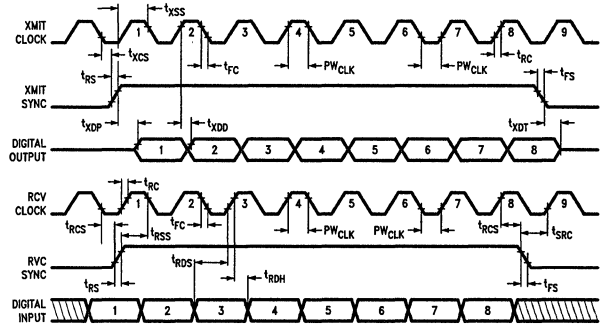
Unless otherwise noted, T_A = 0°C to 70°C, V^+ = +5V±5%, V^- = −5V ± 5%. All digital signals are referenced to DIGITAL GROUND and are measured at V_{IH} and V_{IL} as indicated in the Timing Waveforms. Limits printed in bold characters are guaranteed for V^+ = 5.0V ±5%, V^- = −5.0V ±5%; T_A = 0°C to 70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization. All timing specifications measured at V_{OH} = 2.0V and V_{OL} = 0.7V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_M	MASTER CLOCK Frequency		1.5	2.048	2.1	MHz
F_X, F_R	XMIT, RCV CLOCK Frequency		0.064	2.048	2.1	MHz
PW_{CLK}	Clock Pulse Width	MASTER, XMIT, RCV CLOCKS	150			ns
t_{RC}, t_{FC}	Clock Rise and Fall Time	MASTER, XMIT, RCV CLOCKS			50	ns
t_{RS}, t_{FS}	Sync Pulse Rise and Fall Time	RCV, XMIT, SYNC			50	ns
t_{RCS}, t_{XCS}	Clock to Sync Delay	RCV, XMIT	0			ns
t_{XSS}	XMIT SYNC Set-Up Time		150			ns
t_{XDD}	XMIT Data Delay	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDP}	XMIT Data Present	Load = 100 pF + 2 LSTTL Loads			200	ns
t_{XDT}	XMIT Data TRI-STATE®				150	ns
t_{SRC}	RCV CLOCK to RCV SYNC Delay		0			ns
t_{RDS}	RCV Data Set-Up Time		0			ns
t_{RSS}	RCV SYNC Set-Up Time		150			ns
t_{RDH}	RCV Data Hold Time		100			ns
t_{XSL}	XMIT SYNC Low Time	64 kHz Operation	300			ns
t_{RSL}	RCV SYNC Low Time	64 kHz Operation	17			(Note 3)

Note 3: RCV SYNC must remain low for at least 17 cycles of MASTER CLOCK, each frame.

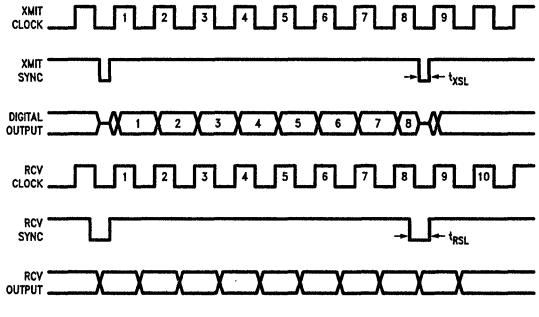
Timing Waveforms

72 kHz or Greater Operation



TL/H/6663–3

64 kHz Operation



TL/H/6663–4

Section 2

ISDN Components

Section 2 Contents

Introduction to National Semiconductor Basic Access I.C. Set 2-3
TP3401, TP3402, TP3403 DASL Digital Adapter for Subscriber Loops 2-8
TP3410 ISDN Basic Access Echo-Cancelling 2B1Q U Transceiver 2-21
TP3420 ISDN S/T Interface Device 2-51
TP3421 ISDN S/T Interface Device with GCI (General Circuit Interface) 2-69
TP3451 ISDN HDLC and GCI Controller 2-87
TP3460 ISDN R Interface Device USART 2-113
TP34XX MICROWIRE Interface Device (MID) 2-128
HPC16400E High-Performance Communications microController 2-129

Introduction To National Semiconductor Basic Access I. C. Set

In developing the architecture of this ISDN chip set, National's major objective has been to create a flexible set of building blocks which provide elegant and cost-effective solutions for a wide range of applications. With just a few highly integrated devices, a broad spectrum of ISDN equipment can be designed, ranging from Central Office and PBX line cards to X.25 and ISDN Terminals and telephones, PC and Terminal Adapters, packet-mode statistical multiplexers, NT-1's and other ISDN equipment.

One of the keys to this flexibility is the concept that device functions in the chip set should be specifically aligned with the first 3 layers of the ISO 7 layer Protocol Reference Model. Thus, National's chip set has a distinct partitioning of functions into several transceivers which provide the bit-level transport for Layer 1, (the Physical Layer), while the functions of Layer 2, (the Data Link Layer), and Layer 3, (the Network Layer), are supported entirely by a single microprocessor. All devices in the chip set, together with other standard components such as COMBOs, can be interconnected via a common serial interface without the need for any "glue" components. The result is a very elegant architecture offering many advantages including the following:

- A high degree of modularity with minimal component count
- The same transceiver at both ends of a loop
- No interrupts for D-Channel flow control
- Powerful Packet buffer management

Other chip set architectures, which divide a layer into some functions in one device and the rest in other devices, are unable to offer all these advantages.

ISDN Chip Set Partitioning

<table>
<tr><th>ISO Layer</th><th>National</th><th colspan="2">Others</th></tr>
<tr><td>4–7</td><td>NS32322</td><td></td><td></td></tr>
<tr><td>3</td><td rowspan="2">HPC16400</td><td>Chip C</td><td rowspan="2">Chip B</td></tr>
<tr><td>2</td><td>Chip B</td></tr>
<tr><td>1</td><td>TP3401 DASL
or TP3410 EC or
TP3420 SID</td><td>Chip A</td><td>Chip A</td></tr>
</table>

NSC Solutions for Layer 1

National's solution for Layer 1 consists of 3 CMOS transceivers, which cover a wide variety of twisted-pair applications for ISDN Basic Access. Each transceiver is capable of transmitting and receiving 2 'B' channels plus 1 'D' channel, and has mode selections to enable it to operate at either end of the loop.

Transceiver Number 1

The TP3401 Digital Adapter for Subscriber Loops (DASL) is a low-cost burst-mode transceiver for 2 wire PBX and private network loops up to 6 kft in range. Scrambled Alternate Mark Inversion coding is used, together with adaptive equalization and timing-recovery, to ensure low bit error rates on a wide variety of cable types. All activation and loop timing control circuitry is also included.

Transceiver Number 2

The TP3410 Echo-canceller is a 2-wire transceiver designed to meet the rigorous requirements of the ANSI 2B1Q Standard for the 'U' interface.

Transceiver Number 3

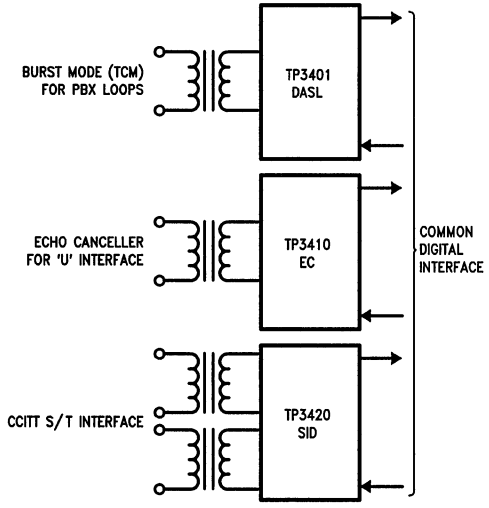
The TP3420 'S' Interface Device (SID), is a 4-wire transceiver which includes all the Layer 1 functions specified in CCITT Recommendation I.430. In addition, the TP3420 includes noise filtering and adaptive equalization, as well as a high resolution digital phase-locked loop, to provide transmission performance far in excess of that specified in I.430. All Activation and 'D' channel access sequences are handled automatically without the need to invoke any action from a microprocessor.

Digital Chip to Chip Interfaces

To retain the flexibility of interfacing components from this chip set with a variety of other products, two digital interfaces are provided on each device. One is for the synchronous transfer of 'B' and 'D' channel information in any of several popular multiplexed serial formats. This means that National's chip to chip interface is all encompassing of proprietary frame structures such as the GCI, IDL, ST-BUS and more.

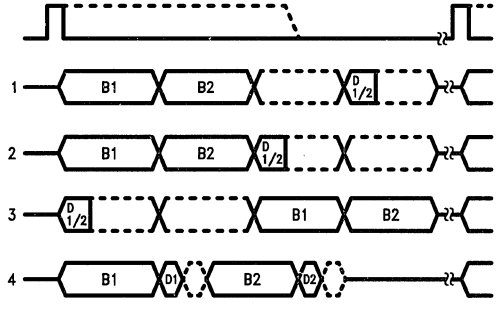
A second interface, for device mode control, e.g. power up/down, setting loopbacks etc., uses the popular MICROWIRE/PLUS™. MICROWIRE/PLUS is a synchronous serial data transfer between a microcontroller and one or more peripheral devices. National's HPC and COPS™ microcontroller families, together with a broad range of peripheral devices, support this interface, which is also easy to emulate with any microprocessor.

NSC ISDN Transceiver Chip Set



TL/X/0008–1

Popular Frame Structures Addressed by NSC ISDN Devices



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NSC Solutions for Layers 2 and 3

National has developed an extremely powerful solution for implementing various protocols for both Layer 2 (Data Link Layer) and Layer 3 (Network Layer), including X.25 LAPB and LAPD (Q.921 and Q.931), together with the capability of several packet-mode Terminal Adaption schemes*. A single device incorporates all the processing for these functions: the HPC16400E. One of National's growing family of 16-bit single chip CMOS microcontrollers, the HPC16400E is based on a high-speed (17 MHz) 16-bit CPU "core". To this core has been added 2 full HDLC formatters supported by DMA to external memory, and a UART.

This set of features makes the HPC16400E an ideal processor for running all the functions of an ISDN Terminal Adapter, TE or telephone, or the communications port of a high-end terminal. In a typical application, one of the HDLC channels may be dedicated to running the LAPD protocol in the 'D' channel, while the other provides packet-mode access to one of the 'B' channels. The UART would serve as an RS232 interface running at any of the standard synchronous or asynchronous rates up to 128 kbaud. A serial interface decoder allows either or both HDLC controllers to be directly interfaced to any of the 3 Layer 1 transceivers or to a variety of backplanes, line-card controllers and other devices using time-division multiplexed serial interfaces.

Because of the large ROM and RAM requirements for Layer 3 and the Control Field procedures of Layer 2 in LAPB and LAPD protocols, the HPC16400E has 256 bytes of RAM and no internal ROM for storage of user variables. Packet storage RAM and all user ROM is off-chip, this is by far the most cost-effective and flexible combination. A multiplexed bus to external memory provides direct addressing for up to 64 kbytes of memory, and on-chip I/O allows for expanded addressing for up to 544 kbytes of memory.

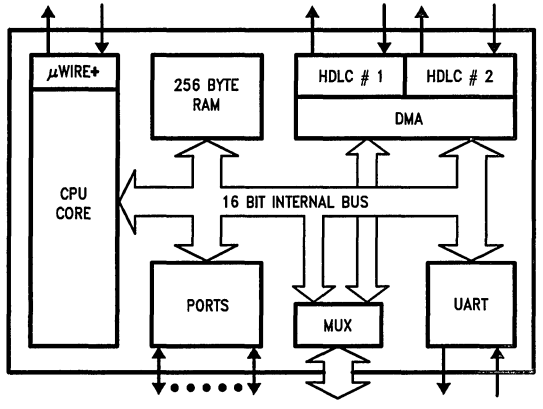
The HDLC controllers on the HPC16400E allow continuous HDLC data rates up to 4.1 Mb/s to be used. In addition to handling all Layer 2 framing, the HDLC circuitry includes automatic multiple address recognition to support, for example, multiple TEI's in LAPD. Furthermore, the DMA controller provides several register sets for packet RAM management with minimal CPU intervention, including "chaining" of successive packets. This integrated design achieves a high throughput of packet data without the need for costly FIFO's and external interrupts, thereby minimizing the impact of packet handling on CPU time.

In many applications a number of other peripheral functions must also be provided, such as sensing switches or scanning a small keyboard, interfacing to a display controller etc. A number of extra I/O ports and a MICROWIRE/PLUS serial data expansion interface are available on the HPC16400E to service these functions. In addition, 4 user configurable 16 bit timer-counters simplify the many timeouts required to manage such a system, including the default timers specified in the various protocol specifications.

Another National product, the TP3451, also provides layer 2 support. The TP3451 is a single channel HDLC controller. LAPB and LAPD protocols are supported on the chip, and 64-byte FIFOs are implemented in each of the transmit and receive paths. The device also acts as a full GCI controller. It may be used in conjunction with the HPC in applications requiring three HDLC channels.

*For example, as per DMI Modes 2 and 3.

HPC16400E Simplified Block Diagram

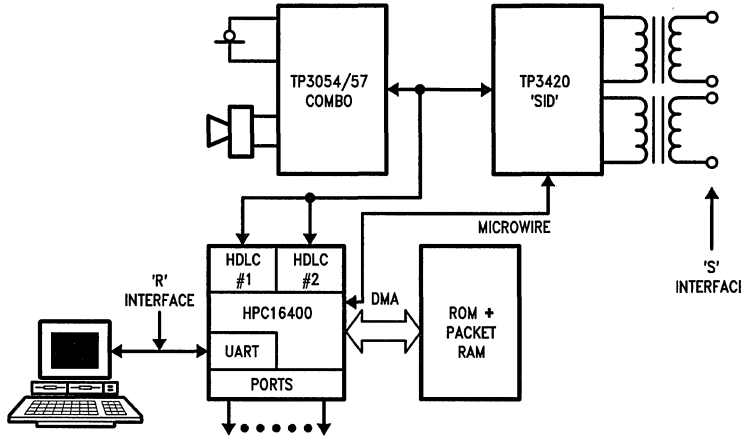


TL/X/0008–3

NSC Solutions: Systems Level

Building an ISDN TE or TA

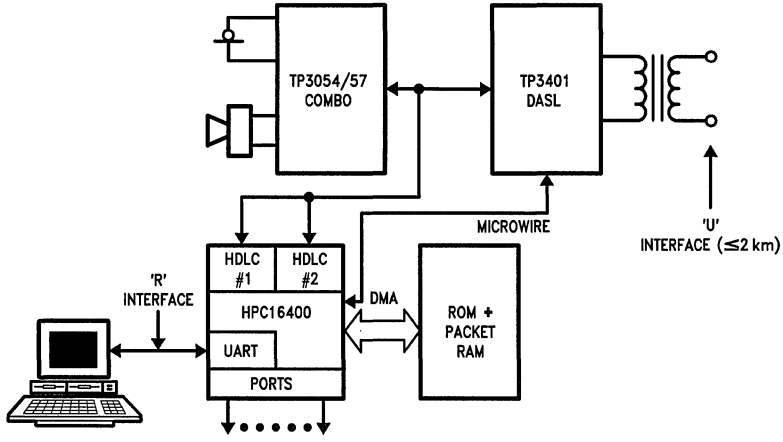
Shown below is a typical application of the chip set in a Basic Access TE, which offers one voice channel and an RS232 interface to support an external terminal. The TP3420 'S' Interface Device ensures that the system is compatible with any 'S' or 'T' standard jack socket and provides the multiplexing for the other devices operating in the 'B' and 'D' channels. All timing for the TE is derived by the TP3420 from the received line signal. In a typical application, LAPD signalling in the 'D' channel is provided via HDLC #1 on the HPC16400E. HDLC #2 is working in conjunction with the UART to provide X.25 or LAPD packet-mode data in a 'B' channel at 64 kb/s. Terminal Adaption of both the data and the terminal handshaking signals is performed by the HPC16400E via the UART and HDLC controller #2, which can use either of the 'B' channels. V.120 (for a single channel) can be supported using this method, with the necessary data buffers set up in internal RAM. The other 'B' channel is occupied by the TP3054/7 PCM COMBO providing the digitized voice channel.



TL/X/0008–4

PBX 2 Wire Terminals

The following example shows how simple it is to convert an 'S' Interface terminal, which requires 2 twisted pairs, to a terminal using only a single pair by replacing the TP3420 SID with a TP3401 DASL. The clean partitioning of device functions makes this possible with no other changes to the design.



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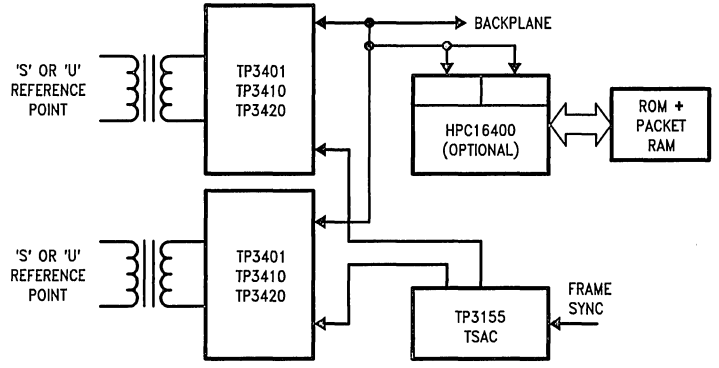
NSC Solutions: Systems Level

Basic Access Line Cards

For operation on a line card in a C.O., PABX or NT-2, each of the 3 transceiver devices can be set to operate as the timing master for the loop, being synchronized to the system clock and controlling all loop frame timing. If programmable time-slot assignment is required, the TP3410 U interface includes this function on-chip. For the TP3401 DASL and TP3420 SID, the TP3155 TSAC provides 8 individually programmable frame sync pulse outputs locked to a common frame marker. 'B' channels can be interfaced to standard backplane interfaces, while 'D' channels can be either multiplexed on and off the card for processing or can undergo Layer 2 processing on the card itself.

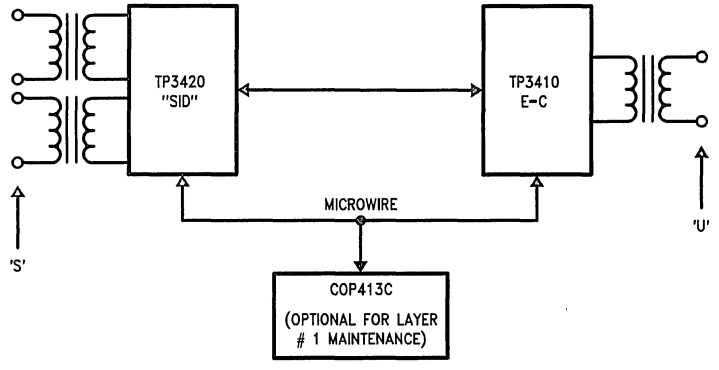
For the latter method, one HPC16400E handles Layer 2 framing for 2 basic access lines. In this manner, packets are first identified as data or signalling type by analysis of the SAPI field, with data packets being routed separately to a packet switch access node. If required, signalling packets can undergo protocol conversion in the HPC to an existing internal switch control protocol.



TL/X/0008–6

Building an NT-1

An NT-1 Network Termination is defined as a Layer 1 device only, which converts the 2-wire long-haul 'U' interface to the limited distance 4-wire 'S' interface. It has no capability for intercepting higher layers of the 'D' channel protocol. As such, it is built simply by connecting a TP3420 SID, configured in NT (or Master) mode, to a TP3410 Echo-canceller operating in Slave mode. Sharing a common 15.36 MHz crystal, these devices pass 'B' and 'D' channel information across the standard 4-wire interface. Layer 1 maintenance protocols across both the 'U' and the 'S/T' interfaces, which are as of yet not definitively specified by most adminstrations, may be handled by a low cost 8-Bit COPS™ Microcontroller via its Microwire Interface.



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National Semiconductor

PRELIMINARY

TP3401, TP3402, TP3403
DASL Digital Adapter for Subscriber Loops

General Description

The TP3401, TP3402 and TP3403 are complete monolithic transceivers for data transmission on twisted pair subscriber loops. They are built on National's double poly microCMOS process, and require only a single +5 Volt supply. Alternate Mark Inversion (AMI) line coding, in which binary '1's are alternately transmitted as a positive pulse then a negative pulse, is used to ensure low error rates in the presence of noise with lower emi radiation than other codes such as Bi-phase (Manchester).

Full-duplex transmission at 144 kb/s is achieved on a single twisted wire pair using a burst-mode technique (Time Compression Multiplexed). Thus the device operates as an ISDN 'U' Interface for short loop applications, typically in a PBX environment, providing transmission for 2 B channels and 1 D channel. On #24 cable, the range is at least 1.8 km (6k ft).

System timing is based on a Master/Slave configuration, with the line card end being the Master which controls loop timing and synchronisation. All timing sequences necessary for loop activation and de-activation are generated on-chip.

Selection of Master and Slave mode operation is programmed via the Microwire Control Interface.

A 2.048 MHz clock, which may be synchronized to the system clock, controls all transmission-related timing functions.

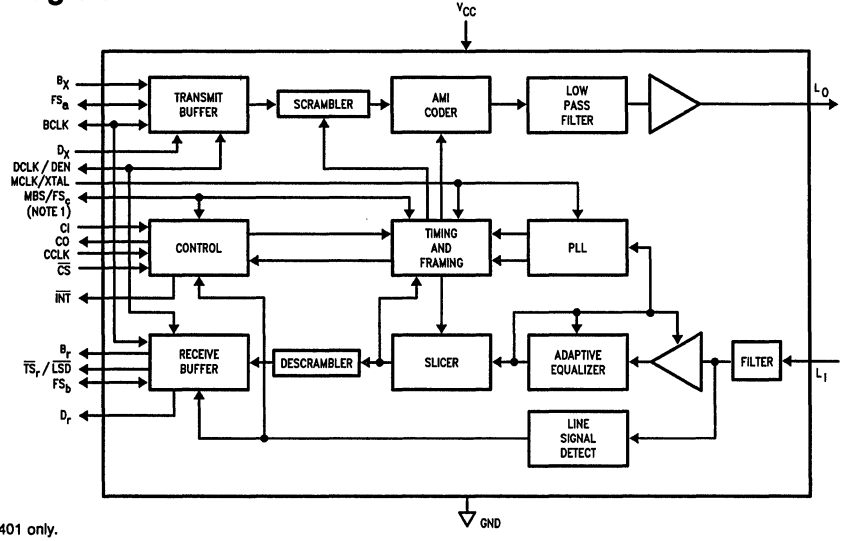
For the TP3401, this clock must be provided from an external source; the TP3402 includes an oscillator circuit requiring an external crystal. The TP3403 includes the functions of both the TP3401 and the TP3402.

Features

Complete ISDN PBX 2-Wire Data Transceiver including:

- 2 B plus D channel interface for PBX U' Interface
- 144 kb/s full-duplex on 1 twisted pair using Burst Mode
- Loop range up to 6 kft (#24AWG)
- Alternate Mark Inversion coding with transmit filter and scrambler for low emi radiation
- Adaptive line equalizer
- On-chip timing recovery, no external components
- Standard TDM interface for B channels
- Separate interface for D channel
- 2.048 MHz master clock
- Driver for line transformer
- 4 loop-back test modes
- Single +5V supply
- MICROWIRE™ compatible serial control interface
- Applications in:
  - PBX Line Cards
  - Terminals
  - Regenerators
- Available in both 20-pin DIP and 28-pin PLCC

Block Diagram

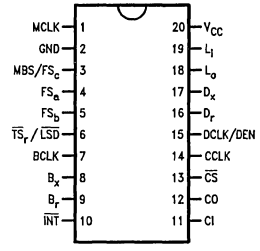


Note 1: TP3401 only.

TL/H/9264–1

Connection Diagram

TP3401 DASL



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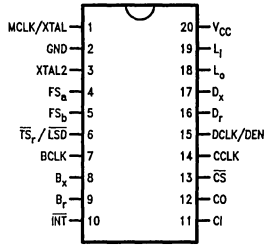
Order Number TP3401J
See NS Package Number J20A

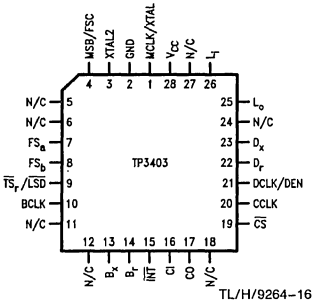
TP3402 DASL



TL/H/9264-15

Order Number TP3402J
See NS Package Number J20A

TP3403 Package Information



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Order Number TP3403V
See NS Package Number V28A

Pin Descriptions

Name	Description
GND	Negative power supply pin, normally 0V. All analog and digital signals are referred to this pin.
V_{CC}	Positive power supply input, which must be $+5V \pm 5\%$.
MCLK (TP3401 only)	The 2.048 MHz Master Clock input, which requires a CMOS logic level clock input from a stable source. Must be synchronous with BCLK.
MCLK/XTAL (TP3402/3403 only)	This pin is the 2.048 MHz Master Clock input, which requires either a crystal to be connected between this pin and XTAL2 or a CMOS logic level clock from a stable source, which must be synchronous with BCLK.
XTAL2 (TP3402 and TP3403 only)	This pin is the output side of the oscillator amplifier.
MBS/FS_C (TP3401 and TP3403 only)	In Master Mode, this pin is the Master Burst Sync input, which may be clocked at 4 kHz to synchronize Transmit bursts from a number of devices at the Master end only. The 4 kHz should be nominally a square wave signal. In Slave mode, this pin is a short Frame Sync output, suitable for driving another DASL in Master Mode to provide a regenerator (i.e. range-extender) capability.
BCLK	Bit Clock logic signal which determines the data shift rate for B channel data on the digital interface side of the device. In Master mode this pin is an input which may be any multiple of 8 kHz from 256 kHz to 2.048 MHz, but must be synchronous with MCLK. In Slave mode this pin is an output at 2.048 MHz.
FS_a	In Master mode only, this pin is the Transmit Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time for transmit B channel data into B_X; FS_a must be synchronous with BCLK and MCLK. In Slave mode only, this pin is a digital output pulse which indicates the 8-bit periods of the B1 channel data transfer at both B_X and B_r.
FS_b	In Master mode only, this pin is the Receive Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time of the device for receive B channel data out from B_r; FS_b must be synchronous with BCLK and MCLK. In Slave mode only, this pin is a digital output pulse which indicates the 8-bit periods of the B2 channel data transfer at both B_X and B_r.
B_X	Digital input for B1 and B2 channel data to be transmitted to the line; must be synchronous with BCLK.
B_r	Digital output for B1 and B2 channel data received from the line.
$\overline{TS_r}/\overline{LSD}$	In Master mode only, this pin is an open-drain output which is normally high impedance but pulls low during both B channel active receive time slots. In Slave mode only, this pin is an output which is normally high impedance and pulls low when a valid line signal is received.
D_X	Digital input for D channel data to be transmitted to the line; must be synchronous with DCLK.
D_r	Digital output for D channel data received from the line.
DCLK/DEN	In Master mode this pin is an input for the 16 kHz serial shift clock for D channel data on D_X and D_r, which should be synchronous with BCLK. It may also be re-configured via the Control Register to act as an enable input for clocking the D channel interface synchronized to BCLK. In Slave mode this is a 16 kHz clock output for D channel data.

*Crystal specifications: 2.048 MHz parallel resonant, $R_S \leq 100\Omega$ with a 20 pF load. Crystal tolerance should be ± 75 ppm for aging and temperature.

2

Pin Descriptions (Continued)

Name	Description
CI	MICROWIRE control channel serial data input.
CO	MICROWIRE control channel serial data output.
CCLK	Clock input for the MICROWIRE control channel.
$\overline{CS}$	Chip Select input which enables the MICROWIRE control channel data to be shifted in and out when pulled low. When high, this pin inhibits the MICROWIRE interface.
$\overline{INT}$	Interrupt output, a latched output signal which is normally high-impedance and goes low to indicate a change of status of the loop transmission system. This latch is cleared when the Status Register is read by the microprocessor.
L_o	Transmit AMI signal output to the line transformer. This pin is capable of driving a load impedance $\geq 60\Omega$.
L_i	Receive AMI signal input from the line transformer. This is a high impedance input which requires an external line termination impedance.

Functional Description

POWER-UP/POWER-DOWN CONTROL

Following the initial application of power, the DASL enters the power-down (de-activated) state, in which all the internal circuits are inactive and in a low power state except for the line-signal detect circuit and the necessary bias circuit; the line output L_o is in a low impedance state and all digital outputs are inactive. All bits in the Control Register power-up initially set to '0', so that the device always initializes as the Master end. Thus, at the Slave end, a control word must be written through the MICROWIRE port to select Slave mode. While powered-down, the Line-Signal Detect circuits in both Master and Slave devices continually monitor the line, to enable loop transmission to be initiated from either end.

To power-up the device and initiate activation, bit C6 in the Control Register must be set high. Setting C6 low de-activates the loop and power-down the device, see Table I.

TABLE I. Power-Up/Power-Down Control (TP3401 Only)

MBS/FS_c Pin I/P at Master	C6 State	Action
4 kHz or 1	0	Powered-down, Line-Signal Detect active
1	1	Powered-up, sending bursts synchronized to FS_a at Master, or received burst at Slave
4 kHz	1	Powered-up, sending bursts synchronized to MBS at Master, or received burst at Slave

LINE TRANSMIT SECTION

Alternate Mark Inversion (AMI) line coding is used on the DASL because of its spectral efficiency and null dc energy content. All transmitted bits, excluding the start bit, are scrambled by a 9-bit scrambler to provide good spectral spreading with a strong timing content. The scrambler feedback polynomial is:

$$x^9 + x^5 + 1.$$

Pulse shaping is obtained by means of a raised cosine switched-capacitor filter, in order to limit rf energy and crosstalk while minimizing inter-symbol interference (isi). *Figure 3* shows the pulse shape at the L_o output, while a template for the typical power spectrum transmitted to the line with random data is shown in *Figure 4*.

The line-driver output, L_o, is designed to drive a transformer through a capacitor and termination resistor. A 1:1 transformer, terminated in 100Ω, results in a signal amplitude of typically 1.3V pk-pk on the line. Over-voltage protection must be included in the interface circuit.

LINE RECEIVE SECTION

The front-end of the receive section consists of a continuous anti-alias filter followed by a switched-capacitor low-pass filter designed to limit the noise bandwidth with minimum intersymbol interference. To correct pulse attenuation and distortion caused by the transmission line an AGC circuit and first-order equalizer adapt to the received pulse shape, thus restoring a "flat" channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

From the equalized output a DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 2.048 MHz. At the Master end of the loop this reference is the network clock (BCLK), which controls all transmit functions; the DPLL clock is used only for received data sampling. At the Slave end, however, a 2.048 MHz crystal is required to generate a stable local oscillator which is used as a reference by the DPLL to run both the receive and transmit sides of the DASL device.

Following detection of the recovered symbols, the received data is de-scrambled by the same x^9+x^5+1 polynomial and presented to the digital system interface circuit.

When the device is de-activated, a Line-Signal Detect circuit remains powered-up to detect the presence of incoming bursts if the far-end starts to activate the loop. From a "cold" start, acquisition of bit timing and equalizer convergence with random scrambled data takes approximately 25 ms at each end of the loop. Full loop burst synchronization is achieved approximately 50 ms after the "activate" command at the originating end.

Functional Description (Continued)

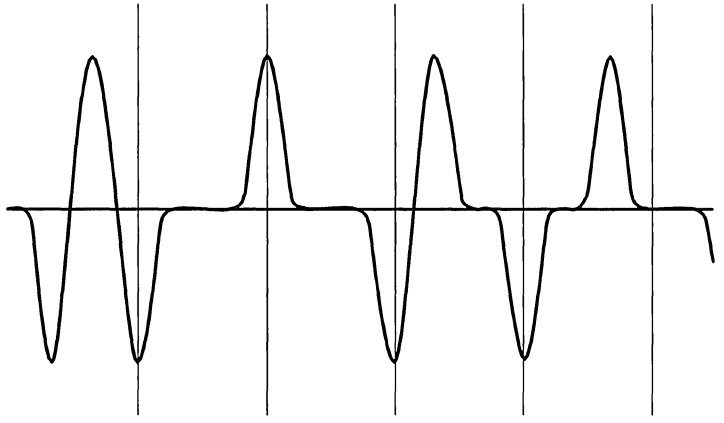

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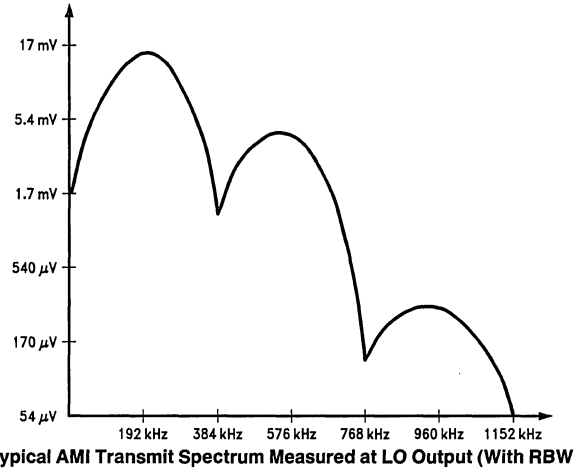
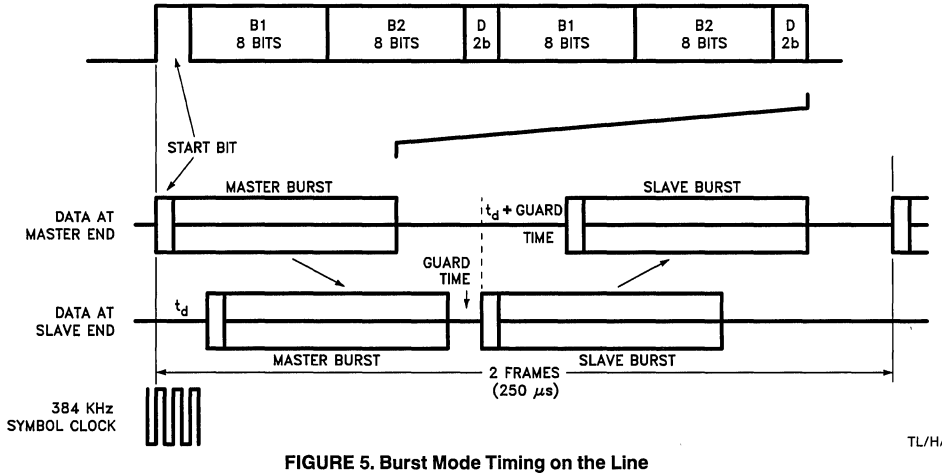
FIGURE 3. Typical AMI Waveform at L_O



TL/H/9264-4

FIGURE 4. Typical AMI Transmit Spectrum Measured at LO Output (With RBW = 100 Hz).



TL/H/9264-5

FIGURE 5. Burst Mode Timing on the Line

Functional Description (Continued)

BURST MODE OPERATION

For full-duplex operation over a single twisted-pair, burst mode timing is used, with the line-card (exchange) end of the link acting as the timing Master.

Each burst from the Master consists of the B1, B2 and D channel data from 2 consecutive frames combined in the format shown in *Figure 5*. During transmit bursts the Master's receiver input is inhibited to avoid disturbing the adaptive circuits. The Slave's receiver is enabled at this time and it synchronizes to the start bit of the burst, which is always an unscrambled '1' (of the opposite polarity to the last '1' sent in the previous burst). When the Slave detects that 36 bits following the start bit have been received, it disables the receiver input, waits 6 line symbol periods to match the other end settling guard time, and then begins to transmit its burst back towards the Master, which by this time has enabled its receiver input. The burst repetition rate is thus 4 kHz, which can either free-run or be locked to a synchronizing signal at the Master end by means of the MBS input (TP3401 only), (See *Figure 10*). In the latter case, with all Master-end transmitters in a system synchronized together, near-end crosstalk between pairs in the same cable binder may be eliminated, with a consequent increase in signal-to-noise ratio (SNR).

ACTIVATION AND LOOP SYNCHRONIZATION

Activation (i.e. power-up and loop synchronization) may be initiated from either end of the loop. If the Master is activating the loop, it sends normal bursts of scrambled '1's, which are detected by the Slave's line-signal detect circuit, causing it to set C0 = 1 in the Status Register, and pull the $\overline{INT}$ pin low. Pin 6, the $\overline{LSD}$ pin, also pulls low. To proceed with Activation, the device must be powered up by writing to the Control Register with C6 = 1. The Slave then replies with bursts of scrambled '1's synchronized to received bursts, and the flywheel circuit at each end searches for 4 consecutive correctly formatted receive bursts to acquire full loop synchronization. Each receiver indicates when it is correctly in sync with received bursts by setting the C1 bit in the Status Register high and pulling $\overline{INT}$ low.

To activate the loop from the Slave end, bit C6 in the Control Register must be set high, which will power-up the device and begin transmission of alternate bursts i.e., the burst repetition rate is 2 kHz, not 4 kHz. At this point the Slave is running from its local oscillator and is not receiving any sync information from the Master. When the Master's line-signal detect circuit recognizes this "wake-up" signal, the Master is activated and begins to transmit bursts, synchronized, as normal, to the MBS or FS_a input with a 4 kHz repetition rate. This enables the Slave's receiver to correctly identify burst timing from the Master and to re-synchronize its own burst transmissions to those it receives. The flywheel circuits then acquire full loop sync as described earlier.

Loop synchronization is considered to be lost if the flywheel finds 4 consecutive receive burst "windows" (i.e. where a receive burst should have arrived based on timing from previous bursts) do not contain valid bursts. At this point bit C1 in the Status Register is set low, the $\overline{INT}$ output is set low and the receiver searches to re-acquire loop sync.

DIGITAL SYSTEM INTERFACE

The digital system interface on the DASL separates B and D channel information onto different pins to provide maximum flexibility. On the B channel interface, phase skew between transmit and receive directions may be accommodated at the Master end since separate frame sync inputs, Fs_a and Fs_b, are provided. Each of these synchronizes a counter which gates the transfer of B1 and B2 channels in consecutive time-slots across the digital interface; since the counters are edge-synchronized the duration of the F_s input signals may vary from a single-bit pulse to a square-wave. The serial shift rate is determined by the BCLK input, and may be any frequency from 128 kHz to 2.048 MHz, as shown in *Figure 6.*

At the Slave end, both Fs_a and Fs_b are outputs. Fs_a goes high for 8 cycles of BCLK coincident with the 8 bits of the B1 channel in both Transmit and Receive directions. Fs_b goes high for the next 8 cycles of BCLK, which are coincident with the 8 bits of the B2 channel in both Transmit and Receive directions. BCLK is also an output at 2.048 MHz, the serial data shift rate, as shown in *Figure 7.* Data may be exchanged between the B1 and B2 channels as it passes through the device, by setting Control bit C0 = 1. An additional Frame Sync output, FS_c, is provided to enable a regenerator to be built by connecting a DASL in Slave Mode to a DASL in Master Mode. The FS_c output from the Slave directly drives the FS_a and FS_b inputs on the Master.

D channel information, being packet-mode, requires no synchronizing input. This interface consists of the transmit data input, D_x, receive data output, D_r, and 16 kHz serial shift clock DCLK, which is an input at the Master end and an output at the Slave end. Data shifts into D_x on falling edges of DCLK and out from D_r on rising edges, as shown in *Figure 11.* DCLK should be Synchronous with BCLK.

An alternative function of the DCLK/DEN pin allows D_x and D_r to be clocked at the same rate as BCLK at the Master end only. By setting bit C1 in the Control Register to a 1, DCLK/DEN becomes an input for an enabling pulse to gate 2 cycles of BCLK for shifting the 2 D bits per frame. Thus, at the Master end, the D channel bits can be interfaced to a TDM bus and assigned to a time-slot (the same time-slot for both transmit and receive), as shown in *Figure 12.*

CONTROL INTERFACE

A serial interface, which can be clocked independently from the B and D channel system interfaces, is provided for microprocessor control of various functions on the DASL device. All data transfers consist of a single byte shifted into the Control Register via CI simultaneous with a single byte shifted out from the Status Register via CO, see *Figure 13.* Data shifts in to CI on rising edges of CCLK and out from CO on falling edges when $\overline{CS}$ is pulled low for 8 cycles of CCLK. An Interrupt output, $\overline{INT}$ goes low to alert the microprocessor whenever a change in one of the status bits, C1 and/or C0 has occurred. This latched output is cleared high following the first CCLK pulse when $\overline{CS}$ is low. No interrupt is generated when status bit C2 (bipolar violation) goes high, however. This bit is set whenever 1 or more violations of the AMI coding rule is received, and cleared everytime the $\overline{CS}$ is pulsed. Statistics on the line bit error rate can be accumulated by regularly polling this bit.

When reading the CO pin, data is always clocked into the Control Register; therefore the CI data word should repeat the previous instruction if no change to the device mode is intended.

Figure 13 shows the timing for this interface, and Table II lists the control functions and status indicators.

TABLE II. Control and Status Register Functions

Bit	State	Control Register Function	Status Register Function
C7	0	Master Mode	Read Back C7 from Control Register
	1	Slave Mode	Read Back C7 from Control Register
C6	0	Deactivate and Power Down	Read Back C6 from Control Register
	1	Power Up and Activate	Read Back C6 from Control Register
C5	0	Normal Through Connection	Read Back C5 from Control Register
	1	Loopback to Digital Interface	Read Back C5 from Control Register
C4	0	Normal Through Connection	Read Back C4 from Control Register
	1	Loopback B1 + B2 + D to Line (Note 1)	Read Back C4 from Control Register
C3	0	Normal Through Connection	Read Back C3 from Control Register
	1	Loopback B1 Only to Line (Note 1)	Read Back C3 from Control Register
C2	0	Normal Through Connection	No Error
	1	Loopback B2 Only to Line (Note 1)	Bipolar Violation Since Last READ (Note 2)
C1	0	DCLK/DEN pin = 16 kHz Clock	Out-Of-Sync
	1	DCLK/DEN pin = D Channel Enable (Note 3)	Loop In-Sync and Activation Complete
C0	0	B1/B2 Channels Direct	No Line Signal at Receiver Input
	1	B1/B2 Channels Exchanged	Line Signal Present at Receiver Input

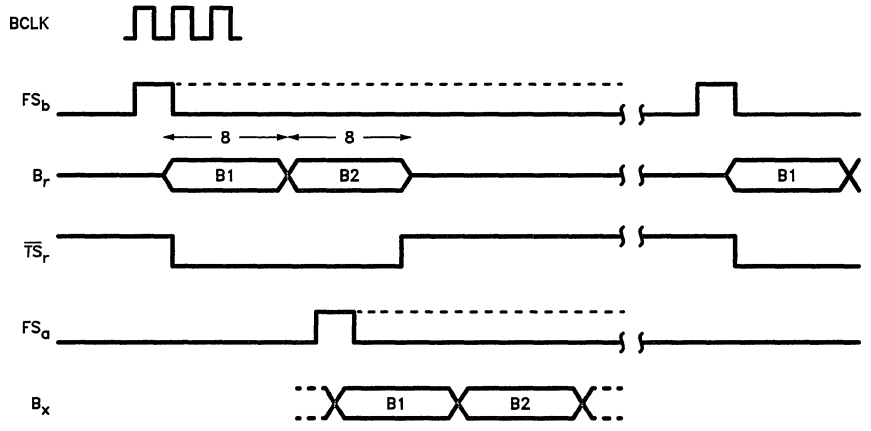
Note 1: Receive data active.

Note 2: After the device is in sync.

Note 3: In Master mode only.

Note 4: C7 is the first bit clocked in and out of the device.

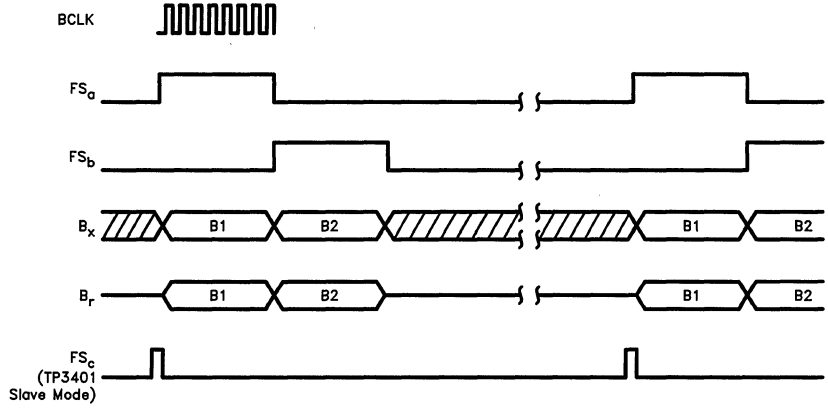
Timing Diagrams



TL/H/9264–6

FIGURE 6. B Channel Interface Timing: Master Mode

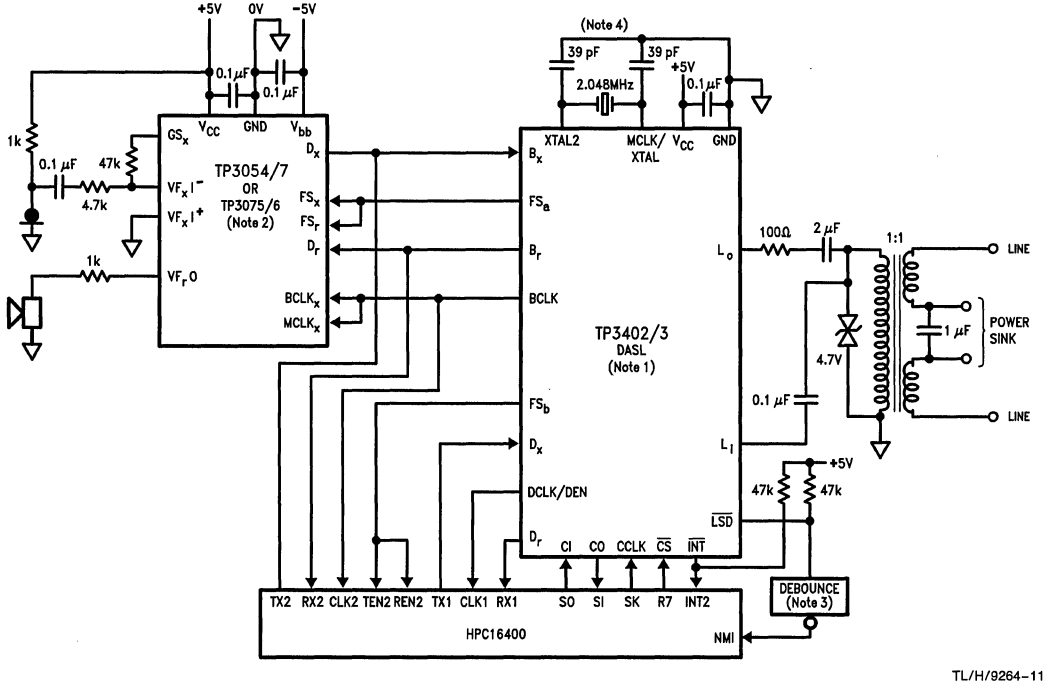
Timing Diagrams (Continued)



TL/H/9264–13

FIGURE 7. B Channel Interface Timing: Slave Mode

Typical Applications



TL/H/9264–11

FIGURE 8. Typical Application for Slave End

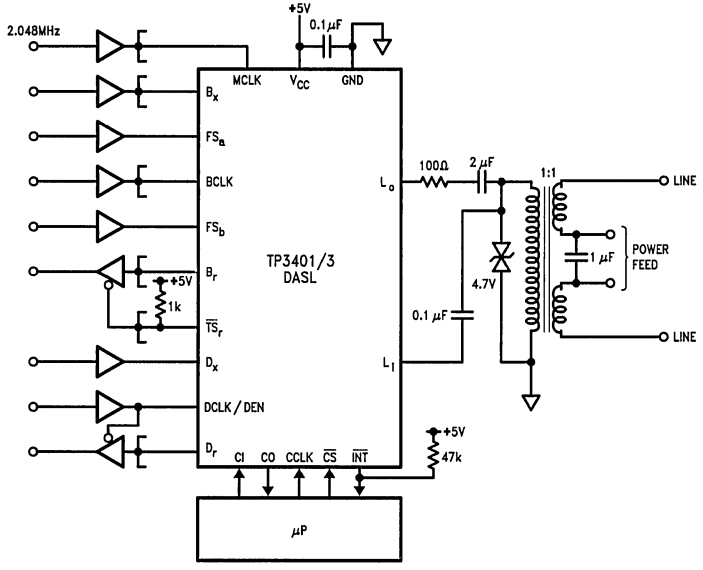
Note 1: The TP3401 may also be used in this configuration with an external MCLK source.

Note 2: The TP3075/6 Programmable Combos also must be connected to the MICROWIRE interface.

Note 3: Only necessary if a mechanical Hookswitch is connected to the NMI input of the HPC.

Note 4: Crystal load capacitors include board and trace capacitance. Oscillator frequency can be checked by measuring the BCLK output frequency when slave mode part is in digital loopback.

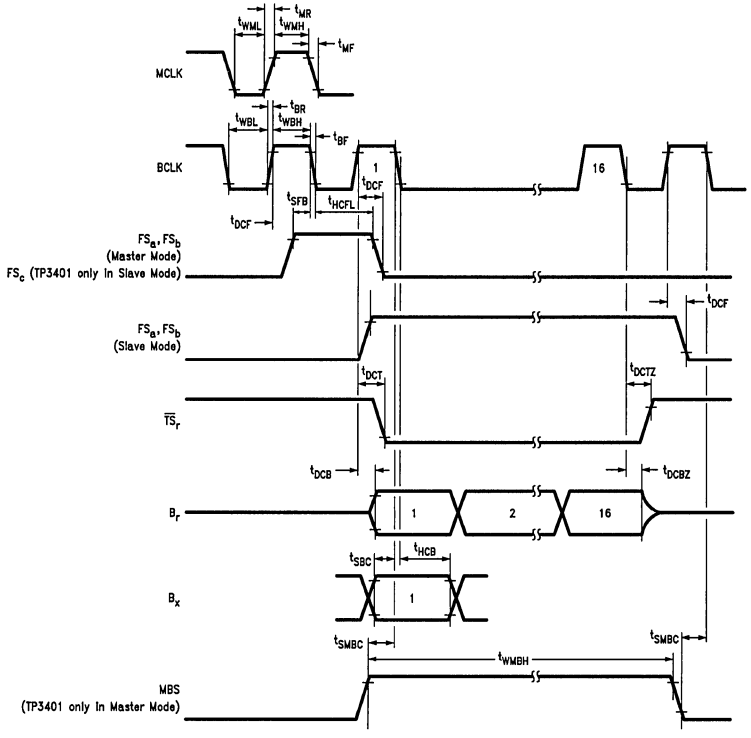
Typical Applications (Continued)



TL/H/9264-12

FIGURE 9. Typical Application for Master End

Timing Diagrams

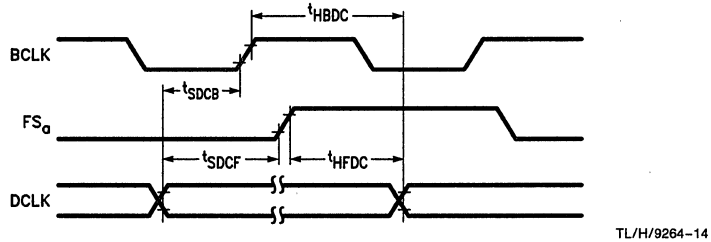


TL/H/9264-7

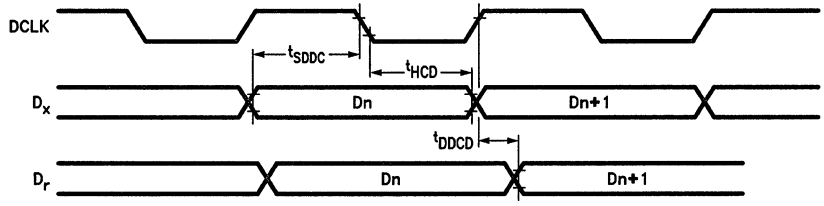
FIGURE 10. B Channel Interface Timing Details

2

Timing Diagrams (Continued)

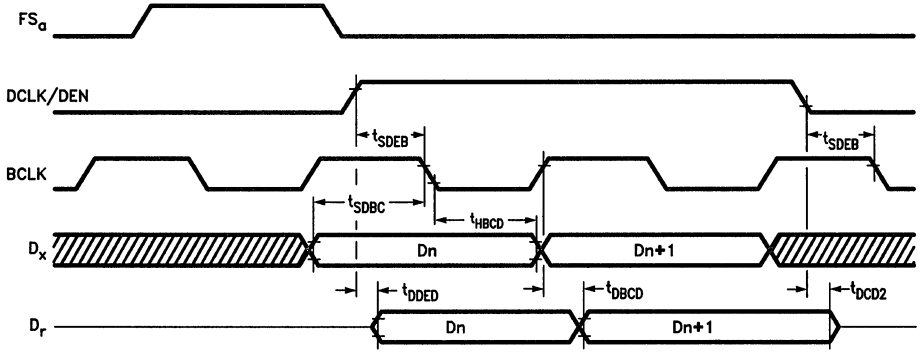


TL/H/9264-14



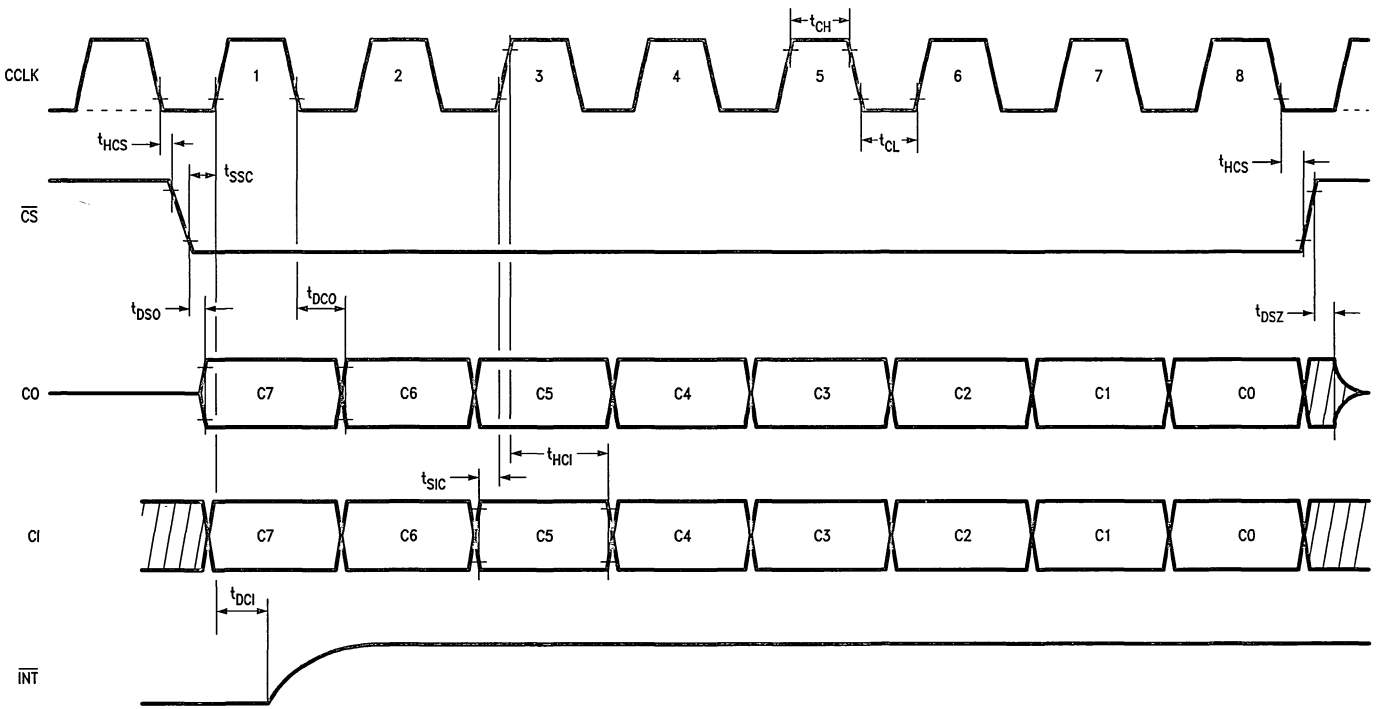
TL/H/9264-8

FIGURE 11. D Channel Interface Timing (Master and Slave Modes, C1 = 0)



TL/H/9264-9

FIGURE 12. D Channel Interface Timing (Master Mode only, C1 = 1)



TL/H/9264–10

FIGURE 13. Control Interface Timing

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at L_i, L_o	$V_{CC}+1V$ to $V_{SS}-1V$
Voltage at any Digital Input	$V_{CC}+1V$ to $V_{SS}-1V$
Storage Temperature Range	−65°C to +150°C
Current at L_o	±100 mA
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating is to be determined.

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are electrical testing limits at V_{CC} = 5.0V and T_A 25°C. All other limits are design goals for V_{CC} = 5.0V ±5% and T_A = 0°C to 70°C. This data sheet is still preliminary and parameter limits are not inidicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs (not MCLK)			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs (not MCLK)	2.2			V
V_{OL}	Output Low Voltage	I_L = 1 mA			0.4	V
V_{OH}	Output High Voltage	I_L = −1 mA	2.4			V
I_{IM}	Input Current at MBS/FS_c	GND < V_{IN} < V_{CC}	−600		10	μA
I_I	Input Current	Any Other Digital Input, GND < V_{IN} < V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE®)	B_r, $\overline{INT}$, $\overline{TS_r}$, CO GND < V_{OUT} < V_{CC}	−10		10	μA
LINE INTERFACES						
R_{Li}	Input Resistance	0V < L_i < 5.0V	200			kΩ
CL_{Lo}	Load Capacitance	CL_{Lo} from L_o to GND.			100	pF
RO	Output Resistance at L_o	Load = 60Ω in Series with 2 μF to GND			3.0	Ω
V_{DC}	Mean d.c. Voltage at L_o	Load = 60Ω in Series with 2 μF to GND		2.0		V
POWER DISSIPATION						
$I_{CC}0$	Power Down Current			1.3	2	mA
$I_{CC}1$	Power Up Current (Activated)	Load at L_o = 200Ω in Series with 2 μF to GND (in Master Mode)			18	mA
TRANSMISSION PERFORMANCE						
	Transmit Pulse Amplitude at L_o	R_L = 200Ω in Series with 2 μF to GND	±0.9	±1.1		Vpk
	Input Pulse Amplitude at L_i		±60			mVpk
	Timing Recovery Jitter	BCLK at Slave Relative to MCLK at Master		100		ns pk-pk
	Activation Time	Complete Loop from Cold Start		50		ms

Timing Characteristics

Unless otherwise noted: V_{CC} = +5V ±5%, T_A = 0°C to 70°C. Typical characteristics are specified at V_{CC} = 5V, T_A = 25°C. All signals are referenced to GND.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MASTER CLOCK INPUT SPECIFICATIONS						
F_{MCK}	Master Clock Frequency			2.048		MHz
	Master Clock Tolerance	Measured Relative to the Slave MCLK	−100		+100	ppm
	Master Clock Input Jitter	2.048 MHz Input, 18 kHz < f < 200 kHz			200	ns pk-pk
t_{WMH}, t_{WML}	Clock Pulse Width Hi & Low for MCLK	$V_{IH} = V_{CC} - 0.5V$ $V_{IL} = 0.5V$	190			ns
t_{MR}, t_{MF}	Rise and Fall Time of MCLK	Used as a Logic Input			15	ns
B CHANNEL INTERFACE ***(Figure 10)***						
F_{BCK}	Bit Clock Frequency	Master Mode Only		2.048		MHz
t_{WBH}, t_{WBL}	Clock Pulse Width Hi & Low for BCLK	$V_{IH} = 2.2V$ $V_{IL} = 0.7V$	190			ns
t_{BR}, t_{BF}	Rise and Fall Time of BCLK	Master Mode requirement for BCLK Source			15	ns
t_{SFB}	Set-Up Time, FS_a and FS_b to BCLK Low	Master Mode Only	20			ns
t_{HCFL}	Hold Time, BCLK Low to FS_a and FS_b Low	Master Mode Only	100			ns
t_{WBH} t_{WBL}	Output Pulse Width High and Low for BCLK	Slave Mode Only Load = 2 LSTTL Inputs Plus 50 pF	195			ns
t_{DCF}	Delay Time, BCLK High to FS_a, FS_b and FS_c Transitions	Slave Mode Only Load = 2 LSTTL Inputs Plus 50 pF			115	ns
t_{SBC}	Set Up Time, B_X Valid to BCLK Low		30			ns
t_{HCB}	Hold Time, BCLK Low to B_X Invalid		50			ns
t_{DCB}	Delay Time, BCLK High to B_r Valid	Load = 2 LSTTL Inputs Plus 100 pF			170	ns
t_{DCBZ}	Delay Time, BCLK Low to B_r High-Impedance	Slave Mode Only	60		220	ns
t_{DCT}	Delay Time, BCLK High to $\overline{TS}_r$ Low	Load = 2 LSTTL Inputs Plus 100 pF			150	ns
t_{DCTZ}	Delay Time, BCLK Low to $\overline{TS}_r$ High-Impedance		60		185	ns
t_{SMBC}	Set-Up Time, MBS to BCLK Low (Note 1)	Master Mode Only (TP3401 and TP3403 only)	60			ns
t_{WMBH}	Width of MBS Input High	Master Mode Only (TP3401 and TP3403 only)		125		μs

Note 1: MBS transitions may occur anywhere in the Frame, and require no specific relationship to FS_a or FS_b.

Timing Characteristics (Continued)

Unless otherwise noted: V_{CC} = +5V ±5%, T_A = 0°C to 70°C. Typical characteristics are specified at V_{CC} = 5V, T_A = 25°C. All signals are referenced to GND.

Symbol	Parameter	Conditions	Min	Max	Units
D CHANNEL INTERFACE *(Figure 11 & 12)*					
t_{SDDC}	Set Up Time, D_X Valid to DCLK Low		100		ns
t_{HCD}	Hold Time, DCLK Low to D_X Invalid		100		ns
t_{DDCD}	Delay Time, DCLK High to D_r Data Valid	Load = 100 pF +2 LSTTL Inputs		220	ns
t_{SDCB}	Set-Up Time, DCLK Transitions to BCLK High	Master Mode Only	50		ns
t_{HBDC}	Hold Time, BCLK High to DCLK Transitions	Master Mode Only	50		ns
t_{SDCF}	Set-Up Time, DCLK Transitions to FS_a HIgh	Master Mode Only	100		ns
t_{HFDC}	Hold Time, FS_a HIgh to DCLK Transition	Master Mode Only. Load = 50 pF	50		ns
t_{DDED}	Delay Time, DEN High to D_r Valid	Load = 100 pF + 2 LSTTL Inputs		200	ns
t_{SDEB}	Set-Up Time, DEN to BCLK Low		100		ns
t_{SDBC}	Set-Up Time, D_x to BCLK Low		30		ns
t_{HBCD}	Hold Time, BCLK Low to D_x Invalid		50		ns
t_{DBCD}	Delay Time, BCLK High to D_r Valid	Load = 100 pF +2 LSSTL Inputs		190	ns
t_{DCDZ}	Delay Time, DEN Low to D_r High Impedance			140	ns
CONTROL INTERFACE *(Figure 13)*					
t_{CH}	CCLK High Duration		250		ns
t_{CL}	CCLK Low Duration		250		ns
t_{SIC}	Setup Time, CI Valid to CCLK High		100		ns
t_{HCI}	Hold Time, CCLK High to CI Invalid		0		ns
t_{SSC}	Setup Time from $\overline{CS}$ Low to CCLK High		200		ns
t_{HCS}	Hold Time from CCLK Low to $\overline{CS}$		10		ns
t_{DCO}	Delay Time from CCLK Low to C0 Data Valid	Load = 100 pF +2 LSTTL Inputs		150	ns
t_{DSO}	Delay Time from $\overline{CS}$ Low to CO Valid	1st Bit Only		100	ns
t_{DSZ}	Delay Time from $\overline{CS}$ High to CO High Impedance			100	ns
t_{DCI}	Delay Time from CCLK1 High to $\overline{INT}$ High Impedance			120	ns

National Semiconductor

PRELIMINARY

TP3410 ISDN Basic Access Echo-Cancelling 2B1Q U Transceiver

General Description

The TP3410 is a complete monolithic transceiver for ISDN Basic Access data transmission at either end of the U interface. Fully compatible with ANSI specification T1.601-1988, it is built on National's advanced double-metal CMOS process, and requires only a single +5V power supply. A total of 160 kbps full-duplex transmission on a single twisted-pair is provided, with user-accessible channels including 2 'B' channels, each at 64 kbps, 1 'D' channel at 16 kbps, and an additional 4 kbps for loop maintenance. 12 kbps of bandwidth is reserved for framing. 2B1Q Line coding is used, in which pairs of binary bits are coded into 1 of 4 quantum levels for transmission at 80k symbols/sec (hence 2 Binary/1 Quaternary). To meet the very demanding specifications for <1 in 10e7 Bit Error Rate even on long loops with crosstalk, the device includes 2 Adaptive Digital Signal Processors, 2 Digital Phase-locked Loops and a controller for automatic activation.

The digital interface on the device can be programmed for compatibility with either of two types of control interface for chip control and access to all spare bits. In one mode a Microwire serial control interface is used together with a 2B+D digital interface which is compatible with the Time-division Multiplexed format of PCM Combo devices and backplanes. This mode allows independent time-slot assignment for the 2 B channels and the D channel.

Alternatively, the GCI (General Circuit Interface) may be selected, in which the 2B+D data is multiplexed together with control, spare bits and loop maintenance data on 4 pins.

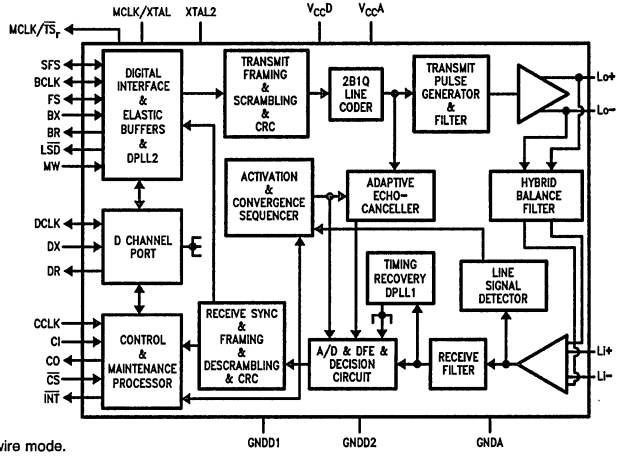
Features

- 2 'B'+'D' channel 160 kbps transceiver for LT and NT
- Meets ANSI T1.601-1988 U.S. Standard
- 2B1Q line coding with scrambler/descrambler
- Range exceeds 18 kft of #26 AWG with bridge taps
- >70 dB adaptive echo-cancellation and equalization
- On-chip timing recovery, no precision external components
- Direct connection to small line transformer
- Automatic activation controller
- Selectable digital interface formats:
  - — TDM with time-slot assigner up to 64 slots, plus MICROWIRE™ control interface
  - — GCI (General Circuit Interface), or
  - — IDL (Inter-chip Digital Link)
- Backplane clock DPLL allows free-running XTAL
- Elastic data buffers meet Q.502 wander/jitter for Slave-slave mode on PBX Trunk Cards and DLC
- EOC and spare bits access with automatic validation
- 2 block error counters
- 6 loopback test modes
- Single +5V supply, 300 mW active power
- 10 mW idle mode with line signal "wake-up" detector

Applications

- LT, NT-1, NT-2 Trunks, U-TE's, Regenerators etc.
- Digital Loop Carrier
- POTS Pair-Gain Systems
- Easy Interface to:
  - — Line Card Backplanes
  - — "S" Interface Device — TP3420
  - — Codec/Filter Combos — TP3054/7 and TP3075/6
  - — LAPD Processor — HPC16400
  - — HDLC Controller — TP3451

Block Diagram

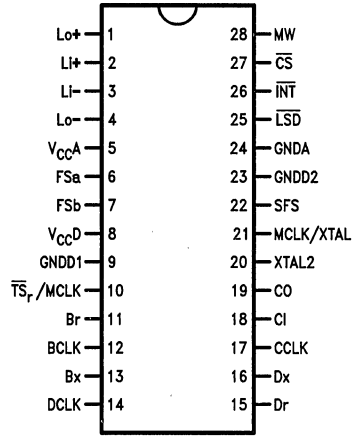


Note: Pin names show Microwire mode.

TL/H/9151–1

Connection Diagrams

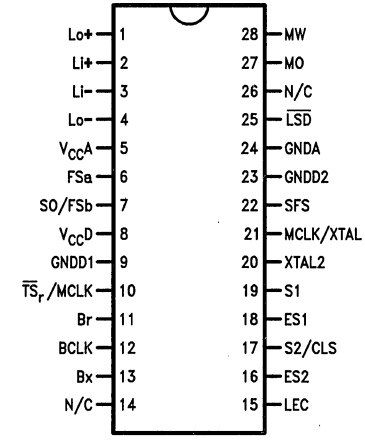
Pin Names for MICROWIRE Mode



TL/H/9151–2

Top View

Pin Names for GCI Mode



TL/H/9151–3

Top View

Order Number TP3410J

Pin Descriptions

Pin No.	Symbol	Description
24 9 23	GNDA GNDD1 GNDD2	Negative power supply pins, which must be connected together close to the device. All digital signals are referenced to these pins, which are normally at the system 0V (Ground) potential.
5	$V_{CC}A$	Positive power supply input for the analog sections, which must be +5V ±5% and must be directly connected to $V_{CC}D$.
8	$V_{CC}D$	Positive power supply input for the digital section, which must be +5V ±5% and must be directly connected to $V_{CC}A$.
21	MCLK/ XTAL	The 15.36 MHz Master Clock input, which requires either a parallel resonance crystal to be tied between this pin and XTAL2, or a CMOS logic level clock input from a stable source (a TTL Logic "1" level is not suitable). This clock does not need to be synchronized to the system clock (BCLK and FS), see Section 5.1.
20	XTAL2	The output of the crystal oscillator, which should be connected to one end of the crystal, if used; otherwise this pin must be left open-circuit.
10	$\overline{TS}r$/ MCLK	This pin has 2 functions: in LT mode it is an open-drain n-channel $\overline{TS}r$ output, which goes low only during the time-slots assigned to the B1 and B2 channels at the Br pin in order to enable the TRI-STATE control of the backplane line-driver. In NT mode it is a full CMOS 15.36 MHz clock output which is frequency-locked to the received line signal (unlike the XTAL pins it is not free-running).
22	SFS	The Superframe Sync pin, which indicates the start of each 12 ms superframe at the U Interface. In NT mode this pin is always an output. In LT mode it may be selected to be either an input or CMOS output via Register CR2; when selected as an output the signal is a square-wave.
25	$\overline{LSD}$	This pin is an open-drain n-channel Line Signal Detector output, which is normally high-impedance and pulls low only when the device is powered down and an incoming wake-up signal is detected from the far-end.
1 4	Lo+ Lo−	Transmit 2B1Q signal differential outputs to the line transformer. When used with an appropriate 1:1.5 step-up transformer and the line coupling circuit recommended in the Applications section, the line signal conforms to the output specifications in the ANSI standard.
2 3	Li+ Li−	Receive 2B1Q signal differential inputs from the line transformer. For normal full-duplex operation, these pins should be connected to the Lo± pins through the recommended coupling circuit, as shown in the Applications section.

*Crystal specifications: 15.36 MHz ±50 ppm parallel resonant; $R_S \leq 20\Omega$. Load with 33 pF to GND each side (+7 pF due to pin capacitance).

Pin Descriptions (Continued)

PIN DESCRIPTIONS SPECIFIC TO MICROWIRE MODE ONLY (MW = 1)

Pin No.	Symbol	Description
28	MW	The Microwire/$\overline{GCI}$ Select pin, which must be tied to $V_{CC}D$ to enable the Microwire Interface with any of the data formats at the Digital System Interface.
12	BCLK	The Bit Clock pin, which determines the data shift rate for 'B' and 'D' channel data on the digital interface side of the device. When Digital System Interface (DSI) Slave mode is selected (see Digital Interfaces section), BCLK is an input which may be any multiple of 8 kHz from 256 kHz to 4.096 MHz. It need not be synchronous with MCLK. When DSI Master mode is selected, this pin is a CMOS output clock at 256 kHz, 512 kHz, 1.536 MHz, 2.048 MHz or 2.56 MHz, depending on the selection in Command Register 1. It is synchronous with the data on Bx and Br.
6	FSa	In DSI Slave mode, this pin is the Transmit Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time for transmit B1 channel data into Bx. In DSI Master mode, this pin is a Frame Sync CMOS output pulse conforming with the selected Digital Interface format.
7	FSb	In DSI Slave mode, this pin is the Receive Frame Sync pulse input, requiring a positive edge to indicate the start of the active channel time of the device for receive B channel data out from Br (see DSI Format section). In DSI Master mode this pin is a Frame Sync CMOS output pulse conforming with the selected Digital Interface format.
13	Bx	The digital input for B and, if selected, D channel data to be transmitted to the line; must be synchronous with BCLK.
11	Br	The TRI-STATE output for B and, if selected, D channel data received from the line; must be synchronous with BCLK.
18	CI	The Microwire control channel data input.
19	CO	The Microwire control channel TRI-STATE output for status information. When not enabled by $\overline{CS}$, this output is high-impedance.
17	CCLK	The Microwire control channel Clock input, which may be asynchronous with BCLK.
27	$\overline{CS}$	The Chip Select input, which enables the Control channel data to be shifted in and out when pulled low. When high, this pin inhibits the Control interface.
26	$\overline{INT}$	The Interrupt output, a latched open-drain output signal which is normally high-impedance, and goes low to indicate a change of status of the loop transmission system. This latch is cleared when the Status Register is read by the microprocessor.
16	Dx	When the D-port is enabled this pin is the digital input for D channel data to be transmitted to the line clocked by DCLK or BCLK, see Register CR2. When the D-port is disabled via CR2, this pin must be tied to GND.
15	Dr	When the D-port is enabled this pin is the TRI-STATE output for D channel data to be received from the line clocked by DCLK or BCLK, see Register CR2.
14	DCLK	When the D-port is enabled, in DSI Slave or Master mode, this is a 16 kHz clock CMOS output for D channel data. When the D-port is disabled or not used, this pin must be left open-circuit.

PIN DESCRIPTIONS SPECIFIC TO GCI MODE ONLY (MW = 0)

Pin No.	Symbol	Description
28	MW	The Microwire/$\overline{GCI}$ select input, which must be tied to GND to enable the GCI mode at the Digital System Interface.
27	MO	The GCI Master/Slave select input for the clock direction. Connect this pin low to select BCLK and FSa as inputs i.e., GCI Slave; Selection of LT or NT mode must be made in register CR2. When MO is connected high, NT Mode is automatically selected, and BCLK, FSa and FSb are outputs, i.e., the GCI Master, see Section 8.
12	BCLK	The Bit Clock pin, which controls the shifting of data on the Bx and Br pins, at a rate of 2 BCLK cycles per data bit. When GCI Slave mode is selected (see Digital Interfaces section), BCLK is an input which may be any multiple of 16 kHz from 512 kHz to 6.144 MHz. It need not be synchronous with MCLK. When GCI Master mode is selected, this pin is a CMOS output clock at 512 kHz or 1.536 MHz, depending on the connection of the S2/CLS pin. It is synchronous with the data on Bx and Br.

Pin Descriptions (Continued)

Pin No.	Symbol	Description
13	Bx	The digital input for multiplexed B, D and control data clocked by BCLK at the rate of 1 data bit per 2 BCLK cycles, and 32 data bits per 8 kHz frame defined by FSa.
11	Br	The open-drain n-channel output for multiplexed B, D and control data clocked by BCLK at the rate of 1 data bit per 2 BCLK cycles, and 32 data bits per 8 kHz frame defined by FSa. A pull-up resistor is required to define the logical 1 state.
6	FSa	In GCI Slave mode (MO connected low), this pin is the 8 kHz Frame Sync pulse input, requiring a positive edge to indicate the start of the GCI slot time for both transmit and receive data at Bx and Br. In GCI Master mode, this pin is the 8 kHz Frame Sync CMOS output pulse.
17 19 7	S2/CLS S1 SO/FSb	In GCI Slave mode (MO = 0): input pins S2, S1 and S0 together provide a 3-bit binary-coded select port for the GCI channel number; S2 is the msb. These pins must be connected either to $V_{CC}D$ or GND to select the 1-of-8 GCI slots which are available if BCLK ≥ 4.096 MHz is used. In GCI Master mode (MO = 1) S2/CLS is the GCI Clock Select input. Connect this pin high to select BCLK = 1.536 MHz; connect CLS low to select BCLK = 512 kHz. SO/FSb is a Frame Sync CMOS output pulse which identifies the B2 channel.
18 16	ES1 ES2	External status inputs, which control the states of 2 bits in the RXM56 Register.
15	LEC	Latched External Control output, which is the output of a latched bit in the TXM56 Register.

Functional Description

1.1 Power-On Initialization

When power is first applied, power-on reset circuitry initializes the TP3410 and puts it into the power-down state, in which all the internal circuits including the Master oscillator are inactive and in a low power state except for the Line-Signal Detect circuit; the line outputs Lo+/Lo− are in a high impedance state and all digital outputs are high-impedance. All programmable registers and the Activation Sequence Controller are reset.

All states in the Command Registers initialize as shown in their respective code tables. The desired modes for all programmable functions may be selected by writing to these registers via the control channel (Microwire or Monitor channel, as appropriate). Microwire is functional regardless of whether the device is powered up or down, whereas the GCI channel requires the BCLK to be running.

1.2 Power-Up/Power-Down Control

Before powering up the device, the Configuration Registers should be programmed with the required modes.

In Microwire mode and GCI Slave mode, the device is powered up and the MCLK started by writing the PUP command, as described in the Activation section. In GCI Master mode, there are 2 methods of powering up the device: the Bx data input can be pulled low (local power-up command) or the 10 kHz wake-up tone may be received from the far-end.

The power-down state may be re-entered by writing a Power-down command. In the power-down state, all programmed register data is retained. Also, if the loop had been successfully activated and deactivated, the adaptive circuits are "frozen" and the coefficients in the Digital Signal Processors are stored to enable rapid reactivation ("warm-start").

1.3 Reset

A software reset command is provided to enable the clearing of the Activation sequencer without disconnecting the power supply to the device, see the Activation section.

2.0 TRANSMISSION SECTION

2.1 Line Coding And Frame Format

For both directions of transmission, 2B1Q coding is used, as illustrated in *Figure 1.* This coding rule requires that binary data bits are grouped in pairs, and each pair is transmitted as a symbol, the magnitude of which may be 1 out of 4 equally spaced voltage levels (a "Quat"). There is no symbol value at 0V in this code, the relative quat magnitudes being ±1 (the "inner" levels) and ±3 (the "outer" levels). No redundancy is included in this code, and in the limit there is no bound to the RDS, although scrambling controls the RDS in a practical sense (RDS is the Running Digital Sum, which is the algebraic summation of all symbol values in a transmission session).

The frame format used in the TP3410 follows the ANSI standard, shown in Table I. Each complete frame consists of 120 quats, with a line bit rate of 80 kq/s, giving a frame duration of 1.5 ms. A 9 quat syncword defines the framing boundary. Furthermore, a "superframe" consisting of 8 frames is defined in order to provide sub-channels within the spare bits M1 to M6. Inversion of the syncword defines the superframe boundary. Prior to transmission, all data, with the exception of the syncword, is scrambled using a self-synchronizing scrambler to implement the specified 23rd-order polynomial. Descrambling is included in the receiver.

First Bit (Sign)	Second Bit (Magnitude)	Quat	Pulse Amplitude (Note 1)
1	0	+3	+2.5V
1	1	+1	+0.83V
0	1	−1	−0.83V
0	0	−3	−2.5V

Note 1: For isolated pulses into a 135Ω termination.

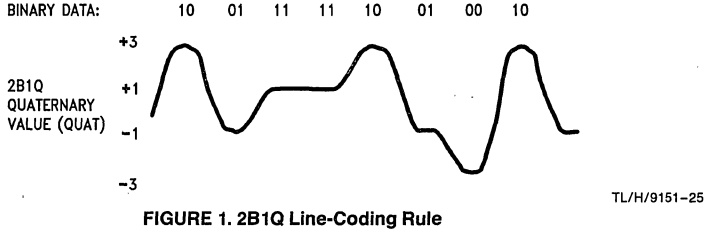


FIGURE 1. 2B1Q Line-Coding Rule

Functional Description (Continued)

		Framing	12x(2B+D)	Overhead Bits (M_1–M_6)					
	Quat Positions	1–9	10–117	118s	118m	119s	119m	120s	120m
	Bit Positions	1–18	19–234	235	236	237	238	239	240
Superframe #	**Basic Frame #**	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW	2B+D	$eoca_1$	$eoca_2$	$eoca_3$	act	1	1
	2	SW	2B+D	$eocd_m$	$eoci_1$	$eoci_2$	dea	1	febe
	3	SW	2B+D	$eoci_3$	$eoci_4$	$eoci_5$	1	crc_1	crc_2
	4	SW	2B+D	$eoci_6$	$eoci_7$	$eoci_8$	1	crc_3	crc_4
	5	SW	2B+D	$eoca_1$	$eoca_2$	$eoca_3$	1	crc_5	crc_6
	6	SW	2B+D	$eocd_m$	$eoci_1$	$eoci_2$	1	crc_7	crc_8
	7	SW	2B+D	$eoci_3$	$eoci_4$	$eoci_5$	1	crc_9	crc_{10}
	8	SW	2B+D	$eoci_6$	$eoci_7$	$eoci_8$	1	crc_{11}	crc_{12}
2, 3, . . .	1	ISW							

(a) Network → NT

		Framing	12x(2B+D)	Overhead Bits (M_1–M_6)					
	Quat Positions	1–9	10–117	118s	118m	119s	119m	120s	120m
	Bit Positions	1–18	19–234	235	236	237	238	239	240
Superframe #	**Basic Frame #**	Sync Word	2B+D	M_1	M_2	M_3	M_4	M_5	M_6
1	1	ISW	2B+D	$eoca_1$	$eoca_2$	$eoca_3$	act	1	1
	2	SW	2B+D	eoc_{dm}	$eoci_1$	$eoci_2$	ps_1	1	febe
	3	SW	2B+D	$eoci_3$	$eoci_4$	$eoci_5$	ps_2	crc_1	crc_2
	4	SW	2B+D	$eoci_6$	$eoci_7$	$eoci_8$	ntm	crc_3	crc_4
	5	SW	2B+D	$eoca_1$	$eoca_2$	$eoca_3$	cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	$eoci_1$	$eoci_2$	1	crc_7	crc_8
	7	SW	2B+D	$eoci_3$	$eoci_4$	$eoci_5$	1	crc_9	crc_{10}
	8	SW	2B+D	$eoci_6$	$eoci_7$	$eoci_8$	1	crc_{11}	crc_{12}
2, 3, . . .	1	ISW							

(b) NT → Network

Note: 8 × 1.5 ms Basic Frames = 12 ms/Superframe. NT-to-Network superframe is offset from Network-to-NT superframe by 60 ± 2 quats (about 0.75 ms). All bits other than the Sync Word are scrambled.

Symbols & Abbreviations

act = activation bit (= 1 during activation)
crc = cyclic redundancy check: covers 2B+D + M_4
  1 = most significant bit
  2 = next significant bit etc.
cso = cold-start-only bit (= 1 to indicate cold-start-only)
dea = deactivation bit (= 0 to announce deactivation)
eoc = embedded operations channel
  a = address bits
  dm = data/message indicator (0 = data, 1 = message)
  i = information (data or message)
febe = far end block error bit (= 0 for errored superframe)
ntm = NT in test mode bit (= 0 to indicate test mode)
ps1, ps2 = power status bits (= 0 to indicate power problems)
Quat = pair of bits forming quaternary symbol
  s = sign bit (first in quat)
  m = magnitude bit (second in quat)
"1" = reserved bit for future standard (= 1)
2B+D = user data, bits 19–234 in frame
M = M-channel, bits 235–240 in frame
SW/ISW = synchronization word/inverted synchronization word, bits 1–18 in frame

TABLE I. 2B1Q Superframe Format and Overhead Bit Assignments

Functional Description (Continued)

2.2 Line Transmit Section

Data to be transmitted to the line consists of the customer's 2B+D channel data and the data from the maintenance processor, plus other "spare" bits in the overhead channels. This data is multiplexed and scrambled prior to addition of the syncword. A pulse waveform synthesizer then drives the transmit filter, which in turn passes the line signal to the line driver. The differential line-driver outputs, Lo+ and Lo−, are designed to drive a transformer through an external termination circuit. A 1:1.5 transformer, designed as shown in the Applications section, results in a signal amplitude of nominally 2.5V pk on the line for single quats of the outer (±3) levels. Note, however, that because of the RDS accumulation of the 2B1Q line code, continuous random data will produce signal swings considerably greater than this on the line. Short-circuit protection is included in the output stage; overvoltage protection must be provided externally.

2.3 Line Receive Section

The receive input signal should be derived from the transformer by means of a coupling circuit as shown in the Applications section. At the front-end of the receive section is a continuous filter followed by a switched-capacitor low-pass filter, which limits the noise bandwidth. A Hybrid Balance Filter provides a degree of analog echo-cancellation in order to limit the dynamic range of the composite signal. An A/D converter then samples the composite received signal prior to the cancellation of the "echo" from the local transmitter by means of an adaptive digital transversal filter (i.e., the "echo-canceller"). Following this, the attenuation and distortion (inter-symbol interference) of the received signal from the far-end, caused by the transmission line, are equalized by a second adaptive digital filter configured as a Decision Feedback Equalizer (DFE), thereby restoring a "flat" channel response with maximum received eye opening over a wide spread of cable attenuation characteristics.

From the received line signal, a Timing Recovery circuit based on a DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 15.36 MHz. Received data is then detected, with automatic correction for line signal polarity if necessary, and a flywheel synchronization circuit searches for and locks onto the frame and superframe syncwords. Frame lock will be maintained until at least 6 consecutive errored sync words are detected, which will cause the flywheel to attempt to re-synchronize. If a loss-of-sync condition persists for 480 ms the device will cease searching, cease transmitting and go into a RESET state.

While the receiver is synchronized, data is descrambled using the specified polynomial, and the individual channels demultiplexed and passed to their respective processing circuits.

Whenever the loop is deactivated, either powered up or powered down, a Line Signal Detect circuit is enabled to detect the presence of an incoming 10 kHz wake-up tone if the far-end starts to activate the loop. The LSD circuit generates an interrupt and, if the device is powered down, pulls the $\overline{\text{LSD}}$ pin low; either of these indicators may be used to alert an external controller, which must respond with the appropriate commands to initiate the activation sequence (see the Activation section).

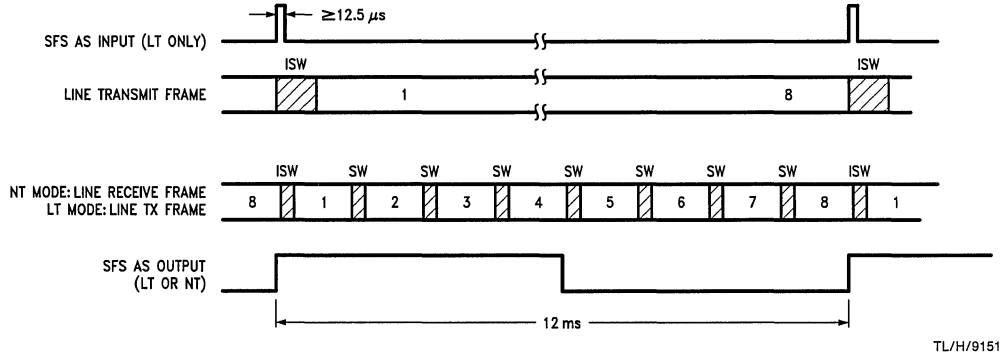
3.0 ACTIVATION CONTROL: OVERVIEW

The TP3410 contains an automatic sequencer for the complete control of the start-up activation sequence specified in the ANSI standard. Both the "cold-start" and the fast "warm-start" are supported. Interaction with an external controller requires only Activate Request and Deactivate Request commands, with the option of inserting breakpoints in the sequence for additional external control if desired. Automatic control of the "act" and "dea" bits in the M4 bit positions is provided, along with the specified 40 ms and 480 ms timers used during deactivation. The only external timer required is a 15 second default timer to prevent system lock-up in the event of a failed activation attempt. Section 11 describes the complete activation handshake between the TP3410 and the controller.

4.0 MAINTENANCE FUNCTIONS: OVERVIEW

4.1 M Channel Processing

In each frame of the superframe there are 6 "Overhead" bits assigned to various control and maintenance functions of the DSL. Some processing of these bits may be programmed via the Command Registers, while interaction with an external controller provides the flexibility to take full advantage of the maintenance channels. New data written to any of the overhead bit Transmit Registers is resynchronized internally to the next available complete superframe or half-superframe, as appropriate. In addition, the SFS pin may be used to indicate the start of each superframe in 1 direction, see *Figure 2* and Register CR2.



TL/H/9151–26

FIGURE 2. Superframe Sync Pin Timing

Functional Description (Continued)

4.2 Embedded Operations Channel

The EOC channel consists of 2 complete 12-bit messages per superframe, distributed through the M1, M2 and M3 bits of each half-superframe as shown in Table I. Each message is composed of 3 fields; a 3-bit address identifying the message destination, a 1-bit indicator for the data mode, i.e., encoded message or raw data, and an 8-bit information byte. The Microwire port or GCI Monitor Channel provides access to the complete 12 bits of every message in the TX EOC and the RXEOC Registers. If one of the defined encoded messages is received, e.g., Send Corrupted CRC, then the appropriate Command Register instruction must be written to the device to invoke the function.

4.3 M4 Bits

The M4 bit position of every frame is a transparent channel in which are transmitted data bits loaded from the M4 Transmit Register TXM4, one byte per superframe. On the receive side the M4 bits from one complete superframe are sent to a checking circuit which holds each new M4 byte and compares it against the previous M4 byte(s) for validation prior to sending it to the RXM4 Receive Register; Register OPR provides several options for control of this validation.

4.4 Spare M5 And M6 Bits

Overhead bits M5 and M6 in frame 1 (M51 and M61) and M5 in frame 2 (M52) are transparently transmitted from the Transmit M56 Spare Bit Register to the line. In the receive direction, data from these bit positions is sent to a checking circuit which holds the new M5/M6 spare bits and compares them against the previous M5/M6 bits for validation prior to sending them to the Receive M56 Spare Bit Register; the OPR Register provides several options for control of this validation.

4.5 CRC Circuit

In the transmit direction an on-chip crc calculation circuit automatically generates a checksum of the 2B + D + M4 bits using the polynomial $x12+x11+x3+x2+x+1$. Once per superframe the crc is transmitted in the specified M5 and M6 bit positions (see Table I). In the receive direction a checksum is again calculated on the same bits as they are received and, at the end of the superframe, compared against the crc transmitted with the data. The result of this comparison generates a "Far End Block Error" bit (the febe bit), which is transmitted back towards the other end of the DSL in the next superframe. If there are no errors in a superframe, febe is set = 1, and if there is one or more errors febe is set = 0.

The TP3410 also includes two readable 8-bit Block Error Counters associated with the febe bits. Each superframe in which febe = 0 is received, or a near-end crc error is detected, the appropriate counter is incremented by 1. When a counter reaches a programmable threshold, an interrupt (if enabled) will be sent to the Control Interface. Reading this interrupt resets that counter. Optionally, the interrupt may be disabled via Register OPR, thereby allowing external software counting to be used if preferred; see the Block Error Counter section for more details.

5.0 DIGITAL INTERFACE: ALL FORMATS

5.1 Clocking

In LT applications (network end of the Loop), the Digital System Interface (DSI) normally accepts BCLK and FS signals from the network, requiring the selection of DSI or GCI Slave mode in Register CR1. A Digital Phase-Locked Loop (DPLL #2) on the TP3410 allows the MCLK frequency to be plesiochronous (i.e. free-running) with respect to the network clock, (BCLK and the 8 kHz FSa input). With a tolerance on the MCLK oscillator of 15.36 MHz ±100 ppm, the lock-in range of DPLL2 allows the network clock frequency to deviate up to ±50 ppm from nominal.

In NT applications, when the device is in NT mode and is slaved to loop timing recovered from the received line signal, DSI or GCI Master mode should normally be selected. In this case BCLK and FS signals are outputs which are phase-locked to the recovered clock. A Slave-slave mode is also provided, however, in which the Digital Interface data buffers on the TP3410 allow BCLK and FSa/b to be input from an external source, which must be frequency-locked (with arbitrary phase) to the received line signal; in this case DSI or GCI Slave mode should be selected.

5.2 Data Buffers

The TP3410 buffers the 2B + D data at the Digital Interface in elastic FIFOs, which are 3 frames deep in each direction. When the Digital Interface is a timing slave these FIFOs compensate for relative jitter and wander between the Digital Interface clocks (BCLK and FSa/b) and bit and frame timing at the Line Interface. Each buffer can absorb wander up to 18 μs in $\geq$ 10 secs without "slip", exceeding CCITT recommendation Q.502. Excessive wander causes a controlled slip of one complete frame.

6.0 DIGITAL INTERFACE DATA FORMATS IN MICROWIRE MODE (MW = 1)

When the MW pin is tied high to enable the Microwire Port for control and status, the Digital System Interface on the TP3410 provides a choice of four multiplexed formats for the B and D channel data, as shown in *Figure 3*. These apply in both LT and NT modes of the device, and selection is made via Register CR1. Selection of DSI Master or Slave mode must also be made in CR1. Within each format there is also an independent selection available to either multiplex the D channel (Tx and Rx) data on the same pins as the B channels, or via the separate D-channel access pins, DCLK, Dx and Dr, see Section 6.3.

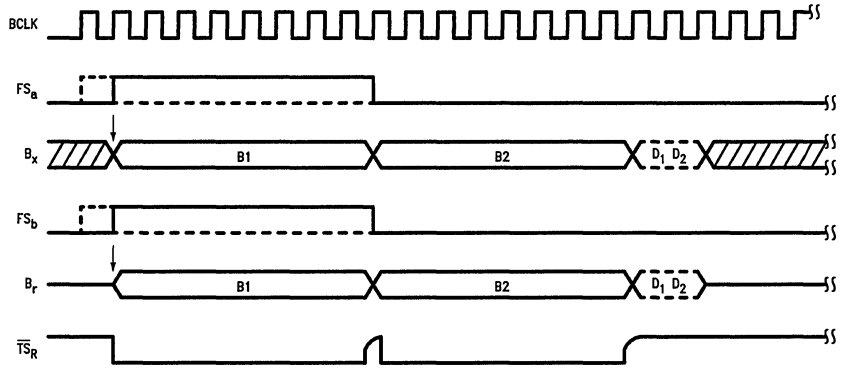
Format 1: In Format 1, the 2B + D data transfer is assigned to the first 18 bits of the frame on the Bx and Br pins. Channels are assigned as follows: B1 (8 bits), B2 (8 bits), D (2 bits), with the remaining bits ignored until the next frame sync pulse. When the D channel port is enabled (see CR2), only the 2 B channels use the Bx and Br pins; the D bits are assigned to the 17th and 18th bits of the frame on the Dx and Dr pins. *Figure 3-1* shows this format in DSI Slave Mode, and *Figure 3-4* shows DSI Master Mode.

Format 2: Format 2 is the IDL, in which the 2B + D data transfer is assigned to the first 19 bits of the frame on the Bx and Br pins. Channels are assigned as follows: B1 (8 bits), D (1 bit), 1 bit ignored, B2 (8 bits), D (1 bit), with the remaining bits ignored until the next frame sync pulse. *Figure 3-2* shows this format in DSI Slave Mode, and *Figure 3-5* shows DSI Master Mode.

Functional Description (Continued)

Format 3: This format provides time-slot assignment capability for the B1 and B2 channels, which can be independently assigned to any 8-bit wide time-slot from 64 (or less) on the Bx and Br pins; the Transmit and Receive directions are also independently assignable. Also the D channel can be assigned to any 2-bit wide time-slot from 256 (or less) on the Bx and Br pins (D port disabled) or on the Dx and Dr pins (see D-Channel Port section). *Figure 3-3* shows this format in DSI Slave Mode, and *Figure 3-6* shows DSI Master Mode; see also Section 6.2.

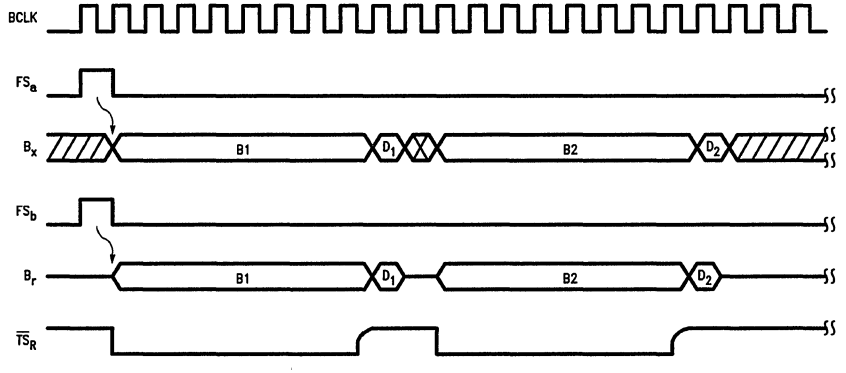
Format 4: This is similar to the GCI format for the 2B+D channels, but excludes the Monitor channel and C/I channel. Channels are assigned to the first 26 bits of each frame as follows: B1 (8 bits), B2 (8 bits), ignored (8 bits), D (2 bits). The remaining bits in the frame are ignored until the next frame sync pulse. The relationship between BCLK and data is the same as in the GCI mode for GCI Channel 0, see *Figure 7* (in DSI Master Mode, BCLK = 512 kHz and FS_a is a square wave output).



TL/H/9151–5

FSa defines B1 channel for Tx.
FSb defines B1 channel for Rx.

FIGURE 3-1. DSI Format 1: Slave Mode

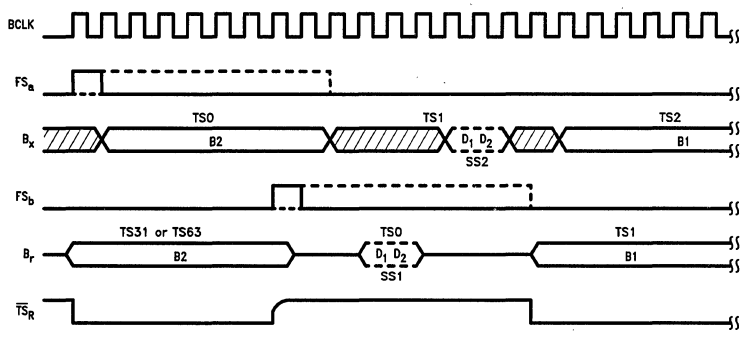


TL/H/9151–6

Delayed timing mode must be selected;
Time-slot immediate mode only (no TSA).

FIGURE 3-2. DSI Format 2 (IDL): Slave Mode

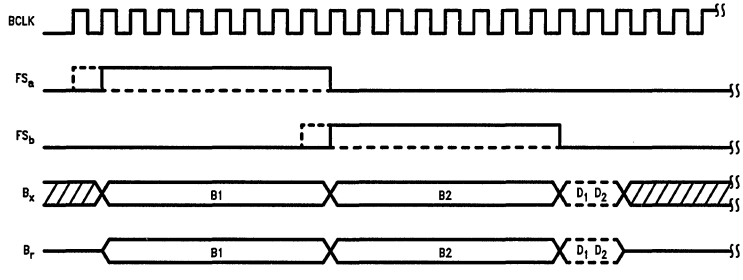
Functional Description (Continued)



TL/H/9151–7

Shown with examples of offset frames and Time-slot Assignments.

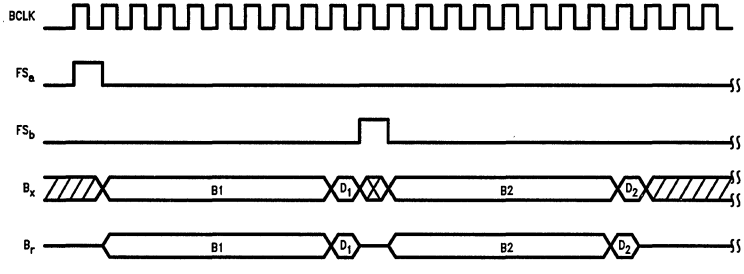
FIGURE 3-3. DSI Format 3 (Time-Slot Assignment) : Slave Mode



TL/H/9151–8

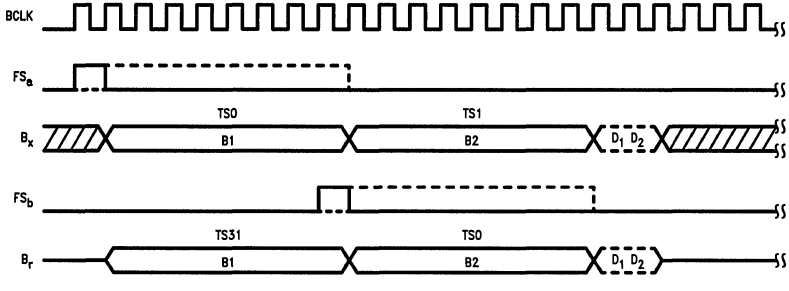
FSa defines B1 channel for Tx and Rx.
FSb defines B2 channel for Tx and Rx.

FIGURE 3-4. DSI Format 1: Master Mode



TL/H/9151–9

FIGURE 3-5. DSI Format 2 (IDL): Master Mode



TL/H/9151–10

FIGURE 3-6. DSI Format 3: Master Mode

Functional Description (Continued)

6.1 FS Relationship To Data (Microwire Mode)

For applications on a line-card, in DSI Slave Mode, the B and D channel slots can be interfaced to a Time-Division Multiplexed (TDM) bus and assigned to a time-slot. The repetition rate of the FS input signals must be 8 kHz and must be synchronized to the BCLK input, which may be any frequency from 256 kHz to 4.096 MHz in 8 kHz increments. Two different relationships may be established between the FS inputs and the actual time-slots on the PCM busses by setting the DDM bit in Control Register CR1, see *Figures 3, 11* and *12*. Non-delayed data mode is similar to long frame timing on the TP3050/60 series of devices (COMBO I): the time-slots are defined by the 8-bit duration FSa and FSb signals. The alternative is to use Delayed Data Mode, which is similar to short frame sync timing on COMBO I, in which each FS input indicates the start of the first time-slot.

Serial B channel data is shifted into the Bx input during each assigned Transmit time-slot on the falling edges of BCLK. During each assigned Receive time-slot, the Br output shifts data out on the rising edges of BCLK. Also, with the device in LT Mode, the $\overline{TSr}$ pin is an open drain n-channel pull-down output which goes low during the selected time-slots for the received B1 and B2 channels at the Br pin to control the TRI-STATE Enable of a backplane line-driver; it is high-impedance at all other times.

In NT Mode, when DSI Master mode is selected, FSa and FSb are outputs indicating the start of both Transmit and Receive B channel data transfers. BCLK is also an output at the serial data shift rate, which is dependent on the format selected. Again, either a delayed or non-delayed relationship between FSa, FSb and the start of the first time-slot can be selected.

6.2 B Channel Time-slot Assignment; Format 3 Only (Microwire Mode)

In Format 3 only, the TP3410 provides programmable time-slot assignment for selecting the Transmit and Receive B channel time-slots. Following power-on, the device is automatically in Non-delayed Data Mode; Delayed Data Mode must first be selected (see CR1) prior to using Time-slot Assignment, and the FS pulses must conform to the Delayed Data timing format. The actual transmit and receive time-slots are then determined by the internal Time-slot Assignment counters, programmed via Control Registers TXB1, TXB2, RXB1 and RXB2. In this mode, a frame may consist of up to 64 time-slots of 8 bits each with BCLK = 4.096 MHz.

A new assignment becomes active on the second frame following the end of the 16-bit Chip Select.

6.3 D Channel Port Selection (Microwire Mode)

In any of the DSI Formats, the 2 D channel bits per frame may either be multiplexed with the B channels on the Bx and Br pins, or may be accessed via the separate D channel port consisting of Dx and Dr. Furthermore, when using the separate D port the data shift clock may either be a continuous, unframed data stream using the 16 kHz clock output at DCLK, see *Figure 4*, or may use the BCLK, see *Figure 5*. Selection of these options is via Control Register CR2.

6.4 D Channel Time-Slot Assignment

In addition to B channel TSA, Format 3 allows independent Time Slot Assignment for the Transmit and Receive D channels, which may be programmed via Registers TXD and RXD. As with the B channels, up to 64 time-slots are available if BCLK = 4.096 MHz, and in addition the 2 D bits may be assigned, in pairs, to specific bit locations within the time-slot; that is in bits 1 and 2; 3 and 4; 5 and 6; or 7 and 8. D channel TSA may be used either with the D channel multiplexed with the B channel data, or with the separate D Channel port clocked with BCLK; it cannot be used with the 16 kHz clock option at DCLK.

Summary of DSI Slave Mode Options

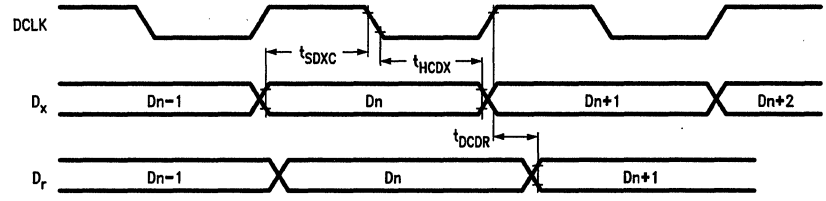
Function	Format Number			
	1	2	3	4
FSa	Tx B1	Tx B1	Tx TS0	Tx B1
FSb	Rx B1	Rx B1	Rx TS0	Rx B1
Non-Delayed Timing?	Yes	No	Yes	Yes
Delayed Timing?	Yes	Yes	Yes	No
Tx and Rx Frames with Any Phase?	Yes	Yes	Yes	Yes
TSA Available?	No	No	Yes	No
D Port Available?	Yes	Yes	Yes	Yes

Summary of DSI Master Mode Options

Function	Format Number			
	1	2	3	4
FSa	B1	B1	TS0	B1
FSb	B1	B2	TS1	B2
FS Formats	Non-Delayed and Delayed	Delayed Only	Non-Delayed and Delayed	Non-Delayed Only
TSA Available?	No	No	Yes	No
D Port Available?	Yes	Yes	Yes	Yes

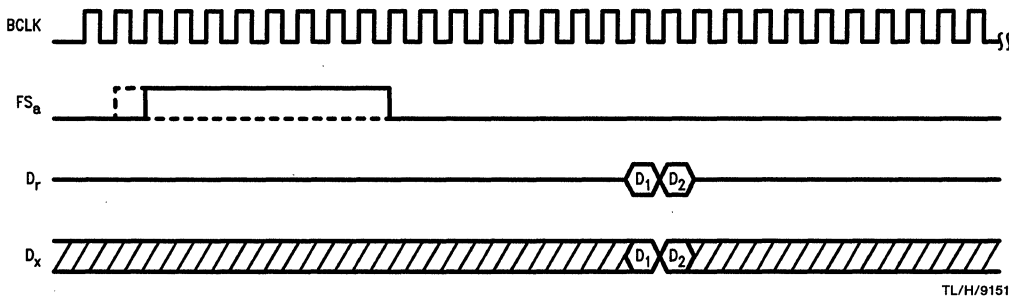
Note: Formats 1, 2 and 4: Tx and Rx frames always aligned.

Functional Description (Continued)



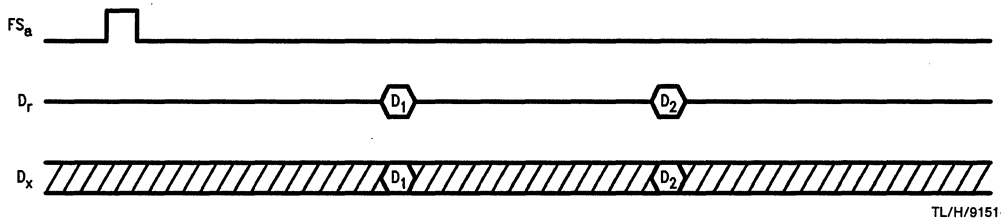
TL/H/9151–11

FIGURE 4. D-Port Interface Timing Using DCLK in 16 kHz Mode



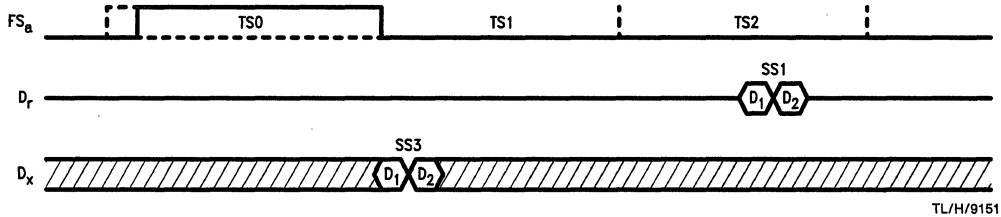
TL/H/9151–12

FIGURE 5-1. Format 1



TL/H/9151–13

FIGURE 5-2. Format 2



TL/H/9151–14

FIGURE 5-3. Format 3

Shown with example of Time-slot Assignment, and $FS_a = FS_b$

FIGURE 5. D-Port Interface Timing Using BCLK

Functional Description (Continued)

7.0 MICROWIRE CONTROL PORT (MW = 1)

When Format 1, 2, 3 or 4 is used, control information and maintenance channel data is written into and read back from the TP3410 via the Microwire port consisting of the control clock CCLK; the serial data input, CI, and output, CO; the Chip Select input, $\overline{CS}$ and the interrupt output $\overline{INT}$. The MW pin must be tied high to enable this port, and the port may be used regardless of whether the device is powered up or down. *Figures 6* and *14* show the timing, which is compatible with the Microwire port on the HPC and COPs families of microcontrollers, and Tables II and III list the control functions and status indicators.

All read and write operations require 2 contiguous bytes. To shift data to and from the TP3410, CCLK must be pulsed high 16 times while $\overline{CS}$ is low. Data on the CI input is shifted into the serial input register on the rising edge of each CCLK pulse; simultaneously, data is shifted out from CO on each falling edge of CCLK. Bit 7 of byte 1 is shifted first. $\overline{CS}$ must return high at the end of the 2nd byte, after which the contents of the input shift register are decoded, and the data is loaded into the appropriate programmable register. Pulling $\overline{CS}$ low also clears the $\overline{INT}$ pin if it was pulled low; a new interrupt condition can only pull the $\overline{INT}$ pin low when $\overline{CS}$ is high. When $\overline{CS}$ is high the CO pin is in the high-impedance state, enabling the CO pins of many devices to be multiplexed together.

8.0 GCI MODE (MW = 0)

Selected by tying the MW pin low, the GCI interface is designed for systems in which PCM and control data are multiplexed together into 4 contiguous bytes per 8 kHz frame. Furthermore, in Subscriber Line Cards and NT1-2's (where the Digital Interface is slaved to external timing) up to 8 GCI channels may be carried in 1 frame of a GCI multiplex, with a combined bit rate from 256 kb/s up to 3088 kb/s. Pin-programmable GCI-channel assignment for 8 GCI channels is provided.

Note that GCI mode on the TP3410 requires messages in the Embedded Operations Channel to be processed by a local microcontroller. In Line card and TE applications, GCI mode can be used with a device such as the TP3451 HDLC controller to provide the interface for the microcontroller to access the EOC Registers. To use the device in an NT-1 or Regenerator, a microcontroller is required and Microwire mode should be used on the TP3410.

8.1 GCI Physical Interface

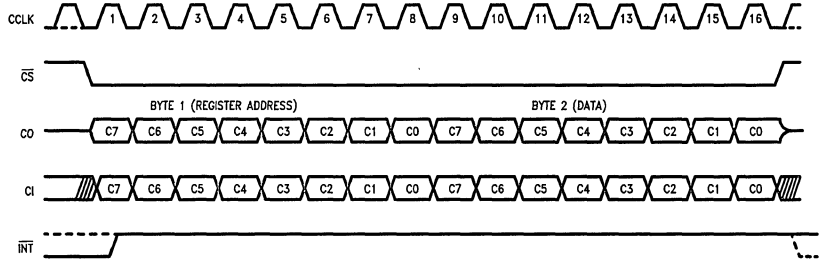
The interface physically consists of four wires:

— Transmit data to line: Bx
— Receive data from line: Br
— Bit clock at 2 cycles/bit: BCLK
— 8 kHz frame sync: FSa

Data is synchronized by the BCLK and FSa clock inputs. FSa insures re-initialization of the time-slot counter at the beginning of each 8 kHz frame, with the rising edge of FSa being the reference time for the first GCI channel bit. Data is clocked in both directions at half the BCLK input frequency. Data bits are output from the device on a rising edge of BCLK and sampled on the second falling edge of BCLK; unused slots are high impedance. Br is an open-drain n-channel output, with internal detection for contention resolution on the Monitor and C/I channels between devices attempting to use the same GCI channel (typically in a TE application).

A device may be either the Master or Slave of the GCI timing. As a Master it is the source of BCLK, FSa and FSb, which are synchronized to the data received from the line, and GCI channel 0 is always used. As a GCI Slave, BCLK and FSa must be sourced externally, typically from a system backplane, and pins S0–S2 must be connected high or low to select the required GCI channel. To use the single channel mode, a 512 kHz BCLK is required, and S2, S1 and S0 must be connected to GND (GCI Channel 0). To use the multiplex mode with a GCI Slave device, the 4 pins are commoned between up to 8 devices, forming a "wire-AND" connection with the Br pins. The BCLK frequency must be at least n × 512 kHz, where n is the number of devices. In fact BCLK may be operated up to 6144 kHz if required, to leave up to 4 additional GCI channels unoccupied by TP3410's (and available for other uses). Clock and channel selection are shown in the following table:

Pin Name	LT and NT1-2	NT1 and TE
MW	0	0
MO	0 (GCI Slave)	1 (GCI Master)
S2/CLS	S2 (msb)	CLS = 0: 512 kHz CLS = 1: 1536 kHz
S1	S1	0
S0/FSb	S0 (lsb)	FSb



TL/H/9151-15

FIGURE 6. Microwire Control Port Timing: MW = 1

Functional Description (Continued)

8.2 GCI Frame Structure

Figure 7 shows the frame structure at the GCI interface. One GCI channel supports one TP3410 using a bandwidth of 256 kbit/s, consisting of the following channels multiplexed together in an 8 kHz frame:

— B1 channel at 8 bits per frame;

— B2 channel at 8 bits per frame;

— Monitor (M) channel at 8 bits per frame;

— Signalling and Control (SC) channel, which is structured as follows:
D Channel at 2 bits per frame;
C/I channel at 4 bits per frame;
A bit, for acknowledgement of M channel bytes;
E bit, which indicates byte boundaries when multiple-byte messages are transferred via the M channel.

8.3 Monitor Channel

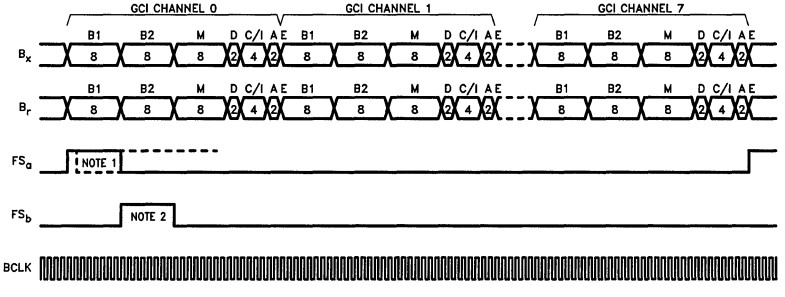
The GCI Monitor channel (byte 3) is used to access all the Command Registers shown in Table II, with the exception of the Activation Control Register, and all the Status Registers shown in Table III with the exception of the Activation Indication Register. Each access to or from one of the listed registers requires a 2-byte message transfer. As shown in Tables II and III, the first byte from the originating device contains the register address, and the second byte is the data byte. Status Registers originate messages in the Monitor channel under control of the Interrupt Stack (in the same manner as when the TP3410 is used in Microwire Mode). In addition a protocol is used, based on the E and A bits in byte 4, to provide an acknowledgement of each Monitor channel byte in either direction, see *Figure 8*.

When no Monitor Channel message is being transferred, the E bit, and the A bit in the reverse direction, are high-impedance (and pulled high by the external resistor if no other device is active in that channel). To initiate a transfer, a device must first verify that it has received the A bit = 1 for at least 2 consecutive GCI frames from the other device before starting the transfer. It then sends the first byte in the Monitor channel, with the associated E bit = 0, and repeats the byte in the next GCI frame. Normally, the receiving device will verify receiving the same byte in 2 consecutive frames and acknowledge this by setting A = 0 for at least 2 frames. If not, the message is aborted by sending A = 0 for only 1 frame.

On detecting the acknowledgement, the sending device then sends the 2nd of the 2 bytes in 2 consecutive GCI frames (or until it is acknowledged), with E = 1 to indicate this is the last byte of the transfer. The receiver verifies this byte is the same for 2 frames and sends an acknowledgement by sending A = 1 in the next frame. If an abort is required, the receiver will maintain A = 1 for another frame. If a Monitor channel message originated by the TP3410 is aborted, it will repeat the complete message until it is successfully acknowledged.

8.4 C/I Channel

The C/I (Command/Indicate) channel in GCI byte 4 is used solely to access the Activation Control Register and the Activation Indication Register in the TP3410. A complete description of these registers is found in Section 11, including the coding of the 4-bit messages. Unlike the Microwire Mode of the device, however, the contents of these 2 registers are transferred repeatedly in the C/I channel, once per GCI frame. A change in transmit message is originated by a change in the Activation Indication Register, while a change in received message is verified in 2 consecutive GCI frames before updating the Activation Control Register and taking the appropriate action.

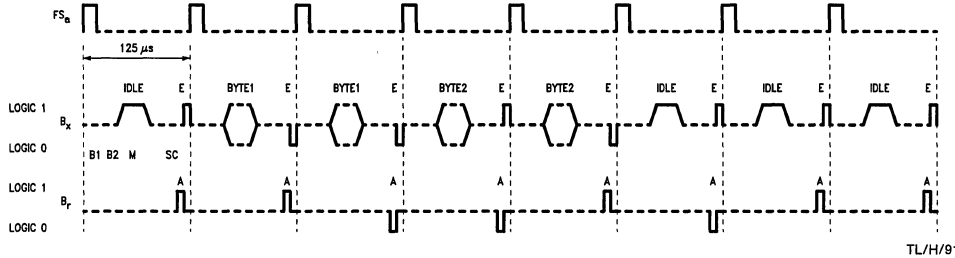


TL/H/9151–16

Note 1: As an output (GCI Master) FS_a is high for 8-bit intervals (16 BCLK cycles). As an input (GCI Slave) FS_a must be high for ≥ 1 BCLK cycle.

Note 2: The FSb output is provided only in GCI Master Mode.

FIGURE 7. GCI Frame Structure (BCLK = 4.096 MHz)



TL/H/9151–27

FIGURE 8. GCI Monitor Channel E and A Bit Protocol

Functional Description (Continued)

TABLE II. Command Registers

Function	Byte 1 (Register Address)								Byte 2 (Data)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
No Operation (NOP)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Write OPR	0	0	1	0	0	0	0	0	CIE	EIE	FIE	OB1	OB0	OC1	OC0	2CE
Readback OPR	0	0	1	0	0	0	0	1	X	X	X	X	X	X	X	X
Write CR1	0	0	1	0	0	0	1	0	FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX
Readback CR1	0	0	1	0	0	0	1	1	X	X	X	X	X	X	X	X
Write CR2	0	0	1	0	0	1	0	0	SSS	NTS	DMO	DEN	DD	BP1	BP2	0
Readback CR2	0	0	1	0	0	1	0	1	X	X	X	X	X	X	X	X
Write CR3	0	0	1	0	0	1	1	0	LB1	LB2	LBD	DB1	DB2	DBD	TLB	0
Readback CR3	0	0	1	0	0	1	1	1	X	X	X	X	X	X	X	X
Write TXB1 TSA	0	0	1	1	0	0	0	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
Readback TXB1	0	0	1	1	0	0	0	1	X	X	X	X	X	X	X	X
Write TXB2 TSA	0	0	1	1	0	0	1	0	0	0	TS5	TS4	TS3	TS2	TS1	TS0
Readback TXB2	0	0	1	1	0	0	1	1	X	X	X	X	X	X	X	X
Write RXB1 TSA	0	0	1	1	0	1	0	0	EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0
Readback RXB1	0	0	1	1	0	1	0	1	X	X	X	X	X	X	X	X
Write RXB2 TSA	0	0	1	1	0	1	1	0	EB2	0	TS5	TS4	TS3	TS2	TS1	TS0
Readback RXB2	0	0	1	1	0	1	1	1	X	X	X	X	X	X	X	X
Write TXD	0	0	1	1	1	0	0	0	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
Readback TXD	0	0	1	1	1	0	0	1	X	X	X	X	X	X	X	X
Write RXD	0	0	1	1	1	0	1	0	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
Readback RXD	0	0	1	1	1	0	1	1	X	X	X	X	X	X	X	X
Write TXM4	0	1	0	0	0	0	0	0	ACT	M42	M43	M44	M45	M46	M47	M48
Write TXM56	0	1	0	0	0	0	1	0	0	0	LEC	M51	M61	M52	TFB	CTC
Write ACT Register	0	1	0	0	0	1	0	0	0	0	0	0	C4	C3	C2	C1
Write ECT1	0	1	0	0	0	1	1	0	O7	O6	O5	O4	O3	O2	O1	O0
Read BEC1	0	1	0	0	0	1	1	1	X	X	X	X	X	X	X	X
Write ECT2	0	1	0	0	1	0	0	0	O7	O6	O5	O4	O3	O2	O1	O0
Read BEC2	0	1	0	0	1	0	0	1	X	X	X	X	X	X	X	X
Write TX EOC Register	0	1	0	1	ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

Note 1: Bit 7 of byte 1 is always the first bit clocked into the device.

Note 2: In the Tx EOC Register:
ea1 = the msb of the EOC destination address;
ea2 = bit 2 of the EOC destination address;
ea3 = the lsb of the EOC destination address;
dm = the EOC data/message mode indicator.

Note 3: X = don't care (it is recommended that these bits be set = 0).

Functional Description (Continued)

TABLE III. Status Registers

Function	Byte 1 (Register Address)								Byte 2 (Data)							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
READABLE CONFIGURATION REGISTERS																
Default (No Change on a Write Cycle)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OPR Contents	0	0	1	0	0	0	0	1	CIE	EIE	FIE	OB1	OB0	OC1	OC0	2CE
CR1 Contents	0	0	1	0	0	0	1	1	FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX
CR2 Contents	0	0	1	0	0	1	0	1	SSS	NTS	DMO	DEN	DD	BP1	BP2	0
CR3 Contents	0	0	1	0	0	1	1	1	LB1	LB2	LBD	DB1	DB2	DBD	TLB	0
TXB1 Contents	0	0	1	1	0	0	0	1	0	0	TS5	TS4	TS3	TS2	TS1	TS0
TXB2 Contents	0	0	1	1	0	0	1	1	0	0	TS5	TS4	TS3	TS2	TS1	TS0
RXB1 Contents	0	0	1	1	0	1	0	1	EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0
RXB2 Contents	0	0	1	1	0	1	1	1	EB2	0	TS5	TS4	TS3	TS2	TS1	TS0
TXD Contents	0	0	1	1	1	0	0	1	DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0
RXD Contents	0	0	1	1	1	0	1	1	DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0
BEC1 (Note 2)	0	1	0	0	0	1	1	1	ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0
BEC2 (Note 2)	0	1	0	0	1	0	0	1	ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0
REGISTERS WHICH GENERATE A MICROWIRE INTERRUPT OR GCI MONITOR CHANNEL MESSAGE (Note 4)																
RXM4	0	1	0	0	0	0	0	0	M41	M42	M43	M44	M45	M46	M47	M48
RXM56 Spare Bits	0	1	0	0	0	0	1	0	0	ES1	ES2	M51	M61	M52	RFB	NEB
ACT Indication Reg	0	1	0	0	0	1	0	0	0	0	0	0	C4	C3	C2	C1
BEC1 (Note 2)	0	1	0	0	0	1	1	0	ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0
BEC2 (Note 2)	0	1	0	0	1	0	0	0	ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0
RX EOC Register (Note 3)	0	1	0	1	ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

Note 1: Bit 7 of byte 1 is always the first bit clocked into the device.

Note 2: BEC1 and BEC2 may be polled, via the appropriate read command (see Table II), at any time to read the current error count.

Note 3: In the Rx EOC Register:
ea1 = the msb of the EOC destination address;
ea2 = bit 2 of the EOC destination address;
ea3 = the lsb of the EOC destination address;
dm = the EOC data/message mode indicator.

Note 4: Changes in contents of these registers are queued on a stack which generates interrupts or messages in the following priority order:

1. ACT Indication Register (Microwire only).
2. RXM4 Register.
3. RX EOC Register.
4. RXM56 Spare Bits Register.
5. BEC1 Register.
6. BEC2 Register.
7. Register Readback request.

Functional Description (Continued)

9.0 COMMAND REGISTER FUNCTIONS

All addressing and bit-level functions are the same for both the Microwire and GCI Monitor Channels, except where noted. An asterisk * indicates the Power-on Reset state of each function. The device modes and Transmit M bits should be programmed while the device is powered down.

9.1 Writing to Command Registers

A command may be written to a register to modify its contents by setting byte 1 bit 0=0. Registers CR1, 2, 3, OPR and the Time-Slot Assignment registers may also be readback to verify the contents by addressing each register with byte 1 bit 0=1. In Microwire Mode, if the device has no data waiting to be read during a command cycle it will return X'0000 (No Change).

9.2 Reading Back Command Registers for Verification

To read back the current state of one of the write-able registers, the appropriate readback command must first be loaded in via the control channel; this will cause an interrupt to be sent to the interrupt stack. In Microwire mode the interrupt must be serviced by a read cycle, in which the command should be a NOP (or a new command). In this cycle the previously addressed register is readback, with byte 1 bit 0=1. In GCI mode, the interrupt stack generates an autonomous one-way message in the Monitor Channel. If any other interrupt conditions should occur during the readback command cycle, the readback result will be queued at the bottom of the stack, and will not generate its interrupt or message until all other interrupts are cleared.

9.3 Configuration Register CR1: Digital Interface

Byte 2							
7	6	5	4	3	2	1	0
FF1	FF0	CK2	CK1	CK0	DDM	CMS	BEX

*CR1 is set to X'00 at Power-On Reset.

FF1, FF0: Digital System Interface Frame Format Selection

These bits are effective in Microwire Mode only (MW=1). They select the Digital Interface format as described in Section 6.

Format	FF1	FF0
*1	0	0
2	0	1
3	1	0
4	1	1

CK0–CK2: Digital Interface Clock Select

In Microwire Mode only, and if DSI Master is selected (CMS = 1), CK0–CK2 bits select from a choice of 5 frequencies for the BCLK output. In GCI Mode, these bits have no effect; also, 256 kHz is not valid with Format 4.

CK2	CK1	CK0	BCLK Frequency:
0	0	0	*256 kHz Master
0	0	1	512 kHz Master
0	1	0	1536 kHz Master
0	1	1	2048 kHz Master
1	0	0	2560 kHz Master

DDM: Delayed Data Mode Select

For Microwire mode, see Section 6.1: FS Relationship to Data. In GCI Mode this bit has no effect.
*DDM = 0 for non-delayed data mode (see *Figure 11*).
DDM = 1 for delayed data mode (see *Figure 12*).

CMS: DSI Clock Master/Slave Select

In Microwire Mode (MW = 1):
CMS = 0 for DSI Slave; may be used in either LT or NT Modes
CMS = 1 for DSI Master; may be used in NT Mode only.
In GCI Mode (MW = 0) this bit has no effect; the MO pin selects GCI Master or Slave.

BEX: B Channel Exchange

This command enables the two B channels to be exchanged as the data passes through the device between the Digital Interface and the Line in both directions. It should not be used if any loopback is selected in the device.
*BEX = 0 for B channels mapped direct, B1 to B1 and B2 to B2.
BEX = 1 for B channels exchanged, B1 to B2 and B2 to B1.

9.4 Configuration Register CR2: Device Modes

Byte 2							
7	6	5	4	3	2	1	0
SSS	NTS	DMO	DEN	DD	BP1	BP2	0

*CR2 is set to X'00 at Power-On Reset.

SSS: Superframe Synchronization Select

This bit is effective in LT mode only; in NT mode the SFS pin is an output. When SSS = 0, SFS is an input which synchronizes the transmit superframe counter on the line.

When SSS = 1, SFS is an output superframe marker pulse.

NTS: NT or LT Select

*NTS = 0 for LT Mode.
NTS = 1 for NT Mode.

DEN: D Channel Port Select

*When DEN = 0, the D channel port is disabled and the D bits are transferred on the Br and Bx pins, clocked by BCLK. The Dx and DCLK pins must also be tied to GND for correct operation.

When DEN = 1, the D channel port is enabled; D bits are transferred on the Dr and Dx pins in a mode selected by the DMO bit, see Section 6.3.

DMO: D Channel Transfer Mode Select

This bit is significant only when the D channel port is selected (DEN bit = 1).

When DMO = 1, D channel data is shifted in and out on Dx and Dr pins in a continuous mode at 16 kbit/s on the falling and rising edges of DCLK respectively, see *Figure 4*.

When DMO = 0, D channel data is shifted in and out on Dx and Dr pins in a burst mode at the BCLK frequency when the assigned time-slots are active, see *Figure 5*.

Functional Description (Continued)

DD: 2B + D Data Disabling

*When DD = 0, 2B + D channel transfer is enabled as soon as the line is completely synchronized.

When DD = 1, B and D channel transfer is inhibited, the data transmitted to line is scrambled 1's, and the 2B + D slots at the receive digital interface port(s) are in the high impedance state.

BP1, BP2: Activation Breakpoints

These bits are effective only in LT mode. They provide for the activation sequence to be either automatically controlled by the TP3410, or for the external controller to be able to halt the sequence at either or both of 2 pre-determined state(s), see the Activation section.

*BP1 = 0 for Breakpoint 1 disabled.
BP1 = 1 for Breakpoint 1 enabled.
*BP2 = 0 for Breakpoint 2 disabled.
BP2 = 1 for Breakpoint 2 enabled.

9.5 Configuration Register CR3: Loopbacks

Byte 2							
7	6	5	4	3	2	1	0
LB1	LB2	LBD	DB1	DB2	DBD	TLB	0

*CR3 is set to X'00 at Power-On Reset.

Line Loopbacks Select: LB1, LB2, LBD

LB1, LB2, LBD bits, when set = 1, loopback each individual B1, B2, or D channel respectively from the line receive input to the line transmit output. They may be set separately or together. Each loopback is operated near the Bx and Br digital interface pins (or Dx and Dr if the D port is selected). These loopbacks may be either transparent, that is data received from the line is also passed on to the digital interface, or non-transparent, in which case the selected channel bits on the digital interface are in the high impedance state; transparency is controlled by the TLB bit.

Digital Loopbacks Select: DB1, DB2, DBD

DB1, DB2 and DBD bits, when set = 1, turn each individual B1, B2, or D channel respectively from the Bx input to the Br output (or Dx and Dr if the D port is selected). They may be set separately or together. Each loopback is operated near the digital interface pins; if Format 3 is selected there is no restriction on the time-slots selected for each direction. These loopbacks may be either transparent, that is data received from the Bx or Dx input is also transmitted to the line, or non-transparent, in which case the selected channel bits to the scrambler are forced low in LT mode or high in NT mode; transparency is controlled by the TLB bit.

TLB: Transparent Loop-Back Enabling

*TLB = 0 for non-transparent loopbacks (B1, B2 or D channel).
TLB = 1 for transparent loopbacks.

9.6 Configuration Registers TXB1, TXB2, RXB1, RXB2: B Channel TSA

These registers are effective when Format 3 is selected only.
TXB1 assigns the Transmit time slot for the B1 channel.
TXB2 assigns the Transmit time slot for the B2 channel.
RXB1 assigns the Receive time slot for the B1 channel.
RXB2 assigns the Receive time slot for the B2 channel.

Register TXB1

Byte 2							
7	6	5	4	3	2	1	0
0	0	TS5	TS4	TS3	TS2	TS1	TS0

At Power-On Reset this register is initialized to X'00.

Register TXB2

Byte 2							
7	6	5	4	3	2	1	0
0	0	TS5	TS4	TS3	TS2	TS1	TS0

At Power-On Reset this register is initialized to X'01.

Register RXB1

Byte 2							
7	6	5	4	3	2	1	0
EB1	ED	TS5	TS4	TS3	TS2	TS1	TS0

At Power-On Reset this register is initialized to X'00.

Register RXB2

Byte 2							
7	6	5	4	3	2	1	0
EB2	0	TS5	TS4	TS3	TS2	TS1	TS0

*At Power-On Reset this register is initialized to X'01.

B Channels Time-Slot Assignment: TS5–TS0

The TS5–TS0 bits define the binary number of the time-slot when the B channel selected is shifted to or from the Bx and Br pins; time-slots are numbered from 0 to 63. New time-slot assignments become effective only at the beginning of a frame.

B1 and D Channel Enables: EB1; ED

*EB1 = 0 to disable the B1 channel; B1 is high-impedance at Br.
EB1 = 1 to enable the B1 channel (must also set DD = 0 in CR2).
*ED = 0 to disable the D channel; D is high-impedance at Br or Dr.
ED = 1 to enable the D channel (must also set DD = 0 in CR2).

B2 Channel Enable: EB2

EB2 = 0 to disable the B2 channel; B2 is high-impedance at Br.
EB2 = 1 to enable the B2 channel (must also set DD = 0 in CR2).

Functional Description (Continued)

9.7 Configuration Register TXD: Transmit D Channel TSA

This register is effective only when Format 3 is selected. D channel TSA may be used when the D channel is accessed either via the Bx/Br or Dx/Dr pins, but the D channel port must be clocked with BCLK (DMO = 0 in CR2).

Byte 2							
7	6	5	4	3	2	1	0
DX5	DX4	DX3	DX2	DX1	DX0	SX1	SX0

*At Power-On Reset this register is initialized to X'08.

Transmit D Channel Time-Slot Assignment Select: DX5–DX0, SX1–SX0

DX5–DX0 bits define the binary number of the 8-bit wide time-slot, where time-slots are numbered from 0 to 63. Within this selected time-slot, the SX1 and SX0 bits define the 2-bit wide sub-slot for the 2 D channel bits. Sub-slots are numbered 0 to 3, as shown in *Figures 5, 11* and *12* and the following table. New time-slot and sub-slot assignments become effective only at the beginning of a frame.

Sub-Slot		Bit Positions within Time-Slot
SX1	SX0	
*0	0	1, 2
0	1	3, 4
1	0	5, 6
1	1	7, 8

9.8 Configuration Register RXD: Receive D Channel TSA

This register is effective only when Format 3 is selected. D channel TSA may be used when the D channel is accessed either via the Bx/Br or Dx/Dr pins, but the D channel port must be selected in the burst mode (DMO = 0 in CR2).

Byte 2							
7	6	5	4	3	2	1	0
DR5	DR4	DR3	DR2	DR1	DR0	SR1	SR0

*At Power-On Reset this register is initialized to X'08.

Receive D Channel Time-Slot Assignment Select: DR5–DR0, SR1–SR0

DR5–DR0 bits define the binary number of the 8-bit wide time-slot, where the time-slots are numbered from 0 to 63. Within this selected time-slot, the SR1 and SR0 bits define the binary number of the 2 D channel bits. Sub-slots are numbered 0 to 3, as shown in *Figure 12* and the following table. New time-slot and sub-slot assignments become effective only at the beginning of a frame.

Sub-Slot		Bit Positions within Time-Slot
SR1	SR0	
*0	0	1, 2
0	1	3, 4
1	0	5, 6
1	1	7, 8

9.9 Configuration Register OPR: Overhead Bit Processing

This register controls the enabling/disabling of conditions which are sent to the Interrupt Stack (see 10.1) as a result of new data in the RXM4 and RXM56 Overhead Bits Registers, and the number of consecutive times a new bit or message is received before being validated. Flexibility is therefore provided to use hardware or external firmware routines for validation, or a combination of both.

Byte 2							
7	6	5	4	3	2	1	0
CIE	EIE	FIE	OB1	OB0	OC1	OC0	2CE

*At Power-On Reset this register is initialized to X'00.

Near-End CRC Interrupt Enable: CIE

CIE

*0 No Interrupt if near-end crc error (Block Error Counters still count).

1 RXM56 Status Register Interrupt is generated, with NEB = 0, each superframe in which the locally-generated crc result does not match the crc in the received superframe.

Block Error Counter Interrupt Enable: EIE

EIE

*0 No Interrupt or Monitor channel message from Block Error Counters.

1 Block Error Counter Interrupts enabled.

febe Bit Interrupt Enable: FIE

FIE

*0 No Interrupt if febe = 0 received (BEC1 still counts).

1 RXM56 Status Register Interrupt is generated, with RFB = 0, each superframe in which febe = 0 is received.

Receive Overhead Bits Interrupt Enable: 0B1, 0B0

These bits determine how many consecutive superframes must be received with the same new data in any of the overhead bit positions M41–M48, M51, M52 and/or M61 before an Interrupt(s) is generated for the RXM4 and/or RXM56 Register, as appropriate. Note that validation checking of the "act" and "dea" bits during activation/deactivation is not affected by OB1/OB0.

OB1	OB0	
*0	0	Interrupt every superframe (no checking).
0	1	Interrupt if any bit changed from previous superframe.
1	0	2 consecutive times for same new bit(s) before Interrupt.
1	1	3 consecutive times for same new bit(s) before Interrupt.

Functional Description (Continued)

Error Counter Configuration: 2CE

When 2CE=0, and if EIE=1, only one Block Error Counter is used for both febe and nebe bits; if both indicate an error within the same superframe, BEC1 is decremented by 1 count only, and BEC2 is not used. When 2CE=1, BEC1 is enabled to count febe errors only, and BEC2 is enabled to count nebe (near-end block errors) only.

Receive Embedded Operations Channel Interrupt Enable: OC1, OC0

These bits determine how many consecutive half-superframes must be received with the same new address or data in the Embedded Operations Channel before an Interrupt is generated for the RX EOC Register.

OC1	OC0	
*0	0	Interrupt every received eoc message (no checking).
0	1	Interrupt every received eoc message which differs from previous message.
1	0	2 consecutive times for same new message before Interrupt.
1	1	3 consecutive times for same new message before Interrupt.

9.10 Transmit M4 Channel Register TXM4 (Write Only)

When the line is superframe synchronized, the device transmits the contents of this register to the line in the M4 overhead bit field once per superframe.

Byte 2							
7	6	5	4	3	2	1	0
ACT	M42	M43	M44	M45	M46	M47	M48

At Power-On Reset, and each time the device is Deactivated (or an Activation attempt fails), this register is initialized to X'7F.

ACT Bit

During the Activation and Deactivation sequences, the ACT bit in this register is generated automatically within the device and transmitted to the line as the "act" bit of the M4 word. When the line is fully Activated, the transmitted bit corresponds to the ACT bit in this register; therefore, when changing the state of other bits on an activated line, a 1 should be written to this bit position.

M42–M48 Bits

As shown in the Frame Formats in Table I, the functions of these bits depend on the mode of the device. They should be programmed as appropriate prior to an Activation Request, with the exception of the M42 bit in LT Mode. This is the dea bit, which is automatically controlled by the device in response to AR and DR commands; the M42 bit in this register is ignored in LT mode.

9.11 Transmit M5/M6 Spare Bits Register TXM56 (Write Only)

Byte 2							
7	6	5	4	3	2	1	0
0	0	LEC	M51	M61	M52	TFB	CTC

At Power-On Reset, and each time the device is Deactivated (or an Activation attempt fails), this register is initialized to X'1E.

M51, M61, M52

The M51, M61, and M52 bits in this register control the appropriate overhead bits transmitted to the line. They should be set = 1 but may be subject to future standardization.

Transmit febe Bit Control: TFB

This bit should normally be set=1. The febe bit transmitted in the M62 bit position is then automatically controlled by the device; febe is the far-end block error bit which is normally high, and set low when a crc (cyclic redundancy check) error has been detected in the previously received superframe. For test purposes, however, febe may be forced continuously low by setting TFB = 0.

Corrupt Transmit crc: CTC

To allow the normal calculation of the crc for the transmitted data to the line, set CTC = 0. In order to send a corrupted crc for test purposes, set CTC = 1, which causes the crc result to be continuously inverted prior to transmission.

Latched External Control: LEC

This bit directly controls the LEC output pin, in GCI mode.

9.12 Transmit EOC Register (Write Only)

When the line is fully superframe synchronized, the device continuously sends the contents of this register to the line twice per superframe in the EOC channel field. The register contents are loaded into the line transmit register every half superframe.

Byte 1				Byte 2							
3	2	1	0	7	6	5	4	3	2	1	0
ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

At Power-On Reset, and each time the device is Deactivated (or an Activation attempt fails), this register is initialized to X'111.

The Tx EOC Register contains 12 bits which correspond to the 12 bits of a message in the Embedded Operations Channel, see Table I:

ea1, ea2 and ea3 correspond to the 3 EOC destination address bits, eoca1, eoca2, eoca3;

the dm bit indicates if the information is in message mode or data mode;

ei1–ei8 correspond to the 8 eoc data bits, eoci1–eoci8.

Only bits 7–4 of byte 1 are used to address this register, as shown in Table I.

9.13 Error Counter Threshold Registers: ECT1, ECT2

Byte 2							
7	6	5	4	3	2	1	0
O7	O6	O5	O4	O3	O2	O1	O0

At Power-On Reset these registers are initialized to X'FF.

Each of these registers is preset with a value which is compared with the value in the corresponding Block Error Counter. When the values match, the appropriate counter interrupt is sent to the stack (if EIE = 1).

Functional Description (Continued)

10.0 STATUS REGISTERS

All Status Register addressing and bit-level functions are the same for both the Microwire and GCI Monitor Channels, except where noted.

10.1 Reading Status Registers In Response To An Interrupt

Conditions occurring in the device which generate Microwire interrupts or GCI Monitor Channel messages are queued in a stack, with a pre-defined priority, see Table III. In Microwire mode the $\overline{INT}$ pin is pulled low and a NOP command should be loaded into the Microwire during the read cycle (or a valid command may be used to modify a register if required). In GCI mode, the interrupt stack generates an autonomous one-way message in the Monitor Channel.

10.2 Receive EOC Register

This register is significant only when the EOC channel processing is enabled (see register OPR).

Byte 1				Byte 2							
3	2	1	0	7	6	5	4	3	2	1	0
ea1	ea2	ea3	dm	ei1	ei2	ei3	ei4	ei5	ei6	ei7	ei8

The Rx EOC Register contains 12 bits which correspond to the 12 bits of a message in the Embedded Operations Channel, see Table I: ea1, ea2 and ea3 correspond to the 3 EOC destination address bits, eoca1, eoca2, eoca3;

the dm bit indicates if the information is in message mode or data mode;

ei1–ei8 correspond to the 8 eoc data bits, eoci1–eoci8.

Only bits 7–4 of byte 1 are used to address this register, as shown in Table II.

When the line is fully superframe synchronized, the device extracts these 12 bits from the channel every half superframe. Each EOC message is validated according to the mode selected in Register OPR, and if a message contains a new address or new data, the Rx EOC Register is sent to the Control Interface, through an interrupt cycle request. If one of the defined coded commands is received, e.g., Send Corrupted CRC, then the appropriate Command Register instruction must be written to the device to select that function.

10.3 RXM4: Receive M4 Overhead Bits Register

This register is significant only when the Spare Bit processing is enabled (see register OPR).

Byte 2							
7	6	5	4	3	2	1	0
M41	M42	M43	M44	M45	M46	M47	M48

The Rx M4 Register consists of 8 bits, which correspond to the M4 overhead bit position in each of the 8 Basic Frames of a superframe. When the line is fully superframe synchronized, the device extracts from the M channel these 8 bits every superframe. At the end of each superframe, the register content is sent to the Interrupt stack, in accordance with the validation mode selected in Register OPR. M41, and M42 in NT mode, are only provided via this register while the line is fully activated (after AI). During the activation and deactivation sequences the "act" and "dea" bits are processed automatically, see the Activation Control section.

10.4 RXM56: Receive M5/M6 Spare Bits Status Register

This regiser is significant only when the Spare Bit processing is enabled (see register OPR).

Byte 2							
7	6	5	4	3	2	1	0
0	ES1	ES2	M51	M61	M52	RFB	NEB

Data in this register consists of 7 bits: M51, M52, M61 and RFB (RFB = receive febe, the far-end block-error indicator from the M62 bit position), all of which correspond to the overhead bits received once per superframe, plus NEB, which is an internally generated bit indicating a near-end block-error. Bits ES1 and ES2 are available in GCI mode only. When the line is fully superframe synchronized, the device loads the register with the received bits M51, M52, M61 and febe every superframe; in GCI mode the ES1 and ES2 input pins are also sampled. The 12-bit crc received from the far-end is also compared at the end of the superframe with the crc previously calculated by the device. If an error is detected, the febe bit in the transmit direction is automatically forced low in the next superframe and the NEB bit in this register is set low also. The register content is sent to the Interrupt stack at the end of each superframe.

10.5 Block Error Counters: BEC1, BEC2

Byte 2							
7	6	5	4	3	2	1	0
ec7	ec6	ec5	ec4	ec3	ec2	ec1	ec0

At Power-On Reset each counter is preset = X'FF.

BEC1

This 8-bit counter is incremented by 1 each superframe in which febe = 0 is received. Alternatively, if bit 2CE = 0 in Register OPR, the counter is incremented if either febe = 0 or nebe = 0 in the same superframe. When the counter reaches the threshold value in the ECT1 register, (and if the Interrupt is enabled by means of the EIE bit in Register OPR), an interrupt is queued in the interrupt stack. The counter may also be read at any time; the count will be the number of errors since the last read of this register. Reading the counter causes the count to be reset to zero.

BEC2

This 8-bit counter is incremented by 1 each superframe in which a near-end crc error is detected. When the counter reaches the threshold value in the ECT2 register, (and if the Interrupt is enabled by means of the EIE bit in Register OPR), an interrupt is queued in the interrupt stack. The counter may also be read at any time; the count will be the number of errors since the last read of this register. Reading the counter causes it to be reset to zero.

Functional Description (Continued)

11.0 ACTIVATION/DEACTIVATION

A common coding table is used for the commands in the Activation Control Register and the status indicators in the Activation Indication Register. They control the Power-Up/Down, Activation and Deactivation states of the device. When the device is in GCI Mode, the 4 significant bits in these registers (3–0) continuously report their current contents in the C/I channel. In Microwire Mode the registers are addressed with a normal 16-bit cycle as shown in Table II.

11.1 Activation Control Register

Byte 2							
7	6	5	4	3	2	1	0
0	0	0	0	C4	C3	C2	C1

At Power-On Reset, and each time the device is Deactivated (or an Activation attempt fails), this register is initialized to X'0F.

Activation commands and status indicators are coded as follows:

CODE				LT MODE		NT MODE	
C4	C3	C2	C1	IND	COM	IND	COM
0	0	0	0	X	PUP/DR	DP/LSD	PUP
0	0	0	1	X	RES	X	RES
0	1	0	0	EI	X	EI	SEI
0	1	0	1	X	PDN	X	PDN
0	1	1	0	SYNC	X	X	X
0	1	1	1	UAI	UAR	UAR	UAI
1	0	0	0	AP	AR	AP	AR
1	1	0	0	AI	AC	AI	AC
1	1	1	1	DI	DI*	DI	DI*

Note 1: X indicates reserved codes which should not be used.

11.2 Activation Commands

PUP — This command powers up the device and starts the oscillator.

PUP/DR — When the TP3410 is in the power-down state, this command powers up the device and starts the oscillator. In LT mode only, when the device is activated, this code is a Deactivation Request, which forces the device through the specified deactivation sequence by setting "dea" = 0 in 6 consecutive superframes before ceasing transmission.

PDN — This power-down command immediately forces the device to a low power state, without sequencing through any of the de-activation states. It should normally only be used after the TP3410 has been put in a known state, e.g., in an NT after a DI status indication has been reported.

AR — Activation Request, which is used after first powering up the device to initiate the specified Activation sequence.

AC — Activation Complete, which may be used to set "act" = 1 in each direction at the completion of activation. In LT mode this is only necessary if Breakpoint 2 is enabled (in Register CR2); in NT mode this is normally required when synchronization on the S/T Interface is confirmed by detection of INFO3.

RES — RES is the reset command which resets the activation sequencer to the Receive Reset state and resets the DSP coefficients in preparation for a cold-start. This command should be used only in the event of a failed activation attempt (expiry of T4 or T5); it does not affect the Command Registers.

SEI — S-Interface Error Indication, which should only be used in an NT-1 when loss of received signal is detected (i.e., INFO 0). This command forces the upstream "act" bit (M41) = 0.

UAR — In an LT, using Restricted Activation mode, this command can be used instead of AR to activate the U Interface without starting activation at the S/T interface.

UAI — In an NT, using Restricted Activation mode, this command sets the upstream M48 bit = 0 to indicate completion of activation.

11.3 Activation Indication Register: (READ ONLY)

Byte 2							
7	6	5	4	3	2	1	0
0	0	0	0	C4	C3	C2	C1

Activation Indicators are coded the same as for the Activation Control Register. In Microwire mode only, at each activation status change the four significant bits in this register are sent to the Interrupt stack. If multiple interrupt conditions should arise simultaneously, this register has the highest priority and will be read first.

11.4 Activation Status Indicators

DP/LSD — When the TP3410 is deactivated, either powered up or powered down, the Line Signal Detector sets this indicator if it detects an incoming 10 kHz wake-up tone. If the device is powered down the $\overline{\text{LSD}}$ pin is also pulled low. In NT mode only, this code also functions as a Deactivation Pending indicator when "dea" = 0 is validated.

SYNC — In LT mode only this indicates when superframe sync is detected, and should be used to stop the external default timer.

AP — Activation Pending, which is used in NT mode to indicate when superframe sync has been acquired and the BCLK and FS outputs are synchronized to the received line signal. In LT mode, the Line Signal Detector sets this indicator if it detects an incoming 10 kHz wake-up tone.

AI — This Activation Indication code indicates that the loop is fully activated, ("act" = 1 has been received), and the 2B + D channels are enabled for data transfer. In LT mode, however, if Breakpoint #2 is enabled via CR2, it is necessary to respond to AI with an AC command. This will cause the device to set "act" = 1 in the transmit frame and open the 2B + D channels for data transfer.

Functional Description (Continued)

EI Loss of frame synchronization will set this Error Indicator and inhibit the 2B+D channel data. If a received line signal can still be detected the device will attempt to recover synchronization for up to 480 ms; if this fails it will enter the RESET state and generate a DI.

DI The Deactivated Indication, which confirms that the loop has been deactivated by means of a Deactivate Request at the LT, and has entered the RESET state. DI* is effective in GCI mode only.

UAI In an LT, this code is the Activation Indication for the U Interface only, when the Restricted Activation sequence is completed.

UAR In NT mode, using Restricted Activation, this indicator is generated when the downstream M48 bit=0 is received.

11.5 Cold Start and Warm Start

When power is first applied to the device, the first AR command will always initiate a cold-start sequence, which may take up to 15 seconds for complete activation. If the device is subsequently deactivated using the correct procedure, and provided power is maintained uninterrupted in either the power-up or power-down state, the next AR instruction automatically sequences through the warm-start procedure, which normally achieves complete loop activation within 300 ms.

11.6 LT Mode Activation/Deactivation

If activation is initiated by the downstream (NT mode) end, when the device is either powered up or down, an AP Interrupt condition will be generated on detection of the 10 kHz "wake-up" tone. The Activation Indication Register will show this condition and, if the device is powered down, the $\overline{\text{LSD}}$ pin will be pulled low.

Prior to initiating activation all registers must be programmed appropriately and the device must then be powered up. The use of the commands and status indicators is the same when activation is initiated locally or from the remote end. If no activation breakpoints are enabled, an AR command will enable the device to proceed with the activation sequence. An external default timer should also be started (in North America the timer value should be 15 seconds if a single loop section is being activated). If activation is not successfully completed before expiry, this timer can be used to provide a fault indication and to generate a RES command to the Activation Control Register to ensure that the Activation Sequencer returns to the Full Reset state (J10 to J1) prior to any re-attempt to activate.

The sequence continues automatically until superframe synchronization is acquired on the SN3 signal received from the NT. At this point the "act" bit is set = 1 in the downstream direction, and the AI Interrupt is generated in the Activation Indication Register. The loop is then fully activated, with all channels in the data stream available for use.

For additional control over the activation sequence, 1 or 2 breakpoint states may be enabled at the LT. Breakpoint 1 will halt the sequence following initial detection of the 10 kHz wake-up signal (TN) from the NT if the TE initiates activation; an AR command is then required to enable activation to continue. Breakpoint 2 will halt the sequence when the loop is fully synchronized, receiving SN3, but the "act" bit is held = 0; this state prevents the S/T Interface from becoming fully activated (the NT1 will maintain INFO2 towards the TEs). An AC command will release this state, allowing activation to be completed. Two bits in Register CR2 control the enabling of these breakpoints.

Deactivation is initiated by writing the DR command in the Activation Control Register, causing "dea"=0 to be transmitted towards the NT. When the NT ceases to transmit, confirmation of deactivation is provided by a DI Status indicator.

11.7 NT Mode Activation/Deactivation

If activation is initiated by the upstream (LT mode) end, when the NT is either powered up or down, a Line Signal Detect Interrupt condition will be generated on detection of the 10 kHz "wake-up" tone. The Activation Indication Register will show this condition and, if the device is powered down, the $\overline{\text{LSD}}$ pin will be pulled low. To proceed with the activation sequence, all registers must be programmed appropriately (see Note 1) and the device must then be powered up. The use of the commands and status indicators is the same when activation is initiated locally or in response to the Line Signal Detect Interrupt. An AR command will enable the device to automatically proceed with the activation sequence. An external default timer should also be started (in North America the timer value should be 15 seconds if a single DSL section is being activated). If activation is not successfully completed before expiry, this timer can be used to provide a fault indication and to generate a RES command to the Activation Control Register to ensure that the Activation Sequencer returns to the Full Reset state (H10 to H1) prior to any re-attempt to activate.

The sequence continues until the NT acquires superframe synchronization on the SL2 signal received from the LT. At this point an AP Interrupt is generated and the device starts transmitting SN3 with "act" = 0. To complete activation, normally when the NT has detected INFO3 signals from a TE, the "act" bit must be set = 1 by writing the AC command to the Activation Control Register. An AI Status indication will finally be generated by the device when the loop is fully synchronized and receiving SL3 frames with "act"=1; this is automatically validated 3 times regardless of the options selected in Register OPR. The loop is then fully activated, with all channels in the data stream available for use.

Deactivation is normally initiated by the LT, which sets "dea"=0 towards the NT. The TP3410 in NT mode will detect and validate this bit 3 times prior to setting the DP interrupt (regardless of the options selected in OPR). Transmission will cease when it is detected that the far-end signal has ceased, after which the device enters the Reset state and generates a DI Interrupt to indicate that deactivation is complete.

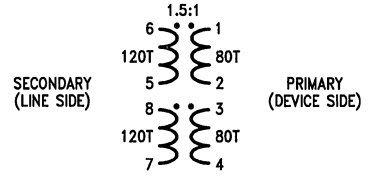
Note 1: The M45 bit conveys an indication of whether the NT can support a warm-start procedure (the "cso" bit). Since the TP3410 automatically supports both cold and warm start, set "cso"=0.

Applications Information

LINE INTERFACE CIRCUIT

It is very important, for compliance with the ANSI Standard, that the recommended line interface circuit shown in *Figure 9* or *10* should be strictly adhered to. The channel response and insertion losses of these circuits have been carefully designed as an integral part of the overall signal processing system to ensure the performance requirements are met under all specified loop conditions. Deviations from this design may result in sub-optimal performance or even total failure of the system to activate on some types of loop.

TRANSFORMER DESIGN



TL/H/9151–18

Turns ratio: Np:Ns = 1:1.5.

Secondary inductance: L_S = 27 mH ±5%.

Winding resistances: 30Ω > (2.25 Rp + Rs) > 10Ω.

Return loss at 40 kHz against 135Ω > 26 dB.

Note: The line interface circuit must also meet the return loss mask specified in the ANSI standard.

Longitudinal balance of secondary: >60 dB for 0 < f < 4 kHz; >55 dB for 4 kHz < f < 160 kHz.

Saturation characteristics: THD < −70 dB when tested with 90 mA D.C. through the secondary and a 40 kHz sine-wave injected into the primary at a level which generates 5 Vp-p into 135Ω at the secondary.

TYPICAL DESIGN

Core: Siemens EP-17 with T38 ferrite and 2 mil paper gap.
Windings:

Winding	Number of Turns	Wire Gauge
1–2	80 Single	#34 AWG
6–5, 8–7	120+120 Bifilar	#36 AWG
3–4	80 Single	#34 AWG

Winding	Inductance	Resistance
1–2 + 3–4	12 mH	4.1Ω
5–6 + 7–8	27 mH	9.5Ω

Note: The split primary winding is designed to minimize leakage inductance.

BOARD LAYOUT

While the pins of the TP3410 are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

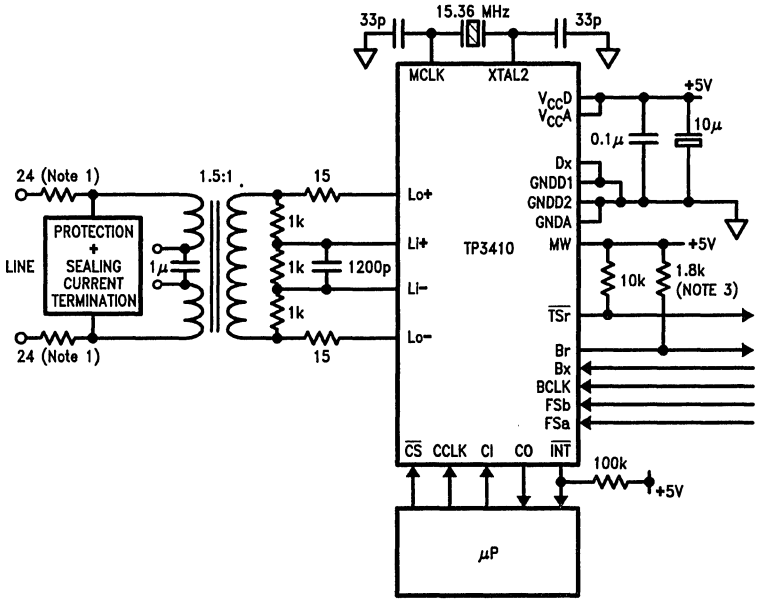
Great care must be taken in the layout of the printed circuit board in order to preserve the high transmission performance of the TP3410. To maximize performance do not use the philosophy of separating analog and digital grounds on the board. The 3 GND pins should be connected together as close as possible to the pins, and the 2 V_{CC} pins should be strapped together. All ground connections to each device should meet at a common point as close as possible to the 3 GND pins in order to prevent the interaction of ground return currents flowing through a common bus impedance. A decoupling capacitor of 0.1 μF should be connected from this common point to the V_{CC} pins. Taking care with the pcb layout in the following ways will also help prevent noise injection into the receiver front-end and maximize the transmission performance:

1. Keep the crystal oscillator components away from the receiver inputs and use a ground plane for shielding around these components.
2. Keep the connections between the device and the components on the Li± inputs short.
3. Keep the connections between the device and transformer short.

ADDITIONAL INFORMATION

For more in-depth information on a variety of applications, the TP3410 Users Manual is a comprehensive guide to the hardware and software required to meet the ANSI interface specification. Performance measurements, demonstrating compliance with ANSI transmission requirements, are also included.

Applications Information (Continued)



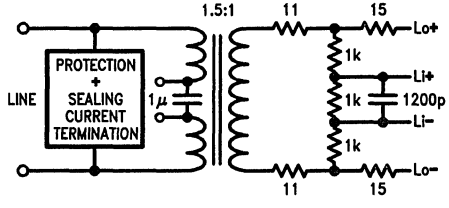
TL/H/9151–19

Note 1: 0.1% matching is required to meet the longitudinal balance specification. The 15Ω and 1k resistors in the line interface circuit should be 1% tolerance, and the capacitors should be 10%.

Note 2: An alternative circuit which removes the 24Ω surge-limiting resistors is shown in *Figure 10.*

Note 3: Only necessary in GCI Mode.

FIGURE 9. Typical Application in Microwire Mode



TL/H/9151–20

Note 1: All resistors 1% tolerance, and capacitors 10%.

Note 2: This circuit provides no surge current limiting for the transformer.

FIGURE 10. Alternative Interface Circuit

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at Li, Lo	V_{CC} + 1V to GND − 1V
Voltage at Any Digital Input	V_{CC} + 1V to GND − 1V
Storage Temperature Range	−65°C to +150°C
Current at Lo	±100 mA
Current at Any Digital Output	±50 mA
Lead Temperature (Soldering, 10 seconds)	300°C
ESD Rating to be Determined.	

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are electrical testing limits at V_{CC} = 5.0V and T_A = 25°C. All other limits are design goals for V_{CC} = 5.0V ±5% and T_A = 0°C to 70°C. This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2.2			V
VILX	Input Low Voltage	MCLK/XTAL Input			0.5	V
VIHX	Input High Voltage	MCLK/XTAL Input	V_{CC} − 0.5			V
V_{OL}	Output Low Voltage	Br, I_O = 3.2 mA All Other Digital Outputs, I_O = 1 mA			0.4	V
V_{OH}	Output High Voltage	Br, I_O = 3.2 mA All Other Digital Outputs, I_O = −1 mA All Outputs, I_O = −100 µA	2.4 2.4 V_{CC} − 0.5			V V V
I_I	Input Current	Any Digital Input, GND < V_{IN} < V_{CC}	−10		10	µA
I_{OZ}	Output Current in High Impedance State (TRI-STATE®)	Br, $\overline{INT}$, $\overline{LSD}$, CO, Dr GND < V_{OUT} < V_{CC}	−10		10	µA
LINE INTERFACES						
RLi	Differential Input Resistance	GND < Li+, Li− < V_{CC}	200			kΩ
CLLo	Load Capacitance	Between Lo+ and Lo− Connected Externally			200	pF
V_{OS}	Differential Output Offset Voltage at Lo+, Lo−		−20		+20	mV
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	All Outputs Open-Circuit		2		mA
$I_{CC}1$	Power Up Current	As Above, Device Activated		55		mA
TRANSMISSION PERFORMANCE						
	Transmit Pulse Amplitude	R_L = 115Ω between Lo+ and Lo− (Note 2)		±3.2		Vpk
	Transmit Pulse Linearity		36			dB
	Input Pulse Amplitude	Differential between Li+ and Li−	±4		±800	mVpk

Note 1: GND refers to GNDA, GNDD1 and GNDD2 commoned together; V_{CC} refers to V_{CC}A and V_{CC}D commoned together.

Note 2: In the circuits shown in *Figures 9* and *10*, terminated in 135Ω, this is equivalent to ±2.5V for isolated pulses of the outer levels. Selection of this test mode is described in the TP3410 Users Manual.

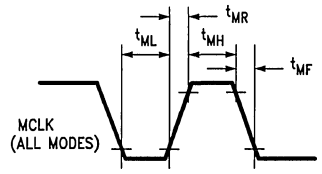
Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FMCK	Master Clock Frequency Master Clock Tolerance	Including Temperature, Aging, Etc.	 −100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
tMH, tML	Clock Pulse Width Hi & Low for MCLK	$V_{IH} = V_{CC} - 0.5V$ $V_{IL} = 0.5V$	20			ns
tMR, tMF	Rise and Fall Time of MCLK	Used as a Logic Input			10	ns
DIGITAL INTERFACE (*Figures 11, 12* and *13*)						
FBCLK	Frequency of BCLK	Formats 1, 2 and 3 GCI and Format 4	256 512		4096 6144	kHz kHz
tWBH	Period of BCLK High	Measured from V_{IH} to V_{IH}	25			ns
tWBL	Period of BCLK Low	Measured from V_{IL} to V_{IL}	25			ns
tRB	Rise Time of BCLK	Measured from V_{IL} to V_{IH}			15	ns
tFB	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			15	ns
tSFB	Setup Time, FS High to BCLK Low	DSI or GCI Slave Only	50			ns
tHBF	Hold Time, BCLK Low to FS, High or Low	DSI or GCI Slave Only	25			ns
tDBF	Delay Time, BCLK High to FS_a and FS_b Transitions	DSI or GCI Master Only			50	ns
tDBD	Delay Time, BCLK High to Data Valid	All Modes Load = 150 pF Plus 2 LSTTL Loads			80	ns
tDBZ	Delay Time, BCLK High to Br, Dr Disabled	All Modes			50	ns
tDBT	Delay Time, BCLK High to $\overline{TS}r$ Low if FS High, or FS High to $\overline{TS}r$ Low if BCLK High	Load = 100 pF Plus 2 LSTTL Loads			50	ns
tZBT	TRI-STATE Time, BCLK Low to $\overline{TS}r$ High				50	ns
tDFD	Delay Time, FS High to Data Valid	Load = 150 pF Plus 2 LSTTL Loads, Applies if FS Rises Later than BCLK Rising Edge in Non-Delayed Data Mode Only			80	ns
tSDB	Setup Time, Data Valid to BCLK Low	All Modes	0			ns
tHBD	Hold Time, BCLK Low to Data Invalid	All Modes	25			ns

Timing Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
MICROWIRE CONTROL INTERFACE (see *Figure 14*)						
tCH	CCLK High Duration		50			ns
tCL	CCLK Low Duration		50			ns
tSIC	Setup Time, CI Valid to CCLK High		25			ns
tHCI	Hold Time, CCLK High to CI Invalid		25			ns
tSSC	Setup Time from $\overline{CS}$ Low to CCLK High		50			ns
tDSO	Delay Time from $\overline{CS}$ Low to CO Valid	Byte 1, Bit C7 Only			50	ns
tDCO	Delay Time from CCLK Low to CO Data Valid	Load = 50 pF Plus 2 LSTTL Inputs			50	ns
tDCZ	Delay Time from $\overline{CS}$ High to CO TRI-STATE				50	ns
tHCS	Hold Time CCLK Low to $\overline{CS}$ Transition		50			ns
tCSH	Duration of $\overline{CS}$ High		200			ns
tDCI	Delay Time CCLK High to $\overline{INT}$ High-Impedance				50	ns
D PORT IN 16 kHz MODE *(Figure 4)*						
tSDXC	Setup Time, Dx to DCLK		65			ns
tHCDX	Hold Time, DCLK to Dx		0			ns
tDCDR	Delay Time, DCLK to Dr	Load = 50 pF Plus 2 LSTTL Inputs			80	ns

Timing Diagrams



TL/H/9151-28

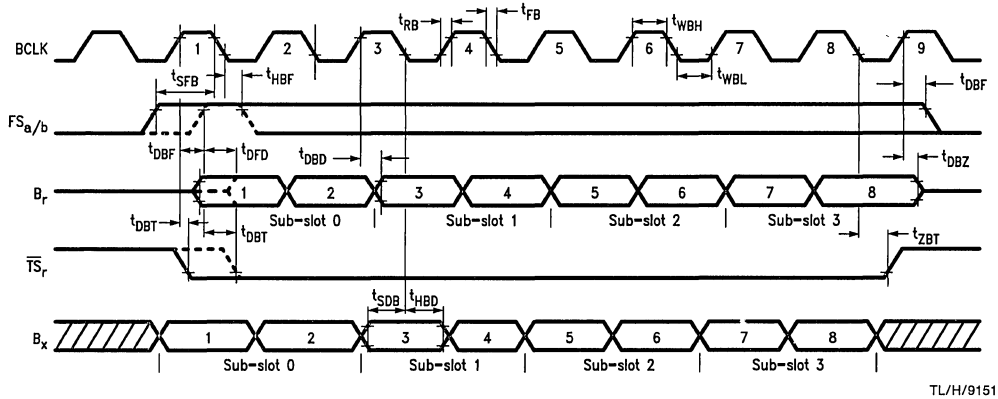


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FIGURE 11. Non-Delayed Data Timing Mode (Formats 1 and 3)

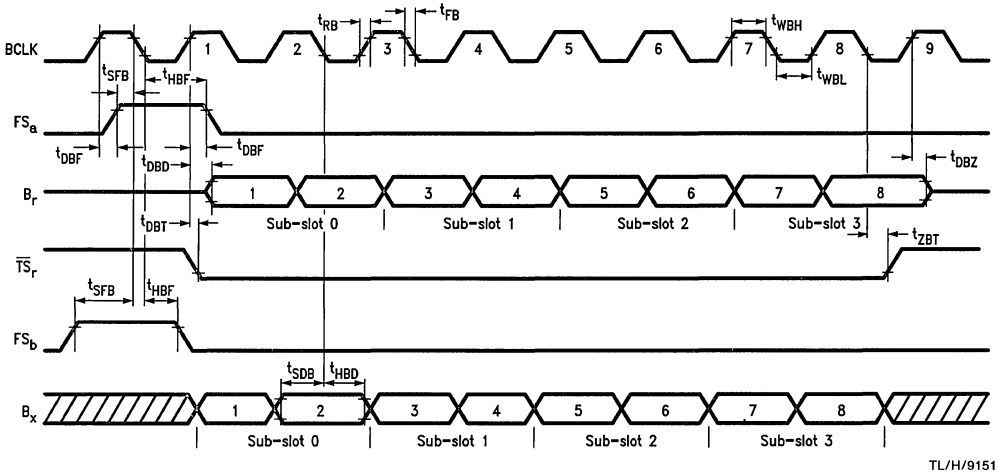

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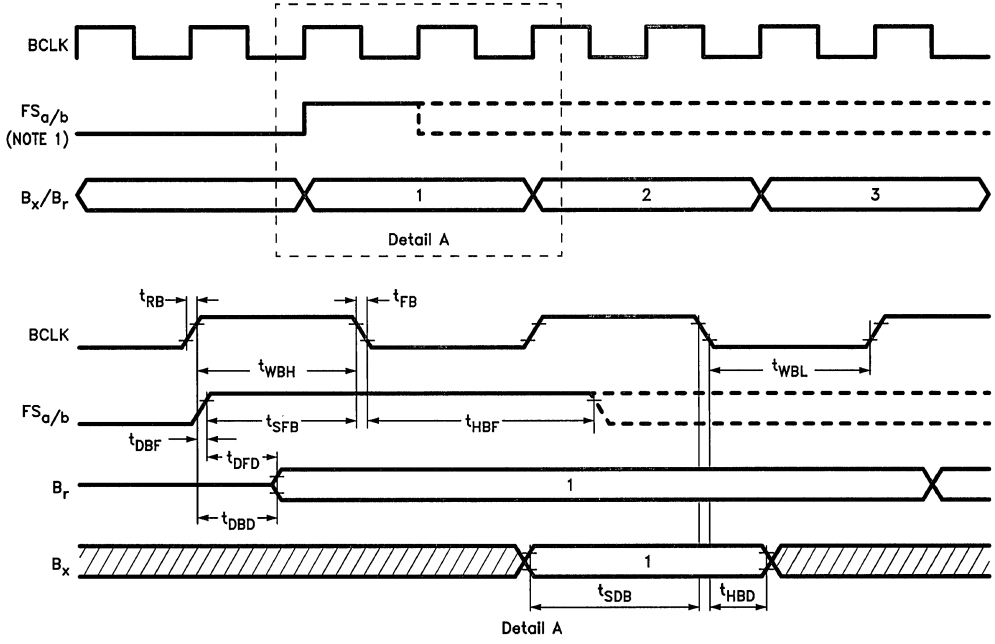
FIGURE 12. Delayed Data Timing Mode (Formats 1, 2 and 3)
(Shown with TS0 Selected)

2

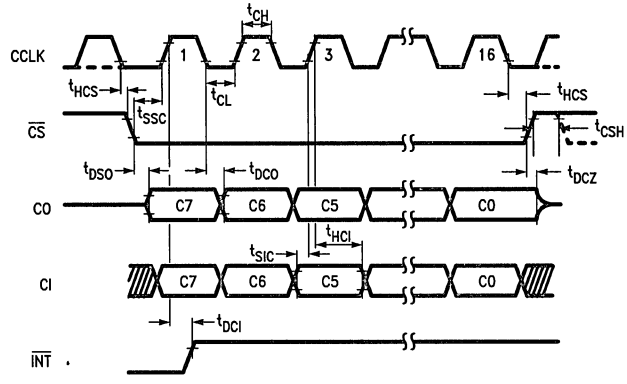
Timing Diagrams (Continued)



TL/H/9151–23

Note 1: As an output (GCI Master) FS_a is high for 8 bit intervals (16 BCLK cycles). As an input (GCI Slave) FS_a must be high for ≥1 BCLK cycle.

FIGURE 13. GCI and Format 4 Timing



TL/H/9151–24

FIGURE 14. Microwire Control Port Timing (MW = 1)

National Semiconductor

PRELIMINARY

TP3420 ISDN S/T Interface Device

General Description

The TP3420 S Interface Device (SID™) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on National's advanced 1.5 micron double-metal CMOS process, and requires only a single +5V supply. All functions specified in CCITT recommendation I.430 and ANSI T1.605-1988 for ISDN basic access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in a TE (Terminal Equipment), in an NT-1 or NT-2 (Network Termination) or as a PABX line-card or trunk-card device.

As specified in I.430, full-duplex transmission at 192 kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. 2 'B' channels, each of 64 kb/s, and 1 'D' channel at 16 kb/s are available for users' data. In addition, the TP3420 provides the 800 b/s "S1" & "Q"multiframe channels for Layer 1 maintenance.

All I.430 wiring configurations are supported by the TP3420 SID, including the "passive bus" for up to 8 TE's distributed within 200 meters of low capacitance cable, and point-to-point and point-to-star connections up to at least 1500 meters (24AWG). Adaptive receive signal processing ensures low bit error rates on any of the standard types of cable pairs commonly found in premise wiring installations when tested with the noise sources specified in I.430.

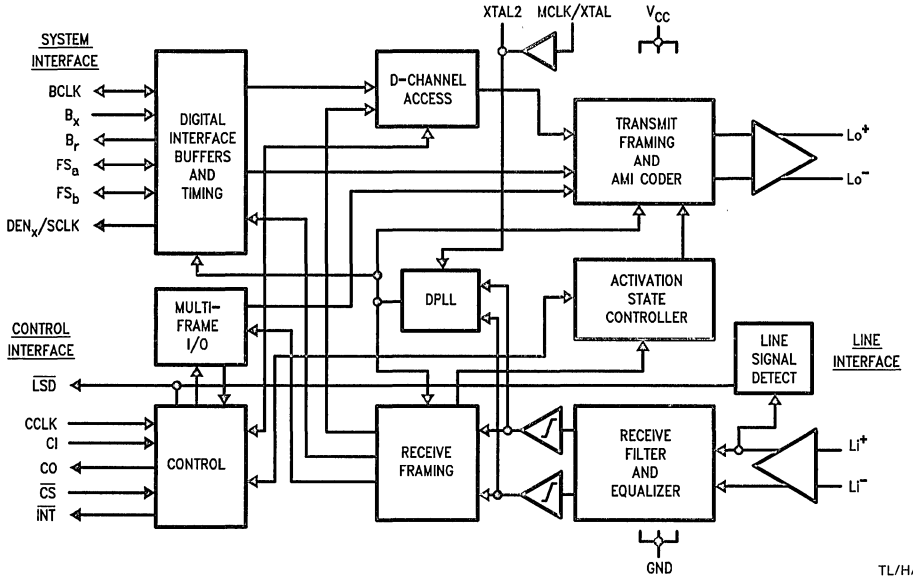
Features

- 2 B + D 4-wire 192 kb/s transceiver
- Selectable TE or NT mode
- Provides all CCITT I.430 layer 1 functions
- Exceeds I.430 range: 1.5 km point-to-point
- Adaptive receiver for high noise immunity
- Adaptive and fixed timing options for NT-1
- Clock resynchronizer and elastic buffers for NT-2/LT
- Slave-slave mode for NT-2 trunks
- S and Q channels with automatic 3x checking
- Selectable system interface formats
- MICROWIRE™ compatible serial control interface
- TP3054/7 Codec/Filter COMBO™ compatibility
- Single +5V supply
- 20-pin package

Applications

- Same Device for NT, TE and PBX Line Card
- Point-to-Point Range Extended to 1.5 km
- Point-to-Multipoint for all I.430 Configurations
- Easy Interface to:
  - LAPD Processor — HPC16400
  - Terminal Adapter — HPC16400
  - Codec/Filter COMBO™ — TP3054/7 and TP3075/6
  - "U" Interface Device — TP3410
  - Line Card Backplanes—No External PLL Needed
- Line Monitor Mode for Test Equipment

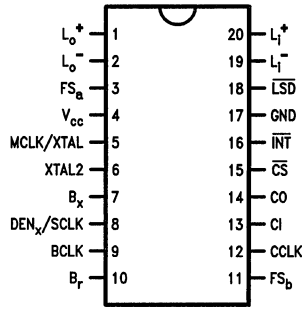
Block Diagram



TL/H/9143–1

Connection Diagrams

TP3420 SID



TL/H/9143–2

Top View

Order Number TP3420J
See NS Package Number J20A or N20A

Pin Descriptions

Name	Description
GND	Negative power supply pin, normally 0V (ground). All analog and digital signals are referenced to this pin.
V_{CC}	Positive power supply input, which must be +5V ±5% relative to GND.
MCLK/XTAL	The 15.36 MHz Master Clock input, which requires either a crystal* to be tied between this pin and XTAL2, or a CMOS logic level clock input from a stable source. When using a crystal, a total of 33 pF load capacitance to GND must also be connected.**
XTAL2	The output of the crystal oscillator, which should be connected to one end of the crystal, and 33 pF of load capacitance to GND.**
BCLK	The Bit Clock pin, which determines the data shift rate for 'B' and 'D' channel data at the digital interface. When NT mode or TES mode is selected, BCLK is a TTL/CMOS input which may be any multiple of 8 kHz from 256 kHz to 4.096 MHz. It need not be synchronous with MCLK. When TEM mode is selected, this pin is a CMOS output at frequency selected by the Digital Interface Format. This clock is phase-locked to the received line signal and is synchronous with the data on B_X and B_r.
FS_a	In NT modes and TES mode, this pin is the Transmit Frame Sync pulse TTL/CMOS input, requiring a positive edge to indicate the start of the active channel time for transmit 'B' and 'D' channel data into B_X. In TEM mode only, this pin is a digital output pulse whose positive indicates the start of the 'B' channel data transfer at both B_X and B_r.
FS_b	In NT modes and TES mode, this pin is the Receive Frame Sync pulse TTL/CMOS input, requiring a positive edge to indicate the start of the active channel time of the device for receive 'B' and 'D' channel data out from B_r. In TEM mode only, when digital interface Format 1 is selected, this pin is an 8 bit wide pulse which indicates the active slot for the B2 channel on the digital interface.
B_X	TTL/CMOS input for 'B' and 'D' channel data to be transmitted to the line; must be synchronous with BCLK.
B_r	CMOS output for 'B' and 'D' channel data received from the line, which is synchronous with BCLK. When not shifting data, this pin is TRI-STATE®.
DEN_X/SCLK	In TEM mode, this pin is a CMOS output which is normally low and pulses high to indicate the active bit-times for 'D' channel Transmit data at the B_X input. It is intended to be gated with BCLK to control the shifting of data from a Layer 2 device to the TP3420 transmit buffer. In NT modes, this pulse occurs in every 8 KHz frame and indicates the location of D channel data input on the B_X pin. In TES mode, this pin is an output synchronized clock (SCLK) at the frequency selected by the Digital Interface Format. This clock is phase-locked to the received line signal, and is intended to be used as the BCLK source.
CI	MICROWIRE control channel serial data TTL/CMOS input.
CO	Control channel serial data CMOS output for status information. When not enabled by $\overline{CS}$, this output is TRI-STATE.
CCLK	TTL/CMOS clock input for the Control Channel.
$\overline{CS}$	Chip Select input which enables the control channel data to be shifted in and out when pulled low. When high, this pin inhibits the Control interface.
$\overline{INT}$	Interrupt output, a latched n-channel open-drain output signal which is normally high impedance, and goes low to indicate a change of status of the loop transmission system.
$\overline{LSD}$	The Line Signal Detect output, an n-channel open-drain output which is normally high-impedance, but pulls low when the device is powered down and a received line signal is detected. It is intended to be used to "wake-up" a microprocessor from a low-power idle mode. This output is high impedance when the device is powered up.
L_o+, L_o-	Transmit AMI signal differential outputs to the line transformer. When used with a 2:1 step-down transformer, the line signal conforms to the output pulse masks in I.430.
L_i+, L_i-	Receive AMI signal differential inputs from the line transformer. The L_i- pin is also the internal voltage reference pin, and must be decoupled to GND with a 10 μf capacitor in parallel with a 0.1 μF ceramic capacitor.

*Crystal specification: 15.36 MHz parallel resonant; $R_s \leq 150\Omega$, C_L = 20 pF and C_O < 7 pF.
**The 33 pF includes any board capacitance.

Functional Description

POWER-ON INITIALIZATION

Following the initial application of power, the TP3420 SID enters the power-down (de-activated) state, in which all the internal circuits including the Master oscillator are inactive and in a low power state except for the Line-Signal Detect circuit; the line outputs L_O+/L_O- are in a high impedance state and the Digital System Interface is inactive. All bits in the Control Register power-up as indicated in Table 1. In both NT and TE modes, a Line-Signal Detect circuit monitors the line while the device is powered-down, to enable loop transmission to be initiated from either end.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate-Mark Inversion (AMI) coding with inverted binary is used, as illustrated in *Figure 1*. This coding rule requires that a binary ONE is represented by 0V high impedance output, whereas a binary ZERO is represented by a positive or negative-going 100% duty-cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c.-balanced line signal.

The frame format used in the TP3420 SID follows the CCITT recommendation specified in I.430 and illustrated in *Figure 2*. Each complete frame consists of 48 bits, with a line bit rate of 192 kb/s, giving a frame repetition rate of 4 kHz. A violation of the AMI coding rule is used to indicate a frame boundary, by using a $0+$ bit followed by a $0-$ balance bit to indicate the start of a frame, and forcing the first binary zero following the balance bit to be of the same polarity as the balance bit.

In the Network Termination (NT) to the Terminal Equipment (TE) transmission direction the frame contains an echo channel, the E bit, which is used to retransmit the D bits that are received from the TE. The last bit of this frame is used as a frame balancing bit. In the TE to NT direction, d.c.-balancing is carried out for each channel, as illustrated in *Figure 2*.

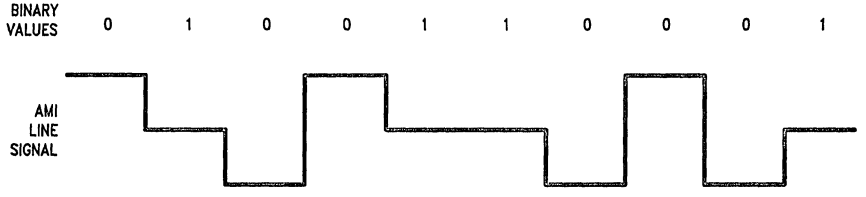
LINE TRANSMIT SECTION

The differential line-driver outputs, L_O+ and L_O-, are designed to drive a transformer with an external termination resistor. A suitable 2:1 transformer, terminated in 50Ω, results in a signal amplitude of nominally 750 mV pk on the line which fully complies with the I.430 pulse mask specifications. When driving a binary 1 symbol the output presents a high impedance in accordance with I.430. When driving a $0+$ or $0-$ symbol a voltage-limited current source is turned on. Short-circuit protection is included in the output stage; over-voltage protection is required externally, see the Applications section.

LINE RECEIVE SECTION

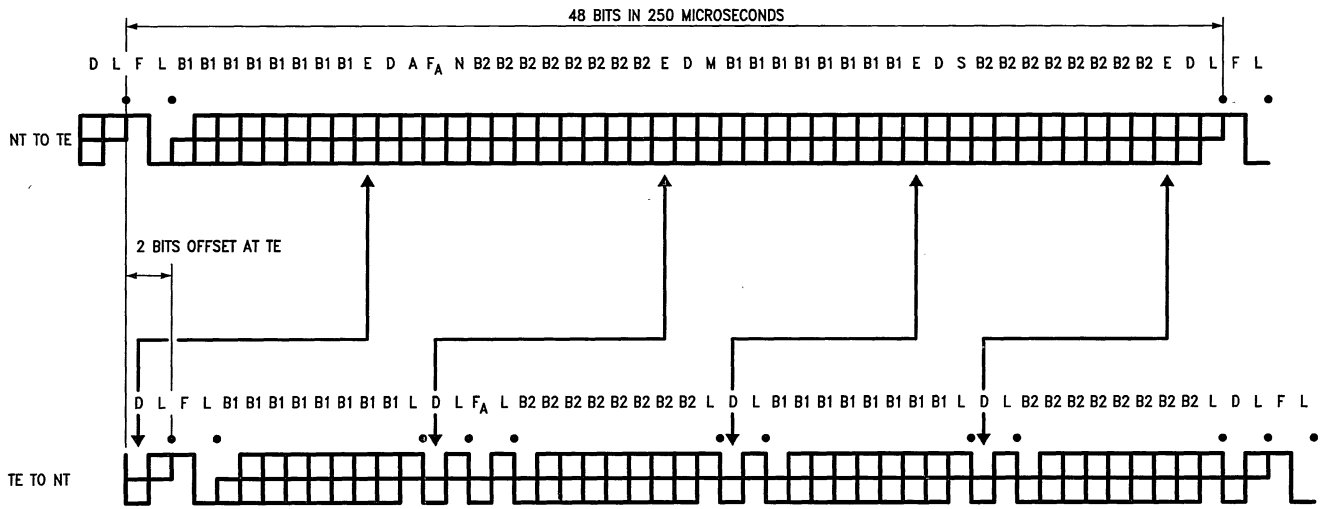
The receive input signal should be derived via a 1:1 transformer, or a 1:2 transformer of the same type used for the transmit direction. At the front-end of the receive section is a continuous filter which limits the noise bandwidth. To correct pulse attenuation and distortion caused by the transmission line in point-to-point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics. This equalizer is always enabled when either TE mode or NT Mode Adaptive Sampling is selected, but is disabled for short passive bus applications when NT Mode Fixed Sampling is selected. An adaptive threshold circuit maximizes the Signal-to-Noise ratio in the eye at the detector for all loop conditions.

A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols.



TL/H/9143–4

FIGURE 1. Inverted AMI Line-Coding Rule



TL/H/9143–5

Legend:

F = **Framing bit**
L = **DC Balancing bit**
D = **D-channel bit**
E = **D-echo-channel bit**
F_A = **Auxiliary framing bit or Q Channel bit**
M = **Multiframe Sync bit**
N = **bit set to a binary value N = $\overline{F_A}$**
B1 = **bit within B-channel 1**
B2 = **bit within B-channel 2**
A = **bit used for activation**
S = **S Channel bit**

• Dots mark the boundaries of those parts of the frame that are independently DC-balanced

FIGURE 2. Frame Format

Functional Description (Continued)

The MCLK input provides the reference clock for the DPLL at 15.36 MHz. Clocks for the digital interface timing may either be derived from this recovered clock, as in TE mode Digital System Interface Master, or may be slaved to an external source, as in the T-interface side of an NT-2 (TES mode). In TES and NT modes, re-timing circuitry on the TP3420 allows the MCLK frequency to be plesiochronous (i.e., free-running) with respect to the network clock, i.e. the 8 kHz FS_a input. With a tolerance on the MCLK oscillator of 15.36 MHz ±100 ppm, the lock-in range of the DPLL allows the network clock frequency to deviate up to ±50 ppm from nominal.

When the device is powered-down (either on initial powering-on of the device or after using a PDN command), a Line-Signal Detect circuit is enabled to detect the presence of incoming data if the far-end starts to activate the loop. The LSD circuit is disabled by a Power-Up (PUP) command.

DIGITAL SYSTEM INTERFACE

The Digital System Interface (DSI) on the TP3420 combines 'B' and 'D' channel data onto common pins to provide maximum flexibility with minimum pin count. Several multiplexed formats of the B and D channel data are available as shown in *Figure 3*. Selection is made via the Control Register.

At this interface, phase skew between transmit and receive frames may be accommodated when the device is a slave at the Digital Interface (NT and TES Modes) since separate frame sync inputs (Figure 3a), FS_a and FS_b, are provided. Each of these synchronizes a counter which gates the transfer of B1 and B2 channels in consecutive time-slots across the digital interface. The serial shift rate is determined by the BCLK input, and may be any multiple of 8 kHz from 256 kHz to 4.096 MHz. Thus, for applications on a PABX line-card (in NT mode), the 'B' and 'D' channel slots can be interfaced to a TDM bus and assigned to a time-slot.

In TE Master Mode (TEM), FS_a is an output (Figure 3b) indicating the start of both transmit and receive 'B' channel data transfers. BCLK is also an output at the serial data shift rate, which is dependent on the format selected, see Table IV.

For applications such as the network side of an NT-2, e.g. a PBX trunk card, the TE Slave (TES) Mode is provided. This "slave-slave" mode allows the transmission side of the device to be a slave to the received frame timing, while the Digital System Interface is also in a slave mode i.e. FS_a, FS_b and BCLK are inputs. The Digital System Interface includes elastic buffers which allow any arbitrary phase relationship between each FS input and the received I.430 frame. Also, jitter and low-frequency wander between the frames across the device is absorbed, up to at least 18 μs pk-pk at frequencies below 10 Hz.

TES Mode also provides a synchronized clock output (SCLK) which is phase-locked to the received line signal; SCLK may be used as the BCLK source.

TABLE IV. DSI Format Rates

Format	BLCK as DSI Master (Output)*	BCLK as DSI Slave (Input)
1	2.048 MHz	256 kHz–4.096 MHz
2	256 kHz	256 kHz–4.096 MHz
3	512 kHz	256 kHz–4.096 MHz
4	2.56 MHz	256 kHz–4.096 MHz

***Note:** also SCLK output in TES Mode.

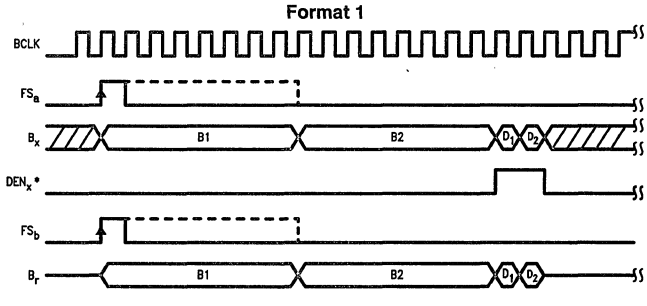
MICROWIRE CONTROL INTERFACE

A serial interface, which can be clocked independently from the 'B' and 'D' channel system interface, is provided for microprocessor control of various functions in the TP3420. This port can be used when the device is powered up or powered down. All data transfers consist of a single byte shifted into the Control Register via the CI pin, simultaneous with a single byte shifted out from the Status Register via the CO pin.

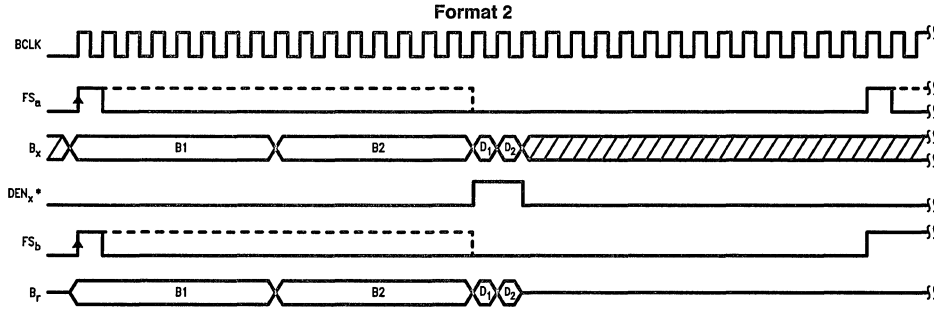
Data shifts in to CI on rising edges of CCLK and out from CO on falling edges when $\overline{CS}$ is pulled low for 8 cycles of CCLK. An Interrupt output, $\overline{INT}$ goes low to alert the microprocessor whenever a change occurs in one or more of the conditions indicated in the Status Register. This latched output is cleared to a high impedance state by the first rising CCLK edge after $\overline{CS}$ goes low. Interrupt Source(s) occurring while another is still pending are stored in a stack and read in sequence, by causing another interrupt at the end of the current $\overline{CS}$ cycle ($\overline{INT}$ can go low only when $\overline{CS}$ is high). When reading the Status Register the CI input is also enabled, therefore a "dummy" command e.g. NOP(X'FF) must be loaded into CI as CO is read.

Figure 4 shows the timing for this interface, and Tables I and II list the control functions and status indicators.

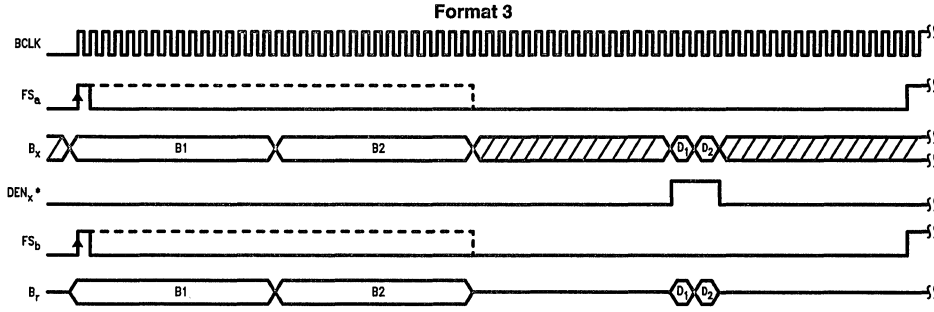
Functional Description (Continued)



TL/H/9143–10



TL/H/9143–13



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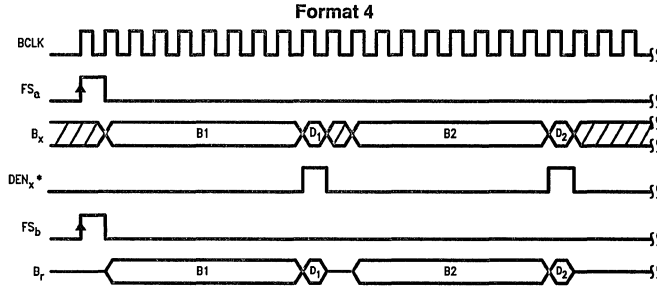

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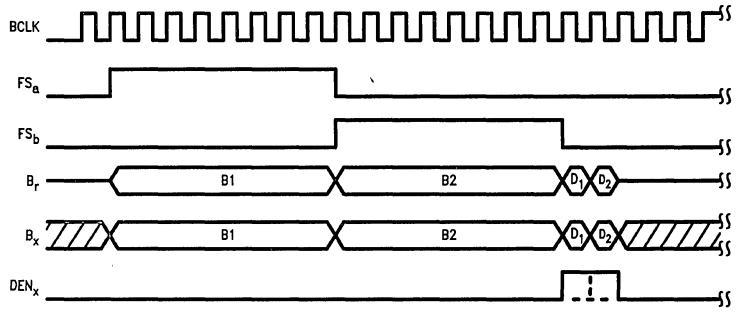
FIGURE 3a. Digital System Interface Formats in NT and TES* modes (DSI Slave)

Note: *In TES mode, DENx outputs SCLK synchronized to the S interface. Format 1, SCLK = 2.048 MHz, Format 2, SCLK = 256 kHz, Format 3, SCLK = 512 kHz, Format 4, SCLK = 2.56 MHz.

Functional Description (Continued)

Format 1



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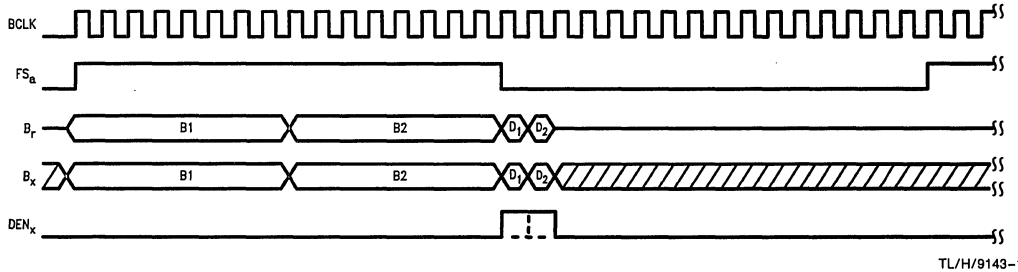
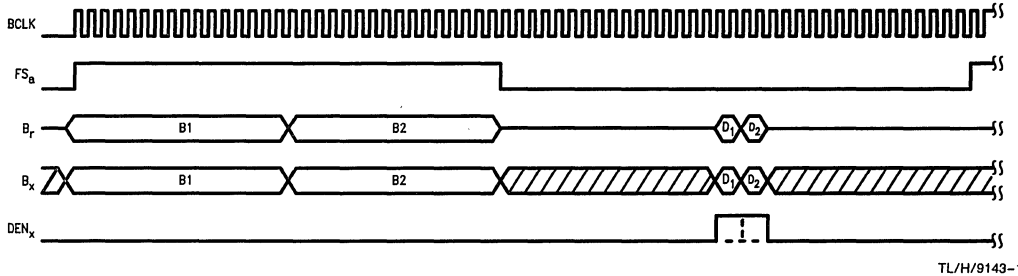
Format 2



TL/H/9143–15

Format 3



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Format 4

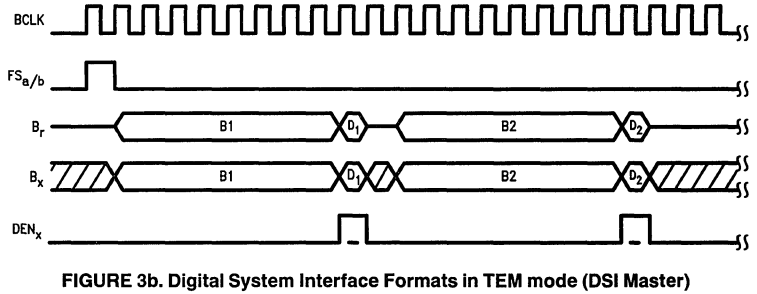

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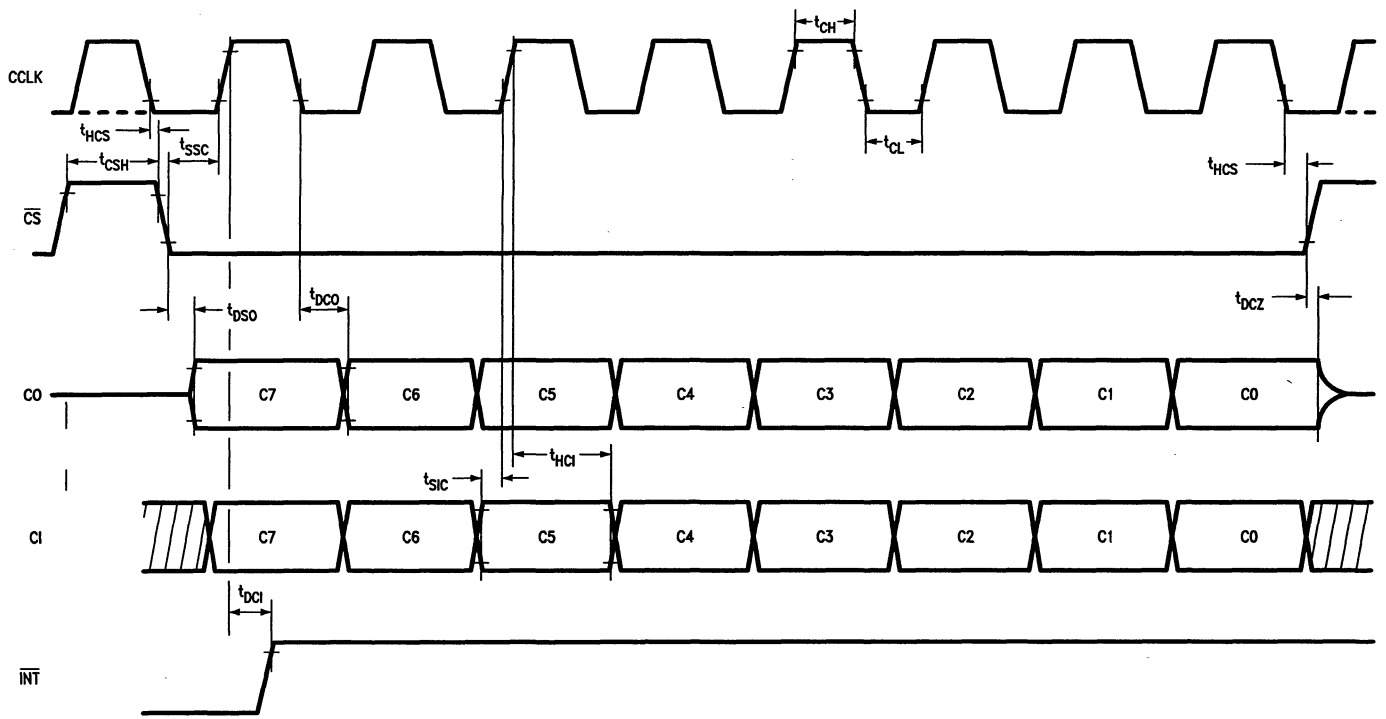
FIGURE 3b. Digital System Interface Formats in TEM mode (DSI Master)



TL/H/9143–7

FIGURE 4. MICROWIRE Control Interface Timing

Functional Description (Continued)

TABLE I. Control Register Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Activation/Deactivation									
No Operation	NOP	1	1	1	1	1	1	1	1
*Power-Down	PDN	0	0	0	0	0	0	0	0
Power-Up	PUP	0	0	1	0	0	0	0	0
Deactivation Request	DR	0	0	0	0	0	0	0	1
Force INFO2 (NT only)	FI2	0	0	0	0	0	0	1	0
Monitor Mode Activation	MMA	0	0	0	1	1	1	1	1
Activation Request	AR	0	0	0	0	0	0	1	1
Device Modes									
*NT Mode, Adaptive Sampling	NTA	0	0	0	0	0	1	0	0
NT Mode, Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Mode, Digital System Interface Slave (Note 1)	TES	0	0	0	0	0	1	1	0
TE Mode, Digital System Interface Master	TEM	0	0	0	0	0	1	1	1
Digital Interface Formats									
*Digital System Interface Format 1	DIF1	0	0	0	0	1	0	0	0
Digital System Interface Format 2	DIF2	0	0	0	0	1	0	0	1
Digital System Interface Format 3	DIF3	0	0	0	0	1	0	1	0
Digital System Interface Format 4	DIF4	0	0	0	0	1	0	1	1
B Channel Exchange									
*B Channels Mapped Direct, B1 to B1, B2 to B2	BDIR	0	0	0	0	1	1	0	0
B Channels Exchanged, B1 to B2, B2 to B1	BEX	0	0	0	0	1	1	0	1
D Channel Access									
D Channel Request, Class 1 Message	DREQ1	0	0	0	0	1	1	1	0
D Channel Request, Class 2 Message	DREQ2	0	0	0	0	1	1	1	1
End of Message Interrupt									
*EOM Interrupt Enabled	EIE	0	0	0	1	0	0	0	0
EOM Interrupt Disabled	EID	0	0	0	1	0	0	0	1
Multiframe Circuit and Interrupt									
Multiframe Circuit and Interrupt Enabled	MIE	0	0	0	1	0	0	1	0
*Multiframe Circuit and Interrupt Disabled	MID	0	0	0	1	0	0	1	1
Multiframe Receive Message 3X Checking									
*Enable 3X Checking	EN3X	0	0	1	0	1	0	0	0
Disable 3X Checking	DIS3X	0	0	1	0	1	0	0	1
Multiframe Transmit Register									
Write to Multiframe Transmit Register	MFT	0	0	1	1	M1	M2	M3	M4
B1 Channel Enable/Disable									
B1 Channel Enabled	B1E	0	0	0	1	0	1	0	0
*B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enable/Disable									
B2 Channel Enabled	B2E	0	0	0	1	0	1	1	0
*B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1

*** Indicates initial state following Power-on Initialization.**

Note 1: Slave-slave mode.

Functional Description (Continued)

TABLE I. Control Register Functions (Continued)

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Loopback Test Modes									
Loopback B1 Towards Line Interface	LBL1	0	0	0	1	1	0	0	0
Loopback B2 Towards Line Interface	LBL2	0	0	0	1	1	0	0	1
Loopback 2B + D Towards Digital Interface	LBS	0	0	0	1	1	0	1	0
Loopback B1 Towards Digital Interface	LBB1	0	0	0	1	1	1	0	0
Loopback B2 Towards Digital Interface	LBB2	0	0	0	1	1	1	0	1
*Clear All Loopbacks	CAL	0	0	0	1	1	0	1	1

*Indicates initial state following power-on.

TABLE II. Status Register Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
No Change	NOC	0	0	0	0	0	0	0	0
Line Signal Detected from Far-End	LSD	0	0	0	0	0	0	1	0
Activation Pending	AP	0	0	0	0	0	0	1	1
End of Message	EOM	0	0	0	0	0	1	1	0
Lost Contention	CON	0	0	0	0	0	1	1	1
Multiframe Receive Buffer Requires Service	MFR	0	0	1	1	M1	M2	M3	M4
Activation Indication	AI	0	0	0	0	1	1	0	0
Error Indication	EI	0	0	0	0	1	1	1	0
Deactivation Indication	DI	0	0	0	0	1	1	1	1

STATUS INDICATOR DESCRIPTIONS

LSD This interrupt indicates that the far-end of the line is attempting to Activate the interface. May be used as an alternative to the $\overline{\text{LSD}}$ pin to "wake-up" a microprocessor.

AP If set, indicates that either INFO 1 frames have been identified in an NT receiver, or INFO 2 or INFO 4 frames have been identified in a TE receiver. Requires an AR control instruction to allow Activation to be completed.

EOM This interrupt occurs when the closing flag of a D-channel message has been transmitted by a TE on the S interface, indicating successful completion of a packet. The Interrupt associated with this bit can be disabled via the Control Register if desired.

CON This interrupt occurs when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit, indicating a lost collision.

MFR This interrupt indicates when the Multiframe receive data buffer requires servicing, see Multiframe Maintenance Section. All Multiframing functions can be disabled via an MID Command if desired.

AI This interrupt indicates that the interface has been successfully Activated in response to an Activation Request.

EI Set when loss of frame alignment is detected.

DI If set, indicates that the interface has been Deactivated.

CONTROL REGISTER INSTRUCTIONS ACTIVATION/DEACTIVATION

PUP This power-up command enables all analog circuitry, starts the XTAL and resets the state machines to the de-activated state, i.e. transmitting INFO 0 (no signal). It also inhibits the LSD output.

PDN This power-down command immediately forces the device to a low power state, without sequencing through any of the de-activation states. It should therefore only be used after the TP3420 has been put in a known state, e.g. in a TE after a DI status indication has been reported. It also enables the LSD circuit.

AR Activation Request initiates the specified Activation sequence. It is recommended that an AR be delayed at least 2 ms after the device is powered-up using the PUP command.

DR Deactivation Request, which forces the device through the appropriate deactivation sequence specified in I.430. Should be used at the NT end only.

FI2 Effective only in NT modes, and only after Activation has been completed, this instruction forces the NT to transmit INFO 2 frames instead of INFO 4, normally to allow testing at the U interface. Provided INFO 3 is still being received from the TE(s), an AP Status Interrupt will be generated and loop synchronization maintained, but 2B + D transmission is inhibited. To restore full loop activation, with the NT sending INFO 4, an AR command is required in the normal way.

Functional Description (Continued)

MMA Intended for test equipment applications, this instruction allows the receive line interface (Li±) to be connected to the TE-to-NT direction twisted pair and to activate on the received INFO 3 signals while being the master of the DSI. The received 2B+D can then be passively monitored (the line transmit output Lo± would not be connected). TE Master mode must be selected first (TEM).

DEVICE MODES

NTA NT Mode, Adaptive Sampling should be selected when the device is in an NT on any wiring configuration up to the maximum specified length for operation. Multiple terminals, if required, must be grouped within approximately 100 meters of each other (depending on cable capacitance, see I.430). The Digital System Interface is a slave to external BCLK and FS sources.

NTF NT Mode Fixed Sampling may be selected when the device is in an NT on a passive bus wiring configuration up to approximately 200 meters in length (depending on cable type). In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed, to enable multiple terminals (nominally up to 8) to be connected anywhere along the passive bus. Again, the DSI is a slave to external BCLK and FS sources.

TEM TE Mode DSI Master should be selected when the device is in a TE. The TP3420 is then the source of the BCLK and FS signals, and access to the Transmit D channel, including the priority and contention resolution control, is enabled as described in the section on TE Mode D-Channel Access.

TES TE Mode DSI Slave, otherwise known as "Slave-slave" mode, should be selected when the device is used on the T-interface side of an NT-2. The TP3420 System Interface is then driven by BCLK and FS sources in the NT-2. Data buffers and a clock re-synchronizer enable this interface to function with jittering sources for BCLK and FS. All D Channel access control circuitry is disabled, i.e. D Channel data at the Bx input is continuously transmitted to the line; there is no monitoring of the D-echo channel from the network direction, and DREQ instructions are ignored. Also, the SCLK function is enabled at the DEN_X/SCLK pin.

DIGITAL INTERFACE FORMATS

DIF1) DIF2) DIF3) DIF4) These instructions select the format of the Digital Interface timing, see *Figures 3a* and *3b*.

B CHANNEL CONTROL

BDIR) BEX) These commands provide for the exchange of data between the B1 and B2 channels as it passes through the device, (Note 1).

Note 1: When enabling a B channel in conjunction with the BEX Command, the channels are referenced at the Digital System Interface, not the line interface e.g. to connect the B1 slot on the DSI with the B2 slot on the line interface, use the BEX and B1E commands.

B1E) B1D) B2E) B2D) When either or both B channels are disabled, binary 1s are transmitted on the line in those B channel bit positions, regardless of data at the Bx input, and the Br output is TRI-STATE in those bit positions.

D CHANNEL ACCESS

DREQ1) DREQ2) This is a request from Layer 2 to the TP3420 in a TE (in Mode TEM only) to attempt to access the transmit D channel at the S interface. Use DREQ1 to select the access priority for a Class 1 message, or DREQ2 for a Class 2 message.

LOOPBACK TEST MODES

Three classes of loopback mode are available on the SID, selected by writing the appropriate Control instruction.

LBS This loopback at the system interface is a full loopback of the 2B+D channels from the B_X input to the B_r output. It may be set when the device is either activated, in which case it is transparent (i.e. the composite signal is also transmitted to the line), or when it is deactivated.

LBL1/2 These loopbacks turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.

LBB1/2 These loopbacks at the Digital System Interface loop the B1 (LBB1) or the B2 (LBB2) channel data from the B_X input to the B_r output. The B_X input data is also sent to the line transmit output.

EXTERNAL SELF-ACTIVATING LOOPBACK

A quick self-test of the device is possible by connecting together the line sides of the transmit and receive transformers. NTA or NTF mode must be selected, and the device can then be activated by the normal command sequence (Note 2).

Note 2: This test mode is not possible by direct connection of L_o± and L_i± pins due to incompatible internal bias voltages.

MULTIFRAME TRANSMIT REGISTER

MFT MIE MID With the device in TE Mode, data entered in bit positions M1, M2, M3 and M4 is transmitted towards the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT Mode, data entered in the M bit positions is transmitted towards the TE in multiframe bit positions S11, S12, S13 and S14 respectively. The Multiframe Channel and Interrupt must be enabled by an MIE command to use these channels; an MID command will disable them, (see Multiframe Maintenance Channel section).

MULTRIFRAME MESSAGE CHECKING

EN3X DIS3X EN3X enables the checking of certain S and Q channel messages before generating the MFR interrupt. DIS3X disables this circuit, so that the MFR interrupt is generated once per multiframe with the new S or Q word (see Multiframe Maintenance section).

Functional Description (Continued)

ACTIVATION/DEACTIVATION: TP3420 IN NT MODE

Activation (i.e. transmission and loop synchronization) may be initiated from either end of the loop. To initiate Activation from the NT, the TP3420 must be powered up, using a PUP command, followed (Note 3) by an AR instruction to the Control Register. Network timing, i.e., an 8 kHz input to FS_a, must be present at this time. The device then begins to send data framed as INFO 2 type, in which bits in the B, D and D-echo channels are set to binary 0. These frames are detected by the TE, which replies with data framed as INFO 3 type, synchronized to received frames. A flywheel circuit in the TP3420 NT searches for 3 consecutive correctly formatted receive frames to acquire frame synchronization. If Multiframing is enabled (MIE), 60 correct frames (3 multiframes) are required to achieve full loop synchronization. When it is correctly in sync with received frames, the NT interrupts the control processor with Status Indication type AP. A second AR command is required to cause the NT to send INFO 4 frames, in which the B and D channels are enabled for transmission; Status Indication type AI is then set, and the $\overline{INT}$ output is pulled low to indicate Activation complete.

Note 3: A delay of ≥2 msecs is recommended to ensure that all internal circuits have settled.

When Activation is initiated by a TE, the TP3420 in NT mode will detect the incoming INFO 1 signal and, if it is powered-down will pull the $\overline{LSD}$ pin and $\overline{INT}$ low, either of which can be used to "wake-up" a microprocessor. A PUP command must then be written to power-up the TP3420. Upon identifying the INFO 1 signal, the device will set Status Indication type AP and pull $\overline{INT}$ low to indicate that Activation is pending. No INFO 2 frames will be transmitted until a Control instruction type AR is written to the device, which allows the Activation sequence to proceed as described above.

Once Activated, loss of frame alignment is assumed by the TP3420 when a time which is equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the NT does detect alignment loss it will start to transmit INFO 2. At this point the Error Indication (EI) primitive is set, the $\overline{INT}$ output is pulled low and the receiver searches to identify the incoming signal and attempt to re-acquire loop synchronization. If it successfully re-establishes synchronization with the incoming signal (INFO 3 frames), a further interrupt is generated with Status Indication type AI and re-activation can be completed by sending an AR command. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, Status Indicator EI is set and $\overline{INT}$ pulled low, with the transmitted frames changed to INFO 2. Deactivation can then be completed by a DR command, following which Status Indication type DI is set and the $\overline{INT}$ output pulled low to indicate De-activation.

If required, a PDN instruction may be written to the Control Register to power-down the device and enable the LSD output.

I.430 recommends 2 timers should be available in an NT. An Activation Request to the TP3420 should be associated with the start of an external Timer 1, if required. Timer 1 should be stopped when the AI interrupt is generated following successful Activation. If Timer 1 expires before AI is generated, however, Control Instruction type DR should be written to the device to force de-activation. Timer 2, which is specified to prevent unintentional reactivation, is not required since the TP3420 can uniquely recognise INFO 1 frames.

ACTIVATION/DEACTIVATION: TP3420 IN TE MODE

To activate the loop with the TP3420 at the TE end the device must first be powered-up by a PUP command, followed (Note 3) by a Control Instruction type AR, which is the Activation Request to begin transmission of INFO 1 frames after verifying that INFO 0 is being received from the NT. INFO 1 is a continuous pattern of 0+, 0−, and 6 '1's repeated. At this point the TE is running from its local oscillator and is not receiving any sync information from the NT. When the NT recognises this "wake-up" signal, it begins to transmit INFO 2, synchronized to the network clock (following activation of the "U" interface, if applicable). This enables the phase-locked loop in the TE's receiver to correctly identify bit timing from the NT and to synchronize its own transmission to that of the NT. On identifying INFO 2 for 3 consecutive frames, the TE changes its transmit data to INFO 3 and awaits the return of INFO 4 from the NT. Identification of INFO 4 completes the Activation sequence, so Status Indication type AI is set, and the $\overline{INT}$ output pulled low.

When Activation is initiated by the NT, if the TP3420 in TE mode is powered down, it will pull the $\overline{LSD}$ pin and $\overline{INT}$ low on receiving a line signal. Either of these can be used to "wake-up" a microprocessor. A PUP command is required to enable the device to power-up, identify the received signal, and acquire bit and frame synchronization. Once INFO 2 has been identified, the TP3420 will pull $\overline{INT}$ low, with Status Indication type AP set, to alert the microprocessor that Activation is pending. The microprocessor must respond by writing Control Instruction type AR in order for Activation to proceed. INFO 3 frames are then transmitted. Finally, an AI Status Indication interrupt is generated when the NT replies with INFO 4 frames.

As in NT mode, once Activated, loss of frame alignment is assumed by the TP3420 when a time equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the TE does detect alignment loss it will cease transmitting immediately. At this point the Error Indication (EI) primitive is set in the Status Register, the $\overline{INT}$ output is pulled low and the receiver searches to re-acquire loop synchronization if INFO 2 or INFO 4 frames are still being received. If synchronization is re-established, a further interrupt is generated, with Status Indication type AI. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, the loop is de-activated, Status Indication type DI is set and the $\overline{INT}$ output pulled low to indicate De-activation.

I.430 does not provide for Deactivation to be initiated by a TE. However, a Power-down state may be forced if required, normally after Deactivation has been established by the network.

If required, an external Timer 3 should be started when an Activation Request is sent to the TP3420. The subsequent AI interrupt, indicating Activation is complete, should be used to stop the timer. If the timer expires before an AI is generated, Control Instruction type DR must be written to the device to force the transmission of INFO 0.

Functional Description (Continued)

TE MODE D-CHANNEL ACCESS

In TE mode DSI Master only, the TP3420 SID arbitrates access for Layer 2 Transmit frames to the D-channel bit positions in accordance with the I.430 Priority Mechanism (I.430 Section 6.1). This mechanism is to resolve contention for the D channel towards the network when 2 or more TEs are connected to a Passive Bus. The shifting of D-channel transmit data from the Layer 2 device into the SID buffer is controlled by gating the DEN_X output with BCLK. When no Layer 2 frame is pending, "1"s are always transmitted by the SID in D-bit positions at the S interface. DEN_X output pulses are inhibited and no D-channel data is shifted into the B_X input. An external Layer 2 device requiring to start transmission of a packet should first prime its Transmit buffer such that the opening flag is ready to be shifted across the digital interface. Then a Control instruction, type DREQ, will initiate the D-channel access sequence. DREQ instructions require either that a Priority Class 1 (signalling) packet, or a Priority Class 2 packet, is selected.

In response to the DREQ instruction, the DEN_X output is enabled to pre-fetch the opening flag from the Layer 2 device into the D-channel buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S interface (in a point-to-multipoint wiring configuration) is transmitting in the D-channel. This is assured by counting consecutive "1"s in the E-bit position of frames received from the NT. At least 8 consecutive "1"s must be detected before transmission of the pending D-channel frame begins, in accordance with Table III.

TABLE III. D-Channel Access Criteria

Number of Consecutive "1"s in the E-Channel	D-Channel Access
7	Abort. Possible re-try by the transmitting TE.
8	Signalling packet (Priority Class 1) may begin (Note 1).
9	Signalling packet may begin unconditionally.
10	Any packet type may begin (Priority Class 2) (Note 2).
11	Any packet type may begin unconditionally

Note 1: Only if, since the SID last transmitted a complete Class 1 packet, a sequence of ≥ 9 consecutive "1"s has been detected in the E-channel.

Note 2: Only if, since the SID last transmitted a complete packet of either class, a sequence of ≥ 11 consecutive "1"s has been detected in the E-channel.

If another TE is active in the D-channel, DEN_X pulses are inhibited once the opening flag is in the Transmit buffer, to prevent further fetching of transmit data from the Layer 2 device until D-channel access is achieved. As soon as the required number of consecutive E-channel "1"s has been counted, the leading 0 of the opening flag is transmitted in the next D-bit position towards the NT. DEN_X pulses are also re-enabled in order to shift D-channel bits from the Layer 2 device into the SID transmit buffer. No interrupts are necessary for local flow control between the Layer 2 processor and the TP3420.

During transmission in the D-channel the TP3420 SID continues to compare each E-bit received from the NT with the D-channel bit previously transmitted before proceeding to send the next D-bit. In the event of a mis-match, a contention for the previous D-bit is assumed to have been won by another TE. Transmission of the current packet therefore ceases and "1"s are transmitted in all following D-bit positions. Status Indication type CON is set, and the $\overline{INT}$ output is pulled low to interrupt the Layer 2 transmit processor. DEN_X output pulses are again inhibited.

In order to retransmit the lost packet, the Layer 2 device must begin as before, by priming its Transmit buffer with the packet header and writing a DREQ instruction into the Control Register.

DEN_X pulses stop immediately after receiving the closing flag on the B_X input from the layer 2 device.

Successful completion of a transmit packet is detected by the TP3420 when the closing flag is transmitted in the D channel. '1's are then transmitted in the following D bit positions. The $\overline{INT}$ output is pulled Low (if enabled), with Status Indication type EOM set, to indicate the End of Message. Also, the Priority Access counters are decremented to the lower priority level within each priority class, in accordance with the I.430 algorithm. Priority is subsequently restored to the higher level when the specified number of consecutive 1's (9 or 11) is detected in the D-echo-bit position.

MULTIFRAME MAINTENANCE CHANNELS (S1 AND Q WORDS)

Each direction of transmission across the S interface included a low-speed (800 b/s) channel for loop maintenance, accessed via the control interface of the TP3420. A multiframe structure, consisting of 20 frames on the S interface, is used to synchronize these channels and convey messages coded into 4-bit words, see Table IV. One word is transmitted downstream (NT-to-TE) in the S1 channel, and one word is transmitted upstream (TE-to-NT) in the Q channel every multiframe.

When the device is in NT mode, the MIE command enables both the transmission of the Multiframe identification algorithm (reversal of the FA/N bits every 5th frame and M bit set = 1 every 20th frame) and it enables the MFR interrupt; the algorithm is present during INFO 2 and INFO 4 frames. In TE modes this command only enables the MFR interrupt, since the device will always search for and synchronize to the multiframing identification bits if the NT is sending them. In all modes there is an option to enable or disable a checking circuit to validate received S or Q channel messages. If enabled by the EN3X command, at the end of each multiframe the received 4-bit word is decoded to determine if it should generate an MFR interrupt immediately, or be stored until 3 consecutive multiframes have contained the same 4-bit word before an interrupt is generated. Table IV lists the codes which are 3-times checked. Note, however, that no other action is taken by the TP3420 in response to received codes (e.g. loopbacks are not automatically implemented); the external controller must take the necessary action. This provides the freedom to implement maintenance functions without constraints from the device, and to utilise the unassigned codes for other functions.

TABLE IV
Codes for Q-Channel and S1-Channel Messages with 3X Checking Enabled

Message	NT-to-TE					TE-to-NT				
	Received at TE				Number of Repetitions before MFR $\overline{INT}$	Received at NT				Number of Repetitions before MFR $\overline{INT}$
	S11	S12	S13	S14		Q1	Q2	Q3	Q4	
Idle (NORMAL)	0	0	0	0	3	1	1	1	1	3
Loss-of-Power Indication	1	1	1	1	1	0	0	0	0	1
STP Pass	0	0	1	0	3	—	—	—	—	—
STF Fail	0	0	0	1	3	—	—	—	—	—
ST Request (Note 1)	—	—	—	—	—	0	0	0	1	3
STI Indication	0	1	1	1	3	—	—	—	—	—
DTSE-IN	1	0	0	0	1	—	—	—	—	—
DTSE-OUT	0	1	0	0	1	—	—	—	—	—
DTSE-IN&OUT	1	1	0	0	1	—	—	—	—	—
LB1 Request	—	—	—	—	—	0	1	1	1	3
LB1 Indication	1	1	0	1	3	—	—	—	—	—
LB2 Request	—	—	—	—	—	1	0	1	1	3
LB2 Indication	1	0	1	1	3	—	—	—	—	—
LB1/2 Request (Note 2)	—	—	—	—	—	0	0	1	1	3
LB1/2 Indication	1	0	0	1	3	—	—	—	—	—
Loss-of-Received-Signal Indication	1	0	1	0	3	—	—	—	—	—
Unassigned	All Other Codes				1	All Other Codes				1

Note 1: The code "0001" will be received by an NT1 when ST Request and any other code (except LP) is sent simultaneously by two or more TEs on a Passive Bus.

Note 2: The code "0011" will be received by an NT1 when the LB1 and LB2 requests are transmitted by two different TEs (NT2s) on a Passive Bus.

Functional Description (Continued)

If the 3X checking circuit is disabled by the DIS3X Command, each received S or Q word generates an MFR interrupt once per multiframe.

The MID command disables the transmission of the Multiframe identification algorithm in NT mode and disables the MFR Interrupt in both NT and TE modes. Both the MIE and MID commands can only be written to the device when it is deactivated (either powered-up or powered-down). The Multiframe Transmit Register should also be loaded with the appropriate "Idle" messages, by means of an MFT instruction, prior to activation.

Applications Information

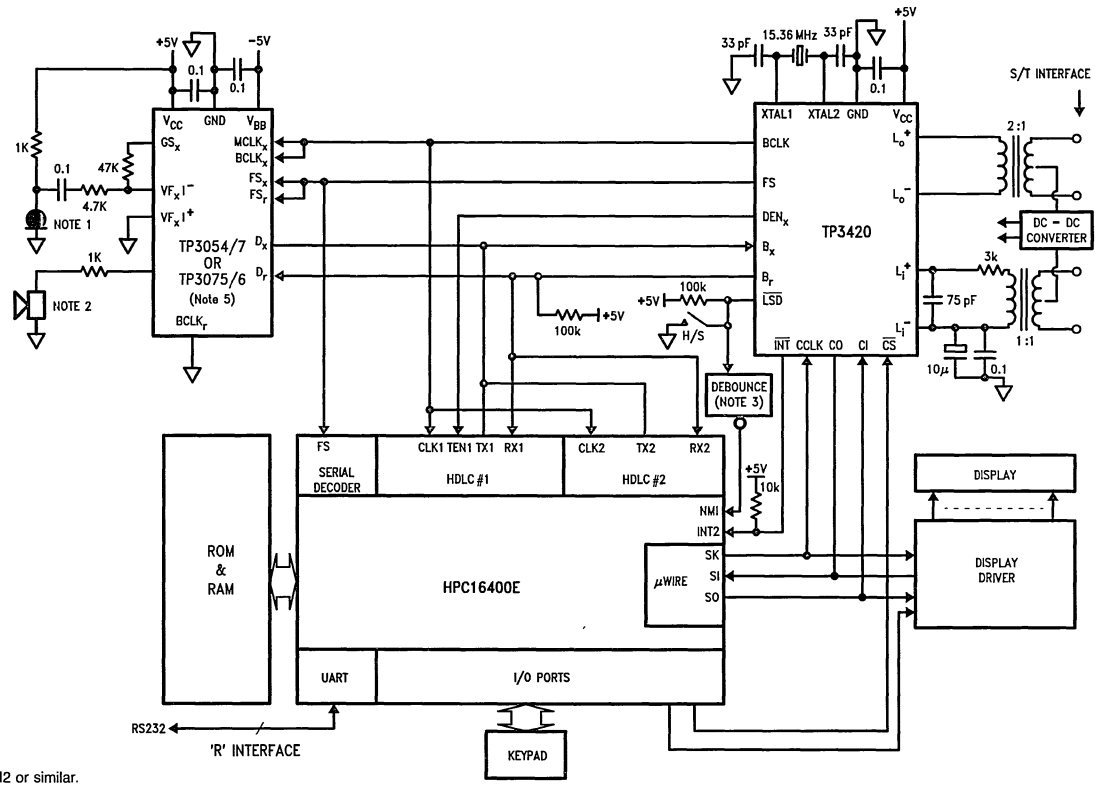
While the pins of the TP3420 SID are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A decoupling capacitor of 0.1 μF should be connected from this common point to V_{CC}. Taking care with the pcb layout in the following ways will help prevent noise injection into the receiver front-end and maximize the transmission performance:

1. keep the crystal oscillator components away from the receiver inputs and use a shielded ground plane around these components.
2. keep the connections between the device and the components on the $L_i\pm$ inputs short; the L_i- capacitors should be connected close to the device pins.
3. keep the connections between the device and the transformers short.

Figure 5 shows a typical application of the TP3420 in an ISDN Terminal.

For more in-depth information on a variety of applications, the TP3420 Users Manual is a comprehensive guide to the hardware and software required to meet the I.430 interface specification. Performance measurements, demonstrating compliance with I.430 and ANSI transmission requirements, are also included.



Note 1: Primotype EM80-PMI2 or similar.

Note 2: Primotype DH31 or similar.

Note 3: Only necessary if a mechanical hook switch is connected to the NMI input of the HPC.

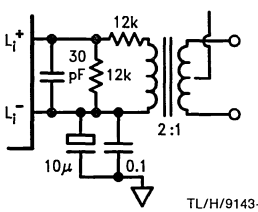
Note 4: See TP3420 User's Manual for Line Interface Protection.

Note 5: The TP3075/6 Programmable Combos also require the MICROWIRE Port to be connected.

FIGURE 5. Typical Application in a TE and/or TA

TL/H/9143–8

Alternative Receive Input Using 2:1 Transformer



TL/H/9143–18

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at L_i, L_0	V_{CC} + 1V to GND − 1V
Voltage at any Digital Input	V_{CC} + 1V to GND − 1V
Storage Temperature Range	−65°C to + 150°C
Current at L_0	± 100 mA
Current at any Digital Output	± 50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics

Unless otherwise noted: limits printed in **bold** characters are electrical testing limits at V_{CC} = 5.0V and T_A = 25°C. All other limits are design goals for V_{CC} = 5.0V ±5%, and T_A = 0°C to 70°C. This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL Input			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL Input	V_{CC} − 0.5			V
V_{OL}	Output Low Voltage	B_r, I_L = 3.2 mA All Other Digital Outputs, I_L = 1 mA			0.4	V
V_{OH}	Output High Voltage	B_r, I_L = −3.2 mA All Other Digital Outputs, I_L = −1 mA All Outputs, I_L = −100 μA	2.4 2.4 V_{CC} − 0.5			V V V
I_I	Input Current	Any Digital Input, GND < V_{IN} < V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE)	B_r, $\overline{INT}$, $\overline{LSD}$, CO GND < V_{OUT} < V_{CC}	−10		10	μA
LINE INTERFACES						
R_{Li}	Differential Input Resistance	GND < L_i+, L_i− < V_{CC}	200			kΩ
CL_{L0}	Load Capacitance	Between L_o+ and L_o−			200	pF
VOS	Differential Output Offset Voltage at L_o+, L_o−	Driving Binary 1s, 220Ω between L_o+ and L_o−	−20		+20	mV
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	All Outputs Open-Circuit		1.0		mA
$I_{CC}1$	Power Up Current	As Above, Device Deactivated (Note 1)		18.0		mA
TRANSMISSION PERFORMANCE						
	Transmit Pulse Amplitude	R_L = 220Ω Between L_o+ and L_o− (Note 2)	±1.55		±1.75	Vpk
	Transmit Pulse Unbalance	0+ Relative to 0−			±5	%
	Input Pulse Amplitude	Differential Between L_i+ and L_i−	±175			mVpk

Note 1: When the device is activated and driving a correctly terminated line, I_{CC1} increases by several mA. A worst-case data pattern, consisting of all binary 0's, increases I_{CC1} by approximately 8 mA.

Note 2: The pulse amplitude at the L_o± pins allows for approximately 1 dB transformer insertion loss to meet the 0.75V pulse mask test when the line is terminated in 50Ω.

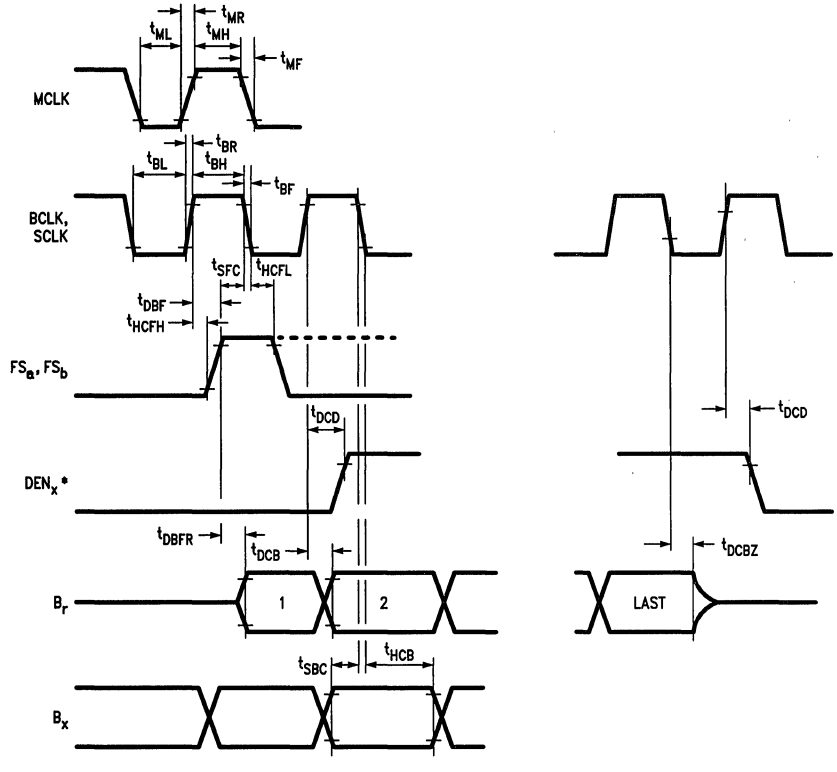
Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
F_{MCK}	Master Clock Frequency Master Clock Tolerance		 −100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
t_{MH}, t_{ML}	Clock Pulse Width Hi & Low for MCLK	$V_{IH} = V_{CC} - 0.5V$ $V_{IL} = 0.5V$	20			ns
t_{MR}, t_{MF}	Rise and Fall Time of MCLK	Used as a Logic Input			10	ns
MICROWIRE CONTROL INTERFACE (see Figure 4)						
t_{CH}	CCLK High Duration		150			ns
t_{CL}	CCLK Low Duration		150			ns
t_{SIC}	Setup Time, CI Valid to CCLK High		50			ns
t_{HCI}	Hold Time, CCLK High to CI Invalid		20			ns
t_{SSC}	Setup Time from $\overline{CS}$ Low to CCLK High		50			ns
t_{DSO}	Delay Time from $\overline{CS}$ Low to CO Valid	Bit C7 only			50	ns
t_{DCO}	Delay Time from CCLK Low to CO Data Valid				50	ns
t_{DCZ}	Delay Time from $\overline{CS}$ High to CO TRI-STATE				60	ns
t_{HCS}	Hold Time CCLK Low to $\overline{CS}$ Transition		0			ns
t_{CSH}	Duration of $\overline{CS}$ High		1			μs
t_{DCI}	Delay Time CCLK1 High to $\overline{INT}$ High-impedance				120	ns
DIGITAL SYSTEM INTERFACE (see Figure 6)						
F_{BCK}	Bit Clock Frequency		256		4096	kHz
t_{BH}, t_{BL}	Clock Pulse Width Hi & Low for BCLK	$V_{IH} = 2.2V$ $V_{IL} = 0.7V$	60			ns
t_{BR}, t_{BF}	Rise and Fall Time of BCLK				15	ns
t_{SBC}	Set up Time, B_X Valid to BCLK Low	All Modes	30			ns
t_{HCB}	Hold Time, BCLK Low to B_X Invalid	All Modes	20			ns

Timing Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL SYSTEM INTERFACE (see Figure 6) (Continued)						
t_{HCFH}	Hold Time, BCLK High to FS_a and FS_b High	NT and TES Modes only	0			ns
t_{SFC}	Set up Time, FS_a to BCLK Low	NT and TES Modes only	50			ns
t_{HCFL}	Hold Time, BCLK Low to FS_a and FS_b Low	NT and TES Modes only	20			ns
t_{DBFR}	Delay Time, FS_b to B_r Valid	NT and TES Modes, Bit 1 only			80	ns
t_{DBF}	Delay Time, BCLK High to FS_a and FS_b Transitions	TEM mode only			50	ns
t_{DCB}	Delay Time, BCLK High to Data Valid	All Modes	20		80	ns
t_{DCBZ}	Delay Time, BCLK Low to Data Invalid	All Modes	50		120	ns
t_{DCD}	Delay Time, BCLK High to DEN_x Transition	TEM Mode only			40	ns

Timing Diagram



TL/H/9143–9

FIGURE 6. Timing Details for Digital System Interface

National Semiconductor

PRELIMINARY

TP3421 ISDN S/T Interface Device with GCI (General Circuit Interface)

General Description

The TP3421 S Interface Device (SID™) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. It is built on National's advanced 1.5 micron M²CMOS process, and requires only a single +5V supply. All functions specified in CCITT recommendation I.430 and ANSI T1.605-1988 for ISDN Basic Access at the 'S' and 'T' interfaces are provided, and the device can be configured to operate either in a TE (Terminal Equipment), in an NT-1 or NT-2 (Network Termination) or as a PABX line-card or trunk-card device.

As specified in I.430, full-duplex transmission at 192 kb/s is provided on separate transmit and receive twisted wire pairs using inverted Alternate Mark Inversion (AMI) line coding. 2 'B' channels, each of 64 kb/s, and 1 'D' channel at 16 kb/s are available for users' data. In addition, the TP3421 provides the 800 b/s "S1" & "Q"multiframe channels for Layer 1 maintenance.

All I.430 wiring configurations are supported by the TP3421 SID, including the "passive bus" for up to 8 TE's distributed within 200 meters of low capacitance cable, and point-to-point and point-to-star connections up to at least 1500 meters (24AWG). Adaptive receive signal processing ensures low bit error rates on any of the standard types of cable commonly found in premise wiring installations when tested with the noise sources specified in I.430.

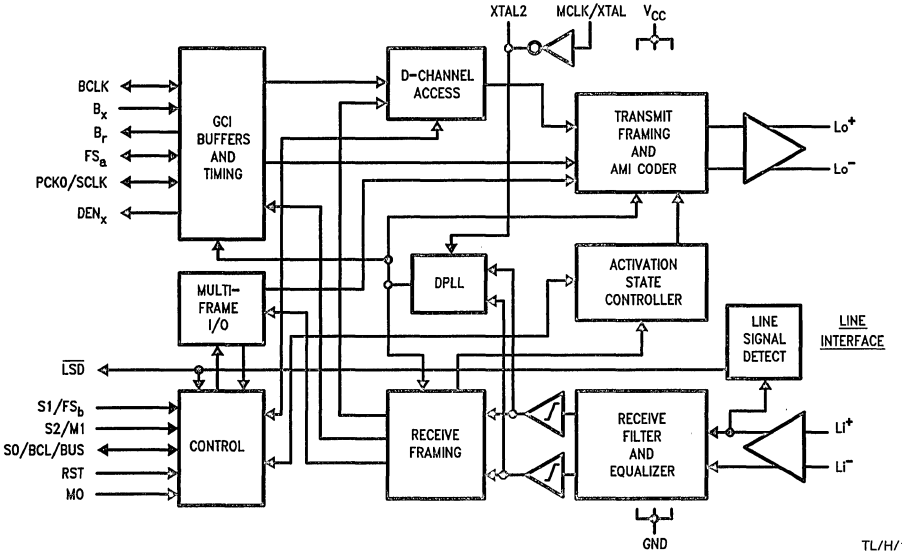
Features

- 2B + D 4-wire 192 kb/s transceiver
- Selectable TE or NT mode
- Provides all CCITT I.430 layer 1 functions
- Exceeds I.430 range: 1.5 km point-to-point
- Adaptive receiver for high noise immunity
- Adaptive and fixed timing options for NT-1
- Clock resynchronizer and elastic buffers for NT-2/LT
- Slave-slave mode for NT-2 trunks
- S and Q channels with automatic 3x checking
- GCI (General Circuit Interface) compatible
- TP3054/7 Codec/filter Combo compatibility
- Single +5V supply
- 20-pin package

Applications

- Same Device for NT, TE and PBX Line Card
- Point-to-Point Range Extended to 1.5 km
- Point-to-Multipoint for all I.430 Configurations
- Line Monitor Mode for Test Equipment

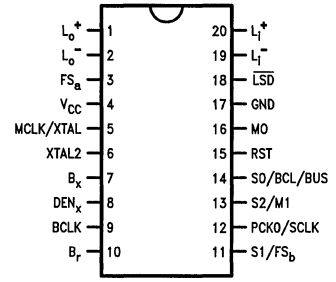
Block Diagram



TL/H/10565–1

Connection Diagrams

TP3421 SID



TL/H/10565–2

Top View

Order Number TP3421J or TP3421N
See NS Package Number J20A or N20A

Pin Descriptions

Note: For definitions of the modes TEM, TES and NT, see the Initialization section.

Name	Description
GND	Negative power supply pin, normally 0V (ground). All analog and digital signals are referenced to this pin.
V_{CC}	Positive power supply input, which must be +5V ±5% relative to GND.
MCLK/XTAL	The 15.36 MHz Master Clock input, which requires either a crystal* to be tied between this pin and XTAL2, or a CMOS logic level clock input from a stable source. When using a crystal, a total of 33 pF load capacitance to GND must also be connected.**
XTAL2	The output of the crystal oscillator, which should be connected to one end of the crystal, and 33 pF of load capacitance to GND.**
BCLK	The Bit Clock pin, which determines the data shift rate for 'B' and 'D' channel data at the GCI. When NT mode or TES mode is selected, BCLK is a TTL/CMOS input which may be any multiple of 8 kHz from 256 kHz to 4.096 MHz. It need not be synchronous with MCLK. When TEM mode is selected, this pin is a CMOS output at 1.536 MHz This clock is phase-locked to the received line signal and is synchronous with the data on B_X and B_r.
FS_a	In NT modes and TES mode, this pin is the GCI Frame Sync pulse TTL/CMOS input, requiring a positive edge to indicate the start of the active channel time for transmit 'B' and 'D' channel data into B_X. In TEM mode only, this pin is a digital output pulse which defines the B1 channel at both B_X and B_r.
B_X	TTL/CMOS input for 'B' and 'D' channel data to be transmitted to the line; must be synchronous with BCLK.
B_r	n-channel output for 'B' and 'D' channel data received from the line which is synchronous with BCLK. When not shifting data, this pin is high-impedance; a pull-up resistor to V_{CC} is required.
DEN_X	In TEM and TES modes, this pin is a CMOS output which is normally low and pulses high to indicate the active bit-times for 'D' channel Transmit data at the B_X input. It is intended to be gated with BCLK to control the shifting of D-channel data from a Layer 2 device to the TP3421 transmit buffer. In NT modes, this pulse occurs in every 8 KHz frame and indicates the location of D channel data input on the B_X pin.
RST	The Reset pin, which must be pulled low at power-on Reset and for normal operation. A high-going pulse on this pin will reset the device in a configuration determined by the Configuration pins.
PCKO/SCLK	In TEM and NT modes this is PCKO, which is a 32 kHz clock output synchronized to the GCI clocks; it is provided for synchronization of a switching regulator in line-powered equipment. In TES mode this is the SCLK output, which is a 1.536 MHz clock locked to the received line signal and intended to be used as the BCLK source. When used on a multi-channel line card, this output may be commoned with the SCLK outputs of other transceivers. A detector circuit ensures that this pin will stay high-impedance to prevent conflict if any other device is driving the SCLK.
$\overline{LSD}$	The Line Signal Detect output, an n-channel open-drain output which is normally high-impedance, but pulls low when the device is powered down and a received line signal is detected. It is intended to be used to "wake-up" a microprocessor from a low-power idle mode. This output is high impedance when the device is powered up.
L_o+, L_o-	Transmit AMI signal differential outputs to the line transformer. When used with a 2:1 step-down transformer, the line signal conforms to the output pulse masks in I.430.
L_i+, L_i-	Receive AMI signal differential inputs from the line transformer. The L_i- pin is also the internal voltage reference pin, and must be decoupled to GND with a 10 μF capacitor in parallel with a 0.1 μF ceramic capacitor.

*Crystal specification: 15.36 MHz parallel resonant; $R_S \leq 150\Omega$, C_L = 20 pF and C_O < 7 pF.
**The 33 pF includes any board capacitance.

Pin Descriptions (Continued)

CONFIGURATION PINS

M0 GCI Mode Selection input pin. To select GCI channel 0 connect M0=0; pin M1 must be used to select TEM or NT1 Mode. To select GCI multiplexed mode connect M0=1; the GCI channel is then selected by pins S0, S1 and S2, and the Control Register must be used to select TE or NT mode.

S0/BCL/BUS The function of this pin is dependent on the device mode selected via the MO pin and the Control Register, as follows:

- S0: in NT modes, and if M0=1, this is the S0 input pin for the lsb of the 3 pin GCI channel selection.
- BUS: in NT modes, and if M0=0, this pin is the the BUS select input pin for use in NT−1 applications: when BUS=0 fixed timing recovery is selected for use on passive bus wiring, and when BUS=1 adaptive timing recovery is selected for use on point-to-point and extended passive bus wiring.
- BCL: In TEM mode only, this pin is an output BCLK at 768 kHz. It is used as the $BCLK_X$ input to the TP3054/7 or TP3075/6 Codec/filter Combos, which clock data at a rate of 1 bit per BCLK cycle.

S1/FS_b

- S1: if M0=1 only (GCI multiplexed mode), this is an input pin for the GCI channel selection.
- FS_b: if M0=0 and M1=0 (TEM mode), this is a Frame Sync output pulse which indicates the active slot for the B2 channel on the GCI.

S2/M1

- S2: if M0=1 only, (GCI multiplexed mode), this is an input pin for the msb of the GCI channel selection.
- M1: if M0=0 this pin is the selection for TE Master or NT1 mode as follows: M1=0 selects TEM mode; M1=1 selects NT1 mode (see also BUS input).

Functional Description

INITIALIZATION

The TP3421 SID device can be operated at either end of an S Interface loop. At the upstream end the mode is called "NT" mode, in which the device is the source of INFO2 and INFO4 frames; choose this mode for PBX (NT2) line cards and NT1 equipment. A selection of adaptive or fixed receiver timing (NTA or NTF mode) must also be made, see Device Modes section.

At the downstream end of the loop the mode is called "TE" mode, in which the device is the source of INFO1 and INFO3 frames; choose this mode for terminal equipment and NT2 trunk side interfaces. Furthermore the digital interface may be configured to be either the master of the timing on the BCLK and FS pins (TE Master mode) or a slave to timing from another device (TE Slave mode). Configuring the TP3421 SID into the required operating modes is accomplished by polarization of pins, as shown in Table I; for TE Slave mode and applications in an NT2/LT the appropriate command must also be written via the GCI Monitor channel prior to the Power-Up command.

TE Master mode is selected solely by appropriate strapping of pins M0 and M1. The device is then powered up by pulling the B_X data input pin low momentarily, thereby starting the GCI clocks needed for transfer of additional control data.

When the NT1 configuration is selected, the device is powered up directly by receiving GCI clocks on BCLK and FS_a inputs (normally by the U transceiver).

When NT2 or TE Slave (TES) mode is selected, the device must first be correctly configured by writing the appropriate command via the GCI Monitor Channel, and then writing the PUP command on the C/I channel.

TABLE I. Mode Selection and Power-Up Control

	Device Mode			
Pin Name	**TE Master**	**TE Slave**	**NT1**	**LT/NT2**
M0	i = 0	i = 1	i = 0	i = 1
S2/M1	i = M1 = 0	i = S2	i = M1 = 1	i = S2
S1/FS_b	o = FS_b	i = S1	Not Used	i = S1
S0/BCL/BUS	o = BCL = 768 kHz	i = S0	i = BUS =0 for NTF =1 for NTA	i = S0
Mode Command	—	TES	—	NTA/NTF
Power-Up	Pull B_X Low	PUP Command	Send BCLK	PUP Command

Note: *i means input, o means output.*

Functional Description (Continued)

POWER-DOWN

Power-down is normally invoked by the PDN command in the GCI C/I Channel. Additionally, in TES, NT1 and NT2 modes, loss of GCI clocks (BCLK and/or FS_a) automatically forces power-down, and in TES, TEM and LT/NT2 modes the DI command is received in the C/I channel after the S-interface is deactivated.

In the power-down state the device retains its programmed modes, which may be changed if required via the GCI Monitor Channel. The Line Signal Detector circuit is enabled, allowing the $\overline{LSD}$ output to pull low if a wake-up signal is detected from the far-end. All other circuits are inactive, including the oscillator, and the L_O+/L_O- outputs are high-impedance. Upon power-up, all analog and I.430 circuits are enabled, the crystal oscillator starts and the activation state machine is reset. The $\overline{LSD}$ output is also disabled.

LINE CODING AND FRAME FORMAT

For both directions of transmission, Alternate-Mark Inversion (AMI) coding with inverted binary is used, as illustrated in *Figure 1*. This coding rule requires that a binary ONE is represented by 0V high impedance output, whereas a binary ZERO is represented by a positive or negative-going 100% duty-cycle pulse. Normally, binary ZEROs alternate in polarity to maintain a d.c.-balanced line signal.

The frame format used in the TP3421 SID follows the CCITT recommendation specified in I.430 and illustrated in *Figure 2*. Each complete frame consists of 48 bits, with a line bit rate of 192 kb/s, giving a frame repetition rate of 4 kHz. A violation of the AMI coding rule is used to indicate a frame boundary, by using a $0+$ bit followed by a $0-$ balance bit to indicate the start of a frame, and forcing the first binary zero following the balance bit to be of the same polarity as the balance bit.

In the Network Termination (NT) to the Terminal Equipment (TE) transmission direction the frame contains an echo channel, the E bit, which is used to retransmit the D bits that are received from the TE. The last bit of this frame is used as a frame balancing bit. In the TE to NT direction, d.c.-balancing is carried out for each channel, as illustrated in *Figure 2*.

LINE TRANSMIT SECTION

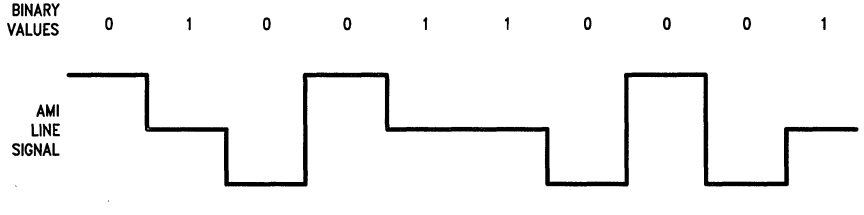
The differential line-driver outputs, L_O+ and L_O-, are designed to drive a transformer with an external termination resistor. A suitable 2:1 transformer, terminated in 50Ω, results in a signal amplitude of nominally 750 mV pk on the line which fully complies with the I.430 pulse mask specifications. When driving a binary 1 symbol the output presents a high impedance in accordance with I.430. When driving a $0+$ or $0-$ symbol a voltage-limited current source is turned on. Short-circuit protection is included in the output stage; over-voltage protection is required externally, see the Applications section.

LINE RECEIVE SECTION

The receive input signal should be derived via a 1:1 transformer, or a 1:2 transformer of the same type used for the transmit direction. At the front-end of the receive section is a continuous filter which limits the noise bandwidth. To correct pulse attenuation and distortion caused by the transmission line in point-to-point and extended passive bus applications, an adaptive equalizer enhances the received pulse shape, thereby restoring a "flat" channel response with maximum eye opening over a wide spread of cable attenuation characteristics. This equalizer is always enabled when either TE mode or NT Mode Adaptive Sampling is selected, but is disabled for short passive bus applications when NT Mode Fixed Sampling is selected. An adaptive threshold circuit maximizes the Signal-to-Noise ratio in the eye at the detector for all loop conditions.

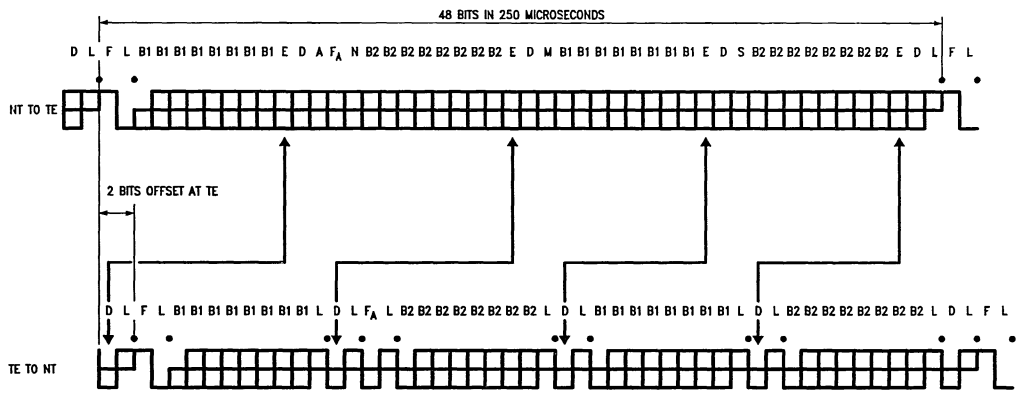
A DPLL (Digital Phase-Locked Loop) recovers a low-jitter clock for optimum sampling of the received symbols. The MCLK input provides the reference clock for the DPLL at 15.36 MHz. Clocks for the digital interface timing may either be derived from this recovered clock, as in TE Master mode, or may be slaved to an external source, as in the T-interface side of an NT-2 (TES mode). In TES and NT modes, re-timing circuitry on the TP3421 allows the MCLK frequency to be plesiochronous with respect to the network clock, i.e. the 8 kHz FS_a input. With a tolerance on the MCLK oscillator of 15.36 MHz ±100 ppm, the lock-in range of the DPLL allows the network clock frequency to deviate up to ±50 ppm from nominal.

When the device is powered-down (either on initial powering-on of the device or after using a PDN command), a Line-Signal Detect circuit is enabled to detect the presence of incoming data if the far-end starts to activate the loop. The LSD circuit is disabled by a Power-Up (PUP) command.



TL/H/10565–3

FIGURE 1. Inverted AMI Line-Coding Rule



TL/H/10565–4

Legend:

F = **Framing bit**
L = **DC Balancing bit**
D = **D-channel bit**
E = **D-echo-channel bit**
F_A = **Auxiliary framing bit or Q Channel bit**
M = **Multiframe Sync bit**
N = **bit set to a binary value N = $\overline{F_A}$**
B1 = **bit within B-channel 1**
B2 = **bit within B-channel 2**
A = **bit used for activation**
S = **S Channel bit**

• Dots mark the boundaries of those parts of the frame that are independently DC-balanced

FIGURE 2. Frame Format

Functional Description (Continued)

General Circuit Interface

Enabled by tying the RST pin low at power-on reset, the GCI interface is designed for systems in which PCM and control data are multiplexed together into 4 contiguous bytes per 8 kHz frame. Furthermore, in Subscriber Line Cards and NT1–2's up to 8 GCI channels may be carried in 1 frame of a GCI multiplex, with a combined bit rate from 256 kb/s up to 3088 kb/s. Pin-programmable GCI-channel assignment for 8 GCI channels is provided.

GCI PHYSICAL INTERFACE

The interface physically consists of four wires:

— Transmit Data to Line: B_X
— Receive Data from Line: B_r
— Bit Clock at 2 cycles/bit: BCLK
— 8 kHz Frame Sync: FS_a

Data is synchronized by the BCLK and FS_a clock inputs. FS_a insures re-initialization of the time-slot counter at the beginning of each 8 kHz frame, with the rising edge of FS_a being the reference time for the first GCI channel bit. Data is clocked in both directions at half the BCLK input frequency. Data bits are output from the device on a rising edge of BCLK and sampled on the second falling edge of BCLK; unused slots are high impedance. B_r is an open-drain n-channel output, with internal detection for contention resolution on the Monitor and C/I channels between devices attempting to use the same GCI channel (typically in a TE application).

A device may be either the Master or Slave of the GCI timing. In TE Master mode it is the source of BCLK and FS_a, which are synchronized to the data received from the line. In TES Slave mode and NT modes BCLK and FS_a must be sourced externally, typically from a system backplane.

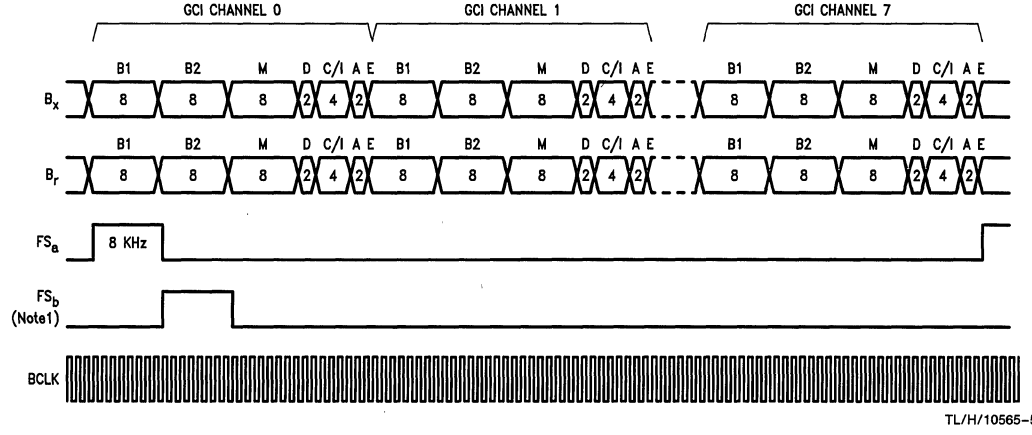
For applications such as the network side of an NT-2, e.g. a PBX trunk card, the TE Slave (TES) Mode is provided. This "slave-slave" mode allows the transmission side of the device to be a slave to the received frame timing, while the GCI is also in a slave mode i.e., FS_a and BCLK are inputs. The GCI includes elastic buffers which allow any arbitrary phase relationship between the FS_a input and the received I.430 frame. Also, jitter and low-frequency wander between the frames across the device is absorbed, up to at least 18 μs pk-pk at frequencies below 10 Hz.

TES Mode also provides a synchronized clock output (SCLK) which is phase-locked to the received line signal; SCLK may be used as the BCLK source. The SCLK outputs of a number of devices may be wire-OR'd together; a detector circuit senses the pin before the SCLK output driver is enabled to prevent more than one activated device driving the wire-OR bus.

GCI FRAME STRUCTURE

Figure 3 shows the frame structure at the GCI interface. One GCI channel supports one TP3421 using a bandwidth of 256 kbit/s, consisting of the following channels multiplexed together in an 8 kHz frame:

— B1 channel at 8 bits per frame;
— B2 channel at 8 bits per frame;
— Monitor (M) channel at 8 bits per frame;
— Signalling and Control (SC) channel, which is structured as follows:
  D channel at 2 bits per frame;
  C/I channel at 4 bits per frame;
  A bit, for acknowledgement of M channel bytes;
  E bit, which indicates the end of the byte.



TL/H/10565–5

Note 1: In TE Master Mode only.

FIGURE 3. GCI Interface Frame Structure (Showing 8-Channel Multiplex with BCLK = 4.096 MHz)

Functional Description (Continued)

General Circuit Interface (Continued)

For line card applications such as PBX's (LT/NT2 mode on the line side or TE Slave mode on the trunk side) multiple GCI channels (32 bits each) may be multiplexed on B_x and B_r. On a typical 2.048 Mb/s time-division multiplexed interface, 8 GCI channels may be multiplexed with a BCLK of 4.096 MHz. GCI channel selection is by means of strapping the S2, S1 and S0 pins high or low, as shown in Table II.

TABLE II. GCI Channel Programming

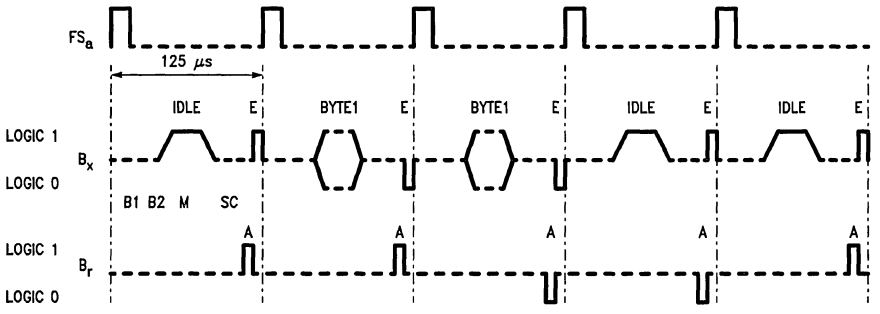
S2	S1	S0	Channel Number	Timeslots
0	0	0	0	0–3
0	0	1	1	4–7
0	1	0	2	8–11
0	1	1	3	12–15
1	0	0	4	16–19
1	0	1	5	20–23
1	1	0	6	24–27
1	1	1	7	28–31

GCI Monitor Channel

The Monitor channel (byte 3) is used for the system controller to access the Control Register functions shown in Table III, and for the device to report changes in the Multiframe Receive Register, as listed in Table IV. Each access to or from one of the listed registers requires a 1-byte data read or write operation. As shown in Tables III and IV, this byte from the originating device contains both a function address and a data field. In addition a protocol is used, based on the E and A bits in byte 4, to provide an acknowledgement of each Monitor channel byte in either direction, see *Figure 4*.

When no Monitor Channel message is being transferred the E bit, and the A bit in the reverse direction, are both high-impedance (and pulled high by the external resistor if no other device is active in that channel). To initiate a transfer, the sending device first verifies that it has received the A bit = 1 for at least 2 consecutive GCI frames from the other device before starting the transfer. It then sends the byte in the Monitor channel, with the associated E bit = 0, and repeats the byte in the next GCI frame. Normally, the receiving device will verify receiving the same byte in 2 consecutive frames and acknowledge this by setting A = 0 for at least 2 frames. If not, the message is aborted by sending A = 0 for only 1 frame.

On detecting the acknowledgement, the sending device then sends E = 1 to indicate this is the last (and only) byte of the transfer. The receiver acknowledges by sending A = 1 in the following frames. If a Monitor channel message originated by the TP3421 is aborted, it will repeatedly attempt the transfer until it is successfully acknowledged.



TL/H/10565–6

FIGURE 4. GCI Monitor Channel Protocol

Functional Description (Continued)

TABLE III. Monitor Channel Control Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Device Modes									
*NT Mode, Adaptive Sampling	NTA	0	0	0	0	0	1	0	0
NT Mode, Fixed Sampling	NTF	0	0	0	0	0	1	0	1
TE Slave Mode	TES	0	0	0	0	0	1	1	0
TE Master Mode	TEM	0	0	0	0	0	1	1	1
Monitor Mode Activation	MMA	0	0	0	1	1	1	1	1
B1 Channel Enable/Disable									
B1 Channel Enabled	B1E	0	0	0	1	0	1	0	0
*B1 Channel Disabled	B1D	0	0	0	1	0	1	0	1
B2 Channel Enable/Disable									
B2 Channel Enabled	B2E	0	0	0	1	0	1	1	0
*B2 Channel Disabled	B2D	0	0	0	1	0	1	1	1
B Channel Exchange									
*B Channels Mapped Direct, B1 to B1, B2 to B2	BDIR	0	0	0	0	1	1	0	0
B Channels Exchanged, B1 to B2, B2 to B1	BEX	0	0	0	0	1	1	0	1
End of Message Indication									
*EOM Indication Enabled	EIE	0	0	0	1	0	0	0	0
EOM Indication Disabled	EID	0	0	0	1	0	0	0	1
Multiframe Circuit									
Multiframe Circuit Enabled	MCE	0	0	0	1	0	0	1	0
*Multiframe Circuit Disabled	MCD	0	0	0	1	0	0	1	1
Multiframe Receive Message 3x Checking									
*Enable 3X Checking	EN3X								
Disable 3X Checking	DIS3X								
Multiframe Transmit Register									
Write to Multiframe Transmit Register	MFT	0	0	1	1	M1	M2	M3	M4
Loopback Test Modes									
Loopback B1 towards Line Interface	LBL1	0	0	0	1	1	0	0	0
Loopback B2 towards Line Interface	LBL2	0	0	0	1	1	0	0	1
Loopback 2B + D towards GCI	LBS	0	0	0	1	1	0	1	0
Loopback B1 towards GCI	LBB1	0	0	0	1	1	1	0	0
Loopback B2 towards GCI	LBB2	0	0	0	1	1	1	0	1
*Clear All Loopbacks	CAL	0	0	0	1	1	0	1	1

*Indicates initial state following power-on.

TABLE IV. Monitor Channel Status Functions

Function	Mnemonic	Bit Number							
		7	6	5	4	3	2	1	0
Multiframe Receive Register Requires Service	MFR	0	0	1	1	M1	M2	M3	M4

Functional Description (Continued)

DEVICE MODES

NTA — NT Mode, Adaptive Sampling should be selected when the device is in an NT on any wiring configuration up to the maximum specified length for operation. Multiple terminals, if required, must be grouped within approximately 100 meters of each other (depending on cable capacitance, see I.430). The GCI is a slave to external BCLK and FS sources.

NTF — NT Mode Fixed Sampling may be selected when the device is in an NT on a passive bus wiring configuration up to approximately 200 meters in length (depending on cable type). In this mode the receiver DPLL is disabled and sampling of the received symbols is fixed, to enable multiple terminals (nominally up to 8) to be connected anywhere along the passive bus. Again, the GCI is a slave to external BCLK and FS sources.

TEM — TE Master Mode should be selected when the device is in a TE. The TP3421 is then the source of the BCLK and FS signals, and access to the Transmit D channel, including the priority and contention resolution control, is enabled as described in the section on TE Mode D-Channel Access.

TES — TE Slave Mode, otherwise known as "Slave-slave" mode, should be selected when the device is used on the T-interface side of an NT-2. The GCI is then driven by BCLK and FS sources in the NT-2. Data buffers and a clock re-synchronizer enable this interface to function with jittering sources for BCLK and FS. All D Channel access control circuitry is disabled, i.e. D Channel data at the B_X input is continuously transmitted to the line; there is no monitoring of the D-echo channel from the network direction. Also, the SCLK function is enabled at the PCKO/SCLK pin.

MMA — Intended for test equipment applications, this instruction allows the receive line interface ($L_I\pm$) to be connected to the TE-to-NT direction twisted pair and to activate on the received INFO 3 signals while being the master of the GCI. The received 2B+D can then be passively monitored (the line transmit output $L_O\pm$ would not be connected). TE Master mode must be selected prior to power-up by connecting M0 = 0 and M1 = 0.

B CHANNEL CONTROL

BDIR) / BEX) — These commands provide for the exchange of data between the B1 and B2 channels as it passes through the device (Note 1).

Note 1: When enabling a B channel in conjunction with the BEX Command, the channels are referenced at the Digital System Interface, not the line interface e.g. to connect the B1 slot on the DSI with the B2 slot on the line interface, use the BEX and B1E commands.

B1E) / B1D) / B2E) / B2D) — When either or both B channels are disabled, binary 1s are transmitted on the line in those B channel bit positions, regardless of data at the B_X input, and the B_r output is high-impedance in those bit positions.

MULTIFRAME TRANSMIT REGISTER

MFT / MCE / MCD — With the device in TE Mode, data entered in bit positions M1, M2, M3 and M4 is transmitted towards the NT in multiframe bit positions Q1, Q2, Q3 and Q4 respectively. With the device in NT Mode, data entered in the M bit positions is transmitted towards the TE in multiframe bit positions S11, S12, S13 and S14 respectively. The Multiframe Channel must be enabled by an MCE command to use these channels; an MCD command will disable them, (see Multiframe Maintenance Channel section).

MULTIFRAME MESSAGE CHECKING

EN3X / DIS3x — EN3x enables the checking of certain S and Q channel messages before generating the MFR indication. DIS3x disables this circuit, so that the received S or Q word generates MFR once per multiframe (see Multiframe Maintenance Section).

LOOPBACK TEST MODES

Three classes of loopback mode are available on the SID, selected by writing the appropriate Control instruction.

LBS — This loopback at the system interface is a full loopback of the 2B+D channels from the B_X input to the B_r output. It may be set when the device is either activated, in which case it is transparent (i.e. the composite signal is also transmitted to the line), or when it is deactivated.

LBL1/2 — These loopbacks turn each individual B channel from the line receive input back to the line transmit output. They may be set separately or together.

LBB1/2 — These loopbacks at the Digital System Interface loop the B1 (LBB1) or the B2 (LBB2) channel data from the B_X input to the B_r output. The B_X input data is also sent to the line transmit output.

EXTERNAL SELF-ACTIVATING LOOPBACK

A quick self-test of the device is possible by connecting together the line sides of the transmit and receive transformers. NTA or NTF mode must be selected, and the device can then be activated by the normal command sequence (Note 2).

Note 2: This test mode is not possible by direct connection of $L_O\pm$ and $L_I\pm$ pins due to incompatible internal bias voltages.

MONITOR CHANNEL STATUS INDICATORS

MFR — This message indicates when the Multiframe receive data buffer requires servicing, after 1 or 3 consecutive identical Multiframe words have been detected, see Table IV. All Multiframing functions can be disabled via an MCD Command if desired.

Functional Description (Continued)

GCI C/I CHANNEL

The C/I (Command/Indicate) channel in GCI byte 4 is used solely to access the Activation Control and Status indicators in the TP3421. Table V shows the coding of the 4 bit messages. A change in status is repeated in the transmit C/I channel in at least 2 consecutive GCI frames, while a change in received message is verified in 2 consecutive GCI frames before taking the appropriate action.

TABLE V. C/I Control Channel Coding

Code	TE Master		TE Slave		NT1		NT2	
C4C3C2C1	Ind.	Com.	Ind.	Com.	Ind.	Com.	Ind.	Com.
0000	DR	PUP/DR	DR	PUP/DR	TIM	DR	TIM	PUP/DR
0001	X	PDN	X	PDN	X	X	X	PDN
0010	X	X	X	X	X	X	X	X
0011	EOM (1)	X	X	X	X	X	X	X
0100	EI	X	EI	X	EI	RSY	EI	X
0101	X	X	X	X	X	X	X	X
0110	X	X	X	X	X	X	X	X
0111	X	X	X	X	X	X	X	X
1000	AP	AR8	AP	AR	AP	AR	AP	AR
1001	CON (1)	AR10	X	X	X	X	X	X
1010	X	ARL	X	ARL	X	ARL	X	ARL
1011	X	X	X	X	X	X	X	X
1100	AI8	X	AI	X	AI	UAR	AI	UAR
1101	AI10	X	X	X	X	X	X	X
1110	AIL	X	AIL	X	AIL	X	AIL	X
1111	DI	DI	DI	DI	DI	DI	DI	DI

(X) codes reserved

(1) codes sent only two times when event occurs.

C/I CHANNEL COMMANDS

PUP/DR When in the power-down state this is the power-up command, which powers up all the circuitry, starts the XTAL and resets the state machine to the deactivated state. In TEM mode, the GCI clocks must be started by pulling the B_X pin low prior to sending PUP/DR. The PUP/DR or DR command is also used in the power-up state as the Deactivate Request, which forces transmission of INFO 0.

PDN This is the power-down command, which forces the device to first send the DI indicator in the C/I channel on B_r for 2 GCI frames, and then to power-down at the end of the assigned GCI channel. It should only be used after the TP3421 has been put in a known state, e.g. in a TE after a DI status has been reported, since it does not force sequencing through any of the deactivation states.

AR Used in NT and TES applications, this is the Activation Request which starts transmission of the appropriate activation sequence.

UAR Used in NT applications only, this command must be used after the AI is generated on detection of INFO 3 from the terminal(s). UAR completes the activation, causing transmission of INFO 4 frames with the 2B + D operational.

AR8 Used in TE Master mode only, this command functions as an Activate Request followed by an immediate access to the transmit D channel with a packet of the high priority class (see the section on TE Mode D-Channel Access).

Functional Description (Continued)

AR10 Used in TE Master mode only, this command functions as an Activate Request followed by an immediate access to the transmit D channel with a packet of the low priority class (see the section on TE Mode D-Channel Access).

ARL The Activate Request for Loopback, which operates a full loopback of the 2B+D channels from the B_X input to the B_r output. It may either be set when the device is activated, in which case it is transparent (the composite signal is also transmitted to the line) or when it is deactivated, in which case it is non-transparent.

DI When used as a command, DI allows the device to automatically power-down if the S Interface is already deactivated.

RSY Effective only in NT modes, and only after Activation has been completed, this instruction forces the NT to transmit INFO 2 frames instead of INFO 4, normally to allow testing at the U interface. Provided INFO 3 is still being received from the TE(s), an AI Status message will be generated and loop synchronization maintained, but 2B+D transmission is inhibited. To restore full loop activation, with the NT sending INFO 4, a UAR command is required in the normal way.

C/I CHANNEL STATUS INDICATORS

TIM Timing Request indicator, which occurs when a deactivated NT has detected a "wake-up" signal, passed a Line Signal Detect upstream and received GCI clocks. TIM acts as confirmation that the device has powered up. This indicator also occurs in an activated NT in response to a DR command.

DR Deactivate Request indicator which is generated when any of the following events occurs:

- — just after power-up when the S line signal has not yet been identified;
- — detection of INFO 0 on an activated (or partially activated) line;
- — after a PUP command while activation is pending.

AI This is the Activation Indication generated when activation is completed in response to an AR command.

AI8 This is the Activation Indication, generated in TE Master mode only, when activation is completed in response to an AR8 command; the D channel access procedure is set in the high priority class.

AI10 This is the Activation Indication, generated in TE Master mode only, generated when activation is completed in response to an AR10 command; the D channel access procedure is set in the low priority class.

AIL This is the Activation Indication Loopback, which indicates that the complete loopback requested via an ARL command is in effect.

AP This is the Activation Pending indication, which occurs in a TE when INFO 2 or INFO 4 frames are detected. An AR command must be sent to allow activation to be completed.

EI This is the Error Indication, which occurs when loss of frame alignment is detected. Also, in a TE, if the line is already activated and the received line signal changes from INFO 4 to INFO 2 (during loop testing) this indicator is generated.

DI This is the Deactivation Indication, which is generated in response to a DI command. After the indicator is acknowledged by the A bit, the device may be powered down, by the PDN command in a TE or by stopping the GCI clocks in an NT1 or NT2.

EOM This is the End of Message indicator, which occurs when the closing flag of a D-channel packet has been transmitted by a TE on the S Interface, indicating successful completion of a packet. The generation of this code can be disabled via the Monitor Channel using the EID command.

CON This is the Contention indicator, which occurs when, during transmission of a packet in the D channel, a received E bit does not match the last transmitted D bit, indicating a lost collision. A new AR8 or AR10 command is necessary to restart the D channel access procedure.

ACTIVATION/DEACTIVATION: TP3421 IN NT MODE

Activation (i.e. transmission and loop synchronization) may be initiated from either end of the loop. To initiate Activation from the NT, the TP3421 must be powered up (see Initialization Section), followed (Note 3) by an AR command in the C/I Channel. Network timing, i.e., an 8 kHz input to FS_a, must be present at this time. The device then begins to send data framed as INFO 2 type, in which bits in the B, D and D-echo channels are set to binary 0. These frames are detected by the TE, which replies with data framed as INFO 3 type, synchronized to received frames. A flywheel circuit in the TP3421 NT searches for 3 consecutive correctly formatted receive frames to acquire frame synchronization. If Multiframing is enabled (MIE), 60 correct frames (3 multiframes) are required to achieve full loop synchronization. When it is correctly in sync with received frames, the NT device sends AI in the C/I channel. A UAR command is required to cause the NT to send INFO 4 frames, in which the B and D channels are enabled for transmission (this command may be delayed until the upstream link indicates that it is also fully activated).

Note 3: A delay of ≥ 2 ms is recommended to ensure that all internal circuits have settled.

Functional Description (Continued)

When Activation is initiated by a TE, the TP3421 in NT mode will detect the incoming INFO 1 signal and, if it is powered-down will pull the $\overline{LSD}$ pin low, which can be used to "wake-up" a microprocessor. The device must then be powered up by the specified initialization procedure. Upon identifying the INFO 1 signal, the device sends AP in the C/I channel. An AR command is required to start sending INFO 2 frames, which allows the Activation sequence to proceed as described above.

Once Activated, loss of frame alignment is assumed by the TP3421 when a time which is equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the NT does detect alignment loss it will start to transmit INFO 2. At this point EI is sent in the C/I channel and the receiver searches to identify the incoming signal and attempt to re-acquire loop synchronization. If it successfully re-establishes synchronization with the incoming signal (INFO 3 frames), AI is sent in the C/I channel and re-activation can be completed by sending a UAR command. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, Status Indicator TIM is sent in the C/I channel, with the transmitted frames changed to INFO 0.

I.430 recommends 2 timers should be available in an NT. An Activation Request to the TP3421 should be associated with the start of an external Timer 1, if required. Timer 1 should be stopped when the AI status message is generated following successful Activation. If Timer 1 expires before AI is generated, however, the DR command should be written to the device to force de-activation. Timer 2, which is specified to prevent unintentional reactivation, is not required since the TP3421 can uniquely recognise INFO 1 frames.

ACTIVATION/DEACTIVATION: TP3421 IN TE MODE

To activate the loop with the TP3421 at the TE end the device must first be powered-up (see Initialization Section), followed by a Control Instruction type AR (Note 3). This is the Activation Request to begin transmission of INFO 1 frames after verifying that INFO 0 is being received from the NT. INFO 1 is a continuous pattern of 0+, 0−, and 6 '1's repeated. At this point the TE is running from its local oscillator and is not receiving any sync information from the NT. When the NT recognises this "wake-up" signal, it begins to transmit INFO 2, synchronized to the network clock (following activation of the "U" interface, if applicable). This enables the phase-locked loop in the TE's receiver to correctly identify bit timing from the NT and to synchronize its own transmission to that of the NT. On identifying INFO 2 for 3 consecutive frames, the TE changes its transmit data to INFO 3 and awaits the return of INFO 4 from the NT. Identification of INFO 4 completes the Activation sequence, which the device indicates by sending AI in the C/I channel.

When Activation is initiated by the NT, if the TP3421 in TE mode is powered down, it will pull the $\overline{LSD}$ pin low on receiving a line signal, which can be used to "wake-up" a microprocessor. The specified initialization procedure is required to enable the device to power-up, identify the received signal, and acquire bit and frame synchronization. Once INFO 2 has been identified, the TP3421 will send AP in the C/I channel. The microprocessor must respond by sending AR in order for Activation to proceed. INFO 3 frames are then transmitted. Finally, when the NT replies with INFO 4 frames, AI is sent in the C/I channel.

As in NT mode, once Activated, loss of frame alignment is assumed by the TP3421 when a time equivalent to three frames has passed without it detecting any of the valid pairs of line code violations which obey the framing rule. If the TE does detect alignment loss it will cease transmitting immediately. At this point EI is sent in the C/I channel, and the receiver searches to re-acquire loop synchronization if INFO 2 or INFO 4 frames are still being received. If synchronization is re-established, AI is sent. If, however, the receiver subsequently identifies that the incoming line signal has ceased, i.e. INFO 0 is being received, the loop is de-activated, and DI is sent to indicate De-activation.

I.430 does not provide for Deactivation to be initiated by a TE. However, a power-down state may be forced if required, normally after Deactivation has been established by the network (see POWER-DOWN section).

If required, an external Timer 3 should be started when an Activation Request is sent to the TP3421. The subsequent AI indication should be used to stop the timer. If the timer expires before an AI is generated, PUP/DR must be sent to the device to force the transmission of INFO 0.

TE MODE D-CHANNEL ACCESS

In TE Master and Slave modes the TP3421 SID arbitrates access for Layer 2 Transmit frames to the D-channel bit positions in accordance with the I.430 Priority Mechanism (I.430 Section 6.1). This mechanism is to resolve contention for the D channel towards the network when 2 or more TEs are connected to a Passive Bus. The shifting of D-channel transmit data from the Layer 2 device into the SID buffer is controlled by gating the DEN_X output with BCLK. When no Layer 2 frame is pending, "1"s are always transmitted by the SID in D-bit positions at the S Interface. DEN_X output pulses are inhibited and no D-channel data is shifted into the B_X input. An external Layer 2 device requiring to start transmission of a packet should first prime its Transmit buffer such that the opening flag is ready to be shifted across the digital interface. Then a C/I command, either AR8 for a Priority Class 1 (signaling) packet or AR10 for a Priority Class 2 packet, will initiate the D-channel access sequence.

In response to the command, the DEN_X output is enabled to pre-fetch the opening flag from the Layer 2 device into the D-channel buffer. Meanwhile, the Priority Counter checks that no other TE connected to the S Interface (in a point-to-multipoint wiring configuration) is transmitting in the D-channel. This is assured by counting consecutive "1"s in the E-bit position of frames received from the NT. At least 8 consecutive "1"s must be detected before transmission of the pending D-channel frame begins, in accordance with Table VI.

Functional Description (Continued)

TABLE VI. D-Channel Access Criteria

Number of Consecutive "1"s in the E-Channel	D-Channel Access
7	Abort. Possible re-try by the transmitting TE.
8	Signalling packet (Priority Class 1) may begin (Note 1).
9	Signalling packet may begin unconditionally.
10	Any packet type may begin (Priority Class 2) (Note 2).
11	Any packet type may begin unconditionally

Note 1: Only if, since the SID last transmitted a complete Class 1 packet, a sequence of ≥ 9 consecutive "1"s has been detected in the E-channel.

Note 2: Only if, since the SID last transmitted a complete packet of either class, a sequence of ≥ 11 consecutive "1"s has been detected in the E-channel.

If another TE is active in the D-channel, DEN_X pulses are inhibited once the opening flag is in the Transmit buffer, to prevent further fetching of transmit data from the Layer 2 device until D-channel access is achieved. As soon as the required number of consecutive E-channel "1"s has been counted, the leading 0 of the opening flag is transmitted in the next D-bit position towards the NT. DEN_X pulses are also re-enabled in order to shift D-channel bits from the Layer 2 device into the SID transmit buffer.

During transmission in the D-channel the TP3421 SID continues to compare each E-bit received from the NT with the D-channel bit previously transmitted before proceeding to send the next D-bit. In the event of a mis-match, a contention for the previous D-bit is assumed to have been won by another TE. Transmission of the current packet therefore ceases and "1"s are transmitted in all following D-bit positions. Status Indication type CON is sent in the C/I channel, and DEN_X output pulses are again inhibited.

In order to retransmit the lost packet, the Layer 2 device must begin as before, by priming its Transmit buffer with the packet header. It must also reset the C/I channel by sending the DI code to the TP3421 in at least 2 consecutive GCI frames, prior to sending a new AR8 or AR10 command.

DEN_X pulses stop immediately after receiving the closing flag on the B_X input from the layer 2 device.

Successful completion of a transmit packet is detected by the TP3421 when the closing flag is transmitted in the D channel. '1's are then transmitted in the following D bit positions. Status Indication type EOM is sent, to indicate the End of Message. Also, the Priority Access counters are decremented to the lower priority level within each priority class, in accordance with the I.430 algorithm. Priority is subsequently restored to the higher level when the specified number of consecutive 1's (9 or 11) is detected in the D-echo-bit position.

MULTIFRAME MAINTENANCE CHANNELS (S1 AND Q WORDS)

Each direction of transmission across the S Interface includes a low-speed (800 b/s) channel for loop maintenance, accessed via the control interface of the TP3421. A multiframe structure, consisting of 20 frames on the S Interface, is used to synchronize these channels and convey messages coded into 4-bit words, see Table VII. One word is transmitted downstream (NT-to-TE) in the S1 channel, and one word is transmitted upstream (TE-to-NT) in the Q channel every multiframe.

When the device is in NT mode, the MIE command enables both the transmission of the Multiframe identification algorithm (reversal of the FA/N bits every 5th frame and M bit set = 1 every 20th frame) and the generation of the MFR indication in the Monitor Channel. The algorithm is present during INFO 2 and INFO 4 frames. In TE modes this command only enables the MFR indication, since the device will always search for and synchronize to the multiframing identification bits if the NT is sending them. In all modes there is an option to enable or disable an automatic checking circuit to validate received S or Q channel words. If this circuit is enabled by the EN3X instruction, at the end of each multiframe the received 4-bit word is decoded to determine if it should generate an MFR indication immediately, or be stored until 3 consecutive multiframes have contained the same 4-bit word before an indication is generated. Table VII lists the codes which are 3-times checked. Note, however, that no other action is taken by the TP3421 in response to received codes (e.g. loopbacks are not automatically implemented); the external controller must take the necessary action. This provides the freedom to implement maintenance functions without constraints from the device, and to utilize the unassigned codes for other functions.

If the 3 times checking circuit is disabled by the DIS3X instruction, each received S or Q word generates an MFR indication once per multiframe.

The MCD command disables the transmission of the Multiframe identification algorithm in NT mode and disables the MFR indication in both NT and TE modes. Both the MCE and MCD commands can only be written to the device when it is deactivated (either powered-up or powered-down). The Multiframe Transmit Register should also be loaded with the appropriate "Idle" messages, by means of an MFT command, prior to activation.

Functional Description (Continued)

TABLE VII. Codes for Q-Channel and S1-Channel Messages with 3x Checking Enabled

Message	NT-to-TE					TE-to-NT				
	Received at TE				Number of Repetitions before MFR Message	Received at NT				Number of Repetitions before MFR Message
	S11	S12	S13	S14		Q1	Q2	Q3	Q4	
Idle (NORMAL)	0	0	0	0	3	1	1	1	1	3
Loss-of-Power Indication	1	1	1	1	1	0	0	0	0	1
STP Pass	0	0	1	0	3	—	—	—	—	—
STF Fail	0	0	0	1	3	—	—	—	—	—
ST Request (Note 1)	—	—	—	—	—	0	0	0	1	3
STI Indication	0	1	1	1	3	—	—	—	—	—
DTSE-IN	1	0	0	0	1	—	—	—	—	—
DTSE-OUT	0	1	0	0	1	—	—	—	—	—
DTSE-IN&OUT	1	1	0	0	1	—	—	—	—	—
LB1 Request	—	—	—	—	—	0	1	1	1	3
LB1 Indication	1	1	0	1	3	—	—	—	—	—
LB2 Request	—	—	—	—	—	1	0	1	1	3
LB2 Indication	1	0	1	1	3	—	—	—	—	—
LB1/2 Request (Note 2)	—	—	—	—	—	0	0	1	1	3
LB1/2 Indication	1	0	0	1	3	—	—	—	—	—
Loss-of-Received-Signal Indication	1	0	1	0	3	—	—	—	—	—
Unassigned	All Other Codes				1	All Other Codes				1

Note 1: The code "0001" will be received by an NT1 when ST Request and any other code (except LP) is sent simultaneously by two or more TEs on a Passive Bus.

Note 2: The code "0011" will be received by an NT1 when the LB1 and LB2 requests are transmitted by two different TEs (NT2s) on a Passive Bus.

Applications Information

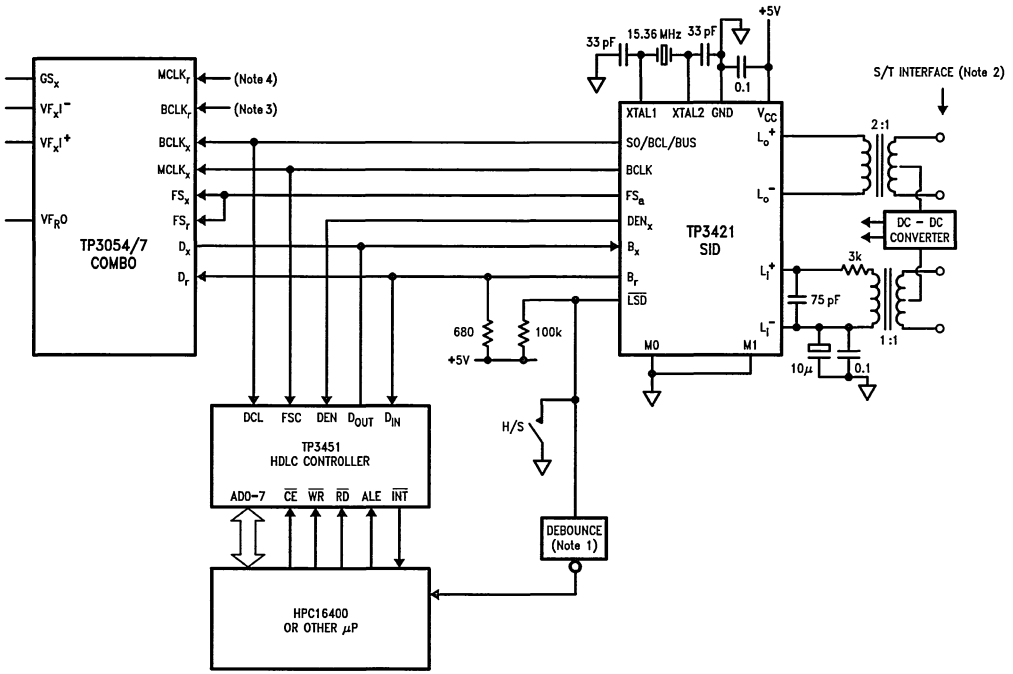
While the pins of the TP3421 SID are well protected against electrical misuse, it is recommended that the standard CMOS practice of applying GND to the device before any other connections are made should always be followed. In applications where the printed circuit card may be plugged into a hot socket with power and clocks already present, an extra long ground pin on the connector should be used.

To minimize noise sources, all ground connections to each device should meet at a common point as close as possible to the GND pin in order to prevent the interaction of ground return currents flowing through a common bus impedance. A decoupling capacitor of 0.1 μF should be connected from this common point to V_{CC}. Taking care with the pcb layout in the following ways will help prevent noise injection into the receiver front-end and maximize the transmission performance:

1. keep the crystal oscillator components away from the receiver inputs and use a shielded ground plane around these components.
2. keep the connections between the device and the components on the $L_i\pm$ inputs short; the L_i- capacitors should be connected close to the device pins.
3. keep the connections between the device and the transformers short.

Figure 5 shows a typical application of the TP3421 in an ISDN Terminal. To provide a voice channel, the TP3054/7 Combo I Codec/filter is shown. Although these Combos clock PCM data at a rate of 1 CLK cycle per bit, direct compatibility with the GCI is provided by connecting the BCL output of the TP3421 (in TEM mode) to the $BCLK_X$ input of the Combo. Data is shifted between devices in the B1 channel at 768 kHz, with the 1.536 MHz GCI clock (BCLK) providing the MCLK for the Combo. If the network assigns the B2 channel to a voice call, the BEX command is used to exchange the B1 and B2 slots between the GCI and S/T interfaces.

For more in-depth information on a variety of applications, the TP3421 Users Manual is a comprehensive guide to the hardware and software required to meet the I.430 interface specification. Performance measurements, demonstrating compliance with I.430 and ANSI transmission requirements, are also included.



TL/H/10565–7

Note 1: Only necessary if a mechanical hook switch is connected to the NMI input of the HPC.

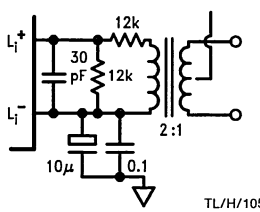
Note 2: See TP3421 User's Manual for Line Interface Protection.

Note 3: For TP3054 (μ-law) leave $BCLK_r$ open-circuit. For TP3057 (A-law) connect $BCLK_r$ low for 1-536 MHz MCLK operation. $BCLK_x$ operates at 768 kHz.

Note 4: To power-up the Combo, $MCLK_r$/PDN must be pulled low.

FIGURE 5. Typical Application in a TE and/or TA

Alternative Receive Input Using 2:1 Transformer



TL/H/10565–8

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Voltage at L_i, L_o Pins	V_{CC} + 1V to GND − 1V
Voltage at any Digital Input	V_{CC} + 1V to GND − 1V
Storage Temperature Range	−65°C to +150°C
Current at L_o Pins	±100 mA
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C

ESD rating to be determined.

Electrical Characteristics

Unless otherwise noted, limits printed in **bold** characters are electrical testing limits at V_{CC} = 5.0V and T_A = 25°C. All other limits are design goals for V_{CC} = 5.0V ±5% and T_A = 0 to 70°C. This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
DIGITAL INTERFACES						
V_{IL}	Input Low Voltage	All Digital Inputs			0.7	V
V_{IH}	Input High Voltage	All Digital Inputs	2.2			V
V_{ILX}	Input Low Voltage	MCLK/XTAL Input			0.5	V
V_{IHX}	Input High Voltage	MCLK/XTAL Input	V_{CC} − 0.5			V
V_{OL}	Output Low Voltage	B_r, I_L = 3.2 mA All Other Digital Outputs, I_L = 1 mA			0.4	V
V_{OH}	Output High Voltage	B_r, I_L = −3.2 mA All Other Digital Outputs, I_L = −1 mA All Outputs, I_L = −100 μA	2.4 2.4 V_{CC} − 0.5			V V V
I_I	Input Current	Any Digital Input, GND < V_{IN} < V_{CC}	−10		10	μA
I_{OZ}	Output Current in High Impedance State (TRI-STATE®)	B_r, $\overline{LSD}$ GND < V_{OUT} < V_{CC}	−10		10	μA
LINE INTERFACES						
R_{Li}	Differential Input Resistance	GND < L_i+, L_i− < V_{CC}	200			kΩ
CL_{L0}	Load Capacitance	Between L_o+ and L_o−			200	pF
VOS	Differential Output Offset Voltage at L_o+, L_o−	Driving Binary 1s, 220Ω between L_o+ and L_o−	−20		+20	mV
POWER DISSIPATION						
$I_{CC}0$	Power Down Current	All Outputs Open-Circuit		1.0		mA
$I_{CC}1$	Power Up Current	As Above, Device Deactivated (Note 1)		18.0		mA
TRANSMISSION PERFORMANCE						
	Transmit Pulse Amplitude	R_L = 220Ω Between L_o+ and L_o− (Note 2)	±1.55		±1.75	Vpk
	Transmit Pulse Unbalance	0+ Relative to 0−			±5	%
	Input Pulse Amplitude	Differential Between L_i+ and L_i−	±175			mVpk

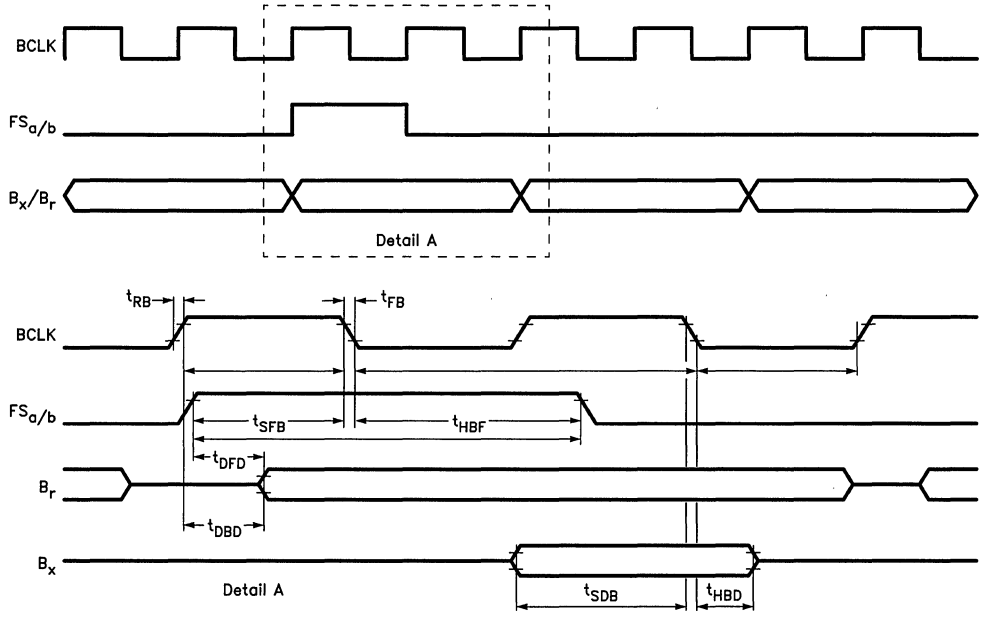
Note 1: When the device is activated and driving a correctly terminated line, I_{CC1} increases by several mA. A worst-case data pattern, consisting of all binary 0's, increases I_{CC1} by approximately 8 mA.

Note 2: The pulse amplitude at the L_o± pins allows for approximately 1 dB tranformer insertion loss to meet the 0.75V pulse mask test when the line is terminated in 50Ω.

Timing Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FMCK	Master Clock Frequency Master Clock Tolerance		 −100	15.36	 +100	MHz ppm
	MCLK/XTAL Input Clock Jitter	External Clock Source			50	ns pk-pk
tMH, tML	Clock Pulse Width Hi & Low for MCLK	$V_{IH} = V_{CC} - 0.5V$ $V_{IL} = 0.5V$	20			ns
tMR, tMF	Rise and Fall Time of MCLK	Used as a Logic Input			10	ns
DIGITAL INTERFACE *(Figure 6)*						
tWBH	Period of BCLK High	Measured from V_{IH} to V_{IH}	25			ns
tWBL	Period of BCLK Low	Measured from V_{IL} to V_{IL}	25			ns
tRB	Rise Time of BCLK	Measured from V_{IL} to V_{IH}			15	ns
tFB	Fall Time of BCLK	Measured from V_{IH} to V_{IL}			15	ns
tHBF	Hold Time, BCLK Low to FS, High or Low		25			ns
tSFB	Setup Time, FS High to BCLK Low		50			ns
tDBD	Delay Time, BCLK High to Data Valid	Load = 150 pF Plus 2 LSTTL Loads			80	ns
tDBZ	Delay Time, BCLK High to Br, Dr Disabled				50	ns
tDFD	Delay Time, FS High to Data Valid	Load = 150 pF Plus 2 LSTTL Loads, Applies if FS Rises Later than BCLK Rising Edge in Non-Delayed Data Mode Only			80	ns
tSDB	Setup Time, Data Valid to BCLK Low		0			ns
tHDB	Hold Time, BCLK Low to Data Invalid		25			ns

Timing Characteristics (Continued)



TL/H/10565–9

FIGURE 6. GCI Timing

National Semiconductor

ADVANCE INFORMATION

TP3451 ISDN HDLC and GCI Controller

General Description

The TP3451 is a microprocessor peripheral communications device designed as both a full-duplex HDLC Framing and formatting controller, and a serial GCI (General Circuit Interface) frame controller. It is built on National's advanced M2CMOS process.

On the bus side of the device, full compatibility is provided for multiplexed and non-multiplexed microprocessor busses from National, Intel and Motorola, including DMA support. 64-byte FIFOs buffer the data in each direction of transmission. The HDLC functions include framing, address field control, and CRC processing for both LAPB and LAPD protocols. Also, in multi-protocol applications, the data paths may be switched to a transparent mode, bypassing the HDLC functions. 4 Status registers are also provided.

On the serial side of the device the data may be synchronously clocked in any of 4 distinct modes:

— Continuous unformatted data up to 4 Mb/s;

— Time-division multiplexed in a time-slot at 8, 16, 56 or 64 kb/s, with programmable time-slot assignment;

— GCI format in either of the 2 B channels or the D channel;

— The extended GCI-SCIT mode for ISDN Terminals.

In GCI mode, the TP3451 supports up to 8 GCI channels and also provides access to the GCI Monitor and Command/Indicate channels. The GCI-SCIT mode provides additional channels for control of local peripheral devices in TE applications.

Features

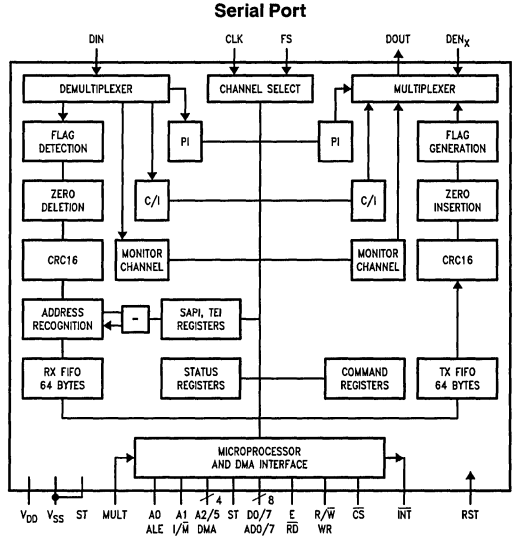
- LAPB and ISDN LAPD controller
- GCI and GCI-SCIT controller for M and C/I channels
- Full-duplex HDLC up to 4 Mb/s (non-GCI)
- Time-slot assigner for up to 64 TDM slots
- Formatter for 8, 16, 56 and 64 kb/s channels
- 4 SAPI and 3 TEI address filtering (LAPD)
- 64-byte FIFOs, with queueing for up to 8 receive frames and 2 transmit frames
- Protocol transparent mode (HDLC bypass)
- Compatible with National, Intel and Motorola μP busses
- DMA support with multiplexed bus
- Comprehensive status reporting
- 28-pin package

Applications

- X.25 terminals and controllers
- ISDN BRI/PRI D channel controller
- ISDN terminal adapters for X.25 and V.120
- ISDN Layer 2 controller for S/T and U BRI line-cards
- Easy interface to:

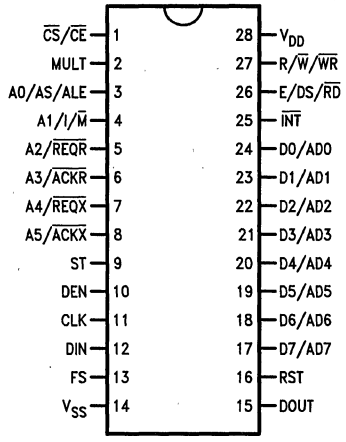
"S" interface device	TP3421
"U" interface device	TP3410
Codec/filter combos	TP3054/7 and TP3075/6
LAPD processor	HPC16400

Block Diagram



TL/H/10727–1

Connection Diagram



TL/H/10727-2

Order Number
TP3451J or TP3451N
NS Package Number J28A or N28B

Pin Descriptions

Name	Pin	Type	Function
V_{DD}	28	I	Positive Power Supply = 5V ± 5%.
V_{SS}	14	I	Signal Ground.
RST	16	I	Reset.
ST	9	I	Special Test (Reserved). Must be tied to V_{SS}.
$\overline{CS}$	1	I	Chip Select. A low level enables the device for read/write operations.
$\overline{INT}$	25	O	Interrupt request is asserted by the device when it requests service. Open drain active low output.
MULT	2	I	Multiplexed Bus. Indicates the μP bus interface selected. MULT = 1: multiplexed bus and DMA available. MULT = 0: address and data bus are separate.
I/$\overline{M}$	4	I	When MULT = 1, I/$\overline{M}$ = 1 selects Intel/National bus timing, and I/$\overline{M}$ = 0 selects Motorola 6803 bus timing.
DEMULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 0)			
A0/A5	3–8	I	Address Bus. Transfers addresses from μP to TP3451.
D0/D7	17–24	I/O	Data Bus. Transfers data between μP and TP3451.
R/$\overline{W}$	27	I	Read/Write. "1" indicates a read operation; "0" a write operation.
E	26	I	Enable. Read/Write operations are synchronized with this signal; its falling edge marks the end of an operation.
MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1; I/$\overline{M}$ = 1)			
AD0/AD7	17–24	I/O	Address/Data Bus. Transfers addresses and data between μP and TP3451.
$\overline{WR}$	27	I	Write. A low on this input indicates a write operation.
$\overline{RD}$	26	I	Read. A low on this input indicates a read operation.
ALE	3	I	Falling edge latches the address from the external A/D bus.

Pin Descriptions (Continued)

Name	Pin	Type	Function
MULTIPLEXED MICROPROCESSOR BUS INTERFACE (MULT = 1; I/$\overline{M}$ = 0)			
AD0/AD7	17–24	I/O	Address/Data Bus. Transfers addresses and data between μP and TP3451.
R/$\overline{W}$	27	I	Read/Write. "1" indicates a read operation; "0" a write operation.
DS	26	I	Data Strobe. Read/Write operations are synchronized with this signal: its falling edge marks the end of an operation.
AS	3	I	Address Strobe. Falling edge latches the address from the external A/D Bus.
DMA (Direct Memory Access): Only when MULT = 1			
$\overline{\text{DMA REQ X}}$ $\overline{\text{DMA REQ R}}$	7 5	O O	Direct Memory Access Requests: these outputs are asserted by the device to request an exchange of byte from the memory; in burst mode only, they are level sensitive.
$\overline{\text{DMA ACK X}}$ $\overline{\text{DMA ACK R}}$	8 6	I I	Direct Memory Access Acknowledge: these inputs are asserted by the DMA controller to signal to the HDLC controller that a byte is being transferred in response to a previous transfer request.
SERIAL PORT IN GCI MODES			
D_{OUT}	15	I/O	Data Output for B and D channels. In GCI mode it outputs B1, B2, M and C/I channels. In GCI-SCIT mode it also functions as D_{IN} for M′ and C/I′ channels (see Table II).
D_{IN}	12	I/O	Data Input for B and D channels. In GCI mode it inputs B1, B2 M and C/I channels. In GCI-SCIT mode (in TE applications) it also functions as D_{OUT} from M″ and C/I″ channels (see Table II).
CLK	11	I	Data Clock which determines the data shift rate for GCI channels on the serial interface, at 2 cycles per bit.
FS	13	I	Frame synchronization. This signal is a 8 kHz signal for frame synchronization. The front edge gives the time reference of the first bit in the frame.
DEN_X	10	I	Transmit Data Enable. In TE mode, this pin is a normally low input pulsing high to indicate the active bit times for D channel transmit at the D_{OUT} pin. It is gated with CLK and the internal time-slot strobes to control the shifting of data from the HDLC controller to an S interface device.
SERIAL PORT IN NON-GCI MODES			
D_{OUT}	15	O	Data Output for B and D channels, clocked by CLK input.
D_{IN}	12	I	Data Input for B and D channels, clocked by CLK.
CLK	11	I	Data Clock, which determines the data shift rate. Two modes: Single or double bit rate.
FS	13	I	Frame synchronization. Used in the time-division multiplexed mode, the rising edge gives the time reference of the first bit of the 8 kHz frame.
DEN_X	10	I	Transmit Data Enable. When high, enables the data at DOUT.

Functional Description

MICROPROCESSOR PORT

Any of 3 microprocessor bus interface standards may be selected by strapping the MULT and I/M pins. Multiplexed bus mode is selected by strapping MULT = 1; Intel/National bus compatibility can then be selected by I/M = 1, or Motorola bus compatibility is selected by strapping I/M = 0. The non-multiplexed Motorola bus mode is selected by strapping MULT = 0. Table I lists the registers which are accessed via the microprocessor port.

DATA FIFOs

The transmit and receive data paths between the microprocessor port and the HDLC section are buffered by means of independent 64-byte FIFOs. Each FIFO is accessible in blocks of up to 32 bytes, and demands service from the μP by generating interrupts. The data transferred through the FIFOs always consists of the address field, control field and information field of each HDLC packet (frame). In the receive direction a status byte is also appended at the end of the frame, containing indicators such as CRC pass/fail, frame abort and data overflow.

SERIAL PORT

This is a synchronous interface consisting of a single data shift clock input, CLK, transmit data output D_{OUT} and receive data input D_{IN}. CLK may run with either 1 or 2 cycles per data bit, selected via register CR2. Data passes between the Serial Port and the FIFOs either via the HDLC section or without HDLC processing (HDLC Bypass), selected via the MODE register. Data is transferred lsb first.

Two additional control input pins are provided. FS is a frame sync input which defines the start of the 8 kHz frame when any of the time-division multiplexed formats (including GCI) are used. DEN_x is an enable/disable control for transmit data at D_{OUT}, for use in ISDN Terminal applications when interfacing the device to the 16 kb/s D channel of an S/T Interface Transceiver (e.g., TP3420/1). The transceiver must exercise flow control for D channel access contention resolution at the S/T interface (for the Passive Bus). Transmit data shifting at D_{OUT} is inhibited when DEN_x is pulled low and enabled when DEN_x is pulled high.

Four different modes are available for data at the serial interface, with selection via register CR1. In the TDM and GCI modes, when the device is operating in a B channel (8-bit time-slot), the data may occupy the complete time-slot at 64 kb/s, or only a partial time-slot for data rates <64 kb/s. Options available are:

- 56 kb/s in the 7 msb's of the time-slot (lsb is not used);
- 16 kb/s, programmable into a 2-bit sub-slot in bits 1 and 2, 3 and 4, 5 and 6 or 7 and 8 of the time-slot;
- 8 kb/s using any 1 bit of the time-slot.

Selection is made in registers CR1 and TSR.

Continuous Mode

In this mode, there is no time-division multiplexing of data, and the FS input is not used. Data may be shifted at rates up to 4 Mb/s continuously in this mode (although the microprocessor routines to service the FIFOs may limit the net throughput to less than this). The DENx input must be pulled high to enable the D_{OUT} pin.

Time-Division Multiplexed (TDM) Mode

In this mode the FS input defines the start of an 8 kHz frame which may consist of up to 64 8-bit time-slots (with CLK shifting at up to 4.096 Mb/s). A programmable time-slot assignment circuit, programmed via the TSR register, allows the data to be programmed to shift only during one of these time-slots (same slot for transmit and receive).

GCI (General Circuit Interface) Mode

When the GCI format is used, the FS input is used for 8 kHz frame synchronization; the data shift clock at CLK must be selected to run at 2 cycles per data bit in register CR2. *Figure 3* shows the GCI frame format, which may have from 1 to 8 GCI channels multiplexed in the frame. The HDLC controller may use either of the B channels or the D channel in any of these GCI channels, selected in the TSR register. In addition, the device provides transmit and receive registers for access to the GCI Monitor channel and Command/Indicate channel. For applications which do not require HDLC, the device may function as a GCI formatter and controller for the Monitor and C/I channels by disabling the HDLC sections (see MODE register). For more details, see the section on GCI Registers.

GCI-SCIT (Special Circuit Interface for Terminals) Mode

The GCI-SCIT mode is an extension of the GCI mode for use in ISDN Terminals, with 3 GCI channels as shown in *Figures 3* and *4*. Channel 0 is used for 2B + D access to the Layer 1 interface and control of the transceiver, and channels 1 and 2 are added for local control of other devices. For more details, see the section on GCI Registers.

HDLC TRANSMITTER

A typical HDLC frame consists of the following data fields:

Flag	Address	Control	Information	CRC	Flag

The HDLC transmit section performs the following functions:

— Flag Generation

A flag (01111110) is generated to delimit the beginning and end of every frame; as an option, the closing flag of one frame may be shared with the opening flag of the next, selected via the MODE register.

— Zero Insertion

A zero is inserted after 5 consecutive ones within an HDLC frame (between flags) to prevent emulation of the flag;

— CRC Generation

The 2-byte CRC (Cyclic Redundancy Check) field transmitted in the frame is generated according to the polynominal $X^{16} + X^{12} + X^5 + 1$;

— Abort Sequence Generator

An HDLC frame may be terminated with an abort sequence under microprocessor control (see CMDR register).

— Interframe Fill

Flags or idle (consecutive ones) may be transmitted during the interframe time (see MODE register).

Functional Description (Continued)

HDLC RECEIVER

The HDLC receive section performs the following functions and reports status on received frames in the RFIFO register:

— Flag Detection

Opening and closing flags (01111110) are detected; shared opening and closing flags are acceptable.

— Zero Deletion

A zero following 5 consecutive ones within the frame is deleted;

— Address Field Recognition

An address filter, with either 1 or 2 bytes, may be selected to determine if a received HDLC frame is accepted or rejected based on the contents of the HDLC address field. Up to 4 SAPI values (0, 63 and 2 user programmable) and/or 3 TEI values (127 and 2 user programmable) may be selected (see registers ACA, ACB, ACC, ACD and ACE). The complete address field is also passed to the RFIFO for address filtering in the μP.

— CRC Checking

The CRC is recalculated on the received frame and compared with the received CRC according to the polynominal $X^{16} + X^{12} + X^5 + 1$;

— Checking for Idle

Fifteen or more consecutive ones are interpreted as "idle";

— Minimum Length Checking.

Register Descriptions

Registers in the TP3451 are accessed via the Microprocessor Port using the addresses shown in Table I. Tables II and III then show how Register CR1 configures the various channels at the Serial Port.

TABLE I. Register Address Map

Address Hex	Read Register Name	Write Register Name
CONFIGURATION REGISTERS		
2B	CR1 (Serial Port)	CR1 (Serial Port)
3E	CR2 (Serial Port)	CR2 (Serial Port)
25		TSR (Time-Slot Register)
HDLC CONTROL REGISTERS		
00	RFIFO	XFIFO
23	STAR (General Status)	CMDR (Command Register)
24	MODE	MODE (HDLC Modes)
25	RFBC (Receive Frame Byte Counter)	
26	ACA (Address Checking)	ACA (Address Checking)
27	ACB	ACB (SAPI x)
28	ACC	ACC (SAPI y)
29	ACD	ACD (TEI a)
2A	ACE	ACE (TEI b)
STATUS REGISTERS WHICH GENERATE INTERRUPTS		
20	ISTA0 (HDLC Status)	ISTA0
21	ISTA1 (GCI Status)	ISTA1
22	ISTA2 (GCI Status)	ISTA2
32	—	MASK0
33	—	MASK1
34	—	MASK2
GCI MONITOR AND C/I CHANNEL ACCESS REGISTERS		
2C	CIR1 (Rx C/I Channel)	CIX1 (Tx C/I Channel)
2D	CIR2 (Rx C/I' Channel)	CIX2 (Tx C/I' Prime Channel)
2E	MONR1 (Rx M Channel)	MONX1/0 (Tx M Channel)
2F	—	MONX1/1 (Tx M Channel Last Byte)
30	MONR2 (Rx M' Channel)	MONX2/0 (Tx M' Channel)
31	—	MONX2/1 (Tx M' Channel Last Byte)

Register Description (Continued)

TABLE II. Serial Port Channel Assignment

Serial Port Mode	CR1 Register								C/I		M		16 kb/s D Channel		64 kb/s (Note 1)		CI′		M′		CI″ (CMS)
	TE	MAS/ SSC	CCs	CMS/ SC	PI	VZ D_{OUT}	MDS1	MDS0	CIR1	CIX1	MONR1	MONX1	DR	DX	BR	BX	CIR2	CIX2	MONR2	MONX2	
Continuous	X	X	X	X	X	X	X	0	← HDLC Frame →												
Time-Division Multiplexed	X	See Table III			X	X	0	1					See Table III								
GCI (Not SCIT)	0	See Table III			X	0/1	1	1	D_{IN}	D_{OUT}	D_{IN}	D_{OUT}	See Table III								
GCI-SCIT D Channel Data SCIT Master	1	1	0	0 1 0 1	0 0 1 1	0/1 0/1 0/1 0/1	1	1	D_{IN} D_{IN} D_{IN} D_{IN}	D_{OUT} D_{OUT}* D_{OUT} D_{OUT}*	D_{IN} D_{IN} D_{IN} D_{IN}	D_{OUT} D_{OUT}* D_{OUT} D_{OUT}*	D_{IN} D_{IN} D_{IN} D_{IN}	D_{OUT} D_{OUT}* D_{OUT} D_{OUT}*			D_{OUT} D_{OUT}	D_{IN} D_{IN}	D_{OUT} D_{OUT}	D_{IN} D_{IN}	D_{OUT}* D_{OUT}*
GCI-SCIT D Channel Data SCIT Slave	1	0	0	0 1 0 1	0 0 1 1	0/1 0/1 0/1 0/1	1	1	D_{IN} D_{IN} D_{IN} D_{IN}	D_{OUT} D_{OUT}* D_{OUT} D_{OUT}*			D_{IN} D_{IN} D_{IN} D_{IN}	D_{OUT} D_{OUT}* D_{OUT} D_{OUT}*			D_{IN} D_{IN}	D_{OUT} D_{OUT}	D_{IN} D_{IN}	D_{OUT} D_{OUT}*	D_{OUT}*
GCI-SCIT B Channel Data See also Table III	1	X	1	0 0	0 1	0/1 0/1	1	1	D_{IN} D_{IN}	D_{OUT} D_{OUT}					D_{IN} D_{IN}	D_{OUT} D_{OUT}	D_{IN}	D_{OUT}	D_{IN}	D_{OUT}	

D_{OUT}*: CMS = 1 and access procedure valid on D and C/I channels.

Note 1: See Table III for sub-multiplexing within a 64 kb/s time-slot.

Note 2: *Figures 4* and *5* identify the GCI and GCI-SCIT channels.

Register Descriptions (Continued)

TABLE III. 64 kb/s Time-Slot Submultiplexing

Serial Port Mode	Time-Slot Submultiplex	TSR Register Assignment	CR1 Register		
			MAS/SSC	CCS	CMS/SC
Time-Division Multiplexed	64 kb/s (Complete B Channel)	Select 1/64 Time-Slots	X	1	0
	16 kb/s (2-Bit Sub-Slot)	Select 1/256 Sub-Slots	X	0	0
	8 kb/s in msb of 16 kb/s Sub-Slot	Select 1/256 Sub-Slots	0	0	1
	8 kb/s in lsb of 16 kb/s Sub-Slot	Select 1/256 Sub-Slots	1	0	1
	8 kb/s in lsb of Time-Slot Only	Select 1/64 Time-Slots	0	1	1
	56 kb/ in 7 msb's of Time-Slot	Select 1/64 Time-Slots	1	1	1
GCI and GCI-SCIT	D Channel	Select GCI Channel	X	0	X
	64 kb/s (Complete B Channel)	Select GCI Channel and B1/B2	X	1	0
	8 kb/s in lsb of Time-Slot Only	Select GCI Channel and B1/B2	0	1	1
	56 kb/s in 7 msb/s of Time-Slot	Select GCI Channel and B1/B2	1	1	X

For all registers the MSB is on the left and LSB on the right.

CR1 **Configuration Register 1**

After Reset 00

This register configures the Serial Port. See Tables II and III.

TE	MAS	CCS	CMS/8	PI	VZ DOUT	MDS1	MDS0

TE — TE Mode.

TE = 1: GCI-SCIT mode selected (must also set MDS0/1 = 1).

TE = 0: Not GCI-SCIT mode.

MAS/SSC — In GCI-SCIT mode with D channel operation, this bit selects Master or Slave of the C/I′ and M′ channels. In other modes it selects sub-slots. See Tables II and III.

CCS — Channel Capacity Selection

CCS = 1: 64 kb/s

CCS = 0: 16 kb/s

CMS/SC — In GCI and GCI-SCIT D channel modes, this bit controls if access to the D and C/I channels is restricted to the Master only, or is accessible by Peripheral devices using local contention resolution. In other modes it selects sub-slots. See Tables II and III.

PI — Peripheral Interface (if TE = 1 only)

PI = 1: CIX2, CIR2, MONX2 and MONR2 registers are enabled for GCI-SCIT mode.

PI = 0: CIX2, CIR2, MONX2 and MONR2 registers are disabled.

VZ DOUT — DOUT forced to zero (to power-up the TP3421 SID or other GCI transceiver).

VZ DOUT = 1: If TIM = 0000 is stored in CIX1 register by the μP, and if CIR1 = DI = 1111 (level is inactive), DOUT is forced to zero when FS and CLK are not detected.

VZ DOUT = 0: If TIM = 0000 is stored in CIX1 and if CIR1 = DI, DOUT functions normally.

MDS1 — Mode Bit 1

MDS1 = 1: GCI mode (M and C/I channels are valid).

MDS1 = 0: Time-division multiplexed mode

MDS0 — Mode Bit 0

MDS0 = 1: TDM or GCI mode (FS input and time-slot multiplexers are active).

MDS0 = 0: Continuous mode (no TDM)

CR2 **Configuration Register 2**

After Reset 00

TLP	ADDR	AD3	AD2	AD1	AD0	CRS	TRI

TLP — Test Loop

TLP = 1: The transmitter is internally connected to the receiver; the transmit output is not activated. The Serial Port must be activated to provide the bit clock and frame Synchronization.

TLP = 0: No test loop.

ADDR — GCI Address Recognition in GCI-SCIT mode. If TE = 1 and PI = 1:

ADDR = 1: The first byte of the message received in MONR2 register is compared with AD0/3. If the bytes match, the message is accepted, otherwise it is ignored.

ADDR = 0: The message in MONR2 is always accepted.

AD0/3 — Address 0/3

When PI = 1, these 4 bits are the GCI address of the device.

AD0/2 — Address bit used by the access procedure to D and C/I channels (TE = CMS = CCS = 1)

CRS — Clock Rate Selection

CRS = 1: Clock frequency is twice the data rate; (GCI).

CRS = 0: Clock frequency and data rate are identical.

TRI — TRI-STATE®

TRI = 1: DOUT is a TRI-STATE output

TRI = 0: DOUT is open drain output

Register Descriptions (Continued)

TSR **Time Slot Register**

After Reset 00

See also Table III.

TSR7	TSR6	TSR5	TSR4	TSR3	TSR2	TSR1	TSR0

In TDM Mode:
(MDS1 = 0 in CRI Register)

a) CCS = 1 in CRI Reg. (64 kbit/s)

Then: TSR2/7 select time-slot relative to FS input (from 0 to 63)

b) CCS = 0 in CRI Reg. (16 kbit/s)

Then: TSR0/7 select 2-bit sub-slot relative to FS input (from 0 to 255).

In GCI mode (MDS1 = 1 in CRI Register):

a) CCS = 1 in CRI Reg. (64 kbit/s)

Then: TSR2 selects B1 or B2:

TSR4/6 select GCI channel (from 0 to 7)

b) CCS = 0 in CRI Reg. (16 kbit/s)

Then: TSR4/6 select GCI channel (from 0 to 7) in D channel.

MODE **HDLC Mode Register**

After Reset 00

DMA	FL1	FL0	ITF	RAC	CAC	NHF	FLA

DMA — DMA Interface

DMA = 1: the DMA interface is active

FL1/0 — HDLC Frame Length

Minimum frame length accepted:

	FL1	FL0
3 bytes	0	0
4 bytes	0	1
5 bytes	1	0
6 bytes	1	1

ITF — Interframe Time Fill

ITF = 1: Flags are transmitted

ITF = 0: IDLE is transmitted

RAC — Receiver Active

RAC = 1: Receiver is enabled

RAC = 0: Receiver is disabled

CAC — Channel Activation

CAC = 1: Receiver and transmitter are active

CAC = 0: Receiver and transmitter are inactive

NHF — HDLC Function Select

NHF = 1: HDLC function disabled (Bypass mode)

FLA — Flag

FLA = 1: Shared flags are transmitted between HDLC frames

FLA = 0: Transmit two flags between HDLC frames

CMDR **Command Register**

After Reset 00H

XHF	XME	RMC	RMD	RHR	XRES	M2RES	M1RES

XHF — Transmit HDLC Frame

Must be set, after loading XFIFO, to start HDLC frame transmission.

XME — Transmit Message End

Must be set when the last byte of the frame is entered in XFIFO.

RMC — Receive Message Complete

Normally used in response to RPF or RME interrupt. Acknowledges that the received frame (or one pool of data) has been read and the corresponding RFIFO is freed.

RMD — Receive Message Delete

May be used in response to RPF or RME interrupt. The entire frame will be ignored by the receiver. The part of frame already stored is deleted.

RHR — Receive HDLC Reset

HDLC receiver is reset.

XRES — Transmit HDLC Reset

HDLC transmitter is reset; XFIFO is cleared and the transmitted frame (if any) is aborted.

M2RES — Monitor 2 Reset

Receive and transmit M′ channel controllers are reset.

M1RES — Monitor 1 Reset

Receive and transmit M′ channel controllers are reset.

FIFOs **RFIFO (Read), XFIFO (Write).**

The address of the currently accessible byte is always 00H. Data is transferred between the FIFOs and the Serial Port with LSB first. When the closing flag of a receive frame is detected, a status byte is added to the data in the RFIFO. This byte is read last and has the following format:

RBC	RDO	CRC	RAB	0	0	0	0

RBC — Receive Byte Count

The length of the received frame is not an integer number of bytes

RDO — Receive Data Overflow

A part of the frame has been lost because the receive FIFO was full

CRC — CRC Check

The received CRC bytes were correct

RAB — Receive Abort

The received frame was aborted

A status byte equal to A0H indicates a correctly received frame (for LAPD).

Register Descriptions (Continued)

ISTA0 **Interrupt Status Register 0**

After Reset 10H

The $\overline{INT}$ pin is activated only when any of the unmasked bits in this register is set = 1. The software should make a copy of this register, since it must be cleared by writing 00H before writing to any of the HDLC and/or GCI registers.

RME	RPF	RFO	XPR	XDU	EXI2	EXI1	0

RME Receive Message End

One complete frame of length less than or equal to 32 bytes, or the last part of a frame of length greater than 32 bytes is stored in the RFIFO.

RPF Receive Pool Full

32 bytes of a frame are in RFIFO. The frame is not yet completely received.

RFO Receive Frame Overflow

A complete frame was lost because no storage space was available in the RFIFO.

XPR Transmit Pool Ready

One data block (32 bytes max) may be entered into the XFIFO.

XDU Transmit Data Underrun

A transmitted frame was terminated with an abort sequence because no data was available for transmission in XFIFO and no XME command was issued. It is not possible to transmit a new frame when this interrupt remains unacknowledged.

EXI1 Extended Interrupt 1

This bit is set if any of the unmasked bits in register ISTA1 is set.

EXI2 Extended Interrupt 2

This bit is set if any of the unmasked bits in register ISTA2 is set.

ISTA1 **Interrupt Status Register 1 (GCI Mode only)**

After Reset 01H

0	0	CIC1	EOM1	XAB1	RMR1	RAB1	XMR1

CIC1 Command/Indicate Change

A change in the contents of CIR1 is detected.

EOM1 End of Message 1 (Monitor Channel)

The last byte of an M channel messge has been received in register MONR1.

XAB1 Monitor Transmit ABORT

The received byte has not been validated in two successive GCI frames. The M channel receiver has sent an ABORT (A bit) to the remote transmitter.

RMR1 Receive Monitor Register

A validated new byte has been received in register MONR1.

RAB1 Receive Abort

The M channel transmitter received an ABORT from the remote receiver.

XMR1 Transmit Monitor Register 1 Ready

A byte can be stored in register MONX1.

ISTA2 **Interrupt Status Register 2 (GCI-SCIT Mode only)**

After Reset 01H

0	0	CIC2	EOM2	XAB2	RMR2	RAB2	XMR2

CIC2 Command/Indicate Change

A change in the contents of CIR2 is detected.

EOM2 End of Message 2 (M′ channel)

The last byte of an M′ channel message has been received in register MONR2.

XAB2 Monitor Transmit ABORT

The received byte has not been validated in two successive GCI frames. The M′ channel receiver has sent an ABORT (A bit) to the remote transmitter.

RMR2 Receiver Monitor Register

A byte has been received in register MONR2.

RAB2 Receive ABORT

The M′ channel transmitter received an ABORT from the remote receiver.

XMR2 Transmit Monitor Register 2 Ready

A byte can be stored in register MONX2.

MASK0 **Interrupt Mask Registers.**

MASK1 After Reset FFH.

MASK2 The three mask registers MASK0, MASK1, MASK2 are associated with the three interrupt registers ISTA0, ISTA1 and ISTA2 respectively.

Each interrupt source in the ISTA registers can be selectively masked by setting to "1" the corresponding bit in the appropriate MASK register. The current status of all interrupt sources, regardless of masking, is indicated when an ISTA register is read by the microprocessor. However, only unmasked sources can generate an interrupt by pulling $\overline{INT}$ low.

STAR **Status Register**

After Reset 40H

XDOV	XFW	IDLE	RLA	DC10	0	0	0

XDOV Transmit Data Overflow

More than 32 bytes are queued in the XFIFO.

XFW Transmit FIFO Write Enable

Data can be entered into the XFIFO.

IDLE IDLE State

15 or more consecutive ones have been detected at DIN.

RLA Receive Line Active

RLA = 1: Indicates an HDLC frame is being received on the line

RLA = 0: Receive channel is idle.

DCIO D and C/I Channels Occupied

DCIO = 1: D and C/I Channels are busy.

Register Descriptions (Continued)

RFBC **Receive Frame Byte Counter**

After Reset 00

See also Table IV.

RDC7	RDC6	RDC5	RDC4	RDC3	RDC2	RDC1	RDC0

RDC 0/7 Receive Data Count

Total number of bytes in the received HDLC frame (without CRC).

RDC 0/4 Indicate the number of bytes in the current block available in RFIFO (m).

RDC 5/7 Indicate the number of 32 byte blocks received (n). If the frame exceeds 223 bytes, RDC 5/7 hold the value "111", and only RCD 0/4 continue to count modulo 32.

The contents of the register are valid after an RME interrupt. The μP must read n + 1 bytes to transfer the received data plus the status byte into memory.

TABLE IV. Receive Frame Byte Counter Operation

Number of Bytes in the Frame Received (without CRC)	RFBC Register		Number of 32 Byte Blocks Previously Read by the μP
	765	43210	
N (Note 1)	n	m	n
1 Min	000	00001	0
2	000	00010	0
3	000	00011	0
30	000	11110	0
31	000	11111	0
32	001	00000	1
33	001	00001	1
62	001	11110	1
63	001	11111	1
64	010	00000	2
222	110	11110	6
223	110	11111	6
224	111	00000	7
256	111	00000	7
257	111	00001	7
	111	—	7

Note 1: For received frames up to 255 bytes in length, N = 32 n + m. Longer frames may be received but only m will be valid; n will stop counting at 111.

ACA **Address Check Register A**

After Reset 00

CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0

CA0 SAPI 0 is recognized if CA0 = 1

CA1 SAPI 63 is recognized if CA1 = 1

CA2 SAPI x is recognized if CA2 = 1

CA3 SAPI y is recognized if CA3 = 1

CA4 TEI 127 is recognized if CA4 = 1

CA5 TEI a is recognized if CA5 = 1

CA6 TEI b is recognized if CA6 = 1

CA7 Address Filter Active if CA7 = 1

If CA0-3 all = 0, all received SAPI values are accepted; if any one or more of these bits = 1, only receive addresses matching the stored SAPI(s) are accepted. If CA4-6 all = 0, all received TEI values are accepted; if any one or more of these bits = 1, only receive addresses matching the stored TEI(s) are accepted. To disable all address filtering set CA7 = 0; registers ACB, ACC, ACD and ACE are then inactive and all received address fields are accepted.

ACB **Address Check Register B**

After Reset 00

The contents of ACB indicate the SAPI x value

SAPI	0	0

6 High Order Bits

ACC **Address Check Register C**

After Reset 00

The contents of ACC indicate the SAPI y value

SAPI	0	0

6 High Order Bits

ACD **Address Check Register D**

After Reset 00

The contents of ACD indicate the TEI a value

TEI	0

7 High Order Bits

ACE **Address Check Register E**

After Reset 00

The contents of ACE indicate the TEI b value

TEI	0

7 High Order Bits

CIX1 **Command/Indicate Transmit Register 1**

After Reset FFH

(GCI Selected Only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4 Code to be transmitted in the outgoing GCI C/I channel. C1 bit is transmitted first.

CIR1 Command/Indicate Receive Register 1

After Reset FFH

(GCI Selected Only)

1	1	1	1	C1	C2	C3	C4

C1, C2, C3, C4 Data from the incoming GCI C/I channel. After CIC1 interrupt in ISTA1, the μP must read this register.

CIX2 **Command/Indicate Transmit Register 2**

After Reset FFH

1	1	P1	P2	P3	P4	P5	P6

P1/P6 Code transmitted in the 2nd GCI channel. P1 bit is transmitted first.

Register Descriptions (Continued)

CIR2 **Command/Indicate Receive Register 2**

After Reset 3FH

(GCI-SCIT in TE mode only)

0	0	P1	P2	P3	P4	P5	P6

P1/P6 The contents of the 2nd C/I channel, which are the different requests received from peripherals to local μP. Up to six peripherals can make simultaneous requests. After CIC2 interrupt in ISTA2, the μP must read this register.

MONX1/0 and MONX1/1 **Monitor Transmit Registers**

(GCI Selected Only)

After Reset FFH

M1	M2	M3	M4	M5	M6	M7	M8

After Reset FF.

The data written in MONX1/0 is transmitted in the outgoing GCI Monitor channel according to the GCI transfer protocol. M1 bit is transmitted first. The last byte of the message (or a single-byte message) must be written to register MONX1/1 to complete the M channel handshake. XMR1 interrupt indicates when these registers are ready for the next byte.

MONR1 **Monitor Receive Register 1**

(GCI Selected Only)

After Reset FFH

M1	M2	M3	M4	M5	M6	M7	M8

The data read from MONR1 is the byte received in the Monitor channel according to the GCI transfer protocol. RMR1 interrupt in ISTA1 indicates when a new byte is available in this register.

MONX2/0 and MONX2/1 **Monitor Transmit Registers**

(GCI-SCIT in TE Mode Only)

After Reset FFH

The data written in MONX2/0 is transmitted in the 2nd GCI M′ channel to a peripheral (if PI = MAX = 1 in register CR1). The last byte of the message (or a single-byte message) must be written to register MONX2/1 to complete the M′ channel handshake. XMR2 interrupt indicates when these registers are ready for the next byte.

MONR2 **Monitor Receive Registers**

(GCI-SCIT in TE Mode Only)

After Reset FFH

The data read from MONR2 is the byte received from the M′ channel in the 2nd GCI channel. RMR2 interrupt in ISTA2 indicates when a new byte is available in this register.

Transmit FIFO Operation

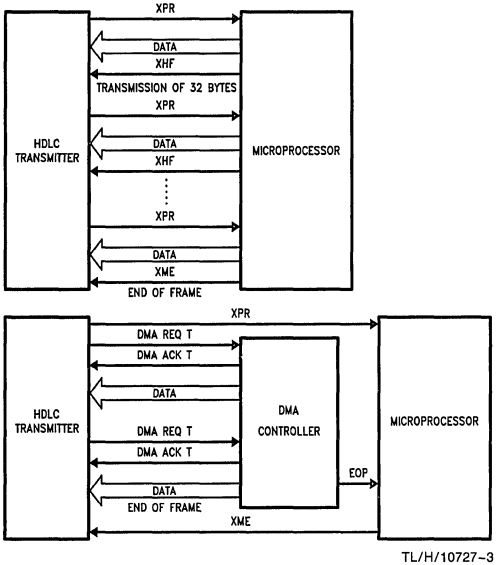
In the transmit direction (towards the HDLC transmitter) the μP may load a block of up to 32 bytes into XFIFO either after first polling the XFW bit in the STAR register, or after an XPR interrupt in ISTA0. To start transmission of a frame the XHF command must be written to the CMDR register. The TP3451 will request another data block by an XPR interrupt if the XFIFO contains less than 32 bytes (unless the XME bit has been set); thus, up to 64 bytes may be stored at any one time.

When the last block of the HDLC frame is loaded into XFIFO, the μP must set the XME bit. After transmission of all remaining XFIFO bytes, the CRC field and closing flag are then added, and the HDLC controller generates a final XPR interrupt.

The XFIFO is implemented as two buffers, each consisting of 32 byte FIFOs. The μP has access to one buffer at a time and passes control to the HDLC hardware by setting the XHF or XME bits in the CMDR register. The HDLC TX hardware empties the buffers and informs the availability of the buffers to the μP via the XPR bit in ISTA0.

The XDOV bit in the STAR register will be set if more than 32 bytes are written into one buffer. The bit will not generate an interrupt but it can be polled by software. If the XFIFO becomes empty while the XME bit has not been set, an abort sequence is generated, followed by interframe fill, and the XDU interrupt is generated. A frame may also be aborted by the XRES command.

Figure 1 shows a typical bus handshake during a transmit HDLC frame.



TL/H/10727–3

FIGURE 1. Bus Handshake during Transmit HDLC Frame

Receive FIFO Operation

In the receive direction, data at the D_{IN} input may be accepted unconditionally, or may be filtered for HDLC address matching if selected in registers ACA, ACB, ACC, ACD and/or ACE. Each received frame which matches one of the enabled addresses, and satisifies the selected minimum length in the MODE register, is sent to the RFIFO with all bytes between the opening flag and the CRC field.

The RFIFO is implemented using eight separate buffers each consisting of eight byte FIFOs. The FIFO buffers are cascaded (or linked in a chain) automatically as required by the length of an incoming packet to form a FIFO up to 64 bytes deep.

Associated with each buffer is a set of registers containing information such as buffer status (full/empty), packet frame status (the packet status byte which can be read after the end of the packet data bytes) and the RFBC (which keeps count of the packet length).

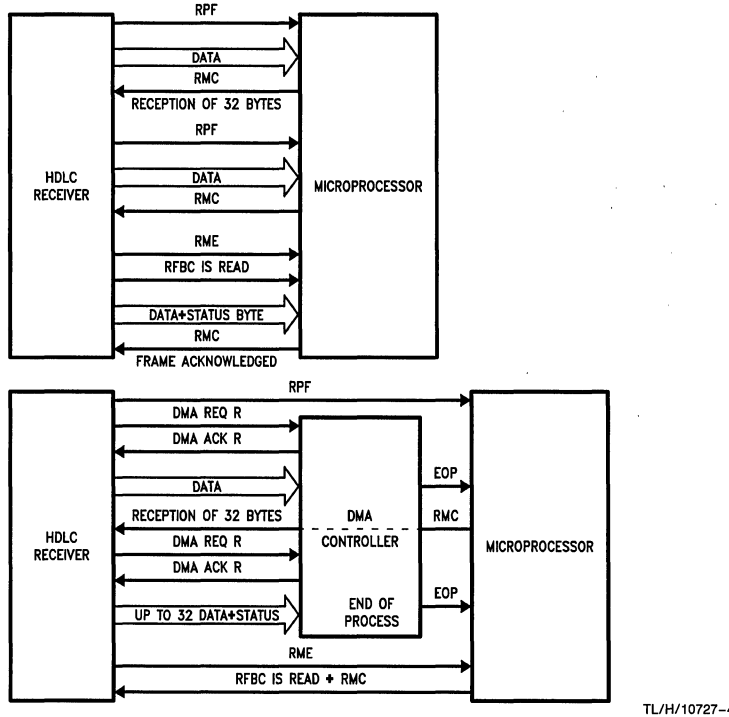
An empty buffer is allocated to an incoming packet, and additional empty buffers (maximum 7) are automatically linked to it as required. After four buffers are full, the RPF Receive Pool Full (a Pool consists of four buffers containing 32 bytes) interrupt is asserted to request service. The detection of a closing flag will freeze the buffer and the associated status registers while asserting the RME interrupt via ISTA0. A short message of 8 bytes or less (including CRC) can be contained in each of the 8 buffers and the complete packet status information can be stored in the 8 sets of associated status registers. Eight RME interrupts may also be queued in this stack.

As data is received, the RFBC keeps track of the number of received bytes even if the packet occupies multiple buffers. RFBC bits 0 to 4 indicate the number of data bytes, m, stored in the current block. At each RFIFO read access by the μP, m is decremented, reaching 0 when the complete block is read. RFBC bits 5 to 7 indicate the total number of 32 byte blocks already received, n. Bits 5 to 7 remain unchanged at each read access. Also, they do not overflow; when a count of n = 7 is reached, a frame length greater than 223 bytes is indicated (see Table IV).

In response to an RME interrupt, the μP must read the RFBC and then read m + 1 bytes from the RFIFO. The μP then releases the buffer(s) by setting the RMC bit in the CMDR register. For a RPF interrupt, the μP must read 32 bytes and then release the four FIFO buffers by setting the RMC bit in the CMDR register. If more than 32 read accesses are performed after an RPF interrupt, the last data byte will be repeated. If more than m + 1 read accesses are performed after an RME interrupt, the packet status byte will be repeated.

The μP can ignore received frame by writing the RMD command to the CMDR register in response to an RPF or RME interrupt. The part of the frame already stored is deleted and the remainder of the frame is ignored. To check if the receive HDLC channel is idle, the IDLE bit in the STAR register can be polled.

Figure 2 shows a typical bus handshake while receiving an HDLC frame.



TL/H/10727–4

FIGURE 2. Bus Handshake during Receive HDLC Frame

FIFO Access Using DMA

The TP3451 has a DMA interface which can be enabled by the DMA bit in the MODE register. The DMA interface is available only when multiplexed bus is selected. When DMA is enabled, the TP3451 asserts $\overline{\text{DMA REQR}}$ or $\overline{\text{DMA REQX}}$ to request an exchange of bytes between the FIFOs and the external memory.

The external DMA controller asserts $\overline{\text{DMA ACKR}}$ or $\overline{\text{DMA ACKX}}$ to access the FIFOs.

These signals are equivalent to the E/DS/RD functions. During DMA access, the $\overline{\text{CS}}$ pin must be inactive (high); AS and E/DS/RD signals can be present. Outside DMA Access, all registers are accessible by the μP except the FIFOs.

FRAME TRANSMISSION

When a 32 byte block is free in XFIFO, $\overline{\text{DMA REQX}}$ goes low and XPR interrupts the μP. The DMA controller can write data in the XFIFO. At the end of the frame, the μP sends XME to the HDLC controller; CRC and closing flag will be sent by the HDLC controller.

FRAME RECEPTION

When one block has been stored in RFIFO, the $\overline{\text{DMA REQR}}$ pin goes low and RPF (or RME) interrupts the μP. The DMA controller reads the RFIFO. After the RME interrupt, the frame length will be available in RFBC register. The block is acknowledged by an RMC command.

GCI Registers

GCI COMMAND/INDICATE PROCEDURE

The two circuits communicating on the GCI interface (e.g., TP3451 and TP3421 SID) send each other a continuous four bit command code in the C/I field.

Receive C/I

The TP3451 stores in every frame the four bits of C/I channel coming from register CIR. This value is compared with the previous one. If a new value appears during two consecutive frames, this new value is loaded in register CIR1 and a CIC1 interrupt is generated.

Transmit C/I

The transmit register CIX1 can be written at any time by the μP. Its content is continuously sent in the C/I channel.

Note: The TIM command (0000) forces a low level on DOUT, if CIR1 = DI (1111) when VZ DOUT = 1, to request FS and CLK.

GCI MONITOR CHANNEL

THE GCI Monitor channel procedure allows bi-directional transmission of control messages in each direction, with acknowledgement using the A bit.

Receive Monitor Channel

An interrupt (bit RMR1 in ISTA1 register) is generated when a new byte is available in register MONR1.

The TP3451 generates an interrupt bit (XAB1 in ISTA1) if it does not receive twice the same byte; it also sends an ABORT to the remote transmitter. An interrupt is also generated (EOM in ISTA1) when it has received an End Of Message indicator via the E bit. Acknowledgement to the remote transmitter is sent if:

— the byte was received twice with the same value:

— the microprocessor reads the previous byte stored in register MONR1.

Transmit Monitor Channel

The TP3451 generates an interrupt (XMR1 in ISTA1) when the MONX1 registers are ready for a message byte. ISTA1 and ISTA0 must be cleared before writing to the MONX1 registers.

A Monitor Channel message must be loaded into register MONX1/0 one byte at a time. When the last message byte is written in register MONX1/1, the device sends the End Of Message indicator (via the E bit) to the remote receiver. If an Abort is received, one interrupt (RAB1) is generated.

GCI-SCIT OPERATION IN M′ AND C/I′ CHANNELS

A procedure is provided which allows bi-directional message transmission between the microprocessor and peripheral devices connected on C/I′ and M′ channels through GCI-SCIT channel 1.

Receive Interrupt on C/I′ (DOUT is an input).

A new value on C/I′ indicates to the TP3451 that one peripheral device in the terminal wants to send a message. Up to six peripherals may generate such an interrupt to the microprocessor.

Each GCI frame, the six bits of the C/I′ channel coming from peripherals are loaded in register CIR′. This value is compared with the previous one and, if a new value appears during two consecutive frames, it is loaded in register CIR2, and a CIC2 interrupt (ISTA2 register) is generated.

The μP may send a message on the M′ channel (DIN becomes an output) to allow the peripheral device to transmit.

Message Transmission on M′ Channel

The TP3451 sets interrupt XMR2 (ISTA2 register) if the MONX2 registers are available. ISTA2 and ISTA0 must be cleared before writing to the MONX2 registers. Writing MONX2 generates a message transmission. When the last byte is stored in register MONX2/1, the device sends the End Of Message indicator (via the E bit) to the remote peripheral.

If an ABORT is received, interrupt RAB2 (ISTA2 register) is generated; the microprocessor must repeat the message.

Message Reception on M′ Channel

Interrupt bit RMR2 (ISTA2 register) is generated when a new byte is available in MONR2 register. Interrupt bit XAB2 (ISTA2 register) is set if it does not read the same byte twice; in this case, it sends an ABORT to the remote peripheral.

The controller generates interrupt bit EOM2 (ISTA2 register) when the End Of Message indicator is received.

GCI Registers (Continued)

ACCESS PROCEDURE TO D AND C/I CHANNELS

Up to eight HDLC controllers may be connected to the D channel and C/I channel in GCI Channel 0. A contention resolution mechanism is provided by CMS (Contention Mode Selection) in GCI Channel 2, see *Figures 3* and *4*. This mechanism allows granting an access without losing data.

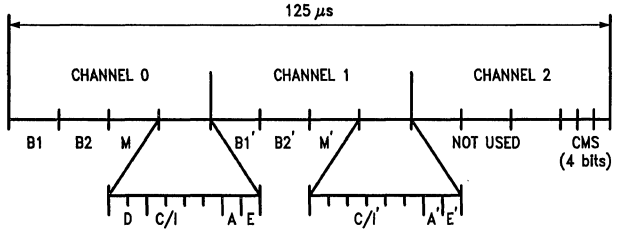
An access request may be generated if CIX1 (Command/Indicate Register 1) contains any code except DI (1111). During the procedure the M channel (with A and E bits) may be used. On input DIN, the GCI controller checks the CMS4 bit, which indicates the status of C/I and D channels.

CMS4 = 1 indicates channels free;
CMS4 = 0 indicates channels busy.

If the channels are free, the HDLC controller starts transmitting its individual address, AD2 on CMS1, AD1 on CMS2, AD0 on CMS3. If an erroneous address is detected, the procedure is terminated immediately. If the complete address can be read without error, the D and C/I channels are occupied and the TP3451 transmits CMS4 = 0. The HDLC controller which has the lowest address has priority over the others.

The access request is withdrawn if the HDLC controller transmits code DI = 1111, and the CMS4 bit is set = 1.

Figure 5 shows flow charts of these procedures.

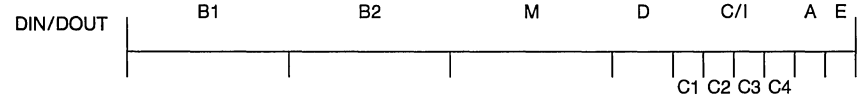


TL/H/10727–5

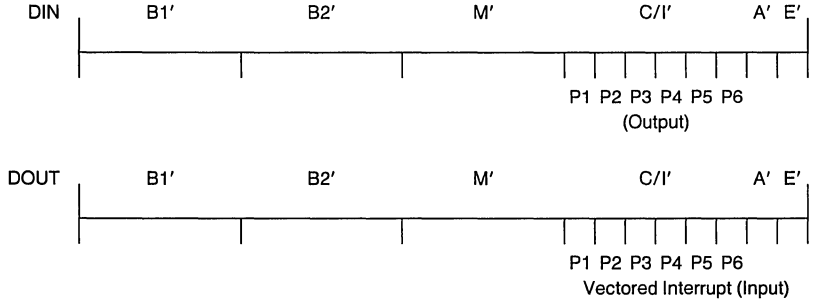
FIGURE 3. GCI-SCIT Frame Format

GCI Registers (Continued)

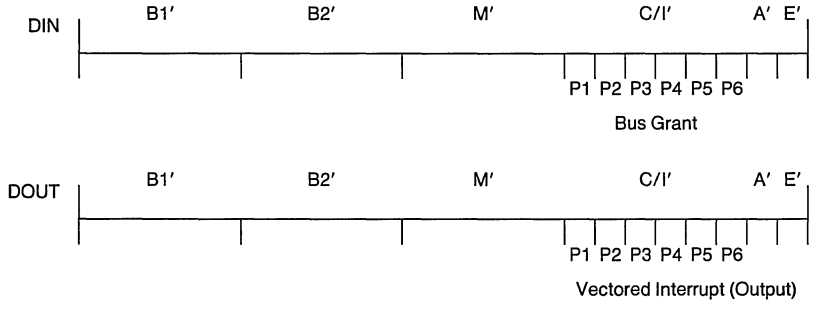
Channel 0



Channel 1, GCI-SCIT Master (MAS = 1 IN CR1)



Channel 1, GCI-SCIT Slave (MAS = 0 IN CR1)



Channel 2

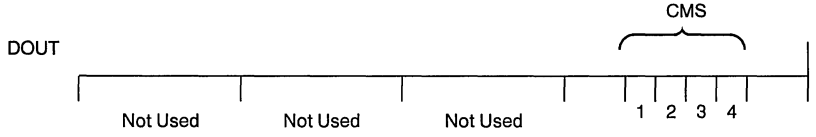
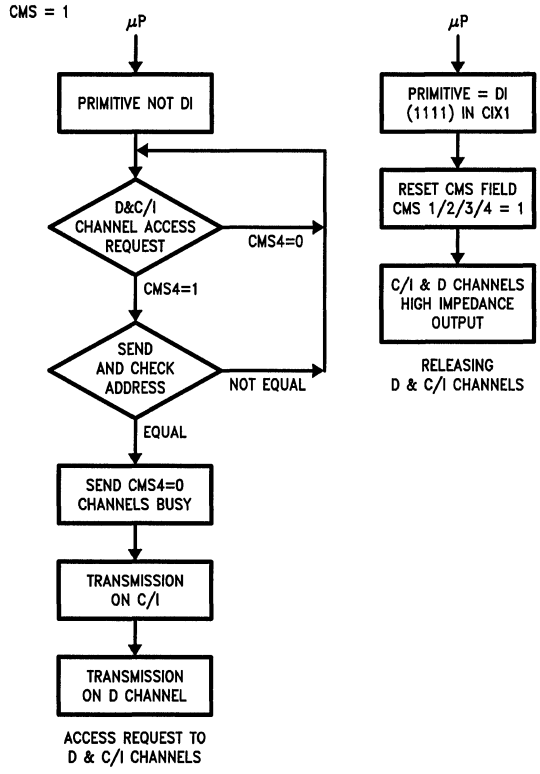


FIGURE 4. GCI-SCIT Channel Format

GCI Registers (Continued)



TL/H/10727–6

FIGURE 5. D and C/I Channels Access Procedure in GCI-SCIT Mode

Applications Information

The TP3451 HDLC controller may be used in a variety of applications, including ISDN TE's and TA's, NT-2's and LT's, both for Basic Rate and Primary Rate.

Figures 6 through *8* illustrate typical TE applications. *Figure 6* shows the TP3451 as the Basic Rate D channel LAPD controller, which may be handling all the traffic for multiple SAPIs (Service Access Point Indicator). The transceiver may be the TP3421 SID or TP3410 UID, in which case GCI mode would be used for the serial interface, or a non-GCI transceiver such as the TP3420 can be used with the programmable TSA on the HDLC controller.

Figure 7 shows a more modular arrangement which takes advantage of the GCI-SCIT mode. One TP3451 handles only the Layer 2 management and signaling logical links (SAPIs 0 and 63), while another module may be added as an option to handle packet data (SAPI 16). The GCI-SCIT mode provides the contention resolution for the 2 (or more) HDLC controllers to access the D channel in GCI channel 0, with one of the devices always assured of using the D channel without loss of data.

Figure 8 can be applied either to a Basic Rate interface, using the TP3421 transceiver, or to a Primary Rate interface with suitable Layer 1 devices. One TP3451 always handles the D channel traffic (at 16 kb/s or 64 kb/s, as appropriate), with another TP3451 assigned to a B channel for X.25 or V.120 circuit-switched data calls. If a call is received from a non-HDLC TE, the HDLC By pass mode can be selected to allow protocol processing in software. A DMA controller may be added as shown to improve data throughput.

In each of these TE/TA applications for Basic Rate, the TP3421 S Interface Device provides the D channel access contention resolution at the S/T interface and exercises local flow control of the D channel HDLC controller by means of the DEN_X pin. This is required only in the direction towards the network; the D channel received from the network is continuously clocked into the D_{IN} input. *Figure 9* illustrates the procedure.

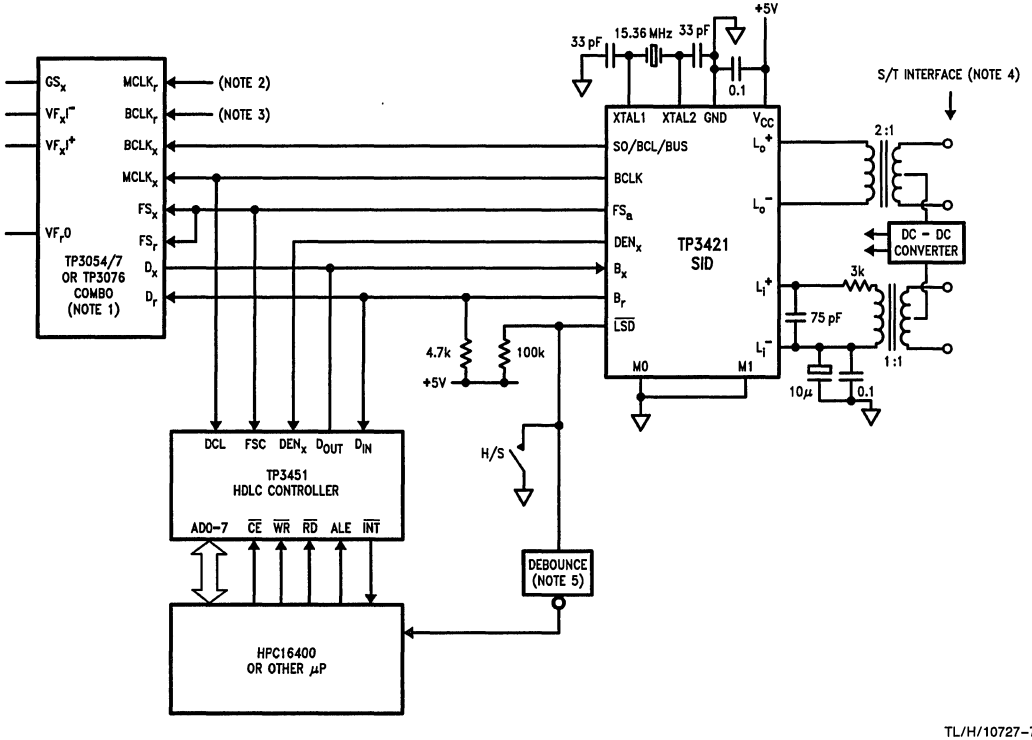
Applications showing the device used for D channel processing in the network are shown in *Figures 10* and *11*. *Figure 10* shows an 8 channel line card with 8 TP3451's multiplexed on the GCI interface, using the GCI channel assigner. Any GCI compatible transceiver may be used, e.g., TP3421 for S/T or TP3410 for U. A GCI compatible exchange circuit may implement the system interface.

Figure 11 shows a centralized processing arrangement. Using a switching network the channels can be concentrated to connect either:

i. Up to 32 64 kb/s channels on a 2 Mb/s highway;

ii. up to 64 64 kb/s channels on a 4 Mb/s highway;

iii. up to 256 Basic Rate D channels on a 4 Mb/s highway.



TL/H/10727–7

Note 1: The TP3076 Combo must be connected to MICROWIRE Interface on the μP to control the programmable gain etc.

Note 2: To power-up the TP3054/7 Combo, MCLK, /PDN must be pulled low.

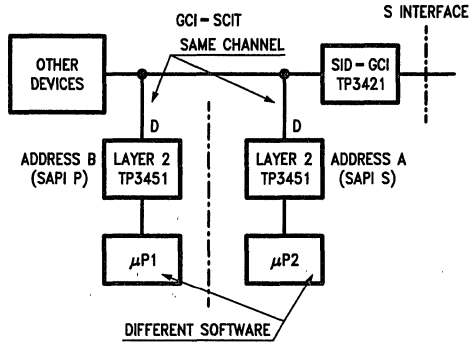
Note 3: For TP3054 (μ-law) leave $BCLK_r$ open-circuit. For TP3057 (A-law) connect $BCLK_r$ low for 1.536 MHz MCLK operation. $BCLK_x$ operates at 768 kHz.

Note 4: See TP3421 User's Manual for Line interface protection.

Note 5: Only necessary if a mechanical hook switch is connected to the NMI input of the HPC.

FIGURE 6. Low Cost ISDN Phone Application

Applications Information (Continued)



TL/H/10727–8

FIGURE 7. LAPB and LAPD Protocol on the Same D Channel Handled with 2 Different HDLC Controllers

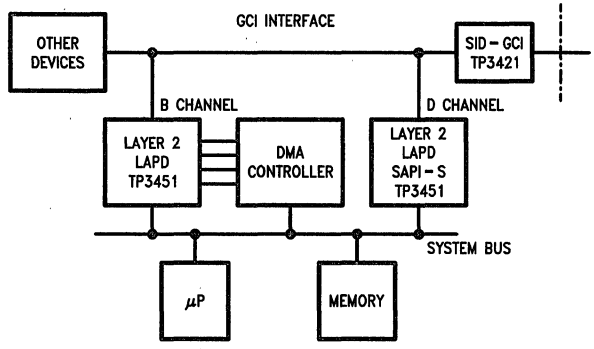


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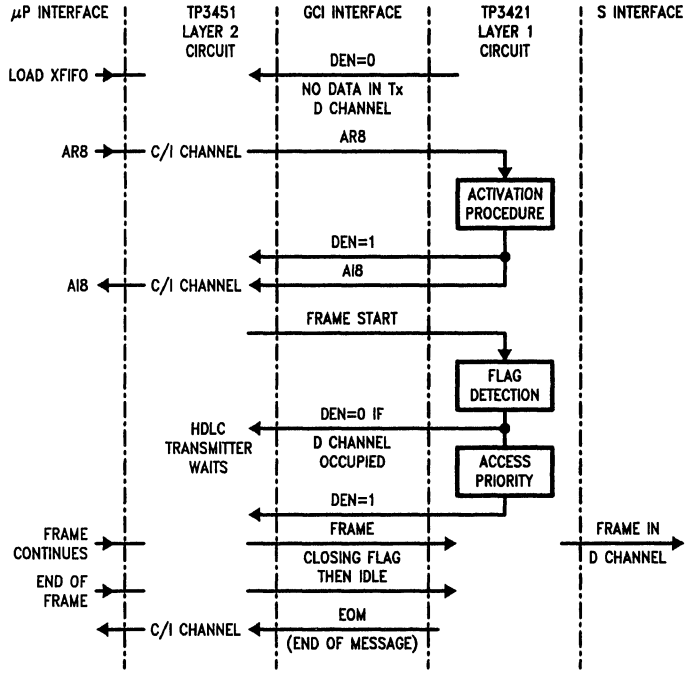
FIGURE 8. LAPB and LAPD Protocol Handling on B and D Channel

Applications Information (Continued)

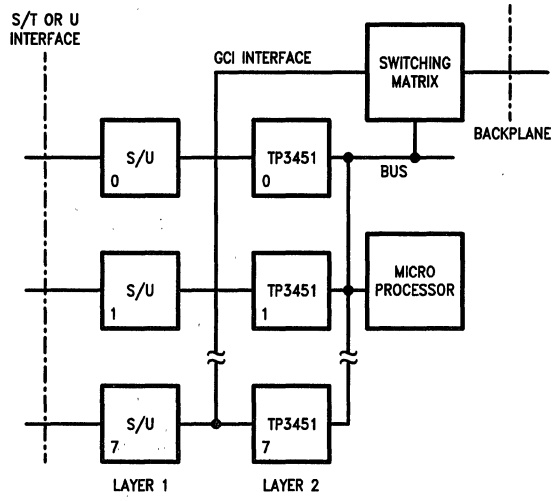


TL/H/10727–10

Note: ARB—Activation Request 8
AIB—Activation Indication with Priority 1

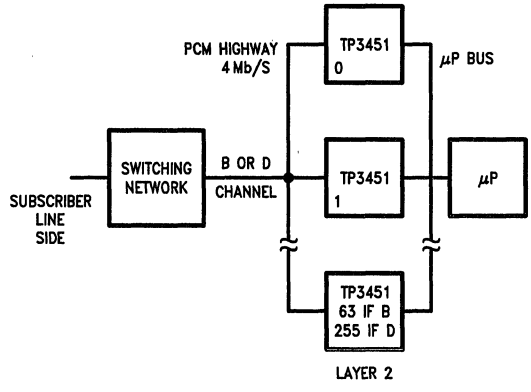
FIGURE 9. Basic Rate Terminal D Channel Transmission Procedure

Applications Information (Continued)



TL/H/10727–11

FIGURE 10. Decentralized D Channel Handling in NT2 or LT



TL/H/10727–12

FIGURE 11. Centralized D Channel Handling in NT2 or LT

Absolute Maximium Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{DD} to V_{SS}	7V
Voltage at any Digital Input	V_{DD} + 1V to V_{SS} −1V
Storage Temp. Range	−65°C to +150°C
Current at any Digital Output	±50 mA
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating to be Determined	

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are electrical testing limits at V_{CC} = 5.0V and T_A = 25°C. All other limits are design goals for V_{CC} = 5.0V ±5% and T_A = 0°C to +70°C. This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	High Level Input Voltage	Maximum Leakage Current: ±10 μA	2	V_{DD} + 0.4	V
V_{IL}	Low Level Input Voltage	Maximum Leakage Current: ±10 μA	V_{SS} − 0.4	0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = −0.4 μA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2 mA		0.45	V
V_{OL} D_{OUT}	Low Level Output Voltage D_{OUT}	I_{OL} = 7 mA		0.45	V
C	Input/Output Capacitance			10	pF
C_{OUT}	Load Capacitance D_{IN}/D_{OUT}			150	pF
	Load Capacitance $\overline{INT}$			150	pF
	Load Capacitance ADD/T			100	pF
I_{DD}	Supply Current				mA

Timing Characteristics

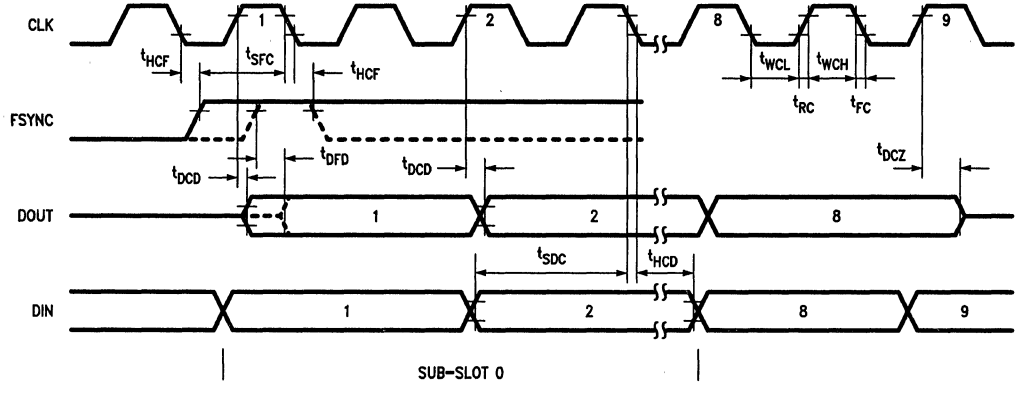
SERIAL PORT (see *Figures 12* and *13*)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
FSync	FS Frequency		0	8		kHz
F_{CLK}	CLK Frequency	GCI Mode; 64 x n x FSync; 1 ≤ n ≤ 8	512		4096	kHz
		Double Clock Mode (Non-GCI); 16 x n x FSync; 1 ≤ n ≤ 64	128		8192	kHz
		Single Clock Mode; 8 x n x FSync; 1 ≤ n ≤ 64	64		4096	kHz
t_{WCH}	Period of CLK High		80			ns
t_{WCL}	Period of CLK Low		80			ns
t_{RC}	Rise Time of CLK				30	ns
t_{FC}	Fall Time of CLK				30	ns
t_{HCF}	Hold Time: CLK to FS		0			ns
t_{SFC}	Set-Up Time: FS to CLK		30			ns
t_{DCD}	Delay Time: CLK High to Data Valid	C_L = 150 pF			80	ns
t_{DCZ}	Delay Time: CLK to Data Disabled		0		80	ns
t_{DFD}	Delay Time: FS High to Data Valid	Applies only if FS Rises Later than CLK Rising Edge. C_L = 150 pF			80	ns
t_{SDC}	Set-Up Time: Data Valid to CLK		20			ns
t_{HCD}	Hold Time: CLK Low to Data Invalid		0			ns

Timing Characteristics (Continued)

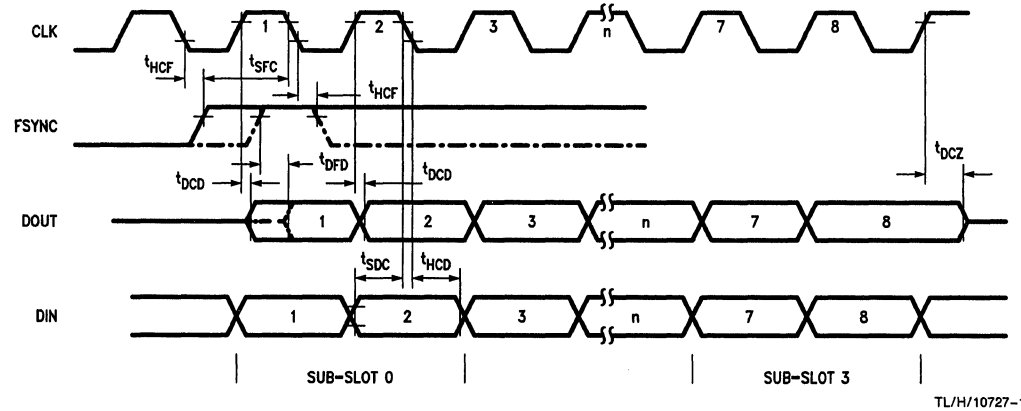
DEN$_X$ Timing (See *Figure 14*)

Symbol	Parameter	Conditions	Min	Max	Units
t_{SDXC}	DEN Setup to CLK		0		ns
t_{HCDX}	DEN Hold from CLK		30		ns



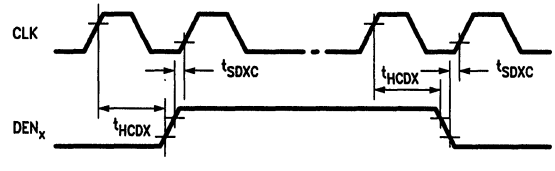
TL/H/10727–13

FIGURE 12. GCI and Double Clock Timing Diagram



TL/H/10727–14

FIGURE 13. Single Clock Timing Diagram



TL/H/10727–15

FIGURE 14. DEN$_X$ Timing

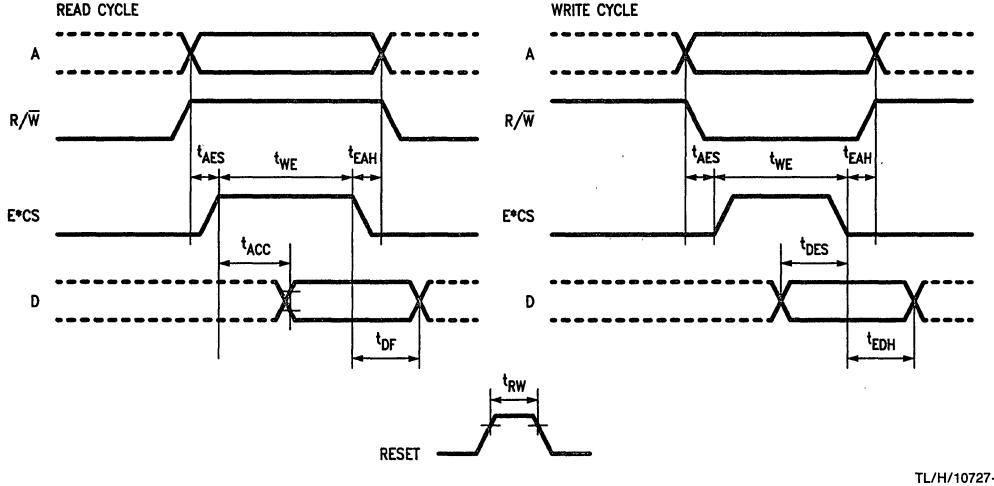
Note: DEN$_X$ normally defines 2-bit periods per frame at D_{OUT} for the D Channel.

Timing Characteristics (Continued)

Microprocessor Bus Timing

READ CYCLE (Non-Multiplexed Mode, *Figure 15*)

Symbol	Parameter	Min	Max	Units
t_{EAH}	Address Hold after E	10		ns
t_{EAH}	R/$\overline{W}$ Hold after E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E. Setup	20		ns
t_{ACC}	Data Delay from E		110	ns
t_{DF}	Output Float Delay		25	ns
t_{WE}	Minimum Width of E	110		ns
WRITE CYCLE (Non-Multiplexed Mode, *Figure 15*)				
t_{EAH}	Address Hold after E	10		ns
t_{EAH}	R/$\overline{W}$ Hold after E	10		ns
t_{AES}	Address to E Setup	20		ns
t_{AES}	R/$\overline{W}$ to E. CS Setup	20		ns
t_{DES}	Data to End of E Setup	35		ns
t_{EDH}	End of E. CS to Data Hold	10		ns
t_{WE}	Minimum Width of E	60		ns
t_{RW}	Minimum Width of Reset	100		ns
t_{RW}	Reset (Load Max 100 pF)	100		ns



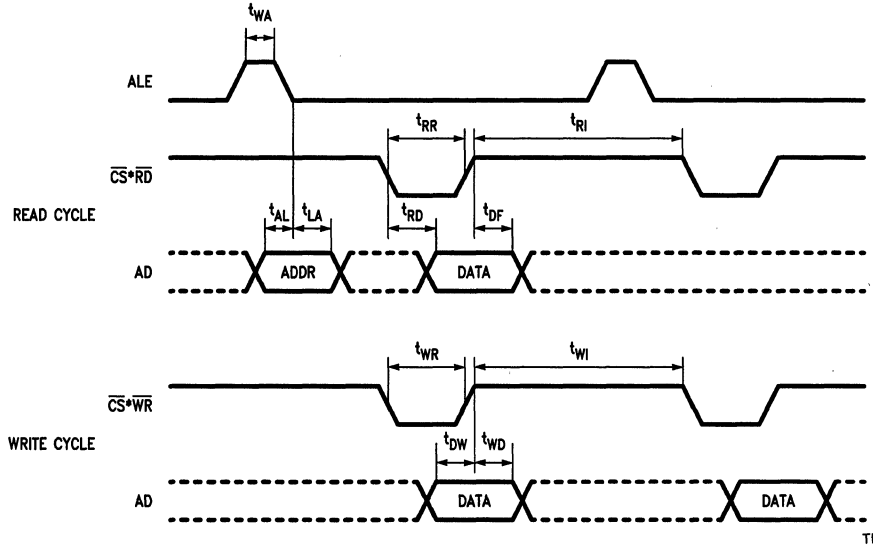
TL/H/10727–16

FIGURE 15. Non-Multiplexed μP Bus Timing

Microprocessor Bus Timing (Continued)

READ CYCLE (Multiplexed Intel/National Mode, *Figure 16*)

Symbol	Parameter	Min	Max	Units
t_{LA}	Address Hold after ALE	10		ns
t_{AL}	Address to ALE Setup	20		ns
t_{RD}	Data Delay from $\overline{RD}$		110	ns
t_{RR}	$\overline{RD}$ Pulse Width	110		ns
t_{DF}	Output Float Delay		25	ns
t_{RI}	$\overline{RD}$ Control Interval	70		ns
t_{WA}	ALE Pulse Width	30		ns
t_{CSS}	$\overline{CE}$ to $\overline{RD}$ or $\overline{WR}$ Set-Up t_{CSS}	20		ns
t_{CSH}	$\overline{CE}$ Hold after $\overline{RD}$ to $\overline{WR}$ t_{CSH}	10		ns
WRITE CYCLE (Multiplexed Intel/National Mode, *Figure 16*)				
t_{WR}	$\overline{WR}$ Pulse Width	60		ns
t_{DW}	Data Setup to $\overline{WR}$	35		ns
t_{WD}	Data Hold after $\overline{WR}$	10		ns
t_{WI}	$\overline{WR}$ Control Interval	70		ns
t_{RW}	Reset Pulse Width	100		ns
RESET CYCLE (Demultiplexed Mode)				
t_{RW}	Reset Pulse Width	100		ns



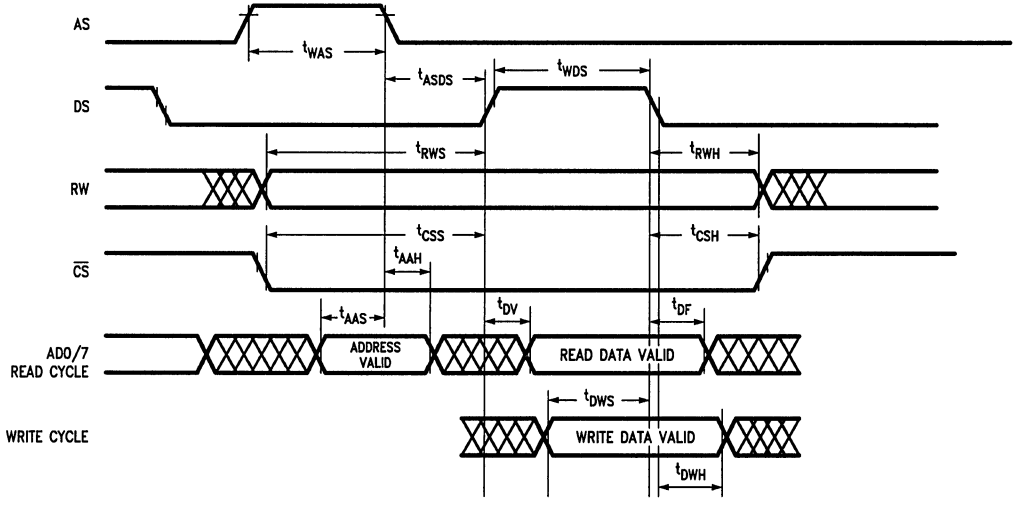
TL/H/10727–17

FIGURE 16. Multiplexed Intel/National μP Bus Timing

Microprocessor Bus Timing (Continued)

MULTIPLEXED MOTOROLA-LIKE μP BUS TIMING *(Figure 17)*

Symbol	Parameter	Min	Max	Units
t_{WAS}	AS Pulse Width	30		ns
t_{WDS}	DS Pulse Width	110		ns
t_{ASDS}	AS Low to DS High	10		ns
t_{RWS}	RW to DS Setup	20		ns
t_{RWH}	RW Hold after DS	10		ns
t_{CSS}	$\overline{CS}$ to DS Setup	20		ns
t_{CSH}	$\overline{CS}$ Hold after DS	10		ns
t_{AAS}	Address to AS Setup	20		ns
t_{AAH}	Address Hold after AS	10		ns
READ CYCLE				
t_{DV}	Data Valid after DS		110	ns
t_{DF}	Output Flat Delay		25	ns
WRITE CYCLE				
t_{DWS}	Data to DS Setup	35		ns
t_{DWH}	Data Hold after DS	10		ns



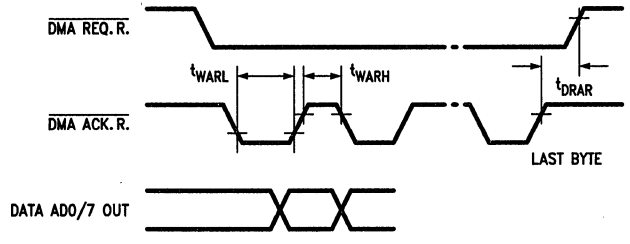
TL/H/10727–18

FIGURE 17. Multiplexed Motorola-Like μP Bus Timing

Microprocessor Bus Timing (Continued)

DMA BUS TIMING (Reception Mode, *Figure 18*)

Symbol	Parameter	Min	Max	Units
t_{ACC}	Data Delay from ACKR		110	ns
t_{DF}	Output Float Delay		25	ns
t_{WARL}	Minimum Width ACKR Low	110		ns
t_{WARH}	Minimum Width ACKR High	70		ns
t_{DRAR}	REQR Delay from ACKR		80	ns

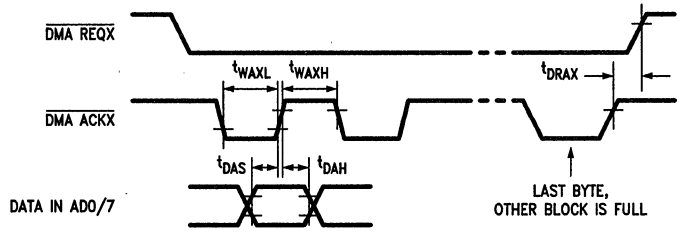


TL/H/10727–19

FIGURE 18. DMA Frame Reception Timing

DMA BUS TIMING (Transmission Mode, *Figure 19*)

Symbol	Parameter	Min	Max	Units
t_{DAS}	Data Setup to ACKX	35		ns
t_{DAH}	Data Hold from ACKX	10		ns
t_{WAXL}	Minimum Width ACKX Low	60		ns
t_{WAXH}	Minimum Width ACKX High	70		ns
t_{DRAX}	REQX Delay from ACKX	80		ns



TL/H/10727–20

FIGURE 19. DMA Frame Transmission Timing

National Semiconductor

PRELIMINARY

TP3460 ISDN R Interface USART

General Description

The TP3460 is a USART which, when connected to a control processor (running the appropriate software) with access to an ISDN B-channel, enables a standards compliant implementation of the CCITT V.110 (ECMA-102) and V.120 Terminal Adaption specifications for serial interface terminals. Conventional UART's and USART's do not comply with many of the requirements of these two standards.

Data rates up to 19.2 kbaud async and 64 kbaud sync are supported.

In asynchronous V.110 mode the TP3460 will compensate the input and output data bandwidths by inserting/deleting stop bits as required, thereby allowing the transmitting terminal to operate at up to 1% overspeed.

In other asynchronous protocols, e.g. V.120, the operation is similar to that of a normal UART where start/stop bits are removed and parity checked.

In synchronous V.110/V.120 modes where the terminal is not synchronous to the ISDN the TP3460, in conjunction with the V.110 software, provides a full implementation of Network Independent Clocking (NIC) to compensate for instantaneous phase differences between the two networks.

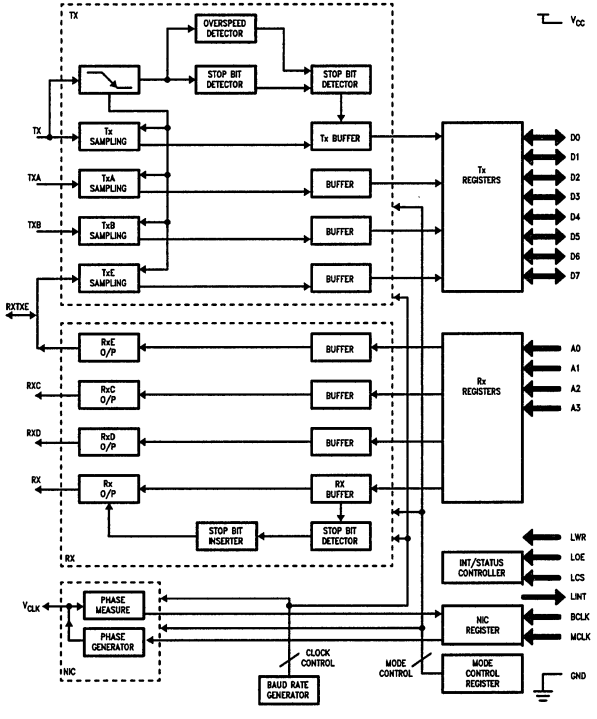
Features

- Full asynchronous and synchronous functions
- Correct V.110 (ECMA-102) start/stop bit processing
- V.110 Co-ordination of S and D bits
- V.120 compatibility
- Network independent clocking
- Asynchronous and synchronous speeds up to 19.2 kbaud
- Synchronous speeds of 48k, 56k and 64k supported
- Synchronous clock master or slave
- Demultiplexed microprocessor bus

Applications

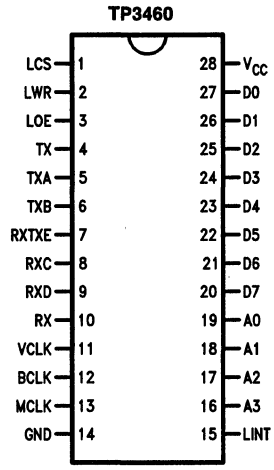
- Multi standard terminal adapters
- Integrated voice/data terminal
- Interworking units between ISDN and non-ISDN
- Host computer connection via Primary Rate Interface

Block Diagram



TL/H/10729–1

Pin Descriptions



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Name	Description
GND	Negative power supply pin, normally 0V (ground). All signals are referenced to this pin.
V_{CC}	Positive power supply input, which must be 5V ± 5%.
D(7:0)	8-bit processor data input/output bus.
A(3:0)	4 address pins for the internal read/write registers.
LWR	This pin controls the direction of the transfer of data between the device and the data bus. When LWR and LCS are both low, the contents are written into the addressed register. When LWR is high and LCS is low a read operation has been selected, control of the data bus is then passed to LOE.
LCS	The chip is selected for a read/write operation when LCS (chip select) is low.
LOE	The output on D(7:0) is enabled when LOE is low.
LINT	Interrupt output, a latched output signal which is normally high-impedance, and goes low when the device requires the processor to service it. LINT will return to a high-impedance state on completion of a status register read.
MCLK	The Master clock input which is programmable to accept either 15–36 MHz or 7.68 MHz.

Name	Description
BCLK	This is the input for the ISDN clock and enables the internally generated baud clock to be synchronized to the ISDN. This clock must be a multiple of 256 kHz and be in the range 256 kHz to 4096 kHz.
Tx	Transmit data for the ISDN B channel via the control processor (receive data from the R-interface terminal). Has internal pull-up resistor to V_{CC}.
Rx	Receive data from the ISDN B channel via the control processor (transmit data to the R-interface terminal).
TxA	Input interchange circuit which is sampled at the same instant as Tx. Has internal pull-up resistor to V_{CC}.
TxB	Input interchange circuit which is sampled at the same instant as Tx. Has internal pull-up resistor to V_{CC}.
RxC	Output interchange circuit which is changed at the same instant as Rx.
RxD	Output interchange circuit which is changed at the same instant as Rx.
RxTxE	Interchange circuit which is selectable either as an output or an input. In both cases the sampling/change instant is identical to the other interchange circuits. Has internal pull-up resistor to V_{CC}.
VCLK	Clock input or output controlling the sampling/change instant for the synchronous applications. If VCLK is programmed as an output then it is synchronous with the BCLK input. Has internal pull-up resistor to V_{CC}.

Functional Description

ASYNCHRONOUS SERIAL INTERFACE

Asynchronous V.110

In V.110 mode (selected via the Mode A Register) the TP3460 functions as the RA0 block. The asynchronous transmitter sets up a virtually transparent path between the Serial Interface and the processor, with the transmitter continually sampling Tx data at the baud rate. The samples (stop and start bits are treated as normal data) are loaded serially into an eight bit buffer.

The sample instant is set to be at the 50% point of a bit. On the start bit edge of each character, the sample point is reset (to ensure accurate sampling).

When the incoming data is running at up to 1% overspeed the TP3460 will delete stop bits (as required), up to a maximum of one out of eight, thus keeping the data rate to the processor at the nominal baud rate.

The receiver reverses the process and monitors the incoming Rx data from the processor to look for missing stop bits. If a missing stop bit is detected then the receiver inserts a stop bit of width $\frac{7}{8}$ and reduces the next seven stop bits by $\frac{1}{8}$, thereby equalizing the input/output bandwidth.

There is no requirement for parity bits to be checked in V.110, however if a parity bit is present then it must be indicated in the Mode A Register so the device can calculate the correct character length.

Asynchronous Non-V.110 Mode

When the TP3460 is used for rate adaption with protocols other than V.110, e.g., V.120, the TP3460 performs as a standard UART. The Asynchronous transmitter strips off the start/stop bits and, for eight bit data, parity can be checked. The character and any parity error are then made available to the processor. The receiver adds on the start/stop bits and regenerates the parity or parity error as required. For seven bit data with parity the parity is not checked but is passed on with the seven data bits in data register.

BREAK DETECTION/GENERATION

V.110 Break Detection

In V.110 the data received on the Tx pin is checked for the presence of a break signal. A break signal is defined as a string of zeroes of length ≥ M where M is the number of bits in the character. The break signal is then conditioned so that the minimum length of break which is passed to the ISDN (V.110 frame) is 2M + 3 zeroes. If the break signal on the TX pin is of length greater than 2M + 3 bits then the whole length of the break signal is passed to the ISDN. The receiver TA should in theory take no action on the break signal, and pass the 2M + 3 zeroes unchanged. However the possibility exists where the receiver TA believes the beginning of the break is a null character with its stop bit deleted. The TA will then insert a stop, creating a null character and shortening the break signal to ≥ M + 4; the break signal however is still greater than the minimum break signal and will be recognized by the receiving terminal.

V.120 Break Detection/Generation

In V.120 the data received on the Tx pin is checked for the presence of a break signal. A break signal is defined as a string of zeroes of length ≥ M where M is the number of bits in the character. The detection of the break generates an interrupt with a Status Register bit signaling the detection (txbrk). The μP should set the Break bit in the frame sent to the ISDN so that the receiver can be instructed to regenerated the break. The TP3460 receiver can be made to generate a break by setting the rxbrk bit in the Par_data Register, upon which the receiver generates a break of 27 zeroes followed by 27 one's. The rxbrk bit is reset automatically by the device.

Interchange Lines

V.110 Interchange Lines

The register structure of the interchange lines is similar to that of the Rx/Tx Data Register. This allows bit-for-bit mapping of transitions on the interchange lines with the data lines, as called for in V.110. However, apart from sampling/clocking at the same time intervals as the Rx/Tx Data Registers, no further manipulation is carried out.

V.120 Interchange Lines

In V.120 mode the interchange circuits behave similarly to those of a UART. Any transition on the Tx Interchange circuits will generate an interrupt. The state of the Tx Interchange lines can be read at any time by reading the Tx_intch Register, and the state of the Rx Interchange lines can be changed at any time by writing to the Rx_intch Register.

SYNCHRONOUS SERIAL INTERFACE

Synchronous V.110/V.120

The operation of the synchronous mode is identical to the asynchronous mode in the way that data is interfaced to the processor. The main difference is that the data I/O is clocked in/out on the clock edges of VCLK. In the synchronous mode, data is transmitted towards the V.24/X.21 interface on the falling edge of VCLK and received on the rising edge of VCLK. In terms of how the data is handled there is no difference between V.110 and V.120, these modes only differ in how the data is presented to the μP. Start bit alignment, stop bit deletion and parity checker do not operate in the synchronous mode.

Master/Slave Clocking

The TP3460 can operate as the receiver or the generator of the data clock. In V.110 mode Network Independent Clocking (NIC) is available to synchronize near and far end clocks. In V.120 the NIC circuit is also available to provide a means of data rate equalization (method not fully defined in V.120).

Network Independent Clocking (NIC)

NIC In V.110

NIC is used when synchronous data signals are received which are not synchronized to the ISDN. In order that both near and far end signals can operate (but asynchronously with the ISDN) the following method is used to allow the passing of relative phase information to allow both near and far end clocks to synchronize themselves dynamically.

(i) The transmitting TA terminal clock (VCLK input) is compared to the ISDN clock, the relative phase is measured, the result is coded into 5% segments and passed to the control processor in PHASE (4:0) bits in the Nic_data Register.

(ii) The processor encodes these 5% segments into 20% increments and inserts them into the 80-bit frame (negative/positive compensation).

(iii) The far end receiving TA decodes the phase shift back to 5% segments and writes this to the TP3460 in PHASE (4:0) bits of the Nic_data Register. The TP3460 then regenerates the output VCLK by comparing it to the ISDN clock and producing the required phase shifted output.

NIC In V.120

The method of clock synchronization in V.120 synchronous modes is not fully defined but is based on monitoring the level to which the receive buffers (μP) are filled and comparing that to the transmit buffers. If both are synchronized then the buffers should fill to precisely the same level, any difference will provide an indication of how much the clock rate should be adjusted. This adjustment can be accomplished by making repeated small adjustments in the phase of the clock (which is derived from the ISDN clock) by using the NIC circuitry.

BAUD RATES

The TP3460 expects the MCLK input to be 15.36 MHz or 7.68 MHz as programmed in the Mode C register, from which it derives the standard baud rates. The appropriate baud rate is selected via Mode B Register from the selection in Table I.

TABLE I. Baud Rates

Baud Rate	Asynchronous	Synchronous	NIC
75	Yes	No	No
150	Yes	No	No
300	Yes	No	No
600	Yes	Yes	Yes
1.2k	Yes	Yes	Yes
2.4k	Yes	Yes	Yes
4.8k	Yes	Yes	Yes
9.6k	Yes	Yes	Yes
12k	Yes	No	No
19.2k	Yes	Yes	Yes
48k	No	Yes	No
56k	No	Yes	No
64k	No	Yes	No

PROCESSOR PARALLEL INTERFACE

The processor interface consists of eight TRI-STATE® bidirectional data lines (D0–D7), four address lines (A0–A3), a read/write control line (LWR), an output enable (LOE), a chip select (LCS) and an interrupt output (LINT). Control of the data lines is defined in Table II.

TABLE II. Processor Control Pins

Mode	LWR	LCS	LOE	I/O
Write	0	0	0	D_{IN}
Write	0	0	1	D_{IN}
—	0	1	0	Hi-Z
—	0	1	1	Hi-Z
Read	1	0	0	D_{OUT}
—	1	0	1	Hi-Z
—	1	1	0	Hi-Z
—	1	1	1	Hi-Z

INTERRUPT GENERATOR

The TP3460 provides a means of signaling to the μP (via LINT and the status register) that its buffers are full/empty and requires service from the μP.

The LINT pin is an open-drain output which goes low when the device requires service. The open-drain output means that several devices can be wired-or and use the same interrupt port, the processor must read the Status Register for confirmation that it was the TP3460 that had generated the interrupt.

If the μP fails to start or complete its service routine for the TP3460 then one or all of the data registers will have been over/under written. There are two flags in the Status Register (txovw, rxunw) to indicate that this has happened.

Depending on the mode of operation, the read of the Status Register (following an interrupt) will signal different actions. In all modes, reading of the Status Register will cause the cancellation of the interrupt.

V.110 Interrupts

In V.110 mode, on reading the Status Register, the **devrdy** flag (device ready) will be set. The status flags of the device can also be read at this point. When the device is ready, the μP can write/read to all data, interchange and NIC registers (or a subset). The μP has up to eight sampled data bits (R-Interface) of time to service the interrupt before the registers will be updated/emptied again.

V.110 Idle Mode

Due to the constant interrupt rate generated in V.110 mode, regardless of the useful data content that is being handled, an idle mode has been included. Idle mode is entered by the device when data on the Tx lines is unchanging and the μP has stopped writing to the Rx Registers (because of unchanging nature of the data being received). The device first flags that it is going to enter idle mode through the Status Register, and if conditions remain unchanged will then cease to generate interrupts. Idle mode is exited by any change on the Tx data lines or a write to any Rx Register. Idle mode operates in V.110 asynchronous mode only. Idle mode can be inhibited via the Mode C register.

V.120 Mode

Unlike V.110, which has only one source of interrupts, V.120 has four. In this manner V.120 behaves very much like a normal UART. The four interrupts are:

(i) **txrdy** A Tx character has been received and is ready to be read.

(ii) **rxrdy** The Rx buffer is empty and ready for another character.

(iii) **intrdy** A Tx interchange circuit has changed state.

(iv) **txbrk** A break signal is present on Tx.

All these interrupts are independent and can occur in any combination. If, however, an interrupt becomes pending while another is being serviced then it is held off until the status register is read and the LINT pin returns to the high impedance state.

REGISTERS

The register organization of the TP3460 is divided into two separate areas, namely the data and control/status. Depending on whether **V.110** or **V.120** mode has been selected, the registers have **dual** meanings.

V.110 Registers

Hex Address	Register	Read/Write
0	Tx_data	Read
1	Rx_data	Read/Write
2	Tx_A	Read
3	Tx_B	Read
4	Rx_C	Read/Write
5	Rx_D	Read/Write
6	Rxtx_E	Read/Write
7	Nic_data	Read/Write
8	Mode_A	Read/Write
9	Mode_B	Read/Write
A	Mode_C	Read/Write
B	Status	Read
F	Mode_D	Read/Write

Tx_data

tx7	tx6	tx5	tx4	tx3	tx2	tx1	tx0

Rx_data

rx7	rx6	rx5	rx4	rx3	rx2	rx1	rx0

Tx_A

txa7	txa6	txa5	txa4	txa3	txa2	txa1	txa0

Tx_B

txb7	txb6	txb5	txb4	txb3	txb2	txb1	txb0

Rx_C

vxc7	vxc6	vxc5	vxc4	vxc3	vxc2	vxc1	vxc0

Rx_D

vxd7	vxd6	vxd5	vxd4	vxd3	vxd2	vxd1	vxd0

Rxtx_e

rxtxe7	rxtxe6	rxtxe5	rxtxe4	rxtxe3	rxtxe2	rxtxe1	rxtxe0

Nic_data

0	0	0	phse4	phse3	phse2	phse1	phse0

Mode_A

lv110	lasync	vmode	data1	data0	parity	polarity	stop

Mode_B

div3	div2	div1	div0	baud3	baud2	baud1	baud0

Mode_C

int	iidle	edir	isbd	isbi	iiovw	iiunw	msel

Mode_D

den	reset	0	0	0	0	loop2	loop1

Status

devrdy	intp	0	txbrk	txica	rxica	txovw	rxunw

V.120 Registers

Hex Address	Register	Read/Write
0	Tx_data	Read
1	Rx_data	Read/Write
2	Tx_intch	Read
3	—	—
4	Rx_intch	Read/Write
5	—	—
6	—	—
7	Par_data	Read/Write
8	Mode_A	Read/Write
9	Mode_B	Read/Write
A	Mode_C	Read/Write
B	Status	Read
F	Mode_D	Read/Write

Tx_data

tx7	tx6	tx5	tx4	tx3	tx2	tx1	tx0

Rx_data

rx7	rx6	rx5	rx4	rx3	rx2	rx1	rx0

Tx_intch

1	1	1	1	1	rxtxe	txb	txa

Rx_intch

0	0	0	0	0	rxtxe	rxd	rxc

Par_data

rxparem	rxbrk	0	phse4	phse3	phse2	phse1	phse0

Mode_A

lv110	lasync	vmode	data1	data0	parity	polarity	stop

Mode_B

div3	div2	div1	div0	baud3	baud2	baud1	baud0

Mode_C

int	0	edir	0	0	0	0	msel

Mode_D

den	reset	0	0	0	0	loop2	loop1

Status

txrdy	rxrdy	intrdy	txbrk	txica	0	txovw	txparerr

Control and Status Registers

Mode_A

msb							lsb
lv110	lasync	vmode	data1	data0	parity	polarity	stop

lv110 Sets the device into either V.110 or V.120 mode.

lv110	Mode
0	V.110
1	V.120

lasync Sets the device into either asynchronous or synchronous mode.

lasync	Mode
0	Asynchronous
1	Synchronous

vmode Defines whether the VCLK pin is a slave of timing (input) or a master of timing (output).

vmode	Mode
0	Input VCLK
1	Output VCLK

data (1:0) Sets the number of data bits in an asynchronous character.

data1	data0	Number of Data Bits
0	0	7
0	1	8
1	0	9*
1	1	—

*Option only valid for V.110 Mode

parity For parity to be selected, the parity bit must be set high.

parity	Mode
0	No Parity
1	Parity

For V.110 mode, the parity bit is only used to determine the number of bits in an asynchronous character.

In the V.120 mode, the Tx circuitry will carry out a parity check and flag any parity error in the Status Register. In the Rx circuitry, a parity bit will be generated which can be transformed to a parity error by setting the rxparerr bit in the Par_data Register. Parity is checked/generated only when there are eight data bits. In the seven data bit case the parity bit is passed to the μP in the Tx_data Register.

polarity Sets the polarity of the parity bit for V.120 mode. (The polarity is not required for the V.110 mode).

polarity	
0	Odd
1	Even

stop Defines the number of stop bits in an asynchronous character.

stop	Number of Stop Bits
0	1
1	2

Mode_B

msb							lsb
div3	div2	div1	div0	baud3	baud2	baud1	baud0

div (3:0) In the synchronous mode, the internal circuitry needs a 256 kHz reference clock. This reference is taken from a divided down BCLK. Div(3:0) sets the divisor of BCLK to generate the 256 kHz reference clock, e.g., if BCLK is 1024 kHz then div(3:0) should be set for a divisor of 4.

div3	div2	div1	div0	divisor
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
0	0	1	1	4
0	1	0	0	5
0	1	0	1	6
0	1	1	0	7
0	1	1	1	8
1	0	0	0	9
1	0	0	1	10
1	0	1	0	11
1	0	1	1	12
1	1	0	0	13
1	1	0	1	14
1	1	1	0	15
1	1	1	1	16

baud(3:0) The R-interface baud rate is set by baud(3:0).

baud3	baud2	baud1	baud0	rate
0	0	0	0	75*
0	0	0	1	150*
0	0	1	0	300*
0	0	1	1	12k*
0	1	0	0	600~
0	1	0	1	1.2k~
0	1	1	0	2.4k~
0	1	1	1	4.8k~
1	0	0	0	9.6k~
1	0	0	1	19.2k~
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	48k^
1	1	1	0	56k^
1	1	1	1	64k^

*Asynchronous mode only
^ Synchronous mode only
~Synchronous and asynchronous modes

Mode_C

msb							lsb
int	iidle	edir	isbd	isbi	iiovw	iiunw	msel

int If int is set, then the TP3460 can be a source of interrupts. It int is low then the interrupt control effectively passes to the iidle bit in the Mode_C Register.

iidle The iidle bit will select the idle mode when low. The idle mode will inhibit interrupts when all the data registers are quiet i.e., the Tx input lines have not changed state for 24 user bits (3 successive interrupts) and the μP has stopped updating the Rx Registers. The iintp (Status Register) bit will then be set indicating that the conditions for idle have been met. If no action is taken by the μP before the point when the next interrupt is due, then the interrupt (and all subsequent interrupts) are turned off. However if at any time data starts changing on the Tx lines or the μP writes to one of the Rx registers then the device will automatically come out of idle mode and start to generate interrupts.

The idle mode does not operate in V.120. Consequently, iidle has no function and the int bit then determines if interrupts are generated.

int	iidle	State
0	0	Turn off interrupts but if data active turn on
0	1	Turn off interrupts
1	0	Interrupts enabled
1	1	Interrupts enabled

edir edir controls whether the interchange pin RxTxE acts as an output or an input.

edir	State
0	Input
1	Output

isbd When this bit is set, the stop bit deletion mechanism (asynchronous mode, Tx direction) is inhibited. If overspeed occurs in the Tx data then a stop bit is deleted immediately without ensuring that it meets the criteria set down in V.110. Isbd operates in V.110 mode only.

isbi When this bit is set, the stop bit insertion (asynchronous mode, Rx direction) is inhibited. Isbi operates in V.110 mode only.

iiovw Inhibit interchange overwrite, iiovw, controls whether an overwrite of the Tx interchange registers will cause the txovw flag in the Status Register to be set, e.g., if the Tx_A Register contains 8 bits which have not been read by the control processor and is overwritten by the transmitter then txovw will be set. Iiovw operates in V.110 mode only.

iiunw Inhibit interchange underwrite, iiunw, controls whether an underwrite of the Tx interchange registers will cause the rxunw flag in the Status Register to be set, e.g., if the device loads the Rxd driver from the Rx_D Register and there has been no control processor write since the previous Rx load then the rxunw bit will be set. Iiunw operates in V.110 mode only.

msel When this bit is set test modes are enabled but not activated.

Mode_D

By setting the den bit in the Mode_D Register, additional control bits become accessible to the μP.

Mode_D behaves like a normal register and can be seen as an extension of the mode registers, its function is to provide additional monitoring functions.

When the den bit is reset all Mode_D functions are automatically terminated.

msb							lsb
den	reset	0	0	0	0	loop2	loop1

den When this bit is set, the other bits in the Mode_D register are enabled.

reset If set, the device will be reset to the power up state, including all μP registers and will force exit from all test modes.

loop2 If set, RX is looped back to TX at R-interface.

loop1 If set, TX is looped back to RX at R-interface.

Status Register in V.110 Mode

msb							lsb
devrdy	iintp	0	txbrk	txica	rxica	txovw	rxunw

devrdy When set, the TP3460 is ready to have its Tx Registers read and its Rx Registers written to. When this flag is set an interrupt is generated. Reading the Status Register will clear the device ready flag and return LINT to the high impedance state.

iintp An inhibit of interrupts is pending. Unless a Tx data change or an Rx Register write operation is carried out before the next interrupt is due, interrupts will be inhibited and the device will go into idle mode.

txbrk Transmitter break of ≥ M bits has been detected. The break detector is only active in asynchronous mode. M = number of bits in a character.

txica The Tx circuitry has lost character alignment due to receiving an incorrectly framed character, i.e., after synchronizing to a start bit edge the start bit failed to validate at the 50% sampling point or the stop bit was not validated (or both). Txica operates in asynchronous mode only.

rxica The Rx circuitry has lost character alignment due to receiving an incorrectly framed character, i.e., a stop bit is missing which does not conform to the criteria defined in V.110 (1 of 8). Rxica operates in asynchronous mode only.

txovw One of the transmit registers has been overwritten.

rxunw An underwrite has occurred in one of the Rx registers.

Status Register in V.120 Mode

msb							lsb
txrdy	rxrdy	intrdy	txbrk	txica	0	txovw	txparerr

txrdy The transmitter has a character ready to be read by the processor.

rxrdy The receiver is ready to send another character.

intrdy One of the Tx interchange circuits has changed state.

txbrk A break signal has been received by the transmitter.

txica The Tx circuitry has lost character alignment due to receiving an incorrectly framed character, i.e., after synchronizing to a start bit edge the start bit failed to validate at the 50% sampling point or the stop bit was not validated (or both). Txica operates in asynchronous mode only.

txovw One of the transmit registers has been overwritten.

txparerr Input transmit character has a parity error.

V.110 Data Registers

Tx_Data

msb							lsb
tx7	tx6	tx5	tx4	tx3	tx2	tx1	tx0

tx(7:0) Contains the last 8 samples from the Tx input pin.

Rx_Data

msb							lsb
rx7	rx6	rx5	rx4	rx3	rx2	rx1	rx0

rx(7:0) Contains the next 8 samples to be output Rx pin.

Tx_A

msb							lsb
txa7	txa6	txa5	txa4	txa3	txa2	txa1	txa0

txa(7:0) Contains the last 8 samples from the interchange input pin TxA. (Sampled at the same instant as Tx.)

Tx_B

msb							lsb
txb7	txb6	txb5	txb4	txb3	txb2	txb1	txb0

txb(7:0) Contains the last 8 samples from the interchange input pin TxB. (Sampled at the same instant as Tx.)

Rx_C

msb							lsb
rxc7	rxc6	rxc5	rxc4	rxc3	rxc2	rxc1	rxc0

rxc(7:0) Contains the next eight bits to be output on the RxC interchange pin. (Output at same instant as Rx.)

Rx_D

msb							lsb
rxd7	rxd6	rxd5	rxd4	rxd3	rxd2	rxd1	rxd0

rxd(7:0) Contains the next eight bits to be output on the RxD interchange pin. (Output at same instant as Rx.)

RxTx_E

msb							lsb
rxtxe7	rxtxe6	rxtxe5	rxtxe4	rxtxe3	rxtxe2	rxtxe1	rxtxe0

rxtxe(7:0) Depending on whether the RxTxE pin has been selected as an input or an output, it contains input data that has been received or is to be transmitted on the RxTxE pin.

Nic_data

msb							lsb
0	0	0	phse4	phse3	phse2	phse1	phse0

phse(4:0) If VCLK is configured as an acceptor of timing (input) then phse(4:0) contains the absolute phase measured between the reference (derived from BCLK) and VCLK in 5% increments. The range of output 0–19 gives a 0% to 95% phase measurement range.

If VCLK is configured as a generator of timing (output) then phse(4:0) must contain the required absolute phase shift in 5% increments. The range of the output 0–19 gives a 0% to 95% phase adjustment. If the input value of phse (4:0) exceeds 19 then the device will generate a phase shift of 95%. The maximum phase jump which can be handled by the NIC circuitry is 25%.

V.120 Data Registers

Tx_data

msb							lsb
tx7	tx6	tx5	tx4	tx3	tx2	tx1	tx0

tx(7:0) Contains the data bits of the last character received on Tx pin.

Rx_data

msb							lsb
rx7	rx6	rx5	rx4	rx3	rx2	rx1	rx0

rx(7:0) Contains the data bits of the next character to be output on the Rx pin.

Tx_intch

msb							lsb
1	1	1	1	1	rxtxe	txb	txa

rxtxe Status of interchange circuit RxTxE.

txb Status of interchange circuit pin TxB.

txa Status of interchange circuit pin TxA.

Rx_intch

msb							lsb
0	0	0	0	0	rxtxe	rxd	rxc

rxtxe The output value of the RxTxE pin. This is only valid when RxTxE is in the output mode, if it is in input mode then the value of RxTxE is ignored.

rxd The output value of the interchange RxD pin.

rxc The output value of the interchange RxC pin.

Par_data

msb							lsb
rxparerr	rxbrk	0	phse4	phse3	phse2	phse1	phse0

rxparerr When active, a parity error is forced in the next Rx character. This bit is reset after each character has been output.

rxbrk When high, the Rx pin is forced to a low for 27 bits after which Rx is forced high for 27 bits. This bit is then reset after the break signal has been output.

phse(4:0) If VCLK is configured as a slave of timing (input) then phse(4:0) contains the absolute phase measured between the reference (derived from BCLK and VCLK) in 5% increments. The range of output 0–19 gives a 0% to 95% phase measurement range.

If VCLK is configured as a master of timing (output) then phse (4:0) in the range 0–19 causes a phase adjustment from 0% to 95% in 5% increments. If the input value of phse(4:0) exceeds 19 then the device will generate a phase shift of 95%. The maximum phase jump which can be handled by the NIC circuitry in a single adjustment is 25%.

POWER ON RESET

The TP3460 has an on-chip Power On Reset (POR) circuit. The POR ensures that all the registers and counters power up correctly into a valid known state. To ensure the POR circuit operates correctly the rise time of the Power Supply (V_{CC}) with respect to GND should not be greater than 10 ms.

The POR states of the μP Registers are:

Address	Register	POR State
0	Tx_data	FF (Hex)
1	Rx_data	FF
2	Tx_a	FF
3	Tx_b	FF
4	Rx_c	FF
5	Rx_d	FF
6	RxTx_e	FF
7	Nic_data	00
8	Mode_a	00
9	Mode_c	00
A	Mode_c	00
B	Status	00
F	Mode_D	00

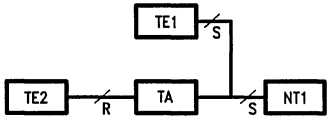
SUMMARY OF V.110/V.120 DIFFERENCES

Parameter	V.110	V.120
Interrupt Sources	devrdy	txrdy rxrdy intrdy txbrk
Stop Bits (async)	Tx: Delete single bit when overspeed Rx: If missing, insert 7/8 Stop Bit and reduce next 7 Stop Bits to 7/8	Tx: Always delete Rx: Always insert
Start Bit (Async)	No alteration	Tx: Always delete Rx: Always insert
Parity (async)	Only required to calculate number of bits in character	Tx: Check Parity, flag if error Rx: Calculate Parity, Forcing Parity Error if required
Data Bits (async)	Only required to calculate number of bits in character	Only required to calculate number of bits in character
Break (async)	Tx: Detect ≥ M Start Bits and force 2M + 3 Start Bits Rx: No alteration (may shorten by inserting Stop Bit)	Tx: Signal Break if Receive ≥ M 0's Rx: Transmit (to Terminal) 27 0's followed by 27 1's
Clocking (sync)	No change	No change

Applications Information

ISDN TERMINAL ADAPTER OVERVIEW

The CCITT reference model, *Figure 1*, illustrates the basic function of a terminal adapter i.e. to connect a non-ISDN terminal (a TE type 2) to the ISDN. V.110 and V.120 are the two CCITT recommended methods for Terminal Adaption.



TL/H/10729–3

TE2: Non ISDN Terminal, i.e., V.24, X.21.

TA: Terminal Adapter

FIGURE 1. ISDN Reference Model

R-INTERFACE CONNECTIONS

DCE Mode

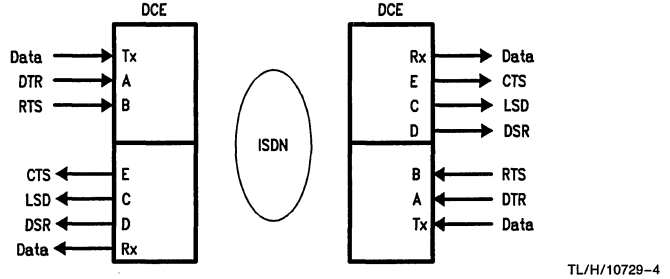
In the normal configuration, the terminal adapter is a DCE (Data Communicating Equipment). In this mode the TP3460 should be configured such that the RxTxE pin is an output. The recommended connection of the DCE interchange circuits is shown in *Figure 2*.

DTE Mode

In the case where the terminal adapter is connected to a modem (interworking), then the TP3460 should be configured as a DTE (Data Terminal Equipment) with the RxTxE pin as an input. The recommended connection of the DTE interchange circuits is shown in *Figure 3*.

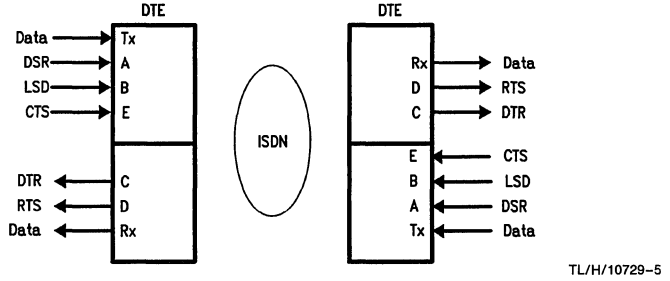
V.110/ECMA-102 TERMINAL ADAPTION

The V.110 method interfaces a TE2 (V.24 or X.21) terminal to the ISDN by means of an 80-bit frame. The frame is connected into the B-channel octets in 4, 2 or 1-bit nibbles depending on the R interface rate. Both synchronous and asynchronous protocols are catered for by using the three stage rate adaption technique, *Figure 4*.



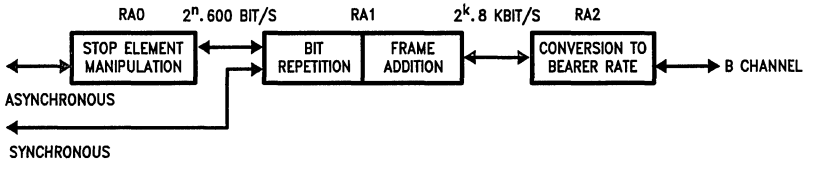
TL/H/10729–4

FIGURE 2. DCE Interchange Connections



TL/H/10729–5

FIGURE 3. DTE Interchange Connections



TL/H/10729–6

FIGURE 4. V.110 Method

RA0

The RA0 function is only required for V.series interfaces and converts asynchronous user data into a synchronous rate of 2^n x 600 bit/s. The format of V.series asynchronous data is a START bit followed by a number of data bits and finally a STOP bit. Unlike a normal UART, RA0 treats START and STOP bits exactly the same as data except for the case of overspeed.

When the terminal is transmitting into the TA at up to 1% overspeed, the input buffers would eventually overflow because the input rate exceeds the output bandwidth. The RA0 detects this scenario and deletes up to one stop bit in every eight characters to equalize the bandwidths.

In the path towards the terminal, the RA0 must detect any valid missing stop bits and re-insert them. When a stop bit has been reinserted, RA0 has more data for the terminal than the user rate will allow. To balance the I/O rates, RA0 shortens the length of the stop bit by 1/8th of a bit for eight characters, thus eliminating the effect of the stop bit insertion. Apart from the overspeed case, RA0 makes no adjustment of the incoming/outgoing data.

RA1

RA1 takes synchronous user data from either the synchronous user interface or the RA0 output and loads it into the 80-bit frame as D-bits. In each 80-bit frame 48 bits are assigned to data and, depending on the user rate, repetition of data can occur. The remaining 32 bits of the frame contain:

(i) Frame alignment information

(ii) Clock speed and relative phasing information

(iii) Interchange circuit and flow control information

RA1 controls the sampling of the interchange circuits and ensures that the data and interchange circuit data retain their relative phase from the local R-Interface (terminal) to the remote R-Interface.

The output/input of RA1 is connected to RA2 and can be at 8k, 16k, or 32 kbits.

RA2

RA2 takes data from RA1 and loads it into the B-channel octet filling either 4, 2 or 1 per octet.

Intermediate Rate kbit/s	No. of Bits Occupied
8	1
16	2
32	4

Therefore, RA2 can multiplex up to 8 different TE's into one B-channel (at the 8 kbit/s intermediate rate).

V.120 TERMINAL ADAPTION

The V.120 method is to take the R-Interface data and convert it into modified LAPD frames using an HDLC protocol.

The Terminal Adaption method is divided into two general categories, protocol sensitive operation for character or message encapsulation and bit transparent operation.

Protocol Sensitive Operation (Asynchronous Mode)

In the direction towards the network, the start and stop bits are removed and parity may be checked. The stripped characters are buffered and transported in modified LAPD frames on a bearer channel. In the direction towards the Terminal, data is reformed into characters by the addition of start and stop bits.

Bit Transparent Operation (Synchronous Mode)

In Bit Transparent Operation the TA encapsulates the bits from the interface at the R-Interface point into V.120 frames as they are received, without modification. These frames are forwarded to a bearer channel. The peer TA removes the bits from the frames and sends them onto the R reference point. No processing or modification of the bits is performed and there is no checking for bit stream errors on the interface at the R reference point.

TERMINAL ADAPTER ARCHITECTURE

The Terminal Adapter utilizes existing TE1 architectures and consists of an ISDN USART (TP3460), a control processor with B-channel access (HPC16400) and an S Interface Device (TP3420). The overall system is shown in *Figure 5*.

A typical application circuit could be configured as shown in *Figure 6*.

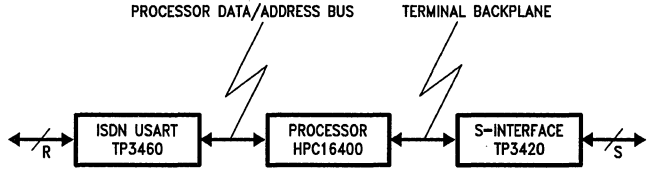
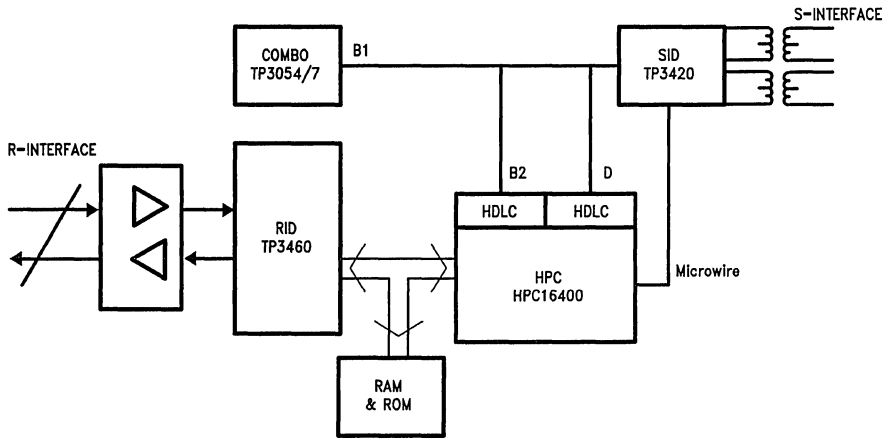


FIGURE 5. Terminal Adapter Architecture



TL/H/10729–8

FIGURE 6. Typical Application Circuit

V.110 Terminal Adapter

The V.110 TA operation is partitioned between the TP3460 and the control processor. The TP3460 functions are shown below with the remaining functions being assigned to the processor.

(i) RA0 including stop bit deletion/insertion
(ii) Tx and Rx sampling
(iii) Interchange circuit sampling with retention of relative phasing with data
(iv) Synchronous clock I/O
(v) Network Independent Clocking

V.120 Terminal Adapter

The V.120 TA operation is partitioned between the TP3460 and the control processor. The TP3460 functions are shown below with the remaining functions being assigned to the processor.

(i) Start/Stop bit removal
(ii) Tx and Rx sampling
(iii) Parity check/generation
(iv) Interchange circuit sampling
(v) Synchronous clock I/O
(vi) Use of NIC circuit to equalize data I/O rates (optional)

Device Electrical Specifications

ABSOLUTE MAXIMUM RATINGS

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V_{CC} to GND	7V
Input Voltage	$-0.3V$ to $V_{CC} + 0.3V$
Storage Temperature Range	$-65°C$ to $+150°C$
Lead Temperature (Soldering, 10 Sec.)	300°C

ELECTRICAL CHARACTERISTICS

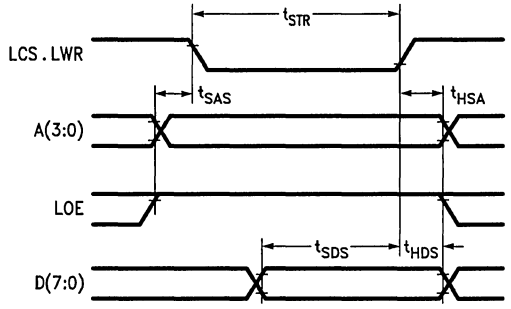
Unless otherwise noted, limits printed in **BOLD** characters are electrical testing limits at $V_{CC} = 5.0V$ and $T_A = 25°$. All other limits are design goals for $V_{CC} = 5.0V \pm 5\%$ and $T_A = 0$ to 70°C. This data sheet is still preliminary and parameter limits are not indicative of characterization data with respect to power supply or temperature variations. Please contact your National Semiconductor Sales Office for the most current product information.

Symbol	Parameter	Conditions	Limits		Units
			Min	Max	
V_{IL}	Input Low Voltage	All Inputs		0.8	V
V_{IH}	Input High Voltage	All Inputs	2.0		V
V_{OL}	Output Low Voltage	Rx, RxC, RxD, RxTxE, VCLK: $I_{OL} = 1$ mA, D(7:0), LINT: $I_{OL} = 2$ mA		0.4	V
V_{OH}	Output High Voltage	Rx, RxC, RxD, RxTxE VCLK: $I_{OH} = 1$ mA, D(7:0): $I_{OH} = 2$ mA	3.7		V
I_{IH}	High Level Input Current	All Inputs		10	μA
I_{IL}	Low Level Input Current	All except Tx, TxA, TxB, RxTxE, VCLK Tx, TxA, TxB, RxTxE, VCLK		−10 −150	μA μA
I_{OZ}	Output Curent in Hi-Z	D(7:0), LINT		±10	μA
I_{CC}	Dynamic Supply Current			7	mA

TIMING CHARACTERISTICS

Symbol	Parameter	Conditions	Typ	Limits		Units
				Min	Max	
f_{MCLK}	Master Clock Frequency	msel = 0	15.36			MHz
		msel = 1	7.68			
f_{BCLK}	Bit Clock Frequency	n x 256 where n = 1 to 16 as defined by div(3:0)		256	4096	kHz
t_{STR}	μP Strobe Width	When MCLK is 15.36 MHz		70		ns
		When MCLK is 7.68 MHz		140		
t_{SAS}	Address Setup Time			10		ns
t_{HSA}	Address Hold Time			10		ns
t_{SDS}	Data Setup Time			40		ns
t_{HDS}	Data Hold Time			10		ns
t_{DV}	Data Valid Delay				70	ns
t_{DZ}	Data TRI-STATE Delay				20	ns
t_{RV}	Rx Output Delay	Synchronous Mode Only			100	ns
t_{STV}	Tx Setup Time	Synchronous Mode Only		50		ns
t_{HTV}	Tx Hold Time	Synchronous Mode Only		50		ns

TIMING DIAGRAMS



TL/H/10729–9

FIGURE 7. μP Write Operation

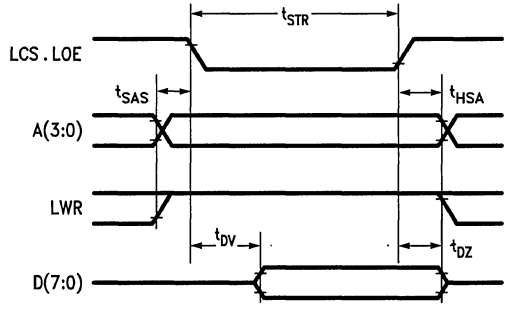


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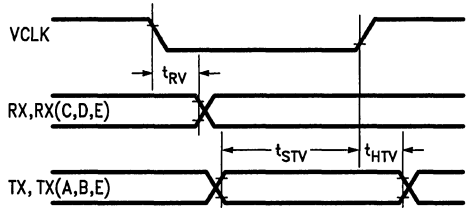
FIGURE 8. μP Read Operation



TL/H/10729–11

FIGURE 9. Serial Interface

National Semiconductor

ADVANCE INFORMATION

TP34XX MICROWIRE™ Interface Device (MID)

General Description

The MICROWIRE™ Interface Device MID gives a general microprocessor (such as National 32000 series processors, Intel 80C188, 80C86 or 80286, Motorola 6800 and 68000 family of processors) the ability to communicate efficiently with Microwire based NSC peripherals for ISDN (e.g., TP3420, TP3410) and Non-ISDN (e.g., EEPROMs, LED drivers) applications.

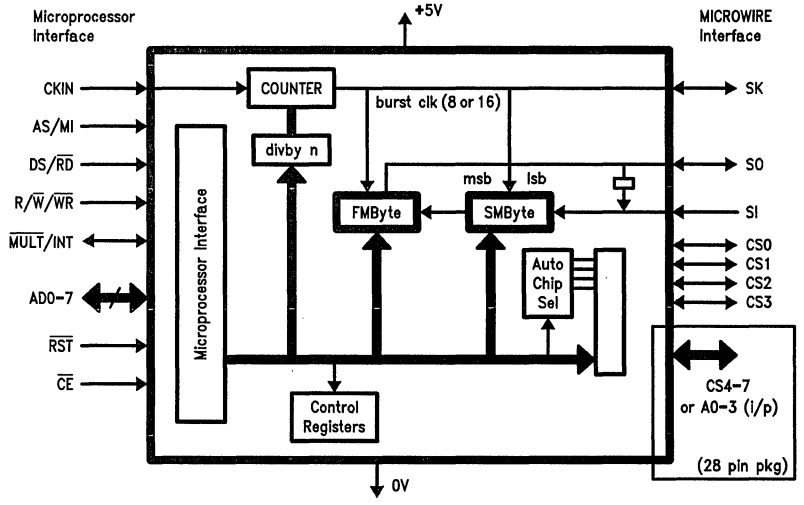
Applications

- ISDN Terminal Adapters
- Digital Line cards (ISDN and Non ISDN)
- Analog Linecards using National COMBO II™
- Interfacing to industry standard serial EEPROMs
- Interfacing to industry standard Microwire peripheral devices such as Analog to Digital Converters, LCD drivers, clock generators

Features

- Multiplexed and Non-multiplexed microprocessor bus compatible
- National/Intel and Motorola microprocessor bus compatible
- CK in up to 20 MHz
- Microwire clock speeds up to 5 MHz
- Directly compatible with 8- and 16-bit Microwire peripherals
- 4 chip select lines (24-pin) or 8 chip select lines (28-pin)
- Memory mapped peripherals
- Programmable Microwire Clock to communicate with devices of different speeds
- Operates as Microwire bus master or slave
- 24-pin Skinny-DIP pkg or 28-pin PLCC
- CMOS, Low Power

Block Diagram



TL/H/10803-1

FIGURE 1. MICROWIRE Interface Device MID

National Semiconductor

PRELIMINARY

HPC16400E/HPC36400E/HPC46400E
High-Performance Communications microController

General Description

The HPC16400E is an upgraded HPC16400. Features have been added to support V.120, the 8-bit mode has been enhanced to support all instructions, and the UART has been changed to provide more flexibility and power. The HPC16400E is fully upward compatible with the HPC16400.

The HPC16400E has 4 functional blocks to support a wide range of communication application-2 HDLC channels, 4 channel DMA controller to facilitate data flow for the HDLC channels, programmable serial interface and UART.

The serial interface decoder allows the 2 HDLC channels to be used with devices using interchip serial link for point-to-point and multipoint data exchanges. The decoder generates enable signals for the HDLC channels allowing multiplexed D and B channel data to be accessed.

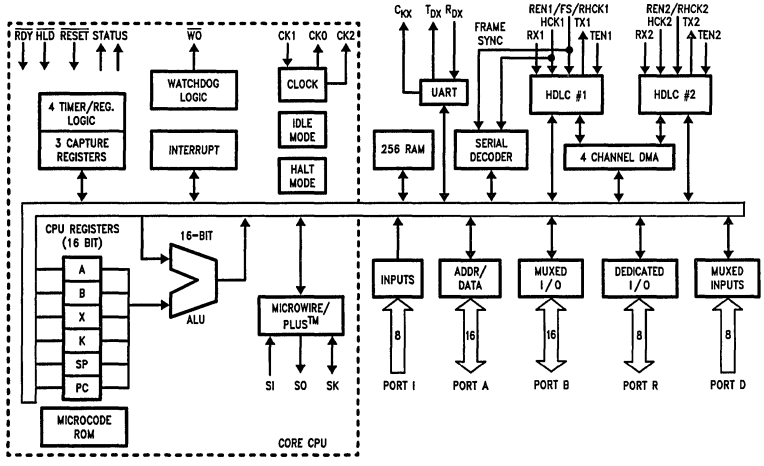
The HDLC channels manage the link by providing sequencing using the HDLC framing along with error control based upon a cyclic redundancy check (CRC). Multiple address recognition modes, and both bit and byte modes of operation are supported.

The HPC16400E is available in 68-pin PLCC, LDCC, PGA and 84-Pin TapePak® packages.

Features

- HPC™ family—core features:
  - 16-bit data bus, ALU, and registers
  - 64 kbytes of external memory addressing
  - FAST!—20.0 MHz system clock
  - Four 16-bit timer/counters with WATCHDOG logic
  - MICROWIRE/PLUS™ serial I/O interface
  - CMOS—low power with two power save modes
- Two full duplex HDLC channels
  - Optimized for ISDN, X.25, V.120, and LAPD applications
  - Programmable frame address recognition
  - Up to 4.65 Mbps serial data rate
  - Built in diagnostics
  - Synchronous bypass mode
  - Optional CRC generation
  - Received CRC bytes can be read by the CPU
- Four channel DMA controller
- 8- or 16-bit external data bus
- UART
  - Full duplex
  - 7, 8, or 9 data bits
  - Even, odd, mark, space or no parity
  - 7/8, 1 or 2 stop bit generation
  - Accurate internal baud rate generation up to 625k baud without penalty of using expensive crystal
  - Synchronous and asynchronous modes of operation
- Serial Decoder
  - Supports 6 popular time division multiplexing protocols for inter-chip communications
  - Optional rate adaptation of 64 kbit/s data rate to 56 kbit/s
- Over ½ Mbyte of extended addressing
- Easy interface to National's DASL, 'U' and 'S' transceivers—TP3400, TP3410 and TP3420
- Commercial (0°C to +70°C), industrial (−40°C to +85°C) and military (−55°C to +125°C) temperature ranges

Block Diagram



TL/DD/10422–1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Total Allowable Source or Sink Current	100 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	300°C
ESD Rating is to be determined	
V_{CC} with Respect to GND	−0.5V to 7.0V
All Other Pins	$(V_{CC} + 0.5)$V to (GND − 0.5)V

Note: *Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.*

DC Electrical Characteristics

V_{CC} = 5.0V ±10% unless otherwise specified, T_A = 0°C to +70°C for HPC46400E, −40°C to +85°C for HPC36400E, −55°C to +125°C for HPC16400E

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC_1}	Supply Current	V_{CC} = 5.5V, f_{in} = 20.0 MHz (Note 1)		70	mA
		V_{CC} = 5.5V, f_{in} = 2.0 MHz (Note 1)		10	mA
I_{CC_2}	IDLE Mode Current	V_{CC} = 5.5V, f_{in} = 20.0 MHz (Note 1)		10	mA
		V_{CC} = 5.5V, f_{in} = 2.0 MHz (Note 1)		2	mA
I_{CC_3}	HALT Mode Current	V_{CC} = 5.5V, f_{in} = 0 kHz (Note 1)		500	μA
		V_{CC} = 2.5V, f_{in} = 0 kHz (Note 1)		150	μA
INPUT VOLTAGE LEVELS—SCHMITT TRIGGERED: RESET, CKI, WO, D0, I1, I2, I3					
V_{IH_1}	Logic High		0.9 V_{CC}		V
V_{IL_1}	Logic Low			0.1 V_{CC}	V
INPUT VOLTAGE LEVELS—PORT A					
V_{IH_2}	Logic High		2.0		V
V_{IL_2}	Logic Low			0.8	V
INPUT VOLTAGE LEVELS—ALL OTHERS					
V_{IH_3}	Logic High		0.7 V_{CC}		V
V_{IL_3}	Logic Low			0.2 V_{CC}	V
I_{LI}	Input Leakage Current	(Note 2)		±1	μA
C_I	Input Capacitance	(Note 3)		10	pF
C_{IO}	I/O Capacitance	(Note 3)		20	pF
OUTPUT VOLTAGE LEVELS					
V_{OH_1}	Logic High (CMOS)	I_{OH} = −10 μA (Note 3)	V_{CC} − 0.1		V
V_{OL_1}	Logic Low (CMOS)	I_{OH} = 10 μA (Note 3)		0.1	V
V_{OH_2}	Port A/B Drive, CK2 (A_0–A_{15}, B_{10}, B_{11}, B_{12}, B_{15})	I_{OH} = −7 mA	2.4		V
V_{OL_2}		I_{OL} = 3 mA		0.4	V
V_{OH_3}	Other Port Pin Drive, $\overline{WO}$ (open drain) (B_0–B_9, B_{13}, B_{14}, R_0–R_7, D_5, D_7)	I_{OH} = −1.6 mA (except $\overline{WO}$)	2.4		V
V_{OL_3}		I_{OL} = 0.5 mA		0.4	V
V_{OH_4}	ST1 and ST2 Drive	I_{OH} = −6 mA	2.4		V
V_{OL_4}		I_{OL} = 1.6 mA (Note 4)		0.4	V
V_{RAM}	RAM Keep-Alive Voltage	(Note 5)	2.5		V
I_{OZ}	TRI-STATE Leakage Current			±5	μA

Note 1: I_{CC_1}, I_{CC_2}, I_{CC_3} measured with no external drive (I_{OH} and I_{OL} = 0, I_{IH} and I_{IL} = 0). I_{CC_1} is measured with $\overline{RESET}$ = V_{SS}. I_{CC_3} is measured with NMI = V_{CC}. CKI driven to V_{IH_1} and V_{IL_1} with rise and fall times less than 10 ns.

Note 2: $\overline{RDY}$/HLD and $\overline{RDY}$/I4 pins have internal pullups and meet this spec only at V_{IN} = V_{CC}.

Note 3: These parameters are guaranteed by design and are not tested.

Note 4: ST2 drive will not meet this spec under condition of RESET pin = low.

Note 5: Test duration is 100 ms.

AC Electrical Characteristics

(see Notes 1 and 4 and *Figures 1* thru *5*), V_{CC} = 5V ±10%, T_A = 0°C to +70°C for HPC46400E, −40°C to +85°C for HPC36400E, −55°C to +125°C for HPC16400E

	Symbol and Formula	Parameter and Notes	Min	Max	Units	Note
Clocks	f_C	CKI Operating Frequency	2	20	MHz	
	$t_{C1} = 1/f_C$	CKI Period	50	500	ns	
	t_{C1R}	CKI Rise Time		7	ns	(Note 1)
	t_{C1F}	CKI Fall Time		7	ns	(Note 1)
	$100\ t_{C1H}/t_{C1}$	CKI Duty Cycle	45	55	%	(Note 1)
	$t_C = 2/f_C$	CPU or DMA Timing Cycle	100		ns	
	$t_{WAIT} = t_C$	CPU or DMA Wait State Period	100		ns	
	t_{DC1C2R}	Delay of CK2 Rising Edge after CKI Falling Edge	0	55	ns	(Note 2)
	t_{DC1C2F}	Delay of CK2 Falling Edge after CKI Falling Edge	0	55	ns	(Note 2)
	$f_U = f_C/8$	External UART Clock Input Frequency		2.5	MHz	
	$f_{MW} = f_C/19$	External MICROWIRE/PLUS Clock Input Frequency		1.25	MHz	
	$t_{HCK} = 4t_{C1} + 14$	HDLC Clock Input Period	214		ns	
Timers	$f_{XIN} = f_C/19$	External Timer Input Frequency		1052	kHz	
	$t_{XIN} = t_C$	Pulse Width for Timer Inputs	100		ns	
	$f_{XOUT} = f_C/16$	Timer Output Frequency		1.25	MHz	
Microwire/Plus	t_{UWS}	MICROWIRE Setup Time — Master	100		ns	
		— Slave	20		ns	
	t_{UWH}	MICROWIRE Hold Time — Master	20		ns	
		— Slave	50		ns	
	t_{UWV}	MICROWIRE Output Valid Time — Master		50	ns	
		— Slave		150	ns	
External Hold	$t_{SALE} = \frac{3}{4}t_C + 40$	$\overline{HLD}$ Falling Edge before ALE Rising Edge	115		ns	
	$t_{HWP} = \frac{3}{4}t_C + 85$	$\overline{HLD}$ Pulse Width	110		ns	
	$t_{HAE} = \frac{3}{4}t_C + 100$	$\overline{HLDA}$ Falling Edge after $\overline{HLD}$ Falling Edge		175	ns	(Note 3)
	$t_{HAD} = \frac{5}{4}t_C + 85$	$\overline{HLDA}$ Rising Edge after $\overline{HLD}$ Rising Edge		210	ns	
	t_{BF}	Bus Float after $\overline{HLDA}$ Falling Edge		66	ns	
	$t_{BE} = t_C - 66$	Bus Enable after $\overline{HLDA}$ Rising Edge	34		ns	

Note 1: These AC characteristics are guaranteed with external clock drive on CKI having 50% duty cycle and with less than 15 pF load on CKO. Spec'd t_{C1R}, t_{C1F}, and CKI duty cycle limits are not tested but are guaranteed functional by design.

Note 2: Do not design with this parameter unless CKI is driven with an active signal meeting T_{C1R} and T_{C1F} specs. When using a passive crystal circuit, its stability is not guaranteed if either CKI or CKO is connected to any external logic other than the passive components of the crystal circuit.

Note 3: t_{HAE} is spec'd for case with $\overline{HLD}$ falling edge occurring at the latest time it can be accepted during the present CPU or DMA cycle being executed. If $\overline{HLD}$ falling edge occurs later, t_{HAE} as long as ($3\ t_C + 4$ WS $+ 72\ t_C + 100$) may occur depending on the following CPU instruction or DMA cycle, its wait states and ready input.

Note 4: WS (t_{WAIT}) × (number of preprogrammed wait states). Minimum and maximum values are calculated at maximum operating frequency, f_C = 20 MHz, with one wait state preprogrammed. These values are guaranteed with AC loading of 100 pF on Port A, 50 pF on CK2, 80 pF on other outputs, and DC loading of the pin's DC spec non CMOS I_{OL} or I_{OH}.

AC Electrical Characteristics (Continued)

CPU and DMA Timing (see Notes 1 and 4 and *Figures 2, 4, 6, 7, 8,* and *9*), V_{CC} = 5V ±10%, T_A = 0°C to +70°C for HPC46400E, −40°C to +85°C for HPC36400E, −55°C to +125°C for HPC16400E

	Symbol	Formula	Cycle	Parameter	Min	Max	Units	Note
Address Cycles	t_{1ALR}		CPU DMA	Delay of ALE Rising Edge after CKI Rising Edge Delay of ALE Rising Edge after CKI Falling Edge	0 0	35 35	ns ns	(Note 2) (Note 2)
	t_{1ALF}		CPU DMA	Delay of ALE Falling Edge after CKI Rising Edge Delay of ALE Falling Edge after CKI Falling Edge	0 0	35 35	ns ns	(Note 2) (Note 2)
	t_{2ALR}	$\frac{1}{4}t_C + 20$	CPU	ALE Rising Edge after CK2 Rising Edge		45	ns	
	t_{2ALF}	$\frac{1}{4}t_C + 20$	CPU	ALE Falling Edge after CK2 Falling Edge		45	ns	
	t_{LL}	$\frac{1}{2}t_C - 9$		ALE Pulse Width	41		ns	
	t_{ST}	$\frac{1}{4}t_C - 16$		Setup of Address Valid before ALE Falling Edge	9		ns	
	t_{VP}	$\frac{1}{4}t_C - 10$ $\frac{1}{2}t_C - 10$	CPU DMA	Hold of Address Valid after ALE Falling Edge	15 40		ns ns	
Read Cycles	t_{ARR}	$\frac{1}{2}t_C - 20$		ALE Falling Edge to $\overline{RD}$ Falling Edge	30		ns	
	t_{ACC}	$t_C + WS - 55$ $\frac{5}{4}t_C + WS - 75$	CPU DMA	Data Input Valid after Address Output Valid		145 150	ns ns	
	t_{RD}	$\frac{1}{4}t_C + WS - 35$ $\frac{1}{2}t_C + WS$	CPU DMA	Data Input Valid after $\overline{RD}$ Falling Edge		90 115	ns ns	
	t_{RW}	$\frac{1}{4}t_C + WS - 10$ $\frac{1}{2}t_C + WS - 15$	CPU DMA	$\overline{RD}$ Pulse Width	115 135		ns ns	
	t_{DR}	$t_C - 15$ $\frac{3}{4}t_C - 15$	CPU DMA	Hold of Data Input Valid after $\overline{RD}$ Rising Edge	0 0	85 60	ns ns	(Note 5) (Note 5)
	t_{RDA}	$t_C - 5$ $\frac{3}{4}t_C - 5$	CPU DMA	Bus Enable after $\overline{RD}$ Rising Edge	95 70		ns ns	(Note 5) (Note 5)
Write Cycles	t_{ARW}	$\frac{1}{2}t_C - 20$		ALE Falling Edge to $\overline{WR}$ Falling Edge	30		ns	
	t_{WW}	$\frac{3}{4}t_C + WS - 15$ $\frac{1}{2}t_C + WS - 15$	CPU DMA	$\overline{WR}$ Pulse Width	160 135		ns ns	
	t_V	$\frac{1}{2}t_C + WS - 40$ $\frac{1}{2}t_C + WS - 50$	CPU DMA	Data Output Valid before $\overline{WR}$ Rising Edge	110 100		ns ns	
	t_{HW}	$\frac{1}{4}t_C - 10$		Hold of Data Output Valid after $\overline{WR}$ Rising Edge	15		ns	
Ready Input	t_{RDYS}			$\overline{RDY}$ Falling Edge before CK2 Rising Edge	45		ns	
	t_{RDYH}			$\overline{RDY}$ Rising Edge after CK2 Rising Edge	0		ns	
	t_{RDYV}	$WS - \frac{1}{4}t_C - 47$ $t_C - 47$	CPU DMA	$\overline{RDY}$ Falling Edge after $\overline{RD}$ or $\overline{WR}$ Falling Edge		28 53	ns ns	(Note 6)

Note 1: These AC characteristics are guaranteed with external clock drive on CKI having 50% duty cycle and with less than 15 pF load on CKO. Spec'd t_{C1R}, t_{C1F}, and CKI duty cycle limits are not tested but are guaranteed functional by design.

Note 2: Do not design with this parameter unless CKI is driven with an active signal meeting T_{C1R} and T_{C1F} specs. When using a passive crystal circuit, its stability is not guaranteed if either CKI or CKO is connected to any external logic other than the passive components of the crystal circuit.

Note 3: t_{HAE} is spec'd for case with $\overline{HLD}$ falling edge occurring at the latest time it can be accepted during the present CPU or DMA cycle being executed. If $\overline{HLD}$ falling edge occurs later, t_{HAE} as long as (3 t_C + 4 WS + 72 t_C + 100) may occur depending on the following CPU instruction or DMA cycle, its wait states and ready input.

Note 4: WS (t_{WAIT}) × (number of preprogrammed wait states). Minimum and maximum values are calculated at maximum operating frequency, f_C = 20 MHz, with one wait state preprogrammed. These values are guaranteed with AC loading of 100 pF on Port A, 50 pF on CK2, 80 pF on other outputs, and DC loading of the pin's DC spec non CMOS I_{OL} or I_{OH}.

Note 5: Formula has $\frac{7}{4}t_C$ for CPU read followed by DMA $\frac{3}{4}t_C$ for DMA read followed by CPU.

Note 6: In HPC in-circuit emulators the t_{RDYV} formulas are WS − $\frac{1}{4}t_C$ − 57 and t_C − 57 yielding minimums of 18 ns and 43 ns for CPU and DMA cycles, respectively.

Timing Waveforms

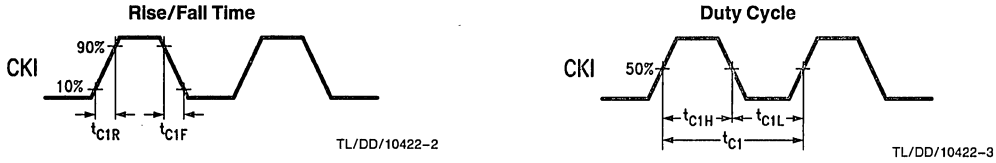
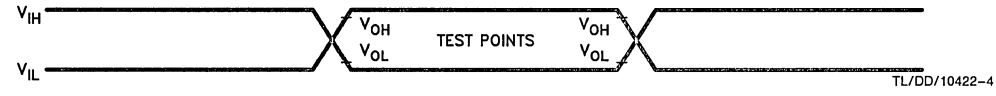


FIGURE 1. CKI Input Signal



Note: AC testing inputs are driven at V_{IH} for a logic "1" and V_{IL} for a logic "0". Output timing measurements are made at V_{OH} for a logic "1" hold or rising edge and at V_{OL} for a logic "0" hold or falling edge.

FIGURE 2. Input and Output for AC Tests

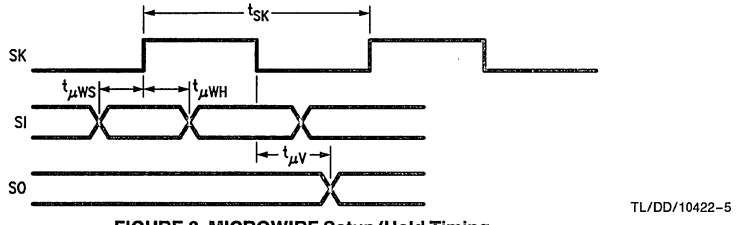


FIGURE 3. MICROWIRE Setup/Hold Timing

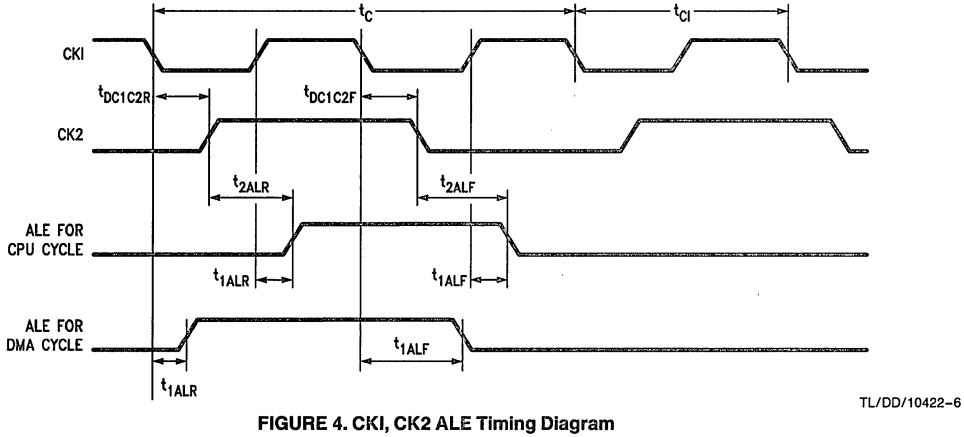


FIGURE 4. CKI, CK2 ALE Timing Diagram

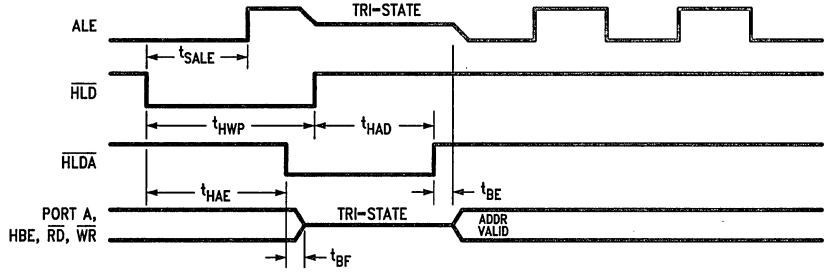
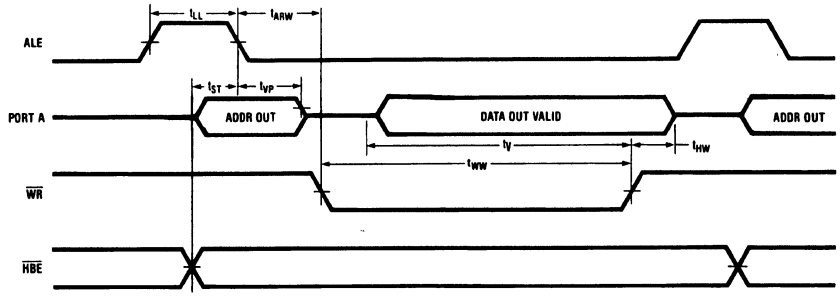


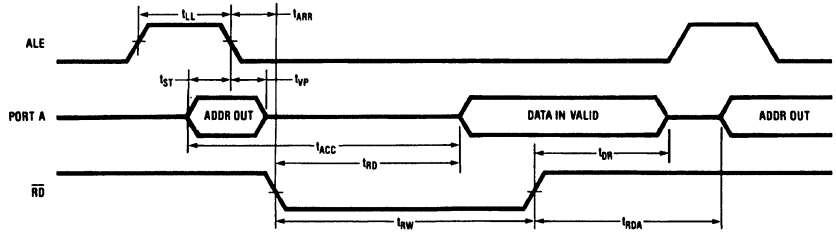
FIGURE 5. External Hold Timing

Timing Waveforms (Continued)



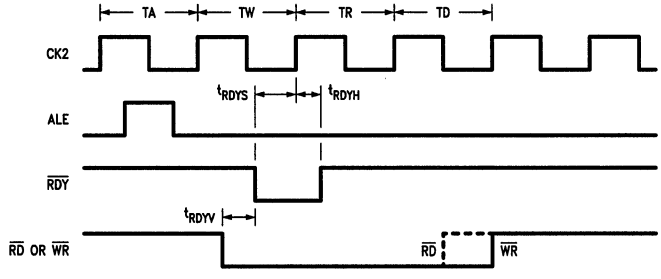
TL/DD/10422-8

FIGURE 6. CPU and DMA Write Cycles



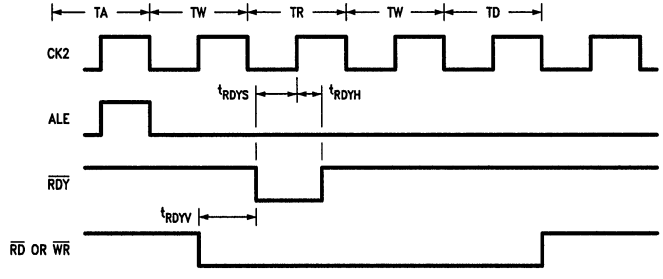
TL/DD/10422-9

FIGURE 7. CPU and DMA Read Cycles



TL/DD/10422-10

FIGURE 8. CPU Ready Mode with 1 Wait State and Ready Wait Extension

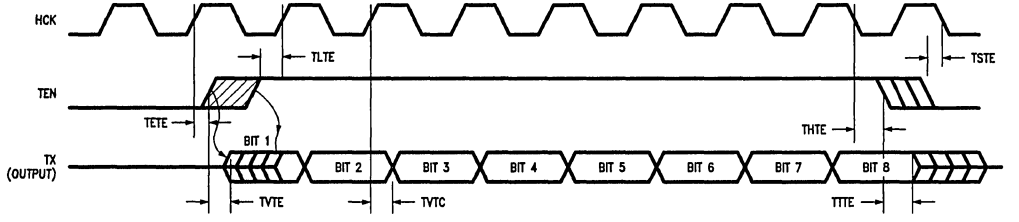


TL/DD/10422-11

FIGURE 9. DMA Ready Mode with 2 Wait States and Ready Wait Extension

Timing Waveforms (Continued)

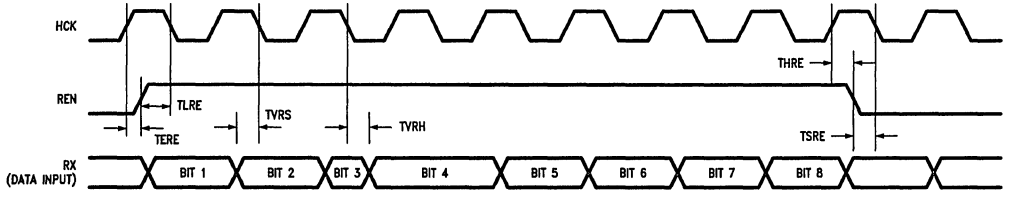
Timing Diagrams for TX Using External Enable



TL/DD/10422–12

Symbol	Parameter	Min	Max	Units
TETE	Hold of TEN Low after HCK Rising Edge	5		ns
TLTE	Setup of TEN Rising Edge before HCK Rising Edge	80		ns
TVTE	Delay of TX Output Valid after TEN Rising Edge		40	ns
TVTC	Delay of TX Output Valid after HCK Rising Edge		45	ns
THTE	Hold of TEN High after HCK Falling Edge	60		ns
TSTE	Setup of TEN Falling Edge before HCK Falling Edge	20		ns
TTTE	Delay of TX Output TRI-STATE® after TEN Falling Edge		40	ns

Timing Diagrams for RX Using External Enable

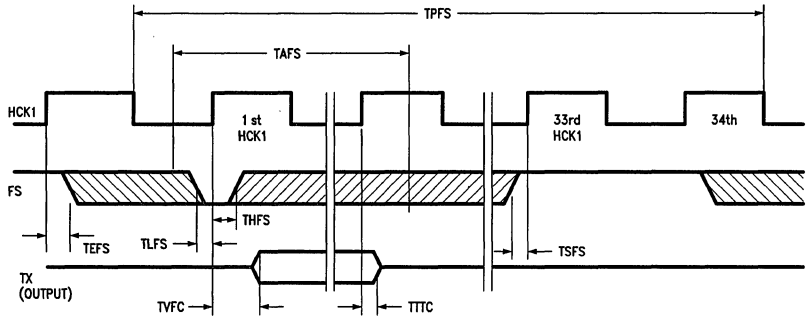


TL/DD/10422–13

Symbol	Parameter	Min	Max	Units
TERE	Hold of REN Low after HCK Rising Edge	5		ns
TLRE	Setup of REN Rising Edge before HCK Falling Edge	30		ns
TVRS	Setup of RX Data Input Valid before HCK Falling Edge	20		ns
TVRH	Hold of RX Data Input Valid after HCK Falling Edge	20		ns
THRE	Hold of REN High after HCK Rising Edge	5		ns
TSRE	Setup of REN Falling Edge before HCK Falling Edge	30		ns

Timing Waveforms (Continued)

Serial Decoder Timing Diagram (Mode 2)



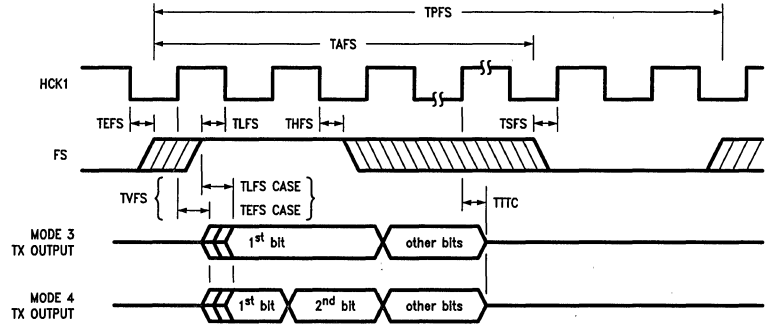
TL/DD/10422–14

Symbol	Parameter	Min	Max	Comments	Units
TPFS	Number of HCK1 Periods between FS Falling Edges	34			
TAFS	Number of HCK1 Rising Edges during FS Low	1	32		
TEFS	Hold of FS High after HCK1 Rising Edge	10		Early FS	ns
TLFS	Setup of FS Falling Edge before HCK1 Rising Edge	20		Late FS, (Note 8)	ns
TVFC	Delay of TX Output Valid after HCK1 Rising Edge		50	(Note 7)	ns
THFS	Hold of FS Low after HCK1 Rising Edge	20			ns
TSFS	Setup of FS Rising Edge before HCK1 Rising Edge	20			ns
TTTC	Delay of TX output TRI-STATE after HCK1 Rising Edge		40		ns

Note 7: This spec is for 1st bit only. Remaining bits are spec'd by transmitter TVTC spec.

Note 8: Receiver specs TVRS and TVRH are required along with TLFS for receiver operation using serial decoder.

Serial Decoder Timing Diagram (Modes 3, 4)



TL/DD/10422–15

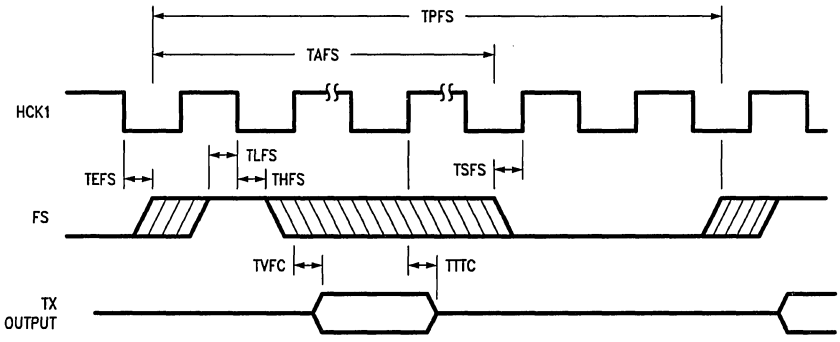
Symbol	Parameter	Min	Max	Comments	Units
TPFS	Number of HCK1 Periods between FS Rising Edges	64		SD Mode 3	
TPFS	Number of HCK1 Periods between FS Rising Edges	32		SD Mode 4	
TAFS	Number of HCK1 Falling Edges during FS High	2	62	SD Mode 3	
TAFS	Number of HCK1 Falling Edges during FS High	2	30	SD Mode 4	
TEFS	Hold of FS Low after HCK1 Falling Edge	10		Early FS	ns
TLFS	Setup of FS Rising Edge before HCK1 Falling Edge	45		Late FS, (Note 8)	ns
TVFS	Delay of TX Output Valid after HCK1 and FS Rising Edges		50	(Note 9)	ns
THFS	Hold of FS High after HCK1 Falling Edge	20			ns
TSFS	Setup of FS Falling Edge before HCK1 Rising Edge	20			ns
TTTC	Delay of TX output TRI-STATE after HCK1 Rising Edge		40		ns

Note 8: Receiver specs TVRS and TVRH are required along with TLFS for receiver operation using serial decoder.

Note 9: This spec is for 1st bit only and is measured from the later of either FS or HCK1 rising edge. Remaining bits are spec'd from HCK1 rising edges by transmitter TVTC spec.

Timing Waveforms (Continued)

Serial Decoder Timing Diagram (Modes 5, 6,7)



TL/DD/10422–16

Symbol	Parameter	Min	Max	Comments	Units
TPFS	Number of HCK1 Periods between FS Rising Edges	34			
TAFS	Number of HCK1 Falling Edges during FS High	1	32		
TEFS	Hold of FS Low after HCK1 Falling Edge	10		Early FS	ns
TLFS	Setup of FS Rising Edge before HCK1 Falling Edge	45		Late FS, (Note 8)	ns
TVFC	Delay of TX Output Valid after HCK1 Rising Edge		50	(Note 7)	ns
THFS	Hold of FS High after HCK1 Falling Edge	20			ns
TSFS	Setup of FS Falling Edge before HCK1 Rising Edge	20			ns
TTTC	Delay of TX output TRI-STATE after HCK1 Rising Edge		40		ns

Note 7: This spec is for 1st bit only. Remaining bits are spec'd by transmitter TVTC spec.

Note 8: Receiver specs TVRS and TVRH are required along with TLFS for receiver operation using serial decoder.

Pin Descriptions

I/O PORTS

Port A is a 16-bit multiplexed address/data bus used for accessing external program and data memory. Four associated bus control signals are available on port B. The Address Latch Enable (ALE) signal is used to provide timing to demultiplex the bus. Reading from and writing to external memory are signalled by $\overline{RD}$ and $\overline{WR}$ respectively. External memory can be addressed as either bytes or words with the decoding controlled by two lines, Bus High Byte enable ($\overline{HBE}$) and Address/Data Line 0 (A0).

Port B is a 16-bit port, with 12 bits of bidirectional I/O. Pins B10, B11, B12 and B15 are the control bus signals for the address/data bus. Port B may also be configured via a function register BFUN to individually allow each bidirectional I/O pin to have an alternate function.

B0:	TDX	UART Data Output
B1:	CFLG1	Closing Flag Output for HDLC #1 Transmitter
B2:	CKX	UART Clock (Input or Output)
B3:	T2IO	Timer2 I/O Pin
B4:	T3IO	Timer3 I/O Pin
B5:	SO	MICROWIRE/PLUS Output
B6:	SK	MICROWIRE/PLUS Clock (Input or Output)
B7:	$\overline{HLDA}$	Hold Acknowledge Output
B8:	TS0	Timer Synchronous Output
B9:	TS1	Timer Synchronous Output
B10:	ALE	Address Latch Enable Output for Address/Data Bus
B11:	$\overline{WR}$	Address/Data Bus Write Output
B12:	$\overline{HBE}$	High Byte Enable Output for Address/Data Bus; also 8-Bit Mode Strap Input on Reset.
B13:	TS2	Timer Synchronous Output
B14:	TS3	Timer Synchronous Output
B15:	$\overline{RD}$	Address/Data Bus Read Output

When operating in the extended memory addressing mode, four bits of port B can be used as follows—

B8:	BS0	Memory bank switch output 0 (LSB)
B9:	BS1	Memory bank switch output 1
B13:	BS2	Memory bank switch output 2
B14:	BS3	Memory bank switch output 3 (MSB)

Port I is an 8-bit input port that can be read as general purpose inputs and can also be used for the following functions:

I0:	HCK2	HLDC #2 Clock Input
I1:	NMI	Nonmaskable Interrupt Input
I2:	INT2	Maskable Interrupt/Input Capture
I3:	INT3	Maskable Interrupt/Input Capture
I4:	INT4/RDY	Maskable Interrupt/Input Capture/Ready Input
I5:	SI	MICROWIRE/PLUS Data Input
I6:	RDX	UART Data Input
I7:	HCK1	HDLC #1 Clock and Serial Decoder Clock Input

Port D is an 8-bit input port that can be read as general purpose inputs and can also be used for the following functions:

D0:	REN1/FS/RHCK1	Receiver #1 Enable/Serial Decoder Frame Sync Input/Receiver #1 Clock Input
D1:	TEN1	Transmitter #1 Enable Input
D2:	REN2/RHCK2	Receiver #2 Enable Input/Receiver #2 Clock Input
D3:	TEN2	Transmitter #2 Enable Input
D4:	RX1	Receiver #1 Data Input
D5:	TX1	Transmitter #1 Data Output
D6:	RX2	Receiver #2 Data Input
D7:	TX2	Transmitter #2 Data Output

Note: Any of these pins can be read by software. Therefore, unused functions can be used as general purpose inputs, notably external enable lines when the internal serial decoder is used.

Port R is an 8-bit bidirectional I/O port available for general purpose I/O operations. Port R has a direction register to enable each separate pin to be individually defined as an input or output. It has a data register which contains the value to be output. In addition, the Port R pins can be read directly using the Port R pins address.

Pin Descriptions (Continued)

POWER SUPPLIES

V_{CC1}, V_{CC2} Positive Power Supply (two pins)
GND Ground for On-Chip Logic
DGND Ground for Output Buffers

Note: There are two electrically connected V_{CC} pins on the chip, GND and DGND are electrically isolated. Both V_{CC} pins and both ground pins must be used.

CLOCK PINS

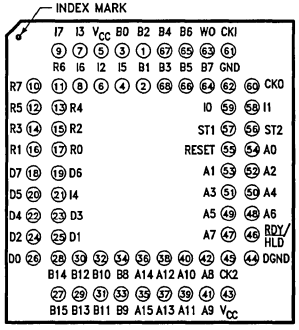
CKI The System Clock Input
CKO The System Clock Output (Inversion of CKI)
Pins CKI and CKO are usually connected across an external crystal.
CK2 Clock Output (CKI divided by 2)

OTHER PINS

$\overline{WO}$ This is an active low open drain output which signals an illegal situation has been detected by the Watch Dog logic.
ST1 Bus Cycle Status Output indicates first opcode fetch.
ST2 Bus Cycle Status Output indicates machine states (skip and interrupt).
$\overline{RESET}$ Active low input that forces the chip to restart and sets the ports in a TRI-STATE mode.
RDY/$\overline{HLD}$ Has two uses, selected by a software bit. This pin is either a READY input to extend the bus cycle for slower memories or a HOLD-REQUEST input to put the bus in a high impedance state for external DMA purposes. In the second case the I4 pin can become the READY input.

Connection Diagrams

Pin Grid Array

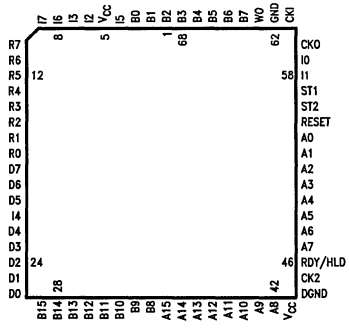


TL/DD/10422-17

Top View

See NS Package Number U68A

Plastic and Leaded Chip Carriers



TL/DD/10422-18

Top View

See NS Package Number EL68A or V68A

Wait States

The HPC16400E provides software selectable Wait States for access to slower memories and for shared bus applications. The number of Wait States for the CPU are selected by two bits in the PSW register. The number of Wait States for DMA are selected by a bit in the Message System Configuration register. Additionally, the RDY input may be used to extend the RD or WR cycle, allowing the HPC to be used in shared memory applications and allowing the user to interface with slow memories and peripherals.

Power Save Modes

Two power saving modes are available on the HPC16400E: HALT and IDLE. In the HALT mode, all processor activities are stopped. In the IDLE mode, the on-board oscillator and timer T0 are active but all other processor activities are stopped. In either mode, on-board RAM, registers and I/O are unaffected (except the HDLC and UART which are reset).

HALT MODE

The HPC16400E is placed in the HALT mode under software control by setting bits in the PSW. All processor activities, including the clock and timers, are stopped. In the HALT mode, power requirements for the HPC16400E are minimal and the applied voltage (V_{CC}) may be decreased without altering the state of the machine. There are two ways of exiting the HALT mode: via the $\overline{RESET}$ or the NMI. The $\overline{RESET}$ input reinitializes the processor. Use of the NMI input will generate a vectored interrupt and resume operation from that point with no initialization. The HALT mode can be enabled or disabled by means of a control register HALT enable. To prevent accidental use of the HALT mode the HALT enable register can be modified only once.

IDLE MODE

The HPC16400E is placed in the IDLE mode through the PSW. In this mode, all processor activity, except the on-board oscillator and Timer T0, is stopped. The HPC16400E resumes normal operation upon timer T0 overflow. As with the HALT mode, the processor is also returned to full operation by the $\overline{RESET}$ or NMI inputs, but without waiting for oscillator stabilization.

HPC16400E Interrupts

Complex interrupt handling is easily accomplished by the HPC16400E's vectored interrupt scheme. There are eight possible interrupt sources as shown in Table I.

TABLE I. Interrupts

Vector/ Address	Interrupt Source	Arbitration Ranking
FFFF|FFFE	Reset	0
FFFD|FFFC	Nonmaskable Ext (NMI)	1
FFFB|FFFA	External on I2	2
FFF9|FFF8	External on I3	3
FFF7|FFF6	External on I4	4
FFF5|FFF4	Internal on Timers	5
FFF3|FFF2	Internal on UART	6
FFF1|FFF0	End of Message (EOM)	7

The 16400E contains arbitration logic to determine which interrupt will be serviced first if two or more interrupts occur simultaneously. Interrupts are serviced after the current instruction is completed except for the RESET which is serviced immediately.

The NMI interrupt will immediately stop DMA activity. Byte transfers in progress will finish thereby allowing an orderly transition to the interrupt service vector (see DMA description). The HDLC channels continue to operate, and the user must service data errors that might have occurred during the NMI service routine.

Interrupt Processing

Interrupts are serviced after the current instruction is completed except for the RESET, which is serviced immediately.

RESET holds on-chip logic in a reset state while low, and triggers the RESET interrupt on its rising edge. All other interrupts are edge-sensitive. NMI is positive-edge sensitive. The external interrupts on I2, I3, and I4 can be software selected to be rising or falling edge sensitive.

Interrupt Control Registers

The HPC16400E allows the various interrupt sources and conditions to be programmed. This is done through the various control registers. A brief description of the different control registers is given below.

INTERRUPT ENABLE REGISTER (ENIR)

RESET and the External Interrupt on I1 are non-maskable interrupts. The other interrupts can be individually enabled or disabled. Additionally, a Global Interrupt Enable Bit in the ENIR Register allows the Maskable interrupts to be collectively enabled or disabled. Thus, in order for a particular interrupt to request service, both the individual enable bit and the Global Interrupt bit (GIE) have to be set.

INTERRUPT PENDING REGISTER (IRPD)

The IRPD register contains a bit allocated for each interrupt vector. The occurrence of specified interrupt trigger conditions causes the appropriate bit to be set. There is no indication of the order in which the interrupts have been received. The bits are set independently of the fact that the interrupts may be disabled. IRPD is a Read/Write register. The bits corresponding to the external interrupts are normally cleared by the HPC16400E upon entering the interrupt servicing routine

For the interrupts from the on-board peripherals, the user has the responsibility of acknowledging the interrupt through software.

INTERRUPT CONDITION REGISTER (IRCD)

Three bits of the register select the input polarity of the external interrupt on I2, I3, and I4.

Servicing the Interrupts

The Interrupt, once acknowledged, pushes the program counter (PC) onto the stack thus incrementing the stack pointer (SP) twice. The Global Interrupt Enable (GIE) bit is reset, thus disabling further interrupts. The program counter is loaded with the contents of the memory at the vector address and the processor resumes operation at this point. At the end of the interrupt service routine, the user does a RETI instruction to pop the stack, set the GIE bit and return to the main program. The GIE bit can be set in the interrupt service routine to nest interrupts if desired. *Figure 10* shows the Interrupt Enable Logic.

Reset

The RESET input initializes the processor and sets all pins at TRI-STATE except CK0, CK2, and WO. HBE and ST2 have pull-downs designed to withstand override. RESET is an active-low Schmitt trigger input. The processor vectors to FFFF:FFFE and resumes operation at the address contained at that memory location.

The $\overline{\text{RESET}}$ pin must be asserted low for at least 16 cycles of the CK2 clock. In applications using the Watchdog feature, $\overline{\text{RESET}}$ should be asserted for at least 64 cycles of the CK2 clock.

On application of power, $\overline{\text{RESET}}$ must be held low for at least five times the power supply rise time to ensure that the on-chip oscillator circuit has time to stabilize.

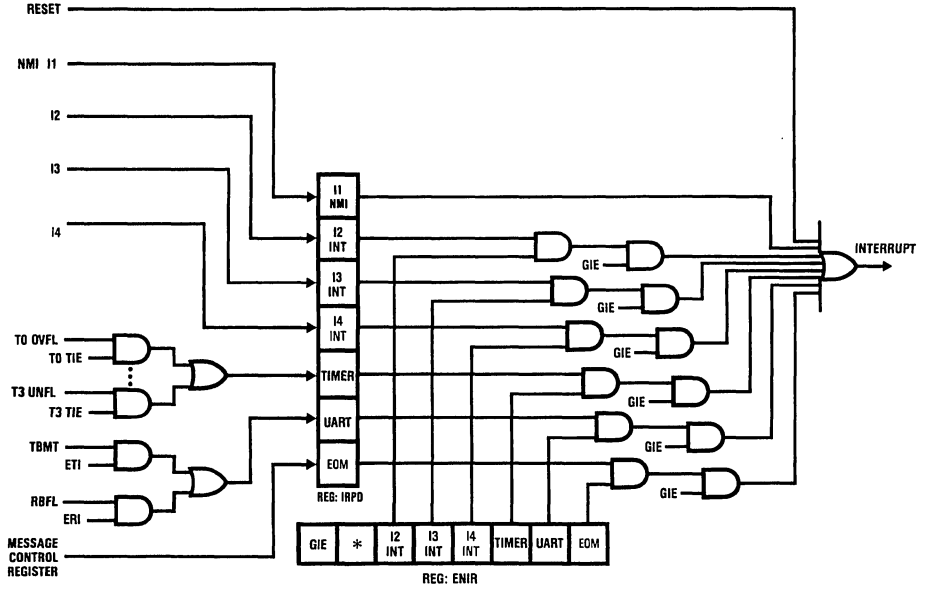
Timer Overview

The HPC16400E contains a powerful set of flexible timers enabling the HPC16400E to perform extensive timer functions; not usually associated with microcontrollers.

The HPC16400E contains four 16-bit timers. Three of the timers have an associated 16-bit register. Timer T0 is a free-running timer, counting up at a fixed CKI/16 (Clock Input/16) rate. It is used for Watch Dog logic, high speed event capture, and to exit from the IDLE mode. Consequently, it cannot be stopped or written to under software control. Timer T0 permits precise measurements by means of the capture registers I2CR, I3CR, and I4CR. A control bit in the register T0CON configures timer T1 and its associated register R1 as capture registers I3CR and I2CR. The capture registers I2CR, I3CR, and I4CR respectively, record the value of timer T0 when specific events occur on the interrupt pins I2, I3, and I4. The control register IRCD programs the capture registers to trigger on either a rising edge or a falling edge of its respective input. The specified edge can also be programmed to generate an interrupt (see *Figure 11*).

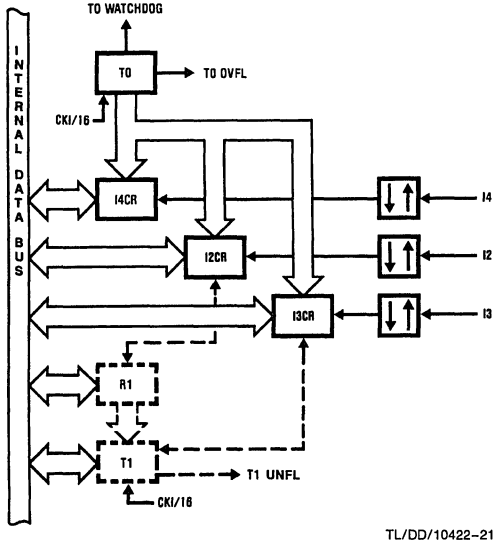
The timers T2 and T3 have selectable clock rates. The clock input to these two timers may be selected from the following two sources: an external pin, or derived internally by dividing the clock input. Timer T2 has additional capability of being clocked by the timer T3 underflow. This allows the user to cascade timers T3 and T2 into a 32-bit timer/counter. The control register DIVBY programs the clock input to timers T2 and T3 (see *Figure 12*).

Timer Overview (Continued)



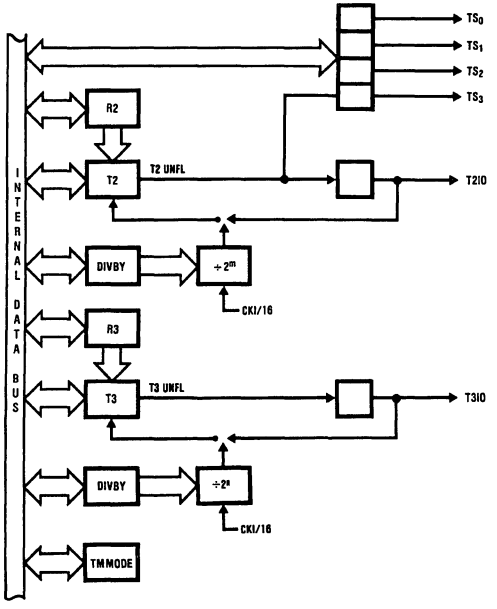
TL/DD/10422–19

FIGURE 10. Interrupt Enable Logic



TL/DD/10422–21

FIGURE 11. Timers T0–T1 Block



TL/DD/10422–20

FIGURE 12. Timers T2–T3 Block

2

Timer Overview (Continued)

The timers T1 through T3 in conjunction with their registers form Timer-Register pairs. The registers hold the pulse duration values. All the Timer-Register pairs can be read from or written to. Each timer can be started or stopped under software control. Once enabled, the timers count down, and upon underflow, the contents of its associated register are automatically loaded into the timer.

SYNCHRONOUS OUTPUTS

The flexible timer structure of the HPC16400E simplifies pulse generation and measurement. There are four synchronous timer outputs (TS0 through TS3) that work in conjunction with the timer T2. The synchronous timer outputs can be used either as regular outputs or individually programmed to toggle on timer T2 underflows (see *Figure 12*). Maximum output frequency for any timer output can be obtained by setting timer/register pair to zero. This then will produce an output frequency equal to ½ the frequency of the source used for clocking the timer.

Timer Registers

There are four control registers that program the timers. The divide by (DIVBY) register programs the clock input to timers T2 and T3. The timer mode register (TMMODE) contains control bits to start and stop timers T1 through T3. It also contains bits to latch, acknowledge and enable interrupts from timers T0 through T3.

Timer Applications

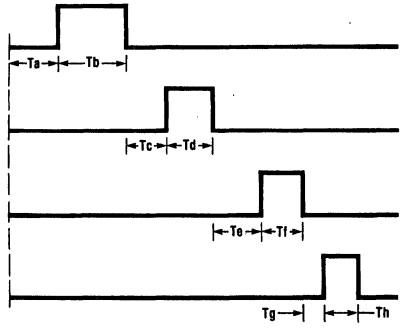
The use of Pulse Width Timers for the generation of various waveforms is easily accomplished by the HPC16400E.

Frequencies can be generated by using the timer/register pairs. A square wave is generated when the register value is a constant. The duty cycle can be controlled simply by changing the register value.

TL/DD/10422–22

FIGURE 13. Square Wave Frequency Generation

Synchronous outputs based on Timer T2 can be generated on the 4 outputs TS0–TS3. Each output can be individually programmed to toggle on T2 underflow. Register R2 contains the time delay between events. *Figure 14* is an example of synchronous pulse train generation.



TL/DD/10422–23

FIGURE 14. Synchronous Pulse Generation

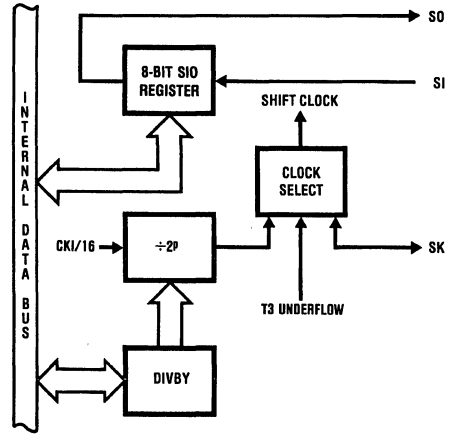
Watch Dog Logic

The Watch Dog Logic monitors the operations taking place and signals upon the occurrence of any illegal activity. The illegal conditions that trigger the Watch Dog logic are potentially infinite loops. Should the Watch Dog register not be written to before Timer T0 overflows twice, or more often than once every 4096 counts, an infinite loop condition is assumed to have occurred. The illegal condition forces the Watch Out (WO) pin low. The WO pin is an open drain output and can be connected to the RESET or NMI inputs or to the users external logic.

MICROWIRE/PLUS

MICROWIRE/PLUS is used for synchronous serial data communications (see *Figure 15*). MICROWIRE/PLUS has an 8-bit parallel-loaded, serial shift register using SI as the input and SO as the output. SK is the clock for the serial shift register (SIO). The SK clock signal can be provided by an internal or external source. The internal clock rate is programmable by the DIVBY register. A DONE flag indicates when the data shift is completed.

The MICROWIRE/PLUS capability enables it to interface with any of National Semiconductor's MICROWIRE peripherals (i.e., ISDN Transceivers, A/D converters, display drivers, EEPROMs).



TL/DD/10422–24

FIGURE 15. MICROWIRE/PLUS

MICROWIRE/PLUS Operation

The HPC16400E can enter the MICROWIRE/PLUS mode as the master or a slave. A control bit in the IRCD register determines whether the HPC16400E is the master or slave. The shift clock is generated when the HPC16400E is configured as a master. An externally generated shift clock on the SK pin is used when the HPC16400E is configured as a slave. When the HPC16400E is a master, the DIVBY register programs the frequency of the SK clock. The DIVBY register allows the SK clock frequency to be programmed in 14 selectable steps from 122 Hz to 1 MHz with CKI at 16 MHz.

The contents of the SIO register may be accessed through any of the memory access instructions. Data waiting to be transmitted in the SIO register is shifted out on the falling edge of the SK clock. Serial data on the SI pin is latched in on the rising edge of the SK clock.

HPC16400E UART

The HPC16400E contains a software programmable UART. The UART (see *Figure 16*) consists of a transmit shift register, a receiver shift register and five addressable registers, as follows: a transmit buffer register (TBUF), a receiver buffer register (RBUF), a UART control and status register (ENU), a UART receive control and status register (ENUR) and a UART interrupt and clock source register (ENUI). The ENU register contains flags for transmit and receive functions; this register also determines the length of the data frame (7, 8 or 9 bits) and the value of the ninth bit in transmission. The ENUR register flags framing, parity, and data overrun errors while the UART is receiving. Other functions of the ENUR register include saving the ninth bit received in the data frame, reporting receiving and transmitting status, and enabling or disabling the UART's Wake-up Mode of operation. The determination of an internal or external clock source is done by the ENUI register, as well as selecting the number of stop bits (7/8, 1, 1 7/8, 2), selecting between the synchronous or asynchronous mode and enabling or disabling transmit and receive interrupts.

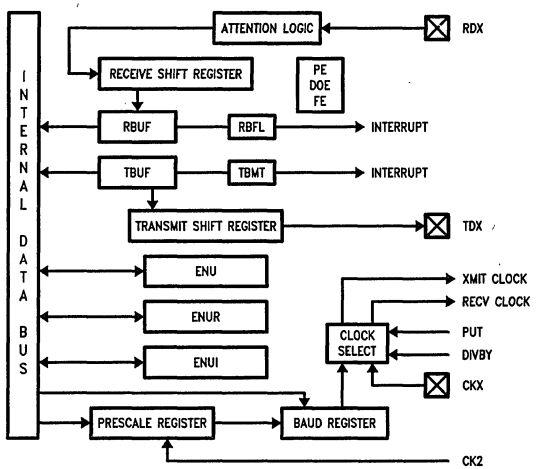
The clock inputs to the Transmitter and Receiver sections of the UART can be individually selected to come from either an off-chip source on the CKX pin or one of the three on-chip sources. Presently, two of the on-chip sources, the Divide-By (DIVBY) Register and the Precision UART Timer (PUT), are primarily for reasons of upward compatibility from earlier HPC family members. The most flexible and accurate on-chip clocking is provided by the third source: the Baud Rate Generator (BRG).

The Baud Rate Generator is controlled by the register pair PSR and BAUD, shown below.

The Prescaler factor is selected by the upper 5 bits of the PSR register (the PRESCALE field), in units of the CK2 clock from 1 to 16 in 1/2 step increments. The lower 3 bits of the PSR register, in conjunction with the 8 bits of the baud register, form the 11-bit BAUDRATE field, which defines a baud rate divisor ranging from 1 to 2048, in units of the prescaled clock selected by the PRESCALE field.

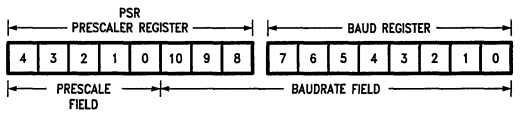
In Asynchronous Mode, the resulting baud rate is 1/16 of the clocking rate selected through the BRG circuit. The maximum baud rate generated using the BRG is 625 kbaud.

In the Synchronous Mode data is transmitted on the rising edge and received on the falling edge of the external clock. Although the data is transmitted and received synchronously, it is still contained within an asynchronous frame; i.e., a start bit, parity bit (if selected) and stop bit(s) are still present.



TL/DD/10422-25

FIGURE 16. UART Block Diagram



TL/DD/10422-26

UART Baud Rate Generator (BRG) Registers PSR and BAUD

UART Attention Mode

The HPC16400E UART features an Attention Mode of operation. This mode of operation enables the HPC16400E to be networked with other processors. Typically in such environments, the messages consist of addresses and actual data. Addresses are specified by having the ninth bit in the data frame set to 1. Data in the message is specified by having the ninth bit in the data frame reset to 0.

The UART monitors the communication stream looking for addresses. When the data word with the ninth bit set is received, the UART signals the HPC16400E with an interrupt. The processor then examines the content of the receiver buffer to decide whether it has been addressed and whether to accept subsequent data.

Programmable Serial Decoder Interface

The programmable serial decoder interface allows the two HDLC channels to be used with devices employing several popular Time Division Multiplexing (TDM) serial protocols for point-to-point and multipoint data exchanges. These protocols combine the 'B' and 'D' channels onto common pins—received data, transmit data, clock and Sync, which normally occurs at an 8 KHz rate and provides framing for the particular protocol.

The decoder uses the serial link clock and Sync signals to generate internal enables for the 'D' and 'B' channels, thereby allowing the HDLC channels to access the appropriate channel data from the multiplexed link.

Additionally, 64 kbit/s to 56 kbits/s rate adaptation can be done using the Serial Decoder generated enable signals B1 or B2. The rate adaption to 56 kbits/s is accomplished by using only the first 7 bits of each B channel time slot for each TDM frame. The transmitter will insert a "1" in the eighth bit of each frame. The receiver will only receive the first seven data bits and skip the eighth bit. See *Figure 17* 65 kbit/56 kbit Rate Adaption Timing Diagram.

HDLC Channel Description

HDLC/DMA Structure

HDLC 1		HDLC 2	
HDLC1 Receive	HDLC1 Transmit	HDLC2 Receive	HDLC2 Transmit
DMAR1	DMAT1	DMAR2	DMAT2

GENERAL INFORMATION

Both HDLC channels on the HPC16400E are identical and operate up to 4.65 Mbps. When used in an ISDN Basic Rate access application, HDLC channel #1 has been designated for use with the 16 kbps D-channel or either B channel and HDLC #2 can be used with either of the 64 kbps B-channels. If the 'D' and 'B' channels are present on a common serial link, the programmable serial decoder interface generates the necessary enable signals needed to access the D and B channel data.

There are two sources for the receive and transmit channel enable signals. They can be internally generated from the serial decoder interface or they can be externally enabled.

LAPD, the Link Access Protocol for the D channel is derived from the X.25 packet switching LAPB protocol. LAPD specifies the procedure for a terminal to use the D channel for the transfer of call control or user-data information. The procedure is used in both point-to-point and point-to-multipoint configurations. On the 16400E, the HDLC controller contains user programmable features that allow for the efficient processing of LAPD Information.

HDLC Channel Pin Description

Each HDLC channel has the following pins associated with it.

HCK — HDLC Channel Clock Input Signal.

RX — Receive Serial Data Input. Data latched on the negative HCK edge.

REN/RHCK — HDLC Channel Receiver Enable Input/Receiver Clock Input.

TEN — HDLC Channel Transmitter Enable Input.

TX — Transmit Serial Data Output. Data clocked out on the positive HCK edge. Data (not including CRC) is sent LSB first. TRI-STATE when transmitter not enabled.

CFLG1 — Closing Flag output for Channel 1.

HDLC Functional Description

TRANSMITTER DESCRIPTION

Data is transferred from external memory through the DMA controller into the transmit buffer register, from which it is loaded into a 8-bit serial shift register. The CRC is computed and appended to the frame prior to the closing flag being transmitted. Data is output at the TX output pin. If no further transmit commands are given the transmitter sends out continous flags, aborts, or the idle pattern as selected by the control register.

An interrupt is generated when the DMA has transferred the last byte from RAM to the HDLC channel for a particular message or on a transmit error condition. An associated transmit status register will contain the status information indicating the specific interrupt source.

To support transmitting data packets at an "R" interface for V.120 in synchronous UI mode, to support the use of the HPC in test equipment, or to support proprietary CRC algorithms the transmitter has the option of preventing the transmitting of the hardware generated CRC bytes.

TRANSMITTER FEATURES

Interframe fill: the transmitter can send either continuous '1's or repeated flags or aborts between the closing flag of one packet and the opening flag of the next. When the CPU commands the transmitter to open a new frame, the interframe fill is terminated immediately.

Abort: the abort sequence, a zero followed by seven ones, will be immediately sent on command from the CPU or on an underrun condition in the DMA.

Bit/Byte boundaries: The message length between packet headers may have any number of bits and is not confined to an integral number of bytes. Three bits in the control register are used to indicate the number of valid bits in the last byte. These bits are loaded by the users software.

RECEIVER DESCRIPTION

Data is input to the receiver on the RX pin. The receive clock can be externally input at either the HCK pin or the REN/RHCK pin.

Incoming data is routed through one of several paths depending on whether it is the flag, data, or CRC.

Once the receiver is enabled it waits for the opening flag of the incoming frame, then starts the zero bit deletion, ad-

HDLC Functional Description (Continued)

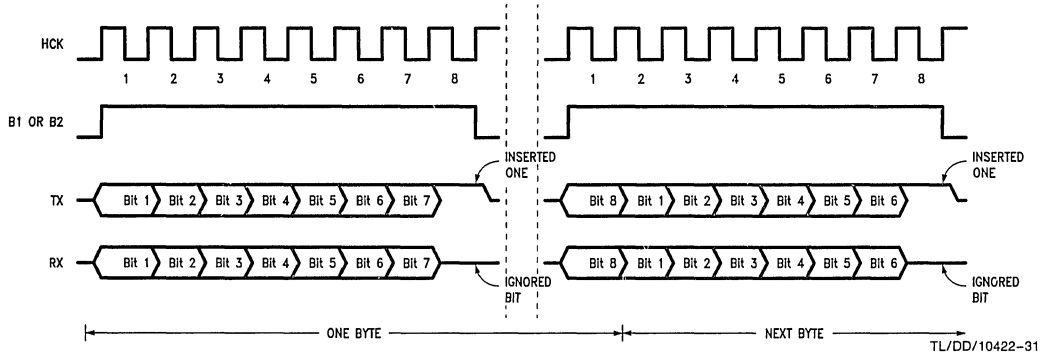


FIGURE 17. 64 kbit/56 kbit Rate Adaption Timing Diagram

dressing handling and CRC checking. All data between the flags is shifted through two 8-bit serial shift registers before being loaded into the buffer register. The user programmable address register values are compared to the incoming data while it resides in the shift registers. If an address match occurs or if operating in the transparent address recognition mode, the DMA channel is signaled that attention is required and the data is transferred by it to external memory. Appropriate interrupts are generated to the CPU on the reception of a complete frame, or on the occurance of a frame error.

The receive interrupt, in conjunction with status data in the control registers allows interrupts to be generated on the following conditions—frame length error, CRC error, receive error, abort and receive complete.

To support V.120 UI data packets at the "R" interface, proprietary CRC algorithms, and test equipment the two bytes preceding the closing flag (usually the CRC bytes) will be loaded into registers. The two bytes can then be read by the CPU and placed into memory. The DMA address pointers used for that particular message will already contain the address that the first byte should be placed into.

RECEIVER FEATURES

Flag sharing: the closing flag of one packet may be shared as the opening flag of the next. Receiver will also be able to share a zero between flags—011111101111110 is a valid two flag sequence for receive (not transmit).

Interframe fill: the receiver automatically accepts either repeated flags, repeated aborts, or all '1's as the interframe fill.

Idle: Reception of successive flags as the interframe fill sequence to be signaled to the user by setting the Flag bit in the Receiver Status register.

Short Frame Rejection: Reception of greater than 2 bytes but less than 4 bytes between flags will generate a frame error, terminating reception of the current frame and setting the Frame Error (FER) status bit in the Receive Control and Status register. Reception of less than 2 bytes will be ignored.

Abort: the 7 '1's abort sequence will be immediately recognized and will cause the receiver to reinitialize and return to searching the incoming data for an opening flag. Reception of the abort will cause the abort status bit in the Interrupt Error Status register to be set and will signal an End of Message (EOMR).

Bit/Byte boundaries: The message length between packet headers may have any number of bits and it is not confined to an integral number of bytes. Three bits in the status register are used to indicate the number of valid bits in the last byte.

Address Recognition: Two user programmable bytes are available to allow frame address recognition on the two bytes immediately following the opening flag. When the received address matches the programmed value(s), the frame is passed through to the DMA channel. If no match occurs, the received frame address information is disregarded and the receiver returns to searching for the next opening flag and the address recognition process starts anew.

Support is provided to allow recognition of the Broadcast address. Additionally, a transparent mode of operation is available where no address decoding is done.

HDLC INTERRUPT CONDITIONS

The end of message interrupt (EOM) indicates that a complete frame has been received or transmitted by the HDLC controller. Thus, there are four separate sources for this interrupt, two each from each HDLC channel. The Message Control Register contains the pending bits for each source.

HDLC ERROR DETECTION

The HDLC/DMA detects several error conditions and reports them in the two Error Status Registers. These conditions are a DMA transmitter underrun, a DMA receiver overrun, a CRC error, a frame too long, a frame too short, and an aborted message.

HDLC CHANNEL CLOCK

Each HDLC channel uses the falling edge of the clock to sample the receive data. Outgoing transmit data is shifted out on the rising edge of the external clock. The maximum data rate when using the externally provided clocks is 4.65 Mb/s.

The receiver/transmitter pair can share a single clock input to save I/O pins, or the inputs can be separated to allow different receive and transmit clocks. This feature allows the receiver and transmitter to operate at different frequencies or enables them to each be synchronized to different parts of the user's system.

CYCLIC REDUNDACY CHECK

There are two standard CRC codes used in generating the 16-bit Frame Check Sequence (FCS) that is appended to the end of the data frame. Both codes are supported and

HDLC Functional Description (Continued)

the user selects the error checking code to be used through software control (HDLC control reg). The two error checking polynomials available are:

(1) CRC-16 ($x^{16} + x^{15} + x^2 + 1$)

(2) CCITT CRC ($x^{16} + x^{12} + x^5 + 1$)

SYNCHRONOUS BYPASS MODE

When the BYPAS bit is set in the HDLC control register, all HDLC framing/formatting functions for the specified HDLC channel are disabled.

This allows byte-oriented data to be transmitted and received synchronously thus "bypassing" the HDLC functions.

LOOP BACK OPERATIONAL MODE

The user has the ability, by setting the appropriate bit in the register to internally route the transmitter output to the receiver input, and to internally route the RX pin to the TX pin.

DMA Controller

GENERAL INFORMATION

The HPC16400E uses Direct Memory Access (DMA) logic to facilitate data transfer between the 2 full Duplex HDLC channels and external packet RAM. There are four DMA channels to support the four individual HDLC channels. Control of the DMA channels is accomplished through registers which are configured by the CPU. These control registers define specific operation of each channel and changes are immediately reflected in DMA operation. In addition to individual control registers, global control bits (MSS and MSSC in Message Control Register) are available so that the HDLC channels may be globally controlled.

The DMA issues a bus request to the CPU when one or more of the individual HDLC channels request service. Upon receiving a bus acknowledge from the CPU, the DMA completes all requests pending and any requests that may have occurred during DMA operation before returning control to the CPU. If no further DMA transfers are pending, the DMA relinquishes the bus and the CPU can again initiate a bus cycle.

Four memory expansion bits have been added for each of the four channels to support data transfers into the expanded memory bank areas.

The DMA has priority logic for servicing DMA requests. The priorities are:

1st priority ..... Receiver channel 1
2nd priority ..... Transmit channel 1
3rd priority ..... Receive channel 2
4th priority ..... Transmit channel 2

RECEIVER DMA OPERATION

The receiver DMA consists of a shift register and two buffers. A receiver DMA operation is initiated by the buffer registers. Once a byte has been placed in a buffer register from the HDLC, it generates a request and upon obtaining control of the bus, the DMA places the byte in external memory.

RECEIVER REGISTERS

All the following registers are Read/Write

A. Frame Length Register

This user programmable 16-bit register contains the maximum number of bytes to be placed in a data "block". If this number is exceeded, a Frame Too Long error is generated. DMA is stopped to prevent memory from being overwritten, however the receiver continues until the closing flag is received in order to check the CRC.

B. CNTRL ADDR 1
DATA ADDR 1
CNTRL ADDR 2
DATA ADDR 2

For split frame operation, the CNTRL ADDR register contains the external memory address where the Frame Header (Control & Address fields) are to be stored and the DATA ADDR register contains an equivalent address for the Information field.

For non-split frame operation, the CNTRL and DATA ADDR registers each contain the external memory address for entire frames.

TRANSMITTER DMA OPERATION

The transmitter DMA consists of a shift register and two buffers. A transmitter DMA cycle is initiated by the TX data buffers. The TX data buffers generate a request when either one is empty and the DMA responds by placing a byte in the buffer. The HDLC transmitter can then accept the byte to send when needed, upon which the DMA will issue another request, resulting in a subsequent DMA cycle.

TRANSMITTER REGISTERS

The following registers are Read/Write:

FIELD ADDRESS 1
BYTE COUNT 1
FIELD ADDRESS 2
BYTE COUNT 2

Field Address 1 and Field Address 2 are starting addresses of blocks of information to be transmitted.

Byte Count 1 and Byte Count 2 are the number of bytes in the block to be transmitted.

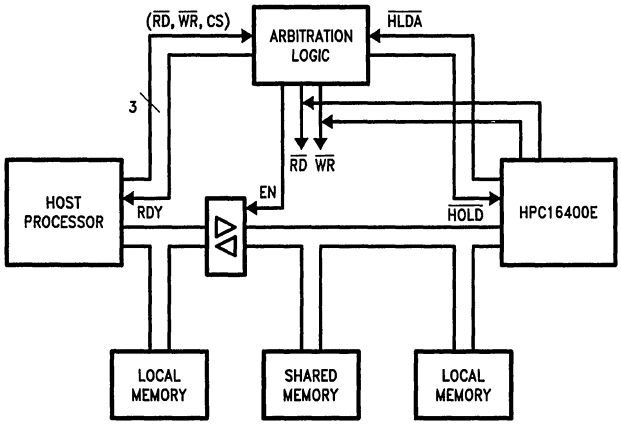
Shared Memory Support

Shared memory access provides a rapid technique to exchange data. It is effective when data is moved from a peripheral to memory or when data is moved between blocks of memory. A related area where shared memory access proves effective is in multiprocessing applications where two CPUs share a common memory block. The HPC16400E supports shared memory access with two pins. The pins are the RDY/$\overline{\text{HLD}}$ input pin and the $\overline{\text{HLDA}}$ output pin. The user can software select either the Hold or Ready function on the RDY/$\overline{\text{HLD}}$ pin by the state of a control bit. The $\overline{\text{HLDA}}$ output must be selected as the $\overline{\text{HLDA}}$ output on pin B7 by software.

The host uses DMA to interface with the HPC16400E. The host initiates a data transfer by activating the $\overline{\text{HLD}}$ input of the HPC16400E. In response, the HPC16400E places its system bus in a TRI-STATE Mode, freeing it for use by the host. The host waits for the acknowledge signal ($\overline{\text{HLDA}}$) from the HPC16400E indicating that the sytem bus is free. On receiving the acknowledge, the host can rapidly transfer data into, or out of, the shared memory by using a conventional DMA controller. Upon completion of the message transfer, the host removes the HOLD request and the HPC16400E resumes normal operations. See *Figure 18* (HPC16400E shared Memory Using HOLD).

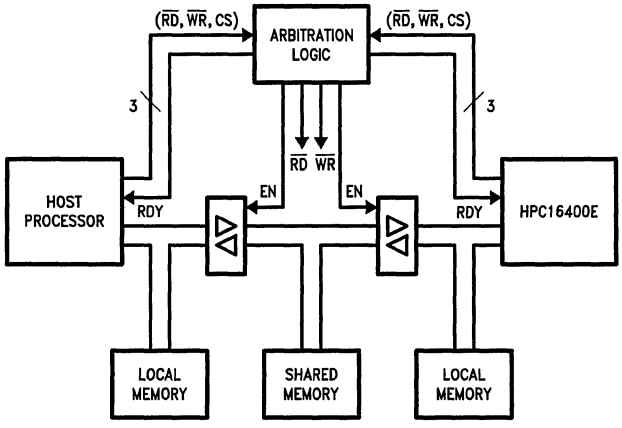
An alternate approach is to use the Ready function available on either the RDY/$\overline{\text{HLD}}$ pin or the INT4/RDY pin. See *Figure 19* (HPC16400E Shared Memory Using READY). This technique is often required when the HPC is sharing memory over a system backplane bus.

Shared Memory Support (Continued)



TL/DD/10422–27

FIGURE 18. HPC16400E Shared Memory Using HOLD



TL/DD/10422–28

FIGURE 19. HPC16400E Shared Memory Using READY

2

Memory

The HPC16400E has been designed to offer flexibility in memory usage. A total address space of 64 kbytes can be addressed with 256 bytes of RAM available on the chip itself.

Program memory addressing is accomplished by the 16-bit program counter on a byte basis. Memory can be addressed directly by instructions or indirectly through the B, X and SP registers. Memory can be addressed as words or bytes. Words are always accessed on even-byte boundaries. The HPC16400E uses memory-mapped organization to support registers, I/O and on-chip peripheral functions.

The HPC16400E memory address space extends to 64 kbytes and registers and I/O are mapped as shown in Table II.

Extended Memory Addressing

If more than 64k of addressing is desired in a HPC16400E system, on board bank select circuitry is available that allows four I/O lines of Port B (B8, B9, B13, B14) to be used in extending the address range. This gives the user a main routine area of 32k and 16 banks of 32k each for subroutine and data, thus getting a total of 536.5k of memory.

Note: If all four lines are not needed for memory expansion, the unused lines can be used as general purpose inputs.

The Extended Memory Addressing mode is entered by setting the EMA control bit in the Message Control Register. If this bit is not set, the port B lines (B8, B9, B13, B14) are available as general purpose I/O or synchronous outputs as selected by the BFUN register.

The main memory area contains the interrupt vectors & service routines, stack memory, and common memory for the bank subroutines to use. The 16 banks of memory can contain program or data memory (note: since the on chip resources are mapped into addresses 0000-01FF, the first 512 bytes of each bank are not usable, actual available memory is 536.5k).

TABLE II. Memory Map

FFFF–FFF0 FFEF–FFD0	Interrupt Vectors JSRP Vectors	
FFCF–FFCE : : 0201–0200	External Expansion	USER MEMORY
01FF–01FE : : 01C1–01C0	On Chip RAM	USER RAM
01BC 01BA 01B8 01B6 01B4 01B2 01B0	CRC Byte 2 CRC Byte 1 Error Status Receiver Status Cntrl Recr Addr Comp Reg 2 Recr Addr Comp Reg 1	HDLC # 2
01AC 01AA 01A8 01A6 01A4 01A2 01A0	CRC Byte 2 CRC Byte 1 Error Status Receiver Status Cntrl Recr Addr Comp Reg 2 Recr Addr Comp Reg 1	HDLC # 1
0195–0194	Watch Dog Register	Watch Dog Logic
0193–0192 0191–0190 018F–018E 018D–018C 018B–018A 0189–0188 0187–0186 0185–0184 0183–0182 0181–0180	T0CON Register TMMODE Register DIVBY Register T3 Timer R3 Register T2 Timer R2 Register I2CR Register/ R1 I3CR Register/ T1 I4CR Register	Timer Block T0–T3
017F–017E 017D–017C	Baud Counter Baud Register	UART Timer
0179–0178 0177–0176 0175–0174 0173–0172 0171–0170	Byte Count 2 Field Addr 2 Byte Count 1 Field Addr 1 Xmit Cntrl & Status	DMAT # 2 (Xmit)
016B–016A 0169–0168 0167–0166 0165–0164 0163–0162 0161–0160	Frame Length Data Addr 2 Cntrl Addr 2 Data Addr 1 Cntrl Addr 1 Recv Cntrl & Status	DMAR # 2 (Recv)
0159–0158 0157–0156 0155–0154 0153–0152 0151–0150	# Bytes 2 Field Addr 2 # Bytes 1 Field Addr 1 Xmit Cntrl & Status	DMAT # 1 (Xmit)
014B–014A 0149–0148 0147–0146 0145–0144 0143–0142 0141–0140	Frame Length Data Addr 2 Cntrl Addr 2 Data Addr 1 Cntrl Addr 1 Recv Cntrl & Status	DMAR # 1 (Recv)
012C 012A 0128 0126 0124 0122 0120	Baud PSR - Prescaler ENUR Register TBUF Register RBUF Register ENUI Register ENU Register	UART
010E 010C 010A 0108 0106 0104 0102 0100	Port R Pins DIR R Register Port R Data Register Message System Configuration Serial Decoder/Enable Configuration Reg Message Pending Message System Control Port D Input	PORTS R & D
00F5–00F4 00F3–00F2 00E6 00E3–00E2	BFUN Register DIR B Register Chip Revision Register Port B	PORT B
00DD–00DC 00D8 00D6 00D4 00D2 00D0	Halt Enable Register Port I Input Register SIO Register IRCD Register IRPD Register ENIR Register	PORT CONTROL & INTERRUPT CONTROL REGISTERS
00CF–00CE 00CD–00CC 00CB–00CA 00C9–00C8 00C7–00C6 00C5–00C4 00C3–00C2 00C0	X Register B Register K Register A Register PC Register SP Register (Reserved) PSW Register	HPC CORE REGISTERS
00BF–00BE : : 0001–0000	On Chip RAM	USER RAM

Note: All unused addresses are reserved by National Semiconductor

Design Considerations

Designs using the HPC family of 16-bit high speed CMOS microcontrollers need to follow some general guidelines on usage and board layout.

Floating inputs are a frequently overlooked problem. CMOS inputs have extremely high impedance and, if left open, can float to any voltage possibly causing internal devices to go into active mode and draw DC current. You should thus tie unused inputs to V_{CC} or ground, either through a resistor or directly. Unlike the inputs, unused outputs should be left floating to allow the output to switch without drawing any DC current.

To reduce voltage transients, keep the supply line's parasitic inductances as low as possible by reducing trace lengths, using wide traces, ground planes, and by decoupling the supply with bypass capacitors. In order to prevent additional voltage spiking, this local bypass capacitor must exhibit low inductive reactance. You should therefore use high frequency ceramic capacitors and place them very near the IC to minimize wiring inductance.

- Keep V_{CC} bus routing short. When using double sided or multilayer circuit boards, use ground plane techniques.
- Keep ground lines short, and on PC boards make them as wide as possible, even if trace width varies. Use separate ground traces to supply high current devices such as relay and transmission line drivers.
- In systems mixing linear and logic functions and where supply noise is critical to the analog components' performance, provide separate supply buses or even separate supplies.
- When using local regulators, bypass their inputs with a tantalum capacitor of at least 1 μF and bypass their outputs with a 10 μF to 50 μF tantalum or aluminum electrolytic capacitor.
- If the system uses a centralized regulated power supply, use a 10 μF to 20 μF tantalum electrolytic capacitor or a 50 μF to 100 μF aluminum electrolytic capacitor to decouple the V_{CC} bus connected to the circuit board.
- Provide localized decoupling. For random logic, a rule of thumb dictates approximately 10 nF (spaced within 12 cm) per every two to five packages, and 100 nF for every 10 packages. You can group these capacitances, but it's more effective to distribute them among the ICs. If the design has a fair amount of synchronous logic with outputs that tend to switch simultaneously, additional decoupling might be advisable. Octal flip-flop and buffers in bus-oriented circuits might also require more decoupling. Note that wire-wrapped circuits can require more decoupling than ground plane or multilayer PC boards.

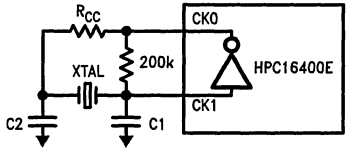
A recommended crystal oscillator circuit to be used with the HPC is shown below. See table for recommended component values. The recommended values given in the table below have yielded consistent results and are made to match a crystal with a 20 pF load capacitance, with some small allowance for layout capacitance.

A recommended layout for the oscillator network should be as close to the processor as physically possible, entirely within 1" distance. This is to reduce lead inductance from long PC traces, as well as interference from other components, and reduce trace capacitance. The layout should contain a large ground plane either on the top or bottom surface of the board to provide signal shielding, and a convenient location to ground both the HPC, and the case of the crystal.

It is very critical to have an extremely clean power supply for the HPC crystal oscillator. Ideally one would like a V_{CC} and ground plane that provide low inductance power lines to the chip. The power planes in the PC board should be decoupled with three decoupling capacitors as close to the chip as possible. A 1.0 μF, a 0.1 μF, and a 0.001 μF dipped mica or ceramic cap mounted as close to the HPC as is physically possible on the board, using the shortest leads, or surface mount components. This should provide a stable power supply, and noiseless ground plane which will vastly improve the performance of the crystal oscillator network.

HPC Oscillator Table

f_C (MHz)	R_{CC} (Ω)	C1 (pF)	C2 (pF)
2	50	82	100
4	50	62	75
6	50	50	56
8	50	47	50
10	50	39	50
12	0	39	39
14	0	33	39
16	0	33	39
18	0	33	33
20	0	33	33



TL/DD/10422-29

Crystal Specifications:
"AT" cut, parallel resonant crystals tuned to the desired frequency with the following specifications are recommended:

Series Resistance < 65Ω

Loading Capacitance: C_L = 20 pF

2

HPC16400E CPU

The HPC16400E CPU has a 16-bit ALU and six 16-bit registers.

Arithmetic Logic Unit (ALU)

The ALU is 16 bits wide and can do 16-bit add, subtract and shift or logic AND, OR and exclusive OR in one timing cycle. The ALU can also output the carry bit to a 1-bit C register.

Accumulator (A) Register

The 16-bit A register is the source and destination register for most I/O, arithmetic, logic and data memory access operations.

Address (B and X) Registers

The 16-bit B and X registers can be used for indirect addressing. They can automatically count up or down to sequence through data memory.

Boundary (K) Register

The 16-bit K register is used to set limits in repetitive loops of code as register B sequences through data memory.

Stack Pointer (SP) Register

The 16-bit SP register is the stack pointer that addresses the stack. The SP register is incremented by two for each push or call and decremented by two for each pop or return. The stack can be placed anywhere in user memory and be as deep as the available memory permits.

Program (PC) Register

The 16-bit PC register addresses program memory.

Addressing Modes

ADDRESSING MODES—ACCUMULATOR AS DESTINATION

Register Indirect

This is the "normal" mode of addressing for the HPC16400E (instructions are single-byte). The operand is the memory addressed by the B register (or X register for some instructions).

Direct

The instruction contains an 8-bit or 16-bit address field that directly points to the memory for the operand.

Indirect

The instruction contains an 8-bit address field. The contents of the WORD addressed points to the memory for the operand.

Indexed

The instruction contains an 8-bit address field and an 8- or 16-bit displacement field. The contents of the WORD addressed is added to the displacement to get the address of the operand.

Immediate

The instruction contains an 8-bit or 16-bit immediate field that is used as the operand.

Register Indirect (Auto Increment and Decrement)

The operand is the memory addressed by the X register. This mode automatically increments or decrements the X register (by 1 for bytes and by 2 for words).

Register Indirect (Auto Increment and Decrement) with Conditional Skip

The operand is the memory addressed by the B register. This mode automatically increments or decrements the B register (by 1 for bytes and by 2 for words). The B register is then compared with the K register. A skip condition is generated if B goes past K.

ADDRESSING MODES—DIRECT MEMORY AS DESTINATION

Direct Memory to Direct Memory

The instruction contains two 8- or 16-bit address fields. One field directly points to the source operand and the other field directly points to the destination operand.

Immediate to Direct Memory

The instruction contains an 8- or 16-bit address field and an 8- or 16-bit immediate field. The immediate field is the operand and the direct field is the destination.

Double Register Indirect using the B and X Registers

Used only with Reset, Set and IF bit instructions; a specific bit within the 64 kbyte address range is addressed using the B and X registers. The address of a byte of memory is formed by adding the contents of the B register to the most significant 13 bits of the X register. The specific bit to be modified or tested within the byte of memory is selected using the least significant 3 bits of register X.

HPC Instruction Set Description

Mnemonic	Description	Action	
ARITHMETIC INSTRUCTIONS			
ADD	Add	MA + Meml → MA	carry → C
ADDS	Add short imm8	MA + imm8 → MA	carry → C
ADC	Add with carry	MA + Meml + C → MA	carry → C
DADC	Decimal add with carry	MA + Meml + C → MA (Decimal)	carry → C
SUBC	Subtract with carry	MA − Meml + C → MA	carry → C
DSUBC	Decimal subtract w/carry	MA − Meml + C → MA (Decimal)	carry → C
MULT	Multiply (unsigned)	MA*Meml → MA & X, 0 → K, 0 → C	
DIV	Divide (unsigned)	MA/Meml → MA, rem. → X, 0 → K, 0 → C	
DIVD	Divide Double Word (unsigned)	(x8 MA)/Meml → MA, rem → X, 0 → K	carry → C
IFEQ	If equal	Compare MA & Meml, Do next if equal	
IFGT	If greater than	Compare MA & Meml, Do next if MA → Meml	
AND	Logical and	MA and Meml → MA	
OR	Logical or	MA or Meml → MA	
XOR	Logical exclusive-or	MA xor Meml → MA	
MEMORY MODIFY INSTRUCTIONS			
INC	Increment	Mem + 1 → Mem	
DECSZ	Decrement, skip if 0	Mem − 1 → Mem, Skip next if Mem = 0	
BIT INSTRUCTIONS			
SBIT	Set bit	1 → Mem.bit (bit is 0 to 7 immediate)	
RBIT	Reset bit	0 → Mem.bit	
IFBIT	If bit	If Mem.bit is true, do next instr.	
MEMORY TRANSFER INSTRUCTIONS			
LD	Load	Meml → MA	
	Load, incr/decr X	Mem(X) → A, X ±1 (or 2) → X	
ST	Store to Memory	MA → Mem	
X	Exchange	A ↔ Mem; Mem ↔ Mem	
	Exchange, incr/decr X	A ↔ Mem(X), X ±1 (or 2) → X	
PUSH	Push Memory to Stack	W → W(SP), SP + 2 → SP	
POP	Pop Stack to Memory	SP − 2 → SP, W(SP) → W	
LDS	Load A, incr/decr B, Skip on condition	Mem(B) → A, B ±1 (or 2) → B, Skip next if B greater/less than K	
XS	Exchange, incr/decr B, Skip on condition	Mem(B) ↔ A,B ±1 (or 2) → B, Skip next if B greater/less than K	
REGISTER LOAD IMMEDIATE INSTRUCTIONS			
LD A	Load A immediate	imm → A	
LD B	Load B immediate	imm → B	
LD K	Load K immediate	imm → K	
LD X	Load X immediate	imm → X	
LD BK	Load B and K immediate	imm → B,imm → K	
ACCUMULATOR AND C INSTRUCTIONS			
CLR A	Clear A	0 → A	
INC A	Increment A	A + 1 → A	
DEC A	Decrement A	A − 1 → A	
COMP A	Complement A	1's complement of A → A	
SWAP A	Swap nibbles of A	A15:12 ← A11:8 ← A7:4 ↔ A3:0	
RRC A	Rotate A right thru C	C → A15 → ... → A0 → C	
RLC A	Rotate A left thru C	C ← A15 ← ... ← A0 ← C	
SHR A	Shift A right	0 → A15 → ... → A0 → C	
SHL A	Shift A left	C ← A15 ← ... ← A0 ← 0	
SC	Set C	1 → C	
RC	Reset C	0 → C	
IFC	IF C	Do next if C = 1	
IFNC	IF not C	Do next if C = 0	

HPC Instruction Set Description (Continued)

Mnemonic	Description	Action
TRANSFER OF CONTROL INSTRUCTIONS		
JSRP	Jump subroutine from table	PC → W(SP),SP+2 → SP W(table#) → PC
JSR	Jump subroutine relative	PC → W(SP),SP+2 → SP,PC+ # → PC (#is +1024 to −1023)
JSRL	Jump subroutine long	PC → W(SP),SP+2 → SP,PC+ # → PC
JP	Jump relative short	PC+ # → PC(# is +32 to −31)
JMP	Jump relative	PC+ # → PC(#is +256 to −255)
JMPL	Jump relative long	PC+ # → PC
JID	Jump indirect at PC + A	PC+A+1 → PC
JIDW		then Mem(PC)+PC → PC
NOP	No Operation	PC ← PC + 1
RET	Return	SP−2 → SP,W(SP) → PC
RETS	Return then skip next	SP−2 → SP,W(SP) → PC, & skip
RETI	Return from interrupt	SP−2 → SP,W(SP) → PC, interrupt re-enabled

Note: W is 16-bit word of memory
MA is Accumulator A or direct memory (8 or 16-bit)
Mem is 8-bit byte or 16-bit word of memory
Meml is 8- or 16-bit memory or 8 or 16-bit immediate data
imm is 8-bit or 16-bit immediate data

Memory Usage

For information on memory usage and instruction timing please refer to the HPC16400E User's Manual (see page 25 for ordering information).

Code Efficiency

The HPC16400E has been designed to be extremely code-efficient. The HPC16400E looks very good in all the standard coding benchmarks; however, it is not realistic to rely only on benchmarks. Many large jobs have been programmed onto the HPC16400E, and the code savings over other popular microcontrollers has been considerable.

Reasons for this saving of code include the following:

SINGLE BYTE INSTRUCTIONS

The majority of instructions on the HPC16400E are single-byte. There are two especially code-saving instructions:

JP is a 1-byte jump. True, it can only jump within a range of plus or minus 32, but many loops and decisions are often within a small range of program memory. Most other micros need 2-byte instructions for any short jumps.

JSRP is a 1-byte call subroutine. The user makes a table of his 16 most frequently called subroutines and these calls will only take one byte. Most other micros require two and even three bytes to call a subroutine. The user does not have to decide which subroutine addresses to put into his table; the assembler can give him this information.

EFFICIENT SUBROUTINE CALLS

The 2-byte JSR instructions can call any subroutine within plus or minus 1k of program memory.

MULTIFUNCTION INSTRUCTIONS FOR DATA MOVEMENT AND PROGRAM LOOPING

The HPC16400E has single-byte instructions that perform multiple tasks. For example, the XS instruction will do the following:

1. Exchange A and memory pointed to by the B register
2. Increment or decrement the B register
3. Compare the B register to the K register
4. Generate a conditional skip if B has passed K

The value of this multipurpose instruction becomes evident when looping through sequential areas of memory and exiting when the loop is finished.

BIT MANIPULATION INSTRUCTIONS

Any bit of memory, I/O or registers can be set, reset or tested by the single byte bit instructions. The bits can be addressed directly or indirectly. Since all registers and I/O are mapped into the memory, it is very easy to manipulate specific bits to do efficient control.

DECIMAL ADD AND SUBTRACT

This instruction is needed to interface with the decimal user world.

It can handle both 16-bit words and 8-bit bytes.

The 16-bit capability saves code since many variables can be stored as one piece of data and the programmer does not have to break his data into two bytes. Many applications store most data in 4-digit variables. The HPC16400E supplies 8-bit byte capability for 2-digit variables and literal variables.

MULTIPLY AND DIVIDE INSTRUCTIONS

The HPC16400E has 16-bit multiply, 16-bit by 16-bit divide, and 32-bit by 16-bit divide instructions. This saves both code and time. Multiply and divide can use immediate data or data from memory. The ability to multiply and divide by immediate data saves code since this function is often needed for scaling, base conversion, computing indexes of arrays, etc.

Part Selection

The HPC family includes devices with many different options and configurations to meet various application needs. The number HPC16400E has been generally used throughout this datasheet to represent the whole family of parts. The following chart explains how to order various options available when ordering HPC family members.

Note: All options may not currently be available.

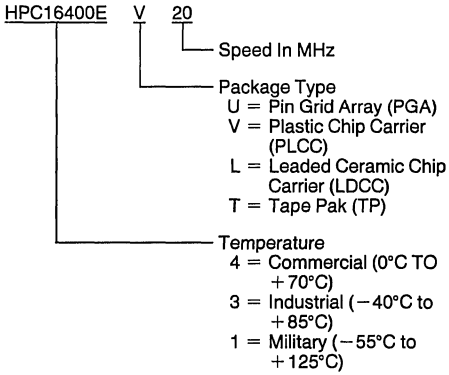


FIGURE 15. HPC Family Part Numbering Scheme

EXAMPLES

HPC46400EV20—Commercial temp (0° to +70°C), PLCC

HPC36400EV20—Industrial temp (−40°C to +85°C), PLCC

Development Support

HPC DEVELOPMENT SYSTEM

The HPC Development System is an in-system emulator (ISE) designed to support National Semiconductor's entire family of HPC microcontrollers. The complete package of hardware and software tools, when combined with an IBM or compatible PC, provides a powerful tool for the development of High Performance microcontroller based products.

The stand alone unit comes complete with vertically mounted circuit boards, a power supply, and an external emulation pod. It is packaged in a UL approved, fan cooled steel case. The unit can be connected to a PC host via an RS-232 link. The software package includes a C compiler, linker, cross assembler, librarian, operating manuals and a source level debugger program.

The ISE provides fully transparent in-circuit emulation at speeds up to 20 MHz 1 waitstate. A 2K word (48-bit wide) real-time trace assists in the non-instrusive monitoring of the system. EPROM programming can be done through the use of the externally mounted EPROM socket. On-line help functions and a diagnostics option allow the user to reduce his programming and debugging time. 8 hardware breakpoints (address/range located), 64 kbytes of user memory, and 8 external trace lines are some of the other features designed into the kit.

Development Tools Selection Table

Microcontroller	Order Part Number	Description	Includes
HPC16400E	HPC-DEV-ISE2	HPC In-System Emulator with PLCC Pod Cable	HPC Microcontroller Development System Manual HPC16400E/HPC46400E User's Manual
	HPC-DEV-IBMC	C-Compiler for IBM PC and Compatibles	C-Compiler Manual Assembler Manual
	HPC-DEV-IBMA	Relocatable Assembler Software for IBM PC and Compatibles	Assembler Manual
	HPC-DEV-WDBC	C Source/Symbolic Debugger with MS-Windows	Debugger User's Manual

Support Documents

Description	Order Number
HPC16400E User's Manual	420420213-001

Development Support (Continued)

DIAL-A-HELPER

Dial-A-Helper is a service provided by the Microcontroller Applications Group. Dial-A-Helper is an electronic bulletin board information system and additionally, provides the capability of remotely accessing the development system at a customer site.

INFORMATION SYSTEM

The Dial-A-Helper system provides access to an automated information storage and retrieval system that may be accessed over standard dial-up telephone lines 24 hours a day. The system capabilities include a MESSAGE SECTION (electronic mail) for communications to and from the Microcontroller Applications Group and a FILE SECTION which consists of several file areas where valuable application software and utilities can be found. The minimum requirement for accessing Dial-A-Helper is a Hayes compatible modem.

If the user has a PC with a communications package then files from the FILE SECTION can be down loaded to disk for later use.

Order P/N: MOLE-DIAL-A-HLP

Information System Package Contains:
- Dial-A-Helper Users Manual
- Public Domain Communications Software

FACTORY APPLICATIONS SUPPORT

Dial-A-Helper also provides immediate factory applications support. If a user is having difficulty in operating a development system, he can leave messages on our electronic bulletin board, which we will respond to.

Voice: (408) 721-5582
Modem: (408) 739-1162
Baud: 300 or 1200 baud
Set-Up: Length: 8-Bit
Parity: None
Stop Bit: 1
Operation: 24 Hrs, 7 Days

Section 3

Analog Telephone Components

Section 3 Contents

TP5088 DTMF Generator for Binary Data 3-3
TP5089 DTMF (Touch-Tone) Generator 3-7
TP5700A Telephone Speech Circuit 3-11

National Semiconductor

TP5088 DTMF Generator for Binary Data

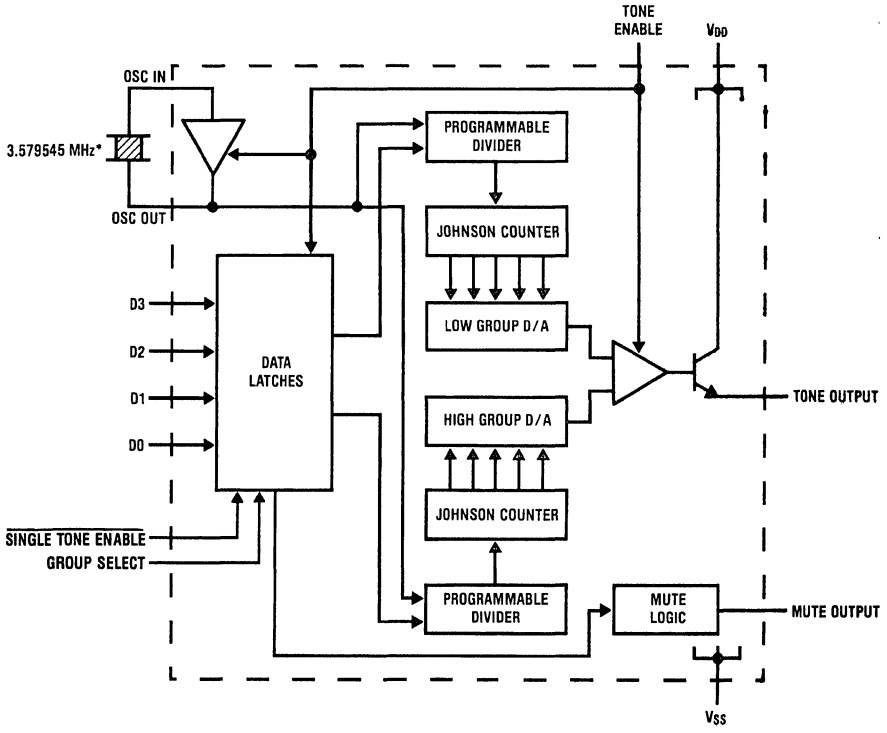
General Description

This CMOS device provides low cost tone-dialing capability in microprocessor-controlled telephone applications. 4-bit binary data is decoded directly, without the need for conversion to simulated keyboard inputs required by standard DTMF generators. With the TONE ENABLE input low, the oscillator is inhibited and the device is in a low power idle mode. On the low-to-high transition of TONE ENABLE, data is latched into the device and the selected tone pair from the standard DTMF frequencies is generated. An open-drain N-channel transistor provides a MUTE output during tone generation.

Features

- Direct microprocessor interface
- Binary data inputs with latches
- Generates 16 standard tone pairs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Better than 0.64% frequency accuracy
- High group pre-emphasis
- Low harmonic distortion
- MUTE output interfaces to speech network
- Low power idle mode
- 3.5V–8V operation

Block Diagram



TL/H/5004–1

*Crystal Specification: Parallel Resonant 3.579545 MHz, $R_S \leq 150\Omega$, L = 100 mH, C_0 = 5 pF, C_1 = 0.02 pF.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{DD}-V_{SS}$)	12V
$\overline{\text{MUTE}}$ Voltage	12V
Maximum Voltage at Any Other Pin	V_{DD} + 0.3V to V_{SS} − 0.3V
Operating Temperature, T_A	−30°C to +70°C
Storage Temperature	−55°C to +150°C
Maximum Power Dissipation	500 mW

Electrical Characteristics

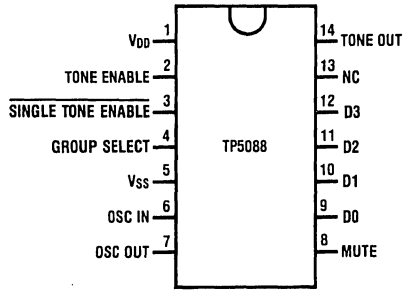
Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = 3.5V to 8V, T_A = 0°C to +70°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage, V_{DD} (min)	Generating Tones	**3.5**			V
Minimum Supply Voltage for Data Input, TONE ENABLE and MUTE Logic Functions		2			V
Operating Current Idle Generating Tones	 R_L = ∞, D0–D3 Open V_{DD} = 3.5V, Mute Open		 55 1.5	 **350** **2.5**	 μA mA
Input Pull-Up Resistance D0–D3 TONE ENABLE			 100 50		 kΩ kΩ
Input Low Level TONE ENABLE, D0–D3				**0.2 V_{DD}**	 V
Input High Level TONE ENABLE, D0–D3		**0.8 V_{DD}**			 V
MUTE OUT Sink Current (TONE ENABLE LOW)	V_{DD} = 3.5V V_o = 0.5V	**0.4**			mA
MUTE OUT Leakage Current (TONE ENABLE HIGH)	V_{DD} = 3.5V V_o = V_{DD}		1		μA
Output Amplitudes Low Group High Group	R_L = 240 Ω V_{DD} = 3.5V T_A = 25°C	 **130** **180**	 170 230	 **220** **310**	 mVrms mVrms
Mean Output DC Offset	V_{DD} = 3.5V V_{DD} = 8V		1.2 3.6		V V
High Group Pre-Emphasis		**2.2**	2.7	**3.2**	dB
Dual Tone/Total Harmonic Distortion Ratio	1 MHz Bandwidth, V_{DD} = 5V R_L = 240Ω	**−20**			dB
Start-Up Time (to 90% Amplitude), t_{OSC}			4		ms
Data Set-Up Time, t_S (*Figure 2*)	V_{DD} = 5V	100			ns
Data Hold Time, t_H	V_{DD} = 5V	280			ns
Data Duration t_W	V_{DD} = 5V	600			ns

Note 1: R_L is the external load resistor connected from TONE OUT to V_{SS}.

Connection Diagram

Dual-In-Line Package



TL/H/5004–2

Top View

Order Number TP5088WM or TP5088N
See NS Package M14B or N14A

Functional Description

With the TONE ENABLE pin pulled low, the device is in a low power idle mode, with the oscillator inhibited and the output transistor turned off. Data on inputs D0–D3 is ignored until a rising transition on TONE ENABLE. Data meeting the timing specifications is latched in, the oscillator and output stage are enabled, and tone generation begins. The decoded data sets the high group and low group programmable counters to the appropriate divide ratios. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine wave cycle. On-chip regulators ensure good stability of tone amplitudes with variations in supply voltage and temperature. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}.

Table I shows the accuracies of the tone output frequencies and Table II is the Functional Truth Table.

TABLE I. Output Frequency Accuracy

Tone Group	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	697	694.8	−0.32
	770	770.1	+0.02
	852	852.4	+0.03
	941	940.0	−0.11
High Group f_H	1209	1206.0	−0.24
	1336	1331.7	−0.32
	1477	1486.5	+0.64
	1633	1639.0	+0.37

Pin Descriptions

V_{DD} (Pin 1): This is the positive supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is also connected to this pin.

V_{SS} (Pin 5): This is the negative voltage supply. All voltages are referenced to this pin.

OSC IN, OSC OUT (Pins 6 and 7): All tone generation timing is derived from the on-chip oscillator circuit. A low-cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 6 and 7. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator is stopped when the TONE ENABLE input is pulled to logic low.

TONE ENABLE Input (Pin 2): This input has an internal pull-up resistor. When TONE ENABLE is pulled to logic low, the oscillator is inhibited and the tone generators and output transistor are turned off. A low to high transition on TONE ENABLE latches in data from D0–D3. The oscillator starts, and tone generation continues until TONE ENABLE is pulled low again.

MUTE (Pin 8): This output is an open-drain N-channel device that sinks current to V_{SS} when TONE ENABLE is low and no tones are being generated. The device turns off when TONE ENABLE is high.

D0, D1, D2, D3 (Pins 9, 10, 11, 12): These are the inputs for binary-coded data, which is latched in on the rising edge of TONE ENABLE. Data must meet the timing specifications of *Figure 2*. At all other times these inputs are ignored and may be multiplexed with other system functions.

TONE OUT (Pin 14): This output is the open emitter of an NPN transistor, the collector of which is connected internally to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group tones superimposed on a DC offset. When not generating tones, this output transistor is turned off to minimize the device idle current.

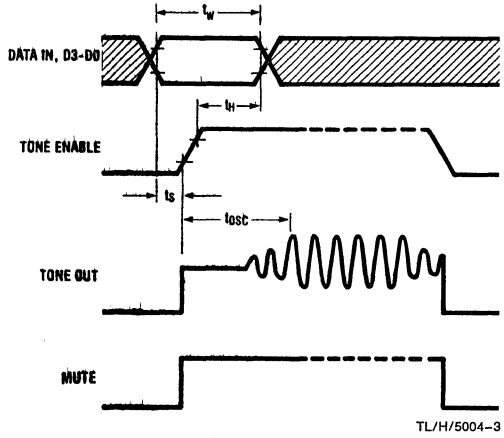
$\overline{\text{SINGLE TONE ENABLE}}$ (Pin 3): This input has an internal pull-up resistor. When pulled to V_{SS}, the device is in single tone mode and only a single tone will be generated at pin 14 (for testing purposes). For normal operation, leave this pin open-circuit or pull to V_{DD}.

GROUP SELECT (Pin 4): This pin is used to select the high group or low group frequency when the device is in single tone mode. It has an internal pull-up resistor. Leaving this pin open-circuit or pulling it to V_{DD} will generate the high group, while pulling to V_{SS} will generate the low group frequency at the TONE OUT pin.

TABLE II. Functional Truth Table

Keyboard Equivalent	Data Inputs				TONE ENABLE	TONES OUT		MUTE
	D3	D2	D1	D0		f_L (Hz)	f_H(Hz)	
X	X	X	X	X	0	0V	0V	0V
1	0	0	0	1	⎍	697	1209	O/C
2	0	0	1	0	⎍	697	1336	O/C
3	0	0	1	1	⎍	697	1477	O/C
4	0	1	0	0	⎍	770	1209	O/C
5	0	1	0	1	⎍	770	1336	O/C
6	0	1	1	0	⎍	770	1477	O/C
7	0	1	1	1	⎍	852	1209	O/C
8	1	0	0	0	⎍	852	1336	O/C
9	1	0	0	1	⎍	852	1477	O/C
0	1	0	1	0	⎍	941	1336	O/C
*	1	0	1	1	⎍	941	1209	O/C
#	1	1	0	0	⎍	941	1477	O/C
A	1	1	0	1	⎍	697	1633	O/C
B	1	1	1	0	⎍	770	1633	O/C
C	1	1	1	1	⎍	852	1633	O/C
D	0	0	0	0	⎍	941	1633	O/C

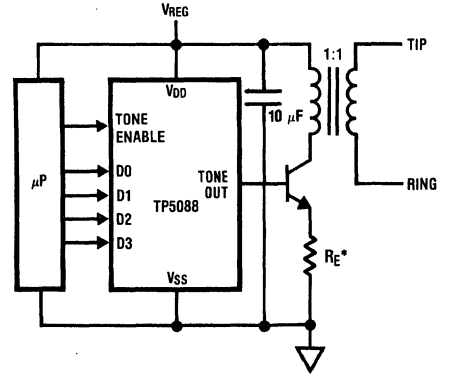
Timing Diagram



TL/H/5004–3

FIGURE 2

Typical Application



TL/H/5004–4

*Adjust R_E for desired tone amplitude.

FIGURE 3

National Semiconductor

TP5089 DTMF (TOUCH-TONE) Generator

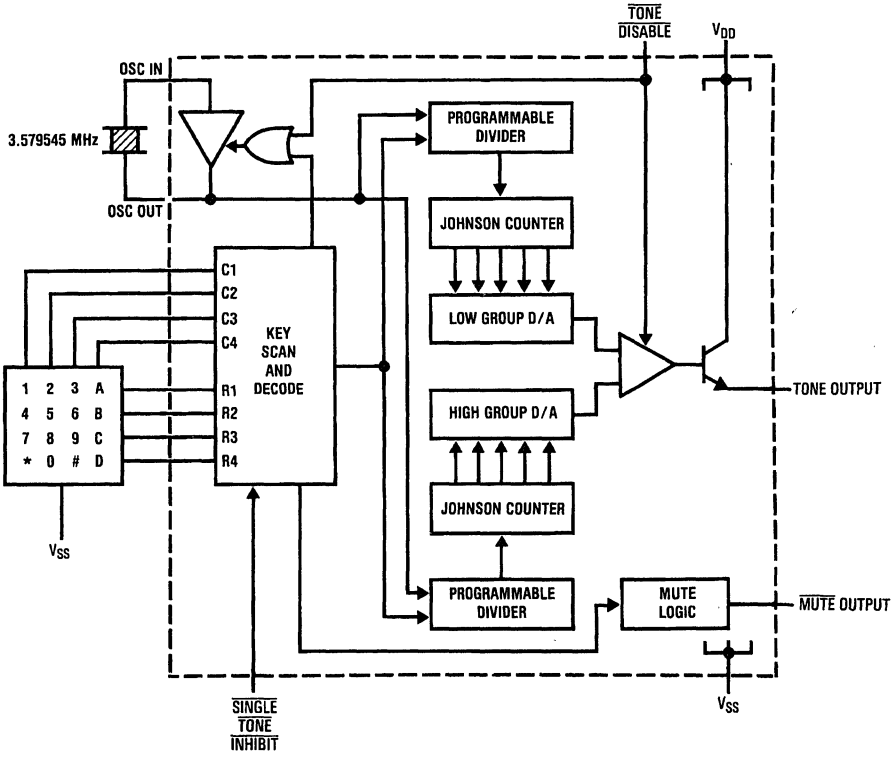
General Description

The TP5089 is a low threshold voltage, field-implanted, metal gate CMOS integrated circuit. It interfaces directly to a standard telephone keypad and generates all dual tone multi-frequency pairs required in tone-dialing systems. The tone synthesizers are locked to an on-chip reference oscillator using an inexpensive 3.579545 MHz crystal for high tone accuracy. The crystal and an output load resistor are the only external components required for tone generation. A $\overline{\text{MUTE}}$ OUT logic signal, which changes state when any key is depressed, is also provided.

Features

- 3.5V–10V operation when generating tones
- 2V operation of keyscan and $\overline{\text{MUTE}}$ logic
- Static sensing of key closures or logic inputs
- On-chip 3.579545 MHz crystal-controlled oscillator
- Output amplitudes proportional to supply voltage
- High group pre-emphasis
- Low harmonic distortion
- Open emitter-follower low-impedance output
- $\overline{\text{SINGLE TONE INHIBIT}}$ pin

Block Diagram



TL/H/5057–1

FIGURE 1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V_{DD} - V_{SS}$) 15V

Maximum Voltage at Any Pin $V_{DD} + 0.3V$ to $V_{SS} - 0.3V$

Operating Temperature $-30°C$ to $+60°C$

Storage Temperature $-55°C$ to $+150°C$

Maximum Power Dissipation 500 mW

Electrical Characteristics

Unless otherwise noted, limits printed in **BOLD** characters are guaranteed for V_{DD} = 3.5V to 10V, T_A = 0°C to +60°C by correlation with 100% electrical testing at T_A = 25°C. All other limits are assured by correlation with other production tests and/or product design and characterization.

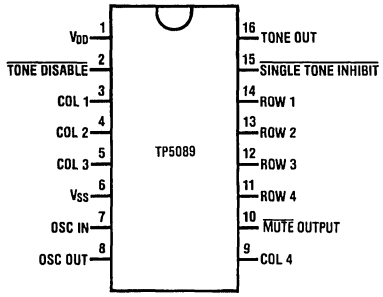
Parameter	Conditions	Min	Typ	Max	Units
Minimum Supply Voltage for Keysense and $\overline{\text{MUTE}}$ Logic Functions		2			V
Minimum Operating Voltage for generating tones		**3.5**			V
Operating Current Idle Generating Tones	Mute open $R_L = \infty$ $V_{DD} = 3.5V$	**25** **2.5**	2 1.1		μA mA
Input Resistors COLUMN and ROW (Pull-Up) $\overline{\text{SINGLE TONE INHIBIT}}$ (Pull-Down) $\overline{\text{TONE DISABLE}}$ (Pull-Up)		 25 120	 50		 kΩ kΩ
Input Low Level				**0.2 V_{DD}**	V
Input High Level		**0.8 V_{DD}**			V
$\overline{\text{MUTE}}$ OUT Sink Current (COLUMN and ROW Active)	$V_{DD} = 3.5V$ $V_o = 0.5V$	**0.4**			mA
$\overline{\text{MUTE}}$ Out Leakage Current	$V_o = V_{DD}$		1		μA
Output Amplitude Low Group	$R_L = 240\ \Omega$ $V_{DD} = 3.5V$	**190**	250	**340**	mVrms
	$R_L = 240\Omega$ $V_{DD} = 10V$	**510**	700	**880**	mVrms
Output Amplitude High Group	$R_L = 240\Omega$ $V_{DD} = 3.5V$	**270**	340	**470**	mVrms
	$R_L = 240\Omega$ $V_{DD} = 10V$	**735**	955	**1265**	mVrms
Mean Output DC Offset	$V_{DD} = 3.5V$ $V_{DD} = 10V$		1.3 4.6		V V
High Group Pre-Emphasis		**2.2**	2.7	**3.2**	dB
Dual Tone/Total Harmonic Distortion Ratio	$V_{DD} = 4V$, $R_L = 240\Omega$ 1 MHz Bandwidth	**−22**	−23		dB
Start-Up Time (to 90% Amplitude)			3	5	mS

Note 1: R_L is the external load resistor connected from TONE OUT to V_{SS}.

Note 2: Crystal specification: Parallel resonant 3.579545 MHz, $R_S \leq 150\ \Omega$, L = 100 mH, C_O = 5 pF, C_I = 0.02 pF.

Connection Diagram

Dual-In-Line Package



TL/H/5057–2

Top View

Order Number TP5089N or TP5089WM
See NS Package N16A and M16B

Pin Descriptions

Symbol	Description
V_{DD}	This is the positive voltage supply to the device, referenced to V_{SS}. The collector of the TONE OUT transistor is connected to this pin.
V_{SS}	This is the negative voltage supply. All voltages are referenced to this pin.
OSC IN, OSC OUT	All tone generation timing is derived from the on-chip oscillator circuit. A low cost 3.579545 MHz A-cut crystal (NTSC TV color-burst) is needed between pins 7 and 8. Load capacitors and a feedback resistor are included on-chip for good start-up and stability. The oscillator stops when column inputs are sensed with no valid input having been detected. The oscillator is also stopped when the $\overline{\text{TONE DISABLE}}$ input is pulled to logic low.
Row and Column Inputs	When no key is pushed, pull-up resistors are active on row and column inputs. A key closure is recognized when a single row and a single column are connected to V_{SS}, which starts the oscillator and initiates tone generation. Negative-true logic signals simulating key closures can also be used.
$\overline{\text{TONE DISABLE}}$ Input	The $\overline{\text{TONE DISABLE}}$ input has an internal pull-up resistor. When this input is open or at logic high, the normal tone output mode will occur. When $\overline{\text{TONE DISABLE}}$ input is at logic low, the device will be in the inactive mode, TONE OUT will be at an open circuit state.
$\overline{\text{MUTE}}$ Output	The $\overline{\text{MUTE}}$ output is an open-drain N-channel device that sinks current to V_{SS} with any key input and is open when no key input is sensed. The $\overline{\text{MUTE}}$ output will switch regardless of the state of the $\overline{\text{SINGLE TONE INHIBIT}}$ input.
$\overline{\text{SINGLE TONE INHIBIT}}$ Input	The $\overline{\text{SINGLE TONE INHIBIT}}$ input is used to inhibit the generation of other than valid tone pairs due to multiple row-column closures. It has a pull-down resistor to V_{SS}, and when left open or tied to V_{SS} any input condition that would normally result in a single tone will now result in no tone, with all other functions operating normally. When tied to V_{DD}, single or dual tones may be generated, see Table II.
TONE OUT	This output is the open emitter of an NPN transistor, the collector of whch is connected to V_{DD}. When an external load resistor is connected from TONE OUT to V_{SS}, the output voltage on this pin is the sum of the high and low group sine-waves superimposed on a DC offset. When not generating tones, this output transistor is turned OFF to minimize the device idle current. Adjustment of the emitter load resistor results in variation of the mean DC current during tone generation, the sinewave signal current through the output transistor, and the output distortion. Increasing values of load resistance decrease both the signal current and distortion.

Functional Description

With no key inputs to the device the oscillator is inhibited, the output transistor is pulled OFF and device current consumption is reduced to a minimum. Key closures are sensed statically. Any key closure activates the $\overline{\text{MUTE}}$ output, starts the oscillator and sets the high group and low group programmable counters to the appropriate divide ratio. These counters sequence two ratioed-capacitor D/A converters through a series of 28 equal duration steps per sine-wave cycle. The two tones are summed by a mixer amplifier, with pre-emphasis applied to the high group tone. The output is an NPN emitter-follower requiring the addition of an external load resistor to V_{SS}. This resistor facilitates adjustment of the signal current flowing from V_{DD} through the output transistor.

The amplitude of the output tones is directly proportional to the device supply voltage.

Functional Description (Continued)

TABLE I. Output Frequency Accuracy

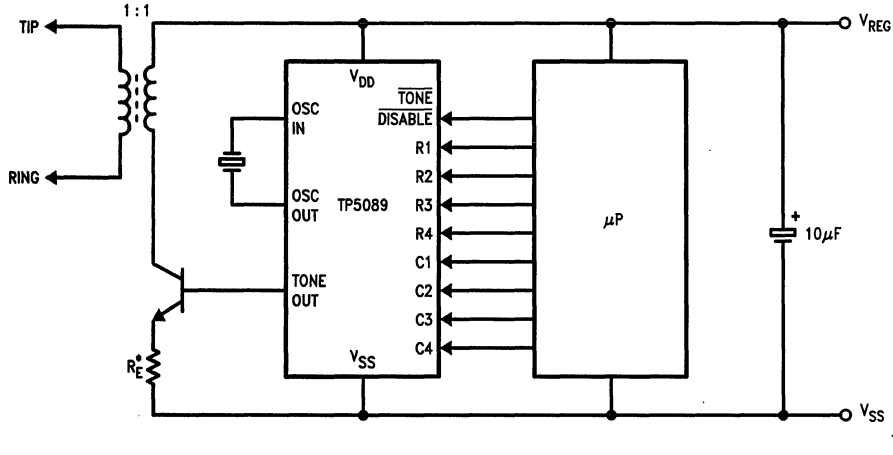
Tone Group	Valid Input	Standard DTMF (Hz)	Tone Output Frequency	% Deviation from Standard
Low Group f_L	R1	697	694.8	−0.32
	R2	770	770.1	+0.02
	R3	852	852.4	+0.03
	R4	941	940.0	−0.11
High Group f_H	C1	1209	1206.0	−0.24
	C2	1336	1331.7	−0.32
	C3	1477	1486.5	+0.64
	C4	1633	1639.0	+0.37

TABLE II. Functional Truth Table

$\overline{\text{SINGLE TONE}}$ $\overline{\text{INHIBIT}}$	$\overline{\text{TONE}}$ $\overline{\text{DISABLE}}$	ROW	COLUMN	TONE OUT		MUTE
				Low	High	
X	0	O/C	O/C	0V	0V	O/C
X	X	O/C	O/C	0V	0V	O/C
X	0	One	One	V_{OS}	V_{OS}	O
X	1	One	One	f_L	f_H	O
1	1	2 or More	One	—	f_H	O
1	1	One	2 or More	f_L	—	O
1	1	2 or More	2 or More	V_{OS}	V_{OS}	O
0	1	2 or More	One	V_{OS}	V_{OS}	O
0	1	One	2 or More	V_{OS}	V_{OS}	O
0	1	2 or More	2 or More	V_{OS}	V_{OS}	O

Note 1: X is don't care state.

Note 2: V_{OS} is the output offset voltage.



TL/H/5057–3

*Adjust R_E for desired tone amplitude.

FIGURE 2. Typical Application

National Semiconductor

TP5700A
Telephone Speech Circuit

General Description

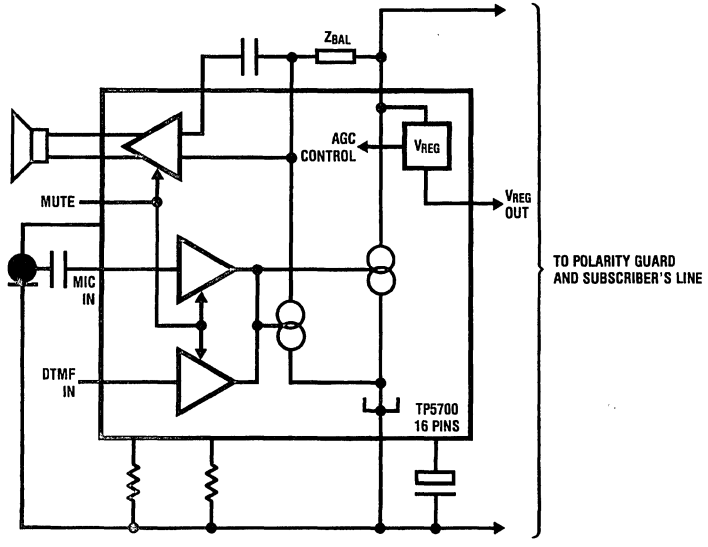
The TP5700A is a linear bipolar device which includes all the functions required to build the speech circuit of a telephone. It replaces the hybrid transformer, compensation circuit and sidetone network used in traditional designs. When used with an electret microphone (with integral FET buffer) and dynamic receiver, superior audio linearity, distortion and noise performance are obtained. Loop attenuation compensation is also included.

The low voltage design enables the circuit to work over a wide range of operating conditions, including long loops, extension telephones and subscriber carrier applications. Operating power is derived from the telephone line.

Features

- 5 mA–120 mA loop operation
- Voltage swing down to 1.0V
- Electret microphone amplifier
- Receive amplifier with push-pull outputs
- Automatic gain compensation for loop length
- Sidetone impedance independent of input impedance
- DTMF interface with muting
- Voltage regulator outputs for DTMF generator etc.
- Works in parallel with a standard phone on 20 mA loop
- Available in small outline surface mount package

Simplified Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

V^+ with Respect to V^-	20V
Voltage at Any Other Pin	$V^+ + 0.3V$ to $V^- - 0.3V$
Operating Temperature, T_A	−25°C to +70°C
Power Dissipation (Note 3)	1W
Storage Temperature, T_S	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

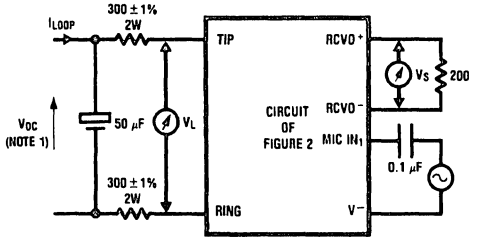
Unless otherwise specified, all tests based on the test circuits shown in *Figure 1*, all limits printed in bold characters are guaranteed at T_A = 0°C to +60°C by correlation with 100% testing at T_A = 25°C. All other limits are assured by by correlation with other production tests, and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{T-R}	Tip-Ring Voltage including nominal 1.4V polarity guard (See *Figure 1*)	I_{LOOP} = 5 mA = 20 mA = 50 mA = 80 mA = 120 mA		2.8 7 10.5 15	**4.5**	V V V V V
V_I	Minimum Instantaneous Voltage Swing	V^+ to V^- $I_{LOOP} \geq$ 5mA		1.0		V
TRANSMIT AMPLIFIER						
R_{XIN}	Input Resistance	From Pin 7 to V^-	15	30	50	kΩ
G_{XA}	Gain at 1 kHz	R_{AGC} = 0Ω to V^- I_{LOOP} = 20 mA, T_A = 25°C only	**33**	35	**37**	dB
G_{XT}	Gain Variation v. T_A			±1		dB
G_{XI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
N_X	Transmit Noise	MIC IN_1 = 0V		12	**18**	dBrnC
S/D_X	Signal/Total Harmonic Distortion	$I_{LOOP} \geq$ 20 mA V_L = 800 mVrms		2	10	%
G_{XM}	Gain Change when MUTED	MUTE IN $\geq V_{MON}$		−55		dB
DTMF AMPLIFIER						
R_{DIN}	Input Resistance	From Pin 8 to V^-	10	20	55	kΩ
G_{XD}	Gain at 1 kHz	R_{AGC} = 0Ω to V^- I_{LOOP} = 20 mA, T_A = 25°C only	**3.5**	5.5	**7.5**	dB
S/D_{XD}	Signal/Total Harmonic Distortion	I_{LOOP} = 20 mA V_L = 1.06 Vrms, T_A = 25°C only		3	**10**	%
G_{XDT}	Gain Variation v. T_A			±1		dB
G_{XDI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
MUTE INPUT						
I_{MIN}	Input Current	Pin 9 = 1.5V		40		μA
V_{MOFF}	MUTE OFF Input Voltage				0.5	V
V_{MON}	MUTE ON Input Voltage		1.5			V

DC Electrical Characteristics (Continued)

Unless otherwise specified, all tests based on the test circuits shown in *Figure 1*, all limits printed in bold characters are guaranteed at T_A = 0°C to +60°C by correlation with 100% testing at T_A = 25°C. All other limits are assured by by correlation with other production tests, and/or product design and characterization.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
RECEIVE AMPLIFIER						
R_{RIN}	Input Resistance	From Pin 12 to V⁻	20	35	55	kΩ
G_{RA}	Gain at 1 kHz	R_{AGC} = 0Ω, MUTE IN ≤ V_{MOFF} I_{LOOP} = 20 mA, T_A = 25°C only	**−5.5**	−4	**−2.5**	dB
G_{RT}	Gain Variation v. T_A			±0.5		dB
G_{RI}	Gain Variation v. I_{LOOP}	I_{LOOP} = 20 to 100 mA		−6		dB
G_{RM}	Gain Change when MUTED	MUTE IN ≥ V_{MON}	−15	−20	−23	dB
N_R	Receive Noise	V_{RCVIN} = 0V		0	**10**	dBrnC
S/D_R	Signal/Total Harmonic Distortion	V_R = 200 mVrms I_{LOOP} ≥ 20 mA		2	**10**	%
V_RC	Output Clipping Level	I_{LOOP} ≥ 20 mA		1		Vp-p
V_{ROS}	Output Offset Voltage				±100	mV
SIDETONE CHARACTERISTICS						
STC	Sidetone Cancellation at 1kHz	20 mA ≤ I_{LOOP} ≤ 100 mA, (Note 2)	**11**	15		dB
VOLTAGE REGULATOR OUTPUTS						
V_{REG1}	Output Voltage, Pin 10	I_{LOOP} ≥ 20 mA MUTE IN ≤ V_{MOFF} MUTE IN ≥ V_{MON}	 **2** **3**	 3.2		 V V
I_{REG1}	Maximum Output Current, Pin 10	MUTE IN ≤ V_{MOFF} MUTE IN ≥ V_{MON}		200 2.7		μA mA
V_{REG2}	Output Voltage, Pin 11	I_{LOOP} ≥ 20 mA	1.1	1.2		V
I_{REG2}	Maximum Output Current, Pin 11	I_{LOOP} ≥ 20 mA	300	500		μA



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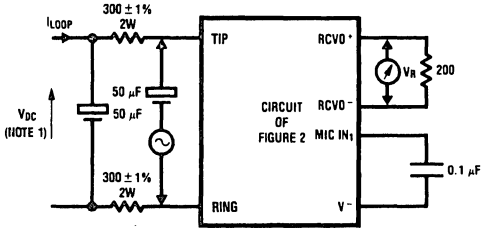
1a. Test Circuit for Transmit and Sidetone



TL/H/5201-3

1b. Test Circuit for Receive

FIGURE 1. Test Circuits for Electrical Characteristics

Note 1. Adjust V_{DC} to set specified I_{LOOP} current.

Note 2. To measure Sidetone Cancellation, set oscillator in *Fig. 1a* for V_L = 100 mVrms; measure V_S. Then in *Fig. 1b* set oscillator = 100 mVrms; measure V_R. STC = 20log V_R/V_S.

Note 3. For operation above 25°C, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 70°C/W junction to ambiant.

Functional Description

The TP5700A Telephone Speech Circuits are powered from the telephone Tip and Ring terminals via a full-wave rectifier bridge to protect against loop polarity reversals. The devices provide the following functions:

LINE REGULATOR

A DC regulator sinks current from the loop in order to maintain a DC slope resistance similar to that of a standard phone.

R_{DC} provides an adjustment for the slope resistance.

MICROPHONE AMPLIFIER

A single-ended input amplifier on the TP5700A enables a low cost electret microphone to be used. This provides superior distortion, linearity and noise performance compared to a traditional carbon microphone. The electret should be capacitively coupled to the amplifier input. The acoustic sensitivity of the microphone is intended to be in the range of −60 to −70 dBV/μBar.

Loss can be inserted if required by adding a resistive potentiometer either at MIC IN_1 or the connection between the pre-amp output and driver stage input. The driver stage pro-

Functional Description (Continued)

vides automatic gain compensation to reduce the gain as loop length decreases. The AGC range can be adjusted by means of R_{AGC} to limit the maximum loss on a short loop from 0 to 6 dB.

RECEIVE AMPLIFIER

This buffer amplifier provides the necessary gain or loss for the receive signal. RCV IN should be AC coupled to SIDETONE (pin 4). Automatic gain control is built into the amplifier to reduce the gain as loop length decreases. The AGC range is adjusted in common with the transmit AGC range with a range of adjustment for maximum loss from 0 to 6 dB. Push-pull complementary outputs provide balanced direct drive to a dynamic transducer, which may have an impedance as low as 100Ω. The effective receive gain can be reduced by adding a resistor in series with the transducer. The receive gain is automatically reduced by 20 dB when the MUTE input is pulled high.

SIDETONE CIRCUIT

The level of Sidetone cancellation may be adjusted by connecting an external balance impedance to SIDETONE (pin 4) and coupling this point to V^+. For good sidetone cancellation the balance impedance should be approximately 10 times the subscriber line input impedance. Some typical component values to match a precise 600Ω termination for test purposes are shown in *Figure 2*. Use the component values shown in the Applications Section for better results over a wide range of telephone line impedances.

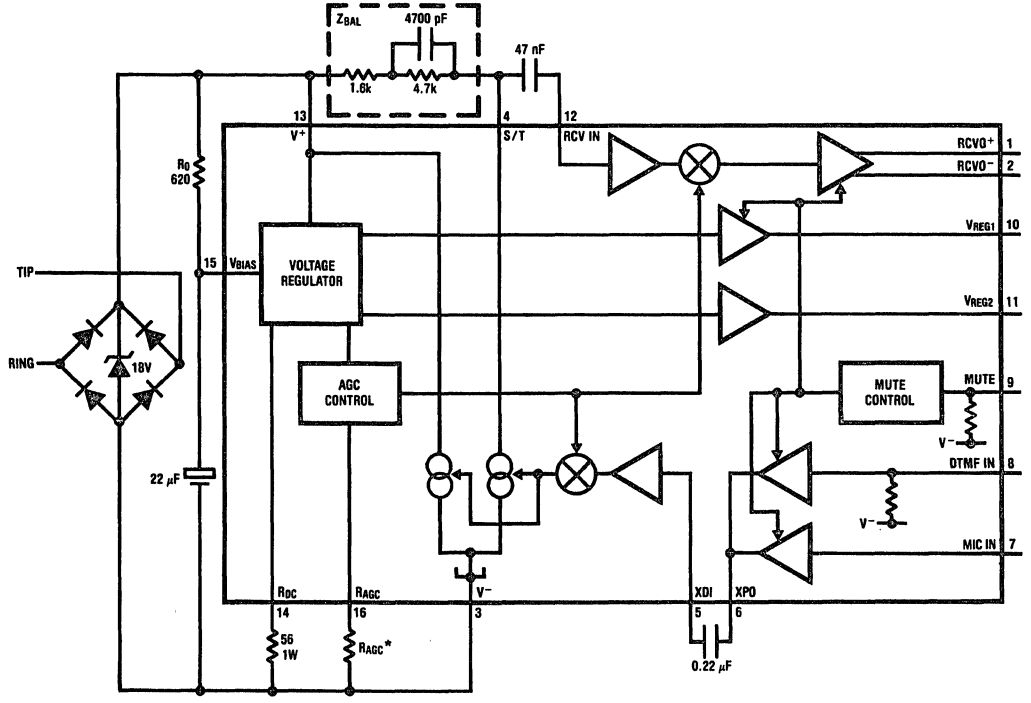
DTMF AMPLIFIER

An additional transmit amplifier is included to enable the open-emitter output of a conventional DTMF generator to be connected to the line via the transmit output stage. This path includes the transmit AGC section. When the MUTE input is pulled high, the DTMF input is enabled and the MIC input disabled. When MUTE IN is open-circuit or pulled to V^- the DTMF input is switched off and the MIC input is enabled.

VOLTAGE REGULATOR OUTPUTS

A precision band-gap voltage reference controls a regulator to provide bias for internal circuits. Two auxiliary outputs are also available. V_{REG1} is provided specifically for powering a low voltage pulse dialer or DTMF generator. In order to protect this output in low voltage situations where the instantaneous voltage across the Speech Circuit may swing below the V_{REG1} output voltage, an internal switch controls the maximum available output current. In speech mode, MUTE IN is low, V_{REG1} output will track approximately ½ the Tip-Ring voltage and the available output current is limited to 200 μA. This is adequate to power a DTMF generator in standby mode. When MUTE IN is pulled high to switch the Speech Circuit to the DTMF dialing mode, V_{REG1} is switched to a 3V regulated output and up to 2 mA may be drawn from it to power the active DTMF generator.

A 1.2V regulated output is also provided at V_{REG2} to power a low voltage 2-wire electret microphone such as the Primo EM80-PMI$_2$.



TL/H/5201–4

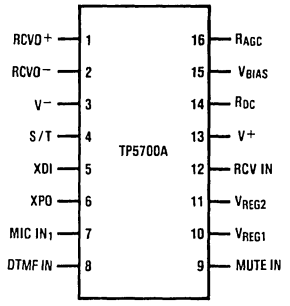
* See Figure 3

Note: Z_{BAL} circuit shown is for test purposes with a resistive line termination. See Applications Information for suggested component values for normal reactive line applications.

FIGURE 2. TP5700A Telephone Speech Circuits

Connection Diagram

Dual-In-Line Package



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Top View

Order Number TP5700AM or TP5700AN
See NS Package M16B or N16A

Pin Descriptions

Pins 1, 2 RCV0+ and RCV0−

The push-pull complementary outputs of the receive amplifier. Dynamic transducers with a minimum impedance of 100 Ω can be directly driven by these outputs.

Pin 3 V−

This is the negative supply input to the device and should be connected to the negative output of the polarity guard. All other voltages on the device are referred to this pin.

Pin 4 S/T

This is the output of the Sidetone cancellation signal, which requires a balance impedance of approximately 10 times the subscriber's line impedance to be connected from this pin to V+ (pin 13).

Pin 5 XDI

The input to the line output driver amplifier. Transmit AGC is applied in this stage.

Pin 6 XPO

This is the transmit pre-amp output which is normally capacitively coupled to pin 5.

Pin 7 MIC IN_1

This is the inverting input to the transmit pre-amplifier and is intended to be capacitively coupled to an FET-buffered electret microphone.

Pin 8 DTMF IN

The DTMF input which has an internal resistor to V− to provide the emitter load resistor for a CMOS DTMF generator. This input is only active when MUTE IN (pin 9) is pulled high.

Pin 9 MUTE IN

The MUTE Input, which must be pulled at least 1.5V higher than V− to mute MIC IN and enable DTMF IN.

Pin 10 V_{REG1}

The regulated output for biasing a pulse dialer or DTMF generator. A 4.7 μF decoupling capacitor to V− should be fitted if this output is used.

Pin 11 V_{REG2}

A 1.2V regulated output suitable for powering a low-voltage electret microphone. A 1μF decoupling capacitor to V− should be fitted if this output is used.

Pin 12 RCV IN

The receive AGC amplifier input.

Pin 13 V+

This is the positive supply input to the device and should be connected to the positive output of the polarity guard. The current through this pin is modulated by the transmit signal.

Pin 14 R_{DC}

An external 1W resistor is required from this pin to V− to control the DC input impedance of the circuit. The nominal value is 56Ω for low voltage operation. Values up to 82Ω may be used to increase the available transmit output voltage swing at the expense of low voltage operation.

Pin 15 V_{BIAS}

This internal voltage bias line must be connected to V+ via an external resistor, R_o, and decoupled to V− with a 22 μF capacitor. R_o dominates the AC input impedance of the circuit and should be 620Ω for a 600Ω input impedance or 910Ω for a 900Ω input impedance.

Pin 16 R_{AGC}

The range of transmit and receive gain variations between short and long loops may be adjusted by connecting a resistor from this pin to V− (pin 3). *Figure 3* shows the relationship between the resistor value and the AGC range. This pin may be left open-circuit to defeat AGC action.

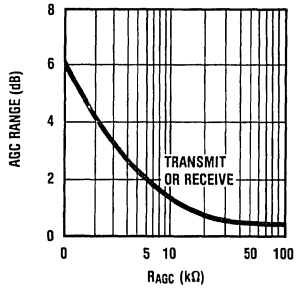

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FIGURE 3

Applications Information

The TP5700A and TP5700 are flexible circuits designed with several user adjustments to enable the performance to be optimized for different applications. The choice of transducer types and the cavities in which they are mounted will also greatly influence the acoustic performance of the telephone. Some of the consequences of circuit adjustments are as follows:

R_{DC} ADJUSTMENT

56Ω is the recommended value for R_{DC} if it is required to meet a maximum Tip-Ring voltage of 4.5V on a 20 mA loop (assuming no more than 1.4V is dropped across the polarity guard). If a higher Tip-Ring voltage is acceptable, R_{DC} may be increased, which will provide a small increase in the available transmit output voltage swing before clipping occurs. R_{DC} should be less than 82Ω to avoid exceeding the maximum rated voltage on a short loop.

R_{AGC} ADJUSTMENT

The available AGC range is more than adequate to compensate for the loss of most loops. R_{AGC} should be chosen only to partly compensate for the anticipated maximum loop loss, as over-compensation may tend to exaggerate the variations of sidetone with loop length.

SIDETONE ADJUSTMENT

The component values used for Z_{BAL} should be selected to provide a clear sidetone sound without excessive "hollowness." The capacitor value and ratio of the two resistors will fix the pole location. To avoid reducing the low voltage performance of the circuit the sum of the two resistors should not exceed 10 kΩ.

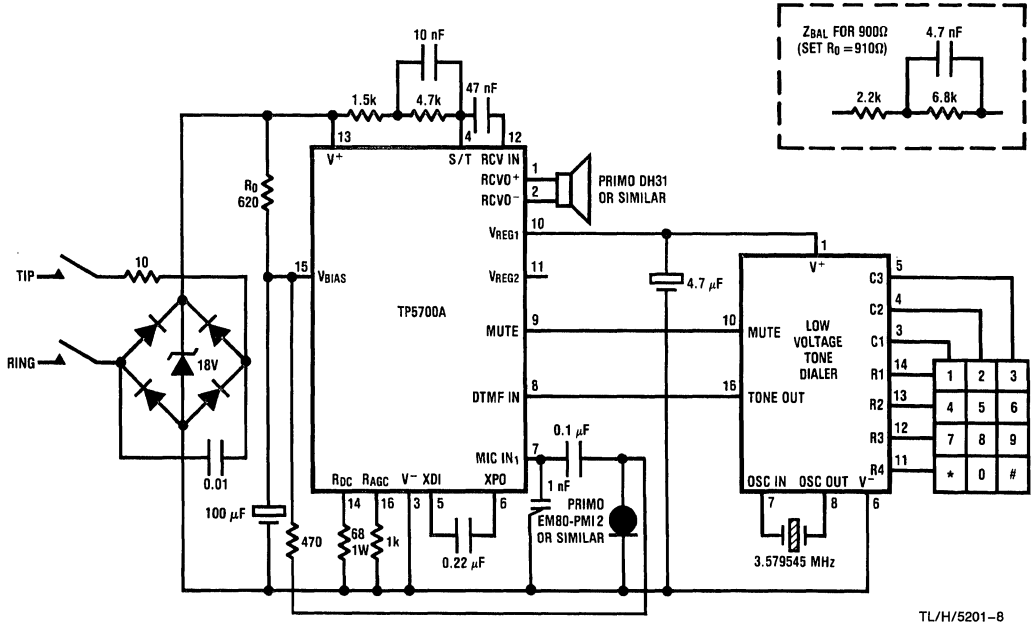
POWERING ELECTRET MICROPHONES

Electret microphones with integral FET buffers are available in both two-wire and three-wire versions and a range of operating voltage ranges. There are four methods of powering the microphone.

1. The 1.2V V_{REG2} output provides the lowest voltage method for microphones rated down to 1V. V_{REG2} must be decoupled with a 1 μF capacitor to ground. (See *Figure 5.*)
2. If V_{REG1} is not required for DTMF generator operation, it may be used to provide up to 200 μA for microphone power.
3. V_{BIAS} (pin 15) may be used as a decoupled, but unregulated, supply for electrets requiring a higher operating voltage than V_{REG1} or V_{REG2}. The additional current drawn through R_0 will, however, raise the minimum operating voltage of the Speech Circuit. If this method is used the decoupling capacitor must be increased to at least 100 μF to maintain good low frequency return loss. (See *Figure 4.*)
4. An electret type with a good power supply rejection ratio can be powered from V+, or a regulated and decoupled supply dropped from V+.

TONE DIALING TELEPHONE

Figure 4 shows the TP5700 directly interfacing to a low voltage DTMF generator. V_{REG1} supplies the necessary 2V minimum bias to enable the low voltage tone dialer to sense key closures and pull its MUTE output high. V_{REG1} then switches to a 3V regulated output to sustain the Tone Dialer during tone generation. The TP5700A DTMF input incorporates the necessary load resistor to V− and provides gain plus AGC action to compensate for loop length. A muted tone level is heard in the receiver. For DTMF generators with a higher output level, a resistive potentiometer should



TL/H/5201–8

FIGURE 4. Typical Tone Dialing Telephone

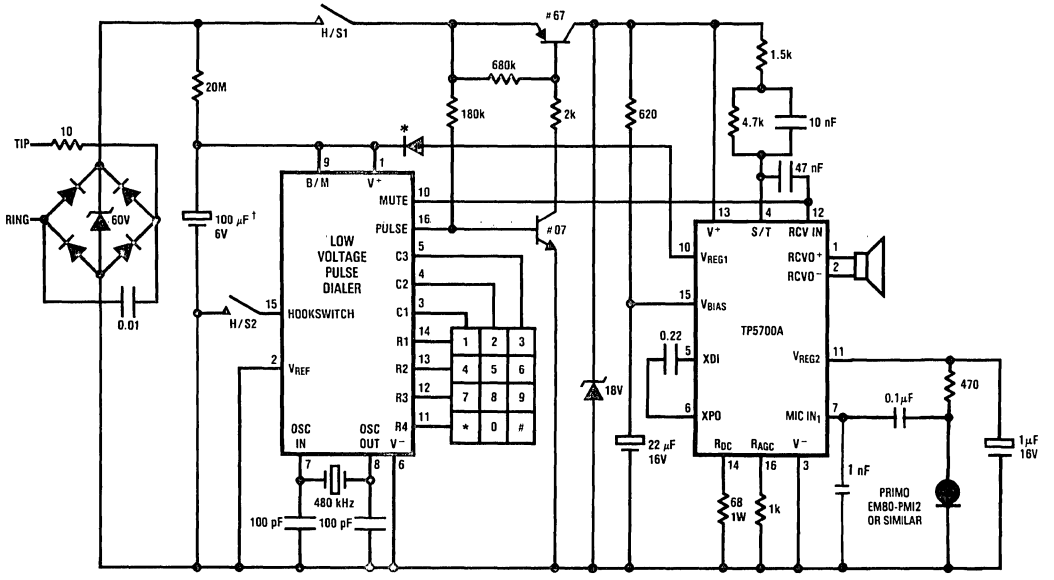
Applications Information (Continued)

be added to reduce the level at the speech circuit DTMF Input. For application requiring higher DTMF level, the signal swing across the device can be raised by using 620Ω in series with 270Ω for R_O. The 270Ω has to be bypassed by a 10 μf capacitor in order to maintain same AC off hook impedance.

PULSE DIALING TELEPHONE

The TP5700A can reduce the number of components required to build a pulse dialing telephone, as shown in *Figure 5*. The usual current source can be eliminated by using the V_{REG1} output to power a low-voltage (1.7V) series mode pulse dialer via a blocking diode. A low forward-voltage drop diode such as a Schottky type is necessary because V_{REG1} is used in its non-regulated mode and its output voltage may fall to 2V on a 20 mA loop. A 100 μF decoupling capacitor is required to hold up the pulse dialer supply voltage during dialing. This capacitor will take about one second to charge up when the telephone is first connected to the line, but thereafter the 20 MΩ resistor required to retain the last-number dialed memory will keep this capacitor charged. Partial muting is obtained by directly connecting the N-channel open-drain MUTE output of the pulse dialer to the RCV IN pin on the Speech Circuit.

A fully muted pulse dialer design requires the use of a shunt-mode dialer.



TL/H/5201–9

*Low voltage drop diode (e.g. Schottky)

† Low leakage type

# Indicates National Semiconductor discrete transistor process number

FIGURE 5. Typical Pulse Dialing Telephone

Section 4

Application Notes

Section 4 Contents

AN-336 Understanding Integrated Circuit Package Power Capabilities 4-3
AN-370 Techniques for Designing with CODEC/Filter COMBO Circuits 4-8
AN-439 TP3200 MC-SLIC Application Guide 4-11
AN-466 Improving the Performance of a High Speed PBX Backplane 4-21
AN-492 "Intuitive ISDN"—An ISDN Tutorial 4-26
AN-509 Using the TP3401, TP3402, TP3403 ISDN PBX Transceivers 4-31
AN-520 Building an ISDN Terminal/Terminal Adapter 4-44
AN-614 COMBO II Programmable PCM CODEC/Filter Family Application Guide 4-52
AN-639 High Voltage Protection Techniques with TP3210 Subscriber Line Interface Module.. 4-69
AN-664 ISDN Basic Rate Interface Terminal Equipment (TE) System Design Guide 4-78
AN-665 TP3420, TP3421 S Interface Device (SID) User's Guide 4-87
Definitions and Timing Conventions 4-129
ISDN Basic Rate Interface Software for the HPC16400 High Performance Data Communications Microcontroller 4-132
ISDN Glossary of Terms 4-143

Understanding Integrated Circuit Package Power Capabilities

National Semiconductor
Application Note 336
Charles Carinalli
Josip Huljev

INTRODUCTION

The short and long term reliability of National Semiconductor's interface circuits, like any integrated circuit, is very dependent on its environmental condition. Beyond the mechanical/environmental factors, nothing has a greater influence on this reliability than the electrical and thermal stress seen by the integrated circuit. Both of these stress issues are specifically addressed on every interface circuit data sheet, under the headings of Absolute Maximum Ratings and Recommended Operating Conditions.

However, through application calls, it has become clear that electrical stress conditions are generally more understood than the thermal stress conditions. Understanding the importance of electrical stress should never be reduced, but clearly, a higher focus and understanding must be placed on thermal stress. Thermal stress and its application to interface circuits from National Semiconductor is the subject of this application note.

FACTORS AFFECTING DEVICE RELIABILITY

Figure 1 shows the well known "bathtub" curve plotting failure rate versus time. Similar to all system hardware (mechanical or electrical) the reliability of interface integrated circuits conform to this curve. The key issues associated with this curve are infant mortality, failure rate, and useful life.

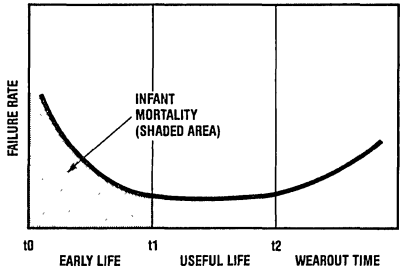


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FIGURE 1. Failure Rate vs Time

Infant mortality, the high failure rate from time t0 to t1 (early life), is greatly influenced by system stress conditions other than temperature, and can vary widely from one application to another. The main stress factors that contribute to infant mortality are electrical transients and noise, mechanical maltreatment and excessive temperatures. Most of these failures are discovered in device test, burn-in, card assembly and handling, and initial system test and operation. Although important, much literature is available on the subject of infant mortality in integrated circuits and is beyond the scope of this application note.

Failure rate is the number of devices that will be expected to fail in a given period of time (such as, per million hours). The mean time between failure (MTBF) is the average time (in hours) that will be expected to elapse after a unit has failed before the next unit failure will occur. These two primary "units of measure" for device reliability are inversely related:

$$\text{MTBF} = \frac{1}{\text{Failure Rate}}$$

Although the "bathtub" curve plots the overall failure rate versus time, the useful failure rate can be defined as the percentage of devices that fail per-unit-time during the flat portion of the curve. This area, called the useful life, extends between t1 and t2 or from the end of infant mortality to the onset of wearout. The useful life may be as short as several years but usually extends for decades if adequate design margins are used in the development of a system.

Many factors influence useful life including: pressure, mechanical stress, thermal cycling, and electrical stress. However, die temperature during the device's useful life plays an equally important role in triggering the onset of wearout.

FAILURE RATES vs TIME AND TEMPERATURE

The relationship between integrated circuit failure rates and time and temperature is a well established fact. The occurrence of these failures is a function which can be represented by the Arrhenius Model. Well validated and predominantly used for accelerated life testing of integrated circuits, the Arrhenius Model assumes the degradation of a performance parameter is linear with time and that MTBF is a function of temperature stress. The temperature dependence is an exponential function that defines the probability of occurrence. This results in a formula for expressing the lifetime or MTBF at a given temperature stress in relation to another MTBF at a different temperature. The ratio of these two MTBFs is called the acceleration factor F and is defined by the following equation:

$$F = \frac{X1}{X2} = \exp\left[\frac{E}{K}\left(\frac{1}{T2} - \frac{1}{T1}\right)\right]$$

Where: X1 = Failure rate at junction temperature T1
X2 = Failure rate at junction temperature T2
T = Junction temperature in degrees Kelvin
E = Thermal activation energy in electron volts (ev)
K = Boltzman's constant

However, the dramatic acceleration effect of junction temperature (chip temperature) on failure rate is illustrated in a plot of the above equation for three different activation energies in *Figure 2*. This graph clearly demonstrates the importance of the relationship of junction temperature to device failure rate. For example, using the 0.99 ev line, a 30° rise in junction temperature, say from 130°C to 160°C, results in a 10 to 1 increase in failure rate.

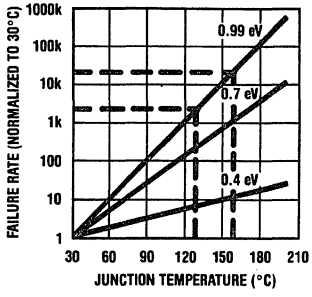

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FIGURE 2. Failure Rate as a Function of Junction Temperature

DEVICE THERMAL CAPABILITIES

There are many factors which affect the thermal capability of an integrated circuit. To understand these we need to understand the predominant paths for heat to transfer out of the integrated circuit package. This is illustrated by *Figures 3* and *4*.

Figure 3 shows a cross-sectional view of an assembled integrated circuit mounted into a printed circuit board.

Figure 4 is a flow chart showing how the heat generated at the power source, the junctions of the integrated circuit flows from the chip to the ultimate heat sink, the ambient environment. There are two predominant paths. The first is from the die to the die attach pad to the surrounding package material to the package lead frame to the printed circuit board and then to the ambient. The second path is from the package directly to the ambient air.

Improving the thermal characteristics of any stage in the flow chart of *Figure 4* will result in an improvement in device thermal characteristics. However, grouping all these characteristics into one equation determining the overall thermal capability of an integrated circuit/package/environmental condition is possible. The equation that expresses this relationship is:

$$T_J = T_A + P_D (\theta_{JA})$$

Where: T_J = Die junction temperature

T_A = Ambient temperature in the vicinity device

P_D = Total power dissipation (in watts)

θ_{JA} = Thermal resistance junction-to-ambient

θ_{JA}, the thermal resistance from device junction-to-ambient temperature, is measured and specified by the manufacturers of integrated circuits. National Semiconductor utilizes special vehicles and methods to measure and monitor this parameter. All interface circuit data sheets specify the thermal characteristics and capabilities of the packages available for a given device under specific conditions—these package power ratings directly relate to thermal resistance junction-to-ambient or θ_{JA}.

Although National provides these thermal ratings, it is critical that the end user understand how to use these numbers to improve thermal characteristics in the development of his system using interface components.

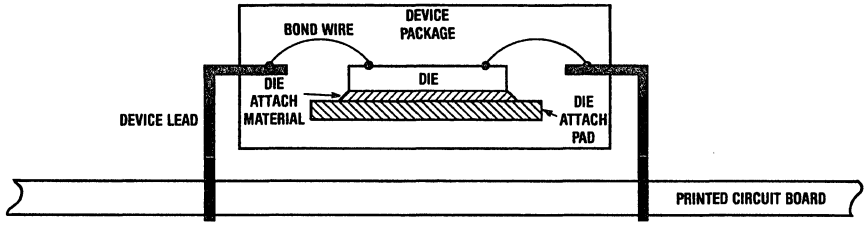

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FIGURE 3. Integrated Circuit Soldered into a Printed Circuit Board (Cross-Sectional View)

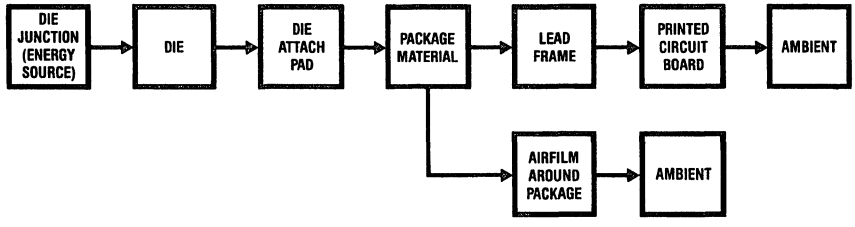

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FIGURE 4. Thermal Flow (Predominant Paths)

DETERMINING DEVICE OPERATING JUNCTION TEMPERATURE

From the above equation the method of determining actual worst-case device operating junction temperature becomes straightforward. Given a package thermal characteristic, θ_{JA}, worst-case ambient operating temperature, T_A(max), the only unknown parameter is device power dissipation, P_D. In calculating this parameter, the dissipation of the integrated circuit due to its own supply has to be considered, the dissipation within the package due to the external load must also be added. The power associated with the load in a dynamic (switching) situation must also be considered. For example, the power associated with an inductor or a capacitor in a static versus dynamic (say, 1 MHz) condition is significantly different.

The junction temperature of a device with a total package power of 600 mW at 70°C in a package with a thermal resistance of 63°C/W is 108°C.

$$T_J = 70°C + (63°C/W) \times (0.6W) = 108°C$$

The next obvious question is, "how safe is 108°C?"

MAXIMUM ALLOWABLE JUNCTION TEMPERATURES

What is an acceptable maximum operating junction temperature is in itself somewhat of a difficult question to answer. Many companies have established their own standards based on corporate policy. However, the semiconductor industry has developed some defacto standards based on the device package type. These have been well accepted as numbers that relate to reasonable (acceptable) device lifetimes, thus failure rates.

National Semiconductor has adopted these industry-wide standards. For devices fabricated in a molded package, the maximum allowable junction temperature is 150°C. For these devices assembled in ceramic or cavity DIP packages, the maximum allowable junction temperature is 175°C. The numbers are different because of the differences in package types. The thermal strain associated with the die package interface in a cavity package is much less than that exhibited in a molded package where the integrated circuit chip is in direct contact with the package material.

Let us use this new information and our thermal equation to construct a graph which displays the safe thermal (power) operating area for a given package type. *Figure 5* is an example of such a graph. The end points of this graph are easily determined. For a 16-pin molded package, the maximum allowable temperature is 150°C; at this point no power dissipation is allowable. The power capability at 25°C is 1.98W as given by the following calculation:

$$P_D @ 25°C = \frac{T_J(max) - T_A}{\theta_{JA}} = \frac{150°C - 25°C}{63°C/W} = 1.98W$$

The slope of the straight line between these two points is minus the inversion of the thermal resistance. This is referred to as the derating factor.

$$\text{Derating Factor} = -\frac{1}{\theta_{JA}}$$

As mentioned, *Figure 5* is a plot of the safe thermal operating area for a device in a 16-pin molded DIP. As long as the intersection of a vertical line defining the maximum ambient temperature (70°C in our previous example) and maximum device package power (600 mW) remains below the maximum package thermal capability line the junction temperature will remain below 150°C—the limit for a molded package. If the intersection of ambient temperature and package power fails on this line, the maximum junction temperature will be 150°C. Any intersection that occurs above this line will result in a junction temperature in excess of 150°C and is not an appropriate operating condition.

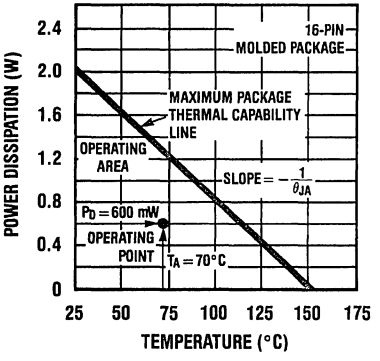

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FIGURE 5. Package Power Capability vs Temperature

The thermal capabilities of all interface circuits are expressed as a power capability at 25°C still air environment with a given derating factor. This simply states, for every degree of ambient temperature rise above 25°C, reduce the package power capability stated by the derating factor which is expressed in mW/°C. For our example—a θ_{JA} of 63°C/W relates to a derating factor of 15.9 mW/°C.

FACTORS INFLUENCING PACKAGE THERMAL RESISTANCE

As discussed earlier, improving any portion of the two primary thermal flow paths will result in an improvement in overall thermal resistance junction-to-ambient. This section discusses those components of thermal resistance that can be influenced by the manufacturer of the integrated circuit. It also discusses those factors in the overall thermal resistance that can be impacted by the end user of the integrated circuit. Understanding these issues will go a long way in understanding chip power capabilities and what can be done to insure the best possible operating conditions and, thus, best overall reliability.

Die Size

Figure 6 shows a graph of our 16-pin DIP thermal resistance as a function of integrated circuit die size. Clearly, as the chip size increases the thermal resistance decreases—this relates directly to having a larger area with which to dissipate a given power.

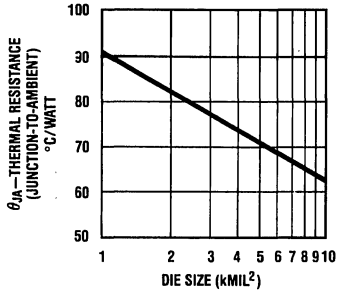

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FIGURE 6. Thermal Resistance vs Die Size

Lead Frame Material

Figure 7 shows the influence of lead frame material (both die attach and device pins) on thermal resistance. This graph compares our same 16-pin DIP with a copper lead frame, a Kovar lead frame, and finally an Alloy 43 type lead frame—these are lead frame materials commonly used in the industry. Obviously the thermal conductivity of the lead frame material has a significant impact in package power capability. Molded interface circuits from National Semiconductor use the copper lead frame exclusively.

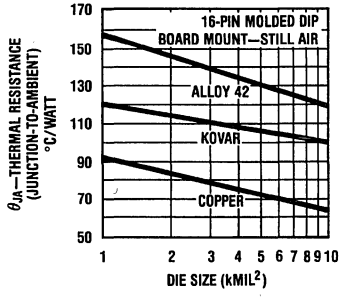

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FIGURE 7. Thermal Resistance vs Lead Frame Material

Board vs Socket Mount

One of the major paths of dissipating energy generated by the integrated circuit is through the device leads. As a result of this, the graph of *Figure 8* comes as no surprise. This compares the thermal resistance of our 16-pin package soldered into a printed circuit board (board mount) compared to the same package placed in a socket (socket mount). Adding a socket in the path between the PC board and the device adds another stage in the thermal flow path, thus increasing the overall thermal resistance. The thermal capabilities of National Semiconductor's interface circuits are specified assuming board mount conditions. If the devices are placed in a socket the thermal capabilities should be reduced by approximately 5% to 10%.

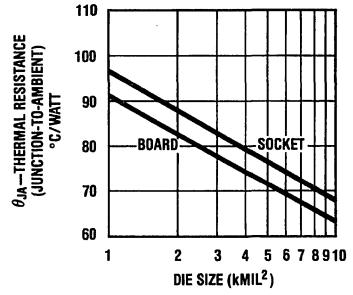

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FIGURE 8. Thermal Resistance vs Board or Socket Mount

Air Flow

When a high power situation exists and the ambient temperature cannot be reduced, the next best thing is to provide air flow in the vicinity of the package. The graph of *Figure 9* illustrates the impact this has on thermal resistance. This graph plots the relative reduction in thermal resistance normalized to the still air condition for our 16-pin molded DIP. The thermal ratings on National Semiconductor's interface circuits data sheets relate to the still air environment.

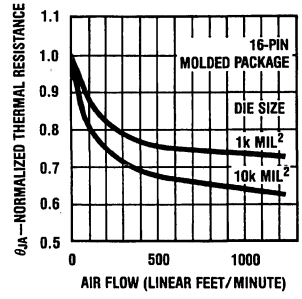

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FIGURE 9. Thermal Resistance vs Air Flow

Other Factors

A number of other factors influence thermal resistance. The most important of these is using thermal epoxy in mounting ICs to the PC board and heat sinks. Generally these techniques are required only in the very highest of power applications.

Some confusion exists between the difference in thermal resistance junction-to-ambient (θ_{JA}) and thermal resistance junction-to-case (θ_{JC}). The best measure of actual junction temperature is the junction-to-ambient number since nearly all systems operate in an open air environment. The only situation where thermal resistance junction-to-case is important is when the entire system is immersed in a thermal bath and the environmental temperature is indeed the case temperature. This is only used in extreme cases and is the exception to the rule and, for this reason, is not addressed in this application note.

NATIONAL SEMICONDUCTOR PACKAGE CAPABILITIES

Figures 10 and *11* show composite plots of the thermal characteristics of the most common package types in the National Semiconductor Interface Circuits product family. *Figure 10* is a composite of the copper lead frame molded package. *Figure 11* is a composite of the ceramic (cavity) DIP using poly die attach. These graphs represent board mount still air thermal capabilities. Another, and final, thermal resistance trend will be noticed in these graphs. As the number of device pins increase in a DIP the thermal resistance decreases. Referring back to the thermal flow chart, this trend should, by now, be obvious.

RATINGS ON INTERFACE CIRCUITS DATA SHEETS

In conclusion, all National Semiconductor Interface Products define power dissipation (thermal) capability. This information can be found in the Absolute Maximum Ratings section of the data sheet. The thermal information shown in this application note represents average data for characterization of the indicated package. Actual thermal resistance can vary from ±10% to ±15% due to fluctuations in assembly quality, die shape, die thickness, distribution of heat sources on the die, etc. The numbers quoted in the interface data sheets reflect a 15% safety margin from the average numbers found in this application note. Insuring that total package power remains under a specified level will guarantee that the maximum junction temperature will not exceed the package maximum.

The package power ratings are specified as a maximum power at 25°C ambient with an associated derating factor for ambient temperatures above 25°C. It is easy to determine the power capability at an elevated temperature. The power specified at 25°C should be reduced by the derating factor for every degree of ambient temperature above 25°C. For example, in a given product data sheet the following will be found:

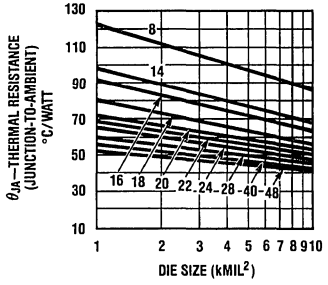
Maximum Power Dissipation* at 25°C
Cavity Package 1509 mW
Molded Package 1476 mW

* Derate cavity package at 10 mW/°C above 25°C; derate molded package at 11.8 mW/°C above 25°C.

If the molded package is used at a maximum ambient temperature of 70°C, the package power capability is 945 mW.

$$P_D \text{ @ } 70°C = 1476 \text{ mW} - (11.8 \text{ mW/°C}) \times (70°C - 25°C)$$
$$= 945 \text{ mW}$$

Molded (N Package) DIP* Copper Leadframe—HTP Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 40-pin 0.6 mil width

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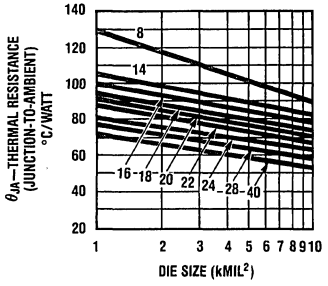
FIGURE 10. Thermal Resistance vs Die Size vs Package Type (Molded Package)

Cavity (J Package) DIP* Poly Die Attach Board Mount—Still Air



*Packages from 8- to 20-pin 0.3 mil width
22-pin 0.4 mil width
24- to 48-pin 0.6 mil width

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FIGURE 11. Thermal Resistance vs Die Size vs Package Type (Cavity Package)

Techniques for Designing with CODEC/Filter COMBO™ Circuits

National Semiconductor
Application Brief
Chris Stacey

PCM CODEC/Filter COMBO devices are complex analog and digital sub-systems on a single chip. They contain, for example, an A/D and a D/A converter, each with 13 bit (for u-law) resolution at low signal levels on the bottom chord of the companding characteristic. The TP3050/60 family of microCmos COMBOs are, however, capable of providing extremely high performance even in the unfriendly electrical environment of a multi-channel subscriber line card so long as the printed circuit board is carefully designed as an integral part of the system. Indeed, this family can achieve performance superior to that of other 1 or 2 chip CODEC/Filter circuits due to two key factors; superior Power Supply Rejection Ratio, particularly at high frequencies, and the fact that the critical connection between the transmit filter and the encoder is carefully shielded inside the device. Nevertheless, the following guidelines should be adhered to in order to maintain this high performance in any switching or transmission system.

GROUND AND POWER SUPPLY LAYOUT

1. Different techniques are necessary for the layout of analog circuits on the card (COMBO, SLIC and any external gain sections) and the digital control and switching circuits. Use the GNDA pin of each COMBO device as the Ground Reference Point (GRP) for each channel. All ANALOG ground connections for each channel should connect as close as possible to the reference point. This includes:
   a. The analog ground from the 4-wire side of the SLIC circuit.
   b. The ground for the transmit op amp connection.
   c. The ground side of the 0.1 μF decoupling capacitors for the +5V and −5V COMBO power supplies.
   d. The analog ground for any external gain or loss adjustment stage.
2. Ground return currents from logic circuits, relays and other audio channels must not flow into or out from the channel GRPs to avoid generating noise voltages. Therefore a separate ground return should be run from each channel GRP to a common point close to the ground pin on the card connector, commonly called the MECCA. Thus there is a STAR formation from the MECCA to each channel GRP. It is NOT recommended to run separate analog and digital ground returns to the shelf power supply. Relays and other circuits operating from the station battery should, however, have a separate return bus to the battery ground.
3. Decouple the +5V and −5V power supplies to the MECCA close to the card connector. A minimum of 10 μF should be used for each supply, and a capacitor type with a low Effective Series Resistance should be selected. Beware of the effects of the inrush current charging these capacitors as the card is plugged into a "hot" socket. This current flowing through the wire and trace inductance can cause voltage spikes which easily exceed the absolute maximum ratings of various devices on the card and may even damage the connector contacts. The trace length from the connector to the capacitors should be kept short, and excessive values of decoupling capacitor avoided.
4. The +5V and −5V supply busses to the COMBO circuits should be routed adjacent to a ground bus to help ensure that any r.f. noise pick-up is common mode. Each supply must be decoupled by 0.1μF capacitors with short traces to the GRP of each COMBO. Ceramic capacitors are best for good high frequency decoupling.
5. The +5V bus for the switching and control logic circuits should be a separate connection from the decoupled point close to the card connector. It should not share any common path with the +5V connection to the COMBO circuits. Each logic circuit should be decoupled with a 0.01 μF ceramic capacitor from +5V to ground close to the device.
6. The ground connections for the logic circuits and low voltage relays may use a ground bus or, better still, a ground grid system to maintain good noise margins on digital signals. This logic ground should connect directly to the card MECCA such that logic ground currents do not share common paths with any channel GRP returns.
7. TTL and LSTTL logic families draw considerably different supply currents when their outputs are in the high and low logic states, causing large switching currents to flow through the busses and decoupling capacitors. In contrast, CMOS logic circuits only draw significant currents during state transitions, and these currents are substantially balanced. A CMOS logic system therefore generates far less electrical noise than a similar TTL System.

   The use of the 74HC CMOS logic family is highly recommended for line card design. It helps to preserve high transmission performance in the analog circuits and offers better noise margins than TTL in the presence of transient voltages induced by relays and ringing signals.

NOISE CONSIDERATIONS

1. Logic signals should be routed well away from the analog circuits and their power supply connections wherever possible to minimize high frequency noise being capacitively coupled into the channel and aliased down into the audio passband by the sampling action of the filters and encoder.
2. All signals and circuits capable of inducing large emf's into the audio signals should be located around the edge of the card wherever possible. This includes:
   a. Relay drive and output signals
   b. Ringing distribution
   c. The 2-wire side of the SLIC circuits.
   d. −48V battery
   e. d.c. to d.c. converters
3. Ground planes may be used to shield audio signals from noise sources such as clock and data signals and the high voltages listed above. A ground plane is only effective, however, if it carries NO NOISE-INDUCING CURRENTS itself. A single point connection from the ground plane to a quiet return is the best way to assure this.
4. The transmit op amp connections become a potential noise source particularly if a high gain is required. The feedback resistor value should not exceed 50K ohms, and the bodies of the feedback and input resistors should be close to the op amp input to minimize capacitive noise pick-up.
5. In asynchronous applications (typically transmission systems) the best idle channel noise and signal/distortion performance will be achieved if the transmit and receive filters are clocked synchronously. Thus the $MCLK_R$/PDN input on the TP3050/60 COMBO devices should either be connected to $MCLK_X$ or controlled solely by logic signals as a PDN input only (the COMBO will automatically use $MCLK_X$ internally). Note that $MCLK_R$ does not need to be synchronized to $BCLK_R$ and FS_R.

CIRCUIT PROTECTION

CMOS CODEC/Filter COMBOs are capable of providing extremely reliable and stable long-term performance provided a few simple precautions are followed:

1. Normal CMOS handling techniques should be used to prevent build-up of static charge on the device. These include the use of conductive carriers, and grounding personnel while handling devices.
2. Ensure that ground is always connected to each device before any other supplies or signals. An extended ground pin should be used on line card connectors.
3. Buffer all digital input and output signals between COMBO circuits and the line card backplane. This both protects the COMBO circuits from backplane transients and preserves good logic signal transition times and noise margins.
4. CMOS inputs, outputs and supply connections must be protected against even momentary transitions outside the supply voltages. Schottky diodes should be fitted on each card between +5V and GND, and between GND and −5V to clamp transient power supply reversals during power-up. Type 1N5820 is a good choice.
5. If the COMBO circuit is connected to a transformer-type of SLIC circuit additional protection is required against line transients. An input resistor of 5K ohms or more is adequate to protect the transmit op amp inputs, VF_XI+ and VF_XI-. If this is not possible, silicon diodes or a pair of back-to-back 3.9V zener diodes (depending on the required dynamic range) should be connected between the vulnerable input and GND.
6. A pair of back-to-back 3.9V zener diodes may also be necessary to protect the receive power amplifier output(s). Select a zener type with a sharp "knee" on the V-I characteristic, and low leakage current at voltages below the knee to avoid impairing the gain-tracking of the receive channel at high signal levels.

Figure 1 illustrates an idealized circuit card layout embodying many of the above techniques. While space constraints may limit the application of some of these techniques, the closer they can be followed, the better the system performance will be.

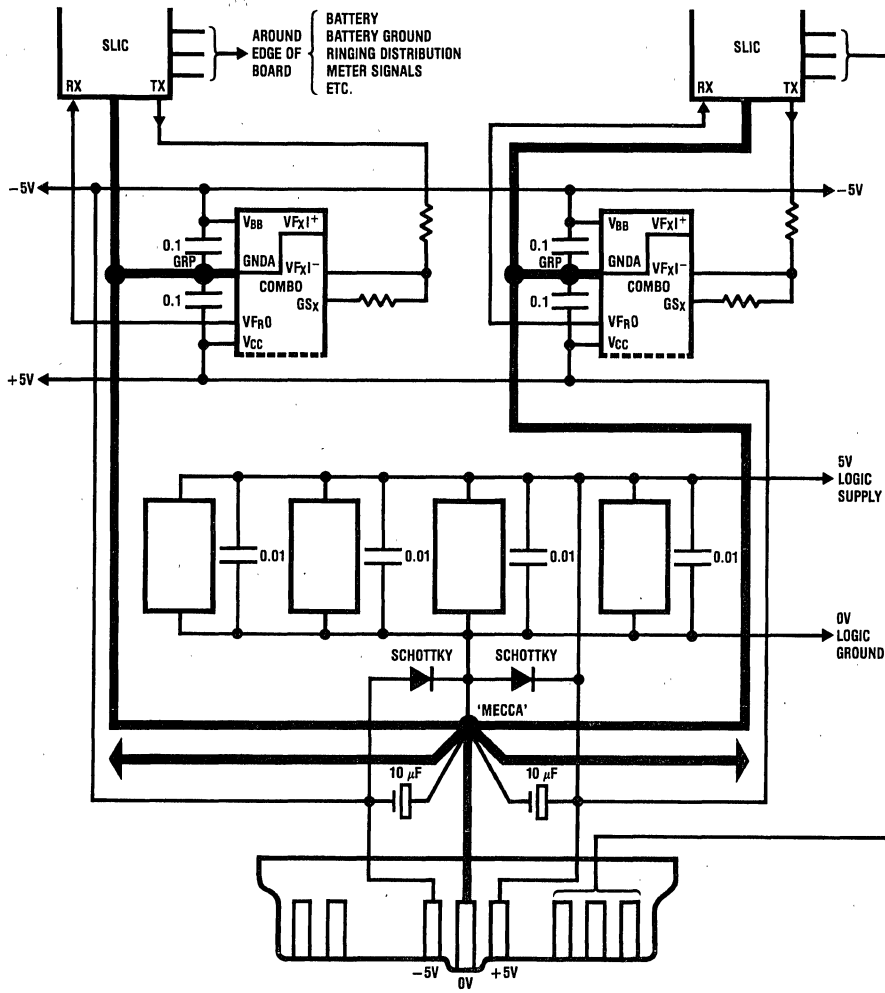

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FIGURE 1. Suggested COMBO PCB Layout

1. Use **'STAR'** Connection For Each Channel To The **'CHANNEL GRP'** At GNDA (Pin 2)
2. Use **'STAR'** Connections From Each **'CHANNEL GRP'** To The PCB **'MECCA'**

TP3200 MC-SLIC Application Guide

National Semiconductor
Application Note 439
T. K. Chin
John Shaw

INTRODUCTION

In a Central Office or Private Branch Exchange, each subscriber's telephone line is interfaced to the switching equipment through a Subscriber Line Interface Circuit (SLIC) on the line card. To integrate the SLIC function has been a challenge for IC designers. The requirements for the SLIC function are very stringent in that they involve an environment of 48V battery feed and up to 150 Vrms of ringing voltage on the line, not to mention the ability to withstand 1500V lightning surges. Another particularly difficult problem to solve is the maintenance of a good longitudinal balance against common mode current induced by adjacent power cables.

Several implementations of an all-monolithic SLIC have been demonstrated, although they require a somewhat expensive high voltage process and involve tradeoffs in performance. A transformer-based SLIC, on the other hand, offers the most cost-effective and reliable solution for many applications.

The TP3200 and TP3204 Magnetic Compensation SLIC are intended to reduce both the size and cost of implementing the SLIC while retaining all the advantages of a transformer-based design. The MC-SLIC also provides on-chip supervision and ring trip functions together with three relay drivers with latched inputs.

This applications note provides line card designers with a thorough understanding of the device's operation as well as some application hints that are useful to the circuit designer.

Block diagrams illustrating the device architecture are shown in *Figure 1*. The TP3200 is designed with PNP relay drivers, while the TP3204 is designed with NPN relay drivers.

MAGNETIC COMPENSATION

The TP3200 family of MC-SLICs reduces the size of the line interface transformer by using a flux cancellation technique. The device senses the loop current magnitude by means of a differential amplifier A1 (see *Figure 2*) and an on-chip high precision sensing resistor bridge across the external feeding resistor pair Rs.

The output of the amplifier A1 produces a voltage proportional to the instantaneous loop current. And the low pass filter formed by R1 and external capacitor CAP1 prevents the AC component of the loop current from disturbing the

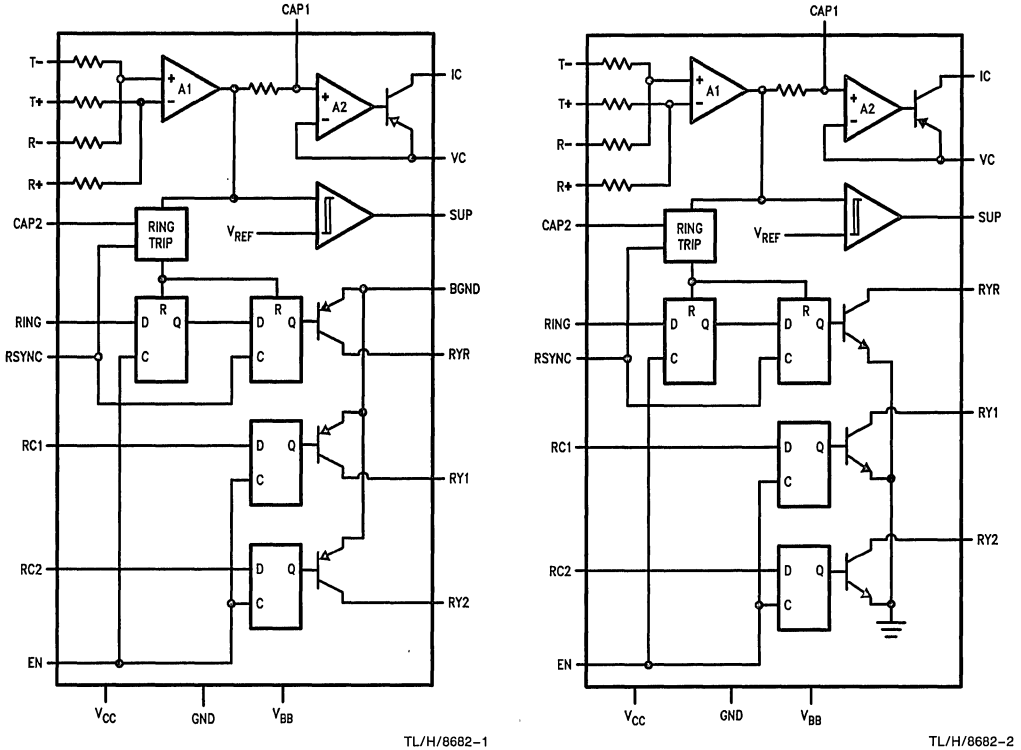

FIGURE 1. Simplified Block Diagram

flux cancellation. For a typical CAP1 of 1 μF, the cutoff frequency is approximately 2 Hz.

The voltage follower A2 and output transistor Q1 reproduce a voltage at VC output, proportional to the average DC loop current. A resistor R_L connected from VC to GND creates a current flow from the IC pin into the compensation winding of the transformer. By proper selection of R_L and the transformer winding ratio, the flux created by the compensation current can exactly cancel the flux produced by the DC loop current. The output current source requires a high output impedance at IC (typically 5 MΩ) in order to ensure that the reflected impedance from the compensation winding to the line will not create a loading effect on the line impedance. The IC pin should be connected to the finish of the compensation winding in order to reduce the capacitive loading of the transformer, thereby, increasing the effective reflected impedance from the compensation winding. It is recommended to connect R_L and CAP1 to the same ground point in order to prevent ground noise from being injected into the subscriber loop via the compensation winding.

With the DC flux removed, the hybrid transformer can be wound on a small ferrite core without an air gap, yet can maintain a large inductance without running into magnetic saturation.

Figure 2 shows a simplified schematic of the magnetic compensation circuit and *Figure 3* is a plot of V_C versus the loop current.

Equations relating to the magnetic compensation circuit are:

$$V_C = A_V \times 2 \times R_S \times I_{LOOP} \quad (1)$$

$$I_C = V_C/R_L$$

$$= A_V \times 2 \times R_S \times I_{LOOP}/R_L \quad (2)$$

For perfect flux cancellation,

$$I_{LOOP} \times 2 \times N_P = I_C \times N_C$$

or,

$$R_L = A_V \times R_S \times N_C/N_P \quad (3)$$

The reflected impedance from the compensation winding is:

$$Z_C = R_{IC} \times (2N_P/N_C)^2$$

Where R_{IC} is the output impedance at IC.

The value of CAP1 is:

$$CAP1 = 1.6/f\ \mu F$$

Where f is the desired upper cutoff frequency.

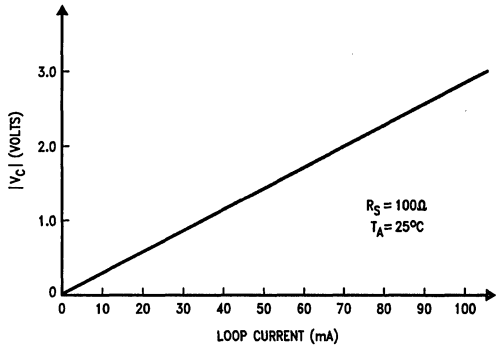

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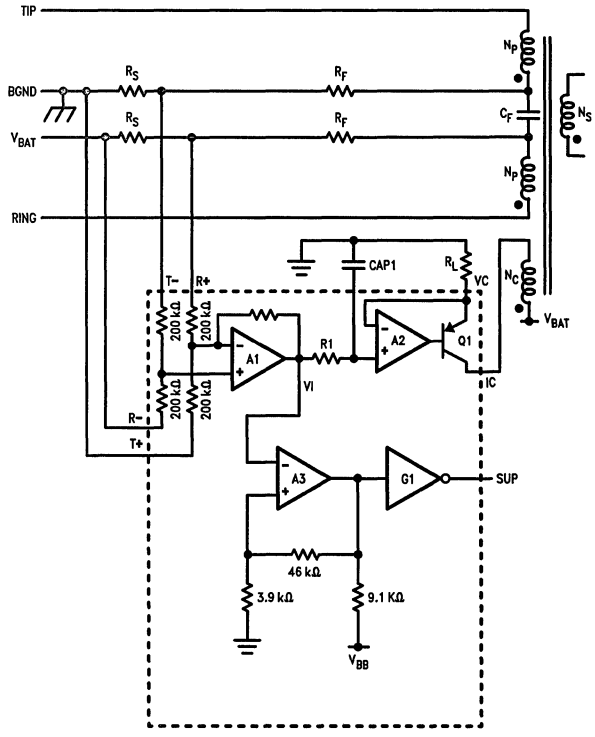
FIGURE 3. V_C Output vs Loop Current



TL/H/8682–3

FIGURE 2. Magnetic Compensation and Supervision Circuit

SUPERVISION

The supervision circuit of the TP3200 family consists of a loop current comparator with hysteresis. It provides status information on off-hook detection, dial pulse replication and ring-trip detection.

Referring back to *Figure 2*, the input to the comparator A3 is taken from the output of amplifier A1, which represents the instantaneous loop current. In the on-hook condition, the SUP output is at logic high. When the loop current rises above 13 mA, the SUP output switches low, indicating off-hook. When the loop current falls below approx. 11 mA, the SUP output will go high, indicating an on-hook condition. These comparator thresholds are selected so that in the extreme case of a very short loop, any possible cable leakage will not be misinterpreted as an off-hook. At the other extreme of a very long loop, there is enough safety margin for reliable detection of off-hook for very weak loop current of less than 15 mA.

During pulse dialing, the loop current changes from 0 mA during the break period and goes back to normal magnitude during the make period. The SUP output will produce a logic-replication of the dial pulses. However, under the worst case condition of a line loaded with 5 ringers, and with a cable leakage of 15 kΩ, the heavy capacitive loading of the ringers will cause excessive delay in loop current decay during break interval, creating dial pulse distortion. This results in shortening of the break period as reflected at the SUP output. *Figure 4* shows the relationship between SUP and the loop current under this condition.

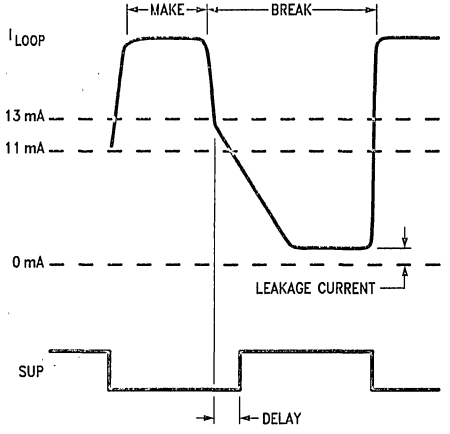


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FIGURE 4. SUP Output Under 5 Ringers and 15 kΩ Cable Leakage

To repeat these dial pulses through the switching system, a software routine is recommended to be included in the call-control processor, which monitors the SUP output and reconstructs the dial pulses in the appropriate break-make ratio.

During ringing, the comparator A3 will detect the instantaneous AC ringing current through the loop and create a waveform at SUP output. During on-hook, the waveform is a square wave with a mark-to-space ratio of larger than 50%. When the telephone goes off-hook, the DC loop current superimposed on the AC ringing current will cause the comparator to generate a waveform with less than 50% duty cycle. This change in duty cycle can be easily monitored by the call-control processor as a test for ring-trip.

This is the most flexible way to detect ring-trip as it is independent of the ringing frequency. However, the CPU must be fast enough to make the detection within 200 mS.

AUTOMATIC RING-TRIP

The automatic ring-trip circuit consists of a ring-trip detection circuit and a double-latched ring relay driver. *Figure 5* shows a simplified schematic diagram.

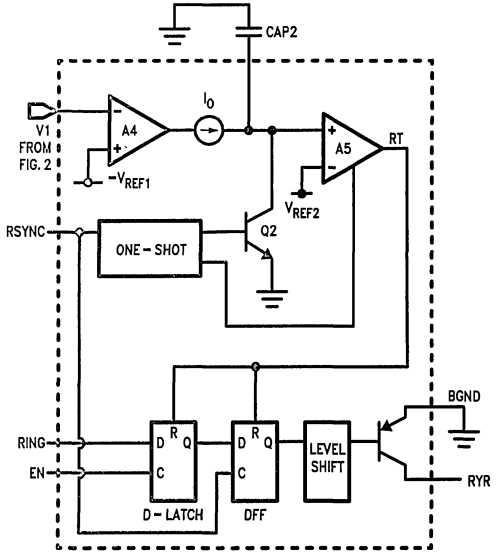

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FIGURE 5. Automatic Ring-Trip Circuit

Based on the state of the RING input, the D-latch is set or reset while the strobe EN is active high, and latched on the falling edge of EN. RSYNC is the clock input to the ring flip-flop. It is driven by the output of the external zero-crossing detector of the ringing voltage on the line. Based upon the state of the output of the D-latch, the ring flip-flop is set or reset at the rising edge of RSYNC. This scheme ensures that the ring relay is turned on or off near the zero crossing of the ringing current to prevent arcing and minimize relay contact wear.

The ring-trip circuit takes its input from the output of amplifier A1, which represents the instantaneous AC ringing current superimposed on the DC off-hook loop current. The comparator A4 compares this instantaneous loop current against a threshold equivalent to approximately 12 mA. Depending upon the polarity of the comparator's output, the constant current source I_O either sources or sinks 10 μA into CAP2. This results in charging and then discharging CAP2 in each ring cycle. Depending on the duty cycle of the output from A4, this charging and discharging process creates a resultant voltage on CAP2 after one ringing cycle, which is then compared against a threshold of about 50 mV at comparator A5. When the DC loop current increases to above 12 mA, the duty cycle of the output of amplifier A4 is less than 50%. The resultant voltage at CAP2 after a

complete ring cycle then exceeds the 50 mV threshold. As a result, the A5 amplifier generates an output at the next rising edge of RSYNC, which resets the ring latches.

Each positive transition of RSYNC enables the comparator A5 for 20 μS via the one-shot circuit, after which CAP2 is discharged to GND for 100 μS via Q2 to ensure that CAP2 always charges up from 0V. The reset pulse from A5 will always appear at the rising edge of RSYNC to ensure that the ring relay is reset at the zero-crossing of the ringing current. *Figure 6* shows the timing diagram for ring-trip.

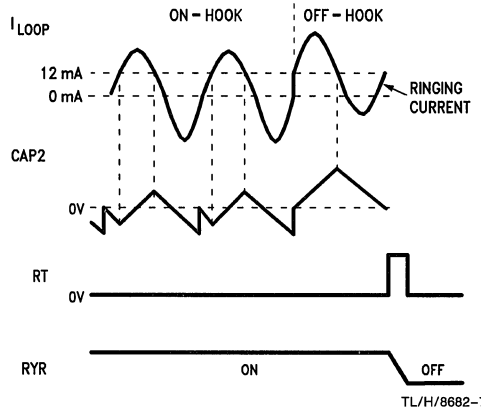

FIGURE 6. Timing Diagram for Ring-Trip

CAP2 is selected such that the constant current source I_O (approx. 10 μA) when integrated over half of one ringing cycle, will not create a charging voltage at CAP2 exceeding ±3V. A 0.1 μF is recommended for ringing frequency range of 16 Hz to 40 Hz, and 0.033 μF for 30 Hz to 70 Hz.

The automatic ring-trip circuit provides a reliable ring-trip detection. Normally, one ring cycle is needed for detection, and the second ring cycle to generate the reset pulse. The worst case ring-trip detection time will be within 3 ringing cycles. If the SUP output is used to detect ring-trip externally, the input at CAP2 should be grounded.

The RING or EN inputs should be kept at logic low after the ring relay is turned on in order to prevent relay chattering when the loop current is near to the 12 mA threshold. This is the condition where the automatic ring-trip tries to turn off the ring relay and the RING and EN inputs try to turn it on again. This results in relay chattering which may cause damage to the relay.

COMPENSATION ACCURACY

The accuracy of flux cancellation is one of the critical factors determining the size of the hybrid transformer. On chip Si-chrome resistors are used for the sensing resistor bridge to ensure high accuracy in loop current tracking. The offset voltage at V_C is zener trimmed to within 30 mV to further minimize the compensation error.

The tolerances of resistors R_S and R_L also contribute to compensation error. The feeding resistors R_S, however, are normally matched to each other to within ±0.1%, as are feeding resistors R_F, to ensure 60 dB longitudinal balance.

The following table shows a list of parameters that contribute to compensation errors:

Parameter	Typical	Tolerance
A_V	0.15 V/V	2%
V_{OS}	0	30 mV
R_S	100Ω	0.1%
R_L	150Ω	0.5%
N_C/N_P	10	0.05%

From Equation 2 above, the compensation error can be derived as follows:

Compensation

$$\text{Error} = I_{LOOP} - I_C \times N_C/2N_P$$
$$= I_{LOOP} - (N_C/2N_P) \times (A_V \times 2R_S \times I_{LOOP} \pm V_{OS})/R_L$$
$$= (1 - N_C/N_P \times A_V \times R_S/R_L) \times I_{LOOP} \pm V_{OS}/R_L$$
$$= \pm(0.026 \times I_{LOOP} + 0.2)\ \text{mA} \quad (4)$$

For a maximum loop current of 100 mA for Central Office application, the worst case compensation error is ±2.8 mA. For a maximum loop current of 60 mA for PBX application, the worst case compensation error is ±1.8 mA. The ferrite material of the hybrid transformer must be able to handle this uncompensated DC current before magnetic saturation starts.

TRANSFORMER DESIGN

The size and design of the hybrid transformer is influenced by the following factors:

1. Low frequency Return Loss, which in turn determines the minimum inductance of the primary windings.
2. The worst case compensation error, which determines the ampere-turn before magnetic saturation occurs.
3. The permeability and magnetization characteristics of the ferrite material.
4. Insertion loss and frequency response.

Figure 7 shows a simplified equivalent circuit for a hybrid transformer. r_p and r_s are the coil resistance of the primary and secondary windings. R_T and C_T are the terminating impedances of the secondary winding, and L is the total primary inductance. As the compensation winding is driven by a high impedance current source, it can be ignored from the equivalent circuit.

The return loss against a reference impedance Z_O can be calculated from the equation:

$$\text{Return Loss} = 20 \log \left| \frac{Z_I + Z_O}{Z_I - Z_O} \right|$$

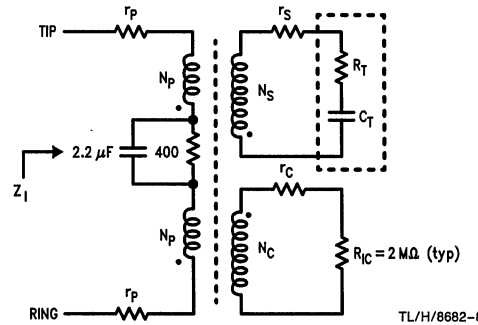

FIGURE 7. Simplified Equivalent Circuit of Hybrid Transformer

Figure 8 is a plot of return loss against a reference impedance of 600Ω + 2.16 μF. To achieve a 20 dB return loss, it can be seen from the plot that it requires a primary inductance of more than 0.8H even under the worst case compensation error of 2.8 mA. An acceptable ferrite is Siemens RM8-T35 ferrite core with a typical inductance factor of 8400 nH/T^2. Following a similar calculation, it can be found that it requires a minimum primary inductance of 1.4H in order to achieve a 20 dB return loss against a reference impedance of 900Ω + 2.16 μF. A suitable ferrite is Siemens RM10-T35 ferrite core with a typical inductance factor of 11000 nH/T^2.

To ensure a 60 dB longitudinal balance, the two primary windings must be carefully wound for symmetry. Usually this is done by winding the two primary windings with bifilar wires of the same gauge. Furthermore, to prevent heating up the ferrite core on a short loop, the primary resistance has to be kept to a minimum and is recommended to be below 30Ω.

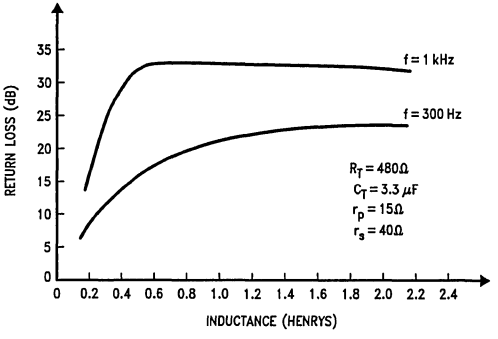

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FIGURE 8. Return Loss Against 600Ω + 2.16 μF

OUTPUT BIASING

The AC signal voltage across the subscriber loop will appear at the IC output and is amplified by the turns ratio $N_C/2N_P$. A suitable DC bias voltage must be provided for the compensation winding to ensure sufficient swing for the AC signals.

At minimum loop current (see *Figure 9a*), the DC bias at IC must be sufficiently positive with respect to the zener voltage to allow the peak negative swing without clipping. Thus:

$$I_{CMIN} \times (R_C + r_C) > N \times V_P - (V_{ZMIN} - |V_{BAT}|_{MAX})$$

or,

$$(R_C + r_C) \times I_{LOOPMIN}/N > N \times V_P - V_{ZMIN} + |V_{BAT}|_{MAX} \quad (5)$$

Where, V_{ZMIN} is the minimum zener voltage at IC

V_{BATMAX} is the maximum battery voltage

R_C is the filtering resistor for the compensation winding

r_C is the coil resistance of the compensation winding

N is the transformer turn ratio $N_C/2N_P$

V_P is the AC peak voltage swing across Tip and Ring

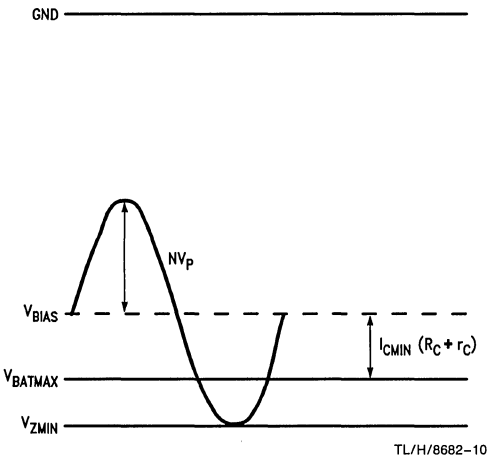

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FIGURE 9a. IC At Minimum Loop Current

At the other extreme with maximum loop current (see *Figure 9b*), the output transistor must not be saturated at the positive peak swing at IC. This requires:

$$|V_{BAT}|_{MIN} > I_{CMAX} \times (R_C + r_C) + V_{CMAX} + |V_{ICSAT}| + N \times V_P$$
$$> (R_C + r_C)\, I_{LOOPMAX}/N + I_{LOOPMAX} \times 2R_S \times A_V + |V_{ICSAT}| + N \times V_P \quad (6)$$

Substituting for $(R_C + r_C)$ from equation 5:

$$|V_{BAT}|_{MIN} > (N \times V_P - V_{ZMIN} + |V_{BAT}|_{MAX}) \times I_{LOOPMAX}/I_{LOOPMIN} + I_{LOOPMAX} \times 2R_S \times A_V + |V_{ICSAT}| + N \times V_P$$

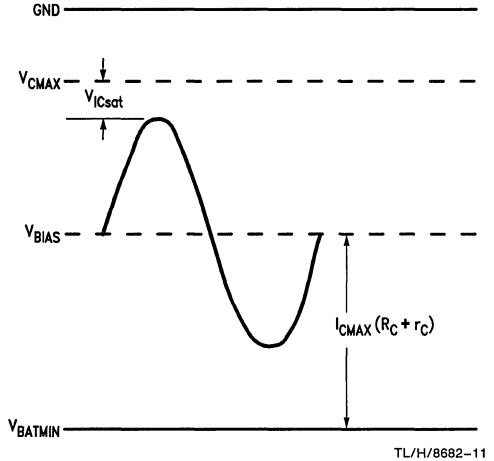

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FIGURE 9b. IC At Maximum Loop Current

The maximum current range of IC of 25 mA places a constraint on the minimum compensation to primary turn-ratio of the transformer.

$$N = N_C/2N_P$$
$$= I_{LOOP}/I_C$$

Thus,

$$N_{MIN} = I_{LOOPMAX}/25 \quad (7)$$

To allow for a +3 dBm line signal over loop current from 20 mA to 100 mA, with a zener voltage of 62V ±5%, and battery voltage of −42V to −54V, the compensation turns ratio and total resistance ($R_C + r_C$) can be calculated from the above equations and is shown in the following table:

	Line Impedance	
	600Ω	900Ω
Minimum N	4.0	4.0
Maximum N	6.67	5.45
Minimum ($R_C + r_C$) for N = 5	712.5Ω	1143.8Ω
Maximum ($R_C + r_C$) for N = 5	1487.5Ω	1401.3Ω

INPUT COMMON MODE RANGE

Consideration should be given to the various subscriber line voltages and currents, such that the magnetic compensation circuitry only operates within its dynamic range.

The A1 amplifier's differential input is biased using negative feedback so that it works within the range of V_{BB} + 0.5V to V_{CC} − 1V, where V_{CC} = +5V ±5%, and V_{BB} = −5V ±5%. The input common mode voltage V_{IN} is given by the following expression:

$$V_{IN} = 0.0155 \times (V_{BAT} + V_R \sin wt + 2R_S \times I_{CM}) - 0.05R_S \times (I_{LOOP} + I_R \sin (wt + A)) \quad (8)$$

where, V_{BAT} is the battery voltage

I_{LOOP} is the DC loop current

V_R is the peak ringing voltage

I_R is the peak ringing current

I_{CM} is the peak longitudinal current of arbitrary phase

It should be noted that for short subscriber loops, the component of voltage at V_{IN} due to the ringing current is in antiphase to the ringing voltage. For longer loops, the phase angle A between the ringing voltage and the ringing current increases. Thus the resulting voltage for V_{IN} will be a vector summation. Under the latter condition, however, the subscriber loop resistance is greater, which will reduce I_{LOOP} and I_R, and consequently reduce their influence on V_{IN}.

As an example, consider an application with V_{BAT} = −48V, V_R = 110V rms at 60 Hz, I_{LOOP} = 100 mA, I_{CM} = 30 mA peak, and a ringer impedance of 2 kΩ + 4.7 μF. During on-hook ringing, the voltage swing at V_{IN} can be derived from equation (8) as follows:

$$-2.93V < V_{IN} < 1.45V$$

When the telephone goes off-hook, and at the point before ring trip, the voltage swing at V_{IN} becomes :

$$-2.86V < V_{IN} < 0.38V$$

This reduction in voltage swing is due to the small phase angle A and the increase of AC ringing current.

OVER-VOLTAGE PROTECTION

The TP3200 family has been designed on a standard 70V bipolar process requiring no expensive dielectric isolation. In fact, any possible line transient voltage is scaled down through the feeding resistors R_S and R_F, insuring that the device will never see more than one half of the line transient. However, to prevent excessively high transient voltage induced by lightning or from nearby power cables, it is essential to provide some protective device across Tip and Ring. It is recommended to put a 10Ω current-limit resistor and a 300V peak transient suppressor from Tip to GND and from Ring to GND.

Moreover, any transient voltage on the line will also be reflected into the compensation winding as well as the secondary winding. Such a transient in the compensation winding is especially significant as it is boosted up by the turns ratio $N_C/2N_P$. A fast acting 62V zener diode is necessary to connect from IC output to GND for protection. On the secondary winding, two 3.9V zener diodes connected back-to-back will insure the COMBO will never see any transient voltage exceeding its supply voltages.

The on-chip relay driver has been designed to sink 30 mA for TP3200 and 80 mA for TP3204. When the relay is turned off, the back emf in the coil winding may possibly cause damage to the output driver. Each relay driver should be protected by a rectifier diode connected close to the relay coil in order to dissipate the stored energy in the coil.

A TYPICAL LINE CIRCUIT APPLICATION

Figure 10 shows a typical line circuit design using a TP3071 COMBO II™ device to perform the CODEC and filtering functions. To provide a +3.17 dBm overload level on the telephone line (0TLP) from the VF_RO receive output, a transformer with 600Ω secondary winding is used along with a series 600Ω terminating resistor. The COMBO II device has an internal programmable hybrid balance network for cancelling the echo. No external balance network components are needed. The SLIC control inputs (EN, RC2, RC1 and RING) are handled via the COMBO II Interface I/O latches, as is the line supervision output. These latches are individually programmable as inputs or outputs. Programming of the COMBO II I/O latches, hybrid balance network, transmit and receive gains, etc. is accomplished via a three pin serial microcomputer bus. The Control Clock (CCLK) and Control Input/Output (CI/O) pins are bussed to all COMBO II devices on the line card. A separate Chip Select ($\overline{CS}$) line is used for each COMBO II.

Ring voltage is applied to the line by breaking the battery feed path and superimposing the AC ring voltage via a 4-pole relay driven from the SLIC RYR output. Normally open contacts short the transformer primary windings when the ring voltage is applied to prevent attenuation and distortion of the ring signal and generation of large transients in the secondary and magnetic compensation windings due to core saturation by the 20 Hz ring current. Also a normally closed contact, in series with 2.2 μF capicator, opens when ringing is applied to prevent shunting the ring current. The two SLIC general purpose relay driver outputs, RY1 and RY2, are used to drive 2-pole battery reversal and test relays.

For additional information on design of a suitable zero crossing detector, see NATIONAL semiconductor Linear Application Note AN-74.

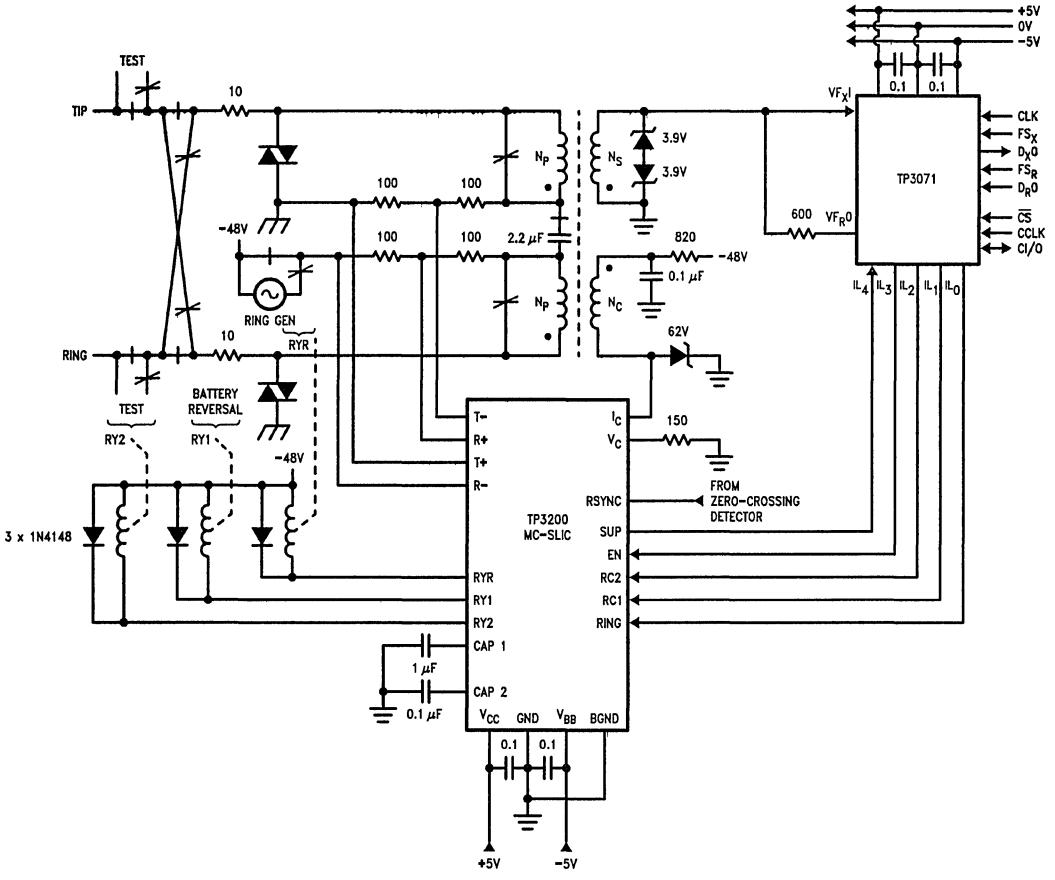

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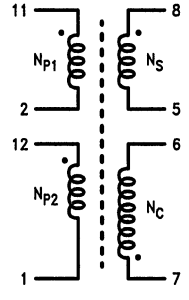
FIGURE 10. A Typical Line Circuit Application

APPENDIX A: Transformer Specification for 600Ω Line Impedance

1. Turn Ratio

Np1:	Start 11,	end 2,	210 T,	AWG #36
Np2:	Start 12,	end 1,	210 T,	AWG #36
Ns :	Start 8,	end 5,	440 T,	AWG #38
Nc :	Start 7,	end 6,	2100T,	AWG #42

2. Ferrite Core
   Siemens RM8-T35 or equivalent
   AL = 8400 nH/T^2 +30/−20%
3. DC Resistance
   Np1: 15Ω max
   Np2: 15Ω max
   Ns : 45Ω max
   Nc : 650Ω max
4. Inductance
   (total primary inductance with Np1 and Np2 in series aiding)
   1.5 H typical at 0 mA primary current
   0.7 H min at 3 mA DC primary current
5. Impedance: 600Ω to 600Ω
6. Frequency response
   ±0.5 dB reference to 1 kHz, 300–3500 Hz
7. Longitudinal Balance
   60 dB min with 2–12 grounded, 6–7 AC decoupled, 5 or 8 grounded
8. Dielectric
   1500 Vrms from primary to any other conductors



TL/H/8682–13

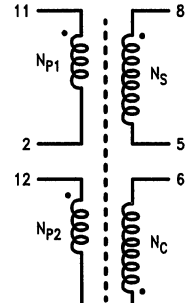
P/N 328-0036
AIE Magnetics
P.O. Box 44000
2801 72nd St. No.
St. Petersburg, FL 33743
(813) 347-2181

APPENDIX B: Transformer Specification for 900Ω Line Impedance

1. Turn Ratio

Np1:	Start 11,	end 2,	255 T,	AWG #36
Np2:	Start 12,	end 1,	255 T,	AWG #36
Ns :	Start 8,	end 5,	440 T,	AWG #38
Nc :	Start 7,	end 6,	2550T,	AWG #41

2. Ferrite Core
   Siemens RM10-T35 or equivalent
   AL = 11000 nH/T^2 +30/−20%
3. DC Resistance
   Np1 : 20Ω max
   Np2 : 20Ω max
   Ns : 55Ω max
   Nc : 800Ω max
4. Inductance
   (total primary inductance with Np1 and Np2 in series aiding)
   2.5 H typical at 0 mA DC primary current
   1.3 H min at 3 mA DC primary current
5. Impedance: 900Ω to 600Ω
6. Frequency response
   ±0.5 dB reference to 1 kHz, 300–3500 Hz
7. Longitudinal Balance
   60 dB min with 2–12 grounded, 6–7 AC decoupled, 5 or 8 grounded
8. Dielectric
   1500 Vrms from primary to any other conductors



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P/N 328-0035

APPENDIX C: Transformer Specification for a Center Tap Transformer

1. Turns Ratio

Np1:	Start 1,	End 4,	175 T
Np2:	Start 3,	End 6,	175 T
Ns1:	Start 12,	End 11,	175 T
Ns2:	Start 11,	End 9,	175 T
Nc :	Start 10,	End 7,	1750T

2. Wire Gauge

   Np1, Np2 wound by Bifilar wires, 0.125 mm
   Ns1, Ns2 wound by Bifilar wires, 0.125 mm
   Nc wound by 0.06 mm wires

3. Ferrite Core

   Siemens RM8-T38 or equivalent,
   $A_L = 12500\ nH/T^2 +30/-40\%$

4. Resistance matching of coils

   Np1 to Np2: 1% max
   Ns1 to Ns2: 1% max

5. Inductance

   (total primary inductance with Np1 and Np2 in series aiding)
   0.8H min at 3 mA DC primary current. f = 300 Hz.

6. High Voltage Isolation

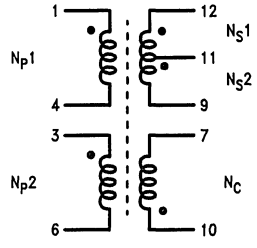
   1500V between all coils

7. Suggested Vendors

   Ferroglen Research Ltd.
   20 Tanfield Road
   Croyden Surrey
   CRO 1 AL

   or

   Gardners Transformers Ltd.
   Christchurch
   Dorset
   BH23 3PN



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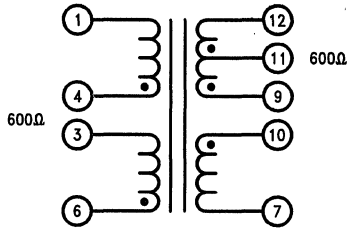
APPENDIX D: Other Transformers Available with Magnetic Compensation Winding



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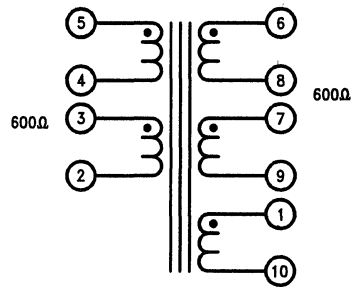
P/N 671-8500
Ferrite Core



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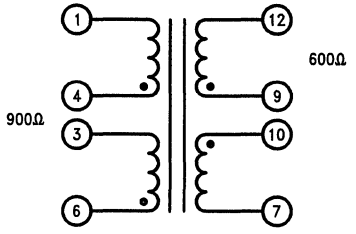
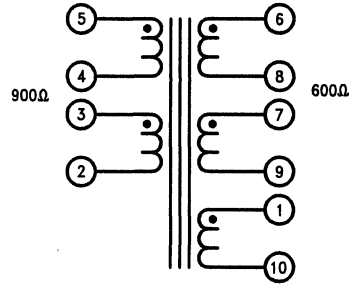
P/N 671-8501
Laminated Core



TL/H/8682–20

P/N 671-8503
Ferrite Core



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Improving The Performance Of A High Speed PBX Backplane

National Semiconductor
Application Note 466
Ramiro Calvo

ABSTRACT

This article will provide solutions to performance problems associated with PBX backplanes. Some of these problems are: long settling time, excessive propagation delay, low impedance bus lines, crosstalk, and electromagnetic radiation (EMR). These problems are caused by high output capacitance drivers that use TTL signal levels. National's solution to these problems is the Backplane Transceiver Logic (BTL) family of devices.

INTRODUCTION

To be able to meet the bandwidth and high system reliability requirements of the next generation PBXs, the industry must use parallel, high speed Pulse Code Modulation (PCM) highways. This article will deal with the following problems encountered by these high speed PCM highways.

- Crosstalk
- Power Consumption
- Noise Margin
- Bus Impedance
- Signal Settling Time
- Propagation Delays
- Propagation Delay Skew
- Live Insertion
- Extending A Bus Beyond The Rack
- Bus Termination
- Pin Layout

I. REDUCING CROSSTALK

Crosstalk can reduce the data integrity of the system or even cause a total shutdown. Crosstalk amplitude is proportional to the slew rate, signal swing, and physical layout of the board. To reduce crosstalk, the DS3890/92/98: shrink the standard TTL three volt swing to the Backplane Transceiver Logic (BTL) one volt swing; slow down the rise and fall time to 6 ns; use low pass filters and precision thresholds on the receivers.

II. REDUCING POWER CONSUMPTION

Because of excessive heat dissipation and a mandatory battery backup, power consumption must be kept to a minimum. Low impedance, open collector busses that use TTL signal levels need drivers capable of sinking approximately 300 mA. By using the BTL one volt signal swing, the drivers need only sink 50 mA. Refer to the section **Signal Settling Time** for more details. The reduction in power consumption will enable PBXs to coexist with other office equipment in "normal" office environments.

III. NOISE MARGIN

Noise margins protect the system from crosstalk, ground noise, and external EMR. The magnitude of the absolute noise margin is a good measure of how well protected the system is against external electro magnetic interference (EMI) and ground noise. The relative noise margin is a good measure as to how well protected the system is against crosstalk, assuming most signals within the system have the

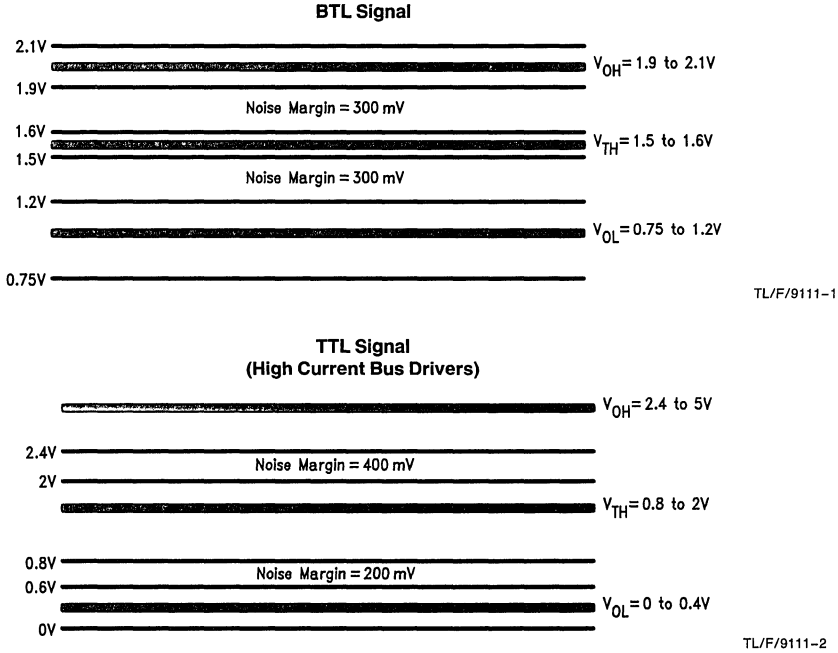

FIGURE 1

same voltage swing. As shown below, BTL signals improve both the absolute and relative noise margins

- Absolute Noise Margin

Despite the smaller signal swing, BTL signals have a 300 mV noise margin, as compared to the 200 or 400 mV guaranteed noise margin in TTL signals (see *Figure 1*). The absolute noise margin is usually not very critical since PBXs are usually well protected from external EMR by the metallic racks.

- Relative Noise Margin

Based on the data sheet guaranteed limits, BTL signals have a 30% [(300 mV absolute noise margin)/(1V signal swing)] relative noise margin, as compared to 7% [(200 mV absolute noise margin)/(3V swing)] in standard TTL signals.

IV. IMPROVING BUS IMPEDANCE

Standard TTL drivers do not have sufficient drive current to drive a heavily loaded backplane. A larger output transistor is needed to increase the drive current. The large TTL output transistor, however, increases the capacitance loading, which decreases the bus impedance, which in turn requires more drive current. The BTL drivers have a Schottky diode in series with the driver transistor's collector. When the driver transistor is off, the diode is reverse biased, which reduces the output capacitance to only 1–2 pF. As shown below, the reduced output capacitance greatly improves the overall bus impedance.

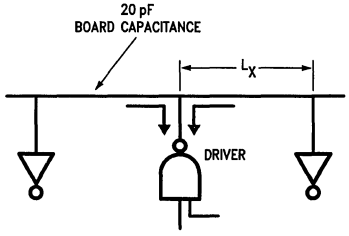

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FIGURE 2

L_X = Board Spacing = 0.6 in

L_{foot} = 20 loads per foot

$C_{X\text{-}TTL}$ = Capacitance per TTL Driver
= Transceiver Capacitance + PC Trace and Connector Capacitance
= 15 pF + 5 pF
= 20 pF per load

$C_{X\text{-}BTL}$ = Capacitance per BTL Driver
= Driver Capacitance + Receiver Capacitance + PC Trace and Connector Capacitance
= 2 pF + 2 pF + 1 pF + 5 pF
= 10 pF per load

$C_{L\text{-}TTL}$ = (20 load per foot) × (20 pF per load)
= 400 pF per Foot

$C_{L\text{-}BTL}$ = (20 load per foot) × (10 pF per load)
= 200 pF per Foot

- Unloaded Bus Impedance

L = Standard PC Board Inductance Per Foot
= 0.2 μH per foot

C = Standard PC Board Capacitance Per Foot
= 20 pF per foot

$Z_O = (L/C)^{1/2}$
$= (0.2\ \mu H/20\ pF)^{1/2} = 100\Omega$

- Loaded Bus Impedance (for a uniform capacitive loading C_X spaced at equal intervals)

$Z_L = Z_O/(1 + C_L/C)^{1/2}$

$Z_{L\text{-}TTL} = 100/(1 + 400/20)^{1/2} = 22\Omega$

$Z_{L\text{-}BTL} = 100/(1 + 200/20)^{1/2} = 30\Omega$

Note that each driver sees TWO loaded line impedances in parallel (see *Figure 2*). This reduces the bus impedance by half.

V. PROPAGATION DELAYS (related to excessive capacitance loading)

Since the DS3890 reduces the backplane capacitance loading, the propagation delay through the bus lines is improved by 28%, as shown below.

- Unloaded Bus Propagation Delay (data based on a single strip line PC board)

$T_P = (LC)^{1/2} = [(0.2\ \mu H/ft) \times (20\ pF/ft)]^{1/2}$
$= 2$ ns per foot

- Loaded Bus Propagation Delay (data based on a single strip line PC board)

$T_{PL} = (T_P) \times (1 + C_L/C)^{1/2}$

$T_{PL\text{-}TTL} = (2\ ns) \times [1 + (400\ pF\ per\ Foot)(20\ pF)]^{1/2}$
$= 9.2$ ns/ft

$T_{PL\text{-}BTL} = T_P \times (1 + C_L/C)^{1/2} = (2\ ns) \times [1 + (200\ pF\ per\ Foot)/(20\ pF)]^{1/2} = 6.6$ ns/ft

Improvement = (6.6 ns per foot)/(9.2 ns per foot) × (100)
= 28%

VI. SIGNAL SETTLING TIME

The signal settling time refers to the amount of time the signal takes to cross the threshold. In low impedance busses, the signaling settling time depends NOT ONLY on the slew rate, but more importantly, on the current driving capability of the driver, bus impedance, reflections, and bus length.

For example, in a fully loaded open collector TTL bus ($Z_{O\text{-}TTL} = 22\Omega$) with 50 mA drivers, the first output transition is [$V_1 = (I_L) \times (Z_O \| Z_O) = (50\ mA) \times (11\Omega)$] 0.55V. This means that the signal does NOT cross the threshold region (V_{TH} = 0.8 to 2V) on the first signal transition (see *Figure 3*). The second transition appears after a round trip prop delay [R.T.D. = (2) × ($T_{L\text{-}TTL}$)]. In a one foot fully loaded bus, the delay can be 18.4 ns [R.T.D. = (2) × (9.2 ns per foot)]. If it takes several signal transitions to cross the threshold, the ACTUAL signal settling time consists of several round trip prop delays. Also note that the signal crosses the threshold in a staircase fashion, which may cause false triggering.

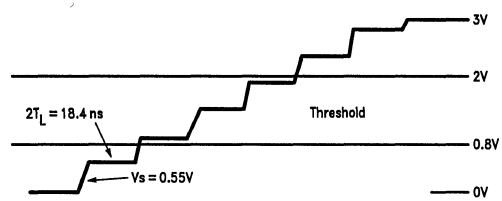

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FIGURE 3

$V_{I\text{-}TTL}$ = (50 mA) × (11Ω) = 0.55V

Round Trip Prop Delay of the Bus = (2) × ($T_{L\text{-}TTL}$)

= (2) × (2 ns per foot)

= 4 ns/ft (unloaded bus)

= (2) × (9.2 ns per foot)

= 18.4 ns/ft (loaded bus)

In a fully loaded BTL bus ($Z_{O\text{-}BTL}$ = 30Ω), the first output transition is 0.75V [V1 = (50 mA) × (15Ω)]. Since V_{TH} is between 1.5V and 1.6V, the FIRST output transition crosses the threshold (see *Figure 4*). The actual settling time consists of ONLY the slew rate. The danger of false triggering is eliminated because the reflections are not seen as the signal crosses the threshold.

$V_{I\text{-}BTL}$ = (50 mA)* (15Ω) = 0.75V

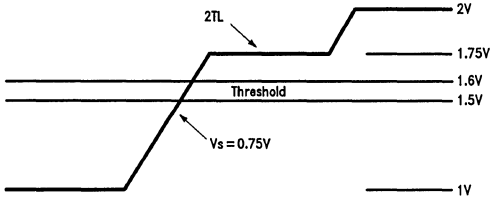

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FIGURE 4

Therefore, despite the slower slew rate, the BTL devices have a much shorter settling time due to the lower output capacitance, one volt signal swing, and precision threshold. This improves the data integrity and speed of the bus.

VII. PROPAGATION DELAY SKEW

The propagation delay consists of the delays through the driver, receiver, and transmission medium (PC strip). These delays can vary if the ICs have differences in their process, temperature, V_{CC}, or PC board layout. In parallel address/data lines, propagation delay skews are very critical. If the signals arrive at their destination at different times, the system must delay all signals to assume for a worst case delay. Therefore, if the propagation delay skew is small, the worst case delay is also small. It is safe to assume that ICs on a single board or system have the same temperature, same V_{CC}, and similar PC board layout configurations. This reduces the propagation delay skew to only the variations in the process.

VIII. LIVE INSERTION GUIDELINES

Live insertion of line cards is a must for PBX maintenance without interrupting customer service. The DS3890/92/98 support live insertion by guaranteeing glitch-free power up/down. However, uncharged by-pass capacitors and board static can bring the system down when plugging in a line card. One way of avoiding these problems is to use an umbilical cord (temporary power line) to discharge static and slowly charge by-pass capacitors. This method will set the line card V_{CC} and GND equal to the levels of the system before it is plugged in.

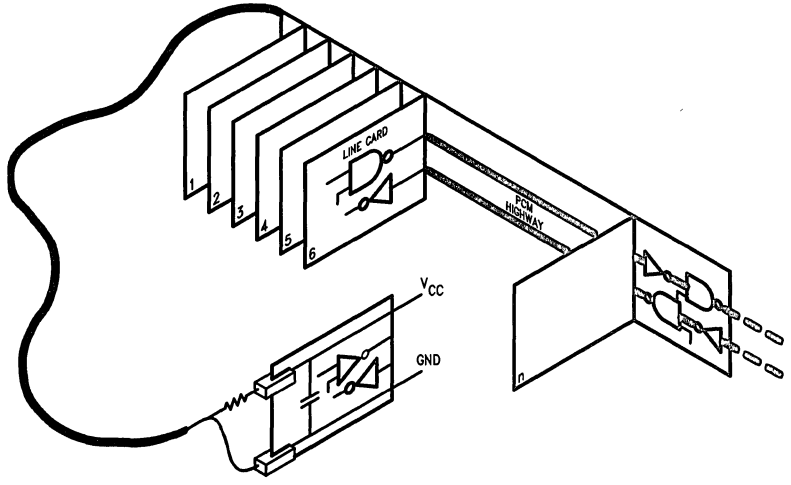

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FIGURE 5. Temporary Power Cord

IX. EXTENDING A BUS BEYOND THE RACK

The DS3898 (BTL repeater) is ideal for cases where the system bus must be extended. If the bus is of considerable length, the repeaters regenerate the signal levels. The repeaters also isolate, or separate, different electrical environments. For example, if a ribbon cable is used to connect one rack to another, the repeaters will isolate the different impedance and noise levels present in a ribbon cable from the bus on the rack.

X. USING THE PROPER BUS TERMINATION

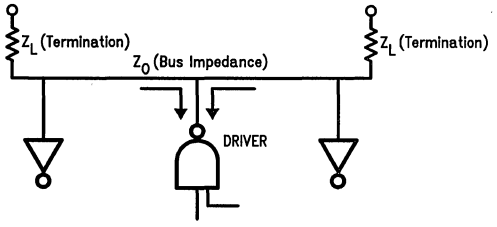

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FIGURE 6

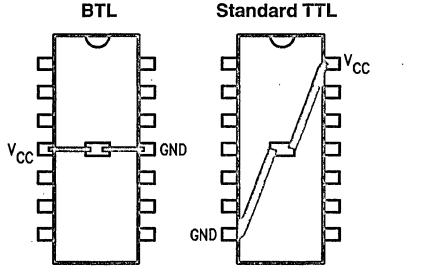
An ideal termination (Z_L) should match the bus impedance (Z_O) in order to eliminate reflections. If the termination matches the impedance of a fully loaded bus, then $Z_L = Z_O = 30\Omega$. With the 30Ω terminations, the driver is required to drive a ($Z_L \| Z_L = 30 \| 30$) 15Ω load. However, the lowest load that a standard TTL driver will guarantee is (5V/50 mA) 100Ω. If the designer uses the ($Z_L \| Z_L = 200 \| 200 = 100\Omega$ load) 200Ω terminations on the 30Ω bus, the reflections will be very large. On the other hand, BTL drivers can guarantee a (1V/50 mA) 20Ω load. In this case, the ($Z_L \| Z_L = 40 \| 40 = 20\Omega$ load) 40Ω terminations will have small reflections. Note that the improvement of the guaranteed load (from 100Ω to 20Ω) was achieved by reducing the voltage swing and driver output capacitance, NOT by increasing the current capabilities of the drivers.

XI. TWO VOLT RAIL

There are many ways of supplying the two volt rail needed for the 90/92/98. Four possibilities are: a separate two volt power supply; a voltage divider; a voltage regulator; and a high current voltage follower. The two volt power supply is very expensive to implement and does not track the five volt supply voltage, thereby reducing the effectiveness of the precision threshold. However, it is very efficient in terms of power consumption, making it appropriate for very large systems. The voltage divider is inexpensive, tracks the five volt supply voltage, but consumes too much current when the line is high. The voltage regulator is moderately efficient with current consumption, but does not track the five volt supply voltage. Finally, the high current voltage follower does not waste current when the line is high; is inexpensive to implement; and tracks the five volt supply voltage. Therefore, the high current voltage follower seems to be the best choice for small systems where cost is a major consideration.

XII. NOISE REDUCTION THROUGH IMPROVED PIN LAYOUT

In order to reduce ground noise caused by long lead inductance, one must make V_{CC} and GND lead lengths as short as possible. The packaging of National's BTL circuits contributes to shorter V_{CC} and GND lead inductance by placing the power pins in the center of the IC package, instead of the corners.



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Top View

FIGURE 7

XIII. OVERVIEW OF THE BTL TRAPEZOIDAL PRODUCT LINE

The BTL Trapezoidal products have low output capacitance (5 pF max), one volt signal swing, and noise immunity features which make them ideal for driving parallel, low impedance bus lines with minimum power dissipation.

- DS3890

The DS3890 is an octal BTL driver. It is designed specifically to overcome problems associated with driving densely populated backplanes. The trapezoidal wave forms and the one volt swing reduces noise coupling to adjacent lines. The open collector driver output allows for wired-OR connections.

- DS3892

The DS3892 is an octal receiver. The receivers have precision thresholds to increase the noise margins, and low pass filters to filter out crosstalk.

- DS3898

The DS3898 is an octal repeater. It combines the BTL characteristics of the DS3890 and DS3892. The part is ideal for extending backplanes.

- DS3896

The DS3896 is an octal high speed schottky bus transceiver with common control signals. It provides high package density for data/address lines.

- DS3897

The DS3897 is a quad transceiver with independent driver input and receiver output pins. It has a separate driver disable for each driver.

- DS3893

The DS3893 is the newest member of the family. It is designed to drive and receive signals at data rates of up to 100 MBaud. The trapezoidal feature has been removed to reduce the propagation delay down to 15 ns for the driver and receiver combination.

National's BTL drivers, receivers, and transceivers offer the most complete approach for operating high speed parallel backplanes.

"Intuitive ISDN"— An ISDN Tutorial

National Semiconductor
Application Note 492
Doug Gremel
Bob Poniatowski

WHAT IS ISDN?

The Integrated Services Digital Network, commonly called ISDN, is simply an all digital communications network which offers its users a variety of different capabilities. In due time, the ISDN will change the way that many, if not all of us communicate, be it through voice, data or video communication. To that end, the ISDN is an invisible rebuilding of the existing telephone network that will allow simultaneous voice and data communication over ordinary telephone lines.

What are the advantages that an integrated services digital network will offer? In order for ISDN to be successful, customers must see an economic payoff associated with ISDN. That payoff is perceived as an increased use of data communications without a linear increase in costs. For users of the network this means that anyone can take either a telephone, personal computer or any other form of data communications equipment and plug them directly into a standard phone jack and gain immediate access to a number of high speed data pipelines. The user will be able to dynamically allocate different 64 kbps channels to each of up to 8 pieces of terminal equipment. By terminal equipment we mean telephones, personal computers, facsimile machines, printers, thermostats, water and gas meters . . . and the list goes on. This revolutionary change will occur without changing the existing installed base of copper wire.

CCITT, the governing body of telecommunications standards defines the ISDN as:

A network evolved from the telephony integrated digital network that provides end-to-end digital connectivity to support a wide variety of services, to which users have access by a limited set of standard multipurpose customer interfaces.

THE CASE FOR ISDN

Without a doubt the past decade has brought us a one hundred fold increase in the utilization of data processing. Unfortunately, that increase has come at the cost of not being able to effectively communicate and share our individual data. We have created isolated islands of data processing.

For years now, telephone exchanges throughout the world have taken advantage of the capabilities of digital central office switching. This is due in great part to help from products such as National's COMBO™ family, which does the analog to digital conversion of voice signals. If one's voice conversation can be converted to a series of 1's and 0's it can be added, or multiplexed with other voice channels and several conversations can be carried simultaneously at high speed over a single phone wire. Presently this analog to digital conversion takes place at the central office switch.

The logical basis for the ISDN is simply to move the point of analog to digital conversion from the central office to the subscriber and make the transmitted signal a digital one. If this were accomplished, the subscriber would be able to take advantage of the ability to send digital data directly over the phone line. Since the phone network would not be able to distinguish between digital voice generated and digital computer generated data, a common access point for both types of services is created.

With a common access point created, the phone companies, among others, will be able to provide new services which customers will pay for. Although it is difficult to measure quantitatively, a resounding increase in productivity should be enjoyed by ISDN's subscribers.

ISDN GOAL: Global Connectivity

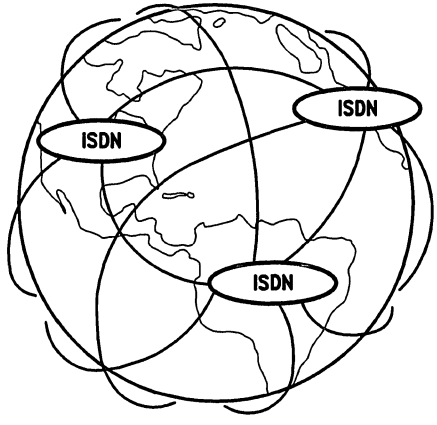

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FIGURE 1. Islands of Data Processing

It's easy to understand why the phone companies are so anxious to implement ISDN. From their point of view, the ISDN represents a new, revenue generating service which takes advantage of their large capital investment in their existing Telecom network. In addition, ISDN will help them keep customers. The RBOC's (Regional Bell Operating Companies) are presently faced with the competitive threat of a host of bi-pass schemes. In addition to the Telecommunications industry, there are also other proponents of ISDN.

The data processing industry has the vested interest in making sure that its equipment can communicate with other pieces of equipment. Many computer manufacturers have, in the past, intentionally tried to lock their customers into buying their equipment by maintaining a proprietary communications architecture. This strategy was sound while the industry was in its infancy, but users are beginning to consider the benefits of an open networking scheme. If there were a common communications backbone, computer manufacturers would benefit by selling more equipment as well as new services.

The proponents of ISDN have many different motivating factors for supporting a worldwide voice/data communications network. A common thread binding all ISDN supporters is the work of the standardization committees. Standards act to ensure inter-operability among a large set of similar equipment. They act for the benefit of three distinct groups. For the users of the network, the primary advantage is one of not being locked into the purchase of one type of equipment. For the service provider, standards guarantee a large user base, thus they encourage the service provider to make the investment necessary to reap any benefits. To manufacturers, building to a specification enables them to produce products of wide appeal and reduces the proprietary nature of equipment.

Along these lines, it has been said that there are 4 cornerstones to ISDN and 4 reasons for companies to invest in ISDN technologies.

Cornerstones

1. ISDN will reduce telephone companies costs by integrating more services over a single access line.
2. ISDN represents increased revenue for telephone companies.
3. ISDN will help proliferate intelligence within and beyond the network.
4. ISDN supports national and international standards.

FIGURE 3. Cornerstones of ISDN

ISDN IMPLEMENTATION ISSUES

The concept of a single access point for voice and data communication has a great deal of appeal. Many experts are saying that the dawn of the true information age will not be at hand until data communications can flow freely. Before we can begin to dream of what the information age will hold, there are several prerequisites that need to be fulfilled. The evolution of ISDN will actually occur in phases. In the first phase, a complete deployment of digital local switching must be in place. The digital central office represents the backbone of the network. Also, ISDN loop terminations will be required for each potential ISDN subscriber. In a second phase of deployment, ISDN capabilities will be extended between switching offices. This requires the deployment of CCITT's common channel signalling called signalling system #7. A third major phase will be the extension of ISDN services between networks. This would mean that a single world wide network would be operational. These prerequisites are outlined in *Figure 4*.

PHASE I	PHASE II	PHASE III
Digital CO's	SS#7	Inter-Networking
Loop Terminations	Digital Trunks	
ISDN Terminal Adaptors		

FIGURE 4. Evolution to ISDN

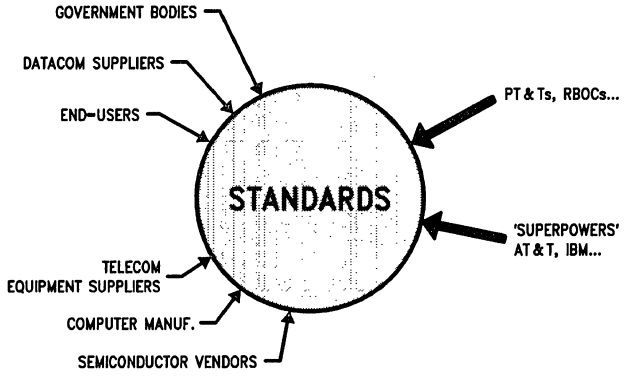

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FIGURE 2. Proponents of ISDN

Without compliance to a set of standards laid out by CCITT, the goal of ISDN will not be realized. The standards that are of most interest to vendors are those dealing with the S and U interfaces. At this point in time, the S interface is the most solidly defined interface. A complete description of the S interface function is outlined in CCITT's document I.430.

Most of the work in the U.S. standardization body, T1D1 is presently focused on the U interface.

Until the time that T1D1 standards are complete, no vendors can legitimately announce products which are "ISDN compatible". Rather, ISDN exists more in the press than it does in reality. Even Bell Operating companies are in the decision making process as to what services will be marketed and how their ISDN networks will be implemented. For this reason, Bell Operating companies are presently undertaking limited field trials using "psuedo-ISDN" services in a very limited manner. These field trials will supply user feedback and will greatly help define new services. In *Figure 5*, a time scale of ISDN implementation events is outlined.

ISDN Time Scale

1987 — T1D1 committee concludes definition of S interface

1987 — Limited field trials by RBOC's begin

1988 — T1E1 Committee concludes definition of U interface

1990 — Phase I implementation begins in some metropolitan areas

1991 — "Services" defined, Field trials complete

1992 — Phase II implementation underway, more metropolitan installations

1995 — Phase III implementation possible

FIGURE 5. ISDN Time-Scale of Implementation

ISDN TERMINOLOGY/DEFINITIONS

In order to convert a subscribers connection from an analog signal to a digital one, the termination at each end of the copper loop must be changed slightly. Upon this conversion, one of two connection types will be offered, Basic or Primary access. Under the **Basic Access** rate, each subscriber will be entitled to the use of 2 B channels and 1 D channel, **(2B + 1D).** For Basic Access each **B Channel** (B for Bearer) represents a 64 kbps channel and the **D Channel** (D for Delta) represents a 16 kbps channel. A minimum transmission rate of 144 kbps full duplex transmission is therefore required for basic access transport. Typically, a basic access subscriber will be a specific, individual subscriber as opposed to a multi-user subscriber such as a corporation, which will require several primary access lines.

Under the **Primary Access** rate, each subscriber in the United States and Japan will be able to transmit and receive over 23 B channels and 1 D channel **(23B + 1D).** This data rate is compatible with the 1.536 Mbps rate for T1 carriers for these countries. For the rest of the world the primary access rate offers users 30 B channels and 1 D channel. However, unlike the basic access rate the D channel in primary access represents a 64 Kbps channel.

In *Figure 6* we see the ISDN reference model for a basic access connection. The reference model shows a block diagram of how the communications link is established. In the diagram, blocks represent equipment or physical, tangible points along the phone line.

In *Figure 6* the **TE or Terminal Equipment** can represent either a digital telephone, a personal computer, a facsimile machine, a printer, a thermostat, gas meter etc. As you can see there are two types of terminal equipment. The **TE1** is a terminal which is synchronized to the ISDN network. This simply means that the terminal equipment was manufac-

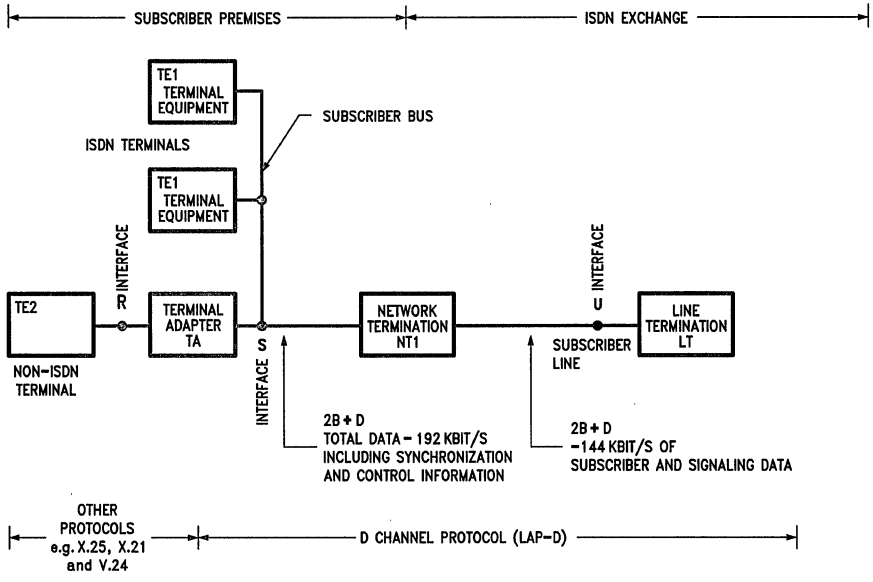

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FIGURE 6. ISDN Basic Access Reference Model

tured with the intention of being compatible with the ISDN network. The **TE2** on the other hand is a terminal which might not now be compatible with the ISDN network. Because TE2's are made before the existence of ISDN, it is the function of the **TA or Terminal Adaptor** to convert either asynchronous or synchronous data from non-ISDN terminals into data which is synchronized with ISDN B or D channels. The data rate must be adapted by stuffing extra bits into the bit stream in a prescribed pattern.

The next block in the model is the **Network Termination or NT.** The NT terminates the network at the user's end of the 2 wire loop (on the subscribers premises). It converts the "U" interface to the "S" and "T" interface and acts as the master end of the user's line. Just like the terminal equipment, the NT is also Customer Premises Equipment (CPE) and will be sold through retail outlets (except in Europe and Canada).

Further along the model is the **LT or Line Termination.** Typically, the LT consists of the "U" interface transceiver and power feeding functions on the ISDN line card.

In addition to the various blocks in the reference point model, the interfaces between the blocks are also of great interest. From the users point of view these interfaces can be considered pieces of copper wire. However, its in the interface between the blocks that the "intelligence" resides which enables the signal to be transmitted down the line. The intelligence is actually a transceiver device which is named appropriately after the interface function it accomplishes.

There are several functions that the **S Interface** fulfills. In addition to electrically connecting (in parallel) up to 8 TE's with the NT, what other functions does the S interface accomplish? For a basic access rate of 2B + D, 3 channels are available for use by 8 pieces of terminal equipment. Part of the S function is to arbitrate the use of these channels to however many TE's reside on the line. Fortunately, chances are good that no one will have more than 1 voice phone hanging on a 2B + D line. Since computers and the like don't need to be operated in real time, the S interface can control the use of the phone connection (always a circuit switched connection) and the 7 other pieces of terminal equipment can share the other 2 channels (packet switched connections). A user can maintain a voice connection on one of the B channels and simultaneously transmit data on the other B and D channels.

In order to get access to a B channel, certain formalities or protocols must be granted. These protocols are all regulated in the D channel. Thus, the term **LAPD for Link Access Protocol in the D Channel** is used to describe the process of attaining a connection via the D channel. LAPD is typically implemented in a software routine rather than being a hardware function.

When transmitted signals pass through the S interface, they are traveling over a 4 wire connection. This is due in part to the fact that the S interface function is required to do all the arbitration and control functions. As such, the distance over which the S interface can function is limited in distance. For a point to point configuration, in which only one TE is connected to the NT, the S interface is specified to have a range of 1 Km. If the S interface is fully burdened by all 8 TE's, a loop length of only 200m can be attained.

In contrast, signals transmitted over the **U Interface** are carried over only 2 wires. This is due to the fact that the phone company supplies only 2 wires to any given subscriber. If you will remember, the NT is considered Customer Premises Equipment (CPE) and physically resides at the end of the 2 wire loop. Now that the transmitted signal travels over only 2 wires rather than 4, the signal must be transmitted in both directions simultaneously. This transmission technique is called **Echo Cancellation.** In an echo cancellation based transmission, signals from the transmitted point are effectively cancelled from the receiver of the transmitted point, therefore the receiver will only hear what the transmitter at the far end of the line is sending. This is a very complex transmission scheme. But none the less, such a scheme is needed to transport the digital signals the required length of as much as 18 kft.

NATIONAL SEMICONDUCTORS ROLE IN THE ISDN

Obviously, the concept of the ISDN would not be possible if not for the technological accomplishments of these past 5 years. At the heart of these advances are the implementation of VLSI integrated circuit technology.

National Semiconductor will play a key role in the evolution towards an Integrated Services Digital Network, VLSI devices which are cost effective solutions must be used if ISDN is going to become a wide scale economic reality.

Because so much of the system itself is becoming integrated into standard devices, National does play a key role in the definition of standards for the ISDN. Along with this participation in standard setting goes the willingness to comply wholeheartedly with those standards.

As the Semiconductor industries' leading supplier of dedicated Telecom IC's, National is in an excellent position to take advantage of its years of experience when implementing new ISDN devices. Key to this success are the relationships built over the years with customers and the ongoing dialog necessary to define successful products.

National is driving standards through T1E1 involvement

National is providing basic silicon blocks which will make ISDN practical

National is providing a silicon architecture which will become a de-facto standard

FIGURE 7. National's Role in the ISDN

In developing the architecture of its ISDN chip set, National's major objective has been to create a flexible set of building blocks which provide elegant and cost-effective solutions for a wide range of applications. With just a few highly integrated devices, a broad spectrum of ISDN equipment can be designed, ranging from Central Office and PBX line cards to X.25 and ISDN Terminals and telephones, PC terminal adaptors, NT's and more.

National's ISDN Chip-Set

TP3400 DASL	TP3076 COMBO II
TP3420 SID	TP3451 HDLC Controller
TP3410 Echo Canceller	TP3460 Rate Adapter
HPC16400 Protocol Controller	

The first device from National is the TP3420 S Interface Device (SID). The SID implements entirely the functions outlined in the CCITT I.430 document (which is the worldwide standard). In addition, the SID includes noise filtering and a high resolution digital phase locked loop to provide transmission performance in excess of that specified in the standard. All activation and D channel access sequences are handled automatically by the SID. The TP3421, a GCI version of the SID (GCI is an interchip protocol popular in Europe) is also available.

The second National transceiver is the TP3401 Digital Adapter for Subscriber Loops (DASL). The DASL is a low cost burst-mode transceiver for 2 wire PBX and private network loops up to 6 kft in length. The DASL functions as a U interface for networks that don't have the long loop lengths of the Central Office.

The TP3410 U Interface Device is the third transceiver offered by National. The TP3410 is a full feature, single chip 2B1Q Echo Canceller which is capable of transmitting data over a 18 kft loop. Features include a fully automatic adaptive receiver, maintenance channel processing, and a programmable time slot assigner. This has resulted in a flexible transceiver solution which is highly integrated with superior transmission performance. The National U Interface complies in full with the ANSI T1.601-1988 standard.

National has also developed a 16-bit microcontroller specifically for use in ISDN applications, the HPC16400. This microcontroller is ideally suited for ISDN. In addition to the HPC 16-bit microcontroller "core", it contains 2 HDLC controllers (used in message processing), an on board UART (for rate adaption), and 4 full DMA channels.

A single channel HDLC controller, the TP3451 is also offered by National. Both LAPB and LAPD protocols are supported on the chip, and 64 byte FIFOs are implemented in each of the transmit and receive paths. The HDLC controller may be used in conjunction with the HPC in TE and TA applications which require three HDLC channels.

The TP3076 COMBO II™ is a Programmable PCM CODEC/Filter. This device features programmable channel gains, time slot assignment, and interface latches to support applications requiring voice channels.

The TP3460 R Interface is a special USART for performing V.110 and V.120 rate adaption. This chip will interface TE2 equipment to the ISDN with full asynchronous and bit synchronous capability.

National's ISDN development board, the TP3500, allows today's designers to prototype their ISDN system quickly and efficiently. Both data and voice calls are supported, with the ability to individually exercise each of National's ISDN components. The system can be controlled from a standard VT100 terminal, and access is provided for a protocol analyzer.

National also provides customers with access to its ISDN Applications Laboratory, a state of the art ISDN development center. The ISDN lab allows customers to review and debug their design with the assistance of National's application engineers. All of the tools necessary to evaluate prototype products are available, including connections to both Northern Telecom and AT&T switches.

All of National's ISDN software has been developed in conjunction with Telenetworks, an independent software vendor specializing in telecommunications software. The complete software package is supported by Telenetworks, and includes training and technical support. The code has been developed in C, and is structured around the MTEX real time operating system.

National has also formed an alliance with SGS Thomson Microelectronics. This means that a second source is available for all of National's ISDN products now and in the future. All of the NSC/ST ISDN products are developed jointly but manufactured separately by both companies. This results in the ability to quickly respond to market trends and standards updates while providing our customers with the advantages of a true second source.

In short, National Semiconductor has the experience, resources, and products to help you develop products for ISDN today.

Using the TP3401/2/3 ISDN PBX Transceivers

National Semiconductor
Application Note 509
Casey Tsai and Bart Vos

INTRODUCTION

The TP3401 Digital Adapter for Subscriber Loops (DASL) is a low-cost burst-mode transceiver for 144 kb/s full-duplex on single twisted-pair PBX and private network loops up to 1.8 km in length. Scrambled alternate mark inversion coding is used, together with adaptive equalization and timing-recovery, to ensure low bit error rates on a wide variety of cable types. A multiplexed interface for two 64 kb/s "B" channels and one 16 kb/s "D" channel is provided. This application note, together with the TP3401 datasheet, provides the system designer with a thorough understanding of the device's operation as well as some sections that are useful to the terminal equipment designer. It covers the following topics:

1. Typical Application at the Terminal End
2. Activation/Deactivation Procedures
3. Repeater Mode Application
4. Transformer Design Guide
5. Surge Protection Methods at the Line Interface
6. Bit Error Rate Performance

1. TYPICAL APPLICATION AT THE TERMINAL END

a. System Description

For the purpose of this application note, a terminal which is designed to offer one PCM voice channel and one data channel will be discussed, although many other combinations can easily be configured.

As shown in *Figure 1*, the HPC16400 Microcontroller and TP3054/7 COMBO™ directly interface to DASL at the terminal end of the loop.

b. Main Controller HPC16400

The HPC16400 is a 16-bit highly integrated microcomputer which supports a wide range of communication application, this chip includes two HDLC channels, a DMA controller, programmable serial interface, UART and MICROWIRE/PLUS™ serial interface. This set of features makes the HPC16400 an ideal processor for running all the functions of an ISDN Terminal Adapter, TE or Telephone.

In a typical application as shown in *Figure 1*, one of the HDLC channels is dedicated to handle the LAPD protocol in the "D" channel, while the other provides packet-mode access to one of the "B" channels. The MICROWIRE/PLUS serial interface is used to transmit/receive the TP3401 control/status register byte for handling its activation/deactivation. The UART would serve as an RS232 interface running at any of the standard synchronous or asynchronous rates up to 128 kbaud. The DMA controller provides several register sets for packet RAM management with minimal CPU intervention, including "chaining" of successive packets.

c. COMBO TP3054 Interface Description

The TP3054 is a μ-law serial interface PCM Codec/Filter COMBO. When power is first applied, power-on reset circuitry initializes the chip and places it into a power-down state. All non-essential circuits are deactivated and the Dx, VFr0 output pins are put in high impedance states. To power-up the device a logical low level, which is controlled by an HPC16400 I/O pin, must be applied to the MCLKr/PDN pin. For synchronous operation, this application uses the same master clock and bit clock which come from the TP3401 for both the transmit and receive directions. In this mode, a clock must be applied to MCLKx/BCLKx pins and the MCLKr/PDN pin is used as a power-down control; also the BCLKr/CLKSEL pin is tied to ground for selecting master clock frequency 2.048 MHz. Both the FSr and FSx frame sync pulses come from the TP3401 for long frame sync operation.

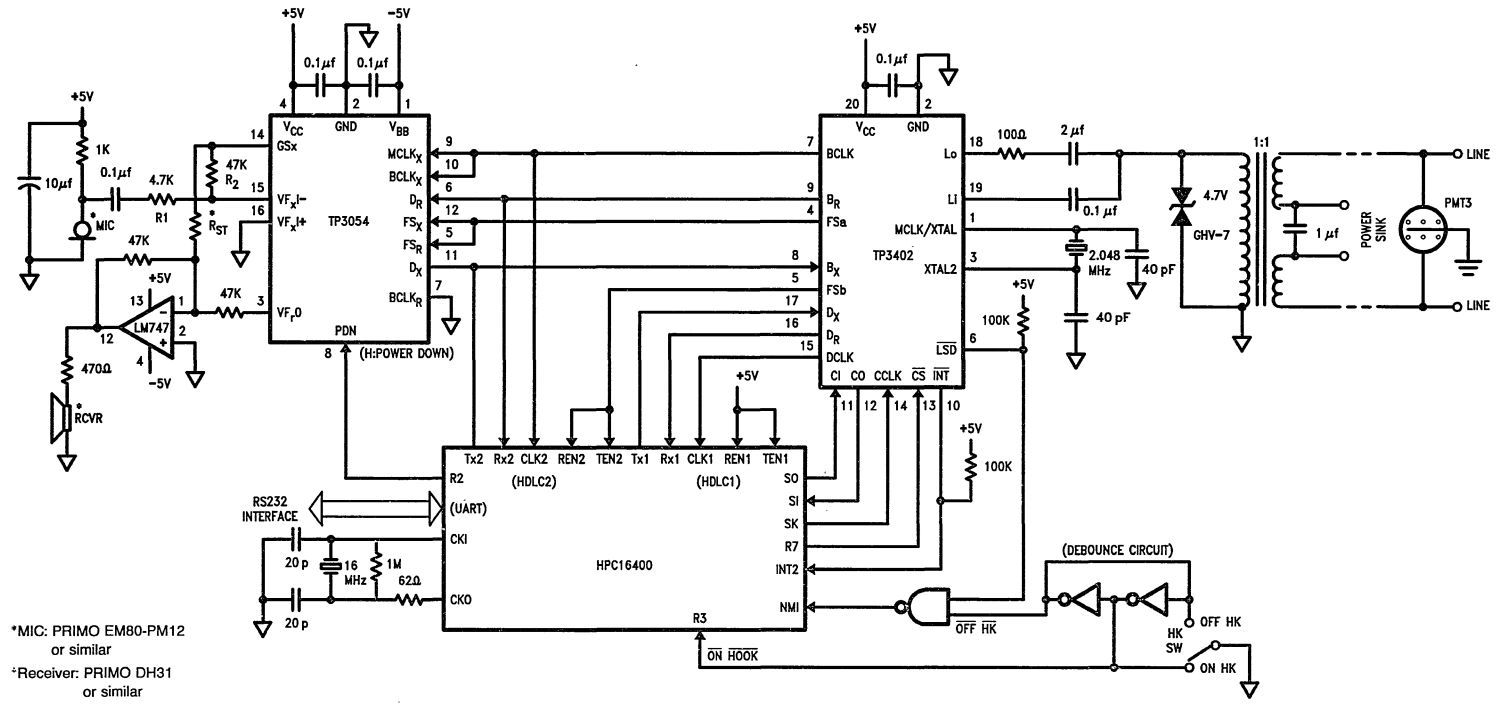
The analog transmit input is an operational amplifier with provision for gain adjustment using two external resistors, R1 and R2. The analog receive output is added with side tone into the LM747 input, and the LM747 output drives the earphone.

d. Activation

The line signal detect output or hook switch, applied to the NMI pin, wakes up the HPC16400. After the HPC16400 wakes up, it starts to read DASL status register bits through MICROWIRE™ to decide which end is initiating the call. The state of the C0 bit indicates whether the far end or the near end is activating the call; C0 is one ($\overline{LSD}$ = 0) for far-end activation and C0 is zero (off-hook) for near-end activation.

The HPC16400 powers up DASL by writing control register bit C6 = 1 through MICROWIRE. DASL starts sending a 2 kHz burst rate of scrambled 1s in the B and D channels to the line. Now HPC16400 is waiting for a MICROWIRE interrupt to check when DASL is in sync. If DASL status bit C1 changes to one (loop-in-sync), first the HPC16400 enables the HDLC 1 port which starts to handle the D channel at the Tx1 output pin, continuously sending FLAGs (01111110) to the far end and at Rx1 input pin looking for FLAGs. Then the HPC16400 powers up the COMBO for B1 channel communication and enables HDLC 2 port for B2 channel communication.

I/O port R3 is connected to $\overline{\text{on-hook}}$ signal as an input port. The HPC16400 polls this input port every 50 ms after the B1 channel is activated to monitor the hook-switch status. If the logic level of R3 pin changes from high to low, this means the terminal end disconnected the call by hook-switch during the B1 channel activation state, so the HPC16400 passes the B1 channel disconnection message to the network through the D channel. (See Section 2).



*MIC: PRIMO EM80-PM12 or similar

‡Receiver: PRIMO DH31 or similar

*RST for side tone gain adjustment. Typical R = 47k

TL/H/9429–1

FIGURE 1. Typical Application for Terminal End

2. ACTIVATION/DEACTIVATION PROCEDURES

a. General Outline of the User-Network Interface

As shown in *Figure 2*, the user-network interface is based on peer-to-peer protocols from layer 1 to layer 3. All signaling messages on the D channel are used to exchange control information between the user and the network for call establishment and termination, and access to network facilities. The main functions in the three protocol layers involving network and terminal are listed below.

Layer 1, physical layer, includes functions for transmission, power feeding, activation/deactivation and maintenance.

Layer 2, data link layer. All data link layer messages in the peer-to-peer protocol are transmitted in frames which are delimited by flags. The denomination of the protocol procedure is LAPD, Link Access Procedures on the D Channel. LAPD includes functions for the provision of one or more logical link connections on the D channel, sequence control of messages, detection of errors and flow control.

Layer 3, network layer, includes functions for establishing, maintaining, and terminating circuit-switched connections, user-to-user signaling connections and packet-switched connections.

b. The Recommended Activation Procedure (Layer 1) from the NETWORK, i.e. TP3401 on a line card, is illustrated in Table I.

c. The Recommended Activation Procedure (Layer 1) from the TERMINAL is illustrated in Table II.

d. A Software Control Flow Chart for USER End Activation/Deactivation (Layer 1) is illustrated in Table III.

e. Call Clearing Procedure (Layer 3) is usually initiated by the user or the network sending signaling messages on the D channel across the user-network interface.

Clearing by the user: The terminal sends a DISConnect message. Following the receipt of a DISConnect message, the network considers the call to be in the disconnect-request state and disconnects the B channel that is used in the call, then the network returns a RELease message to the terminal. On receipt of the RELease message the terminal releases the B channel and the call reference, then sends a RELease COMplete message to the network.

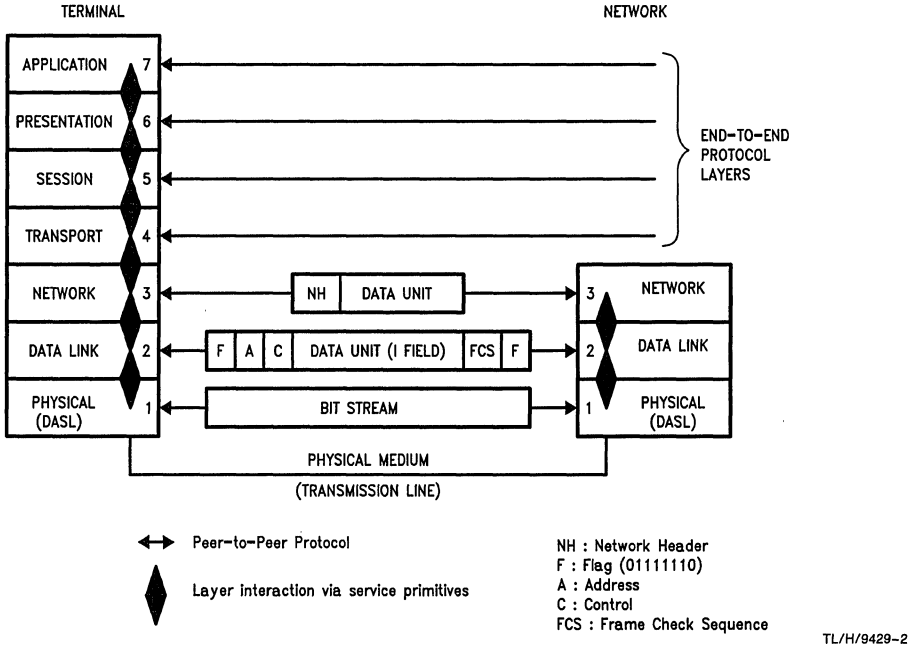


FIGURE 2. Protocol for the Signaling Procedure on the D Channel

Clearing by the network: The network sends a DISConnect message across the user-network interface and disconnects the B channel that was used in the call. Following the receipt of a DISConnect message, the user sends a RELease message to the network. On receipt of the RELease message, the network returns a RELease COMplete message to the terminal and releases the B channel and call reference for future use.

Note 1: Before loop-in-sync (C1 = 1) at the SLAVE (terminal) end, Fsa/Fsb and Fsc (TP3401 only) output pins are zero, the Br data output pin is tri-stated, Dr data output pin is high, BCLK and DCLK are free running outputs at 2.048 MHz and 16 kHz respectively, Bx and Dx data input pins are ignored, Lo output pin is sending 2 kHz burst rate of scrambled 1s in the B and D channels to the line.

Note 2: Before loop-in-sync (C1 = 1) at the MASTER (network) end, the Br data output pin is high during Fsb enable, otherwise that pin is tri-stated; Dr data output pin is high, $\overline{TS}_r$ output pin is low during B1/B2 received time slot, Bx and Dx data input pins are ignored, Lo output pin is sending 4 kHz burst rate of scrambled 1s in the B and D channels to the line.

Note 3: After the bit C1 = 1 (loop-in-sync) at the SLAVE (terminal) end, the HPC can start a timer and wait 2 ms to allow the network end to acquire loop-in-sync before attempting to enable B and D channels.

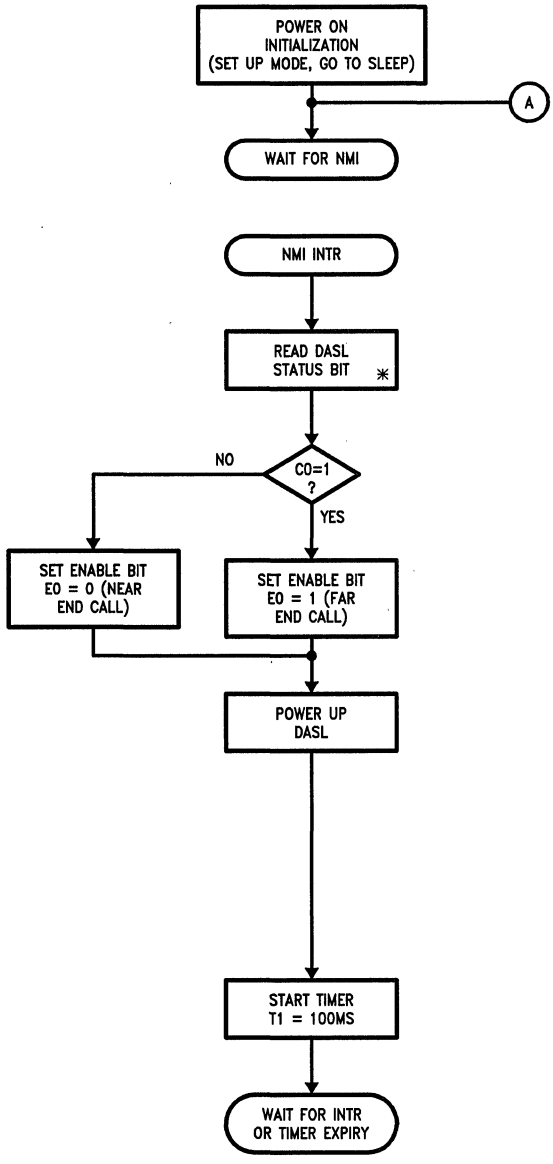
TABLE I. Activation from the Network End

Terminal End		Line	Network End	
HPC or μP	**DASL (SLAVE)**		**DASL (MASTER)**	**HPC or μP**
				1. Powers up DASL by writing control register bit C6 = 1 through MICROWIRE. Also starts the Default Timer.
	3. $\overline{LSD}$ pin goes low to wake up HPC, DASL status bit C0 changes to one and generates a MICROWIRE interrupt to the HPC.	← Tx 4 kHz burst	2. Starts sending 4 kHz burst rate of scrambled 1s in B and D channels to the line.	
4. Reads DASL status register and writes control register bit C6 = 1 through MICROWIRE to power up DASL. Also starts the Default Timer.				
	5. Starts sending 2 kHz burst rate of scrambled 1s in the B and D channels to the line.	→ Tx 2 kHz burst	6. The line signal detect circuit changes status bits C0 to one and generates a MICROWIRE interrupt to the HPC.	7. Reads DASL status register through the MICROWIRE interface.
	8. Flywheel circuit searches for 4 consecutive correctly formatted bursts, then sets status bit C1 = 1 (loop-in-sync) and generates a MICROWIRE interrupt. DASL starts to send 4 kHz burst data. (Note 1)	→ Tx 4 kHz burst (loop-in-sync)	10. Same as step 8. C1 = 1, loop-in-sync. (Note 2)	
9. Reads DASL status register. If C1 = 1, the HPC stops the Timer, enables the HDLC port to handle D channel signaling data first, then enables the B channels for voice data. (Note 3)				11. Same as step 9.
		← Tx 4 kHz burst (loop-in-sync)		

TABLE II. Activation from the Terminal End

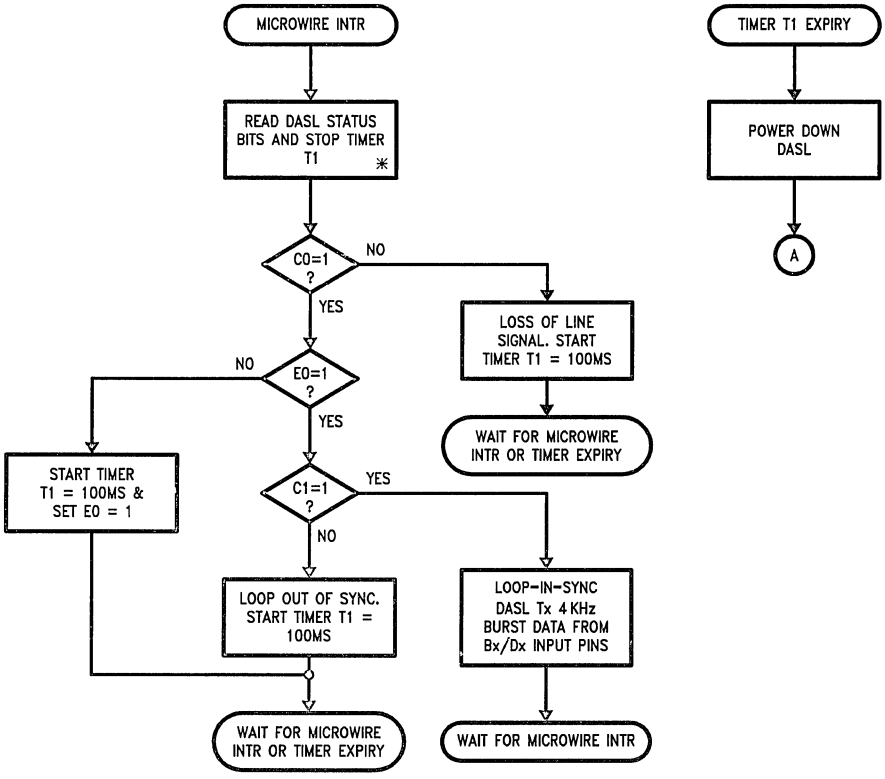
Terminal End		Line	Network End	
HPC or μP	DASL (SLAVE)		DASL (MASTER)	HPC or μP
1. Powers up DASL by writing control register bit C6 = 1 through MICROWIRE. Also starts Default Timer.	2. Starts sending 2 kHz burst rate of scrambled 1s in the B and D channels to the line.	→ Tx 2 kHz burst	3. The line signal detect circuit changes status bit C0 to one and generates a MICROWIRE interrupt to the HPC.	4. Reads DASL status register and writes control register bit C6 = 1 through MICROWIRE to power up DASL. Also starts the Default Timer.
	6. $\overline{\text{LSD}}$ pin goes low, DASL status bit C0 changes to one and generates a MICROWIRE interrupt to the HPC.	← Tx 4 kHz burst	5. Starts sending 4 kHz burst rate of scrambled 1s in the B and D channels to the line.	
7. Reads DASL status register through the MICROWIRE interface.	8. Flywheel circuit searches for 4 consecutive correctly formatted bursts, then sets status bit C1 = 1 (loop-in-sync) and generates a MICROWIRE interrupt.			
9. Reads DASL status register. If C1 = 1, the HPC stops the Timer, enables the HDLC port to handle D channel signaling data first, then enables the B channels for voice data. (Note 3)	DASL starts to send 4 kHz burst data. (Note 1)	→ Tx 4 kHz burst (loop-in-sync) ← Tx 4 kHz burst (loop-in-sync)	10. Same as step 8. C1 = 1 loop-in-sync. (Note 2)	11. Same as step 9.

TABLE III. Activation/Deactivation Flow Chart at Terminal (Slave) End



TL/H/9429–3

TABLE III. Activation/Deactivation Flow Chart at Terminal (Slave) End (Continued)



TL/H/9429–4

*When reading the CO pin, data is always clocked into the CI pin, therefore the CI data word should be set to repeat the previous data word if no change in device mode is intended.

3. REPEATER MODE APPLICATION

a. System Description

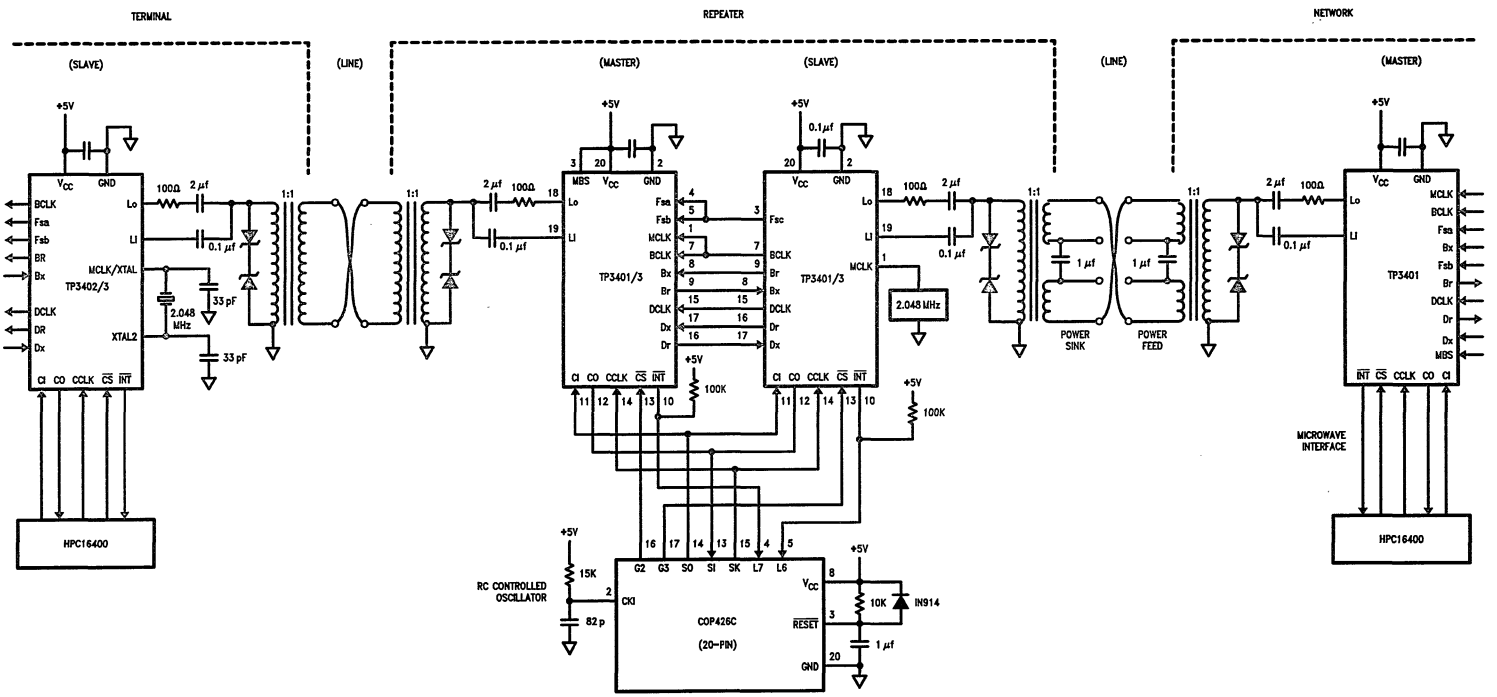
In applications where a range beyond 1.8 km is required, a simple back-to-back connection of two DASLs provides a range extension capability out to 3.6 km. A low-cost microcontroller manages the activation and deactivation of the two loops, and B and D channel data passes transparently through between the two loops. Power for the REPEATER can be sourced from either end of the system.

As shown in *Figure 3*, two DASLs, which are connected back to back as master and slave to form a REPEATER, are directly controlled by a COP426C. The COP426C (Controller Oriented Processor) is a 4-bit complete microcomputer containing all system timing, MICROWIRE serial interface, 1k × 8 ROM and 64 × 4 RAM, 15 I/O lines, programmable read/write 8-bit timer/event counter, a true vectored interrupt and three-level subroutine stack.

In a typical application, the $\overline{INT}$ output pins of the two DASLs connect to L6 and L7 input pins of the COP426C. Also the G2 and G3 output pins of COP426C provide a chip select ($\overline{CS}$) signal to each DASL to enable the MICROWIRE serial interface. The COP426C, running on a slow R-C controlled clock, polls the input ports L6 and L7 every 4 ms. If either of these inputs changes to zero, the COP426C starts to run its activation/deactivation program as shown in the flow chart in Table VI; otherwise the COP426C goes to the idle mode, which takes only about 1 mA current for power saving. During activation, the loop at the Network end will always fully synchronize before the loop at the terminal end can synchronize. Network timing is thus passed on to the terminal. Only the Slave-mode DASL on the network side requires a 2.048 MHz clock oscillator; the Master-mode DASL on the terminal side uses the Slave's BCLK output as its MCLK timing source.

b. The Recommended Activation Procedure (Layer 1) from the NETWORK is illustrated in Table IV.

c. The Recommended Activation Procedure (Layer 1) from the TERMINAL is illustrated in Table V.



TL/H/9429–5

FIGURE 3. Typical REPEATER Application

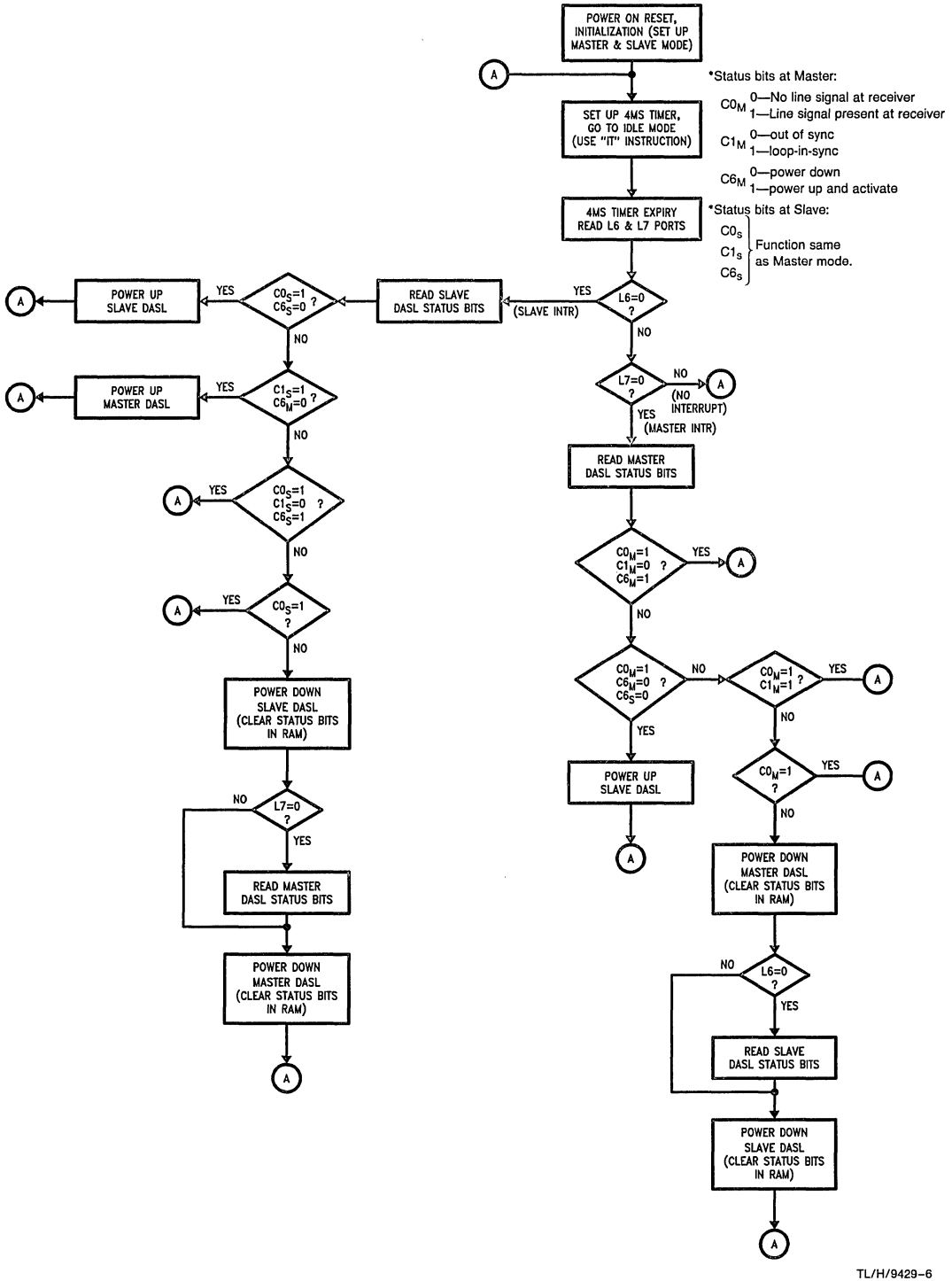
TABLE IV. Activation from Network for Repeater

Terminal End	Line	Repeater		Line	Network End
DASL (SLAVE)		DASL (MASTER)	DASL (SLAVE)		DASL (MASTER)
					1. HPC powers up DASL by writing control bit C6 = 1 through MICROWIRE and also starts the Default Timer. DASL starts sending 4 kHz burst rate of scrambled 1s in the B/D channels to the line.
			2. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to COP. COP reads DASL status register and writes control bit C6 = 1 through MICROWIRE to power up the DASL. DASL starts sending 2 kHz burst rate of scrambled 1s in the B/D channels to the line.	← Transmit 4 kHz burst → Transmit 2 kHz burst	3. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the HPC. HPC reads DASL status register through the MICROWIRE interface.
		5. COP powers up DASL by writing control bit C6 = 1 through MICROWIRE. DASL starts sending 4 kHz burst rate of scrambled 1s in the B/D channels to the line.	4. DASL flywheel circuit searches for 4 consecutive correctly formatted bursts and sets status bit C1 = 1, also DASL generates MICROWIRE interrupt and sends 4 kHz burst data from digital interface Bx and Dx to the line. COP reads DASL status register through MICROWIRE.		
6. $\overline{\text{LSD}}$ pin goes low to wake up HPC, DASL status bit C0 changes to 1 and generates MICROWIRE interrupt to HPC. HPC reads DASL status register and writes control bit C6 = 1 through MICROWIRE to power up the DASL. DASL starts sending 2 kHz burst rate of scrambled 1s in the B/D channels to the line.	← Transmit 4 kHz burst → Transmit 2 kHz burst → Transmit 4 kHz burst (loop-in-sync)	8. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the COP. COP reads DASL status register through MICROWIRE interface.		→ Transmit 4 kHz burst (loop-in-sync) ← Transmit 4 kHz burst (loop-in-sync)	7. DASL flywheel circuit searches for 4 consecutive correctly formatted bursts and sets status bit C1 = 1, also DASL generates an interrupt and sends 4 kHz burst data that comes from digital interface Bx/Dx to the line. HPC reads DASL status register. If C1 = 1, HPC stops the Timer, enables the HDLC port to handle D channel signaling data first, then enables B channel. for voice data
9. Same as step 7. C1 = 1, loop-in-sync.	← Transmit 4 kHz burst loop-in-sync)	10. Same as step 4. C1 = 1, loop-in-sync.			
		ACTIVATION COMPLETION			

TABLE V. Activation From Terminal for Repeater

Terminal End	Line	Repeater		Line	Network End
DASL (SLAVE)		DASL (MASTER)	DASL (SLAVE)		DASL (MASTER)
1. HPC powers up DASL by writing control bit C6 = 1 through MICROWIRE and starts the Default Timer. DASL starts sending 2 kHz burst rate of scrambled 1s in the B/D channels to the line.	→ transmit 2 kHz burst	2. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the COP. COP reads DASL status register through MICROWIRE interface.	3. COP powers up DASL by writing control bit C6 = 1 through MICROWIRE. DASL starts sending 2 kHz burst rate of scrambled 1s in the B/D channels to the line.	→ Transmit 2 kHz burst	4. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the HPC. HPC reads DASL status register starts the Default Timer, writes control bit C6 = 1 through MICROWIRE to power up DASL. DASL starts sending 4 kHz burst rate of scrambled 1s in the B/D channels to the line.
			5. Same as step 2.	← Transmit 4 kHz burst	
			6. DASL flywheel circuit searches for 4 consecutive correctly formatted bursts and sets status bit C1 = 1, also DASL generates an interrupt and sends 4 kHz burst data from digital interface Bx and Dx to the line. COP reads DASL status register through MICROWIRE.		
		7. COP powers up DASL by writing control bit C6 = 1 through MICROWIRE. DASL starts sending 4 kHz burst rate of scrambled 1s in the B/D channels to the line.			
8. DASL status bit C0 changes to 1 and generates a MICROWIRE interrupt to the HPC. HPC reads DASL MICROWIRE interface.	← transmit 4 kHz burst			→ Transmit 4 kHz burst (loop-in-sync)	9. DASL flywheel circuit searches for 4 consecutive correctly formatted bursts and sets status bit C1 = 1, also DASL generates an interrupt, sends 4 kHz burst data that comes from digital interface Bx/Dx to the line. HPC reads DASL status register. If C1 = 1, HPC stops the Timer, enables the HDLC port to handle D channel signaling data first, then enables the B channels for voice data.
10. Same as step 9. C1 = 1, loop-in-sync.	→ transmit 4 kHz burst (loop-in-sync) ← transmit 4 kHz burst (loop-in-sync)	11. Same as step 6. C1 = 1, loop-in-sync.		← Transmit 4 kHz burst (loop-in-sync)	
		ACTIVATION COMPLETION			

TABLE VI. Activation/Deactivation Flow Chart for REPEATER Mode



TL/H/9429–6

4. TRANSFORMER DESIGN GUIDE

Two different transformer designs are described here, one for "DRY" loops, in which no D.C. current is flowing, and one for "WET" loops in which power feed current is supplied to the terminal via split windings. A 1:1 turns ratio is used, with a 100Ω termination impedance for good line impedance matching over the bandwidth of the line signal.

a. Dry transformer: no D.C. current through the transformer.

Dry transformer specification:

1. Ferrite core
   Siemens EP13-T38 or equivalent
   AL = 7000 nH/T-2 (ungapped)
2. Windings

Np	1–2	50T(AWG #34)
Ns1	3–4	25T(AWG #34)
Ns2	5–6	25T(AWG #34)

3. Inductance
   16 mH (ungapped) at 1 kHz
4. D.C. resistance
   Np = 0.52Ω (max)
   Ns1 = Ns2 = 0.26Ω (max)
5. Impedance
   100Ω
6. Frequency response
   Bandwidth: −3 dB down at 1 kHz and 1 MHz
   Return loss: More than 20 dB from 48 kHz to 192 kHz

b. Wet transformer: designed for ≤50 mA current through the transformer.

Wet transformer specification:

1. Ferrite core
   Siemens EP13-T38 or equivalent
   AL = 500 nH/T-2 (with 1-mil paper gapped)
2. Windings

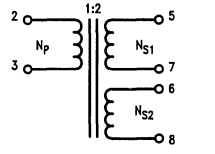
Np	1–2	130T(AWG #34)
Ns1	3–4	65T(AWG #34)
Ns2	5–6	65T(AWG #34)

3. Inductance
   8.7 mH (with 1-mil paper gapped) at 1 kHz
4. D.C. resistance
   Np = 3.0Ω (max)
   Ns1 = Ns2 = 2.0Ω (max)
5. Impedance
   100Ω
6. Frequency response
   Bandwidth: −3 dB down at 1.3 kHz and 900 kHz
   Return loss: More than 20 dB from 48 kHz to 192 kHz

Following is a list of vendors of 1:1 and 1:2 transformers which have been designed for use with the TP3401 DASL.

U.S.

1. AIE Magnetics (Florida); phone 813-347-2181.
   Part Number: 1:1 (center tapped) 325-0244 (EP10 core);
2. Schott Corporation (Nashville); phone 615-889-8800.
   Part Numbers: 1:1 (center tapped) 11085; (dry)
   1:1 (center tapped) 11086 (50 mA DC)



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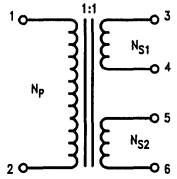

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5. SURGE PROTECTION METHODS AT THE LINE INTERFACE

There are two main sources of transient high voltages, lightning and short circuit wiring faults to commercial power systems. The induced overvoltage can seriously damage voltage sensitive components, so at least two levels of protection are required on the line interface as shown in *Figure 4*.

a. Protection at Secondary of Transformer

The protector at the secondary of the transformer is usually placed on the line at a distance greater than 25 meters from the linecard; the impedance of the line will ensure that this protector always operates first. A suitable protector is a gas discharge tube, which has high insulation resistance, low capacitance and high current capability, such as a three electrode gas discharge surge arrester PTM3(310).

PMT3(310) Specifications:
Manufacturer: General Instrument Corp.
D.C. breakdown voltage: 250V
Pulse breakdown voltage: Less than 1600V at a ramp speed of 10,000 V/μs
Peak surge current: 10,000 A
Holdover voltage: 100V and 150V minimum
Surge life: 400 surges average (500A, 10/1000 μs)
Capacitance: Less than 5 pF

b. Protection at Primary of Transformer

The protection at the primary of the transformer can be provided by either a Zener diode or Varister; in the application shown in *Figure 4* is one GHV-7 Varister.

GHV-7 Specifications:
Manufacturer: General Semiconductor Industries, Inc.
Breakdown voltage Bv: 4.7V
Max surge current: 30 A (8.4 ms), 100 A (1.0 ms)
Capacitance: Less than 150 pF

6. BIT ERROR RATE PERFORMANCE

a. General Description

On the receiver side of DASL, data detection is accomplished by threshold comparison synchronized to the received signal timing. A first-order adaptive equalizer has been computer optimized and field tested on a variety of PBX and short range subscriber networks. Performance objectives are based on standard twisted pair cable characteristics. The equalized signal is processed by a wave-difference time-extractor and loop filter circuit followed by level data-detection. A novel design of an early-late DPLL with effective 30 ns step increments guarantees timing precision and stability.

b. Test Set-Up

The following BER measurements for DASL have been taken in burst mode at 144 kb/s full duplex two wire transmission, using 1:1 transformers.

Loop lengths of up to 2 km of 22 AWG, 24 AWG and 26 AWG cable have been used.

For the measurements on the 22 AWG and 26 AWG cable, a TAS 2100 loop emulator was used.

A white noise signal, band-limited to 500 kHz, was inserted at the receiver's input.

Bit error rates were measured by transmitting 100 million bits using pseudo random patterns.

1 km/24 AWG, input signal level 295 mV_{PP}:

noise level ($\mu V/\sqrt{Hz}$)	BER
14.1	0.0 E-7
17.7	1.0 E-7
21.2	1.3 E-5

2 km/24 AWG, input level 95 mV_{PP}:

noise level ($\mu V/\sqrt{Hz}$)	BER
3.5	0.0 E-7
5.3	9.7 E-7
7	8.8 E-5

1 km/22 AWG, input level 440 mV_{PP}:

noise level ($\mu V/\sqrt{Hz}$)	BER
22.1	0.0 E-7
28.3	2.0 E-6
35.4	9.1 E-5

1.8 km/26 AWG, input level 75 mV_{PP}:

noise level ($\mu V/\sqrt{Hz}$)	BER
3.5	0.0 E-7
5.3	4.3 E-7
7	8.4 E-6

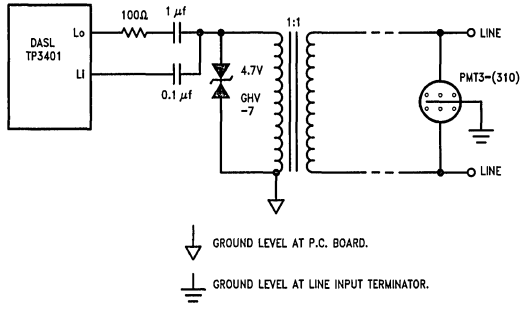
In addition to the above mentioned test method, BE rates have also been measured in the presence of a single tone interference signal at approximately twice the frequency of the main spectral lobe (in this case 400 kHz).

Range 1 km/24 AWG cable, 295 mV_{PP} input level:

BER = 0.0 E7 for a 53 mV_{PP} sine wave at 400 kHz.

Range 2 km/24 AWG cable, 95 mV_{PP} input level:

BER = 0.0 E-7 for a 14.4 mV_{PP} sine wave at 400 kHz.



TL/H/9429–8

FIGURE 4. Typical Protection Arrangement

Building an ISDN Terminal/ Terminal Adapter

National Semiconductor
Application Note 520
Chris Stacey

Originally Presented at WESCON 1987

INTRODUCTION

As ISDN starts to gather momentum, an ever-increasing variety of equipment will need to be designed, both by traditional Telecom switching and transmission vendors and by the data communications industry. ISDN chip sets which have not been defined with this perspective in mind are likely to be cumbersome and not cost-effective to use. A chip set for ISDN Basic Access which provides a high level of integration while retaining architectural flexibility is described here, beginning at the 'Layer 1' boundary, the 'S/T' interface.

The 'S/T' Interface

CCITT specification I.430 defines the physical layer of this interface for ISDN Basic Access. The 'S' interface is a full-duplex interface which passes the 2 'B' channels and the 'D' channel between the Network Termination (NT-1 or NT-2) and the customer's terminals, together with some additional bits used for synchronization, contention control in the 'D' channel, and other housekeeping functions. A transceiver is required for transmission at the 192 kb/s bit rate, over separate transmit and receive twisted pairs (2 pairs already exist in both office and residential telephone wiring within the premises in many countries). Alternate Mark Inversion coding, with the binary data inverted, is used.

2 additional twisted pairs are specified as an option, 1 for power and 1 for spare, making this an 8 wire interface if fully equipped. A plug and jack have been standardized so that the 'S' interface can be a "universal portability point" for ISDN terminals from any manufacturer in the world, see *Figure 1.*

An interesting feature of the 'S' interface is that it includes one of the elements of Local Area Networking: multiple access with contention resolution to enable up to 8 terminals to use the interface, even though there are only 2 'B' channels and 1 'D' channel. Collisions are allowed and resolved only in the 'D' channel, however, and a TE cannot use a B channel until it has first requested and been allocated one, using Layer 3 call control procedures via the D channel.

AN ADVANCED ISDN CHIP SET

In developing the architecture of this ISDN chip set, a major objective has been to create a flexible set of building blocks which provide elegant and cost-effective solutions for a wide range of applications. With just these few highly integrated devices a broad spectrum of ISDN equipment can be designed, ranging from Control Office and PBX line cards to X.25 and ISDN Terminals and telephones, PC and Terminals Adapters, packet-mode statistical multiplexers, NT-1's, and other ISDN equipment.

A key factor here is that device functions in the chip set are specifically aligned with the first 3 layers of the OSI 7 layer Protocol Reference Model. Thus this chip set has a distinct partitioning of functions into several transceivers which provide the bit-level transport for Layer 1, the Physical Layer, while the functions of Layer 2, the Data Link Layer, and Layer 3, the Network Layer, are supported entirely by a single microprocessor. All devices in the chip set, together with other standard components such as PCM Codec/filter Combos, can be interconnected via a common serial interface without the need for any "glue" components. The re-

'S' INTERFACE: THE UNIVERSAL "PORTABILITY" POINT

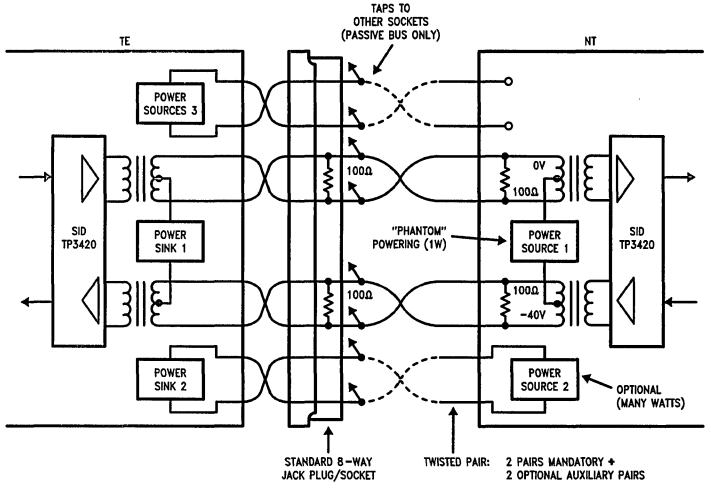


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FIGURE 1. The S Interface

sult is a very elegant architecture offering many advantages including the following:

1. a high degree of modularity with minimal component count;
2. the same transceiver can be used at either end of a loop;
3. simplified software for packet management;
4. minimization of CPU interrupts;
5. tight coupling between Layers 2 and 3;
6. simplified exchange of primitives between Layers.

The Chip Set: Layer 1

For Layer 1, 2 CMOS transceivers have been developed to cover a wide variety of twisted-pair applications for Basic Access. Each transceiver is capable of transmitting and receiving 2 "B" channels plus 1 "D" channel, and has mode selections to enable it to work at either end of the loop. As shown in *Figure 2*, these devices are:

1. The TP3420 'S' Interface Device (SID), a 4-wire transceiver which includes all the Layer 1 functions specified in CCITT Recommendation I.430. This specifications covers the interface between the Terminal Equipment (TE) and the Network Termination (NT) on the customer's premises. In addition the TP3420 includes adaptive equalization and filtering, as well as a high resolution digital phase-locked loop in the receive side to provide transmission performance far superior to the minimum requirements of I.430. All Activation and 'D' channel access algorithms are handled automatically without the need to invoke any action from a microprocessor.
2. The second transceiver is the TP3401 Digital Adapter for Subscriber Loops (DASL), which is a low-cost burst-mode transceiver for 2-wire PBX and private network loops up to 6 kft in range. Scrambled Alternate Mark Inversion coding is used, together with adaptive equalization and timing-recovery, to ensure low bit error rates on a wide variety of cable types. All activation and loop timing control circuitry is also included. While this transmission scheme has not been standardized, it offers a practical solution for wiring installations where only a single pair is available, at lower cost than the 'S' Interface.

Note: Another transceiver has now been developed, the TP3410 2B1Q Echo-canceller for the U Interface. A TE/TA for direct connection to the U Interface maybe designed using this device, see the TP3410 datasheet.

TP3420 S INTERFACE TRANSCEIVER

This CMOS device, shown in *Figure 3,* has been designed to meet the latest version of the U.S. Draft Standard for the S/T interface, including the late addition of the 800 b/s bidirectional multiframing channel for Layer 1 maintenance messages. It also includes the Activation state machines to enable the same device to be used at either the NT or TE end of the loop, simply by mode selection during device initialization. For applications in which the TE is powered remotely from the NT or line card , requiring a low power deactivated state, the device can be totally powered down, with the exception of a line signal detect circuit, so that power-up and Activation can be initiated by either end of the loop.

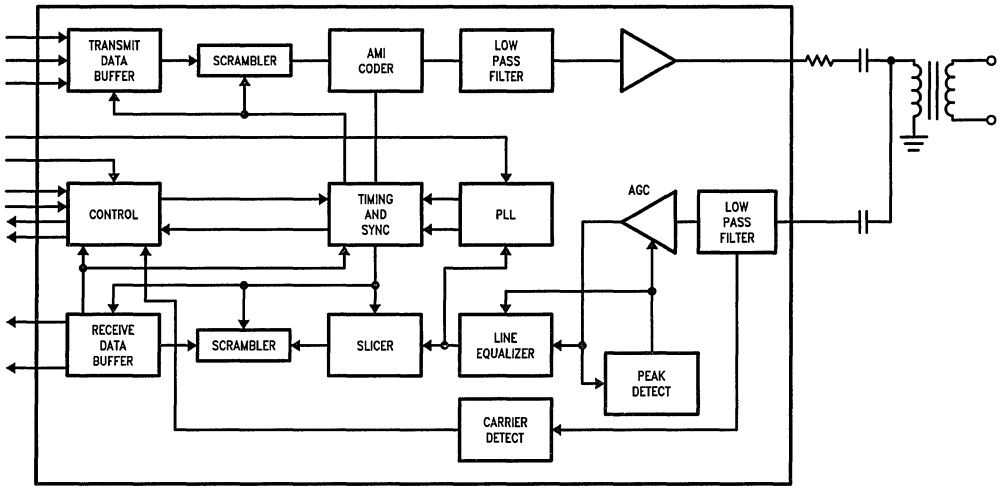

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FIGURE 2. TP3401 Transceiver

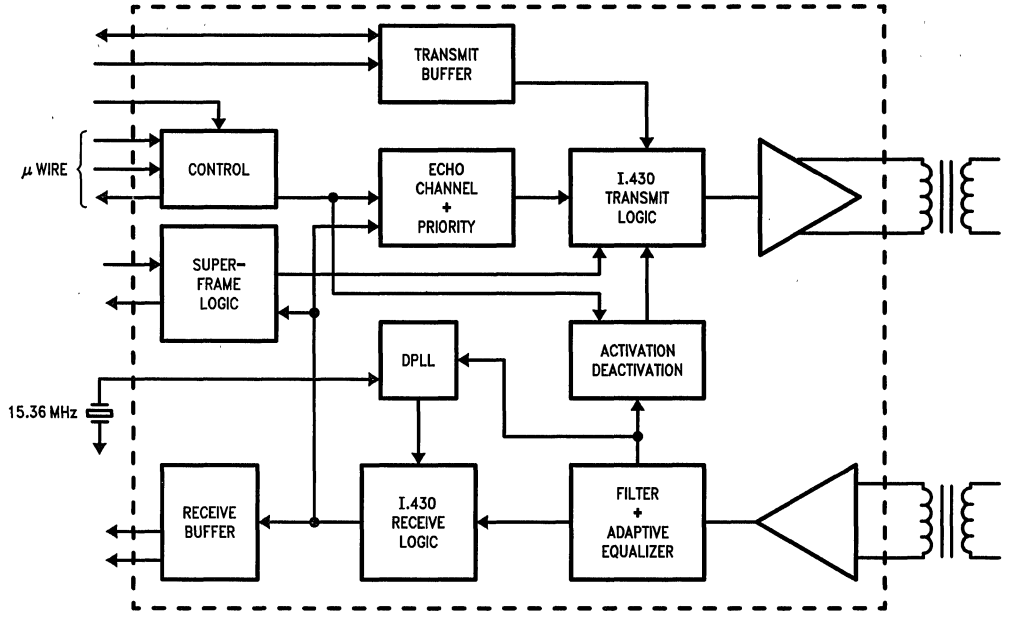


FIGURE 3. TP3420 SID

Various twisted pair wiring schemes are outlined in I.430, although in practice it is highly desirable that the transceiver should be able to work well on any existing premises wiring without special 'grooming'. Unfortunately, the transmission performance tests called up in I.430 are not as stressful on the transceiver design as are those in the recently completed 'U' Interface specification. The problem is exacerbated by the fast rise and fall times specified for the rectangular transmitted pulses, the spectrum of which includes high energy levels at frequencies in excess of 500 kHz. Bearing in mind that the cable is usually low-cost unshielded twisted pair, there is a distinct possibility that, in the presence of noise, crosstalk and jitter on the S interface, the customer will find that the better than 1 in 10E−7 BER provided on the U interface is not preserved through to the TE.

To prevent this it is important that the receiver section of the S transceiver should be designed with some additional noise margin. Certainly the TP3420, by virtue of its receiver filtering and equalization, can function with very low BER over many wiring schemes which exceed those specified, even when the received 'eye' is virtually closed by noise and jitter. Furthermore, since jitter at the digital interface in an NT can be considerably worse than that specified, for example when the U interface has been derived from a carrier system which passes its own jitter on, resynchronizers are used in the data buffers on the TP3420 to accommodate a high degree of jitter and low-frequency wander without 'slip'.

NT-2 Synchronization with the TP3420

Another feature of the device is particularly useful when designing an NT-2. The NT-2, typically a PBX, has a number of S Interfaces on the customers' side and, if it uses Basic Access to the network, each trunk is a T Interface to an NT-1 (in the classical reference model). Linking the two is the time-slot interchanging switch matrix. *Figure 4* shows the arrangement.

Functionally the S and T interfaces are identical, i.e. both conform to I.430. Thus, the TP3420 can operate on the S Interface side of the switch, with NT Mode selected (either fixed or adaptive receive sampling as appropriate for the wiring), while on the T Interface side the TP3420 operates like a terminal, in TE Mode. However, the complete NT-2 must have all its clocking and data interfaces synchronized to the network. This requires a system clock at, typically, 2.048 MHz, to be phase-locked to one of the T interfaces.

Normally, therefore, the construction of a discrete PLL to generate this frequency-locked clock is necessary; however the TP3420 includes this PLL, with a CLK output, when it is programmed to be in the TE Mode but the Slave of the digital system interface. Thus, any one of the TP3420's can be chosen as the source of this clock, and all will take their BCLK and FS timing from the same one, i.e. they are slaved to the network clock and synchronized to each other. In this way, the complete NT-2 is synchronized to any one of the activated T interfaces, and the clocking is synchronized all the way from the terminal to the network.

THE CHIP SET: LAYER 2 AND LAYER 3

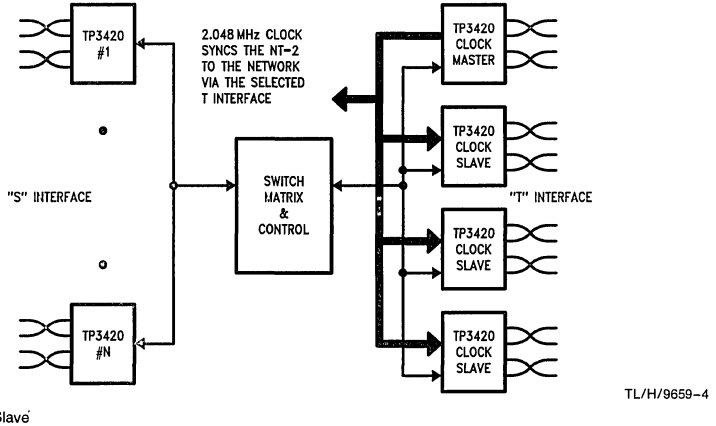
Complementing the Layer 1 transceivers, a highly integrated communications controller has been developed for implementing both Layer 2 (Data Link Layer) and Layer 3 (Network Layer) of various protocols, including X.25 LAPB and LAPD (Q.921 and Q.931), together with the capability of several Terminal Adapation schemes. A single device can run all the processing for these functions: the HPC16400. One of National's growing family of 16-bit single chip CMOS microcontrollers, the HPC16400 is based on a high-speed (20 MHz) 16-bit CPU 'core', which achieves instruction cycle times as low as 200 ns. To this core has been added 2 full HDLC formatters supported by DMA to external memory, and a UART, see *Figure 5.*

The set of features included on the HPC16400 makes it an ideal processor for running all the Layer 2 and 3 functions of an ISDN Terminal Adapter, TE or telephone, or the communications port of an X.25 or multi-protocol terminal. Because of the large ROM and RAM requirements for Layer 3 and the Control Field elements of procedure of Layer 2 in LAPB and LAPD protocols, the HPC16400 is configured as a ROMless processor. 256 bytes of RAM are provided on the core for storage of user variables; packet storage RAM and all user ROM is off-chip, this being by far the most cost-effective and flexible combination. A multiplexed bus to external memory provides direct addressing for up to 64 kbytes of memory, with additional control outputs available for expanded addressing for up to 544 kbytes of memory. Interrupts are managed by a vectored interrupt handler, which includes arbitration logic to process up to 8 pending interrupts, from both internal and external sources.

The HDLC controllers on the HPC16400 allow continuous HDLC data rates up to 4.6 Mb/s to be used, making it ideal for Primary Access and proprietary higher speed networks as well as Basic Access channels. Minor differences in the framing between these HDLC-based protocols, such as the need for different interframe-fill characters for Basic and Primary rate, and options on the CRC algorithm, can be selected during initialization. In addition to handling all Layer 2 framing, the HDLC circuitry includes automatic multiple address recognition on incoming Layer 2 frames, to support, for example, multiple TEI's in LAPD.

As an aid in implementing multiple protocols within the one design, a 'Bypass' mode is included for each HDLC channel, whereby the HDLC framing circuits are bypassed. Thus a straightforward USRT interface is then established, enabling non-HDLC protocols to be run in software. This mode may be selected and deselected at will, so that data transfer sessions between different types of terminal can be handled on a per-call basis. To enable the speed capabilities of the HDLC channels to be fully exploited, they interface to external data buffer RAM via a Direct Memory Access controller on the device. A bus request is issued by the DMA controller to the CPU when one or more of the individual HDLC channels request service. Upon receiving a bus acknowledge from the CPU, the DMA completes all requests pending,

NT-2 Synchronization



TP3420 Can Be Clock Master or Slave

FIGURE 4. NT-2

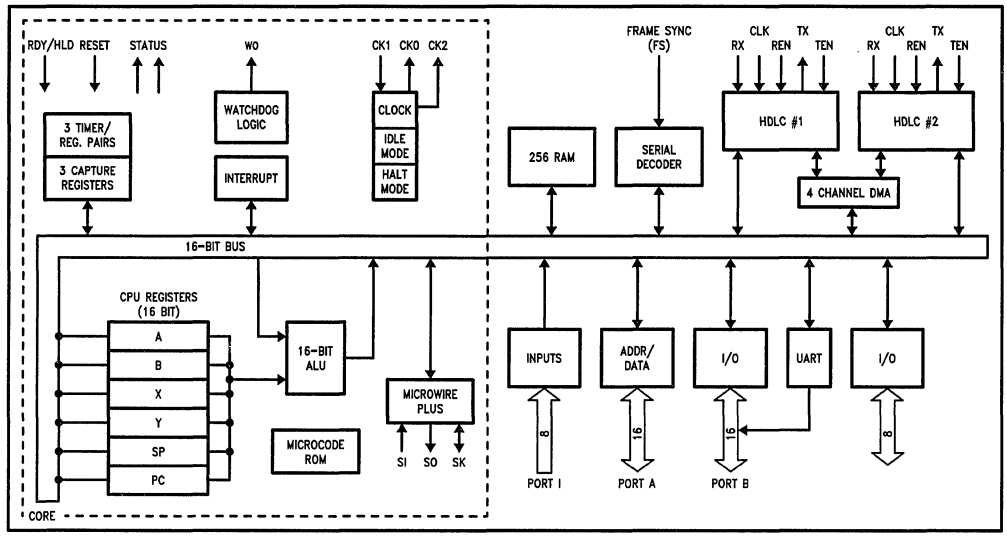


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FIGURE 5. HPC 16400 Block Diagram

and any that may occur during this operation, before relinquishing the bus back to the CPU. All this takes place merely by stealing bus cycles away from the CPU, there is no need for "pushing" and "popping" the stack as is the case where the Layer 1 transceiver includes FIFOs for data buffering, which demand service by means of interrupts.

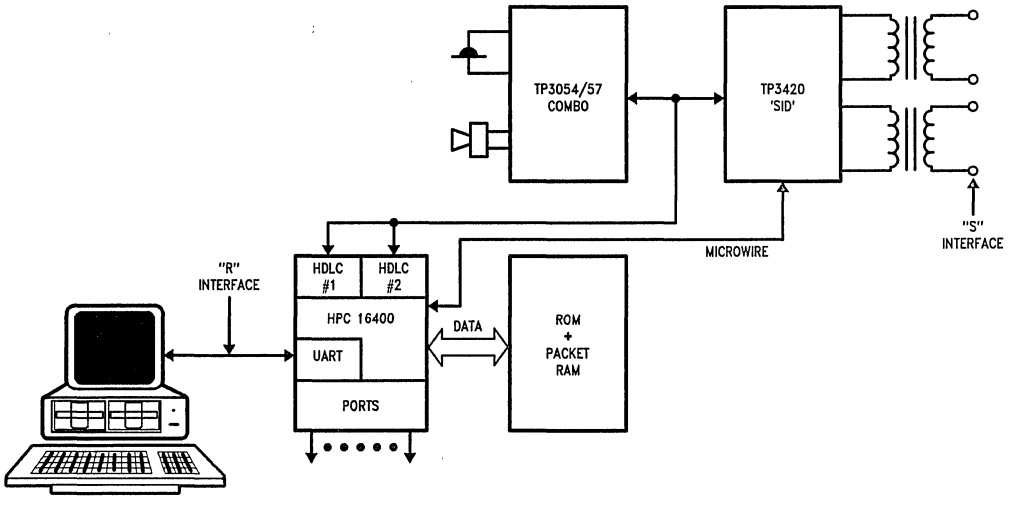
Furthermore, several register sets are included to simplify packet RAM management, again with minimal CPU intervention. These registers facilitate "chaining" of successive packets, in which the memory pointers for the following packet can be set up during transfer of the current packet so that there is no latency period between packets during high-speed transmission. Additionally, if required, the header and Information fields of Layer 2 frames can be segmented into different areas of memory to help structure the packet RAM economically. This integrated design achieves a high throughput of packet data without the need for costly FIFO's and external interrupts, thereby minimizing the impact of packet handling on CPU time.

TYPICAL TE/TA APPLICATIONS

Figure 6 shows a typical application of the chip set in a Basic Access TE which offers one voice channel and an RS232 interface to support an external terminal. Other combinations, such as 2 voice channels or 2 data channels are easily implemented by adding a second Combo or an external HDLC controller, and a few gates are all that is necessary to multiplex between them. The TP3420 'S' Interface Device ensures that the system is compatible with any 'S' or 'T' standard jack socket and provides the multiplexing signals for the other devices operating in the 'B' and 'D' channels; all timing for the TE is derived by the TP3420 from the received line signal.

In the application shown, LAPD signalling in the 'D' channel is provided via HDLC #1 on the HPC16400. The UART would serve as an RS232 interface and, by using a 15.36 MHz crystal, which can be shared between the HPC and the SID, all the standard asynchronous baud rates up to 19,200 (and beyond) can be generated. Terminal adapation of the data and the terminal handshaking signals is performed by the HPC16400 via the UART and HDLC controller #2, which can be assigned to either of the 'B' channels.

For voice calls, the TP3054/7 Codec/filter Combos are quite suitable, since the analog ports are readily interfaced to an electret microphone and a moving-coil earpiece, with a sidetone leak path added. B and D channel data passes between the devices multiplexed together, clocked by the BCLK output from the SID, and synchronized by the 8 kHz frame sync, FS, from SID. A serial interface decoder allows either or both HDLC controllers to be directly interfaced and synchronized to either of the Layer 1 transceivers or to a variety of backplanes, line-card controllers and other devices using time-division multiplexed serial interfaces. Both the SID and the HPC16400 include several selectable formats for this multiplexing, to simplify the interface to other vendors' Codecs. Format 1 on the SID is the correct one for the TP3054 Combo, while on the HPC Serial Decoder, Format 4 is the correct choice for this combination of devices. Although the simplified interface timing on the TP3054/7 means that it will always need to use the B1 channel to and from the SID, the SID has a control function which allows it to to exchange data between the B1 and B2 channels as it passes through it. Thus, if the network assigns channel B2 to a voice call, SID does the exchange from the Combo in



TL/H/9659–6

FIGURE 6. Typical Terminal Application

the B1 channel on the Digital System Interface to the B2 channel on the S Interface. Because of the way the Serial Decoder on the HPC is designed, its HDLC channel #1 will normally be selected for the D channel, while either HDLC controller can be used for data in either B channel.

In applications where the TE must go into a low-power mode when there are no calls in progress, the HPC is put into the HALT mode, with all other devices powered-down. The correct way to restart the HPC to initiate a call is to pull the Non-maskable Interrupt high. Since this may be invoked by an off-hook signal in the TE, or by the SID's Line Signal Detector detecting a wake-up signal (INFO 2 on the S interface) and pulling low, these 2 signals are simply NOR'd together to pull NMI high. The LSD output has been designed to prevent multiple pulses from repeatedly causing interrupts; mechanical hookswitches, however, may bounce, requiring a simple R-C debouncing filter to be inserted.

In many applications a number of other peripheral functions must also be provided, such as sensing switches or scanning a small keyboard, interfacing to a display controller etc. A number of extra I/O pins and a MICROWIRE/PLUS™ serial data expansion interface are available on the HPC 16400 to service these functions. In addition, 4 user configurable 16 bit timer-counters simplify the many time-outs required to manage such a system, including the default timers specified in the various protocol specifications. A "Watchdog" timer can also be enabled, to provide a means for recovery from erroneous software states.

D-Channel Flow Control

D-Channel Flow Control refers to the way the HPC transfers a Layer 2 frame (or packet) to the SID transmit buffer, and from there onto the S Interface in a Terminal. When the Layer 2 entity wants to transmit a packet, it does not know if another TE is already occupying the D Channel, since all the D Channel monitoring and contention resolution is done at Layer 1 by the SID. To transmit its packet, therefore, the HPC primes its HDLC #1 transmit buffer, ready to send byte 1, then sends a DREQ (D-channel Request) over MICROWIRE™ to the SID. DREQ messages must also indicate if the pending packet is high priority, for signalling, or low priority, for all other types of data. The TP3420 SID then uses a special clock control output to fetch data from the HPC, multiplexed on the digital system interface. Concurrently, it tests to see if the D Channel towards the NT is in use by another TE, by checking the number of consecutive 1s counted in the D-echo channel from the NT. When the access algorithm allows, SID starts transmitting D-channel bits from its buffer, beginning with the opening flag, and clocks further D channel bits from the HPC's HDLC #1 to the SID, always 2 bits per 8 kHz frame. As the HPC empties its transmit buffer, a DMA cycle is prompted to replenish it. Thus, D-channel data now flows from the HPC through SID and onto the S interface without interrupts until either:

i) the TP3420 SID detects that it has lost a collision with another TE, so it stops fetching data from the HPC, transmits 1s in the following D-bit positions on the S interface, and INTerrupts the HPC with a CONtention message;

or:

ii) the SID detects the closing flag passing through onto the S interface, forces 1's into the D-channel after the closing flag, stops fetching data, and sends an EOM (End of Message) INTerrupt to the HPC.

Note that the HPC cannot follow immediately with another packet because the successful TE must now decrement its priority and check that no other TE starts using the D-channel. Thus TEs waiting to send signalling packets all succeed in order first, and data packets are only sent when no TE has a signalling packet pending.

TERMINAL ADAPTION

One of the hurdles facing the widespread deployment of ISDN is the confusion over terminal adaption techniques. While the X.31 standard has been adopted for connection of X.25 terminals to Packet switches via the ISDN, the situation for the majority of terminals which will require circuit-switched access is far less certain. Currently, there is only one standard, V.110, which is CCITT approved for these applications, although certain recent additions for the support of asynchronous terminals have yet to be ratified. There are, however, several other contenders, most notably a recent spec, colorfully known a V.tad, which is a simpler technique than V.110, and offers the major advantage that

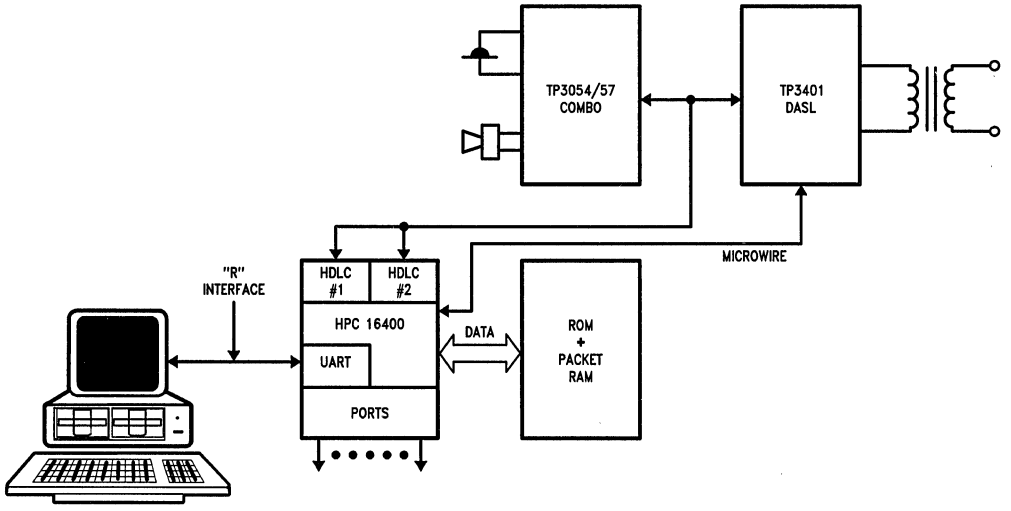
data is rate adapted into HDLC frames using Q.921 procedures. V.tad, proposed by the U.S., is currently under the scrutiny of CCITT. Then there are several proprietary schemes in existence, notably AT&T's DMI mode 2 and Northern Telecom's T-Link, which are already deployed in the network, yet will not be standardized at the national or international level. Thus there is considerable interest in terminal adapters which can support multiple protocols, a task for which the HPC16400 is ideally suited.

To build a terminal adapter around the HPC, an area of external RAM is first set up as the data buffers for the 2 directions. Different software modules are then called up to assemble and disassemble the frames to and from the network, using the appropriate method of rate adapting the data. HDLC channel #2 provides access to either of the B channels in the SID Layer 1 transceiver. For a data call using V.110 or other non-HDLC based protocols, the bypass mode is selected for the HDLC framing circuits, while for a V.tad call the HDLC circuits are switched in, this being selectable on a call-by-call basis if desired. On the terminal side, for a V.24/RS232C async terminal interface, the onboard UART provides the start/stop bit manipulation and terminal clocking functions between the terminal and the data buffers. For a TA plug-in card for a PC, an INS8250 or 16450 UART can be added to interface to the backplane if it is required to maintain compatibility with existing DOS I/O drivers. Either way, it takes the power of an HPC16400, with its high speed processing, efficient compiling of high-level languages and expandable address space, to implement these multiple, complex, real-time tasks.

Note: V.tad is now numbered as V.120 in the CCITT Blue Book.

PBX 2-Wire Terminals

Thus far, the terminal designs discussed have been based on compatibility with the S Interface Layer 1 specification. *Figure 7* shows how simple it is to convert an 'S' Interface terminal, which of course requires 2 twisted pairs, to a terminal using only a single pair by replacing the TP3420 SID by a TP3401 DASL. The clean partitioning of device functions makes this possible with practically no other changes to the design.



TL/H/9659–7

FIGURE 7. 2-Wire Terminal Application

Basic Access Line Cards

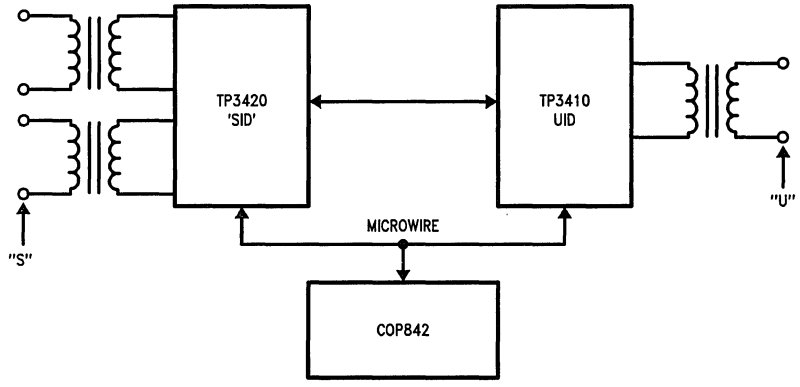
For operation on a line card in a PABX or NT-2, such as that shown in *Figure 7*, both of the transceiver devices can be set to operate as the timing master for the loop, being synchronized to the system clock and controlling all loop frame timing. If programmable time-slot assignment is required, the TP3155 TSAC provides 8 individually programmable frame sync pulse outputs locked to a common frame marker. 'B' channels can be interfaced to standard backplane interfaces, while 'D' channels can be either multiplexed on and off the card for processing or can undergo Layer 2 processing on the card itself.

Building an NT-1

An NT-1 Network Termination is defined as a Layer 1 device only, which converts the 2-wire public network 'U' interface to the limited distance 4-wire 'S' interface on the customer's premises. It has no capability for intercepting higher layers of the 'D' channel protocol. As such, it is built simply by connecting a TP3420 SID, configured in NT mode, to a U Interface transceiver operating in Slave mode. Layer 1 maintenance protocols across both the 'U' and 'S/T' interfaces, which are as yet still in a state of flux for most administrations, may be handled by a low-cost COPs Microcontroller via its serial MICROWIRE interface. *Figure 8* shows the arrangement.

SUMMARY

Designing ISDN equipment is not going to be a cakewalk for this first generation. There are numerous new standard specifications to become familiar with, and many protocol and real-time processing problems to be overcome. The chip set described here provides designers with the confidence of knowing that the hardware is fully compliant with the latest standards, and that the necessary processing power is available in the HPC to satisfy a wide range of designs without the need to re-learn a different set of components for every new product.



TL/H/9659–8

FIGURE 8. NT-1 Application

COMBO II™ Programmable PCM CODEC/Filter Family Application Guide

National Semiconductor
Application Note 614
Gary Rothrock

TABLE OF CONTENTS

INTRODUCTION
DIFFERENCES AMONG DEVICES IN THE FAMILY
ABSOLUTE vs. RELATIVE SIGNAL LEVELS
TRANSMIT GAIN/RECEIVE ATTENUATION CODE BIT VALUES
NOISE PERFORMANCE AT HIGH TRANSMIT GAINS
MINIMUM RECEIVE ATTENUATION vs. OUTPUT LOADING
RECEIVE OUTPUT COUPLING—AC vs. DC
TRANSMIT INPUT COUPLING—AC vs. DC
VARIATION OF TRANSMIT INPUT RESISTANCE WITH SIGNAL LEVEL
TRANSMIT TO RECEIVE INTRACHANNEL CROSSTALK
PRINCIPLES OF QUIET LINE CARD DESIGN
LATCH-UP PREVENTION TECHNIQUES
ASYNCHRONOUS OPERATION
RESERVED CONTROL INTERFACE REGISTER ADDRESSES
TROUBLESHOOTING GUIDE
REFERENCES
APPENDIX I. COMBO II 0dBm0 LEVELS vs. GAIN CODES

INTRODUCTION

CODEC/Filter COMBO™ devices are designed for use in telecommunication systems such as digital Central Office switches, PABXs, PCM transmission equipment and digital telephone sets. The TP3070 series COMBO II devices are second generation combined PCM CODEC and Filter devices having a number of functions which are programmable via a serial control port. Please refer to the TP3070/TP3071 and TP3075/TP3076 data sheets for a detailed description of the device functions and specifications. This application note will expand on those areas needing additional emphasis and treat a number of other areas as well.

DIFFERENCES AMONG DEVICES IN THE FAMILY

The COMBO II device family consists of four devices at the present time—TP3070, TP3071, TP3075 and TP3076. It is expected that new derivative members will join the family as warranted by the marketplace. The TP3070 is the basic device type and exhibits the full feature set. This device is mounted in a 28-pin package. The TP3071 utilizes the same die and is mounted in a 20-pin package, sacrificing several features due to pin limitations. The TP3070 is suitable for almost any CODEC/Filter application where programmable features are needed. The TP3071 is recommended in applications where some of these features are not needed and can be traded off for a smaller package size.

The TP3075 and TP3076 devices have the hybrid balance function deleted. These devices are targeted for ISDN and digital phone applications where the COMBO is in the phone and the connection is 4-wire all the way to the handset. This completely eliminates the need for the hybrid balance function and allows a reduction in the cost of the device. Another application for these devices is in 4-wire trunks, where again the hybrid balance function is not needed. The TP3075 has a 28-pin package and the full complement of COMBO II features, except for the hybrid balance function. The TP3076 is mounted in a 20-pin package and has a reduced feature set suitable for low cost digital phone applications.

The TP3070 and TP3075 have dual PCM ports which allow on-chip access to system redundant PCM bus structures. This provides increased reliability in the event one bus goes down, allowing traffic to be switched to the other bus and preventing any lines from being out of service. Redundant bussing also provides twice the traffic capacity of a single bus system. In the event of failure of one bus, only half the traffic capacity is lost. With BCLK rates of 4.096 MHz, 64 timeslots are available on each bus, for a total of 128 timeslots accessible directly by the device.

The TP3071 and TP3076 have only a single PCM port (Port 0 for the TP3071 and Port 1 for the TP3076) rather than the dual ports of the TP3070 and TP3075, eliminating the on-chip access to redundant PCM bus structures. At the same time, the number of accessible timeslots is also halved relative to the number available in a system with redundant PCM busses. With the single PCM port and BCLK rates of 4.096 MHz, a maximum of 64 timeslots are available.

The TP3070 and TP3075 have six interface latches available while the TP3071 is limited to five and the TP3076 has four. The control interface for the TP3070, TP3075 and TP3076 consists of four pins; chip select ($\overline{CS}$), control clock (CCLK), control data input (CI), and control data output (CO). The TP3071 has the control input and control output pins combined into a single control input/output (CI/O) pin.

Separate bit clock (BCLK) and master clock (MCLK) pins are provided for the TP3070, TP3075 and TP3076. Allowable bit clock rates are 64 kHz to 4.096 MHz, in 8 kHz increments, as long as BCLK is synchronous with MCLK. Allowable MCLK rates are 512 kHz, 1.536, 1.544, 2.048 and 4.096 MHz. The TP3071 device has a single pin which serves both BCLK and MCLK functions. Because of this, BCLK rates for the TP3071 are restricted to the MCLK rates only.

The TP3076 has no Master Reset (MR) pin for resetting the internal registers. All devices reset internal registers to a benign state when power is applied to the device pins and can also be programmed to the same conditions via the serial control interface.

The transmit gain of the TP3075 and TP3076 is 1.4 dB higher than the TP3070 and TP3071. With the transmit programmable gain set for 0 dB, the TP3070 and TP3071 levels at VF_XI corresponding to 0 dBm0 are +6.4 dBm (600Ω). For the TP3075 and TP3076, the 0 dBm0 levels at VF_XI are +5.0 dBm (600Ω).

ABSOLUTE vs. RELATIVE SIGNAL LEVELS

In the COMBO II specifications, many signal and noise levels are specified as relative levels (dBm0, dBm0p, dBrnc0) rather than absolute levels (dBm, dBmp, dBrn). When doing

measurements of device performance, it is necessary to convert the absolute level readings to relative levels for comparison to specifications. The conversion factor needed will depend on the transmit gain and receive attenuation programmed into the device.

Most meters which have a dBm readout assume a 600Ω impedance, although they only measure voltage. A reading of 0.775 Vrms will be displayed as 0 dBm, no matter what the actual circuit impedance or power level. PCM levels are specified relative to the overload level (CODEC full scale). The 0 dBm0 test tone level is defined to be 3.17 dB below the overload level for μ-Law systems and 3.14 dB below the overload level for A-Law systems.

For the TP3070 and TP3071, with the transmit gain programmed to 0 dB (11111111), the overload level at VF_XI is 2.33 Vrms for μ-Law and 2.32 Vrms for A-Law. With the receive attenuation programmed for 0 dB (11111111), the overload level at VF_RO is 2.83 Vrms for μ-Law and 2.82 Vrms for A-Law. The 0 dBm0 test tone level will be 3.17 or 3.14 dB below the overload levels, or 1.619 Vrms (transmit) and 1.964 Vrms (receive). A meter calibrated in 600Ω will read these levels as +6.4 dBm (transmit) and +8.1 dBm (receive). To convert to relative dBm0, dBm0p, or dBrnc0 levels, 6.4 dB must be subtracted from the meter reading for transmit levels, and 8.1 dB must be subtracted for receive levels. At any other programmed transmit gain or receive attenuation, the conversion factors will be different. In general, the transmit conversion factor to be subtracted from the meter reading is:

+6.4 dB − programmed gain (dB)

The receive conversion factor to be subtracted is:

+8.1 dB − programmed attenuation (dB)

For the TP3075 and TP3076, the transmit conversion factor to be subtracted from meter readings is:

+5.0 dB − programmed gain (dB)

The receive conversion factor for the TP3075 and TP3076 is the same as that of the TP3070 and TP3071. See Appendix I. for a complete listing of binary gain codes for all 255 transmit and receive gains and corresponding 0dBm0 levels in dBm and Vrms at VF_XI and VF_RO. Note that the circuit points under discussion here are at the device VF_XI and VF_RO pins. When doing in-system tests, levels on the telephone line tip and ring conductors will probably differ because of circuit gains and/or losses between the device pins and the telephone line. Additional conversion factors will be necessary to account for these gains and losses.

TRANSMIT GAIN/RECEIVE ATTENUATION CODE BIT VALUES

The data sheet gives equations to calculate the binary codes required for given VF_XI input and VF_RO output rms voltages at 0 dBm0. Table I is convenient for converting the programmed gain value in dB to the binary code and vice versa. For dB to binary conversion, use the following algorithm:

1. To determine Bits 7 and 6, select the largest dB value in the left table which is less than or equal to the gain value to be converted.
2. Subtract the selected dB value from the gain value to be converted.
3. To determine bits 5 and 4, select the largest dB value in the center table which is less than or equal to the remainder.
4. Subtract this selected dB value from the remainder.
5. To determine bits 3, 2, 1 and 0, look up this remainder in the rightmost table.

See Note 1. in the table for binary to dB conversion.

NOISE PERFORMANCE AT HIGH TRANSMIT GAINS

In general, the use of high values of transmit gain is not recommended unless system noise requirements are not stringent. The Transmit (idle channel) Noise and Transmit Signal to Total Distortion are both specified with transmit gain set to 0 dB. Although the transmit amplifiers are designed for low noise, there will still be some degradation in noise performance for these parameters at high transmit gains. The degradation in S/D and idle noise for the TP3070 and TP3071 is about 3 dB at low signal levels and 25.4 dB gain, while the TP3075 and TP3076 are about 1.5 dB better due to the elimination of the input summing amplifier, as shown in *Figures 1* and *2*.

TABLE I. Transmit Gain and Receive Attenuation Code Bit Values

Bit Number 7	Bit Number 6	Gain dB
0	0	19.2
0	1	12.8
1	0	6.4
1	1	0.0

Bit Number 5	Bit Number 4	Gain dB
0	0	4.8
0	1	3.2
1	0	1.6
1	1	0.0

Bit Number 3	Bit Number 2	Bit Number 1	Bit Number 0	Gain dB
0	0	0	0	1.5
0	0	0	1	1.4
0	0	1	0	1.3
0	0	1	1	1.2
0	1	0	0	1.1
0	1	0	1	1.0
0	1	1	0	0.9
0	1	1	1	0.8
1	0	0	0	0.7
1	0	0	1	0.6
1	0	1	0	0.5
1	0	1	1	0.4
1	1	0	0	0.3
1	1	0	1	0.2
1	1	1	0	0.1
1	1	1	1	0.0

Note 1: Add the three dB values for transmit gain or receive attenuation. Bit 7 = MSB.

Note 2: All zero code specifies no output.

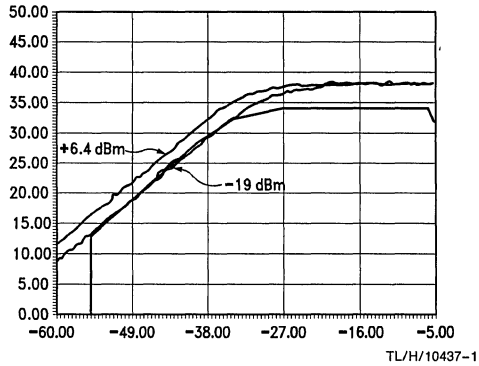


FIGURE 1. TP3070 and TP3071 S/D at 0 dB and 25.4 dB gain (Noise Method)

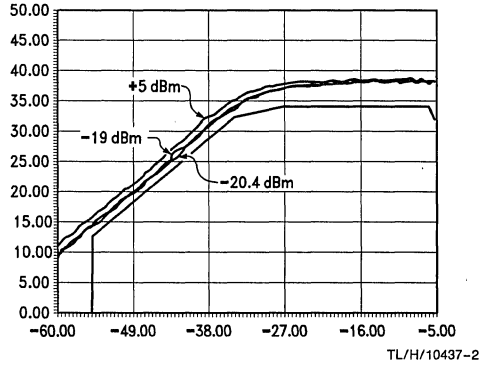


FIGURE 2. TP3075 and TP3076 S/D at 0 dB, 24.0 dB and 25.4 dB gain (Noise Method)

MINIMUM RECEIVE ATTENUATION vs. OUTPUT LOADING

When programmed for 0 dB receive attenuation, the nominal receive 0 dBm0 level at VF_RO will be 1.964 Vrms. This is equivalent to a +3.17 dBm0 overload level of 2.83 Vrms for μ-Law, or 4 Vpk; slightly less for A-Law. The receive output can drive to ±4 Vpk with load impedances of ≥15 kΩ. When driving heavier loads, the output swing capability is reduced. To prevent distortion on signal peaks, some attenuation should be programmed in. For a load impedance at VF_RO of ≥600Ω, the maximum output is ±3.8 Vpk. To account for this, a minimum attenuation of at least 0.5 dB [= 20 log (3.8/4.0) rounded up to the next higher tenth of a dB] should be programmed in. For load impedances of ≥300Ω, the maximum output level is ±3.5 Vpk, and a minimum attenuation of 1.2 dB should be programmed in.

The maximum output power obtainable with 300Ω and 600Ω loads, assuming the minimum programmed attenuations, is more than sufficient for most 2-wire applications. With 0.5 dB of programmed attenuation and 600Ω load, the +3.17 dBm0 output level will be 2.67 Vrms. Maximum power delivered from the amplifier will be 11.9 mW = +10.75 dBm. With 1.2 dB of programmed attenuation and 300Ω load, the +3.17 dBm0 output level will be 2.46 Vrms. Maximum power delivered from the amplifier will be 20.2 mW = +13.06 dBm.

The 2-wire line interface is usually at 0TLP (transmission level point) or less on the receive side of a digital switch. Assuming 0TLP, the 0 dBm0 level will be 0 dBm, and the overload level will be +3.17 dBm. Allowing 1 dB for transformer loss and 3 dB for loss in the matching resistor typically used in series with the amplifier output, the maximum power the amplifier needs to supply is +7.17 dBm. With 600Ω load there will be over 3.5 dB of margin and with 300Ω load there will be about 5.9 dB of margin.

RECEIVE OUTPUT COUPLING—AC vs. DC

When driving a transformer load, AC coupling may or may not be necessary. Required capacitance values can be large because of the low impedances, transformer roll-off due to magnetizing inductance, and tight specs on frequency response and return loss at low frequencies. It is therefore desirable to use DC coupling if possible. This can be done if the DC current flow from the VF_RO output is kept low.

The output offset voltage at VF_RO is specified at ±200 mV, maximum. In a typical circuit configuration, VF_RO is connected through a matching resistor to the transformer winding, the other end of which is connected to ground. DC current will flow through the matching resistor and transformer winding as a result of this voltage offset from ground. The VF_RO output can supply 3.5V peak with a 300Ω load, or 11.6 mA peak. The sum of DC current and peak AC signal current should not exceed this to prevent distortion of the full load signal peaks.

Example: If we assume we need +3 dBm delivered to the line at + 3 dBm0, and transformer and matching resistor losses total 4 dB, the amplifier will need to supply +7 dBm = 5 mW. Assuming the reflected transformer impedance and matching resistor total 600Ω, the amplifer output voltage will be $E = \sqrt{PR} = 1.732$ Vrms = 2.45 Vpk. Peak signal current will be $I = E/R = 2.45/0.6 = 4.1$ mA. DC current flow should then be less than 11.6 − 4.1 = 7.5 mA. If the matching resistor and transformer winding resistance total 300Ω, the actual DC current flow will be no more than $I = 0.2V/0.3k = 0.67$ mA and no capacitor is required in this case. Note that for high levels of output signal, lower values of resistance to ground, and/or lower impedance levels, a large value capacitor may be required.

The effect of the DC current flow on the transformer also needs to be considered. If an iron core transformer is being used which can handle the DC loop current, the few mA flowing due to offset will probably be of little or no consequence. Small ferrite transformers not designed to handle a DC flux should be evaluated to determine the effect on inductance and signal distortion of the expected worst case DC current flow. Even currents below 1 mA can impact performance of some ferrite transformers. If transformer performance is inadequate because of the DC flux, a capacitor will be needed.

TRANSMIT INPUT COUPLING—AC vs. DC

AC coupling to the transmit input (VF_XI) may or may not be necessary. The device has sufficient headroom to handle up to 200 mV of DC offset applied at the VF_XI input when the transmit gain is programmed for 0 dB, and up to about 10 mV when programmed for 25.4 dB gain. The product of applied input offset voltage and programmed transmit gain should not exceed 200 mV. If it does, distortion and noise performance may be degraded for high level signals near +3 dBm0.

In applications where this 200 mV product may be exceeded, capacitive coupling should be used to eliminate the DC offset. No ground reference is required at VF_XI. The minimum input resistance spec at VF_XI is 390 kΩ, and if a 0.1 μF

coupling capacitor is used, the response at 300 Hz will be down only an additional 0.0008 dB.

VARIATION OF TRANSMIT INPUT RESISTANCE WITH SIGNAL LEVEL

The input resistance (R_{VFXI}) at VF_XI is specified as 390 kΩ, minimum. Typically, it is about 600 kΩ and will vary slightly with the input signal level at VF_XI. This variation in input resistance with signal level will result in low level signal distortion since the loading on the source impedance will not be constant. The magnitude of distortion will depend on the source impedance. Source impedances of 10 kΩ or less will ensure distortion products are better than 80 dB down. At typical telecom impedances of 900Ω or less, distortion products will be down more than 100 dB. Unless good distortion performance is not important in the application, source impedances much above 10 kΩ are not recommended as measurable impact on system distortion performance may result.

The absolute gain will also be impacted by loading on the source impedance. This error will be ≤0.02 dB for 1 kΩ source impedances and ≤0.22 dB for 10 kΩ source impedances.

TRANSMIT TO RECEIVE INTRACHANNEL CROSSTALK

The COMBO II CODEC/Filter is manufactured using the National high density M²CMOS process. One characteristic of this process is high digital speeds which induce large current transients in the power supply and ground lines. In particular, the D_X0 or D_X1 digital output drivers will produce significant V_{CC} and GND transients when their outputs change state, if heavy capacitive loading exists on the outputs. These transients may be under sampled by internal analog circuitry and will produce in-band noise. For most parameters there is little effect, but *for crosstalk from transmit to receive (CTXR), the effect can be quite large.* Under worst case conditions, CTXR can be degraded to as low as 66 dB from a nominal 80 dB. In many applications, this level of performance may be perfectly acceptable. Two wire circuits, for example, normally have no spec on crosstalk between the transmit and receive sides of the same line or trunk circuit. However, in applications such as four wire trunk circuits, transmit to receive intrachannel crosstalk performance may be marginal and methods must be considered for improvement.

Three approaches for reducing the effects of internally generated digital noise are: reduce the magnitude of the noise at the source, i.e., the current transients; reduce the resulting V_{CC} voltage noise caused by the current transients; and reduce the sensitivity of the device to V_{CC} noise.

The D_X0 and D_X1 output buffers have the largest effect on device noise performance, and as may be expected, D_X0 and D_X1 loading also has a significant effect. The worst case 66 dB CTXR is experienced with a load of 200 pF on the D_X pin. Therefore, if CTXR levels of 66 dB are not acceptable, National recommends that the capacitive loading on D_X0 and D_X1 be limited to about 50 pF.

Another technique which can be used in cases where heavy capacitive loading is unavoidable, is to use a small resistor (100Ω) in series with the D_X0 and D_X1 outputs. This also reduces the magnitude of the current spikes as well as provides device protection in the event of shorts on the bus. The effect of this impedance on timing will be minimal but it should be taken into account to ensure no timing specs are violated under worst case conditions.

In the future, National plans to modify the D_X0 and D_X1 output drivers to reduce the crossover supply current spikes and to control the output dV/dt to reduce the current transients due to capacitive loading.

To reduce the internally generated supply noise each COMBO II device should have a 0.1 μF capacitor connected from V_{CC} to GND as close as possible to the device pins. This is essentially the same precaution as recommended for externally generated digital noise, except the focus is on minimizing the distance from the device to the 0.1 μF bypass capacitor. Ideally it should be placed physically on the pins of the COMBO II device. The use of sockets moves the bypass capacitor physically further from the device, and therefore should be avoided. If sockets are necessary, the low profile type (i.e., Augat) may be used with minimal degradation.

As discussed above, it is critical to minimize the distance and inductance from the device to the bypass capacitor. It follows that larger packages force the capacitor further from the device in the same way that sockets do. Therefore, if CTXR is a critical parameter, it is advisable to use the TP3070V/75V (28-Pin PLCC) or the TP3071J/76J (20-Pin DIP) devices in place of the TP3070J/75J (28-Pin DIP).

PRINCIPLES OF QUIET LINE CARD DESIGN

PCM CODEC/Filter COMBO devices are complex analog and digital sub-systems on a single chip. They contain, for example, an A/D and D/A converter, each with 13 bit (for μ-Law) resolution in the lowest chord, near the origin of the companded transfer characteristic. This corresponds to a dynamic range of about 78 dB. In addition, the COMBO II family of devices has programmable transmit gain and receive attenuation with a programming range of 25.4 dB, giving an overall dynamic range of about 103 dB. With the transmit side programmed for 25.4 dB gain, the 0 dBm0 level at the VF_XI input pin will be 87 mVrms. At −75 dBm0, the input signal level will be 15.5 μVrms. Needless to say, very low level noise signals may impact transmission performance.

Due to the high resolution and low noise requirements of the analog circuitry, care must be taken to minimize the effect of digital noise on analog performance. By understanding the potential problems and taking precautionary measures, the COMBO II will deliver the performance required for high quality voice transmission even in the unfriendly electrical environment of a multi-line subscriber line card. Layout of printed circuit boards and breadboards **MUST** be considered part of the design task if low noise performance is to be assured.

Logic noise is generated both externally and internally in a typical COMBO II application. The use of high speed digital circuitry on the line card produces high frequency noise on the +5V supply line which is coupled into the analog circuitry by parasitic capacitances, device non-linearities and finite power supply rejection ratios of the amplifiers. This noise is mixed with the switching frequency of the switched capacitor clocks or the encoder or decoder clocks and may produce frequency components which lie within the voice band.

General Principles for Logic Circuitry

Linecards typically involve digital as well as analog circuitry on the card and it is important to minimize logic circuit noise not only to maintain good noise margins for the logic, but also to keep the overall logic noise level on the board as low

as possible for the analog circuitry. The basic points for logic portions of the board are:

1. Provide a high quality power and ground system.
2. Provide good high frequency supply decoupling on each component as well as low frequency decoupling for the board.
3. Keep signal line and component lead lengths as short as possible.
4. Route signal lines such that potential noise sources and logic signals are kept well away from analog circuits and analog power supply lines. In addition, special care may be needed for sensitive low level signal lines and high impedance points.
5. Take into consideration ground return and supply current paths.
6. Use the 74HC CMOS logic family or similar rather than TTL or LSTTL.

A good power and ground system has several beneficial effects. Since logic circuits draw relatively large transient currents during switching, ground and power lines must be low impedance to prevent appreciable voltage spikes from being developed. Because of the very high frequency components associated with the current spikes, ground and power lines must be low inductance as well as low resistance. For low inductance, power and ground traces on PC boards should be as wide as practical.

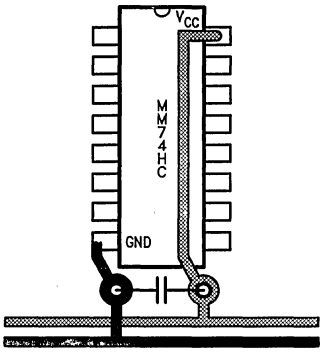
The ideal ground arrangement is a ground plane since inductance and resistance are very low and signal lines benefit from the closeness of ground as well. A ground plane will provide a lower characteristic impedance for the signal lines which helps reduce crosstalk noise from other signal lines. Noise will be injected into lines via a voltage divider formed by the capacitive coupling between lines and the line impedance. Reducing the line impedance therefore reduces the coupled noise voltage. In addition, the presence of ground has a shielding effect between lines which reduces crosstalk even further. The line characteristic impedance will be mainly a function of the dielectric constant of the board material, thickness of the board, and width of the conductor. For common $1/16$th inch epoxy fiberglass PC boards with a dielectric constant of about 5, a trace width of 20 mils (0.02 inch) will provide a characteristic impedance of 105Ω, which is reasonable for logic interconnections. The ground plane is normally on the component side of the board and all (or nearly all) interconnections between components are placed on the other side.

If a ground plane is not feasible because of high circuit density or is unavailable for other reasons, the next best approach is to simulate a ground plane by providing a rectangular grid of ground and power lines. Ground traces are run all around the digital circuit area of the board on all four sides. The ICs are then placed in rows with a ground bus running between each row. The ground busses are connected through at both ends to the ground busses on the periphery of the digital circuit area. A similar bussing arrangement is provided for the +5V supply as well, although it may not completely encircle the logic area and busses may not be connected through on both ends. Ground and +5 traces may be on either or both sides of the board. Generally, most traces are run vertically on one side of the board and horizontally on the other to avoid as many crossovers as possible. IC locations should be selected to minimize trace lengths between chips as well as between chips and connector pins. After the signal lines are run, interconnections between the ground busses should be placed wherever possible. It is often possible to add additional ground interconnections by rerouting a few traces or changing them to the other side of the board. This rectangular grid helps minimize the pathlength for the logic ground return currents. Because of the greater distance from ground, the characteristic impedance of signal lines will be higher than with a ground plane, resulting in more crosstalk due to capacitive coupling and reduced shielding effect. Noise on power and ground lines will also be higher because of higher resistance and inductance than with a ground plane. There will, however, be a great improvement over the situation where little attention is paid to power and ground arrangements and minimizing signal trace lengths.

The major functions of power supply decoupling for logic circuits are to maintain a very low supply impedance at high frequencies throughout the logic area, and to supply transient currents locally, which will reduce spikes on power and ground lines greatly. It is good practice to place a large electrolytic capacitor (at least 10 μF) and a ceramic disc capacitor (0.1 μF) from each supply to ground as close to the point where power enters the board as possible. This helps prevent external noise on the system backplane power and ground busses from entering the board. In addition, it reduces the amount of noise injected into the backplane busses from the linecard. The +5V and ground paths between these capacitors and the backplane connector should be kept very short. If the path lengths are significant, large transients may be produced in the +5V and ground lines due to capacitor in-rush currents when power is applied to the circuit. To prevent excessive inrush currents and possible burning of contacts, overly large values of electrolytic decoupling capacitor should be avoided. Both types of capacitor are necessary to provide a low impedance at both low and high frequencies. An electrolytic will provide the large capacitance needed to maintain a low impedance at lower frequencies. At frequencies above 1 MHz, most electrolytics appear inductive and a good high frequency capacitor with low Effective Series Resistance (ESR), such as a ceramic disc capacitor, is necessary to maintain a low impedance at higher frequencies.

Additional ceramic disc capacitors should be placed from +5V to ground throughout the logic circuit area, one for every IC. Ideally, the local bypass capacitor should supply all of the transient current required by the logic device it serves. Capacitor lead lengths should be kept short to minimize inductance and capacitor placement should minimize the current path length between the capacitor and the power and ground pins of the chip it serves. Illustrated in *Figure 3* are some examples of PC layouts for logic devices, for different bussing schemes. Note that in all cases, the logic device V_{CC} and GND connections meet the bus connections at the capacitor solder pads. This ensures that transient currents flowing from the busses to the capacitor do not flow in the paths between the capacitor and device power pins, minimizing the magnitude of transient voltages applied to the device.

Short line lengths will help to reduce crosstalk between signal lines due to capacitive coupling. For digital circuits, however, the major advantage of short line lengths will be in greatly reduced distortion of signal waveforms due to reflections. Reflections occur on a signal line wherever impedance changes occur on the line. All signal conductors have some characteristic impedance which is a function of their physical dimensions and distance from ground. If the line characteristic impedance (Z_0) is equal to the load imped-



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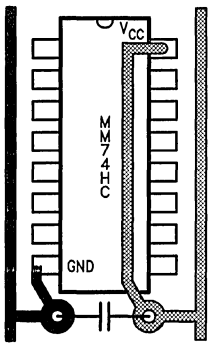

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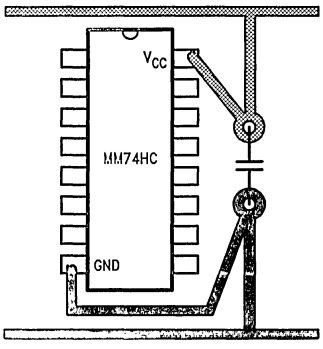

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FIGURE 3. PC Layout Examples for Logic Devices

ance, all energy will be transferred to the load and no reflection will result. The problem with logic circuits is that normally the gate input impedance is much higher than the line impedance and a gross mismatch occurs which causes reflections. If the round trip propagation delay from driving gate to receiving gate and back to the driving gate is much less than the transition time of the signal at the driver output, all reflections (and re-reflections) will occur and die out before the transition is complete and will not be noticeable on the waveform. For round trip delays approaching the order of the driver rise and fall times, some waveform distortion will be noticeable, while large overshoots and ringing will occur for longer line lengths. Propagation delays of 1.5–2 ns/foot are typical for epoxy fiberglass PC boards. The implications of this are greatest for backplane logic signals where distances are significant.

TTL and LSTTL logic families draw considerably different supply currents when their outputs are in the HIGH and LOW logic states, causing large switching currents to flow through the busses and decoupling capacitors. In contrast, CMOS logic circuits only draw significant currents during state transitions, and these currents are substantially equal. A CMOS logic system therefore generates far less electrical noise than a similar TTL system. Use of the 74HC CMOS logic family is highly recommended for line card design. It helps to preserve high quality transmission performance in the analog circuits and offers better noise margins than TTL in the presence of transient voltages induced by relays and ringing signals.

General Principles for Analog Circuitry and COMBO II Devices

Different techniques are necessary for the layout of analog circuits (COMBO II, SLIC and any external analog sections) than for digital logic circuits on the card.

The GND pin of each COMBO II device should be used as the Ground Reference Point (GRP) for each line circuit. All analog ground connections for a single line circuit should connect directly to the reference point. This includes:

1. The analog ground from the 4-wire side of the SLIC circuit
2. The grounds for any analog networks or gain stages at the transmit VF_XI input or receive VF_RO output.
3. The ground side of the 0.1 μF decoupling capacitors for the +5V and −5V COMBO II power supplies.

Ground return currents from logic circuits, relays, etc., must not flow through the analog ground lines to avoid generating noise transient voltages in the ground lines. Separate analog and digital ground busses should be used on the card and should meet only at the point where +5V and −5V are decoupled to ground near the card connector. Likewise, separate analog and digital +5V busses should be run to the analog circuitry and to the logic circuits from the decoupled point near the card connector. It is NOT recommended to run separate analog and digital ground busses nor separate analog and digital +5V lines all the way to the system backplane. The analog +5V and −5V supply busses should be routed adjacent to the analog ground bus to help ensure that any noise pick-up is common mode. Relays and other circuits operating from the −48V battery supply should, however, have a separate return bus to the battery ground.

All signals and circuits capable of inducing large emf's into the analog circuitry should be located around the edge of the card whenever possible. This includes:

1. Relay drive and output signals
2. Ringing distribution
3. The 2-wire side of SLIC circuitry
4. −48V battery
5. DC to DC converters.

The switching frequency of converters **MUST** be synchronized with COMBO II clocks to prevent audible beat frequencies which may otherwise fall in the passband.

To minimize external digital noise injection into the COMBO II device, it is very important to connect a 0.1 μF ceramic capacitor from V_{CC} to GND near the COMBO II device as well as at each noise source. It is critical that the length of the capacitor leads (and lead extensions via PCB traces to the device V_{CC} and GND pins) be kept as short as possible to minimize lead resistance and inductance and the resulting voltage spikes generated by transient currents flowing through these supply impedances. The V_{CC} and GND traces from the COMBO II pins and those from the supply busses should meet at the capacitor through holes or solder pads as shown in *Figure 4*. This eliminates the generation of voltage spikes in the COMBO II V_{CC} and GND connections to the capacitor due to logic transient currents flowing through a common trace length to the capacitor.

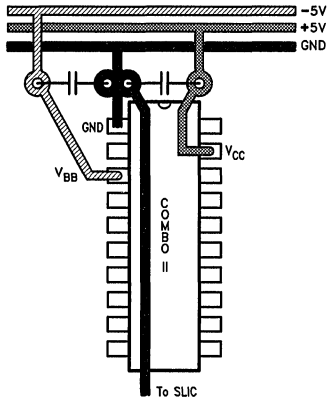

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FIGURE 4. PC Layout Example for COMBO II Devices

Another technique sometimes used to further decouple V_{CC} is to add a small impedance, such as an inductor or a resistor, in series with the COMBO II V_{CC} trace on the backplane side of the 0.1 μF capacitor. There are potential problems with this approach in that the COMBO II supply may increase more slowly than that of the digital circuitry. This may result in COMBO II inputs momentarily becoming more positive than the V_{CC} potential, possibly triggering latch-up. For this reason, a series impedance in the COMBO II V_{CC} line is not recommended unless Schottky diodes are used as described in the section on latch-up. A second potential problem is the reduction is supply voltage at the device power supply pins, especially under heavy loading conditions. Generally, a series resistance should not exceed 10Ω.

Normally, there is far less noise on the V_{SS} supply line allowing simple bypassing with a 0.1 μF capacitor. Decoupling V_{SS} with a series resistor or inductor is not recommended since the impedance reduces the effectiveness of the Schottky clamping diode which should be connected between V_{SS} and GND as described in the section on latch-up. If decoupling with a series element is required, the Schottky diode must be connected on the device side of the impedance, in essence requiring a diode for each COMBO II device rather than one per board.

Shown in *Figure 5* is an example of a PC layout for a portion of a line card utilizing the techniques described above.

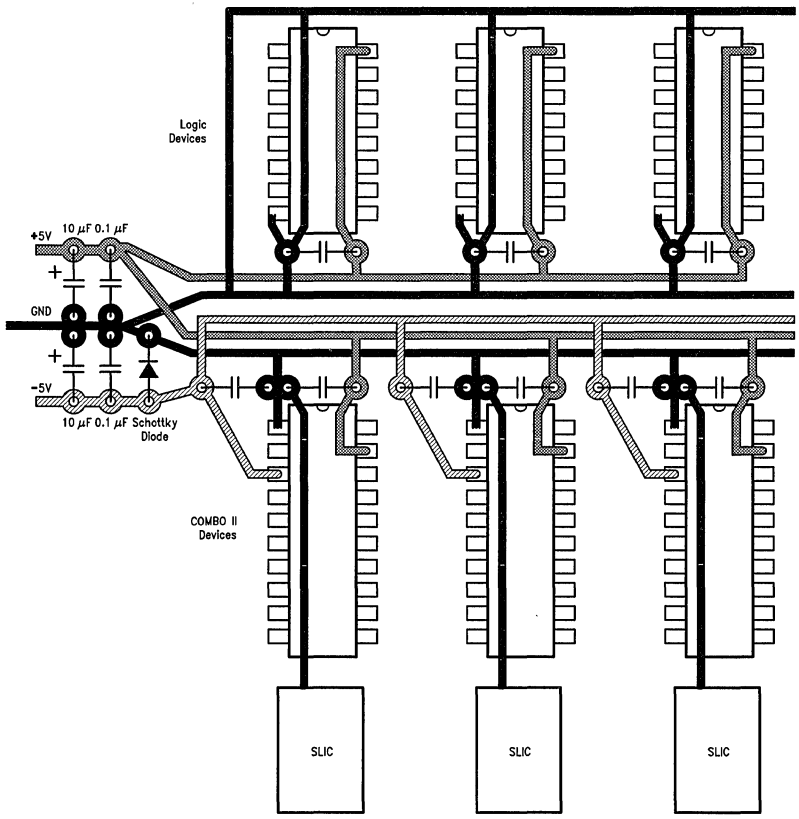

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FIGURE 5. PC Board Layout Example

LATCH-UP PREVENTION TECHNIQUES

CMOS devices are subject to latch-up under certain conditions and it is important to understand what conditions can cause latch-up so the proper precautions can be taken. This is particularly important in telecommunications applications where it is necessary to insert a PC board into a system which is already powered up. Latch-up is a parasitic SCR type action which, when once triggered, causes continuous current flow through the device, usually limited only by circuit impedances and power supply capability.

With COMBO II devices, this SCR takes the form of parasitic bipolar NPN and PNP transistors. The NPN transistor base is the device substrate (also V_{BB}). The emitter is at Ground, collector at V_{CC}. If V_{BB} is allowed to go above Ground enough to turn on the base-emitter junction, the NPN will conduct current from V_{CC} to Ground. Current flow in the NPN also supplies base current to the PNP, which in turn supplies more current for the NPN. If the currents are large enough, the base currents may be sustained by internal IR drops even if V_{BB} is then connected to $-5V$, resulting in latch-up. This scenario can occur when boards are plugged into a "hot" system, if precautions are not taken. When connector contacts are allowed to mate in random order, logic signals, Ground and V_{CC} may be applied to the device before V_{BB} comes up. The logic signals then forward bias input protection diodes, charging the floating V_{BB} to above Ground potential, and turning on the parasitic NPN.

There are two types of protective measures:

1. Proper sequencing of logic signals and power supplies to prevent the NPN turn-on
2. Limiting the V_{BB} voltage to no more than a few tenths of a volt above Ground

The ideal sequence of power supplies and logic signals is Ground first, V_{BB}, then V_{CC}, and logic signals last. This ensures that Absolute Maximum Ratings for inputs are not exceeded, even momentarily during the power up transient, as logic signals will not exceed power supply voltages. It also ensures that the parasitic NPN is not turned on by having V_{BB} floating while Ground, V_{CC} and/or logic signals are applied. Given below are some practical methods of sequencing logic signals and power supplies and other methods of achieving protection.

Mechanically, sequencing of connections can be accomplished by using advanced connector pins or selectively shortening card edge connector contact metal. If ground, V_{BB} and V_{CC} are mechanically sequenced, these pins should be close together to minimize angle errors when inserting boards. Some sequencing can be done electrically as well. If COMBO inputs and outputs are buffered from the backplane by logic devices running from the same V_{CC} supply as the COMBO device, the logic signals cannot exceed the V_{CC} voltage. Note that if different V_{CC} supplies are used for the buffer logic and the COMBO, this protection will be lost unless the COMBO supply comes up first. Even when a single V_{CC} source is used, power supply decoupling which includes a series element in the V_{CC} line to the COMBO can cause the same effect by slowing the rise of V_{CC} voltage at the COMBO V_{CC} pin.

Buffering of all inputs and outputs from the backplane is also recommended to prevent ringing of logic signals on the buses which may exceed the supply rails from being applied to the COMBO device input and output pins. If input buffers are not used, series 1 kΩ resistors are recommended to limit current to inputs which go directly to the backplane. Note that use of series resistors will have a small impact on worst case signal timing. Even though inputs are buffered, other circuits connected between V_{CC} and V_{BB}, such as op amps, may pull V_{BB} above ground if V_{CC} precedes V_{BB}. If this other circuitry can supply enough current to trigger latch-up, a Schottky diode will be needed across V_{BB} as explained below.

If full sequencing is not practical in the application, at least the Ground pin should be advanced to ensure that Ground makes contact first. A Schottky diode should then be placed between V_{BB} and Ground such that it is forward biased if V_{BB} goes above Ground (anode connected to V_{BB}). This will limit the NPN base-emitter voltage to a few tenths of a Volt and prevent turn-on. A low cost device suitable for this application is the 1N5820. One per board should be sufficient unless series impedances are used in the V_{BB} line between the diode and the COMBO II V_{BB} pin. If series impedances are necessary to provide additional supply decoupling, or for other reasons, it is likely that one diode per COMBO II device will be necessary, as the series impedance will spoil the low voltage clamping action of the Schottky diode. In designs where series impedances are used along with one diode per COMBO II device, a smaller diode, the 1N5817, may be considered.

No matter which latch-up protection method is selected, the final circuit should be thoroughly tested for immunity to latch-up. Testing should include repeated insertion of a number of boards of each type into the actual live system and monitoring for latch-up. Boards should be inserted at different angles to simulate all possible connector contact sequences which can occur. Manual sequencing of signals and power supplies to the boards should also be performed to ensure all possible combinations have been tested.

ASYNCHRONOUS OPERATION

The COMBO II family of devices was not designed for asynchronous transmission applications where independent transmit and receive clocks are required. The devices have only one master clock pin (MCLK) and one bit clock pin (BCLK) which serve both transmit and receive sides of the device. With the use of a minor amount of external logic, however, operation in asynchronous systems can be achieved. Impact on transmission performance due to resynchronizing receive data will be negligible, but a high degree of care is required to minimize the level of beat frequencies produced in the output to an acceptable level. These beat frequencies are the difference between the two asynchronous clock frequencies and tend to fall below 200 Hz. If close attention is paid to power supply decoupling, grounding, and reducing receive clock noise on these as well as signal lines, these frequencies will not be audible. The COMBO device **MUST** be well isolated from the receive clock frequency and its higher order components.

The basic concept consists of buffering the receive data and retiming both the data and receive frame sync pulse using the transmit bit clock. In this way, the COMBO II device itself can continue to operate entirely in a synchronous manner. There are many ways to implement this—per bit, per sample, per frame, per line, per linecard, per system, etc. The technique and circuit described below uses a per sample and per line technique and can be used to demonstrate and/or evaluate transmission performance with asynchronous operation. Type of system, system requirements, and how partitioning and implementation of various functions have been accomplished will determine which is the

optimum approach for each COMBO II application. To minimize cost and associated PC board area, the synchronization logic circuitry could be incorporated into a gate array chip which is commonly used to handle the backplane interface and other miscellaneous logic functions required on the linecard.

The per sample per line technique consists of temporarily storing each receive PCM data byte in a buffer (see *Figure 6*). The byte is clocked into the buffer using the system receive clock ($BCLK_R$). After all eight bits have been received, the system transmit clock ($BCLK_X$), also used as BCLK for COMBO II, is used to clock the byte out of the register, and into the COMBO device. At the same time, a new receive frame sync pulse (FS_R') is generated for the COMBO II device, using the system $BCLK_X$ timing. The system transmit clock ($BCLK_X$) should also be used as MCLK for the COMBO II device (i.e., BCLK and MCLK pins connected together). If BCLK is not an allowable MCLK frequency (512, 1536, 1544, 2048 or 4096 kHz), BCLK and MCLK must still be synchronous with respect to each other.

Assuming 2.048 MHz BCLK rates and that clocking of data out of the buffer begins two bit periods after the buffer is filled, the delay will be 10 BCLK periods, or about 5 μs. This delay will change as $BCLK_X$ and $BCLK_R$ drift with respect to each other, until a full BCLK period of delay change has accumulated. At this point, a jump of one $BCLK_X$ period occurs in the delay associated with the generation of the new receive frame sync pulse, as well as in clocking of data into the COMBO device. Note that no data bits have been lost, only a $BCLK_X$ period has been slipped resulting in a slight jitter of the decoded sample pulse width. The peak to peak magnitude of this jitter will be one BCLK period, or about 0.5 μs. Since the sample pulse width is 125 μs, distortion components would be down about 48 dB if this jitter occurred on every sample. Assuming 50 ppm clock accuracies, the worst case difference frequency is 200 Hz, which will also equal the number of samples per second which have jitter. With 8k samples per second occurring, distortion will be down another 32 dB because of the low density of jittered samples. Considering both aspects, the worst case distortion levels to be expected from this jitter will be 80 dB below the signal level, at least 40 dB below the level of normal quantizing distortion. If clock frequencies are better than their specified tolerance, as they typically should be, actual distortion will be even lower.

Figure 7 illustrates a circuit for implementing the block diagram for non-delayed timing mode. The circuit consists of an MM74HC164 shift register (R1) which is used as the data buffer, another MM74HC164 which counts the received data bits (R2), and some additional logic which selects the clocks to be applied to the buffer and generates the new receive frame sync pulse. FF1 senses the beginning of the cycle by clocking in a HIGH on the system receive frame sync rising edge. FF2 and FF3 control the switchover from $BCLK_R$ to $BCLK_X$ to prevent overlap of clock pulses at R1 and R2 clock inputs. FF4 provides a one bit delay to prevent missing the first data bit of the byte. The 100 kΩ resistor and 0.01 μF capacitor function as a power-up clear to ensure the register starts in the all zero state.

Figure 8 is a timing diagram for the circuit. At the end of the previous cycle, FF1 has been cleared to LOW at the Q output, which disables $BCLK_R$ at the L1 clock select logic (MM74HC58). The Q outputs of FF2 and FF3 have also been cleared to LOW. The LOW at the Q output of FF3 disables $BCLK_X$. The cycle begins with the occurrence of a system receive frame sync pulse, signifying the arrival of another receive data byte. The rising edge of the system receive frame sync pulse (FS_R) clocks a HIGH to the Q output of FF1, since the D input is connected HIGH. This enables $BCLK_R$ at L1, which has been inverted to allow the data to be clocked into R1 in the center of the data period. R2 shifts in a logic HIGH at the A serial input with each $BCLK_R$ pulse. After eight clock pulses, the Qh output goes HIGH. This is inverted and used to clear FF1, which in turn disables further $BCLK_R$ pulses at L1. Since R2 Qh output is now HIGH, FF2 and FF3 are no longer being cleared and are allowed to shift the HIGH at FF2 D input to FF3 Q output after 2 $BCLK_X$ rising edges. $BCLK_X$ is enabled, and the receive data byte is shifted out of R1 and into COMBO II, through FF4. At the same time, since FF1 has been cleared to a LOW at the Q output, R2 now shifts the LOW level present at the A/B inputs into the register. After eight $BCLK_X$ pulses, Qh returns LOW. This again clears FF2 and FF3, and disables $BCLK_X$ at L1. The cycle is now complete. The Q output of FF3 is used as the new receive frame sync pulse (FS_R') as it is HIGH when $BCLK_X$ is enabled.

FF4 provides an additional one bit delay of the receive data to prevent the first data bit from being missed when data is clocked into COMBO II. This is needed because R1 clocks on positive edges while COMBO II clocks in data on negative edges. The MSB data bit will be available at R1 output after eight $BCLK_R$ pulses. When the register is clocked by the rising edge of the first $BCLK_X$ pulse, this data bit will be shifted to FF4. The following negative edge of $BCLK_X$ will clock this bit into the COMBO II. Without FF4, the MSB would be lost.

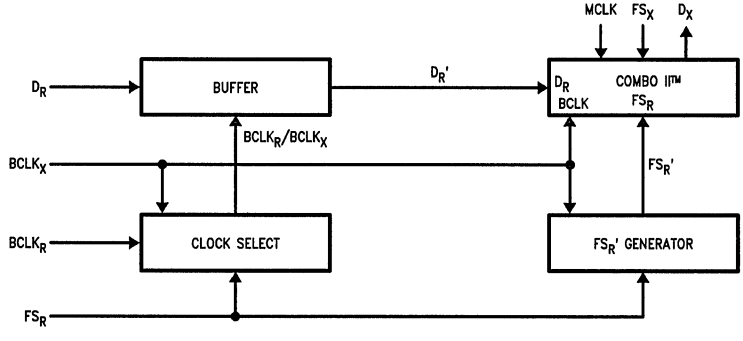

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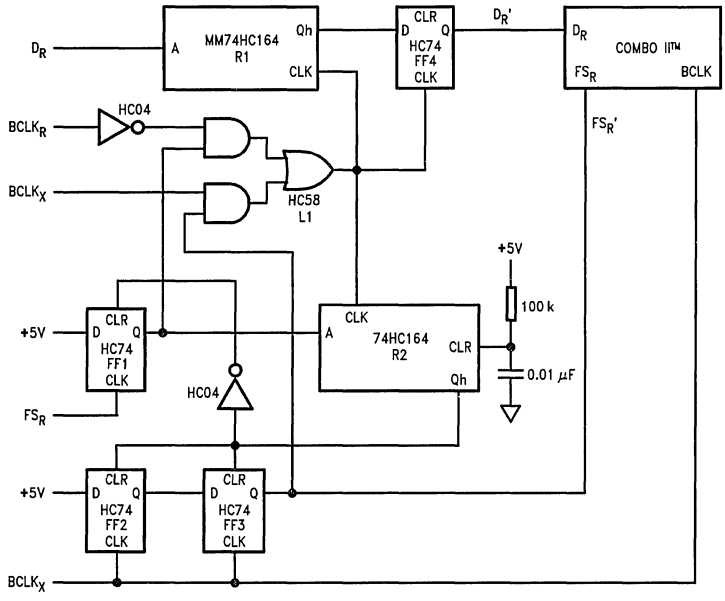
FIGURE 6. Synchronizer Block Diagram



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Note: All unused inputs tied HIGH.

FIGURE 7. Synchronizer Circuit

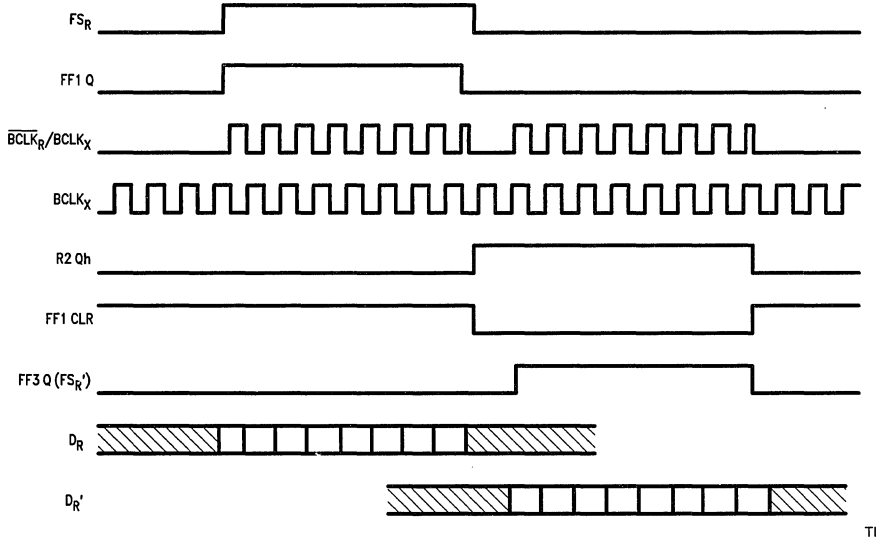

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FIGURE 8. Synchronizer Circuit Timing

RESERVED CONTROL INTERFACE REGISTER ADDRESSES

Four bits are used in the first byte of each control register instruction as a register address. Of the sixteen possible combinations, ten are used currently to address programming registers, seven of which are given in Table I of the data sheet. The remaining three hybrid balance register addresses are: Hybal1 = 0110 (hex 6), Hybal 2 = 0111 (hex 7), and Hybal 3 = 1000 (hex 8).

The remaining six addresses, 0011 (hex 3) and 1011 (hex B) through 1111 (hex F) are reserved for future use and should not be used in a control instruction. Attempting access using these addresses may cause improper operation of the device or render it nonfunctional until it is reset or a power down command is issued. Programming software should be written to ensure no spurious addresses are generated.

TROUBLESHOOTING GUIDE

Trouble	Potential Cause
No Tx Output at D_X	Enable bit set to zero (Tx Time slot and Port assignment register). Tx gain register set to "off" (all zeros). Tx Port select bit set incorrectly. For TP3071 devices, this bit must always be set to zero. For TP3076 devices, it must always be set to one. For TP3070 and TP3075 devices, this bit must be set to zero or one depending on which port is being used. Device is powered down. Send any control instruction with bit 7 of byte 1 (power up/down control bit) set to logic LOW. Device has been reset. This may be caused by applying power to the device, Master Reset (MR) pin going HIGH, or large negative transient on V_{CC}. MR should be LOW for normal operation. Program all registers to desired states.
No Rx Output at VF_RO	Enable bit set to zero (Rx Time slot and Port assignment register). Rx gain register set to "off" (all zeros). Rx Port select bit set incorrectly. For TP3071 devices, this bit must always be set to zero. For TP3076 devices, it must always be set to one. For TP3070 and TP3075 devices, this bit must be set to zero or one depending on which port is being used. Device is powered down. Send any control instruction with bit 7 of byte 1 (power up/down control bit) set to logic LOW. Device has been reset. This may be caused by applying power to the device, Master Reset (MR) pin going HIGH, or large negative transient on V_{CC}. MR should be LOW for normal operation. Program all registers to desired states.
High Distortion at VF_RO and D_X	Timing mode programmed incorrectly. If the system uses Non Delayed Data timing and the device is programmed for Delayed Data timing, or vice versa, Rx PCM data will be read incorrectly at the D_R input, causing high distortion of the signal at the receive output. Also, D_X output data may be misread by the system. Program bit 3 of byte 2 of the Control Register instruction for the proper mode. Rx gain register incorrectly set for load. See section entitled "Minimum Receive Attenuation vs. Output Loading".
Incorrect Response to Control Instructions	Byte count synchronization has been lost in the control interface logic. Three solutions exist when the current state of the byte count is unknown: 1. Remove and reapply power to the device; 2. pulse the Master Reset (MR) pin momentarily HIGH; or 3. send the single byte power up/down instruction. Devices having the CI/O pin should not use option three.
Excessive Tx to Rx Crosstalk	High capacitive loading on D_X0 and/or D_X1 output(s). Minimize capacitive loading as much as possible, at least to 50 pF or less. If heavy capacitive loading cannot be avoided, place a 100Ω resistor in series with the D_X output(s) to reduce the magnitude of current spikes. Be sure to consider the effect of the added delay on timing if a series resistor is used. Inadequate or ineffective power supply decoupling. A 0.1 μF decoupling capacitor should be placed from V_{CC} to GND as close as possible to the device pins. Do not use sockets, as this increases the distance between capacitor and device pins. If sockets are necessary, use low profile sockets. Use the smaller packages (PLCC or 20-pin DIP) rather than the 28-pin DIP.
Device Gets Hot	Latch-up has occurred due to violation of Absolute Maximum Ratings when signal voltages instantaneously exceed power supply voltages, or supply voltage polarity reversals have occurred. These may occur when power is applied to the system or a board is plugged into a hot system. Solutions: prevent signals from reaching the device inputs before power supply voltages (sequence connector pins: Ground first, V_{BB}, then V_{CC}, signals last), or connect a Schottky diode from V_{BB} to Ground. If V_{CC} may go negative with respect to ground, a Schottky diode may also be required from V_{CC} to Ground. Eliminate excessive ringing on logic signals so supply voltages are not exceeded. Eliminate series decoupling resistors or inductors in V_{CC} and V_{BB} lines to COMBO device as this delays supply voltages with respect to signal voltages.

TROUBLESHOOTING GUIDE (Continued)

Trouble	Potential Cause
Other Improper Functioning	Register contents are scrambled. Reset device by removing and reapplying power or taking the Master Reset (MR) pin momentarily HIGH. Program all ten registers to desired states.
	Damaged device. Replace with good device.
	Violation of PCM or Control Interface timing specs. Verify with oscilloscope that all timing relationships at the device pins meet data sheet spec requirements.
	Wiring error. Inspect ALL device pins with oscilloscope for presence of correct signals and absence of incorrect signals. Inspection should be done directly on the device pins to ensure problems due to bad solder joints or socket connections are found.

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APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes

TP3075/6 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
5.0	1.375	0.0	6.4	1.619	255	11111111	8.1	1.964	0.0
4.9	1.359	0.1	6.3	1.600	254	11111110	8.0	1.941	0.1
4.8	1.344	0.2	6.2	1.582	253	11111101	7.9	1.919	0.2
4.7	1.328	0.3	6.1	1.564	252	11111100	7.8	1.897	0.3
4.6	1.313	0.4	6.0	1.546	251	11111011	7.7	1.875	0.4
4.5	1.298	0.5	5.9	1.528	250	11111010	7.6	1.854	0.5
4.4	1.283	0.6	5.8	1.511	249	11111001	7.5	1.833	0.6
4.3	1.269	0.7	5.7	1.494	248	11111000	7.4	1.812	0.7
4.2	1.254	0.8	5.6	1.477	247	11110111	7.3	1.791	0.8
4.1	1.240	0.9	5.5	1.460	246	11110110	7.2	1.770	0.9
4.0	1.225	1.0	5.4	1.443	245	11110101	7.1	1.750	1.0
3.9	1.211	1.1	5.3	1.426	244	11110100	7.0	1.730	1.1
3.8	1.198	1.2	5.2	1.410	243	11110011	6.9	1.710	1.2
3.7	1.184	1.3	5.1	1.394	242	11110010	6.8	1.691	1.3
3.6	1.170	1.4	5.0	1.378	241	11110001	6.7	1.671	1.4
3.5	1.157	1.5	4.9	1.362	240	11110000	6.6	1.652	1.5
3.4	1.144	1.6	4.8	1.347	239	11101111	6.5	1.633	1.6
3.3	1.131	1.7	4.7	1.331	238	11101110	6.4	1.615	1.7
3.2	1.118	1.8	4.6	1.316	237	11101101	6.3	1.596	1.8
3.1	1.105	1.9	4.5	1.301	236	11101100	6.2	1.578	1.9
3.0	1.092	2.0	4.4	1.286	235	11101011	6.1	1.560	2.0
2.9	1.080	2.1	4.3	1.271	234	11101010	6.0	1.542	2.1
2.8	1.067	2.2	4.2	1.257	233	11101001	5.9	1.524	2.2
2.7	1.055	2.3	4.1	1.242	232	11101000	5.8	1.507	2.3
2.6	1.043	2.4	4.0	1.228	231	11100111	5.7	1.490	2.4
2.5	1.031	2.5	3.9	1.214	230	11100110	5.6	1.472	2.5
2.4	1.019	2.6	3.8	1.200	229	11100101	5.5	1.456	2.6
2.3	1.008	2.7	3.7	1.186	228	11100100	5.4	1.439	2.7
2.2	0.996	2.8	3.6	1.173	227	11100011	5.3	1.423	2.8
2.1	0.985	2.9	3.5	1.159	226	11100010	5.2	1.406	2.9
2.0	0.973	3.0	3.4	1.146	225	11100001	5.1	1.390	3.0
1.9	0.962	3.1	3.3	1.133	224	11100000	5.0	1.374	3.1
1.8	0.951	3.2	3.2	1.120	223	11011111	4.9	1.358	3.2
1.7	0.940	3.3	3.1	1.107	222	11011110	4.8	1.343	3.3
1.6	0.930	3.4	3.0	1.095	221	11011101	4.7	1.328	3.4
1.5	0.919	3.5	2.9	1.082	220	11011100	4.6	1.312	3.5
1.4	0.908	3.6	2.8	1.070	219	11011011	4.5	1.297	3.6
1.3	0.898	3.7	2.7	1.057	218	11011010	4.4	1.282	3.7
1.2	0.888	3.8	2.6	1.045	217	11011001	4.3	1.268	3.8
1.1	0.878	3.9	2.5	1.033	216	11011000	4.2	1.253	3.9
1.0	0.868	4.0	2.4	1.022	215	11010111	4.1	1.239	4.0
0.9	0.858	4.1	2.3	1.010	214	11010110	4.0	1.225	4.1
0.8	0.848	4.2	2.2	0.998	213	11010101	3.9	1.211	4.2
0.7	0.838	4.3	2.1	0.987	212	11010100	3.8	1.197	4.3
0.6	0.829	4.4	2.0	0.976	211	11010011	3.7	1.183	4.4
0.5	0.819	4.5	1.9	0.964	210	11010010	3.6	1.170	4.5
0.4	0.810	4.6	1.8	0.953	209	11010001	3.5	1.156	4.6
0.3	0.800	4.7	1.7	0.942	208	11010000	3.4	1.143	4.7
0.2	0.791	4.8	1.6	0.932	207	11001111	3.3	1.130	4.8
0.1	0.782	4.9	1.5	0.921	206	11001110	3.2	1.117	4.9
0.0	0.773	5.0	1.4	0.910	205	11001101	3.1	1.104	5.0
−0.1	0.764	5.1	1.3	0.900	204	11001100	3.0	1.092	5.1
−0.2	0.756	5.2	1.2	0.890	203	11001011	2.9	1.079	5.2
−0.3	0.747	5.3	1.1	0.880	202	11001010	2.8	1.067	5.3
−0.4	0.738	5.4	1.0	0.869	201	11001001	2.7	1.055	5.4

APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes (Continued)

TP3075/6 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
−0.5	0.730	5.5	0.9	0.860	200	11001000	2.6	1.042	5.5
−0.6	0.722	5.6	0.8	0.850	199	11000111	2.5	1.031	5.6
−0.7	0.713	5.7	0.7	0.840	198	11000110	2.4	1.019	5.7
−0.8	0.705	5.8	0.6	0.830	197	11000101	2.3	1.007	5.8
−0.9	0.697	5.9	0.5	0.821	196	11000100	2.2	0.996	5.9
−1.0	0.689	6.0	0.4	0.811	195	11000011	2.1	0.984	6.0
−1.1	0.681	6.1	0.3	0.802	194	11000010	2.0	0.973	6.1
−1.2	0.673	6.2	0.2	0.793	193	11000001	1.9	0.962	6.2
−1.3	0.666	6.3	0.1	0.784	192	11000000	1.8	0.951	6.3
−1.4	0.658	6.4	0.0	0.775	191	10111111	1.7	0.940	6.4
−1.5	0.651	6.5	−0.1	0.766	190	10111110	1.6	0.929	6.5
−1.6	0.643	6.6	−0.2	0.757	189	10111101	1.5	0.918	6.6
−1.7	0.636	6.7	−0.3	0.749	188	10111100	1.4	0.908	6.7
−1.8	0.628	6.8	−0.4	0.740	187	10111011	1.3	0.898	6.8
−1.9	0.621	6.9	−0.5	0.732	186	10111010	1.2	0.887	6.9
−2.0	0.614	7.0	−0.6	0.723	185	10111001	1.1	0.877	7.0
−2.1	0.607	7.1	−0.7	0.715	184	10111000	1.0	0.867	7.1
−2.2	0.600	7.2	−0.8	0.707	183	10110111	0.9	0.857	7.2
−2.3	0.593	7.3	−0.9	0.699	182	10110110	0.8	0.847	7.3
−2.4	0.587	7.4	−1.0	0.691	181	10110101	0.7	0.838	7.4
−2.5	0.580	7.5	−1.1	0.683	180	10110100	0.6	0.828	7.5
−2.6	0.573	7.6	−1.2	0.675	179	10110011	0.5	0.819	7.6
−2.7	0.567	7.7	−1.3	0.667	178	10110010	0.4	0.809	7.7
−2.8	0.560	7.8	−1.4	0.660	177	10110001	0.3	0.800	7.8
−2.9	0.554	7.9	−1.5	0.652	176	10110000	0.2	0.791	7.9
−3.0	0.547	8.0	−1.6	0.645	175	10101111	0.1	0.782	8.0
−3.1	0.541	8.1	−1.7	0.637	174	10101110	0.0	0.773	8.1
−3.2	0.535	8.2	−1.8	0.630	173	10101101	−0.1	0.764	8.2
−3.3	0.529	8.3	−1.9	0.623	172	10101100	−0.2	0.755	8.3
−3.4	0.523	8.4	−2.0	0.616	171	10101011	−0.3	0.747	8.4
−3.5	0.517	8.5	−2.1	0.608	170	10101010	−0.4	0.738	8.5
−3.6	0.511	8.6	−2.2	0.602	169	10101001	−0.5	0.730	8.6
−3.7	0.505	8.7	−2.3	0.595	168	10101000	−0.6	0.721	8.7
−3.8	0.499	8.8	−2.4	0.588	167	10100111	−0.7	0.713	8.8
−3.9	0.494	8.9	−2.5	0.581	166	10100110	−0.8	0.705	8.9
−4.0	0.488	9.0	−2.6	0.574	165	10100101	−0.9	0.697	9.0
−4.1	0.482	9.1	−2.7	0.568	164	10100100	−1.0	0.689	9.1
−4.2	0.477	9.2	−2.8	0.561	163	10100011	−1.1	0.681	9.2
−4.3	0.471	9.3	−2.9	0.555	162	10100010	−1.2	0.673	9.3
−4.4	0.466	9.4	−3.0	0.549	161	10100001	−1.3	0.665	9.4
−4.5	0.461	9.5	−3.1	0.542	160	10100000	−1.4	0.658	9.5
−4.6	0.455	9.6	−3.2	0.536	159	10011111	−1.5	0.650	9.6
−4.7	0.450	9.7	−3.3	0.530	158	10011110	−1.6	0.643	9.7
−4.8	0.445	9.8	−3.4	0.524	157	10011101	−1.7	0.635	9.8
−4.9	0.440	9.9	−3.5	0.518	156	10011100	−1.8	0.628	9.9
−5.0	0.435	10.0	−3.6	0.512	155	10011011	−1.9	0.621	10.0
−5.1	0.430	10.1	−3.7	0.506	154	10011010	−2.0	0.614	10.1
−5.2	0.425	10.2	−3.8	0.500	153	10011001	−2.1	0.607	10.2
−5.3	0.420	10.3	−3.9	0.495	152	10011000	−2.2	0.600	10.3
−5.4	0.415	10.4	−4.0	0.489	151	10010111	−2.3	0.593	10.4
−5.5	0.410	10.5	−4.1	0.483	150	10010110	−2.4	0.586	10.5
−5.6	0.406	10.6	−4.2	0.478	149	10010101	−2.5	0.579	10.6
−5.7	0.401	10.7	−4.3	0.472	148	10010100	−2.6	0.573	10.7
−5.8	0.397	10.8	−4.4	0.467	147	10010011	−2.7	0.566	10.8
−5.9	0.392	10.9	−4.5	0.462	146	10010010	−2.8	0.560	10.9

APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes (Continued)

TP3075/6 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
−6.0	0.388	11.0	−4.6	0.456	145	10010001	−2.9	0.553	11.0
−6.1	0.383	11.1	−4.7	0.451	144	10010000	−3.0	0.547	11.1
−6.2	0.379	11.2	−4.8	0.446	143	10001111	−3.1	0.541	11.2
−6.3	0.374	11.3	−4.9	0.441	142	10001110	−3.2	0.535	11.3
−6.4	0.370	11.4	−5.0	0.436	141	10001101	−3.3	0.529	11.4
−6.5	0.366	11.5	−5.1	0.431	140	10001100	−3.4	0.522	11.5
−6.6	0.362	11.6	−5.2	0.426	139	10001011	−3.5	0.516	11.6
−6.7	0.358	11.7	−5.3	0.421	138	10001010	−3.6	0.511	11.7
−6.8	0.353	11.8	−5.4	0.416	137	10001001	−3.7	0.505	11.8
−6.9	0.349	11.9	−5.5	0.411	136	10001000	−3.8	0.499	11.9
−7.0	0.345	12.0	−5.6	0.407	135	10000111	−3.9	0.493	12.0
−7.1	0.341	12.1	−5.7	0.402	134	10000110	−4.0	0.488	12.1
−7.2	0.338	12.2	−5.8	0.397	133	10000101	−4.1	0.482	12.2
−7.3	0.334	12.3	−5.9	0.393	132	10000100	−4.2	0.476	12.3
−7.4	0.330	12.4	−6.0	0.388	131	10000011	−4.3	0.471	12.4
−7.5	0.326	12.5	−6.1	0.384	130	10000010	−4.4	0.466	12.5
−7.6	0.322	12.6	−6.2	0.380	129	10000001	−4.5	0.460	12.6
−7.7	0.319	12.7	−6.3	0.375	128	10000000	−4.6	0.455	12.7
−7.8	0.315	12.8	−6.4	0.371	127	01111111	−4.7	0.450	12.8
−7.9	0.311	12.9	−6.5	0.367	126	01111110	−4.8	0.445	12.9
−8.0	0.308	13.0	−6.6	0.362	125	01111101	−4.9	0.440	13.0
−8.1	0.304	13.1	−6.7	0.358	124	01111100	−5.0	0.435	13.1
−8.2	0.301	13.2	−6.8	0.354	123	01111011	−5.1	0.430	13.2
−8.3	0.297	13.3	−6.9	0.350	122	01111010	−5.2	0.425	13.3
−8.4	0.294	13.4	−7.0	0.346	121	01111001	−5.3	0.420	13.4
−8.5	0.291	13.5	−7.1	0.342	120	01111000	−5.4	0.415	13.5
−8.6	0.287	13.6	−7.2	0.338	119	01110111	−5.5	0.410	13.6
−8.7	0.284	13.7	−7.3	0.334	118	01110110	−5.6	0.406	13.7
−8.8	0.281	13.8	−7.4	0.331	117	01110101	−5.7	0.401	13.8
−8.9	0.278	13.9	−7.5	0.327	116	01110100	−5.8	0.396	13.9
−9.0	0.274	14.0	−7.6	0.323	115	01110011	−5.9	0.392	14.0
−9.1	0.271	14.1	−7.7	0.319	114	01110010	−6.0	0.387	14.1
−9.2	0.268	14.2	−7.8	0.316	113	01110001	−6.1	0.383	14.2
−9.3	0.265	14.3	−7.9	0.312	112	01110000	−6.2	0.378	14.3
−9.4	0.262	14.4	−8.0	0.308	111	01101111	−6.3	0.374	14.4
−9.5	0.259	14.5	−8.1	0.305	110	01101110	−6.4	0.370	14.5
−9.6	0.256	14.6	−8.2	0.301	109	01101101	−6.5	0.366	14.6
−9.7	0.253	14.7	−8.3	0.298	108	01101100	−6.6	0.361	14.7
−9.8	0.250	14.8	−8.4	0.295	107	01101011	−6.7	0.357	14.8
−9.9	0.247	14.9	−8.5	0.291	106	01101010	−6.8	0.353	14.9
−10.0	0.245	15.0	−8.6	0.288	105	01101001	−6.9	0.349	15.0
−10.1	0.242	15.1	−8.7	0.285	104	01101000	−7.0	0.345	15.1
−10.2	0.239	15.2	−8.8	0.281	103	01100111	−7.1	0.341	15.2
−10.3	0.236	15.3	−8.9	0.278	102	01100110	−7.2	0.337	15.3
−10.4	0.234	15.4	−9.0	0.275	101	01100101	−7.3	0.333	15.4
−10.5	0.231	15.5	−9.1	0.272	100	01100100	−7.4	0.330	15.5
−10.6	0.228	15.6	−9.2	0.269	99	01100011	−7.5	0.326	15.6
−10.7	0.226	15.7	−9.3	0.266	98	01100010	−7.6	0.322	15.7
−10.8	0.223	15.8	−9.4	0.263	97	01100001	−7.7	0.318	15.8
−10.9	0.220	15.9	−9.5	0.260	96	01100000	−7.8	0.315	15.9
−11.0	0.218	16.0	−9.6	0.257	95	01011111	−7.9	0.311	16.0
−11.1	0.215	16.1	−9.7	0.254	94	01011110	−8.0	0.308	16.1
−11.2	0.213	16.2	−9.8	0.251	93	01011101	−8.1	0.304	16.2
−11.3	0.211	16.3	−9.9	0.248	92	01011100	−8.2	0.301	16.3
−11.4	0.208	16.4	−10.0	0.245	91	01011011	−8.3	0.297	16.4

APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes (Continued)

TP3075/6 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
−11.5	0.206	16.5	−10.1	0.242	90	01011010	−8.4	0.294	16.5
−11.6	0.203	16.6	−10.2	0.239	89	01011001	−8.5	0.290	16.6
−11.7	0.201	16.7	−10.3	0.237	88	01011000	−8.6	0.287	16.7
−11.8	0.199	16.8	−10.4	0.234	87	01010111	−8.7	0.284	16.8
−11.9	0.196	16.9	−10.5	0.231	86	01010110	−8.8	0.281	16.9
−12.0	0.194	17.0	−10.6	0.229	85	01010101	−8.9	0.277	17.0
−12.1	0.192	17.1	−10.7	0.226	84	01010100	−9.0	0.274	17.1
−12.2	0.190	17.2	−10.8	0.223	83	01010011	−9.1	0.271	17.2
−12.3	0.188	17.3	−10.9	0.221	82	01010010	−9.2	0.268	17.3
−12.4	0.185	17.4	−11.0	0.218	81	01010001	−9.3	0.265	17.4
−12.5	0.183	17.5	−11.1	0.216	80	01010000	−9.4	0.262	17.5
−12.6	0.181	17.6	−11.2	0.213	79	01001111	−9.5	0.259	17.6
−12.7	0.179	17.7	−11.3	0.211	78	01001110	−9.6	0.256	17.7
−12.8	0.177	17.8	−11.4	0.209	77	01001101	−9.7	0.253	17.8
−12.9	0.175	17.9	−11.5	0.206	76	01001100	−9.8	0.250	17.9
−13.0	0.173	18.0	−11.6	0.204	75	01001011	−9.9	0.247	18.0
−13.1	0.171	18.1	−11.7	0.201	74	01001010	−10.0	0.244	18.1
−13.2	0.169	18.2	−11.8	0.199	73	01001001	−10.1	0.242	18.2
−13.3	0.167	18.3	−11.9	0.197	72	01001000	−10.2	0.239	18.3
−13.4	0.165	18.4	−12.0	0.195	71	01000111	−10.3	0.236	18.4
−13.5	0.163	18.5	−12.1	0.192	70	01000110	−10.4	0.233	18.5
−13.6	0.162	18.6	−12.2	0.190	69	01000101	−10.5	0.231	18.6
−13.7	0.160	18.7	−12.3	0.188	68	01000100	−10.6	0.228	18.7
−13.8	0.158	18.8	−12.4	0.186	67	01000011	−10.7	0.225	18.8
−13.9	0.156	18.9	−12.5	0.184	66	01000010	−10.8	0.223	18.9
−14.0	0.154	19.0	−12.6	0.182	65	01000001	−10.9	0.220	19.0
−14.1	0.153	19.1	−12.7	0.180	64	01000000	−11.0	0.218	19.1
−14.2	0.151	19.2	−12.8	0.178	63	00111111	−11.1	0.215	19.2
−14.3	0.149	19.3	−12.9	0.175	62	00111110	−11.2	0.213	19.3
−14.4	0.147	19.4	−13.0	0.173	61	00111101	−11.3	0.210	19.4
−14.5	0.146	19.5	−13.1	0.171	60	00111100	−11.4	0.208	19.5
−14.6	0.144	19.6	−13.2	0.170	59	00111011	−11.5	0.206	19.6
−14.7	0.142	19.7	−13.3	0.168	58	00111010	−11.6	0.203	19.7
−14.8	0.141	19.8	−13.4	0.166	57	00111001	−11.7	0.201	19.8
−14.9	0.139	19.9	−13.5	0.164	56	00111000	−11.8	0.199	19.9
−15.0	0.138	20.0	−13.6	0.162	55	00110111	−11.9	0.196	20.0
−15.1	0.136	20.1	−13.7	0.160	54	00110110	−12.0	0.194	20.1
−15.2	0.134	20.2	−13.8	0.158	53	00110101	−12.1	0.192	20.2
−15.3	0.133	20.3	−13.9	0.156	52	00110100	−12.2	0.190	20.3
−15.4	0.131	20.4	−14.0	0.155	51	00110011	−12.3	0.188	20.4
−15.5	0.130	20.5	−14.1	0.153	50	00110010	−12.4	0.185	20.5
−15.6	0.128	20.6	−14.2	0.151	49	00110001	−12.5	0.183	20.6
−15.7	0.127	20.7	−14.3	0.149	48	00110000	−12.6	0.181	20.7
−15.8	0.125	20.8	−14.4	0.148	47	00101111	−12.7	0.179	20.8
−15.9	0.124	20.9	−14.5	0.146	46	00101110	−12.8	0.177	20.9
−16.0	0.123	21.0	−14.6	0.144	45	00101101	−12.9	0.175	21.0
−16.1	0.121	21.1	−14.7	0.143	44	00101100	−13.0	0.173	21.1
−16.2	0.120	21.2	−14.8	0.141	43	00101011	−13.1	0.171	21.2
−16.3	0.118	21.3	−14.9	0.139	42	00101010	−13.2	0.169	21.3
−16.4	0.117	21.4	−15.0	0.138	41	00101001	−13.3	0.167	21.4
−16.5	0.116	21.5	−15.1	0.136	40	00101000	−13.4	0.165	21.5
−16.6	0.114	21.6	−15.2	0.135	39	00100111	−13.5	0.163	21.6
−16.7	0.113	21.7	−15.3	0.133	38	00100110	−13.6	0.161	21.7
−16.8	0.112	21.8	−15.4	0.132	37	00100101	−13.7	0.160	21.8
−16.9	0.110	21.9	−15.5	0.130	36	00100100	−13.8	0.158	21.9

APPENDIX I. COMBO II 0 dBm0 Levels vs. Gain Codes (Continued)

TP3075/6 TX 0 dBm0		TX Gain, dB	TP3070/1 TX 0 dBm0		Decimal Code	Binary Code	Receive 0 dBm0		RX Atten, dB
dBm (600Ω)	Vrms		dBm (600Ω)	Vrms			dBm (600Ω)	Vrms	
−17.0	0.109	22.0	−15.6	0.129	35	00100011	−13.9	0.156	22.0
−17.1	0.108	22.1	−15.7	0.127	34	00100010	−14.0	0.154	22.1
−17.2	0.107	22.2	−15.8	0.126	33	00100001	−14.1	0.152	22.2
−17.3	0.106	22.3	−15.9	0.124	32	00100000	−14.2	0.151	22.3
−17.4	0.104	22.4	−16.0	0.123	31	00011111	−14.3	0.149	22.4
−17.5	0.103	22.5	−16.1	0.121	30	00011110	−14.4	0.147	22.5
−17.6	0.102	22.6	−16.2	0.120	29	00011101	−14.5	0.146	22.6
−17.7	0.101	22.7	−16.3	0.119	28	00011100	−14.6	0.144	22.7
−17.8	0.100	22.8	−16.4	0.117	27	00011011	−14.7	0.142	22.8
−17.9	0.098	22.9	−16.5	0.116	26	00011010	−14.8	0.141	22.9
−18.0	0.097	23.0	−16.6	0.115	25	00011001	−14.9	0.139	23.0
−18.1	0.096	23.1	−16.7	0.113	24	00011000	−15.0	0.137	23.1
−18.2	0.095	23.2	−16.8	0.112	23	00010111	−15.1	0.136	23.2
−18.3	0.094	23.3	−16.9	0.111	22	00010110	−15.2	0.134	23.3
−18.4	0.093	23.4	−17.0	0.109	21	00010101	−15.3	0.133	23.4
−18.5	0.092	23.5	−17.1	0.108	20	00010100	−15.4	0.131	23.5
−18.6	0.091	23.6	−17.2	0.107	19	00010011	−15.5	0.130	23.6
−18.7	0.090	23.7	−17.3	0.106	18	00010010	−15.6	0.128	23.7
−18.8	0.089	23.8	−17.4	0.105	17	00010001	−15.7	0.127	23.8
−18.9	0.088	23.9	−17.5	0.103	16	00010000	−15.8	0.125	23.9
−19.0	0.087	24.0	−17.6	0.102	15	00001111	−15.9	0.124	24.0
−19.1	0.086	24.1	−17.7	0.101	14	00001110	−16.0	0.122	24.1
−19.2	0.085	24.2	−17.8	0.100	13	00001101	−16.1	0.121	24.2
−19.3	0.084	24.3	−17.9	0.099	12	00001100	−16.2	0.120	24.3
−19.4	0.083	24.4	−18.0	0.098	11	00001011	−16.3	0.118	24.4
−19.5	0.082	24.5	−18.1	0.096	10	00001010	−16.4	0.117	24.5
−19.6	0.081	24.6	−18.2	0.095	9	00001001	−16.5	0.116	24.6
−19.7	0.080	24.7	−18.3	0.094	8	00001000	−16.6	0.114	24.7
−19.8	0.079	24.8	−18.4	0.093	7	00000111	−16.7	0.113	24.8
−19.9	0.078	24.9	−18.5	0.092	6	00000110	−16.8	0.112	24.9
−20.0	0.077	25.0	−18.6	0.091	5	00000101	−16.9	0.110	25.0
−20.1	0.076	25.1	−18.7	0.090	4	00000100	−17.0	0.109	25.1
−20.2	0.076	25.2	−18.8	0.089	3	00000011	−17.1	0.108	25.2
−20.3	0.075	25.3	−18.9	0.088	2	00000010	−17.2	0.107	25.3
−20.4	0.074	25.4	−19.0	0.087	1	00000001	−17.3	0.105	25.4
OFF	OFF	OFF	OFF	OFF	0	00000000	OFF	OFF	OFF

High Voltage Protection Techniques with TP3210 Subscriber Line Interface Module

National Semiconductor
Application Note 639
Duncan Bremner
Telecom Products

1.0 INTRODUCTION

The objective of this application note is to demonstrate a solution which removes some of the traditional accuracy constraints on the protection components without impacting performance. It then goes on to develop protection schemes which are completely resettable. The note begins with a brief discussion of the protection problems associated with subscriber line interface circuits, and outlines the basic requirements which these devices meet. This is followed by a discussion of the National Semiconductor **S**ubscriber **L**ine **I**nterface **M**odule (**SLIM™**) device, demonstrating the unique advantages this part has over the more conventional solutions. Finally, two protection systems are analyzed in detail, and the measured performance of these is shown. These results, combined with the information contained in the note, will allow a linecard designer to completely specify the protection components required to meet the desired performance level.

2.0 SLIC PROTECTION PROBLEMS

To understand the problems in protecting line circuits, a basic review of the traditional protection layout is useful in appreciating the direction in which protection technology is moving. The line interface protection networks are traditionally split into primary, secondary, and tertiary protection components. *Figure 1* shows the layout of a conventional switch protection scheme for both subscriber and trunk lines exiting the central office. The secondary and tertiary levels are normally combined at the linecard. The protection levels are typically 1000V peak after primary protection and around 80V peak after secondary protection. This value is, of course, dependent on the clamp voltage of the shunt protection element used in the secondary circuit.

2.1 Primary Protection

The primary components are responsible for handling the large disturbances such as a lightning strike close to the central switch location. They are normally situated on the main distribution frame (MDF), where the subscriber cables enter the office. All disturbing currents arrested by the primary protection components are directed away from the main body of the switch, via a separate protection ground connection and are discharged harmlessly to earth. A typical implementation of primary protection would employ gas discharge tubes (GDT), which limit the voltages exiting the MDF to less than 1000V peak. The benefit of positioning primary protection on the MDF is twofold.

Firstly, it avoids having large transient currents flowing in the office wiring. This ensures that the current rating of the wiring is never exceeded, and also ensures that the voltages present after the MDF are relatively low (less than 1000V peak), which avoids any damaging secondary arcing between adjacent points inside the office. Secondly, by ensuring that the energy is shunted safely away to earth, the operation of the majority of the switch remains unaffected. This is especially important when serving large rural areas with a high incidence of thunderstorms.

2.2 Secondary Protection

The secondary protection components reside either on the linecard itself, or immediately on the backplane adjacent to the card connector, and are designed to handle the residual current which passes the primary protection. This consists of power cross currents and power induction products which are of sufficiently low voltage to pass through the primary protectors. The secondary protection schemes employ two separate elements to protect the sensitive line card components. Firstly, a series element which limits the current flowing onto the linecard, and secondly, a shunt element which limits the voltage. This shunt element can be a simple bridge rectifier connected between the battery terminals which shunts the current to either battery or ground, or more commonly, an active thyristor device which shunts the current to protection ground only. This device, when triggered, returns transient energy either to the local protection ground connection at the linecard or, preferably, returns it to a remote protection ground, usually the same as the protec-

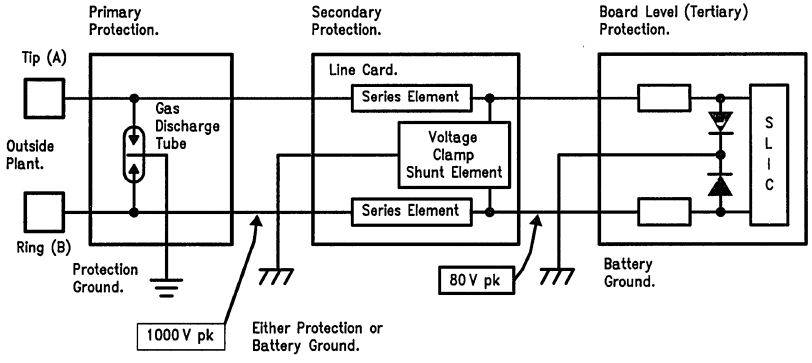

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FIGURE 1. Conventional Switch Protection Arrangement

tion ground used on the MDF. When using remote grounds, this can give rise to 1000V differences between Battery ground and the protection ground. This configuration is popular in North America and specialized knowledge and design techniques must be employed to cope with this since the voltage stress on the line card components is high. The **SLIM** device is one of the few devices which can meet this requirement and thus is especially useful for applications using separate ground systems.

While providing the necessary protection, the protection components must not degrade the transmission characteristics in any way during normal speech and signaling modes. It is this area that compromises between good protection and meeting specifications are frequently made, but these are avoided when using the **SLIM** device.

3.0 PROTECTION COMPROMISES

There are two areas which affect the selection of the protection components used. These are the DC voltage headroom requirements for the electronic SLICs to operate correctly, and the Longitudinal Balance requirements imposed on the circuit by the transmission specifications.

3.1 DC Headroom Limitations

The DC headroom implications are shown in *Figure 2.* In order for an electronic SLIC to function correctly, a certain voltage headroom is required for linear operation. This means that there is an interaction between feeding line current to the maximum long loop requirement, and allowing sufficient headroom for SLIC amplifer operation. From *Figure 2*, it can be seen that line current flows from the amplifier via Rprotect, the series protection elements. If the values of these are not carefully chosen, the voltage headroom may be impacted, and hence maximum long loop requirements compromised.

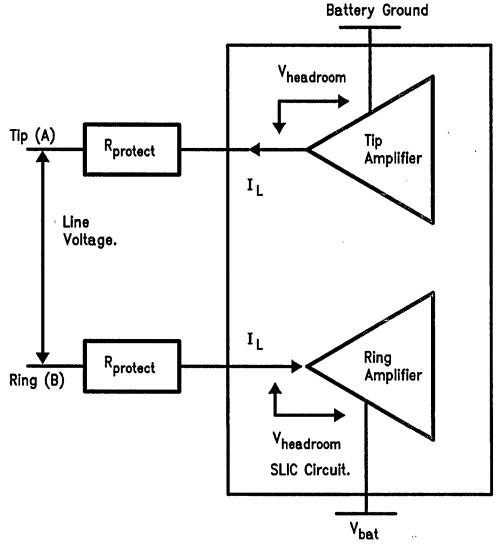

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FIGURE 2. DC Headroom Limitations

The longitudinal balance tests are probably the most stringent requirements placed on the front end of the line interface circuit, and are normally directly affected by the selection of the protection resistors. In order to meet these requirements, the matching of resistance from the Tip(A) and Ring(B) legs of the circuit to ground must typically be better than 1%. In most circuits, the burden of this precise matching requirements is placed directly on the series protection elements. This results in escalating costs for these components, but with the **SLIM**, these precise requirements are eliminated.

However, the problems of DC headroom and longitudinal balance can be eliminated if resourceful design techniques are employed to desensitise the series protection elements from impacting the feeding law. These techniques are employed in the new National Semiconductor **SLIM** which, by optimal use of complementary technologies, removes much of the restrictions on accuracy requirements from the protection components.

3.3 SLIM Protection

The National Semiconductor **SLIM** device is a completely new concept in subscriber connections to the central switch which uses a mixture of technologies to attain an optimal performance/cost ratio. This ratio is not just in the component cost required to implement the SLIC function, but the total manufacturing cost. The **SLIM** device is designed to minimize the number and cost of external components resulting in a substantial cost saving on a complete line circuit basis. This system cost reduction philosophy is particularly prevalent in the way the protection scheme is implemented. The tolerances for the protection components are orders of magnitude less than normally required to attain the performance levels which this part achieves, with a corresponding reduction in the cost of these components. A working knowledge of the principles employed to allow this will now be presented, followed by some results showing how insensitive the technique is to changes and mismatches in the protection components.

Conventional protection schemes, outlined in *Figure 1*, separate the linecard protection into secondary protection and tertiary protection. Using the **SLIM** approach, the module itself carries the tertiary protection components, and the series elements of the secondary protection are included in a sensing loop which cancels any errors which may arise due to poor matching of the resistance values as shown in *Figure 3.* The benefit of this approach is that the burden of matching these components is removed to a large degree from the board manufacturer.

This approach is only possible using a careful mix of technologies which enable the voltage ratings at the primary/secondary interface to be met. This is achieved by manufacturing SLIM on a thick film hybrid module which will stand in excess of 1000V peak without failing. By using these thick film techniques, and by accurately trimming, a very high degree of longitudinal rejection can be maintained. Typical figures of 75dB are measured at the final test stage of the completed module using 100Ω, 1% protection resistors.

Since the module employs a control loop to guarantee the longitudinal balance of the system, it can also synthesize the longitudinal terminating resistance on each leg of the subscriber line, i.e., the resistance from each leg to ground

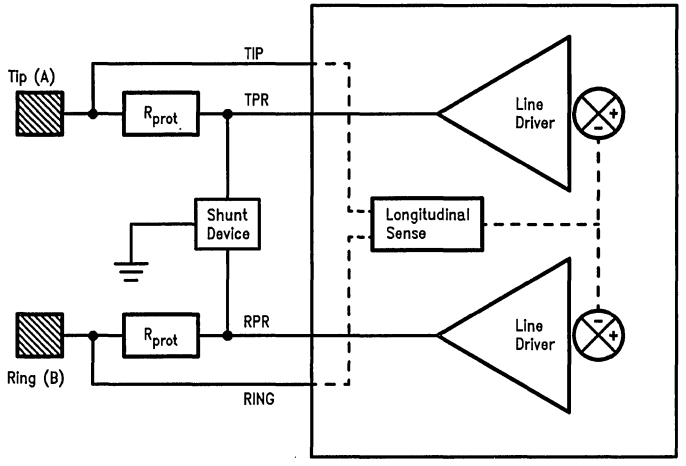

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FIGURE 3. SLIM Protection Arrangement

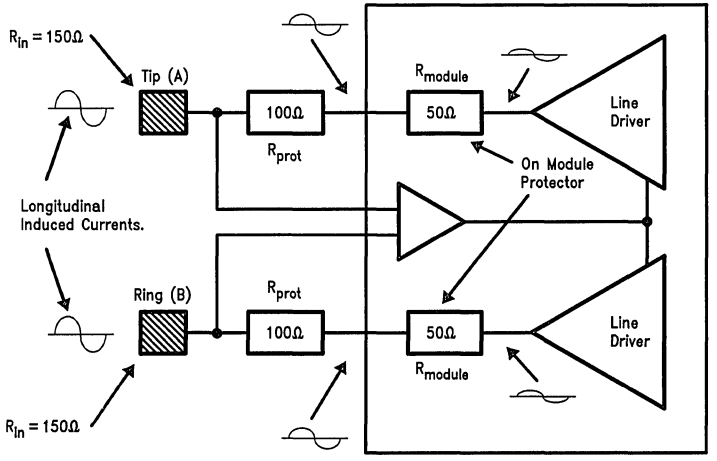

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FIGURE 4. Synthesized Longitudinal Resistance

in response to longitudinal signals. The advantage of synthesizing this resistance is that the control of longitudinal voltages appearing at the line terminals is much tighter, maintaining a more consistent longitudinal balance figure. Secondly, and more importantly, by carefully matching the synthesized resistance with the physical resistance consisting of the on module resistance and the external protection resistance, an improvement in signal handling capability in the presence of high levels of longitudinal current can be achieved. *Figure 4* shows this graphically.

Referring to the conventional protection layout in *Figure 1,* it is important that the module protection is sufficient to withstand the currents which are allowed to pass through the secondary shunt protection device. Using the **SLIM**, the module has series protection elements incorporated in the design which are capable of surviving in excess of 80V each leg. The applications advantage of this is that the shunt protector can be directly connected across the output of the **SLIM** device at the TPR and RPR terminals.

Overall the **SLIM** device has been designed with the end application in mind. The optimum mix of technologies has been used to achieve the most cost effective solution to the OEM, not just in component cost, but also in the external components and manufacturing costs. This philosophy can be seen in the way in which the protection function is partitioned, enabling the user to achieve previously unattainable levels of performance from wide tolerance components. It is this systems approach to the problem which enables **SLIM** users to obtain a competitive advantage compared with conventional solutions to the protection problem. The remaining sections of this applications note will deal with the results of laboratory tests, followed by an examination of the various protection options available with this versatile device, outlining the strengths and weakness of the different solutions.

4.0 LABORATORY MEASUREMENTS

The previous sections have concentrated on the effectiveness of the **SLIM** device in meeting longitudinal requirements while incorporating very loose tolerance protection components. However, as yet there have been no quantitive measure of the performance which can be attained with the part. The results which are presented here were measured under laboratory conditions using a Wilcom T207E Longitudinal Balance Test Set, measured in accordance with IEEE 455-1976 Recommendations. The tests were measured on typical devices from standard production runs, and are representative of the results which can be expected from a **SLIM** based line circuit.

The tests were designed to investigate the behavior of the part under 3 different line conditions, while varying the protection resistances, $R_{protect}$. The graphs show results for 3 different test frequencies to allow appreciation of the sensitivity of the results. The devices were tested for sensitivity to the absolute value of resistors (both resistors matched to within 0.1%) and then the mismatch sensitivity between the two protection resistors, one resistor being held constant and the other was reduced in value. This second test was carried out with the fixed resistor having the values of 120Ω, 100Ω, and 80Ω, the other leg having resistors 20% different.

The results presented below are the worst case results of the devices tested. The measurements were made at 0 mA, 20 mA, and 42 mA line current. These correspond to on-hook, 1900Ω loop resistance, and 750Ω loop resistance.

4.1 Absolute Value Sensitivity

Figures 5, 6 and *7* show the results of Longitudinal Balance against Resistor Value of Rprotect both resistors matched to within 0.1%. These results are measured at 62 Hz, 1000 Hz, and 3400 Hz for the 3 stipulated line conditions.

The overall trend of these results indicate that the Longitudinal Balance is better than 60 dB for all values of protection resistor between 90Ω and 120Ω. Values substantially greater than 120Ω are not recommended since these will reduce the operating voltage headroom of the output amplifiers as explained earlier.

4.2 Matching Sensitivity

The tests for the matching sensitivity were carried out in a similar fashion except the resistor in one of the legs was held constant. The results recorded in *Figures 8, 9* and *10* indicate the worst case result between the two legs. The results shown in *Figure 8* illustrate the trade-off between resistor matching ratio and the longitudinal balance which can be achieved for I_{loop} = 0 mA, while *Figures 9* and *10* show I_{loop} = 20 mA and 42 mA respectively. This is shown for fixed resistors of 120Ω, 100Ω, and 80Ω while the other leg was varied. The graphs show the results for 20% mismatch between legs. From the graphs, it can be seen that the longitudinal balance achieved using very loose tolerance parts is very high. If tighter specifications are required, slightly closer tolerance resistors may be specified, but these are still cheaper than the high tolerance devices required to meet these specifications using conventional line circuits. It is important to note that during all these tests,

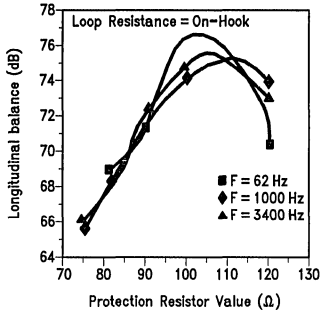

FIGURE 5. Longitudinal Balance vs Resistor Value

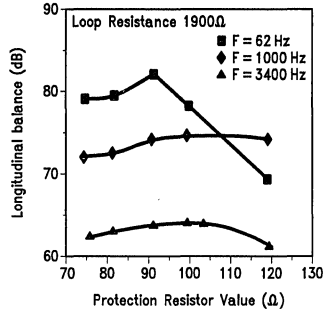

FIGURE 6. Longitudinal Balance vs Resistor Value

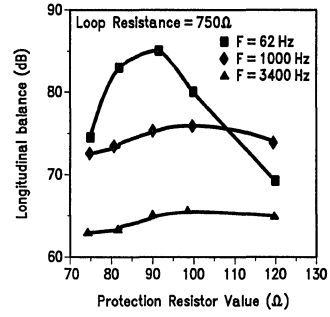

FIGURE 7. Longitudinal Balance vs Resistor Value

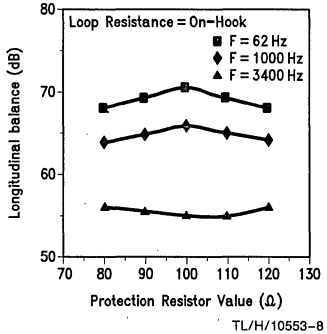

FIGURE 8. Longitudinal Balance for 20% Mismatch

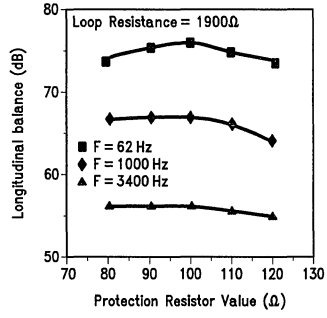

FIGURE 9. Longitudinal Balance for 20% Mismatch

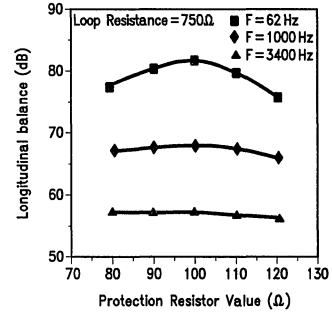

FIGURE 10. Longitudinal Balance for 20% Mismatch

the module passed all the longitudinal capability tests, easily handling the 21 mArms per leg specified in the Datasheet.

Summarizing the results presented in this section, the absolute value of the resistors can be in the range 80Ω to 120Ω, with a matching tolerance up to 20%. However, in order to meet the more stringent requirements such as Bellcore, and to cope with the long term effects of Lightning and power cross, the resistors should be 100Ω, ±5%. This will ensure meeting the requirements at end of life. These results now enable protection options to be examined in detail, and with an understanding of the capabilities of the **SLIM** device, a prediction of the effectiveness of these options can be made.

5.0 PROTECTION OPTIONS

These options can be split into roughly two areas, which follow slightly different philosophies regarding the purpose of protection. These are Fusible, or manual resettable systems, and Auto-resetting systems. Both of these consist of the same elements. The difference between these is the type of series protection element used. Before discussing the differences in detail, a study of the individual protection components is worthwhile.

5.1 Shunt Protection Devices

The shunt protection device in this application can be any one of three configurations. *Figure 11* shows the least expensive shunt protector available for the application. It consists of a bridge rectifier connected across the subscriber wires, and returning the fault current to either the battery ground or the battery supply, dependent on the polarity of the fault current. This system is very effective at protecting the line circuits since the voltage transitions are restricted to approximately a forward diode voltage beyond the supply rails, however, the injection of large fault transients onto the battery supply is not desirable for many administrations. This is particularly a problem when the negative battery potential is generated using a switch mode power supply, which while capable of sourcing large currents, is incapable of sinking current. A fault condition which dumps substantial current into the battery could increase the battery potential causing damage. If this protection system does prove adequate for the application, then the required specification for the diode bridge is 20A surge capability (2A continuous), 100V rating.

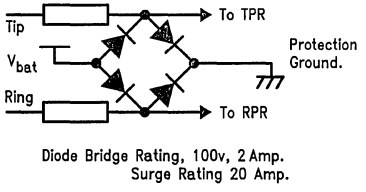

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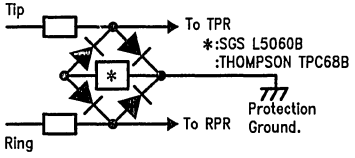
FIGURE 11. Low Cost Shunt Protector

The second shunt protection configuration, *Figure 12*, is designed to avoid dumping the fault transients into the office battery supply, thus ensuring that the battery potential remains unaffected during a fault condition. In this circuit, the positive going transients are returned to battery ground connection as in the diode bridge, but the negative transients are passed to a transient surge protector.

This 2 terminal device operates as a voltage/current sensitive thyristor. When the voltage appearing at the terminals of the device exceed the zener voltage (V_Z) rating of the device, the unit enters a voltage clamp region. If the fault voltage continues to rise, the current into the shunt protector will rise correspondingly through the series protection element, until the breakover current threshold (I_{bo}) is exceeded. At this point the device fires, causing the voltage across the device to collapse, and returning all the current to the battery ground terminal. The device remains in this state until the current has reduced to below the holding current of the device, whereupon the protector resets itself.



TL/H/10553–12

FIGURE 12. Protection Using a Shunt Suppressor Device

To aid understanding, the V-I characteristics are shown in *Figure 13*, highlighting the important features on the characteristics. This diagram also shows the characteristics of the two basic types of suppressor; namely symmetric and asymmetric types. The Asymmetric (shown dotted), have the advantage of a forward diode characteristic in one direction which reduces the power dissipated by the SLIC during a fault condition.

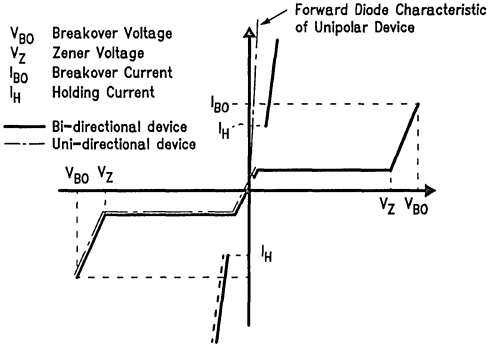


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FIGURE 13. Shunt Suppressor V-I Characteristic

The final shunt protection scheme, *Figure 14*, is a development of the circuit shown in *Figure 12*. In this circuit, the diode bridge is discarded, and the two shunt components are replaced by a single device. This 3 terminal device protects against faults occurring between the two subscriber wires and to ground. These devices are slightly more expensive than the previous option, but are competitive when the savings in board area and assembly costs are taken into account.

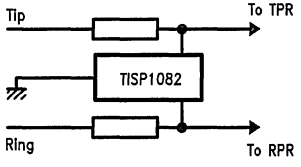

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FIGURE 14. Terminal Shunt Protector

For use with the **SLIM** module, the ideal type of shunt protector is the unipolar type since this limits the potential to within a forward diode voltage (V_{BE}) of the battery ground potential. The advantage of this is a limitation of the power dissipation on module during a fault condition. The breakover voltage should be 85V or less, but the breakover current is not important for correct **SLIM** operation. The choice of 2 or 3 terminal can be made on a purely financial basis of whether the addition of a diode bridge circuit increases the cost over the 3 terminal device.

5.2 Series Protection Elements

To complete the protection function, a method of limiting the current into the shunt device is required, and this is the task of the series elements. These elements, one in each of the subscriber wires operate by, in the case of fusible systems, interrupting the current flow after it exceeds a predefined value, or, in the case of auto-resetting systems, by reducing the current level to a safe level when hot. To ensure that the choices are not constrained, the strengths and weaknesses of both manual and auto resetting systems are put forward, thus allowing the designer to appraise both systems and choose the most suitable one.

The choice of series protector must be made with the protection specifications in mind. Many specifications require that the protection components must withstand a particular level of disturbance without damage. Usually it is these which govern the choice of series element. The principle factors affecting the choice are the power dissipation of the device during a fault condition, and the rupturing current in the case of fusible systems. However, if there is a time constraint placed on the test conditions, the thermal mass of the device must be incorporated into the calculations, though this can often be done by referring to the manufacturers datasheet which contains this information.

The choice between a fusible and a resettable system is one which is often governed by the specifications, usually because the resettable systems cannot achieve the long term balance requirements. As has been shown in the results section previously, this constraint does not apply to users of the **SLIM** device, thus opening new opportunities to users who desire auto-resetting protection without the compromise on balance performance.

5.3 Fusible (Manual Resettable) Systems

The benefit of employing a manual resettable system is that if a fault occurs on a particular line, after the protection has been fired, the line is disconnected from the switch until the fault is cleared and the system reset. This means that the remainder of the switch can function completely, without the board heating problems etc. which may occur using other protection systems. However, the disadvantage of the manual system is the requirement for human intervention to replace or reset the line protection. This is especially important in a distributed switch system where the protection circuits are not all in the same location.

Figure 15 shows the schematic for a fusible protection circuit. The series elements can be fuses, resistors, or circuit breakers which are triggered if the rupturing current of the device is exceeded. For the **SLIM** device, the maximum current which the element must pass for correct operation is the maximum line feed current plus the worst case longitudinal current which may appear on line. However, many authorities require that the protection elements can withstand a short term power cross for a finite period of time, a typical

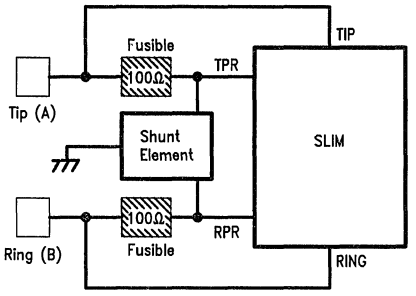

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FIGURE 15. Fusible Resistor Implementation

example may be 200 Vrms, from a generator impedance of 150Ω for a period of 5 seconds. The reason for this is to ensure that the protection systems do not trip on short term faults caused by a transient power cross situation, but survive long enough for the electricity supply authority circuit breakers to respond to the fault, thus avoiding a false or unnecessary failure.

Until now, the manual resettable or fusible systems have been most popular in the industry since the matching accuracy of the series elements can be carefully controlled to ensure good balance. The problem in the future using this type of protection is the expansion in distributed switching systems employing local street furniture. The costs of replacing protection in these locations is much greater, but it is argued that the incidence of faults will also reduce due to the shorter line lengths. In order to reduce this cost to a minimum, and improve the time taken to reinstate service to the client, auto resetting systems can be more effective, and these are described in the following section.

5.4 Auto-Resetting Systems

The Auto-Resettable protection system has always been attractive to line card designers. The inherent advantage is the system guards against any fault which may occur on the line, and after occurence, resets automatically, without any requirement for human intervention. Unfortunately, the compromises to achieve this were traditionally too great to warrant the change to auto systems. With the advent of the **SLIM**, these compromises are not necessary, and the implementation of automatic protection becomes a realistic possibility irrespective of the severity of the longitudinal balance specification.

The basic principle behind these protection schemes is the use of a PTC device as the series element in the secondary protection circuit. During a fault condition, this device dissipates power which causes self heating. The temperature increase of the device causes the resistance to increase, thus regulating the current flow. Eventually, thermal equilibrium is reached, and this state is held until the fault condition is removed. The device then cools and normal service is re-established. The choice of the PTC device is relatively painless once the critical parameters are decided, but to understand the impact of these parameters, an appreciation of the operation and construction of the device is useful.

6.0 PTC CONSTRUCTION AND OPERATION

Positive temperature coefficient devices come in a variety of forms depending on the application required. For the line card protection application, the devices required are designed to act as switching elements with a carefully defined,

abrupt switching characteristic. The most common method of implementing the switching function is to use thermistors. The operation of these is now discussed.

6.1 Thermistors

Switching type PTC thermistors are made from semiconducting barium titanate ceramic material. This material exhibits a temperature-resistance characteristic as shown in *Figure 16.* Over the lower portion of their characteristic, the thermistor resistance is low and relatively constant (a slight negative coefficient is present at low temperatures due to the intrinsic negative temperature coefficient from the semiconducting material). As the temperature is raised above the Curie point, the magnetic domains in the material realign themselves, and the material becomes more resistive until eventually the material approaches an insulator. In a switching type of device, this action is designed to take place abruptly over a 10–15°C temperature change. Over this range, the resistance of the thermistor changes by five or six orders of magnitude, from say 10Ω to 1 MΩ.

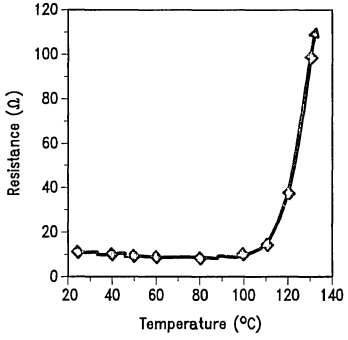

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FIGURE 16. Thermistor Temperature-Resistance

If, instead of using external temperature as the heating source, current flowing through the device is used, the traditional V-I characteristic for this type of device can be measured, see *Figure 17.* This curve has two distinct regions which are important for the application.

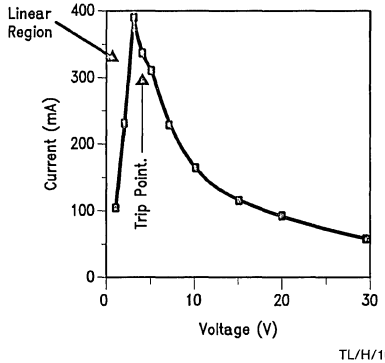

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FIGURE 17. V-I Thermistor Characteristics

First the linear region. This is the area of normal operation where the device does not exhibit any switching behavior. If current value less than the value of the trip current, It, is flowing through the device, the temperature rise of the thermistor is insufficient to trip the device. If however, the current is increased above the trip level, the temperature rise is sufficient for the resistance to increase. To ensure correct operation in the application, the thermistor chosen must be rated so that the Trip Point is never exceeded during normal operation at the maximum ambient temperature.

6.2 Maximum Ratings

When using thermistors it is imperative never to exceed the manufacturers ratings for the device. These ratings give the maximum voltage and current which the device is capable of switching. The voltage rating is principally defined by the thickness and resistivity of the device. The switching current rating is very important since exceeding this value will cause the device to fracture. This is caused by the physical properties of the material which have an intrinsic energy-time product capacity. If attempts are made to dissipate an excessive amount of energy, the differential expansion inside the device due to local heating set up large stresses in the brittle ceramic material which consequently shears and fractures. In general the larger the cross sectional area of the device, the greater the switching current can be handled, and this parameter is one of the most crucial in selecting the correct device.

If these limits are not exceeded, the resistance value of the thermistor is very predictable, and will return to the initial starting value repeatedly, independent of the number of switching cycles the device has undergone. In lab tests, a thermistor was repeatedly hit with a 30 second burst of 250 Vrms mains voltage, sufficient to stress it at the maximum ratings, then allowed to cool for 5 minutes, after which a resistance measurement was made. This cycle was repeated over 450 times, and the results logged. The resistance of the device did not vary more than ±0.5% over this test.

Hopefully, this is sufficient to dispel the myth that thermistors are unstable devices and are not repeatably resettable after undergoing numerous switching operations. Now that the basic operating principles of thermistors have been explained, the limitations from an applications point of view can be appreciated, and put into context.

6.3 Specifying Thermistors

As outlined in the above section, thermistors have five basic parameters which must be specified on ordering. These are:

1. Operating temperature range. Normally for telecom equipment this is 0°C to +70°C. This does not need to take the temperature rise due to self heating into account.
2. Maximum operating current (non switch). This is normally in the range 80–100 mA, for most telecom applications. It is important to rate this parameter at the maximum operating ambient temperature.
3. Maximum voltage rating. This parameter is set by the voltage which the device must withstand when the source resistance of the generator is zero. This is important when the resistance of the device increases to a high value, (much greater than the source resistance of the generator), when the rating should be equal to or exceed the test voltage.

4. Maximum current capability. This parameter must be chosen dependant on the peak cold current the device will be required to handle at the instant a fault occurs.
5. Finally, the cold resistance of the device. This will be defined to a large extent by the previous parameters, but if a choice exists, should be chosen to be as large as possible in order to increase switching time, and reduce the currents injected into the line card during a fault.

7.0 WORKED EXAMPLE 1

Take the case of a linecard which must survive a mains cross fault of 250 Vrms for 15 minutes, from a source resistance of 30Ω, after which the part must reset to normal operation. Assume that the longitudinal specification must exceed 50 dB across the frequency band 50 Hz to 3400 Hz. Operating temperature range 0°C to +70°C.

First, referring to the performance graphs in the measurements section, it can be seen that the absolute value, and the matching requirements to meet this spec are very loose, so we have a relatively free choice for the value of device we eventually choose.

1. Temperature Operating Range: 0°C to +70°C.
2. Operating current. The **SLIM** device has a maximum feed current of 43 mA. Modulating this, the worst case longitudinal current, say 20 mArms, gives maximum operating current of 48 mArms. Therefore require a thermistor which must be able to handle 48 mArms at the maximum operating temperature (70°C). Note the use of RMS currents since we are interested in the heating effect of the current.
3. Voltage spec for device: 250 Vrms (min). (Since the resistance of the series element will increase to become much greater than the source resistance.)
4. Peak current handling requirements. Given that the test condition has a 30Ω source impedance, then short circuit current capability of the source is 12 Apeak (8.33 Arms). This suggests a fairly large thermistor to withstand a peak current as high as this. A suitable device which has a current rating close to this is YS960 which has a peak current rating of 10A. This device has a cold resistance of 10Ω, which when added to the source resistance gives a total resistance of 40Ω across the 250 Vrms source. This gives a peak current of 8.83A.

An alternative method is to choose a thermistor with a higher cold resistance. This increases the resistance in series with the source resistance thus reduces the peak current handling requirements. If a thermistor has a cold resistance of 40–50Ω, it only requires to handle a maximum current of 5A in the example given, and has the added advantage that the current flow into the protection ground is also reduced. This tradeoff is dependent on the availability of suitable thermistors. The calculation of this parameter must always be done using this somewhat iterative method to arrive at a suitable device.

The choice of a suitable device is often restricted by the limitations of one of the test requirements, and experience shows that this is often the peak current requirements. After the device has been selected, the predicted performance level can read off the graphs plotted in the results section checking the validity of the selection.

8.0 WORKED EXAMPLE 2

If the longitudinal requirements are much more strict, such as those imposed by the Bell specifications, the value selected becomes more critical. Referring to the results graphs suggests a value of 75–120Ω for the series elements. In the case of the thermistor selected in the first example, this is not so, but can be made very easily. Since the shunt protector device is connected across the junction of the series elements and the module pins, anything behind this node is protected by the secondary protection. In order to improve the longitudinal balance performance of the circuit, it is necessary to place additional resistance in series with the thermistors to increase the combined value of the resistance closer to 100Ω. This can be done with two resistors which would raise the resistance to around 85Ω overall. Care should be taken in the power rating of these resistors since during fault conditions, these must cope with the difference in shunt protector trigger voltage, Vbo, and the battery supply. This can cause a substantial amount of power to be dissipated in this condition. A schematic showing the implementation of this technique is given in *Figure 18.*

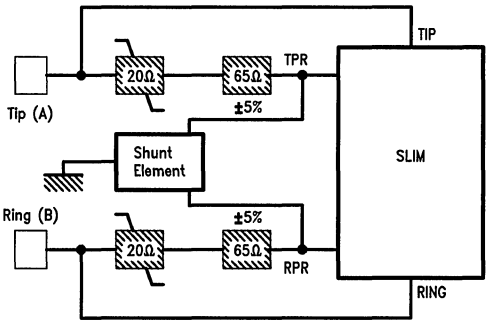

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FIGURE 18. Protection Schematic for Stringent Longitudinal Requirements

9.0 CONCLUSIONS

At the outset of this applications note, the objective was to show the ease of designing protection networks using the **SLIM** module. Due to the philosophy behind the **SLIM** of reducing the cost of the overall application, the protection constraints are much less stringent than in conventional line interface circuits, which allows previously unavailable protection schemes to be employed. Below is a summary of the advantages and disadvantages of the fusible and auto-resetting systems.

Fusible Systems

Advantages

1. Low Installation Cost.
2. Low Power dissipation on board during fault conditions.
3. Total disconnection of subscriber wires when fault occurs.

Disadvantages

1. Relatively high replacement costs.
2. Labor intensive, especially in distributed switching systems.
3. Non-resettable, thus causing unnecessary out of service time for users.
4. Possibility of operating due to transient fault.

Auto Resetting Systems

Advantages

1. Good for remote locations.
2. No unnecessary down time for users.
3. Completely automatic.
4. Low maintenance.
5. Low instances of transient operation.

Disadvantages

1. Increased Installation costs.
2. Small amount of on-card heating due to thermistor dissipation (2–3W).
3. Line not totally disconnected during fault condition.

Given these choices, and bearing in mind the industry moving toward decentralized switches, the auto resetting systems technique is more applicable to the requirements of the market where maintenance costs are at a premium. There are now companies taking advantage of this opportunity and manufacture complete modules containing the thermistors and shunt protectors designed for direct mounting onto the line card. These modules are ideal for applications attempting to minimize the board footprint for compact systems employing 16 lines on a card, but do incur a slight cost penalty.

Finally, included as an appendix to this note is a list of suppliers of shunt protectors, series fuse elements, fusible resistors or fusible links, and a supplier list of thermistors. This list is not intended to be exhaustive, but more a starting point for those who are interested in pursuing the subject further. It is hoped that in writing this note that the author has highlighted the major problems in trying to design protection schemes for line card applications, and helped in dispelling any misconceptions in the application of thermistors in this area.

APPENDIX

Below are listed suppliers of protection components. Suppliers of Fusible series protection components.

1. Welwyn Electronics.
Bedlington, Northumberland NE22 7AA England
Tel. (0670) 822181.

2. International Resistive Company, Inc.
Post Office Box 1860,
Boone, North Carolina, 28607-1860 USA
Tel. (704) 264-8861.

Suppliers of PTC Series Elements.

1. Raychem Corporation,
Polyswitch Products, 300 Constitution Drive
Menlo Park, Calif., 94025-1164 USA
Tel. (415) 361-6900.

2. Mullard Ltd.
Mullard House, Torrington Place
London, WC1E 7HD

3. STC Components
Thermistor Division,
Crown Industrial Estate,
Priorwood Road,
Taunton,
Somerset,
TA2 8QY.
England.
Tel. (0823) 335200.

Suppliers of Shunt Protection Devices.

1. Texas Instruments,
Power Products Division.

2. Teccor Electronics Inc.
1801, Hurd Drive,
Irving, Texas 75038-4385 USA
Tel. (214) 580-1515.

Lucas Semiconductors Ltd.
Garetts Green Lane,
Birmingham.
B33 0YA.
England.
Tel. (021) 784-6855.

ISDN Basic Rate Interface Terminal Equipment (TE) System Design Guide

National Semiconductor
Application Note 664
Telenetworks

PREFACE

This System Design Guide is intended to aid a system design engineer in implementing an ISDN Basic Rate Interface (BRI) Terminal Equipment (TE) application. The Design Guide is divided into the following sections:

1.0 ISDN Basic Rate Interface Overview

2.0 ISDN BRI Terminal Equipment Functional Requirements

3.0 ISDN BRI Terminal Equipment Design Solution

4.0 Summary

Section 1 is intended to introduce ISDN BRI and to give some justification for implementing such an application. Section 2 presents the necessary hardware and software functional subsystems, without getting into specific implementation details. Section 3 presents a design solution for the ISDN BRI application, introducing the National Semiconductor HPC16400E Microcontroller along with the Telenetworks ISDN software packages. Section 4 summarizes the ideas presented in this System Design Guide.

References for this System Design Guide are found in Appendix A.

For more information regarding ISDN BRI implementations contact your local National Semiconductor representative or contact Telenetworks at (707) 778-6500.

1.0 ISDN BASIC RATE INTERFACE OVERVIEW

The Integrated Services Digital Network (ISDN) Basic Rate Interface (BRI) provides a replacement for the current subscriber line interface offering into businesses and homes. As shown in *Figure 1*, the ISDN BRI offering uses the same copper pair as the current conventional phones, but provides more and better services to the subscriber. To harness these services it is necessary to follow the prescribed layered protocols for developing ISDN BRI Terminal Equipment (TE). This System Design Guide functionally defines these protocols and proposes an implementation solution for a particular ISDN BRI terminal design. This section defines what ISDN BRI services are and why they are worth the investment in a new technology.

The INTEGRATED part of ISDN is apparent in two domains: the integration of voice and data on the same interface, and the integration of an out-of-band signaling (D) channel with the bearer (B) channels. The advantages of this integration are defined in the following paragraphs.

The SERVICES part of ISDN are the main reason for ISDN's potential growth and acceptance in the future. Basic Voice and Basic Data services, and even the "Big 4" Supplementary Services (HOLD/RETRIEVE, CONFERENCE, DROP, and TRANSFER), are not enough to propagate the ISDN cause. All of these services are available with the current analog Centrex service offerings. For ISDN to be truly successful, cost-effective end-user applications must be developed and supported that require the extended services that are only available through ISDN, e.g., Keyset services, User-to-User data, and telemetry services on the D channel.

The DIGITAL part of ISDN provides three digital channels (B1, B2 and D) between the Customer Premise Equipment (CPE) terminals and the Central Office. Any combination of voice and/or data services can be provided on either of the two bearer channels, while both signaling and data can be sent over the D channel. For example, two voice circuits can be implemented over the same wire pair that previously only supported one. Data can be sent at up to 64 kbits/second, rather than the current nominal rate of 2400 baud using a modem. End-to-end digitized information is less susceptible to noise, allowing for clearer voice quality and less data retransmissions. Several data links running at sub-rates (less than 64 kbits/second) can be multiplexed onto a B channel or the D channel using various time division multiplexing techniques not available in the analog domain, thus taking full advantage of the channel bandwidth.

The NETWORK part of ISDN includes marketing and tariffing issues. For ISDN to be successful digital facilities must be available from end-to-end, i.e., no isolated ISDN islands. The network must provide signaling and bearer services throughout the country (and eventually the world), using Signaling System #7 as the inter-office backbone. The network is also responsible for the appropriate billing mechanisms for the ISDN services. User-driven applications must be developed and supported by the network, along with a cost-effective tariffing structure.

BRI ISDN will slowly become available to the general public. It is currently being deployed in large metropolitan areas, targeted for business environments. Just when more general deployment will occur depends on the rate of depreciation of current equipment, tariffing rates for the ISDN services, and user acceptance of the new ISDN technology. End-users are just now becoming educated on the virtues of ISDN. Ultimately, the end-users will have to drive OEM vendors to provide ISDN terminal equipment that brings special services to them. These services will have to either cost less than currently available services, or be value-added and cost effective. The remainder of this document provides OEM vendors with an idea of what is involved in designing an ISDN BRI terminal, and what "building blocks" are available for implementing such a terminal.

There are several types of ISDN Terminal Equipment (TE). TEs can be Voice and/or Data; PC-based or stand-alone; synchronous and/or asynchronous; 0B+D, 1B+D, or 2B+D; X.25, V.120, or V.110, or any combination of data protocol support. *Figure 1* shows a generic stand-alone voice/data terminal configuration.

ISDN Basic Rate Interface
Terminal Equipment Application

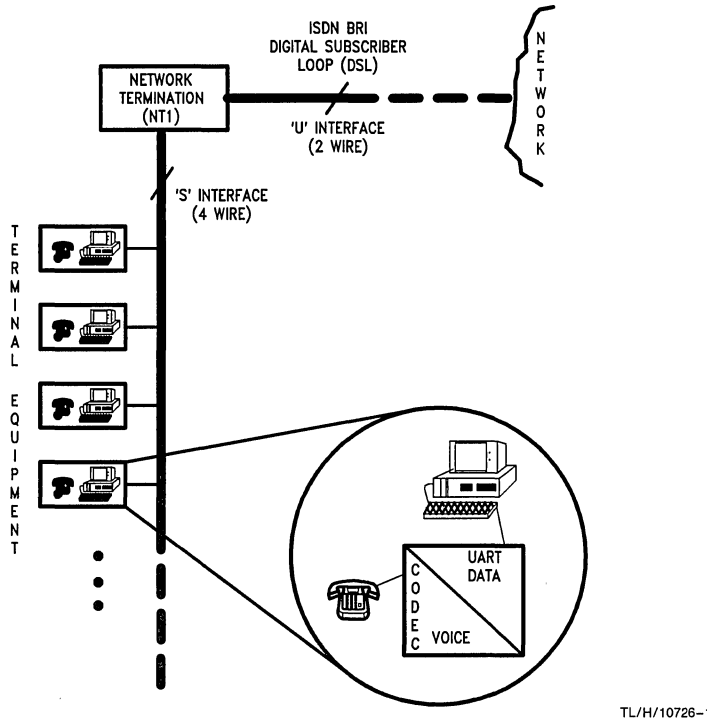

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FIGURE 1

2.0 ISDN BRI TERMINAL EQUIPMENT FUNCTIONAL REQUIREMENTS

The ISDN BRI Terminal Equipment (TE) Functional Requirements are layered, in accordance with the OSI Layered Model. ISDN applications include requirements at the Physical Layer, the Data Link Layer, the Network Layer and the Application Layer. *Figure 2* reflects these layered functions for each of the following subsystems: the Digital Subscriber Signaling System #1 (DSS1) protocol requirements, the data protocol termination requirements, and the Maintenance and Management requirements.

Several types of data protocols exist today (e.g., X.25, V.120, V.110, DMI, and T-Link). This System Design Guide focuses on the requirements necessary to design an ISDN BRI voice/data terminal, using the X.25 asynchronous and synchronous data protocol for terminal adaptation. The definition of the layered requirements for the other forementioned data protocols is beyond the scope of this Design Guide. The X.25 data protocol was chosen because it is the most prevalent data protocol today, as well as the best defined protocol. The requirements for transporting X.25 data on an ISDN BRI terminal are defined as part of this paper and are more generally defined in CCITT Recommendation X.31.

2.1 System-Level Requirements

A relatively powerful CPU engine is necessary to process the DSS1 and data communication protocols. Small 8-bit microcontrollers are not generally adequate for the task. On the order of 128 kbytes of ROM are necessary to implement these CCITT protocol requirements, assuming the code is compiled from a high-level language such as "C".

Careful consideration must be given to controlling an ISDN BRI application. There are several asynchronous, detailed processes going on that require some level of coordination regarding process scheduling, buffer management, message passing, and timer handling. Selection of an adequate design environment in which to nest the various processes is of utmost importance. Use of a multitasking executive is recommended.

2.2 Physical Layer Requirements

To make a terminal a member of the ISDN passive "S" Interface bus a front end "S" interface device is necessary. This device must allow for D channel contention and understand the framing channel. Such a device will take varying degrees of software intervention and control, depending on the device architecture. The I.430 activation (and optionally deactivation) sequence must be followed to initialize the "S" interface device of an ISDN BRI terminal.

For a voice application, a CODEC is needed to convert analog voice into digital PCM. A keypad and hookswitch, along with a display, are also required. Some software intervention is necessary to activate and deactivate these devices, debounce hardware inputs, and control these devices. A call progress tone generator is also required to "play" progress tones (e.g., DIALTONE, BUSY, and RINGBACK) to the ear. A set of telephony device driver modules must be available to interface to these hardware devices.

For data applications, hardware and software drivers are needed to control the R interface devices. For asynchronous data applications a UART is required, along with a UART Software Driver module to control the interface. For synchronous data applications a USART is required, along with an HDLC Software Driver module to control the interface.

In some applications it is not desirable to hard-wire a particular bearer channel to the CODEC or to the HDLC port. In these cases it may be necessary to provide a switching device to dynamically switch a bearer channel to either of the two sources.

Semiconductor vendors have developed several types of internal digital formats that allow these various devices to communicate. Serial decoding is the physical layer function that presents the S interface data to the particular devices. Care must be taken to ensure that the selected Layer 1 devices all provide the appropriate digital format.

2.3 Link Layer Requirements

The OSI Link Layer (2) is defined by two sets of procedures: High-Level Data Link Control (HDLC) procedures and Link Access Procedures (LAP). HDLC procedures are typically done in hardware with synchronous channel controllers. Link Access Procedures are typically done in software, although some silicon devices do offer limited LAP functionality.

As shown in *Figure 2*, two HDLC Controllers are required: one to terminate the D Channel and one to terminate one of the Bearer Channels for data. HDLC software device drivers are needed to control both of these HDLC channels. From a software implementation point of view, DMA controlled HDLC channels are much more desirable than FIFO-based channels because they ease the CPU interaction requirements.

The D Channel termination at Layer 2 requires implementation of the Line Access Procedures of CCITT Recommendation Q.921, more commonly referred to as LAPD. LAPD provides in-sequence, error-free transmission of frames to the higher layers. LAPD can handle multiple logical links. For the ISDN BRI there are at least three logical links, one for signaling functions (SAPI = 0, TEI = X), one for maintenance functions (SAPI = 63, TEI = 127), and one for D channel data (SAPI = 16, TEI = Y). "X" and "Y" are arbitrary, but valid, TEI assignment values.

The X.25 B Channel data termination at Layer 2 requires implementation of the Link Access Procedures of CCITT Recommendation X.25, more commonly referred to as LAPB. Like LAPD, LAPB also provides in-sequence, error-free frames to the higher layers. LAPB can only handle one logical link at Layer 2.

2.4 Network Layer Requirements

The ISDN DSS1 D Channel signaling termination at Layer 3 requires implementation of the Protocol Control procedures of CCITT Recommendation Q.931. These procedures include setting up and tearing down local access connections between the terminal and the Central Office. These connections can be for voice or data services and can be requested for the BRI B or D channels.

For X.25 data calls all packets must be processed by the Layer 3 Packet Layer Process (PLP). These procedures include setting up and tearing down virtual packet switch connections between end-to-end X.25 terminals. These virtual connections are established "in-band" during the X.25 call setup phase.

ISDN Basic Rate Interface
Terminal Equipment (TE) Functional Requirements

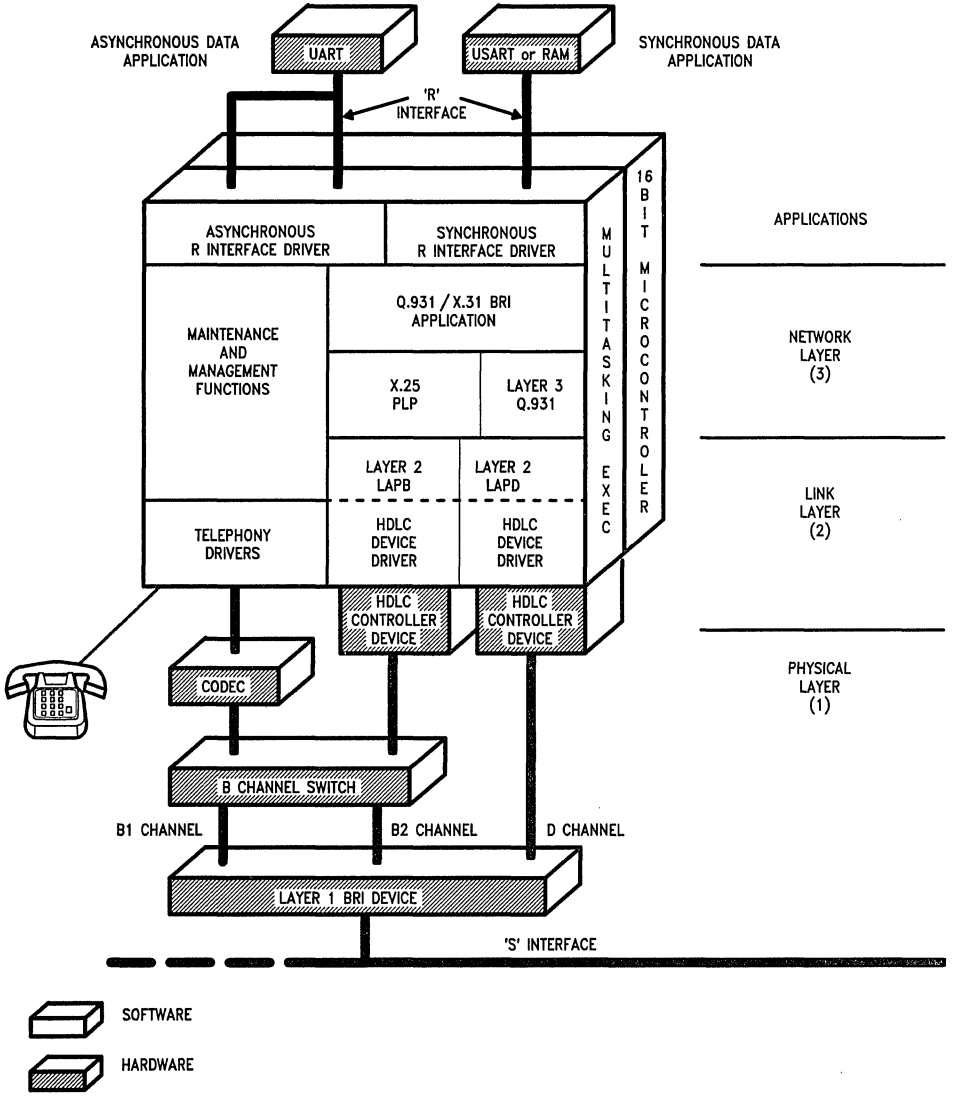

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FIGURE 2

2.5 Application Layer Requirements

As mentioned above, for the sake of this System Design Guide a hypothetical stand-alone ISDN voice/data terminal (TE) will be defined that allows voice or data services on either of the two bearer (B) channels. It will support synchronous and asynchronous X.25 data connections on either bearer channel, and asynchronous data on the D signaling channel.

A Basic Rate Interface Application Controller is required that includes the Call Control procedures of Q.931 and X.31. This controller keeps track of which protocol is on which channel. It must also interface to the I/O device drivers for the asynchronous and synchronous terminals, as well as the voice-related telephony hardware.

For the X.25 asynchronous data application the TE expects a data application to be running on a PC connected via the "R" interface, a local UART. The TE intercepts commands across the "R" interface and translates them into DSS1 Setup and Teardown commands. Service can be requested for either the B or D channel. Once a channel is setup, then the data phase (packet transfer) is established with the X.25 PLP. When data transfer is complete the PC Application will disconnect with a particular command which will be translated into a DSS1 release sequence, at which time the channel will be available for another service.

For the X.25 synchronous data application a synchronous X.25 DTE is expected at the other side of the "R" interface. A USART is required with a special HDLC device driver module to terminate the 56 kbit/second data stream. The driver initially monitors the link for a link establishment indication (SABM). If the DTE requests service first, (link establishment indication is sent by the DTE), an ISDN bearer channel is requested via the DSS1 protocol on the D channel. If the network requests service first the network will setup the bearer channel using the DSS1 protocol, and then establish the data link in-band with the DTE. After successful setup of a B channel, packets are sent between the DTE and the packet handler. At the end of the data session the network side is expected to disconnect the data link in-band (with a Layer 2 DISC command) and then release the call using DSS1 release procedures.

Voice service is controlled entirely within the TE. During the time that synchronous data service is being provided on one of the B channels, it is recommended that the TE only allow asynchronous data service on the D channel to avoid voice service from being blocked. In a passive bus arrangement, i.e., multiple TEs on the same S interface, it is recommended that asynchronous data service only be allowed on the D channel. Of course this is a decision that must be made, and enforced, at the application layer.

2.6 Maintenance and Management Requirements

Every application of this magnitude requires some degree of maintenance and management. Some maintenance functionality is required by the Network, while some of the functionality is strictly application dependent. The major maintenance functions include provisioning the TE, statistic collection and reporting, physical layer alarm reporting and recovery, protocol breakdown recovery, and resource depletion handling. Other peripheral maintenance functions include loopback mechanisms, human interface capability, and software PROM revision maintenance.

Procedures from I.430 are necessary to activate and optionally deactivate terminals on the "S" Interface. Procedures for TEI assignment are defined in CCITT Recommendation Q.921, and in the AT&T and NTI switch specifications. Parameter negotiation procedures are also defined in these switch specifications. For any BRI implementation, extensions must be made to the Maintenance and Management functions beyond what is defined in specifications.

It is generally prudent to introduce a UART-based maintenance interface into a design of this complexity. This interface allows for message tracing, limited process interaction, and optional program download and debug capability all from a PC or terminal attached to the UART. A maintenance interface software driver module is needed to manage the screen output and keyboard input functions for the terminal attached to the UART. This interface can be shared with the asynchronous data application, only being available when the data application is not operating.

3.0 ISDN BRI TERMINAL EQUIPMENT DESIGN SOLUTION

Figure 3 presents an implementation solution for the ISDN BRI Terminal Equipment (TE) requirements. The solution revolves around the National Semiconductor HPC16400E Microcontroller and the Telenetworks ISDN Software packages.

Hardware Solution

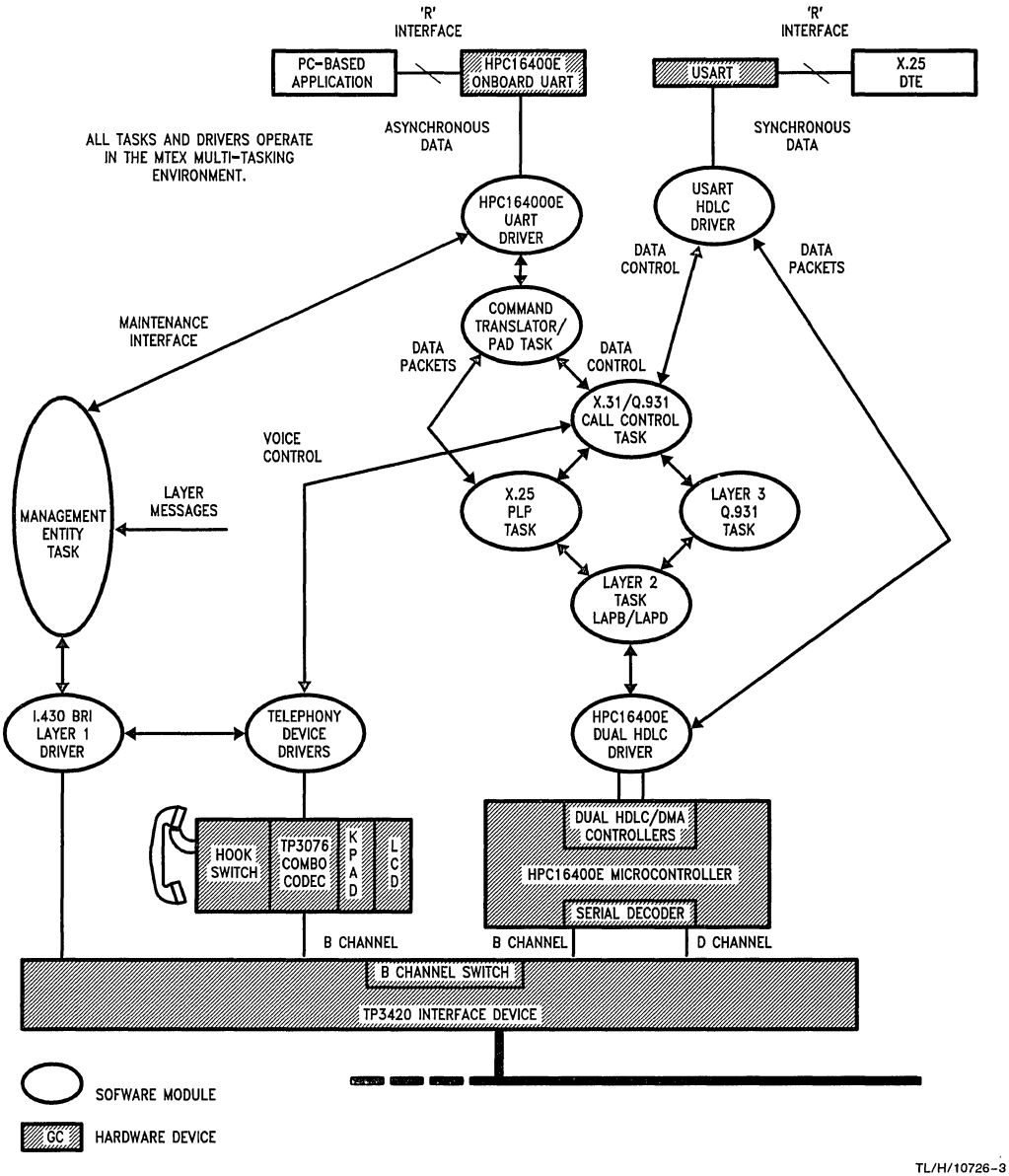
- NSC HPC16400E
  - Powerful 16-Bit Microcontroller:
  - 2 Onboard HDLC/DMA Controllers
  - 1 Onboard UART
  - 4 Onboard Timers
  - Synchronous Serial Time-Slot Decoder
  - General Purpose I/O Ports
  - 8 Prioritized Interrupt Levels
  - MICROWIRE® Interface
- NSC TP3420 S Interface Device (SID)
- NSC TP3076 COMBO™ Codec
- USART

Software Solution

Telenetworks ISDN Software Off-the-Shelf Packages
- MTEX Multitasking Executive
- I.430 BRI Layer 1 Driver
- HPC16400E Dual HDLC/DMA Driver
- Layer 2 Task
- Layer 3 Q.931 Task
- X.25 Packet Layer Process Task
- Prototype X.31/Q.931 Call Control Task
- Basic Management Entity Task
- HPC16400E UART Driver

Custom Software Development (by Telenetworks or OEM)
- USART HDLC Driver
- Application Specific X.31/Q.931 Call Control Task
- Command Translator/PAD Task
- Extended Management Entity Task
- Extended Applications for Supplementary Services
- Telephony Device Drivers

ISDN Basic Rate Interface NSC TE System Solution



TL/H/10726–3

FIGURE 3

3.1 System-Level Solution

The NSC HPC16400E is a powerful 16-bit CPU engine that is fully capable of processing the DSS1 and B-Channel data communication protocols. The HPC16400E has two flexible onboard HDLC/DMA controller channels that are ideal for terminating the D Channel and data on a B channel. It has an onboard UART to terminate the asynchronous data interface, 4 onboard timers, and several general purpose I/O pins. The HPC16400E can address 544 kbytes of memory space, however for the ISDN BRI application the entire memory space should be less than 128 kbytes.

An off-the-shelf Multitasking Executive, MTEX, that was designed specifically for controlling ISDN BRI terminal applications has been hosted on the HPC16400E. MTEX has the following subsystems:

Task Scheduler
Mail Manager
Timer Handler
Memory Manager.

MTEX was designed to provide an environment for communication protocol applications, with special built-in features to handle timers and flow control. Processes, such as Layer 2 Link Access Procedures and Layer 3 protocols, are designed as tasks running under MTEX. Intertask messaging is via the MTEX Mail utilities. MTEX also provides memory management utilities for buffer management.

3.2 Physical Layer Solution

The National Semiconductor "S" Interface Device (SID-TP3420) terminates the "S" Interface at the physical layer. The off-the-shelf I.430 BRI Layer 1 software driver module is available to control the SID as defined by CCITT recommendation I.430. The SID also has a built-in mechanism for "switching" the bearer channels upon command. The SID communicates with the NSC HPC16400E via NSC's MICROWIRE interface. The MICROWIRE interface is a three-wire serial interface (SI, SO, and CLK).

The NSC COMBO Codec, TP3076 can be used for terminating the voice path in the TE and converts to analog voice signals. The COMBO communicates via the MICROWIRE interface.

The HPC16400E onboard UART is ideal for the asynchronous data interface and for the maintenance interface. The UART has a high resolution clock for rates up to 19.2 kbaud. An off-the-shelf HPC16400E UART software driver module is available that interfaces to this UART. This driver fields messages from tasks and outputs them to the UART, as well as receiving input from the UART and sending it to the appropriate task.

A synchronous communication device is needed to terminate the synchronous data interface. NSC makes a standalone USART for just this purpose, the TP3460. A special USART HDLC software driver module is needed to control the USART and monitor the interface for particular commands. The requirements for this driver are defined below in the synchronous data application section of this document.

Custom Layer 1 Telephony drivers and routines are needed to control such things as hookswitch, keypad input, LCD or LED updates, local tone generation, power ringing, and various other application dependent telephony device requirements.

The HPC16400E has a programmable onboard Serial Time-Slot Decoder that provides an interface to the B and D channels of several popular chip-to-chip interface formats.

3.3 Link Layer Solution

The HPC16400E has two independent HDLC/DMA controller channels integrated onboard with the Central Processing Unit. For ISDN BRI applications, one channel runs at 16 kbits/second for the D Channel, the other runs at 64 kbits/second for data on a B Channel. The DMA Controllers receive and transmit entire frames prior to interrupting the processor. This allows for a much simpler Layer 2 Driver design than would a FIFO-based HDLC controller. The HPC16400E has several other features which ease the implementation of the ISDN BRI application. These features are defined in the following paragraphs.

The HPC16400E can operate in a special split field mode where the Layer 2 Header data is placed in one buffer, while the following Layer 3 Information data is placed in another buffer. This feature eases the memory management requirements of an application and decreases the need for copying messages from buffer to buffer.

If the split field feature is not used then HPC16400E DMA chaining features can be fully exploited to simplify the application design. On the receive side, four buffers can be made available for incoming frames. When a frame arrives, an interrupt is generated by the DMA Controller. While the processor is responding to the interrupt and fielding the current message, new frames that arrive will automatically be placed into memory buffers. Up to 4 messages can arrive without any processor intervention. On the transmit side two messages can be output, delimited by a closing/opening flag, without processor intervention. If the split field feature described above is used then two frames can be chained on the receive side, with no chaining available on the transmit side.

The HPC16400E can be programmed to recognize particular Layer 2 addresses (SAPI-TEI combinations). This feature is useful if the terminal is to be used in a passive bus arrangement. In such an arrangement messages not intended for a particular terminal on the bus can be filtered by the terminal and discarded without any processor intervention.

The two HDLC/DMA channels are controlled by an off-the-shelf HPC16400E Dual HDLC/DMA software driver module. The driver consists of an Interrupt Service Routine, and two Service Request Tasks, one for each channel. The driver is responsible for initializing the synchronous channel hardware, and controlling the transmission and reception of frames. It is also required to handle buffer management for messages in both directions. Buffers must be allocated for incoming messages and deallocated after the transmission of outbound messages. One exception to this rule is that after transmission, I frame buffers are NOT deallocated by the Driver since they may need to be retransmitted if unacknowledged. The Layer 2 Software Module has the responsibility for deallocating transmitted I frame buffers when the appropriate acknowledgement is received. This driver configures both HPC16400E HDLC/DMA channels to use the split field feature.

The D Channel is terminated at Layer 2 with the off-the-shelf Layer 2 Software Task providing the LAPD solution. The LAPD was prototyped after the CCITT 1988 Blue Book version for Q.921, however it has been tailored to implement the Layer 2 Specifications in the 5ESS 5E5 generic software release from AT&T, and the DMS100 BCS-28 generic software release from Northern Telecom. LAPD logical entities are defined based on SAPI and TEI.

The B Channel is also terminated at Layer 2 with the off-the-shelf Layer 2 Software Task providing the LAPB solution. The LAPB was prototyped after the CCITT 1988 Blue Book version for X.25 Layer 2.

3.4 Network Layer Solution

The off-the-shelf Layer 3 Q.931 Task is designed to implement the call setup and teardown protocols as defined in the CCITT Blue Book version for Q.931. The Layer 3 Task has also been tailored to implement both the Layer 3 Specifications in the 5ESS 5E5 generic software release from AT&T, and the DMS100 BCS-28 generic software release from Northern Telecom. This protocol terminates the D Channel at Layer 3. Network Link logical entities are defined based on Channel Endpoint Suffix (CES), Call Reference and Call ID.

The off-the-shelf Layer 3 X.25 Packet Layer Processor (PLP) Task is designed to implement the establishment of X.25 virtual data connections. Layer 3 PLP logical entities are defined based on CES and Logical Channel Number.

3.5 Application Layer Solution

Applications by their very nature are proprietary, so very little can be offered "off-the-shelf". Certain functions have been "standardized" at the application layer, but in general custom code design and development is necessary. Supplementary Services are defined in both the voice and data domain, however the invocation of these services is very application dependent and requires custom solutions.

Telenetworks does offer a prototype X.31/Q.931 Call Control module that controls voice calls over an ISDN interface, as well as asynchronous and synchronous X.25 data calls. For the voice application this module controls various telephony devices by communicating with the Telephony Device driver modules. It also expects to communicate with a Command Translator/PAD Task and a USART/HDLC software driver module, as defined in the following paragraphs.

3.5.1 Asynchronous Data Application

For this specific X.25 asynchronous data application example the TE expects to communicate with a PC running the Hayes Modem application program. The Hayes Modem program communicates out of the PC UART toward a modem. The "expected" modem is replaced by the ISDN TE. A Command Translator/PAD Task will be needed to interpret the Hayes AT commands for setting up and tearing down the desired bearer service.

If the PC user wants service, then a service request with a called party number arrives at the TE in a Hayes command and is translated into an ISDN Setup command. This data control message is sent to the X.31/Q.931 Call Control Task. The DSS1 protocol then sets up the appropriate data service on either the D or a B channel. If the network side wants service then the network sets up an ISDN call using the DSS1 call setup procedures. In this case the appropriate data control response is sent from the Call Control Task to the Command Translator/PAD Task.

Once the call setup sequence has reached the ACTIVE state then the data phase is entered, at which time the Command Translator/PAD Task acts like a Packet Assembler/Disassembler (PAD) and communicates directly with the X.25 PLP Task. In this example, data is rate adapted from a nominal 1200 baud rate at the UART to either the 16 kbits/second D channel rate or the 64 kbits/second B channel rate.

After the data session the call is cleared either by a Hayes command from the PC application or from the far end. In either case, the X.25 link is released, and then the ISDN facility is released using the DSS1 call clearing procedures.

3.5.2 Synchronous Data Application

For this X.25 synchronous data application example the TE expects to communicate with an X.25 Data Terminal Equipment (DTE) running synchronous 56 kbits/second data. A synchronous channel controller device (USART) terminates the "R" interface. A custom USART device driver module will be needed to control the USART and to monitor certain data control commands.

When an X.25 DTE requests service it typically sends a Layer 2 LAPB SABM command to establish the data link. The USART HDLC driver module intercepts this SABM and sends a data control service request to the X.31/Q.931 Call Control Task. This message prompts the Call Control Task to set up an ISDN bearer channel using the DSS1 call setup procedures. Once the call setup sequence has reached the ACTIVE state then the Call Control Task sends a message to the USART HDLC driver module that a bearer channel is available. The USART driver then sends the SABM directly to the HPC16400E HDLC driver module. The network side can also request service, in which case the Packet Handler sets up the ISDN bearer channel using the DSS1 call setup procedures. In this case the Call Control Task prompts the USART driver module that a bearer channel is available.

In either of the above cases, DTE to DCE is established and the data phase is entered. During the data phase packets are transmitted directly from the USART driver to the HPC16400E dual HDLC driver without any intervention by the TE. In this example, data is rate adapted from the nominal 56 kbits/second rate to the ISDN 64 kbits/second B channel rate.

After the data session the network side is responsible for initiating the call clearing process by first disconnecting the X.25 data link with a LAPB DISConnect command. The network side then clears the ISDN facility with the DSS1 call clearing procedures. The Call Control Task informs the USART driver module that the bearer channel has been released.

3.6 Maintenance and Management Solution

Most of the Management Entity Task's functions are application dependent, such as provisioning the ISDN BRI terminal, collecting statistics from the various hardware devices, and alarm detection and recovery. These functions will require custom code development.

As previously mentioned a software driver is available that activates and optionally deactivates a BRI terminal. This driver works in concert with Layer 2, the Management Entity procedures, the particular application, and of course the NSC SID.

The TEI Assignment procedures are also included in the Management Entity Task. Provisions have been made for both automatic and non-automatic TEI assignment procedures. TEI Check and Verify procedures are also included.

Management functions such as parameter negotiation and higher layer processes are application dependent and require custom solutions.

The HPC16400E onboard UART can be used for the maintenance interface. This interface is defined in the physical layer section of this document. The maintenance features would only be available when the asynchronous data services are not in progress. Additional commands must be added to the PC application program to control the maintenance interface.

3.7 Software Development Environment

The process of developing a software application around the Telenetworks ISDN software will vary greatly depending on the application and the target hardware. The procedure given below is an example that might apply to the development of an ISDN BRI application. Task_View, a testing tool developed by Telenetworks, is defined below, as well as the software tools that are available for the NSC HPC16400E.

In a typical ISDN BRI application there are two main areas of software development. First, device drivers must be written for the particular telephony hardware that exists in the target system (e.g., Layer 1 drivers and DMA/HDLC drivers). Second, a Call Control Application Task must be designed to control the telephony hardware and interface to the Layer 3 Protocol Control Tasks.

Typically, in such a development process, the target hardware is not available at the time that software development begins. This suggests a three step software development process. First, the Call Control Application Task is written and is unit-tested in a PC environment. Second, when the target hardware becomes available, the telephony hardware drivers are written and unit-tested in this target environment. Finally, the entire system software is integrated and tested with the hardware.

3.8 Task_View Description

To aid in testing ISDN software modules Telenetworks has developed Task_View. Task_View is a special-purpose debugging task that can be run, together with other tasks, under the MTEX Multitasking Executive. It reads and interprets a user-supplied ASCII file, containing a test scenario. Under control of the test scenario, Task_View sends mail messages to a specified mailbox (or mailboxes), where they are read by the task(s) under test. Mail messages sent by the task(s) in response to this input are then displayed by Task_View. In this way tasks can be debugged in isolation, before integration into the complete target environment.

The full-featured Task_View operates only in a PC environment, since it uses the DOS file system to handle the test scenario files. This is less of a limitation than it might appear, since many tasks interact only with the MTEX Multitasking Executive and can be unit tested and debugged in a PC environment, running under the PC version of MTEX, before integration with other tasks in the target environment. However, some modules, in particular I/O drivers, can only be tested in the target hardware environment. A simplified version of Task_View has been ported into the embedded HPC environment for testing of the I/O Drivers. Task_View has also been ported into the Sun workstation development environment.

3.9 NSC Development Tools

Below is a list of the development tools available for the NSC HPC16400E.

HPC "C" Compiler
HPC Linker
HPC PROM tools
HPC Microcontroller On-Line Emulator (MOLE™)
NSC TP3500 ISDN Evaluation Target System.

4.0 SUMMARY

As ISDN BRI becomes more and more prevalent, users will require terminal vendors to provide new ISDN products or to implement ISDN interfaces into their current products. This System Design Guide has attempted to present a comprehensive design solution for those vendors interested in designing an ISDN BRI product. NSC and Telenetworks are committed to providing ISDN solutions to the telecom industry. This Design Guide did not discuss implementation of the two public data protocols, V.120 and V.110. It also did not discuss implementation of any private data protocols such as DMI and T-Link. This was intentional in an effort to somewhat scope the Design Guide. However both NSC and Telenetworks have developed design support for these protocols and others. NSC has just announced their "R" Interface Device, the TP3460, which provides many of the hardware sensitive functions of V.110. Certain V.110 and V.120 software modules are available to also aid a designer in developing a terminal adapter for these protocols.

For more information on ISDN BRI implementations contact your local National Semiconductor representative or contact Telenetworks at (707) 778-6500.

APPENDIX A: REFERENCES

5ESS ISDN Basic Rate Interface Specification, 5E5 Generic Program, AT&T Document 5D5-900-311, December 1987, Chapter III (Layer 2 and Management Entity) and Chapter IV (Layer 3).

DMS-100 Basic Rate Interface Specification, Northern Telecom Document NIS S208-4, October 1988, Section C (Layer 2 and Management Entity) and Section D (Layer 3 Functional Mode).

CCITT Recommendations Q.921, Q.931, X.25, X.31, and I.430 "Blue Books", Geneva 1989.

National Semiconductor HPC16400E Data Sheet.

National Semiconductor HPC16400E User's Manual.

TP3420/TP3421 S Interface Device (SID) User's Guide

National Semiconductor
Application Note 665
R. Patipatyadar
V.P. Shenoy
C. Stacey

Table of Contents

1.0 INTRODUCTION

2.0 LINE INTERFACE AND TRANSMISSION PERFORMANCE

2.1 Master Clock Source
- 2.1.1 Crystal Oscillator
- 2.1.2 External Oscillator Configuration
- 2.1.3 List of Recommended Crystal Manufacturers

2.2 Line Transformer Requirements
- 2.2.1 Line Transformer Ratio
- 2.2.2 Line Transformer Electrical Parameters
- 2.2.3 Printed Circuit Board Layout Considerations
- 2.2.4 Recommended Line Transformer Manufacturers

2.3 External Protection Circuitry
- 2.3.1 DC Bias Capacitors for Analog Reference

2.4 Transmission Performance

3.0 TP3420 DIGITAL SYSTEM INTERFACE

3.1 Digital System Interface Formats

3.2 TP3420 Digital System Interface and μP Connection
- 3.2.1 TP3420 and HPC16400E Connection for D-Channel
- 3.2.2 TP3420 and HPC16400E Connection for B Channel

3.3 TP3420 Digital System Interface and TP3076 COMBO® Connection

3.4 NT-2 Synchronization (TP3420/1)

3.5 Slave-Slave Mode and Elastic Buffers (TP3420/1)

4.0 DIGITAL CONTROL INTERFACE

4.1 The MICROWIRE™ Bus

4.2 TP3420 SID to HPC16400E MICROWIRE Connection

4.3 TP3420 SID COMMAND and STATUS Bytes

4.4 TP3420/1 Receive Timing Recovery

4.5 TP3420/1 Line Signal Detect (LSD) and Wake-Up Signal for μP

5.0 ACTIVATION AND DEACTIVATION

5.1 S Interface Loop Activation Initiated from the TE End

5.2 S Interface Loop Activation Initiated from the NT End

5.3 S Interface Loop Deactivation Initiated from the NT Side

5.4 D-Channel Request and Flow Control

5.5 Software Driver Considerations

6.0 TERMINAL EQUIPMENT (TE) ACTIVATION FLOW CHARTS

7.0 NETWORK TERMINATION (NT) ACTIVATION FLOW CHARTS

8.0 TEST LOOPBACK MODES

8.1 Normal Data Mode (No Loopbacks)

8.2 System Loopback Mode LBS

8.3 System Loopback Mode LBB1, LBB2

8.4 Line Loopback Mode LBL1, LBL2

9.0 ADDITIONAL TEST FEATURES

9.1 External Local Analog Loopback

9.2 Monitor Mode Activation

RELATED MATERIAL

This manual assumes that the user is familiar with the ISDN Basic Rate Interface and its applications.

Other applicable documents include:

- TP3420 "S" Interface Device (SID) Data Sheet
- TP3421 SID with GCI Data Sheet
- TP3076 COMBO II™ Data Sheet
- HPC16400E Communications Controller Data Sheet
- HPC16400E User's Manual
- CCITT I.430 Basic Access User-Network Interface—Layer 1 Specification
- ANSI T1.605 Specification

1.0 INTRODUCTION

The TP3420/1 SID (S Interface Device) is a complete monolithic transceiver for data transmission on twisted pair subscriber loops. All functions specified in CCITT recommendation I.430 for ISDN basic access at the "S" and "T" interfaces are provided, and the device can be configured to operate either in a TE (Terminal Equipment), in an NT-1 or NT-2 (Network Termination) or as PABX line-card device.

As specified in I.430, full-duplex transmission at 192 kb/s is provided on separate transmit and receive twisted pair wires using Alternate Mark Inversion (AMI) line coding. Various channels are combined to form the 192 kb/s aggregate rate, including 2 "B" channels, each of 64 kb/s, and 1 "D" channel at 16 kb/s. In addition, the 800 b/s multiframe channels for layer 1 maintenance is provided.

All I.430 wiring configurations are supported by the SID, including the "Passive Bus" for up to 8 TE's distributed within 200 meters of low capacitance cable, and point-to-point connections up to at least 1500 meters. Adaptive signal processing enables the device to operate with low bit error rates on any of the standard types of cable pairs commonly found in premise wiring installations.

This user's guide is intended to complement the device data sheets and is primarily aimed at ISDN TE, NT1, NT2 and TA designs that incorporate SID S/T transceivers. The user should refer to the TP3420, TP3421, TP3075/3076 ISDN COMBO and HPC16400E data sheets for specific functions supported by these devices.

2.0 LINE INTERFACE AND TRANSMISSION PERFORMANCE

The components that are integral parts of the system design around the S/T interface and work in conjunction with the SID are dealt with in this section. Choice of the appropriate components will lead to reliable equipment design and superior performance.

2.1 Master Clock Source

The clock source for TP3420/1 may be provided with a commercially available crystal or an external clock source meeting the frequency requirements as explained in the following sections.

2.1.1 Crystal Oscillator

The SID clock source may be either a quartz crystal operating in parallel mode or an external signal source at 15.36 MHz. The complete oscillator (crystal plus the oscillator circuit) must meet a frequency tolerance specification of ±100 ppm total to comply with the CCITT I.430 specification for TE applications. The frequency tolerance limits span the conditions of full operating temperature range (commercial or industrial) and effects due to aging and part-to-part parameter variations.

The crystal is connected between pin 5 (MCLK/XTAL) and pin 6 (XTAL2), with a 33 pF total capacitance from each pin to ground as shown in *Figure 1*. The external capacitors must be mica or high-Q ceramic type. The use of NP0 (Negative-Positive Zero coefficient) capacitors is highly recommended to ensure tight tolerance over the operating temperature range. The 33 pF capacitance includes the external capacitor plus any trace and lead capacitance on the board.

Crystal Requirements:

Nominal frequency of 15.360 MHz, frequency tolerance (accuracy, temperature and aging) less than ±60 ppm, with $R_S < 150\Omega$, $C_L = 20$ pF, parallel mode, CO (shunt capacitance) < 7 pF.

An external circuit may be driven directly from the pin XTAL2 (pin 6) provided that the load presented is greater than 50 kΩ shunted by a total of 33 pF of capacitance.

Crystal oscillator board layout is critical and should be designed with short traces that do not run parallel when in close proximity (to minimize coupling between adjacent pins). On multi-layered boards a ground layer should be used to prevent coupling from signals on adjacent board layers. Ground traces on either side of the high frequency trace also helps isolate the noise pickup.

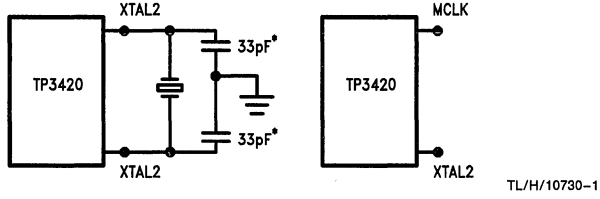
2.1.2 External Oscillator Configuration

An external 5V drive clock source may be connected to the MCLK (pin 5) input pin of the SID as shown in *Figure 1*. The nominal frequency should be 15.36 MHz with a tolerance of ±80 ppm. The SID provides a load of about 7 pF at the MCLK input pin.

2.1.3 List of Recommended Crystal Manufacturers

Monitor Products Co., Inc.
502 Via Del Monte
Oceanside, CA 92504
(619) 433-4510

Part No. MM-38A 15.36 MHz N
Freq. Tolerance (Total) ±60 ppm



*This includes the trace and lead capacitance on the board

FIGURE 1. Clock Circuits

2.2 Line Transformer Requirements

The electrical characteristics of the pulse transformer for the ISDN "S" interface are defined to meet the output and input signal and the line impedance characteristics as defined in CCITT recommendation I.430. The transformer provides isolation for the line card or terminal from the line; it also provides a means to transfer power to the terminal over the S-loop via the 'phantom" circuit created by center-tapping the line side windings. A transformer is used both at the transmit and the receive end of the loop. These notes specify the tolerances of a transformer that is employed with the SID to meet the CCITT recommendation on output pulse mask and impedance requirements.

2.2.1 Line Transformer Ratio

The transmit and the receive transformers can be the same (with a winding ratio of 1:2) or optionally, the receive transformer could have a transformer ratio of 1:1. The primary of the transformer is connected to the S loop while the secondary is connected to the device.

Transmit and Receive Transformer:
Turns ratio (Np/Ns) = 1:2 ±1%

Optional Receive Transformer:
Turns ratio (Np/Ns) = 1:1 ±1%

2.2.2 Line Transformer Electrical Parameters

The tolerance on the electrical parameters of the 1:2 line transformer are tabulated in Table I below.

TABLE I. Line Transformer Electrical Parameters

Parameter	Min	Typ	Max	Units
Ns/Np	1.98	2	2.02	—
Lp	22	30	37.5	mH
Ls	80	120	150	mH
Rp			12	Ω
Rs			5	Ω
LLp			16	μH
LLs			32	μH

The parameter mnemonics and their significance are explained in the paragraphs below.

The total capacitance looking into the primary winding when the secondary is open circuit should be ≤ 220 pF.

Line Transformer Winding Inductance (Lp, Ls)

The total inductance looking into the terminal from the "S" loop should be greater than 22 mH (> 2.5 kΩ between 20 kHz and 80 kHz). This is necessary to meet the low frequency output impedance specification in I.430 of > 2500Ω for frequencies ≥ 20 kHz. The primary winding of the transformer (the main component of inductance) should therefore have greater than 22 mH of inductance (Lp). The secondary winding inductance (Ls) is generally 4 Lp for the 1:2 transformer and Ls = Lp for the 1:1 transformer.

Total Capacitance at the Terminal End

I.430 specifies that the impedance into the Transmitter and Receiver must be > 2500Ω for frequencies < 80 kHz in a TE. The capacitance dominates this impedance, and must be limited to < 795 pF.

There are various contributors to this output capacitance:

— The TE cord, 300 pF (for the 7m length) capacitance or 350 pF (for the 10m length).

— the device driver pins, 10 pF–25 pF.

— The over-voltage protection circuit consisting of shunting diodes (8 pF).

The 1:2 transformer multiplies the capacitance on its secondary connections by 4 when observed from the line side. An allowable maximum for other distributed stray capacitances; Cd, is given by:

7m Cord Case: $(25 + 8) \times 4 + Cd + 300 \leq 800$ pF
which gives $Cd \leq 368$ pF

10m Cord Case: $(25 + 8) \times 4 + Cd + 350 \leq 800$ pF
which gives $Cd \leq 316$ pF

This is the most stringent case and determines the maximum allowable distributed capacitance Cd for the transformer and other miscellaneous capacitances.

Total Capacitance at the Network End

At the network end, there is no cord specified but the 2500Ω minimum impedance limit extends up to 106 kHz. The total capacitance must therefore be < 600 pF, hence:

$(25 + 8) \times 4 + Cd \leq 600$ pF
which gives $Cd \leq 468$ pF

By restricting the Cd for the transformer to be ≤ 220 pF, sufficient margin is allowed for miscellaneous capacitances and flexibility in the protection circuit arrangement.

Line Transformer Winding Resistance Rp and Rs

Since the device output driver is a voltage-limited current source type, the value of the DC resistance of the transformer secondary is not critical.

The DC resistance of the primary side of the transformer does affect the load seen by the current source driver and hence needs to be constrained in order to meet the overall specification of ±10% maximum variation of the output pulse height when terminated into 50Ω.

Line Transformer Leakage Inductance

Unlike competing devices the TP3420/1 controls the output pulse transition times, and hence the leakage inductance is not critical. Overshoot and ringing are within the pulse mask for values in excess of 50 μH.

Longitudinal Balance

The longitudinal balance specification is as follows:

10 kHz to 300 kHz: ≥ 54 dB
300 kHz to 1 MHz: Value decreasing at 20 dB per decade.

Bifilar windings on the line side are necessary to meet these requirements.

2.2.3 Printed Circuit Board Layout Considerations

Taking care of the pcb layout in the following ways will help prevent noise injection into the receiver front-end and maximize the transmission performance:

place the transformer and TP3420/1 on the same ground plane;
keep short connections between the transformer and TP3420/1;
keep short connections from the transmission lines to the transformer;
minimize crosstalk between the transmit and receive pairs;
minimize crosstalk from the crystal into the transmit and receive pairs.

2.2.4 Recommended Line Transformer Manufacturers

Preliminary tests indicate that the following transformers with the TP3420/1 meet the CCITT I.430 requirement for pulse mask and output impedance parameters:

Pulse Engineering:
Part No: PE64995. Phone: 619-268-2454.

MID-COM:
Part No: 571-5915. Phone: 605-886-4385 or 1-800-643-2661.

Vernitron Corporation (AIE Magnetics):
Part No: 328-0044 Phone: 813-347-2181.

2.3 External Protection Circuitry

Precautions are to be taken to ensure that the TP3420/1 is protected against electrical surges and other interferences due to electromagnetic fields, power line faults and lightning discharges that may occur in the transmission medium. Protection circuits that are external to the device are recommended on both the primary and secondary sides of the line transformer. *Figure 2* provides a full protection circuit for the SID in TE mode. The diode stacks at the Lo and Li pins of the device are primarily provided to offer low impedance paths to electrical surges. On the transmit side in a TE they also avoid the clamping of the signals from other TE's and ensure that the minimum output impedance requirements are met even if V_{CC} is lost. In NT/LT applications only a single diode from each Lo pin to V_{CC} is required. External resistors in the receive path of the SID limit the surge current through the diodes and also form part of the low pass noise limiting input filter. This circuit can withstand at least 1000V pulses on the S interface. All the diodes in this circuit are of the type 1N4004. Low capacitance diodes are necessary to avoid exceeding the maximum allowed capacitance for the complete connecting cord and circuit impedance.

For surge protection on exposed wiring interfaces, a low capacitance gas discharge tube should be added across the terminals as shown in *Figure 2*. In addition to surge protection, the transformer must be protected against power line faults by the addition of fuses or low value ($<10\Omega$) fusible resistors. The series resistance of the protection must however, be taken into account when specifying the resistance of the transformer windings, to ensure that the transmit pulse mask requirements are met.

2.3.1 DC Bias Capacitors for Analog Reference

Two decoupling capacitors (0.1 μF mica) and 10 μF (electrolytic) are connected between pin 19 of the device and its ground connection. These capacitors decouple the midpoint of a two-resistor potential divider (inside the device) and provide an internally buffered reference for the analog circuitry.

2.4 Transmission Performance

The TP3420/1 SID is designed with the goal of substantially exceeding the transmission performance requirements as specified in the I.430. This is made possible in the design by employing complex signal-processing techniques in the receiver front end design. For example, in the receive path, an analog prefilter removes >200 kHz noise signals, which is then followed by an adaptive line equalizer to correct for the attenuation of loops in excess of 1.5 km in length with superior performance. A continuously tracking adaptive threshold circuit optimizes the slicing levels in the detection circuits for correct detection of received data even on long lossy loops. Finally a digital filter discriminates against in-band noise. This architecture results in longer range error-free transmission in point-to-point applications, and greater spread of terminals in extended passive bus applications than simpler first-generation tranceivers.

The SID transmission performance was measured on 24 AWG PIC cable which has approximately 90 nF/km capacitance and 180 Ω/km resistance. This cable has a loss of 7.8 dB/km at 96 kHz. Performance was measured with three different configurations, namely:

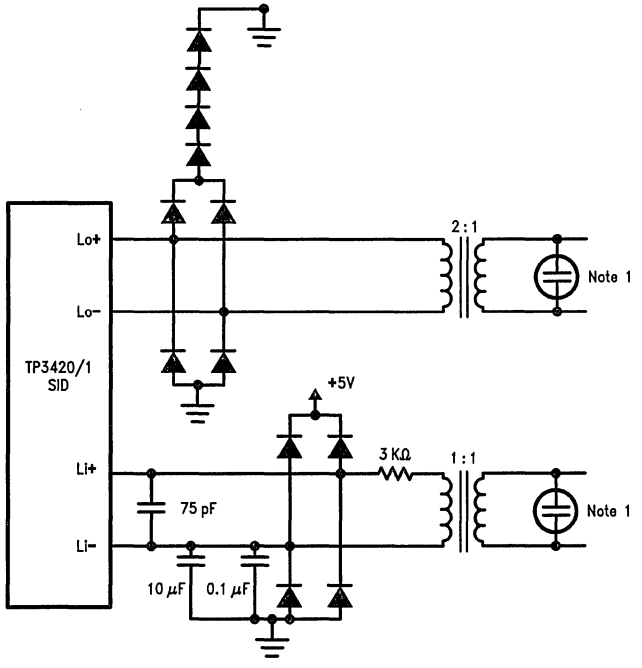
1. Point-to-Point;
2. Short Passive Bus;
3. Extended Passive Bus.

In all these tests, noise sources recommended by the I.430/ANSI standard per Section 8.6.2.1 were complied with. The setups are shown in *Figures 3, 4* and *5*, along with the tables showing the actual range measured versus the I.430 recommended range. Noise sources were located close to the NT receiver and injected via two 1 kΩ resistors to avoid affecting the loop impedance significantly. Activation and error-free transmission could be accomplished on either end of the S interface in the case of the point-to-point configuration and from any one of the TEs in the case of both passive bus configurations. The error-rate was measured in a B channel in these tests.

The TEs and NT in all these configurations used TP3420/1 SIDs. The NT device in the point-to-point and extended passive bus cases was in NTA mode while the short passive bus used NTF mode. The results tabulated show that the SID exceeds the I.430 and ANSI range requirements.

Pulse Shape and Impedance Templates

As shown in *Figure 6*, the TP3420/1 SID transmitter output pulse shape and amplitude comply with the specified pulse masks for both the 50Ω and 400Ω test load impedance cases. Plots in *Figures 7a* and *7b* show the receiver input impedance and output impedance. These tests were done with the recommended Pulse Engineering transformers. The SID output drivers are specifically designed with controlled rising and falling transitions for minimal pulse overshoot and undershoot with a wide range of transformer designs. Furthermore, the following figures show the transmit and receive impedance templates are met with the specified cable connected and the protection networks shown in Section 2.3. The device has been successfully tested for pulse shape and impedance with various other manufacturers' transformers.



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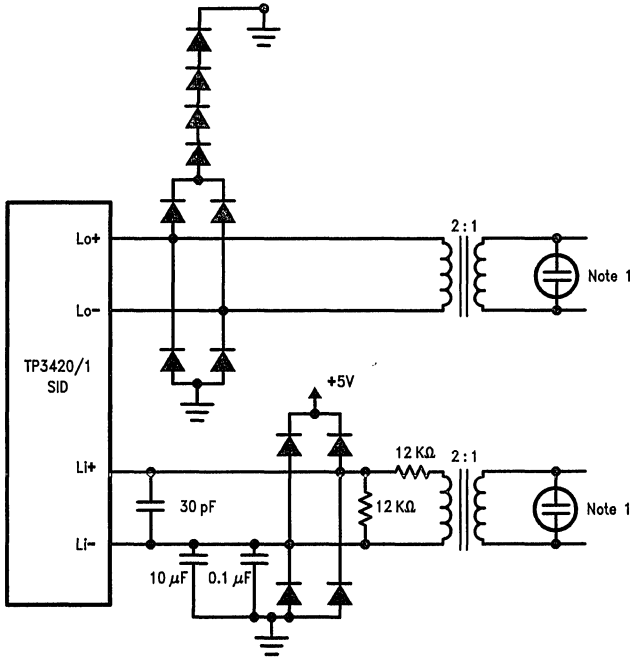
Note 1: Not normally required if TE is used only on internal wiring.

FIGURE 2a. External Protection Circuit—TE Application, Receive Transformer Ratio = 1:1



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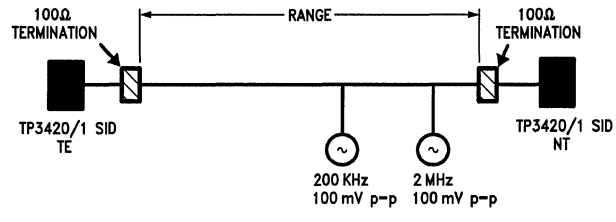
Note 1: Not normally required if TE is used only on internal wiring.

FIGURE 2b. External Protection Circuit—TE Application, Receive Transformer Ratio = 2:1



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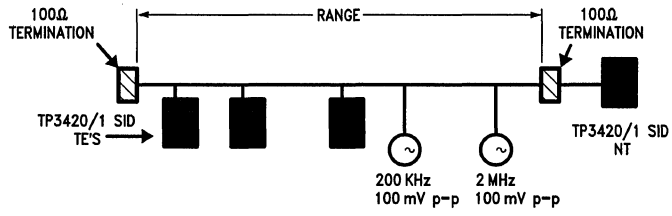
TP3420 SID	I.430 Specification
1800m	1000m

FIGURE 3. SID Point-to-Point Range Measurement



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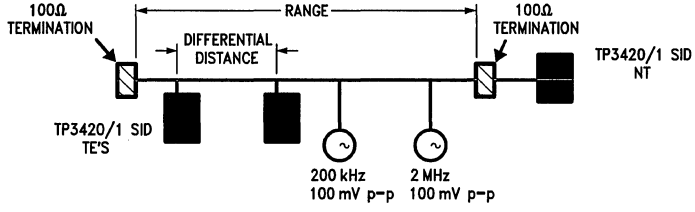
TP3420 SID	I.430 Specification
200m	100m–200m

FIGURE 4. SID Short Passive Bus Range Measurement



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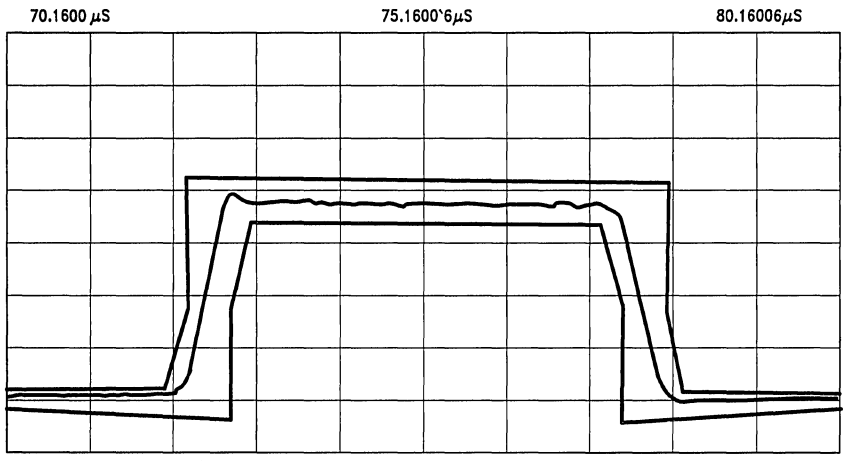
TP3420 SID		I.430 Specification	
Range Meters	Differential Distance Meters	Range Meters	Differential Distance Meters
675	275	500	25 to 50
1075	275		
1250	250		
1500	100		
1650	50		

FIGURE 5. SID Extended Passive Bus Range Measurement



FUNCTION1 = 200.6 mVOLTS/DIV
TIMEBASE = 1.00 μS/DIV

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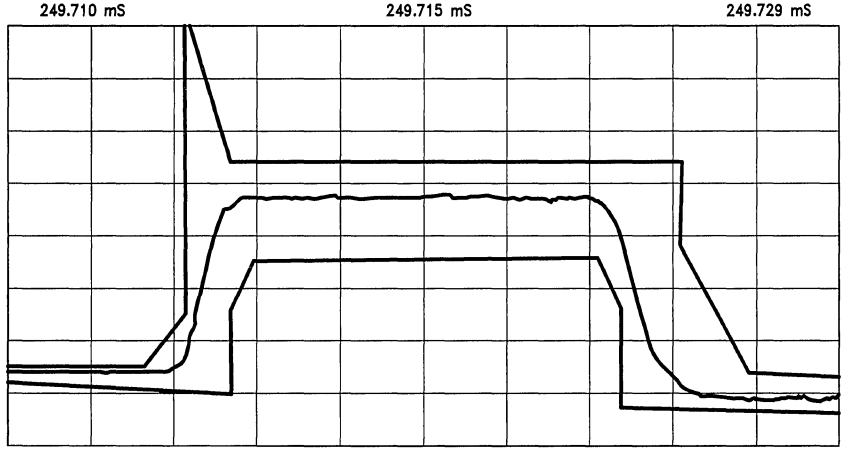
FIGURE 6a. SID Output Pulse Shape and Amplitude vs Mask (50Ω)



CH. 1 = 299.5 mVOLTS / DIV
TIMEBASE = 1.00 μS / DIV

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FIGURE 6b. SID Output Pulse Shape and Amplitude vs Mask (400Ω)

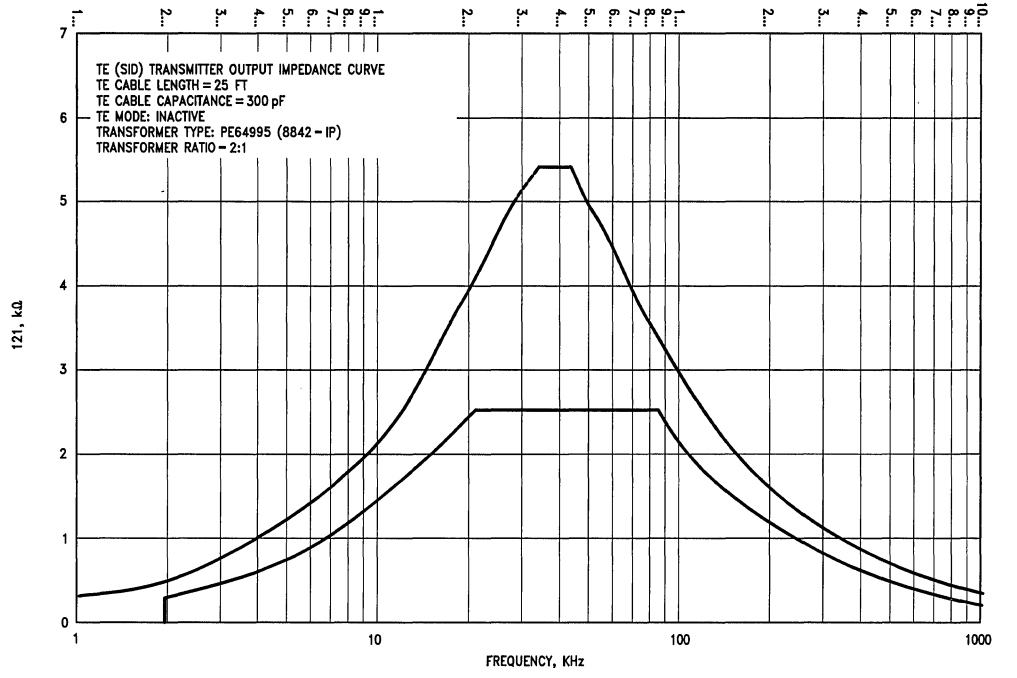

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FIGURE 7a. SID Receiver Input Impedance Curve

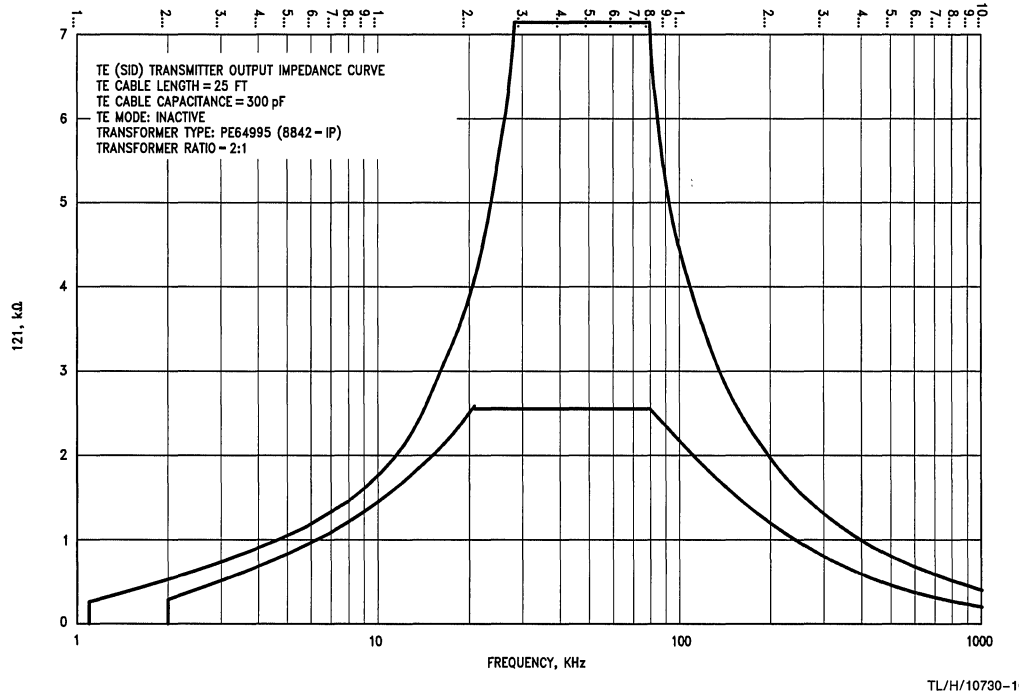

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FIGURE 7b. SID Transmitter Output Impedance Curve

3.0 TP3420 DIGITAL INTERFACE

To retain the flexibility of interfacing the TP3420 with a variety of other products, two digital interfaces are provided on this device. The first interface is called the Digital System Interface (DSI) and is for synchronous transfer of B and D channel information in one of the several popular schemes which encompass proprietary frame structures such as COMBO, IOM, SLD and IDL. The second interface is National's popular MICROWIRE/PLUS interface which provides a means for synchronous serial data transfer between a microcontroller and one or more peripheral devices and is used for device mode control purposes.

The TP3421 device uses the GCI interface format, see the TP3421 Datasheet.

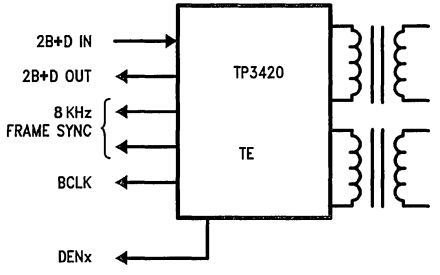
3.1 Digital System Interface Formats

The Digital System Interface (DSI) combines B1, B2 and D channel data onto common pins Br and Bx to provide maximum flexibility. At this interface, phase skew between transmit and receive directions may be accommodated at the line card or NT-1/2 end since separate frame sync inputs FSa and FSb are provided. Each of these synchronizes a counter which gates the transfer of B1 and B2 channels in consecutive time-slots across the digital interface. The serial shift rate is determined by the BCLK input and may be any frequency from 256 kHz to 4.096 MHz. Thus, for applications on a PABX line card (in NT mode), the B1, B2 and D channel slots can be interfaced to a TDM bus and assigned to a time slot.

At the TE end, FSa is an output indicating the start of both the transmit and receive B channel data transfers. BCLK is also an output at the serial data shift rate, which is dependent on the DSI format selected. *Figure 8* illustrates the directions of BCLK, FSa and FSb clocks depending on the device mode TEM and TES or NT mode respectively.

Four multiplexed formats of B1, B2 and D channel data are supported by TP3420 SID and selection of these formats is via the control register.

TE Mode: DSI Master (TEM)



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NT Mode DSI Slave (NTA or NTF) and TE Mode DSI Slave (TES)

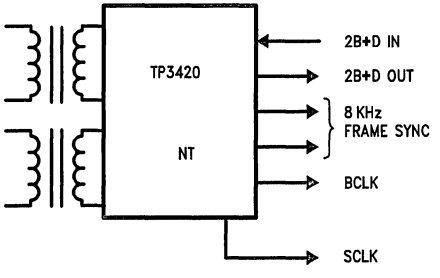

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FIGURE 8. TP3420 SID Digital System Interface

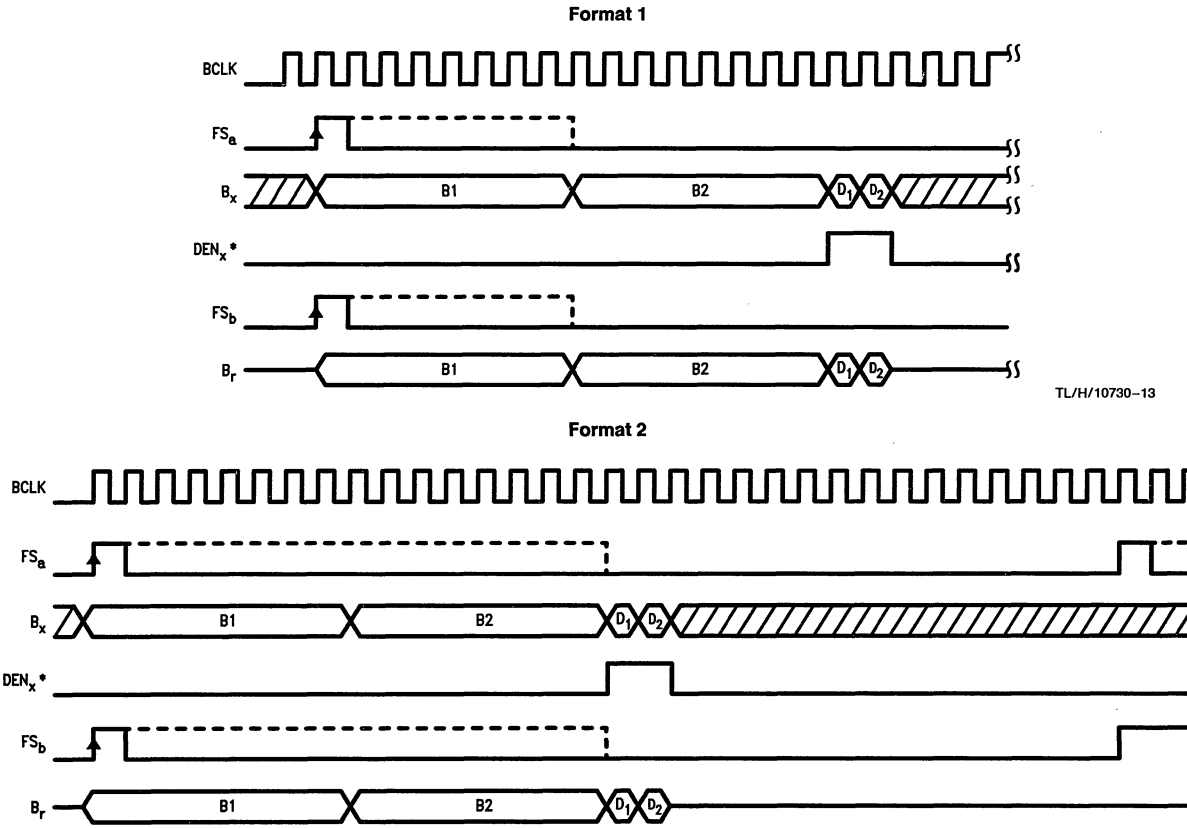
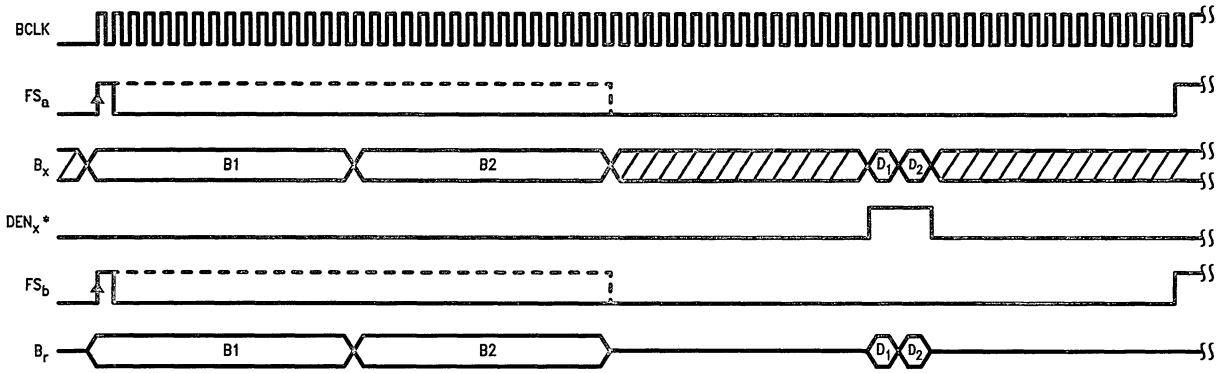


FIGURE 9. Digital System Interface Formats in NT and TES Modes

Format 3



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Format 4

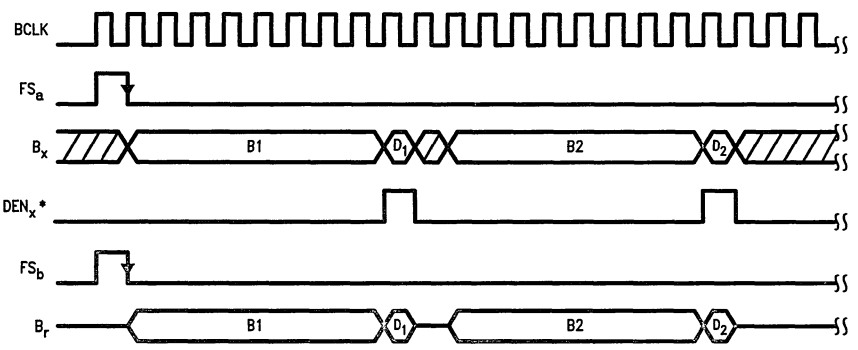

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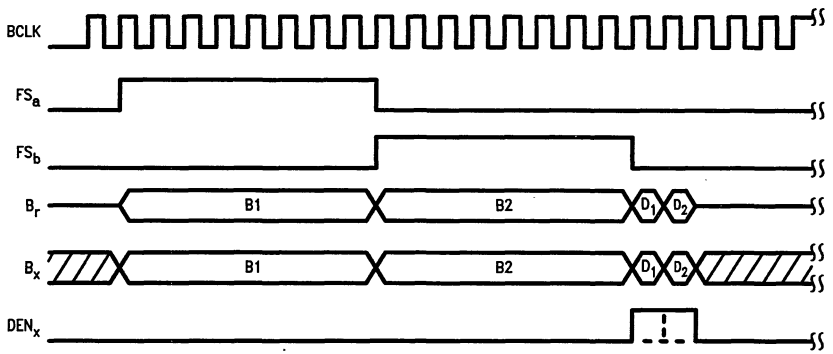
FIGURE 9. Digital System Interface Formats in NT and TES Modes (Continued)

Format 1



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Format 2

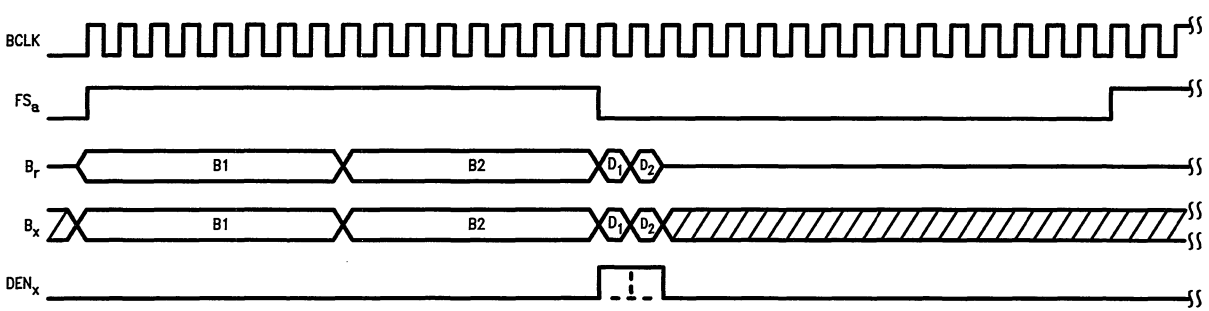

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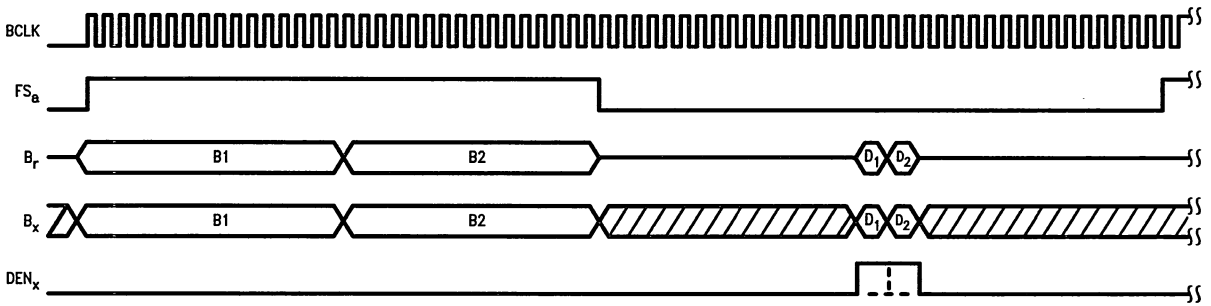
FIGURE 10. Digital System Interface Formats in TEM Mode

Format 3



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Format 4

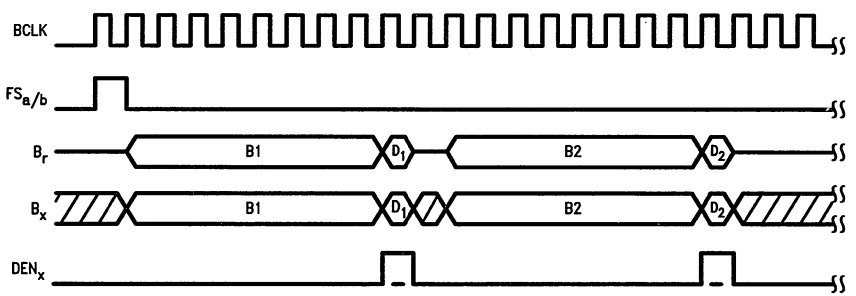

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FIGURE 10. Digital System Interface Formats in TEM Mode (Continued)

Figure 9 illustrates the four Digital Interface Formats for the NT and TES modes of the SID device and *Figure 10* shows these formats for the TEM mode. Table II presents the BCLK rates of the four DIF formats in both the Master and Slave modes.

TABLE II. DSI Format Rates

Format	BCLK as DSI Master	BCLK as DSI Slave
1	2.048 MHz	2.56 KHz–4.096 MHz
2	256 kHz	"
3	512 kHz	"
4	2.56 MHz	"

3.2 TP3420 SID Digital System Interface and HPC16400E Connection

TP3420 SID, when used with National's HPC16400E Microcontroller, provides an elegant ISDN solution for TE and Line-card architectures. While the SID implements all the S interface functions, Layer 2 and 3 signaling and protocol layer procedures may be implemented in the HPC16400E by connecting the D-channel to HDLC#1 via the Digital System Interface. At the same time, one of the B channels may be routed to HDLC#2 on the HPC16400E for data protocol implementations.

The Serial Decoder block of the HPC16400E provides a means of flexible configuration of the device for various applications. *Figure 11* illustrates a simple block diagram functional description of the serial decoder and the various signals associated with it. The serial decoder is controlled by the contents of the SERDEC register of the HPC16400E.

Because the TP3420 has four different formats for multiplexing B and D channels on its Digital System Interface, it is important to setup the HPC16400E in the correct mode for compatibility with the chosen digital interface format from the TP3420 as shown in Table III below:

TABLE III. Relationship between the HPC Serial Mode and the SID DIF Format

HPC Serial Mode	SID DIF Format
4	1
4	2
3	3
7	4

This is done by the upper 3 bits of the SERDEC register in the HPC16400E.

The serial decoder of the HPC16400E in conjunction with the ENABLE SELECT logic provides the enable signal for data multiplexing. The serial decoder services the 2 HDLC channels (for a detailed discussion on the Serial decoder please refer to the HPC16400E data sheet). For each HDLC channel, there are two ENABLE SIGNALS, one for the Receiver and one for the TRANSMITTER. Each HDLC channel ENABLE signal can be connected to the EXTERNAL RECEIVER/TRANSMITTER ENABLE (REN1, TEN1, REN2 and TEN2) or the Internally Generated Enable strobe signals (B1, B2 and D) or can be used for ANDing of the EXTERNAL ENABLE and INTERNAL channel strobe signal. The HDLC Channel Enable Signals are selected by setting the 5 lower SERDEC register bits as shown in Tables IV and V:

TABLE IV. HDLC Enable Signals for Channel #1

Case	SERDEC Bit			TX1	RX1
	2	1	0		
1	x	0	0	D & TEN1	D
2	x	0	0	TEN1	D
3	1	1	0	B1	B1
4	1	1	1	B2	B2
5	0	1	1	TEN1	REN1
6	0	1	1	TEN1	B1

TABLE V. HDLC Enable Signals for Channel #2

Case	SERDEC Reg Bit			TX2	RX2
	4	3	2		
1	0	0	0	B1	B1
2	0	0	1	B2	B2
3	0	1	0	TEN2 & B1	REN2 & B1
4	0	1	1	TEN2 & B2	REN2 & B2
5	1	0	x	1	1
6	1	1	x	TEN2	REN2

3.2.1 TP3420 SID and HPC16400E Connection for D-Channel

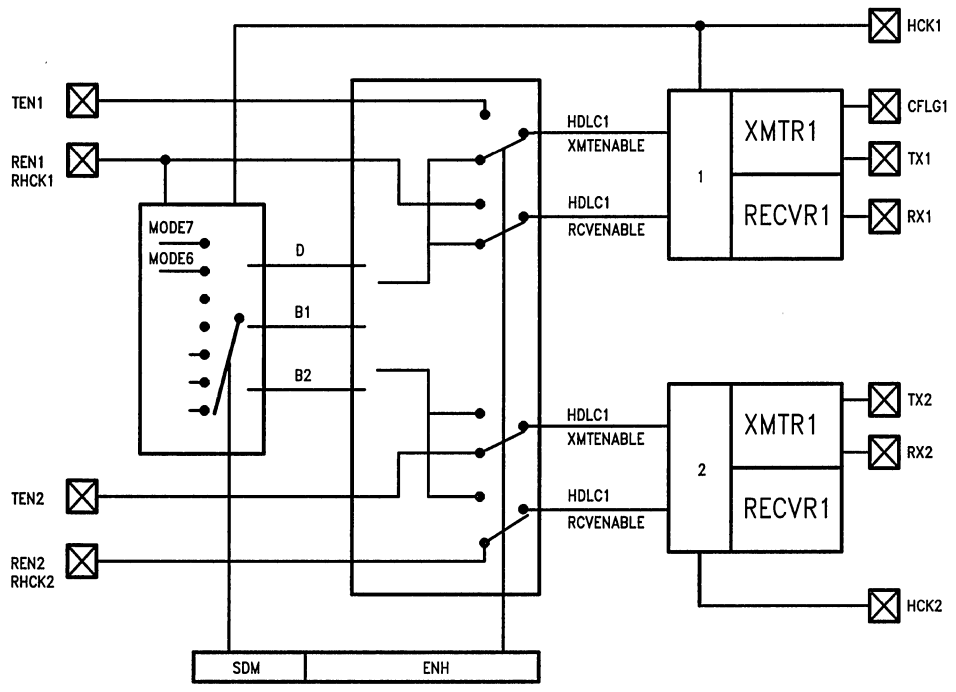
Figure 12 shows the connection of TP3420 SID's Digital System Interface signals to the HPC16400E serial decoder and HDLC Controllers 1 and 2 for the D-channel and B channel respectively. For D-channel selection into the HDLC#1, the FSa signal on the DSI has to be connected to the REN1 (pin D0) signal on the serial decoder/HDLC #1. In this application Case 1 of HDLC enable signals for channel #1 in Table IV is used.

3.2.2 TP3420 SID and HPC16400E Connection for B Channel

For B channel selection into the HDLC#2, Case 1 or Case 2 of the HDLC enable signals for channel #2 for B1 or B2 channel respectively is used from Table V.

3.3 TP3420 SID Digital System Interface and TP3076 COMBO Connection

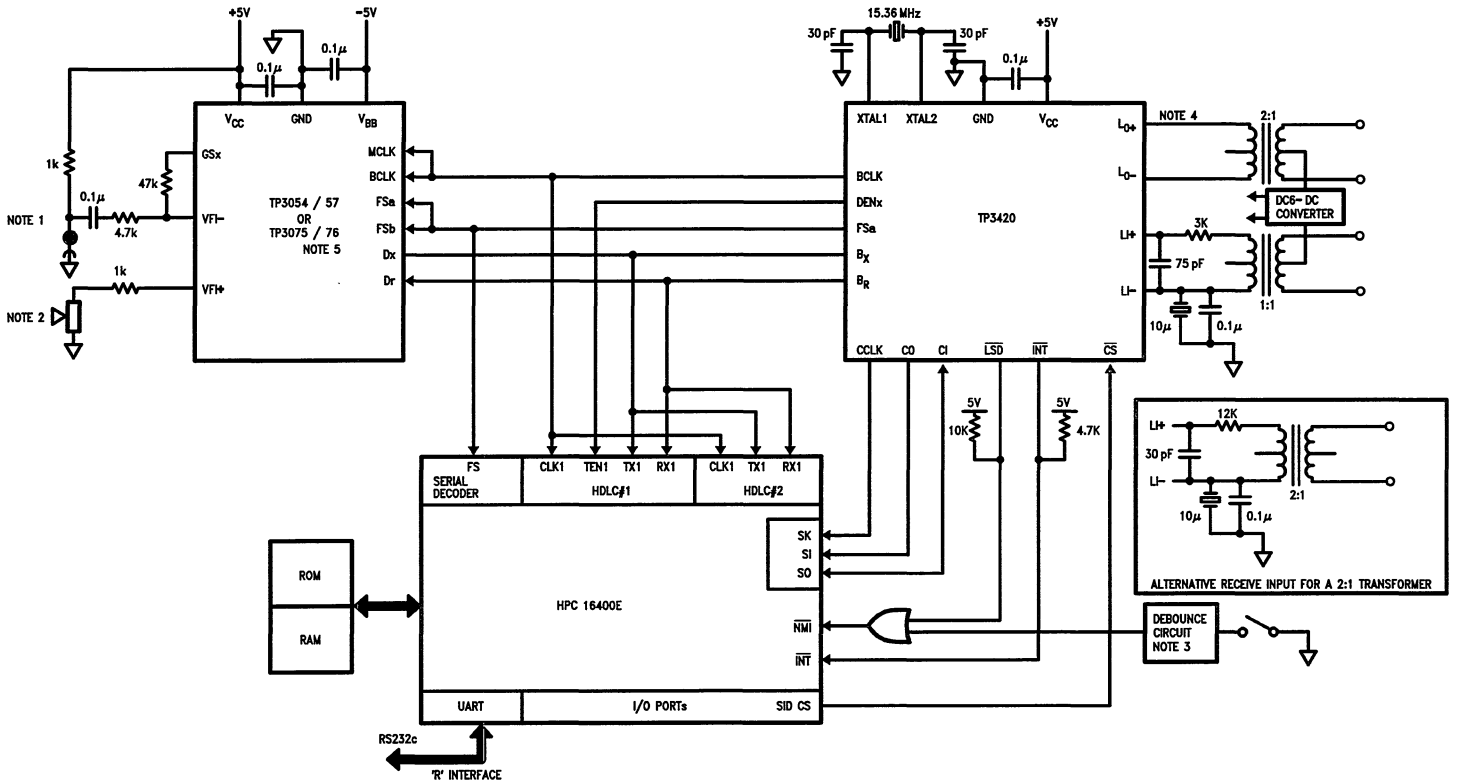
When one of the B channels in the ISDN stream is PCM coded voice, an ideal solution is to connect this B channel to a TP3075/TP3076, National's PCM CODEC/filter for ISDN. The TP3075/3076 are second generation combined PCM CODEC and filter devices optimized for digital telephone applications. The devices are A-law and μ-law programmable and employ a conventional serial PCM interface capable of being clocked up to 4.096 MHz. A number of programmable functions, including the transmit and receive gains, may be controlled via a serial control port. Please refer to TP3075/TP3076 data sheet for more details.



TL/H/10730–21

Note: All switches are independent. This diagram does not show ANDing of internal and external enables.

FIGURE 11. HPC16400E Serial Decoder Block



TL/H/10730–22

Note 1: Primo type EM80-PMI2 or similar

Note 2: Primo type DH31 or similar

Note 3: Only necessary if a mechanical switch is connected to the NMI input of the HPC

Note 4: See Line Interface Protection circuit section.

Note 5: When using TP3075/76, connect the MICROWIRE bus to the part.

FIGURE 12. Typical Application in a TE and/or TA

The diagram of *Figure 12* shows the connection between the TP3420 and TP3076 in the implementation of an ISDN phone. TP3420 SID is programmed for DIF1 format at the DSI in this application. Besides, the voice channel should always be in B1 slot of the DIF FORMAT1 for this setup to work. If the network assigns the B2 channel to a voice call, it has to be switched into the B1 slot in the DSI frame format using the command BEX in the TP3420 control register. The FSx, FSr pins on the TP3076 are connected to the Fs pin on the TP3420. MCLK, BCLK on the TP3076 are connected to BCLK on the TP3420, and Dx, DR signals on the TP3076 are connected to Bx and Br signals respectively on the TP3420 SID. Under these conditions, and assuming μ-law is chosen, for proper operation the control register on the TP3076 is programmed as follows:

TP3076 Control Register Contents

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0

In this case, the TP3076 is in non-delayed timing mode and the time slot always begins with the leading edge of frame sync input FSx, FSr.

3.4 NT-2 Synchronization (TP3420/1)

This section applies to both the TP3420 and TP3421.

The NT-2, typically a PBX, has a number of S interfaces on the customer's side and, if it uses Basic Access to the network, each trunk is a T interface to an NT-1 as shown in *Figure 13.* Functionally the S and T interfaces are identical, i.e. both conform to I.430. Thus, the SID can operate on the S interface side, with NT mode selected (either fixed or adaptive receive sampling as appropriate for the wiring), and on the T interface side the SID operates like a terminal, in TE mode. However, the complete NT-2 must have all its clocking and data interfaces synchronized to the network. This requires a system clock, at typically 2.048 MHz, to be phase-locked to one of the T interfaces. The SID includes this PLL, with an SCLK output on the DENx pin, when used in TE mode DSI Slave (TES) only. Any one of the SID's can provide this clock, but all will take their BCLK and Fs timing from the same one, i.e. they are slaved to the network clock and synchronized to each other. In this way, clocking is synchronized all the way from the network to the terminal.

3.5 Slave-Slave Mode and Elastic Buffers (TP3420/1)

This section applies to both the TP3420 and TP3421.

When SID is used in TE mode (TES), it is a timing slave to the network, but the digital interface is also in a slave mode, i.e., Fs and BCLK are inputs and is referred to as "slave-slave" mode. A typical slave-slave application is on the network side of an NT-2, or PBX, at the T interface. Not only does this application require the device to cope with arbitrary phase relationships between the I.430 receive frame and the 8 kHz Fs, but also the possibility of "slips" arises. A slip may occur when the frame phase relationships across the device are not fixed, but jitter sufficiently to cause loss of data and frame sync. At frequencies below 10 Hz this form of jitter is called "wander", and CCITT specification Q.502 shows that wander up to 18 μs peak-peak may arise over a 24 Hour period. An elastic store is included in both the transmit and receive paths of the SID for two reasons:

1. To allow complete flexibility for any time-slot to be assigned at the digital interface, regardless of the phase of the receive I.430 frame. In addition, separate FS inputs for transmit and receive allow them to have independent frame and time slot alignments.
2. To absorb wander between the frame phases across the device up to the limits specified in Q.502.

Each elastic store, in conjunction with some control circuitry, is used to adjust the output timing requirements gradually for error free transmission performance. *Figure 14* shows the general mechanism supported by the SID in either direction which utilizes a serial-to-parallel converter, a buffer and a parallel-to-serial converter. The incoming data (2B + D) is transferred into the register as each word is accumulated in the serial-to-parallel converter. Some time later, data in the buffer is transferred to the output parallel-to-serial converter as a complete word is shifted out. The wander detector circuit controls the transfers to the parallel-to-serial converter in such a way as to absorb wander by varying delays through the elastic store. The SID is designed to absorb the CCITT wander specified over 24 hours, which can be up to 18 μs peak-to-peak.

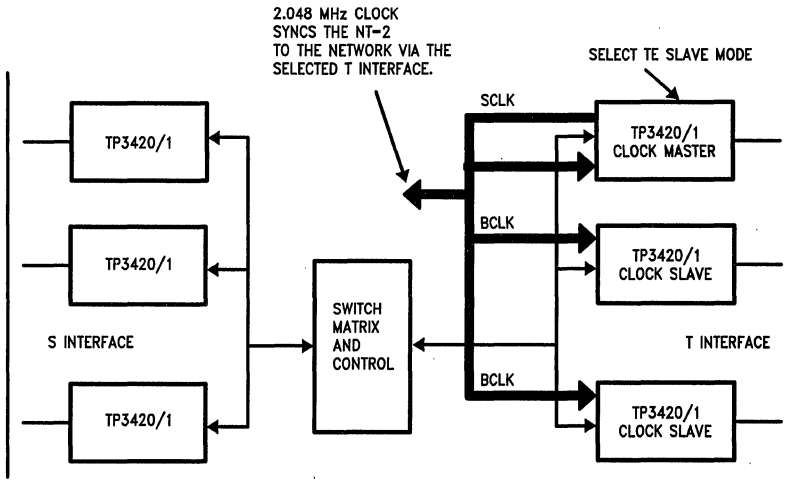
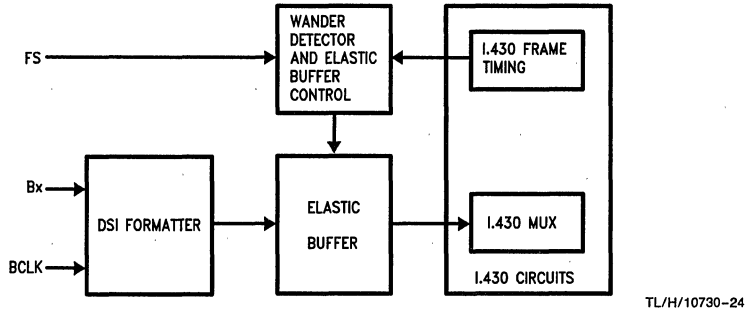


FIGURE 13. TP3420/1 Showing NT-2 Synchronization



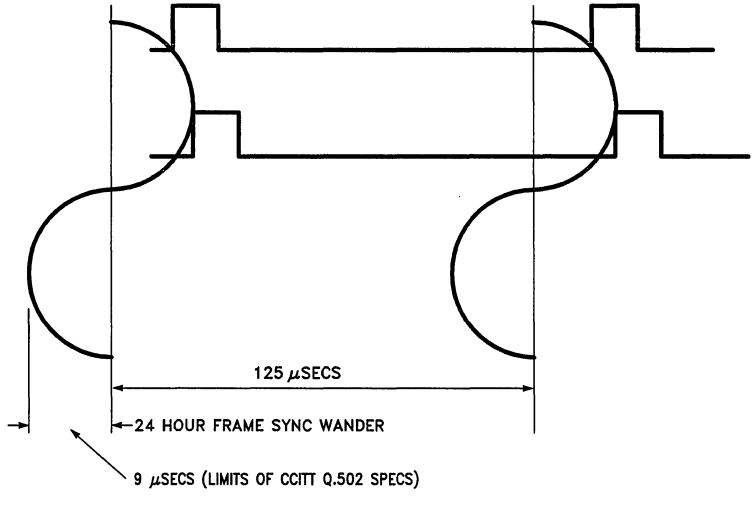
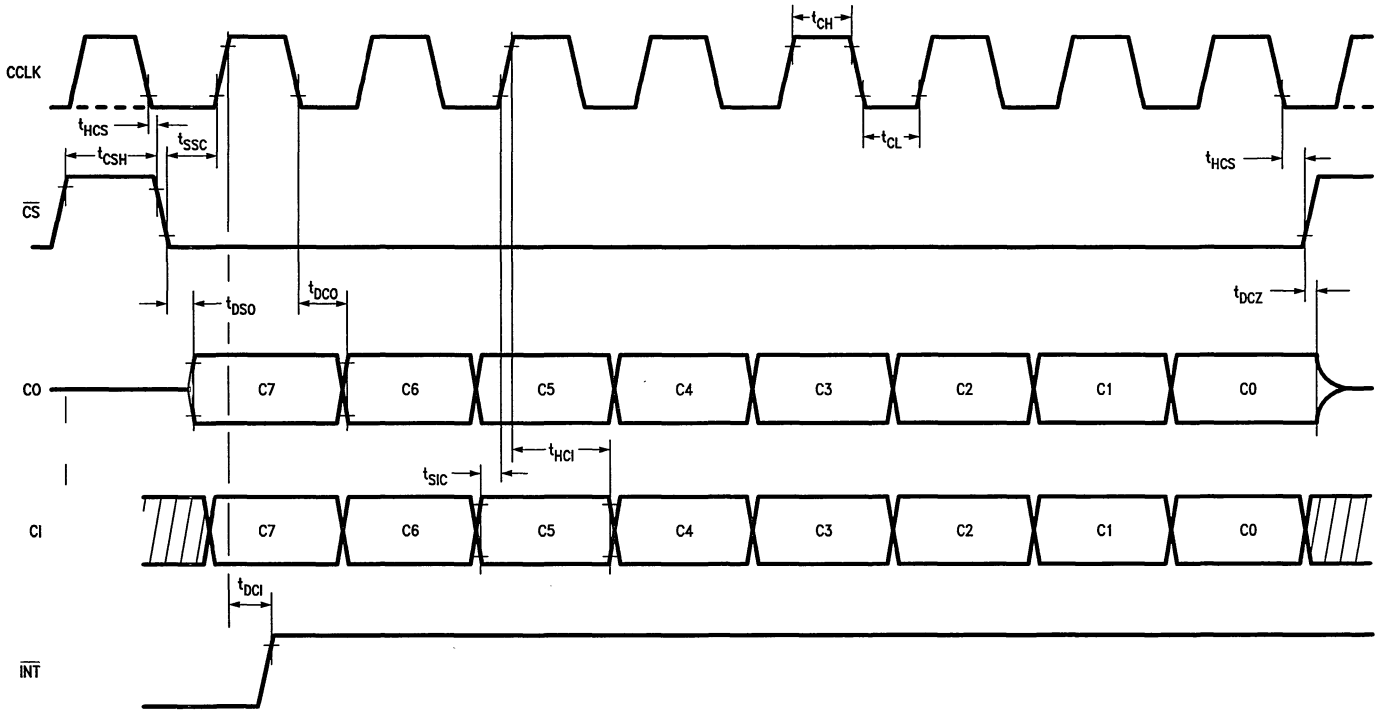


FIGURE 14. TP3420/1 Slave-Slave Mode and Elastic Buffer (TX Side)



TL/H/10730–26

FIGURE 15. TP3420 Microwire Control Interface Timing

4.0 DIGITAL CONTROL INTERFACE (TP3420 Only)

The digital control interface for the TP3420 SID is compatible with National's industry standard MICROWIRE/PLUS™ interface. This approach provides easy integration into already existing microcontroller applications.

4.1 The MICROWIRE Bus

The MICROWIRE compatible interface on the TP3420 is provided for microprocessor control of various functions in the device. MICROWIRE is used for slow speed control and status data, while all the real time user data in B and D-channels is routed via the DSI so that speed of response to interrupts is not a critical issue.

In the MICROWIRE control interface implementation in the TP3420, with reference to the control interface timing shown in *Figure 15*, the following actions take place:

Data transfers consist of a single byte shifted into the control register of SID via the CI pin while a single byte is shifted out from the status register of SID via the CO pin.

$\overline{CS}$ is to be pulled low for 8 clock cycles of CCLK.

Data waiting to be received into CI is clocked on rising edge of CLK.

Data waiting to be transmitted out of CO is clocked out on the falling edge of CCLK.

$\overline{INT}$ goes low to alert the microprocessor when changes in the status register occur. $\overline{INT}$ returns to the high impedance state on the rising edge of CCLK after $\overline{CS}$ goes low.

Note: When reading an interrupt from SID, a NOP (hex FF) must be loaded into CI.

4.2 TP3420 SID to HPC16400E MICROWIRE Connection

The MICROWIRE/PLUS interface on HPC16400E has an 8-bit parallel loaded, serial shift register using SI as the input and SO as output. SK is the clock for the serial shift register (SIO). SK clock can be provided from an internal HPC timer or from an external source, and the internal clock is programmable by the DIVBY register. A DONE flag indicates when the 8-bit data shift is completed.

The HPC16400E should be configured in the Master mode for operations in this case. A control bit in the IRCD register determines whether the HPC16400E is in master or slave mode for MICROWIRE/PLUS applications. *Figure 12* illustrates the use of HPC™ MICROWIRE/PLUS in controlling the TP3420 MICROWIRE interface.

4.3 TP3420 SID COMMAND and STATUS Bytes

The control commands and status indication functions supported by the TP3420 allow it to be flexibly used in various sytem applications with relative ease. The command controls are in distinct groups of functions, and in most of these, only one function may be active from each group at a time. There are 32 distinct commands available. Listed below are the various control functions and status indication functions. Please refer to the TP3420 SID data sheet for mnemonic explanations.

Most of these commands and status indicators are common with those used on the TP3421, which has the GCI interface instead of the MICROWIRE interface.

Activation/Deactivation

Command	Status
PDN	LSD
PUP	AP
AR	EI
DR	DI
FI2	
MMA	

Device Modes

Command	Status
NTA	
NTF	
TEM	
TES	

Digital Interface Formats

Command	Status
DIF1	
DIF2	
DIF3	
DIF4	

B1/B2 Channel Control

Command	Status
B1E	
B2E	
B1D	
B2D	
BDIR	
BEX	

D-Channel Access

Command	Status
DREQ1	CON
DREQ2	EOM

End of Message Interrupt

Command	Status
EIE	
EID	

Multiframe

Command	Status
MFT	MFR
MIE	
MID	

Loopback Tests

Command	Status
LBS	
LBL1	
LBL2	
LBB1	
LBB2	
CAL	

4.4 TP3420/1 Receive Timing Recovery

The TP3420/1 has two receive clock timing options available in its system implementations as shown in the conceptual diagram of *Figure 16*.

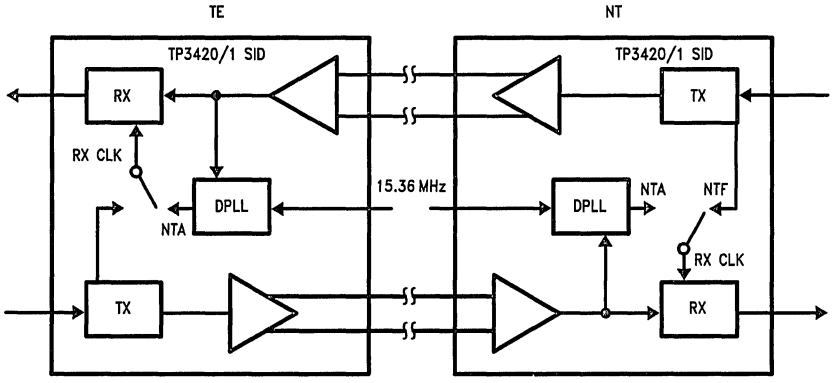
In adaptive timing mode, the DPLL is locked to timing in the received bit stream. This mode is used in TE applications for both point-to-point, short and extended passive bus configurations, whereas in NT mode this is used for point-to-point and extended passive bus configurations only.

For application in the NT of a short passive bus only, the multiple TE's with different round trip delays cause wide variations in the zero crossings so that a DPLL cannot generate a clean clock reliably. Therefore the receive sampling DPLL is bypassed in this mode by selecting the NTF command. In Fixed timing mode, the DPLL is locked to TXCLK and phased at 4 μs with respect to the leading edge of the derived clock. Also, in the fixed timing mode, the equalizer is disabled.

4.5 TP3420/1 Line Signal Detect (LSD) and Wake-Up Signal for μP

The Line Signal Detect circuit in the SID is active when the device is in the power down state. Upon detecting a valid signal, the $\overline{\text{LSD}}$ pin on the device is pulled low from its normally high impedance state, and also the $\overline{\text{LSD}}$ bit in the Status Register is set (TP3420 only). The $\overline{\text{LSD}}$ pin may be used for waking up a local microprocessor from a low power idle mode and subsequently powering up SID itself. The $\overline{\text{LSD}}$ pin goes into the high impedance state upon powering up (PUP) the SID and the LSD circuit in the device is disabled in powered-up mode.

Figure 17 shows a simple concept of using the $\overline{\text{LSD}}$ pin on the TP3420 SID in waking up HPC16400E, the local microcontroller. The LSD signal is tied to the NMI pin of the HPC16400E. When a remote activation request is sensed by the SID, it pulls the $\overline{\text{LSD}}$ pin low and the NMI pin detects the inverted LSD signal to wake-up the HPC16400E. The $\overline{\text{INT}}$ signal on the TP3420 SID may also be used for these wake-up procedures because the LSD bit in the status register may be read upon the $\overline{\text{INT}}$ signal going low.



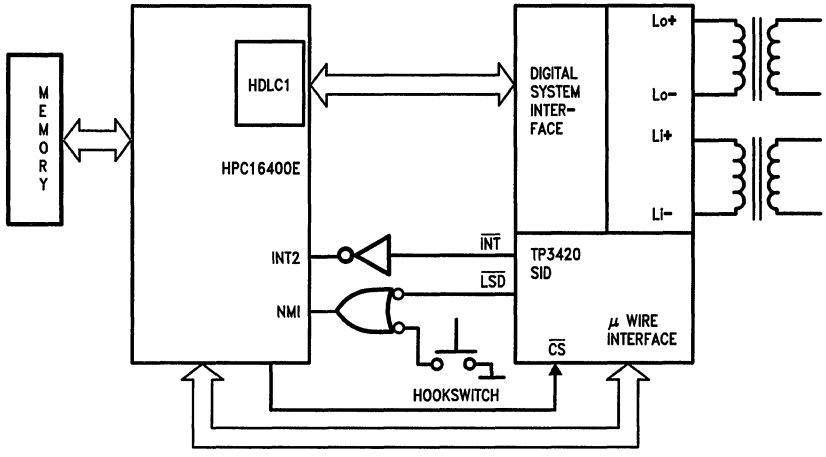
TL/H/10730–27

TP3420/1 SID has 2 RX CLK Timing Options:

1. DPLL Adaptive timing, locked to RX data
   Used in TE mode always
   Used in NT mode for point-point only
2. Fixed Timing, locked to TX CLK and phased at 4 μs after TX edges
   Used in NT mode for passive bus only

The NT/TE bits select both the timing mode and the state machines for activation control.

FIGURE 16. TP3420/1 Receive Timing Circuitry



TL/H/10730–28

FIGURE 17. TP3420 SID, Line Signal Detect Circuit Connection to HPC16400E

5.0 ACTIVATION AND DEACTIVATION USING TP3420 SID AND HPC16400E

TP3420 SID and HPC16400E combination makes an ideal system solution for ISDN terminals (TE's). When this hardware combination is used in a system, implementing CCITT recommended activation and deactivation procedures is simplified considerably. Assuming both the TE and NT ends of the system employ the TP3420 and HPC16400E combination, the activation/deactivation procedures for specific cases are explained below.

Activation procedures for the TP3421 are similar to those described here, but conform to the GCI specification for the C/I (Command/Indicate) Channel (see TP3421 Datasheet).

5.1 S Interface Loop Activation Initiated from the TE End

Figure 18 illustrates various commands and status indications and the resultant INFO signals for a successful activation of the S interface for the case when a TE has initiated the activation procedure. This discussion, however, does not indicate the timers that are required in an activation procedure (see Section 6). The following sequence of events must take place for the TE initiated activation of the S interface:

TE SIDE: TP3420 SID is first powered up and then the AR command is sent. This forces INFO1 pattern onto the S interface towards the NT.

NT SIDE: The TP3420 on the NT side senses the INFO1, and issues an LSD interrupt to the local controller. On powering up the SID, the AP byte in the status register is set and the local HPC must respond by sending the AR command. This causes the NT SID to send INFO2 frames on the S interface.

The TE SID, upon recognition of INFO2 frames, sends INFO3 frames on the S interface.

NT SIDE: Upon recognizing INFO3 frames, the NT SID issues an AI interrupt to the processor to indicate pending activation. Now the HPC repeats the AR command in the TP3420 control register and SID sends INFO4 frames on the S interface.

TE SIDE: The TE SID now receives INFO4 frames and issues an AI indication to the local processor.

NT SIDE: The SID issues an AI indication to the local processor.

At this point the S interface is activated.

5.2 S Interface Loop Activation Initiated from the NT End

Figure 19 illustrates various commands and status indications and resultant INFO signals for a successful activation of the S interface for the case when a NT has initiated activation procedure. This discussion however does not indicate the timers that are required in an activation procedure (see Section 6). The following sequence of events must take place for the NT initiated activation of the S interface:

NT SIDE: TP3420 SID is first powered up and then the AR byte in the command register is sent to initiate the S interface activation procedure. This causes the NT SID to send INFO2 frames on the S interface.

TE SIDE: Upon detecting the received signals across the S interface, the TE SID issues an interrupt to the local HPC indicating LSD. The HPC16400E powers up the TP3420, which then detects valid INFO2 frames and issues AP status indication to the HPC16400E. HPC16400E responds to this by issuing an AR command, causing the TP3420 SID to send INFO3 frames on the S interface.

NT SIDE: Upon detecting the INFO3 pattern on the S interface, the NT SID alerts the local processor by setting the AP interrupt. The NT side processor responds by issuing an AR command, causing the NT SID to send INFO4 frames on the S interface. Also, at this time SID indicates a successful activation of the S interface by issuing an AI status to the local HPC16400E.

TE SIDE: The TE SID, upon recognizing the INFO4 frames, indicates to the local HPC the state of successful activation via the AI interrupt.

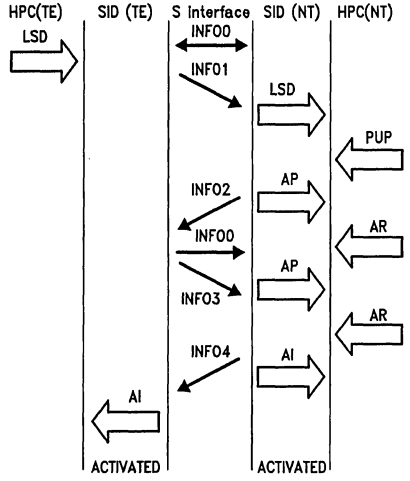


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FIGURE 18. Activation Initiated by TE

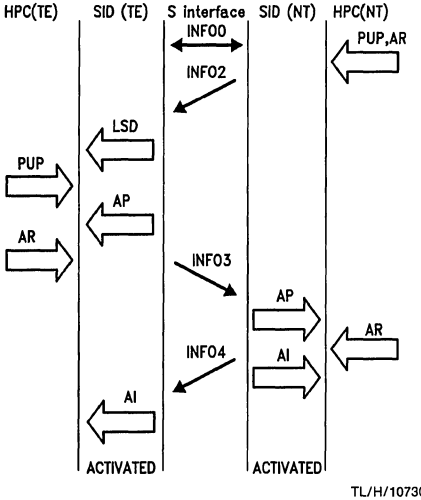

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FIGURE 19. Activation Initiated by NT

5.3 S Interface Loop Deactivation Initiated from the NT Side

An activated S interface may be deactivated by generating a DR command in the NT as shown in *Figure 20*. This will force the transmitter of the TP3420 to send INFO0 on the line. The SID in the TE side of the loop detects INFO0 and supplies DI status to the local management entity and also forces INFO0 on its transmitter output. The SID on the NT side will detect the INFO0 and informs the local management entity via DI status. The local controllers on both TE and NT may optionally power down the SID to save power.

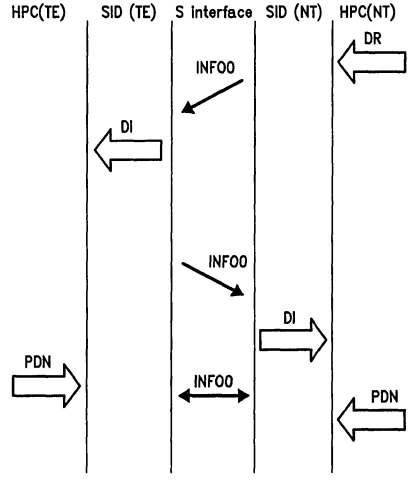

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FIGURE 20. Deactivation Initiated by NT

5.4 D-Channel Request and Flow Control (TP3420/1)

On the S interface, no TE can use a B channel until it is assigned by the network via the D channel. Therefore there is never a contention problem in a B channel. The D channel, however, carries multiple logical links to and from multiple physical end points (TE's). Therefore packets from different TE's may contend for the use of the D channel towards the network. This multiple access contention is resolved on the S interface by making use of the layer 2 HDLC framing rules *(Figure 21)*. TP3420 and TP3421 implement the D channel access control via a collision detection mechanism as described in I.430 Section 6.1 for both TE and NT modes *(Figure 22)*.

D channel flow control refers to the way the μP transfers a layer 2 frame or packet to the SID transmit buffer, and from there onto the S interface in a terminal. When the layer 2 wants to transmit a packet, it does not know if another TE is already occupying the D channel, since all D channel monitoring and contention resolution is done by the SID. To transmit its packet, the following sequence of events takes place:

the HDLC controller primes its transmit buffer, ready to send byte 1;

the μP sends a DREQ (D channel request) over MICROWIRE to the TP3420 (or the Monitor Channel to the TP3421). DREQ messages must also indicate if the pending packet is high priority for signaling (use DREQ1) or low priority for other types of data (use DREQ2).

SID starts pulsing DENx to the HDLC; DENx is gated with the BCLK in the HPC16400E, so 2 D channel bits are clocked from the HDLC into SID's transmit buffer every 125 μs across the DSI. No D channel bits are transmitted on the S interface yet;

SID senses when the opening flag (01111110) from the HPC is in its buffer. It then stops pulsing DENx.

SID now tests to see if the D channel towards the NT is in use by another TE, by checking the number of consecutive 1's counted in the D echo channel. When the access algorithm allows, SID starts transmitting D channel bits from its buffer, beginning with the opening flag.

The SID also now restarts pulsing DENx to fetch further D channel bits from the HDLC to the SID transmit buffer, always 2 bits per 125 μs frame.

D channel data now flows from the HDLC through SID onto the S interface until either:

SID detects that it has lost a collision with another TE, so it stops pulsing DENx, transmits 1's in the following D bit positions on the S interface, and interrupts the μP with a CON message;

or the SID detects the closing flag passing through onto the S interface, forces 1's into the D channel after the closing flag, stops pulsing DENx and sends an EOM interrupt to the μP.

Note that the μP cannot follow immediately with another packet because the successful TE must now decrement its priority and check that no other TE starts using the D channel (the SID does this automatically). Thus TE's waiting to send signaling packets all succeed in order first, and data packets are only sent when no TE has a signaling packet pending.

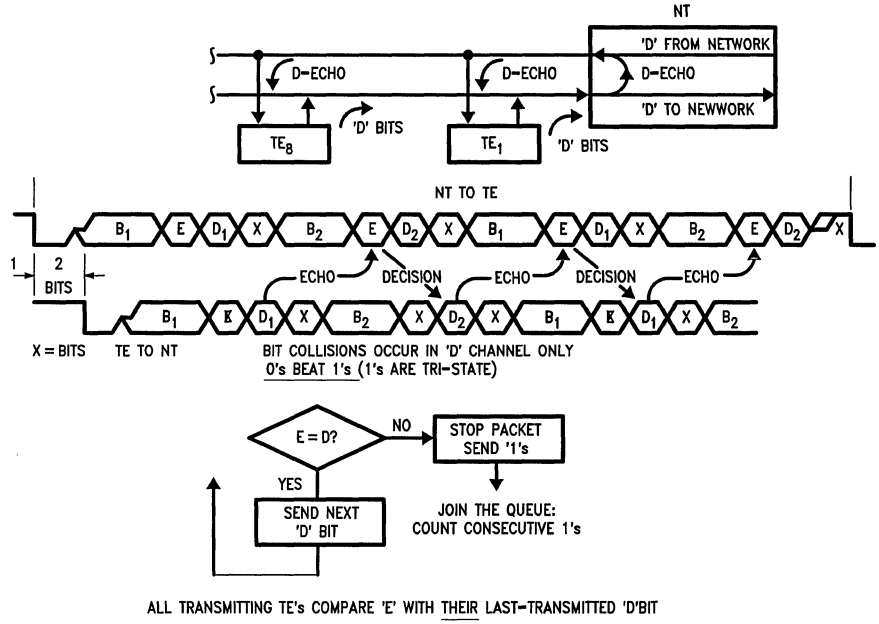

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FIGURE 21. D-Channel/Access Control

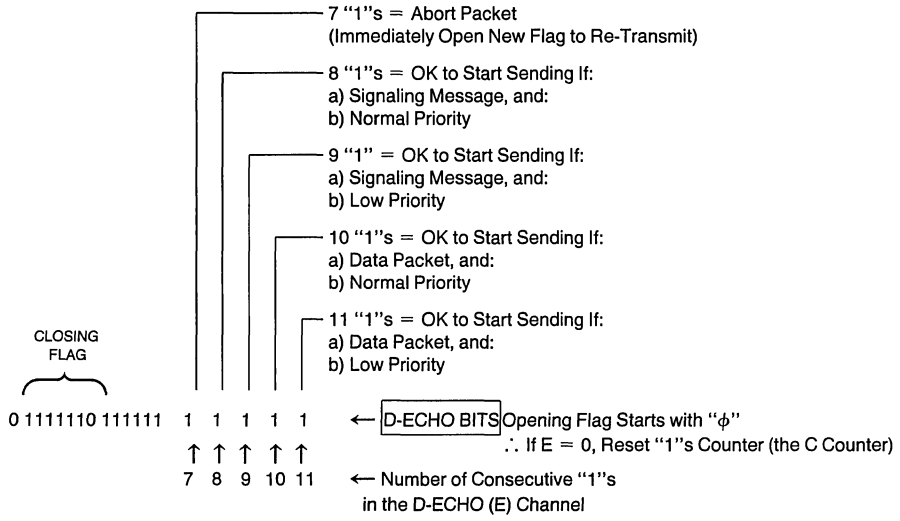


FIGURE 22. D-Channel Flow Control Via Priority Counting

5.5 Software Driver Considerations

The TP3420 performs several control functions and the software driver can be structured into modules to handle these functions separately:

"S" loop Activation and Deactivation: The Software driver and the SID must go through a series of activation states and flowcharts to implement these functions, which are described in the earlier section on activation and deactivation. The main function of the layer 1 driver is to handle this function. A Management Entity task communicates with the layer 1 driver to indicate whether a Remote activation or a Local activation is needed (by processing the condition of the Local ON/OFF Hook switch and the LSD interrupt from SID).

D-Channel Access: The layer 2 (HDLC) driver communicates with the layer 1 driver when D-channel packets are to be transmitted in the TE mode by means of the DREQ1 (Signaling packet) and DREQ2 (Data packet) commands. The EOM or CON status must be communicated to the layer 2 for either successful or failed transfer of the packet. In the NT modes the D-channel packets are transferred to SID without interacting with a layer 1 driver. In all modes, the received D-channel packets are passed straight to the layer 2 driver without interaction with the layer 1 driver.

Multiframe Channel Data: Multiframe maintenance frame channel received data interrupt (MFRxxxx) and transmit data command (MFTxxxx) are transferred directly to the Management entity task to process, and take appropriate action.

SID Command and Status Servicing: The SID will process all data appearing on its CI (MICROWIRE input port) pin, and so commands are processed by SID whenever a MICROWIRE handshake to SID takes place. When servicing a Status Interrupt to SID, it is recommended to send a NOP (No-Operation—FF Hex) command unless a valid command needs to be sent at the same time. Normally, when SID receives a command it will send a No Change Status (00 Hex) back to the HPC controller. It is possible (very rarely though) that while in the critical software section of sending a Command to SID, that a SID interrupt occurs (but is ignored because it may have been masked off temporarily) and the actual transfer of the Command results in servicing of the SID interrupt and a change of status value is returned to the HPC. The software driver must look at the received byte and if it is not 00 hex may decide to take appropriate action. The actual application may govern actions taken by the software.

6.0 TERMINAL EQUIPMENT (TE) FLOW CHARTS

The flow-charts provided in the text below relate the CCITT I.430 specified activation and deactivation flowcharts to the implementation flowcharts when using the TP3420 SID device. The key for symbols differentiates between actions taken by the SID and actions required from the software driver. The Initialization State is entered during the power-on initialization of all drivers as well as whenever a RESET is executed. Note that some of the TE state flowcharts *(Figures 23a–i)* are directly supported in the TP3420 SID, and hence the software driver need not implement the state. The notes provide some guidance.

CCITT defines states that a TE would go through during the process of Activation and Deactivation on the S Interface. These are known as the F states. The software drivers recommended for the TP3420 implement additional internal states as described below:

F1:	Power supply is turned off (TE not plugged in to the power source).
INITIALIZE:	TP3420 SID initialization.
F2:	The power supply is ON, however, the receiver has not yet processed the signal received (TE Connected).
POWER DOWN:	TP3420 SID in Power Down mode.
F3:	Deactivated state.
F4:	The activation of layer 1 was initiated by the TE (INFO1); the TE waits for an INFO2 (Awaiting Signal).
F5:	Once the signal is received, the TE stops transmitting INFO1 and processes the received signal (INFO2 or INFO4) Synchronizing.
F6:	The TE recognized receipt of an INFO2 and waits for an INFO4 (Synchronized).
F7:	Active State of the TE (Activated).
F8:	The TE lost the frame synchronization and is trying to resynchronize itself (Lost Framing).

Supervisory timer T3 can be as long as 15 seconds for applications where a TE is connected via an NT-1 to the Central Office over an S interface loop followed by a U interface loop.

The SID layer 1 driver has internal states and it moves from one state to the next depending on status of the SID or a Primitive command from layer 2 or the Management Entity.

An Interrupt Service Routine (ISR) can be designed just to service the SID interrupt and set a software flag or send mail to the layer 1 driver task. The ISR can also be used to light status LEDs or some other indicators.

The Management Entity task (or similar supervisory task) has to decide whether a valid Remote Activation is in progress before activating the layer 1 driver task. Hence the LSD (Line Signal Detect) interrupt signal is sent to this task to be processed. Although some analog filtering is provided in the SID chip, further filtering in the software can provide additional immunity to unintentional wake-ups caused by noise on the line. On the first occurrence of the LSD interrupt, the task sets the count value to 1 and after a 5 ms period sends a *PDN* command to SID to reset the LSD circuit in the SID. If another LSD interrupt occurs immediately (<2 ms), then a valid continuous signal is being received and the layer 1 driver is notified by setting the remote-activation flag. If a second LSD interrupt is not received within the time-out period, then the system is reset.

TE State F2 (TE Connected State)

The software driver should wait in this state until it receives an Activate Request (PH-AR) as a primitive either from layer 2 or the Management Entity task. It then checks to see whether this was a Local Activation or Remote Activation depending on the state of the Local Activation Flag.

For Local Activation, the driver sends the Power Up *(PUP)* command to SID and waits at least 2 ms for the SID circuit to settle, then sends *AR* to SID. This causes it to start sending INFO1 signal and the software proceeds to TE state F4.

For Remote Activation, the driver sends *PUP* to SID and starts internal timer t to ensure that *AP* is received within, say, 10 ms to indicate good INFO2 signals are being received rather than noise.

TE State Power Down

Power down is a state in the software (normally reached after deactivation) where the driver can decide to Power Down *(PDN)* the TP3420 SID after a 10 ms wait to allow any spurious residual signals on the line to die away. This prevents false triggering of the LSD immediately after power down. Once the loop is completely deactivated and the local TE has finished communication, the local processor may also be put in Low power or Idle mode.

TE State F3 (Deactivated State)

This state is normally reached from F2 as a follow up to Remote Activation. An AP status indication from SID could mean that TP3420 SID has either received INFO2 (normal activation) or INFO4 (as in the case where the TE was attached to an already active passive bus). In either case, the driver sends *AR* and goes to state F6 after starting ISDN supervisory timer T3 to ensure prompt activation.

If timer t had timed out indicating no AP was received (no INFO2 or INFO4) then it was a false alarm and the driver goes back to state F2 after Power Down state.

TE State F4 (Awaiting Signal)

In this state TP3420 SID is waiting to receive some signal after Local Activation was started and it is transmitting INFO1. On receiving INFO any, INFO2 or INFO4 it sends out INFO0 while it is synchronizing its internal clocks to the incoming signal. The chip moves on to state F5.

Since this state is a transition state implemented in the SID, the driver is unlikely to receive the T3 expiration indication and should move on to the next state.

TE State F5 (Identifying Signal)

The SID tries to identify the incoming signal. Upon receiving and identifying INFO2, the SID derives bit and frame timing information and sends out INFO3 based on this timing.

Since some of the state actions are directly handled by SID, the driver goes on to state F6, the Synchronized state.

TE State F6 (Synchronized)

After sending INFO3, the next place the SID device needs to interact with the driver software is in this state.

Upon detecting INFO4, SID raises the AI (Activation Indication) status and informs the driver that it has been fully activated. The driver then stops timer T3 and sends out primitives PH = AI, and MPH = AI to the layer 2 and ME tasks. The driver then moves to state F7.

If the far end decided not to continue with activation, then it would send out INFO0 which would result in a DI status from the local SID. The software would then send out the PH = DI and MPH = DI primitives and moves to F2 state via the Power Down procedure.

If timer T3 expires (far end loop activation was not completed), then driver can decide to abandon the attempt by powering down *(PDN)* the SID. Appropriate error messages may be sent to the Management Entity (ME).

If the far end signal is unrecognizable, perhaps due to excessive jitter or noise, the synchronization may be lost, in which case SID would interrupt the processor with Error Indication (EI) and send out INFO0 while it is trying to regain synchronization. A timer could provide a reasonable time window. The TE is then in State F8 (Lost Framing).

TE State F7 (Activated)

This is the fully activated state in which the TE could proceed with data or voice communication. The layer 1 SID driver is then waiting for remote deactivation or occurrence of an error condition. A TE is not allowed to locally initiate deactivation of the loop.

If the NT deactivates, it sends out INFO0, which is received by the TE SID, which indicates the DI status. The driver informs the layer 2 and ME tasks of the DI indication. The SID is subsequently set in Power Down mode and the software driver returns to F2 state.

If the SID receives INFO2, indicating a partial deactivation, it sets the AP status and sends INFO3 (without needing another *AR* command). The software can go to state F6.

Under INFO any or Lost Framing conditions, the SID generates the EI Interrupt and sends INFO0 while trying to resynchronize. A timer could be used to allow a reasonable time window for this to happen. The driver then moves to state F6.

TE State F8 (Lost Framing)

This state is reached if framing is lost (due to an unrecognizable signal) after the AI state.

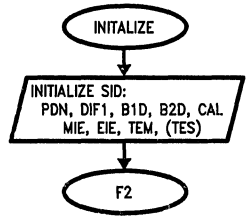
If a valid INFO2 is recognized, the SID generates the AP interrupt and proceeds by sending INFO3. The driver then moves on to state F6.

If INFO4 is recognized, the SID indicates AI and returns to the fully activated state again. The driver moves to state F7 after indicating MPH_E12 (resynchronized) to the ME.

If a clear INFO0 is detected, the DI status is indicated and the SID may be powered down.

If the time window (monitored by timer t) for re-synchronizing expires, the TE can attempt to deactivate locally. After sending INFO0, the terminal should stay in F8 state until it receives either DI (deactivated) or AP (resynchronized) indication from the SID. After receiving DI, the SID may be powered down.

TE Initialize



TL/H/10730–33

NOTES:

ACTIONS TAKEN BY THE SID ACTIVATION STATE MACHINE

	SIGNAL BEING RECEIVED BY THE SID
	SIGNAL BEING SENT BY SID
AI	STATUS OF SID
t	INTERNAL TIMER (25 ms TO 100 ms)
T3	SUPERVISORY TIMER (UP TO 15 s)

ACTIONS REQUIRED FROM SOFTWARE

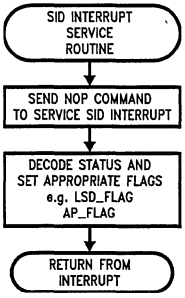
	STABLE SOFTWARE STATES
	SOFTWARE EVENTS
	SOFTWARE EVENTS
	SOFTWARE DECISION POINT
AR	COMMANDS SENT TO SID
AR_FLAG	SOFTWARE FLAG INDICATING SID STATUS
PH-...	PHYSICAL LAYER PRIMITIVE
MPH-...	MANAGEMENT ENTITY PHYSICAL LAYER PRIMITIVE

TL/H/10730–34

FIGURE 23a. TE Initialization Flow Chart

TE—Interrupt Servicing

SID Status Interrupt Service Routine



TL/H/10730–35

Filtering of False LSD Triggering in Power Down Mode

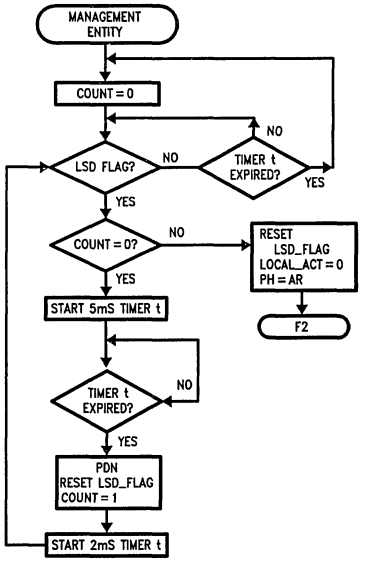


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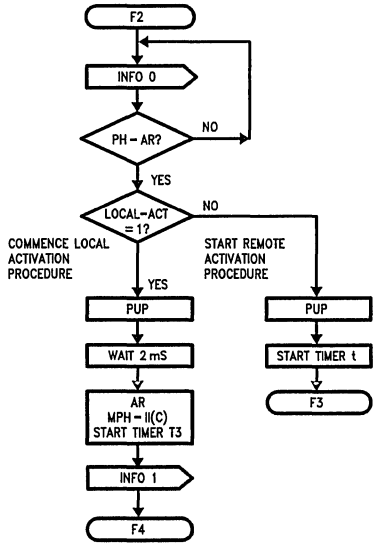
FIGURE 23b. TE Interrupt Servicing Flowchart

TE—F2 State



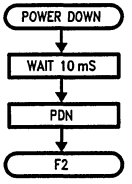


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FIGURE 23c. TE F2 State Flowchart

TE—F3 State

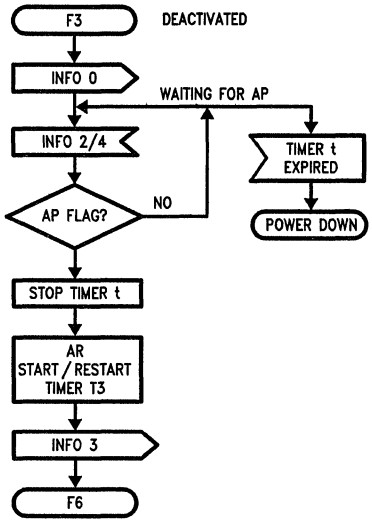

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FIGURE 23d. TE F3 State Flow Chart

TE—F4 State

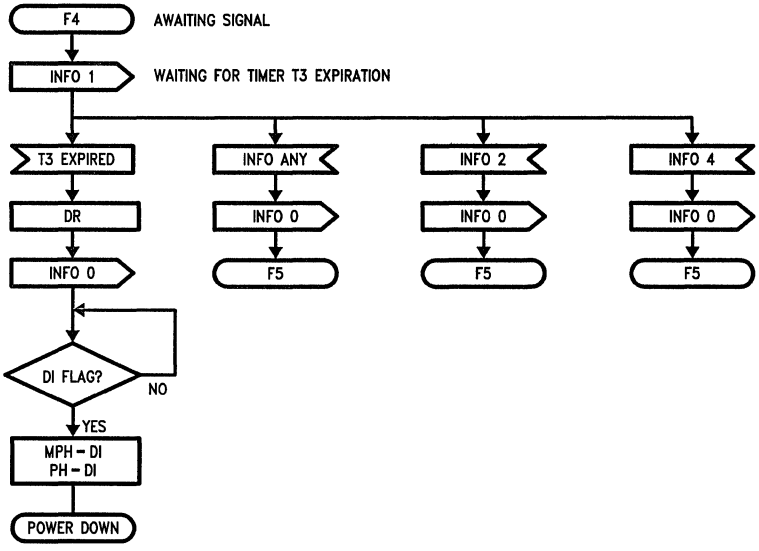

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FIGURE 23e. TE F4 State Flow Chart

TE—F5 State

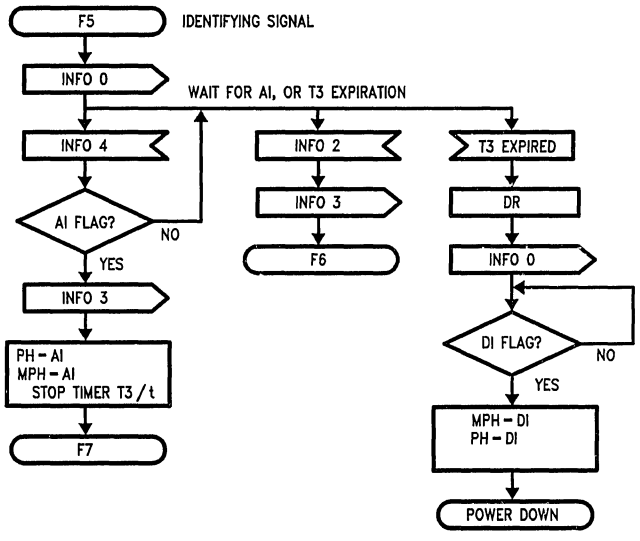

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FIGURE 23f. TE F5 State Flow Chart

TE—F6 State

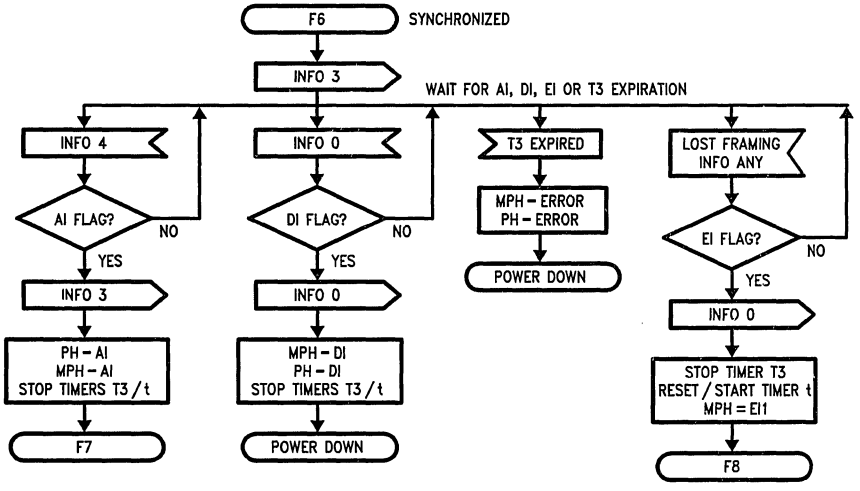

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FIGURE 23g. TE F6 State Flow Chart

TE—F7 State

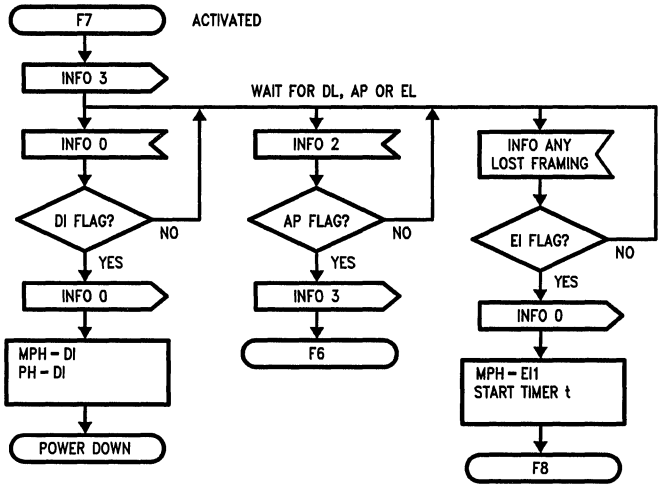

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FIGURE 23h. TE F7 State Flow Chart

TE—F8 State

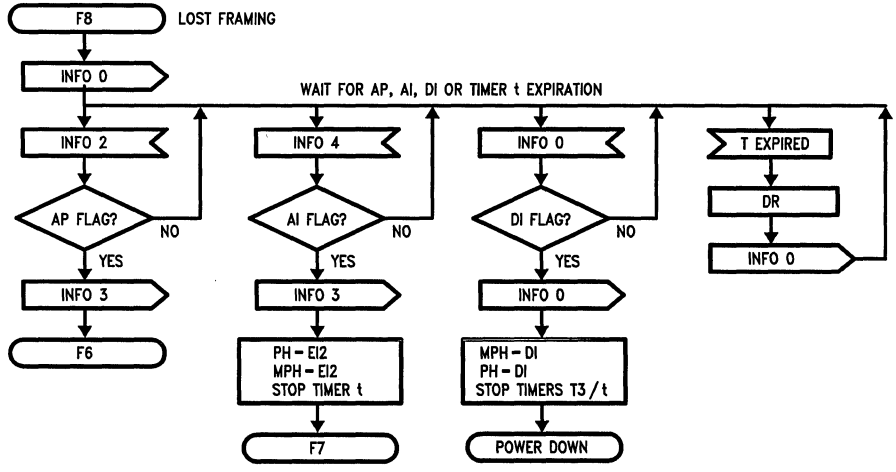

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FIGURE 23i. TE F8 State Flow Chart

7.0 NETWORK TERMINATION (NT) FLOW CHARTS

The G States are defined in CCITT recommendation I.430 as the states that an NT would go through to Activate/Deactivate the S interface loop. The software driver may need additional internal states as described below *(Figures 24a–g)*:

INITIALIZE: SID intialization for NT mode

G0: NT connected state (not defined in I.430)

POWER DOWN: Power Down mode of SID

G1: Deactivated condition. Idle state, i.e., layer 1 is not ready to transmit data.

G2: The activation of layer 1 was initiated by TE or NT; the NT is waiting for INFO3 from a TE (Pending Activation).

G3: Active state of NT, (Activated)

G4: Deactivation phase, the NT is waiting for the deactivation confirmed by TE (INFO0) and the completion of a count (Timer T2 if used) in order to change to state G1 (Pending Deactivation).

The flowcharts described below relate the I.430 specified activation/deactivation flowcharts to the implementation flowcharts when using TP3420 SID. The key for symbols differentiates between actions taken by the SID and actions required from the software driver.

The Initialize state is activated during the power-on initialization of all drivers as well as whenever a RESET is executed.

Note that some of the NT state flowcharts are directly implemented in the SID device and hence, the software driver need not stay in the state. The notes provide some guidance.

Supervisory timer T1 can be as long as 15 seconds for applications where a TE is connected through an NT1 device to the Central Office via a U interface loop.

Supervisory timer T2 is not required for applications using TP3420 SID because it is able to uniquely detect the INFO1 signal immediately after reaching the Deactivated State (DI), thereby preventing unintentional reactivation if a TE is slow to terminate the INFO3 signal.

The SID layer 1 driver has internal states and it moves from one state to the next depending on the device status or a Primitive command from Layer 2 or the Management Entity (ME).

An Interrupt Service Routine (ISR) can be designed just to service the SID interrupt and set a software flag or send mail to the layer 1 driver task. The ISR can also be used to light status LEDs or some other indicators.

The ME task (or similar supervisory task) must decide whether a valid Remote Activation is in progress before activating the layer 1 driver task. Hence the LSD (Line Signal Detect) interrupt signal is sent to this task to be processed. Although some analog filtering is provided in the SID chip, further filtering in the software can provide additional noise immunity. On the first occurrence of the LSD Interrupt, the task sets the count value to 1 and after a 5 ms period sends a *PDN* command to SID to re-enable the LSD circuit in the SID. If another LSD interrupt occurs immediately (<2 ms), than a valid continuous signal is being received and the layer 1 driver is notified by setting the remote-activation flag. If a second LSD is not received within the time-out period then the system is reset.

NT state G0 (NT Connected State)

The software driver should wait in this state until it receives an Activate Request (PH-AR) as a primitive command from either the Layer 2 or ME task. It then checks to see whether this was a Local Activation or Remote Activation depending on the state of the Local Activation Flag.

For Local Activation, the driver sends the Power Up *(PUP)* command to SID, waits at least 2 ms for the circuit to settle and then sends *AR* to SID which causes it to start sending INFO2 frames. The software proceeds to NT state G2.

For Remote Activation, the driver sends *PUP* to SID and starts internal timer t to ensure that AP is received within, say, 10 ms to indicate good INFO1 signal being received rather than noise.

NT State Power Down

Power Down is a state in the software (reached normally after deactivation) when the driver can decide to Power Down *(PDN)* SID after a 10 ms wait to allow any spurious residual signals on the line to die away. This prevents false triggering of the LSD immediately after power down.

NT State G1 (Deactivated State)

This state is normally reached from G0 as a follow up to Remote Activation. An AP status indication from SID could mean that SID has received INFO1. The driver then sends *AR* and goes to state G2 after starting ISDN supervisory timer T1 to ensure prompt activation. The SID starts sending INFO2.

If timer t had timed out indicating no AP was received (no INFO1) then it was a false alarm and the driver goes back to state G0 after Power Down state.

NT State G2 (Pending Activation)

After sending INFO2, the next time the SID needs to interact with the driver software is in this state.

When INFO3 is recognized, the SID indicates an Activation Pending Status (AP). The NT side layer 1 driver can then proceed to send a second *AR* to enable SID to complete the activation procedure. The SID starts sending INFO4 and generates the AI status to inform the driver that it has been fully activated. The driver then stops timer T1 and sends out primitives PH-AI, and MPH-AI to the layer 2 and ME tasks. The driver then moves to state G3.

If timer T1 expires (INFO3 was not received), the driver can decide to deactivate by sending *DR* and waiting for DI before powering down the SID. The NT may optionally continue sending INFO2 until any TE is ready to respond with INFO3.

In some cases timer T1 may not be used and the first *AR* would cause the SID to continuously send INFO2. In this case, the link may be deactivated with a local Deactivation Request *(DR)*. The software would go through the state G4 for deactivation.

NT State G3 (Activated)

This is the fully activated state in which the NT can proceed with data or voice communication. The layer 1 SID driver is then waiting for local deactivation or occurrence of an error condition.

The NT could deactivate the loop locally by sending *DR* to SID which sends out INFO0. The driver informs the layer 2 and ME tasks of the DI indication. The software moves to state G4 to deactivate.

In some applications, the NT may partially deactivate by sending *FI2* (Force INFO2) to SID. This causes the SID to start sending INFO2 frames; the software and the SID return to state G2.

Under Not-Info-3 or Lost Framing conditions, the SID generates the EI status and sends INFO2 in an attempt to allow resynchronization of the loop. The software and SID move to state G2.

NT State G4 (Pending Deactivation)

This state allows orderly deactivation of the loop. All residual signals on the S interface are allowed to die out before remote activation is allowed. Timer T2 is used to provide a time delay (25 ms to 100 ms).

However the SID has the ability to uniquely identify an incoming INFO1 signal and hence timer T2 may not be used. The software driver may go straight to the Power Down state.

Local Activation is allowed if PH-AR is received and the software returns immediately to state G0.

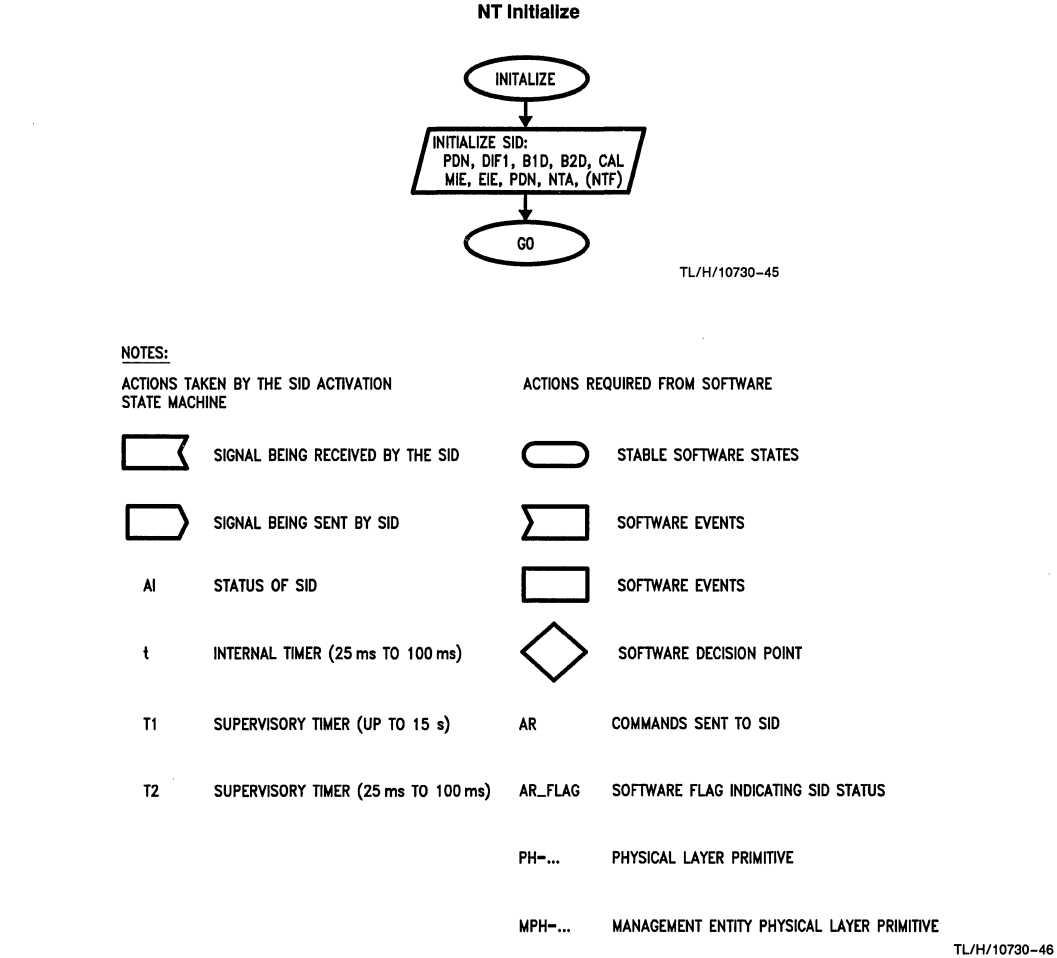
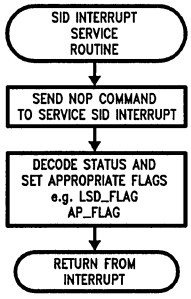


FIGURE 24a. NT Initialization Flow Chart

NT—SID Interrupt Servicing

SID STATUS Interrupt Service Routine



TL/H/10730–47

Filtering of False LSD Triggering in Power Down Mode

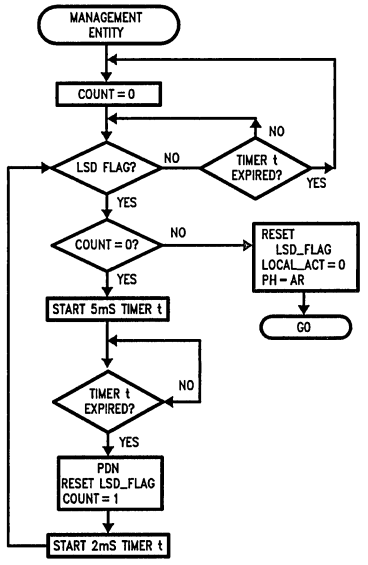


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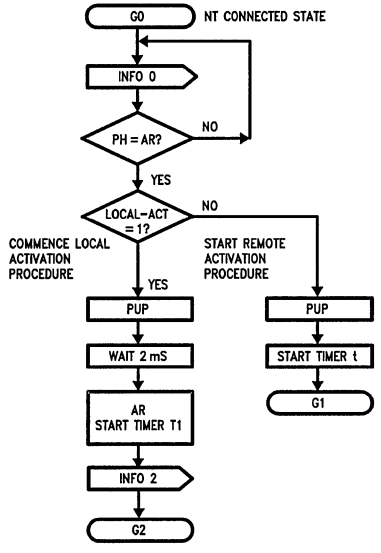
FIGURE 24b. NT Interrupt Servicing Flow Chart

NT—G0 State



TL/H/10730–49

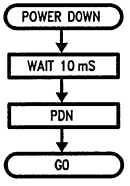


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FIGURE 24c. NT G0 State Flow Chart

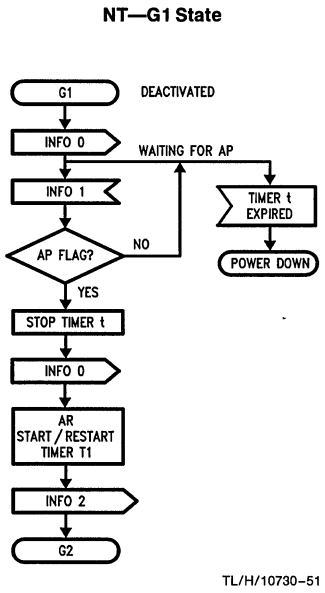


FIGURE 24d. NT G1 State Flow Chart

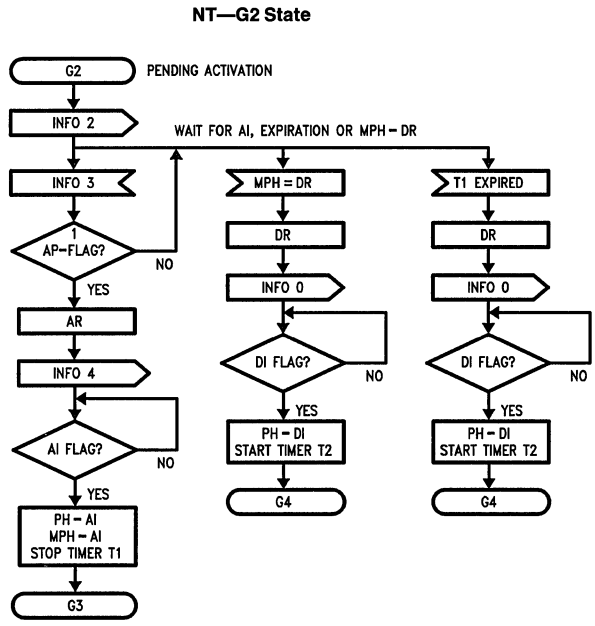


FIGURE 24e. NT G2 State Flow Chart

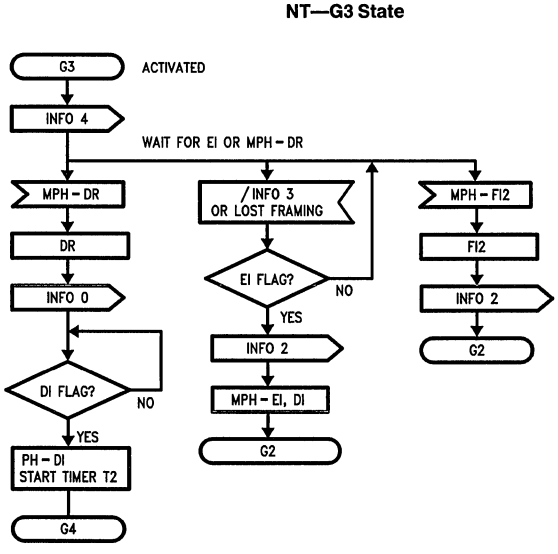


FIGURE 24f. NT G3 State Flow Chart

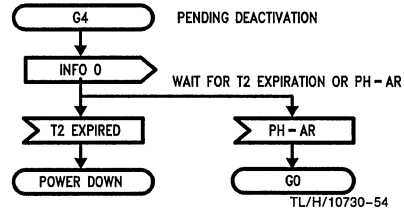


FIGURE 24g. NT G4 State Flow Chart

8.0 SID TEST LOOPBACK MODES

The TP3420 and TP3421 provide three classes of loopback modes, namely:

Full 2B+D loopback at the system interface (LBS);

Individual B channel loopback at the line interface (LBL1/LBL2);

Individual B channel loopback at the system interface (LBB1/LBB2).

These loopbacks may be activated via MICROWIRE commands into TP3420 or Monitor Channel commands in the TP3421. Using the loopback modes provided in the device, various system loopbacks recommended in the CCITT I.430 may be implemented.

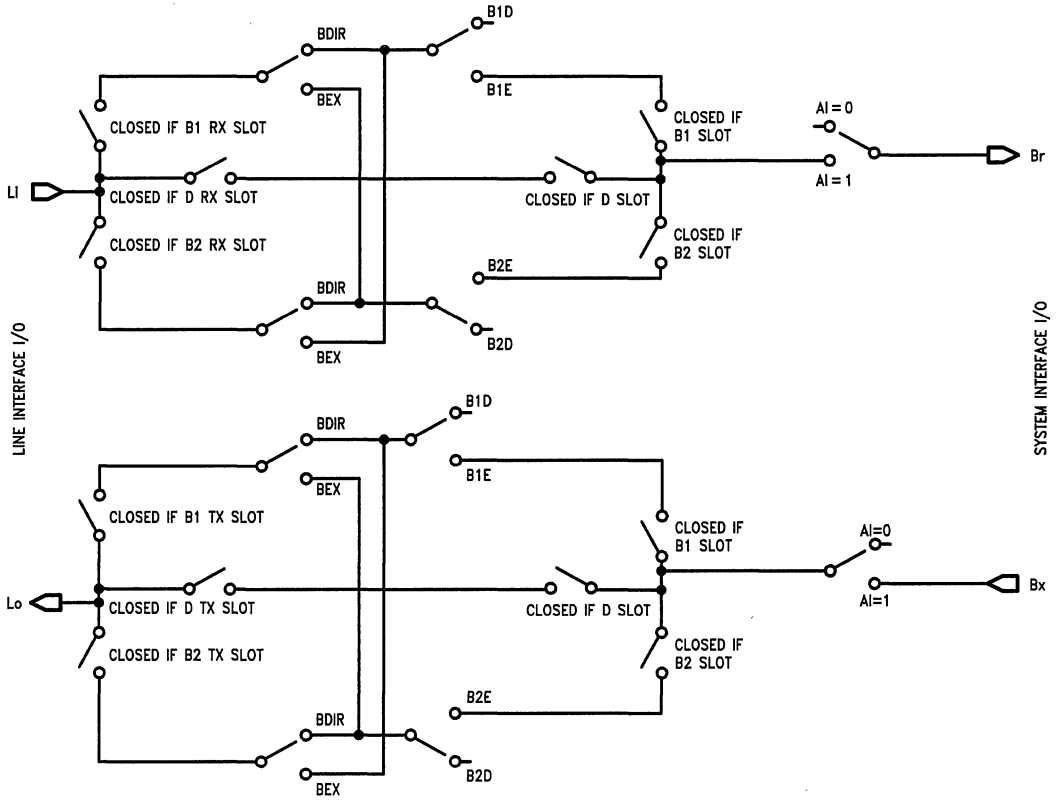
In order to use SID loopback modes effectively in implementing the I.430 loopbacks, an explanation of each test loopback mode is in order here. In the explanation below, we refer to the B1, B2 and D **Tx** and **Rx** slots and B1, B2 and D slots as shown in *Figure 25*.

8.1 Normal Data Mode (No Loopbacks)

SID is powered up with clear all loopbacks (CAL) mode. In this mode, the function diagram of the device is as illustrated in *Figure 25*. This shows normal data paths when no test loopbacks are in effect. The switches are positioned according to the state of the device selected through commands.

8.2 System Loopback Mode LBS

Figure 26 shows a schematic diagram illustrating the system loopback function (LBS). Upon writing the LBS command into the command register, various internal switches are positioned as in *Figure 26* if B1 and B2 channels are enabled. Bx data may be output onto the Lo pins of the line interface at the valid slots of the B1, D and B2 data periods on the Digital System Interface pin Bx and Br for the Format selected.



TL/H/10730–55

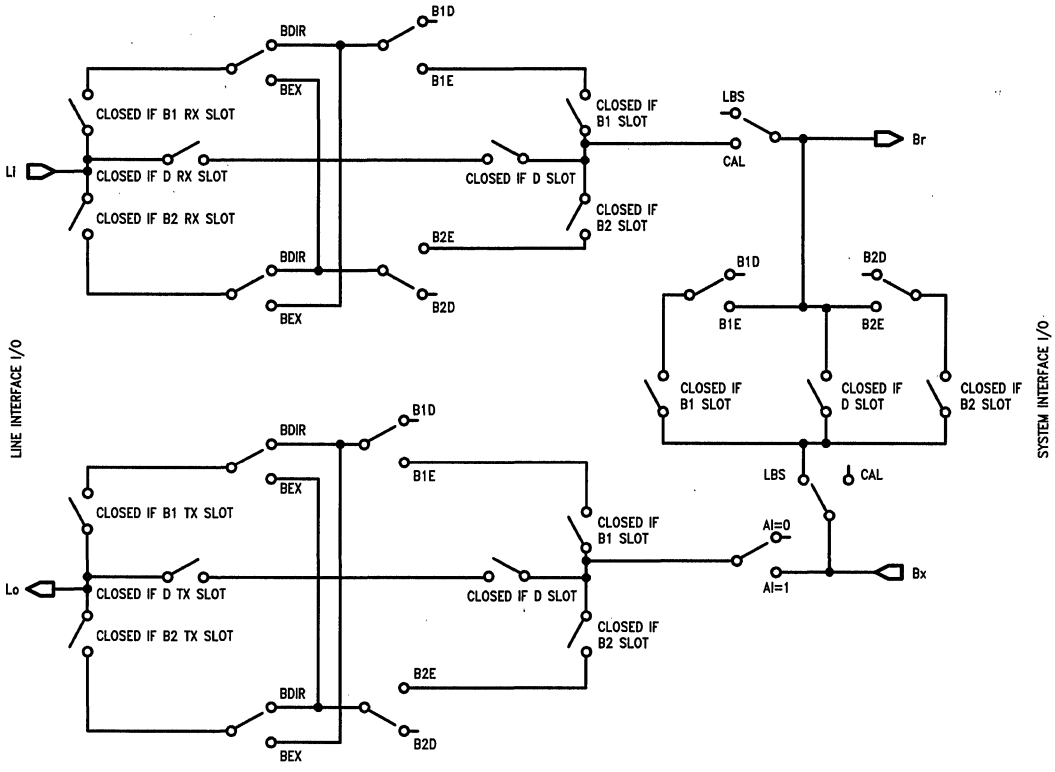
Internal Control Signals

B1 Tx/Rx Slot:
B2 Tx/Rx Slot: Referenced to I.430 Line Interface Lo/Li time slot
D Tx/Rx Slot:
B1 Slot:
B2 Slot: Referenced to Digital System Interface Bx/Br time slot
D Slot:

External Command/Status

BDIR: B-CH mapped direct, B1 to B1, B2 to B2
BCX: B-CH exchanged, B1 to B2, B2 to B1
B1C: B1-CH enabled B2C: B2-CH enabled
B1D: B1-CH disabled B2D: B2-CH disabled
AI: Activation Indication

FIGURE 25. Normal Data Paths Diagram (No Loopbacks)



TL/H/10730–56

Internal Control Signals

B1 Tx/Rx Slot:
B2 Tx/Rx Slot: Referenced to I.430 line interface Lo/Li time slot
D Tx/Rx Slot:
B1 Slot:
B2 Slot: Referenced to Digital System Interface Bx/Br time slot
D Slot:
(Note: For NT/TES modes, FSa and FSb inputs have to be same phase)

External MICROWIRE Command/Status

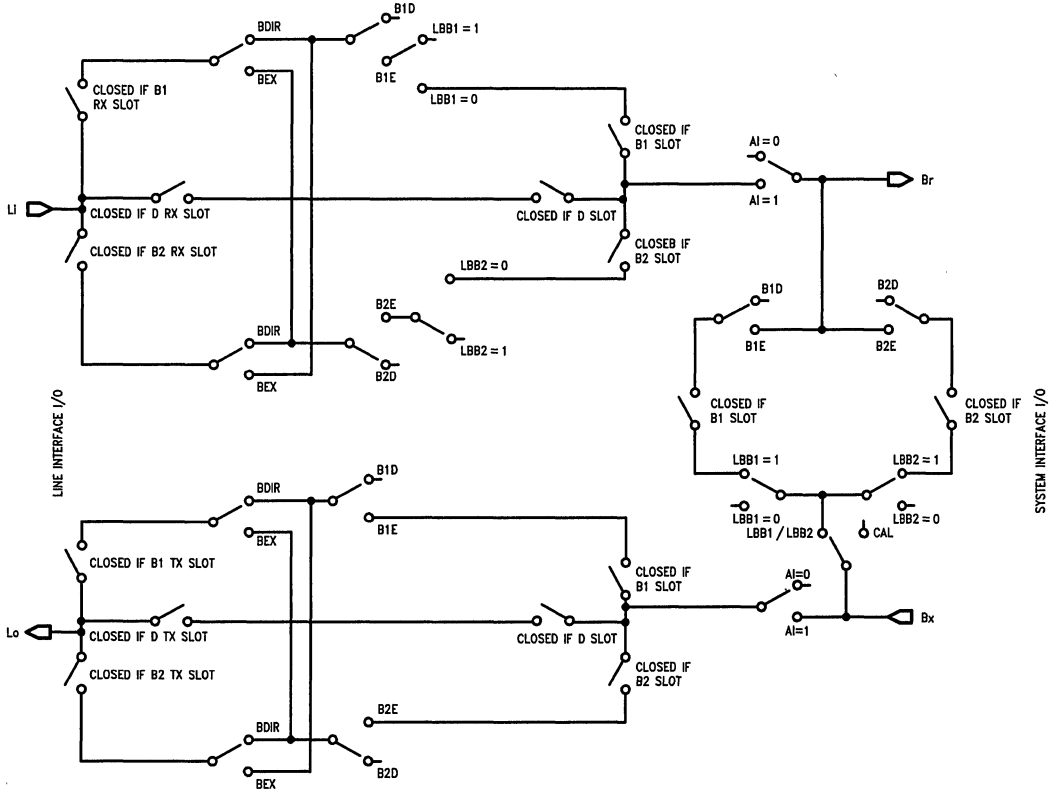
LBS: Loopback 2B + D towards system interface
CAL: Clear all loopbacks
BDIR: B-CH mapped direct, B1 to B1, B2 to B2
BEX: B-CH exchanged, B1 to B2, B2 to B1
B1E: B1-CH enabled B2E: B2-CH enabled
B1D: B1-CH disabled B2D: B2-CH disabled
AI: Activation indication

FIGURE 26. TP3420/1 System Loopback Function Diagram (LBS)

8.3 System Loopback Mode LBB1, LBB2

Figure 27 shows a schematic diagram when LBB1 or LBB2 system loopbacks are used. LBB1 and LBB2 loopback modes may be chosen independently when B1 and/or B2 respectively are to be looped back to the system interface (from Bx to Br), while at the same time B1, B2 and D data to the line interface (Bx to Lo) may be allowed. Also, at the same time, B2 or B1 and D channel data may be allowed from the line interface to the system interface (Li to Br). Data transfers across line interface and system interface are possible only when SID is in the activated state (AI = 1).

For example, in *Figure 27* when LBB1 is enabled, the B1 channel from the system interface is looped back (assuming B1 is enabled). At this time B1, B2 and D channels may be transferred across the interfaces if AI is true; also, B2 and D channels may be transferred from Li to Br.



TL/H/10730–57

Internal Control Signals

B1 Tx/Rx Slot:
B2 Tx/Rx Slot: Referenced to I.430 line interface Lo/Li time slot
D Tx/Rx Slot:
B1 Slot:
B2 Slot: Referenced Digital System Interface Bx/Br time slot
D Slot:
Note: For NT/TES modes, FSa and FSb inputs have to be same phase
Note: No B-CH data loopback from Bx to Br

External Command/Status

LBB1: Loopback B1 towards system interface if LBB1 = 1
LBB2: Loopback B2 towards system interface if LBB2 = 1
CAL: Clear all loopbacks
BDIR: B-CH mapped direct, B1 to B1, B2 to B2
BEX: B-CH exchanged, B1 to B2, B2 to B1
B1E: B1-CH enabled B2E: B2-CH enabled
B1D: B1-CH disabled B2D: B2-CH disabled
AI: Activation Indication

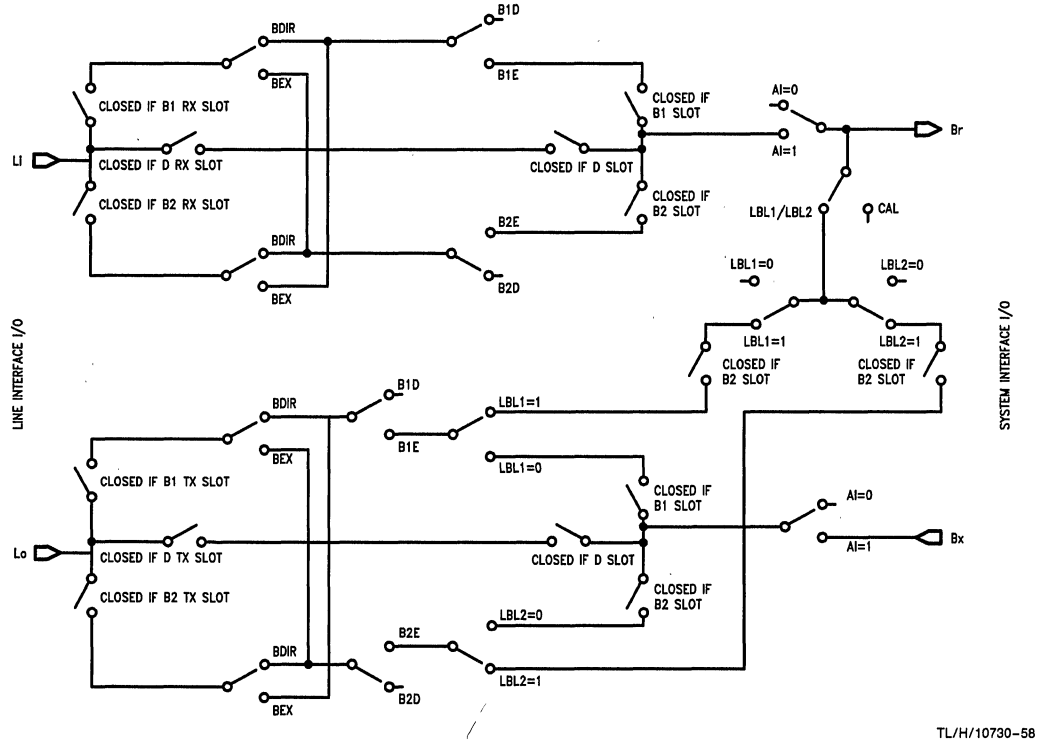
FIGURE 27. TP3420/1 System Loopback Function Diagram (LBB1, LBB2)

8.4 Line Loopack Mode LBL1, LBL2

LBL1 and LBL2 commands are used independently to select line loopback mode as shown in the function diagram of *Figure 28* when B1 and/or B2 are to be looped back to the line interface (from Li to Lo), while at the same time B1, B2 and D data to the system interface (Li to Br) may be allowed. Also, at the same time B2 or B1 and D channel data may be allowed from the system interface to the line interface (Bx to Lo). Of course, once again the transfers across the interfaces are conditional upon AI = 1 and the appropriate channels being enabled.

For example, when LBL1 is chosen, the B1 channel from the line interface is looped back. Notice at the same time B1, B2 and D channels are transferred to the Br pin of the system interface and also B2 and D channels from the system interface are transferred to the Lo pin of the line interface.

Figure 29 illustrates the simplified loopback functions that the device can be configured into.



Internal Control Signals

B1 Tx/Rx Slot:
B2 Tx/Rx Slot : Referenced to I.430 Line Interface Lo/Li time slot
D Tx/Rx Slot:
B1 Slot:
B2 Slot: Referenced to Digital System Interface Bx/Br time slot
D Slot:
Note: For NT/TES modes, FSa to FSb inputs have to be same phase
Note: No D-CH data loopback from Li to Lo

External Command/Status

LBL1: Loopback B1 towards line interface if LBL1 = 1
LBL2: Loopback B2 towards line interface if LBL2 = 1
CAL: Clear all loopbacks
BDIR: B-CH mapped direct, B1 to B1, B2 to B2
BEX: B-CH exchanged, B1 to B2, B2 to B1
B1E: B1-CH enabled B2E: B2-CH enabled
B1D: B1-CH disabled B2D: B2-CH disabled
AI: Activation Indication

FIGURE 28. TP3420/1 System Loopback Function Diagram (LBL1, LBL2)

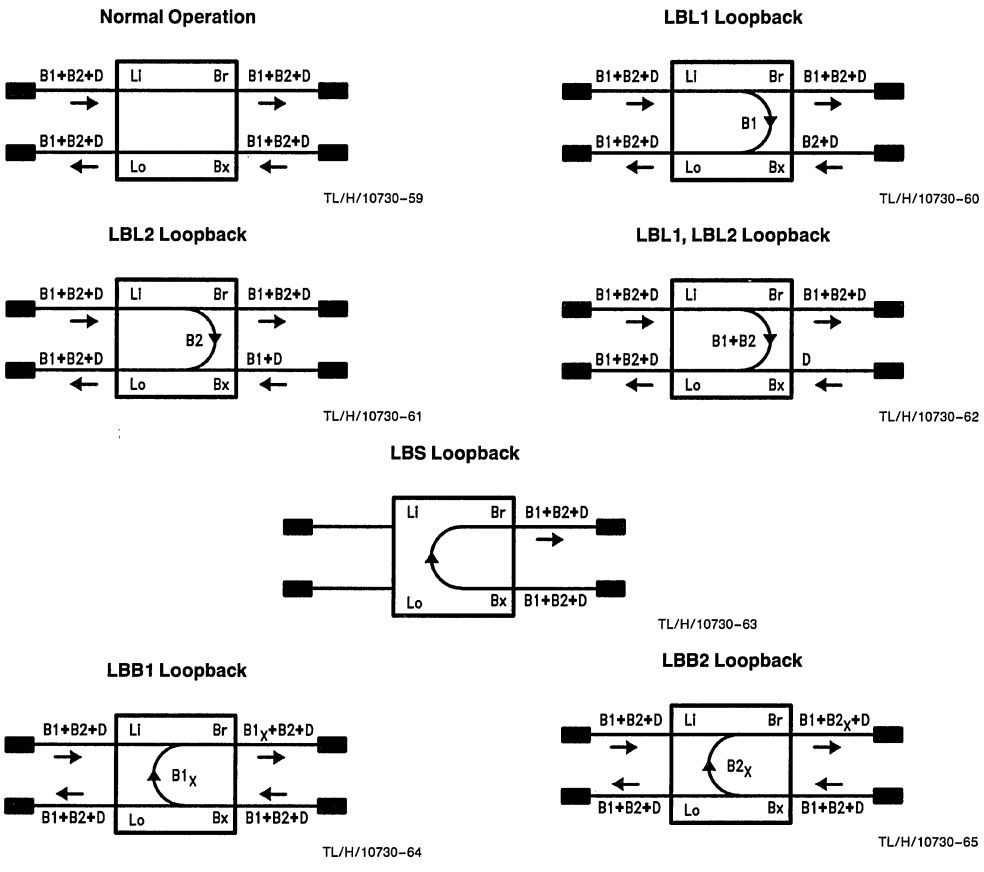


FIGURE 29. TP3420/1 Test Loopback Summary

9.0 ADDITIONAL TEST FEATURES

The TP3420/1 SID devices also include several system features intended for system test and system instrumentation purposes, namely the external local analog loopback and monitor mode activation as explained below.

9.1 External Local Analog Loopback

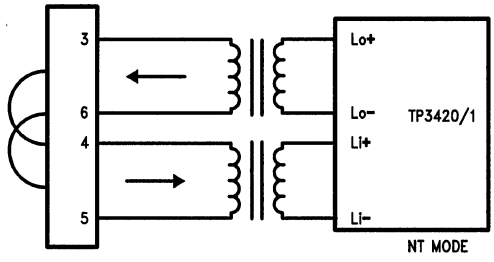
External local analog loopback is physically accomplished by connecting the line output signals after the transmit transformer to the line input signals before the receive transformer as shown in *Figure 30*. The SID is set in NTA or NTF mode and the local loop is activated with the following command sequence:

NTA (or NTF), PUP, AR. Receive status AP, AR, receive status AI.

The B channels are enabled (B1E, B2E) to transfer data on the B channels. Data can be sent or received on the D channel at 16 kbps. B and D channel data, fed in at the Bx input, is returned on the Br output after being looped at the external line interface. BCLK and FS signals need to be supplied to the SID operating in NT mode.

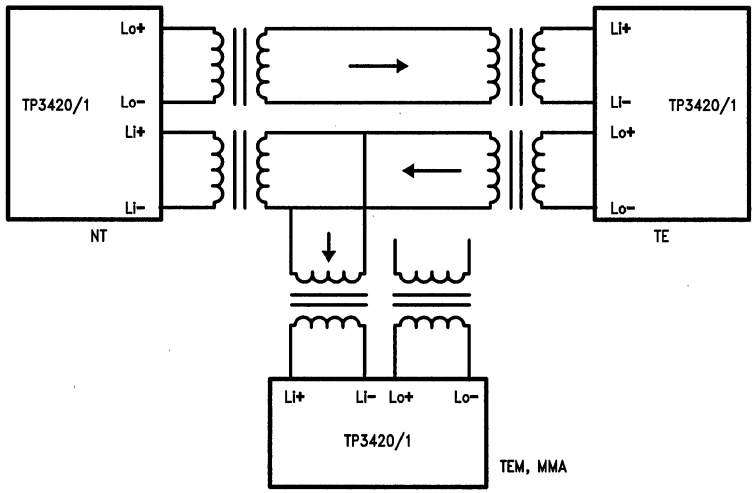
9.2 Monitor Mode Activation

The SID device may be configured for applications where D and/or B channels may be monitored in the upstream direction on an S interface pair as shown in *Figure 31*. The SID is to be first configured into TEM mode for this application and then MMA is written into the command register. This puts the TP3420/1 into a psuedo-NT mode in which it receives and activates on the incoming INFO3 frames. Note that in this application of the device, only the receiver section is actively connected to the S interface. This feature is targeted at applications where B and D channels are monitored for network analysis, as in protocol analyzers and line testers. Line monitoring in the downstream direction requires another device operating normally in TE Mode.



TL/H/10730–66

FIGURE 30. External Loopback Activation



TL/H/10730–67

FIGURE 31. Monitor Mode Application

Definitions and Timing Conventions

DEFINITIONS

V_{IH} — V_{IH} is the DC input level above which an input level is guaranteed to appear as a logical one. This parameter is to be measured by performing a functional test at reduced clock speeds and nominal timing, (i.e. not minimum set-up and hold times or output strobes), with the high level of all driving signals set to V_{IH} and maximum supply voltages applied to the device. (See *Figures 1a, b*)

V_{IL} — V_{IL} is the DC input level below which an input level is guaranteed to appear as a logical zero to the device. This parameter is measured in the same manner as V_{IH} but with all driving signal low levels set to V_{IL} and minimum supply voltages applied to the device. (See *Figures 1a, b*)

V_{OH} — V_{OH} is the minimum DC output level to which an output placed in a logical one state will converge when loaded at the maximum specified load current. (See *Figures 1a, b*)

V_{OL} — V_{OL} is the maximum DC output level to which an output placed in a logical zero state will converge when loaded at the maximum specified load current. (See *Figures 1a, b*)

Threshold Region — The threshold region is the range of input voltages between V_{IL} and V_{IH}.

Valid Signal — A signal is Valid if it is in one of the valid logic states, (i.e. above V_{IH} or below V_{IL}). In timing specifications, a signal is deemed valid at the instant it enters a valid state.

Invalid Signal — A signal is Invalid if it is not in a valid logic state, i.e. when it is in the threshold region between V_{IL} and V_{IH}. In timing specifications, a signal is deemed Invalid at the instant it enters the threshold region.

TIMING CONVENTIONS

For the purposes of this timing specification the following conventions apply:

Input Signals — All input signals may be characterized as: $V_L = 0.4V$, $V_H = 2.4V$, $t_R < 10$ ns, $t_F < 10$ ns.

Period — The period of clock signal is designated at t_{Pxx} where xx represents the mnemonic of the clock signal being specified. (See *Figure 2*)

Rise Time — Rise times are designated as t_{Ryy}, where yy represents a mnemonic of the signal whose rise time is being specified. t_{Ryy} is measured from V_{IL} to V_{IH}. (See *Figure 3*)

Fall Time — Fall times are designated as t_{Fyy}, where yy represents a mnemonic of the signal whose fall time is being specified. t_{Fyy} is measured from V_{IH} to V_{IL}. (See *Figure 3*)

Pulse Width High — The high pulse width is designated as t_{WzzH}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. High pulse widths are measured from V_{IH} to V_{IH}. (See *Figure 4*)

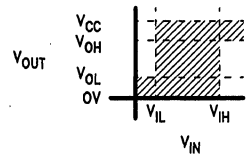
Pulse Width Low — The low pulse width is designated as t_{WzzL}, where zz represents the mnemonic of the input or output signal whose pulse width is being specified. Low pulse widths are measured from V_{IL} to V_{IL}. (See *Figure 4*)

Set-up Time — Set-up times are designated as t_{Swwxx}, where ww represents the mnemonic of the input signal whose set-up time is being specified relative to a clock or strobe input represented by mnemonic xx. Set-up times are measured from the ww Valid to xx Invalid. (See *Figures 5a, b*)

Hold Time — Hold times are designated as t_{Hxxww}, where ww represents the mnemonic of the input signal whose hold time is being specified relative to a clock or strobe input represented by mnemonic xx. Hold times are measured from xx Valid to ww Invalid. (See *Figures 5a, b*)

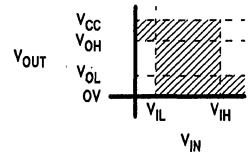
Delay Time — Delay times are designated as $t_{Dxxyy[H|L]}$, where xx represents the mnemonic of the input reference signal and yy represents the mnemonic of the output signal whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum delay times are measured from xx Valid to yy Valid. Minimum delay times are measured from xx Valid to yy Invalid. This parameter is tested under the load conditions specified in the Conditions column of the Timing Specifications section of each datasheet. (See *Figures 6a, b*)

Disable Time — The Disable time is designated as $T_{Zxxyy[H|L]}$, where xx represents the mnemonic of the input reference signal and yy represents the output whose timing is being specified relative to xx. The mnemonic may optionally be terminated by an H or L to specify the high going or low going transition of the output signal. Maximum and minimum disable times are measured from xx Valid to yy Invalid. This parameter is tested with a resistive load as specified in the Conditions column of the Timing Specifications section of each datasheet. No capacitive loading is added. (See *Figures 7a, b*)



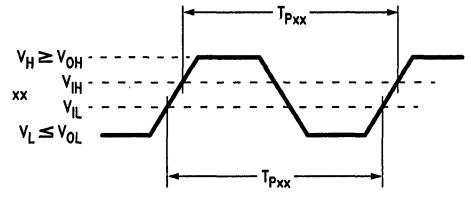
TL/H/10725–1

FIGURE 1a. Allowed DC States for Non-Inverting Logic Gates



TL/H/10725–2

FIGURE 1b. Allowed DC States for Inverting Logic Gates



TL/H/10725–3

FIGURE 2

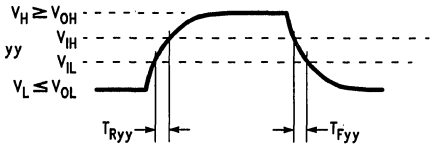


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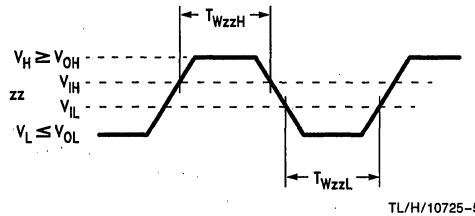
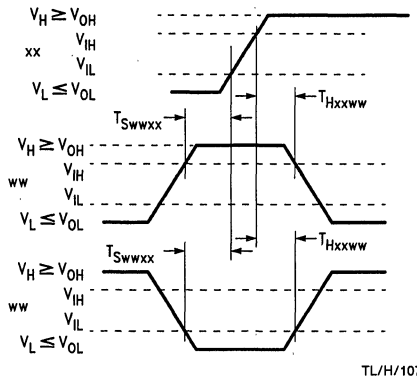
FIGURE 3



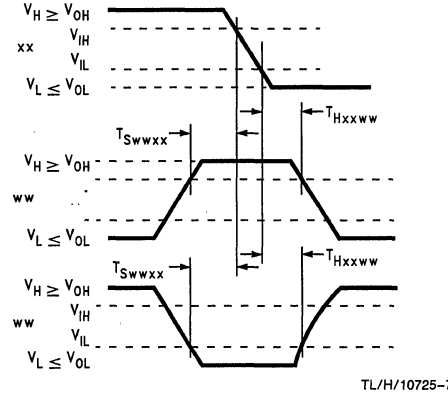
TL/H/10725–5

FIGURE 4



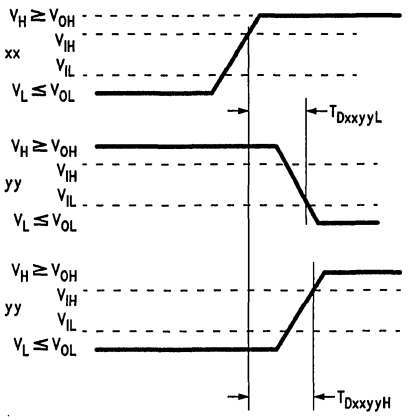
TL/H/10725–6

FIGURE 5a



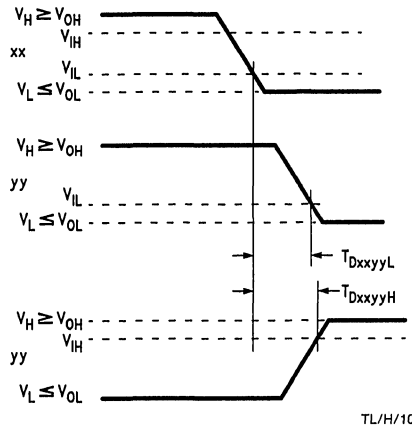
TL/H/10725–7

FIGURE 5b



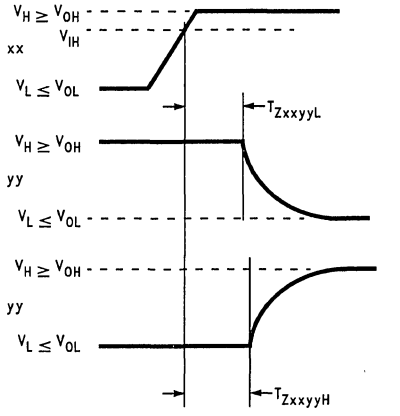
TL/H/10725–8

FIGURE 6a



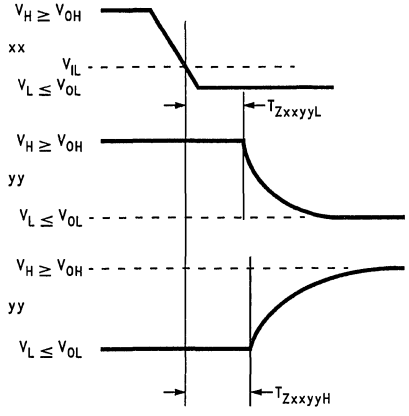
TL/H/10725–9

FIGURE 6b



TL/H/10725–10

FIGURE 7a



TL/H/10725–11

FIGURE 7b

National Semiconductor

ISDN Basic Rate Interface Software for the HPC16400 High Performance Data Communications Microcontroller

General Description

The ISDN Basic Rate Interface Software Package implemented on the National Semiconductor HPC™ Microcontroller Family contains the software elements that are necessary to implement CCITT standards Q.921 and Q.931 as approved by T1D1 for North America.

The software package is designed to be easily unbundled and used independently by a software developer. Each layer or function is written as a separate software task. This modular design and well defined task interface make it easy to interface application dependent software to the modules provided. The coding standards for software development have been designed to ensure development of consistent, structured code, which can be easily used and maintained over the life of the code.

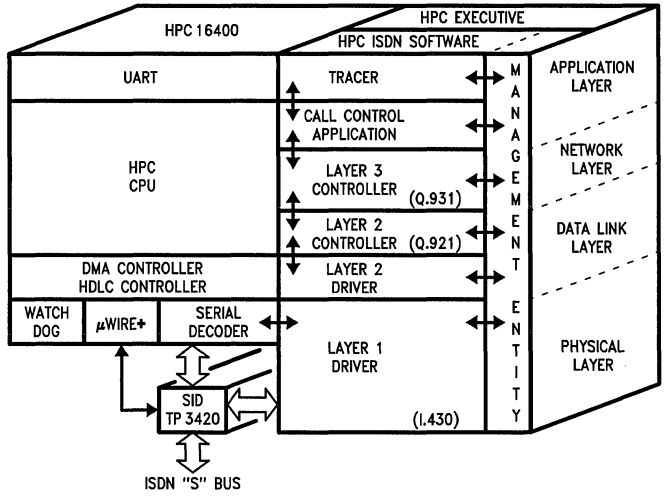
This software is supplied as a disk set and is used in conjunction with HPC development tools and software.

Features

- Multi-tasking executive
- Preemptive scheduling
- Modular software design
- Multiple timer facility
- HPC physical layer I/O interface
- Layer 2 link access procedure for the D channel (LAPD)
- Layer 2 link access procedure for the B channel (LAPB)
- Layer 3 protocol control procedure for a terminal endpoint
- Layer management entity support
- Demonstration Call Control Task
- Task_View task exerciser and debugger
- Message trace capability
- Split frame message formatting
- Source code in C language

Block Diagram

HPC ISDN Software



TL/DD/10077–1

1.0 Architectural Description

1.1 INTRODUCTION

This description defines the software required to implement the ISDN Basic Rate Interface on the HPC family of microcontrollers, including the HPC16400 which has onboard hardware specifically designed for Data Communication and ISDN applications.

The software consists of the following main parts, shown in overview in *Figure 1.1:*

- HPC Executive, providing an operating environment and services for the ISDN software and for additional application software written by OEM users of the HPC.
- I/O Drivers, interfacing to the DMA/HDLC controllers on the HPC16400 and to the TP3420 "S" Interface Device.
- Data Link Layer Software, implementing the CCITT Q.921 and X.25 link access procedures (LAPD and LAPB).
- Network Layer Software, implementing the Protocol Control Procedures defined in the CCITT Q.931 standard.
- Demonstration Call Control Module, allowing a development engineer at a terminal to make and receive ISDN phone calls which exercise the above software.
- Tracer Module, allowing a development engineer at a terminal to monitor the operation of the above software.
- Management Entity Module

1.2 SOFTWARE ARCHITECTURAL PRINCIPLES

1.2.1 Modular Multitasking Environment

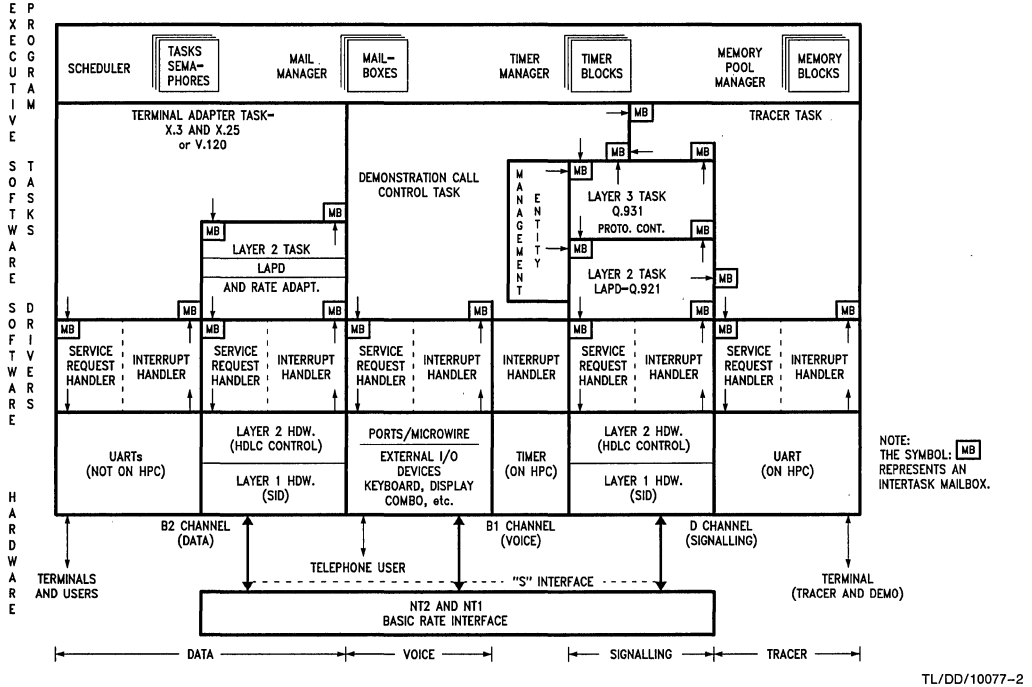
Eack layer or function is written as a separate software task. Intertask communications and the interface between tasks and I/O drivers is by means of mail messages and semaphores, which are managed by the multi-tasking HPC Executive.

This modular design and well defined intertask interface make it easy for users to interface application-dependent software to the modules provided. The services of the HPC Executive (mail, semaphores, timers, memory management) facilitate the writing of software tasks and I/O drivers. These services are available to all tasks and to interrupt-level drivers.

1.2.2 Event-Driven State-Machine Architecture

Telecommunication software typically involves many invocations of the same code (one per call, one per logical connection, etc.) and requires a particular software architecture: tasks must be structured as event-driven state machines. Each task has one or more mailboxes and operates by picking up mail, one message at a time, from the mail queue, and processing the message to completion before returning for the next mail message.

Each "entity" within a task (each call, each logical connection, etc.) has a state block, indicating its current state. After picking up a mail message, the task identifies the entity involved in the message, accesses the state block for that entity, processes the message based on the state of the entity, and finally sets the state block to the new state of the entity.



TL/DD/10077–2

FIGURE 1.1 HPC16400 Software for ISDN

1.0 Architectural Description (Continued)

1.2.3 Coding Standards

The coding standards for software development have been designed to ensure development of consistent, structured code, which can be easily used and easily maintained over the life of the code.

1.3 HPC EXECUTIVE

The HPC Executive provides an operating environment for the Layer 2 and Layer 3 tasks, the application tasks, the various support tasks, and the I/O drivers which interface to the hardware. It provides the following services to the tasks and I/O drivers:

- Scheduling of tasks that are ready to run, based on task priority. Preemptive scheduling and time slicing can be optionally enabled.
- Task-task and driver-task communication, by means of mail messages, which can be sent and picked up, and semaphores, which can be signaled and awaited.
- Timers, which are equivalent to mail messages with a specified delay and which allow tasks and drivers to time their activities and time out when an expected event does not occur.
- Memory management, to allocate and deallocate fixed-size buffers as needed by tasks and drivers.

Application tasks and I/O drivers developed by users of the HPC can easily be inserted in the HPC Executive environment and can take full advantage of its services.

1.4 ISDN TELECOMMUNICATIONS STANDARDS

1.4.1 CCITT Standards

The Layer 2 Task implements CCITT specification Q.921 (LAPD) and Layer 2 (LA{B) of CCITT specification x.25. The last CCITT published version of specification Q.921 is the 1984 Red Book with subsequent CCITT produced revisions. The Layer 2 Task LAPD implementation is based on the version issued in December 1986, CCITT Document COM XI-R 43-E, with the minor revisions issued in September 1987, Temporary Document 644-E Rev. 1. This version is expected to be very close to the next CCITT published version, The 1988 Blue Books. The Layer 2 Task LAPB implementation is based on the 1984 Red Book.

The Layer 3 Task implements the Protocol Control Procedures of CCITT Specification Q.931. Since this specification was still subject to revision, the software is based on the latest version of Q.931 distributed at the ECSA/ANSI T1D1 meeting in September 1987. This version is significantly changed from the 1984 Red Books.

However it is expected to be close to the next CCITT published version, the 1988 Blue Books.

In terms of the September 1987 T1D1 version of the specification, the Layer 3 Task implements the circuit-switched procedures described in Section 5. The Layer 3 Task implements the Protocol Control procedures and some of the Resource Management. The Call Control Task implements a demonstration version of the Call Control Procedures and the balance of the Resource Management.

In terms of the specification and description language (SDL) diagrams in the Q.931 specification, the Layer 3 Task implements *Figure 38* (26 pages).

The establishment and release of logical links are fully covered in the Layer 2 specifications (Q.921), but the Layer 3 aspects of this are not handled in the version of Q.931 on which the Layer 3 Task is based. Therefore, additional Layer 3 states and SDL diagrams have been created and additional software has been written to handle this requirement.

1.5 ISDN TELECOMMUNICATIONS SOFTWARE

The software packages described below are designed to be easily "unbundled" and used independently by a software developer.

1.5.1 Layer 1 I/O Driver

The Layer 1 I/O Driver controls the HPC MICROWIRE/PLUS™ interface, and the onboard Serial Decoder. This driver is responsible for the hardware initialization, the control of the Serial Decoder, the activation and the deactivation of the Layer 1 I/O device. Use of the HPC Executive mail and semaphore services makes this driver simple to implement and easy to enhance by users that require additional Layer 1 hardware interfaces.

1.5.2 Layer 2 I/O Driver

The Layer 2 I/O Driver controls the HDLC/DMA controllers onboard the HPC16400, and interfaces this hardware to the Layer 2 Task. This driver is responsible for the hardware initialization, the reception of frames toward the HPC, the transmission of frames away from the HPC, and appropriate error handling. Use of the HPC Executive mail and semaphore services makes this driver simple to implement and easy to replace with alternative drivers that a user may wish to develop.

1.5.3 Layer 2 Task

The Layer 2 Task implements the full LAPD protocol defined in Q.921, providing error free in-sequence transmission, reception and multiplexing of messages received by an HDLC controller connected to the D signaling channel. The event-driven state machine architecture, described above, enables a single software module to support simultaneous activity on multiple logical connections. The Layer 2 Task also supports X.25 LAPB processing for messages received by a second HDLC controller connected to a bearer B channel.

1.5.4 Layer 3 Task

The Layer 3 Task implements the user side of the Protocol Control Procedures of Q.931, which are used to setup, answer, suspend, resume, and disconnect a call. Specifically, it implements all of *Figure 2*/Q.931 of Q.931. The event-driven state machine architecture, described above, enables a single software module to support simultaneous activity relating to calls on both bearer B channels.

1.5.5 Demonstration Call Control Task

The latest versions of Q.931 separate the Layer 3 procedures into Protocol Control Procedures and Call Control Procedures. Call Control Procedures are application dependent. These procedures handle bearer channel selection and actual establishment of the voice channel. As Q.931 notes, these procedures can also be considered to be part of the Applications Layer. The Call Control Task implements a minimal subset of the Call Control Procedures, for demonstration purposes. In an actual application, this task will be replaced by an application-specific task, tailored to the capabilities of the actual terminal equipment (number of terminals, handsets, etc.).

1.5.6 Management Entity Task

The Management Entity Task, which is only generically defined in Q.921 and Q.931, handles housekeeping functions

1.0 Architectural Description (Continued)

for all layers. These functions include TEI negotiation with the network management entity, and the handling of unrecoverable errors. This task implements as much of the management entity as is currently defined and in addition whatever is necessary for the operation of the other tasks.

1.5.7 Tracer Task

The Tracer Task serves two purposes; to demonstrate the lower ISDN layers via a menu-driven telephone emulation mode, and to trace system mail message traffic.

1.5.8 Task_View Task Exerciser and Debugger

Task_View is a special-purpose task that can be inserted into the multi-tasking Executive environment in place of the Tracer Task. It reads and interprets a user supplied ASCII scenario file. Under control of this senario file, Task_View sends mail messages to a specified mailbox (or mailboxes), where they are read by the task under test. Mail messages sent by the task under test in response to this input are then displayed by Task_View. In this way the task may be exercised and debugged.

2.0 Functional Description

2.1 INTRODUCTION

This description defines the functional requirements of the ISDN Basic Rate Interface Software Package implemented on the National Semiconductor HPC Microcontroller Family. Specifically, the HPC16400 Software Package implements or supports the following high-level functions:

- Multi-Tasking Executive
- HPC Physical Layer I/O Interface
- Layer 2 Link Access Procedure for the D Channel (LAPD)
- Layer 2 Link Access Procedure for the B Channel (LAPB)
- Layer 3 Protocol Control Procedure for a Terminal Endpoint
- Management Entity Support
- Call Control Demonstration Task
- Message Trace Capability

The HPC ISDN Software Package has been divided into several functional software elements, as illustrated in the HPC ISDN Functional Block Diagram, *Figure 2.1*. These functional elements correspond to software modules. The purpose of this section is to introduce the various software elements, to define their interactions, and to relate their functionality to the appropriate ISDN standards, where applicable.

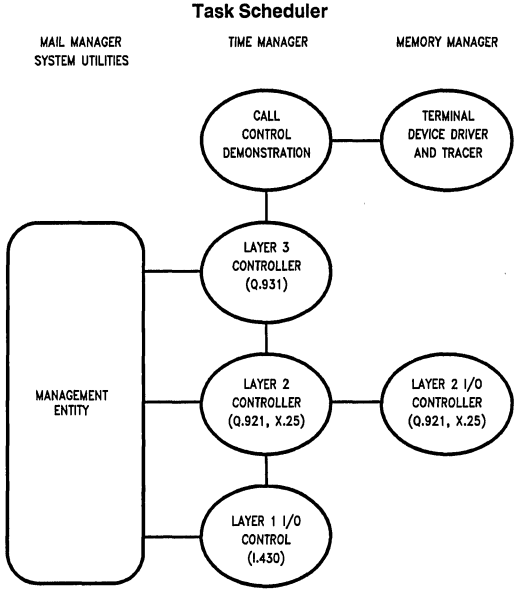
The HPC ISDN Software Package will require additional software drivers and application-specific tasks prior to serving as a useful ISDN Terminal Endpoint (TE) entity. The HPC ISDN software has been coded and documented to allow easy integration of additional application code.

The HPC ISDN Software elements illustrated in *Figure 2.1* have been divided into the following categories.

- HPC Executive (2.2)
- I/O Device Drivers (2.3)
- ISDN Layer Protocol Tasks (2.4)
- Application Tasks (2.5)
- System Utilities (2.6)

The HPC Executive contains software elements that are necessary for HPC ISDN Applications. These elements include a Multi-Tasking Scheduler, a Memory Manager, a Timer Manager and a Mail Manager. The HPC Executive software elements are tightly coupled, and streamlined for the National Semiconductor HPC family of controllers.

The I/O Device Drivers interface the HPC hardware elements to the HPC ISDN Software. The Layer 1 Driver implements the ISDN PHYSICAL Layer 1 requirements for the HPC ISDN system. The Layer 2 Driver interfaces the HPC DMA/HDLC controller channels to the Layer 2 Link Access



TL/DD/10077–3

FIGURE 2.1 HPC ISDN Software Functional Block Diagram

2.0 Functional Description (Continued)

Procedures. The Terminal Device Driver interfaces the HPC on-board UART to the ISDN Software. Device initialization sequences, service request tasks and accompanying interrupt service routines are all defined in the I/O Device Driver section of this document.

The Layer Protocol Tasks implement the ISDN DATA LINK Layer 2 and the NETWORK Layer 3 requirements for the HPC ISDN system. These tasks are designed to be hardware configuration and application independent. The Layer 2 Task provides both the "USER SIDE" and the "NETWORK SIDE" implementation of the CCITT Specification Q.921. The Layer 3 Task provides the "USER SIDE" implementation of CCITT Specification Q.931.

The Layer 2 Task has been designed to use many of the same routines to implement the link access procedures on either the signaling D channel or the bearer B channel (LAPD or LAPB). Design decisions have also been made to facilitate the implementation of V.120, the new rate adaption scheme that processes LAPD frames on a bearer B channel.

The Management Entity Task and the Call Control Task are Application (Specific) Tasks that are closely coupled to the specific system hardware configuration and the Central Office Network Entity Software. These tasks are provided for demonstration purposes to drive the ISDN layer entities. Application users must either replace or extensively rewrite these tasks to match their particular ISDN Application environment.

The System Utilities include the power-up reset Main Task, the NMI handler, the Timer interrupt handler, and the Watchdog Task.

The Tracer utility provides the capability of on-line tracing of intertask mail messages and task states. Tracer is primarily a passive task; it displays messages that it receives from other tasks. Tracer also provides a user interface for Telephone Simulation.

The remainder of this document is devoted to defining each of the software elements at the functional level. Where applicable, specific ISDN standard documents such as CCITT Q.921, Q.931 and X.25 will be referenced, rather than duplicating the information here.

2.2 HPC EXECUTIVE

The HPC Executive provides a multitasking environment within which the ISDN and applications tasks can run and it provides various system services to those tasks. The services of the Executive are available to both tasks and interrupt service routines.

2.2.1 Tasks, Priorities, and the Ready Queue

A task is a subroutine which can be run (called) by the Executive. Tasks are managed by the Executive as Task Control Blocks (TCB's). A task's TCB contains all the parameters needed by the Exeuctive to handle the task, in particular, the task's priority and its current starting address.

Tasks which are not blocked waiting for a semaphore or for mail are considered to be ready to run and their TCB's are queued on the Ready Queue, in the order of the tasks' priorities. The Task Scheduler runs the task at the head of the Ready Queue, i.e., the highest priority task that is ready to run. In this way the processor is always given to the highest priority task that is ready to run.

Once a task is started, it continues to run until it does a Semaphore Wait, ReadMail, or Return or, until a higher priority task is put on the Ready Queue, at which time the scheduler has the opportunity to once again choose the task at the head of prioritized Ready Queue and run that task.

A task may change the priority of any task, including itself. The priority change takes place immediately, to the extent that the target task's TCB is updated with the new priority and the queue in which the target task's TCB is waiting is resorted to reflect the new priority.

If the target task is in the Ready Queue and its new priority is higher than the priority of the running task, then the target task will run once all protected sections are exited. See Section 2.2.3, below.

2.2.2 Semaphores

A semaphore is a global variable, accessed through the Executive, which can be Signaled (incremented) by one task and Waited on by another task. A semaphore is typically used to manage the sharing between tasks of some resource, e.g., an I/O device, mail messages, etc. At any moment the value of a semaphore may be positve, negative, or zero. A positive value indicates the number of resources available, a negative value indicates the number of tasks waiting for resources and a zero value indicates that there are no resources available and no tasks waiting for them.

When a task Waits on a semaphore, if the semaphore has a nonzero positive value, the task will immediately go on the Ready Queue and the semaphore value will be decremented by one. On the other hand, if the semaphore has a zero or negative value, the task will be queued on the semaphore and the semaphore value will be decremented by one. When a task Signals a semaphore, the semaphore's value is incremented by one and the highest priority task waiting on the semaphore is put on the Ready Queue.

A common use for a semaphore is the management of a non-shareable resource, such as an I/O device. When the device is available, the associated semaphore has the value $+1$. When a task wishes to obtain exclusive use of the device, it Waits on the semaphore, which is then decremented to 0, with the task going immediately back on the Ready Queue. If another task then attempts to use the device, its Wait call will cause it to be placed on the Semaphore Queue and the value of the semaphore will be decremented to -1. Other tasks may also Wait on the semaphore, each decrementing its value by one. The negative value of the semaphore indicates the number of tasks Waiting for the device. The waiting tasks are ordered in the semaphore queue according to their priority. When the first task is done with the device, it Signals the semaphore, which moves the first waiting task to the Ready Queue and increments the semaphore or, if there are no waiting tasks, returns the semaphore to its original value of $+1$.

2.2.3 Preemptive Scheduling

Preemptive scheduling enables the executive to respond quickly to high priority events. If a task that is waiting on a Semaphore Queue modes to the Ready Queue and if that task is of higher priority than the currently running task, then, as soon as the currently running task emerges from all critical sections and non-preempt sections, the currently running task will stop running. The task that was moved to the Ready Queue will run. The preempted task will be placed on the Ready Queue in the normal manner.

2.0 Functional Description (Continued)

Executive functions allow preemption to be selectively turned on or off by task or for an entire application.

2.2.4 Time Slicing

Time slicing modifies the task scheduling algorithm as follows: at each "tick" of the timer clock (the clock which also controls the time-out timers), if the currently running task has the same priority as the task at the head of the Ready Queue, then, if the currently running task is not in a non-preempt section, it will stop running and the task at the head of the Ready Queue will run. The task that stops running is placed on the Ready Queue in the normal manner, i.e., after all tasks of equal priority. Time slicing enables the Executive to share the processor equally between tasks of equal priority.

2.2.5 Mailboxes and Mail Messages

The main form of intertask communication is the sending and receiving of mail. Mailboxes exist independently of tasks; any task may send mail to any mailbox and any task may read mail from any mailbox. However, in a typical system, each task has one mailbox from which it reads all its mail and to which other tasks send mail destined for that task.

Mail is prioritized. When a task calls upon the Executive to perform a SendMail, it specifies the priority of the message, which is inserted in the specified mailbox queue sorted by priority.

2.2.6 Timers

The Executive includes a timing facility specifically designed to handle the time-outs typical of telecom protocols and other real-time applications.

Timers are essentially a form of delayed mail. When a task sets a timer, the task provides a mailbox identifier, a mail message, and a time delay value. When the specified time delay is up, i.e. when the timer "expires", the mail message is mailed to the specified mailbox. When a task sets a timer, it receives a timer ID, which can be used to cancel the timer, if necessary, before it expires.

2.2.7 Memory Management

The memory manager is responsible for allocating and deallocating fixed-size memory blocks from fixed-size pools, which are completely defined at compile time. A memory pool may reside in extended memory.

2.2.8 System Module and Interface Module

The Multi-Tasking Executive Software is available either as source code or as object code. The interface module, which must be modified to insert application tasks, is always supplied as source code.

2.3 I/O DEVICE DRIVERS

I/O Device Drivers serve as interface routines between the HPC hardware machinery and the HPC Executive and Application Tasks. "Input" operations (data heading toward Application Tasks) are typically fielded by an Interrupt Service Routine (ISR). The ISR may SEND information to the appropriate task via the system mail facility, or it may signal the appropriate semaphore to schedule an I/O task. "Output" operations (data heading away from Application Tasks) are typically fielded by Service Request (SRQ) Tasks. SRQ Tasks communicate directly with the hardware control registers to initiate output operations. These tasks often work closely with their accompanying ISR for output initiation and completion. Higher layer tasks send mail messages to he SRQ Tasks, using the system mail facility to queue messages pending output.

The HPC ISDN Software includes three I/O Device Drivers: the Layer 1 Driver, the Layer 2 Driver and the Terminal Driver. The functionality of these drivers is defined below. Details of particular Device Driver ISR and SRQ Task interactions are defined in the Software User's Manual.

2.3.1 Layer 1 I/O Device Driver

The Layer 1 I/O Device Driver provides implementation of the ISDN PHYSICAL Layer 1 for the HPC environment. This Device Driver controls the NSC MICROWIRE/PLUS Interface to the NSC TP3420 "S" Interface Device (SID), and the HPC16400 onboard, Serial Decoder. Control of a COMBO™ Codec, a display, and a keypad has been implemented later by either adding to this driver, or using it as a model for additional drivers.

The primary responsibility of this driver is to initialize and control the SID. The higher layer ISDN tasks mail activation and deactivation messages to the Layer 1 Service Request Task. This task sends the appropriate command to the SID via the MICROWIRE/PLUS Interface. The SID interrupts the HPC whenever it changes state. The Layer 1 Interrupt Service Routine fields responses when the SID changes state and mails the information to the Layer 2 Controller Task and to the Management Entity Task.

The Serial Decoder is initialized to MODE 4, with the ISDN D Channel terminated by DMA/HDLC Channel #1, and Bearer Channel B2 terminated by DMA/HDLC Channel #2. The SID can swap B1 and B2 internally to allow voice or data on either channel.

The Layer 1 I/O Device Driver can communicate with any other Task via the System Mail Utilities.

2.3.2 Layer 2 I/O Device Driver

The Layer 2 I/O Device Driver interfaces the two HPC16400 onboard DMA/HDLC channels; one to the 16 kbit per second "D" signaling channel, and one to the 64 kbit per second bearer (B2) channel. The Layer 2 Service Request Task receives Physical Layer (PH) Primitives from the Layer 2 Controller Task via the system mail utility. The Layer 2 Interrupt Service Routine handles block messages received from the DMA Controller and mails them as Physical Layer (PH) Data Primitives to the Layer 2 Controller Task. This generic mail message interface allows an Application User to easily introduce external DMA and HDLC Controllers, and accompanying device drivers, that either replace or complement the existing onboard controllers.

HDLC/DMA Channel #1 is attached to the ISDN signaling D channel, and will be referred to as the LAPD Channel. HDLC/DMA Channel #2 is attached to bearer channel B2, and will be referred to as the LAPB Channel. The two channels operate independently of each other as much as possible. Since they share the same interrupt hardware, the Layer 2 Interrupt Service Routine must poll the Message Pending Register and the Error Status Register to determine the source of each interrupt. Both HDLC/DMA channels use the HPC field separation feature for transmission and reception of data. This feature relieves some memory concerns, since it allows small memory buffers to be used for mes-

2.0 Functional Description (Continued)

sages that only have headers. In the transmit direction this feature allows large contiguous buffers to be broken up into smaller send buffers without having to copy them following a header. Issues specific to the HDLC/DMA Channels are defined below.

HDLC/DMA Channel #2, the LAPB Channel, requires frame sizes to be nominally 130 bytes, 2 bytes of header and 128 bytes of information. Provision can be made for messages with up to 1026 bytes, 2 bytes header and 1024 bytes of information.

The presentation of data between the Layer 2 Driver and Layer 2 Controller is identical regardless of which channel the frames are associated with.

2.3.3 Terminal Device Driver and Tracer

The Terminal Device Driver interfaces to the HPC onboard UART. The associated SRQ Driver Task, referred to as Tracer, serves primarily as a high-level demonstration vehicle. Tracer can field mail messages from any other task in the system, as well as keystroke mail messages from its accompanying ISR. Tracer's responsibilities include the following functions:

- Management of the Telephone Simulation User Interface,
- Display Management of the System Trace Mail Messages,
- Proper Display of Task-Related Information

The Telephone Simulation function of Tracer allows the user to enter "telephony-like" keystroke characters, that are passed to Tracer, then on to the ISDN layer tasks for processing. Menu responses are fielded by Tracer to select various levels of the Trace function, as well as to enter and exit the Telephone Simulation mode.

Depending on the level of trace that is selected, Tracer receives mail messages from the system tasks and properly formats them on the CRT display. Tracer offers various levels of trace capability. Trace can be turned off all together, in which case only the application layer Telephone Simulation inputs will be displayed. Trace can display all messages from every layer, or it can be set to "zoom" to display only the messages at a particular layer. Messages will generally have address fields and data fields.

The Terminal Driver's Interrupt Service Routine (ISR) handles keyboard characters from the UART and mails them to the Tracer SRQ Task for further processing. The ISR also handles transmission completion of a character that has been sent to the CRT.

The data structures and hardware interface requirements for the Terminal Device Driver, and capabilities of Tracer, are defined in the Software User's Manual.

2.4 ISDN LAYER PROTOCOL TASKS

The ISDN Layer Protocol Tasks provide implementation of the DATA LINK Layer 2 and the NETWORK Layer 3 in accordance with the protocol definitions of the CCITT Specifications. The two Layer Protocol Tasks (the Layer 2 Controller Task and the Layer 3 Controller Task) are designed to satisy the ISDN Basic Rate Interface (BRI) Terminal Equipment requirements. They are independent of user applications and hardware environment. The PHYSICAL Layer 1 implementation is defined in the I/O Device Driver section of this document. Implementation of layers above the NETWORK Layer 3 are specific to user applications. Two such layer tasks are provided, the Demonstration Call Control Task and the Management Entity Task. These tasks are defined in the Application Task section of this document.

The purpose of the Layer 2 Controller Task is to provide the NETWORK Layer 3 with an error free, sequenced data frame service. The Layer 2 Controller Task uses CCITT Specifications Q.921 and X.25 and the primary functional specifications. The Layer 2 Controller Task satisifies the Link Access Procedures for both the D Channel and the B Channel (LAPD and LAPB). Design considerations have also been included for the future implementation of V.120, the new CCITT rate adaption scheme.

The Layer 2 Controller Task's data frame delivery service allows the Layer 3 Controller Task to confidently setup and teardown user voice and data calls on the available facilities. The Layer 3 Controller Task uses CCITT Specification Q.931 as the primary functional specification. Note that the X.25 Layer 3 packet processor task is not included in the initial software package.

The Layer Protocol Tasks require a somewhat non-conventional task architecture in order to simultaneously manage a significant number of multiple logical connections. This event-driven state-machine architecture requires that a state memory block be created and maintained for each logical connection. When a Layer Protocol Task "wakes up" due to the arrival of mail, the message's address is interrogated to determine which logical connection is to receive the mail. The particular logical connection's state block is retrieved and the mail message is processed per the CCITT Specification requirements, depending on the state of the particular logical connection. Typically, processing the mail message results in sending a Primitive message to another task, and updating the logical connection's state block. The Layer Protocol Task then returns to its mail box to pick up any subsequent mail.

The interface between all of the ISDN Layer Tasks is deliberately achieved via the System Mail Utilities. This ensures a distinct, uniform layering mechanism in the event that application programmers wish to replace layers with their own implementations.

2.4.1 Layer 2 Controller Task

The primary job of the ISDN Data Link Layer 2 is to deliver error-free, sequenced data frames to the Network Layer 3. The Layer 2 Controller Task implements the following Layer 2 Link Access Procedures (LAP) for the HPC ISDN Software Package:

- LAPB per the X.25 CCITT Specification.
- LAPD per the Q.921 CCITT Specification.
- V.120 Terminal Adaption capability.

Since the Q.921 LAPD requirements were derived from the X.25 LAPB requirements, most of the same Layer 2 Controller Task routines can be used to implement both LAPB and LAPD. Design considerations have been made to allow future implementation of V.120.

The Layer 2 Controller Task communicates with the Layer 2 DMA/HDLC Controller Device Driver Task and the Management Entity Task, via the System Mail Utilities. These tasks interrogate the mail message headers to determine whether to process the frames using LAPB or LAPD procedures. The

2.0 Functional Description (Continued)

LPAD frames are mailed to the Q.931 Layer 3 Controller Task, while the LAPB frames are mailed to the X.25 Layer 3 Task.

The HPC16400 HDLC hardware handles the Layer 2 HDLC Procedures, which includes bit stuffing, address recognition, and Frame Check Sequence generation and detection. The Layer 2 Controller Task is responsible for the Layer 2 "Data Link Procedure", which includes the following functions:

- Data Transmission
- Protocol Exception Management
- LAPD-Specific Functions.

To accomplish these functions the Layer 2 Controller supports the full set of Layer 2 Peer-to-Peer messages defined in the CCITT Specification Q.921. These messages are listed below and defined further in the Software User's Manual.

UI	Unnumbered Information Frames
UA	Unnumbered Acknowledge
SABM(E)	Set Asynchronous Balanced Mode (Extended)
DISC	Disconnect Command
DM	Disconnect Mode
I	Acknowledged Information Frames
RR	Receiver Ready
RNR	Receiver Not Ready
REJ	Request Recrimination of Frames
FRMR	Unrecoverable Error, Frame Reject

The Layer 2 Controller Task also supports the primitives required to communicate with the other ISDN tasks.

2.4.1.1 Layer 2 Data Transmission

Layer 2 peer-to-peer Data Transmission is supported with two modes: Unacknowledged Data Mode and Multi-Frame Acknowledged Data Mode. The Unacknowledged Data Mode is used primarily for setting up logical connections and for peer-to-peer Management Entity communication. This mode uses the Unnumbered Information (UI) and the Unnumbered Acknowledge (UA) messages. The Multi-Framed Acknowledged Mode is established by the Set Asynchronous Balanced Mode (SABM) command. This mode provides the mechanism for acknowledgement of data frame transport in each direction. The Multi-Frame Acknowledged Mode is terminated with the Disconnect (DISC) command. The response to the DISC message can be either an Unnumbered Acknowledge (UA) message or a Disconnect Mode (DM) message. The actual Layer 2 data frames are transmitted in the Information (I) messages, while in the Multi-Framed Acknowledged Mode.

The Layer 2 Controller is responsible for avoiding message congestion and buffer overflow. A Layer 2 entity can issue the Receive Ready (RR) command to its peer to indicate that it is ready to continue data transmission. Likewise, the Layer 2 Controller can issue the Receiver Not Ready (RNR) command to its peer to indicate that it is not ready for data transmission.

2.4.1.2 Layer 2 Protocol Exception Management

The Layer 2 Controller Task is responsible for handling exceptions to the Data Link Protocol. These exceptions are of two types: recoverable and unrecoverable. Recoverable exceptions in the receive direction are typically failed frames, which are handled by requesting the retransmission of the failed frame with the Reject (REJ) command. Recoverable exceptions in the transmit direction include the expiry of a Layer 2 Timer. Timer expiry requires the retransmission of the frame that was not acknowledged in time, and all subsequent frames. Timer expiry also prompts a message to the Management Entity. Unrecoverable exceptions result in the Frame Reject (FRMR) response. A message to the Management Entity Task is also sent in this case.

2.4.1.3 Layer 2 LAPD-Specific Functions

The following Layer 2 Controller Task functions are LAPD specific. These functions involve establishing and maintaining multiple logical data link connections. Note that a LAPB connection will be maintained as a special independent logical connection.

A two byte address is required for each logical data link. This address is referred to as the Data Link Connection Identifier (DLCI). The DLCI consists of a Service Access Point Identifier (SAPI) and a Terminal Endpoint Identifier (TEI). The Layer 2 Controller Task is responsible for supporting the TEI Assignment Procedure and the TEI Verification Procedure. These procedures are both initiated by the Management Entity. The Layer 2 Controller Task supports both the Automatic and Non-Automatic TEI Assignment Procedures.

Establishment of the LAPD multi-frame acknowledged data transmission mode requires an extended command (SABME) to prompt the peer entity that the frames are intended for a particular logical data connection identified by the accompanying DLCI. The Layer 2 Controller Task maintains each logical link's state and data frames independently, as explained earlier in this section.

The Layer 3 Controller Task addresses and maintains independent logical connections via an identifier called a Connection Endpoint Suffix (CES). Since the CES is different from the Layer 2 Terminal Endpoint Identifier (TEI), a mapping function is required. The Layer 2 Controller Task maintains a CES–TEI translation procedure to properly address Layer 3 logical entities.

2.4.2 Layer 3 Controller Task

The Layer 3 Controller Task implements the application independent portion of the ISDN NETWORK Layer 3 protocol, per the Q.931 CCITT Specification. The primary responsibility of the Layer 3 Controller Task is to establish a network access connection link between a terminal and its peer in the Central Office.

The Layer 3 Controller Task communicates with both the Layer 2 Controller Task and the Call Control Task by sending primitives via the System Mail Utilities. The Layer 3 Controller Task also communicates with the Management Entity Task. The HPC ISDN Layer 3 Controller Task is responsible for the following NETWORK functions:

- Call Establishment and Clearing
- Call Suspension and Resumption
- Call Status and Notification
- Protocol Exception Management.

2.0 Functional Description (Continued)

The Layer 3 Controller Task supports all the Network Layer Peer-to-Peer messages defined in the CCITT Specification Q.931, i.e.:

- Call Establishment and Clearing Messages:

ALERT	Alerting
CALL PROC	Call Proceeding
CONN	Connect
CONN ACK	Connect Acknowledge
INFO	Information
PROG	Progress
SETUP	Setup
SETUP ACK	Setup Acknowledge
DISC	Disconnect
REL	Release
REL COM	Release Complete

- Call Suspension and Resumption Messages

RESUME	Resume
RESUME ACK	Resume Acknowledge
RESUME REJ	Resume Reject
SUSPEND	Suspend
SUSPEND ACK	Suspend Acknowledge
SUSPEND REJ	Suspend Reject

- Miscellaneous Messages

NOTIFY	Notify
STATUS	Status
STATUS EN	Status Enquiry
USER INFO	User Information

2.4.2.1 Call Establishment And Clearing

The Layer 3 Controller Task's primary responsibility is to establish and clear user network connections on available bearer channel facilties. The Q.931 CCITT Specifications include Call Establishment and Clearing of both circuit-switched and packet-switched calls. Initially, the HPC ISDN Software Package only supports circuit-switched call procedures on Basic Rate Interface (BRI) Bearer Channels. The Layer 3 Controller Task is responsible for Call Reference assignment and maintenance. The Layer 3 Controller Task supports Call Establishment using both the Overlap and Non-Overlap (enbloc) addressing modes.

The procedure for establishing and clearing network connections is defined in CCITT Specification Q.931. It is important to note that the Layer 3 Controller Task maintains an associated state block for each network connection. Primitive mail messages arriving at the Layer 3 Controller Task will be interrogated to determine which network connection is to receive the mail. The mail message is processed depending on the state of the network connection. This processing typically includes the transmission of a Primitive to another Layer Task, and the appropriate update of the network connection state block.

2.4.2.2 Call Suspension And Resumption

Call Suspension (SUSPEND) requires that the Bearer Channel facility and the Call Reference for a call be temporarily relinquished. The network connection is left intact, but in the suspend state. The RESUME command reactivates the call by obtaining a Bearer Channel facility and establishing a new Call Reference. The Suspend function is somewhat analogous to the call HOLD feature.

2.4.2.3 Call Status And Notification

The Network can request the status of a network connection at any time via the USER INFO, NOTIFY and STATUS Commands. The information includes Service Validation and Channel Configuration.

2.4.2.4 Layer 3 Protocol Execption Management

The Layer 3 Controller is responsible for handling exceptions to the Network Control Protocol. The primary Layer 3 Controller Task protocol exception is the expiry of the Layer 3 timer. Such an exception requires the retransmission of the particular command and may prompt a message to the Management Entity Task.

2.4.2.5 Timer Support

The Layer 3 Controller supports the following system timers per CCITT Specification Q.931:

T303	SETUP ACK Timer
T305	DISCONNECT ACK Timer
T308	RELEASE ACK Timer
T313	CONNECT ACK Timer

2.4.2.6 SDL Updates

The Layer 3 Controller Task very closely follows the SDL procedures illlustrated in CCITT Specification Q.931, with a few enhancements. These enhancements are listed here and fully defined in the Software User's Manual.

a. Three new SDL States have been added to accommodate establishing the Data Link corresponding to a particular CES. The new states are:
   - IDLESTATE
   - RELEASEWAIT
   - ESTABLISHWAIT

b. The Q.931 NULLSTATE SDL now accepts a new command, CCBROADCASTRESP. This command is sent from the Call Control Task to allow transistion from the NULLSTATE(0) to the CALLPRESENT State(6) during a Network Originated call via the Broadcast mechanism.

2.5 APPLICATION TASKS

The Application Tasks are very dependent on both the terminal equipment configuration and the far-end Network Entity software implementation. The HPC ISDN Software Package includes two sample Application Tasks: the Demonstration Call Control Task and the Management Entity Task. Both of these tasks can be replaced or updated when ported to a particular application. These tasks are included in the HPC ISDN Software Package primarily to verify the operation of the OSI Layer Protocol Tasks and the HPC Device Drivers.

2.5.1 Demonstration Call Control Task

The Demonstration Call Control Task is closely coupled to the specific facilities of an application. The interaction between the Layer 3 Controller Task and Call Control is defined in CCITT Specification Q.931. In the HPC ISDN Application, the Call Control Task communicates with the Layer 3 Controller Task and the Tracer Task. The availability of two circuit switched voice bearer channels is simulated in the Call Control Task. The Call Control Task sends standard Terminal Equipment prompts and messages to the Tracer Task where they are displayed on a UART driven CRT. The Call Control Task has the following responsibilities:

- B Channel Resource Management

2.0 Functional Description (Continued)

- Connection Endpoint Suffix (CES) Allocation
- Conversion between L3 Primitives and Terminal Action.

The Call Control Task and the Layer 3 Controller Task communicate via the NL_DATA_REQ and NL_DATA_IND Primitives. The messages that are supported between these tasks are listed below.

- Commands from Call Control to Layer 3

CC_SETUP_REQ	Setup Request
CC_SETUP_RESP	Setup Response
CC_SETUP_REJ_REQ	Setup Reject
CC_INFO_REQ	Information
CC_DISCONNECT_REQ	Disconnect
CC_RELEASE_REQ	Release
CC_ALERTING_REQ	Alerting
CC_BROADCAST_RESP	Broadcast Response
CC_CALLPROC_REQ	Call Proceeding
CC_PROGRESS_REQ	Progress
CC_NOTIFY_REQ	Notify
CC_RESUME_RQ	Resume
CC_RESUME_REJ	Resume Reject
CC_SUSPEND_REQ	Suspend Request
CC_SUSPEND_REJ	Suspend Reject

- Command from Layer 3 to Call Control

CC_SETUP_IND	Setup
CC_SETUP_CONF	Setup Confirm
CC_SETUP_COMP_IND	Setup Complete
CCI_NFO_IND	Information Indication
CC_ALERTING_IND	Alerting
CC_PROGRESS_IND	Progress
CC_DISCONNECT_IND	Disconnect
CC_RELEASE_IND	Release
CC_CALLPROC_IND	Call Proceeding
CC_RELEASE_CONF	Release Confirm
CC_STATUS_IND	Status Indication
CC_ERORR_IND	Error Indication
CC_RESUME_CONF	Resume Confirm

The Call Control Task also communicates with the Tracer Task using single byte keystroke like commands. These commands are packaged mail messages containing two bytes: the first byte is the Sender Task's ID, the second byte is the keystroke command. The following messages are sent between Call Control and Tracer:

- Keystroke Commands from Tracer to Call Control Task

TR_ON_HOOK	ON Hook
TR_OFF_HOOK	OFF Hook
TR_DIGIT_1	Digit 1
TR_DIGIT_2	Digit 2
TR_DIGIT_3	Digit 3
TR_DIGIT_4	Digit 4
TR_DIGIT_5	Digit 5
TR_DIGIT_6	Digit 6
TR_DIGIT_7	Digit 7
TR_DIGIT_8	Digit 8
TR_DIGIT_9	Digit 9
TR_DIGIT_0	Digit 0
TR_DIGIT_STAR	Digit *
TR_DIGIT_POUND	Digit #

- Commands from Call Control Task to Tracer

TR_IDLE	Idle, ON HOOK
TR_DIALTONE	Dial Tone
TR_DIALING	Dialing
TR_RINGING	Ringing
TR_BUSY	Busy
TR_CONVERSATION	Conversation
TR_RINGBACK	Ringback
TR_ERROR	Error

2.5.2 Management Entity Task

The Management Entity Task is closely coupled to the accompanying Network Management Entity design and to the terminal hardware configuration. Implementation design decisions have been made that make the Management Entity Task unique to a particular application, while still following the general requirements of the CCITT Specifications. Modifications will be required in the Management Entity Task prior to its successful operation in a particular application environment. The Management Entity Task that is included in the HPC ISDN Software Package presumes a particular hardware configuration and Central Office Software implementation.

The Management Entity Task communicates with the Layer 3 Controller Task, the Layer 2 Controller Task, and the Layer 1 Device Driver Task via the System Mail Utilities.

The Management Entity Task has the following responsibilities:

- Initialization of the Terminal Equipment
- Configuration of the Terminal Equipment
- TEI Assignment and Verification
- Multiple Error Notification
- Unrecoverable Error Notification
- Activation/Deactivation of the Terminal Equipment.

2.6 SYSTEM UTILITIES

The system utilities initializes the HPC system upon power-up, and provide support for various machine specific features of the HPC.

2.6.1 Power-Up Reset Main Task

This task is the entry point upon system power-up. The Main Task is responsible for:

— Initializing the general HPC Hardware.

— Initializing the HPC Executive Data Structures.

— Queuing up the Tasks on the Ready Queue.

The Main Task starts with the highest priority, 255. After running, the Main Task has served its purpose and is removed from the system by waiting on a semaphore which is typically never signaled.

2.6.2 Nonmaskable Interrupt (NMI) Handler

Since terminal power is generally a concern, the HPC can go into an idle, low-power mode when the Terminal Equipment is idle. In this mode the HPC is awakened via an NMI, prompted by a local off hook indication, or by a far-end line

2.0 Functional Description (Continued)

signal detection signal from the SID. Conditions for determining when to go in and out of idle mode are application dependent.

2.6.3 Timer Interrupt Handler

The Timer Interrupt Handler fields interrupts from two of the HPC onboard timers. Timer T0, the Watchdog Timer, overflows every 65536 clock counts. When this occurs the Timer Interrupt Handler mails a message to start the Watchdog Task. Timer T1, the ISDN Software Timer, overflows every 10 ms. The ISDN Software Clock is incremented every tenth Timer T1 overflow, resulting in an ISDN Clock with 100 ms resolution, which is used by the Executive Timer facility.

2.6.4 Watchdog Task

A special task is performed by the HPC's watchdog feature to verify system sanity. The Watchdog Task waits for a mail message that is sent by the Timer Interrupt Handler when Timer T0 overflows. This operation requires that the Watchdog Task be regularly scheduled by the HPC Executive. The Watchdog Task is assigned the highest task priority, 255.

3.0 Ordering Information

3.1 LICENSE AGREEMENT

A license agreement is required for the use and sale of the National Semiconductor ISDN Software. Contact your local National Semiconductor field sales office for more information or contact the factory direct at:

National Semiconductor
ISDN Software Support
M/S 16-174
2900 Semiconductor Drive
Santa Clara, CA 95051

(408) 721-5719

3.2 SOFTWARE ORDER INFORMATION

ISDN software is available in either Object or Source Code format. A Demonstration package is also available. Manuals are included with the Demonstration package and with the Executive and Basic Rate Interface Software packages.

Basic Rate Interface (BRI) software is available for several different central office switches. The generic BRI includes a generalized CCITT Switch Interface.

Each BRI Package contains the following modules:

- Layer 1 Driver (controls S device)
- Layer 2 Driver (controls DMA/HDLC)
- Layer 2 Controller (Q.921)
- Layer 3 Controller (Q.931 Protocol Control)
- Management Entity (Q.921 and Q.931)
- Call Control (Demonstration Application)
- Tracer (Demonstration and Development Tool)

The Multi-Tasking Executive contains two modules:

- Executive Core Module
- Executive Interface Module

The Executive Interface Module is always supplied as source code to allow modification to insert application tasks.

A Multi-Tasking Executive is required to run the Basic Rate Interface.

Order Part Number	Description
Multi-Tasking Executive	
HPC-ISDN-EXEC-O	Multi-Tasking Executive Object Code
Basic Rate Interface	
HPC-ISDN-BRI-S	Basic Rate Interface (Generic) Source Code
HPC-ISDN-BRID-S	Basic Rate Interface (DMS-100) Source Code
HPC-ISDN-BRI5-S	Basic Rate Interface (5ESS) Source Code
Demonstration Package	
HPC-ISDN-PCDEMO	ISDN Basic Rate Interface Demonstration (includes Multi-Tasking Executive and Basic Rate Interface Software Manuals)

4.0 Other Related Information

4.1 DEVICE INFORMATION

Additional technical information on devices referenced in this datasheet is available from National:

HPC16400 High Performance microController
HPC16083 High Performance microController
TP3076 COMBO II™
TP3420 CCITT S/T Interface

4.2 DEVELOPMENT SUPPORT INFORMATION

Development tools are available for the HPC Family of Microcontrollers. These tools support the ISDN development environment. ISDN software must be ordered separately.

4.2.1 ISDN Demonstration Kit

A kit is available that demonstrates the software and hardware discussed in this datasheet. Included in this kit is a TP3500 development board featuring the HPC16400, TP3070 COMBO II, TP3420 "SID" and ISDN Basic Rate Interface software in ROM. A complete set of manuals are included. This demonstration kit may be ordered from National, part number.

ISDN-TP3500-Kit

4.2.2 Development Systems

Several different Microcontroller-On-Line-Emulator Development Systems are available for hardware and software development of the HPC Family of Microcontrollers. Complete information on Development Systems and Accessories may be found in the Microcontroller Development Support Datasheet.

National Semiconductor

ISDN Glossary of Terms

ISDN— Integrated Services Digital Network. ISDN supports both digitized-voice and data transmission.

ISO Layered Protocol Model

The ISO (International Standards Organization) has defined a 7 layer model structure which describes convenient break points between various parts of the hardware and software in any data communications system.

Layer 1: Physical layer, that is the hardware which transports bits across interfaces. This includes ISDN transceivers, modems etc., power supplies, methods of activating and de-activating a transmission link, and also the transmission medium itself, such as wire, fiber, plugs and sockets, etc.

Layer 2: Data Link layer, which describes a basic framing structure and bit assignments to enable higher layer messages to be passed across a physical link. HDLC framing, addressing and error control are the major elements of this layer in ISDN.

Layer 3: Network layer, that is those parts of a message associated with setting-up, controlling and tearing-down a call through the network. These are all software control functions, and generally this is the highest layer in the ISO protocol model which is specific to the ISDN protocols.

The top 4 layers relate to the structure of the actual application programs;

Layer 4: Transport layer, concerned with defining sources and destinations within an operating system for the transfer of application programs.

Layer 5: Session layer.

Layer 6: Presentation layer.

Layer 7: Application layer.

These layers are generally running on a high level machine, and discussion regarding this machine is outside the scope of this document.

"B" Channel, or DS0 Channel

A "B" (for Basic) channel is a 64 kb/s full-duplex transparent data channel. It is octet (= byte) oriented, that is it can be considered as a channel bearing 8k octets/sec. "B" channels are synchronized to the network and are generally circuit-switched. The 64 kb/s rate is also known as a DS0 interface.

"D" Channel

The "D" channel is a packet-mode message-oriented channel on which the data-link layer (layer 2) protocol is carried in HDLC frames. At a basic access point the "D" channel runs at 16 kb/s, while at a primary access point it runs at 64 kb/s. (There is no reason why a "D" channel could not be defined to run at even higher speeds, e.g., 1.544 Mb/s or 2.048 Mb/s, though that does not seem to be a part of current standardization work.)

Three types of data may be handled by a "D" channel:

1. Type "s" (signaling) using Q.931/2 procedures at layer 3.
2. Type "p" (packet) user's packet-oriented data.
3. Type "t" (telemetry) data, typically alarms and energy monitoring functions operating at a low scan rate.

The data type is identified by the SAPI (Service Access Point Identifier) in the HDLC extended address field.

LAPD

Link Access Protocol in the "D" channel is the name given to the packet-mode signaling protocol defined in CCITT specs Q920 and Q921 for the data link layer (layer 2). At layer 2, LAPD uses the HDLC framing format. This protocol defines the bits, bytes and sequence of states necessary between the user and the network to establish, control and terminate calls using any of the 100 or more types of services which may be available via an ISDN. If the users at both ends of the call are connected to the ISDN, and there is a through path for the D channel, then end-to-end call control is also possible.

Primary Access to the ISDN

Primary access is provided at a DS1 interface, consisting of either:

1. Twenty-three "B" channels plus one 64 kb/s "D" channel at 1.544 Mb/s (North America), or:
2. Thirty "B" channels plus one 64 kb/s "D" channel at 2.048 Mb/s (Europe and Rest of World).

CCITT specification I.431 defines the multiplexing and control schemes for primary access.

Basic Access to the ISDN

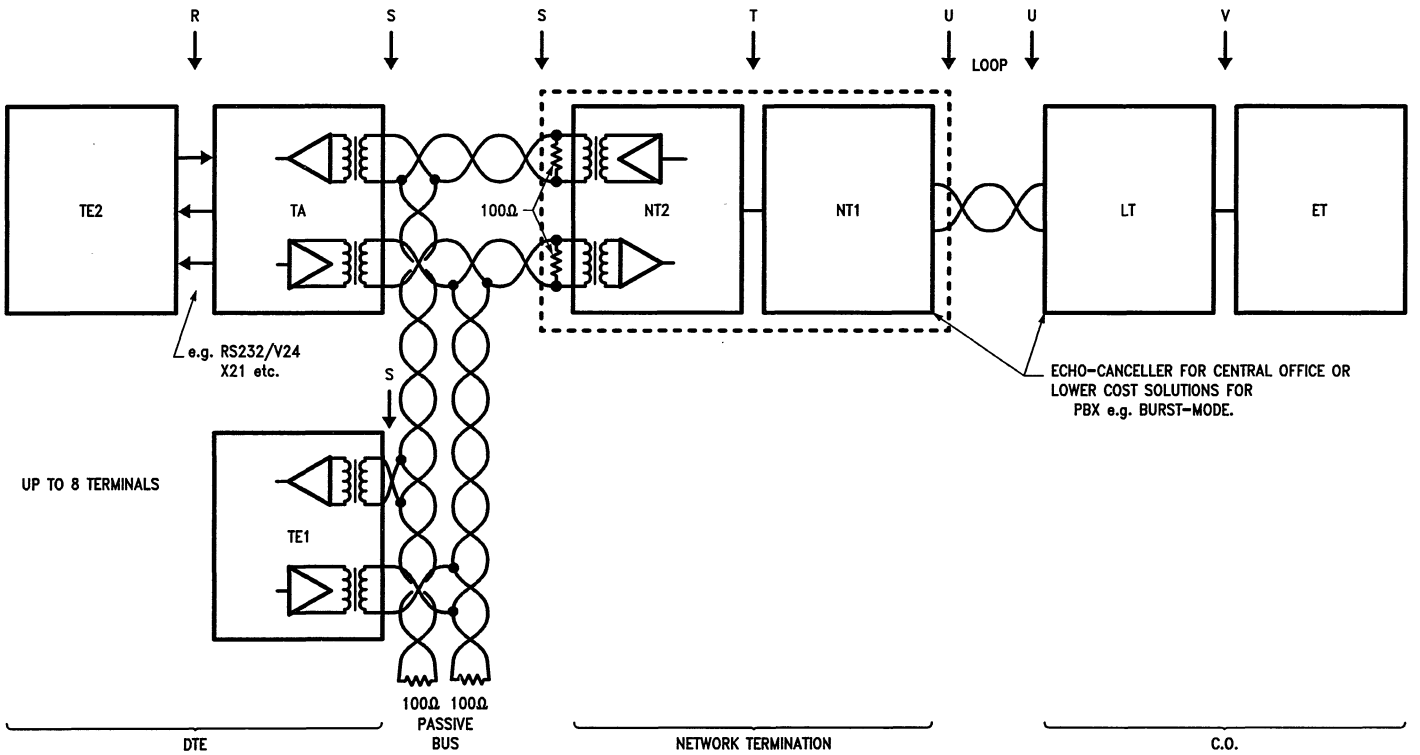
Two independent "B" channels (B1 and B2) together with a "D" channel operating at 16 kb/s form the basic access structure. A minimum transmission rate of 144 kb/s full duplex is therefore required for basic access transport, although for transmission, additional bits are added for framing and maintenance.

Figure 1 shows the names of the functional blocks and interfaces as defined in CCITT specifications.

U Interface

The "U" interface is the single twisted pair loop between a customer's premises and the local Central Office. To transmit 144 kb/s or more full-duplex over this link, which may be several miles long and have over 40 dB of attenuation of the data signal, requires a complex transceiver. Adaptive echo-cancellation techniques are necessary and, although the transmission format is not yet standardized by CCITT, considerable work in the U.S. T1D1.3 ISDN Study Group has established a standard for North America. 160 kb/s is the transmission rate, while the line code is 2B1Q.

2B1Q Line Code— Line code in which two binary bits are converted into one quaternary (4-level) symbol for transmission across the U interface.



TE: Terminal Equipment
TA: Terminal Adaptor (Protocol Conversion & Rate Adaption for Non-ISDN Terminals)
NT2: Network Termination 2 (Switching)
NT1: Network Termination 1 (Loop Transceiver, Power Extraction)
LT: Line Termination (Loop Transceiver, Power Feed)
ET: Exchange Termination (Protocol Handling, MUX/DEMUX, Switching)

FIGURE 1. The ISDN Interfaces

S Interface— A reference point on the customer side of the NT2 to which you can connect either an ISDN terminal (TE1) or a TA; for example, the interface through which a digital telephone could connect to a PABX. This interface accommodates point-to-point operation and point-to-multi-point for up to 8 terminals (the "Passive Bus").

The "S" interface passes the same 2 "B" channels and the "D" channel on to the terminals, together with some additional bits used for synchronization, contention control in the "D" channel, and other housekeeping functions. CCITT specification I.430 defines the physical layer of this interface. A transceiver is required for transmission at the 192 kb/s bit rate, over separate transmit and receive twisted pairs (which already exist in both office and residential telephone wiring within the premises in many countries). Alternate Mark Inversion coding is used.

2 additional pairs are specified as an option, 1 for power and 1 for spare, making this an 8 wire interface. A plug and jack have been standardized so that the "S" interface can be a "universal portability point" for ISDN terminals from any manufacturer in the world.

T Interface— Electrically identical to the S interface, the T interface links the NT2 to the NT1 (informally on business premises only).

R Interface— Connects a terminal adapter (TA) to non-ISDN (TE2) equipment, often through an RS232C port.

TE—Terminal Equipment

Two sub-groups of terminals are defined:

1. TE-1 is a full ISDN terminal which is synchronized to the network channels (not just the far-end terminal) and uses LAPD signaling. It connects to the ISDN at the "S" reference point, which is intended to be the point in the network at which any type of **Basic** Access terminal can be connected, i.e., the "portability" point.
2. TE-2 is a non-ISDN terminal, generally one of today's asynchronous or synchronous terminals operating at rates < 64 kb/s. This includes terminals which have RS232C, RS449, V.21, V.24, V.35, X.21 or X.25 packet-mode interfaces. Each type of interface must be adapted from the "R" reference point to the "S" reference point by means of a Terminal Adapter (TA).

TA—Terminal Adapter

A terminal adapter converts either asynchronous or synchronous data from non-ISDN terminals into data which is synchronized with ISDN B or D channels. The data rate must be adapted by means of stuffing extra bits in a prescribed pattern into the bit stream to adapt the data rate to a 64 kb/s B Channel or 16 kb/s D Channel.

Terminal adaption also requires the conversion of modem handshaking signals to ISDN compatible signaling, and currently there are 2 competing schemes: either using LAPD in the D channel (i.e. out-of-band signaling) or applying LAPD-type messages but passing them end-to-end via the B channel (i.e. in-band). There are strong arguments for both methods, mostly concerned with how signaling is converted at the boundary between an ISDN and today's network ("interworking"), and it remains to be seen which will win as a standard.

NT—Network Termination

The NT terminates the network at the user's end of the 2 wire loop at the customer's premises. There are 2 categories of NT. An NT-1 converts the "U" interface to the "S" and "T" interface (see *Figure 1*) and acts as the "master" end of the user's passive bus. B and D channels must pass transparently through the NT, and there is no capability for intercepting LAPD messages in the NT-1.

Thus a typical NT-1 for **Basic Access** will consist of an "S" interface transceiver and a "U" interface transceiver connected back-to-back with appropriate power supplies and fault monitoring capability.

An NT can also be an intelligent controller such as a PABX. LAN access node, or a terminal cluster controller, in which case it is called an NT-2.

LT—Line Termination

Typically, the LT consists of the "U" interface transceiver and power feeding functions on the ISDN line card. These functions must interface to the switch at the "V" reference point, which is not currently being standardized by CCITT. It could be a proprietary backplane interface or a nationally specified interface which would allow the LT to be physically and electrically separated from the switch.

CO— Central office. The telephone switching location nearest the customer's premises.

Activation/De-activation

Activation is the process of powering up the Layer 1 "S" and "U" interfaces from their standby (i.e. de-activated) states and sending specific signals across the interfaces to get the whole loop synchronized to the network. A small state machine in each TE and the NT controls this sequence of events, and uses timers to ensure that, if the activation attempt should fail for any reason, the user or network is alerted. At the end of a call an orderly exit from the network is effected by sending de-activation sequences before any equipment can power-down.

Section 5

Physical Dimensions/ Appendices

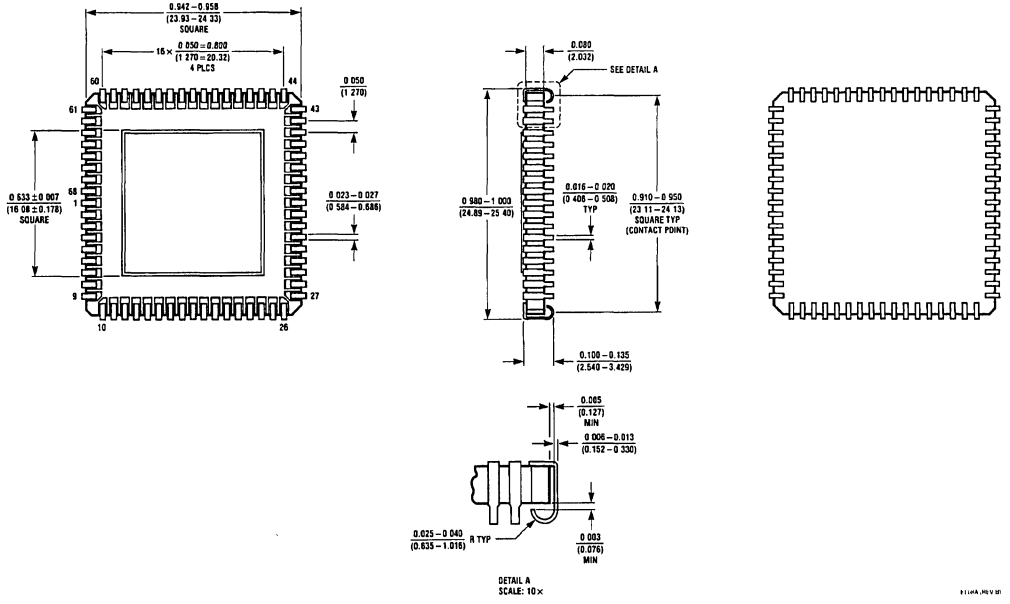
Section 5 Contents

Physical Dimensions 5-3
Bookshelf
Distributors

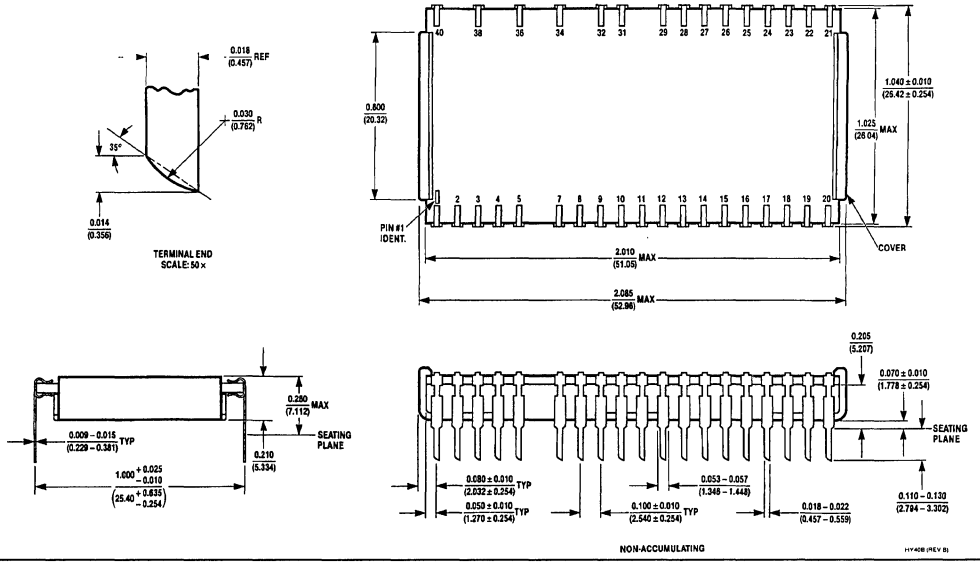
National Semiconductor

All dimensions are in inches (millimeters)

68L Leaded Chip Carrier (E)
NS Package Number EL68A



40 Lead Dual-In-Line Hybrid Package (HY)
NS Package Number HY40B



40 Lead Dual-In-Line Hybrid Package (HY)
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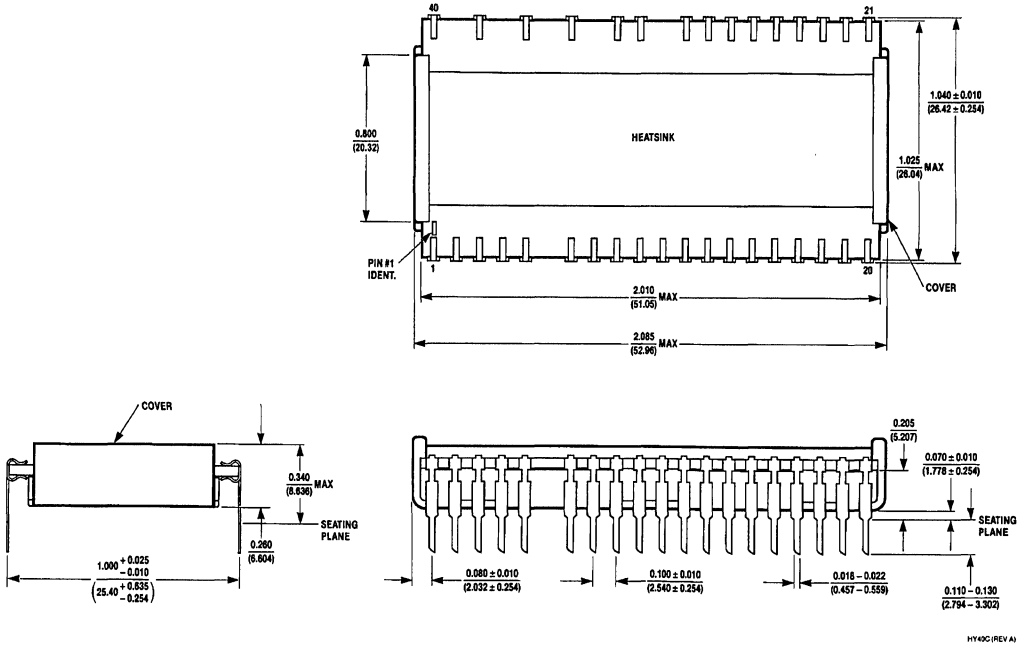
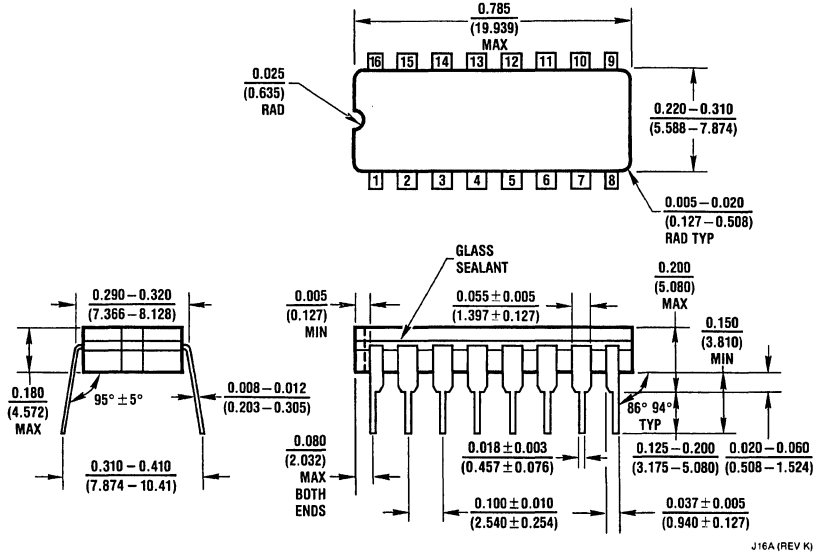


16 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J16A



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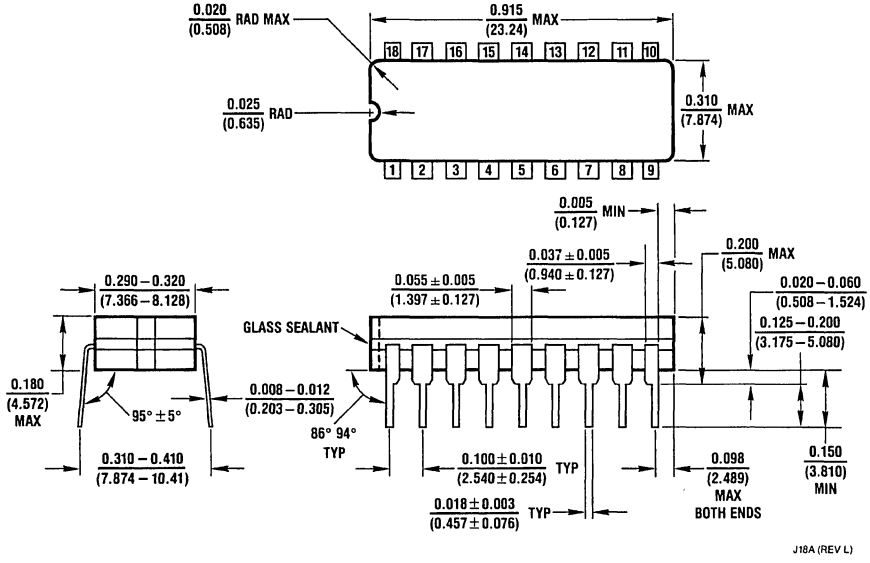

J18A (REV L)

20 Lead Ceramic Dual-In-Line Package (J)
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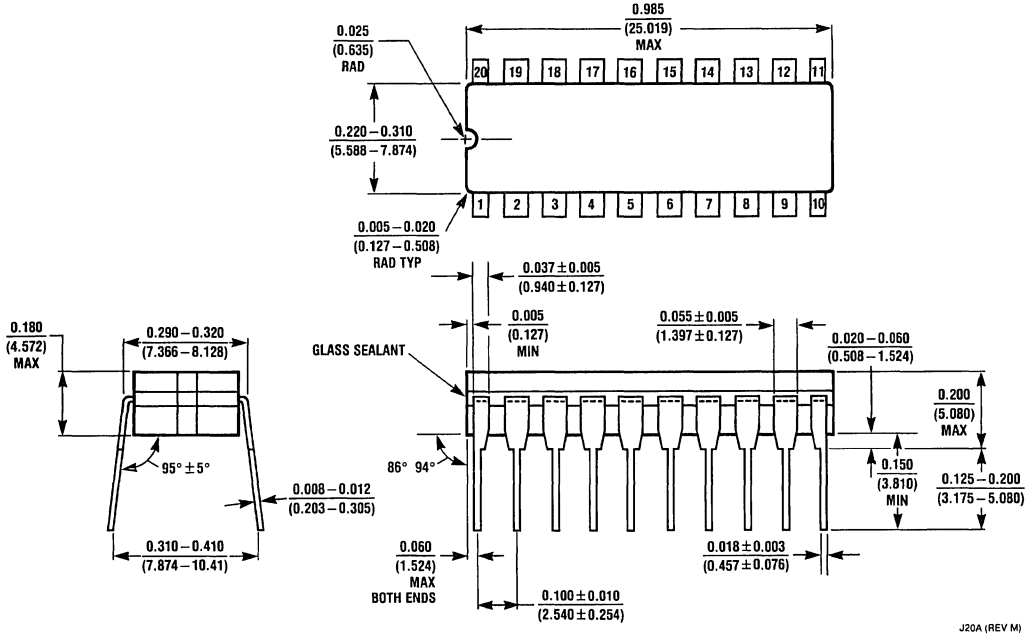
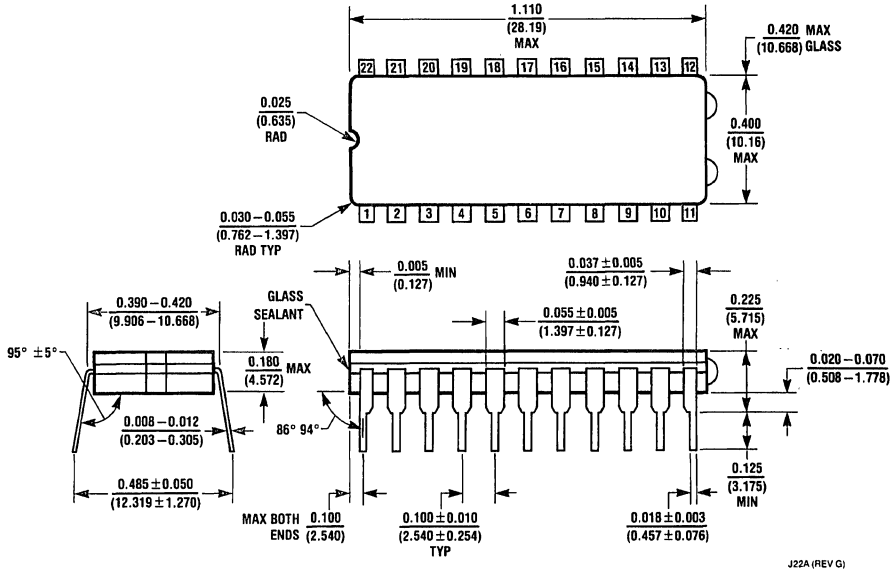


J20A (REV M)

22 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J22A



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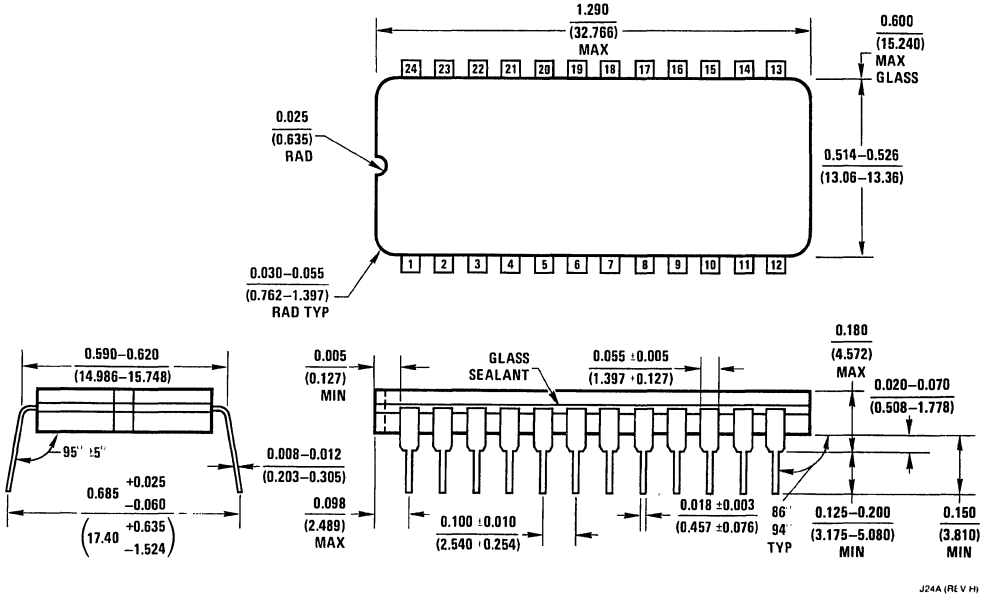
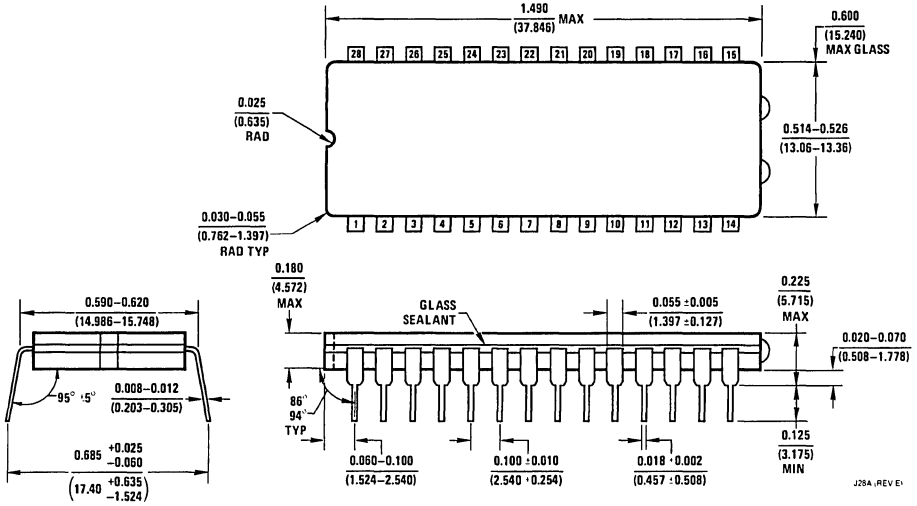
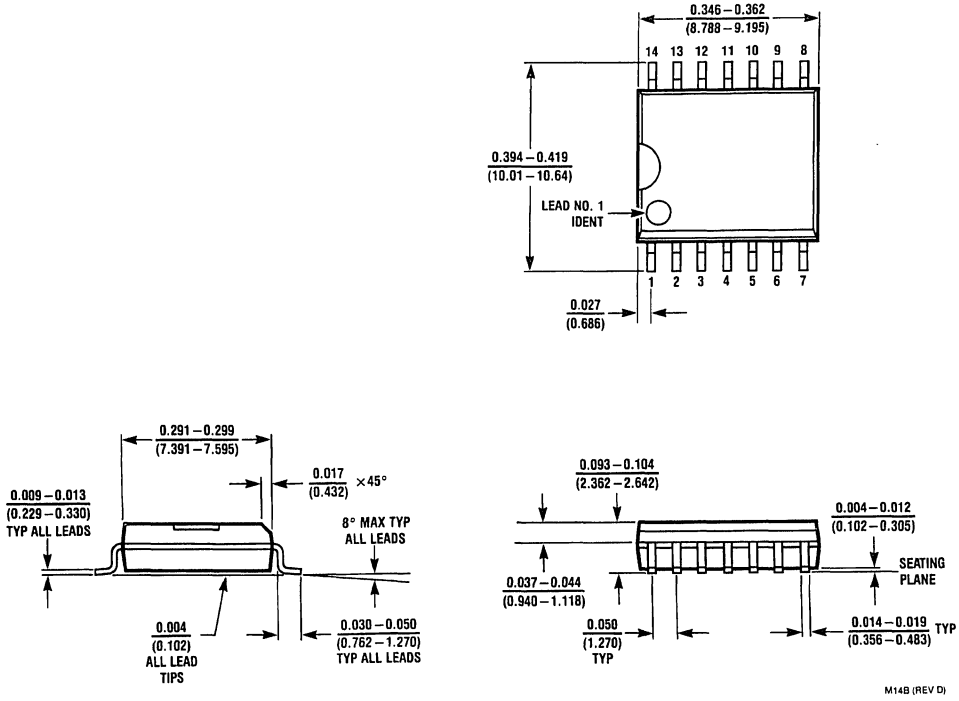


28 Lead Ceramic Dual-In-Line Package (J)
NS Package Number J28A



14 Lead (0.300" Wide) Molded Small Outline Package (M)
NS Package Number M14B



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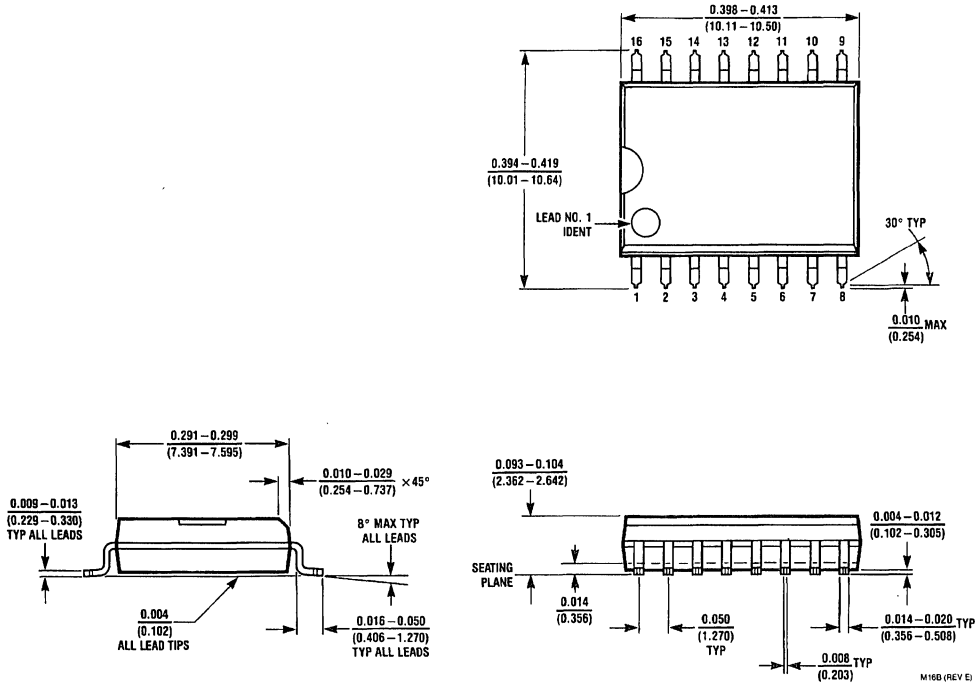
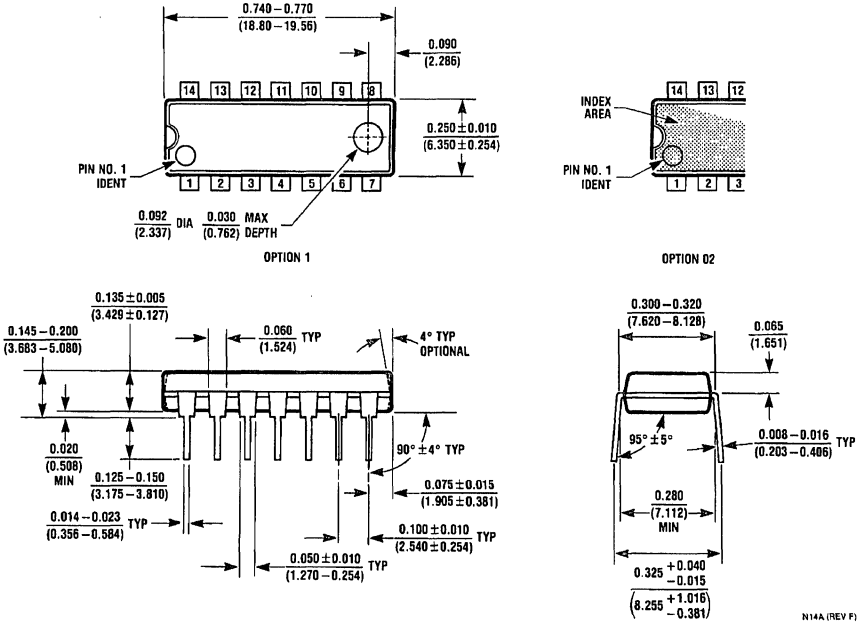
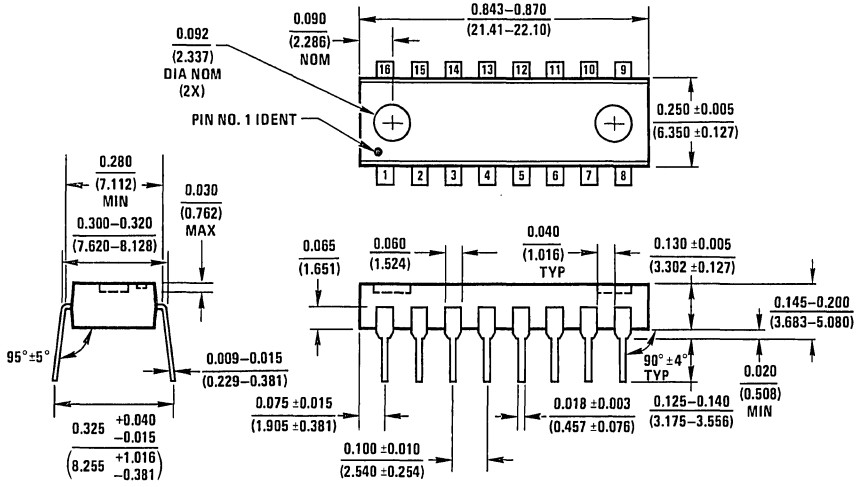
NS Package Number M16B



14 Lead Molded Dual-In-Line Package (N)
NS Package Number N14A

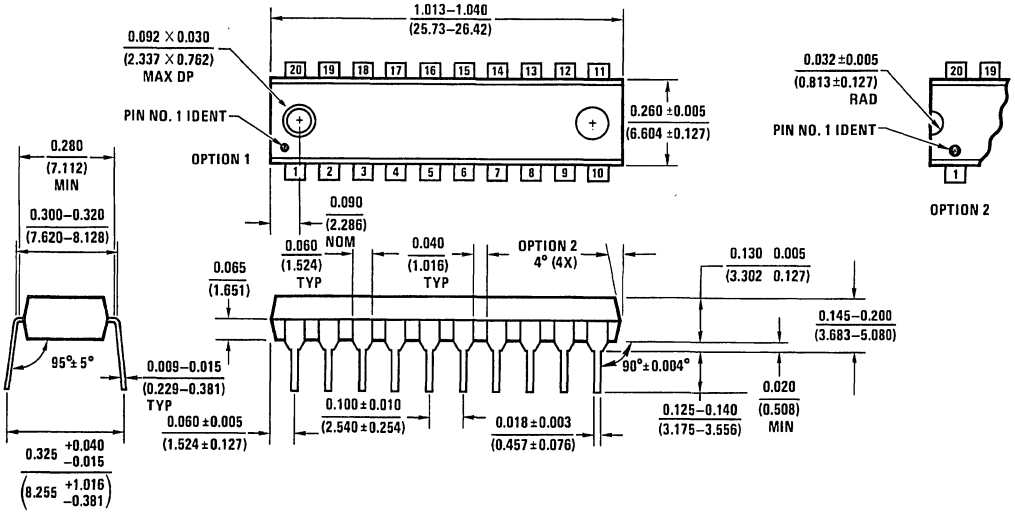


16 Lead Molded Dual-In-Line Package (N)
NS Package Number N16A



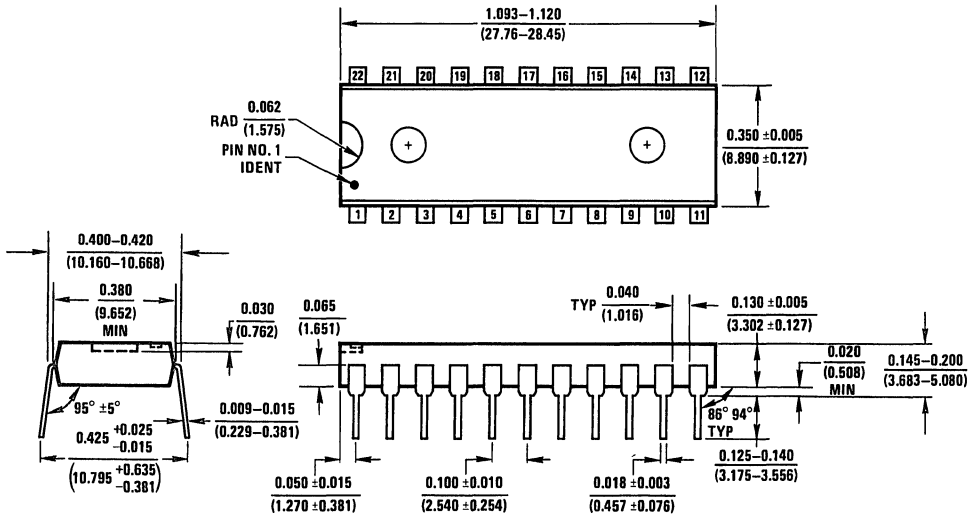
N16A (REV E)

20 Lead Molded Dual-In-Line Package (N)
NS Package Number N20A



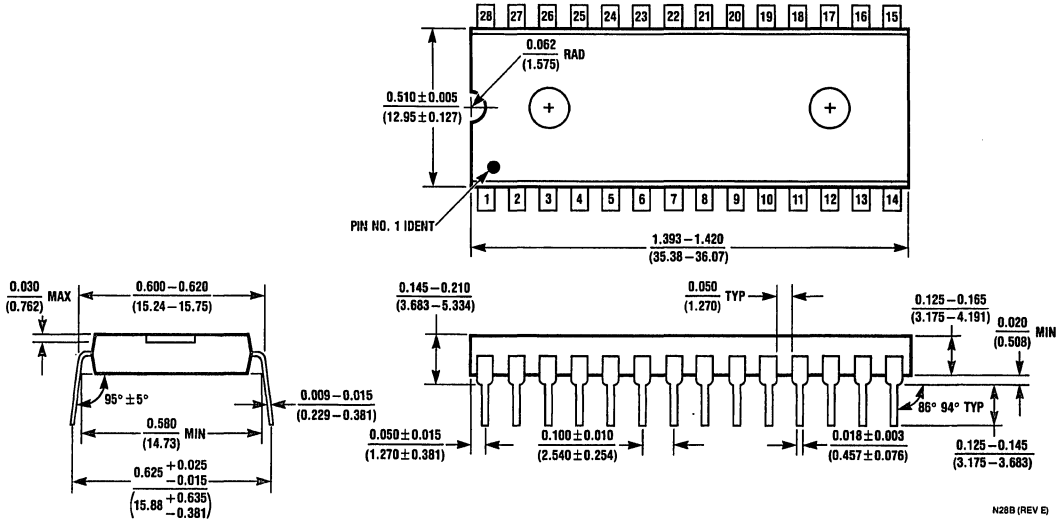
N20A (REV G)

22 Lead Molded Dual-In-Line Package (N)
NS Package Number N22A



N22A (REV D)

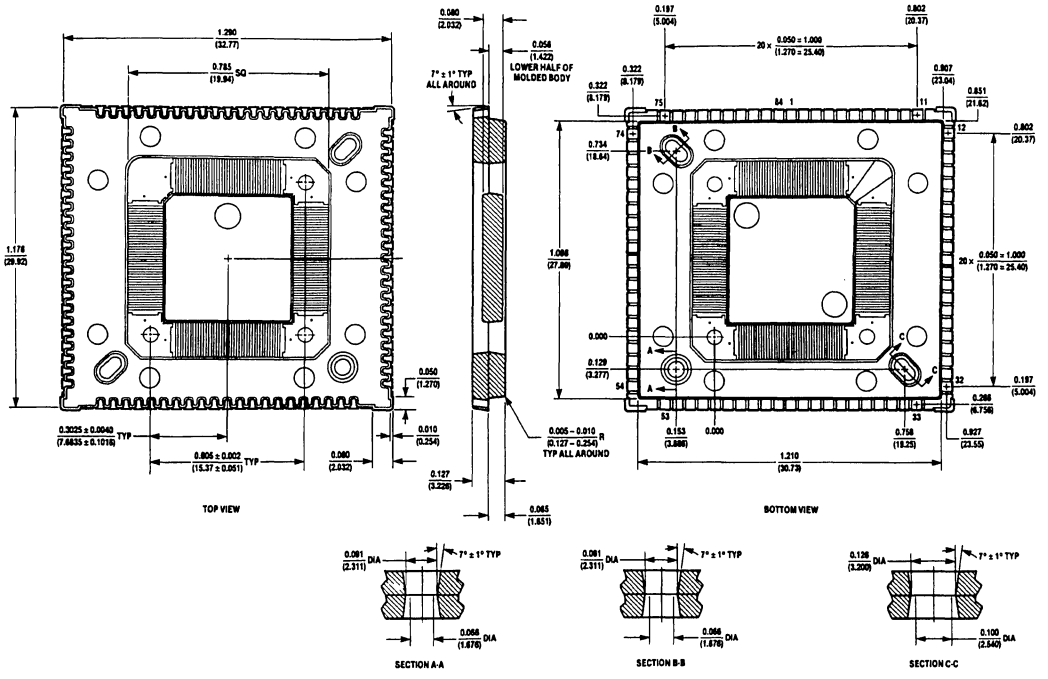
28 Lead Molded Dual-In-Line Package (N)
NS Package Number N28B



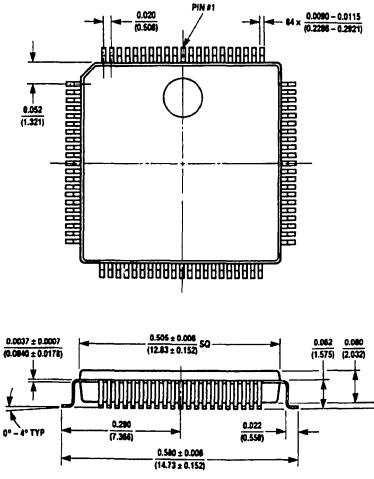
N28B (REV E)

84 Lead TapePak Package (TP)
NS Package Number TP84A

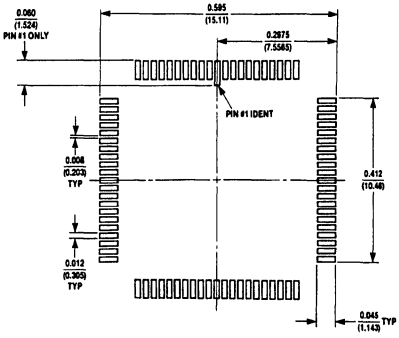
PACKAGE CONFIGURATION AS SHIPPED



RECOMMENDED FORMED AND EXCISED PACKAGE OUTLINE

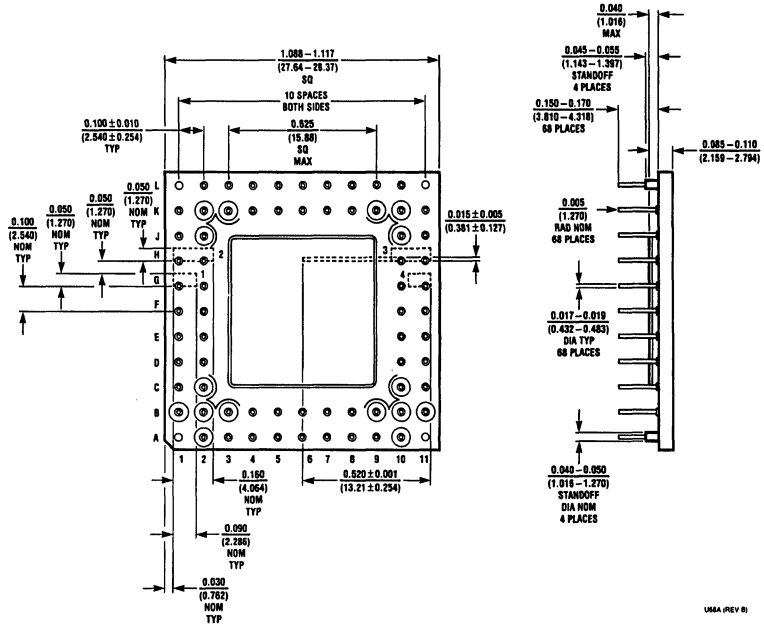


FOOTPRINT TO BE USED



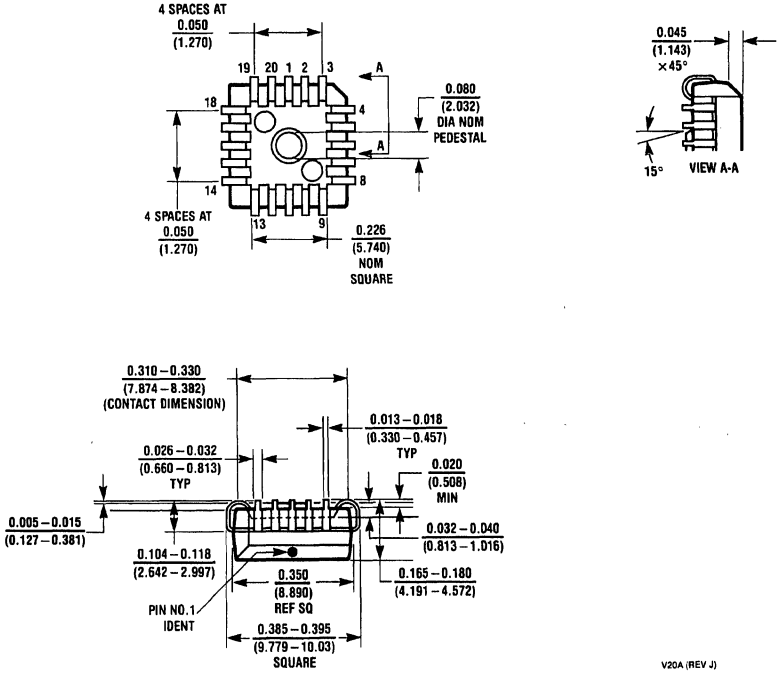
TP84A (REV A)

68 Pin Ceramic Grid Array Package (U)
NS Package Number U68A



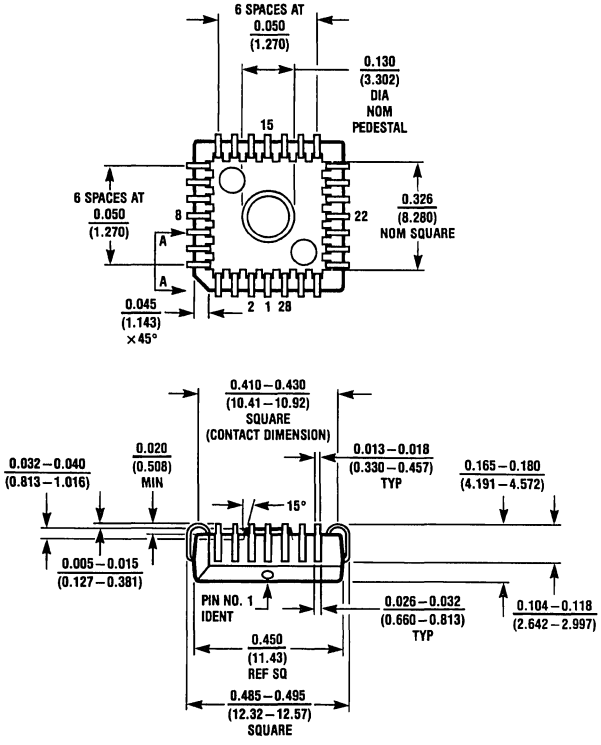
U68A (REV B)

20 Lead Plastic Chip Carrier (V)
NS Package Number V20A



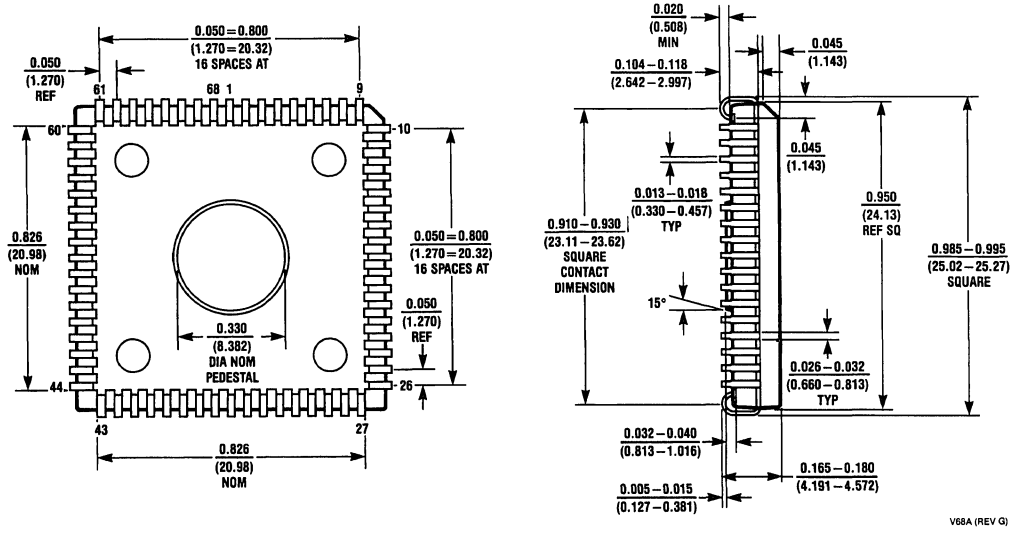
V20A (REV J)

28 Lead Plastic Chip Carrier (V)
NS Package Number V28A



V28A (REV G)

68 Lead Plastic Chip Carrier (V)
NS Package Number V68A



V68A (REV G)

NOTES

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