SESSION I: HIGH-SPEED DATA RECOVERY

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WAM 1.1: A 33Mb/s Data Synchronizing Phase-Locked-Loop Circuit

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THIS PAPER will describe a 127mil x 116mil oxide-isolated bipolar phase-locked loop (PLL) IC which combines analog, ECL and TTL circuitry to achieve serial data synchronization for disk and tape-based mass storage applications over a 250Kb/s to 33 Mb/s NRZ baud rate range.

A voltage-controlled oscillator (VCO), phase-locked to serial data pulses, generates a continuous chain of time windows for pulse capture. To minimize capture errors in jittering data, the window is centered about the mean bit position via a delay of exactly one half of the VCO period placed at the phase comparator input. The delay line and VCO were designed to be nearly identically to obtain precise matching, each employing a ring oscillator and an ECL programmable-modulus counter; Figures 1 and 2. The delay line ring oscillator, with current (and therefore frequency) equal to that of the VCO ring oscillator, is energized by the incoming data pulse and stopped once the counter reaches the half modulus point. The counter then issues an output pulse and is reset. Counter moduli are stepped in factors of two from M = 2 to M = 64 to produce a net 96:1 operating range, while requiring only a 3:1 frequency range of the ring oscillators; Figure 3. Timing accuracy of the delay line has been achieved to within 1ns at 24Mb/s operating rate.

Fine adjustment of the delay line current produces a window displacement effect, stobing. However, delay responds as the inverse of ring oscillator input current, yielding an unwidely control relationship. A method for direct, linear delay modulation via a 5b digital control word, has been used; Figure 3. The input of a current mirror is configured with a binary-weighted current-steering network, so that the control word, M, effectively modulates the net input transistor size. The reflected current fed to the ring oscillator then varies inversely with M, producing direct relationship to M in the time delay. LSB increments of 380ps at a 24Mb/s data rate have been achieved. Capture of single, shifted data bits, where the strobe function has been used to compensate for an inherent window skew in the device (M = –2), is illustrated in Figure 6. The lightly-dashed line represents nominal position of the leading edge of the input bit (window center).

VCO frequency and control voltage runaway are typical vulnerabilities in data synchronizers. Figure 4 shows a frequency-discriminating feedback loop that regulates the VCO control voltage, and thus the operating frequency, preventing unbounded variations. A *reference* PLL, with a VCO ring oscillator identical to that of the primary PLL, is locked to a reference frequency. A comparator block has been included to sense when the primary oscillator current crosses thresholds placed symmetrically above and below the reference current. If either threshold is crossed, the comparator forces a correction at the primary PLL phase comparator, preventing further VCO control voltage excursions.

In an integrated current-or voltage-controlled ring oscillator, the absolute gain

$$F_{out} = K_a \times I_{in} \text{ (or } F_{out} = K_b \times V_{in}) \quad (1)$$

is inherently difficult to specify due to IC process variations. The relationship

$$F_2/F_1 = K_c \times I_2/I_1 \quad (2)$$

holds relatively constant, however, particularly for small frequency variations. Inclusion of an exponential voltage-to-current converter, as shown in the VCO (Figure 2), yields a fixed $\Delta F/F_o$ ratio (F_o = operating frequency) for a given input variation ΔV. For the entire VCO,

$$F_{out} = [K_1]e\,(K_2 V_{in}/V_t), \quad (3)$$

where K_1 includes the current-to-frequency conversion gain of the ring oscillator and K_2 is an input amplification gain constant. The VCO gain is

$$K_{vco} = dF/dV = [K_1 K_2/V_t]e\,(K_2 V_{in}/V_t), \quad (4)$$

Normalized to the operating frequency, this becomes

$$K_{vco}/F_o = [K_1 K_2/V_t]e(K_2 V_{in}/V_t) \div [K_1]e(K_2 V_o/V_t) \approx K_2/V_t, \quad (5)$$

valid for small-signal operation where $V_{in} \approx V_o$. Thus,

$$K_{vco} \approx K_2/V_t \times F_o, \quad (6)$$

yielding VCO gain behavior which is relatively independent of general IC process variations. A typical relationship of K_{vco} = 1.3 x F_o has been achieved.

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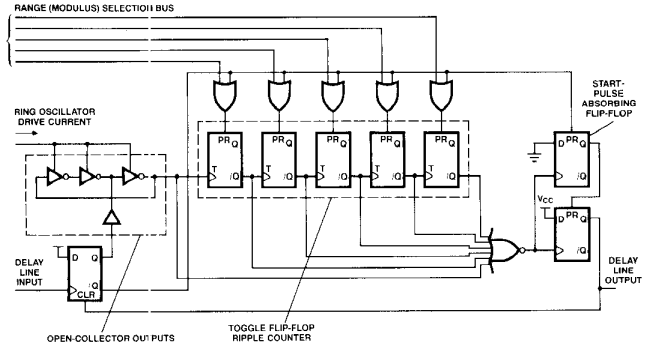


FIGURE 1 -- Delay line based on a ring oscillator and a programmable-modulus counter.

[See pages 276-277 for Figures 5, 6, 7]

FIGURE 2 – Complete voltage-controlled oscillator with 96:1 operating range.

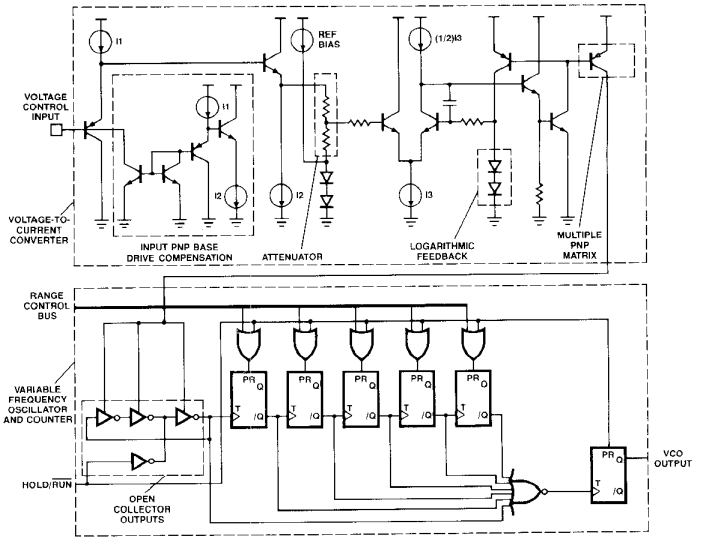
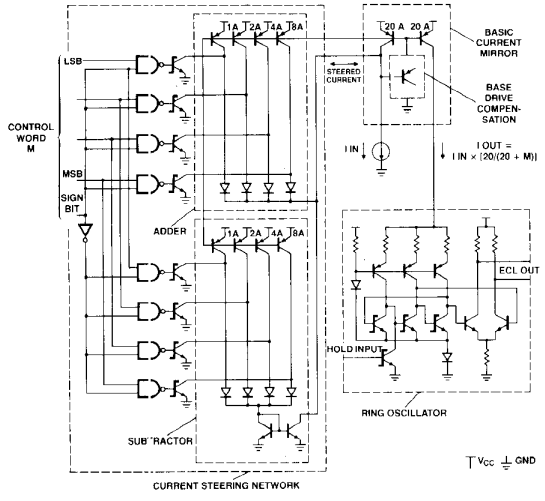


FIGURE 3 -- Current mirroring with reciprocal digital-gain control



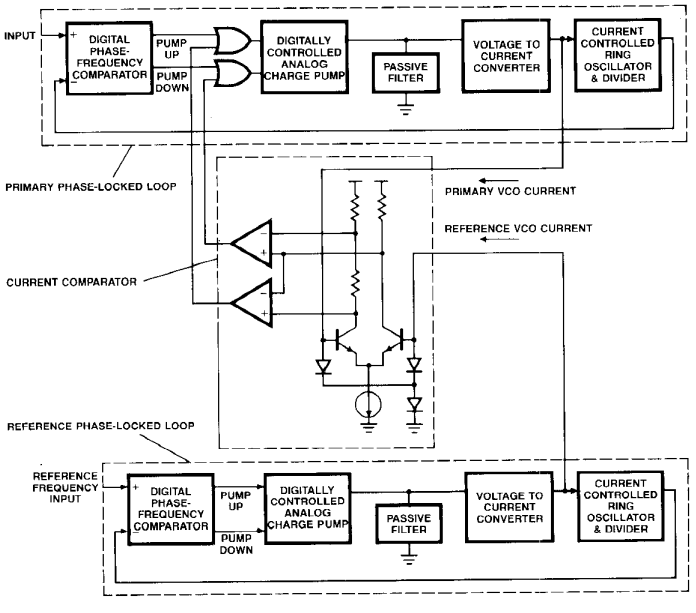


FIGURE 4 – PLL with range-regulated voltage-controlled oscillator.

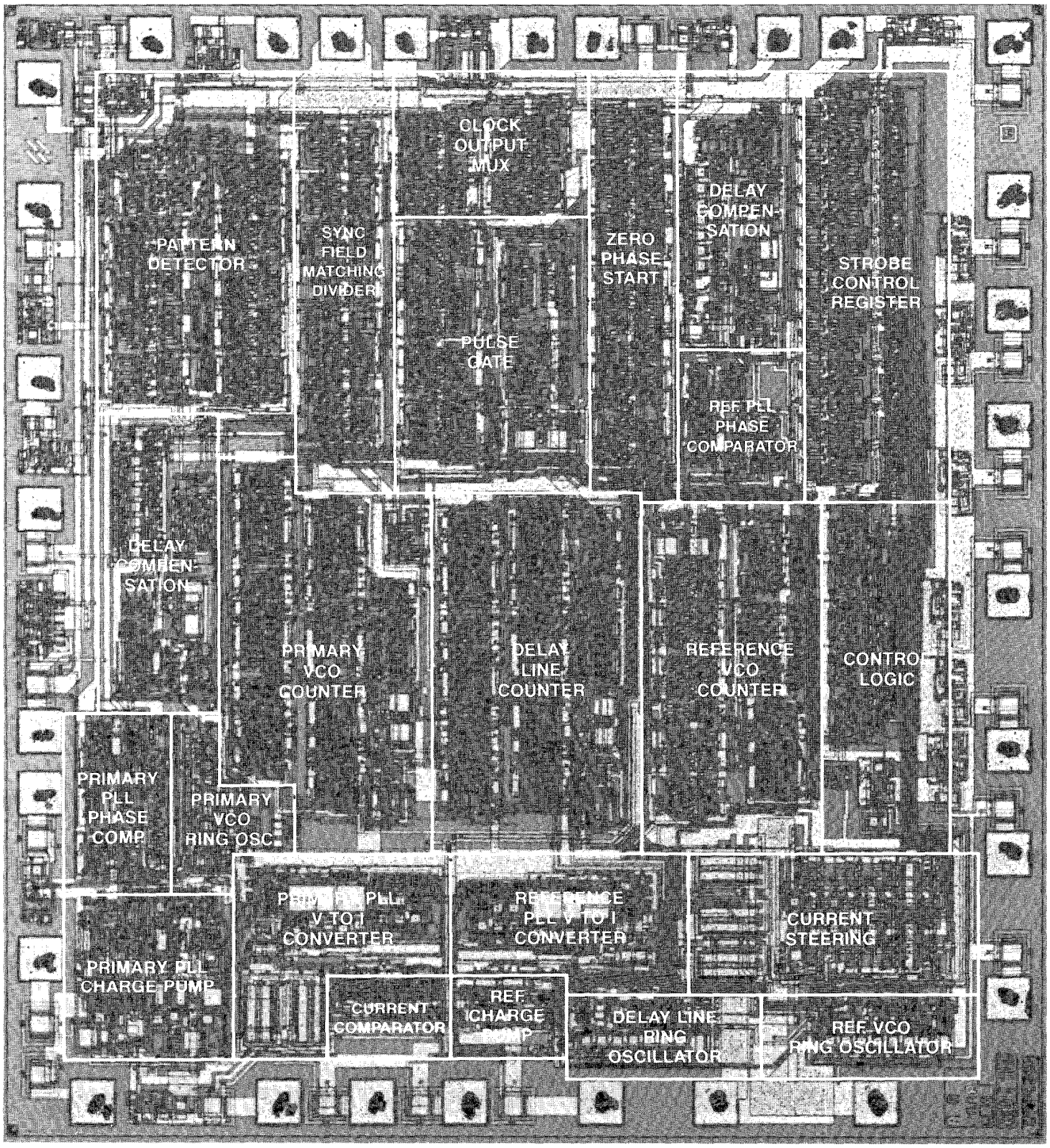


FIGURE 7 – Die photograph of data synchronizer.

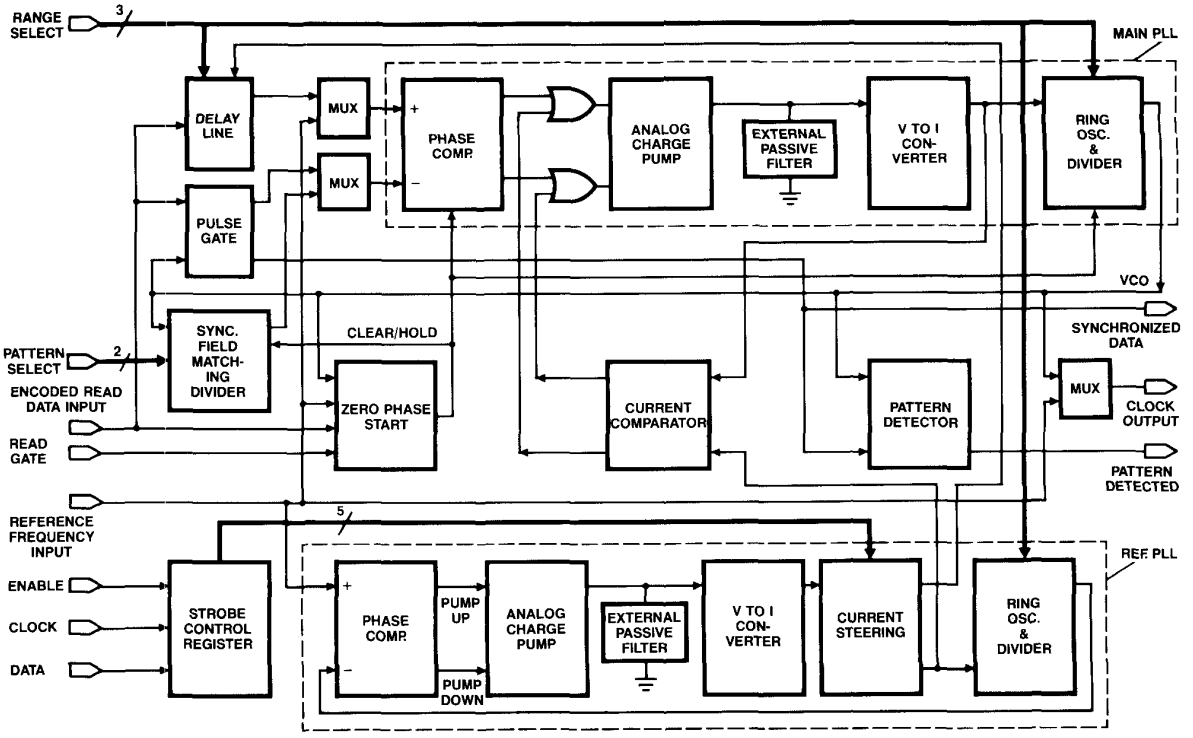


FIGURE 5 – Data synchronizer system diagram.

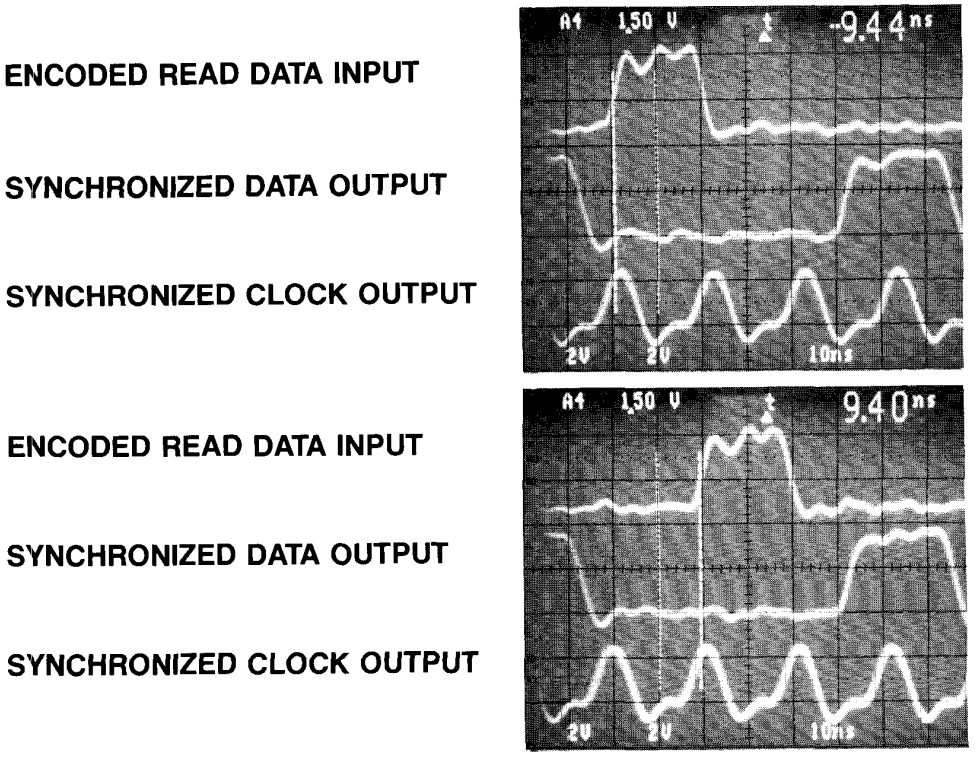


FIGURE 6 – Capture of shifted bits with manually de-skewed window, strobe M = -2: *(a)* early shift, *(b)* late shift.