NCR

MICROELECTRONICS DIVISION

SCSI ENGINEERING NOTEBOOK

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I ALL USERS OF THE NCR 5385 SCSI PROTOCOL CONTROLLER

TO: ALL USER'S OF THE NCR 5385 SCSI PROTOCOL CONTROLLER

Between Revision 9 and Revision 10 of the SCSI draft-proposed standard, the ANSC X3T9.2 subcommittee respecified a few of the SCSI bus timings with regard to a bus phenomenon referred to as the "Wire-OR glitch". This problem was not known to exist, at least to the X3T9.2 subcommittee until the article entitled "Wire-OR Logic on Transmission Lines" appeared in the June 1983 issue of IEEE Micro.

The problem is basically this: If a wire-OR'ed circuit turns off while the others are still driving the line, this signal may glitch to the off state for a period of time approximately equal to twice the associated cable delay. Since cable delays can be as much as 2.0 nsec/ft, a 200 nsec glitch could possible occur on a 50 ft. cable.

Since Busy (BSY) and Reset (RST) are defined to be "wire-OR" signals, they are susceptible to this glitch. In most cases a glitch on RST will not create a problem, however, a glitch on BSY during arbitration or reselection could create a confusing situation on the SCSI bus.

The table below is a comparison of the timing changes. These timings are defined in section 4.7 of the SCSI draft proposed standard.

	Revision 9 Timings	Revision 14A Timings
Arbitration Delay	1.7 usec	2.2 usec
Bus Clear Delay	650 nsec	800 nsec
Bus Free Delay	100 nsec	800 nsec
Bus Set Delay	1.1 usec	1.8 usec
Bus Settle Delay	450 nsec	400 nsec

The NCR 5385 operates to the Revision 9 timings and is being used in many non-arbitrating environments. The NCR 5385 can be made to accommodate the latest timing changes using external circuitry. Design assistance is available.

The NCR 5386 will supercede the NCR 5385 and will reflect the latest ANSI timings. The NCR 5386 is both pin and software compatible with the NCR 5385. The NCR 5385 is being used to prototype arbitrating SCSI designs with the intent of migrating to the NCR 5386 for production.

It is important to note: If you intend for your design to operate in a full arbitrating environment, do not plan to use systems which operate to the old timings. Mixing the "old" timings with the "new" timings may have catastrophic results.

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II DETAILED DIFFERENCES BETWEEN THE NCR 5385 AND THE NCR 5386

DETAILED DIFFERENCES BETWEEN THE NCR 5385 AND THE NCR 5386

The NCR 5386 SCSI Protocol Controller is a superset of the NCR 5385 design. It is pin and software compatible with the NCR 5385. The primary differences are the hardware timings that were altered between Revision 9 and Revision 10 of the ANSI draft-proposed standard. The following paragraphs detail the differences between the NCR 5385 and the NCR 5386.

ITEM #1

If the NCR 5385 is issued a Disconnect command after an interrupt occurs, the INT signal (pin 19) does not reset.

The NCR 5386 will be modified so that the INT signal (pin 19) will be reset when a Disconnect command is issued.

ITEM #2

The NCR 5385 may spuriously generate an invalid parity error status during an Initiator output or a Target send operation.

The NCR 5386 will be modified to hold the parity error status reset during Initiator output or Target send operations.

ITEM #3

If a controller designed with the NCR 5385 wishes to halt a Target send operation in order to change to a new bus phase, he must issue the Pause command. Currently the Pause command requires that one or two bytes of data be sent to the chip before a new command can be issued.

The Target send state machine will be modified in the NCR 5386 so that a new command may be issued immediately after the Pause command. The extraneous data bytes will not be required.

ITEM #4

If transferring data as a Target device and the NCR 5385 detects an active ATN signal (pin 5), a Bus Service interrupt will immediately be generated.

Firmware designers have suggested that this interrupt is easier to service if the interrupt is delayed until the end of the current transfer. Therefore, the NCR 5386 will be modified so that the notification of ATN will occur during the normal Function Complete interrupts, at the end of the transfer.

ITEM #5

If the ACK signal (pin 10) is active, floating or not being received as a low level (0) input during power-up, the NCR 5385 will fail self-diagnostics. This precludes the ability to power-up the NCR 5385 on a bus that is actively transferring data.

The NCR 5386 will be able to power-up on an active SCSI bus by blocking the ACK signal while performing internal self-diagnostics.

ITEM #6

The NCR 5385 latches the value of the phase lines (MSG, C/D, & I/O) into the Auxiliary Status Register on either INT (pin 19) or RD/ (pin 31) being active. If the RD/ (pin 31) pulse is greater than six clock periods in length, the possibility exists that a Bus Service interrupt may reflect the wrong phase line values.

The NCR 5386 design will latch the phase lines into the Auxiliary Status Register only when INT (pin 19) is active.

ITEM #7

If operating the NCR 5385 in the Target receive mode and an exit condition occurs (Pause command or parity error), the Transfer Counter will be decremented one count too many before exiting the state machine.

The NCR 5386 design will add an additional term to the Target receive state machine to prevent the Transfer Counter from decrementing before leaving the state machine.

ITEM #8

The NCR 5385 has doubly buffered data register. Since there is only one data register full flag, there is no way to determine if the chip contains one or two bytes of data.

The NCR 5386 will use bit 0 of the Auxiliary Status Register as a flag for indicating the Data Register II is full. This register may be read by activating CS/ (pin 21) with A3-A0=1000 (pins 26, 25, 23 & 22) and then pulsing the RD/ signal (pin 31). (Please refer to the MPU read timings on page 34 of the NCR 5385 SCSI Protocol Controller Data Sheet.)

ITEM #9

When the NCR 5385 is transferring data in the DMA mode, DREQ (pin 29) will go active one extra time after the Transfer Counter reaches zero. No data is transferred for this unwanted data request.

The NCR 5386 will be modified so that the extra DREQ (pin 29) will be suppressed.

ITEM #10

The NCR 5385 was designed to early revisions of the ANSI SCSI draft-proposed document. Between Revision 9 and Revision 10 of the specification, six protocol timing changes were made to accommodate a bus phenomenon referred to as a "Wired-or-Glitch".

Revision 14 is the document being forwarded out of the ANSI sub-committee and will be the document that the industry will use for system designs. The NCR 5386 will reflect the latest timings documented in Revision 14 of the draft-proposed standard. A summary of the timing differences are listed in the table below.

	Revision 9 Timings	Revision 10-14 Timings
Arbitration Delay	1.7 usec	2.2 usec
Bus Clear Delay	650 nsec	800 nsec
Bus Free Delay	100 nsec	800 nsec
Bus Set Delay	1.1 usec	1.8 usec
Bus Settle Delay	450 nsec	400 nsec

ITEM #11

The NCR 5385 generates and optionally checks for parity on the SCSI bus. Many customers would like to have the parity bit available on the memory/MPU bus.

The NCR 5386 will optionally support parity through the chip by using ID0 (pin 14) as the data parity through signal. To accomplish this, the ID Register (A3-A0=0101) will become a read/write register. If this register is not written the NCR 5386 will assume the mode of the NCR 5385 and use the signals ID0-ID2 (pins 14-12) to determine the device ID. If bit 7 of this register is written with a one (1) the chip will check and pass parity in both directions. ID0 (pin 14) will now be used to pass parity to and from the memory/MPU bus. ID1 and ID2 will not be used. If this bit is not on (1), parity operation will be identical to the NCR 5385.

ITEM #12

If the NCR 5385 is performing a Target send operation and ACK (pin 10) does not drop within 500 nsec after the next to last request (REQ, pin 11), the Function Complete interrupt will precede the transfer of the last data byte. A bus hang condition will occur if a new command is written to the NCR 5385 before the last data transfer takes place.

The NCR 5386 will be modified so that the Function Complete interrupt can not occur until after the last byte of data has been transferred.

ITEM #13

If a hardware reset is issued to the NCR 5385 while the internal ROM sequencer is addressing certain locations, the chip will "hang-up" when RST (pin 4) goes inactive.

The NCR 5386 will be modified so that the chip is properly reset whenever a hardware reset occurs. (RST, pin 4 active for a minimum period of 100 nsec.)

ITEM #14

Several low-end controllers do not monitor BSY during the selection process. Additionally, they do not check to see if more than two ID's are valid on the bus during selection. Both conditions are requirements of the proposed ANSI specification. The NCR 5385 while moving from Arbitration into Selection, asserts SBEN/ (pin 20) while the data bus is tri-stated. This causes all the data signals on the SCSI bus to go active for approximately three clock cycles. During this time both BSYOUT (pin 42) and SELOUT (pin 32) are active. Since low-end controllers, such as the Xebec S-1410, do not monitor BSY but detect SEL and their ID active, they become falsely selected.

The NCR 5386 will be modified so that Xebec S1410 type controllers may be selected without using external hardware to prevent the false selection.

ITEM #15

Some low-end SCSI controllers will change bus phases while the NCR 5385, connected as an Initiator, is still asserting ACK (pin 10). The proposed ANSI specification states the phase lines should never change while REQ or ACK are active. If this occurs while the Target is sequencing from the Status to the Message In phase, the NCR 5385 is tricked into thinking that the last status byte transferred was the Message In byte and leaves ACK (pin 10) active so that the message may be rejected.

The NCR 5386 will be modified so that changes on the phase lines will be ignored after the data has been received. (Data is received on the rising edge of ACK (pin 10).)

ITEM #16

The NCR 5386 will provide Bus Service interrupts for phase changes that occur irregardless of the condition of REQ.

Many controllers allow the phase lines to spuriously changebetween valid bus phases. Because of this, the NCR 5386 will be modified so that spurious phase changes will not create unwanted interrupts. Bit 3 of the Control Register, when set to a one (1), will cause Bus Service interrupts to occur only if REQ (pin 11) is valid. If bit 3 of the Control Register is a zero (0), operation will be identical to the NCR 5385.

ITEM #17

If the NCR 5385 is connected as an Initiator and REQ (pin 11) does not go inactive within approximately 10 usec (@ 10 mhz) after ACK (pin 10) has been asserted, the chip believes that an additional REQ has occurred. This condition may cause the bus to hang. Fortunately, only the ADES Python streaming tape controller is known to exhibit this problem.

The NCR 5386 will be modified so that slow handshaking devices will be accommodated.

ITEM #18

If performing DMA reads and writes to the NCR 5385, DACK/ (pin 27) must go inactive within 1.5 clock periods of RD/ (pin 31) or WR/ (pin 30) going inactive.

The NCR 5386 will not impose a maximum time for de-asserting DACK/ after RD/ (pin 31) or WR/ (pin 30) goes inactive.

ITEM #19

The NCR 5385 provides asynchronous handshaking capability to 1.5 Mbytes/sec.

A version of the NCR 5386, the NCR 5386 S, will provide synchronous handshaking (offset of 1) to 3.0 Mbytes/sec.

THE NCR 5385E

The NCR 5385E is an enhanced version of the NCR 5385. It was designed as a 'stop gap' for users desiring the functional differences of the NCR 5386. This chip operates to the latest ANSI timings (Rev. 14a) and corrects many of the anomalies found in the NCR 5385.

Items 1, 2, 4, 5, 6, 10, 13, 14, 17 and 18 of this document are included in the NCR 5385E design.

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III USING THE NCR 5385

USING THE NCR 5385

Several companies are designing systems based on the NCR 5385/5386. Many are encountering the same difficulties during the integration/debugging design phase. Some of these problems have been created by formatters that do not comply to the proposed ANSI specification, and others are anomalies of the NCR 5385 that will be corrected in the NCR 5386 design. Please use the following notes to assist in the debugging process.

SYMPTOM #1

After power-up, the Diagnostic Status Register contains an '86H'.

PROBABLE CAUSE/SOLUTION:

When the NCR 5385 is powered-on, it automatically performs an internal self-test diagnostic. A portion of this test passes a byte of date through all the internal data registers. If ACK (pin 10) is floating or not being received a low-level input, data from the signals SB0-SB7 will be clocked into the input data register and the data compare test will fail.

In host adapter designs that do not implement the Target role, ACK (pin 10) should at least be pulled down if there is no receiver dedicated to this signal.

This condition implies that an SCSI bus device using the NCR 5385 cannot be powered-up on an SCSI bus that is actively transferring data, unless ACK (pin 10) is externally blocked. The NCR 5386 will block ACK (pin 10) during power-up diagnostics.

SYMPTOM #2

While connected as an Initiator, a Bus Service interrupt occurs for phase changes that do not require data transfers.

PROBABLE CAUSE/SOLUTION:

The NCR 5385 will interrupt for phase changes regardless of the condition of REQ (pin 11). When a phase change is detected by the chip, the phase lines (MSG, C/D, & I/O) are monitored for twelve clock periods. If the phase lines have

indeed changed, the chip monitors the BSYIN (pin 17) signal for an additional twelve clock periods to determine if the chip is still connected. If so, a Bus Service interrupt occurs indicating a phase change. The user must respond to this phase change by reading the Auxiliary Status Register, reading the Interrupt Register, and issuing a Transfer Info or a Transfer Pad command.

EXAMPLE: A Test Unit Ready command has been issued to a Target device. After completing the Command phase the Target switches to the Data Out phase since this is the normal bus sequencing. Because these is no data phase associated with the Test Unit Ready command the Target will now proceed to the Status phase.

The 5385 will interrupt after the change to the Data Out phase. This interrupt should be serviced by reading the Auxiliary Status Register, reading the Interrupt register and re-issuing the Transfer Info command. Unless this is performed the Bus Service interrupt for the Status phase will not occur.

The Adaptec disk controller boards, after sending the Command Complete message for the Message In phase may change phases twice before lowering BSYIN (pin 17) and disconnecting. Here again, these interrupts must be serviced in order to see the Disconnect interrupt.

The NCR 5386 will have the option of operating as the NCR 5385 or interrupting for phase changes only if REQ (pin 11) is active.

SYMPTOM #3

While connected as an Initiator, the phase lines change but no interrupt occurs.

PROBABLE CAUSE/SOLUTION:

In order for the NCR 5385 to generate an interrupt, the previous interrupt must be properly serviced. Please refer to SYMPTOM #2.

SYMPTOM #4

A Target device becomes illegally selected.

PROBABLE CAUSE/SOLUTION:

Many low-end controllers do not obey the proposed ANSI standard for becoming selected. Many do not monitor the BSY signal on the SCSI bus and most do not check to see if more than two device ID"s are active during Selection. Some controllers violate both rules for selection.

The NCR 5385 while moving from the Arbitration phase to the Selection phase will tri-state the data lines SB0-SB7 and assert SBEN/ (pin 20) while SELOUT (pin 32) and BSYOUT (pin 42) are still active. The tri-stated data lines appear as high level inputs to the bus transceivers and all data lines will be active for three clock periods. The NCR 5385 will then drive the data lines to the proper state and lower BSYOUT (pin 42) to enter the Selection phase.

Controllers that do not monitor BSY and that do not check to see if more than two device ID's are active during selection, may become selected before the NCR 5385 releases the BSYOUT (pin 42) signal. Similarly, if an attempted selection has failed, a Target may become selected while the NCR 5385 is sequencing signals to remove itself from the bus. This is a characteristic of the Xebec S-1410 and some of the S-1410 'like' controllers.

In order to accommodate these controllers, SBEN/ (pin 20) should be delayed three clock cycles to prevent the data bus from going active until the Selection phase has been entered. The NCR 5386 will allow for these devices to reside on the SCSI bus without requiring additional hardware.

SYMPTOM #5

While connected as an Initiator, ACK (pin 10) remains active on the SCSI bus.

PROBABLE CAUSE/SOLUTION:

Some controllers when finished with the Status phase, move to the Message In phase without monitoring the condition of the ACK signal. If ACK (pin 10) is still active when the phase lines change to the Message In phase, the NCR 5385 thinks that the Status byte that was transferred was the Message In byte and leaves ACK (pin 17) active so that the Message may be rejected.

A Message Accepted command may be issued to release ACK (pin 17) so that the 'real' Message In byte may be transferred. After receiving what would normally be the Command Complete message, another Message Accepted command should be issued. The NCR 5386 will tolerate phase line changes after ACK (pin 17) has gone active.

This is also a characteristic of the Xebec S-1410 controller.

SYMPTOM #6

While connected as an Initiator, two Bus Service interrupts for the same bus phase occurs.

PROBABLE CAUSE/SOLUTION:

First, the NCR 5385 will generate a Bus Service interrupt if REQ (pin 11) goes active when the Transfer Counter is zero. This is used to indicate a counter overflow condition and is normal operation for the part.

This symptom may also occur if the NCR 5385 is connected to a very slow handshaking Target device. When operating the NCR 5385 at 5 Mhz, if the Target does not respond to the assertion of ACK (pin 17) by de-asserting REQ (pin 11)within approximately 20 usec the NCR 5385 believes another request (REQ) has occurred. (This time is approximately 10usec when operating the part at 10 Mhz.) If this occurs, the chip will become 'hung' and will have to be reset.

EXAMPLE: While using an ADSI Python streaming tape controller, the controller changes to the Status phase. The NCR 5385 generates a Bus Service interrupts upon entering the Status phase, received the Status byte and on occasion will generate another Bus Service interrupt. (Sometimes the Python controller de-asserts REQ quickly enough so as not to generate the second interrupt.) This is the only controller (that I'm aware of) that exhibits this symptom.

The NCR 5386 will accommodate slow handshaking devices.

SYMPTOM #7

The NCR 5385 'hangs' during data transfers.

PROBABLE CAUSE/SOLUTION:

Two conditions may cause the NCR 5385 to 'hang' during data transfers. The first condition is described in SYMPTOM #6 where REQ (pin 11) is de-asserted later than 10 usec after ACK (pin 17) is asserted. The second condition occurs if DACK/ stays active longer than 1.5 clock periods after RD/ or WR/ goes inactive during DMA transfers. This time is the parameters tRDC (max) and tWDC (max) on page 35 of the NCR 5385 SCSI Protocol Controller Data Sheet, document no. MC-704.

To correct this problem your DMA interface may be designed so that DACK/ goes inactive along with the RD/ and WR/ strobes. The NCR 5386 will correct this problem.

SYMPTOM #8

The NCR 5385 'hangs' after being issued a hardware Reset.

PROBABLE CAUSE/SOLUTION:

The NCR 5385 is sensitive to the hardware Reset condition when operating in certain modes. To be sure that the chip has been properly reset, issue a Reset command to the chip, wait at least 260 clock cycles and read the Diagnostic Status Register. The NCR 5385 should now be reset. If this register does not contain an '80H' re-issue the Reset command and repeat the above sequence. This will insure that the chip has been reset properly. The NCR 5386 will not exhibit this problem.

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IV INTERFACING THE NCR 5385 SCSI PROTOCOL CONTROLLER TO THE XEBEC S1419 WINCHESTER DISK CONTROLLER

INTERFACING THE NCR 5385 SCSI PROTOCOL CONTROLLER TO THE XEBEC S1410 WINCHESTER DISK CONTROLLER

The Xebec S1410 Winchester disk controller is non-compliant with the SCSI draft proposed standard in two areas involving the hardware level interface. (This note will not discuss the software non-compliant issues.)

The first violation involves the selection phase. Section 4.4.3, Rev. 10 of the SCSI draft proposed standard describes the selection phase for both arbitrating and non-arbitrating systems. The second paragraph on page 16 reads; "In all systems, the Target shall determine that it is selected when both of SEL and its bus device ID are true and both BSY and I/O are false for at least a Bus Settle Delay."

The Xebec S1410 controller does not monitor BSY and therefore may be falsely selected.

If the NCR 5385 device, connected as an Initiator, attempts to select the Xebec controller, the following will occur:

The NCR 5385 tri-states the SCSI data Bus (SB0-SB7,SBP) prior to selection. Since SBEN/ is inactive the external bus transceivers will be receiving the data bus. In order to prevent contention at the NCR 5385/transceiver interface, the data bus remains tri-stated while SBEN/ goes active. Three clock cycles after SBEN/ goes active its bus device ID and the Target's ID will be asserted on the data bus. BSYOUT which has been active throughout this period and will be released a minimum of 100 nsec after the ID bits are asserted. (Please refer to page 37 and 38 of the NCR 5385 SCSI Protocol Controller Data Sheet for a detailed description of the Initiator Selection Timings.)

Since the data bus was tri-stated when SBEN/ went active, this floating state appears as a high-level input and the inverting transceiver will drive the SCSI data bus to the active state until the 5385 asserts the data bus (approximately three clock cycles later). Because the Xebec controller does not monitor BSY and since SEL and all the data lines are active, the Xebec controller will always be selected regardless of its bus device ID.

Many transceivers have independent driver/receiver enables. To avoid this false selection, SBEN/ may be used to disable the bus receivers and SBEN/ delayed three clock periods (SBEN.D/) may be used to enable the bus drivers.

The second area where a possible violation can occur is during phase changes. Section 4.4.5, Rev. 10 of the SCSI draft proposed standard describes the Information Transfer Phases. Paragraph one on page 19 reads: "Additionally, during each information transfer phase, the Target shall continuously envelope the REQ/ACK handshake(s) with C/D, I/O, and MSG signals in such a manner that these control signals are valid for a Bus Settle Delay before the REQ of the first handshake and remain valid until the deassertion of ACK at the end of the last handshake.

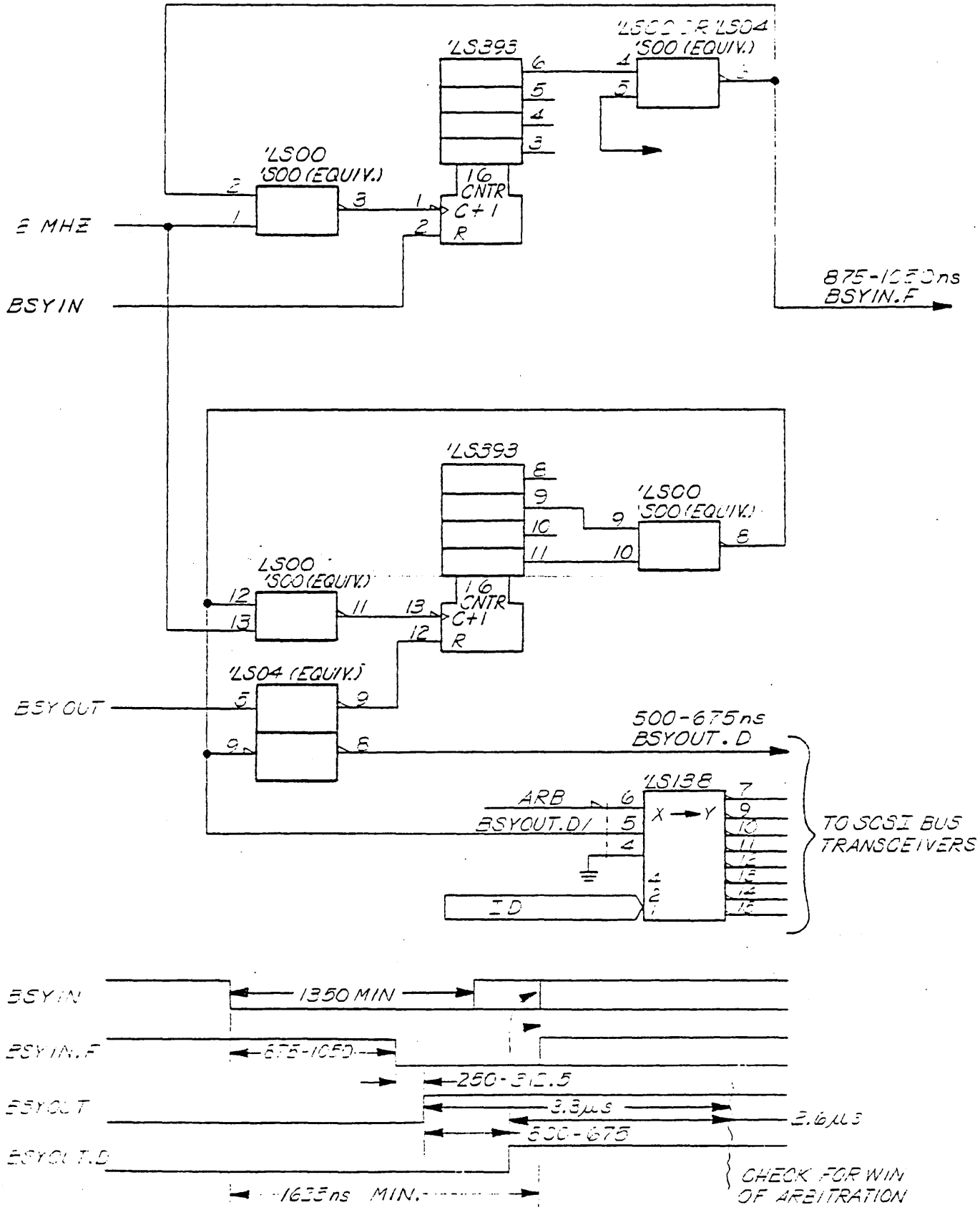
The Xebec C1410 Winchester disk controller may change phases before ACK goes inactive. It is known that the Xebec controller will change from the Status phase to the Message In phase before ACK goes inactive. This phase change generates an interrupt to the processor and ACK is left active on the bus, thus preventing a data transfer for the Message In phase. In order to continue normally a Message Accepted command must be sent to the NCR 5385 after receipt of the interrupt for the Message In phase so that the ACK signal may be released.

One needs to be aware of these exceptions when designing drivers for the NCR 5385 that are intended to operate with the Xebec S1410 controller.

V MODIFYING THE NCR 5385 TO THE POST REVISION 10 TIMINGS

1. 8 MHZ
2. 10 MHZ

MODIFYING THE NCR 5385
TO THE POST REVISION 10 TIMINGS
8 MHz



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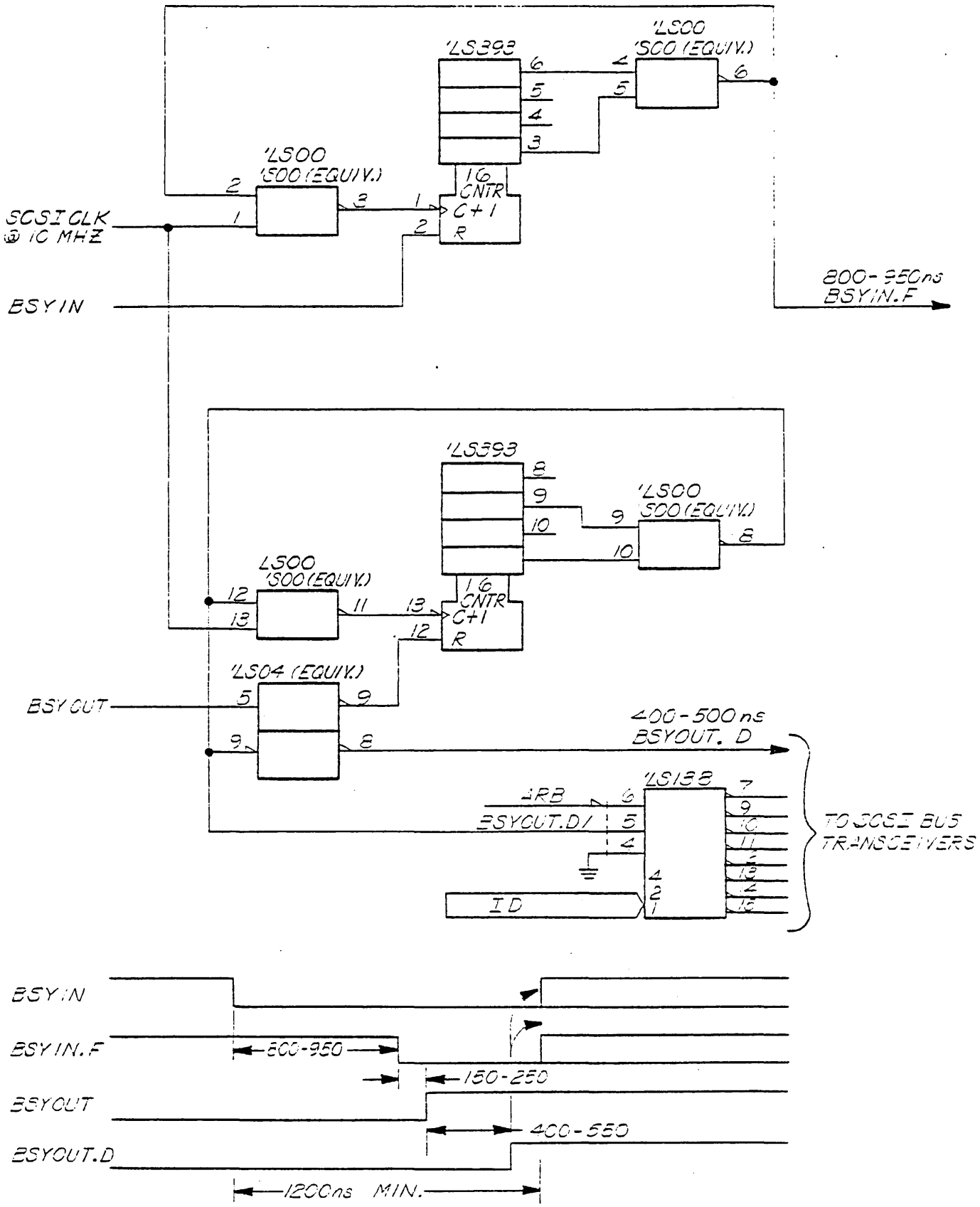
MODIFYING THE NCR 5385
TO THE POST REVISION 10 TIMINGS
10 MHz

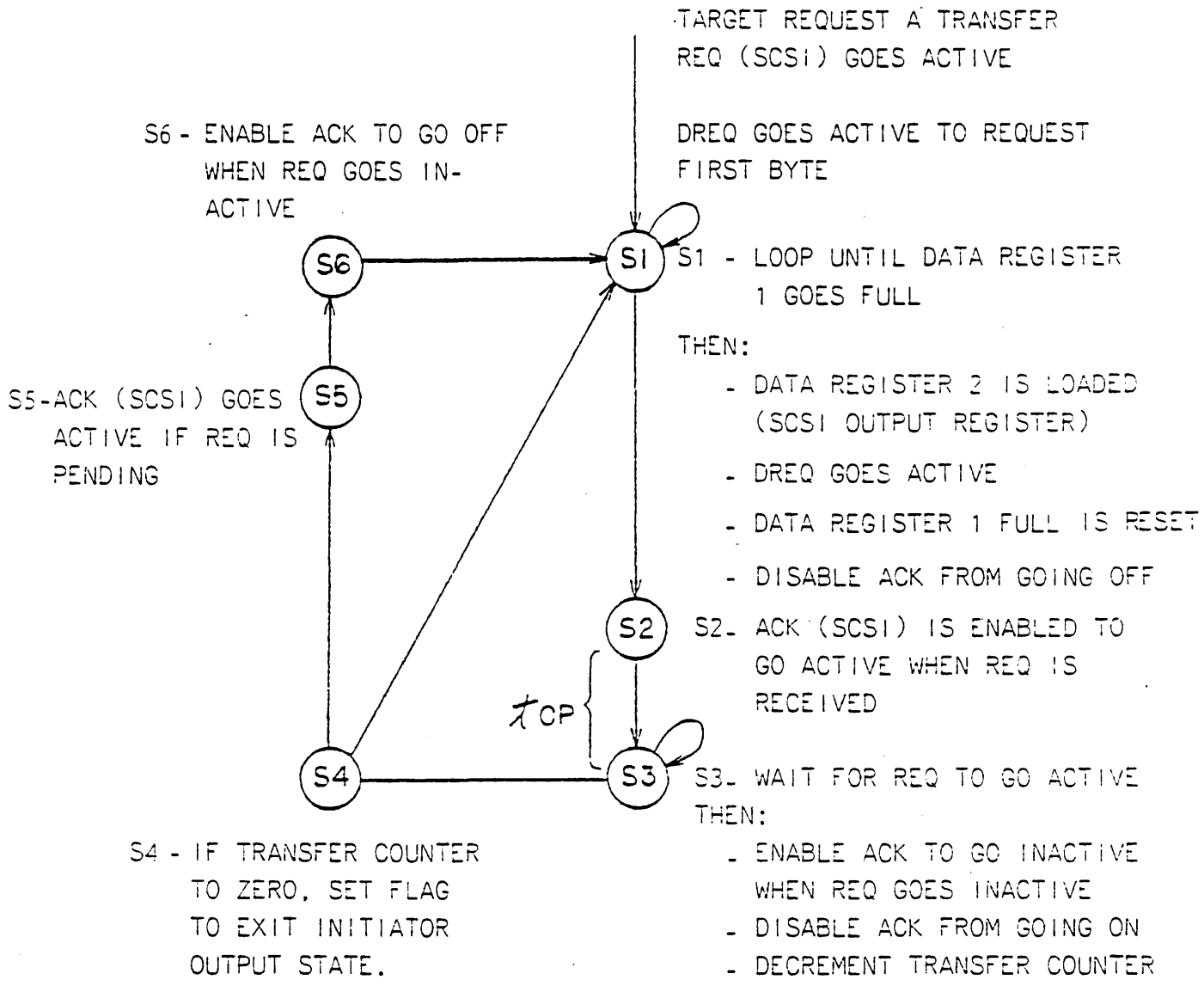


VI NCR 5385 STATE MACHINE OPERATION

1. INITIATOR OUTPUT STATE MACHINE
2. TARGET RECEIVE STATE MACHINE
3. INITIATOR INPUT STATE MACHINE
4. TARGET SEND STATE MACHINE

NCR 5385 STATE MACHINE OPERATION

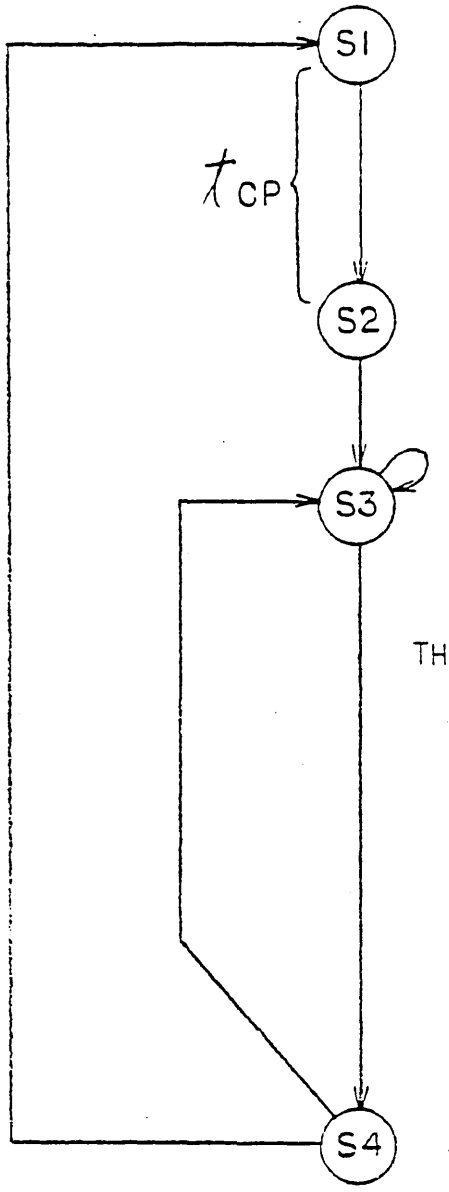
INITIATOR OUTPUT STATE MACHINE



tCP = CLOCK PERIOD

100 NS $\leq$ tCP $\leq$ 200 NS

TARGET RECEIVE STATE MACHINE



S1 - DECREMENT TRANSFER COUNTER
- ENABLE REQ (SCSI) TO GO ACTIVE WHEN ACK GOES INACTIVE

S2 - DELAY ONE CLOCK PERIOD (tCP)

S3 - WAIT FOR DATA REGISTER 3 TO GO FULL & FOR DATA REGISTER 1 TO GO EMPTY*

THEN:

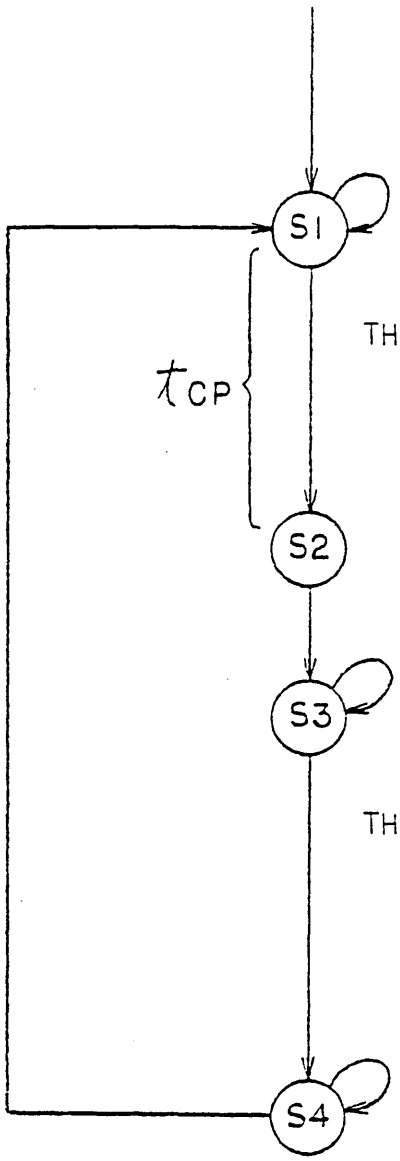
- ENABLE REQ TO GO ACTIVE WHEN ACK GOES INACTIVE
- LOAD DATA REGISTER 3 INTO DATA REGISTER 1
- SET DREQ
- SET DATA REGISTER 1 FULL FLAG

S4 - DECREMENT TRANSFER COUNTER (NOTE: THE TRANSFER IS DECREMENTED BEFOR THE BYTE IS TRANSFERRED TO KEEP THE THROUGHPUT UP.)
- IF TRANSFER COUNTER GOES TO ZERO, SET FLAG TO EXIT TARGET RECEIVE.

tCP = CLOCK PERIOD
100 NS $\leq$ tCP $\leq$ 200 NS

* DATA REGISTER 3 IS LOADED WHEN ACK GOES ACTIVE.

INITIATOR INPUT STATE MACHINE



TARGET REQUESTS A TRANSFER (REQ (SCSI) GOES ACTIVE)

ACK GOES ACTIVE AND SCSI INPUT DATA REGISTER IS LOADED, (DATA REGISTER 3)*

S1- WAIT FOR REQ TO GO ACTIVE (FROM STATE S4)

THEN:

- TRANSFER COUNTER IS DECREMENTED
- ACK IS DISABLED FROM GOING ACTIVE

S2 - ENABLE ACK TO GO. INACTIVE WHEN REQ GOES INACTIVE

S3 - WAIT FOR DATA REGISTER 1 TO GO EMPTY

THEN:

- LOAD DATA REGISTER 1 FROM DATA REGISTER 3
- SET DREQ
- SET DATA REGISTER 1 FULL FLAG

S4 - WAIT FOR ACK TO GO INACTIVE

THEN:

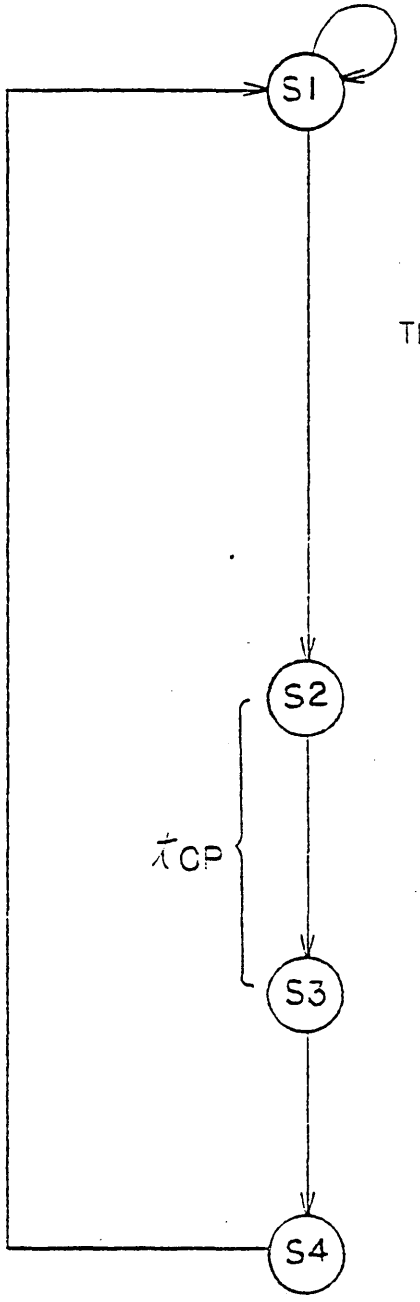
- ENABLE ACK TO GO ACTIVE WHEN REQ GOES ACTIVE
- DISABLE ACK FROM GOING OFF
- IF TRANSFER COUNTER GOES TO ZERO, SET FLAG TO EXIT INITIATOR INPUT STATE

TCP = CLOCK PERIOD

100 NS $\leq$ TCP $\leq$ 200 NS

* DATA REGISTER 3 IS LOADED WHEN ACK GOES ACTIVE

TARGET SEND STATE MACHINE



S1 - WAIT FOR DATA REGISTER 1 TO GO FULL AND FOR THE PREVIOUS BYTE OF DATA TO BE TRANSFERRED (REQ GOES INACTIVE)

THEN:

- DATA REGISTER 2 IS LOADED
- DREQ GOES ACTIVE
- DATA REGISTER 1 FULL IS RESET

S2 - ENABLE REQ TO GO ACTIVE WHEN ACK GOES INACTIVE

S3 - DECREMENT TRANSFER COUNTER

S4 - IF TRANSFER COUNTER EQUAL ZERO, SET FLAG TO EXIT TARGET SEND STATE

TCP = CLOCK PERIOD

100 NS $\leq$ TCP $\leq$ 200 NS

VII SINGLE-CHIP SCSI CONTROLLER CONTAINS HIGH-CURRENT BUS DRIVERS (NCR 5380)

SINGLE-CHIP SCSI CONTROLLER CONTAINS HIGH-CURRENT BUS DRIVERS

NCR Microelectronics, the makers of the first single-chip SCSI Protocol Controller, the NCR 5385, is announcing the newest member of its SCSI product family, the NCR 5380. The NCR 5380 is designed to provide a low-cost SCSI interface solution. The 40-pin NMOS device includes the high-current bus drivers which allows for direct connection to the SCSI bus. It fully supports the latest ANSC X3T9.2 draft-proposed specification, yet is versatile enough to be used with older SCSI designs.

The chip contains high-current bus transceivers capable of sinking 48 ma at 0.5 V. The addition of the high-current bus transceivers significantly reduces the amount of logic required for SCSI bus interconnection. External logic is also reduced because the NCR 5380 is capable of driving the MPU bus directly and no external clock circuitry is required.

The chip is easy to use because of its simple architecture. Any SCSI bus signal may be readily controlled with an MPU write or the signal may be sampled with the appropriate MPU read. Providing direct control over all SCSI bus signals allows the user to implement portions or all of the SCSI protocol in software.

Parity is always generated by the NCR 5380 and is optionally checked on the SCSI bus. When a parity error is detected, the controlling MPU is interrupted.

DMA transfers are supported to 1.5 Mbytes/sec. DMA operations are initiated by writing to one of three on-chip registers. The first register starts any DMA send operation. The next two registers, when written, begin the Target receive and Initiator receive operations, respectively. The system MPU is interrupted for phase changes that occur during DMA transfers or when the external DMA device signals the NCR 5380 that it has completed the specified data transfer.

The NCR 5380 supports arbitration, including reselection and can operate in both the Initiator and Target roles. Thus, it can be used in multi-user/multi-tasking environments and can occupy any node on the SCSI bus. The NCR 5380 generates interrupts whenever it becomes selected or reselected.

Prototype quantities will be available in October, at a cost of $31.00 per device. Production will start in January of 1985.

VIII DIFFERENCES BETWEEN THE NCR 5385/86 AND THE 5380

DIFFERENCES BETWEEN THE NCR 5385/86 AND THE NCR 5380

	5385/86	5380
O.C. Bus Xceivers	External	On-chip
Data Buffering	Double	Single
Xfer Counter	24 Bit	None
Protocol Handling	Auto	Firmware
Max. Xfer Rate	2.5 Mbps(T)	1.5 Mbps
Diff. Pair Support	Yes	NCR 5381

(T) - Theoretical Maximum

NCR 5385 FAMILY OF DEVICES

NCR 5385

- Currently in production, 1st family member

NCR 5385E

- Currently being sampled
- "Stop-gap" measure to NCR 5386 customers
- Supports current ANSI timings
- Manufactured until NCR 5386 is in production

NCR 5386

- Samples January '85, Production March '85
- Supports current ANSI timings
- Superset of NCR 5385/85E

NCR 5386S

- Samples 3Q '85
- Identical to NCR 5386 with synchronous operation to 3 Mbytes/sec