Price $2.50

CATALOG 1977

NEC micro computers, inc.

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MEMORY SELECTION GUIDE

DEVICE	SIZE	TECHNOLOGY	ACCESS TIME	CYCLE	SUPPLY VOLTAGES	PACKAGE MATERIAL	PACKAGE PINS
DYNAMIC RANDOM ACCESS MEMORIES							
μPD411	4K x 1 TS	NMOS	150 ns	380 ns	+12, +5, −5	Cerdip	22
μPD411-4	4K x 1 TS	NMOS	135 ns	320 ns	+15, +5, −5	Cerdip	22
μPD411A	4K x 1 TS	NMOS	200 ns	400 ns	+12, +5, −5	Plastic	22
μPD411M	4K x 1 TS	NMOS	200 ns	400 ns	+12, +5, −5	Cerdip	22
μPD418	4K x 1 TS	NMOS	200 ns	400 ns	+12, −5	C/P	18
μPD414	4K x 1 TS	NMOS	200 ns	375 ns	+12, +5, −5	C/P	16
μPD414A (F)	4K x 1 TS	NMOS	150 ns	320 ns	+12, +5, −5	C/P	16
μPD416	16K x 1 TS	NMOS	150 ns	375 ns	+12, +5, −5	C/P	16
STATIC RANDOM ACCESS MEMORIES							
μPD2101AL	256 x 4 TS	NMOS	250 ns	250 ns	+5	Plastic	22
μPD2102AL	1K x 1 TS	NMOS	250 ns	250 ns	+5	Plastic	16
μPD2111AL	256 x 4 TS	NMOS	250 ns	250 ns	+5	Plastic	18
μPD5101	256 x 4 TS	CMOS	800 ns	800 ns	+5	Plastic	22
μPD5101L	256 x 4 TS	CMOS	450 ns	450 ns	+5	Plastic	22
μPB2205	1K x 1 OC	Bipolar	50 ns	50 ns	+5	Cerdip	16
μPD410	4K x 1 TS	NMOS	100 ns	220 ns	+12, +5, −5	Cerdip	22
μPB2400 (F)	4K x 1 OC	Bipolar	50 ns	50 ns	+5	Cerdip	18
μPB2401 (F)	4K x 1 TS	Bipolar	50 ns	50 ns	+5	Cerdip	18
μPD4104 (F)	4K x 1 TS	NMOS	200 ns	310 ns	+5	C/P	18
μPD2114 (F)	1K x 4 TS	NMOS	300 ns	300 ns	+5	C/P	18
μPD6508 (F)	1K x 1 TS	CMOS	200 ns	200 ns	+5	C/P	16
MASK PROGRAMMED READ ONLY MEMORIES							
μPD464	256 x 8 TS	NMOS	450 ns	450 ns	+12, +5	C/P	24
μPD2308	1K x 8 TS	NMOS	450 ns	450 ns	+12, +5, −5	Cerdip	24
μPD2316A	2K x 8 TS	NMOS	450 ns	450 ns	+5	C/P	24
μPD2316E (F)	2K x 8 TS	NMOS	450 ns	450 ns	+5	C/P	24
μPD2332	4K x 8 TS	NMOS	450 ns	450 ns	+5	C/P	24
FIELD PROGRAMMABLE READ ONLY MEMORIES							
μPB403	256 x 4 OC	Bipolar	60 ns	60 ns	+5	Cerdip	16
μPB405	512 x 8 OC	Bipolar	70 ns	70 ns	+5	Cerdip	24
μPB425	512 x 8 TS	Bipolar	70 ns	70 ns	+5	Cerdip	24
μPB406	1K x 4 OC	Bipolar	70 ns	70 ns	+5	Cerdip	18
μPB426	1K x 4 TS	Bipolar	70 ns	70 ns	+5	Cerdip	18
μPB408 (F)	1K x 8 OC	Bipolar	85 ns	120 ns	+5	Cerdip	24
μPB428 (F)	1K x 8 TS	Bipolar	85 ns	120 ns	+5	Cerdip	24
μPB427 (F)	1K x 8 TS	Bipolar	120 ns	120 ns	+5	Cerdip	24
μPD2716 (F)	2K x 8 TS	NMOS	450 ns	450 ns	+5	Cerdip	24
μPD454	256 x 8 TS	NMOS	800 ns	800 ns	+12, −5*	Cerdip	24
μPD458	1K x 8 TS	NMOS	450 ns	450 ns	+12, −5*	Cerdip	28

(F) Future Product

* Read Mode

MEMORY ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
AMD	AM2101	256 x 4 SRAM	μPD2101AL
	AM2101	1024 x 1 SRAM	μPD2102AL
	AM2111	256 x 4 SRAM	μPD2111AL
	AM27LS00	256 x 1 SRAM	μPB2200/μPB2202
	AM27LS01	256 x 1 SRAM	μPB2206
	AM27LS02	16 x 4 SRAM	μPB2089/μPB2289
	AM27LS10	256 x 4 PROM	μPB403
	AM27S80	1024 x 8 PROM	μPB408
	AM27S81	1024 x 8 PROM	μPB428
	AM3101	16 x 4 SRAM	μPB2089
	Sn7489	16 x 4 SRAM	μPB2089
	Sn74S289	16 x 4 SRAM	μPB2289
	AM9050	4096 x 1 DRAM	μPD418
	AM9060	4096 x 1 DRAM	μPD411/μPD411A
	AM9101	256 x 4 SRAM	μPD2101AL
	AM9102	1024 x 1 SRAM	μPD2102AL
	9107	4096 x 1 DRAM	μPD411/μPD411A
	AM9111	256 x 4 SRAM	μPD2111AL
	AM9208	1024 x 8 ROM	μPD2308
	AM9216	2048 x 8 ROM	μPD2316E
EM&M Semi	4200	4096 x 1 SRAM	μPD410
	4402	4096 x 1 SRAM	μPD410
	R03-8316A	2048 x 8 ROM	μPD2316A
	R03-8316B	2048 x 8 ROM	μPD2316A
Fairchild	2101L	256 x 4 SRAM	μPD2101AL
	2102	1024 x 1 SRAM	μPD2102AL
	3508	1024 x 8 ROM	μPD2308
	3538	256 x 4 SRAM	μPD2101AL
	FM4027	4096 x 1 DRAM	μPD414A
	4096	4096 x 1 DRAM	μPD414
	F16K	16384 x 1 DRAM	μPD416
	7489	16 x 4 SRAM	μPB2089
	93411	256 x 1 SRAM	μPB2206
	93415	1024 x 1 SRAM	μPB2205
	93417	256 x 4 PROM	μPB403
	93438	512 x 8 PROM	μPB405
	93448	512 x 8 PROM	μPB425
	93452	1024 x 4 PROM	μPB406
	93453	1024 x 4 PROM	μPB426
Fujitsu	MB2114	1024 x 4 SRAM	μPD2114
	MB7054	1024 x 4 PROM	μPB426
	MB7057	256 x 4 PROM	μPB403
	MB7059	1024 x 4 PROM	μPB406
	MB8101	256 x 4 SRAM	μPD2101AL
	MB8107	4096 x 1 DRAM	μPD411/μPD411A
	MB8111	256 x 4 SRAM	μPD2111AL
	MB8116	16384 x 1 DRAM	μPD416
	MB8224	4096 x 1 DRAM	μPD414
	MB8227	4096 x 1 DRAM	μPD414A
	MB8308	1024 x 8 ROM	μPD2308
	MBM93415	1024 x 1 SRAM	μPB2205

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
Harris	HPROM-1024A	256 x 4 PROM	μPB403
	HM6501	256 x 4 SRAM	μPD5101
	HM6508	1024 x 1 SRAM	μPD6508
	HM7610	256 x 4 PROM	μPB403
	HM7640	512 x 8 PROM	μPB405
	HM7641	512 x 8 PROM	μPB425
	HM7642	1024 x 4 PROM	μPB406
	HM7643	1024 x 4 PROM	μPB426
Intersil	2608	1024 x 8 ROM	μPD2308
	2616	2048 x 8 ROM	μPD2316
	IM5501	16 x 4 SRAM	μPB2089/μPB2289
	IM5508	1024 x 1 SRAM	μPB2205
	IM5523A	256 x 1 SRAM	μPB2200/μPB2202
	IM5533A	256 x 1 SRAM	μPB2206
	IM5603	256 x 4 PROM	μPB403
	IM5605	512 x 8 PROM	μPB405
	IM5625	512 x 8 PROM	μPB425
	IM6508A	1024 x 1 SRAM	μPD6508
	7005	4096 x 1 DRAM	μPD414
	7027	4096 x 1 DRAM	μPD414A
	7101	256 x 4 SRAM	μPD2101AL
	7111	256 x 4 SRAM	μPD2111AL
	7114	1024 x 4 SRAM	μPD2114
	7116	16384 x 1 DRAM	μPD416
	7270	4096 x 1 DRAM	μPD418
	7271A	4096 x 1 DRAM	μPD418
	7280/A	4096 x 1 DRAM	μPD411/μPD411A
	IM7552	512 x 1 SRAM	μPD2102AL
Intel	2101	256 x 4 SRAM	μPD2101AL
	2102	1024 x 1 SRAM	μPD2102AL
	2104	4096 x 1 DRAM	μPD414/μPD414A
	2107	4096 x 1 DRAM	μPD411/μPD411A
	2111	256 x 4 SRAM	μPD2111AL
	2114	1024 x 4 SRAM	μPD2114
	2116	16384 x 1 DRAM	μPD416
	2308	1024 x 8 ROM	μPD2308
	2316A	2048 x 8 ROM	μPD2316A
	2316E	2048 x 8 ROM	μPD2316E
	3101A	16 x 4 SRAM	μPB2089/μPB2289
	3107	256 x 1 SRAM	μPB2206
	3106	256 x 1 SRAM	μPB2200/μPB2202
	3601	256 x 1 PROM	μPB403
	3604	512 x 8 PROM	μPB405
	3605	1024 x 4 PROM	μPB406
	3608	1024 x 8 PROM	μPB408
	3624	512 x 8 PROM	μPB425
	3625	1024 x 4 PROM	μPB426
	3628	1024 x 8 PROM	μPB428
	4316A	2048 x 8 ROM	μPD2316A
	5101	256 x 4 SRAM	μPD5101
	8101A	256 x 4 SRAM	μPD2101AL
	8102A	1024 x 1 SRAM	μPD2102AL
	8111A	256 x 4 SRAM	μPD2111AL
	8308	1024 x 8 ROM	μPD2308
	8316A	2048 x 8 ROM	μPD2316A

MEMORY ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
MMI	6300	256 x 1 PROM	μPB403
	6340	512 x 8 PROM	μPB405
	6341	512 x 8 PROM	μPB425
	6348	512 x 8 PROM	μPB405
	6349	512 x 8 PROM	μPB425
	6352	1024 x 4 PROM	μPB406
	6353	1024 x 4 PROM	μPB426
	6380	1024 x 8 PROM	μPB408
	6381	1024 x 8 PROM	μPB428
	6530	256 x 1 SRAM	μPB2206
	6531	256 x 1 SRAM	μPB2200/μPB2202
	6560	16 x 4 SRAM	μPB2089/μPB2289
Mostek	MK30000	1024 x 8 ROM	μPD2308
	MK31000	2048 x 8 ROM	μPD2316A
	MK32000	4096 x 8 ROM	μPD2332
	MK34000	2048 x 8 ROM	μPD2316E
	MK4027	4096 x 1 DRAM	μPD414A
	MK4102	1024 x 1 SRAM	μPD2102AL
	MK4104	4096 x 1 SRAM	μPD4104
	MK4116	16384 x 1 DRAM	μPD416
Motorola	MCM2102	1024 x 1 SRAM	μPD2102AL
	MCM2111	256 x 4 SRAM	μPD2111AL
	MCM6604	4096 x 1 DRAM	μPD414
	MCM6616	16384 x 1 DRAM	μPD416
	MCM68111	256 x 4 SRAM	μPD2111AL
	MCM68317	2048 x 8 ROM	μPD2316E
	MCM7640	512 x 8 PROM	μPB405
	MCM7641	512 x 8 PROM	μPB425
	MCM7642	1024 x 4 PROM	μPB406
	MCM7643	1024 x 4 PROM	μPB426
National	MM2101	256 x 4 SRAM	μPD2101AL
	MM2102A	1024 x 1 SRAM	μPD2102AL
	MM2111	256 x 4 SRAM	μPD2111AL
	MM2316A	2048 x 8 ROM	μPD2316A
	MM4280	4096 x 1 DRAM	μPD411M
	MM5280A	4096 x 1 DRAM	μPD411/μPD411A
	MM5281	4096 x 1 DRAM	μPD411/μPD411A
	DM7489	16 x 4 SRAM	μPB2089/μPB2289
	MM74S289	16 x 4 SRAM	μPB2089/μPB2289
	DM74S387	256 x 4 PROM	μPB403
	DM74S572	1024 x 4 PROM	μPB406
	DM74S573	1024 x 4 PROM	μPB426
	MM74C920	256 x 4 SRAM	μPD5101
	DM7535	256 x 4 PROM	μPB403
	DM7574	256 x 4 PROM	μPB403
	DM77S295	512 x 8 PROM	μPB405
	DM77S296	512 x 8 PROM	μPB425
	DM93415	1024 x 1 SRAM	μPB2205

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
Signetics	2101	256 x 4 SRAM	μPD2101AL
	2102	1024 x 1 SRAM	μPD2102AL
	2111	256 x 4 SRAM	μPD2111AL
	2316	2048 x 8 ROM	μPD2316
	2601	256 x 4 SRAM	μPD2101AL
	2608	1024 x 8 ROM	μPD2308
	2611	256 x 4 SRAM	μPD2111AL
	2680	4096 x 1 DRAM	μPD411/μPD411A
	N3101A	16 x 4 SRAM	μPB2089/μPB2289
	74S89	16 x 4 SRAM	μPB2089/μPB2289
	74S200	256 x 1 SRAM	μPB2200
	74S201	256 x 1 SRAM	μPB2200
	74S301	256 x 1 SRAM	μPB2202
	82S07	256 x 1 SRAM	μPB2206
	N82S10	256 x 1 SRAM	μPB2206
	82S16	256 x 1 SRAM	μPB2206
	82S17	256 x 1 SRAM	μPB2200/μPB2202
	82S26	256 x 4 PROM	μPB403
	N82S115	512 x 8 PROM	μPB425
	82S126	256 x 4 PROM	μPB403
	N82S136	1024 x 4 PROM	μPB406
	N82S137	1024 x 4 PROM	μPB426
	82S140	512 x 8 PROM	μPB405
	82S141	512 x 8 PROM	μPB425
	N93415A	1024 x 1 SRAM	μPB2205
T.I.	TMS2101	256 x 4 SRAM	μPD2101AL
	TMS2102	1024 x 1 SRAM	μPD2102AL
	TMS4027	4096 x 1 DRAM	μPD414A
	TMS4033	1024 x 1 SRAM	μPD2102AL
	TMS4034	1024 x 1 SRAM	μPD2102AL
	TMS4039	256 x 4 SRAM	μPD2101AL
	TMS4042	256 x 4 SRAM	μPD2111AL
	TMS4050	4096 x 1 DRAM	μPD418
	TMS4051	4096 x 1 DRAM	μPD418
	TMS4060	4096 x 1 DRAM	μPD411/μPD411A
	TMS4116	16384 x 1 DRAM	μPD416
	TMS4732	4096 x 8 ROM	μPD2332
	SN74S44	512 x 8 PROM	μPB425
	SN7489	16 x 4 SRAM	μPB2089/μPB2289
	SN74S201	256 x 1 SRAM	μPB2200
	SN74S289	16 x 4 SRAM	μPB2089/μPB2289
	SN74S301	256 x 1 SRAM	μPB2200/μPB2202
	SN74S314	1024 x 1 SRAM	μPB2205
	SN74S387	256 x 4 PROM	μPB403
	SN74S475	512 x 8 PROM	μPB405

FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION

The μPD411 Family consists of six 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411 Family is designed using dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is a non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

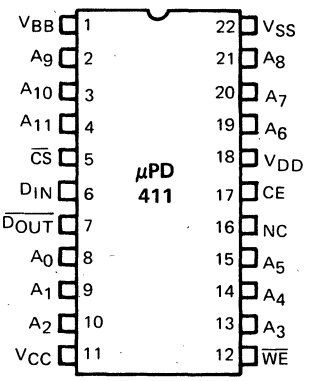
All of these products are guaranteed for operation over the 0 to 70°C temperature range.

Important features of the μPD411 family are:

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power/0.3 mW (Typ.)
- Power Supply: +12, +5, -5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Ceramic Dual-in-Line Package
- Replacement for INTEL'S 2107B, TI'S 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411-E	350 ns	800 ns	960 ns	1 ms
μPD411	300 ns	470 ns	650 ns	2 ms
μPD411-1	250 ns	470 ns	640 ns	2 ms
μPD411-2	200 ns	400 ns	520 ns	2 ms
μPD411-3	150 ns	380 ns	470 ns	2 ms
μPD411-4	135 ns	320 ns	320 ns	2 ms

PIN CONFIGURATION



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$A_0 - A_5$	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	Power (-5V)
NC	No Connection

Rev/2

FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

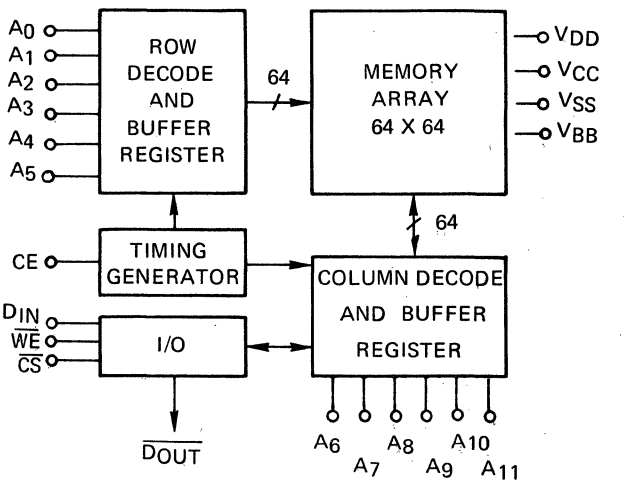
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*μPD411-E = 1 millisecond refresh period.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

	μPD411 FAMILY (EXCEPT 411-4)	μPD411-4
Operating Temperature	0°C to +70°C	+10°C to +55°C
Storage Temperature	−55°C to +150°C	−55°C to +150°C
All Output Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
All Input Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{DD}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{CC}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Power Dissipation	1.0W	1.5W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V,
Except V_{DD} = +15V ±5% for 411-4.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = $V_{ILC\ MIN}$ to $V_{IHC\ MAX}$
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	$I_{DD\ OFF}$		20	200	μA	CE = −1.0V to 0.6V
V_{DD} Supply Current during CE on	$I_{DD\ ON}$		35④	60⑤	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C,
μPD411-E	$I_{DD\ AV}$		29	60	mA	Cycle Time = 800 ns
μPD411	$I_{DD\ AV}$		37	60	mA	Cycle Time = 470 ns
μPD411-1	$I_{DD\ AV}$		37	60	mA	Cycle Time = 470 ns
μPD411-2	$I_{DD\ AV}$		37	60	mA	Cycle Time = 400 ns
μPD411-3	$I_{DD\ AV}$		41	65	mA	Cycle Time = 380 ns
μPD411-4	$I_{DD\ AV}$		55	80	mA	Cycle Time = 320 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	$I_{CC\ OFF}$		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.0		0.6	V	
Input High Voltage	V_{IH}	2.4 ④		V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	−1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}−1	V_{DD}	V_{DD}+1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA

Notes:
① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.
V_{CC} is connected to output buffer only.
④ 3.5V for μPD411-E
⑤ 65 mA for μPD411-3
80 mA for μPD411-4
⑥ 41 mA for μPD411-3
55 mA for μPD411-4

CAPACITANCE

T_a = 0° − 70°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance, $\overline{CS}$	C_{AD}		4	6	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pF	V_{IN} = V_{SS}
Data Output Capacitance	C_{OUT}		5	7	pF	V_{OUT} = 0V
D_{IN} and $\overline{WE}$ Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
Cycle Time	t_{CY}	800		470		470		400		380		320		ns
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	210	3000	200	3000	ns
CE Output Delay	t_{CO}		330		280		230		180		130		115	ns
Access Time	t_{ACC}		350		300		250		200		150		135	ns
CE to $\overline{WE}$	t_{WL}	40		40		40		40		40		40		ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		0		ns

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CY}	800		470		470		400		380		320		ns
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	210	3000	200	3000	ns
$\overline{WE}$ to CE off	t_W	200		180		180		150		150		65		ns
CE to $\overline{WE}$	t_{CW}	380		300		260		230		210		200		ns
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		40		ns
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		100		65		ns

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

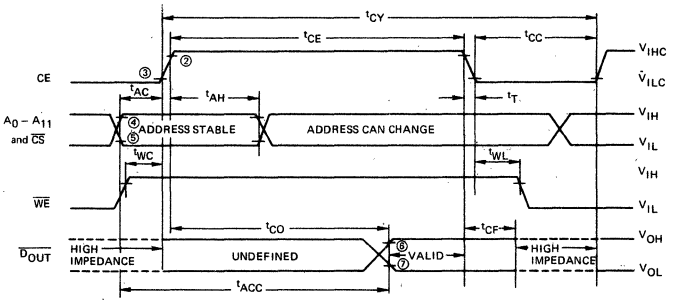
READ-MODIFY-WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read–Modify–Write (RMW) Cycle Time	t_{RWC}	960		650		640		520		470		320		ns
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	300	3000	200	3000	ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		0		ns
$\overline{WE}$ to CE off	t_W	200		180		180		150		150		65		ns
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		100		65		ns
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		40		ns
CE to Output Display	t_{CO}		330		280		230		180		130		115	ns
Access Time	t_{ACC}		350		300		250		200		150		135	ns

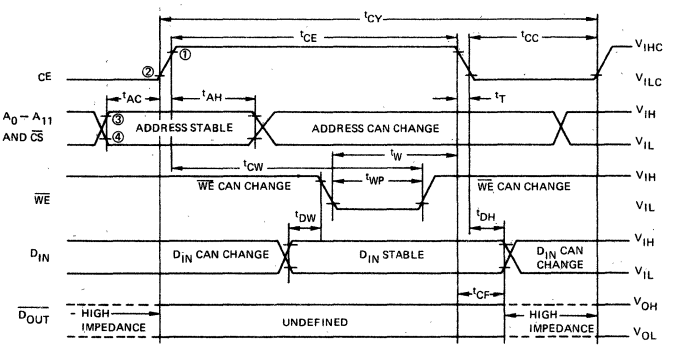
TIMING WAVEFORMS

READ CYCLE ①



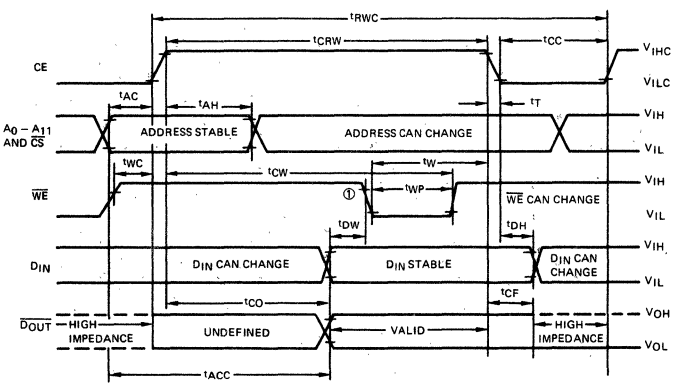
Notes: ① For refresh cycle row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.
② V_{DD} −2V is the reference level for measuring timing of CE.
③ V_{SS} +2V is the reference level for measuring timing of CE.
④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑥ V_{SS} +2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑦ V_{SS} +0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

WRITE CYCLE



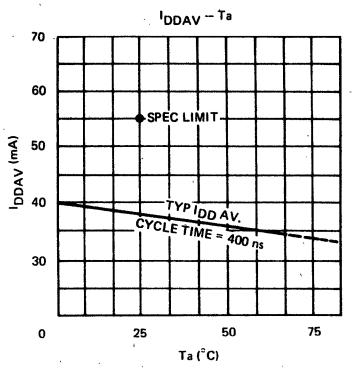
Notes: ① V_{DD} −2V is the reference level for measuring timing of CE.
② V_{SS} +2V is the reference level for measuring timing of CE.
③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

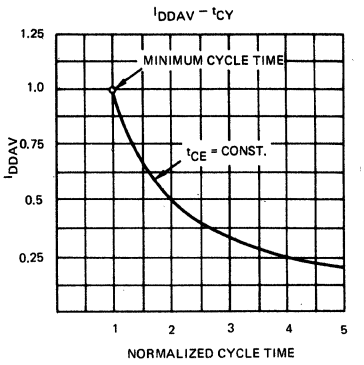
READ-MODIFY-WRITE CYCLE

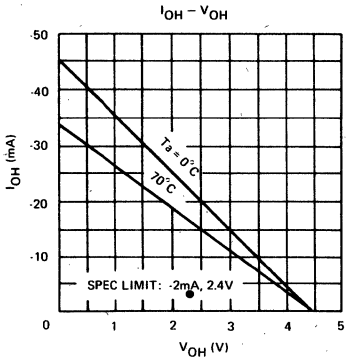


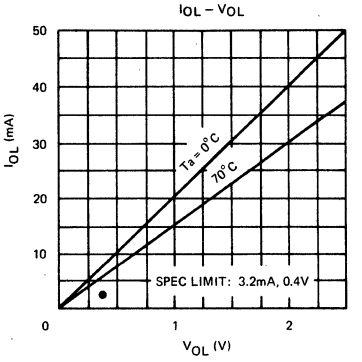
Note: ① $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

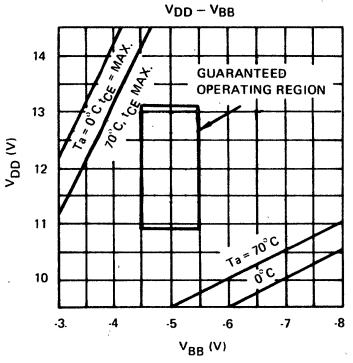
TYPICAL OPERATING CHARACTERISTICS (Except 411-4)

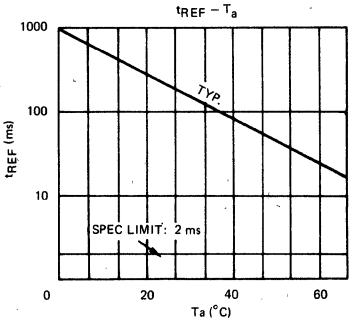












POWER CONSUMPTION

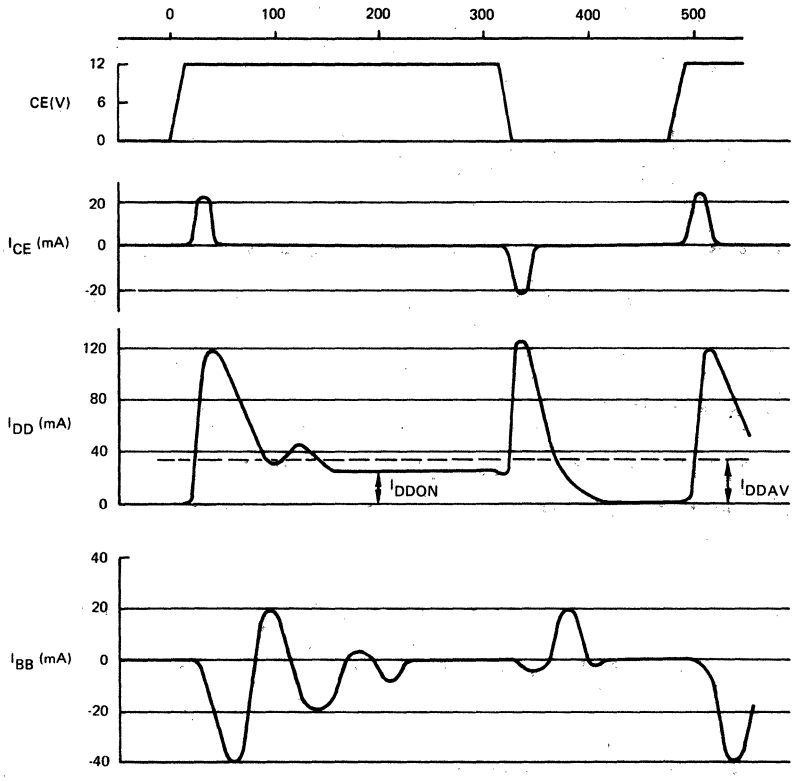
Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$.

Typical power dissipation for each product is shown below.

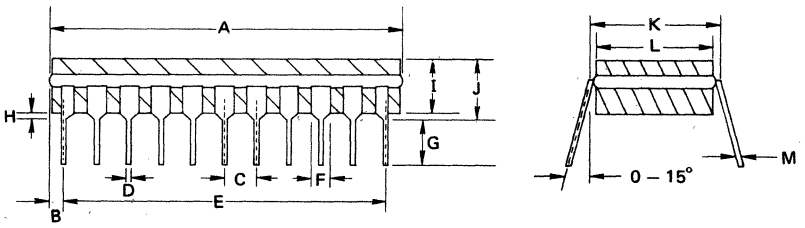
	mW (TYP.)	CONDITIONS
μPD411-E	350	Ta = 25° C, t_{cy} = 800ns, t_{CE} = 380ns
μPD411	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 300ns
μPD411-1	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 260ns
μPD411-2	450	Ta = 25° C, t_{cy} = 400ns, t_{CE} = 230ns
μPD411-3	550	Ta = 25° C, t_{cy} = 380ns, t_{CE} = 210ns
μPD411-4	660	Ta = 25° C, t_{cy} = 320ns, t_{CE} = 200ns

See above curves for power dissipation versus cycle time.

CURRENT WAVEFORMS



PACKAGE OUTLINE μPD411D



ITEM	MILLIMETERS	INCHES
A	27.43 MAX	1.079 MAX
B	1.27 MAX	0.05 MAX
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 MAX	0.165 MAX
J	5.08 MAX	0.200 MAX
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

4096 BIT DYNAMIC RAMS

DESCRIPTION

The μPD411A Family consists of four 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411A Family is designed using dynamic circuitry which reduces the standby power dissipation.

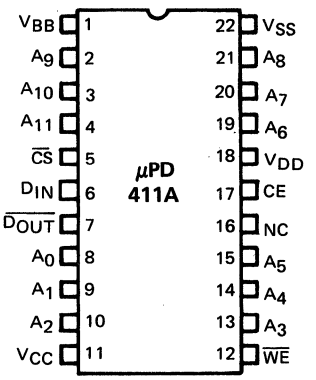
Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power 0.7 mW (Typ.)
- Power Supply +12, +5, −5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Plastic Dual-in-Line Package
- Replacement for INTEL's 2107B, TI's 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411A-E	350 ns	800 ns	960 ns	1 ms
μPD411A	300 ns	470 ns	650 ns	2 ms
μPD411A-1	250 ns	430 ns	600 ns	2 ms
μPD411A-2	200 ns	400 ns	520 ns	2 ms

PIN CONFIGURATION



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$A_0 - A_5$	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	(Power −5V)
NC	No Connection

FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

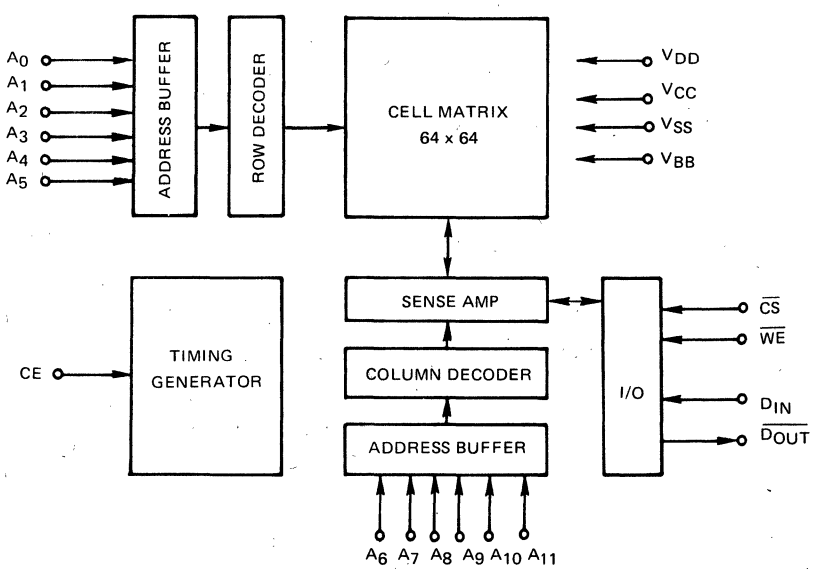
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*μPD411A-E = 1 millisecond refresh period.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Output Voltage ①	+20 to −0.3 Volts
All Input Voltages ①	+20 to −0.3 Volts
Supply Voltage V_{DD} ①	+20 to −0.3 Volts
Supply Voltage V_{CC} ①	+20 to −0.3 Volts
Supply Voltage V_{SS} ①	+20 to −0.3 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP. ①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF		50	200	μA	CE = −1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON		35	50	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411A-E	I_{DD} AV		25	40	mA	Cycle Time = 800 ns
μPD411A	I_{DD} AV		38	55	mA	Cycle Time = 470 ns
μPD411A-1	I_{DD} AV		38	55	mA	Cycle Time = 430 ns
μPD411A-2	I_{DD} AV		38	55	mA	Cycle Time = 400 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 1	V	
CE Input Low Voltage	V_{ILC}	−1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD} − 1	V_{DD}	V_{DD} + 1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}			6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}			6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}			6	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}			7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}			7	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE1}			27	pF	V_{IN} = V_{SS}
	C_{CE2}			22	pF	V_{IN} = V_{DD}

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Time Between Refresh	t_{REF}		1		2		2		2	ms	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
Cycle Time	t_{CY}	800		470		430		400		ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
CE Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	
CE to $\overline{WE}$	t_{WL}	40		40		40		40		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Cycle Time	t_{CY}	800		470		430		400		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = ITTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	
CE to $\overline{WE}$	t_{CW}	380		300		260		230		ns	
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	

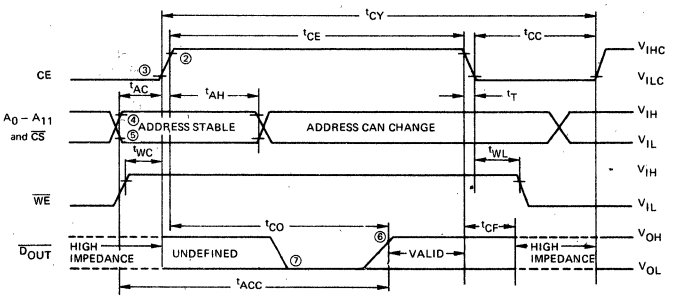
Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

READ-MODIFY-WRITE CYCLE

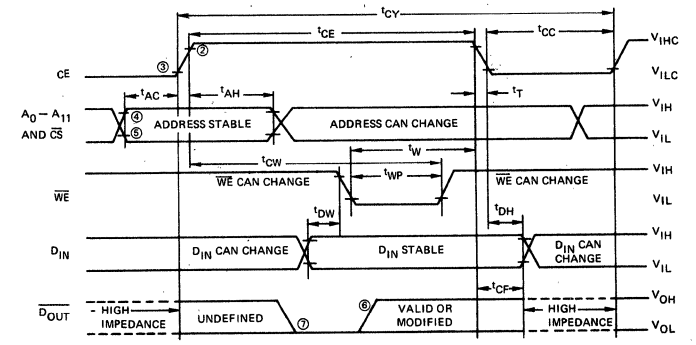
T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	960		650		600		520		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
CE to Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	

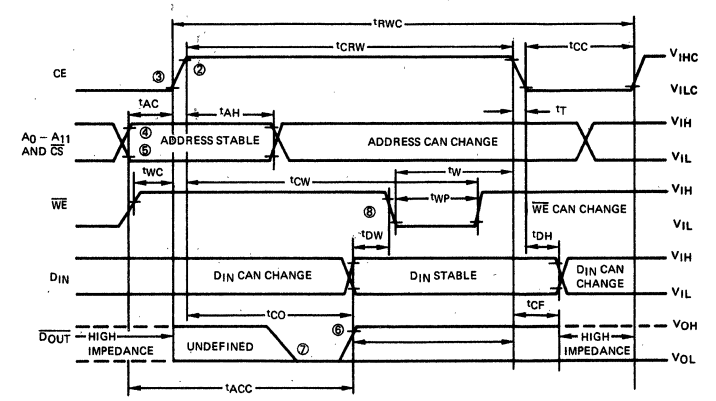
READ AND REFRESH CYCLE ①



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② V_{DD} – 2V is the reference level for measuring timing of CE.

③ V_{SS} + 2V is the reference level for measuring timing of CE.

④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

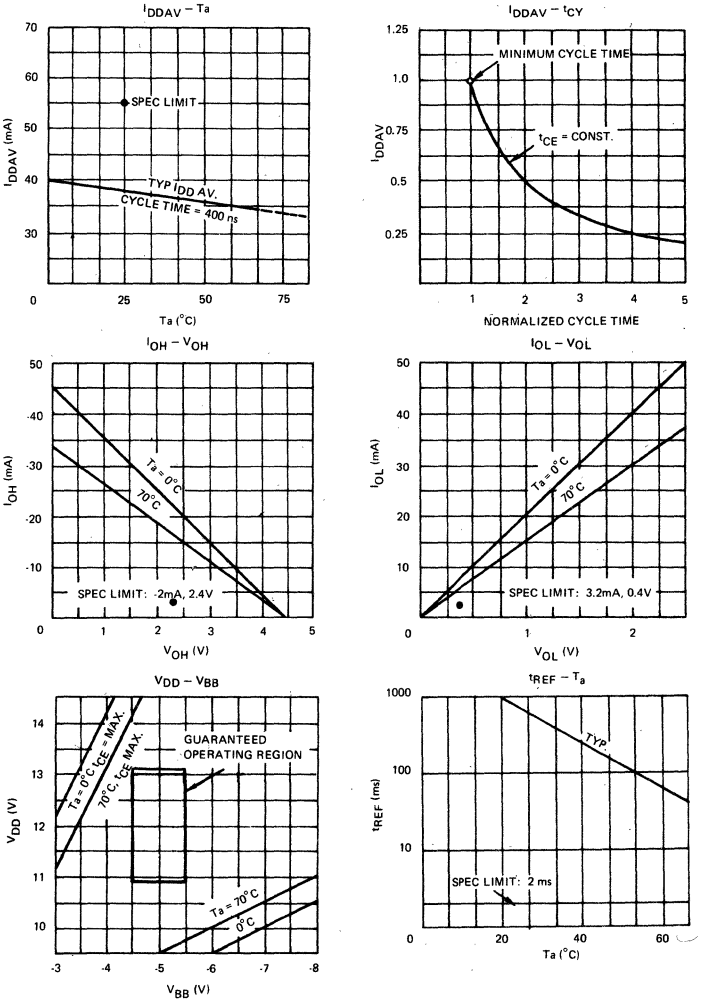
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑥ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑧ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

TYPICAL OPERATING CHARACTERISTICS



POWER CONSUMPTION

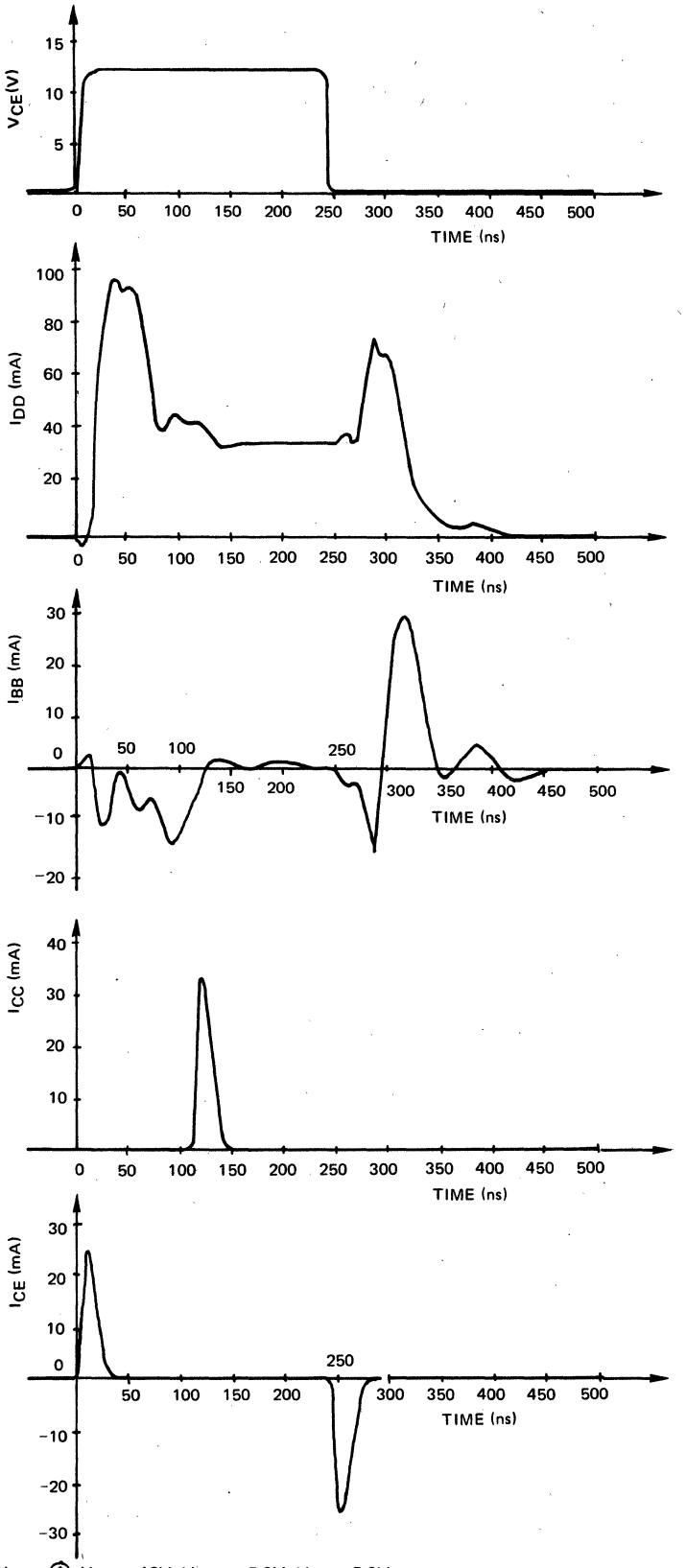
Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$

Typical power dissipation for each product is shown below.

	mW (TYP.)	CONDITIONS
μPD411A-E	300 mW	$T_a = 25°C$, $t_{cy} = 800$ ns, $t_{CE} = 380$ ns
μPD411A	460 mW	$T_a = 25°C$, $t_{cy} = 470$ ns, $t_{CE} = 300$ ns
μPD411A-1	460 mW	$T_a = 25°C$, $t_{cy} = 430$ ns, $t_{CE} = 260$ ns
μPD411A-2	460 mW	$T_a = 25°C$, $t_{cy} = 400$ ns, $t_{CE} = 230$ ns

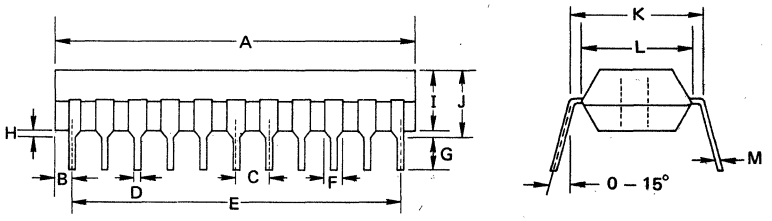
See curve above for power dissipation versus cycle time.

CURRENT WAVEFORMS ①



Note: ① V_{DD} = 12V, V_{BB} = −5.0V, V_{CC} = 5.0V

PACKAGE OUTLINE
μPD411AC



μPD411AC (Plastic)

ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

4096 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD411-M Family consists of three 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where wide operating environmental temperatures are important design considerations. The μPD411-M Family is designed using dynamic circuitry which reduces the standby power dissipation.

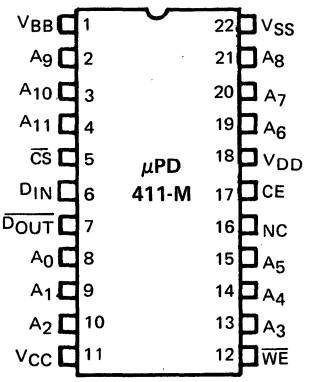
Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

- 4096 Words x 1 Bit Organization.
- Wide Operating Temperature Range (T_a = –40 to +85°C).
- TTL Compatibility on All Inputs (except CE).
- Three-State Output Providing TTL Compatibility.
- 22 Pin Dual-In-Line Ceramic Package.
- 3 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME	POWER DISSIPATION
μPD411-M	300 ns	470 ns	650 ns	2 ms	65 mA
μPD411-1M	250 ns	430 ns	600 ns	2 ms	65 mA
μPD411-2M	200 ns	400 ns	520 ns	2 ms	65 mA

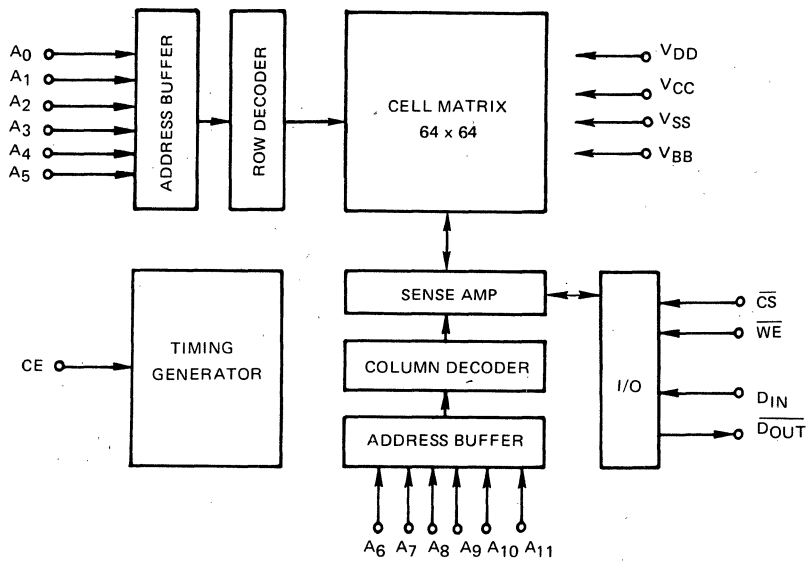
PIN CONFIGURATION



PIN NAMES

A_0 - A_{11}	Address Inputs
A_0 - A_5	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	Power (-5V)
NC	No Connection

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−40°C to +85°C ①
Storage Temperature	−55°C to +150°C
All Output Voltages	−0.3 to +20 Volts ②
All Input Voltages	−0.3 to +20 Volts ②
Supply Voltage V_{DD}	−0.3 to +20 Volts ②
Supply Voltage V_{CC}	−0.3 to +20 Volts ②
Supply Voltage V_{SS}	−0.3 to +20 Volts ②
CE Input Voltage	−0.3 to +20 Volts
Power Dissipation	1.0W

Notes: ① Still Air
② Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C.

CAPACITANCE

V_{CC} = +5V ± 5%, V_{DD} = +12V ± 5%, V_{SS} = 0V, V_{BB} = −5V ± 5%, T_a = −40 to +85°C

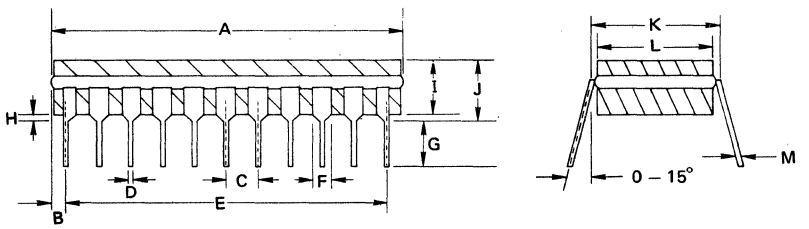
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}			7	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}			6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}			6	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}			7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}			7	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE1}			27	pF	V_{IN} = V_{SS}
	C_{CE2}			22	pF	V_{IN} = V_{DD}

DC CHARACTERISTICS

$T_a = -40°C$ to $+85°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}			10	μA	$V_{IN} = V_{IL}$ MIN to V_{IH} MAX
CE Input Load Current	I_{LC}			10	μA	$V_{IN} = V_{ILC}$ MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}			10	μA	CE = V_{ILC} or $\overline{CS} = V_{IH}$ V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF			200	μA	CE = -1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON			65	mA	CE = V_{IHC}, $T_a = 25°C$
Average V_{DD} Current μPD411-M μPD411-1M μPD411-2M	 I_{DD} AV I_{DD} AV I_{DD} AV			 65 65 65	 mA mA mA	$T_a = 25°C$ Cycle Time = 470 ns Cycle Time = 430 ns Cycle Time = 400 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF			10	μA	CE = V_{ILC} or $\overline{CS} = V_{IH}$
Input Low Voltage	V_{IL}	-1.0		0.6	V	
Input High Voltage	V_{IH}	2.6		V_{CC} + 1	V	
CE Input Low Voltage	V_{ILC}	-1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD} - 1	V_{DD}	V_{DD} + 1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = -2.0 mA
Time Between Refresh	t_{REF}			2	ms	

Notes: ① Typical values are for $T_a = 25°C$ and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.



PACKAGE OUTLINE μPD411-MD

ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

AC CHARACTERISTICS

READ CYCLE

T_a = –40°C to +85°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD411-M		μPD411-1M		μPD411-2M			
		MIN	MAX	MIN	MAX	MIN	MAX		
Time Between Refresh	t_{REF}		2		2		2	ms	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1_{TTL} Gate V_{ref} = 2.0 or 0.8 Volts
Address to CE Set Up Time	t_{AC}	0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		ns	
CE Off Time	t_{CC}	130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	ns	
Cycle Time	t_{CY}	470		430		400		ns	
CE on Time	t_{CE}	300	3000	260	3000	230	3000	ns	
CE Output Delay	t_{CO}		280		230		180	ns	
Access Time	t_{ACC}		300		250		200	ns	
CE to $\overline{WE}$	t_{WL}	40		40		40		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		ns	
$\overline{CS}$ Hold Time	t_{CSH}	150		150		150		ns	
$\overline{CS}$ Set Up Time	t_{CSC}	0		0		0		ns	

WRITE CYCLE

T_a = –40°C to +85°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD411-M		μPD411-1M		μPD411-2M			
		MIN	MAX	MIN	MAX	MIN	MAX		
Cycle Time	t_{CY}	470		430		400		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1_{TTL} Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		ns	
CE Off Time	t_{CC}	130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	ns	
CE on Time	t_{CE}	300	3000	260	3000	230	3000	ns	
$\overline{WE}$ to CE off	t_W	180		180		150		ns	
CE to $\overline{WE}$	t_{CW}	300		260		230		ns	
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		ns	
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		ns	
$\overline{CS}$ Set Up Time	t_{CSC}	0		0		0		ns	
$\overline{CS}$ Hold Time	t_{CSH}	150		150		150		ns	

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

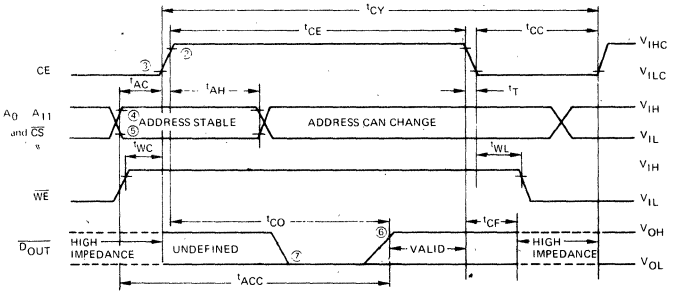
READ-MODIFY-WRITE CYCLE

T_a = –40°C to +85°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = –5V ± 5%, V_{SS} = 0V, unless otherwise noted.

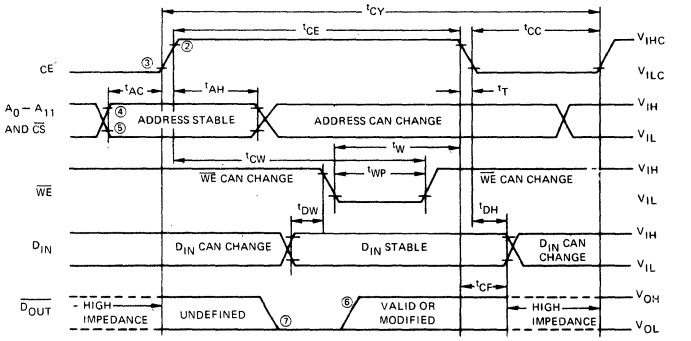
PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPD411-M		μPD411-1M		μPD411-2M			
		MIN	MAX	MIN	MAX	MIN	MAX		
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	650		600		520		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1_{TTL} Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		ns	
CE Off Time	t_{CC}	130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	ns	
CE Width During RMW	t_{CRW}	480	3000	430	3000	350	3000	ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		ns	
$\overline{WE}$ to CE off	t_W	180		180		150		ns	
$\overline{WE}$ Pulse Width	t_{WP}	180		180		150		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		ns	
CE to Output Delay	t_{CO}		280		230		180	ns	
Access Time	t_{ACC}		300		250		200	ns	
CE on Time	t_{CE}	480	3000	430	3000	350	3000	ns	
$\overline{CS}$ Set Up Time	t_{CSC}	0		0		0		ns	
$\overline{CS}$ Hold Time	t_{CSH}	150		150		150		ns	
CE to $\overline{WE}$	t_{CW}	480		430		350		ns	

TIMING WAVEFORMS

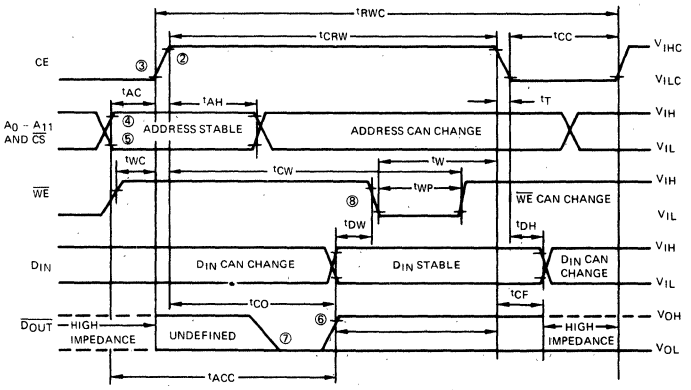
READ AND REFRESH CYCLE ①



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② V_{DD} – 2V is the reference level for measuring timing of CE.

③ V_{SS} + 2V is the reference level for measuring timing of CE.

④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑥ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑧ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

DESCRIPTION

The NEC μPD414 is a 4096 words by 1 bit Dynamic N channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The μPD414 uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The μPD414 is packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either cerdip or plastic.

The use of the 16 pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the μPD414 on 6 address input pins. The two 6 bit address words are latched into the μPD414 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

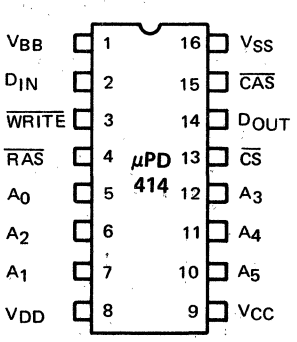
The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention. Refreshing is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2 milliseconds.

FEATURES

- 4096 Words x 1 Bit Organization
- Refresh Period 2 ms
- Standard 16 Pin Cerdip and Plastic Packages
- Low Standby Power
- All Inputs Including Clocks TTL Compatible
- Standard Power Supplies +12V, +5V, -5V
- Gated $\overline{CAS}$ Characteristic
- On-Chip Latches for Addresses, Chip Select and Data In
- Simple Memory Expansion Chip Select
- Output is Three State, TTL Compatible; Data is Latched and Valid into Next Cycle
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD414-E	350 ns	500 ns	700 ns
μPD414	300 ns	425 ns	590 ns
μPD414-1	250 ns	375 ns	480 ns
μPD414-2	200 ns	375 ns	420 ns

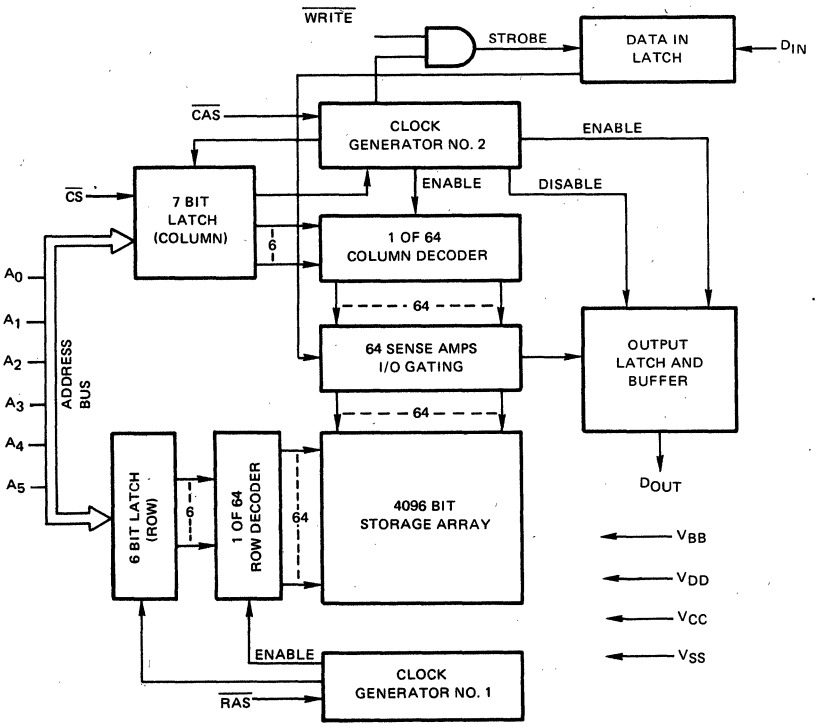
PIN CONFIGURATION



PIN NAMES

A_0-A_5	Address Inputs
$\overline{CAS}$	Column Address Strobe
$\overline{CS}$	Chip Select
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +25 Volts
All Input Voltages ①	−0.5 to +25 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +25 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted. ①②

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Capacitance	C_{AD}			10	pF	V_{IN} = V_{SS}
$\overline{CAS}$, $\overline{RAS}$, $\overline{CS}$ Capacitance	C_C			7	pF	V_{IN} = V_{SS}
Data Output Capacitance	C_{OUT}			8	pF	V_{OUT} = 0V
D_{IN} and $\overline{WRITE}$ Capacitance	C_{IN}			7	pF	V_{IN} = V_{SS}

Notes: ① All voltages referenced to V_{SS}. The only requirement for the sequence of applying voltages to the device is that V_{DD}, V_{CC}, and V_{SS} should never be 0.5V or more negative than V_{BB}.

② Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, ① V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ②	MAX		
Input Load Current (any input)	I_{LI}			10	μA	⑤
Output Leakage Current for High Impedance State	I_{LO}			10	μA	Chip deselected ⑥⑦
V_{DD} Supply Current	$I_{DD}OFF$ ③			2.0	mA	$\overline{CAS}$ and $\overline{RAS}$ at V_{IH}. Chip deselected. ⑥
Average V_{DD} Current	$I_{DD}AV$ ③			35	mA	Cycle time = Min ④ t_{RP} = 150 ns, T_a = 25°C
V_{CC} Supply Current when deselected	$I_{CC}OFF$			10	μA	⑧
Average V_{BB} Current	I_{BB} ③			75	μA	
Average V_{DD} Power Supply Current During "$\overline{RAS}$ only" cycles	I_{DD3}			28	mA	④
Input Low Voltage (any input)	V_{IL}	−1.0		0.8	V	①⑨
Input High Voltage except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4		7.0	V	①⑨
Output Low Voltage	V_{OL}	0		0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH}	2.4		7.0	V	I_{OH} = −5.0 mA
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	①
Supply Voltage	V_{CC}	V_{SS}	5.0	V_{DD}	V	① ⑩
Supply Voltage	V_{SS}	0	0	0	V	①
Supply Voltage	V_{BB}	−4.5	−5.0	−5.5	V	①
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	⑨

Notes:
① All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
② Typical values are for T_a = 25°C and nominal power supply voltages.
③ The I_{DD} current flows to V_{SS}. The I_{BB} current is the sum of all leakage currents.
④ Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
⑤ All device pins at 0 volts except V_{BB} which is at −5 volts and the pin under test which is at +10 volts.
⑥ Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
⑦ $0V \leq V_{OUT} \leq +10V$.
⑧ When chip is selected V_{CC} supply current is dependent on output loading; V_{CC} is connected to output buffer only.
⑨ Device speed is not guaranteed at input voltages greater than TTL levels (0 to +5V).
⑩ Output voltage will swing from V_{SS} to V_{CC} if $V_{CC} \leq V_{DD} - 4$ volts. If $V_{CC} \geq V_{DD} - 4$ volts, the output will swing from V_{SS} to a voltage somewhat less than V_{DD}.

AC CHARACTERISTICS

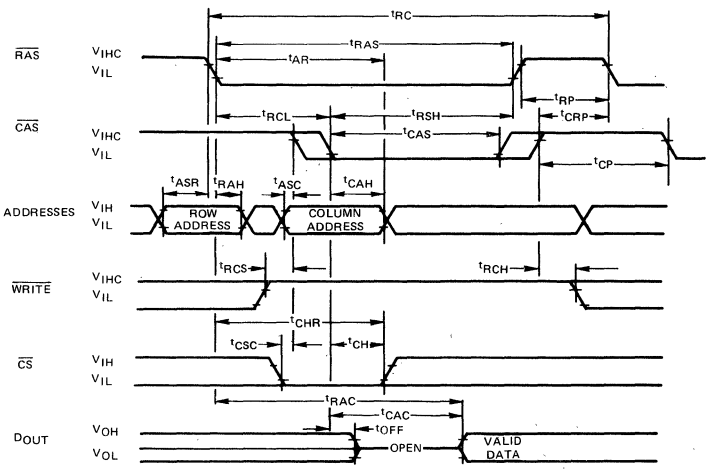
T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS												SYMBOL	TEST CONDITIONS
		414-E			414			414-1			414-2				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Random read or write cycle time	t_{RC}	500			425			375			375			ns	②
Read write cycle time	t_{RWC}	700			590			480			420			ns	
Access time from row address strobe	t_{RAC}			350			300			250			200	ns	③ ⑤
Access time from column address strobe	t_{CAC}			200			165			140			135	ns	④ ⑤
Output buffer turn-off delay	t_{OFF}			100			80			60			50	ns	⑥
Row address strobe precharge time	t_{RP}	150			125			120			120			ns	
Row address strobe pulse width	t_{RAS}	350		32,000	300		32,000	250		32,000	200		32,000	ns	
Row address strobe hold time	t_{RSH}	200			165			140			135			ns	
Column address strobe pulse width	t_{CAS}	200		3,000	165		3,000	140		3,000	135		3,000	ns	
Row to column strobe lead time	t_{RCL}	110		150	90		135	35		110	25		65	ns	⑦
Row address set-up time	t_{ASR}	0			0			0			0			ns	
Row address hold time	t_{RAH}	100			80			35			25			ns	
Column address set-up time	t_{ASC}	0			0			0			0			ns	
Column address hold time	t_{CAH}	100			80			60			40			ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	210			170			160			120			ns	
Chip select set-up time	t_{CSC}	0			0			0			0			ns	
Chip select hold time	t_{CH}	100			80			60			40			ns	
Chip select hold time referenced to $\overline{RAS}$	t_{CHR}	210			170			160			120			ns	
Transition time (rise and fall)	t_T	5		50	5		50	3		50	3		50	ns	⑧
Read command set-up time	t_{RCS}	0			0			0			0			ns	
Read command hold time	t_{RCH}	0			0			0			0			ns	
Write command hold time	t_{WCH}	150			130			75			55			ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	260			220			160			120			ns	
Write command pulse width	t_{WP}	200			165			75			55			ns	
Write command to row strobe lead time	t_{RWL}	200			165			140			135			ns	
Write command to column strobe lead time	t_{CWL}	200			165			140			135			ns	
Data in set-up time	t_{DS}	0			0			0			0			ns	⑨
Data in hold time	t_{DH}	150			130			110			110			ns	⑨
Data in hold time referenced to $\overline{RAS}$	t_{DHR}	260			220			195			175			ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	0			0			0			0			ns	
Column precharge time	t_{CP}	150			125			120			120			ns	
Refresh period	t_{RFSH}			2			2			2			2	ms	
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	200			165			90			80			ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	350			300			175			145			ns	⑩

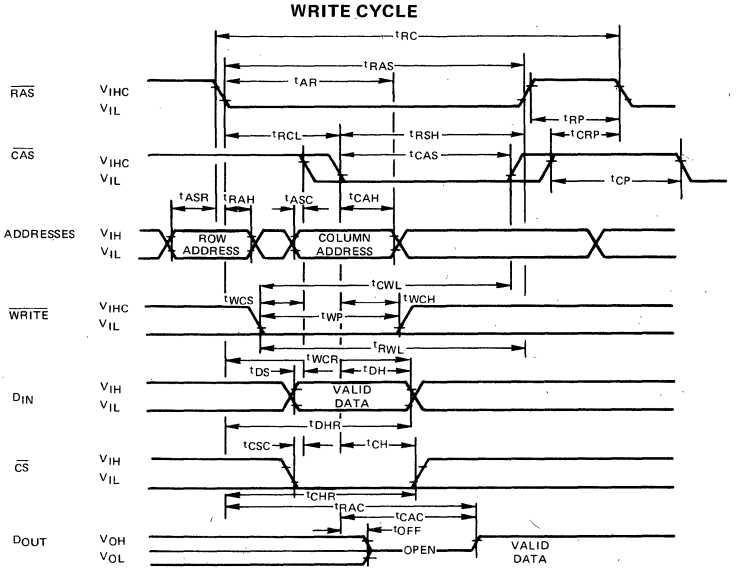
Notes:
① A.C. measurements assume t_T = 5 ns.
② Minimum cylce time (t_{RC}) is greater than $t_{RAS} + t_{RP} + 2t_T$ in order to limit power dissipation.
③ Assumes that $t_{RCL} + t_T \leq t_{RCL}$ (max).
④ Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max).
⑤ Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
⑥ Assumes that $t_{RCL} + t_T \geq t_{RCL}$ (max). If $t_{RCL} + t_T < t_{RCL}$ (max), $60 + t_{RCL}$ (max) − $t_{RCL} - t_T$ ns min.
⑦ Operation within the t_{RCL} (max) limit insures that t_{RAC} (max) can be met. t_{RCL} (max) is specified as a reference point only; if t_{RCL} is greater than the specified t_{RCL} (max) limit, then access time is controlled exclusively by t_{CAC}.
⑧ V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
⑨ These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
⑩ t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only:
If $t_{CWD} + t_T \leq t_{CWD}$ (min), the data out latch will contain high level data.
If $t_{CWD} \geq t_{CWD}$ (max) + t_T and $t_{RWD} \geq t_{RWD}$ (max) + t_T, the data out latch will contain the data read from the selected cell.
If t_{CWD} does not meet the above constraints, then data out latch will contain indeterminate data.

TIMING WAVEFORMS

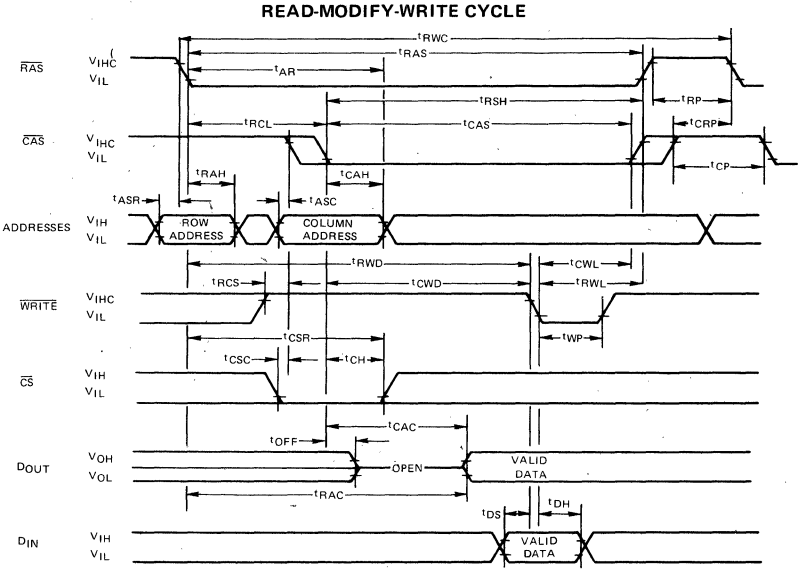
READ CYCLE



WRITE CYCLE

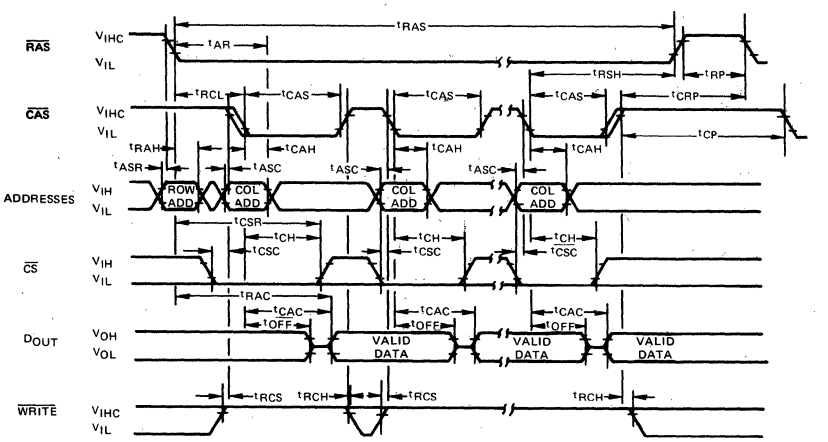


READ-MODIFY-WRITE CYCLE

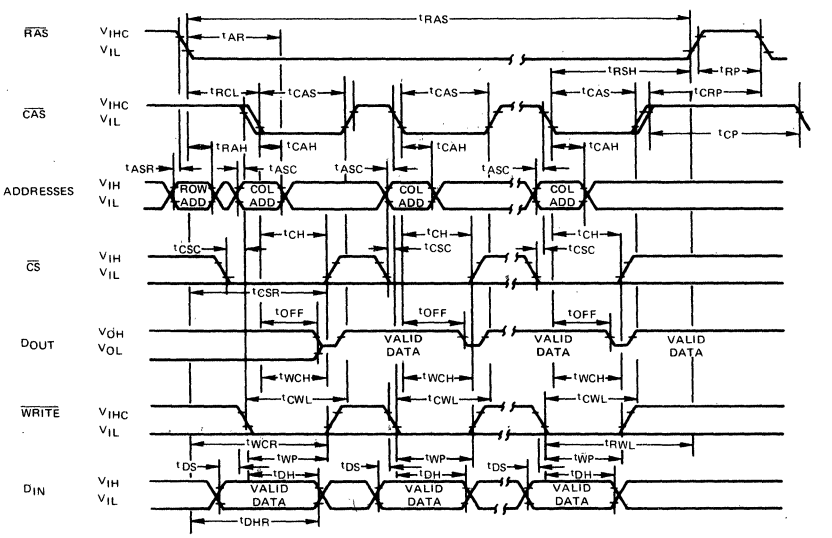


TIMING WAVEFORMS (CONT.)

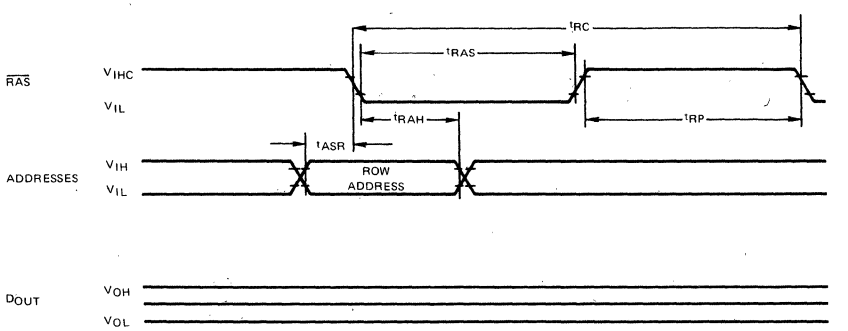
PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



"RAS ONLY" REFRESH CYCLE



Note: D_{OUT} remains unchanged from previous cycle.

ADDRESSING

The 12 address bits required to decode 1 of 4096 bit locations are multiplexed onto the 6 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 6 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the column address and chip select signals are applied and $\overline{CAS}$ is brought low. Since the column address and chip select are not needed internally until a time of t_{RCL} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{RCL} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, Data out will unconditionally assume a logic "1" state. If $\overline{WRITE}$ is mode active after the access time, as in a read/write cycle, the output will reflect the data read. The output data is latched and will remain in its proper state until the next negative transition of $\overline{CAS}$.

PAGE MODE

The μPD414 may also be operated in page mode for either reading or writing by keeping $\overline{RAS}$ low after strobing in the row address, and cycling $\overline{CAS}$ for each new column address.

REFRESH

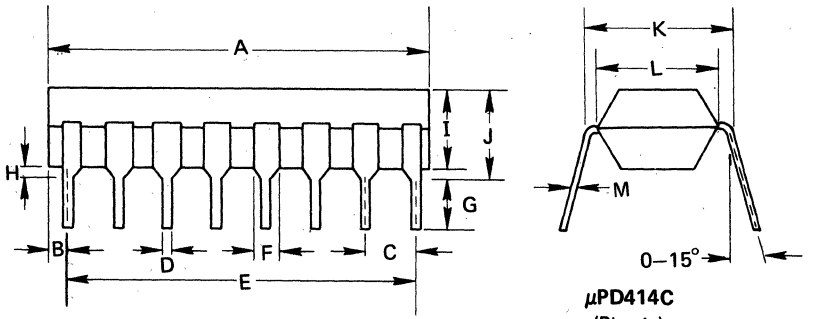
Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 64 row addresses every 2 milliseconds or less. Any memory cycle will refresh the chip regardless of the state of chip select although the chip must be deselected if a write cycle is used to avoid altering data. The data output will go to the high impedance state if chip select is high when $\overline{CAS}$ is brought low.

Refresh may also be achieved by cycling $\overline{RAS}$ only and strobing in each of the 64 row addresses. The data output will remain unaffected by this "$\overline{RAS}$-only" refresh.

$\overline{CAS}$ ONLY OPERATION

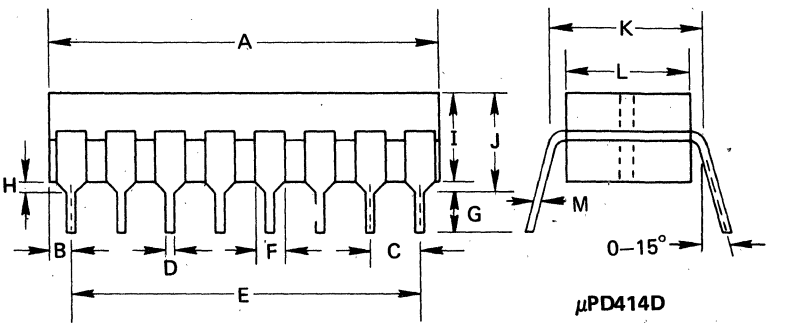
If $\overline{RAS}$ is decoded and applied only to the desired chips, the remaining chips will dissipate no power on the $\overline{CAS}$ edges. In addition, the outputs will assume the high impedance state regardless of chip select.

PACKAGE OUTLINE
μPD414C/D



μPD414C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



μPD414D
(Cerdip)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

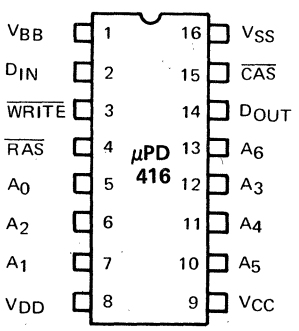
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, -5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 20 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	510 ns
μPD416-1	250 ns	430 ns	430 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	375 ns	375 ns

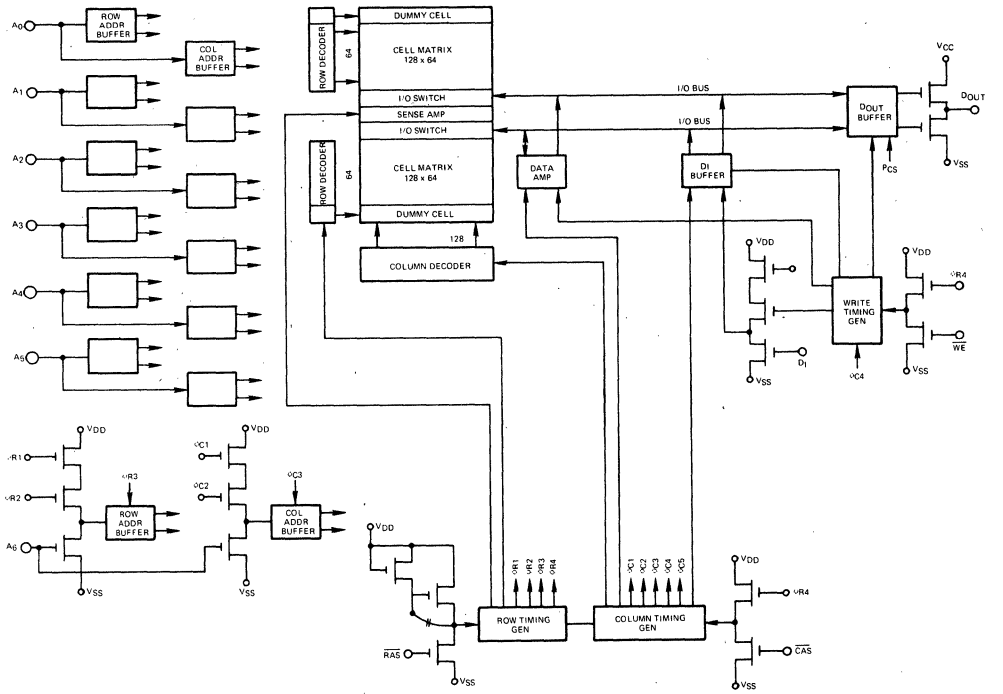
PIN CONFIGURATION



PIN NAMES

A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

DC CHARACTERISTICS

T_a = 0°C to +70°C ①, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	②
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	② ③
Supply Voltage	V_{SS}	0	0	0	V	②
Supply Voltage	V_{BB}	−4.5	−5.0	−5.5	V	②
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	②
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	V_{IH}	2.4		7.0	V	②
Input Low (Logic 0) Voltage, all inputs	V_{IL}	−1.0		0.8	V	②
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min. ④
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{DD} Current	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns ④
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns ④
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns ⑤
Standby V_{CC} Current	I_{CC2}	−10		10	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	−10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns ⑤
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	−10		10	μA	V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = -5 mA ③
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: ① T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

② All voltages referenced to V_{SS}.

③ Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

④ I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

⑤ I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. **At all other times I_{CC} consists of leakage currents only.**

DERATING CURVES

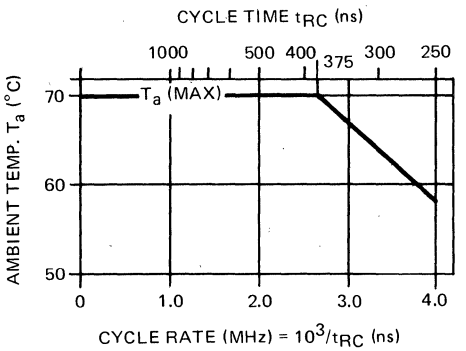


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz ($t_{CYC} < 375$ ns) is determined by T_a (max) [°C] = 70 - 9.0 x (cycle rate [MHz] -2.66).

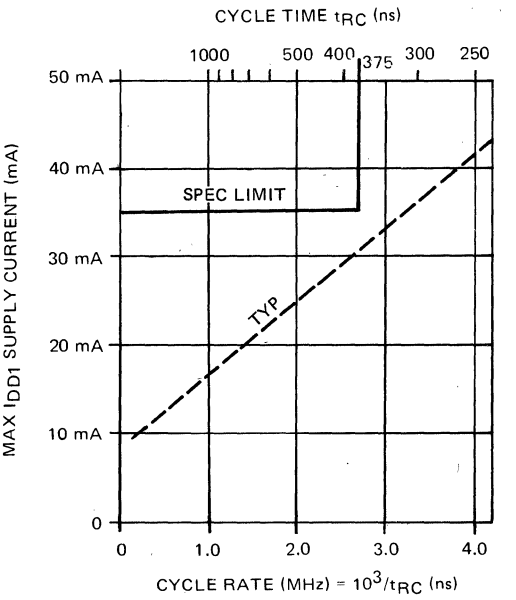


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

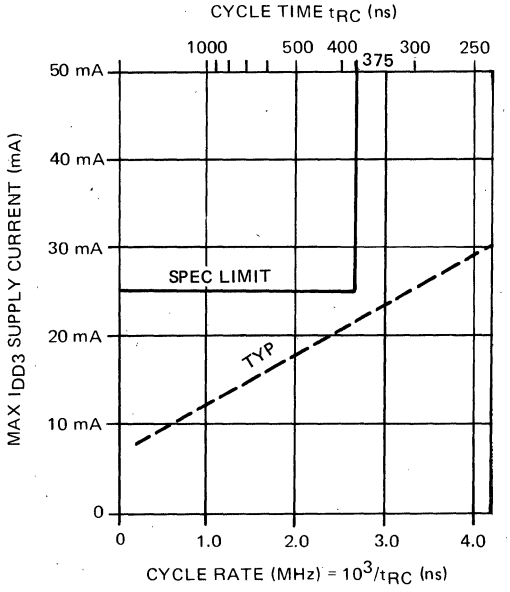


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

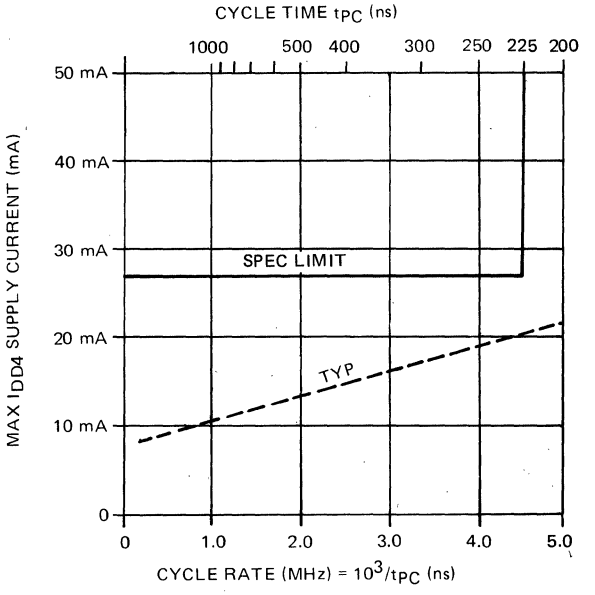


FIGURE 4

Maximum I_{DD4} versus cycle rate for device operation in page mode.

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS								UNIT	TEST CONDITIONS
		μPD416		μPD416-1		μPD416-2		μPD416-3			
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	510		430		375		375		ns	③
Read-write cycle time	t_{RWC}	510		430		375		375		ns	③
Page mode cycle time	t_{PC}	330		280		225		170		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		170		135		100	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	70	0	50	0	40	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		170		120		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	32,000	250	32,000	200	32,000	150	32,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		170		135		100		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	170	10,000	135	10,000	100	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		−20		−20		ns	
Row address set-up time	t_{ASR}	0		0		0		0		ns	
Row Address hold time	t_{RAH}	40		35		25		20		ns	
Column address set-up time	t_{ASC}	−10		−10		−10		−10		ns	
Column address hold time	t_{CAH}	90		75		55		45		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		ns	
Read command set-up time	t_{RCS}	0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		ns	
Write command pulse width	t_{WP}	90		75		55		45		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		100		80		60		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		100		80		60		ns	
Data-in set-up time	t_{DS}	0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		ns	
$\overline{CAS}$ precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		ns	
Refresh period	t_{REF}		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−10		−10		−10		−10		ns	
CAS to $\overline{WRITE}$ delay	t_{CWD}	140		120		95		70		ns	
RAS to $\overline{WRITE}$ delay	t_{RWD}	210		175		160		120		ns	

Notes:

(1) AC measurements assume t_T = 5 ns.

(2) V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

(3) The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.

(4) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.

(5) Assumes that $t_{RCD} \geq t_{RCD}$ (max).

(6) Measured with a load equivalent to 2 TTL loads and 100 pF.

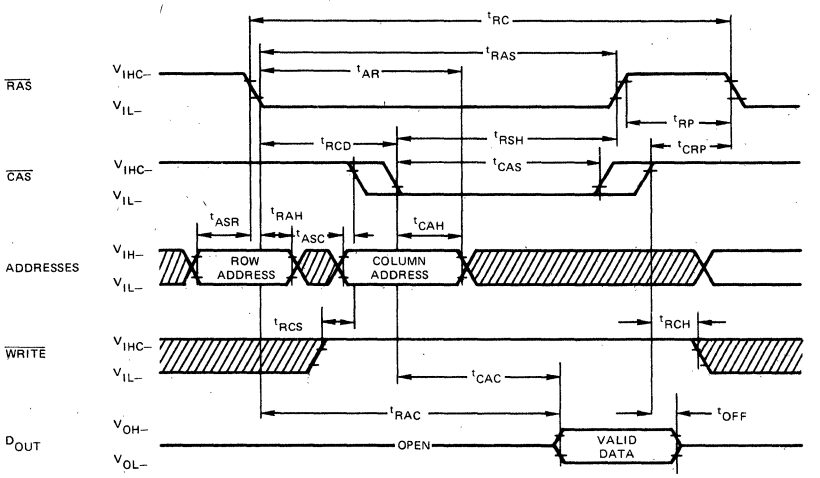
(7) t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

(8) Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

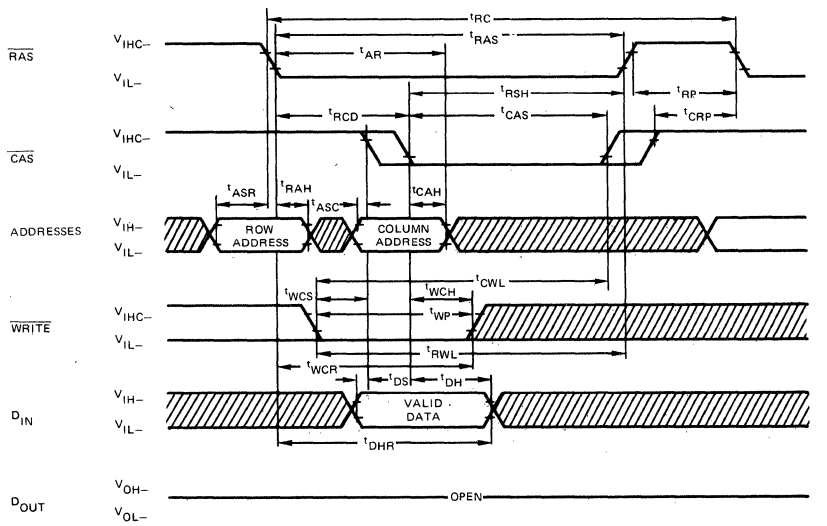
(9) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.

TIMING WAVEFORMS

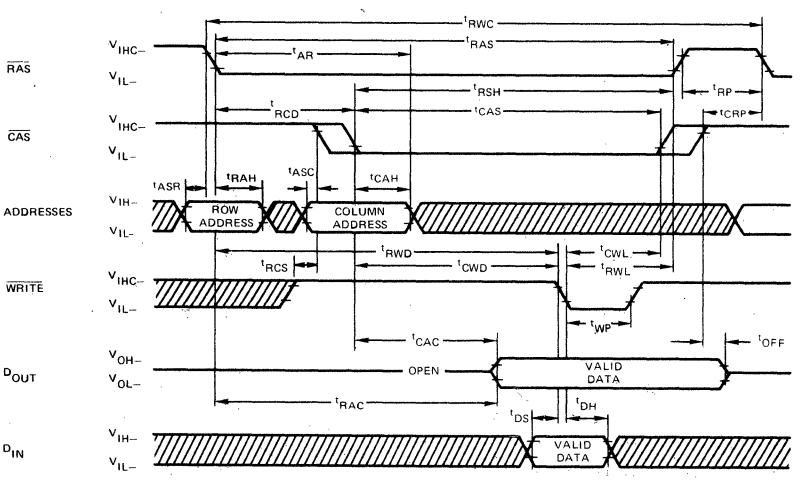
READ CYCLE



WRITE CYCLE

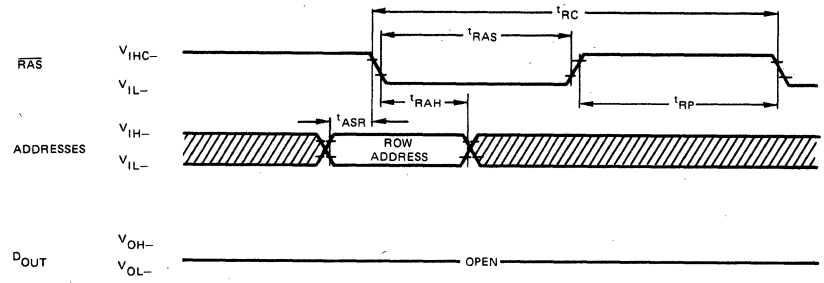


READ-WRITE/READ-MODIFY–WRITE CYCLE



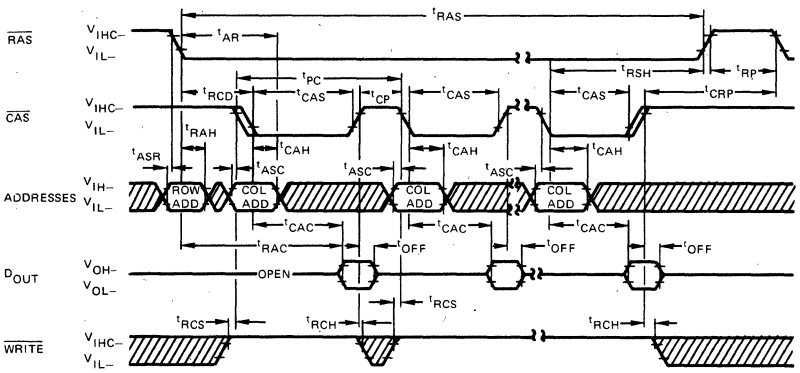
TIMING WAVEFORMS (CONT.)

"RAS-ONLY" REFRESH CYCLE

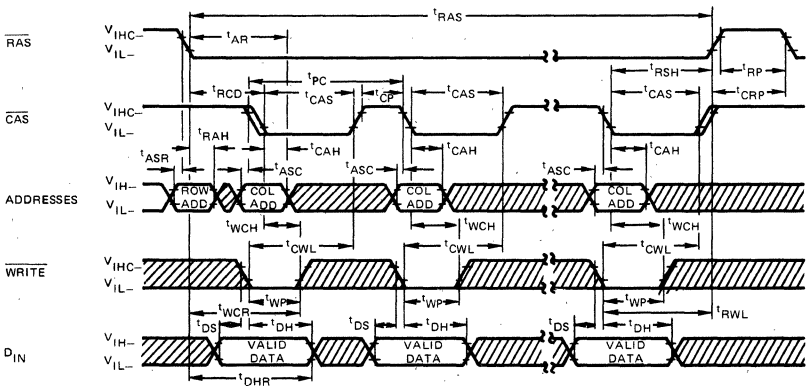


Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

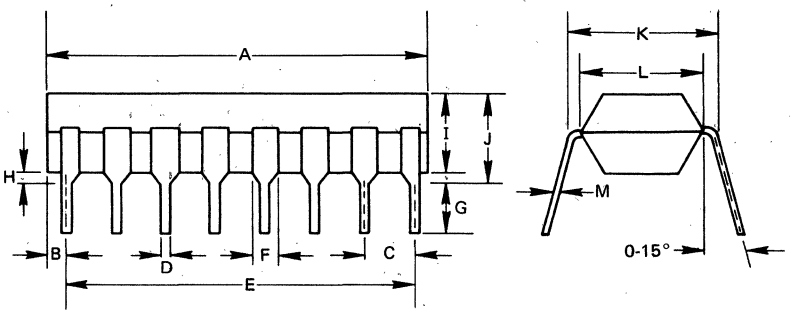
REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only" cycles can be used for simple refreshing operation.

CHIP SELECTION

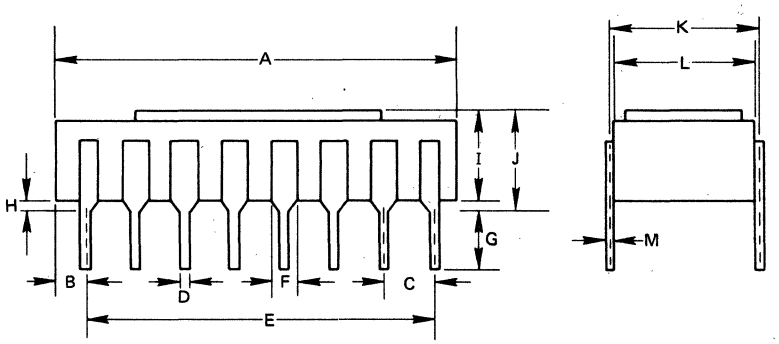
Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

PACKAGE OUTLINE
μPD416C/D



μPD416C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



μPD416D
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

4096 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD418 series is composed of high speed, dynamic, 4096 words x 1 bit, N channel, MOS, random access memories.

All inputs, except the clock (chip enable), are fully TTL compatible and require no pull-up resistors. The low capacitance of the address and control inputs precludes the need for specialized drivers. The data input and output are multiplexed to facilitate compatibility with a common bus system.

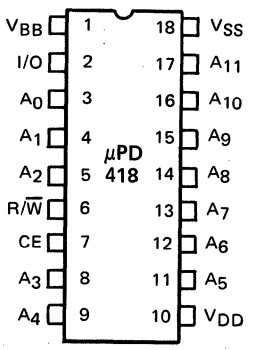
The μPD418 has only one clock (chip enable), to simplify system design. The low capacitance clock input requires a positive voltage (+12 volts) which can be driven by a variety of widely available drivers.

FEATURES

- 4096 words x 1 bit Organization
- High Memory Density – 18 Pin Cerdip and Plastic Package
- 10% Supply Margins
- Multiplexed Data Input/Output
- High Speed Access, Low Power Dissipation (370 mW Max)
- Full TTL Compatibility on All Inputs (except CE)
- Resistors for Address Inputs Provided on Chip
- Open Drain Output Buffer
- Single Low Capacitance Clock (CE)
- Power Supply +12V, –5V
- Replacement for TI's 4050 and Equivalent Devices
- 3 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	POWER (TYP)
μPD418D	300 ns	470 ns	650 ns	200 mW
μPD418D-1	250 ns	430 ns	610 ns	200 mW
μPD418D-2	200 ns	400 ns	580 ns	200 mW

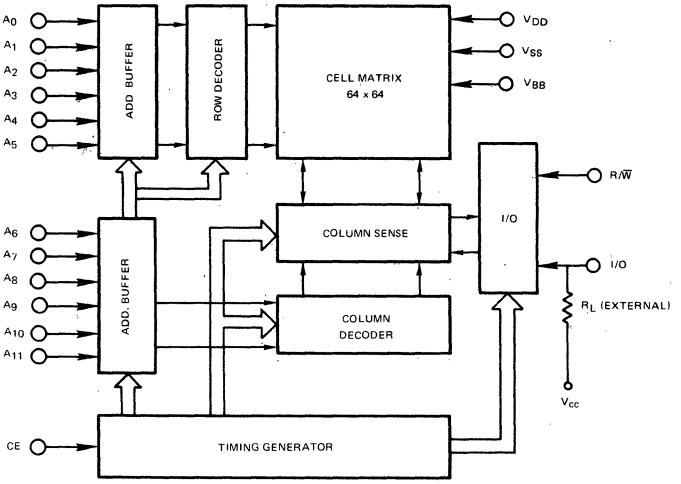
PIN CONFIGURATION



PIN NAMES

A_0-A_{11}	Address Input
A_0-A_5	Refresh Address
$R/\overline{W}$	Read/Write Control
I/O	Input/Output Terminal
CE	Chip Enable (Clock)
V_{DD}	Power Supply (+12V)
V_{BB}	Power Supply (–5V)
V_{SS}	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.3 to +25 Volts
All Input Voltages ①	−0.3 to +25 Volts
Supply Voltage V_{DD} ①	−0.3 to +25 Volts
Supply Voltage V_{SS} ①	−0.3 to +25 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%,① V_{SS} = 0V unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ②	LIMITS MAX	UNIT	TEST CONDITIONS
Input Current (All Inputs Except CE)	I_I			10	μA	V_I = −0.3V to 5.5V
CE Input Current	I_I(CE)			10	μA	V_I = −0.3V to 13.6V
Supply Current From V_{DD} Standby	I_{DD}(OFF)			200	μA	V_I(CE) = 0.6V
Supply Current From V_{DD}	I_{DD}(ON)		6	15	mA	V_I(CE) = 13.6V
Average Supply Current From V_{DD} During Read or Write Cycle	I_{DD}(av)		16	28	mA	Minimum Cycle Timing μPD418
			16	28		Minimum Cycle Timing μPD418-1
			16	28		Minimum Cycle Timing μPD418-2
Average Supply Current From V_{DD} During Read-Modify-Write Cycle	I_{DD}(av)			28	mA	Minimum Cycle Timing μPD418
				28		Minimum Cycle Timing μPD418-1
				28		Minimum Cycle Timing μPD418-2
Supply Current From V_{BB}	I_{BB}			100	μA	V_{BB} = −5.5V, V_{DD} = 13.2V, V_{SS} = 0V
High Level Output Voltage	V_{OH}	2.4		V_{CC}	V	t_a = Guaranteed max access time, R_L = 2.2 kΩ to 5.5V, C_L = 50pF, Load = 1 TTL Gate
Low Level Output Voltage	V_{OL}	V_{SS}		0.4	V	
Low Level Output Current	I_{OL}	5			mA	t_a = Guaranteed max access time, C_L = 50pF, V_{OL} = 0.4V
High Level Input Voltage (Except CE)	V_{IH}	2.2		5.5	V	
High Level CE Voltage	V_{IH}(CE)	V_{DD} − 1		V_{DD} + 1	V	
Low Level Input Voltage (Except CE)	V_{IL}	−0.6		0.6	V	
Low Level CE Voltage	V_{IL}(CE)	−0.6		0.6	V	

Notes: ① All voltages referenced to V_{SS}.
② Typical values are for T_a = 25°C and nominal power supply voltages.

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V + 10%, V_{SS} = 0V unless otherwise noted

PARAMETER	SYMBOL	LIMITS μPD418 MIN.	LIMITS μPD418 MAX.	LIMITS μPD418-1 MIN.	LIMITS μPD418-1 MAX.	LIMITS μPD418-2 MIN.	LIMITS μPD418-2 MAX.	UNIT	TEST CONDITIONS
Refresh Time	t_{ref}		2		2		2	ms	
Read Cycle Time	$t_C(rd)$	470		430		400		ns	
Pulse Width, CE High	$t_{W}(CEH)$	300	4000	260	4000	230	4000	ns	
Pulse Width, CE Low	$t_W(CEL)$	130		130		130		ns	
CE Rise Time	$t_r(CE)$		40		40		40	ns	
CE Fall Time	$t_f(CE)$		40		40		40	ns	
Address Setup Time	$t_{su}(ad)$	0		0		0		ns	
Read Setup Time	$t_{su}(rd)$	0		0		0		ns	
Address Hold Time	$t_h(ad)$	150		150		150		ns	
Read Hold Time	$t_h(rd)$	40		40		40		ns	
Access Time From Address	$t_a(ad)$		300		250		200	ns	C_L = 50pF, R_L = 2.2 kΩ to 5.5V Load = 1 TTL Gate, $t_r(CE)$ = 20 ns
Access Time From CE	$t_a(CE)$		280		230		180	ns	
Propagation Delay Time, Low to High Level Output From CE	t_{PLH}	40		40		40		ns	C_L = 50pF, R_L = 2.2 kΩ to 5.5V Load = 1 TTL Gate

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD418 MIN.	LIMITS μPD418 MAX.	LIMITS μPD418-1 MIN.	LIMITS μPD418-1 MAX.	LIMITS μPD418-2 MIN.	LIMITS μPD418-2 MAX.	UNIT	TEST CONDITIONS
Refresh Time	t_{ref}		2		2		2	ms	
Write Cycle Time	$t_C(wr)$	470		430		400		ns	
Pulse Width, CE High	$t_W(CEH)$	300	4000	260	4000	230	4000	ns	
Pulse Width, CE Low	$t_W(CEL)$	130		130		130		ns	
Write Pulse Width	$t_W(wr)$	180		180		180		ns	
CE Rise Time	$t_r(CE)$		40		40		40	ns	
CE Fall Time	$t_f(CE)$		40		40		40	ns	
Address Setup Time	$t_{su}(ad)$	0		0		0		ns	
Data Setup Time	$t_{su}(da)$	150		150		150		ns	
Write Pulse Setup Time	$t_{su}(wr)$	200		200		200		ns	
CE High to Write Delay Time ⑦ ⑧	$t_d(CEH\text{-}wr)$		40		40		40	ns	
Data Hold Time	$t_h(da)$	40		40		40		ns	
Address Hold Time	$t_h(ad)$	150		150		150		ns	
Write Hold Time ⑦ ⑧	$t_h(wr)$		40		40		40	ns	

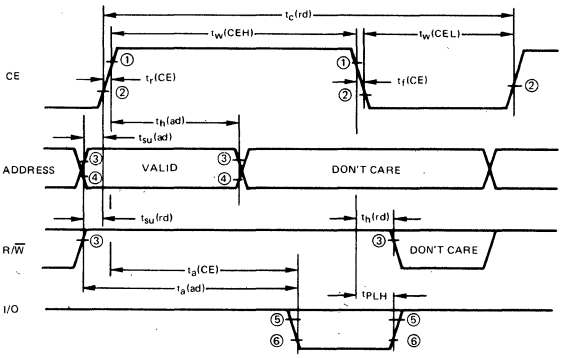
READ-MODIFY-WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V unless otherwise noted.

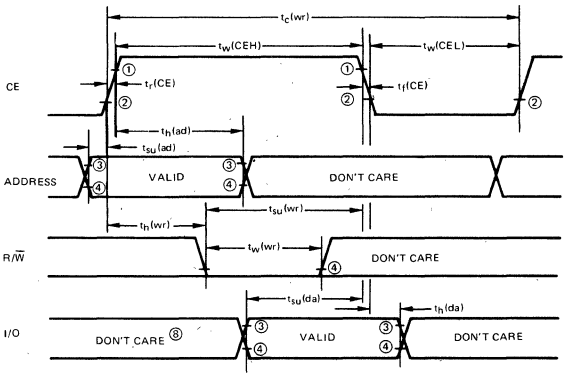
PARAMETER	SYMBOL	LIMITS μPD418 MIN.	LIMITS μPD418 MAX.	LIMITS μPD418-1 MIN.	LIMITS μPD418-1 MAX.	LIMITS μPD418-2 MIN.	LIMITS μPD418-2 MAX.	UNIT	TEST CONDITIONS
Refresh Time	t_{ref}		2		2		2	ms	
Read Modify Write Cycle Time	$t_C(RMW)$	650		610		580		ns	
Pulse Width, CE High	$t_W(CEH)$	480	4000	440	4000	410	4000	ns	
Pulse Width, CE Low	$t_W(CEL)$	130		130		130		ns	
Write Pulse Width	$t_W(wr)$	180		180		180		ns	
CE Rise Time	$t_r(CE)$		40		40		40	ns	
CE Fall Time	$t_f(CE)$		40		40		40	ns	
Write Pulse Setup Time	$t_{su}(wr)$	200		200		200		ns	
Address Setup Time	$t_{su}(ad)$	0		0		0		ns	
Read Pulse Setup Time	$t_{su}(rd)$	0		0		0		ns	
Data Setup Time	$t_{su}(da)$	150		150		150		ns	
Data Hold Time	$t_h(da)$	40		40		40		ns	
Address Hold Time	$t_h(ad)$	150		150		150		ns	
Access Time From Address	$t_a(ad)$		300		250		200	ns	C_L = 50pF, R_L = 2.2 kΩ to 5.5V Load = 1 TTL Gate, $t_r(CE)$ = 20 ns
Access Time From CE	$t_a(CE)$		280		230		180	ns	C_L = 50pF, R_L = 2.2 kΩ to 5.5V Load = 1 TTL Gate

TIMING WAVEFORMS

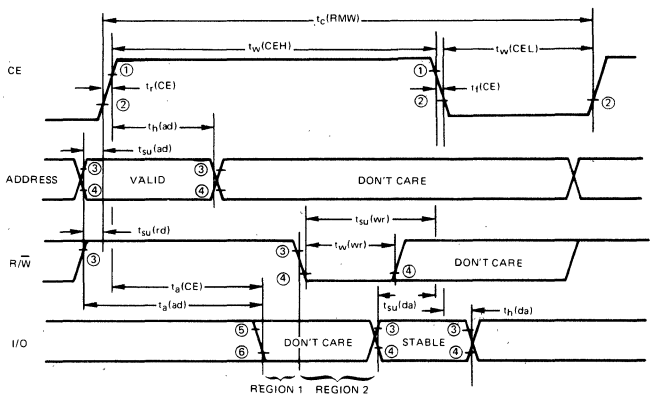
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① V_{DD} − 2V is the reference level for measuring timing of CE.
② V_{SS} + 2V is the reference level for measuring timing of CE.
③ V_{IH} MIN. is the reference level for measuring timing of addresses, R/$\overline{W}$, I/O (Write cycle).
④ V_{IL} MAX. is the reference level for measuring timing of addresses, R/$\overline{W}$, I/O (Write cycle).
⑤ V_{OH} MIN. is the reference level for measuring timing of I/O (Read cycle).
⑥ V_{OL} MAX. is the reference level for measuring timing of I/O (Read cycle).
⑦ During the time from the rise of CE to the fall of R/$\overline{W}$, R/$\overline{W}$ is permitted to change from high to low only.
⑧ If R/$\overline{W}$ remains high more than t_h(wr) from CE goes to high, the Data in driver must be disabled until R/$\overline{W}$ goes to low. (See Note 9.)
⑨ In region 1, Data out is valid until the I/O terminal is forced high or low by the data in driver. A transition from low to high is permissible but additional power to overcome the output buffer will be required. A transition from high to low is permitted without power penalty. In region 2, during the time from the fall of R/$\overline{W}$ to (t_f(R/$\overline{W}$) + 50 ns, MAX.), a transition from low to high permissible but additional power to overcome the output buffer will be required.

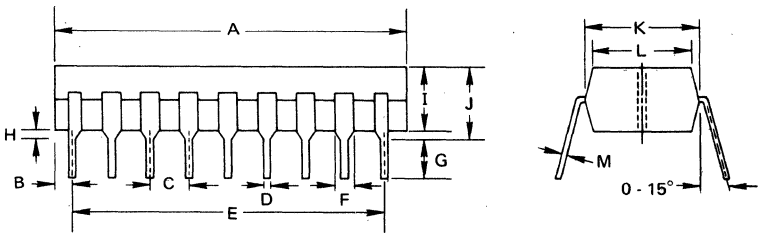
CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%①
V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance Address Inputs	C_I(ad)		3.5	6	pF	V_I = 0V
Input Capacitance CE Input	C_I(CE)		13	18	pF	V_I(CE) = 12V
			13	18		V_I(CE) = 0V
Input Capacitance R/$\overline{W}$ Input	C_I(R/$\overline{W}$)		4.5	6	pF	V_I = 0V
I/O Terminal Capacitance	C_I(I/O)		5	7	pF	V_I = 0V

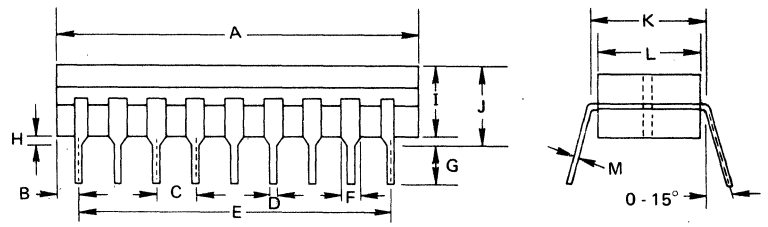
Note: ① All voltages referenced to V_{SS}.

PACKAGE OUTLINE μPD418C/D



μPD418C (Plastic)

ITEM	MILLIMETERS	INCHES
A	22.5 MAX.	0.89
B	1.09	0.04
C	2.54	0.10
D	0.50 ± 0.10	0.02
E	20.32	0.80
F	1.2 MIN.	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

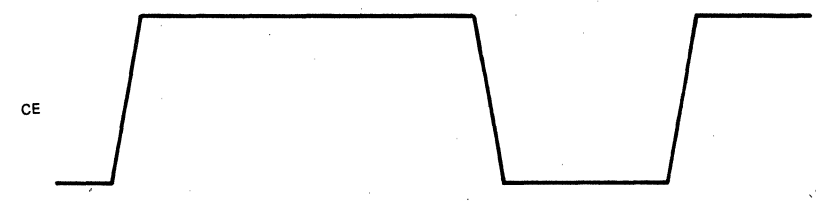


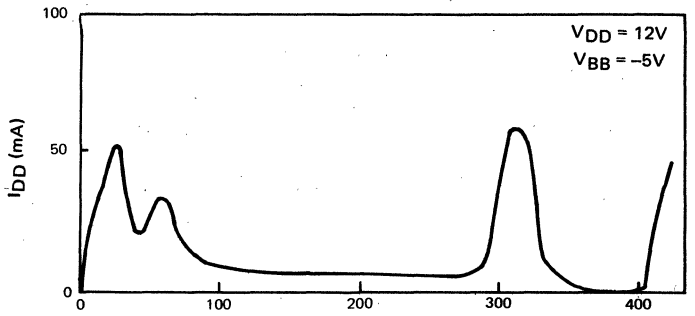
μPD418D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

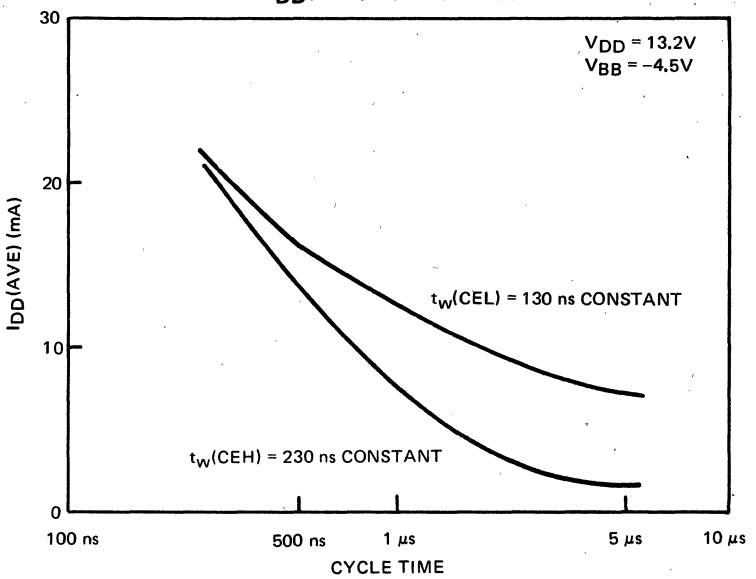
I_{DD} CHARACTERISTICS

I_{DD} WAVEFORM





I_{DD}(AVE) VS CYCLE TIME



1024-BIT BIPOLAR TTL RAM

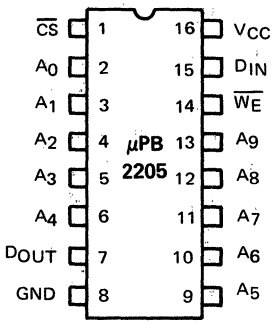
DESCRIPTION

The NEC μPB2205 integrated circuits are high-speed Open-Collector TTL interface, 1024-bit Random Access Memories.

FEATURES

- 1024 Words x 1 Bit Organization (Fully Decoded)
- TTL Interface
- Fast Access Time – 50 ns max.
- Power Consumption – 500 mW typ.
- A Chip Select Input for Memory Expansion
- Open-Collector Output
- Ceramic 16-Lead Dual-In-Line Package
- Compatibility with Fairchild's "93415" and Equivalent Devices

PIN CONFIGURATION

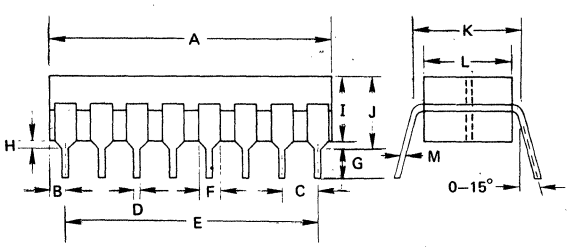


FUNCTION TABLE

CHIP SELECT	WRITE ENABLE	OPERATION	OUTPUT
0	0	WRITE	1
0	1	READ	Non-Inverted Data Written in Memory
1	X	HOLD	1

X – High or Low.

PACKAGE OUTLINE μPB2205D



ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	$0.46^{+0.10}_{-0.05}$	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-25°C to +75°C
Storage Temperature	-65°C to +150°C
Output Voltage	-0.5 to +5.5 Volts
Input Voltage	-0.5 to +5.5 Volts
Supply Voltage V_{CC}	-0.5 to +7 Volts
Output Current	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 75°C; V_{CC} = 4.75 to 5.25V ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.40	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.50	V	I_{OL} = 16 mA
Output High Current	I_{OH}			100	μA	V_{OH} = 5.25V
Input Clamp Voltage	$-V_{IC}$			1.3	V	$-I_I$ = 12 mA
Power Supply Current	I_{CC}		100	155	mA	All input except W_E grounded.

Note: ① Guaranteed with transverse airflow exceeding 400 linear F.P.M. and two minute warm-up.

Typical thermal resistance values of the package are:

θ_{JA} (Junction to Ambient) = 50° C/W (at 400 F.P.M. airflow)

θ_{JA} (Junction to Ambient) = 70° C/W (Free Air)

Under free air condition, ambient temperature is guaranteed 0°C to 65°C.

AC CHARACTERISTICS

T_a = 0°C to 75°C; V_{CC} = 4.75 to 5.25V

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
Read Access Time	Address Access	t_{AA}	10		50	ns
	$\overline{CS}$ Access	t_{ACS}	5		30	ns
	$\overline{CS}$ Recovery	t_{RCS}			30	ns
Write Pulse Width Time		t_W			60	ns
Write Set-Up Time	Address Set-Up	t_{WSA}	25			ns
	Data-In Set-Up	t_{WSD}	5			ns
	$\overline{CS}$ Set-Up	t_{WSCS}	5			ns
Write Hold Time	Address Hold	t_{WHA}	5			ns
	Data-In Hold	t_{WHD}	5			ns
	$\overline{CS}$ Hold	t_{WHCS}	5			ns
Write Disable Time		t_{WD}			40	ns
Write Recovery Time		t_{WR}			40	ns

Notes: ① Output Load – Fig. 1. Capacitances C_L in Fig. 1 including jig and scope.

② Input Waveform – 0V for "0" level and 3.0V for "1" level, less than 10 ns for both rise and fall time.

③ Measurement Reference – 1.5V for both inputs and output.

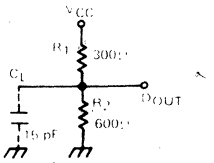
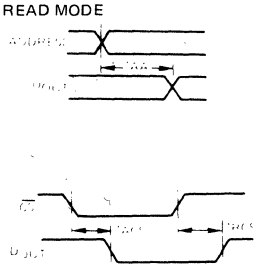


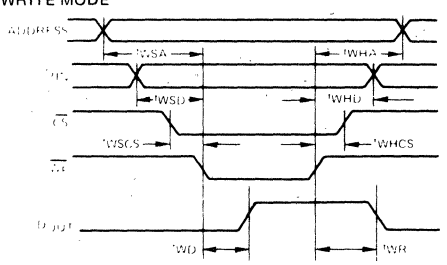
Figure 1

TIMING WAVEFORMS

READ MODE



WRITE MODE



4096 BIT HIGH SPEED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD410 is a very high speed 4K bit static random access memory. It is organized as 4096 words by 1 bit per word and fabricated using N channel silicon gate MOS technology.

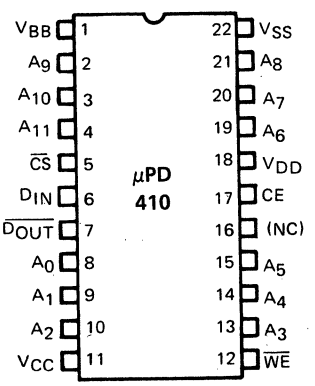
All signals to the device are TTL compatible except for Chip Enable which is standard +12 Volt MOS level.

Circuit operation starts with the rising edge of CE. Data is latched and valid until falling edge of CE. Address and Chip Select signals are latched on-chip to simplify system timing requirements.

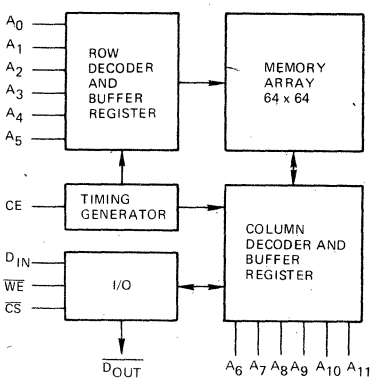
FEATURES

- 4096 Words x 1 Bit Organization
- Fully Decoded
- TTL Compatible (except CE)
- High Speed-Access Time: 100 ns max.
- Cycle Time: 220 ns min.
- Static Operation — No Refresh Required
- Standby Power: 75 mW max.
- Active Power: 470 mW typ.
- Supply Voltages: V_{DD} = +12V, V_{CC} = +5V, V_{BB} = -5V
- Address Registers on the Chip
- Three State Output
- Standard 22 Pin Ceramic Dual-in-Line Package
- Pin Compatible with μPD411 and Other 4K Dynamic RAMs

PIN CONFIGURATION



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.3 to +20 Volts①
All Input Voltages	-0.3 to +20 Volts①
Supply Voltage V_{DD}	-0.3 to +20 Volts①
Supply Voltage V_{CC}	-0.3 to +20 Volts①
Supply Voltage V_{SS}	-0.3 to +20 Volts①
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

*T_a = 25°C

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ±5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}			10	μA	V_{IN} = V_{IL}MIN to V_{IH} MAX
CE Input Leakage Current	I_{LC}			10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current	I_{LO}			10	μA	$\overline{CE}$ = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DDOFF}			200	μA	CE = -1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DDON}			60	mA	CE = V_{IHC}
Average V_{DD} Current	I_{DDAV}			60	mA	Cycle Time = min
V_{BB} Supply Current	I_{BB}			100	μA	
V_{CC} Supply Current during CE off	I_{CCOFF}			15	mA	$\overline{CE}$ = V_{ILC} or $\overline{CS}$ = V_{IH}
Average V_{CC} Current	I_{CCAV}			21	mA	D_{OUT} = No load
Input Low Voltage	V_{IL}	-1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	-1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}-1		V_{DD}+1	V	
Output Low Voltage	V_{OL}	0		0.4	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = 2.0 mA

Note: ① Typical values are for T_a = 25°C and nominal supply voltages.

CAPACITANCE

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

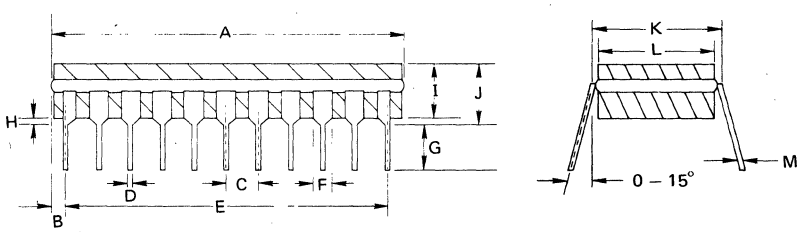
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}		4	6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}		4	6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}		5	7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}		8	10	pf	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pf	V_{IN} = V_{SS}

AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = −5V ± 5%; V_{SS} = 0V (410-2: T_a = 0°C to 55°C)

PARAMETER	SYMBOL	LIMITS									UNIT	TEST CONDITIONS
		410			410-1			410-2				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
READ, WRITE AND READ-MODIFY-WRITE												
Address to CE Set Up Time	t_{AC}	0			0			0			ns	
Address Hold Time	t_{AH}	90			70			50			ns	
CE Off Time	t_{CC}	190			140			90			ns	
CE Transition Time	t_T	0		40	0		40	0		40	ns	
CE off to Output High Impedance State	t_{CF}	0		90	0		90	0		90	ns	
READ												
Cycle Time	t_{CY}	440			330			220			ns	t_T = 10 ns
CE on Time	t_{CE}	230		2000	170		2000	110		2000	ns	
CE Output Delay	t_{CO}			190			140			90	ns	Load = 50 pF + ITTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}			200			150			100	ns	$t_{ACC} = t_{AC} + t_{CO} + t_T$
CE to $\overline{WE}$	t_{WL}	20			20			20			ns	
$\overline{WE}$ to CE on	t_{WC}	0			0			0			ns	
WRITE												
Cycle Time	t_{CY}	440			330			220			ns	t_T = 10 ns
CE on Time	t_{CE}	230		2000	170		2000	110		2000	ns	
$\overline{WE}$ to CE off	t_W	130			100			70			ns	
CE to $\overline{WE}$	t_{CW}	130			100			70			ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0			0			0			ns	
D_{IN} Hold Time	t_{DH}	60			40			20			ns	
$\overline{WE}$ Pulse Width	t_{WP}	130			100			70			ns	
READ-MODIFY-WRITE												
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	560			420			280			ns	t_T = 10 ns
CE Width During RMW	t_{CRW}	350		2000	260		2000	170		2000	ns	
$\overline{WE}$ to CE on	t_{WC}	0			0			0			ns	
$\overline{WE}$ to CE off	t_W	130			100			70			ns	
$\overline{WE}$ Pulse Width	t_{WP}	130			100			70			ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0			0			0			ns	
D_{IN} Hold Time	t_{DH}	60			40			20			ns	
CE to Output Delay	t_{CO}			190			140			90	ns	Load = 50 pF + ITTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}			200			150			100	ns	$t_{ACC} = t_{AC} + t_{CO} + t_T$

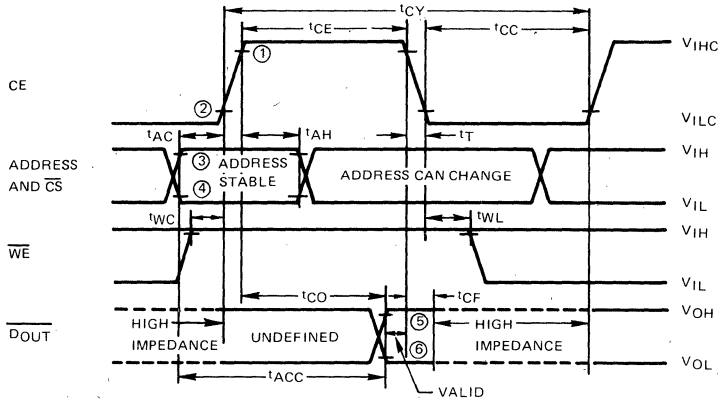
PACKAGE OUTLINE μPD410D



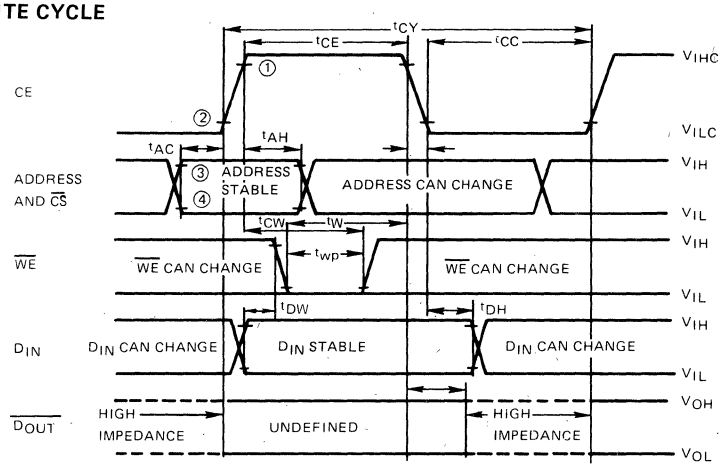
ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

TIMING WAVEFORMS

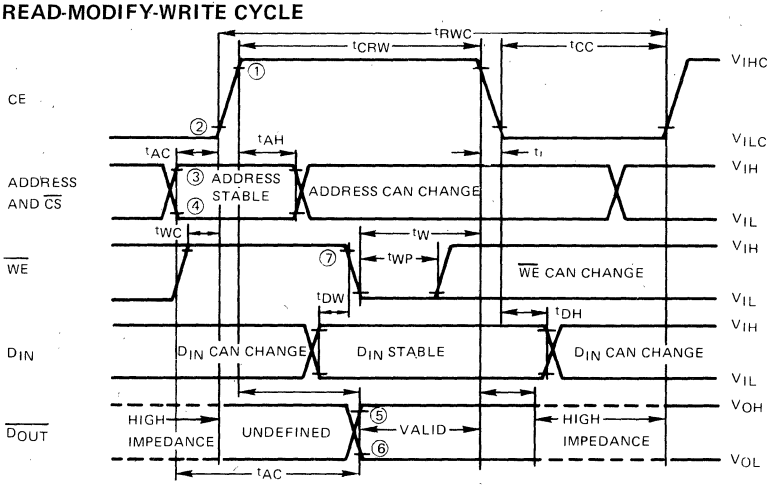
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:
① V_{DD} − 2V is the reference level for measuring timing of CE.
② V_{SS} + 2V is the reference level for measuring timing of CE.
③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑤ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑥ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑦ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

μPD2101AL
μPD2101AL-2
μPD2101AL-4

1024 BIT (256 X 4) STATIC MOS RAM WITH SEPARATE I/O

DESCRIPTION

The μPD2101ALC is a 256 word by 4 bit static random access memory requiring no clocks or refreshing. It features high speed, low cost, and simplicity of interfacing.

It is directly TTL compatible in all respects; inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bidirectional logic in a common I/O system. Output data is the same polarity as input data, and readout is non-destructive.

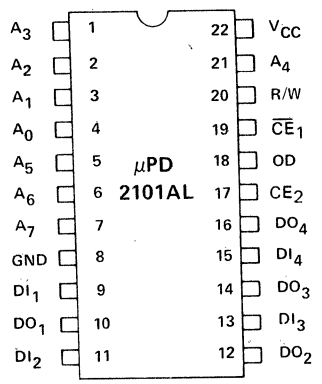
The μPD2101ALC family of devices offers access times from 450 ns to 250 ns with a typical standby mode power dissipation of only 36 mW.

The use of NEC's N-channel silicon gate MOS process, with its excellent protection from contamination, permits the use of a low cost 22 pin plastic package in providing a high performance, high reliability MOS circuit at a most cost effective price level. The μPD2101ALC is pin-compatible with the μPD5101C CMOS static RAM.

FEATURES

- 256 x 4 Organizations to Meet Needs for Small System Memories
- Access Time – 250 to 450 nsec max
- Directly TTL Compatible – All Inputs and Output
- Static MOS – No Clocks or Refreshing Required
- Simple Memory Expansion – Chip Enable Input
- Low Standby Power – 36 mW typ.
- Low Cost Packaging – 22 Pin Plastic Dual-In-Line Configuration
- Low Operating Power
- Three-State Output – OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

PIN CONFIGURATION



PIN NAMES

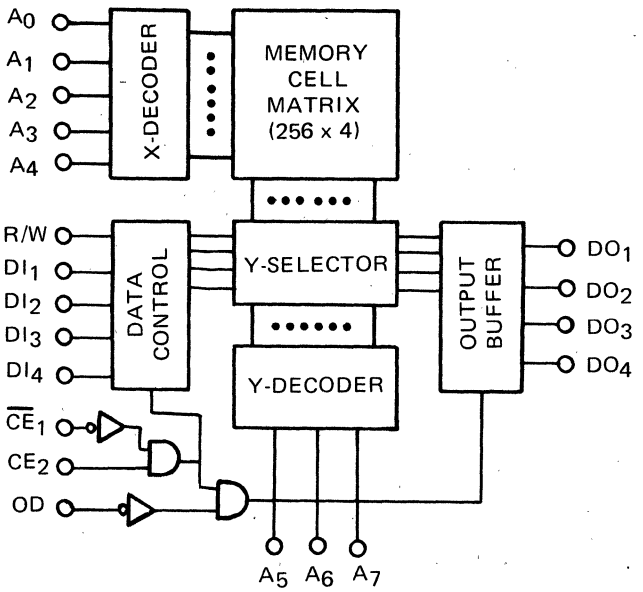
DI_1–DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0–A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1–DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

OPERATION MODES

$\overline{CE}_1$	CE_2	OD	CHIP	OUTPUT MODE
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			No-Selected	

μPD2101AL

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+10	μA	V_O = +2.4V to V_{CC} $\overline{CE}_1$ = +2.0V
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = +0.4V $\overline{CE}_1$ = +2.0V
Power Supply Current	I_{CC1}			+60	mA	V_I = +5.25V I_O = 0 mA T_a = +25°C
Power Supply Current	I_{CC2}			+70	mA	V_I = +5.25V I_O = 0 mA T_a = −10°C to +70°C

AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			180			150			130	ns
Output Disable to Output	t_{OD}			150			130			120	ns
Data Output to High Z State	t_{DF}*	0		130	0		115	0		100	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

*t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.

WRITE CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Write Cycle Time	t_{WC}	450			350			250			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	180			150			130			ns
Data Setup Time	t_{DW}	180			150			130			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	160			130			120			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			10			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY CHARACTERISTICS

$T_a = -10°C$ to $+70°C$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP①	MAX.		
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby	V_{CES}	2.0			V	$2.0V \leq V_{PD} \leq 5.25V$
		V_{PD}			V	$1.5V \leq V_{PD} < 2.0V$
Standby Current Drain	I_{PD1}		24	36	mA	All Inputs = $V_{PD1} = 1.5V$
Standby Current Drain	I_{PD2}		30	45	mA	All Inputs = $V_{PD2} = 2.0V$
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC}②			ns	

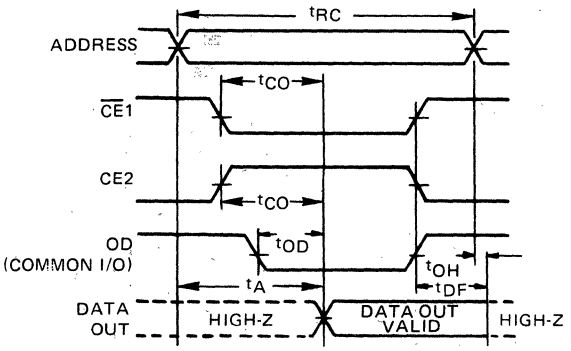
Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage.
② $t_R = t_{RC}$ (Read Cycle Time).

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			8	pf	$V_I = 0V$
Output Capacitance	C_{OUT}			12	pf	$V_O = 0V$

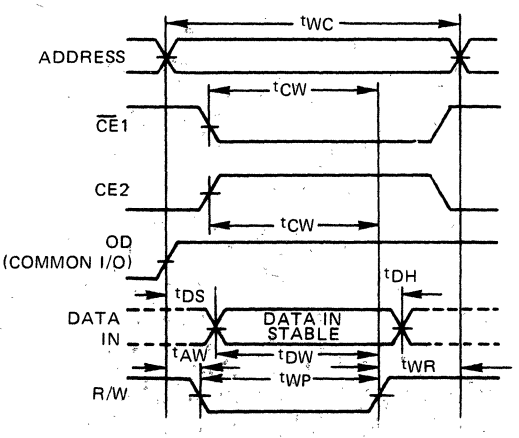
TIMING WAVEFORMS

READ CYCLE



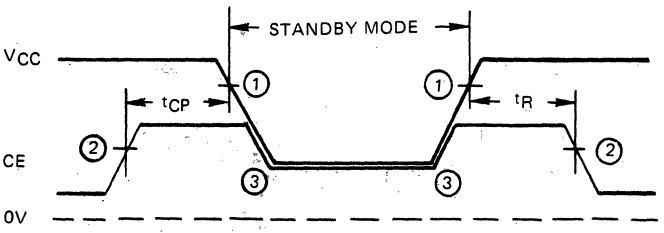
Notes: (1) OD should be tied low for separate I/O operation.
(2) R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



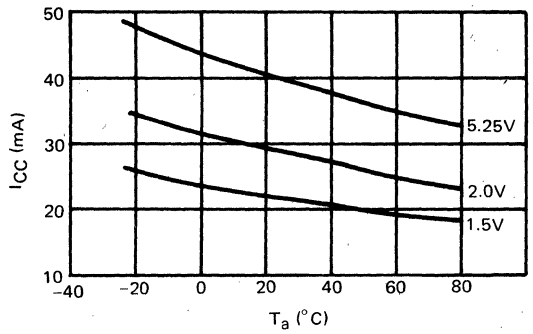
Notes: (1) 4.75V
(2) 2.0V
(3) 1.5V

AC CONDITIONS OF TEST

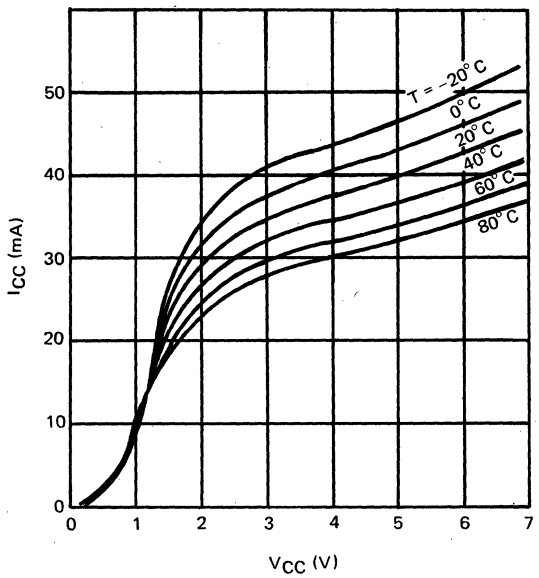
Input Pulse Levels	+0.8V to +2.0V
Input Pulse Rise and Fall Times	20 ns
Timing Measurement Reference Level	1.5V
Output Load	1 TTL + 100 pF

TYPICAL OPERATING CHARACTERISTICS

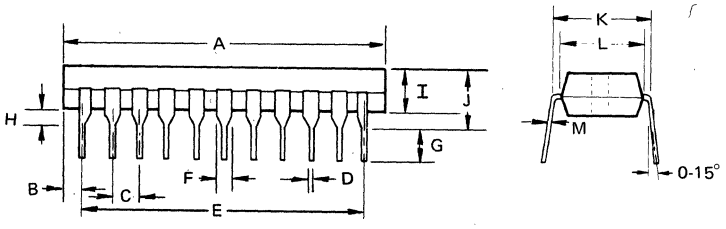
I_{CC} VS T_a



I_{CC} VS V_{CC}



PACKAGE OUTLINE μPD2101ALC



ITEM	MILLIMETERS	INCHES
A	28.0 MAX.	1.10 MAX.
B	1.4 MAX	0.025
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.7 MAX.	0.18 MAX.
J	5.2 MAX.	0.20 MAX.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

μPD2102AL
μPD2102AL-2
μPD2102AL-4

1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD2102AL is a 1024 words by one bit static Random Access Memory requiring no clocks or refreshing. A family of devices with maximum access times ranging from 250 ns to 450 ns meet the requirements of microcomputer memory applications where speed, low cost and easy interfacing are prime design objectives.

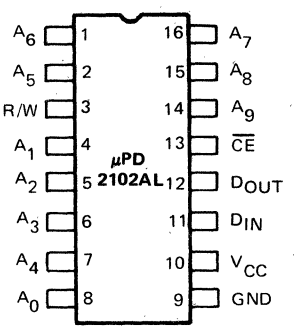
All μPD2102AL inputs and outputs are TTL compatible. A single chip-enable ($\overline{CE}$) pin is provided for selection of an individual device in systems with OR-tied outputs. Output data is the same polarity as input data and is nondestructively read out. Only a single +5 volt supply is required. In standby mode, with the supply lowered to 1.5 volts, power dissipation is reduced to 42 mW max.

The μPD2102AL family is fabricated using NEC's N-channel MOS silicon gate process, providing excellent contamination protection. This process permits the use of a low cost plastic package (16 pin) and enables high performance, highly reliable MOS circuits to be produced.

FEATURES

- Access Time – μPD2102AL-2 – 250 ns Max
  μPD2102AL – 350 ns Max
  μPD2102AL-4 – 450 ns Max
- Single +5 Volts Supply Voltage
- Directly TTL Compatible – All Inputs and Output
- Static MOS – No Clocks or Refreshing Required
- Low Power – Typically 150 mW
- Low Standby Power – 42 mW max
- Three-State Output – OR-TIE Capability
- Simple Memory Expansion – Chip Enable Input
- Fully Decoded – On Chip Address Decode
- Inputs Protected – All Inputs have Protection against Static Charge
- Low Cost Packaging – 16 Pin Plastic Dual-In-Line Configuration

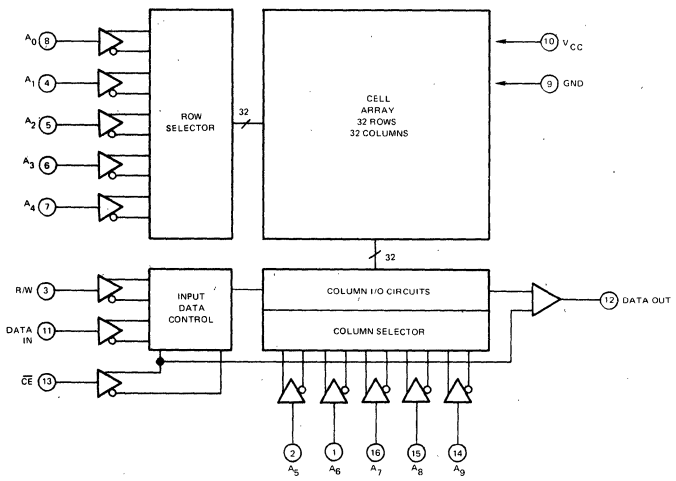
PIN CONFIGURATION



PIN NAMES

$A_0 - A_9$	Address Inputs
R/W	Read/Write
$\overline{CE}$	Chip Enable
V_{CC}	Power (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -10°C to 70°C
Storage Temperature . . . . . -65°C to +125°C
Voltage On Any Pin . . . . . -0.5 to +7 Volts ①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10°C to +70°C; V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP ①	MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}			±10	μA	V_{IN} = 0 to 5.25V
I/O Leakage Current	I_{LOH}			+5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = +2.4V to V_{CC}
I/O Leakage Current	I_{LOL}			-10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
Power Supply Current	I_{CC1}		30	70	mA	All Inputs = 5.25V, Data Out Open
Input "Low" Voltage	V_{IL}	-0.5		+0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC}	V	
Output "Low" Voltage	V_{OL}			+0.4	V	I_{OL} = 2.1 mA
Output "High"	V_{OH}	2.4			V	I_{OH} = -100 μA

Note: ① Typical values are for T_a = 25°C and nominal supply voltage

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		3	5	pf	V_{IN} = 0V
Output Capacitance	C_{OUT}		7	10	pf	V_{OUT} = 0V

AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V$ ±5% unless otherwise noted

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		2102AL-4		2102AL		2102AL-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle	t_{RC}	450		350		250		ns	$t_T = t_r = t_f = 100$ ns $C_L = 100$ pF Load = 1 TTL Gate $V_{ref} = 2.0$ or 0.8V
Access Time	t_A		450		350		250	ns	
Chip Enable to Output Time	t_{CO}		230		180		130	ns	
Previous Read Data Valid in Respect to Address	t_{OH1}	40		40		40		ns	
Previous Read Data Valid in Respect to Chip Enable	t_{OH2}	0		0		0		ns	

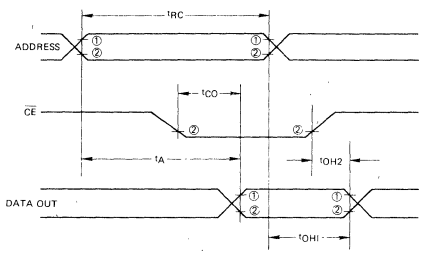
WRITE CYCLE

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise noted

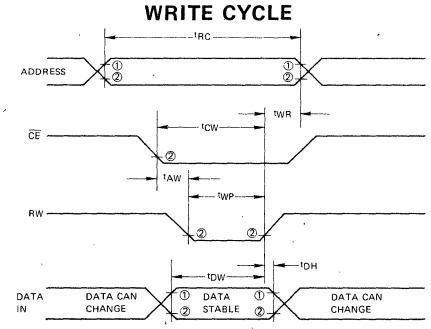
PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		2102AL-4		2102AL		2102AL-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Write Cycle	t_{WC}	450		350		250		ns	$t_T = t_r = t_f = 100$ ns $C_L = 100$ pF Load = 1 TTL Gate $V_{ref} = 2.0$ or 0.8V
Address to Write Setup Time	t_{AW}	20		20		20		ns	
Write Pulse Width	t_{WP}	300		250		180		ns	
Write Recovery Time	t_{WR}	0		0		0		ns	
Data Setup Time	t_{DW}	300		250		180		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
Chip Enable to Write Setup Time	t_{CW}	300		250		180		ns	

TIMING WAVEFORMS

READ CYCLE



WRITE CYCLE



Notes. ① 2.0 Volts
② 0.8 Volts

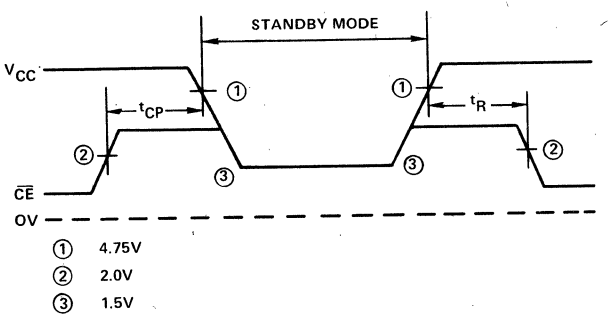
STANDBY CHARACTERISTICS

$T_a = 0$ to $+70°C$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}$ Bias in Standby	V_{CES}	2.0			V	$+2.0V \leq V_{PD} \leq +5.25V$
		V_{PD}			V	$+1.5V \leq V_{PD} < +2.0V$
Standby Current Drain	I_{PD1}		14	28	mA	All Inputs, $V_{PD1} = +1.5$
Standby Current Drain	I_{PD2}		18	38	mA	All Inputs, $V_{PD2} = +2.0V$
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC} ①			ns	

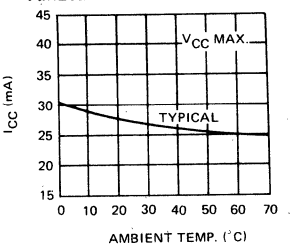
① t_{RC} = Read Cycle Time

STANDBY MODE TIMING WAVEFORM

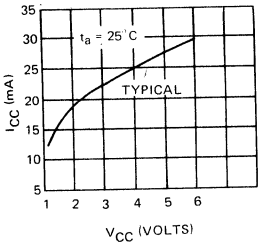


TYPICAL CHARACTERISTICS

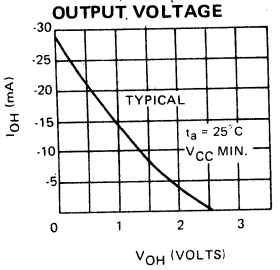
POWER SUPPLY CURRENT VS AMBIENT TEMPERATURE



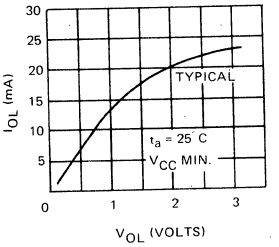
POWER SUPPLY CURRENT VS SUPPLY VOLTAGE



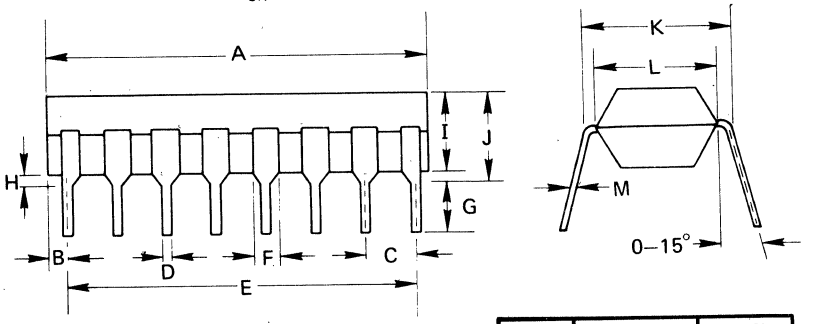
OUTPUT SOURCE CURRENT VS OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS OUTPUT VOLTAGE



PACKAGE OUTLINE μPD2102ALC



ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.02 MIN
I	4.05 MAX	0.16 MAX
J	4.55 MAX	0.18 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

μPD2111AL
μPD2111AL-2
μPD2111AL-4

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

DESCRIPTION

The μPD2111AL is a 256 words by 4 bits static random access memory fabricated with N-channel MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

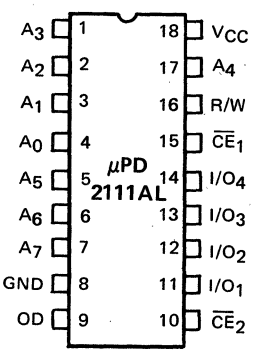
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

All members in the μPD2111AL family feature a low standby power mode with the supply voltage being reduced to +1.5V.

FEATURES

- 256 Words x 4 Bits Organization
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Static MOS – No Clocks or Refreshing Required
- Access Time – 250 ns to 450 ns max.
- Simple Memory Expansion – Chip Enable Inputs
- Fully Decoded – On Chip Address Decode
- Inputs Protected – All Inputs have Protection Against Static Charge
- Low Cost Packaging – 18 Pin Plastic Dual-In-Line Configuration
- Three-State Output – OR-Tie Capability
- Low Standby Power

PIN CONFIGURATION



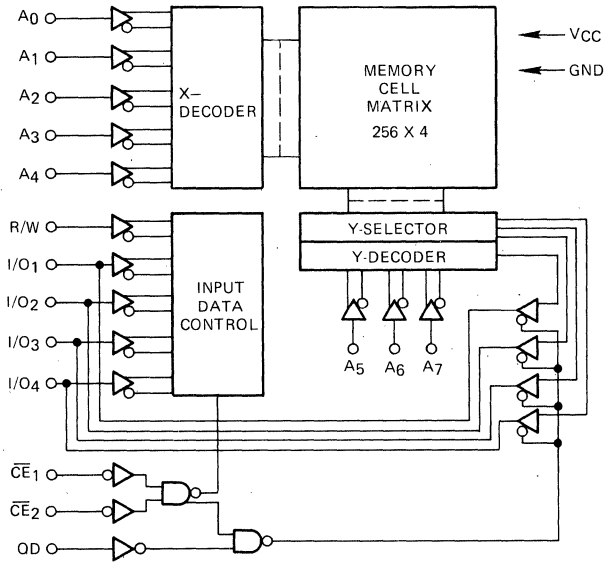
PIN NAMES

$A_0 - A_7$	Address Inputs
OD	Output Disable
R/W	Read/Write Input
$\overline{CE}_1$	Chip Enable 1
$\overline{CE}_2$	Chip Enable 2
$I/O_1 - I/O_4$	Data Input/Output

OPERATION MODES

$\overline{CE}_1$	$\overline{CE}_2$	OD	Chip Output Status	
0	0	0	Selected	Data Output
0	0	1		High Z
Others			Unselected	State

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10 to +70° C; V_{CC} = +5V ± 5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage		V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage		V_{IL}	−0.5		+0.8	V	
Output High Voltage	2111AL-4	V_{OH}	+2.4			V	I_{OH} = −150 μA
	2111AL 2111AL-2		+2.4			V	I_{OH} = −200 μA
Output Low Voltage		V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High		I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low		I_{LIL}			−10	μA	V_I = OV
Output Leakage Current High		I_{LOH}			+5	μA	V_O = +2.4V to V_{CC} $\overline{CE}$ = +2.0V
Output Leakage Current Low		I_{LOL}			−10	μA	V_O = +0.4V $\overline{CE}$ = +2.0V
Power Supply Current	2111AL-4	I_{CC1}			50	mA	V_I = +5.25V
	2111AL 2111AL-2				55	mA	I_O = 0 mA T_a = +25° C
Power Supply Current	2111AL-4	I_{CC2}			60	mA	V_I = +5.25V
	2111AL 2111AL-2				65	mA	I_O = 0 mA T_a = −10 to +70°C

AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			310			240			180	ns
Output Disable to Output	t_{OD}			250			180			130	ns
Data Output to High Z State	t_{DF} ①	0		200	0		150	0		130	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

Note: ① t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, $\overline{CE}_2$, or OD, whichever occurs first.

WRITE CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Write Cycle Time	t_{WC}	270			220			170			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	250			200			150			ns
Data Setup Time	t_{DW}	250			200			150			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	250			200			150			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			20			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

AC CONDITIONS OF TEST

Input Pulse Levels	+0.8V to +2.0V
Input Pulse Rise and Fall Times	20 ns
Timing Measurement Reference Level	1.5V
Output Load	1 TTL + 100 pF

STANDBY CHARACTERISTICS

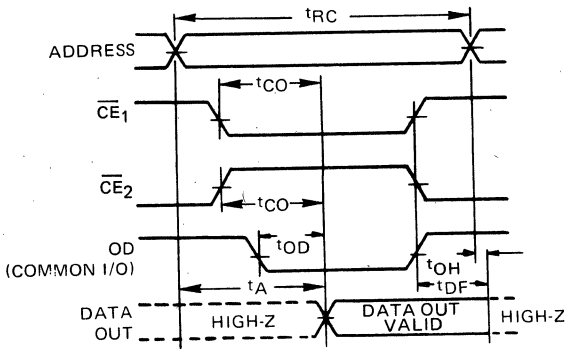
$T_a = -10°C$ to $+70°C$

PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP ①	MAX		
V_{CC} in Standby		V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby		V_{CES}	2.0			V	$2.0V \leq V_{PD} \leq 5.25V$
			V_{PD}			V	$1.5V \leq V_{PD} < 2.0V$
Standby Current Drain	2111AL-4	I_{PD_1}			36	mA	All Inputs = $V_{PD_1} = 1.5V$
	2111AL/AL-2				38		
Standby Current Drain	2111AL-4	I_{PD_2}			45	mA	All Inputs = $V_{PD_2} = 2.0V$
	2111AL/AL-2				48		
Chip Deselect to Standby Time		t_{CP}	0			ns	
Standby Recovery		t_R	t_{RC} ②			ns	

Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage
② $t_R = t_{RC}$ (Read Cycle Time)

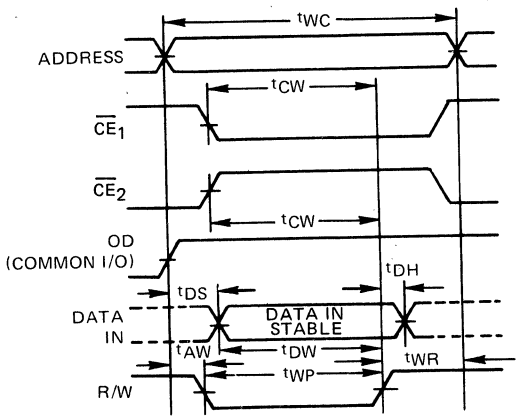
TIMING WAVEFORMS

READ CYCLE



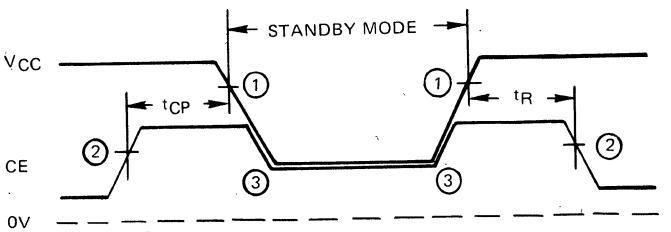
Notes: ① OD should be tied low for separate I/O operation.
② R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



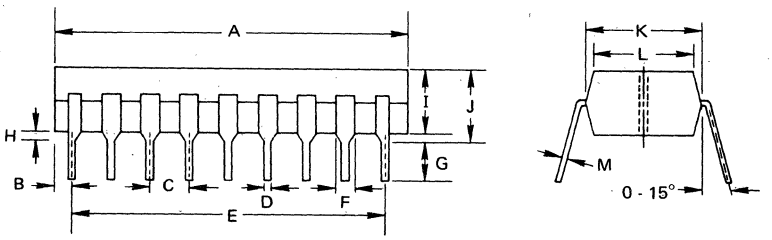
Notes: ① 4.75V
② 2.0V
③ 1.5V
④ If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two. $\overline{CE}$ may be either of $\overline{CE}_1$ or $\overline{CE}_2$.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			8	pf	$V_I = 0V$
Output Capacitance	C_{OUT}			12	pf	$V_O = 0V$

PACKAGE OUTLINE μPD2111ALC



ITEM	MILLIMETERS	INCHES
A	22.5 MAX.	0.89
B	1.09	0.04
C	2.54	0.10
D	0.50 ± 0.10	0.02
E	20.32	0.80
F	1.2 MIN.	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION

The μPD5101-E is a very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memory. It meets the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

All inputs and outputs of the μPD5101-E are TTL compatible. Two chip enables ($\overline{CE}_1$, CE_2) are provided, with the device being selected when $\overline{CE}_1$ is low and CE_2 is high. The μPD5101-E can be placed in standby mode, drawing 15 μA maximum, by driving $\overline{CE}_1$ high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

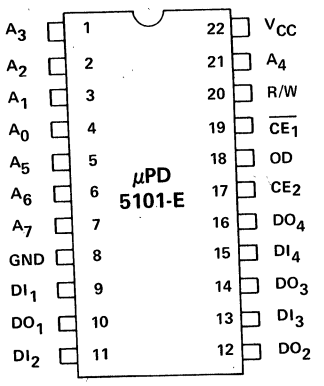
The μPD5101-E has separate input and output lines. It can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is non-destructively read out. Read mode is selected by placing a high on the R/W pin. The μPD5101-E is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

The μPD5101-E is fabricated using NEC's complementary MOS (CMOS) process and is packaged in a 22-pin dual-in-line package.

FEATURES

- Directly TTL Compatible – All Inputs and Outputs
- Three-State Output
- Access Time – 800 ns
- Single +5V Power Supply
- CE_2 Controls Unconditional Standby Mode

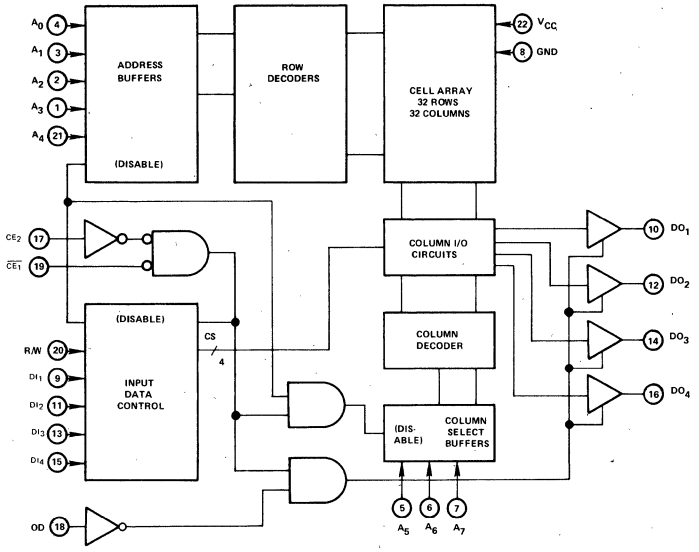
PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_4$	Data Input
$A_0 - A_7$	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$, CE_2	Chip Enables
OD	Output Disable
$DO_1 - DO_4$	Data Output
V_{CC}	Power (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
Voltage On Any Pin With Respect to Ground . . . . . −0.3 Volts to V_{CC} +0.3 Volts
Power Supply Voltage . . . . . −0.3 to +7.0 Volts

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP①	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Leakage	I_{LIH} ②			1	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL} ②			−1	μA	V_{IN} = 0V
Output High Leakage	I_{LOH} ②			1	μA	$\overline{CE_1}$ = 2.2V, $V_{OUT} = V_{CC}$
Output Low Leakage	I_{LOL} ②			−1	μA	$\overline{CE_1}$ = 2.2V, V_{OUT} = 0.0V
Operating Current	I_{CC1}		9	22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE_1}$ ⩽0.01V, Outputs Open
Operating Current	I_{CC2}		13	27	mA	V_{IN} = 2.2V Except $\overline{CE_1}$ ⩽0.65V, Outputs Open
Standby Current	I_{CCL} ②			15	μA	V_{IN} = 0 to 5.25V CE_2 ⩽ 0.2V
Input Low Voltage	V_{IL}	−0.3		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
Output High Voltage	V_{OH2}	3.5			V	I_{OH} = −100 μA

Notes: ① Typical values at T_a = 25°C and nominal supply voltage.
② Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance (All Input Pins)	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		12	20	pF	V_{OUT} = 0V

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C, V_{CC} = 5V ±5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Read Cycle	t_{RC}	800			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Access Time	t_A		415	800	ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}		400	800	ns	Timing measurement reference level: 1.5 Volt
Chip Enable (CE_2) to Output	t_{CO2}		440	850	ns	Output load: I_{TTL}
Output Disable to Output	t_{OD}		145	350	ns	Gate and C_L = 100 pF
Data Output to High Z State	t_{DF}	0		200	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	100		ns	
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	250		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Write Cycle	t_{WC}	800			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Write Delay	t_{AW}	200	−120		ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE_1}$) to Write	t_{CW1}	600	275		ns	Timing measurement reference level: 1.5 Volt
Chip Enable (CE_2) to Write	t_{CW2}	600	295		ns	Output load: I_{TTL}
Data Setup	t_{DW}	400			ns	Gate and C_L = 100 pF
Data Hold	t_{DH}	100	−160		ns	
Write Pulse	t_{WP}	400	190		ns	
Write Recovery	t_{WR}	50	−130		ns	
Output Disable Setup	t_{DS}	200			ns	

LOW V_{CC} DATA RETENTION CHARACTERISTICS

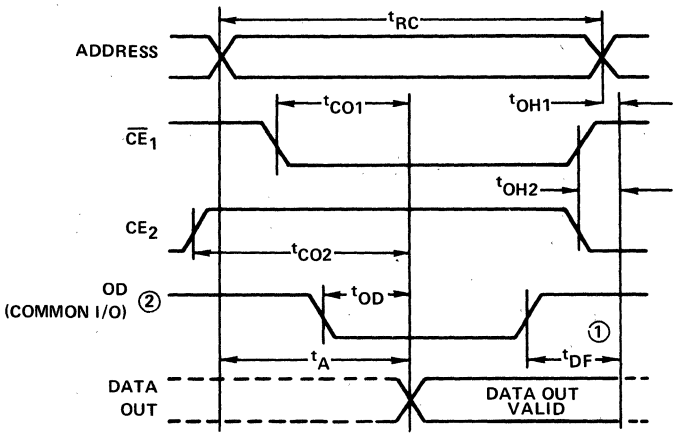
T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leq +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	V_{CCDR} = +2.0 to +3.0V; $CE_2 \leq +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC}①			ns	

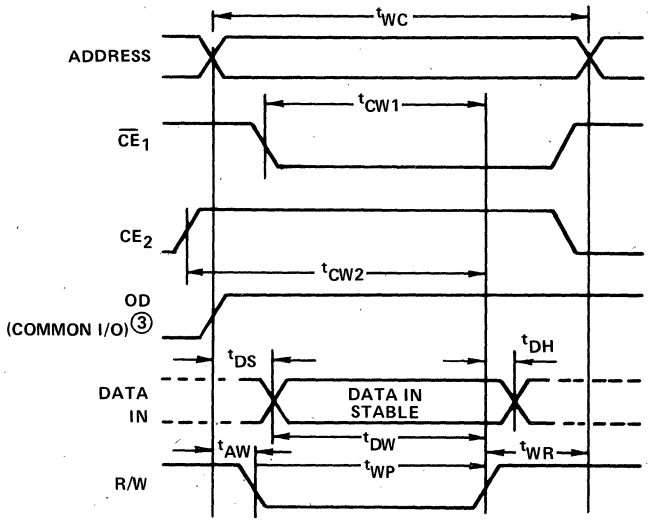
Note: ① t_{RC} = Read Cycle Time

TIMING WAVEFORMS

READ CYCLE

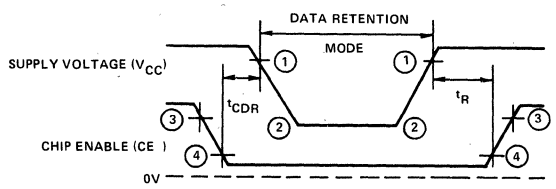


WRITE CYCLE



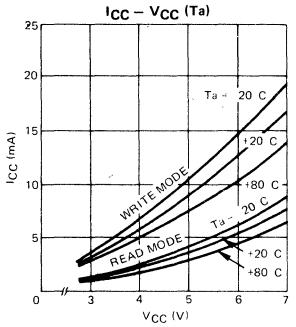
Notes: ① Typical values are for T_a = 25°C and nominal supply voltage.
② OD may be tied low for separate I/O operation.
③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

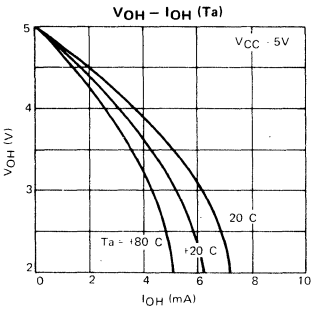
LOW V_{CC} DATA RETENTION

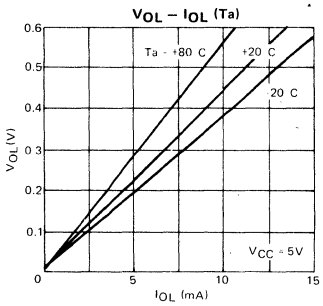


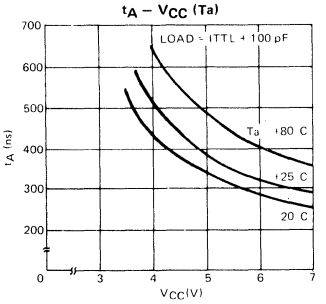
Notes: ① 4.75V
② V_{CCDR}
③ V_{IH}
④ 0.2V

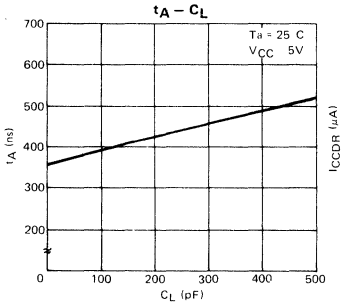
TYPICAL OPERATING CHARACTERISTICS

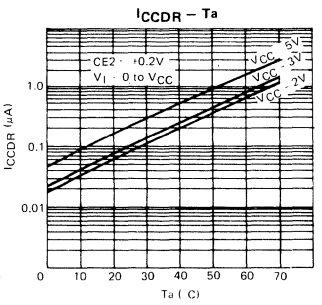




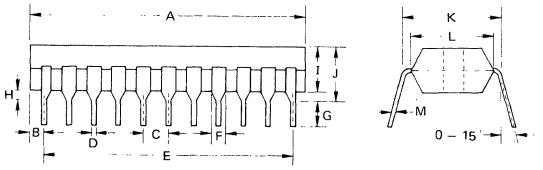








PACKAGE OUTLINE μPD5101C-E



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 ± 0.10	0.02 ± 0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION

The μPD5101L and μPD5101L-1 are very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memories. They meet the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

All inputs and outputs of the μPD5101L and μPD5101L-1 are TTL compatible. Two chip enables ($\overline{CE}_1$, CE_2) are provided, with the devices being selected when $\overline{CE}_1$ is low and CE_2 is high. The devices can be placed in standby mode, drawing 10 μA maximum, by driving $\overline{CE}_1$ high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

The μPD5101L and μPD5101L-1 have separate input and output lines. They can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is nondestructively read out. Read mode is selected by placing a high on the R/W pin. Either device is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

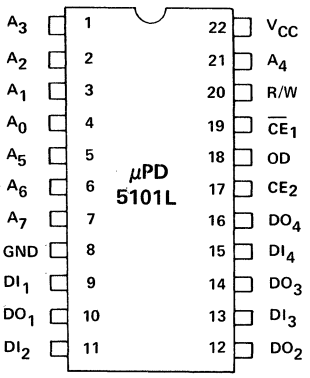
The μPD5101L and μPD5101L-1 are fabricated using NEC's silicon gate complementary MOS (CMOS) process.

3

FEATURES

- Directly TTL Compatible – All Inputs and Outputs
- Three-State Output
- Access Time – 650 ns (μPD5101L); 450 ns (μPD5101L-1)
- Single +5V Power Supply
- CE_2 Controls Unconditional Standby Mode
- Available in a 22-pin Dual-in-Line Package

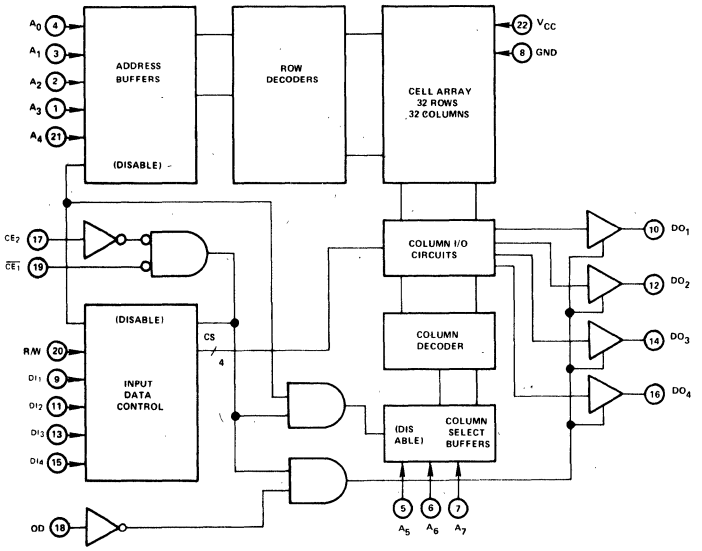
PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_4$	Data Input
$A_0 - A_7$	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$, CE_2	Chip Enables
OD	Output Disable
$DO_1 - DO_4$	Data Output
V_{CC}	Power (+5V)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
Voltage On Any Pin With Respect to Ground . . . . . −0.3 Volts to V_{CC} +0.3 Volts
Power Supply Voltage . . . . . −0.3 to +7.0 Volts

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Leakage	I_{LIH} (2)			1	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL} (2)			−1	μA	V_{IN} = 0V
Output High Leakage	I_{LOH} (2)			1	μA	$\overline{CE}_1$ = 2.2V, $V_{OUT} = V_{CC}$
Output Low Leakage	I_{LOL} (2)			−1	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.0V
Operating Current	I_{CC1}			22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Operating Current	I_{CC2}			27	mA	V_{IN} = 2.2V Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Standby Current	I_{CCL} (2)			10	μA	V_{IN} = 0 to 5.25V $CE_2 \leq$ 0.2V
Input Low Voltage	V_{IL}	−0.3		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
Output High Voltage	V_{OH2}	3.5			V	I_{OH} = −100 μA

Notes: (1) Typical values at T_a = 25°C and nominal supply voltage.
(2) Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance (All Input Pins)	C_{IN}		4	8	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0V

AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Read Cycle	t_{RC}	650			450			ns	Input pulse amplitude: 0,65 to 2,2 Volts
Access Time	t_A			650			450	ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE}_1$) to Output	t_{CO1}			600			400	ns	Timing measurement reference level: 1,5 Volt
Chip Enable (CE_2) to Output	t_{CO2}			700			500	ns	Output load: I_{TTL}
Output Disable to Output	t_{OD}			350			250	ns	Gate and C_L = 100 pF
Data Output to High Z State	t_{DF}	0		150	0		130	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0			0			ns	
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0			0			ns	

WRITE CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		5101L			5101L-1				
		MIN	TYP	MAX	MIN	TYP	MAX		
Write Cycle	t_{WC}	650			450			ns	Input pulse amplitude: 0,65 to 2,2 Volts
Write Delay	t_{AW}	150			130			ns	
Chip Enable ($\overline{CE}_1$) to Write	t_{CW1}	550			350			ns	Input rise and fall times: 20 ns
Chip Enable (CE_2) to Write	t_{CW2}	550			350			ns	Timing measurement reference level: 1,5 Volt
Data Setup	t_{DW}	400			250			ns	
Data Hold	t_{DH}	100			50			ns	Output load: I_{TTL}
Write Pulse	t_{WP}	400			250			ns	Gate and C_L = 100 pF
Write Recovery	t_{WR}	50			50			ns	
Output Disable Setup	t_{DS}	150			130				

LOW V_{CC} DATA RETENTION CHARACTERISTICS

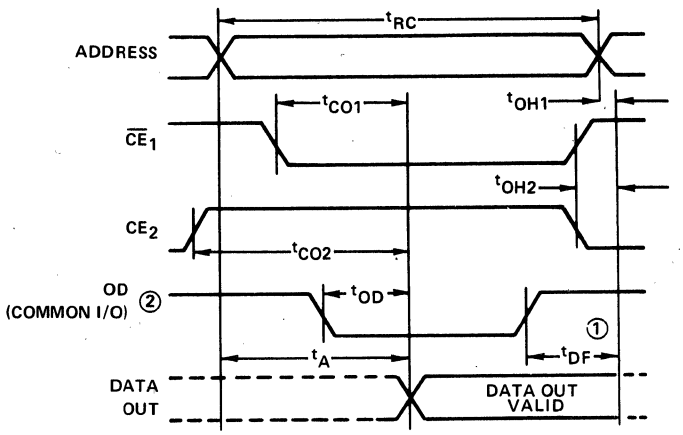
T_a = 0°C to 70°C

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leqslant +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	V_{CCDR} = +2.0V $CE_2 \leqslant +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC}①			ns	

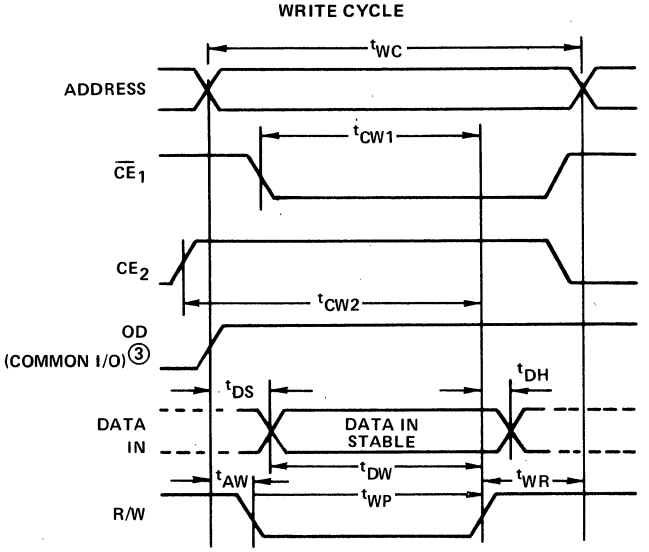
Note: ① t_{RC} = Read Cycle Time

TIMING WAVEFORMS

READ CYCLE

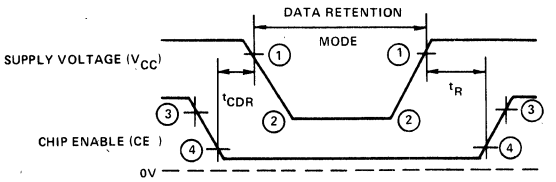


WRITE CYCLE



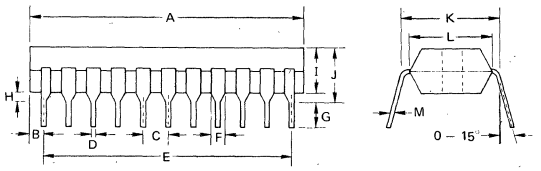
Notes: ① Typical values are for T_a = 25°C and nominal supply voltage.
② OD may be tied low for separate I/O operation.
③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

LOW V_{CC} DATA RETENTION



Notes: ① 4.75V
② V_{CCDR}
③ V_{IH}
④ 0.2V

PACKAGE OUTLINE
μPD5101LC



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 ± 0.10	0.02 ± 0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

FULLY DECODED 2048 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

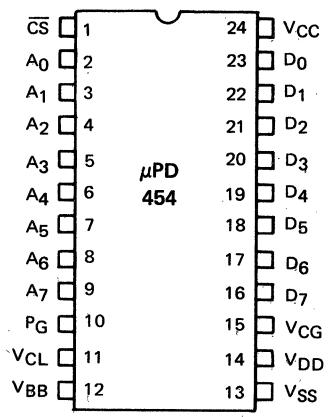
The μPD454 EEPROM, a 256 Words x 8 Bits Read Only Memory, is designed for rapid development of microcomputer systems. The ability to electrically program, erase, and reprogram the μPD454 provides a fast and convenient means of debugging both hardware and software designs.

The μPD454 is pin for pin compatible with NEC's μPD464 mask programmed ROM.

FEATURES

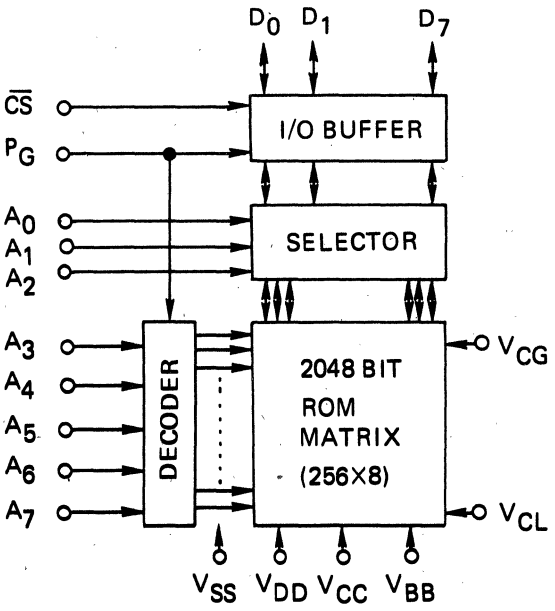
- Electrically Erasable and Programmable
- Fully Decoded, 256 Words x 8 Bits Organization
- Access Time 800 ns Max
- Low Power: 245 mW (Typ.) in Read Operation
  670 mW (Typ.) in Programming Operation
- Fast Programming and Erasure Speed
- Low Power for Programming and Erasure
- Static, No Clock Required
- Input/Output TTL Compatible for Read and Programming Operation
- Three-State Output, OR-Tie Capability
- N-Channel MOS Fabrication
- Two Power Supplies, +12V and +5V for Read Operation
- 24 Pin Ceramic DIP

PIN CONFIGURATION



Rev/1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.3 to +11 Volts①
All Input Voltages	−0.3 to +11 Volts①
Supply Voltage V_{DD}	−0.3 to +15 Volts①
Supply Voltage V_{CC}	−0.3 to +7 Volts①
Supply Voltage V_{BB}	V_{SS} to −7 Volts②
Supply Voltage P_G	−0.3 to +30 Volts①②
Supply Voltage V_{CL}	−0.3 to +43 Volts①②
Supply Voltage V_{CG}	−44 to +30 Volts①②

Notes: ① Relative to V_{BB}.
② Data in the memory cell is not guaranteed to be preserved.
Specifies ratings which will not cause permanent damage to the device.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			15	pF	f = 1 MHz

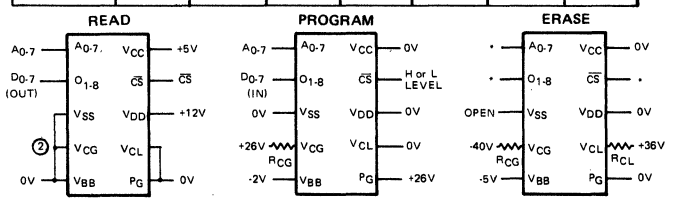
PIN DEFINITION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1	$\overline{CS}$	CHIP SELECT	Chip selection, active low
2-9	A_0–A_7	ADDRESS BUS	Memory address
10	P_G	+26V (TYP) Power Supply	Power supply for programming operation
11	V_{CL}	+36V (TYP) Power Supply	Power supply for erasing operations
12	V_{BB}	Substrate Power Supply	Power supply
13	V_{SS}	GROUND	Ground Reference
14	V_{DD}	+12V Power Supply	Power supply for read operations
15	V_{CG}	−44 to +30 Power Supply	Power supply for control of programming and erasure operations
16-23	D_7–D_0	Data Input/Output	Data In for programming operations. Data Output for read operations.
24	V_{CC}	+5V Power Supply	Power supply for read operations

SUPPLY VOLTAGES

Typical values. Unit – Voltage.

MODE \ PIN	V_{DD}(14)	V_{CC}(24)	V_{BB}(14)	P_G(10)	V_{CL}(11)	V_{CG}(15)	V_{SS}(13)
Read	+12	+5	0	0	0	0	0
Program	0	0	−2	+26	0	+26	0
Erase	0	0	−5	0	+36	−40	Open
Verify "0"	+12	+5		0	0	+3	0
Verify "1"	+12	+5		0	0	−3	0

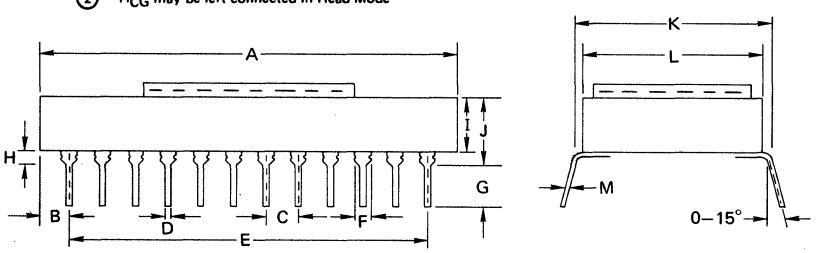


Notes: * = Either High or Low Level, or Open.

① R_{CG} and R_{CL} are Protection Resistors
R_{CG} = 10 kΩ ± 10%, 1/4W
R_{CL} = 200Ω ± 10%, 10W

② R_{CG} may be left connected in Read Mode

PACKAGE OUTLINE μPD454D



ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

READ OPERATION

DC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

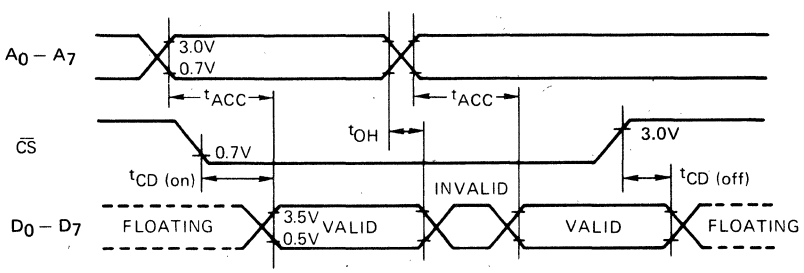
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Output High Voltage	V_{OH}	3.5			V	$I_{OH} = -2.0$ mA
Output Low Voltage	V_{OL}			0.5	V	$I_{OL} = 1.7$ mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = +3.0V$
Input Leakage Current Low	I_{LIL}			-10	μA	$V_I = +0.7V$
Output Leakage Current High	I_{LOH}			+100	μA	$\overline{CS}$ = "1" $V_O = 3.5V$
Output Leakage Current Low	I_{LOL}			-10	μA	$\overline{CS}$ = "1" $V_O = 0.4V$
V_{DD} Supply Current	I_{DD}		20		mA	
V_{CC} Supply Current	I_{CC}			0.3	mA	with no load

AC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$,
$V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Access Time	t_{ACC}			800	ns	1 TTL + 100 pF
$\overline{CS}$ to Output On Delay	$t_{CD(on)}$			200	ns	
$\overline{CS}$ to Output Off Delay	$t_{CD(off)}$	0		200	ns	
Output Hold Time	t_{OH}	0			ns	

TIMING WAVEFORMS



PROGRAMMING OPERATION

Before the μPD454 is programmed the device must be erased. All bit locations must contain a zero (0). The μPD454 programming procedure is word by word one word at a time.

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

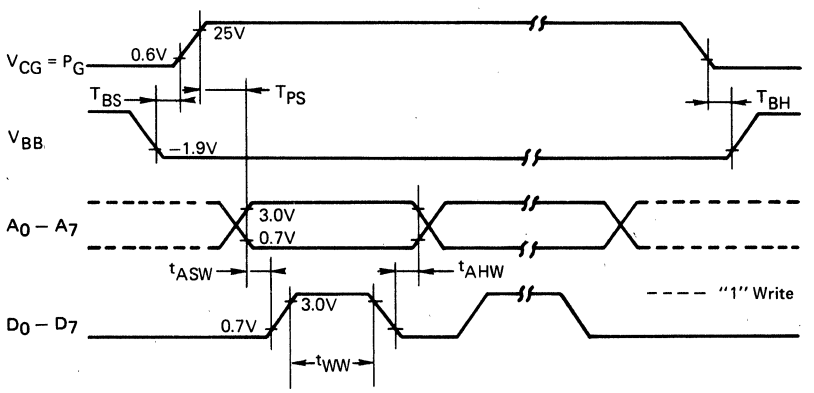
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Supply Voltage	V_{BB}	-1.9	-2.0	-2.1	V	
Supply Voltage	P_G	25	26	27	V	
Supply Voltage	V_{CG}	25	26	27	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}		-8		mA	
Supply Current (P_G)	I_G		+25		mA	
Supply Current (V_{CG})	I_{CG}			+10	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Setup Time	t_{ASW}	10			μs	
Address Hold Time	t_{AHW}	10			μs	
Write Data Width	t_{WW}	20		100	ms	per one word
V_{BB} Setup Time	T_{BS}	1.0			μs	
V_{BB} Hold Time	T_{BH}	1.0			μs	
P_G, V_{CG} Setup Time	T_{PS}	10			μs	

TIMING WAVEFORMS



ERASURE OPERATION*

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$
$\overline{CS}$, $A_0 - A_7$ and $D_0 - D_7$ = Either HIGH or LOW level, or non-connected

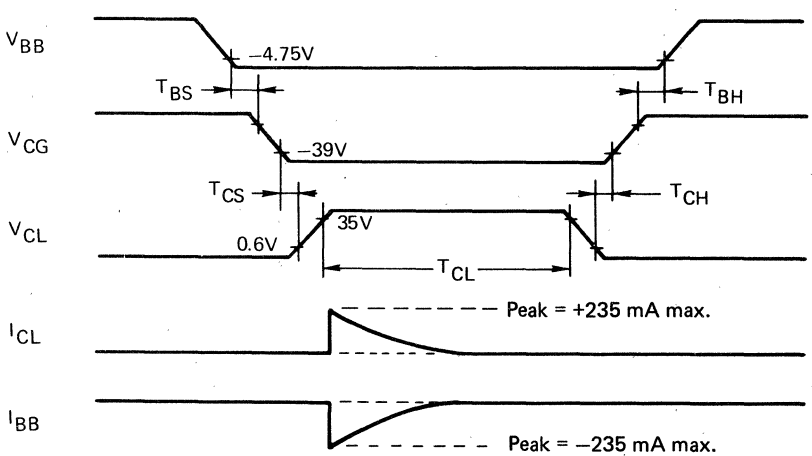
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{BB}	-4.75	-5.0	-5.25	V	
Supply Voltage	V_{CL}	+35	+36	+37	V	through R_{CL}
Supply Voltage	V_{CG}	-39	-40	-41	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}			-235	mA	Initial peak current. See timing chart.
Supply Current (V_{CL})	I_{CL}			-235	mA	
Supply Current (V_{CG})	I_{CG}			-20	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$
$\overline{CS}$, $A_0 - A_7$ and $D_0 - D_7$ = Either HIGH or LOW level, or non-connected

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clear Time	T_{CL}			60	sec	
V_{BB} Setup Time	T_{BS}	0			μs	
V_{BB} Hold Time	T_{BH}	0			μs	
V_{CG} Setup Time	T_{CS}	1.0			μs	
V_{CG} Hold Time	T_{CH}	1.0			μs	

TIMING WAVEFORMS



Note: The supply currents I_{BB} and I_{CL} diminish to almost zero within T_{CL}.

*Erasure operation clears all 2048 bits to Logic "0" simultaneously.

FULLY DECODED 8192 BIT ELECTRICALLY ERASABLE AND PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

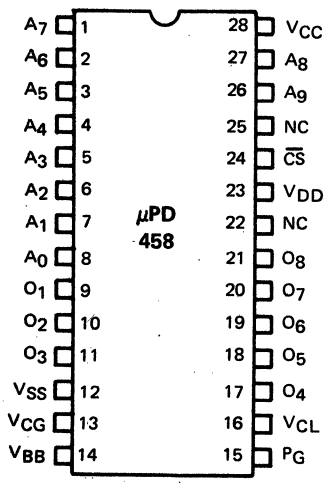
The μPD458 is an Electrically Erasable and Reprogrammable Read Only Memory (EEPROM), organized as 1024 words by 8 bits.

The μPD458 is fabricated with N-channel MOS technology and is packaged in a 28 pin ceramic DIP.

FEATURES

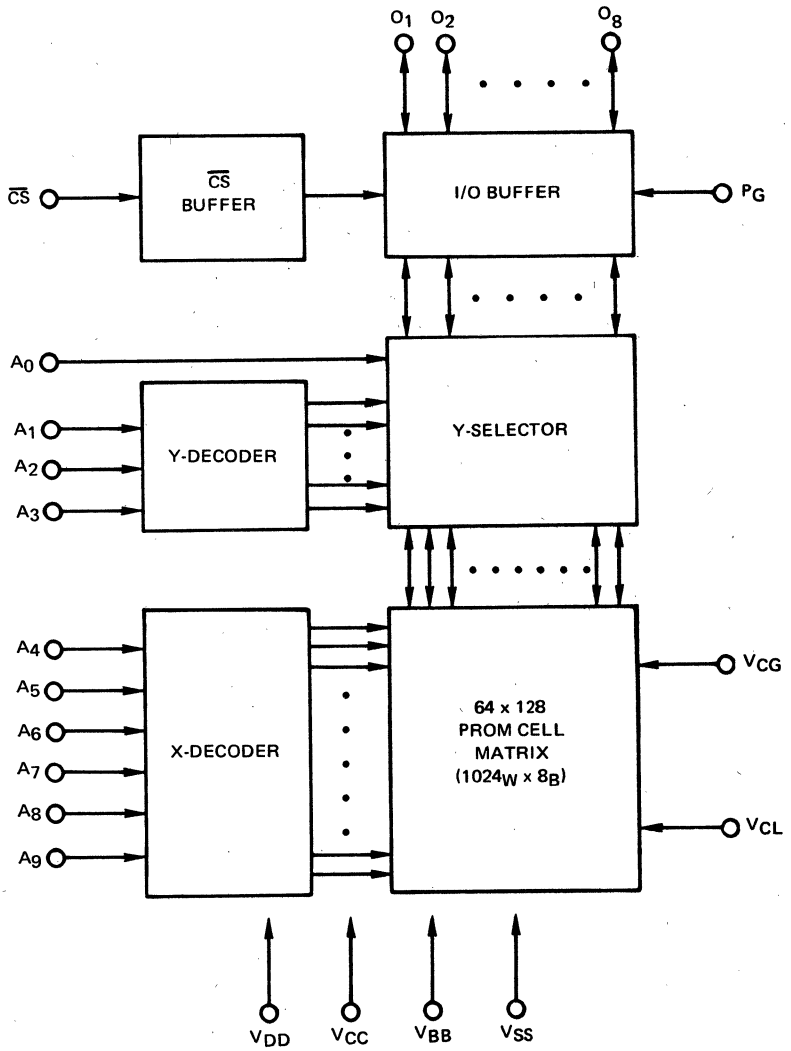
- Electrically Erasable and Reprogrammable
- Fully Decoded, 1024 Words x 8 Bits Organization
- Access Time – 450 ns max.
- Fast Programming and Erasure Speed
- Simple Worst-case Verification of Programmed Data and Erasure
- Static, No Clock Required
- Input/Output TTL Compatible for Read and Programming Operation
- Three-State Output, OR-Tie Capability
- N-Channel MOS
- Two Power Supplies, +12V and +5V for Read
- 28 Pin Ceramic DIP

PIN CONFIGURATION



NC: No Connection

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.3 to +11 Volts①
All Input Voltages	−0.3 to +11 Volts①
Supply Voltage V_{DD}	−0.3 to +15 Volts①
Supply Voltage V_{CC}	−0.3 to +7 Volts①
Supply Voltage V_{BB}	V_{SS} to −7 Volts②
Supply Voltage P_G	−0.3 to +30 Volts①②
Supply Voltage V_{CL}	−0.3 to +43 Volts①②
Supply Voltage V_{CG}	−44 to +30 Volts①②

Notes: ① Relative to V_{BB}.

② Data in the memory cell is not guaranteed to be preserved.
Specifies ratings which will not cause permanent damage to the device.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

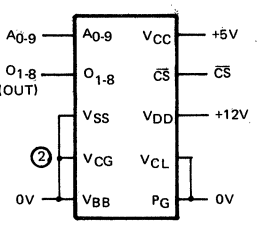
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			15	pF	f = 1 MHz

SUPPLY VOLTAGES

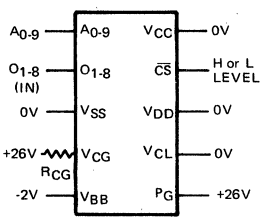
Typical values. Unit – Voltage.

MODE \ PIN	V_{DD}(23)	V_{CC}(28)	V_{BB}(14)	P_G(15)	V_{CL}(16)	V_{CG}(13)	V_{SS}(12)
Read	+12	+5	0	0	0	0	0
Program	0	0	−2	+26	0	+26	0
Erase	0	0	−5	0	+36	−40	0 or Open
Verify "0"	+12	+5		0	0	+3	0
Verify "1"	+12	+5		0	0		0

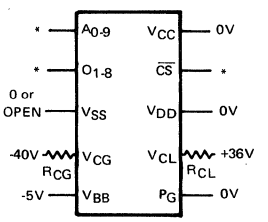
READ



PROGRAM



ERASE



Notes: * = Either High or Low Level, or Open.

① R_{CG} and R_{CL} are Protection Resistors
R_{CG} = 10 kΩ ± 10%, 1/4W
R_{CL} = 200Ω ± 10%, 10W

② R_{CG} may be left connected in Read Mode.

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	INPUT/ OUTPUT	FUNCTION
1 – 8, 26, 27	$A_0 – A_9$	Input	Address Input
24	$\overline{CS}$	Input	Chip Select Input (Active Low)
9 – 11, 17 – 21	$O_1 – O_8$	Output	Data Out for Read Operation
		Input	Data Input for Programming Operation
15	P_G	Power Supply	Power Supply for Programming Operation
16	V_{CL}	Power Supply	Power Supply for Erasure Operation
13	V_{CG}	Power Supply	Power Supply for Control Gate for Programming and Erasure Operation
14	V_{BB}	Power Supply	Power Supply for Substrate Bias
23	V_{DD}	Power Supply	+12V Power Supply for Read Operation
28	V_{CC}	Power Supply	+5V Power Supply for Read Operation
12	V_{SS}	GND	Ground Reference

READ OPERATION

DC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

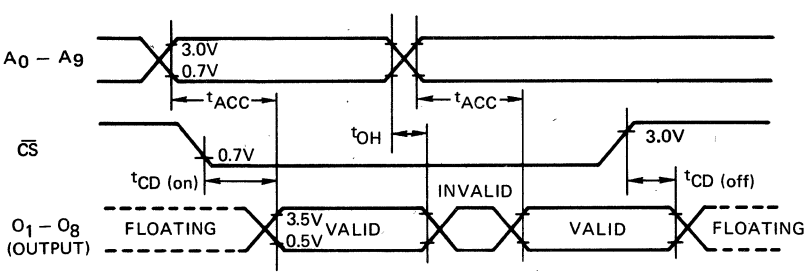
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Output High Voltage	V_{OH}	3.5			V	$I_{OH} = -2.0$ mA
Output Low Voltage	V_{OL}			0.5	V	$I_{OL} = 1.7$ mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = +3.0V$
Input Leakage Current Low	I_{LIL}			-10	μA	$V_I = +0.7V$
Output Leakage Current High	I_{LOH}			+20	μA	$\overline{CS}$ = "1" $V_O = 3.5V$
Output Leakage Current Low	I_{LOL}			-10	μA	$\overline{CS}$ = "1" $V_O = 0.4V$
V_{DD} Supply Current	I_{DD}		55	80	mA	
V_{CC} Supply Current	I_{CC}		20	30	mA	with no load

AC CHARACTERISTICS

$T_a = -10$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = P_G = V_{CL} = V_{CG} = V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Access Time	t_{ACC}			450	ns	1 TTL + 100 pF
$\overline{CS}$ to Output On Delay	$t_{CD(on)}$			200	ns	
$\overline{CS}$ to Output Off Delay	$t_{CD(off)}$	0		200	ns	
Output Hold Time	t_{OH}	0			ns	

TIMING WAVEFORMS



PROGRAMMING OPERATION

Programming is performed word by word and one word at a time. Address and an 8 bit programming word for that address should be input at the same time. High level data "1" given through one of Data Input terminals ($O_1 - O_8$) writes a high level data "1" into the memory cell specified with the address input and its bit position.

After erasure, all memory cells of the μPD458 contain cleared data "0". By this programming operation, only the memory cells which contain data "0" are programmed to high level data "1" by high level input. Thus before normal programming operation, the μPD458 should undergo erasure operation to clear all bits to "0".

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

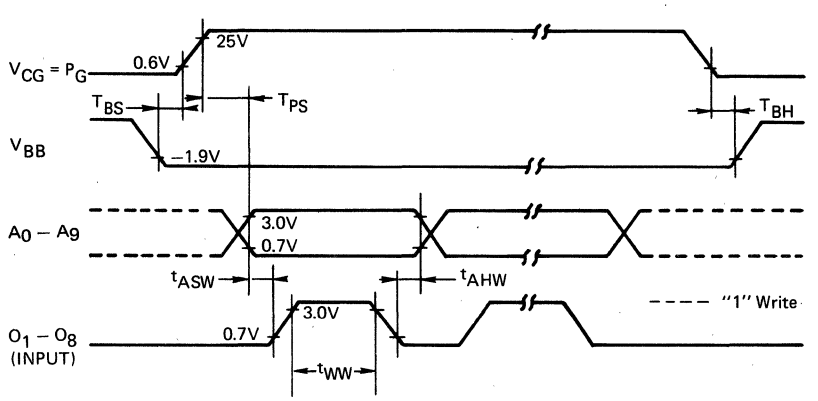
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input High Voltage	V_{IH}	3.0		5.25	V	
Input Low Voltage	V_{IL}	0		0.7	V	
Supply Voltage	V_{BB}	-1.9	-2.0	-2.1	V	
Supply Voltage	P_G	25	26	27	V	
Supply Voltage	V_{CG}	25	26	27	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}		-8	-15	mA	
Supply Current (P_G)	I_G		+30	+50	mA	
Supply Current (V_{CG})	I_{CG}			+20	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = V_{SS} = V_{CL} = 0V$. $\overline{CS}$ = Either HIGH or LOW level.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address Setup Time	t_{ASW}	10			μs	
Address Hold Time	t_{AHW}	10			μs	
Write Data Width	t_{WW}	40		100	ms	per one word
V_{BB} Setup Time	T_{BS}	1.0			μs	
V_{BB} Hold Time	T_{BH}	1.0			μs	
P_G, V_{CG} Setup Time	T_{PS}	10			μs	

TIMING WAVEFORMS



ERASURE OPERATION*

DC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$ or Open
$\overline{CS}$, $A_0 - A_9$ and $O_1 - O_8$ = Either HIGH or LOW level, or non-connected

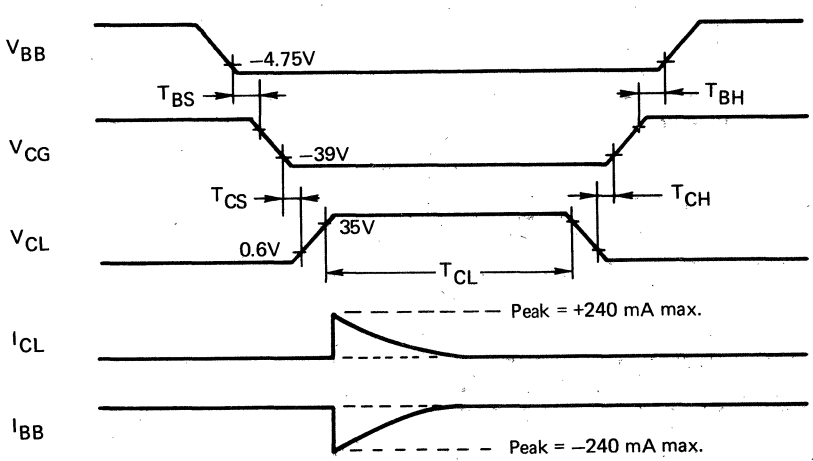
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Supply Voltage	V_{BB}	-4.75	-5.0	-5.25	V	
Supply Voltage	V_{CL}	+35	+36	+37	V	through R_{CL}
Supply Voltage	V_{CG}	-39	-40	-41	V	through R_{CG}
Supply Current (V_{BB})	I_{BB}			-240	mA	Initial peak current. See timing chart.
Supply Current (V_{CL})	I_{CL}			+240	mA	
Supply Current (V_{CG})	I_{CG}			-20	μA	

AC CHARACTERISTICS

$T_a = 25°C \pm 2°C$, $V_{DD} = V_{CC} = P_G = 0V$, $V_{SS} = 0V$ or Open
$\overline{CS}$, $A_0 - A_9$ and $O_1 - O_8$ = Either HIGH or LOW level, or non-connected

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clear Time	T_{CL}		60		sec	
V_{BB} Setup Time	T_{BS}	0			μs	
V_{BB} Hold Time	T_{BH}	0			μs	
V_{CG} Setup Time	T_{CS}	1.0			μs	
V_{CG} Hold Time	T_{CH}	1.0			μs	

TIMING WAVEFORMS



Note: The supply currents I_{BB} and I_{CL} diminish to almost zero within T_{CL}.

*Erasure operation clears all 8192 bits to Logic "0" simultaneously.

APPENDIX
PROM PROGRAMMER
DESIGN

To insure integrity and retention of data programmed in the μPD458, the following requirements are specified for the μPD458 supply voltage and current levels. The PROM PROGRAMMER should be designed such that voltages provided to the PROM socket be within the range specified on any occasion including power on/off to the programmer, power on/off to the μPD458, and in READ, WRITE or ERASE operation. Surge or noise voltages beyond the specified range are to be avoided.

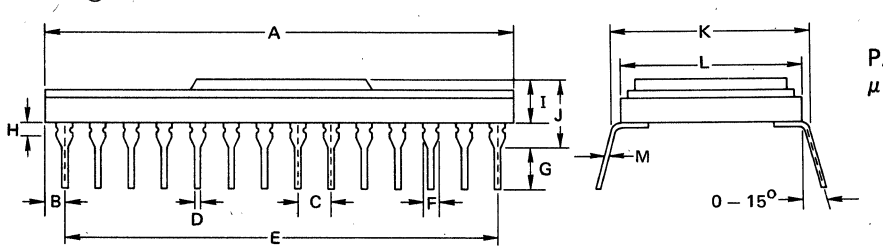
Setting V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5% and V_{CG} = +3V ± 0.1V after erasure and comparing data read from the μPD458 with zero effectively tests for proper erasure.

Setting V_{DD}= +12V ± 5%, V_{CC} = +5V ± 5% and V_{CG} = -3V ± 0.1V after programming and comparing data read from the μPD458 with the desired data coupled with erase verification, provides a simple test of worst-case temperature and long-term data retention.

Under normal Read Mode conditions, V_{CG} should either be grounded directly or held at 0V ± 0.1V through R_{CG}. R_{CG} is required when any non-zero voltage is applied to V_{CG}.

SYMBOL	LIMITS②									UNIT	TEST CONDITIONS
	READ			PROGRAM			ERASE				
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
V_{DD}	+11.4	+12	+12.6	-0.3	0	+0.3	-0.3	0	+0.3	V	
V_{CC}	+4.75	+5	+5.25	-0.3	0	+0.3	-0.3	0	+0.3	V	
V_{CG}	-0.1	0	+0.1	+25	+26	+27	-39	-40	-41	V	
V_{BB}	-0.1	0	+0.1	-1.9	-2	-2.1	-4.75	-5	-5.25	V	
P_G	-0.3	0	+0.3	+25	+26	+27	-0.3	0	+0.3	V	
V_{CL}	-0.1	0	+0.1	-0.1	0	+0.1	+35	+36	+37	V	
I_{CC}		+20	+30			-0.2			-0.2	mA	①
I_{DD}		+55	+80			-0.2			-0.2	mA	①
I_{CG}			+10			+20			-20	μA	①
I_{BB}			-0.2		-8	-15			-240	mA	①
I_{PG}			-0.2		+30	+50			-0.2	mA	①
I_{CL}			-0.5			-10			+240	mA	①

Notes: ① At typical supply voltage
② All voltages relative to VSS = 0V.

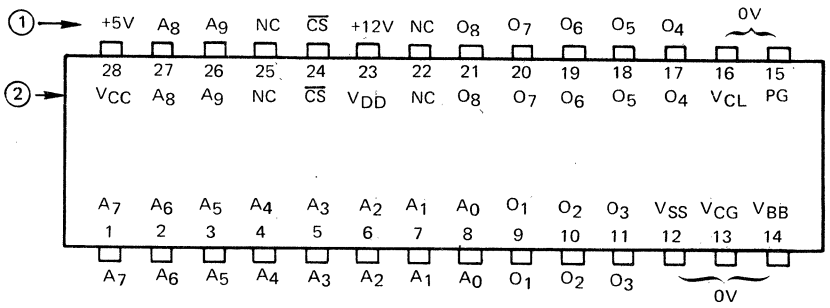


PACKAGE OUTLINE
μPD458D

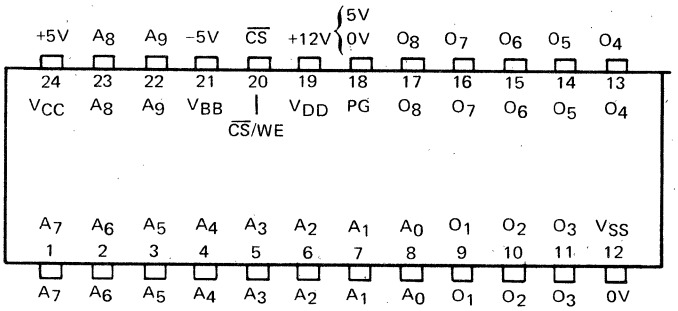
ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.41 MAX.
B	1.5 MAX.	0.059 MAX
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

μPD458

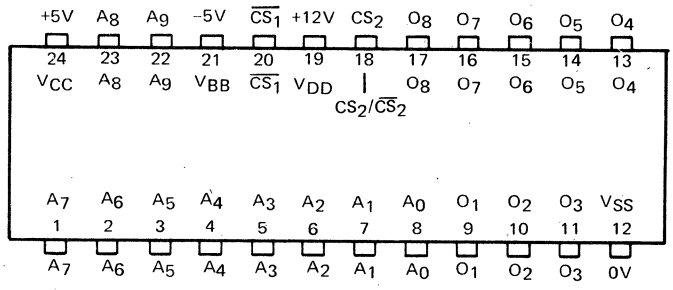
μPD458D (EEPROM)



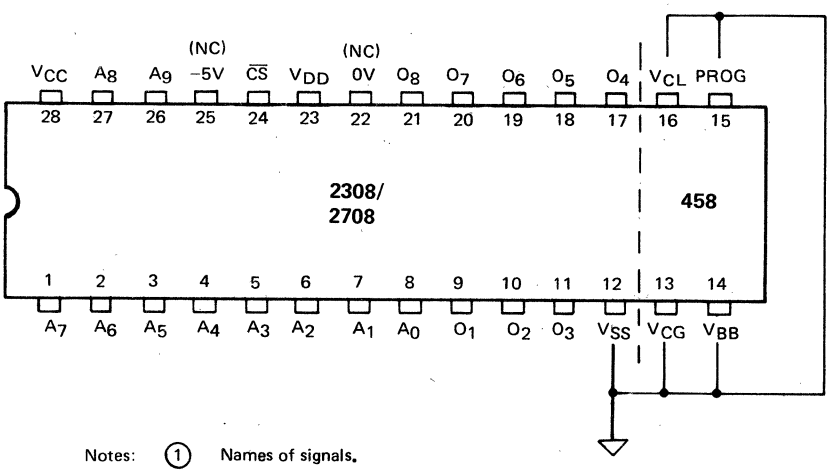
2708 (PROM ERASABLE WITH ULTRAVIOLET)



μPD2308C/D – 2308 (MASK ROM)



COMMON PIN CONFIGURATION



Notes: ① Names of signals.
② Names of the terminal.

4

1024-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

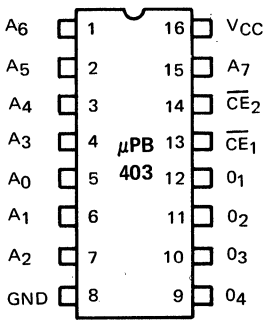
DESCRIPTION

The μPB403 is a high speed electrically programmable fully decoded 1024 bit TTL read only memory. On-chip address decoding, two chip enable inputs and open-collector outputs allow easy expansion of memory capacity. The μPB403 is fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 256 Words x 4 Bits Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 30 ns TYP.
- Medium Power Consumption: 450 mW TYP.
- AIM (Avalanche Induced Migration) Technology
- Two Chip Enable Inputs for Memory Expansion
- Open-Collector Outputs
- Ceramic 16-Pin Dual-In-Line Package
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: Intersil's IM5603A (both in programming and as a ROM), Harris HPROM1024A and Equivalent Devices (as a ROM)

PIN CONFIGURATION



OPERATION

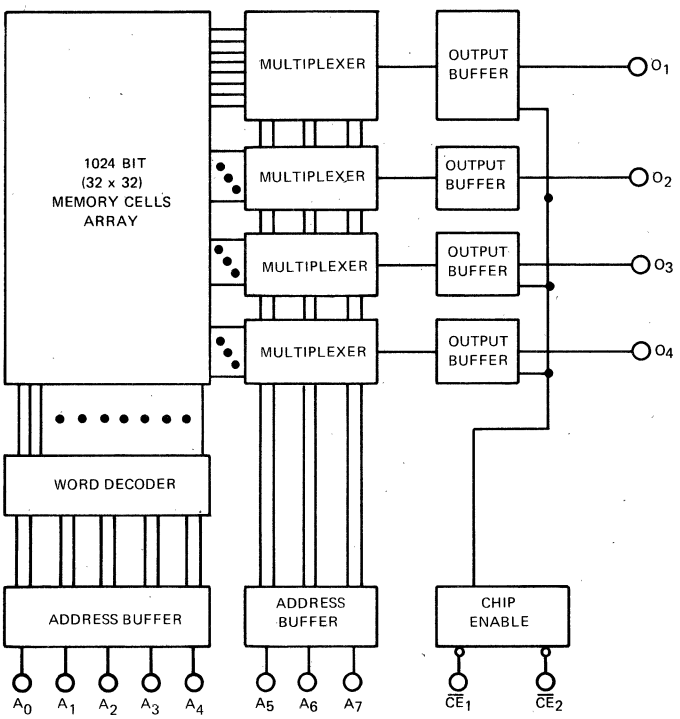
Programming

A logic one can be permanently programmed into a selected bit location in accordance with the programming procedures specified. First, the desired word is selected by the eight TTL address inputs. Either or both of the two chip enable inputs should be at a logic one (high). Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, and programming is complete.

Reading

To read the memory, both of the two chip enable inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip enable inputs are at logic one (high), all the outputs will be high (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−25°C to +75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +65°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			1.0	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$				μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		90	130	mA	All Inputs Grounded

AC CHARACTERISTICS

T_a = 25°C, V_{CC} = 5.0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Address Access Time	t_{AA}		30	60	ns	See Notes
Chip Enable Access Time	t_{ACE}			30	ns	
Chip Enable Disable Time	t_{DCE}			30	ns	

Notes:
① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

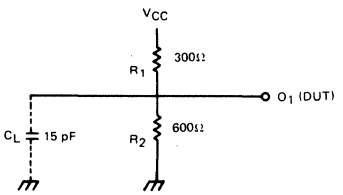
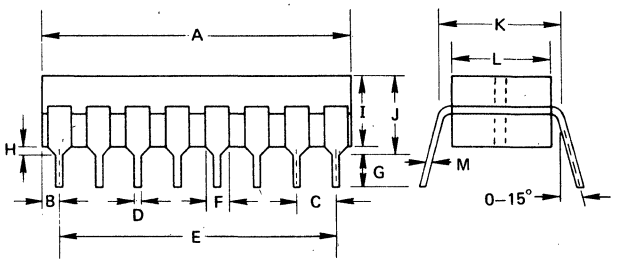


Figure 1

PACKAGE OUTLINE μPB403D



ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB403. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state.

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The μPB403 is disabled by forcing 2 mA into one of the chip enables. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This operation is also executed with 2 mA being forced into a chip enable. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

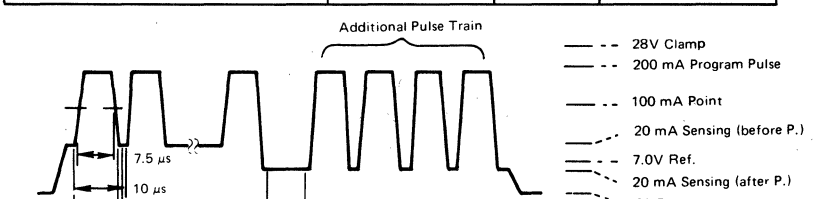


Figure 2. Typical Output Voltage Waveform

4096-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

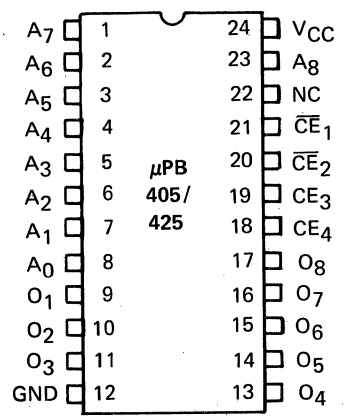
DESCRIPTION

The μPB405 and μPB425 are high speed, electrically programmable, fully decoded 4096-bit TTL read only memories. On-chip address decoding, four chip enable inputs and open-collector outputs allow easy expansion of memory capacity. The μPB405 and μPB425 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 512 WORDS X 8 BITS Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 70 ns max. (μPB425)
- Medium Power Consumption: 600 mW TYP.
- Four Chip Enable Inputs for Memory Expansion
- Open-Collector Outputs (μPB405)/Three-State Outputs (μPB425)
- Ceramic 24-Lead Dual In-Line Package
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: Intersil's IM5605/5625 (both in programming and as a ROM), Harris' HPROM HM-7640/7641 and Equivalent Devices (as a ROM).
- A.I.M. (Avalanche Induced Migration) Technology

PIN CONFIGURATION



NC: No Connection

OPERATION

Chip Enable logic is defined by:

$\overline{CE}_1$	$\overline{CE}_2$	CE_3	CE_4	CE'
0	0	1	1	0
All other combinations				1

Where: CE' = 0 denotes chip selected
CE' = 1 denotes chip deselected

Programming

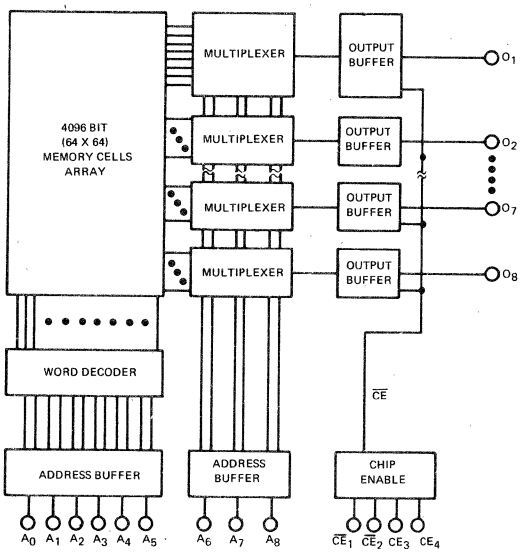
A logic one can be permanently programmed into a selected bit location in accordanc with the programming procedures specified. First, the desired word is selected by the eight TTL address inputs. The four Chip Enable inputs must be set so that CE' is a logical one. Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, and programming is complete.

Reading

To read the memory, the four Chip Enable inputs must be set so that CE' is a logical zero. The outputs then correspond to the data programmed in the selected words. When the four Chip Enable inputs are set so that CE' becomes a logical one, all the outputs will be high (floating).

4

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−25°C to +75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C .

DC CHARACTERISTICS

T_a = 0°C to +65°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$	40			μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		120	160	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = −2.4 mA
Output Short Circuit Current①	$-I_{SC}$	15		60	mA	V_O = 0V

NOTE: ① Applicable to μPB425D only.

AC CHARACTERISTICS

T_a = 25°C, V_{CC} = 5.0V

PARAMETER	SYMBOL	LIMITS 405-E/425-E			LIMITS 425			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Address Access Time	t_{AA}			100		40	70	ns	
Chip Enable Access Time	t_{ACE}			70			35	ns	
Chip Enable Disable Time	t_{DCE}			70			35	ns	

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

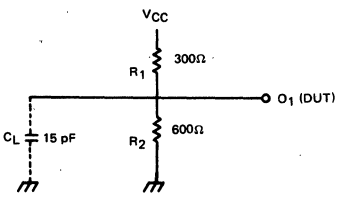
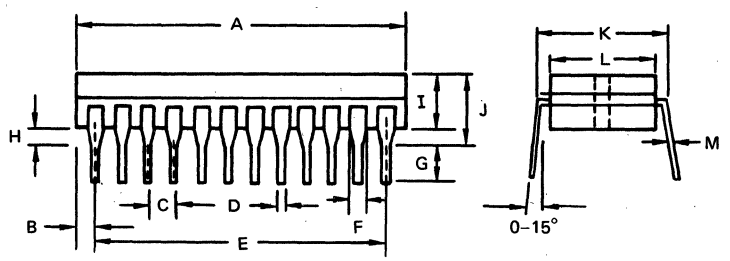


Figure 1

PACKAGE OUTLINE μPB405/425D



ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB405 and μPB425. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state.

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The μPB405 and μPB425 are disabled in accordance with the truth table on page 2. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

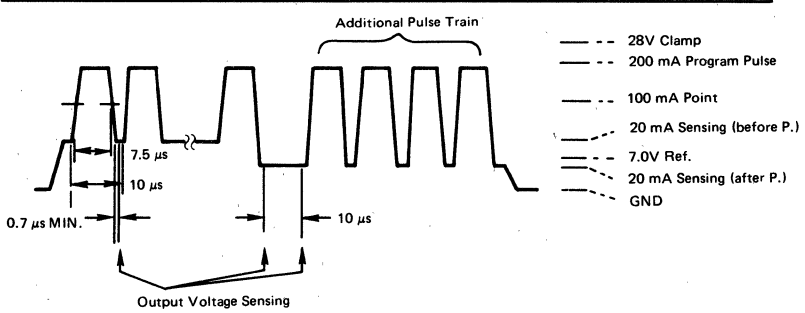


Figure 2. Typical Output Voltage Waveform

μPB406
μPB406-E
μPB426
μPB426-E

4096-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

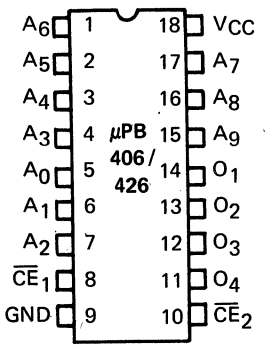
DESCRIPTION

The μPB406 and μPB426 are high speed electrically programmable fully decoded 4096-bit TTL read only memories. On-chip address decoding, two chip enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB406 and μPB426 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 1024 WORDS X 4 BITS Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 70 ns MAX. (406/426)
- Medium Power Consumption: 500 mW TYP.
- Two Chip Enable Inputs for Memory Expansion
- Open-Collector Output (μPB406, μPB406 E)/Three-State Outputs (μPB426, μPB426-E)
- Ceramic 18-Lead Dual In-Line Package
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: Intersil's IM56S06/56S26 (both in programming and as a ROM), Harris' HPROM HM-7642/7643 and Equivalent Devices (as a ROM)
- A.I.M. (Avalanche Induced Migration) Technology

PIN CONFIGURATION



OPERATION

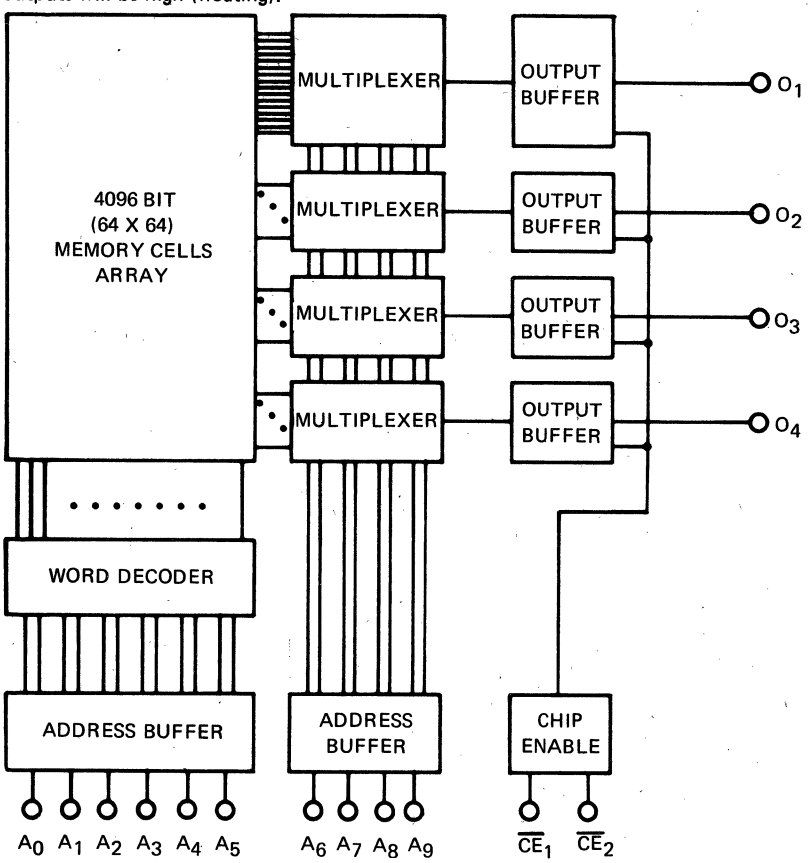
Programming

A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the ten address inputs in TTL levels. Either or both of the two chip enable inputs must be at a logic one (high). Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

To read the memory, both of the two chip enable inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip enable inputs are at logic one (high), all the outputs will be high (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−25°C to +75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +65°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IL}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$	40			μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = −2.4 mA
Output Short Circuit Current①	$-I_{SC}$	15		60	mA	V_O = 0V

NOTE: ① Applicable to μPB426D only.

AC CHARACTERISTICS

T_a = 25°C, V_{CC} = 5.0V

PARAMETER	SYMBOL	LIMITS 406-E/426-E			LIMITS 406/426			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Address Access Time	t_{AA}			100		40	70	ns	
Chip Enable Access Time	t_{ACE}			70			40	ns	
Chip Enable Disable Time	t_{DCE}			70			40	ns	

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

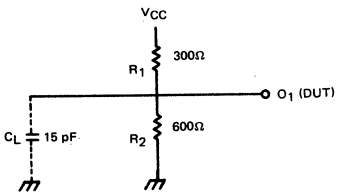
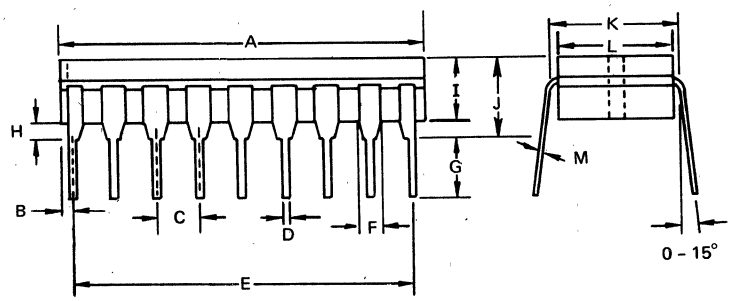


Figure 1

PACKAGE OUTLINE μPB406/426D



ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB406 and μPB426. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state. Either or both of the two chip enable inputs must be at a logic one (high).

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

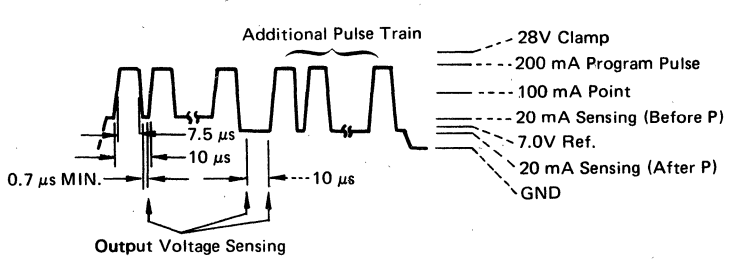


Figure 2 — Typical Output Voltage Waveform

FULLY DECODED 2048 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The μPD464 is a 2048 bit (256 x 8) mask programmable Read Only Memory. It is pin-for-pin compatible with NEC's Electrically Eraseable Programmable ROM (EEPROM), the μPD454. The μPD464 features high speed operation, making it suitable for large volume microcomputer memory applications that used the μPD464 for initial prototyping.

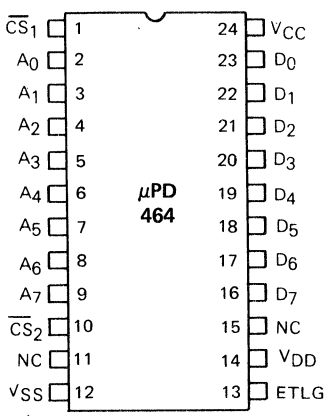
All inputs and outputs of the μPD464 are TTL compatible. Two chip select pins ($\overline{CS}_1$, $\overline{CS}_2$) are provided for selection of an individual device in systems with OR-tied outputs. Two power supplies, +12 volts and +5 volts, are required.

The μPD464 is fabricated using NEC's N-channel MOS silicon gate process, providing excellent contamination protection. This process enables high performance, highly reliable MOS circuits to be produced. The μPD464 is packaged in a 24-pin ceramic or plastic dual-in-line package.

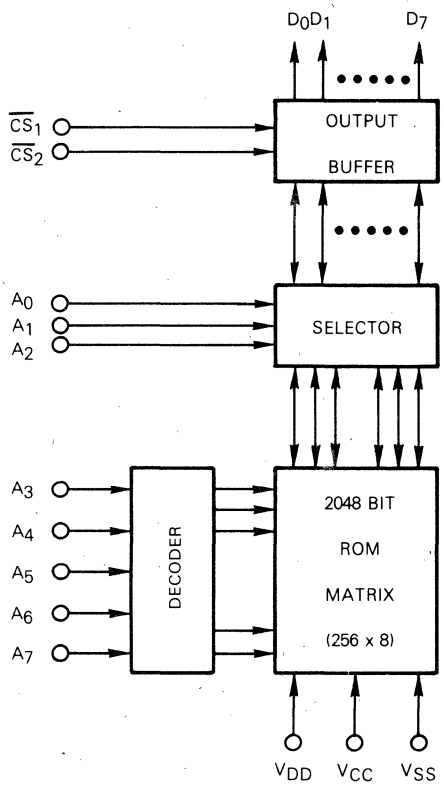
FEATURES

- Fully Decoded, 256 Words x 8 Bits Organization
- Access Time 450 ns Max.
- Static, No Clock Required
- Input/Output TTL Compatible
- Three-State Output, OR-Tie Capability
- N-Channel MOS Fabrication
- Two Power Supplies, +12V and +5V
- 24 Pin Ceramic or Plastic DIP

PIN CONFIGURATION



BLOCK DIAGRAM



PIN IDENTIFICATION

PIN			
NO.	SYMBOL	NAME	FUNCTION
1	$\overline{CS_1}$ ①	CHIP SELECT 1	Chip selection, active low
2–9	A_0–A_7	ADDRESS BUS	Memory address
10	$\overline{CS_2}$ ①	CHIP SELECT 2	Chip selection, active low
11	NC		No connection
12–13	V_{SS}	GROUND	Ground Reference
14	V_{DD}	+12V Power Supply	Power Supply
15	NC		No connection
16–23	D_7–D_0	Data output	Data Output
24	V_{CC}	+5V Power Supply	Power Supply

Note: ① Chip is selected only when both $\overline{CS_1}$ and $\overline{CS_2}$ are low.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−0.3 to +7 Volts
All Input Voltages	−0.3 to +7 Volts
Supply Voltage V_{DD}	−0.3 to +15 Volts
Supply Voltage V_{CC}	−0.3 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{DD} = +12V \pm 5\%$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	+2.4		V_{CC}	V	
Input Low Voltage	V_{IL}	-0.3		+ 0.7	V	
Output High Voltage	V_{OH}	+3.5			V	$I_{OH} = -1.0$ mA
Output Low Voltage	V_{OL}			0.5	V	$I_{OL} = +1.7$ mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = +2.4V$
Input Leakage Current Low	I_{LIL}			-10	μA	$V_I = +0.7V$
Output Leakage Current High	I_{LOH}			+10	μA	$V_O = +3.5V$
Output Leakage Current Low	I_{LOL}			-10	μA	$V_O = +0.4V$
V_{DD} Supply Current	I_{DD}		35	55	mA	
V_{CC} Supply Current	I_{CC}		20	30	mA	

CAPACITANCE

$T_a = -10°C$ to $+70°C$; $V_{DD} = +12V \pm 5\%$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

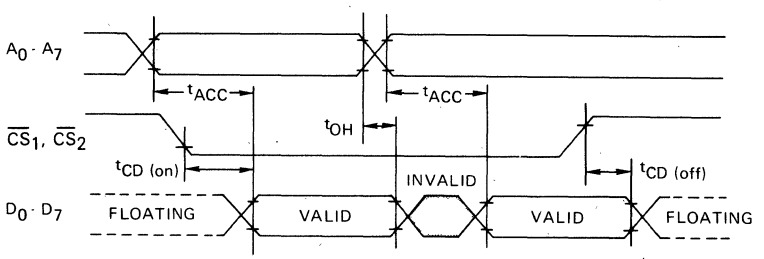
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}		6	15	pF	f = 1 MHz
Output Capacitance	C_{OUT}		8	15	pF	f = 1 MHz

AC CHARACTERISTICS

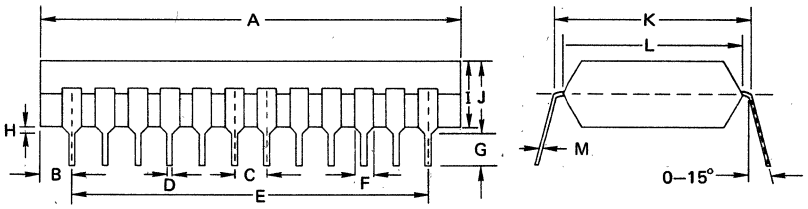
$T_a = -10°C$ to $+70°C$; $V_{DD} = +12V \pm 5\%$; $V_{CC} = +5V \pm 5\%$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Access Time	t_{ACC}			450	ns	1 TTL + 100 pF
$\overline{CS}$ to Output On Delay	t_{CD} (on)			250	ns	
$\overline{CS}$ to Output Off Delay	t_{CD} (off)	0		250	ns	
Output Hold Time	t_{OH}	20			ns	

TIMING WAVEFORM

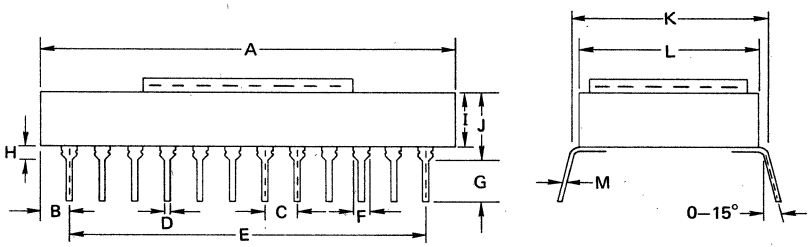


PACKAGE OUTLINE
μPD464C/D



μPD464C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD464D (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

FULLY DECODED 8192 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

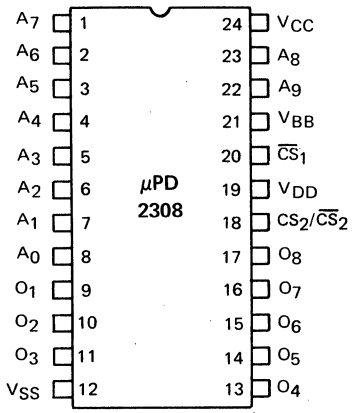
The NEC μPD2308 is a high speed 8,192 bit mask programmable Read Only Memory organized as 1024 words by 8 bits. The μPD2308 is fabricated with N-channel MOS technology.

Two Chip Selects are provided – $\overline{CS}_1$ which is negative true, and $CS_2/\overline{CS}_2$ which may be programmed either negative or positive true at the mask level.

FEATURES

- 1024 Words by 8 bits Organization
- Fast Access – 450 ns max
- Two Chip Select Inputs for Easy Memory Expansion
- TTL Compatible – All Inputs and Outputs
- Three State Output – OR-Tie Capability
- Fully Decoded
- Standard Power Supplies – +12V, ±5V
- 24 Pin Plastic or Ceramic Dual-in-Line Package
- Pin Compatible with INTEL 8308

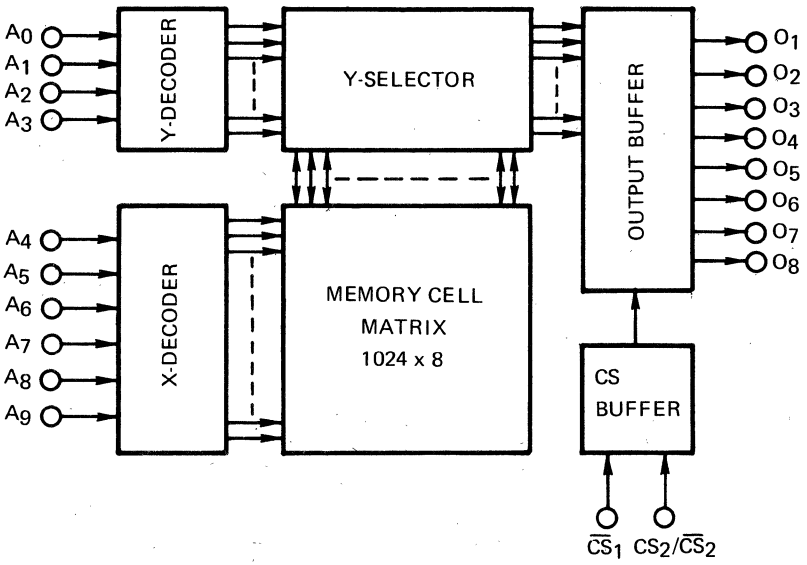
PIN CONFIGURATION



PIN NAMES

$A_0 - A_9$	Address Inputs
$\overline{CS}_1$	Chip Select 1
$CS_2/\overline{CS}_2$	Chip Select 2
$O_1 - O_8$	Data Outputs

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Input Voltages	−1 to +7 Volts ①
All Output Voltages	−1 to +7 Volts ①
Supply Voltage V_{DD}	−1 to +15 Volts ①
Supply Voltage V_{CC}	−1 to +7 Volts ①
Supply Voltage V_{BB}	−2 to −8 Volts

Note: ① V_{BB} = −5.25 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{DD} = +12V±5%, V_{CC} = +5V±5%, V_{BB} = −5V±5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current (All Input Pins)	I_{LI}			±10	μA	V_I = 0 to 5.25V
Output Leakage Current	I_{LO}			±10	μA	V_O = 0–5.25V Chip Deselected
Input Low Voltage	V_{IL}	V_{SS} −1		0.8	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 1.0	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −4 mA
Output High Voltage	V_{OH2}	3.7			V	I_{OH} = −1 mA
Power Supply Current V_{CC}	I_{CC}		14	30	mA	
Power Supply Current V_{DD}	I_{DD}		15	30	mA	
Power Supply Current V_{BB}	I_{BB}			−1	mA	
Power Dissipation	P_D			545	mW	

Note: Typical values are for T_a = 25°C and nominal supply voltage.

CAPACITANCE

T_a = 25°C; V_{BB} = −5V; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			6	pF	V_{DD}, V_{CC} and all other pins tied to V_{SS}
Output Capacitance	C_{OUT}			12	pF	

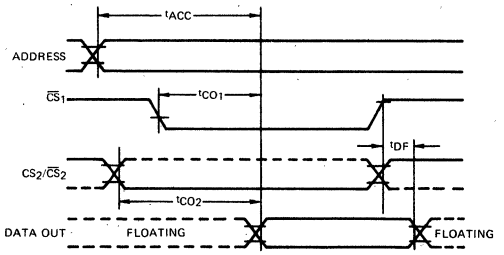
AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = 0V$

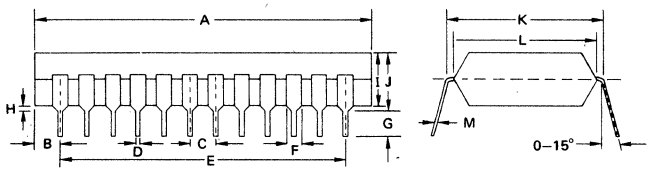
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Address to Output Delay Time	t_{ACC}		250	450	ns	$t_T = t_R = t_F = 20$ ns $V_{REF} = 2.4V, 0.8V$ $V_{IN} = 0.65V, 3.3V$ LOAD = 1 TTL GATE $C_L = 100$ pF
Chip Select 1 to Output Delay Time	t_{CO_1}		125	200	ns	
Chip Select 2 to Output Delay Time	t_{CO_2}		140	220	ns	
Chip Deselect to Output Float Time	t_{DF}		140	220	ns	

Note: Typical values are for $T_a = 25°C$ and nominal supply voltage.

TIMING WAVEFORMS

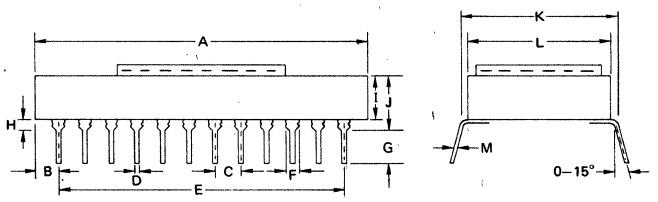


PACKAGE OUTLINE μPD2308C/D



μPD2308C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD2308D (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

FULLY DECODED 16,384 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

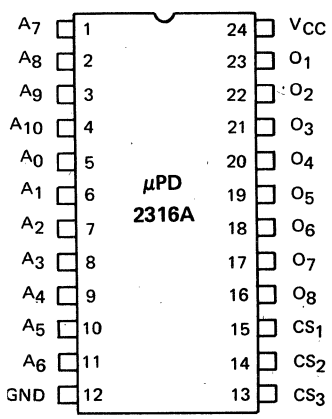
The NEC μPD2316A is a high speed 16,384 bit mask programmable Read Only Memory organized as 2048 words by 8 bits. The μPD2316A is fabricated with N-channel MOS technology.

The inputs and outputs are fully TTL compatible. The device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and desired chip select code is fixed during the masking process.

FEATURES

- Access Time 450 ns Max
- 2048 Words x 8 Bits Organization
- Single +5V Power Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Three Programmable Chip Select Inputs for Easy Memory Expansion
- Three-State Output — OR-Tie Capability
- On Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Direct Replacement for Intel 2316A/8316A
- Available in 24-pin plastic or ceramic package.

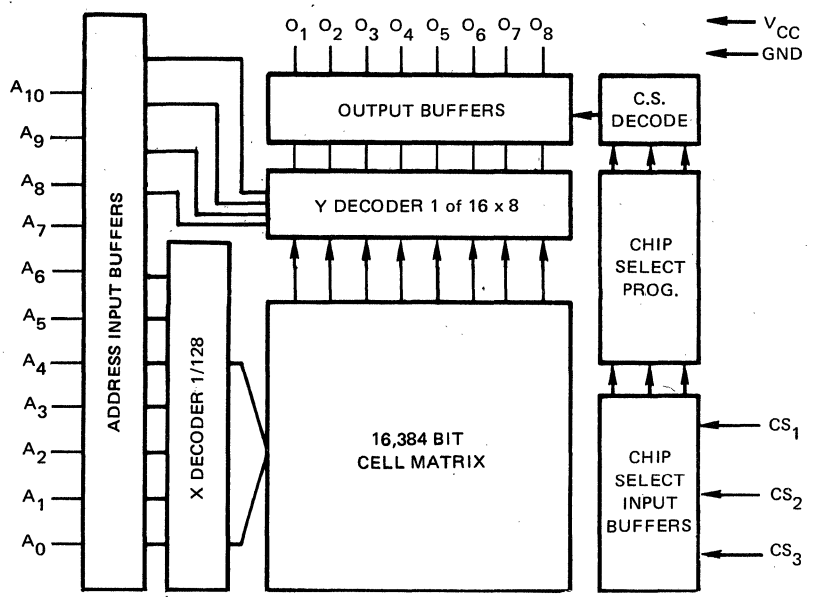
PIN CONFIGURATION



PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_8$	Data Outputs
$CS_1 - CS_2$	Programmable Chip Select Inputs

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Voltage on Any Pin . . . . . −0.5 to +7.0 Volts ①

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5 ± 5% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP ①	MAX		
Input Load Current (All Input Pins)	I_{LI}		1	10	μA	V_{IN} = 0 to 5.25V
Output Leakage Current	I_{LOH}			10	μA	CS = 2.2V (Deselected) V_{OUT} = V_{CC}
Output Leakage Current	I_{LOL}			−10	μA	CS = 2.2V (Deselected) V_{OUT} = 0V
Power Supply Current	I_{CC}			104	mA	All inputs 5.25V Data Out Open
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = 200μA

Note: ① Typical values for T_a = 25°C and nominal supply voltage.

CAPACITANCE

$T_a = 25°C$; f = 1 MHz

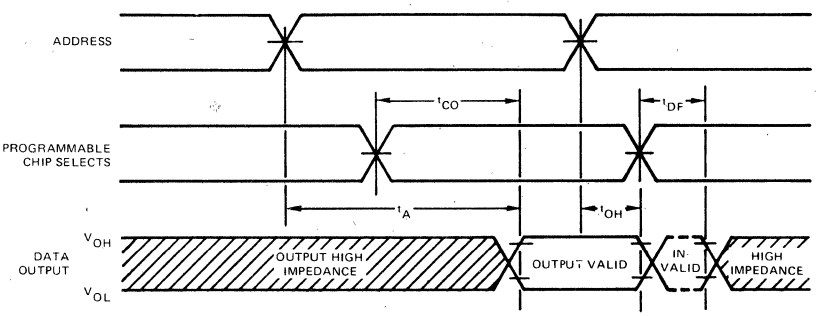
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pf	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pf	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

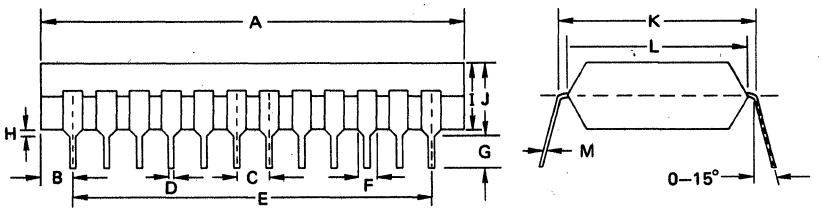
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	$t_T = t_r = t_f = 20$ ns $V_{ref\ in} = 1.5V$ $V_{ref\ out} = .45, 2.2V$ Output LOAD = 1 TTL GATE $C_L = 100$ pf
Chip Select to Output Enable Delay Time	t_{CO}			150	ns	
Chip Deselect to Output Data Float Delay Time	t_{DF}	0		150	ns	
Output Hold Time	t_{OH}	20			ns	

TIMING WAVEFORMS



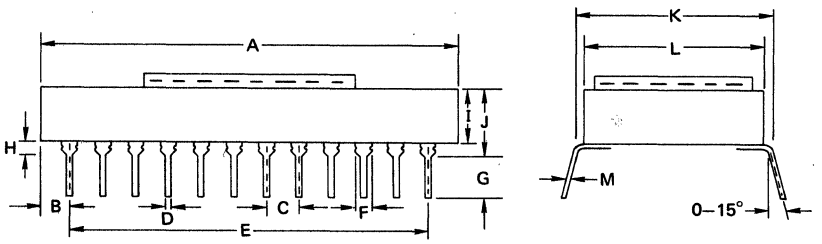
4

PACKAGE OUTLINE
μPD2316AC/D



μPD2316AC (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD2316AD (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

FULLY DECODED 32,768 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD2332 is a Fully Decoded 32,768 Bit Mask Programmable Read-Only Memory organized as 4,096 Words by 8 Bits. The μPD2332 has two chip select inputs and the combination of "High"/"Low" levels of these inputs is mask-programmable.

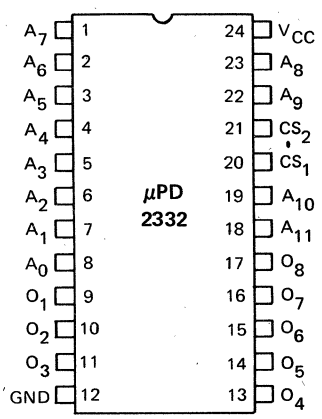
The μPD2332 is fabricated with sophisticated N-channel MOS technology and features high speed and TTL compatibility for simple interface with bipolar circuits.

FEATURES

- 4096 Words x 8 Bits Organization
- Directly TTL Compatible — All Inputs and Outputs
- Fully Static (No Clock or Refresh Required)
- Single +5V Power Supply
- High Speed — Access Time 450 ns Max.
- Three-State Output — OR-Tie Capability
- Two Programmable Chip Select Inputs for Easy Memory Expansion
- N-Channel MOS Technology
- Pin Compatible with TI TMS4732
- 24 Pin Plastic or Ceramic Dual-in-Line Package

4

PIN CONFIGURATION



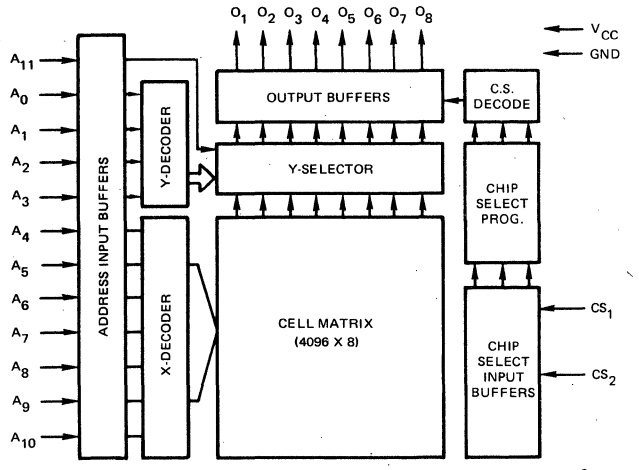
PIN NAMES

$A_0 - A_{11}$	Address Inputs
$O_1 - O_8$	Data Outputs
$CS_1 - CS_2$	Programmable Chip Select Inputs

When ordering the μPD2332, specify a chip select combination of CS_1 and CS_2 from the following.

CS_2	CS_1
0	0
0	1
1	0
1	1

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Supply Voltage On Any Pin . . . . . −0.5 to +7.0 Volts①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	
Output Leakage Current	I_{LOH}			+10	μA	CS = 2.2V (Deselected) V_{OUT} = V_{CC}
Output Leakage Current	I_{LOL}			−10	μA	CS = 2.2V (Deselected) V_{OUT} = 0V
Power Supply Current	I_{CC}		55	110	mA	All inputs 5.25V Data Out Open
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = −100 μA

Note: ① Typical Values for T_a = 25°C and nominal supply voltages.

CAPACITANCE

T_a = 25°C; f = 1 MHz

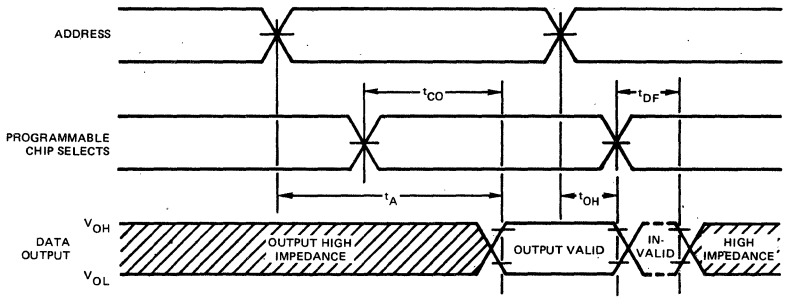
PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

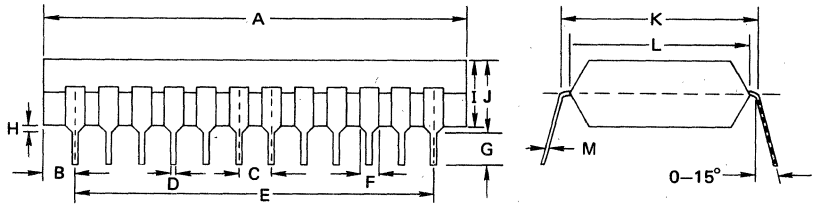
T_a = −10°C to +70°C, V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	t_T = t_r = t_f = 20 ns
Chip Select to Output Enable Delay Time	t_{CO}			150	ns	C_L = 100 pF
Chip Deselect to Output Data Float Delay Time	t_{DF}	0		150	ns	Load = ITTL gate
Output Hold Time	t_{OH}	20			ns	V_{IN} = 0.8 to 2V V_{ref} Input = 1.5V V_{ref} Output = 0.45/2.2V

TIMING WAVEFORMS

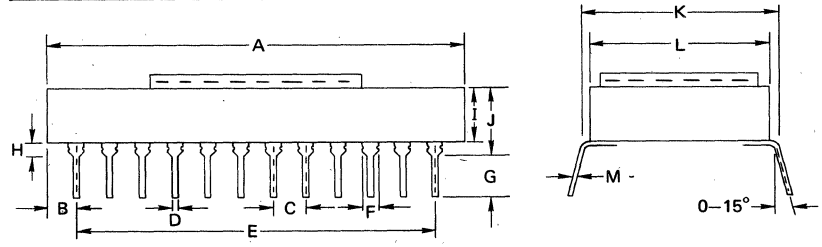


PACKAGE OUTLINE μPD2332C/D



μPD2332C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD2332D (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

CUSTOM MASK ROM DEVICES

- FLEXIBILITY ON MASK FORMAT

NEC Microcomputers, Inc. is able to accept mask patterns for its custom mask ROM devices in a variety of formats which suit different customer needs without any loss in turnaround time. Among the formats included are:

- Sample ROMs
- Prototype PROMs (2708's, 1702's, etc.)
- BNPF Paper Tapes
- HEX Paper Tapes
- Cassette Tapes
- Timesharing Files

- SPEED OF COMPUTERIZED LINK WITH FACTORY

Earth satellites and the world-wide GE Mark III timesharing system provide the reliable and instant communication of ROM mask patterns to factory. Likewise, patterns may be returned for verification the same day. Customers who are GE-TSS users may entirely avoid format problems by transferring files directly.

- RELIABILITY OF VERIFICATION PROCEDURES

Thoroughly tested verification procedures protect against unnecessary delays or costly mistakes. NEC Microcomputers, Inc. has the technical staff and facilities to return ROM mask patterns to the customer in the format most convenient to him. Sample devices may also be provided prior to full production delivery to assure that the device is entirely satisfactory before a production commitment.

NEC microcomputers, inc.

PRELIMINARY

μPD414A
μPD414A-1
μPD414A-2
μPD414A-3

4K BIT DYNAMIC RAM

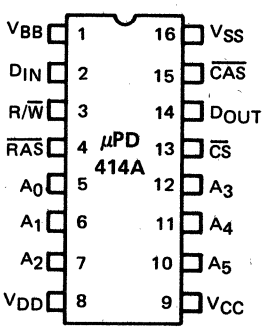
DESCRIPTION

The NEC μPD414A is a 4096 words by 1 bit dynamic Random Access Memory fabricated with N-channel MOS technology. It features high performance, low power, and 16 pin packaging for high system bit density. The 12 bit address is multiplexed into the chip in two 6 bit halves. Flexible I/O control allows common or separate I/O data busses.

FEATURES

- Four speeds: 300 ns (μPD414A)
  250 ns (μPD414A-1)
  200 ns (μPD414A-2)
  150 ns (μPD414A-3)
- ±10% Supply Tolerance
- Gated $\overline{CAS}$ Operation
- Latched Output
- Three State Output
- Fully TTL Compatible
- Replacement for 4027 Type Devices

PIN CONFIGURATION



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NEC microcomputers, inc.

PRELIMINARY

μPD6508
μPD6508-1

1K (1024x1) STATIC CMOS RAM

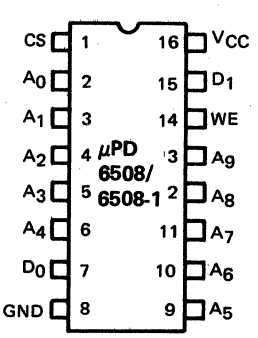
DESCRIPTION

The NEC μPD6508/6508-1 are high speed, low power, silicon gate CMOS RAMs organized as 1024 words by 1 bit. It features extremely low power requirements and data retention to +3 volts V_{CC}.

FEATURES

- Extremely Low Power Operation
- High Speed – 250 ns Max (μPD6508-1)
- TTL Compatible, All Inputs and Outputs
- Static Operation
- On Chip Register Address
- Replacement for 5608 Type Devices

PIN CONFIGURATION



NEC microcomputers, inc.

PRELIMINARY

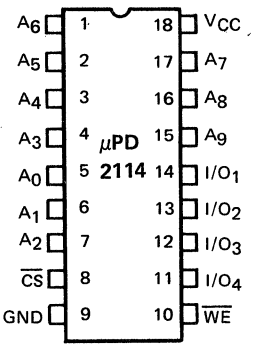
μPD2114

4K (1024x4) STATIC RAM

DESCRIPTION

The NEC μPD2114 is a 4096 bit, fully static Random Access Memory, organized as 1024 words by 4 bits. It is fabricated with N-channel silicon gate technology and is housed in an 18 pin package for high system bit densities.

PIN CONFIGURATION



FEATURES

- High Density 18 Pin Package
- Completely Static
- Directly TTL Compatible — All Inputs and Outputs
- Single +5V Supply
- Low Operating Power — 0.06 mW/Bit Typ
- Access Time — 250 ns Typical

NEC microcomputers, inc.

PRELIMINARY

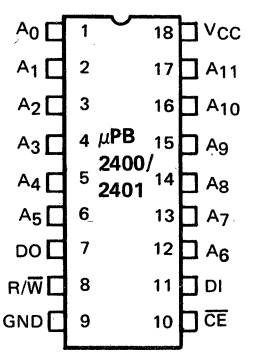
μPB2400
μPB2401

4096 BIT STATIC BIPOLAR RAM

DESCRIPTION

The NEC μPB2400 and μPB2401 are static, Random Access Memories organized as 4096 words by 1 bit. The devices feature operation from a single +5 volt supply, and are fully TTL compatible. Fast data out disable time allows a common I/O data bus structure.

PIN CONFIGURATION



FEATURES

- 4096 Words x 1 Bit Organization
- Fast Read and Write Cycle — 75 ns Typ
- Low Power Operation — 500 mW Typ
- Single +5 Volt Supply
- 18 Pin Cerdip Package
- Latched Data Outputs
- Three State (μPB2401) or Open Collector (μPB2400) Output
- Replacement for 74S400/401

PRELIMINARY

μPD4104

4096 × 1 STATIC NMOS RAM

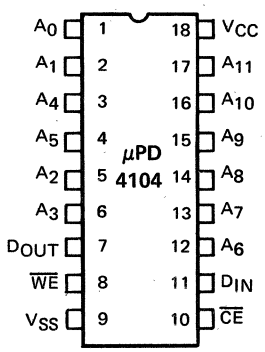
DESCRIPTION

The NEC μPD4104 is a high speed 4096 bit Static RAM organized as 4096 words by 1 bit. The use of static storage circuitry eliminates the need for refresh while the dynamic control circuitry provides substantially lower power dissipation than fully static types.

FEATURES

- Fast Access Time — 200 ns
- High System Density — 18 Pin Package
- Fully TTL Compatible — All Inputs and Outputs
- Single +5V Supply

PIN CONFIGURATION



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NEC microcomputers, inc.

PRELIMINARY

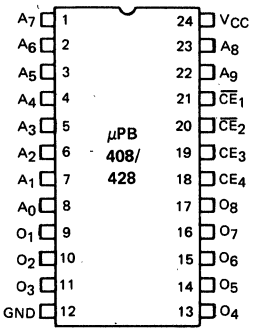
μPB408
μPB428

8192 BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPB408 and μPB428 are high speed, electrically programmable, 8192 bit, TTL, Read Only Memories. Three chip enable inputs and three state (μPB428) or open collector (μPB408) outputs allow OR-tying outputs for ease of memory expansion. The devices are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the desired bit locations.

PIN CONFIGURATION



FEATURES

- 1024 Words x 8 Bits Organization
- Fast Access Time - 85 ns Max
- Three State (μPB428) or Open Collector (μPB408) Outputs
- Replacement for 6380/6381 Type Devices

NEC microcomputers, inc.

PRELIMINARY

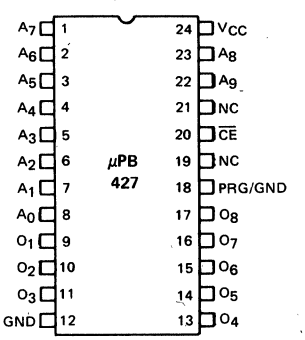
μPB427

8192 BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPB427 is a high speed, electrically programmable, 8192 bit, TTL, Read Only Memory. Three-state outputs and a chip enable input allow easy expansion of memory capacity. The μPB427 is fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the desired bit locations.

PIN CONFIGURATION



FEATURES

- 1024 Words x 8 Bits Organization
- Fast Read Access Time - 120 ns Max
- Power Switching - 750 mW Max Selected
  - 350 mW Max Unselected
- Three State Outputs
- Replacement for 2708 Type Devices as a ROM

NEC microcomputers, inc.

PRELIMINARY

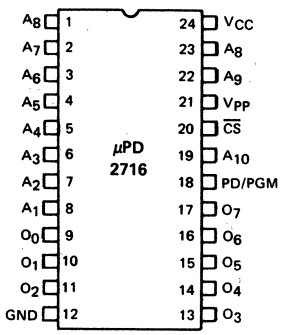
μPD2716

16K ULTRAVIOLET ERASABLE PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD2716 is a 16,384 bit ultraviolet erasable and electrically programmable Read Only Memory organized as 2048 words by 8 bits. Its 450 ns access time and single +5 volt supply make it ideal for microprocessor applications.

PIN CONFIGURATION



FEATURES

- Single +5 Volt Supply (Read Mode)
- Simple Programming
- Inputs and Outputs TTL Compatible in Read and Program Mode
- Low Power - 525 mW Max Active
  - 132 mW Max Standby

5

NEC microcomputers, inc.

PRELIMINARY

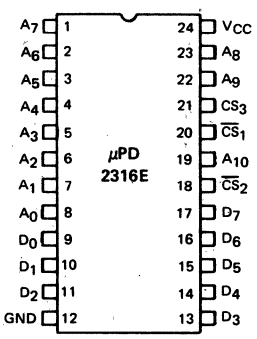
μPD2316E

16K (2048x8) MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

The NEC μPD2316E is a high speed 16,384 bit mask programmable Read Only Memory organized as 2148 words by 8 bits. All inputs and outputs are fully TTL compatible. These devices operate with a single +5V supply. The three chip select inputs are programmable; any combination of active high or low level chip select inputs can be defined and fixed during the masking process.

PIN CONFIGURATION



FEATURES

- Access Time - 450 ns Max
- 2048 Words x 8 Bits Organization
- Single +5V Supply
- Directly TTL Compatible
- Three Programmable Chip Selects
- Three State Outputs — OR-Tie Capabilities
- Direct Replacement for 2316E Type Devices

MICROCOMPUTER INDEX

μCOM-4

Processors

μCOM-8

Processors

Peripherals

New Products

New Families

μCOM-8 MICROCOMPUTER SELECTION GUIDE

DEVICE	PRODUCT	SIZE	TECHNOLOGY	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
			MICROPROCESSORS				
μPD8080A	Microprocessor (Enhanced)	8 bit	NMOS	3-state	2 MHz	+12, ±5	40
μPD8080AF	Microprocessor (Compatible)	8 bit	NMOS	3-state	2 MHz	+12, ±5	40
μPD8080AF-2	Microprocessor (Compatible)	8 bit	NMOS	3-state	2.5 MHz	+12, ±5	40
μPD8080AF-1	Microprocessor (Compatible)	8 bit	NMOS	3-state	3.0 MHz	+12, ±5	40
			RAMs				
μPD410	Static RAM	4096 x 1	NMOS	3-state	100 ns – 200 ns	+12, ±5	22
μPD5101	Static RAM	256 x 4	CMOS	3-state	800 ns	+5	22
μPD2101AL	Static RAM	256 x 4	NMOS	3-state	250 ns – 450 ns	+5	22
μPD2102AL	Static RAM	1024 x 1	NMOS	3-state	250 ns – 450 ns	+5	16
μPD2111AL	Static RAM	256 x 4	NMOS	3-state	250 ns – 450 ns	+5	18
μPD2114(F)	Static RAM	1024 x 4	NMOS	3-state	200 ns – 450 ns	+5	18
μPD411A	Dynamic RAM	4096 x 1	NMOS	3-state	200 ns – 350 ns	+12, ±5	22
μPD411	Dynamic RAM	4096 x 1	NMOS	3-state	150 ns – 350 ns	+12, ±5	22
μPD414	Dynamic RAM	4096 x 1	NMOS	3-state	200 ns – 350 ns	+12, ±5	16
μPD416	Dynamic RAM	16K x 1	NMOS	3-state	150 ns – 350 ns	+12, ±5	16
μPD418	Dynamic RAM	4096 x 1	NMOS	3-state	200 ns – 300 ns	+12, –5	18
			ROMs				
μPD464	Mask ROM	256 x 8	NMOS	3-state	450 ns	+12, +5	24
μPD2308	Mask ROM	1024 x 8	NMOS	3-state	450 ns	+12, ±5	24
μPD2316A	Mask ROM	2048 x 8	NMOS	3-state	450 ns	+5	24
μPD2332	Mask ROM	4096 x 8	NMOS	3-state	450 ns	+5	24
			PROMs				
μPB405/25	Field Programmable ROM	512 x 8	Bipolar	Open Collec. 3-state	70 ns	+5	24
μPD454	Electrically Erasable Programmable ROM	256 x 8	NMOS	3-state	800 ns	+12, +5*	24
μPD458	Electrically Erasable Programmable ROM	1024 x 8	NMOS	3-state	450 ns	+12, +5*	28

(F) Future Product
* Read Mode

μCOM-8 MICROCOMPUTER SELECTION GUIDE

DEVICE	PRODUCT	SIZE	TECHNOLOGY	OUTPUT	CYCLE	SUPPLY VOLTAGES	PINS
			SYSTEM SUPPORT				
μPD371	Tape Cassette Controller	8 bit	NMOS	3-state	2 MHz	+12, ±5	42
μPD372	Floppy Disk Controller	8 bit	NMOS	3-state	2 MHz	+12, ±5	42
μPD379	Synchronous Receiver/ Transmitter	8 bit	NMOS	3-state	800K baud	+12, ±5	42
μPD758	Seiko Printer Controller (#EP-101)	4 bit	NMOS	3-state	1 MHz	+12, ±5	42
μPD764	Seiko Printer Controller (#CR-330)	4 bit	NMOS	3-state	1 MHz	+5	42
μPB8212	I/O Port	8 bit	Bipolar	3-state	—	+5	24
μPB8214	Priority Interrupt Controller	3 bit	Bipolar	Open Collec.	3 MHz	+5	24
μPB8216	Bus Driver Non-Inverting	4 bit	Bipolar	3-state	—	+5	16
μPB8224	Clock Generator/ Driver	—	Bipolar	Hi-Level Clock	—	+12, +5	16
μPB8226	Bus Driver Inverting	4 bit	Bipolar	3-state	—	+5	16
μPB8228	System Controller	8 bit	Bipolar	3-state	—	+5	28
μPB8238	System Controller	8 bit	Bipolar	3-state	—	+5	28
μPD8251	Programmable Communication Interface (ASYNC/SYNC)	8 bit	NMOS	3-state	A9.6K baud S56K baud	+5	28
μPD8253(F)	Programmable Timer	8 bit	NMOS	3-state	2 MHz	+5	24
μPD8255	Peripheral Interface	8 bit	NMOS	3-state	—	+5	40
μPD8257	Programmable DMA Controller	8 bit	NMOS	3-state	3 MHz	+5	40
μPD8259(F)	Programmable Interrupt Controller	8 bit	NMOS	3-state	—	+5	28

(F) Future Product

μCOM-4 MICROCOMPUTER SELECTION GUIDE

DEVICE	PRODUCT	ROM	RAM	I/O	INTERRUPT LEVELS	INSTRUCTIONS	CYCLE	SUPPLY VOLTAGES	PINS
				MICROPROCESSORS					
μPD548	μCOM-42 CPU	1920 x 10	96 x 4	35	2	72	10 μs	-10	42
μPD546	μCOM-43 CPU	2000 x 8	96 x 4	35	1	80	10 μs	-10	42
μPD547	μCOM-44 CPU	1000 x 8	64 x 4	35	1	58	10 μs	-10	42
μPD550	μCOM-45 CPU	640 x 8	32 x 4	21	1	58	10 μs	-10	28
μPD555	μCOM-42 Evachip	—	96 x 4	36	2	72	10 μs	-10	64
μPD556	μCOM-43 Evachip	—	96 x 4	36	1	80	10 μs	-10	64

MICROCOMPUTER ALTERNATE SOURCE GUIDE

MANUFACTURER	PART NUMBER	DESCRIPTION	NEC REPLACEMENT
AMD	AM8080A/9080A	Microprocessor (2.0 MHz)	μPD8080AF
	AM8080A-2/9080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	AM8080A-1/9080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	AM8085	Microprocessor	μPD8085
	AM8155	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155
	AM8212	I/O Port (8-Bit)	μPB8212
	AM8214	Priority Interrupt Controller	μPB8214
	AM8216	Bus Driver, Non-Inverting	μPB8216
	AM8224	Clock Generator/Driver	μPB8224
	AM8226	Bus Driver, Inverting	μPB8226
	AM8228	System Controller	μPB8228
	AM8238	System Controller	μPB8238
	AM8251	Programmable Communications I/F, (Async/Sync)	μPD8251
	AM8255	Programmable Peripheral I/F	μPD8255
	AM8257	Programmable DMA Controller	μPD8257
	AM8355	Programmable Peripheral Interface with 2K x 8 ROM	μPD8257
Intel	8080A	Microprocessor (2.0 MHz)	μPD8080AF
	8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	8035	Microprocessor	μPD8035
	8048	Microprocessor with ROM	μPD8048
	8085	Microprocessor	μPD8085
	8155	Programmable Peripheral Interface with 256 x 8 RAM	μPD8155
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8224	Clock Generator/Driver	μPB8224
	8226	Bus Driver, Inverting	μPB8226
	8228	System Controller	μPB8228
	8238	System Controller	μPB8238
	8251	Programmable Communications I/F, (Async/Sync)	μPD8251
	8253	Programmable Timer	μPD8253
	8255	Programmable Peripheral Interface	μPD8255
	8255A	Programmable Peripheral Interface	μPD8255A
	8257	Programmable DMA Controller	μPD8257
	8259	Programmable Interrupt Controller	μPD8259
	8355	Programmable Peripheral Interface with 2K x 8 ROM	μPD8355
	8748	Microprocessor with EPROM	μPD8748
	8755	Programmable Peripheral Interface with 2K x 8 EPROM	μPD8755
National	INS8080A	Microprocessor (2.0 MHz)	μPD8080AF
	INS8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	INS8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	8212	I/O Port (8-Bit)	μPB8212
	8214	Priority Interrupt Controller	μPB8214
	8216	Bus Driver, Non-Inverting	μPB8216
	8224	Clock Generator/Driver	μPB8224
	8226	Bus Driver, Inverting	μPB8226
	8228	System Controller	μPB8228
	8238	System Controller	μPB8238
	INS8251	Programmable Communications I/F, (Async/Sync)	μPD8251
	INS8255	Programmable Peripheral Interface	μPD8255
T.I.	TMS8080A	Microprocessor (2.0 MHz)	μPD8080AF
	TMS8080A-2	Microprocessor (2.5 MHz)	μPD8080AF-2
	TMS8080A-1	Microprocessor (3.0 MHz)	μPD8080AF-1
	SN74S412	I/O Port (8-Bit)	μPB8212
	SN74LS424	Clock Generator/Driver	μPB8224
	SN74S428	System Controller	μPB8228
	SN74S438	System Controller	μPB8238

NEC microcomputers, inc.

INTRODUCING THE μCOM-4 FAMILY — A LINE OF SINGLE CHIP 4-BIT MICROCOMPUTERS

In order to provide the power of microcomputers to the cost sensitive consumer/controller markets, NEC Microcomputers, Inc. offers a family of low cost, powerful 4-bit parallel single chip microcomputers. All of these devices contain on-chip read-only-memory (ROM) for program storage, data storage memory (RAM) and extensive input/output capability.

The family is divided into two applications areas. The μCOM-42 microcomputer's architecture and instruction set is designed to facilitate its use in Electronic Cash Register (ECR)/Scale products. The μCOM-43/44/45 microcomputers are designed for general purpose controller applications and are ideal devices for industrial controls, appliance controls, games, etc.

Both families are supported by NEC's high volume production capability, evaluation chips and evaluation kits, PDA-80 software development system and extensive documentation.

μCOM-42

DESCRIPTION

The μCOM-42 (Part No. μPD548C) is a single chip microcomputer that is ideally suited for Electronic Cash Register (ECR), Point of Sale (POS) and Electronic Scale applications.

Containing a 4-bit Parallel ALU, ROM for program storage and RAM for data storage, the μCOM-42 provides an economical and simple solution to many Vending/Calculating requirements.

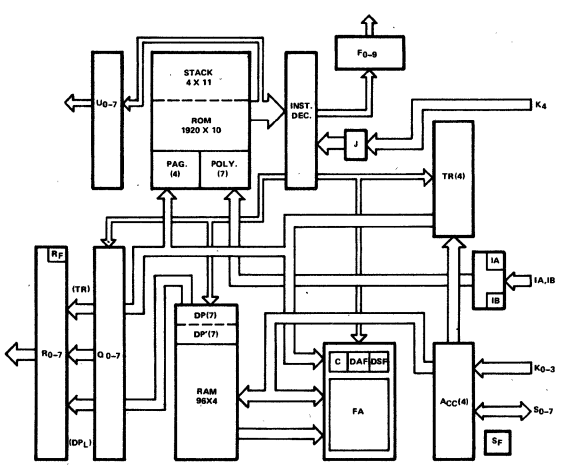
Because of its extensive instruction set and five input/output ports, the μCOM-42 is capable of controlling an 8 x 4 keyboard, an 8 digit display and low cost ECR-type printers.

Finally, the on-chip RAM space can be augmented by an external μPD5101 CMOS RAM (256 x 4 bits) for applications requiring low power data retention.

FEATURES

- Stand alone 4-bit microcomputer
- All 72 instructions are single byte
- 10 μsec instruction cycle
- 1920 x 10-bit program memory (ROM)
- 96 x 4-bit data memory (RAM)
- 4-level stack
- 2 Interrupt request lines
- I/O compatible with TTL
- 10 discrete output ports ($F_0 - F_9$)
- Two 8-bit output ports ($U_0 - U_7$, $R_0 - R_7$)
- One 4-bit input port ($K_0 - K_3$)
- One 4-bit input/output port ($S_0 - S_3$)
- One single bit testable input port (K_4)
- Single phase TTL level clock (200 KHz max.)
- Single supply, −10V PMOS technology
- 42 pin plastic dual-in-line package

BLOCK DIAGRAM μCOM-42 (μPD548C)



μCOM-43

DESCRIPTION

The μCOM-43 (Part No. μPD546C) is a 4-bit parallel microcomputer that is especially suited for a wide range of low cost, sophisticated controller applications.

The μPD546C contains all the functional blocks necessary to enable its use for both industrial and non-industrial controller applications. These blocks include: a 4-bit parallel ALU; 2K by 8-bit ROM for program storage; 96 x 4-bit RAM for data storage; 35 input/output lines; a programmable interval timer; interrupt capability; and on-board clock generator.

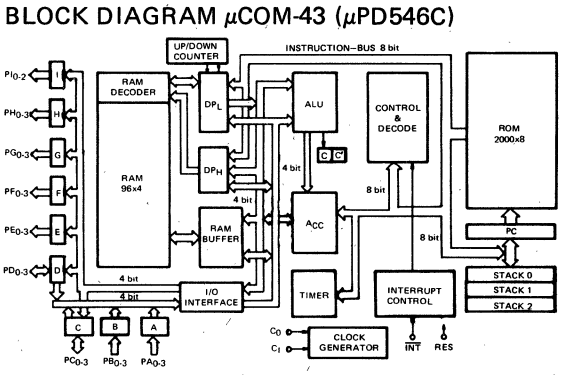
The 80 instructions of the μCOM-43 are designed to perform controller oriented functions and for efficient use of the program memory space. These 80 instructions include a number of multi-function instructions, powerful I/O instructions including single bit manipulation, and test-and-skip instructions for conditional processing.

Thus, the μCOM-43's large ROM memory, extensive I/O, and other hardware features in combination with its powerful instruction set opens up new areas for inexpensive yet sophisticated controllers.

FEATURES

- Stand alone 4-bit microcomputer for control applications
- 80 powerful instructions capable of: binary addition; decimal addition and subtraction; and logical operations
- 10 μsec instruction cycle
- 2000 x 8-bit program memory (ROM)
- 96 x 4-bit data memory (RAM)
- 35 input/output lines consisting of: two 4-bit input ports, two 4-bit input/output ports, four 4-bit output ports, one 3-bit output port. All capable of both single bit manipulation and 4-bit parallel processing
- 3-level stack
- Six 4-bit working registers
- Hardware interrupt including enable/disable capability
- On-chip programmable interval timer
- On-chip clock generator
- Open drain, TTL compatible outputs
- Single supply, −10V PMOS technology
- 42 pin plastic dual-in-line package

BLOCK DIAGRAM μCOM-43 (μPD546C)



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μCOM-44

DESCRIPTION

The μCOM-44 (Part No. μPD547C) is a 4-bit parallel microcomputer that is ideally suited for a wide range of low cost, general purpose controller applications.

The μPD546C contains all the functional blocks needed for a low cost, stand alone, high volume controller. These blocks include: a 4-bit parallel ALU; 1K by 8-bit ROM for program storage; 64 by 4-bit RAM for data storage; 35 input/output lines; interrupt capability and an on-board clock generator.

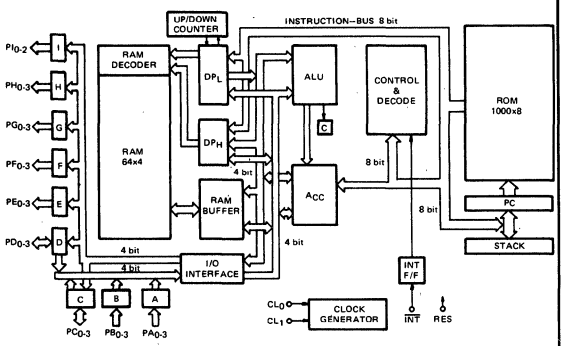
The 58 instructions of the μCOM-44 are designed to perform controller oriented functions and for efficient use of the program memory space. These 58 instructions include a number of multi-functional instructions, powerful I/O instructions including single bit manipulation, and test-and-skip instructions for conditional processing.

The μCOM-44 is ideally suited for consumer/industrial controller functions because of its extensive I/O, on-board ROM/RAM space and its powerful instruction set.

FEATURES

- Stand alone 4-bit microcomputer for control applications
- 58 powerful instructions capable of:
  Binary addition; decimal addition and subtraction; and logical operations
- 10 μsec instruction cycle
- 1000 x 8-bit program memory (ROM)
- 64 x 4-bit data memory (RAM)
- 35 Input/Output lines consisting of:
  Two 4-bit input ports
  Two 4-bit input/output ports
  Four 4-bit output ports
  One 3-bit output port
  All capable of both single bit manipulation and 4-bit parallel processing
- Single level stack
- On-chip clock generator
- Open drain, TTL compatible outputs
- Single supply, −10V PMOS technology
- 42 pin plastic dual-in-line package

BLOCK DIAGRAM μCOM-44 (μPD547C)



μCOM-45

DESCRIPTION

The μCOM-45 (Part No. μPD550C) is a single chip microcomputer designed for extremely low cost, general purpose controller/consumer/ appliance applications.

The μPD550C contains all the system blocks necessary to build an inexpensive, yet fully functional controller. The blocks include: a 4-bit parallel ALU; 640 by 8-bit ROM for program storage; 32 by 4-bit RAM for data storage; 21 input/output lines; interrupt capability and an on-board clock generator.

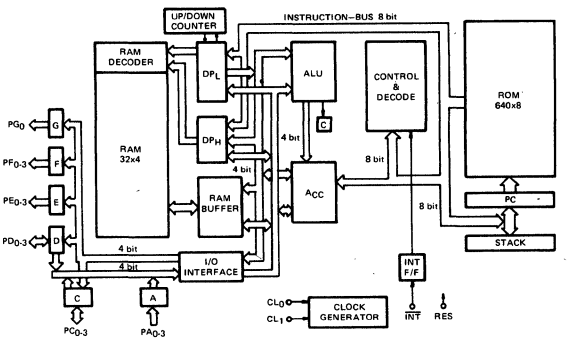
The 58 instructions of the μCOM-45 are designed to perform controller oriented functions and for efficient use of the program memory space. These 58 instructions include a number of multi-functional instructions, powerful I/O instructions including single bit manipulation, and test-and-skip instructions for conditional processing.

The μCOM-45 opens up entire new areas of controller applications because of its extremely low cost and powerful functions.

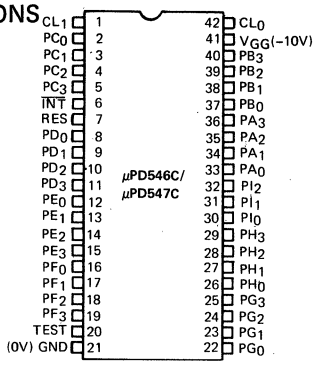
FEATURES

- Stand alone 4-bit microcomputer for consumer/control applications
- 58 powerful instructions capable of:
  Binary addition; decimal addition and subtraction; and logical operations
- 10 μsec instruction cycle
- 640 x 8-bit program memory (ROM)
- 32 x 4-bit data memory (RAM)
- 21 Input/Output lines consisting of:
  One 4-bit input port
  Two 4-bit input/output ports
  Two 4-bit output ports
  One 1-bit output port
  All capable of both single bit manipulation and 4-bit parallel processing
- Single level stack
- On-chip clock generator
- Open drain, TTL compatible outputs capable of −35V
- Single Supply, −10V PMOS technology
- 28 pin plastic dual-in-line package

BLOCK DIAGRAM μCOM-45 (μPD550C)

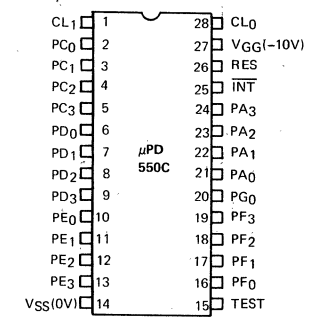


μCOM-43/44/45 PIN CONFIGURATIONS



PIN NAMES

CL_0–CL_1	External Clock Source
PC_0–PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
TEST	Input for Testing (Normally GND)
PG_0–PG_3	Output Port G
PH_0–PH_3	Output Port H
PI_0–PI_3	Output Port I
PA_0–PA_3	Input Port A
PB_0–PB_3	Input Port B



PIN NAMES

CL_0–CL_1	External Clock Source
PC_0–PC_3	Input/Output Port C
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
PG_0	Output Port G
PA_0–PA_3	Input Port A
$\overline{INT}$	Interrupt Input
RES	Reset

μCOM-43/44/45 INSTRUCTION SETS

①	②	③	④	⑤
CLA	1	1	$A_{CC} \leftarrow 0$	
CMA	1	1	$A_{CC} \leftarrow (\overline{A_{CC}})$	
CIA	1	1	$A_{CC} \leftarrow (\overline{A_{CC}})+1$	
INC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+1$ skip if Carry	Carry
DEC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})-1$ skip if Borrow	Borrow
CLC	1	1	$C \leftarrow 0$	
STC	1	1	$C \leftarrow 1$	
XC	1	1	$(C) \rightleftharpoons (C')$	
RAR	1	1	$(A_{CCn-1}) \leftarrow (A_{CCn})$ $C \leftarrow (A_{CC0})$, $(A_{CC3}) \leftarrow (C)$	
INM	1	1/2-3	$[(DP)] \leftarrow [(DP)]+1$ skip if $[(DP)]=0$	$[(DP)]=0$
DEM	1	1/2-3	$[(DP)] \leftarrow [(DP)]-1$ skip if $[(DP)]=F$	$[(DP)]=F$
AD	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+[(DP)]$ skip if Carry	Carry
ADS	1	1/2-3	$A_{CC}, C \leftarrow (A_{CC})+[(DP)]+(C)$ skip if Carry	Carry
ADC	1	1	$A_{CC}, C \leftarrow (A_{CC})+[(DP)]+(C)$	
DAA	1	1	$A_{CC} \leftarrow (A_{CC})+6$	
DAS	1	1	$A_{CC} \leftarrow (A_{CC})+10$	
EXL	1	1	$A_{CC} \leftarrow (A_{CC}) \forall [(DP)]$	
LI	1	1	$A_{CC} \leftarrow I_3I_2I_1I_0$	
S	1	1	$[(DP)] \leftarrow (A_{CC})$	
L	1	1	$A_{CC} \leftarrow [(DP)]$	
LM	1	1	$A_{CC} \leftarrow [(DP)]$ $DP_H \leftarrow (DP_H) \forall 0M_1M_0$	
X	1	1	$(A_{CC}) \rightleftharpoons [(DP)]$	
XM	1	1	$(A_{CC}) \rightleftharpoons [(DP)]$ $DP_H \leftarrow (DP_H) \forall 0M_1M_0$	
XD	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$ $DP_L \leftarrow (DP_L)-1$ skip if $(DP_L)=F$	$(DP_L)=F$
XMD	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$ $DP_H \leftarrow (DP_H) \forall 0M_1M_0$ $DP_L \leftarrow (DP_L)-1$ skip if $(DP_L)=F$	$(DP_L)=F$

①	②	③	④	⑤
XI	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$ $DP_L \leftarrow (DP_L)+1$ skip if $(DP_L)=0$	$(DP_L)=0$
XMI	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$ $DP_H \leftarrow (DP_H) \forall 0M_1M_0$ $DP_L \leftarrow (DP_L)+1$ skip if $(DP_L)=0$	$(DP_L)=0$
LDI	2	2	$DP \leftarrow I_6-I_0$	
LDZ	1	1	$DP_H \leftarrow 0$ $DP_L \leftarrow I_3I_2I_1I_0$	
DED	1	1/2-3	$DP_L \leftarrow (DP_L)-1$ skip if $(DP_L)=F$	$(DP_L)=F$
IND	1	1/2-3	$DP_L \leftarrow (DP_L)+1$ skip if $(DP_L)=0$	$(DP_L)=0$
TAL	1	1	$DP_L \leftarrow (A_{CC})$	
TLA	1	1	$A_{CC} \leftarrow (DP_L)$	
XHX	1	2	$(X) \rightleftharpoons (DP_H)$	
XLY	1	2	$(Y) \rightleftharpoons (DP_L)$	
THX	1	2	$X \leftarrow (DP_H)$	
TLY	1	2	$Y \leftarrow (DP_L)$	
XAZ	1	2	$(Z) \rightleftharpoons (A_{CC})$	
XAW	1	2	$(W) \rightleftharpoons (A_{CC})$	
TAZ	1	2	$Z \leftarrow (A_{CC})$	
TAW	1	2	$W \leftarrow (A_{CC})$	
XHR	1	2	$(R) \rightleftharpoons (DP_H)$	
XLS	1	2	$(S) \rightleftharpoons (DP_L)$	
SMB	1	1	$[(DP,B_1B_0)] \leftarrow 1$	
RMB	1	1	$[(DP,B_1B_0)] \leftarrow 0$	
TMB	1	1/2-3	skip if $[(DP,B_1B_0)]=1$	$[(DP,B_1B_0)]=1$
TAB	1	1/2-3	skip if $(A_{CC}(B_1B_0))=1$	$(A_{CC}(B_1B_0))=1$
CMB	1	1/2-3	skip if $(A_{CC}(B_1B_0))$ $= [(DP,B_1B_0)]$	$(A_{CC}(B_1B_0))$ $=[(DP,B_1B_0)]$
SFB	1	2	FLAG $(B_1B_0) \leftarrow 1$	
RFB	1	2	FLAG $(B_1B_0) \leftarrow 0$	
FBT	1	2/3-4	skip if (FLAG $(B_1B_0))=1$	(FLAG$(B_1B_0))=1$
FBF	1	2/3-4	skip if (FLAG $(B_1B_0))=0$	(FLAG$(B_1B_0))=0$
CM	1	1/2-3	skip if $(A_{CC})=[(DP)]$	$(A_{CC}) = [(DP)]$
CI	2	2/3-4	skip if $(A_{CC})=I_3I_2I_1I_0$	$(A_{CC})=I_3I_2I_1I_0$
CLI	2	2/3-4	skip if $(DP_L)=I_3I_2I_1I_0$	$(DP_L)=I_3I_2I_1I_0$

①	②	③	④	⑤
TC	1	1/2-3	skip if (C)=1	(C)=1
TIT	1	1/2-3	skip if (INT F/F)=1 INT F/F←0	(INT F/F)=1
JCP	1	1	$PC_{5-0} \leftarrow P_5-P_0$	
JMP	2	2	$PC \leftarrow P_{10}-P_0$	
JPA	1	2	$PC_{5-0} \leftarrow A_3A_2A_1A_000$	
EI	1	1	INTE F F←1	
DI	1	1	INTE F F←0	
CZP	1	1	STACK←(PC) $PC \leftarrow 00000P_3P_2P_1P_000$	
CAL	2	2	STACK←(PC) $PC \leftarrow P_{10}-P_0$	
RT	1	2	PC←(STACK)	
RTS	1	3-4	PC←(STACK) PC←(PC)+1,2	Unconditional
STM	2	2	TM F F←0 $TIMER \leftarrow I_5-I_0$	
TTM	1	1/2-3	skip if (TM F/F)=1	(TM F/F)=1
SEB	1	2	PORT E $(B_1B_0) \leftarrow 1$	
REB	1	1	PORT E $(B_1B_0) \leftarrow 0$	
SPB	1	1	PORT $(DP_L,B_1B_0) \leftarrow 1$	
RPB	1	1	PORT $(DP_L,B_1B_0) \leftarrow 0$	
TPA	1	2/3-4	skip if (PORT A $(B_1B_0))=1$	(PORT A $(B_1B_0))$ = 1
TPB	1	1/2-3	skip if (PORT (DL_L,B_1B_0) =1	(PORT $(DP_L$, $B_1B_0))=1$
OE	1	2	PORT E←(A_{CC})	
OP	1	1	PORT $(DP_L) \leftarrow (A_{CC})$	
OCD	2	2	PORT C,D←I_7-I_0	
IA	2	2	$A_{CC} \leftarrow$(PORT A)	
IP	1	1	$A_{CC} \leftarrow$(PORT (DP_L))	
NOP	1	1	No Operation	

Notes: ① MNEMONIC
② BYTES
③ CYCLES
④ DESCRIPTION
⑤ CONDITION FOR SKIP
☐ These Instructions Apply Only to the μCOM-43.

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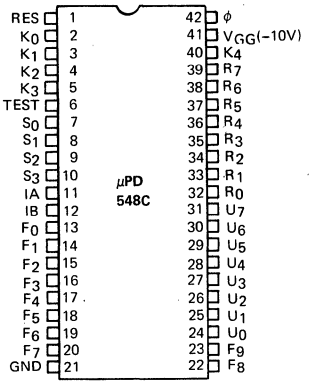
μCOM-42 PIN CONFIGURATION



PIN NAMES

RES	Reset
K_0–K_3	Input Port K
TEST	Input for Testing (Normally V_{GG})
S_0–S_3	Input/Output Port S
IA, IB	Interrupt Input Ports
F_0–F_9	Output Port F
U_0–U_7	Output Port U
R_0–R_7	Output Port R
K_4	Input Port for Condition Test
ϕ	Clock Input

μCOM-42 INSTRUCTION SET

①	②	③	④
CMA	1	$A_{CC}\leftarrow(\overline{A_{CC}})$	
CIA	1	$A_{CC}\leftarrow(\overline{A_{CC}})+1$	
INA	1/2	$A_{CC}\leftarrow(A_{CC})+1$	Carry=1
DEA	1/2	$A_{CC}\leftarrow(A_{CC})-1$	Borrow≠1
RFC	1	C←0	
SFC	1	C←1	
DSM	1	Decimal Subtract Mode	
DAM	1	Decimal Add Mode	
AD	1/2	$A_{CC}\leftarrow(A_{CC})+[DP]$	Carry=1
ADC	1	A_{CC},C←$(A_{CC})+[DP]+(C)$	
ADI	1/2	$A_{CC}\leftarrow(A_{CC})+I_3I_2I_1I_0$	Carry=1
LM	1	$A_{CC}\leftarrow[DP]$ $DP_H\leftarrow(DP_H)\veebar M_2M_1M_0$	
XM	1	$(A_{CC})\leftrightarrow[DP]$ $DP_H\leftarrow(DP_H)\veebar M_2M_1M_0$	
XMI	1/2	$(A_{CC})\leftrightarrow[DP]$ $DP_H\leftarrow(DP_H)\veebar M_2M_1M_0$ $DP_L\leftarrow(DP_L)+1$	(DP_L)=8 or (DP_L)=0
XMD	1/2	$(A_{CC})\leftrightarrow[DP]$ $DP_H\leftarrow(DP_H)\veebar M_2M_1M_0$ $DP_L\leftarrow(DP_L)-1$	(DP_L)=F or (DP_L)=7
LI	1	$A_{CC}\leftarrow I_3I_2I_1I_0$	
LDI	1	$DP\leftarrow I_6$–I_0	
IND	1/2	$DP_L\leftarrow(DP_L)+1$	(DP_L)=8 or (DP_L)=0
DED	1/2	$DP_L\leftarrow(DP_L)-1$	(DP_L)=F or (DP_L)=7
XDP	1	(DP)↔(DP')	
ZAG	1	$000DP_L\leftarrow(DP)$	

①	②	③	④
XTA	1	$(A_{CC})\leftrightarrow(TR)$	
LTI	1	$TR\leftarrow I_3I_2I_1I_0$	
QS1	1	$Q_{n+1}\leftarrow Q_n,Q_0\leftarrow 1$	
QS0	1	$Q_{n+1}\leftarrow Q_n,Q_0\leftarrow 0$	
SB	1	$[DP,B_1,B_0]\leftarrow 1$	
RB	1	$[DP,B_1,B_0]\leftarrow 0$	
SBT	1/2	Skip if $[DP,B_1,B_0]=1$	B_1B_0=1
SC	1/2	Skip if (C)=1	(C)=1
SEM	1/2	Skip if $(A_{CC})=[DP]$	$(A_{CC})=[DP]$
SEI	1/2	Skip if $(A_{CC})=I_3I_2I_1I_0$	$(A_{CC})=I_3I_2I_1I_0$
SK4	1/2	Skip if K_4=1	K_4=1
JPT	1	$PC\leftarrow(TR),P_{6-0}$	
JPA	1	$PC_{6-4}\leftarrow P_{6-4}$ $PC_{3-0}\leftarrow P_{3-0}\vee(A_{CC})$	
JCP	1	$PC_{6-0}\leftarrow P_{6-0}$	
CAL	1	[STACK]←(PC) $PC\leftarrow 1000P_6P_5P_4P_3P_2P_1P_0$	
RT	1	PC←[STACK]	
RTS	2	PC←[STACK] PC←(PC)+1	
EIA	1	Enable IA port	
DIA	1	Disable IA port	
EIB	1	Enable IB port	
DIB	1	Disable IB port	
OIU	1	$U_{7-0}\leftarrow I_{7-0}$ $R_{7-0}\leftarrow(Q_{7-0})$	
ERO	1	Enable R port	
DRO	1	Disable R port	

①	②	③
OQR	1	R←(Q)
OTR	1	$R_{7-4}\leftarrow(TR),R_{3-0}\leftarrow(DP_L)$
SFS	1	S←(A_{CC})
RFS	1	S port Input Mode
IS	1	$A_{CC}\leftarrow S$
IK	1	$A_{CC}\leftarrow K$
RF1	1	$F_1\leftarrow 0$
SF1	1	$F_1\leftarrow 1$
RF2	1	$F_2\leftarrow 0$
SF2	1	$F_2\leftarrow 1$
RF3	1	$F_3\leftarrow 0$
SF3	1	$F_3\leftarrow 1$
RF4	1	$F_4\leftarrow 0$
SF4	1	$F_4\leftarrow 1$
RF5	1	$F_5\leftarrow 0$
SF5	1	$F_5\leftarrow 1$
RF6	1	$F_6\leftarrow 0$
SF6	1	$F_6\leftarrow 1$
RF7	1	$F_7\leftarrow 0$
SF7	1	$F_7\leftarrow 1$
RF8	1	$F_8\leftarrow 0$
SF8	1	$F_8\leftarrow 1$
RF9	1	$F_9\leftarrow 0$
SF9	1	$F_9\leftarrow 1$
RF0	1	$F_0\leftarrow 0$
SF0	1	$F_0\leftarrow 1$
NOP	1	No Operation

Notes: ① **MNEMONIC**
② **CYCLES**
③ **DESCRIPTION**
④ **CONDITION FOR SKIP**

DEVELOPMENT TOOLS

The μCOM-4 microcomputer family is fully supported with all the necessary hardware and software development tools. These tools include assemblers, evaluation chips and evaluation kits.

For software development, cross-assemblers that run on our 8080A-based PDA-80 are available along with support documentation. The PDA-80 allows the user to program PROMs directly without having to use a paper tape medium.

For hardware and software development, evaluation kits and evaluation chips are available. The EVACHIPS (μPD555D for the μCOM-42 and μPD556D for the μCOM-43/44/45) have all the functional capabilities of their production equivalents, except they do not contain on-chip ROM. Instead they have the ability to address external memory. In addition, they give the designer the ability to single step through his program in order to ease debugging.

The evaluation kits (EVAKIT-42 and EVAKIT-43), using the appropriate EVACHIP, provide the designer with a single pc board containing: LED's for display of internal registers and instruction code; switches for setting breakpoints; on-board PROM sockets; and reset and single-step capability. The combination of EVAKIT and EVACHIP give the μCOM-4 system designer all the tools needed for initial design/debugging and prototype fabrication.

For further information, contact: NEC microcomputers, inc.

μPD8080AF 8-BIT N-CHANNEL MICROPROCESSOR FAMILY

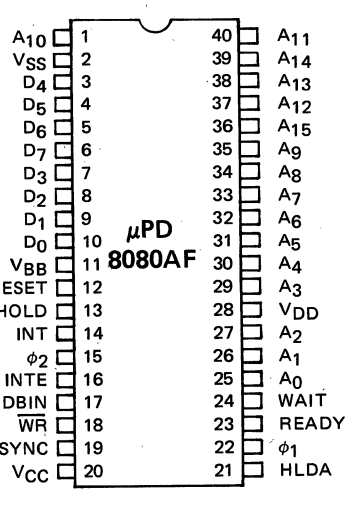
DESCRIPTION

The μPD8080AF is a complete 8-bit parallel processor for use in general purpose digital computer systems. It is fabricated on a single LSI chip using N-channel silicon gate MOS process, which offers much higher performance than conventional microprocessors (1.28 μs minimum instruction cycle). A complete microcomputer system is formed when the μPD8080AF is interfaced with I/O ports (up to 256 input and 256 output ports) and any type or speed of semiconductor memory. It is available in a 40 pin ceramic or plastic package.

FEATURES

- 78 Powerful Instructions
- Three Devices — Three Clock Frequencies
  μPD8080AF — 2.0 MHz
  μPD8080AF-2 — 2.5 MHz
  μPD8080AF-1 — 3.0 MHz
- Direct Access to 64K Bytes of Memory with 16-Bit Program Counter
- 256 8-Bit Input Ports and 256 8-Bit Output Ports
- Double Length Operations Including Addition
- Automatic Stack Memory Operation with 16-Bit Stack Pointer
- TTL Compatible (Except Clocks)
- Multi-byte Interrupt Capability
- **Fully** Compatible with Industry Standard 8080A
- Available in either Plastic or Ceramic Package

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The μPD8080AF contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8080AF also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8080AF utilizes a 16-bit address bus to directly address 64K bytes of memory, is fully TTL compatible (1.9 mA), and utilizes the following addressing modes: Direct; Register; Register Indirect; and Immediate.

The μPD8080AF has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8080AF also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

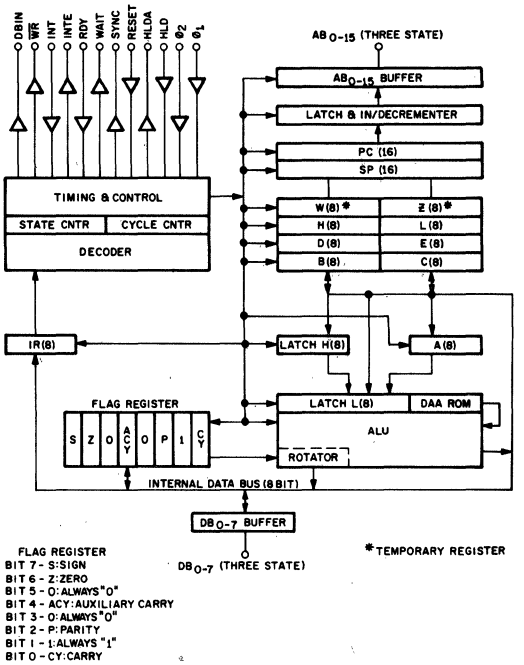
This processor is designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data busses are employed to allow direct interface to memories and I/O ports. Control signals, requiring no decoding, are provided directly by the processor. All busses, including the control bus, are TTL compatible.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address and data lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8080AF has the capability to accept a multiple byte instruction upon an interrupt. This means that a CALL instruction can be inserted so that any address in the memory can be the starting location for an interrupt program. This allows the assignment of a separate location for each interrupt operation, and as a result no polling is required to determine which operation is to be performed.

NEC offers three versions of the μPD8080AF. These processors have all the features of the μPD8080AF except the clock frequency ranges from 2.0 MHz to 3.0 MHz. These units meet the performance requirements of a variety of systems while maintaining software and hardware compatibility with other 8080A devices.

BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 25-27, 29-40	$A_{15} - A_0$	Address Bus (output three-state)	The address bus is used to address memory (up to 64K 8-bit words) or specify the I/O device number (up to 256 input and 256 output devices). A_0 is the least significant bit.
2	V_{SS}	Ground (input)	Ground
3-10	$D_7 - D_0$	Data Bus (input/ output three-state)	The bidirectional data bus communicates between the processor, memory, and I/O devices for instructions and data transfers. During each sync time, the data bus contains a status word that describes the current machine cycle. D_0 is the least significant bit.
11	V_{BB}	V_{BB} Supply Voltage (input)	−5V ± 5%
12	RESET	Reset (input)	If the RESET signal is activated, the program counter is cleared. After RESET, the program starts at location 0 in memory. The INTE and HLDA flip-flops are also reset. The flags, accumulator, stack pointer, and registers are not cleared. (Note: External synchronization is not required for the RESET input signal which must be active for a minimum of 3 clock periods.)
13	HOLD	Hold (input)	HOLD requests the processor to enter the HOLD state. The HOLD state allows an external device to gain control of the μPD8080AF address and data buses as soon as the μPD8080AF has completed its use of these buses for the current machine cycle. It is recognized under the following conditions: • The processor is in the HALT state. • The processor is in the T_2 or T_W stage and the READY signal is active. As a result of entering the HOLD state, the ADDRESS BUS ($A_{15} - A_0$) and DATA BUS ($D_7 - D_0$) are in their high impedance state. The processor indicates its state on the HOLD ACKNOWLEDGE (HLDA) pin.
14	INT	Interrupt Request (input)	The μPD8080AF recognizes an interrupt request on this line at the end of the current instruction or while halted. If the μPD8080AF is in the HOLD state, or if the Interrupt Enable flip-flop is reset, it will not honor the request.
15	ϕ_2	Phase Two (input)	Phase two of processor clock.
16	INTE ①	Interrupt Enable (output)	INTE indicates the content of the internal interrupt enable flip-flop. This flip-flop is set by the Enable (EI) or reset by the Disable (DI) interrupt instructions and inhibits interrupts from being accepted by the processor when it is reset. INTE is automatically reset (disabling further interrupts) during T_1 of the instruction fetch cycle (M_1) when an interrupt is accepted and is also reset by the RESET signal.
17	DBIN	Data Bus In (output)	DBIN indicates that the data bus is in the input mode. This signal is used to enable the gating of data onto the μPD8080AF data bus from memory or input ports.
18	$\overline{WR}$	Write (output)	$\overline{WR}$ is used for memory WRITE or I/O output control. The data on the data bus is valid while the $\overline{WR}$ signal is active ($\overline{WR}$ = 0).
19	SYNC	Synchronizing Signal (output)	The SYNC signal indicates the beginning of each machine cycle.
20	V_{CC}	V_{CC} Supply Voltage (input)	+5V ± 5%
21	HLDA	Hold Acknowledge (output)	HLDA is in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at: • T_3 for READ memory or input operations. • The clock period following T_3 for WRITE memory or OUTPUT operations. In either case, the HLDA appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.
22	ϕ_1	Phase One (input)	Phase one of processor clock.
23	READY	Ready (input)	The READY signal indicates to the μPD8080AF that valid memory or input data is available on the μPD8080AF data bus. READY is used to synchronize the processor with slower memory or I/O devices. If after sending an address out, the μPD8080AF does not receive a high on the READY pin, the μPD8080AF enters a WAIT state for as long as the READY pin is low. (READY can also be used to single step the processor.)
24	WAIT	Wait (output)	The WAIT signal indicates that the processor is in a WAIT state.
28	V_{DD}	V_{DD} Supply Voltage (input)	+12V ± 5%

Note: ① After the EI instruction, the μPD8080AF accepts interrupts on the second instruction following the EI. This allows proper execution of the RET instruction if an interrupt operation is pending after the service routine.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to + 70°C
Storage Temperature (Ceramic Package) ..... −65°C to +150°C
Storage Temperature (Plastic Package) ..... − 40°C to + 125°C
All Output Voltages ① ..... −0.3 to +20 Volts
All Input Voltages ① ..... −0.3 to +20 Volts
Supply Voltages V_{CC}, V_{DD} and V_{SS} ① ..... −0.3 to +20 Volts
Power Dissipation 1.5W

Note: ① Relative to V_{BB}.

COMMENT; Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

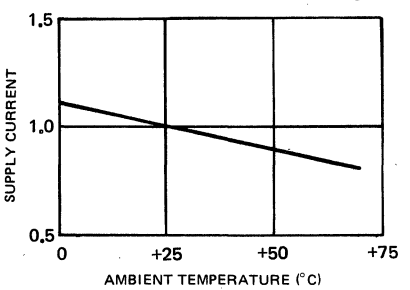
*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage	V_{ILC}	V_{SS} − 1		V_{SS} + 0.8	V	
Clock Input High Voltage	V_{IHC}	9.0		V_{DD} + 1	V	
Input Low Voltage	V_{IL}	V_{SS} − 1		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	3.3		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.9 mA on all outputs
Output High Voltage	V_{OH}	3.7			V	I_{OH} = −150 μA ②
Avg. Power Supply Current (V_{DD})	$I_{DD(AV)}$		40	70	mA	t_{CY} min
Avg. Power Supply Current (V_{CC})	$I_{CC(AV)}$		60	80	mA	
Avg. Power Supply Current (V_{BB})	$I_{BB(AV)}$		0.01	1	mA	
Input Leakage	I_{IL}			±10 ②	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Clock Leakage	I_{CL}			±10 ②	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
Data Bus Leakage in Input Mode	I_{DL} ①			−100 ②	μA	$V_{SS} \leq V_{IN} \leq V_{SS}$ + 0.8V
				−2 ②	mA	V_{SS} + 0.8V $\leq V_{IN} \leq V_{CC}$
Address and Data Bus Leakage During HOLD	I_{FL}			+10 ②	μA	$V_{ADDR/DATA} = V_{CC}$
				−100 ②		$V_{ADDR/DATA} = V_{SS}$ + 0.45V

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED ③



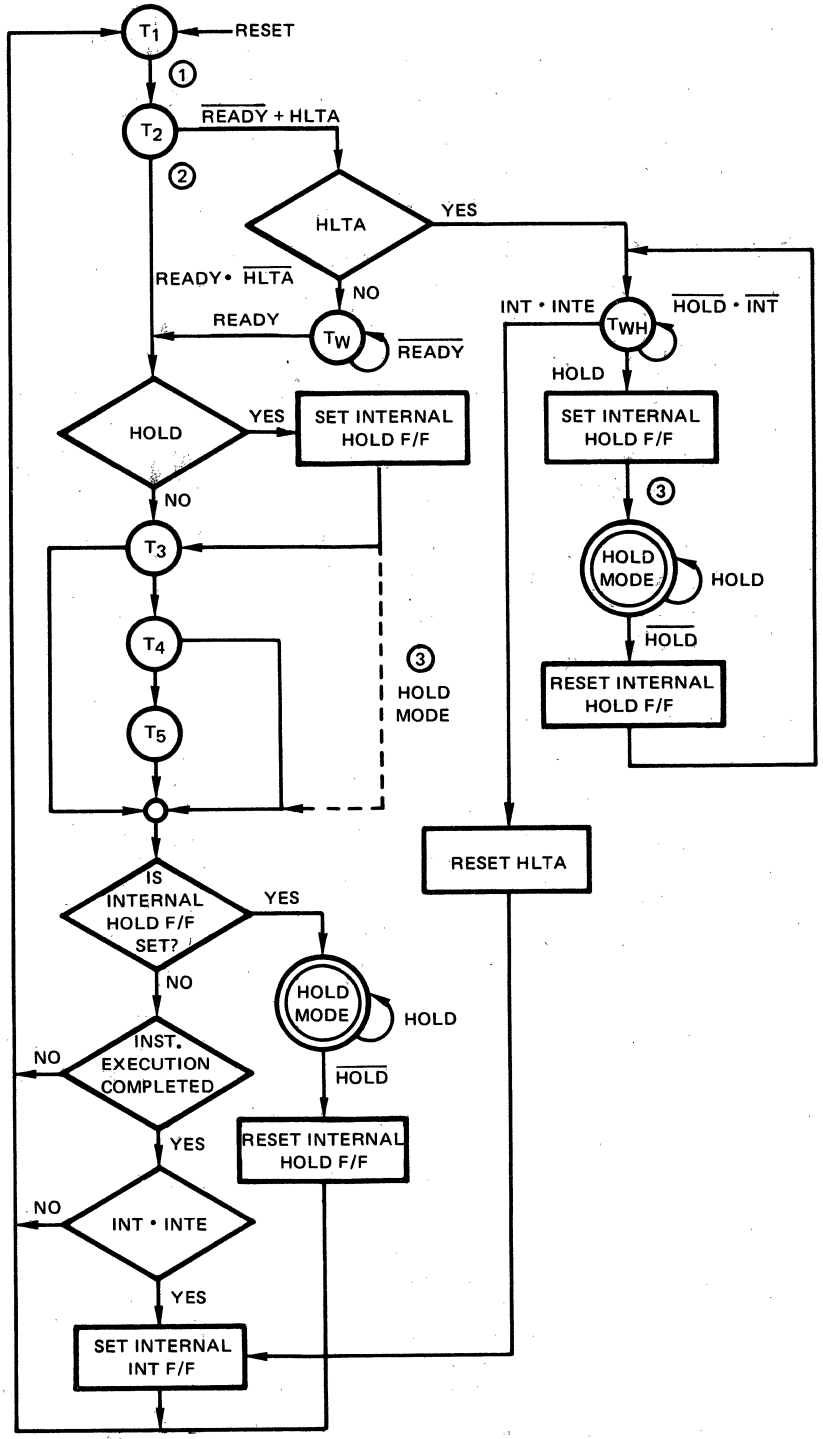
Notes: ① When DBIN is high and $V_{IN} > V_{IH}$ internal active pull-up resistors will be switched onto the data bus.
② Minus (−) designates current flow out of the device.
③ ΔI supply/ΔT_a = −0.45%/°C.

CAPACITANCE

T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = −5V.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ		17	25	pF	f_c = 1 MHz
Input Capacitance	C_{IN}		6	10	pF	Unmeasured Pins
Output Capacitance	C_{OUT}		10	20	pF	Returned to V_{SS}

PROCESSOR STATE TRANSITION DIAGRAM



Notes:
① INTE F/F IS RESET IF INTERNAL INT F/F IS SET.
② INTERNAL INT F/F IS RESET IF INTE F/F IS RESET.
③ IF REQUIRED, T_4 AND T_5 ARE COMPLETED SIMULTANEOUSLY WITH ENTERING HOLD STATE.

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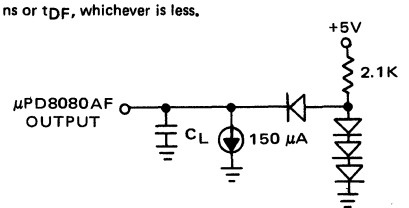
AC CHARACTERISTICS
μPD8080AF

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

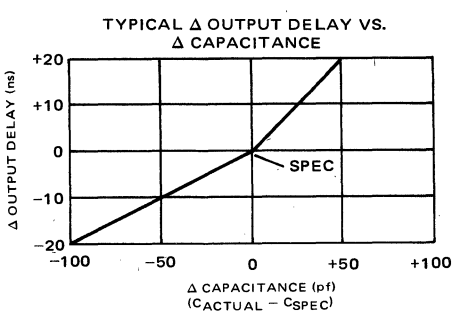
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.48		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	220			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	80			nsec	
Address Output Delay From φ2	t_{DA} ②			200	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			220	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	30			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	150			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	120			nsec	
HOLD Setup Time to φ2	t_{HS}	140			nsec	
INT Setup Time During φ2 (During φ1 in Halt Mode)	t_{IS}	120			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes: ① Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.

② Load Circuit.



③ Actual $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} > t_{CY}$ Min.



AC CHARACTERISTICS
μPD8080AF-2

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.38		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	175			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	70			nsec	
Address Output Delay From φ2	t_{DA} ②			175	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			200	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	20			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	130			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued:

④ The following are relevant when interfacing the μPD8080AF to devices having V_{IH} = 3.3V.

a. Maximum output rise time from 0.8V to 3.3V = 100 ns at C_L = SPEC.

b. Output delay when measured to 3.0V = SPEC +60 ns at C_L = SPEC.

c. If $C_L \neq$ SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.

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AC CHARACTERISTICS
μPD8080AF-1

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.32		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		25	nsec	
φ1 Pulse Width	$t_{\phi1}$	50			nsec	
φ2 Pulse Width	$t_{\phi2}$	145			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	60			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	60			nsec	
Address Output Delay From φ2	t_{DA} ②			150	nsec	C_L = 50 pF
Data Output Delay From φ2	t_{DD} ②			180	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			110	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		130	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	10			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	120			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 50 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued: ⑤

Device	t_{AW}
μPD8080AF	$2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$
μPD8080AF-2	$2\,t_{CY} - t_{D3} - t_{r\phi2} - 130$
μPD8080AF-1	$2\,t_{CY} - t_{D3} - t_{r\phi2} - 110$

⑥

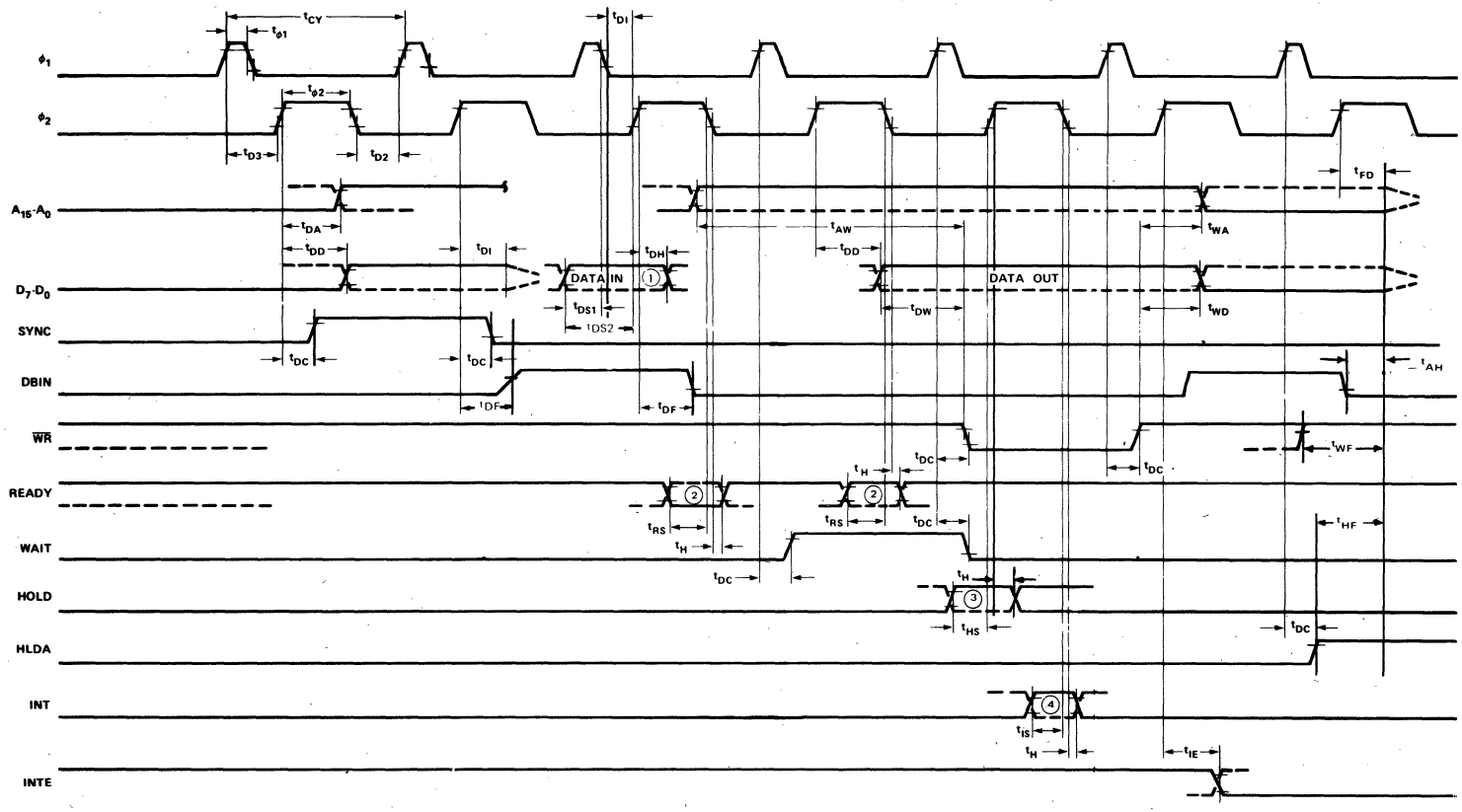
Device	t_{DW}
μPD8080AF	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-2	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-1	$t_{CY} - t_{D3} - t_{r\phi2} - 150$

⑦ If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.

⑧ $t_{HF} = t_{D3} + t_{r\phi2} - 50$ ns.

⑨ $t_{WF} = t_{D3} + t_{r\phi2} - 10$ ns.

TIMING WAVEFORMS ⑤ ⑥



Notes: ① Data in must be stable for this period during DBIN • T_3. Both t_{DS1} and t_{DS2} must be satisfied.

② Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)

③ Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)

④ Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized in the following instruction. (External synchronization is not required.)

⑤ This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

⑥ Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V; "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.

INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8080AF has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8080AF. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8080AF instruction set.

The special instruction group completes the μPD8080AF instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

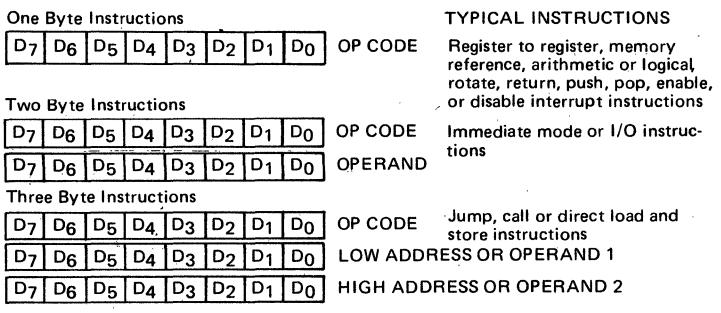
DATA AND INSTRUCTION FORMATS

Data in the μPD8080AF is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.



INSTRUCTION SET TABLE

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	5				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	5	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	5	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	17				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	11/17				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	11/17				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	11/17				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	11/17				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	11/17				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	11/17				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	11/17				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	11/17				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	5/11				
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11				
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11				
RC	Return on carry	1	1	0	1	1	0	0	0	5/11				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11				
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11				
RP	Return on positive	1	1	1	1	0	0	0	0	5/11				
RM	Return on minus	1	1	1	1	1	0	0	0	5/11				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	11				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	11				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	11				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	11				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	5				
INX D	Increment DE	0	0	0	1	0	0	1	1	5				
INX H	Increment HL	0	0	1	0	0	0	1	1	5				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	5				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	5				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	5				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	5				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	5				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	18				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	5				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	5				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RST A	Restart	1	1	A	A	A	1	1	1	11				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				CY
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	7				

Notes:

[1] Operand Symbols used
A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.

[3] Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
= flag not affected
0 = flag reset
1 = flag set

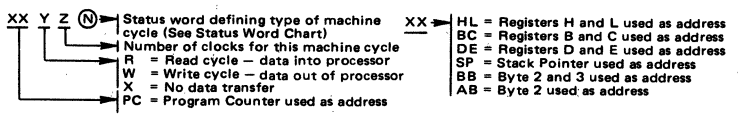
INSTRUCTION CYCLE TIMES

One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$). During ϕ_1 • SYNC of each machine cycle, a status word that identifies the type of machine cycle is available on the data bus.

Execution times and machine cycles used for each type of instruction are shown below.

INSTRUCTION	MACHINE CYCLES EXECUTED	CLOCK TIMES (MIN/MAX)
RST X and PUSH RP	PCR5 (1) SPW3 (5) SPW3 (5)	11
All CALL Instructions	PCR5 (1) PCR3 (2) PCR3 (2) SPW3 (5) SPW3 (5)	11/17
All Conditional RETURN Instructions	PCR5 (1) SPR3 (4) SPR3 (4)	5/11
RET Instructions	PCR4 (1) SPR3 (4) SPR3 (4)	10
XTHL	PCR4 (1) SPR3 (4) SPR3 (4) SPW3 (5) SPW5 (5)	18
DAD RP	PCR4 (1) PCX3 (X) PCX3 (X)	10
INR R; INX RP, DCR R; DCX RP; PCHL; MOV R, R; SPHL	PCR5 (1)	5
All JUMP Instructions and LXI RP	PCR4 (1) PCR3 (2) PCR3 (2)	10
POP RP	PCR4 (1) SPR3 (4) SPR3 (4)	10
LDA	PCR4 (1) PCR3 (2) PCR3 (2) BBR3 (2)	13
STA	PCR4 (1) PCR3 (2) PCR3 (2) BBW3 (3)	13
LHLD	PCR4 (1) PCR3 (2) PCR3 (2) BBR3 (2) BBR3 (2)	16
SHLD	PCR4 (1) PCR3 (2) PCR3 (2) BBW3 (3) BBW3 (3)	16
STAX B	PCR4 (1) BCW3 (3)	7
STAX D	PCR4 (1) DEW3 (3)	7
LDAX B	PCR4 (1) BCR3 (2)	7
LDAX D	PCR4 (1) DER3 (2)	7
MOV R, M; ADD M; ADC M; SUB M; SB B M; ANA M; XRA M; ORA M; CMP M	PCR4 (1) HLR3 (2)	7
INR M and DCR M	PCR4 (1) HLR3 (2) HLW3 (3)	10
MVI M	PCR4 (1) PCR3 (2) HLW3 (3)	10
MVI R; ADI; ACI; SUI; SBI; ANI; XRI; ORI; CPI	PCR4 (1) PCR3 (2)	7
MOV M, R	PCR4 (1) HLW3 (3)	7
EI; DI ADD R; ADC R; SUB R; SBB R; ANA R; XRA R; ORA R; CMP R; RLC; RRC; RAL; RAR; DAA; CMA; STC; CMC; NOP; XCHG	PCR4 (1)	4
OUT	PCR4 (1) PCR3 (2) ABW3 (7)	10
IN	PCR4 (1) PCR3 (2) ABR3 (6)	10
HLT	PCR4 (1) PCX3 (9)	7

Machine Cycle Symbol Definition



Underlined (XXYZ(N)) indicates machine cycle is executed if condition is True.

STATUS INFORMATION DEFINITION

SYMBOLS	DATA BUS BIT	DEFINITION
INTA ①	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart or CALL instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO}$ = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP ①	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR ①	D_7	Designates that the data bus will be used for memory read data.

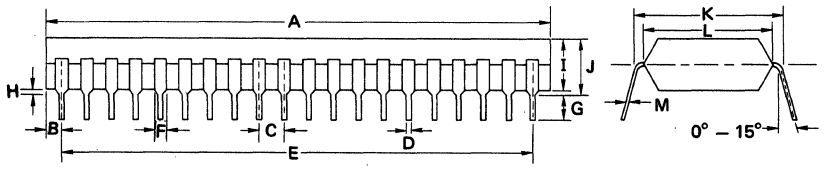
Note: ① These three status bits can be used to control the flow of data onto the μPD8080AF data bus.

STATUS WORD CHART

TYPE OF MACHINE CYCLE

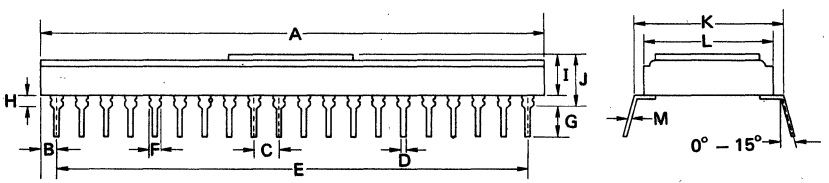
DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INT. ACK. WHILE HALT
											← Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

PACKAGE OUTLINE
μPD8080AFC/D



μPD8080AFC
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.10
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8080AFD
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.100
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.5	0.531
M	0.30 ± 0.1	0.012 ± 0.004

8-BIT N-CHANNEL MICROPROCESSOR

DESCRIPTION

The μPD8080A is a complete 8-bit parallel processor for use in general purpose digital computer systems, which offers higher performance than conventional 8080A microprocessors. It is fabricated on a single LSI chip using N-channel silicon gate MOS process.

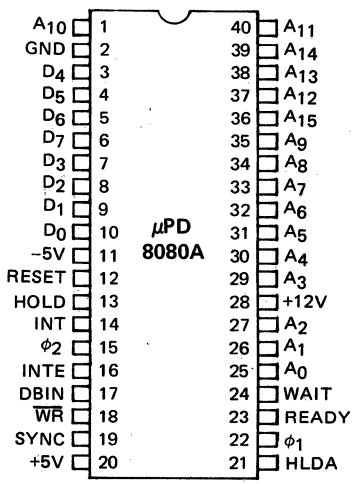
This processor is designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data busses are employed to allow direct interface to memories and I/O ports. Control signals, requiring no decoding, are provided directly by the processor. All busses, including the control bus, are TTL and CMOS compatible.

The μPD8080A has the capability to accept a multiple byte instruction upon an interrupt. This means that a CALL instruction can be inserted so that any address in the memory can be the starting location for an interrupt program. This can be accomplished without auxilliary circuit because INTA is active for all three bytes of the CALL instruction. Another important feature is that the decimal adjust accumulator instruction operates correctly after subtraction as well as after addition; thus BCD subtraction can be performed at the same speed as BCD addition.

FEATURES

- Software and Pin Compatible with Industry Standard 8080A
- Clock Frequency – 2.0 MHz
- Equivalent to the μPD8080AF with Enhancements
- Direct BCD Subtraction as well as Addition
- MOV r, r Executes in 4 Clock Cycles
- Interrupt Acknowledge is Active for 3 Byte Instructions such as CALL
- Available in a 40-pin Ceramic Package

PIN CONFIGURATION



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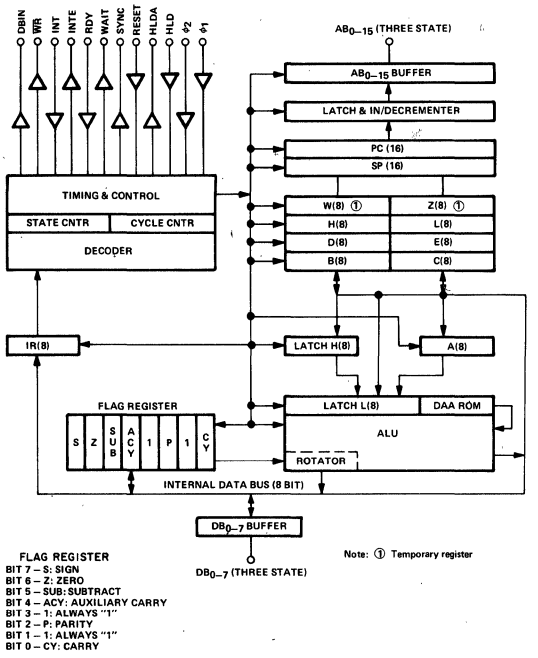
BLOCK DIAGRAM



FLAG REGISTER
BIT 7 – S: SIGN
BIT 6 – Z: ZERO
BIT 5 – SUB: SUBTRACT
BIT 4 – ACY: AUXILIARY CARRY
BIT 3 – 1: ALWAYS "1"
BIT 2 – P: PARITY
BIT 1 – 1: ALWAYS "1"
BIT 0 – CY: CARRY

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +150°C
All Input or Output Voltages	−0.3 to +20 Volts ①
V_{CC}, V_{DD} and V_{SS}	−0.3 to +20 Volts ①
Power Dissipation	1.5W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = GND, unless otherwise specified.

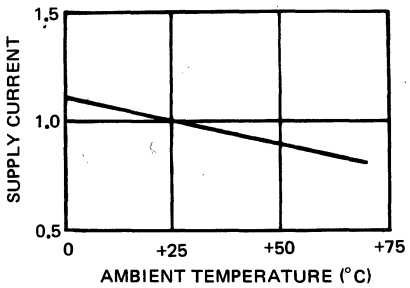
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Input Low Voltage	V_{ILC}	V_{SS} − 1		V_{SS} + 0.8	V	
Clock Input High Voltage	V_{IHC}	9.0		V_{DD} + 1	V	
Input Low Voltage	V_{IL}	V_{SS} − 1		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	3.0		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.9 mA on all outputs
Output High Voltage	V_{OH}	3.7 3.5			V V	I_{OH} = −150 μA ② I_{OH} = −1.0 mA
Avg. Power Supply Current (V_{DD})	$I_{DD(AV)}$		55	75	mA	t_{CY} min
Avg. Power Supply Current (V_{CC})	$I_{CC(AV)}$		50	70	mA	
Avg. Power Supply Current (V_{BB})	$I_{BB(AV)}$		0.01	1	mA	
Input Leakage	I_{IL}			±10 ②	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Clock Leakage	I_{CL}			±10 ②	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
Data Bus Leakage in Input Mode	I_{DL} ①			+10 ② −10	μA μA	$V_{IN} = V_{CC}$ $V_{IN} = V_{SS}$ + 0.45V
Address and Data Bus Leakage During HOLD	I_{FL}			+10 ② −10	μA	$V_{ADDR/DATA} = V_{CC}$ $V_{ADDR/DATA} = V_{SS}$ + 0.45V

Notes: ① There are no internal pull-up resistors on the inputs.
② Minus (−) designates current flow out of the device.

CAPACITANCE $T_a = 25°C$; $V_{CC} = V_{DD} = 0V$; $V_{BB} = -5V$

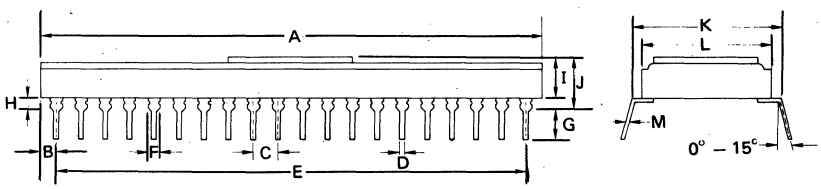
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ		17	25	pF	f_c = 1 MHz
Input Capacitance	C_{IN}		6	10	pF	Unmeasured Pins
Output Capacitance	C_{OUT}		10	20	pF	Returned to V_{SS}

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED ①



Note: ① $\Delta I_{supply}/\Delta T_a = -0.45\%/°C$.

PACKAGE OUTLINE μPD8080AD



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

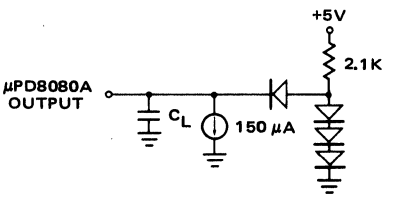
AC CHARACTERISTICS

T_a = −10°C to 70°C; V_{DD} = +12V ± 5%; V_{CC} = +5V ± 5%; V_{BB} = −5V ± 5%; V_{SS} = 0V, unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.48		2.0	μs	
Clock Rise and Fall Time	t_r, t_f	0		50	ns	
φ1 Pulse Width	$t_{\phi 1}$	60			ns	
φ2 Pulse Width	$t_{\phi 2}$	220			ns	
Delay φ1 to φ2	t_{D1}	0			ns	
Delay φ2 to φ1	t_{D2}	70			ns	
Delay φ1 to φ2 Leading Edges	t_{D3}	80			ns	
Address Output Delay From φ2	t_{DA} ②			200	ns	C_L = 100 pf
Data Output Delay From φ2	t_{DD} ②			220	ns	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	ns	C_L = 50 pf
DBIN Delay From φ2	t_{DF} ②	25		140	ns	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	ns	
Data Setup Time During φ1 and DBIN	t_{DS1}	30			ns	
	t_{DS2}	⑤				
Data Hold Time From φ2 During DBIN	t_{DH} ①	50			ns	
INTE Output Delay From φ2	t_{IE} ②			200	ns	C_L = 50 pf
READY Setup Time During φ2	t_{RS}	120			ns	
READY Setup Time to φ1 High	$t_{RS\phi 1}$	240			ns	
HOLD Setup Time to φ2	t_{HS}	140			ns	
INT Setup Time During φ2 (for all modes)	t_{IS}	120			ns	
Hold Time From φ2 (READY, INT, HOLD)	t_H	0			ns	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	ns	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑥			ns	C_L = 100 pf: Address, Data C_L = 50 pf: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑦			ns	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑧			ns	
Address Stable From $\overline{WR}$	t_{WA} ②	⑧			ns	
HLDA to Float Delay	t_{HF} ②	⑨			ns	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑩			ns	
Address Hold Time After DBIN During HLDA	t_{AH} ②	−20			ns	

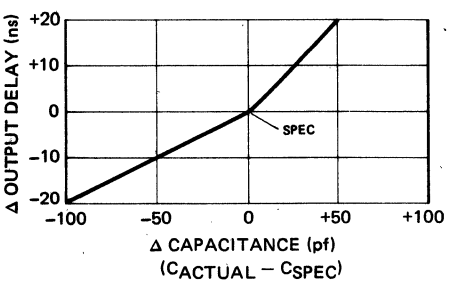
Notes: ① Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.

② Load Circuit



③ Actual $t_{CY} = t_{D3} + t_{r\phi 2} + t_{\phi 2} + t_{f\phi 2} + t_{D2} + t_{r\phi 1} > t_{CY}$ Min.

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE



④ The following are relevant when interfacing the μPD8080A to devices having V_{IH} = 3.3V.
- a. Maximum output rise time from 0.8V to 3.3V = 100 ns at C_L = SPEC.
- b. Output delay when measured to 3.0V = SPEC + 60 ns at C_L = SPEC.
- c. If $C_L \neq$ SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.

⑤ No restrictions.

⑥ $t_{AW} = 2\,t_{CY} - t_{D3} - t_{r\phi 2} - 140$

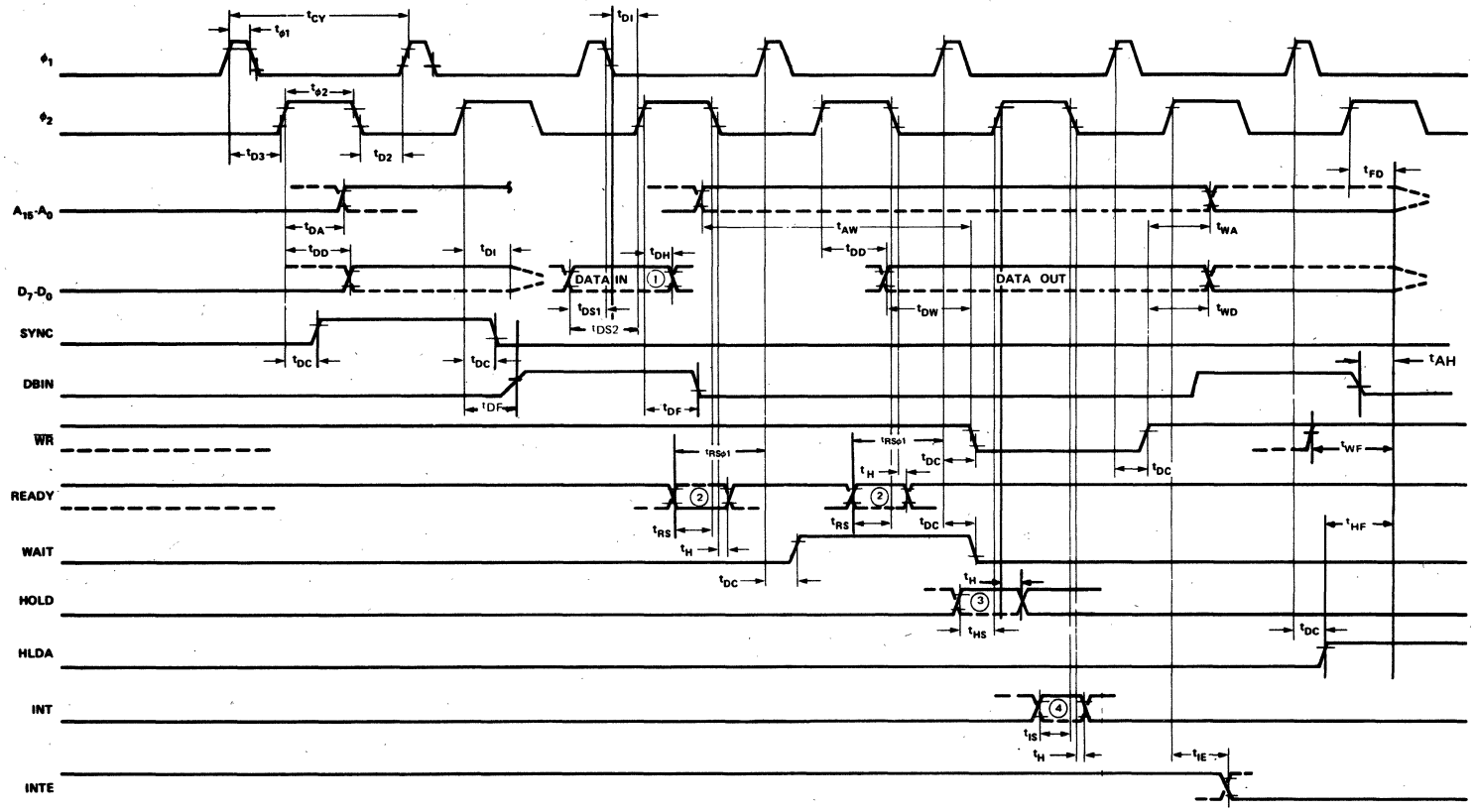
⑦ $t_{DW} = t_{CY} - t_{D3} - t_{r\phi 2} - 170$

⑧ If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi 2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.

⑨ $t_{HF} = t_{D3} + t_{r\phi 2} - 50$ ns.

⑩ $t_{WF} = t_{D3} + t_{r\phi 2} - 10$ ns.

TIMING WAVEFORMS ⑤ ⑥



① Data in must be stable for this period during DBIN T_3. t_{DS1} must be satisfied.

② Ready signal must be stable for this period during T_2. (Must be externally synchronized.)

③ Hold signal must be stable for this period during T_2 when entering hold mode, and during T_3, T_4 and T_5 when in hold mode. (External synchronization is not required.)

④ Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized on the following instruction. (External synchronization is not required.)

⑤ This timing diagram shows timing relationships only; it does not represent any specific machine cycle.

⑥ Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.0V; "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.

INSTRUCTION SET TABLE

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE							
MOV d,s	Move register to register	0 1 d d d s s s	4				
MOV M,s	Move register to memory	0 1 1 1 0 s s s	7				
MOV d,M	Move memory to register	0 1 d d d 1 1 0	7				
MVI d,D8	Move immediate to register	0 0 d d d 1 1 0	7				
MVI M,D8	Move immediate to memory	0 0 1 1 0 1 1 0	10				
INCREMENT/DECREMENT							
INR d	Increment register	0 0 d d d 1 0 0	5	•	•	•	
DCR d	Decrement register	0 0 d d d 1 0 1	5	•	•	•	
INR M	Increment memory	0 0 1 1 0 1 0 0	10	•	•	•	
DCR M	Decrement memory	0 0 1 1 0 1 0 1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR							
ADD s	Add register to A	1 0 0 0 0 s s s	4	•	•	•	•
ADC s	Add register to A with carry	1 0 0 0 1 s s s	4	•	•	•	•
SUB s	Subtract register from A	1 0 0 1 0 s s s	4	•	•	•	•
SSB s	Subtract register from A with borrow	1 0 0 1 1 s s s	4	•	•	•	•
ANA s	AND register with A	1 0 1 0 0 s s s	4	•	•	•	o
XRA s	Exclusive OR register with A	1 0 1 0 1 s s s	4	•	•	•	o
ORA s	OR register with A	1 0 1 1 0 s s s	4	•	•	•	o
CMP s	Compare register with A	1 0 1 1 1 s s s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR							
ADD M	Add memory to A	1 0 0 0 0 1 1 0	7	•	•	•	•
ADC M	Add memory to A with carry	1 0 0 0 1 1 1 0	7	•	•	•	•
SUB M	Subtract memory from A	1 0 0 1 0 1 1 0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1 0 0 1 1 1 1 0	7	•	•	•	•
ANA M	AND memory with A	1 0 1 0 0 1 1 0	7	•	•	•	o
XRA M	Exclusive OR memory with A	1 0 1 0 1 1 1 0	7	•	•	•	o
ORA M	OR memory with A	1 0 1 1 0 1 1 0	7	•	•	•	o
CMP M	Compare memory with A	1 0 1 1 1 1 1 0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR							
ADI D8	Add immediate to A	1 1 0 0 0 1 1 0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1 1 0 0 1 1 1 0	7	•	•	•	•
SUI D8	Subtract immediate from A	1 1 0 1 0 1 1 0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1 1 0 1 1 1 1 0	7	•	•	•	•
ANI D8	AND immediate with A	1 1 1 0 0 1 1 0	7	•	•	•	o
XRI D8	Exclusive OR immediate with A	1 1 1 0 1 1 1 0	7	•	•	•	o
ORI D8	OR immediate with A	1 1 1 1 0 1 1 0	7	•	•	•	o
CPI D8	Compare immediate with A	1 1 1 1 1 1 1 0	7	•	•	•	•
ALU – ROTATE							
RLC	Rotate A left, MSB to carry (8-bit)	0 0 0 0 0 1 1 1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0 0 0 0 1 1 1 1	4				•
RAL	Rotate A left through carry (9-bit)	0 0 0 1 0 1 1 1	4				•
RAR	Rotate A right through carry (9-bit)	0 0 0 1 1 1 1 1	4				•
JUMP							
JMP ADDR	Jump unconditional	1 1 0 0 0 0 1 1	10				
JNZ ADDR	Jump on not zero	1 1 0 0 0 0 1 0	10				
JZ ADDR	Jump on zero	1 1 0 0 1 0 1 0	10				
JNC ADDR	Jump on no carry	1 1 0 1 0 0 1 0	10				
JC ADDR	Jump on carry	1 1 0 1 1 0 1 0	10				
JPO ADDR	Jump on parity odd	1 1 1 0 0 0 1 0	10				
JPE ADDR	Jump on parity even	1 1 1 0 1 0 1 0	10				
JP ADDR	Jump on positive	1 1 1 1 0 0 1 0	10				
JM ADDR	Jump on minus	1 1 1 1 1 0 1 0	10				
CALL							
CALL ADDR	Call unconditional	1 1 0 0 1 1 0 1	17				
CNZ ADDR	Call on not zero	1 1 0 0 0 1 0 0	11/17				
CZ ADDR	Call on zero	1 1 0 0 1 1 0 0	11/17				
CNC ADDR	Call on no carry	1 1 0 1 0 1 0 0	11/17				
CC ADDR	Call on carry	1 1 0 1 1 1 0 0	11/17				
CPO ADDR	Call on parity odd	1 1 1 0 0 1 0 0	11/17				
CPE ADDR	Call on parity even	1 1 1 0 1 1 0 0	11/17				
CP ADDR	Call on positive	1 1 1 1 0 1 0 0	11/17				
CM ADDR	Call on minus	1 1 1 1 1 1 0 0	11/17				
RETURN							
RET	Return	1 1 0 0 1 0 0 1	11				
RNZ	Return on not zero	1 1 0 0 0 0 0 0	5/11				
RZ	Return on zero	1 1 0 0 1 0 0 0	5/11				
RNC	Return on no carry	1 1 0 1 0 0 0 0	5/11				
RC	Return on carry	1 1 0 1 1 0 0 0	5/11				
RPO	Return on parity odd	1 1 1 0 0 0 0 0	5/11				
RPE	Return on parity even	1 1 1 0 1 0 0 0	5/11				
RP	Return on positive	1 1 1 1 0 0 0 0	5/11				
RM	Return on minus	1 1 1 1 1 0 0 0	5/11				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR							
LXI B,D16	Load immediate register pair BC	0 0 0 0 0 0 0 1	10				
LXI D,D16	Load immediate register pair DE	0 0 0 1 0 0 0 1	10				
LXI H,D16	Load immediate register pair HL	0 0 1 0 0 0 0 1	10				
LXI SP,D16	Load immediate Stack Pointer	0 0 1 1 0 0 0 1	10				
PUSH							
PUSH B	Push register pair BC on stack	1 1 0 0 0 1 0 1	11				
PUSH D	Push register pair DE on stack	1 1 0 1 0 1 0 1	11				
PUSH H	Push register pair HL on stack	1 1 1 0 0 1 0 1	11				
PUSH PSW	Push A and flags on stack	1 1 1 1 0 1 0 1	11				
POP							
POP B	Pop register pair BC off stack	1 1 0 0 0 0 0 1	10				
POP D	Pop register pair DE off stack	1 1 0 1 0 0 0 1	10				
POP H	Pop register pair HL off stack	1 1 1 0 0 0 0 1	10				
POP PSW	Pop A and flags off stack	1 1 1 1 0 0 0 1	10	•	•	•	•
DOUBLE ADD							
DAD B	Add BC to HL	0 0 0 0 1 0 0 1	11				•
DAD D	Add DE to HL	0 0 0 1 1 0 0 1	11				•
DAD H	Add HL to HL	0 0 1 0 1 0 0 1	11				•
DAD SP	Add Stack Pointer to HL	0 0 1 1 1 0 0 1	11				•
INCREMENT REGISTER PAIR							
INX B	Increment BC	0 0 0 0 0 0 1 1	5				
INX D	Increment DE	0 0 0 1 0 0 1 1	5				
INX H	Increment HL	0 0 1 0 0 0 1 1	5				
INX SP	Increment Stack Pointer	0 0 1 1 0 0 1 1	5				
DECREMENT REGISTER PAIR							
DCX B	Decrement BC	0 0 0 0 1 0 1 1	5				
DCX D	Decrement DE	0 0 0 1 1 0 1 1	5				
DCX H	Decrement HL	0 0 1 0 1 0 1 1	5				
DCX SP	Decrement Stack Pointer	0 0 1 1 1 0 1 1	5				
REGISTER INDIRECT							
STAX B	Store A at ADDR in B	0 0 0 0 0 0 1 0	7				
STAX D	Store A at ADDR in D	0 0 0 1 0 0 1 0	7				
LDAX B	Load A at ADDR in B	0 0 0 0 1 0 1 0	7				
LDAX D	Load A at ADDR in D	0 0 0 1 1 0 1 0	7				
DIRECT							
STA ADDR	Store A direct	0 0 1 1 0 0 1 0	13				
LDA ADDR	Load A direct	0 0 1 1 1 0 1 0	13				
SHLD ADDR	Store HL direct	0 0 1 0 0 0 1 0	16				
LHLD ADDR	Load HL direct	0 0 1 0 1 0 1 0	16				
MOVE REGISTER PAIR							
XCHG	Exchange DE and HL register pairs	1 1 1 0 1 0 1 1	4				
XTHL	Exchange top of stack and HL	1 1 1 0 0 0 1 1	17				
SPHL	HL to Stack Pointer	1 1 1 1 1 0 0 1	4				
PCHL	HL to Program Counter	1 1 1 0 1 0 0 1	5				
INPUT/OUTPUT							
IN A	Input	1 1 0 1 1 0 1 1	10				
OUT A	Output	1 1 0 1 0 0 1 1	10				
EI	Enable interrupts	1 1 1 1 1 0 1 1	4				
DI	Disable interrupts	1 1 1 1 0 0 1 1	4				
RST A	Restart	1 1 A A A 1 1 1	11				
MISCELLANEOUS							
CMA	Complement A	0 0 1 0 1 1 1 1	4				
STC	Set carry	0 0 1 1 0 1 1 1	4				1
CMC	Complement carry	0 0 1 1 1 1 1 1	4				Cy
DAA	Decimal adjust A	0 0 1 0 0 1 1 1	4	•	•	•	•
NOP	No-operation	0 0 0 0 0 0 0 0	4				
HLT	Halt	0 1 1 1 0 1 1 0	7				

NOTES:

[1] Operand Symbols used
A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.

[3] Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
= flag not affected
0 = flag reset
1 = flag set

INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes. These instructions operate exactly like the μPD8080AF except as noted.

In addition to the four testable flags, the μPD8080A has two more flags (ACY, SUB) that are not directly testable. They are used for multiple precision arithmetic operations, particularly with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset. The Subtract flag is set if the last instruction resulted in a subtract operation being performed; it is reset if an add operation was performed. Also, arithmetic flags are not affected by logical instructions.

DATA AND INSTRUCTION FORMATS

Data in the μPD8080A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

One Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE

Two Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND

Three Byte Instructions

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2

TYPICAL INSTRUCTIONS

Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions

Immediate mode or I/O instructions

Jump, call or direct load and store instructions

INSTRUCTION CYCLE TIMES

One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$). During ϕ_1 SYNC of each machine cycle, a status word that identifies the type of machine cycle is available on the data bus.

Execution times and machine cycles used for each type of instruction are shown below.

INSTRUCTION	MACHINE CYCLES EXECUTED	CLOCK TIMES (MIN/MAX)
RST X and PUSH RP	PCR5 ① SPW3 ⑤ SPW3 ⑤	11
All CALL Instructions	PCR5 ① PCR3 ② PCR3 ② SPW3 ⑤ SPW3 ⑤	11/17
All RET Instructions	PCR5 ① SPR3 ④ SPR3 ④	5/11
XTHL	PCR5 ① SPR3 ④ SPW3 ⑤ SPR3 ④ SPW3 ⑤	17
DAD RP	PCR5 ① PCX3 ◯ PCX3 ◯	11
INR R; INX RP, DCR R; DCX RP; PCHL	PCR5 ①	5
All JUMP Instructions and LXI RP	PCR4 ① PCR3 ② PCR3 ②	10
POP RP	PCR4 ① SPR3 ④ SPR3 ④	10
LDA	PCR4 ① PCR3 ② PCR3 ② BBR3 ②	13
STA	PCR4 ① PCR3 ② PCR3 ② BBW3 ③	13
LHLD	PCR4 ① PCR3 ② PCR3 ② BBR3 ② BBR3 ②	16
SHLD	PCR4 ① PCR3 ② PCR3 ② BBW3 ③ BBW3 ③	16
STAX B	PCR4 ① BCW3 ③	7
STAX D	PCR4 ① DEW3 ③	7
LDAX B	PCR4 ① BCR3 ②	7
LDAX D	PCR4 ① DER3 ②	7
MOV R, M; ADD M; ADC M; SUB M; SB B M; ANA M; XRA M; ORA M; CMP M	PCR4 ① HLR3 ②	7
INR M and DCR M	PCR4 ① HLR3 ② HLW3 ③	10
MVI M	PCR4 ① PCR3 ② HLW3 ③	10
MVI R; ADI; ACI; SUI; SBI; ANI; XRI; ORI; CPI	PCR4 ① PCR3 ②	7
MOV M, R	PCR4 ① HLW3 ③	7
MOV R,R, EI; DI ADD R; ADC R; SUB R; SBB R; ANA R; XRA R; ORA R; CMP R; RLC; RRC; RAL; RAR; DAA; CMA; STC; CMC; NOP; XCHG, SPHL	PCR4 ①	4
OUT	PCR4 ① PCR3 ② ABW3 ⑦	10
IN	PCR4 ① PCR3 ② ABR3 ⑥	10
HLT	PCR4 ① PCX3 ⑩	7

Machine Cycle Symbol Definition

XX Y Z (N) — Status word defining type of machine cycle (See Status Word Chart)
Number of clocks for this machine cycle
R = Read cycle – data into processor
W = Write cycle – data out of processor
X = No data transfer
PC = Program Counter used as address

XX — HL = Registers H and L used as address
BC = Registers B and C used as address
DE = Registers D and E used as address
SP = Stack Pointer used as address
BB = Byte 2 and 3 used as address
AB = Byte 2 used as address

Underlined (XXYZ(N)) indicates machine cycle is executed if condition is True.

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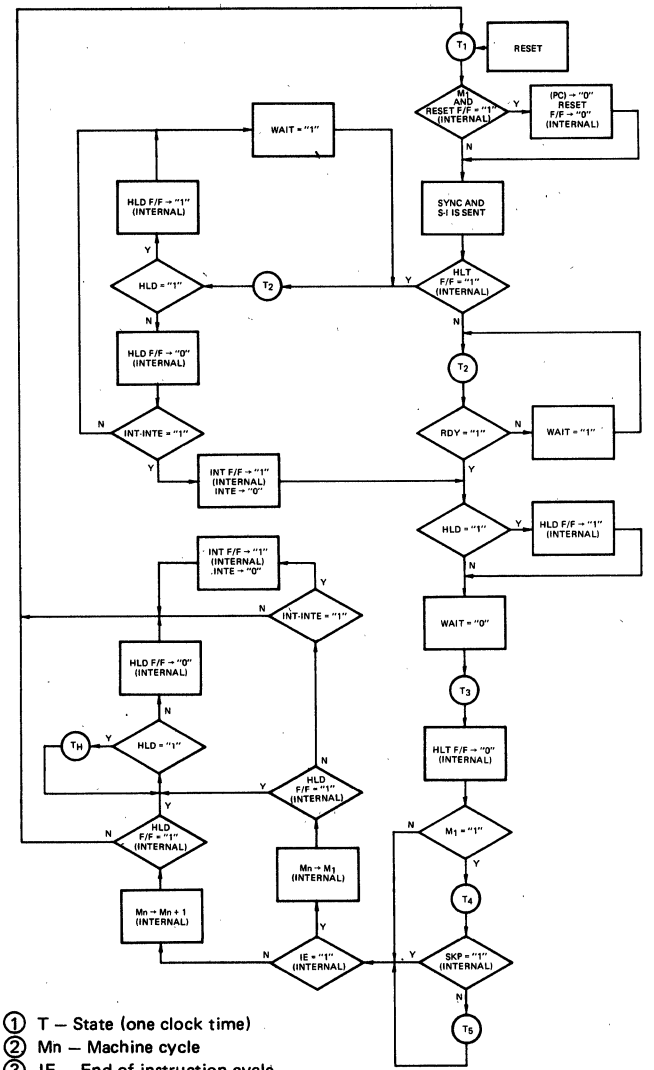
PROCESSOR STATE TRANSITION DIAGRAM



Notes:
① T – State (one clock time)
② Mn – Machine cycle
③ IE – End of instruction cycle
④ S-I – Status information
⑤ SKP – Skip signal (internal)
⑥ HLD F/F (internal) is reset when HLD signal returns to zero.
⑦ HLT F/F (internal) is set when HALT instruction is executed.
⑧ RESET F/F (internal) is set when reset signal is activated.

STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE (M_1)	INT. ACK. (M_2, M_3)	HALT ACKNOWLEDGE	INT. ACK. WHILE HALT
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪
D_0	INTA	0	0	0	0	0	0	0	1	1	0	1
D_1	WO	1	1	0	1	0	1	0	1	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	0	1	0
D_4	OUT	0	0	0	0	0	0	1	0	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	0	0	0

(N) STATUS WORD

PRIORITY INTERRUPT CONTROLLER

DESCRIPTION

The μPB8214 is an eight-level priority interrupt controller. Designed to simplify interrupt driven microcomputer systems, the μPB8214 requires a single +5V power supply and is packaged in a 24 pin plastic Dual-in-line package.

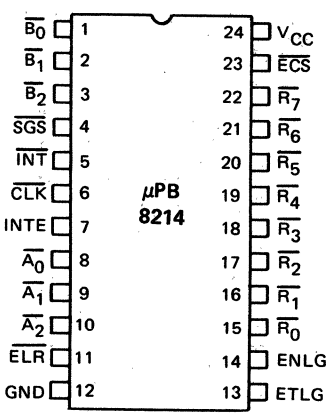
The μPB8214 accepts up to eight interrupts, determines which has the highest priority and then compares that priority with a software created current status register. If the incoming request is of a higher priority than the interrupt currently being serviced, an interrupt request to the processor is generated. Vector information that identifies the interrupting device is also generated.

The interrupt structure of the microcomputer system can be expanded beyond eight interrupt levels by cascading μPB8214s. The μPB8214's interrupt and vector information outputs are open collector and control signals are provided to simplify expansion of the interrupt structure.

FEATURES

- Eight Priority Levels
- Current Status Register and Priority Comparator
- Easily Expanded Interrupt Structure
- Single +5 Volt Supply

PIN CONFIGURATION



PIN NAMES

Inputs:		
$\overline{R_0}$–$\overline{R_7}$	Request Levels ($\overline{R_7}$ Highest Priority)	
$\overline{B_0}$–$\overline{B_2}$	Current Status	
$\overline{SGS}$	Status Group Select	
$\overline{ECS}$	Enable Current Status	
INTE	Interrupt Enable	
$\overline{CLK}$	Clock (INT F-F)	
$\overline{ELR}$	Enable Level Read	
ETLG	Enable This Level Group	
Outputs:		
$\overline{A_0}$–$\overline{A_2}$	Request Levels	Open
$\overline{INT}$	Interrupt (Act. Low)	Collector
ENLG	Enable Next Level Group	

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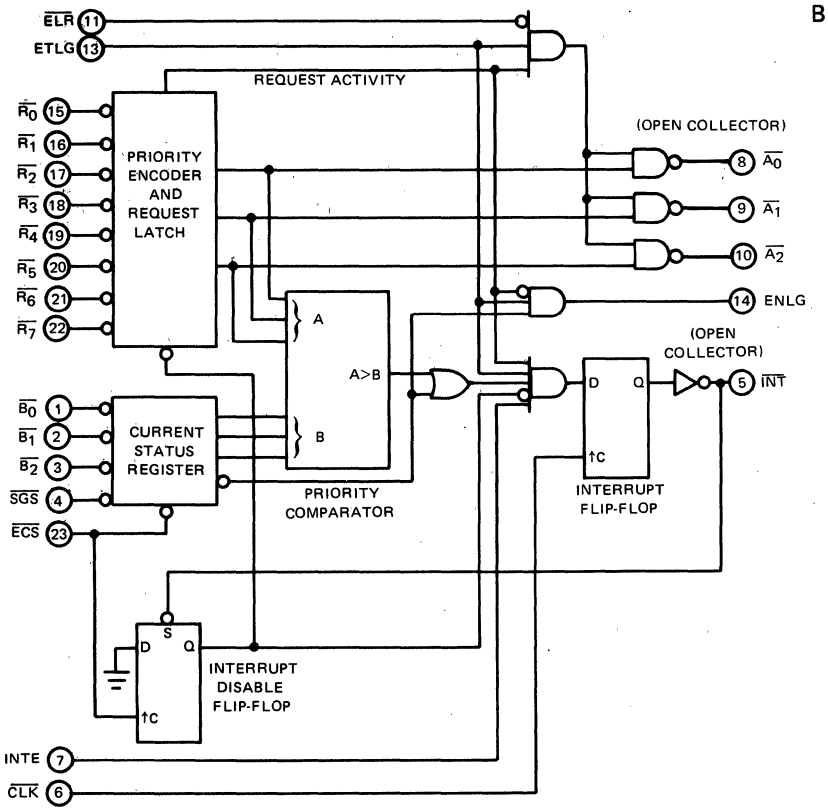
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

General

The μPB8214 is an LSI device designed to simplify the circuitry required to implement an interrupt driven microcomputer system. Up to eight interrupting devices can be connected to a μPB8214, which will assign priority to incoming interrupt requests and accept the highest. It will also compare the priority of the highest incoming request with the priority of the interrupt being serviced. If the serviced interrupt has a higher priority, the incoming request will not be accepted.

A system with more than eight interrupting devices can be implemented by interconnecting additional μPB8214s. In order to facilitate this expansion, control signals are provided for cascading the controllers so that there is a priority established among the controllers. In addition, the interrupt and vector information outputs are open collector.

Priority Encoder and Request Latch

The priority encoder portion of the μPB8214 accepts up to eight active low interrupt requests ($\overline{R_0}$–$\overline{R_7}$). The circuit assigns priority to the incoming requests, with $\overline{R_7}$ having the highest priority and $\overline{R_0}$ the lowest. If two or more requests occur simultaneously, the μPB8214 accepts the one having the highest priority. Once an incoming interrupt request is accepted, it is stored by the request latch and a three-bit code is output. As shown in the following table, the outputs, ($\overline{A_0}$–$\overline{A_2}$) are the complement of the request level (modulo 8) and directly correspond to the bit pattern required to generate the one byte RESTART (RST) instructions recognized by an 8080A. Simultaneously with the $\overline{A_0}$–$\overline{A_2}$ outputs, a system interrupt request ($\overline{INT}$) is output by the μPB8214. It should be noted that incoming interrupt requests that are *not* accepted are not latched and must remain as an input to the μPB8214 in order to be serviced.

FUNCTIONAL DESCRIPTION (CONT.)

RESTART GENERATION TABLE

PRIORITY REQUEST		RST	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			1	1	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	1	1	1
LOWEST	$\overline{R_0}$	7	1	1	1	1	1	1	1	1
	$\overline{R_1}$	6	1	1	1	1	0	1	1	1
	$\overline{R_2}$	5	1	1	1	0	1	1	1	1
	$\overline{R_3}$	4	1	1	1	0	0	1	1	1
	$\overline{R_4}$	3	1	1	0	1	1	1	1	1
	$\overline{R_5}$	2	1	1	0	1	0	1	1	1
	$\overline{R_6}$	1	1	1	0	0	1	1	1	1
HIGHEST	$\overline{R_7}$	0*	1	1	0	0	0	1	1	1

*CAUTION: RST 0 will vector the program counter to location 0 (zero) and invoke the same routine as the "RESET" input to 8080A.

Current Status Register

The current status register is designed to prevent an incoming interrupt request from overriding the servicing of an interrupt with higher priority. Via software, the priority level of the interrupt being serviced by the microprocessor is written into the current status register on $\overline{B_0}$–$\overline{B_2}$. The bit pattern written should be the complement of the interrupt level.

The interrupt level currently being serviced is written into the current status register by driving $\overline{ECS}$ (Enable Current Status) low. The μPB8214 will only accept interrupts with a higher priority than the value contained by the current status register. Note that the programmer is free to use the current status register for other than as above. Other levels may be written into it. The comparison may be completely disabled by driving $\overline{SGS}$ (Status Group Select) low when $\overline{ECS}$ is driven low. This will cause the μPB8214 to accept incoming interrupts only on the basis of their priority to each other.

Priority Comparator

The priority comparator circuitry compares the level of the interrupt accepted by the priority encoder and request latch with the contents of the current status register. If the incoming request has a priority level higher than that of the current status register, the $\overline{INT}$ output is enabled. Note that this comparison can be disabled by loading the current status register with $\overline{SGS}$=0.

Expansion Control Signals

A microcomputer design may often require more than eight different interrupts. The μPB8214 is designed so that interrupt system expansion is easily performed via the use of three signals: ETLG (Enable This Level Group); ENLG (Enable Next Level Group); and $\overline{ELR}$ (Enable Level Read). A high input to ETLG indicates that the μPB8214 may accept an interrupt. In a typical system, the ENLG output from one μPB8214 is connected to the ETLG input of another μPB8214, etc. The ETLG of the μPB8214 with the highest priority is tied high. This configuration sets up priority among the cascaded μPB8214's. The ENLG output will be high for any device that does not have an interrupt pending, thereby allowing a device with lower priority to accept interrupts. The $\overline{ELR}$ input is basically a chip enable and allows hardware or software to selectively disable/enable individual μPB8214's. A low on the $\overline{ELR}$ input enables the device.

FUNCTIONAL DESCRIPTION (CONT.)

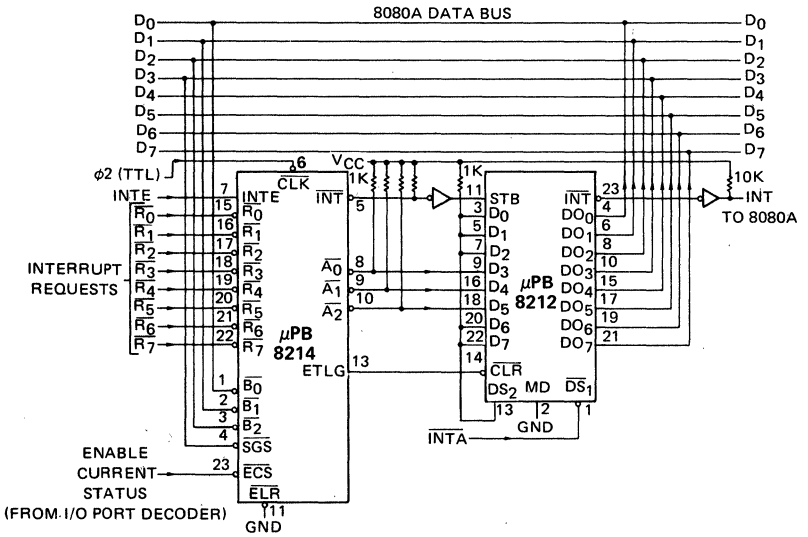
Interrupt Control Circuitry

The μPB8214 contains two flip-flops and several gates which determine whether an accepted interrupt request to the μPB8214 will generate a system interrupt to the 8080A. A condition gate drives the D input of the interrupt flip-flop whenever an interrupt request has been completely accepted. This requires that: the ETLG (Enable This Level Group) and INTE (Interrupt Enable) inputs to the μPB8214 are high; the $\overline{ELR}$ input is low; the incoming request must be of a higher priority than the contents of the current status register; and the μPB8214 must have been enabled to accept interrupt requests by the clearing of the interrupt disable flip-flop.

Once the condition gate drives the D input of the interrupt flip-flop high, a system interrupt ($\overline{INT}$) to the 8080A is generated on the next rising edge of the $\overline{CLK}$ input to the μPB8214. This $\overline{CLK}$ input is typically connected to the $\phi 2$ (TTL) output of an 8224 so that 8080A set-up time specifications are met. When $\overline{INT}$ is generated, it sets the interrupt disable flip-flop so that no additional system interrupts will be generated until it is reset. It is reset by driving $\overline{ECS}$ (Enable Current Status) low thereby writing into the current status register.

It should be noted that the open collector $\overline{INT}$ output from the μPB8214 is active for only one clock period and thus must be externally latched for inputting to the 8080A. Also, because the $\overline{INT}$ output is open collector, when μPB8214's are cascaded, an $\overline{INT}$ output from any one will set all of the interrupt disable flip-flops in the array. Each μPB8214's interrupt disable flip-flop must then be cleared individually in order to generate subsequent system interrupts.

TYPICAL μPB8214 CIRCUITRY



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output and Supply Voltages	-0.5 to +7 Volts
All Input Voltages	-1.0 to +5.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS $T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Clamp Voltage (all inputs)	V_C			-1.0	V	I_C=-5mA
Input Forward Current: ETLG input	I_F		-.15	-0.5	mA	V_F=0.45V
all other inputs			-.08	-0.25	mA	
Input Reverse Current: ETLG input	I_R			80	μA	V_R=5.25V
all other inputs				40	μA	
Input LOW Voltage: all inputs	V_{IL}			0.8	V	V_{CC}=5.0V
Input HIGH Voltage: all inputs	V_{IH}	2.0			V	V_{CC}=5.0V
Power Supply Current	I_{CC}		90	130	mA	②
Output LOW Voltage: all outputs	V_{OL}		.3	.45	V	I_{OL}=10mA
Output HIGH Voltage: ENLG output	V_{OH}	2.4	3.0		V	I_{OH}=-1mA
Short Circuit Output Current: ENLG output	I_{OS}	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$–$\overline{A_2}$	I_{CEX}			100	μA	V_{CEX}=5.25V

CAPACITANCE ③ $T_a = 25°C$

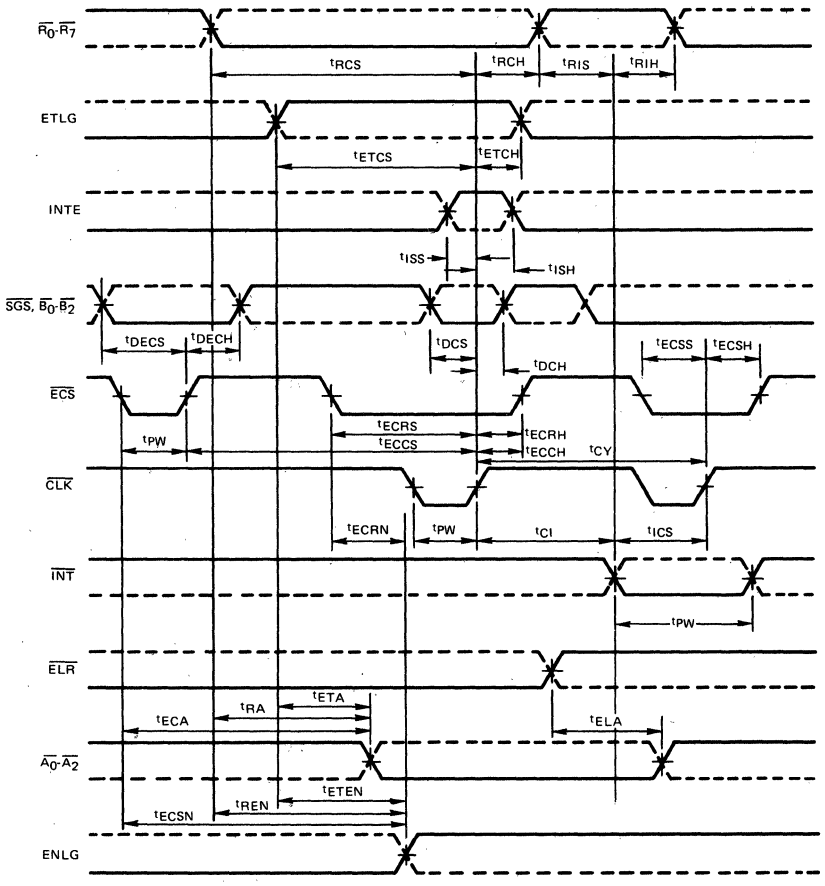
PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	10	pF	V_{BIAS}=2.5V
Output Capacitance	C_{OUT}		7	12	pF	V_{CC}=5V f=1mHz

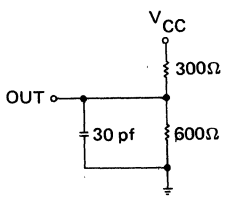
AC CHARACTERISTICS $T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
$\overline{CLK}$ Cycle Time	t_{CY}	80	50		ns	Input pulse amplitude: 2.5 Volts
$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	t_{PW}	25	15		ns	
INTE Setup Time to $\overline{CLK}$	t_{ISS}	16	12		ns	
INTE Hold Time after $\overline{CLK}$	t_{ISH}	20	10		ns	
ETLG Setup Time to $\overline{CLK}$	t_{ETCS}④	25	12		ns	Input rise and fall times: 5 ns between 1 and 2 Volts
ETLG Hold Time After $\overline{CLK}$	t_{ETCH}④	20	10		ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECCS}④	80	50		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECCH}⑤	0			ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECRS}⑤	110	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECRH}⑤	0				Output loading of 15 mA and 30 pF.
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECSS}④	75	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECSH}④	0			ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{CLK}$	t_{DCS}④	70	50		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{CLK}$	t_{DCH}④	0			ns	Speed measurements taken at the 1.5 Volts levels.
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{CLK}$	t_{RCS}⑤	90	55		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{CLK}$	t_{RCH}⑤	0			ns	
$\overline{INT}$ Setup Time to $\overline{CLK}$	t_{ICS}	55	35		ns	
$\overline{CLK}$ to $\overline{INT}$ Propagation Delay	t_{CI}		15	25	ns	
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{INT}$	t_{RIS}⑥	10	0		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{INT}$	t_{RIH}⑥	35	20		ns	
$\overline{R_0}$–$\overline{R_7}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{RA}		80	100	ns	
$\overline{ELR}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ELA}		40	55	ns	
$\overline{ECS}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ECA}		100	120	ns	
ETLG to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ETA}		35	70	ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{ECS}$	t_{DECS}⑥	15	10		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{ECS}$	t_{DECH}⑥	15	10		ns	
$\overline{R_0}$–$\overline{R_7}$ to ENLG Propagation Delay	t_{REN}		45	70	ns	
ELTG to ENLG Propagation Delay	t_{ETEN}		20	25	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECRN}		85	90	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECSN}		35	55	ns	

Notes:
① Typical values are for T_a=25°C, V_{CC}=5.0V
② $\overline{B_0}$–$\overline{B_2}$, $\overline{SGS}$, $\overline{CLK}$, $\overline{R_0}$–$\overline{R_4}$ grounded, all other inputs and all outputs open.
③ This parameter is periodically sampled and not 100% tested.
④ Required for proper operation if INTE is enabled during next clock pulse.
⑤ These times are not required for proper operation but for desired change in interrupt flip-flop.
⑥ Required for new request or status to be properly loaded.

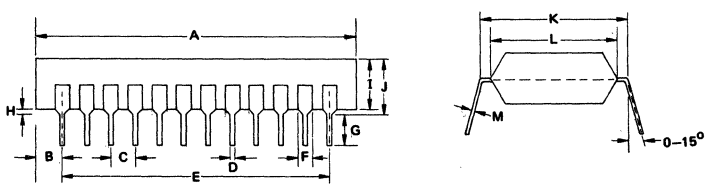
TIMING WAVEFORMS





TEST CIRCUIT

PACKAGE OUTLINE μPB8214C



ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.28
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	3.2 MIN.	0.125 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	0.25 ± 0.1	0.01 ± 0.004

CLOCK GENERATOR AND DRIVER FOR 8080A PROCESSORS

DESCRIPTION

The μPB8224 is a single chip clock generator and driver for 8080A processors. The clock frequency is determined by a user specified crystal and is capable of meeting the timing requirements of the entire 8080A family of processors. MOS and TTL level clock outputs are generated.

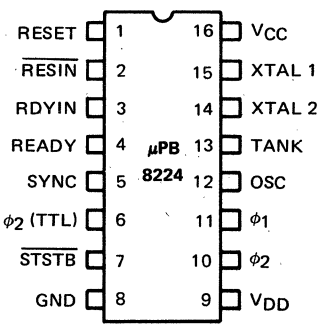
Additional logic circuitry of the μPB8224 provides signals for power-up reset, an advance status strobe and properly synchronizes the ready signal to the processor. This greatly reduces the number of chips needed for 8080A systems.

The μPB8224 is fabricated using NEC's Schottky bipolar process.

FEATURES

- Crystal Controlled Clocks
- Oscillator Output for External Timing
- MOS Level Clocks for 8080A Processor
- TTL Level Clock for DMA Activities
- Power-up Reset for 8080A Processor
- Ready Synchronization
- Advanced Status Strobe
- Reduces System Package Count
- Available in 16-pin Cerdip and Plastic Packages

PIN CONFIGURATION



PIN NAMES

$\overline{RESIN}$	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
$\overline{STSTB}$	Status STB Output
ϕ_1	Processor Clocks
ϕ_2	
XTAL 1	Crystal Connections
XTAL 2	
TANK	Used With Overtone Crystal
OSC	Oscillator Output
ϕ_2 (TTL)	ϕ_2 CLK (TTL Level)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

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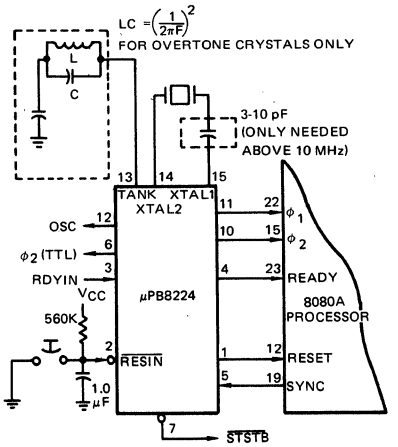
Clock Generator

The clock generator circuitry consists of a crystal controlled oscillator and a divide-by-nine counter. The crystal frequency is a function of the 8080A processor speed and is basically nine times the processor frequency, i.e.:

$$\text{Crystal frequency} = \frac{9}{t_{CY}}$$

where t_{CY} is the 8080A processor clock period.

A series resonant fundamental mode crystal is normally used and is connected across input pins XTAL1 and XTAL2. If an overtone mode crystal is used, an additional LC network, AC coupled to ground, must be connected to the TANK input of the μPB8224 as shown in the following figure.



The formula for the LC network is:

$$LC = \left(\frac{1}{2\pi F}\right)^2$$

where F is the desired frequency of oscillation.

The output of the oscillator is input to the divide-by-nine counter. It is also buffered and brought out on the OSC pin, allowing this stable, crystal controlled source to be used for derivation of other system timing signals. The divide-by-nine counter generates the two non-overlapping processor clocks, ϕ_1 and ϕ_2, which are buffered and at MOS levels, a TTL level ϕ_2 and internal timing signals.

The ϕ_1 and ϕ_2 high level outputs are generated in a 2-5-2 digital pattern, with ϕ_1 being high for two oscillator periods, ϕ_2 being high for five oscillator periods, and then neither being high for two oscillator periods. The TTL level ϕ_2,ϕ_2 (TTL), is normally used for DMA activities by gating the external device onto the 8080A bus once a Hold Acknowledge (HLDA) has been issued.

Additional Logic

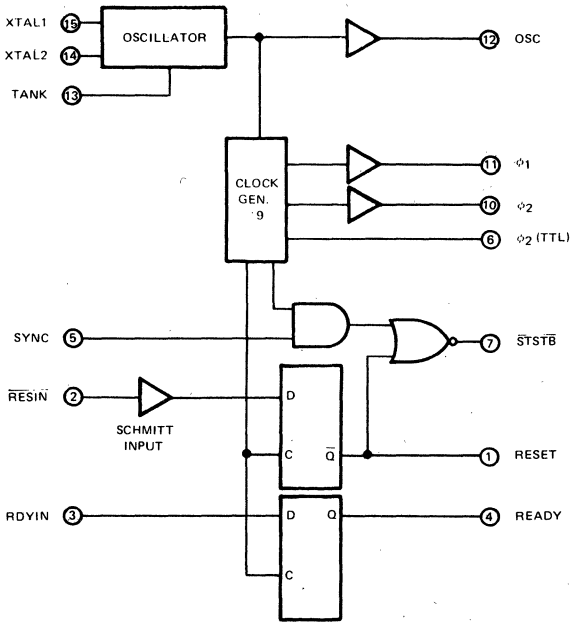
In addition to the clock generator circuitry, the μPB8224 contains additional logic to aid the system designer in the proper timing of several interface signals.

The $\overline{\text{STSTB}}$ signal indicates, at the earliest possible moment, when the status signals output from the 8080A processor are stable on the data bus. $\overline{\text{STSTB}}$ is designed to connect directly to the μPB8228 System Controller and automatically resets the μPB8228 during power-on Reset.

The $\overline{\text{RESIN}}$ input to the μPB8224 is used to automatically generate a RESET signal to the 8080A during power initialization. The slow rise of the power supply voltage in an external RC network is sensed by an internal Schmitt Trigger. The output of the Schmitt Trigger is gated to generate an 8080A compatible RESET. An active low manual switch may also be attached to the RC circuit for manual system reset.

The RDYIN input to the μPB8224 accepts an asynchronous "wait request" and generates a READY output to the 8080A that is fully synchronized to meet the 8080A timing requirements.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output Voltages (TTL)	−0.5 to +7 Volts
All Output Voltages (MOS)	−1.0 to +13.5 Volts
All Input Voltages	−1.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts
Supply Voltage V_{DD}	−0.5 to +13.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Current Loading	I_F			−0.25	mA	V_F = 0.45V
Input Leakage Current	I_R			10	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C			−1.0	V	I_C = −5 mA
Input "Low" Voltage	V_{IL}			0.8	V	V_{CC} = 5.0V
Input "High" Voltage	V_{IH}	2.6			V	Reset Input
		2.0				All Other Inputs
RESIN Input Hysteresis	V_{IH}-V_{IL}	0.25			V	V_{CC} = 5.0V
Output "Low" Voltage	V_{OL}			0.45	V	(Φ1, Φ2), Ready, Reset, STSTB
						I_{OL} = 2.5 mA
				0.45	V	All Other Inputs
						I_{OL} = 15 mA
Output "High" Voltage	V_{OH}					
Φ1, Φ2		9.4			V	I_{OH} = −100 μA
READY, RESET		3.6			V	I_{OH} = −100 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Output Short Circuit Current (All Low Voltage Outputs Only)	I_{SC} ①	−10		−60	mA	V_O = 0V, V_{CC} = 5.0V
Power Supply Current	I_{CC}			115	mA	
Power Supply Current	I_{DD}			15	mA	

Note: ① Caution, Φ1 and Φ2 output drivers do not have short circuit protection

CAPACITANCE①

T_a = 25°C; f = 1 MHz; V_{CC} = 5V; V_{DD} = 12V; V_{BIAS} = 2.5V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	

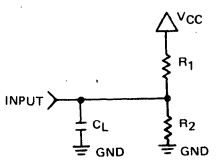
Note: ① This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

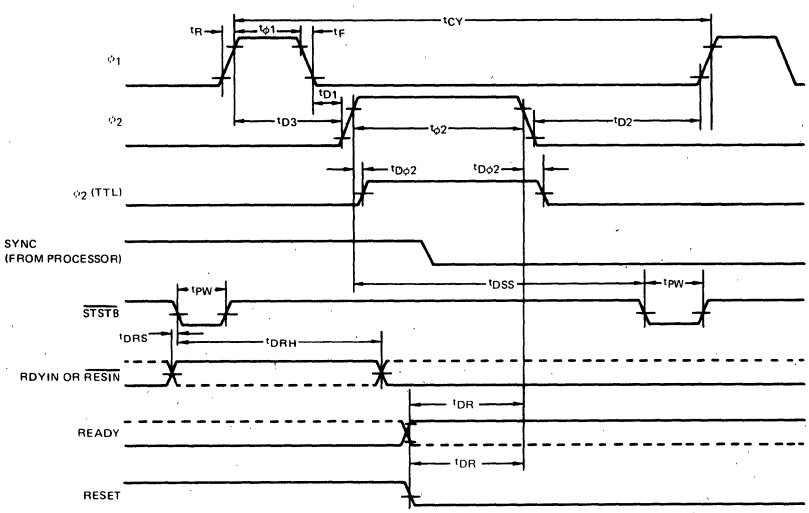
PARAMETER	SYMBOL	LIMITS ① MIN	LIMITS ① TYP	LIMITS ① MAX	UNIT	TEST CONDITIONS
ϕ_1 Pulse Width	$t_{\phi 1}$	$\frac{2t_{CY}}{9}$ −20 ns			ns	C_L = 20 pF to 50 pF
ϕ_2 Pulse Width	$t_{\phi 2}$	$\frac{5t_{CY}}{9}$ −35 ns				
ϕ_1 to ϕ_2 Delay	t_{D1}	0				
ϕ_2 to ϕ_1 Delay	t_{D2}	$\frac{2t_{CY}}{9}$ −14 ns				
ϕ_1 to ϕ_2 Delay	t_{D3}	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +20 ns		
ϕ_1 and ϕ_2 Rise Time	t_R			20		
ϕ_1 and ϕ_2 Fall Time	t_F			20		
ϕ_2 to ϕ_2 (TTL) Delay	$t_{D\phi 2}$	−5		+15	ns	ϕ_2 TTL, CL = 30 pF R_1 = 300Ω R_2 = 600Ω
ϕ_2 to $\overline{STSTB}$ Delay	t_{DSS}	$\frac{6t_{CY}}{9}$ −30 ns		$\frac{6t_{CY}}{9}$	ns	
$\overline{STSTB}$ Pulse Width	t_{PW}	$\frac{t_{CY}}{9}$ −15 ns			ns	$\overline{STSTB}$, CL = 15 pF R_1 = 2K R_2 = 4K
RDYIN Setup Time to $\overline{STSTB}$	t_{DRS}	50 ns − $\frac{4t_{CY}}{9}$				
RDYIN Hold Time After $\overline{STSB}$	t_{DRH}	$\frac{4t_{CY}}{9}$				
READY or RESET to ϕ_2 Delay	t_{DR}	$\frac{4t_{CY}}{9}$ −25 ns			ns	Ready and Reset CL = 10 pF R_1 = 2K R_2 = 4K
Crystal Frequency	f_{CLK}		$\frac{9}{t_{CY}}$		MHz	
Maximum Oscillating Frequency	f_{MAX}			27	MHz	

Note: ① t_{CY} represents the processor clock period



TEST CIRCUIT

TIMING WAVEFORMS



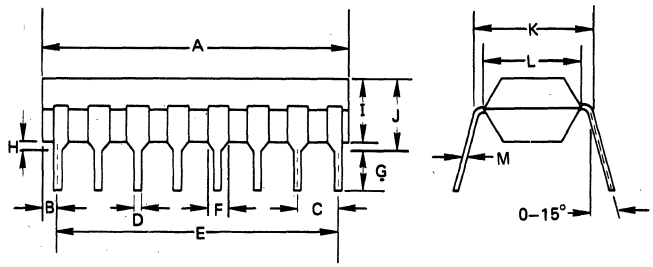
Voltage Measurement Points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

CRYSTAL REQUIREMENTS

Tolerance	0.005% at 0°C–70°C
Resonance	Series (Fundamental) ①
Load Capacitance	20-35 pF
Equivalent Resistance	75-20 ohms
Power Dissipation (Min)	4 mW

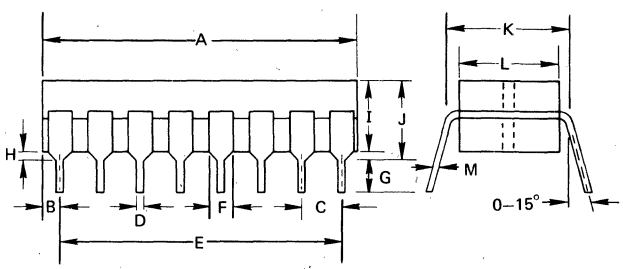
Note: ① With tank circuit use 3rd overtone mode.

PACKAGE OUTLINE μPB8224C/D



μPB8224C (Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	0.01



μPB8224D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	$0.0098^{+0.0039}_{0.0019}$

8080A SYSTEM CONTROLLER AND BUS DRIVER

DESCRIPTION

The μPB8228/8238D is a single chip controller and bus driver for 8080A based systems. All the required interface signals necessary to connect RAM, ROM and I/O components to a μPD8080A are generated.

The μPB8228/8238D provides a bi-directional three-state bus driver for high TTL fan-out and isolation of the processor data bus from the system data bus for increased noise immunity.

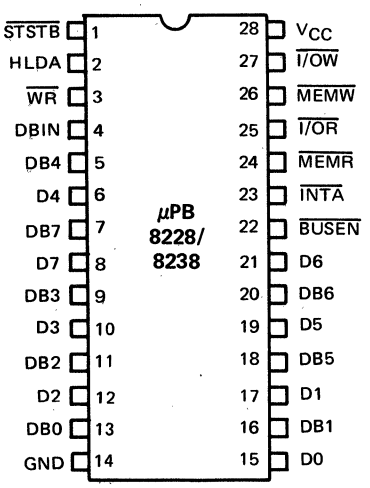
The system controller portion of the μPB8228/8238D consists of a status latch for definition of processor machine cycles and a gating array to decode this information for direct interface to system components. The controller can enable gating of a multi-byte interrupt onto the data bus or can automatically insert a RESTART 7 onto the data bus without any additional components.

Two devices are provided. The μPB8228D for small systems without tight write timing constraints and the μPB8238D for larger systems.

FEATURES

- System Controller for 8080A Systems
- Bi-Directional Data Bus for Processor Isolation
- 3.60V Output High Voltage for Direct Interface to 8080A Processor
- Three State Outputs on System Data Bus
- Enables Use of Multi-Byte Interrupt Instructions
- Generates RST 7 Interrupt Instruction
- μPB8228 for Small Memory Systems
- μPB8238 for Large Memory Systems
- Reduces System Package Count
- Schottky Bipolar Technology

PIN CONFIGURATION



NC: No Connection

PIN NAMES

D7-D0	Data Bus (Processor Side)
DB7-DB0	Data Bus (System Side)
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
DBIN	DBIN (From Processor)
$\overline{INTA}$	Interrupt Acknowledge
HLDA	HLDA (From Processor)
$\overline{WR}$	WR (From Processor)
$\overline{BUSEN}$	Bus Enable Input
$\overline{STSTB}$	Status Strobe (From μPB8224)
V_{CC}	+5V
GND	0 Volts

FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver

The eight bit, bi-directional bus driver provides buffering between the processor data bus and the system data bus. On the processor side, the μPB8228/8238D exceeds the minimum input voltage requirements (3.0V) of the μPD8080A. On the system side, the driver is capable of adequate drive current (10 mA) for connection of a large number of memory and I/O devices to the bus. Signal flow in the bus driver is controlled by the gating array and its outputs can be forced into a high impedance state by use of the $\overline{\text{BUSEN}}$ input.

Status Latch

The Status Latch in the μPB8228/8238D stores the status information placed on the data bus by the 8080A at the beginning of each machine cycle. The information is latched when $\overline{\text{STSTB}}$ goes low and is then decoded by the gating array for the generation of control signals.

Gating Array

The Gating Array generates "active low" control signals for direct interfacing to system components by gating the contents of the status latch with control signals from the 8080A.

$\overline{\text{MEM/R}}$, $\overline{\text{I/OR}}$ and $\overline{\text{INTA}}$ are generated by gating the DBIN signal from the processor with the contents of the status latch. $\overline{\text{I/OR}}$ is used to enable an I/O input onto the system data bus. $\overline{\text{MEM/R}}$ is used to enable a memory input.

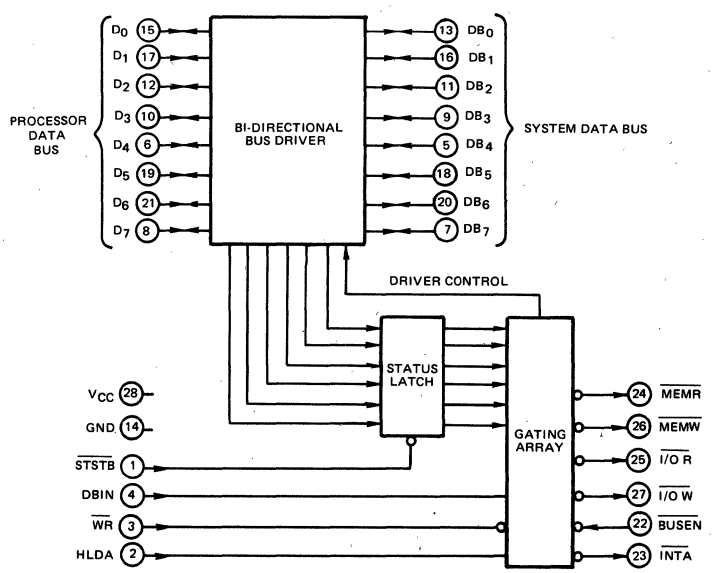
$\overline{\text{INTA}}$ is normally used to gate an interrupt instruction onto the system data bus. When used with the μPD8080A processor, the μPB8228/8238D will decode an interrupt acknowledge status word during all three machine cycles for a multi-byte interrupt instruction. For 8080A type processors that do not generate an interrupt acknowledge status word during the second and third machine cycles of a multi-byte interrupt instruction, the μPB8228/8238 will internally generate an $\overline{\text{INTA}}$ pulse for those machine cycles.

The μPB8228/8238D also provides the designer the ability to place a single interrupt instruction onto the bus without adding additional components. By connecting the +12 volt supply to the $\overline{\text{INTA}}$ output (pin 23) of the μPB8228/8238D through a 1K ohm series resistor, RESTART 7 will be gated onto the processor data bus when DBIN is active during an interrupt acknowledge machine cycle.

$\overline{\text{MEM/W}}$ and $\overline{\text{I/OW}}$ are generated by gating the $\overline{\text{WR}}$ signal from the processor with the contents of the status latch. $\overline{\text{I/OW}}$ indicates that an output port write is about to occur. $\overline{\text{MEM/W}}$ indicates that a memory write will occur.

The data bus output buffers and control signal buffers can be asynchronously forced into a high impedance state by placing a high on the $\overline{\text{BUSEN}}$ pin of the μPB8228/8238. Normal operation is performed with $\overline{\text{BUSEN}}$ low.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.5 to 5.5 Volts
Output Currents	100 mA

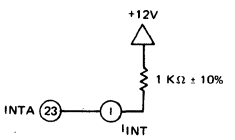
COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input Clamp Voltage, All Inputs	V_C			−1.0	V	V_{CC} = 4.75V; I_{CC} = −5 mA
Input Load Current, $\overline{STSTB}$	I_F			500	μA	V_{CC} = 5.25V V_F = 0.45V
D_2 and D_6				750	μA	
D_0, D_1, D_4, D_5, and D_7				250	μA	
All Other Inputs				250	μA	
Input Leakage Current, $\overline{STSTB}$	I_R			100	μA	V_{CC} = 5.25V V_R = 5.0V
DB_0 through DB_7				20	μA	
All Other Inputs				100	μA	
Input Threshold Voltage, All Inputs	V_{TH}	0.8		2.0	V	V_{CC} = 5V
Power Supply Current	I_{CC}			190	mA	V_{CC} = 5.25V
Output Low Voltage, D_0 through D_7	V_{OL}			0.45	V	V_{CC} = 4.75V; I_{OL} = 2 mA
All Other Outputs				0.48	V	I_{OL} = 10 mA
Output High Voltage, D_0 through D_7	V_{OH}	3.6			V	V_{CC} = 4.75V; I_{OH} = −10 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Short Circuit Current, All Outputs	I_{OS}	15		90	mA	V_{CC} = 5V
Off State Output Current, All Control Outputs	$I_{O(off)}$			100	μA	V_{CC} = 5.25V; V_O = 5.0V
				−100	μA	V_O = 0.45V
INTA Current	I_{INT}			5	mA	(See Figure below)



INTA TEST CIRCUIT

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			12	pF	V_{BIAS} = 2.5V,
Output Capacitance Control Signals	C_{OUT}			15	pF	V_{CC} = 5.0V,
I/O Capacitance (D or DB)	$C_{I/O}$			15	pF	f = 1 MHz

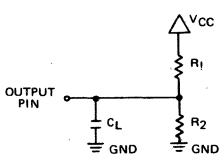
NOTE: This parameter is periodically sampled and not 100% tested.

AC CHARACTERISTICS

$T_a = 0°C$ to $70°C$, $V_{CC} = 5V \pm 5\%$

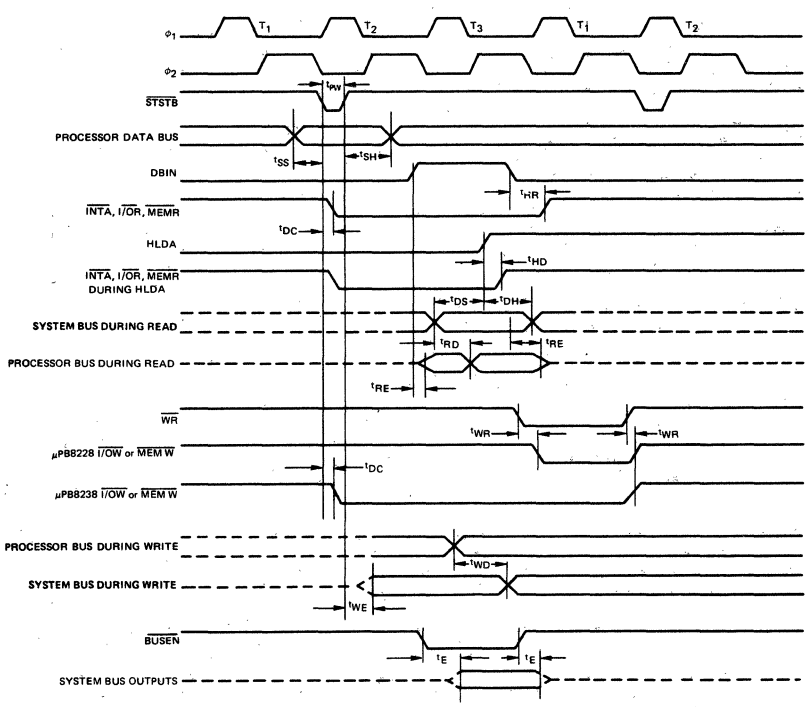
PARAMETER	SYMBOL	LIMITS MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Width of Status Strobe	t_{PW}	22			ns	
Setup Time, Status Inputs D_0-D_7	t_{SS}	8			ns	
Hold Time, Status Inputs D_0-D_7	t_{SH}	5			ns	
Delay from $\overline{STSTB}$ to any Control Signal	t_{DC}	20		60	ns	$C_L = 100$ pF
Delay from DBIN to Control Outputs	t_{RR}			30	ns	$C_L = 100$ pF
Delay from DBIN to Enable/ Disable 8080A Bus	t_{RE}			45	ns	$C_L = 25$ pF
Delay from System Bus to 8080A Bus during Read	t_{RD}			30	ns	$C_L = 25$ pF
Delay from $\overline{WR}$ to Control Outputs	t_{WR}	5		45	ns	$C_L = 100$ pF
Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$	t_{WE}			30	ns	$C_L = 100$ pF
Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	t_{WD}	5		40	ns	$C_L = 100$ pF
Delay from $\overline{\text{System Bus Enable}}$ to System Bus DB_0-DB_7	t_E			30	ns	$C_L = 100$ pF
HLDA to Read Status Outputs	t_{HD}			25	ns	
Setup Time, System Bus Inputs to HLDA	t_{DS}	10			ns	
Hold Time, System Bus Inputs to HLDA	t_{DH}	20			ns	$C_L = 100$ pF

For D_0-D_7: $R_1 = 4$ KΩ, $R_2 = \infty\Omega$, $C_L = 25$ pF. For all other outputs: $R_1 = 500\Omega$, $R_2 = 1$ KΩ, $C_L = 100$ pF.



TEST CIRCUIT

TIMING WAVEFORMS



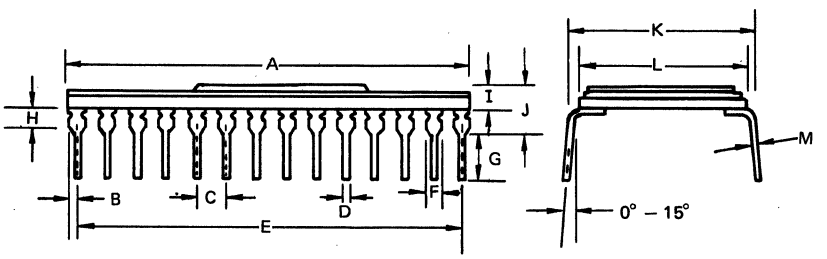
VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

8

STATUS WORD CHART

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE (M_1)	INT. ACK. (M_2, M_3)	HALT ACKNOWLEDGE	INT. ACK. WHILE HALT	
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	⑪	Ⓝ STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	1	0	1	
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	0	1	0	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	0	μPD8080A OUTPUT
D_5	M_1	1	0	0	0	0	0	0	1	0	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	0	
D_7	MEMR	1	1	0	1	0	0	0	0	0	0	0	
24	$\overline{MEMR}$	0	0	1	0	1	1	1	1	1	1	1	
26	$\overline{MEMW}$	1	1	0	1	0	1	1	1	1	1	1	μPB8228/8238 OUTPUT
25	$\overline{I/OR}$	1	1	1	1	1	0	1	1	1	1	1	
27	$\overline{I/OW}$	1	1	1	1	1	1	0	1	1	1	1	
23	$\overline{INTA}$	1	1	1	1	1	1	1	0	0	1	0	
PIN NO.		SIGNAL STATUS											
		μPB8228/8238 CONTROL SIGNALS											

PACKAGE OUTLINE μPB8228/8238D



ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.42 MAX.
B	1.5 MAX.	0.59 MAX.
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.30
F	1.27	0.05
G	3.2 MIN.	0.13 MIN.
H	1.9	0.07
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

MAGNETIC TAPE CASSETTE/ CARTRIDGE CONTROLLER

DESCRIPTION

The NEC μPD371 is a high performance N-Channel LSI tape cassette/cartridge controller designed to interface between most cassette or cartridge tape drives and most microprocessors or minicomputers.

The μPD371 converts 8-bit parallel data into serial phase encoded data to be written on tape and converts phase encoded data read from tape into 8-bit parallel data, calculates the CRC during write operations, verifies the CRC during read operations, informs the processor program when to send data bytes during write operations and when to read bytes during read operations, converts tape drive status signals into register bit levels which may be read by the processor program and converts software commands into signals which may be understood by the tape drive(s).

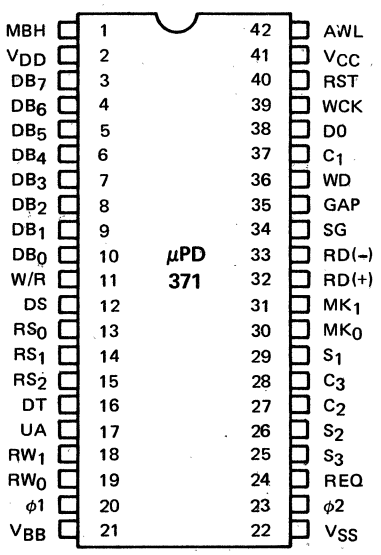
The μPD371 read and write data paths are completely separate to allow read-after-write data verification.

The μPD371 places no limitation on the selection of tape speed since the μPD371 maximum data transfer rate is considerably faster than that of the fastest cassette or cartridge drive.

FEATURES

- Compatible with ANSI, ECMA and ISO standard
- Also compatible with most other standards
- Hardware CRC generation and verification
- Read-after-write capability
- High speed file search
- Multiple drive capability
- May read or write on one drive while rewinding or file searching on another
- Maximum Data Transfer rate of 375K bits/sec equivalent to 468 IPS at 800 BPI

PIN CONFIGURATION



8

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−40°C to +125°C
All Output Voltages	−1 to +8 Volts ①
All Input Voltages	−1 to +8 Volts ①
Clock Voltages	−1 to +16 Volts ①
Supply Voltage V_{DD}	−1 to +16 Volts ①
Supply Voltage V_{CC}	−1 to +8 Volts ①
Supply Voltage V_{BB}	−10 to 0 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

Note: ① V_{BB} = −5V ± 5%. All voltages measured with respect to GND.

DC CHARACTERISTICS

T_a = 0 − 70°C V_{DD} = +12V ± 5% V_{CC} = +5V ± 5% V_{BB} = −5V ± 5% V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	0		+0.8	V	
Output High Voltage	V_{OH}	+3.5			V	I_{OH} = −1 mA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +1.7 mA
Clock Input High Voltage	V_{OH}	+9		V_{DD}	V	
Clock Input Low Voltage	V_{OL}	0		+0.65	V	
Input Leakage Current	I_{LIH}			+10	μA	V_I = +3.0V
Input Leakage Current: $DB_0 - DB_7$	$I_{LIL\,1}$			−10	μA	V_I = +0.8V
Input Leakage Current: All Except $DB_0 - DB_7$ (~25K Internal Pull-ups)	$I_{LIL\,2}$			−1.0	mA	V_I = +0.4V
Clock Input Leakage Current	I_{LOH}			+20	μA	V_O = +9.0V
Clock Input Leakage Current	I_{LOL}			−20	μA	V_O = +0.65V
Output Leakage Current	I_{LOH}			+10	μA	V_O = +3.5V
Output Leakage Current	I_{LOL}			−10	μA	V_O = +0.4V
Power Supply Current (V_{DD})	I_{DD}		+20		mA	
Power Supply Current (V_{CC})	I_{CC}		+30		mA	
Power Supply Current (V_{BB})	I_{BB}			−2	mA	

CAPACITANCE

T_a = 25°C, V_{DD} = V_{CC} = V_{SS} = 0V, V_{BB} = −5V

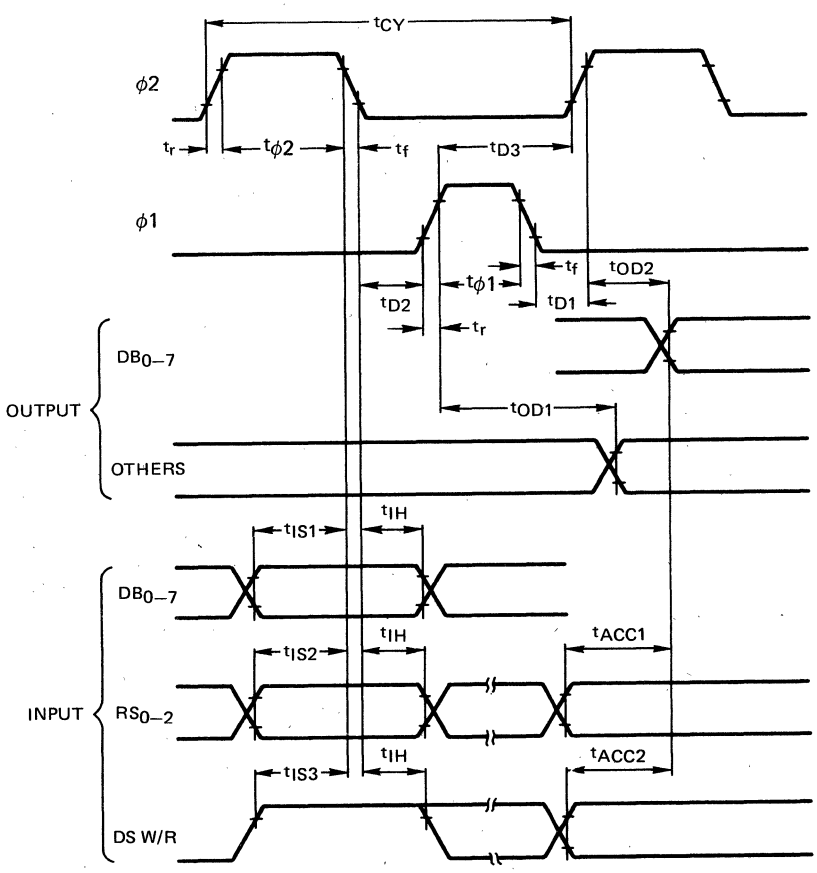
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_O			35	pF	fc = 1 MHz. All pins except measuring pin are grounded.
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

AC CHARACTERISTICS

$T_a = 0 - 70°C$, $V_{DD} = +12V \pm 5\%$, $V_{CC} = +5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$, $V_{SS} = CU$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Clock Period	t_{CY}	480		5000	ns	
Clock Rise and Fall Times	t_r, t_f	0		50	ns	
$\phi1$ Pulse Width	$t_{\phi1}$	60			ns	
$\phi2$ Pulse Width	$t_{\phi2}$	220			ns	
$\phi1$ to $\phi2$ Delay	t_{D1}	0			ns	
$\phi2$ to $\phi1$ Delay	t_{D2}	70			ns	
Delay $\phi1$ to $\phi2$ Lead Edges	t_{D3}	80			ns	
Data Out Delay from $\phi1$	t_{OD1}			480	ns	1TTL & CL = 30 pF
Data Out Delay from $\phi1$	t_{OD2}			260	ns	1TTL & CL = 30 pF
$RS_0 - RS_2$ to Output Delay	t_{ACC1}			300	ns	1TTL & CL = 30 pF
DS, W/R to Output Delay	t_{ACC2}			200	ns	1TTL & CL = 30 pF
$DB_0 - DB_7$ to $\phi2$ Setup Time	t_{IS1}	250			ns	
$RS_0 - RS_2$ to $\phi2$ Setup Time	t_{IS2}	350			ns	
DS, W/R to $\phi2$ Setup Time	t_{IS3}	150			ns	
Input Hold Time from $\phi2$	t_{IH}	30			ns	

TIMING WAVEFORMS



Note: Timing Measurement Levels:
Clock High/Low Voltage = 9.0V/0.65V
Input High/Low Voltage = 3.0V/0.8V
Output High/Low Voltage = 2.0V/0.8V

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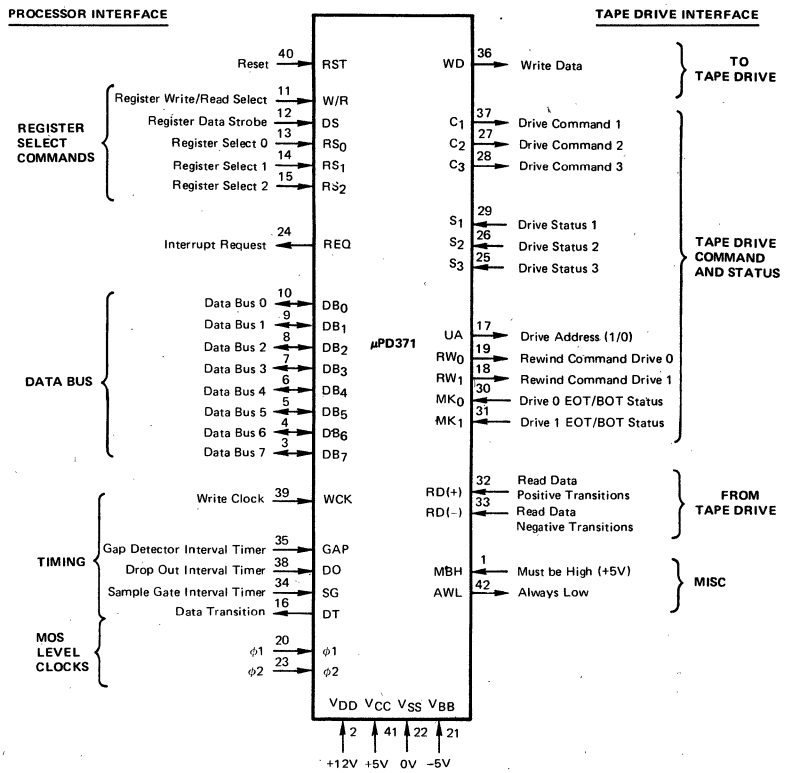
PIN IDENTIFICATION①

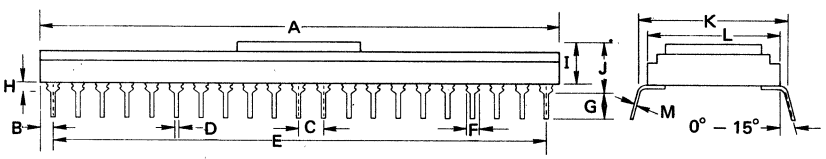
PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
RESET			
40	RST	Reset	A logic one at this pin causes a general reset of the μPD371.
REGISTER SELECT COMMANDS AND DATA BUS			
11	W/R		W/R, DS and RS_0 – RS_2 control Data Bus transfers between the μPD371 and the processor as follows: Writing into a μPD371 register: When W/R is a logic one, information the processor places on DB_0 – DB_7 is written into the μPD371 WRITE REGISTER selected by RS_0 – RS_2. The information is strobed into the register by a logic one at DS. Reading from a μPD371 register: When W/R is a logic zero, information from the μPD371 READ REGISTER selected by RS_0 – RS_2 is placed on DB_0 – DB_7 to be read by the processor. The information remains on DB_0 – DB_7 as long as DS is a logic one.
12	DS		
13 – 15	RS_0 – RS_2		
3 – 10	DB_0 – DB_7	Data Bus	
INTERRUPT REQUEST			
24	REQ		The μPD371 may be operated with either interrupt or polling techniques. If the interrupt technique is chosen, REQ should be connected to the interrupt request input of the processor. There are three sources of interrupt: READ BUFFER FULL, WRITE BUFFER EMPTY and GAP DETECTION.
TIMING			The user must provide four timing signals to the μPD371 – one for write operations and three for read operations. Each is defined in terms of T, where T is the period between successive data transitions in the phase encoded data written onto or read from tape.
39	WCK		WCK determines the WRITE DATA (WD, pin 36) transfer rate. WCK should have a period of 0.5T. DT is a pulse provided by the μPD371 to be used in the generation of the three read timing signals – SG, DO, and GAP. DT occurs at each data transition in the data read from tape. The internal read data sample gate is closed following each data transition and is reopened by a positive transition at SG 0.75T μsec after each DT pulse. A positive transition should be made at DO whenever a DT pulse stream ceases for a period of 1.5T μsec. A positive transition should be made at GAP whenever a DT pulse stream ceases for a period of 4T μsec. $\phi1$ and $\phi2$ are MOS level (12V) clock pulses. The timing of $\phi1$ and $\phi2$ is shown in the Timing Diagram.
16	DT		
34	SG		
38	DO		
35	GAP		
20	$\phi1$		
23	$\phi2$		
WRITE DATA			
36	WD		Phase encoded data to be written on tape leaves the μPD371 at pin 36.
TAPE DRIVE COMMAND AND STATUS			
37	C_1		C_1, C_2 and C_3 are general purpose tape drive commands. C_1, C_2 and C_3 are set and reset by the software manipulation of bits 5, 6 and 7, respectively, in Write Register 3. Since C_1, C_2 and C_3 are defined by software, they may be configured for any purpose. Typical uses for C_1, C_2 and C_3 are WRITE ENABLE, FORWARD and REVERSE.
27	C_2		
28	C_3		
29	S_1		S_1, S_2 and S_3 are general purpose tape drive status inputs. Their logic levels are indicated by bits 3, 4 and 7 of Read Register 1, respectively. Typical tape drive status signals are WRITE PERMIT, CASSETTE IN PLACE and SIDE. The μPD371 can adapt to any tape drive status signal set with a slight change in software.
26	S_2		
25	S_3		
DUAL TAPE DRIVE SYSTEM COMMAND AND STATUS			
17	UA	Unit Address	Selects Drive 0 when low and Drive 1 when high.
19	RW_0	Rewind 0	Rewind Command for Drive 0.
18	RW_1	Rewind 1	Rewind Command for Drive 1.
30	MK_0	Marker 0	EOT/BOT status from Drive 0.
31	MK_1	Marker 1	EOT/BOT status from Drive 1.
READ DATA			
32	RD(+)	Read Data (+)	A positive pulse from the tape drive at each positive transition in the read data.
33	RD(–)	Read Data (–)	A positive pulse from the tape drive at each negative transition in the read data.
MISCELLANEOUS			
1	MBH		MBH must be tied to the V_{CC} (+5V) supply.
42	AWL		AWL is a logic low output under all normal operating conditions of the μPD371.
POWER SUPPLY VOLTAGES			
2	V_{DD}		+12V
41	V_{CC}		+5V
22	V_{SS}		Ground
21	V_{BB}		–5V

Note: ① Refer to diagram on following page.

PIN IDENTIFICATION (CONT.)



PACKAGE OUTLINE μPD371



ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

ADDRESSABLE INTERNAL REGISTERS

From the point of view of the processor program, the μPD371 makes the tape drive (or multiple drive system) appear as ten addressable registers. The program controls the drive(s) and transmits data to be written on tape by manipulating bits in the six μPD371 Write Registers. The program senses the status of the drive(s) and reads data stored on tape by reading bits from the four μPD371 Read Registers.

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS_2	RS_1	RS_0		7	6	5	4	3	2	1	0
				WRITE REGISTERS								
1	0	0	0	WR_0	RST	MBL	SRS	WME	WCR	X	WMD	GNT
1	0	0	1	WR_1	WRR	RRR	X	RRE	RRD	GRE	GRD	X
1	0	1	0	WR_2	WD_7	WD_6	WD_5	WD_4	WD_3	WD_2	WD_1	WD_0
1	0	1	1	WR_3	C_3	C_2	C_1	RRI	RW	X	X	X
1	1	0	1	WR_5	X	X	X	RME	RMD	X	X	X
1	1	1	0	WR_6	X	X	X	X	X	X	X	UA
				READ REGISTERS								
0	0	0	0	RR_0	AWH	AWL	C_2	C_3	RDF	GRQ	WRQ	RRQ
0	0	0	1	RR_1	S_3	MK	MKF	S_2	S_1	RW	C_1	UA
0	0	1	0	RR_2	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0
0	0	1	1	RR_3	WD	GPF	REC	CRE	DOE	COR	NBR	NAR

X = NOT USED

ADDRESSABLE INTERNAL REGISTER BIT IDENTIFICATION

BIT	SYMBOL	NAME
WRITE REGISTER 0		
0	GNT	Gap Noise Tolerance
1	WMD	Write Mode Disable
2	–	Not used
3	WCR	Write CRC
4	WME	Write Mode Enable
5	SRS	Status Reset
6	MBL	Must Be Low
7	RST	Reset
WRITE REGISTER 1		
0	–	Not used
1	GRD	Gap Request Disable
2	GRE	Gap Request Enable
3	RRD	Read Request Disable
4	RRE	Read Request Enable
5	–	Not used
6	RRR	Read Request Reset
7	WRR	Write Request Reset
WRITE REGISTER 2		
0 – 7	WD_0 – WD_7	Write Buffer Register
WRITE REGISTER 3		
0	–	Not used
1	–	Not used
2	–	Not used
3	RW	Rewind
4	RRI	Rewind Reset Inhibit
5	C_1	Command One
6	C_2	Command Two
7	C_3	Command Three
WRITE REGISTER 4		
–	–	Not used
WRITE REGISTER 5		
0	–	Not used
1	–	Not used
2	–	Not used
3	RMD	Read Mode Disable
4	RME	Read Mode Enable
5	–	Not used
6	–	Not used
7	–	Not used

BIT	SYMBOL	NAME
WRITE REGISTER 6		
0	UA	Unit Address
1 – 7	–	Not used
READ REGISTER 0		
0	RRQ	Read Request
1	WRQ	Write Request
2	GRQ	Gap Request
3	RDF	Read Flag
4	C_3	Command 3
5	C_2	Command 2
6	AWL	Always Low
7	AWH	Always High
READ REGISTER 1		
0	UA	Unit Address
1	C_1	Command 1
2	RW	Rewind
3	S_1	Status 1
4	S_2	Status 2
5	MKF	Marker Flag
6	MK	Marker
7	S_3	Status 3
READ REGISTER 2		
0 – 7	RD_0 – RD_7	Read Buffer Register
READ REGISTER 3		
0	NAR	Noise After Record
1	NBR	Noise Before Record
2	COR	Command Overrun
3	DOE	Drop Out Error
4	CRE	CRC Error
5	REC	Record Detection
6	GPF	Gap Flag
7	WD	Write Data

FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD372D is a single LSI floppy disk controller chip which contains the circuitry to read, write, track seek, load and unload the head, generate and detect CRC characters, and perform all other floppy disk operations. It is completely compatible with the IBM, Minifloppy*TM, hard sector, and other formats and controls up to 4 floppy disk drives. The μPD372D may be interfaced directly to a host processor; or to a controller processor first, which in turn is interfaced to the host. These processors do not necessarily have to be of the 8080A type.

Data transfers to and from the μPD372D are done through addressable internal registers. These internal regsiters allow a large variety of system architectures to be configured; they provide status information on the drive, as well as perform data transfers between the drive and the processor.

The μPD372D issues interrupts to the processor upon detection of an address mark and then when each subsequent data byte is available during either reading or writing. An 8-bit bi-directional data bus and 5 register select lines provide access to the 9 internal registers' contents. An internal interval timer is provided which facilitates performing such drive timing functions as: stepping rate, head settling time, track settling time, etc.

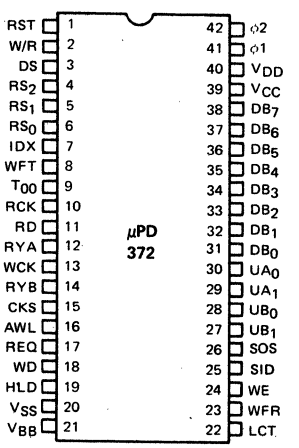
*TMShugart Associates.

FEATURES

- Compatible with IBM 3740 format
- Also compatible with other formats including Minifloppy and hard sector
- Controls up to four floppy disk drives
- Can perform overlap seeks
- Input and output TTL compatible (except for $\phi 1$ and $\phi 2$)
- Interfaces to most microprocessors including 8080A
- Standard power supplies (+12V, +5V and -5V)
- Controls most floppy disk drives including:

CALCOMP 140, 142	ORBIS 74, 76/77
CDC BR803	PERSCI 70, 75
INNOVEX 210, 410	REMEX RFS 7400
PERTEC FD400	SHUGART SA400 (Minifloppy)
POTTER DD4740	WANGCO 82 (Minifloppy)
SHUGART SA900, SA800	GSI MDD50 (Minifloppy)
GSI 110	

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
All Output Voltages . . . . . −1.0 to +8 Volts①
All Input Voltages . . . . . −1.0 to +8 Volts①
Clock Voltage . . . . . −1.0 to +16 Volts①
Supply Voltage V_{DD} . . . . . −1.0 to +16 Volts①
Supply Voltage V_{CC} . . . . . −1.0 to +8 Volts①
Supply Voltage V_{BB} . . . . . −10 to +0 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

Note: ① V_{BB} = −5V ± 5%

DC CHARACTERISTICS

T_a = −70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH}	+3.0		V_{CC}	V	
Low Level Input Voltage	V_{IL}	0		+0.8	V	
High Level Output Voltage	V_{OH}	+3.5			V	I_{OH} = −1.0 mA
Low Level Output Voltage	V_{OL1}①			+0.5	V	I_{OL} = +1.7 mA
	V_{OL2}②			+0.5	V	I_{OL} = +3.3 mA
High Level Clock Voltage	$V_{\phi H}$	+9		V_{DD}	V	
Low Level Clock Voltage	$V_{\phi L}$	0		+0.8	V	
High Level Input Leakage Current	I_{LIH}			+10	μA	V_I = +3.0V
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_I = +0.8V
High Level Clock Leakage Current	$I_{L\phi H}$			+10	μA	V_ϕ = +9.0V
Low Level Clock Leakage Current	$I_{L\phi L}$			−10	μA	V_ϕ = +0.8V
High Level Output Leakage Current	I_{LOH}			+10	μA	V_O = +3.5V
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_O = +0.5V
Power Supply Current (V_{DD})	I_{DD}		+20		mA	
Power Supply Current (V_{CC})	I_{CC}		+23		mA	
Power Supply Current (V_{BB})	I_{BB}			−2	mA	

Notes: ① CKS, REQ, UA_0, UA_1, UB_0, UB_1, DB_0–DB_7.
② WD, HLD, LCT, WE, WFR, SOS, SID.

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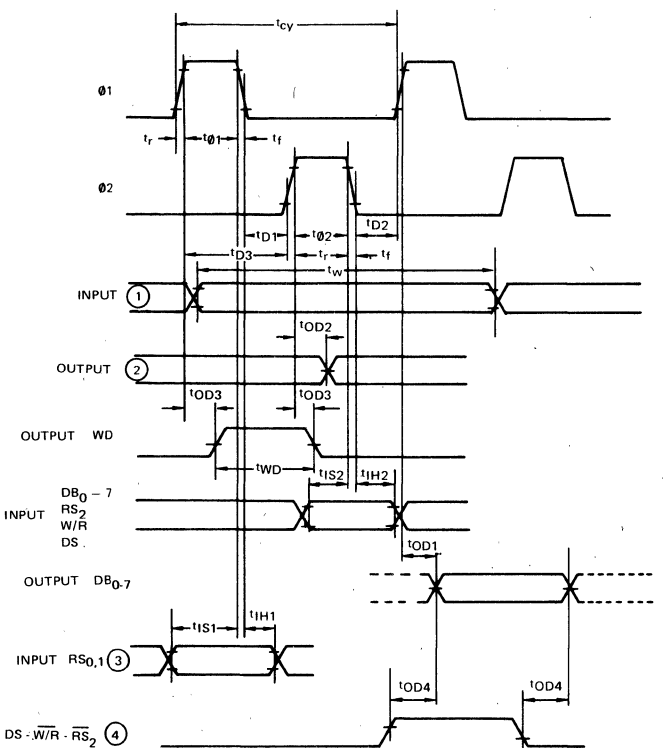
AC CHARACTERISTICS

T_a = 0 −70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY}	480		2000	ns	
Clock Rise and Fall Times	t_r, t_f	0		50	ns	
ϕ_1 Pulse Width	$t_{\phi 1}$	60			ns	
ϕ_2 Pulse Width	$t_{\phi 2}$	90			ns	
ϕ_1 to ϕ_2 Delay	t_{D_1}	0			ns	
ϕ_2 to ϕ_1 Delay	t_{D_2}	70			ns	
Delay ϕ_1 to ϕ_2 Leading Edges	t_{D_3}	100			ns	
Data Out Delay from ϕ_1	t_{OD_1}			90	ns	1 TTL and C_i = 30 pF
Data Out Delay from ϕ_2 ①	t_{OD_2}			200	ns	1 TTL and C_i = 30 pF
Data Out Delay from ϕ_2 ②	t_{OD_2}			200	ns	2 TTL and C_i = 50 pF
WD Delay Time	t_{OD_3}			120	ns	2 TTL and C_i = 50 pF
Data Out Delay from DS · $\overline{W/R}$ · $\overline{RS_2}$	t_{OD_4}			200	ns	
Data Setup Time to ϕ_1	t_{IS_1}	150			ns	
Data Setup Time to ϕ_2	t_{IS_2}	120			ns	
Data Hold Time from ϕ_1	t_{IH_1}	10			ns	
Data Hold Time from ϕ_2	t_{IH_2}	10			ns	
WD pulse width	t_{WD}	t_{D3}-40	t_{D_3}		ns	
Input pulse width ③	t_W	t_{CY}+150			ns	

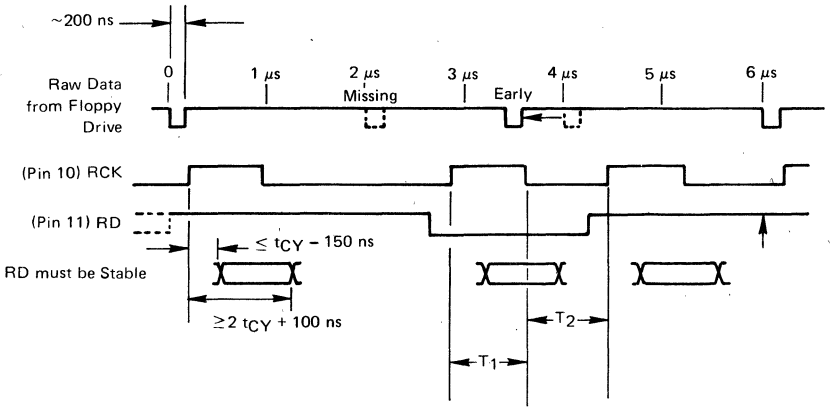
Notes: ① CKS, AWL, REQ, UA_0, UA_1, UB_0, UB_1.
② HLD, LCT, WFR, WE, SOS, SID.
③ IDX, RYA, RYB, RST, WFT, T_{00}, WCK, RCK.

TIMING WAVEFORMS



Notes: ① IDX, RYA, RYB, RST, WFT, T_{OO}, WCK, RCK.
② CKS, WFR, SOS, SID, REQ, HLD, $UA_{\phi,1}$, $UB_{\phi,1}$, WE, LCT.
③ RS_O, RS_1 input must not make level transition within t_{IS1} and t_{IH1} times, or register contents may be modified.
④ The logic condition which places μPD372 information on DB_{0-7} is DS · $\overline{W/R}$ · $\overline{RS_2}$. Care must be taken to insure that this condition is not met inadvertently if DS, W/R and RS_2 are allowed to change state asynchronously.

READ CLOCK (RCK) AND READ DATA (RD) REQUIRED BY μPD372

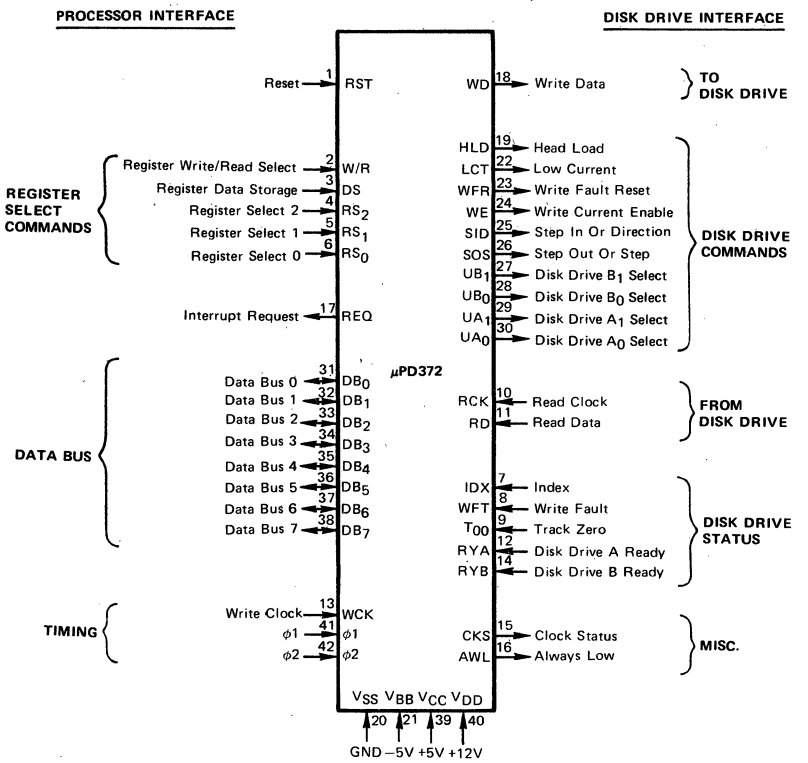


Notes: ① $t_{CY} = \phi 1$ Clock Period
② $T_1 \geq t_{CY} + 160$ ns
③ $T_2 \geq t_{CY} + 160$ ns

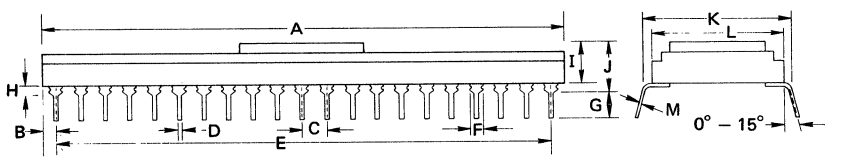
PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION	FUNCTION
1	RST	Reset	Input	Processor	Initializes internal registers, counters and F/F's
2	W/R	Register Write/ Read Select			W/R = 1 implies DB_{0-7} data written into μPD372 registers
3	DS	Data Strobe			DB_{0-7} Write and read strobe
4-6	RS_ϕ RS_1 RS_2	Register Select			Internal Register Select
7	IDX	Index		FDD	Pulse Signal that indicates start of Disk track
8	WFT	Write Fault			Write Fault Signal
9	T_{00}	Track 00			Indicates that Head is positioned on Track 00
10	RCK	Read Clock			
11	RD	Read Data			
12	RYA	Ready A			Indicates that FDD A is Ready
13	WCK	Write Clock		Processor	
14	RYB	Ready B		FDD	Indicates that FDD B is Ready
15	CKS	Clock States	Output		
16	AWL	Always Low			Always a logic zero
17	REQ	Request		Processor	Interrupt Request
18	WD	Write Data		FDD	Serial Write Data (Clock & Data Bits)
19	HLD	Head Load			Command which causes R/W head to contact disk
22	LCT	Low Current			Command to lower write current for inner tracks
23	WFR	Write Fault Reset			Signal to reset write fault latch
24	WE	Write Enable			
25	SID	Step In or Direction			R/W head step control
26	SOS	Step Out or Step			R/W head step control
27-30	UA_0, UA_1 UB_0, UB_1	FDD Select			FDD Unit Select
31-38	DB_{0-7}	Data Bus	Input/ Output	Processor	Bi-directional data bus

PIN IDENTIFICATION (CONT.)



PACKAGE OUTLINE μPD372D



ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

INTERNAL REGISTER IDENTIFICATION

BIT	SYMBOL	NAME	FUNCTION
		WRITE REGISTER 0	
0		Not Used	
1	WFR	Write Fault Reset	Resets Pin 23 to Zero
2	LCT	Low Current	Sets Pin 22, Should be Zero for TRKS > 43
3	HLD	Head Load	Sets Pin 19, Loading FDD Head
4		Not Used	
5		Not Used	
6	MBL	Must Be Low	
7	RST	Reset	Software Reset, Same Effect as Pin 1
		WRITE REGISTER 1	
0	UA_0	Unit A_0 Select	Device Select Pin 30
1	UA_1	Unit A_1 Select	Device Select Pin 29
2	UAS	Unit A Strobe	Strobe for Enabling UA_0 and OA_1 to be Loaded
3	CB_3	Clock Bit 3	Enables Clock Pulse #3 to be Written
4	CB_4	Clock Bit 4	Enables Clock Pulse #4 to be Written
5	CB_5	Clock Bit 5	Enables Clock Pulse #5 to be Written
6		Not Used	
7	CBS	Clock Bit Strobe	Enables Clock Bits to be Loaded
		WRITE REGISTER 2	
0	WD_0	Write Data Bit 0	
1	WD_1	Write Data Bit 1	
2	WD_2	Write Data Bit 2	
3	WD_3	Write Data Bit 3	
4	WD_4	Write Data Bit 4	
5	WD_5	Write Data Bit 5	
6	WD_6	Write Data Bit 6	
7	WD_7	Write Data Bit 7	
		WRITE REGISTER 3	
0	CCW	Cyclic Check Words	One During R/W, Zero for CRC Reset
1	CCG	Cyclic Check Generator Start	Starts CRC Generator in Write Mode
2	WER	Write Enable Reset	Resets Pin 24 to Zero
3	IXS	Index Start	Enable Index Hole Detection
4	WES	Write Enable Set	Sets Pin 24 to One
5	STT	Start	Enables Read and Write Operations to Occur
6	WCS	Write Clock Set	Write Clock Selected
7	RCS	Read Clock Set	Read Clock Selected
		WRITE REGISTER 4	
0	UB_0	Unit B_0 Select	Device Select Pin 28
1	UB_1	Unit B_1 Select	Device Select Pin 27
2	UBS	Unit B Strobe	Strobe for Enabling UB_0, UB_1 to be Loaded
3		Not Used	
4		Not Used	
5	SOS	Step Out or Step	Sets Pin 26 to One
6	SID	Step In or Direction	Sets Pin 25 to One
7	STS	Step Strobe	Enables SOS and SID to be Loaded
		WRITE REGISTER 5	
0–7		This Register Not Used	
		WRITE REGISTER 6	
0	DRR	Data Register Reset	Resets DRQ (RR_0 Bit 0)
1	IRR	Index Request Reset	Resets IRQ (RR_0 Bit 1)
2	TRR	Timer Request Reset	Resets TRQ (RR_0 Bit 2)
3		Not Used	
4		Not Used	
5		Not Used	
6		Not Used	
7		Not Used	

INTERNAL REGISTER IDENTIFICATION (CONT.)

BIT	SYMBOL	NAME	FUNCTION
		READ REGISTER 0	
0	DRQ	Data Request	Read Data Byte from RR_2 or Write Data Byte into WR_2
1	IRQ	Index Request	Set by Physical Index Pulse
2	TRQ	Timer Request	Set by Every 512th Write CLK Pulse
3	ERR	Error	Logical OR of WFT + RYA + COR
4	UB_0	Drive B_0 Selected	
5	UB_1	Drive B_1 Selected	
6	RYB	Drive B Ready	Ready Signal from Pin 14
7	ALH	Always High	Always Contains a Logical One
		READ REGISTER 1	
0	UA_0	Drive A_0 Selected	
1	UA_1	Drive A_1 Selected	
2	WFT	Write Fault	Indicates Status of Pin 8
3	RYA	Drive A Ready	Indicates Status of Pin 12
4	COR	Command Overrun	Processor Did Not Respond in Time to a DRQ
5	DER	Data Error	CRC Error During Read
6	T_{00}	Track Zero	Indicates Status of Pin 9
7	WRT	Write Mode	Indicates which Clock WCK or RCK has been Selected
		READ REGISTER 2	
0	RD_0	Read Data Bit 0	
1	RD_1	Read Data Bit 1	
2	RD_2	Read Data Bit 2	
3	RD_3	Read Data Bit 3	
4	RD_4	Read Data Bit 4	
5	RD_5	Read Data Bit 5	
6	RD_6	Read Data Bit 6	
7	RD_7	Read Data Bit 7	

ADDRESSABLE INTERNAL REGISTERS

Data is transferred to the μPD372's internal addressable registers by signals W/R (Write=1, Read=0), DS (Data Strobe) and RS_0–RS_2 (Register Select 0, 1 and 2). Timing constraints for these signals are shown in the Timing Diagram. Diagram below shows register allocations and functional content.

REGISTER ADDRESS				REGISTER NAME	BIT NUMBERS							
W/R	RS_2	RS_1	RS_0		7	6	5	4	3	2	1	0
				WRITE REGISTERS								
1	0	0	0	WR_0	RST	MBL	X	X	HLD	LCT	WFR	X
1	0	0	1	WR_1	CBS	X	CB_5	CB_4	CB_3	UAS	UA_1	UA_0
1	0	1	0	WR_2	WD_7	WD_6	WD_5	WD_4	WD_3	WD_2	WD_1	WD_0
1	0	1	1	WR_3	RCS	WCS	STT	WES	TXS	WER	CCG	CCW
1	1	0	0	WR_4	STS	SID	SOS	X	X	UBS	UB_1	UB_0
1	1	1	0	WR_6	X	X	X	X	X	TRR	IRR	DRR
				READ REGISTERS								
0	0	0	0	RR_0	ALH	RYB	UB_1	UB_0	ERR	TRQ	IRQ	DRQ
0	0	0	1	RR_1	WRT	T_{00}	DER	COR	RYA	WFT	UA_1	UA_0
0	0	1	0	RR_2	RD_7	RD_6	RD_5	RD_4	RD_3	RD_2	RD_1	RD_0

X = NOT USED

SP372-8-77-GN-CAT

SYNCHRONOUS RECEIVER/TRANSMITTER

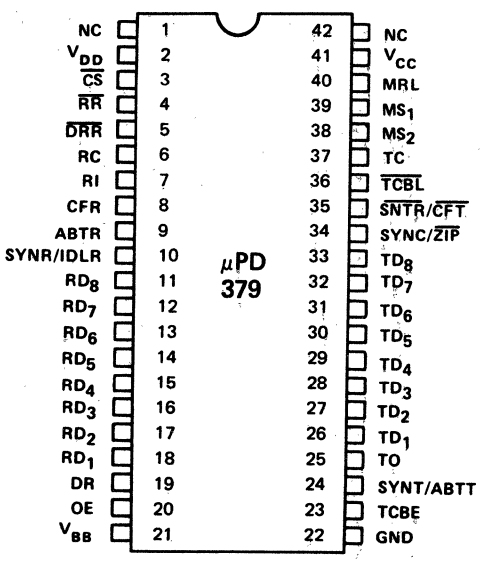
DESCRIPTION

The μPD379 Synchronous Receiver/Transmitter is an MOS LSI monolithic circuit that performs all the receiving and transmitting functions associated with Basic and High Level Data Link Control Procedures. This circuit is fabricated using N-channel AL-Gate MOS technology, allowing all inputs and outputs to be directly TTL compatible. The operation mode, baud rate and synchronous character are changeable through the use of external control. The μPD379 is packaged in a 42 pin Dual-in-line ceramic package.

FEATURES

- Suitable for Synchronous Basic and High Level Data Link Control Procedures (BiSync or SDLC)
- Full or Half Duplex Operation
- Fully Double Buffered Transmit and Receive
- Directly TTL Compatible
- Three-State Data Outputs
- Programmable Sync Word
- Detection/Rejection of Flag, Abort and Idle Patterns
- Zero Insertion and Rejection
- Indication of Overrun and Underrun Errors
- 800K Bits/Sec Operating Speed

PIN CONFIGURATION



NC: NO CONNECTION

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Basic Sync Mode Transmission

The Sync character may be 16 in hexadecimal or it may be set to any other pattern in the Closed Mode. When the mode control register is loaded with MS_1 = high and MS_2 = low, the μPD379 enters the Basic Sync mode from the Closed Mode. The Sync character is continuously transmitted until a transmission data character is loaded. After a data character is loaded, it is serialized and transmitted out from the TO (Transmitter Output) line. If an underrun occurs, Sync character(s) are again transmitted automatically until the next data character is loaded. Transmission data is sent out from LSB (TD_1) first to MSB (TD_8) last on the TO line.

Basic Sync Mode Receive

The RI (Receiver Input) line first searches for Sync characters. Once an 8-bit Sync character has been detected, the following received bits are treated as data characters and outputted on lines RD_1 – RD_8 in parallel.

When device operation is started, the receiver section should be first brought into Closed mode or should be reset in order to ensure synchronization.

SDLC Mode Transmission

Until a data character is loaded, the Flag pattern (7E in hexadecimal) is automatically transmitted continuously. After a data character is loaded, it is serialized and transmitted out from LSB (TD_1) to MSB (TD_8) on the TO line. In transmitting data characters, a dummy bit 0 is automatically inserted immediately following five (5) successive 1's. This is called Zero-Insertion and is performed in order to maintain synchronization with the receiver and to avoid duplication of Flag pattern in data characters. (Zero-Insertion may be prohibited optionally with the $\overline{ZIP}$ command, if necessary.) If an underrun occurs while data characters are being transmitted, an Abort pattern (FF in hexadecimal) and then a Flag pattern are automatically transmitted. After that, the Flag pattern is again automatically transmitted until the next data character is loaded.

If a low level is placed on the $\overline{CFT}$ (Closing Flag Transmit) line while a data character is being transmitted, a Closing Flag will be transmitted immediately following transmission of the current data character.

SDLC Mode Receive

First, the Flag pattern is searched for on the RI line. Once a Flag pattern is detected, inserted zero's are rejected from all the following characters except Flag, Abort (7 to 14 successive 1's) and Idle (15 successive 1's) patterns, and then deserialized and output on the RD_1 – RD_8 lines in parallel.

If an overrun occurs, all the following data inputs are neglected and the μPD379 goes back to the first stage to search for the next Flag pattern.

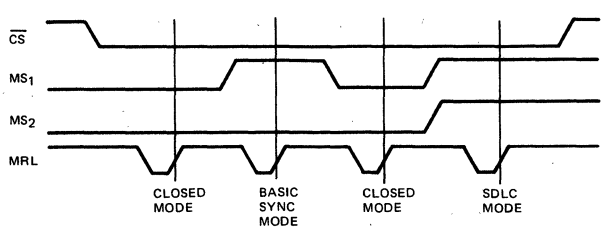
Closed Mode

When there is a change of mode, it must pass through the closed mode. In the closed mode, the following input signals may be used:

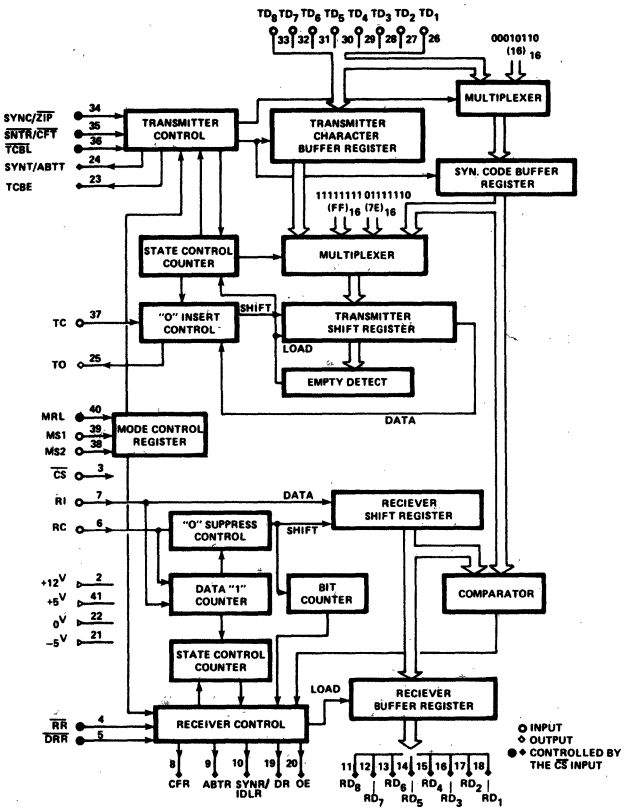
$\overline{CS}$, SYNC, $\overline{TCBL}$, MS1, MS2, MRL, TD_1 – TD_8

After leaving the closed mode, Sync characters are transmitted synchronously with the rising edge of TC. The receiver operates synchronously with the falling edge of RC, after $\overline{RR}$ = 1.

The following timing diagram shows how mode changes may be accomplished.



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	0°C to +70°C
Storage Temperature	-40°C to +125°C
All Output Voltages	0V to +8.0V ①
All Input Voltages	0V to +8.0V ①
Supply Voltage V_{CC}	0V to +8.0V ①
Supply Voltage V_{DD}	0V to +16.0V ①
Supply Voltage V_{BB}	10.0V to 0V

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

Note: ① V_{BB} = -5 ± 5%

AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = -5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Frequency	f_c	DC		800	KHz	TC, RC
Pulse Width	t_{PW}					TC, RC
		250			ns	MRL
		250			ns	$\overline{TCBL}$
		250			ns	$\overline{SNTR/CFT}$
		250			ns	$\overline{ZIP}$
		400			ns	$\overline{RR}$
		250			ns	$\overline{DRR}$
Setup Time	$t_{SET\ UP}$	250			ns	
Hold Time	t_{HOLD}	150			ns	
Rise Time	t_r			150	ns	
Fall Time	t_f			150	ns	
Pulse Interval	t_{cc}	100			ns	
Output Delay	t_{pd1}		180	270	ns	C_L = 20 pf
Time	t_{pd2}		410	600	ns	1 TTL Load
Fan Out	N			1		Standard TTL Load

*50% Duty Cycle

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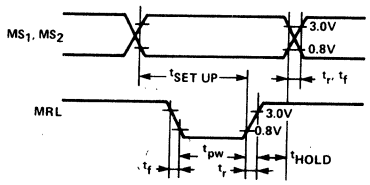
PIN IDENTIFICATION

PIN		FUNCTION	
NO.	SYMBOL	BASIC SYNC MODE	SDLC MODE
1	NC	No Connection	
2	V_{DD}	+12V Power Supply	
3	$\overline{CS}$	Chip Select – When "1", the following inputs are disabled and the outputs are put into the high impedance state: (Input Disabled) $\overline{RR}$, $\overline{DRR}$, SYNC/$\overline{ZIP}$, SYNR/$\overline{CFT}$, $\overline{TCBL}$, MRL; (Output-High Impedance) CFR, ABTR, SYNR/IDLR, RD_1 – RD_8, DR, OE, TCBE, CYNT/ABTT	
4	$\overline{RR}$	Receiver Reset – Receiver portion is reset with a "0" and operation is stopped RD_1 – RD_8 – – – – "1" CFR, ABTR, SYNR/IDLR, AR, OE – – – – "0"	
5	$\overline{DRR}$	Data Received Reset – Resets DR flag to "0"	
6	RC	Receiver Clock – Receiver clock input. Trailing edge of clock is located in the center of receiver input bits (RI).	
7	RI	Receiver Input – Received data serial input	
8	CFR	(Normally "0")	Closing Flag Received – Goes high whenever a Flag has been received during data reception. Goes low on the rising edge of DR or OE commands
9	ABTR	("0" Constant)	Abort Received – Becomes "1" when 7 – 14 continuous "1"s are received, after receiving the flag. Goes low on the rising edge of DR or OE commands.
10	SYNR / IDLR	Sync Character Received – Goes high when synchronization has occurred, or whenever the contents of the Sync Character Buffer and the contents of the Receiver Character Buffer coincide. Goes low when DR goes high and the RD_1 – RD_8 outputs are different from the Sync Character.	Idle Pattern Received – Becomes "1" (Idle) when it receives 15 consecutive "1"s. Goes low on the rising edge of DR or OE outputs.
11 – 18	RD_8 – RD_1	Receiver Data Outputs – Received character output terminal (RD_1:LSB RD_8:MSB)	
19	DR	Data Received – Goes high when the received character has been transferred from the Receiver Shift Register to the Receiver Buffer Register	
		DR does not go high for the first Sync Character input. It is reset when DRR is driven low.	DR does not go high for Flag, Abort or Idle Patterns. It is reset when (1) $\overline{DRR}$ = "0", (2) On the rising edge of OE, (3) Seven (7) successive "1"s have been received.
20	OE	Overrun Error – OE = "1" shows that DR was still high when the received character is moved from the receiving shift register to the receiving buffer register	
		OE is reset if DR is low when the received character is transferred from the Receiver Shift Register to the Receiver Buffer Register	It is reset on the rising edge of DR
21	V_{BB}	–5V Power Supply	
22	V_{SS}	Ground	
23	TCBE	Transmitter Character Buffer Register Empty – TCBE = "1" when the transmitter character buffer is empty.	
		TCBE is reset when $\overline{TCBL}$ is driven low	It is reset when: (1) $\overline{TCBL}$ = "0", (2) When $\overline{CFT}$ = "0" in the data transmission mode, (3) One-half bit before ABTT goes high.
24	SYNT / ABTT	SYNC Character Transmit – SYNT = "1" when a synchronous character is being transmitted. It is reset when: (1) $\overline{SNTR}$ = "0", (2) when transmission of data commences	Abort Pattern Transmit – ABTT = "1" when an Abort Pattern is being transmitted
25	TO	Transmitter Output – Transmitter data output. TO = "1" in the closed mode.	
26 – 33	TD_1 – TD_8	Transmitter Data Inputs – Transmitter character input. (TD_1 = LSB, TD_8 = MSB)	
34	SYNC / $\overline{ZIP}$	SYNC Character – In the Closed Mode, the SYNC line is used to select a SYNC character to be loaded into the SYNC Character Buffer. The selected SYNC character is loaded into the buffer on the rising edge of TCBL and is selected as follows: (1) When SYNC = "0", the character placed on the TD_1 – TD_8 inputs is loaded, (2) When SYNC = "1", 16 Hexadecimal is loaded.	Zero Insertion Prohibit – When $\overline{ZIP}$ is driven low, zero-insertion will be prohibited for all subsequent data characters until a Closing Flag or an Abort Pattern is transmitted.
35	$\overline{SNTR}$ / $\overline{CFT}$	SYNC Character Transmit Reset – When $\overline{SNTR}$ is driven low, SYNT is reset to "0".	Closing Flag Transmit – During transmission, $\overline{CFT}$ low causes the following operations to occur: (1) TCBE Output is reset to "0", (2) The Closing Flag will be transmitted after the end of transmission of the current data character.
36	$\overline{TCBL}$	Transmitter Character Buffer Load – (1) In the closed Mode: the SYNC Character Buffer is loaded on the rising edge of $\overline{TCBL}$. If the SYNC input is low, the buffer is loaded with the data on the TD_1 – TD_8 inputs; if SYNC is high, the buffer is loaded with (16) Hex. (2) In the Basic SYNC or SDLC Modes: When $\overline{TCBL}$ is driven low (a) TCBE is reset to "0" and (b) the data character on the TD_1 – TD_8 inputs is loaded into the Transmitter Character Buffer. The loaded character is latched on the rising edge of $\overline{TCBL}$.	
37	TC	Transmitter Clock – Clock input for transmission.	
38	MS_2	Mode Select 2	
39	MS_1	Mode Select 1 Used to select one of three modes. MS_1 MS_2 MODE L L Closed Mode L H Closed Mode H L Basic Synchronous Mode H H SDLC Synchronous Mode In the closed mode TO and RD_1 – RD_8 are high, all other outputs are low.	
40	MRL	Mode Control Register Load – When MRL is low, the operational mode is selected by the current status of MS_1 and MS_2. When MRL goes high, the operational mode is latched based upon the status of MS_1 and MS_2.	
41	V_{CC}	+5V Power Supply	
42	NC	No Connection	

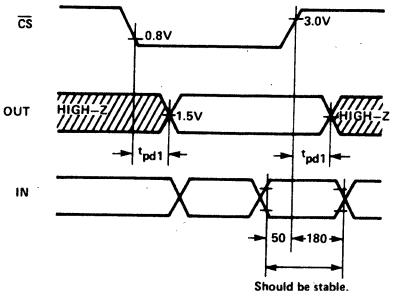
TIMING WAVEFORMS

MODE SELECT



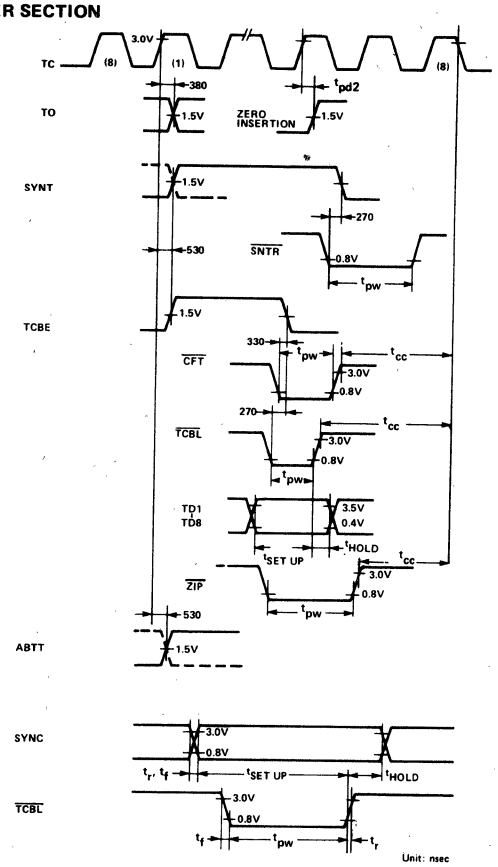
MODE	MS_1	MS_2	MRL
Closed	0	0 or 1	
Basic Sync	1	1	
SDLC	1	1	

CHIP SELECT



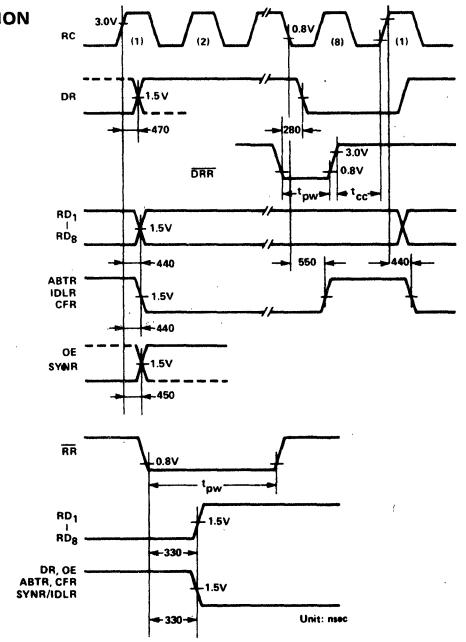
Unit:nsec

TRANSMITTER SECTION



Unit: nsec

RECEIVER SECTION



TIMING WAVEFORMS (CONT.)

DC CHARACTERISTICS

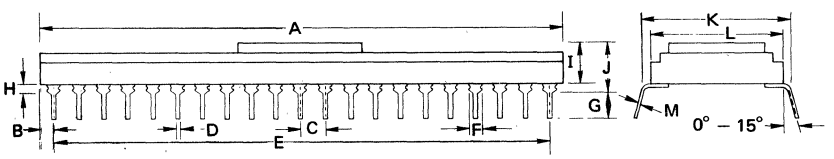
$T_a = 0^oC$ to $+70^oC$, $V_{DD} = 12V + 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	3.0		V_{DD}	V	With Built-in
Input Low Voltage	V_{IL}			0.8	V	pull-up resistors
Output Leakage Current	I_{OL}	−20		20	μA	V_o = 0.4 to 3.5V (CS)= 3.5V
Output High Voltage	V_{OH}	3.5			V	I_{OH} = −100μA
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 1.6mA
Input Low Current	I_{IL}			−1.4	mA	V_{IL} = 0.4V
V_{DD} Supply Current	I_{DD}		15	20	mA	
V_{CC} Supply Current	I_{CC}		40	65	mA	
V_{BB} Supply Current	I_{BB}		−0.2	−2.0	mA	
Fan-out	N			1		Standard TTL Load

CAPACITANCE

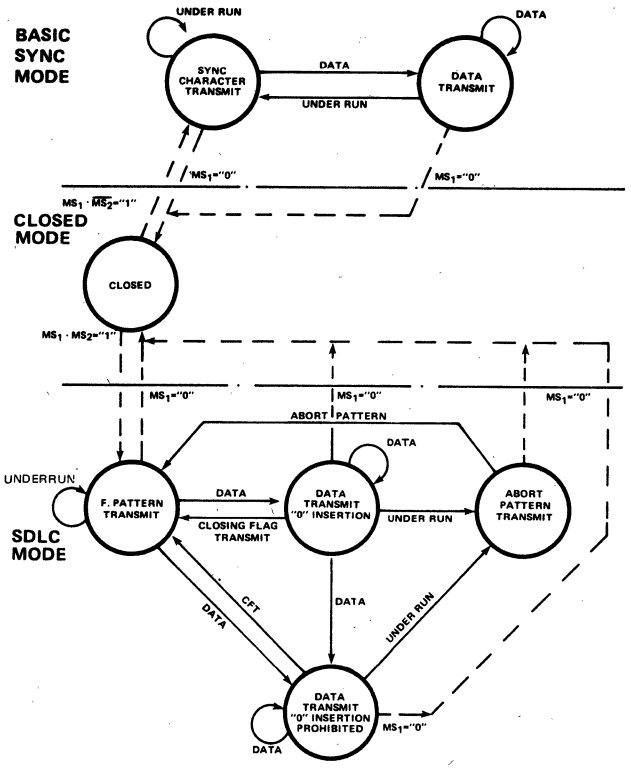
Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			20	pf	f = 1 MHz
Output Capacitance	C_{OUT}			20	pf	f = 1 MHz

PACKAGE OUTLINE μPD379D

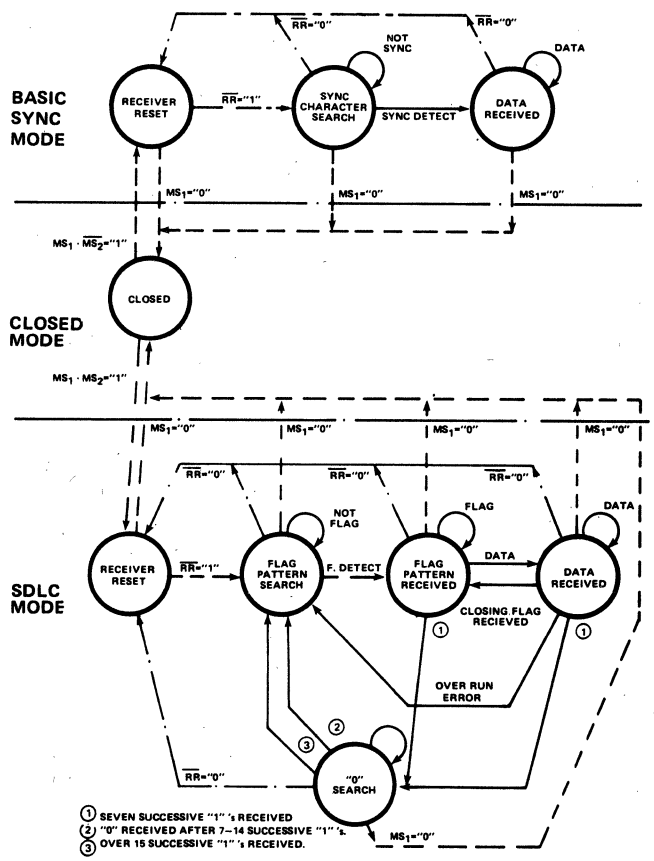


ITEM	MILLIMETERS	INCHES
A	53.5 MAX	2.1 MAX
B	1.35	0.05
C	2.54	0.10
D	50.80	2.0
F	1.27	0.05
G	2.54 MAX	0.10 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.21 MAX
K	15.24	0.60
L	13.50	0.53
M	0.3	0.012

TRANSMITTER STATE DIAGRAM



RECEIVER STATE DIAGRAM



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PRINTER CONTROLLER

DESCRIPTION

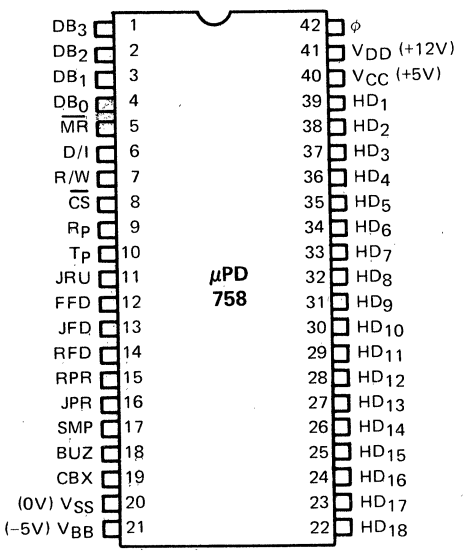
The μPD758 is a digital LSI device designed to control SEIKO 101 Series drum-type impact printers. It can be used with either single or double printer systems. The μPD758, ideally suited for low-cost Electronic Cash Register (ECR) systems, frees the processor from direct control of the printer and simplifies the peripheral circuitry.

Using a few of the possible 18 instructions, the controlling processor need only load the μPD758 with the characters to be printed, and issue the appropriate print instruction. The μPD758 then assumes control of the printer, keeping track of the printer drum position and generating hammer drive signals at the approproate time. The μPD758 also has separate output drives that are under software control. These are typically used to drive the STAMP input to the printer and to provide discrete drives for BUZZER and CASH BOX functions of the ECR system.

FEATURES

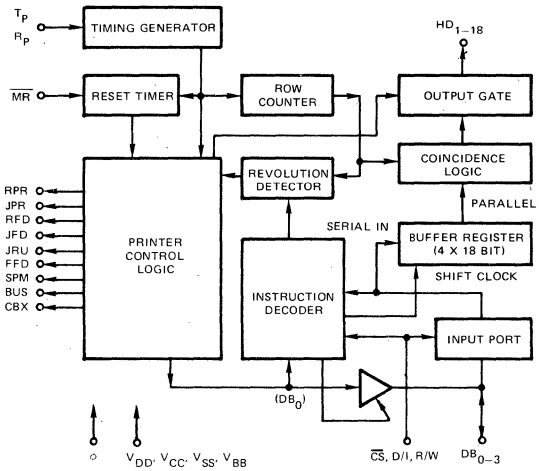
- Usable with SEIKO 101 Series Printers (CR101T[d], EP101S) and equivalents
- ECR Printer and Line Feed Control Capability
- 18 Powerful Instructions
- Controls up to 18 columns
- Controls up to 16 characters
- Input/Output TTL Compatible
- N-Ch MOS
- 42 Pin Plastic DIP
- Power Supplies, +12V, +5V and -5V

PIN CONFIGURATION



μPD758

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Input and Output Voltages	−1 to +7 Volts ①
Clock Voltage	−1 to +7 Volts ①
Supply Voltage V_{DD}	−1 to +15 Volts
Supply Voltage V_{CC}	−1 to +7 Volts
Supply Voltage V_{BB}	−2 to −8 Volts

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{SS} = 0V, V_{BB} = −5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+3.0		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Output High Voltage	V_{OH}	+3.5			V	I_{OH} = −1.0 mA
Output Low Voltage	V_{OL}			+0.5	V	I_{OL} = +1.7 mA
High Level Clock Voltage	$V_{\phi H}$	+3.0		V_{CC}	V	
Low Level Clock Voltage	$V_{\phi L}$	−0.5		+0.8	V	
High Level Input Leakage Current	I_{LIH}			+10	μA	V_I = +3.0V
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_I = +0.8V
High Level Output Leakage Current	I_{LOH}			+10	μA	V_O = +3.5V
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_O = +0.5V
Supply Current	I_{BB}			−300	μA	V_{BB} = −5.25V
Supply Current	I_{DD}		17		mA	
Supply Current	I_{CC}		27		mA	

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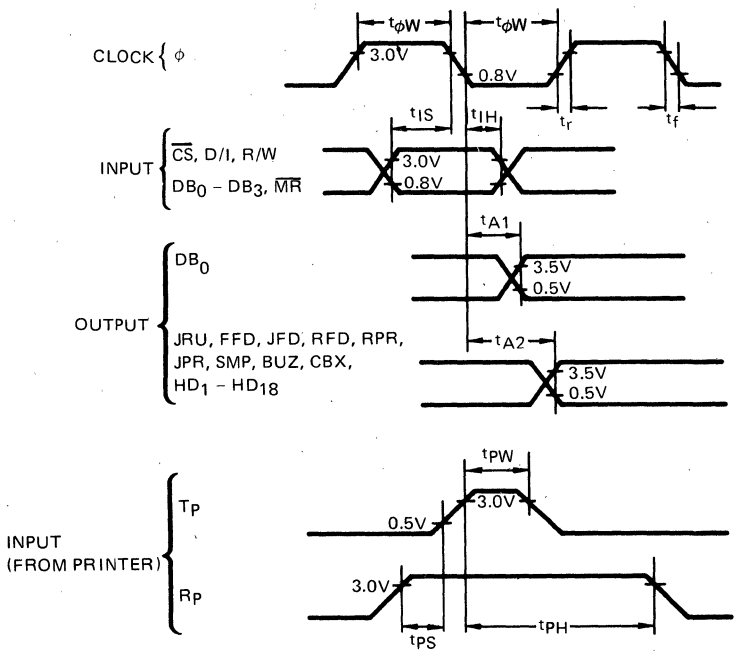
CAPACITANCE

T_a = −10 to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{SS} = 0V, V_{BB} = −5V ± 5%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			10	pF	f = 1 MHz
Output Capacitance	C_{OUT}			10	pF	f = 1 MHz

TIMING WAVEFORMS



AC CHARACTERISTICS

T_a = −10 to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{SS} = 0V, V_{BB} = −5V ± 5%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Clock Rise and Fall Time	t_r, t_f			50	ns	
Clock Pulse Width	$t_{\phi W}$	0.45		2.0	μs	
Output Delay Time	t_{A1}			430	ns	$1T^2L$ & C_L = 100 pF
	t_{A2}			700	ns	$1T^2L$ & C_L = 100 pF
Input Setup Time	t_{IS}	400			ns	
Input Hold Time	t_{IH}	40			ns	
Pulse Width for TP Input	t_{PW}	2			clock period	
RP Input Setup Time	t_{PS}	0			clock period	
RP Input Hold Time	t_{PH}	3			clock period	

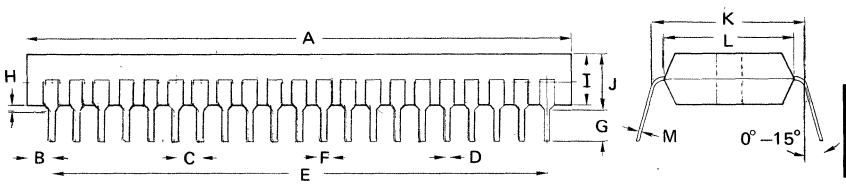
INSTRUCTION TABLE

INST. NO.	OPERATION	BUSY	D/I	R/W	DB			
					3	2	1	0
1	CHECK DB0 FOR BUSY FLAG STATUS	BF①	X②	0	X	X	X	BF
2	STORE DATA (dddd) INTO BUFFER REGISTER	0	0	1	d③	d	d	d
3a	NO OPERATION	1	0	1	X	X	X	X
3b		1	1	1	0	X	X	X
3c		1	1	1	1	1	X	X
3d		0	1	1	0	0	0	0
4	PRINT BUFFER REGISTER CONTENTS TO JOURNAL	0	1	1	0	0	0	1
5	PRINT BUFFER REGISTER CONTENTS TO RECEIPT	0	1	1	0	0	1	0
6	PRINT BUFFER REGISTER CONTENTS TO JOURNAL AND RECEIPT	0	1	1	0	0	1	1
7	FAST FEED AND STAMP RECEIPT	0	1	1	0	1	0	0
8	PRINT STORED DATA ONTO JOURNAL AND FEED ONE LINE	0	1	1	0	1	0	1
9	PRINT STORED DATA ONTO RECEIPT AND FEED ONE LINE	0	1	1	0	1	1	0
10	PRINT STORED DATA ONTO RECEIPT AND JOURNAL AND FEED BOTH ONE LINE	0	1	1	0	1	1	1
11	DRIVE CASH BOX OUTPUT	X	1	1	1	0	0	0
12	DRIVE BUZZER OUTPUT FOR FOUR CHARACTER PERIODS	X	1	1	1	0	0	1
13	RESET BUZZER OUTPUT	X	1	1	1	0	1	0
14	DRIVE BUZZER OUTPUT UNTIL RESET	X	1	1	1	0	1	1
15	DRIVE STAMP OUTPUT	0	1	1	1	1	0	0
16	FEED JOURNAL ONE LINE	0	1	1	1	1	0	1
17	FEED RECEIPT ONE LINE	0	1	1	1	1	1	0
18	FEED BOTH RECEIPT AND JOURNAL ONE LINE	0	1	1	1	1	1	1

Notes: ① BF = Busy Flag
② X = Don't Care
③ d = Data

PACKAGE OUTLINE

μPD758C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

PRINTER CONTROLLER

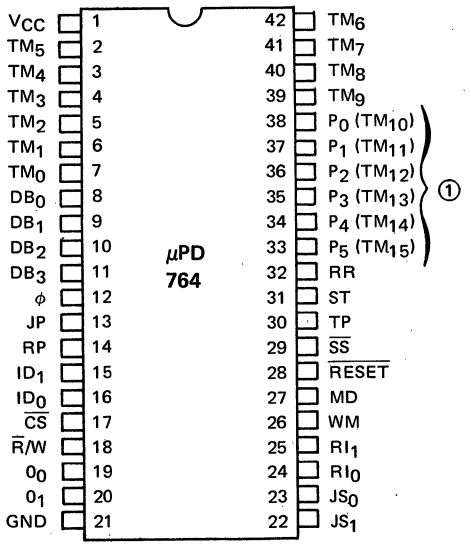
DESCRIPTION

The μPD764 is a digital LSI device designed to control SEIKO CR-330 or M-310 rolling contact printers. The μPD764, which is ideally suited for low-cost Electronic Cash Register (ECR) systems, frees the processor from direct control of the printer and simplifies the peripheral circuitry.

The processor need only load the μPD764 with the characters to be printed and issue the appropriate print command. The μPD764 then assumes control of the printer – positioning the print wheels, initiating the rolling contact print process, feeding paper and feeding ribbon automatically without further processor intervention.

FEATURES

- Compatible with SEIKO CR-330 and M-310 Printers.
- Simple Interface to 4-Bit, 8-Bit and 16-Bit Microprocessors.
- 23 Powerful Instructions.
- 4-Bit Data Bus for Print Data and Instruction Inputs.
- 16 Digit Data Buffer.
- 16 Trigger Magnet Drive Outputs for the M-310 and 10 for the CR-330.
- Single Phase Clock Input. 300, 400 or 500 kHz Selectable.
- Input/Output and Clock TTL Compatible.
- N-Channel MOS.
- Single +5V Power Supply.



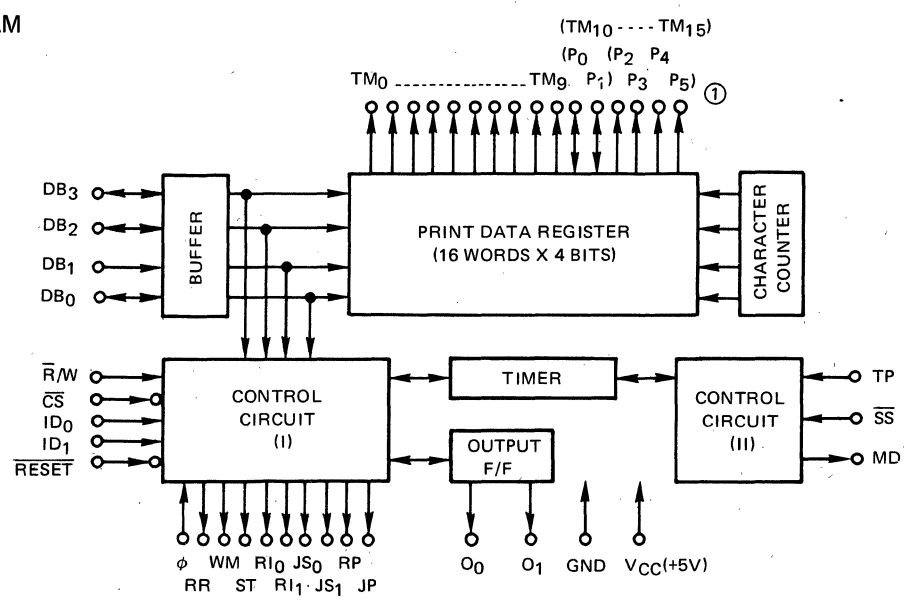
Note: ① $P_0 - P_{15}$ for CR-330 Printer
$TM_{10} - TM_{15}$ for M-310 Printer

μPD764

PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	INPUT/ OUTPUT	FUNCTION
7 – 2 42 – 39	$TM_0 - TM_9$	O	Trigger Magnet Drive
8, 10, 11 9	DB_0, DB_2, DB_3 DB_1	I/O I	Data Bus
12	ϕ	I	Single Phase Clock (TTL Level)
13	JP	O	Journal Print Drive
14	RP	O	Receipt Print Drive
16, 15	$ID_0 - ID_1$	I	Instruction/Data Selector
17	$\overline{CS}$	I	Chip Select (Active Low)
18	$\overline{R}/W$	I	Read/Write Control – "0" = Read, "1" = Write
19, 20	O_0, O_1	O	Output F/F
23	JS_0	O	Journal Stop Plunger Drive
22	JS_1	O	Journal Stop Plunger Hold Current Control
24	RI_0	O	Receipt Issue Plunger Drive
25	RI_1	O	Receipt Issue Plunger Hold Current Control
26	WM	O	Journal Wind Motor Drive
27	MD	O	Motor Drive
28	$\overline{RESET}$	1	Reset Input (Active Low) O_0, O_1: Reset to "0". ϕ: Set to 300 kHz Mode $DB_0 - DB_3$: Set to Hi-Z State Instruction Register: cleared Busy Flag: cleared Character Counter: Set to F in Hexidecimal $P_0 - P_1$: Set as Input Port $P_2 - P_5$: Set as Output Port (Output all "0")
29	$\overline{SS}$	I	Stop Signal from Printer
30	TP	I	Timing Pulse from Printer
31	ST	O	Stamp Plunger Drive
32	RR	O	Red Ribbon Select Control
36 – 33	$P_2 - P_5$ or $TM_{12} - TM_{15}$	O O	4-Bit Parallel Output Port when reset or specified with an instruction. Trigger Magnet Drive (for M-310 Printer) when specified with an instruction.
38, 37	$P_0 - P_1$ or $TM_{10} - TM_{11}$	I O	2-Bit Parallel Input Port when reset or specified with an instruction. Trigger Magnet Drive (for M-310 Printer) when specified with an instruction.

BLOCK DIAGRAM



Note: ① $P_0 - P_{15}$ for CR-330 Printer
$TM_{10} - TM_{15}$ for M-310 Printer

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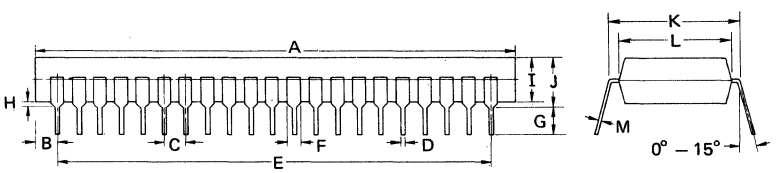
INSTRUCTION SET

NO.	MNEMONIC	FUNCTION	DB				ID	
			3	2	1	0	1	0
1	RS	Receipt – Stamp	0	0	0	1	1	1
2	RFF	Receipt – Fast Feed	0	0	1	0	1	1
3	RFPS	Receipt – Fast Feed, Print and Stamp	0	0	1	1	1	1
4	JPF	Journal – Print and Paper Feed	0	1	0	0	1	1
5	JP	Journal – Print	0	1	0	1	1	1
6	JF	Journal – Feed	0	1	1	0	1	1
7	RPF	Receipt – Print and Feed	1	0	0	0	1	1
8	RP	Receipt – Print	1	0	0	1	1	1
9	RF	Receipt – Feed	1	0	1	0	1	1
10	JRPF	Journal and Receipt – Print and Feed	1	1	0	0	1	1
11	JRP	Journal and Receipt – Print	1	1	0	1	1	1
12	JRF	Journal and Receipt – Feed	1	1	1	0	1	1
13	RR	Set Red Ribbon	0	0	0	1	0	1
14	RTM	Set $P_0 - P_1$ as Input Port and $P_2 - P_5$ as Output Port	0	0	1	0	0	1
15	STM	Set $P_0 - P_5$ as $TM_{10} - TM_{15}$	0	0	1	1	0	1
16	SFM	Set to ϕ = 400 kHz Operation Mode	0	1	0	0	0	1
17	SFH	Set to ϕ = 500 kHz Operation Mode	0	1	0	1	0	1
18	RSO	Reset Output F/F 0 (O_0)	0	1	1	0	0	1
19	STO	Set Output F/F 0 (O_0)	0	1	1	1	0	1
20	RS1	Reset Output F/F 1 (O_1)	1	0	1	0	0	1
21	ST1	Set Output F/F 1 (O_1)	1	0	1	1	0	1
22	RSB	Reset Output F/Fs 0 and 1 (O_0 and O_1)	1	1	1	0	0	1
23	STB	Set Output F/Fs 0 and 1 (O_0 and O_1)	1	1	1	1	0	1

PACKAGE OUTLINE
μPD764C



ITEM	MILLIMETERS	INCHES
A	56.0 MAX	2.2 MAX
B	2.6 MAX	0.1 MAX
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	50.8	2.0
F	1.5	0.059
G	3.2 MIN	0.126 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.20 MAX
J	5.72 MAX	0.22 MAX
K	15.24	0.6
L	13.2	0.52
M	0.3 ± 0.1	0.01 ± 0.004

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
All Inputs and Outputs	−0.5 to +7 Volts
V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 to +70°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2.2			V	
Input Low Voltage	V_{IL}			+0.6	V	
Output High Voltage	V_{OH}	V_{CC} −2.45			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL1}			0.4	V	I_{OL} = +1.1 mA
	V_{OL2}			0.6	V	I_{OL} = +1.7 mA
High Level Input Leakage Current	I_{LIH}			+10	μA	V_I = +2.2V
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_I = +0.6V
High Level Output Leakage Current	I_{LOH}			+10	μA	$V_O = V_{CC}$ −2.45V
Low Level Output Leakage Current	I_{LOL}			−10	μA	V_O = +0.4V
Supply Current	I_{CC}		45		mA	

AC CHARACTERISTICS

T_a = −10 to +70°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Cycle Time	t_{CY}	2		5	μs	
Clock Rise and Fall Time	t_r, t_f			70	ns	
Clock Pulse Width	$t_{\phi W}$	0.45			μs	
Output Delay Time	t_{A1}			430	ns	
	t_{A2}			800	ns	$1T^2$ L & C_L = 100 pF
	t_{A3}			2.0	μs	
Input Setup Time	t_{IS_1}	400			ns	
	t_{IS_2}	400			ns	
Input Hold Time	t_{IH_1}	40			ns	
	t_{IH_2}	100			ns	
Pulse Width for Tp Input	t_{TP}	5			t_{CY}	
$\overline{SS}$ Input Pulse Width	t_{SS}	5			t_{CY}	
$\overline{RESET}$ Input Pulse Width	t_{RES}	5			t_{CY}	

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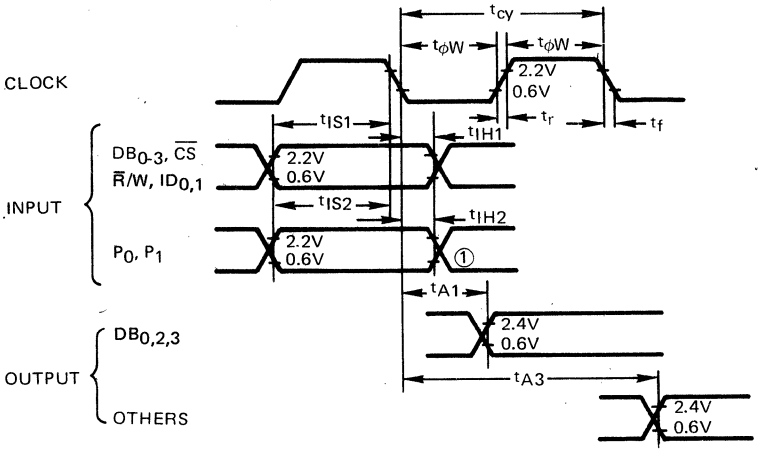
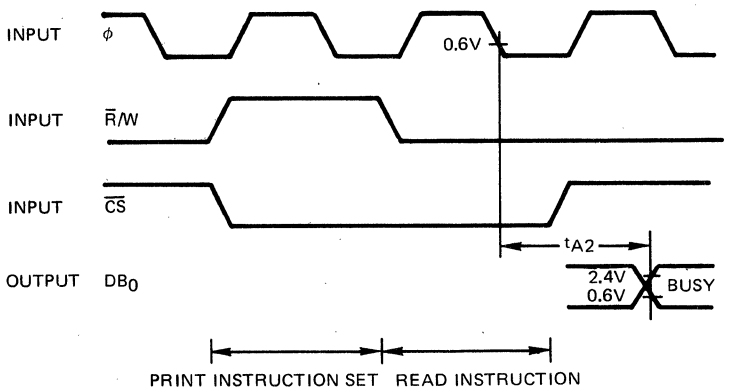
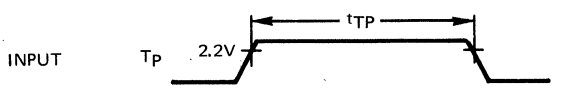
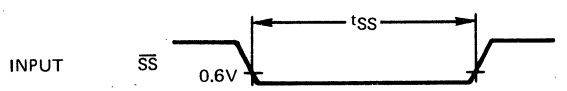
TIMING WAVEFORMS

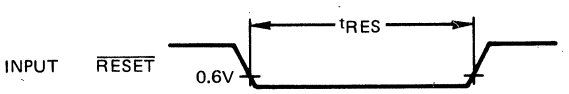


Note: ① If a Read instruction is performed just following an instruction that sets Busy Flag, the output delay of DB_0 (Busy) is t_{A2} as follows.









EIGHT-BIT INPUT/OUTPUT PORT

DESCRIPTION

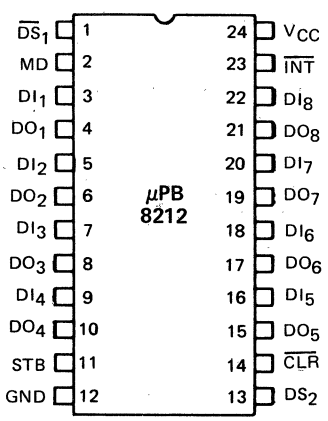
The μPB8212 input/output port consists of an 8-bit latch with three-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the control and generation of interrupts to the microprocessor.

The device is multimode in nature and can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

FEATURES

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current – 0.25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080A Processor
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in 24-pin Plastic and Cerdip Packages

PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_8$	Data In
$DO_1 - DO_8$	Data Out
$\overline{DS}_1$, DS_2	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt (Active Low)
$\overline{CLR}$	Clear (Active Low)

8

Rev/1

Data Latch

The 8 flip-flops that compose the data latch are of a "D" type design. The output (Q) of the flip-flop follows the data input (D) while the clock input (C) is high. Latching occurs when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$).
(Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The output of the data latch (Q) are connected to three-state, non-inverting output buffers. These buffers have a common control line (EN); enabling the buffer to transmit the data from the outputs of the data latch (Q) or disabling the buffer, forcing the output into a high impedance state (three-state).

This high-impedance state allows the designer to connect the μPB8212 directly to the microprocessor bi-directional data bus.

Control Logic

The μPB8212 has four control inputs: $\overline{DS}_1$, DS_2, MD and STB. These inputs are employed to control device selection, data latching, output buffer state and the service request flip-flop.

$\overline{DS}_1$, DS_2 (Device Select)

These two inputs are employed for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

Service Request Flip-Flop (SR)

The (SR) flip-flop is employed to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output (Q) of the (SR) flip-flop is connected to an inverting input of a "NOR" gate. The other input of the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

MD (Mode)

This input is employed to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is in the output mode (high) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

When MD is in the input mode (low) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

STB is employed as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop triggers on the negative edge of STB which overrides $\overline{CLR}$.

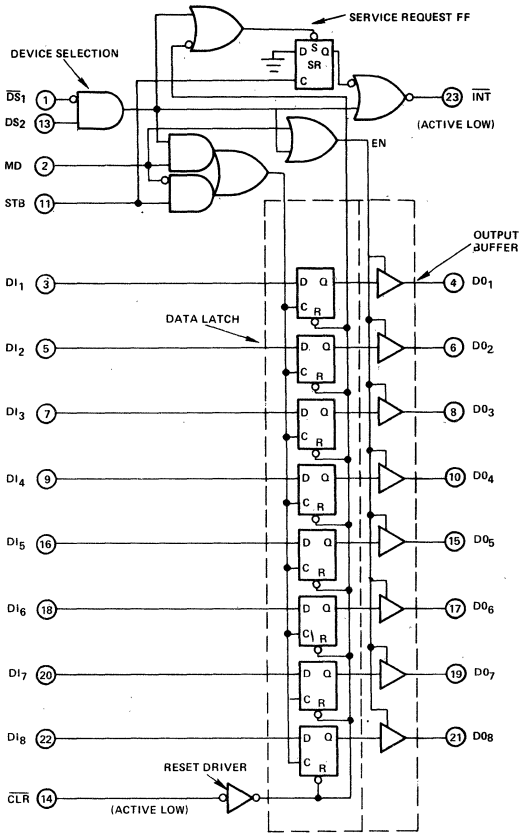
ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

BLOCK DIAGRAM



STB	MD	$(\overline{DS_1} \cdot DS_2)$	DATA OUT EQUALS
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

$\overline{CLR}$	$(\overline{DS_1} \cdot DS_2)$	STB	SR ②	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	0	0	③	③
1	↘	0	1	1
1	0	↘	0	0
1	1	0	1	0
1	1	↘	0	0

Notes: ① $\overline{CLR}$ resets data latch sets SR flip-flop. (No effect on output buffer)
② Internal SR flip-flop
③ Previous data remains

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$

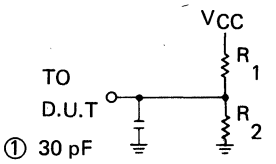
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current ACK, DS_2, CR, $DI_1 - DI_8$ Inputs	I_F		−0.14	−0.25	mA	$V_F = 0.45V$
Input Load Current MD Input	I_F		−0.25	−0.75	mA	$V_F = 0.45V$
Input Load Current $\overline{DS_1}$ Input	I_F		−0.26	−1.0	mA	$V_F = 0.45V$
Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs	I_R			10	μA	$V_R = 5.25V$
Input Leakage Current MD Input	I_R			30	μA	$V_R = 5.25V$
Input Leakage Current $\overline{DS_1}$ Input	I_R			40	μA	$V_R = 5.25V$
Input Forward Voltage Clamp	V_C		−0.85	−1.3	V	$I_C = -5$ mA
Input "Low" Voltage	V_{IL}			0.85	V	
Input "High" Voltage	V_{IH}	2.0			V	
Output "Low" Voltage	V_{OL}		0.26	0.45	V	$I_{OL} = 15$ mA
Output "High" Voltage	V_{OH}	3.65	4.0		V	$I_{OH} = -1$ mA
Short Circuit Output Current	I_{SC}	−15	−38	−75	mA	$V_O = 0V$
Output Leakage Current High Impedance State	I_O			20	μA	$V_O = 0.45V/5.25V$
Power Supply Current	I_{CC}		103	130	mA	

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Pulse Width	t_{pw}	30			ns	Input Pulse Amplitude = 2.5V
Data To Output Delay	t_{pd}		20	30	ns	
Write Enable To Output Delay	t_{we}			40	ns	Input Rise and Fall Times = 5 ns
Data Setup Time	t_{set}	15			ns	
Data Hold Time	t_h	20			ns	Between 1V and 2V
Reset to Output Delay	t_r			40	ns	Measurement made at 1.5V with 15 mA and 30 pF Test Load
Set To Output Delay	t_s			30	ns	
Output Enable/Disable Time	t_e/t_d			45	ns	①
Clear To Output Delay	t_c			55	ns	②

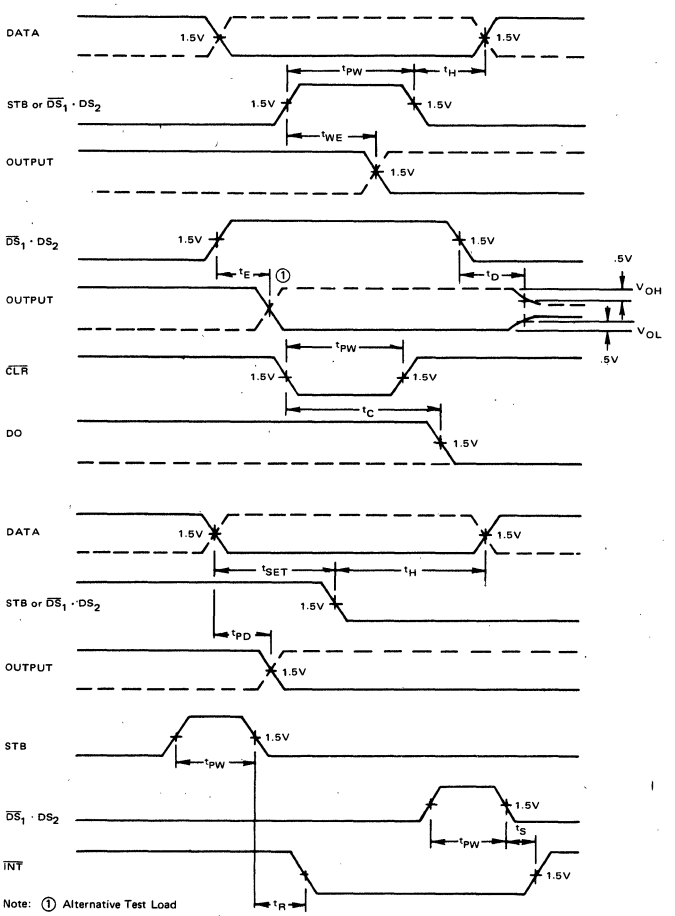
Notes: ① R_1 = 300Ω/10KΩ; R_2 = 600Ω/1KΩ
② R_1 = 300Ω; R_2 = 600Ω



TEST CIRCUIT

Note: ① Including Jig and Probe Capacitance

TIMING WAVEFORMS



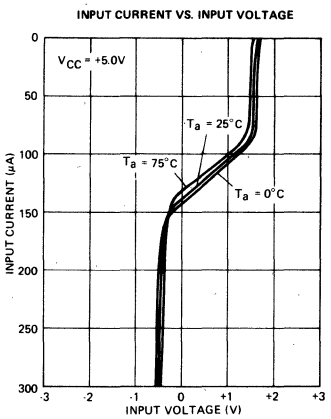
CAPACITANCE ①

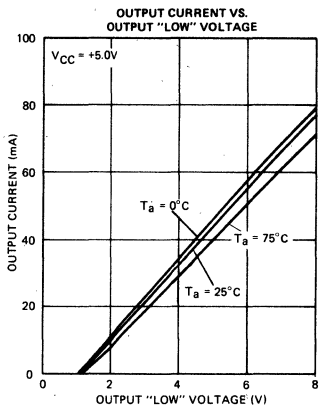
T_a = 25°C; V_{CC} = +5V; V_{BIAS} = 2.5V; f = 1 MHz

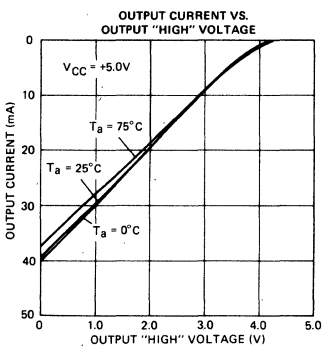
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		7	12	pF	$\overline{DS_1}$, MD
Input Capacitance	C_{IN}		4	9	pF	DS_2, CLR, STB, $DI_1 - DI_8$
Output Capacitance	C_{OUT}		6	12	pF	$DO_1 - DO_8$

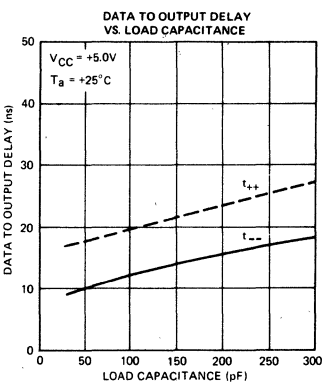
Note: ① This parameter is periodically sampled and not 100% tested

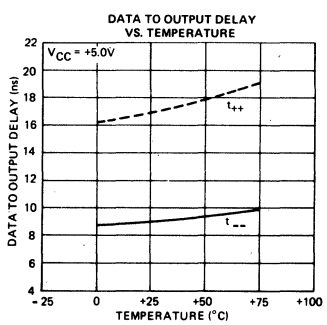
TYPICAL CHARACTERISTICS

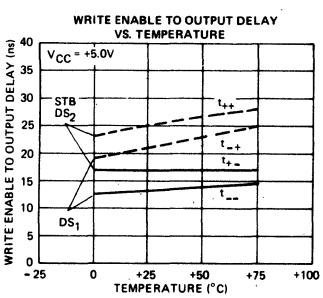












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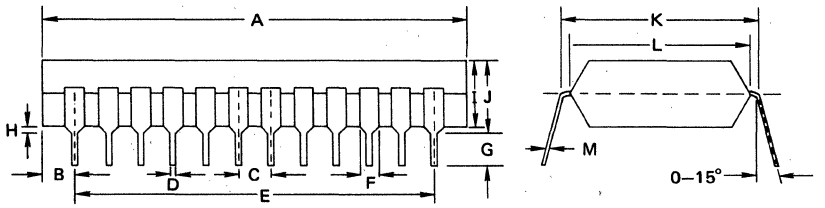
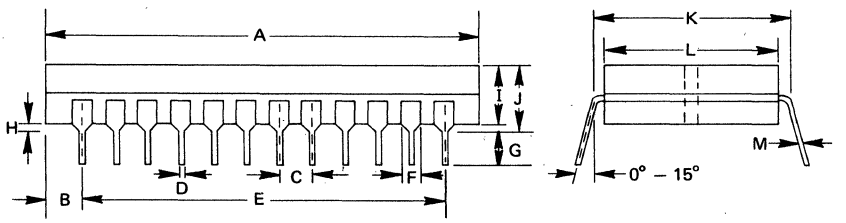
PACKAGE OUTLINE
μPB8212C/D



μPB8212C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPB8212D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER

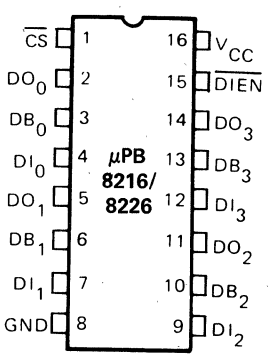
DESCRIPTION

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V (V_{OH}), and for high capacitance terminated bus structures, the DB outputs provide a high 55 mA (I_{OL}) capability.

FEATURES

- Data Bus Buffer Driver for μCOM-8 Microprocessor Family
- Low Input Load Current – 0.25 mA Maximum
- High Output Drive Capability for Driving System Data Bus
- 3.65V Output High Voltage for Direct Interface to μCOM-8 Microprocessor Family
- Three State Outputs
- Reduces System Package Count
- Available in 16 pin packages: Cerdip and Plastic

PIN CONFIGURATION



PIN NAMES

DB_0 DB_3	Data Bus Bi Directional
DI_0 DI_3	Data Input
$DO_0 - DO_3$	Data Output
$\overline{DIEN}$	Data in Enable Direction Control
$\overline{CS}$	Chip Select

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Rev/2

FUNCTIONAL DESCRIPTION

Microprocessors like the 8080A are MOS devices and are generally capable of driving a single TTL load. This also applies to MOS memory devices. This type of drive is sufficient for small systems with a few components, but often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The μPD8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

Each buffered line of the four bit driver consists of two separate buffers. They are three state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this is used to interface to the system side components such as memories, I/O, etc. Its interface is directly TTL compatible and it has high drive (55 mA). For maximum flexibility on the other side of the driver the inputs and outputs are separate. They can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080A Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080A processor is achieved with an adequate amount of noise immunity (650 mV worst case).

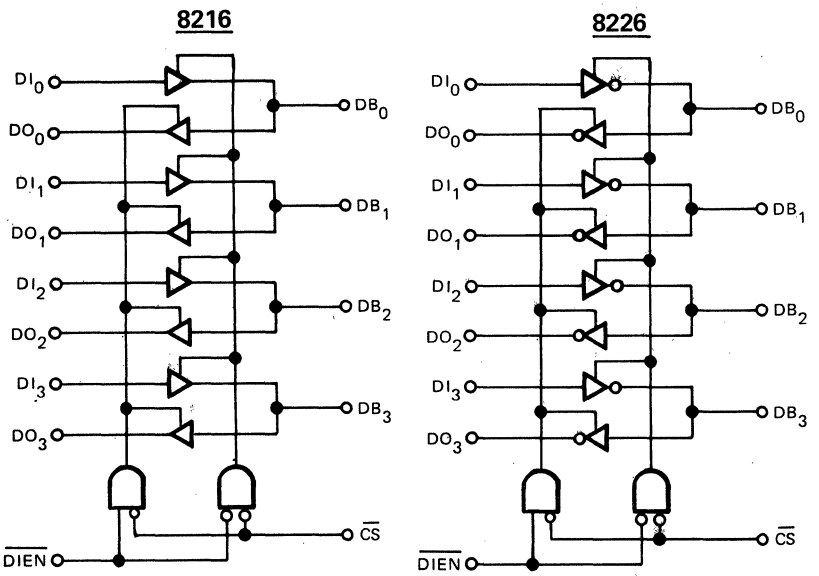
Control Gating $\overline{CS}$, $\overline{DIEN}$

The $\overline{CS}$ input is used for device selection. When $\overline{CS}$ is "high" the output drivers are all forced to their high-impedance state. When it is "low" the device is selected (enabled) and the data flow direction is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the data flow direction (see Block Diagrams for complete truth table). This directional control is accomplished by forcing one of the pair of buffers to its high impedance state. This allows the other to transmit its data. This is accomplished by a simple two gate circuit.

The μPB8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.

BLOCK DIAGRAMS



$\overline{DIEN}$	$\overline{CS}$	RESULT
0	0	DI → DB
1	0	DB → DO
0	1	High Impedance
1	1	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature (Cerdip) . . . . . −65°C to +150°C
(Plastic) . . . . . −65°C to +125°C
All Output and Supply Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −1.3 to +5.5 Volts
Output Currents . . . . . 125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V±5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current $\overline{DIEN}$, $\overline{CS}$		I_{F1}			−0.5	mA	V_F = 0.45
Input Load Current All Other Inputs		I_{F2}			−0.25*	mA	V_F = 0.45
Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		I_{R1}			20	μA	V_R = 5.25V
Input Leakage Current DI Inputs		I_{R2}			10	μA	V_R = 5.25V
Input Forward Voltage Clamp		V_C			−1.3	V	I_C = −5 mA
Input "Low" Voltage		V_{IL}			0.95	V	
Input "High" Voltage		V_{IH}	2.0			V	
Output Leakage Current (3-State)	DO	I_O			20	μA	V_O = 0.45/5.25V
	DB	I_O			100		
Power Supply Current	8216	I_{CC}			130	mA	
	8226	I_{CC}			120	mA	
Output "Low" Voltage		V_{OL1}			0.45	V	DO Outputs I_{OL} = 15 mA DB Outputs I_{OL} = 25 mA
Output "Low" Voltage	8216	V_{OL2}			0.6	V	DB Outputs I_{OL} = 55 mA
	8226	V_{OL2}			0.6	V	DB Outputs I_{OH} = 50 mA
Output "High" Voltage		V_{OH1}	3.65			V	DO Outputs I_{OH} = −1 mA
Output "High" Voltage		V_{OH2}	2.4			V	DB Outputs I_{OH} = −10 mA
Output Short Circuit Current		I_{OS}	−15 −30		−65 −120	mA mA	DO Outputs V_O = 0V DB Outputs V_{CC} = 5.0V

Note: ① Typical values are for T_a = 25°C, V_{CC} = 5.0V.

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	V_{BIAS} = 2.5V V_{CC} = 5V T_a = 25°C f = 1 MHz
Output Capacitance	C_{OUT1}			10 ②	pF	
Output Capacitance	C_{OUT2}			18 ③	pF	

Notes: ① This parameter is periodically sampled and not 100% tested.
② DO Output.
③ DB Output.

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AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V±5%

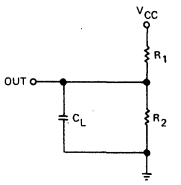
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input to Output Delay DO Outputs		t_{PD1}			25	ns	C_L = 30 pF, R_1 = 300Ω, R_2 = 600Ω ④
Input to Output Delay	8216	t_{PD2}			30	ns	C_L = 300 pF, R_1 = 90Ω,
DB Outputs	8226	t_{PD2}			25	ns	R_2 = 180Ω 4
Output Enable Time	8216	t_E			65	ns	② ④
	8226	t_E			54	ns	
Output Disable Time		t_D			35	ns	③ ④

Notes: ① Typical values are for T_a = 25°C, V_{CC} = 5.0V

② DO Outputs, C_L = 30 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 300 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

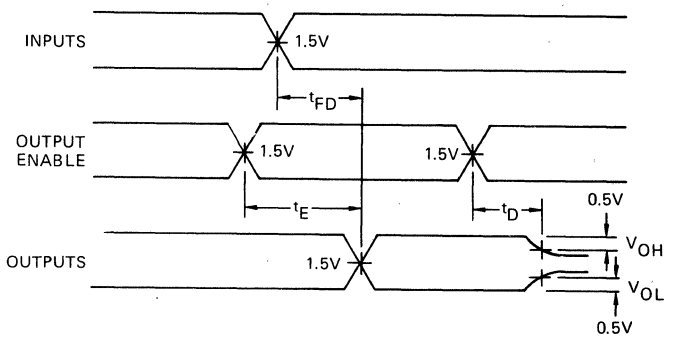
③ DO Outputs, C_L = 5 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 5 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

④ Input pulse amplitude: 2.5V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

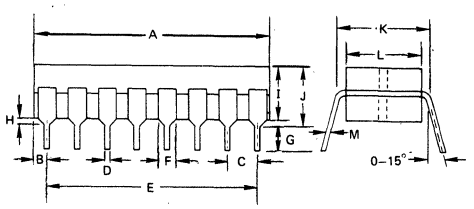


TEST CIRCUIT

TIMING WAVEFORMS

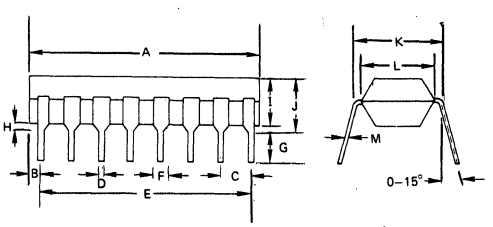


PACKAGE OUTLINE μPB8216C/D μPB8226C/D



μPB8216/8226D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	$0.0098^{+0.0039}_{0.0019}$



μPB8216/8226C (Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX	0.76 MAX
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	0.01

PROGRAMMABLE COMMUNICATION INTERFACE

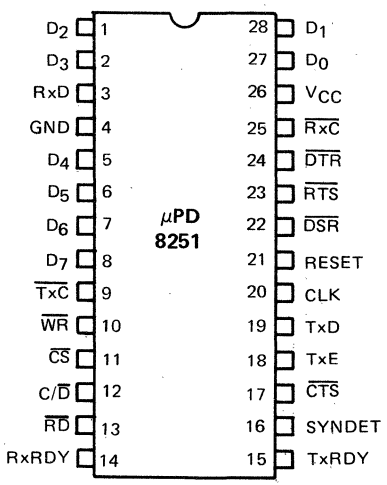
DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) is designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the μPD8080 or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART STATUS including data format errors and control signals such as TxE and SYNDET is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate – Synchronous – DC to 56K Baud
  – Asynchronous – DC to 9.6K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply
- Separate Device, Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
V_{CC}	+5 Volt Supply
GND	Ground

8

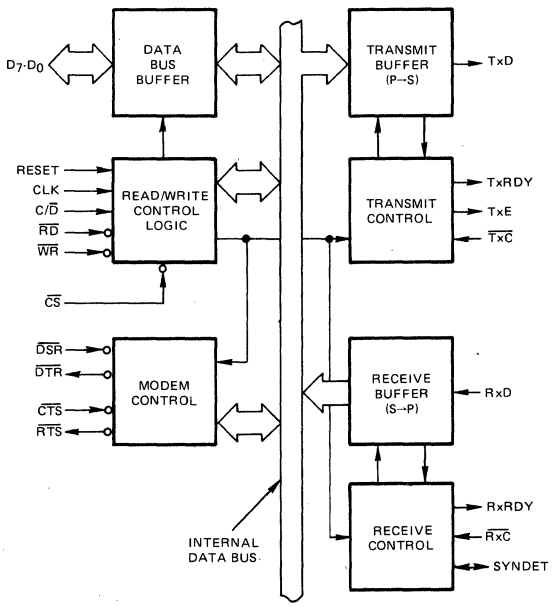
Rev/1

FUNCTIONAL DESCRIPTION

The μPD8251 Universal Synchronous/Asynchronous Receiver/Transmitter is designed specifically for 8080 microcomputer systems but works with most 8-bit processors. Operation of the 8251, like other I/O devices in the 8080 family, is programmed by system software for maximum flexibility.

In the receive mode, a communication interface device must convert incoming serial format data into parallel data and make certain format checks on the data. And in the transmit mode, the device must format data into serial data. The device must also supply or remove characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

BLOCK DIAGRAM



BASIC OPERATION

C/D	RD	WR	CS	
0	0	1	0	8251 → Data Bus
0	1	0	0	Data Bus → 8251
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltages	-0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

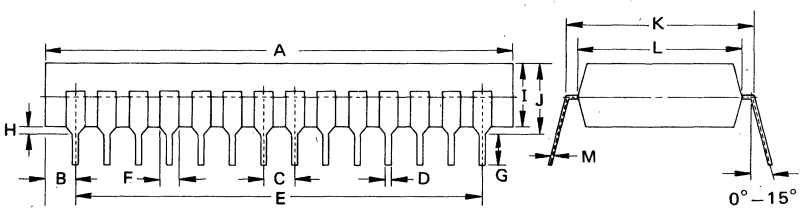
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	GND –.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = –100 μA
Data Bus Leakage	I_{DL}			–50	μA	V_{OUT} = 0.45V
				10		V_{OUT} = V_{CC}
Input Load Current	I_{IL}			10	μA	@5.5V
Power Supply Current	I_{CC}		45	80	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE μPD8251C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

AC CHARACTERISTICS

BUS PARAMETERS: ①

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable before $\overline{READ}$, ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	50			ns	
Address Hold Time for $\overline{READ}$, ($\overline{CS}$, $\overline{CD}$)	t_{RA}	5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	430			ns	
Data Delay from $\overline{READ}$	t_{RD}			350	ns	C_L = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}	25		200	ns	C_L = 100 pF C_L = 15 pF
Recovery Time Between WRITES ②	t_{RV}	6			t_{CY}	
WRITE						
Address Stable before $\overline{WRITE}$	t_{AW}	20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Set-Up Time for $\overline{WRITE}$	t_{DW}	200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			ns	
OTHER TIMING						
Clock Period ③	t_{CY}	.420		1.35	μs	
Clock Pulse Width	$t_{\Phi W}$	220		0.7t_{CY}	ns	
Clock Rise and Fall Time	t_R, t_F	0		50	ns	
TxD Delay from Falling Edge of $\overline{TxC}$	t_{DTx}			1	μs	C_L = 100 pF
Rx Data Set-Up Time to Sampling Pulse	t_{SRx}	2			μs	C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2			μs	C_L = 100 pF
Transmitter Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate	f_{Tx}	DC DC		56 520	KHz KHz	
Transmitter Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{TPW}	12 1			t_{CY} t_{CY}	
Transmitter Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{TPD}	15 3			t_{CY} t_{CY}	
Receiver Input Clock Frequency 1X Baud Rate 16X and 64X Baud Rate	f_{Rx}	DC DC		56 520	KHz KHz	
Receiver Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{RPW}	12 1			t_{CY} t_{CY}	
Receiver Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{RPD}	15 3			t_{CY} t_{CY}	
TxRDY Delay from Center of Data Bit	t_{Tx}			16	t_{CY}	C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{Rx}			20	t_{CY}	
Internal Syndet Delay from Center of Data Bit	t_{IS}			25	t_{CY}	
External Syndet Set-Up Time before Falling Edge of $\overline{RxC}$	t_{ES}	16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}			16	t_{CY}	C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}				t_{CY}	
Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	16			t_{CY}	

Notes:
① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.
② This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.
③ The TxC and RxC frequencies have the following limitations with respect to CLK.
For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
For 16X and 64X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(4.5\ t_{CY})$
④ Reset Pulse Width = 6 t_{CY} minimum.

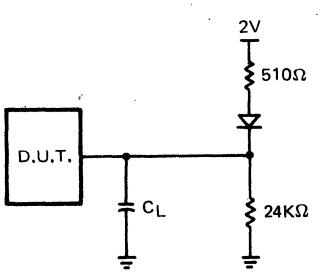
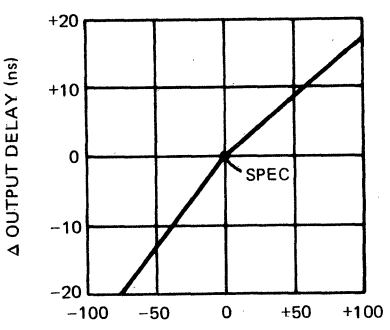


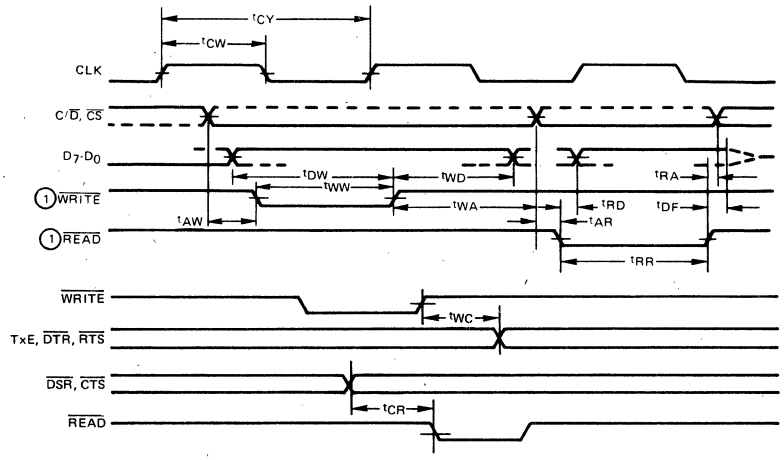
Figure 1.

TEST LOAD CIRCUIT

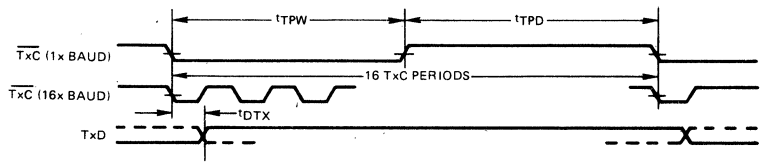


Typical Δ Output Delay Versus Δ Capacitance (pF)

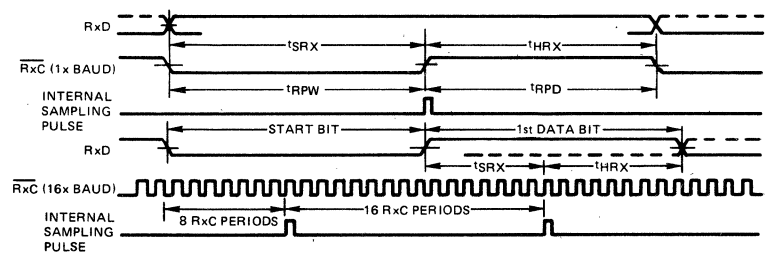
TIMING WAVEFORMS



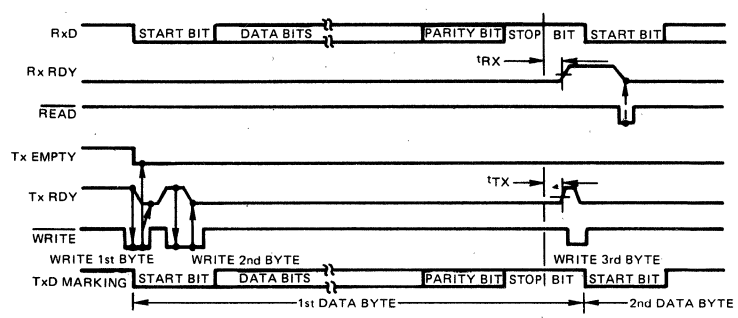
READ AND WRITE TIMING



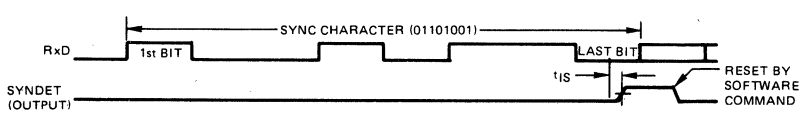
TRANSMITTER CLOCK AND DATA



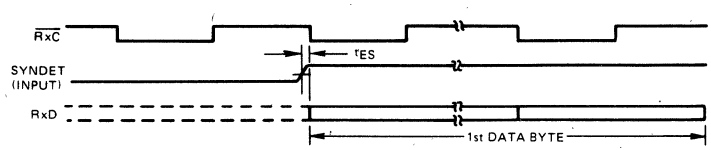
RECEIVER CLOCK AND DATA



TxRDY AND RxRDY TIMING (ASYNC MODE)



INTERNAL SYNC DETECT



EXTERNAL SYNC DETECT

Note: (1) Write and Read pulses have no timing limitation with respect to CLK.

PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the 8251 to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/ Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the μPD8251 to accept the data or control word which the processor is writing out to the USART via the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the μPD8251 to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART for reading and writing to the processor.
Modem Control			The μPD8251 has a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

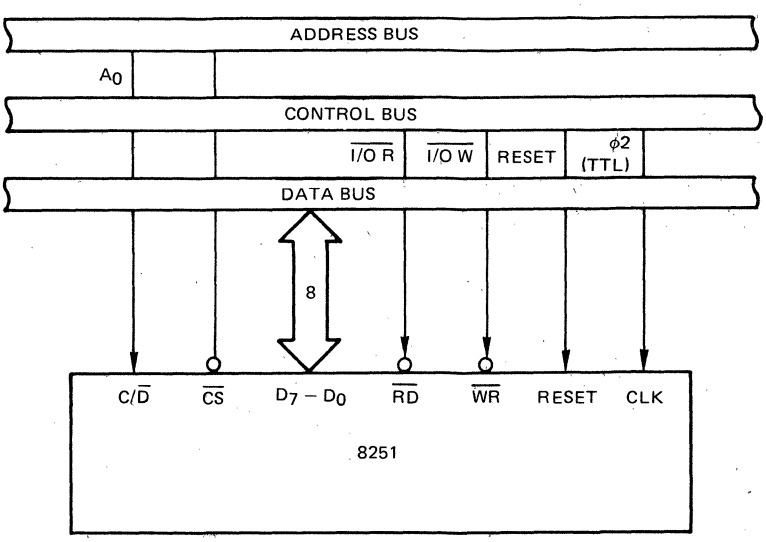
TRANSMIT BUFFER/ CONVERTER

The Transmit Buffer/Converter receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD output.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for Polled operation. Loading a character from the processor automatically resets TxRDY.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

8251 INTERFACE TO 8080 STANDARD SYSTEM BUS



RECEIVER BUFFER

The Receiver Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 sets the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1,16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 on the rising edge of $\overline{RxC}$. (1)
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.

Note: (1) Since the μPD8251 will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):	If the Baud Rate equals 300:
$\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)	$\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
$\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)	$\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
$\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)	$\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 to define the desired mode and communications format. The control words will specify the BAUD RATE FACTOR (1x, 16x, 64x), CHARACTER LENGTH (5 to 8), NUMBER OF STOP BITS (1, 1-1/2, 2), ASYNCHRONOUS or SYNCHRONOUS MODE, SYNDET (IN or OUT), PARITY, etc.

After receiving the control words, the μPD8251 is ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new Command Words.

μPD8251 PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A Reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D} = 1$) followed by a software reset command instruction (40 Hex) can be used to initialize the 8251.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

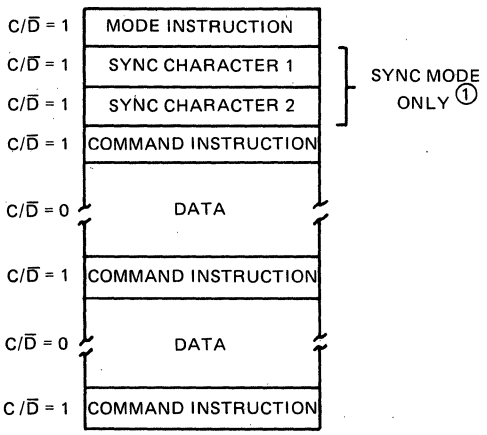
MODE INSTRUCTION

This control word specifies the general characteristics of the interface regarding the SYNCHRONOUS or ASYNCHRONOUS MODE, BAUD RATE FACTOR, CHARACTER LENGTH, PARITY, and NUMBER OF STOP BITS. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

TYPICAL DATA BLOCK



NOTE ① The second SYNC character is skipped if MODE instruction has programmed the 8251 to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the 8251 to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

ASYNCHRONOUS TRANSMISSION

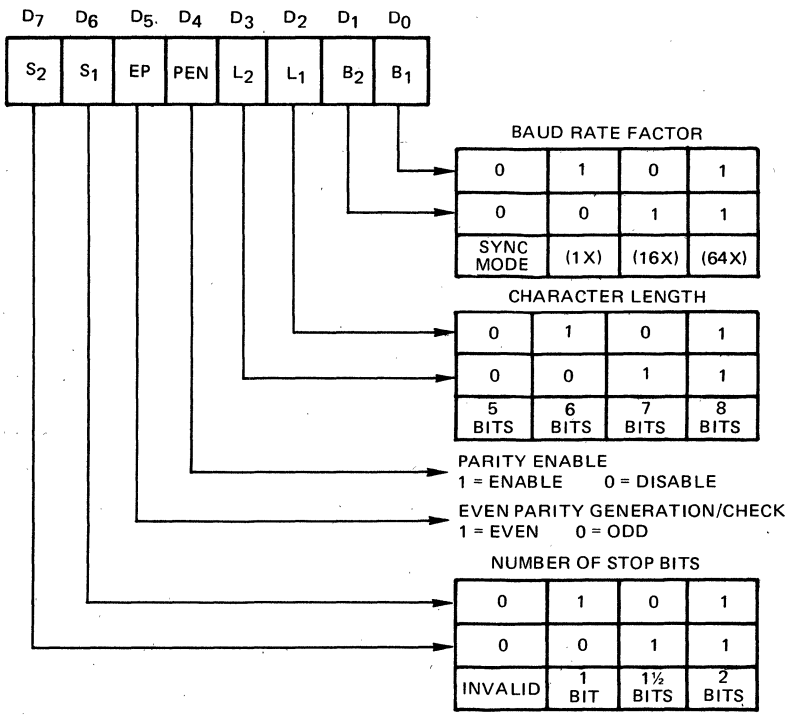
When a data character is written into the μPD8251, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bits(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}/16$ or $\overline{TxC}/64$, as defined by the Mode Instruction.

If no data characters have been loaded into the μPD8251, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

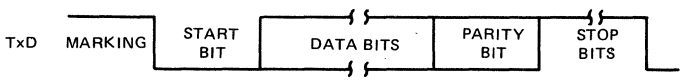
ASYNCHRONOUS RECEIVE

The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the data, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

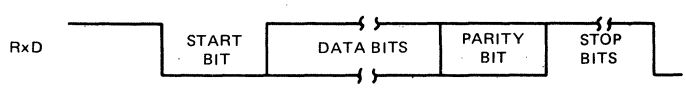
MODE INSTRUCTION FORMAT ASYNCHRONOUS MODE



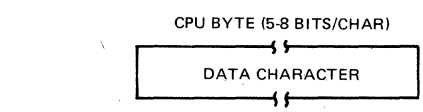
TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



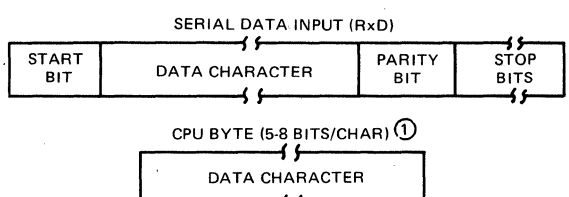
TRANSMITTER OUTPUT



RECEIVER INPUT



TRANSMISSION FORMAT



NOTE ①: IF CHARACTER LENGTH IS DEFINED AS 5, 6, OR 7 BITS; THE UNUSED BITS ARE SET TO "ZERO."

RECEIVE FORMAT

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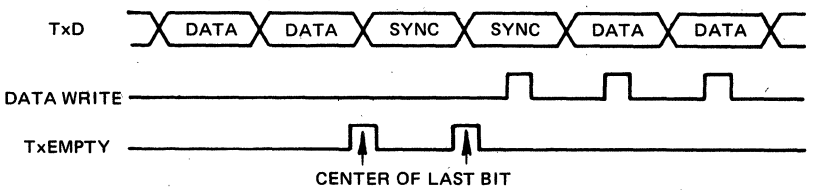
SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 receives the first character from the processor which is usually a SYNC character. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

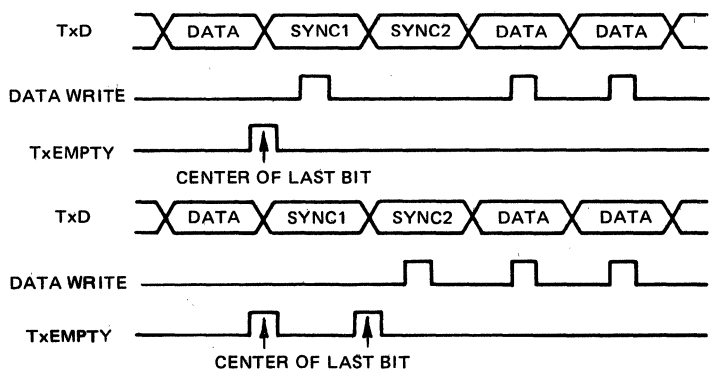
Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 Transmitter Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 becomes empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

TxEMPTY go high at the middle of the last data bit when the Transmit Register is EMPTY. TxEMPTY goes low again as sync characters are transmitted. See figure below.

FOR SINGLE SYNC CHARACTER OPERATION



FOR DOUBLE SYNC CHARACTER OPERATION (BISYNC)



SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

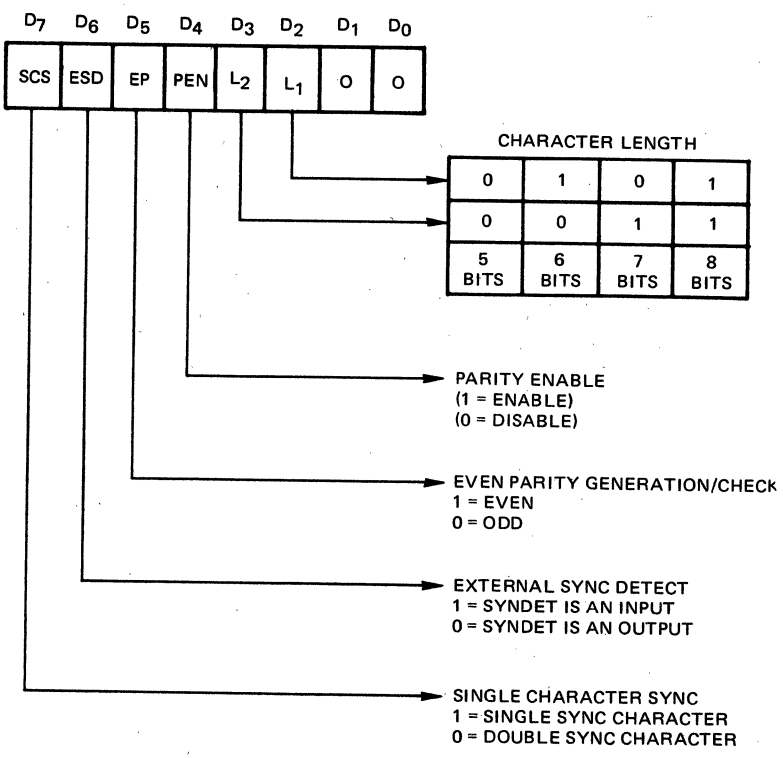
Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receiver Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 leaves the HUNT mode and is in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

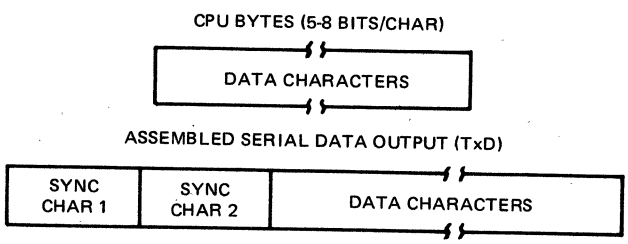
Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. Framing errors do not apply in the Synchronous format.

The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

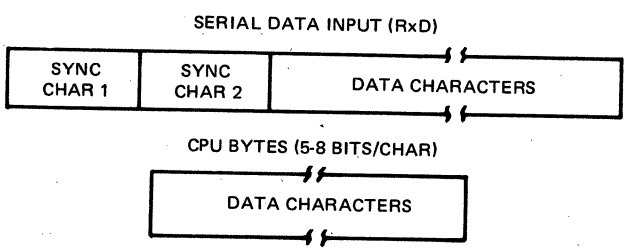
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

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COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 has been specified by the Mode Instruction and the SYNC character(s) have been entered, if in SYNC mode, the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s), as needed, are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The μPD8251 has features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of a 16 clock period.

PARITY ERROR

When a parity error is detected, the PE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

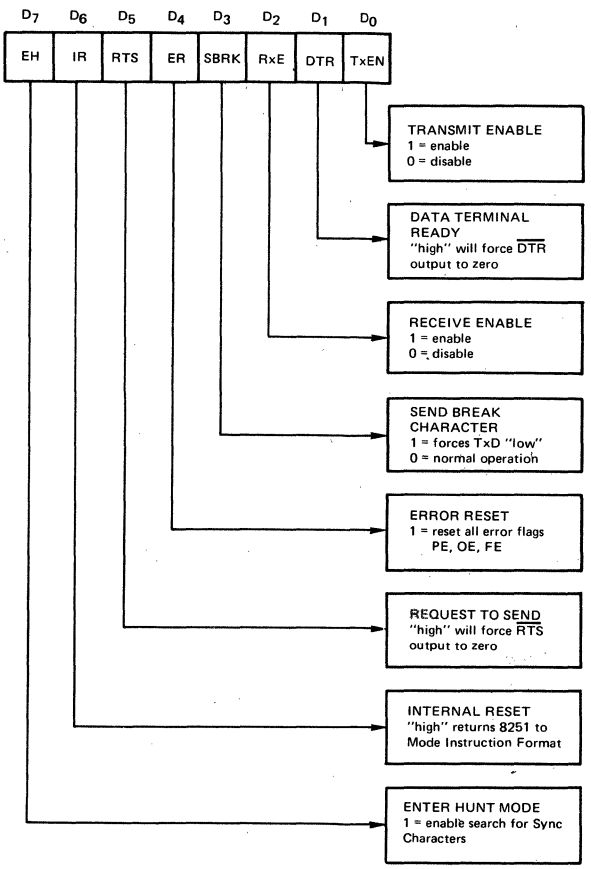
If the processor fails to read a data character before the one following is available, the OE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

FRAMING ERROR ①

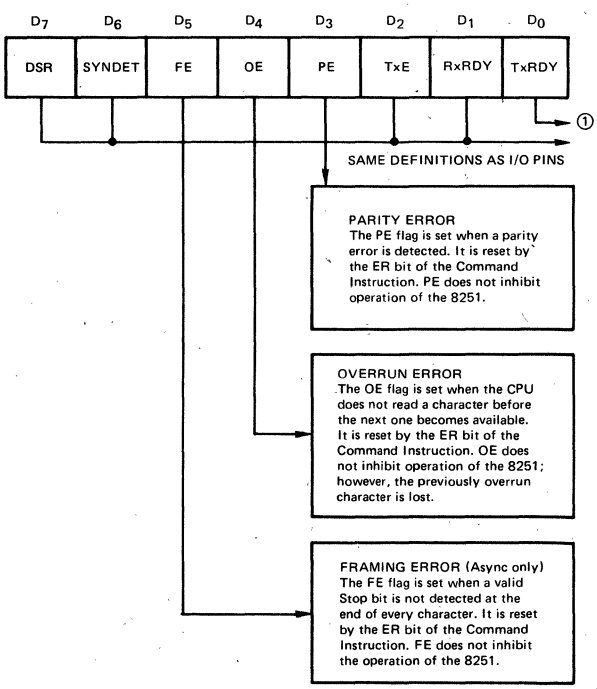
If a valid STOP bit is not detected at the end of a character, the FE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

COMMAND INSTRUCTION FORMAT



STATUS READ FORMAT



Note: ① TxRDY status bit is not totally equivalent to the TxRDY output pin, the relationship is as follows:
TxRDY status bit = DB Buffer Empty
TxRDY (pin 15) = DB Buffer Empty • CTS • TxEn

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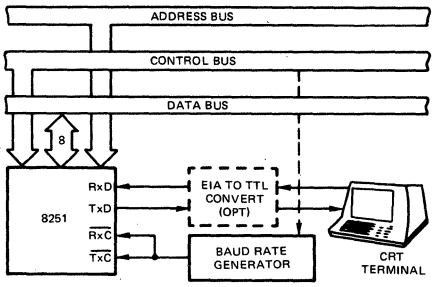
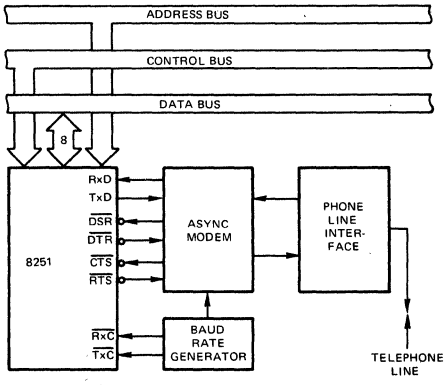
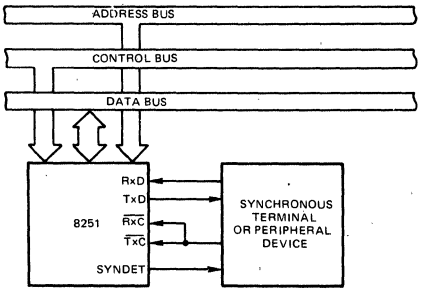
APPLICATION OF THE μPD8251



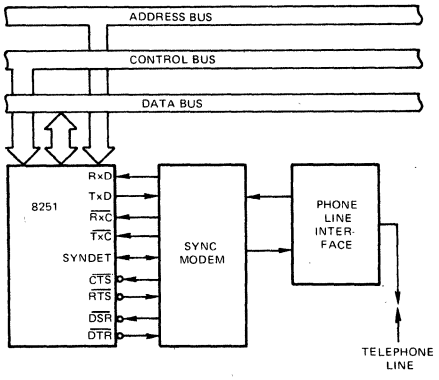
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE



SYNCHRONOUS INTERFACE TO TELEPHONE LINES

PROGRAMMABLE PERIPHERAL INTERFACE

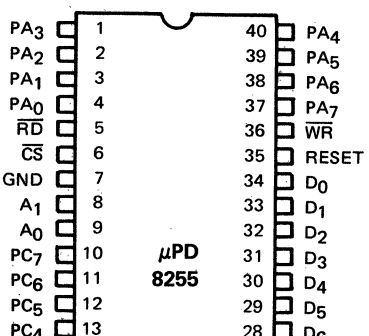
DESCRIPTION

The μPD8255 is a general purpose programmable INPUT/OUTPUT device designed for use with the 8080A microprocessor. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three major modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in a set of 8 and a set of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bidirectional Bus mode, (MODE 2), uses the 8 lines of Port A for a bidirectional bus, and five lines from Port C for bus control signals. The μPD8255 is packaged in a 40 pin plastic DIP.

FEATURES

- Fully Compatible with the 8080A Microprocessor Family
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 2 mA Darlington Drive Outputs for Printers and Displays
- LSI Drastically Reduces System Package Count
- Standard 40 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

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Rev/1

FUNCTIONAL DESCRIPTION

General

The μPD8255 Programmable Peripheral Interface (PPI) is designed for use in 8080A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A data and control busses with the μPD8255. The μPD8255 is functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, eight bit Data Bus Buffer (D_0-D_7) of the μPD8255 can be directly interfaced to the 8080A system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the 8080A. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255 for communication with the 8080A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9

Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode, The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I – Port A and upper Port C (PC_7-PC_4)

Group II – Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents can not be read back to the processor.

Ports A, B, and C

The three 8-bit I/O ports (A, B, and C) in the μPD8255 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255 is further enhanced by special features unique to each of the ports.

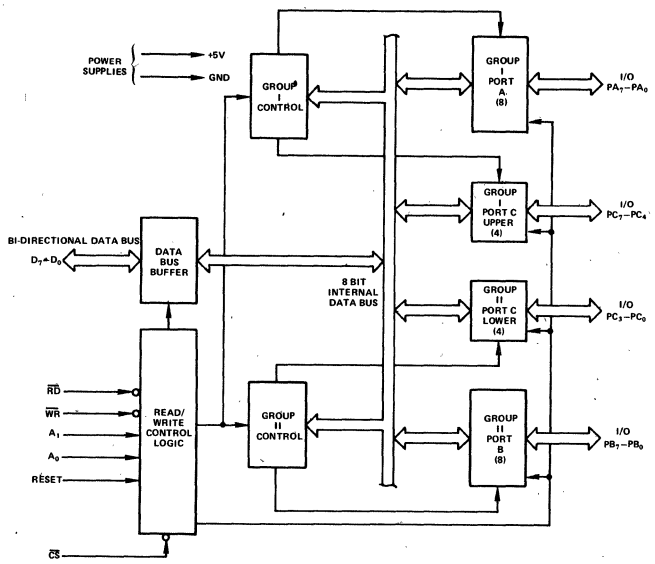
Port A = An 8-bit data output latch/buffer and data input latch.

Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.

Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4 bit control and status ports for use with Ports A & B.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages ①	−0.5 to +7 Volts
All Input Voltages ①	−0.5 to +7 Volts
Supply Voltages ①	−0.5 to +7 Volts

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a ≅ 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS}-.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 1.7 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = 50 μA (−100 μA for D. B. Port)
Darlington Drive Current	I_{OH} ①	1	2	4	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
Power Supply Current	I_{CC}		40	120	mA	V_{CC} = +5V, Output Open
Input Leakage Current	I_{LIH}			10	μA	V_{IN} = V_{CC}
Input Leakage Current	I_{LIL}			−10	μA	V_{IN} = 0.4V
Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}; $\overline{CS}$ = 2.0V
Output Leakage Current	I_{LOL}			−10	μA	V_{OUT} = 0.4V, $\overline{CS}$ = 2.0V

Note: ① Any set of eight (8) outputs from either Port A, B, or C can source 2 mA into 1.5 volts.

CAPACITANCE

T_a = 25°C; V_{CC} = V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

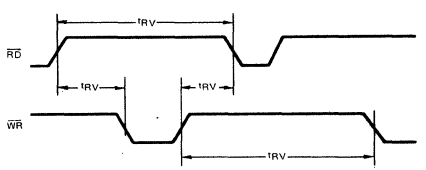
AC CHARACTERISTICS

8080 BUS PARAMETERS:
$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$, $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable Before $\overline{READ}$	t_{AR}	50			ns	
Address Stable After $\overline{READ}$	t_{RA}	0			ns	
$\overline{READ}$ Pulse Width	t_{RR}	405			ns	
Data Valid From $\overline{READ}$	t_{RD}			295	ns	CL = 100 pF
Data Float After $\overline{READ}$	t_{DF}			150	ns	CL = 100 pF
		10			ns	CL = 15 pF
Time Between $\overline{READS}$ and/or $\overline{WRITES}$	t_{RV}	850			ns	②
WRITE						
Address Stable Before $\overline{WRITE}$	t_{AW}	20			ns	
Address Stable After $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Valid To $\overline{WRITE}$ (L.E.)	t_{DW}	10			ns	
Data Valid After $\overline{WRITE}$	t_{WD}	35			ns	
OTHER TIMING						
$\overline{WR}$ = 0 To Output	t_{WB}			500	ns	CL = 50 pF
Peripheral Data Before $\overline{RD}$	t_{IR}	0			ns	
Peripheral Data After $\overline{RD}$	t_{HR}	50			ns	
$\overline{ACK}$ Pulse Width	t_{AK}	500			ns	
$\overline{STB}$ Pulse Width	t_{ST}	350			ns	
Per. Data Before T.E. Of $\overline{STB}$	t_{PS}	60			ns	
Per. Data After T.E. Of $\overline{STB}$	t_{PH}	150			ns	
$\overline{ACK}$ = 0 To Output	t_{AD}			400	ns	CL = 50 pF
$\overline{ACK}$ = 0 To Output Float	t_{KD}			300	ns	CL = 50 pF
		20				CL = 15 pF
$\overline{WR}$ = 1 To $\overline{OBF}$ = 0	t_{WOB}			300	ns	CL = 50 pF
$\overline{ACK}$ = 0 To $\overline{OBF}$ = 1	t_{AOB}			450	ns	CL = 50 pF
$\overline{STB}$ = 0 To IBF = 1	t_{SIB}			450	ns	CL = 50 pF
$\overline{RD}$ = 1 To IBF = 0	t_{RIB}			360	ns	CL = 50 pF
$\overline{RD}$ = 0 To INTR = 0	t_{RIT}			450	ns	CL = 50 pF
$\overline{STB}$ = 1 To INTR = 1	t_{SIT}			400	ns	CL = 50 pF
$\overline{ACK}$ = 1 To INTR = 1	t_{AIT}			400	ns	CL = 50 pF
$\overline{WR}$ = 0 To INTR = 0	t_{WIT}			850	ns	CL = 50 pF

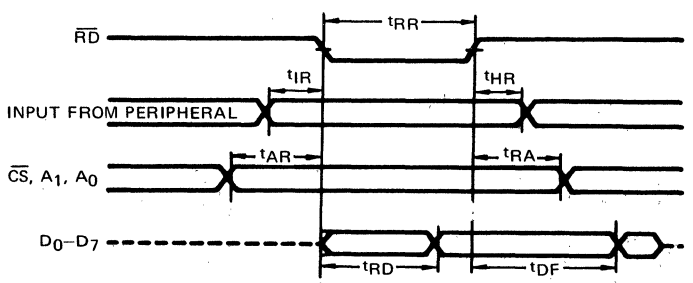
Notes: ① Period of Reset pulse must be at least 50 μs during or after power on. Subsequent Reset pulse can be 500 ns min.

②

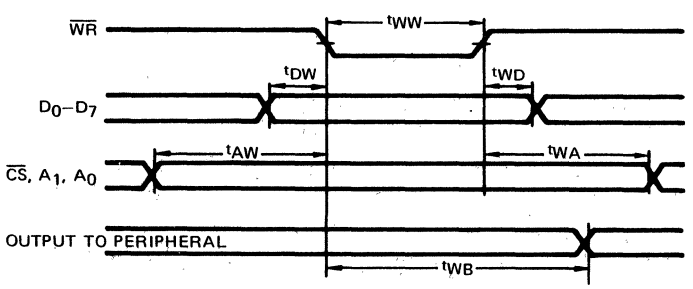


TIMING WAVEFORMS

MODE 0



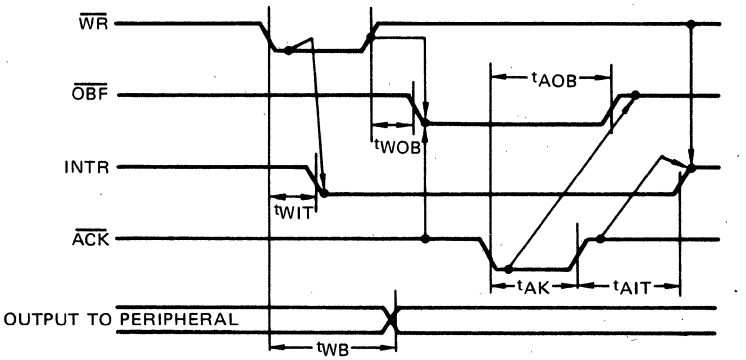
BASIC INPUT



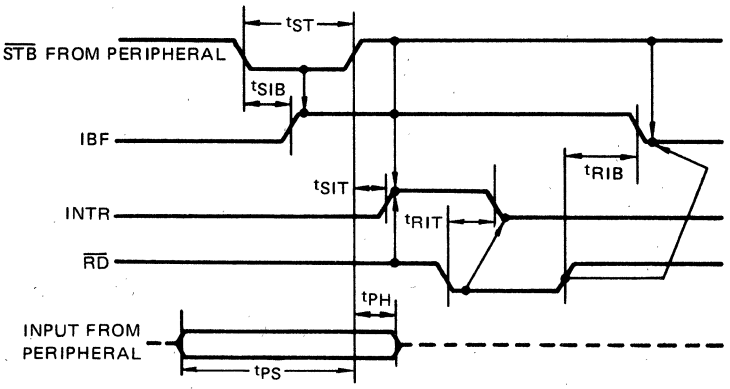
BASIC OUTPUT

TIMING WAVEFORMS (CONT.)

MODE 1

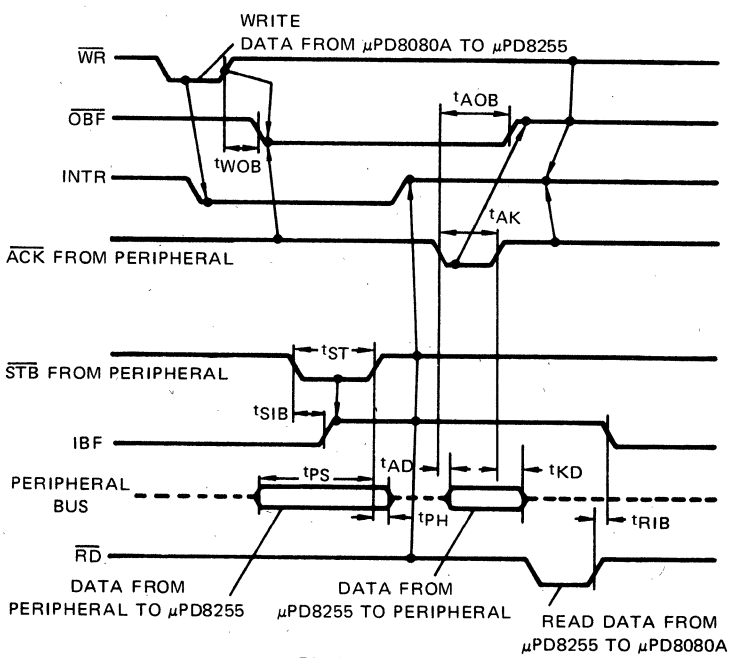


STROBED OUTPUT



STROBED INPUT

MODE 2



BI-DIRECTIONAL

Note: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

MODES

The μPD8255 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.
- 16 different configurations in MODE 0
- Two 8-bit ports and two 4-bit ports
- Inputs are not latched
- Outputs are latched

MODE 1

- MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C.
- Two I/O Groups (I and II)
- Both groups contain an 8-bit data port and a 4-bit control/data port
- Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

- MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.
- An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})
- Both inputs and outputs are latched
- An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

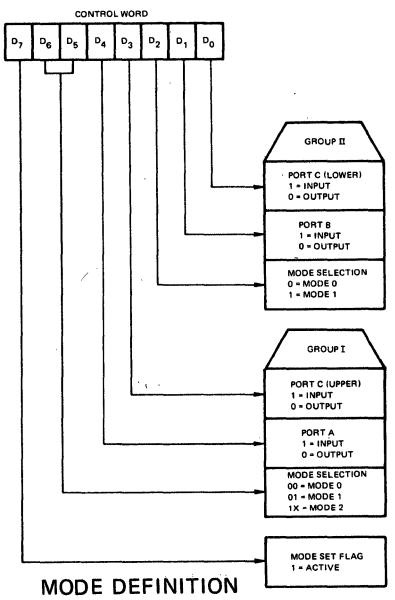
INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

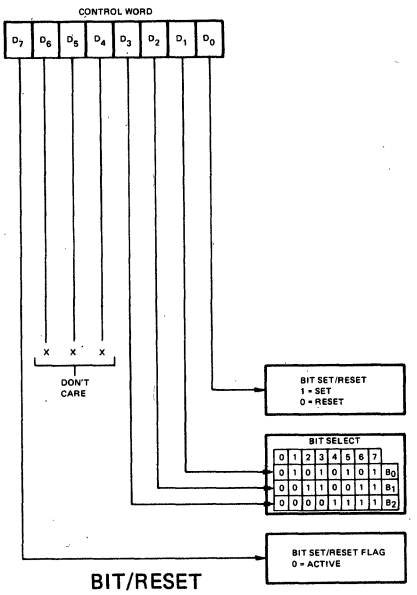
DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

NOTES: ① X means "DO NOT CARE."
② All conditions not listed are illegal and should be avoided.

FORMATS

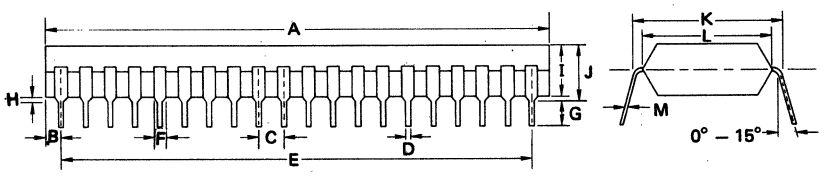


MODE DEFINITION



BIT/RESET

PACKAGE OUTLINE
μPB8255C



μPD8255C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.5 MIN	0.06 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

PROGRAMMABLE DMA CONTROLLER

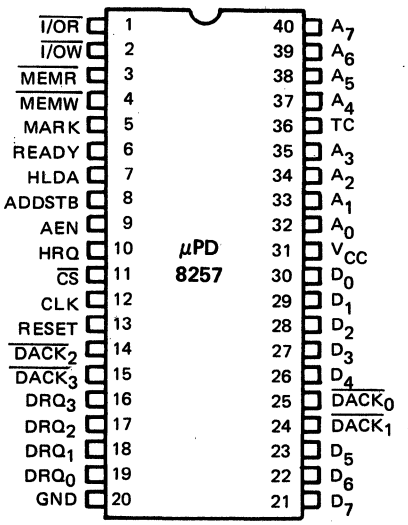
DESCRIPTION

The μPD8257 is a programmable four-channel Direct Memory Access (DMA) controller. It is designed to simplify high speed transfers between peripheral devices and memories. Upon a peripheral request, the 8257 generates a sequential memory address, thus allowing the peripheral to read or write data directly to or from memory. Peripheral requests are prioritized within the 8257 so that the system bus may be acquired by the generation of a single HOLD command to the 8080. DMA cycle counts are maintained for each of the four channels, and a control signal notifies the peripheral when the preprogrammed member of DMA cycles has occurred. Output control signals are also provided which allow simplified sectored data transfers and expansion to other 8257 devices for systems requiring more than four DMA channels.

FEATURES

- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Automatic Load Mode
- Single TTL Clock
- Single +5V Supply
- Expandable
- 40 Pin Plastic Dual-In-Line Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus
A_7-A_0	Address Bus
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
CLK	Clock Input
RESET	Reset Input
READY	Ready
HRQ	Hold Request (to 8080A)
HLDA	Hold Acknowledge (from 8080A)
AEN	Address Enable
ADSTB	Address Strobe
TC	Terminal Count
MARK	Modulo 128 Mark
DRQ_3-DRQ_0	DMA Request Input
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA Acknowledge Out
$\overline{CS}$	Chip Select
V_{CC}	+5 Volts
GND	Ground

FUNCTIONAL DESCRIPTION

The 8257 is a programmable, Direct Memory Access (DMA) device and when used with an 8212 I/O port device, it provides a complete four-channel DMA controller for use in 8080 based systems. Once initialized by an 8080 CPU, the 8257 will block transfer up to 16,364 bytes of data between memory and a peripheral device without any attention from the CPU, and it will do this on all 4-DMA channels. After receiving a DMA transfer request from a peripheral, the following sequence of events occur within the 8257.

- It acquires control of the system bus (placing 8080 in hold mode).
- Resolves priority conflicts if multiple DMA requests are made.
- A 16 bit memory address word is generated with the aid of an 8212 in the following manner:

  The 8257 outputs the least significant eight bits (A_0-A_7) which go directly onto the address bus.

  The 8257 outputs the most significant eight bits (A_8-A_{15}) onto the data bus where they are latched into an 8212 and then sent to the high order bits on the address bus.
- The appropriate memory and I/O read/write control signals are generated allowing the peripheral to receive or deposit a data byte directly from or to the appropriate memory location.

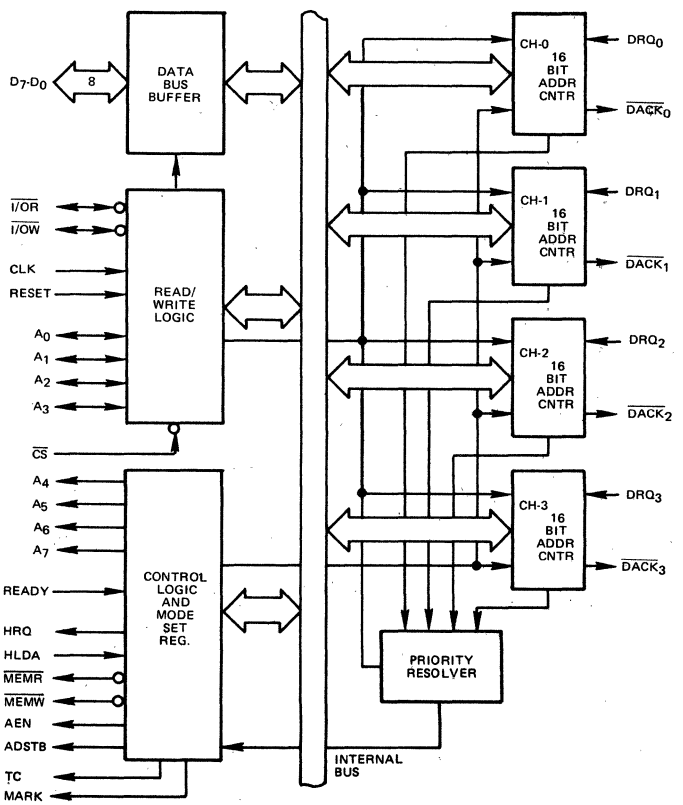
Block transfer of data (e.g., a sector of data on a floppy disk) either to or from a peripheral may be accomplished as long as the peripheral maintains its DMA Request (DRQ_n). The 8257 retains control of the system bus as long as DRQ_n remains high or until the Terminal Count (TC) is reached. When the Terminal Count occurs, TC goes high, informing the CPU that the operation is complete.

There are three different modes of operation:

- DMA read; which causes data to be transferred from memory to a peripheral;
- DMA write; which causes data to be transferred from a peripheral to memory; and
- DMA verify; which does not actually involve the transfer of data.

The DMA read and write modes are the normal operating conditions for the 8257. The DMA verify mode responds in the same manner as read/write except no memory or I/O read/write control signals are generated, thus preventing the transfer of data. The peripheral gains control of the system bus and obtains DMA Acknowledgements for its requests, thus allowing it to access each byte of a data block for check purposes or accumulation of a CRC (Cyclic Redundancy Code) checkword. In some applications it is necessary for a block of DMA read or write cycles to be followed by a block of DMA verify cycles to allow the peripheral to verify its newly acquired data.

BLOCK DIAGRAM



AC CHARACTERISTICS PERIPHERAL (SLAVE) MODE

BUS PARAMETERS

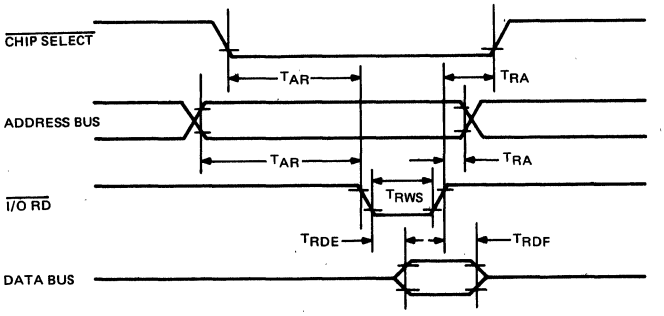
T_a = 0°C to 70°C; V_{CC} = 5V ± 5%; GND = 0V ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Adr or $\overline{CS}$↓ Setup to $\overline{Rd}$↓	T_{AR}	50			ns	
Adr or $\overline{CS}$↑ Hold from $\overline{Rd}$↑	T_{RA}	0			ns	
Data Access from $\overline{Rd}$↓	T_{RDE}	0		300	ns	C_L = 100pF
DB→Float Delay from $\overline{Rd}$↑	T_{RDF}			150	ns	C_L = 100pF
		20			ns	C_L = 15pF
$\overline{Rd}$ Width	T_{RW}	300			ns	
WRITE						
$\overline{CS}$↓ Setup to $\overline{Wr}$↓	T_{CW}	300			ns	
$\overline{CS}$↑ Hold from $\overline{Wr}$↑	T_{WC}	20			ns	
Adr Setup to $\overline{Wr}$↓	T_{AW}	20			ns	
Adr Hold from $\overline{Wr}$↑	T_{WA}	20			ns	
Data Setup to $\overline{Wr}$↓	T_{DW}	200			ns	
Data Hold from $\overline{Wr}$↑	T_{WD}	35			ns	
Wr Width	T_{WWS}	200			ns	
OTHER TIMING						
Reset Pulse Width	T_{RSTW}	300			ns	
Power Supply↑(V_{CC}) Setup to Reset↓	T_{RSTD}	500			μs	
Signal Rise Time	T_r			20	ns	
Signal Fall Time	T_f			20	ns	
Reset to First $\overline{IOWR}$	T_{RSTS}	2			t_{CY}	

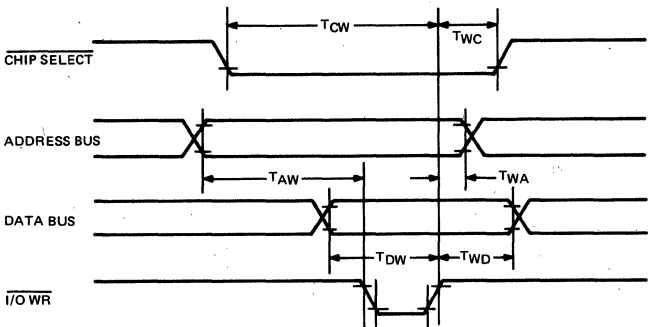
Note: ① All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V.

TIMING WAVEFORMS PERIPHERAL (SLAVE) MODE

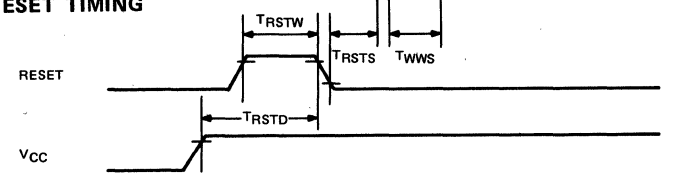
READ TIMING



WRITE TIMING



RESET TIMING



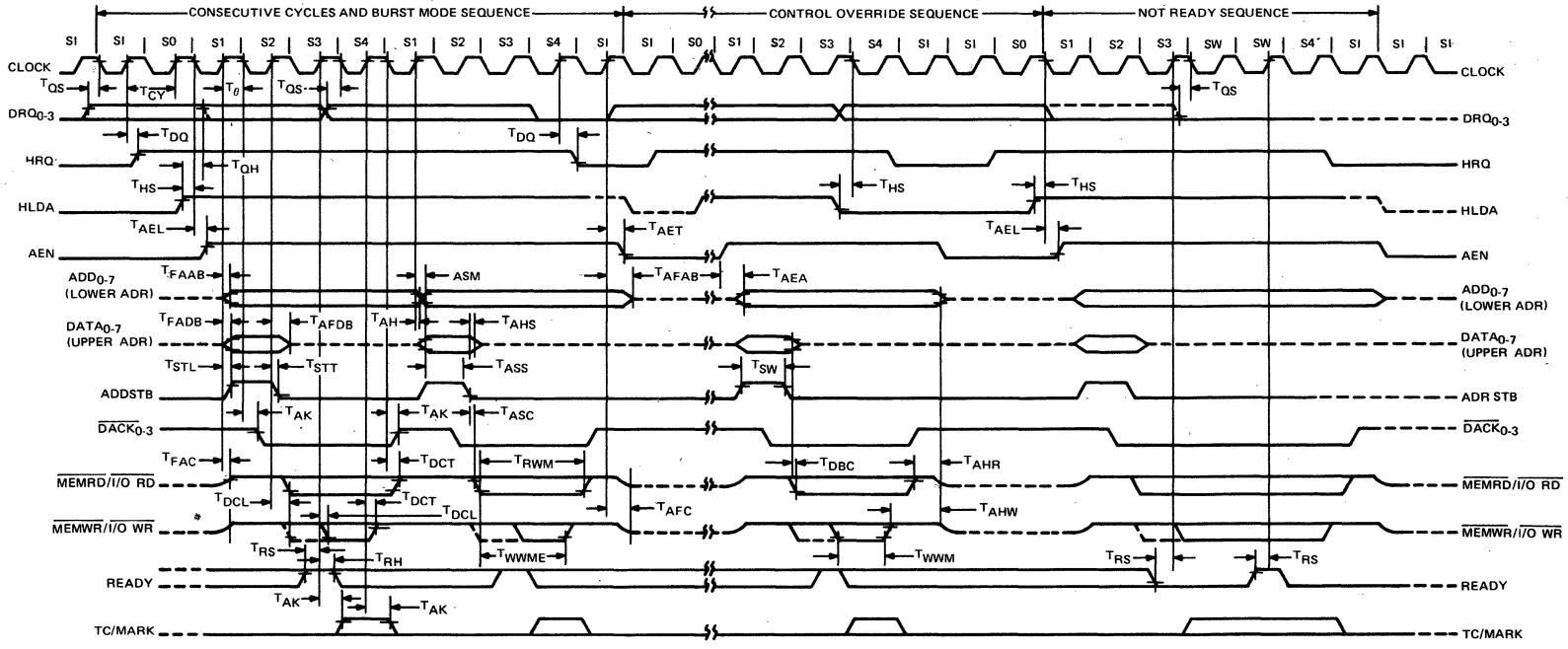
AC CHARACTERISTICS DMA (MASTER) MODE

T_a = 0°C to 70°C; V_{CC} = +5V ±5%; GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Cycle Time (Period)	T_{CY}	0.330		4	μs	
Clock Active (High)	T_θ	150		.8T_{CY}	ns	
DRQ↑ Setup to θ↓ (SI, S4)	T_{QS}	120				
DRQ↓ Hold from HLDA↑	T_{QH}	0				④
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 2.0V)	T_{DQ}			160	ns	①
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 3.3V)	T_{DQ1}			250	ns	③
HLDA↑ or ↓Setup to θ↓ (SI, S4)	T_{HS}	100			ns	
AEN↑ Delay from θ↓ (S1)	T_{AEL}			300	ns	①
AEN↓ Delay from θ↑ (SI)	T_{AET}			200	ns	①
Adr (AB) (Active) Delay from AEN↑ (S1)	T_{AEA}	20			ns	④
Adr (AB) (Active) Delay from θ↑ (S1)	T_{FAAB}			250	ns	②
Adr (AB) (Float) Delay from θ↑ (SI)	T_{AFAB}			150	ns	②
Adr (AB) (Stable) Delay from θ↑ (S1)	T_{ASM}			250	ns	②
Adr (AB) (Stable) Hold from θ↑ (S1)	T_{AH}	T_{ASM}–50				②
Adr (AB) (Valid) Hold from $\overline{Rd}$↑ (S1,SI)	T_{AHR}	60			ns	④
Adr (AB) (Valid) Hold from $\overline{Wr}$↑ (S1, SI)	T_{AHW}	300			ns	④
Adr (DB) (Active) Delay from θ↑ (S1)	T_{FADB}			300	ns	②
Adr (DB) (Float) Delay from θ↑ (S2)	T_{AFDB}	T_{STT}+20		250	ns	②
Adr (DB) Setup to Adr Stb↓ (S1-S2)	T_{ASS}	100			ns	④
Adr (DB) (Valid) Hold from Adr Stb↓ (S2)	T_{AHS}	50			ns	④
Adr Stb↑ Delay from θ↑ (S1)	T_{STL}			200	ns	①
Adr Stb↓ Delay from θ↑ (S2)	T_{STT}			140	ns	①
Adr Stb Width (S1-S2)	T_{SW}	T_{CY}–100			ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr Stb↓ (S2)	T_{ASC}	70			ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr (DB) (Float) (S2)	T_{DBC}	20			ns	④
DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark↑ Delay from θ↑ (S3) and TC/Mark↓ Delay from θ↑ (S4)	T_{AK}			250	ns	①⑤
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from θ↑ (S2) and $\overline{Wr}$↓ Delay from θ↑ (S3)	T_{DCL}			200	ns	②⑥
$\overline{Rd}$↑ Delay from θ↓ (S1, SI) and $\overline{Wr}$↑ Delay from θ↑ (S4)	T_{DCT}			200	ns	②⑦
$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑ (S1)	T_{FAC}			300	ns	②
$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑ (SI)	T_{AFC}			150	ns	②
$\overline{Rd}$ Width (S2-S1 or SI)	T_{RWM}	2T_{CY} + T_θ–50			ns	④
$\overline{Wr}$ Width (S3-S4)	T_{WWM}	T_{CY}–50			ns	④
$\overline{Wr}$ (Ext) Width (S2-S4)	T_{WWME}	2T_{CY}–50			ns	④
READY Set Up Time to θ↑ (S3, Sw)	T_{RS}	30			ns	
READY Hold Time from θ↑ (S3, Sw)	T_{RH}	20			ns	

Notes:
① Load = 1 TTL
② Load = 1 TTL + 50pF
③ Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V
④ Tracking Specification
⑤ $\Delta T_{AK} < 50$ ns
⑥ $\Delta T_{DCL} < 50$ ns
⑦ $\Delta T_{DCT} < 50$ ns

TIMING WAVEFORMS
DMA (MASTER) MODE



DMA OPERATION

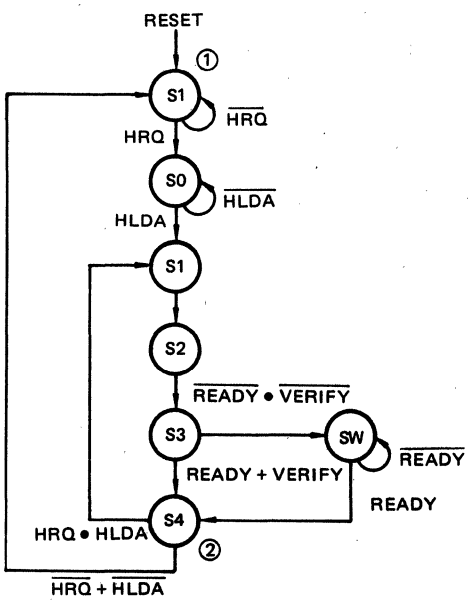
Internally the 8257 contains six different states (S0, S1, S2, S3, S4 and SW), the duration of each state is determined by the input clock. In the idle state, (S1), no DMA operation is being executed. A DMA cycle is started upon receipt of one or more DMA Requests (DRQ_n), then the 8257 enters the S0 state. During state S0 a Hold Request (HRQ) is sent to the 8080 and the 8257 waits in S0 until the 8080 issues a Hold Acknowledge (HLDA) back. During S0, DMA Requests are sampled and DMA priority is resolved (based upon either the fixed or priority scheme). After receipt of HLDA, the DMA Acknowledge line ($\overline{DACK}_n$) with the highest priority is driven low selecting that particular peripheral for the DMA cycle. The DMA Request line (DRQ_n) must remain high until either a DMA Acknowledge ($\overline{DACK}_n$) or both $\overline{DACK}_n$ and TC (Terminal Count) occur, indicating the end of a block or sector transfer (burst mode).

The DMA cycle consists of four internal states; S1, S2, S3 and S4. If the access time of the memory or I/O device is not fast enough to return a Ready command to the 8257 after it reaches state S3, then a Wait state is initiated (SW). One or more than one Wait state occurs until a Ready signal is received, and the 8257 is allowed to go into state S4. Either the extended write option or the DMA Verify mode may eliminate any Wait state.

If the 8257 should lose control of the system bus (i.e., HLDA goes low) then the current DMA cycle is completed, the device goes into the S1 state, and no more DMA cycles occur until the bus is reacquired. Ready setup time (t_{RS}), write setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) should all be carefully observed during the handshaking mode between the 8257 and the 8080.

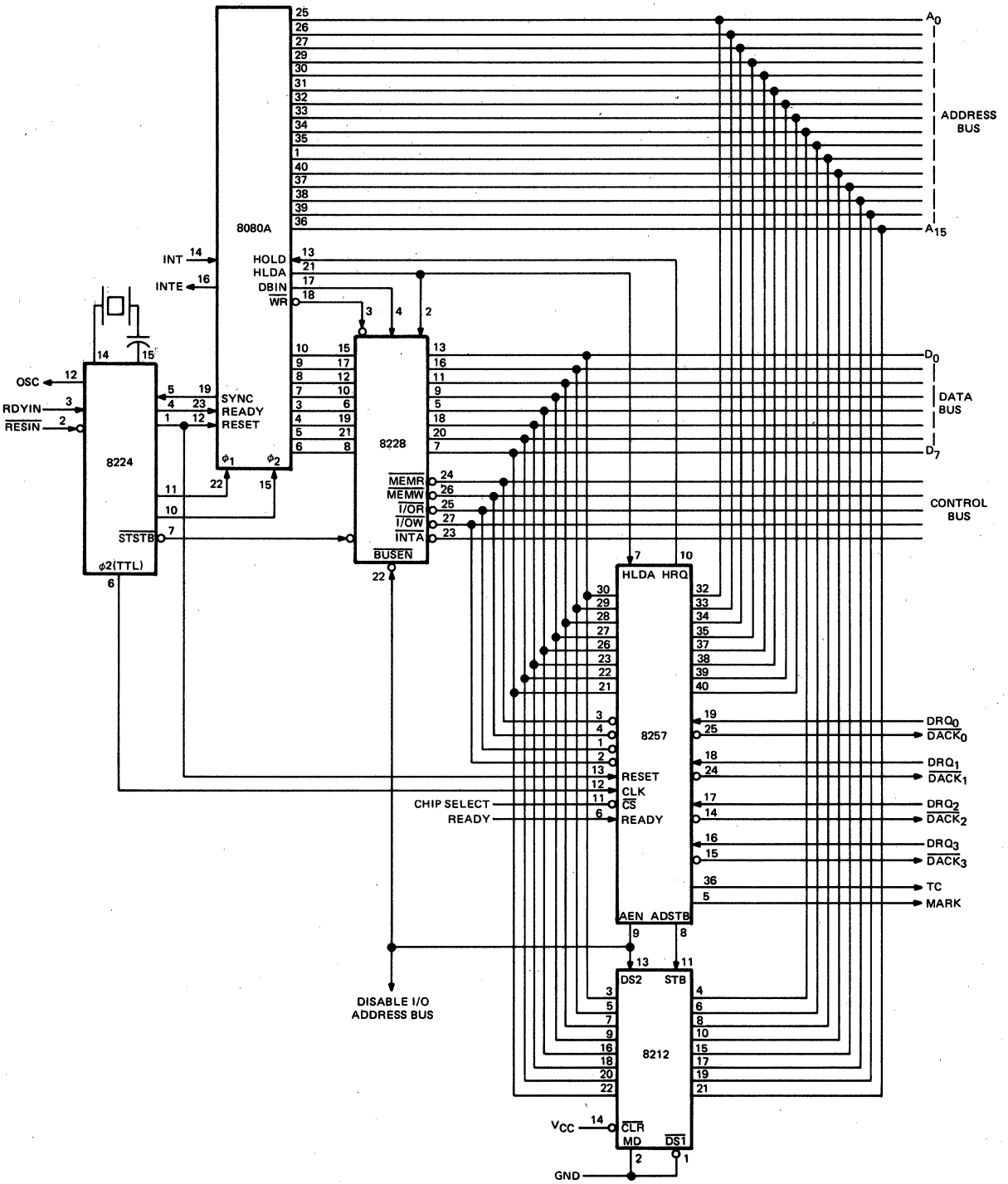
During DMA write cycles, the I/O Read ($\overline{I/O\ R}$) output is generated at the beginning of state S2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S2 and the I/O Write ($\overline{I/O\ W}$) goes low at the beginning of state S3. No Read or Write control signals are generated during DMA verify cycles.

DMA OPERATION STATE DIAGRAM



Notes: ① HRQ is set if DRQ_n is active.
② HRQ is reset if DRQ_n is not active.

TYPICAL 8257
SYSTEM INTERFACE SCHEMATIC



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin ..... -0.5 to +7 Volts ①
Power Dissipation ..... 1 Watt

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Low Voltage	V_{IL}	-0.5		0.8	Volts	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	Volts	
Output Low Voltage	V_{OL}			0.45	Volts	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	Volts	I_{OH} = -150 μA for AB, DB and AEN I_{OH} = -80 μA for others
HRQ Output High Voltage	V_{HH}	3.3		V_{CC}	Volts	I_{OH} = -80 μA
V_{CC} Current Drain	I_{CC}			120	mA	
Input Leakage	I_{IL}			10	μA	V_{IN} = V_{CC}
Output Leakage During Float	I_{OFL}			10	μA	V_{OUT} ①

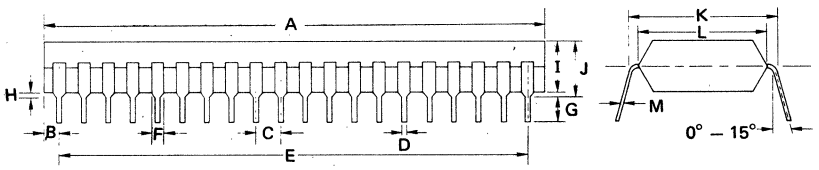
Note: ① $V_{CC} > V_{OUT} >$ GND + 0.45V

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

NEC microcomputers, inc.

PRELIMINARY

μPD8253

PROGRAMMABLE INTERVAL TIMER

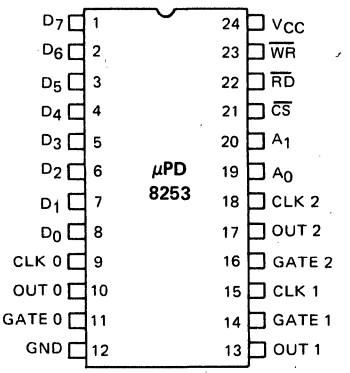
DESCRIPTION

The NEC μPD8253 is a fully programmable, multi-mode, 16-bit counter/timer. It is designed as a general purpose device capable of interfacing directly to an 8080 microprocessor system as an array of I/O ports. The μPD8253 can generate accurate time delays under the control of system software. It contains three independent 16-bit counters which can be clocked at rates from DC to 2 MHz.

FEATURES

- Three Independent 16-Bit Counters
- DC to 2 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- 24 Pin Dual-In-Line Package
- +5V NMOS Technology

PIN CONFIGURATION



NEC microcomputers, inc.

PRELIMINARY

μPD8255A

PROGRAMMABLE PERIPHERAL INTERFACE

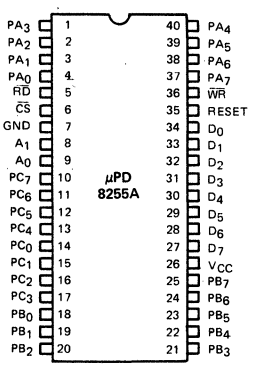
DESCRIPTION

The NEC μPD8255A is a programmable peripheral interface device having 24 programmable I/O pins. It is directly compatible with the 8080 microprocessor system, and normally no extra logic is required to interface to the 8080A. The system software can individually program each of the 24 I/O pins into two groups of twelve for the three major modes of operation.

FEATURES

- Completely TTL Compatible
- Fully Compatible with NEC μP Families
- Direct Bit Set/Reset Capabilities Easing Control Application Interface
- 40 Pin Dual-In-Line Package
- Reduces System Package Count
- Capabilities to Drive Darlington Pairs

PIN CONFIGURATION



PROGRAMMABLE INTERRUPT CONTROLLER

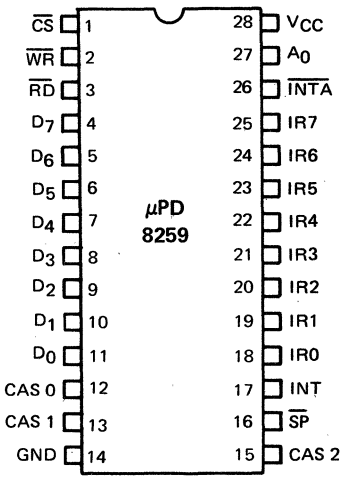
DESCRIPTION

The NEC μPD8259 is a programmable interrupt controller which can handle up to eight vectored priority interrupts in an 8080 microprocessor system. It can be cascaded to extend the vectored priority interrupt capability to 64 without extra circuitry. It is system software programmable with a selection of priority algorithms available which can be dynamically changed at any time.

FEATURES

- Eight Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Algorithms
- Individual Request Mask Capability
- Single +5V Supply
- Static Circuitry (No Clock)

PIN CONFIGURATION



NEC microcomputers, inc.

PRELIMINARY

μPD8085

SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

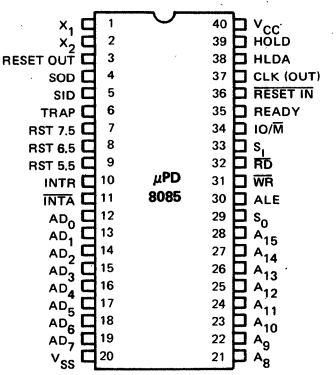
DESCRIPTION

The NEC μPD8085 is the next generation single chip 8-bit microprocessor. It provides full software compatibility with the 8080A but with an improved, higher system speed. The μPD8085's higher level of system integration allows the functions of the μPD8224 (clock generator) and the μPD8228 (system controller) to be incorporated into its design. Together with the μPD8155/8156 (2K RAM) and the μPD8355/8755 (16K ROM/EPROM) a minimum system can be configured using just three IC's. The DATA BUS of the μPD8085 multiplexes the 8-bit address bus and the 8-bit data bus to achieve greater system throughput. The μPD8155/8156 and the μPD8355/8755 memory products have on-chip address latches which provide direct interfacing to the μPD8085.

FEATURES

- Single +5V Supply
- 1.3 μs Instruction Cycle
- On-Chip System Controller
- 100% Software Compatibility with the μCOM-8 Family
- On-Chip Clock Generator (with External Crystal or RC Network)
- Four Vectored Interrupts (One is Non-Maskable)
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory

PIN CONFIGURATION



NEC microcomputers, inc.

PRELIMINARY

μPD8155

μPD8156

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

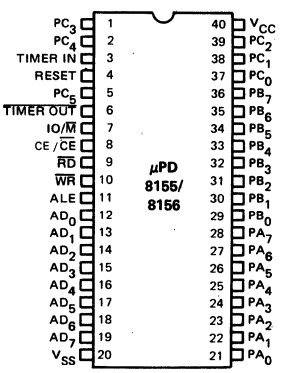
DESCRIPTION

The NEC μPD8155 and μPD8156 2048-bit Static Random Access Memories are organized as 256 x 8 and are fully compatible with the μPD8085 microprocessor system. Three I/O pins allow programmable status and handshaking capabilities with the processor. The on-chip 14 bit counter timer is fully programmable by the system software.

FEATURES

- 256 Words x 8 Bits Organization
- 400 ns Access Time (No Wait States Required)
- Multiplexed Address and Data Bus
- Programmable 14 Bit Binary Counter/Timer
- 1 Programmable 6 Bit I/O Port
- 2 Programmable 8 Bit I/O Ports

PIN CONFIGURATION



μPD8355
μPD8755

16,384 BIT ROM WITH I/O / 16,384 BIT EPROM WITH I/O

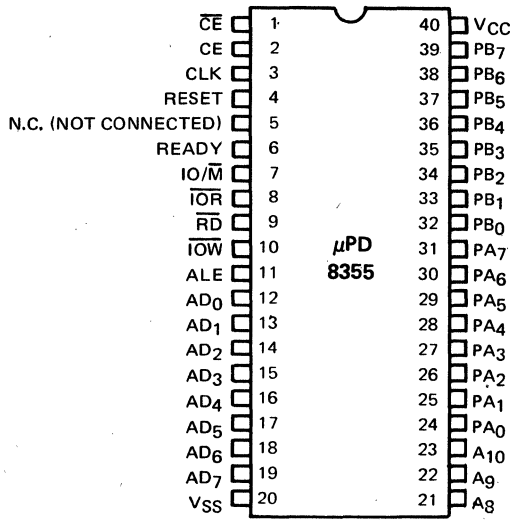
DESCRIPTION

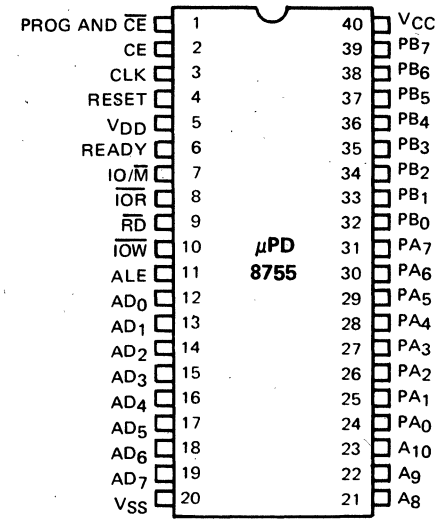
The NEC μPD8355 is a 16,384 bit Read Only Memory with I/O organized as 2048 words x 8 bits. The μPD8755 is a 16,384 bit erasable and electrically programmable Read Only Memory. Access time for both devices is 400 ns so no wait state are required in the processor. There are two separately programmable, 8 bit wide I/O ports for interfacing to the processor.

FEATURES

- 2048 Words x 8 Bits
- Single +5V Power Supply
- Internal Address Latch
- 2 General Purpose 8 Bit I/O Ports
- Multiplexed Address and Data Bus
- Direct Compatibility with μPD8085 and μPD8048

PIN CONFIGURATIONS





PRELIMINARY

μPD8048
μPD8748
μPD8035

SINGLE COMPONENT 8-BIT MICROCOMPUTER

DESCRIPTION

The NEC μPD8048/8748/8035 are complete, single-chip, NMOS microcomputers requiring only a single +5V power supply. There are three interchangeable microcomputers in this family to allow the user maximum freedom in systems implementation. In addition, if system expansion is necessary, the μPD8048/8748/8035 are fully compatible with NEC's family of 8080A peripherals including memory devices.

The on-chip features of the μPD8048 include 1K x 8 bits of Read Only Memory for firm program storage, 64 x 8 bits of Random Access Memory which can be used as a scratch pad, 27 I/O lines, an 8-bit counter/timer and clock, oscillator and clock driver circuitry requiring only an off-the-chip crystal.

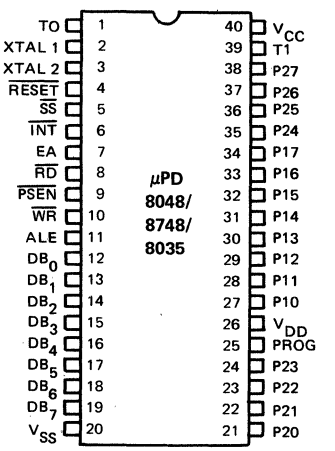
The μPD8035 is functionally and pin-for-pin compatible with the μPD8048 but without the 1K x 8 bit ROM, which is intended for use with external memory.

The μPD8748 is also fully compatible with both the μPD8048 and μPD8035. In this device the 1K x 8 bit ROM has been replaced with a 1K x 8 bit erasable, electrically programmable ROM to provide the user with the flexibility of changing the program memory contents.

FEATURES

- 8 Bit Parallel Processor, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single +5V Supply
- 2.5 μsec and 5.0 μsec Cycle Versions
  All Instructions 1 or 2 Cycles
- Over 90 Instructions: 70% Single Byte
  None Over Two Bytes
- 1K x 8 ROM/EPROM, 64 x 8 RAM,
  27 I/O Lines
- Programmable Counter/Timer
- Easily Expandable Memory and I/O
- Single Level Interrupt
- Compatible with μCOM-8 Series Peripherals

PIN CONFIGURATION



NEC microcomputers, inc.

PRELIMINARY
μPB2901

μPB2901 4-BIT MICROPROCESSOR SLICE

DESCRIPTION

The NEC μPB2901 is a four-bit microprocessor slice, with an expandable bus structure extending interface capabilities to all other members of the μPB2900 series family. The internal functions of the μPB2901 include an eight-function ALU, sixteen addressable registers using separate read and read/write address busses, an auxiliary register and shifting logic.

Other members of the μPB2900 series family are:

μPB2902 . . . . . 4-Bit Carry Look-Ahead
μPB2909 . . . . . 4-Bit Microprogram Sequencer
μPB2911 . . . . . 4-Bit Microprogram Sequencer
μPB2905 . . . . . OC Bus Transceiver with Tri-State Receiver
μPB2906 . . . . . OC Bus Transceiver with Parity
μPB2907 . . . . . OC Bus Transceiver with Parity and Tri-State Receiver
μPB2915 . . . . . Tri-State Bus Transceiver with Tri-State Receiver
μPB2916 . . . . . Tri-State Transceiver with Parity
μPB2917 . . . . . Tri-State Bus Receiver with Parity and Tri-State Receiver
μPB2918 . . . . . 4-Bit D-Register with Standard and Tri-State Output

FEATURES

- 4-Bit CPU Slice
- Standard 40 Pin Dual-In-Line Package
- Register-to-Register, Read/Modify/Write Time of 150 ns (Worst Case)
- 8 Function ALU
- 16 Working Registers
- Auxiliary Register
- Shifting Logic

NEC microcomputers, inc.

PRELIMINARY
μPDZ-80

SINGLE CHIP 8-BIT MICROPROCESSOR

DESCRIPTION

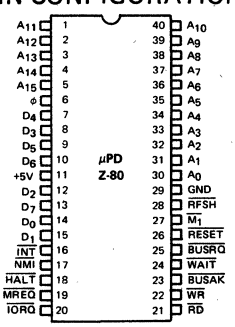
The NEC μPDZ-80 is a third generation, N-Channel microprocessor providing many advancements over second generation microprocessors. The μPDZ-80 processor offers a savings in systems throughput and reduced memory requirements through its expanded 158 software instruction set, while maintaining software compatibility with the 8080A. The expanded instruction set allows for a higher level of system operation by providing for memory-to-memory block transfers, bit manipulation and sampling in any register or memory location, enhanced 16-bit and BCD arithmetic, new I/O features such as I/O block transfers and expanded addressing modes (indexed and relative).

The μPDZ-80 provides all the control and refresh control signals for interfacing with most 4K static or dynamic memories. Only an external address decoder is needed for the static memories' chip selects. In addition, seventeen registers and 208 bits of programmer usable Read/Write memory on-chip all contribute to the power and versatility of this device.

FEATURES

- 158 Instructions (Including all 78 Instructions of the 8080A)
- 17 Internal Register
- Three Modes of Fast Interrupt Response and a Non-Maskable Interrupt
- Direct Interface with Standard Speed Dynamic or Static Memories
- 1.6 μs Instruction Execution Time
- Single +5V Supply
- Single-Phase TTL Clock
- TTL Compatible Tri-State Address and Data Busses

PIN CONFIGURATION



SALES REPRESENTATIVES

U.S. REPRESENTATIVES

Alabama
20th Century Marketing, Inc.
Huntsville AL 35806 205/772-9237

Arizona
Summit Sales
Scottsdale AZ 85251 602/994-4587

Arkansas
W. Pat Fralia Co.
Fort Worth TX 76116 817/640-9101
817/649-8981

California
CERCO
San Diego CA 92111 714/560-9143

Electronic Component Marketing
Fullerton CA 92613 714/879-9460

Trident Associates
Sunnyvale CA 94086 408/734-5900

Colorado
D/Z Associates, Inc.
Denver CO 80204 303/534-3649

Connecticut
Contact Sales, Inc.
Burlington MA 01803 617/273-1520

ROME
Melville NY 11746 516/249-0011

Trionic Associates, Inc.
Great Neck NY 11021 516/466-2300

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NEC microcomputers, inc.

THE μCOM-8 MICROCOMPUTER PROGRAM CARD

This program card provides a concise summary of the information necessary for programming and operating a μCOM-8 microcomputer system. The full set of 78 instructions is explained in terms of:

- Source/Destination Operations
- Assembly Language Mnemonics
- Effect on Status Flags
- Instruction Machine Codes
- Program Counter Control Instructions
- Increment/Decrement Instructions
- Shift Instructions
- Restart Instructions
- Special Instructions
- Assembly Language Format

The operator of a μCOM-8 can readily determine not only what the μCOM-8 does, but all possible sources and destinations of data, the assembly language mnemonics, the machine codes which implement the instructions, simply by noting the matrix intersection entries. For example, the intersection of source "[HL]" and destination "s → LReg" in the upper matrix incorporates the mnemonics MOV d,M. This means that the contents of the memory addressed by the HL register pair can be moved to the L Reg (the d in the mnemonic represents any of the possible destinations—in this case the L register). Similarly, the same intersection in the lower matrix contains the entry "6E," the machine code for implementing this instruction.

The only mnemonics and machine codes not actually in the matrices are those for Jump, Call, and Return. These entries are listed in separate tables to the right of the matrices.

Several abbreviations and symbols are used on this card as defined below.

s	=	source of data for instruction (vertical)
d	=	destination of data for instruction (horizontal)
B_2	=	second byte of instruction
B_3B_2	=	second and third bytes of instruction, B_2 is least significant byte
( )	=	contents of register, or register pair as designated by item(s) in parenthesis
[ ]	=	contents of memory as addressed by items in brackets
PSW	=	Program Status Word
SP	=	Stack Pointer
PC	=	Program Counter
Cy	=	Carry Flag
EXPX	=	Expression with value limited to the number of bits indicated by X
D8	=	8-bit data quantity, expression, or constant, always B_2 of instruction
D16	=	16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR	=	16-bit memory address

*μCOM is a trademark of NEC.

NUMERICAL LISTING OF μCOM-8 MACHINE CODES

00	NOP		30	···		60	MOV	H,B	90	SUB	B	C0	RNZ		F0	RP	
01	LXI	B,D16	31	LXI	SP,D16	61	MOV	H,C	91	SUB	C	C1	POP	B	F1	POP	PSW
02	STAX	B	32	STA	ADDR	62	MOV	H,D	92	SUB	D	C2	JNZ	ADDR	F2	JP	ADDR
03	INX	B	33	INX	SP	63	MOV	H,E	93	SUB	E	C3	JMP	ADDR	F3	DI	
04	INR	B	34	INR	M	64	MOV	H,H	94	SUB	H	C4	CNZ	ADDR	F4	CP	ADDR
05	DCR	B	35	DCR	M	65	MOV	H,L	95	SUB	L	C5	PUSH	B	F5	PUSH	PSW
06	MVI	B,D8	36	MVI	M,D8	66	MOV	H,M	96	SUB	M	C6	ADI	D8	F6	ORI	D8
07	RLC		37	STC		67	MOV	H,A	97	SUB	A	C7	RST	0	F7	RST	6
08	···		38	···		68	MOV	L,B	98	SBB	B	C8	RZ		F8	RM	
09	DAD	B	39	DAD	SP	69	MOV	L,C	99	SBB	C	C9	RET		F9	SPHL	
0A	LDAX	B	3A	LDA	ADDR	6A	MOV	L,D	9A	SBB	D	CA	JZ		FA	JM	ADDR
0B	DCX	B	3B	DCX	SP	6B	MOV	L,E	9B	SBB	E	CB	···		FB	EI	
0C	INR	C	3C	INR	A	6C	MOV	L,H	9C	SBB	H	CC	CZ	ADDR	FC	CM	ADDR
0D	DCR	C	3D	DCR	A	6D	MOV	L,L	9D	SBB	L	CD	CALL	ADDR	FD	···	
0E	MVI	C,D8	3E	MVI	A,D8	6E	MOV	L,M	9E	SBB	M	CE	ACI	D8	FE	CPI	D8
0F	RRC		3F	CMC		6F	MOV	L,A	9F	SBB	A	CF	RST	1	FF	RST	7
10	···		40	MOV	B,B	70	MOV	M,B	A0	ANA	B	D0	RNC				
11	LXI	D,D16	41	MOV	B,C	71	MOV	M,C	A1	ANA	C	D1	POP	D			
12	STAX	D	42	MOV	B,D	72	MOV	M,D	A2	ANA	D	D2	JNC	ADDR			
13	INX	D	43	MOV	B,E	73	MOV	M,E	A3	ANA	E	D3	OUT	D8			
14	INR	D	44	MOV	B,H	74	MOV	M,H	A4	ANA	H	D4	CNC	ADDR			
15	DCR	D	45	MOV	B,L	75	MOV	M,L	A5	ANA	L	D5	PUSH	D			
16	MVI	D,D8	46	MOV	B,M	76	HLT		A6	ANA	M	D6	SUI	D8			
17	RAL		47	MOV	B,A	77	MOV	M,A	A7	ANA	A	D7	RST	2			
18	···		48	MOV	C,B	78	MOV	A,B	A8	XRA	B	D8	RC				
19	DAD	D	49	MOV	C,C	79	MOV	A,C	A9	XRA	C	D9	···				
1A	LDAX	D	4A	MOV	C,D	7A	MOV	A,D	AA	XRA	D	DA	JC	ADDR			
1B	DCX	D	4B	MOV	C,E	7B	MOV	A,E	AB	XRA	E	DB	IN	D8			
1C	INR	E	4C	MOV	C,H	7C	MOV	A,H	AC	XRA	H	DC	CC	ADDR			
1D	DCR	E	4D	MOV	C,L	7D	MOV	A,L	AD	XRA	L	DD	···				
1E	MVI	E,D8	4E	MOV	C,M	7E	MOV	A,M	AE	XRA	M	DE	SBI	D8			
1F	RAR		4F	MOV	C,A	7F	MOV	A,A	AF	XRA	A	DF	RST	3			
20	···		50	MOV	D,B	80	ADD	B	B0	ORA	B	E0	RPO				
21	LXI	H,D16	51	MOV	D,C	81	ADD	C	B1	ORA	C	E1	POP	H			
22	SHLD	ADDR	52	MOV	D,D	82	ADD	D	B2	ORA	D	E2	JPO	ADDR			
23	INX	H	53	MOV	D,E	83	ADD	E	B3	ORA	E	E3	XTHL				
24	INR	H	54	MOV	D,H	84	ADD	H	B4	ORA	H	E4	CPO	ADDR			
25	DCR	H	55	MOV	D,L	85	ADD	L	B5	ORA	L	E5	PUSH	H			
26	MVI	H,D8	56	MOV	D,M	86	ADD	M	B6	ORA	M	E6	ANI	D8			
27	DAA		57	MOV	D,A	87	ADD	A	B7	ORA	A	E7	RST	4			
28	···		58	MOV	E,B	88	ADC	B	B8	CMP	B	E8	RPE				
29	DAD	H	59	MOV	E,C	89	ADC	C	B9	CMP	C	E9	PCHL				
2A	LHLD	ADDR	5A	MOV	E,D	8A	ADC	D	BA	CMP	D	EA	JPE	ADDR			
2B	DCX	H	5B	MOV	E,E	8B	ADC	E	BB	CMP	E	EB	XCHG				
2C	INR	L	5C	MOV	E,H	8C	ADC	H	BC	CMP	H	EC	CPE	ADDR			
2D	DCR	L	5D	MOV	E,L	8D	ADC	L	BD	CMP	L	ED	···				
2E	MVI	L,D8	5E	MOV	E,M	8E	ADC	M	BE	CMP	M	EE	XRI	D8			
2F	CMA		5F	MOV	E,A	8F	ADC	A	BF	CMP	A	EF	RST	5			

HEX-ASCII TABLE

	0	1	2	3	4	5	6	7
0	NULL	DL* ESCAPE	SP	0	@	P	‘	p
1	START HDG	DC† 1	!	1	A	Q	a	q
2	START TEXT	DC† 2	"	2	B	R	b	r
3	END TEXT	DC† 3	#	3	C	S	c	s
4	END TRANS	DC† 4 (STOP)	$	4	D	T	d	t
5	ENQUIRY	NEG ACK	%	5	E	U	e	u
6	ACK	SYNC IDLE	&	6	F	V	f	v
7	BELL	END TRANS BLK	’	7	G	W	g	w
8	BACKSPACE	CANCEL	(	8	H	X	h	x
9	HORIZ TAB	END MEDIUM	)	9	I	Y	i	y
A	LINE FEED	SUBSTITUTE	*	:	J	Z	j	z
B	VERT TAB	ESCAPE	+	;	K	[	k	{
C	FORM FEED	FILE SEP	,	<	L	\	l	¦
D	RETURN	GROUP SEP	-	=	M	]	m	}
E	SHIFT OUT	RECORD SEP	.	>	N	^	n	~
F	SHIFT IN	UNIT SEP	/	?	O	—	o	DELETE

*DATA LINK, †DEVICE CONTROL

To form a code for any character on the chart, first locate the character. The most significant hex digit of the code is the column number at the top, and the least significant digit is the row number at the left.

Example:
The code for A = 41
* = 2A

NEC μcom-8 mnemonics & machine codes

CARRY FLAG	BIT 0							•	•	•	•	0	0	0	•							•					•		•	•	1	C̄	•
PARITY FLAG	BIT 2							•	•	•	•	•	•	•	•							•					•						•
ZERO FLAG	BIT 6							•	•	•	•	•	•	•	•							•					•						•
SIGN FLAG	BIT 7							•	•	•	•	•	•	•	•							•					•						•

Effect of Operations on Status Flags:
• = Affected,
(blank) = Not Affected,
0 = Cleared.

DESTINATIONS OF DATA FOR INSTRUCTIONS

Bold Face Letters are Actual Mnemonics Used for Instruction

	A	B	C	D	E	H	L	M	A	B	C	D	E	H	L	M	A	B	C	D	E	H	L	M	A	B	C	D	E	H	L	M
	s→A Reg	s→B Reg	s→C Reg	s→D Reg	s→E Reg	s→H Reg	s→L Reg	s→[HL]	s+(A)→A	s+(A)+CY→A	s−(A)→A	s−(A)−CY→A	s∧(A)→A	s∀(A)→A	s∨(A)→A	s−(A)→FLAG	s→[BC]	s→[DE]	s→OB$_2$	s→[B$_3$B$_2$]	s→PC	PC→STACK, s→PC	s→PUSH STACK	s→AF	s→BC	s→DE	s→HL	s→SP	s→[HL]→HL			
	ADI	ACI	SUI	SBI	ANI	XRI	ORI	CPI																								
B$_2$	MVI d, B$_2$																		OUT B$_2$													
A (A Reg)	MOV d,s							MOV M,s	ADD s	ADC s	SUB s	SBB s	ANA s	XRA s	ORA s	CMP s			STA B$_3$B$_2$													
B (B Reg)																			STAX d													
C (C Reg)																																
D (D Reg)																																
E (E Reg)																																
H (H Reg)																																
L (L Reg)																																
M [HL]	MOV d,M																															
B [BC]	LDAX s																															
D [DE]																																
IB$_2$	IN B$_2$																															
[B$_3$B$_2$]	LDA B$_3$B$_2$																															
B$_3$B$_2$																																
POP STACK																																
PSW (AF Reg)																																
B (BC Reg)																																
D (DE Reg)																																
H (HL Reg)																																
SP (SP)																																

1-BYTE OPERATIONS
2-BYTE OPERATIONS

LHLD B$_3$B$_2$
LXI d,B$_3$B$_2$
POP d
XCHG
SHLD B$_3$B$_2$
PUSH s
DAD s
PCHL
SPHL

	B$_2$	3E	06	0E	16	1E	26	2E	36	C6	CE	D6	DE	E6	EE	F6	FE															
A	(A Reg)	7F	47	4F	57	5F	67	6F	77	87	8F	97	9F	A7	AF	B7	BF	02	12	D3	32											
B	(B Reg)	78	40	48	50	58	60	68	70	80	88	90	98	A0	A8	B0	B8															
C	(C Reg)	79	41	49	51	59	61	69	71	81	89	91	99	A1	A9	B1	B9															
D	(D Reg)	7A	42	4A	52	5A	62	6A	72	82	8A	92	9A	A2	AA	B2	BA															
E	(E Reg)	7B	43	4B	53	5B	63	6B	73	83	8B	93	98	A3	AB	B3	BB															
H	(H Reg)	7C	44	4C	54	5C	64	6C	74	84	8C	94	9C	A4	AC	B4	BC															
L	(L Reg)	7D	45	4D	55	5D	65	6D	75	85	8D	95	9D	A5	AD	B5	BD															
M	[HL]	7E	46	4E	56	5E	66	6E		86	8E	96	9E	A6	AE	B6	BE															
B	[BC]	0A																														
D	[DE]	1A																														
IB$_2$		DB																														
[B$_3$B$_2$]		3A																														
B$_3$B$_2$																																
POP STACK																																
PSW	(AF Reg)																															
B	(BC Reg)																															
D	(DE Reg)																															
H	(HL Reg)																															
SP	(SP)																															

1-BYTE OPERATIONS
2-BYTE OPERATIONS

2A																																
01	11	21	31																													
F1	C1	D1	E1																													
F5																																
C5																																09
D5																																19
E5																																29
22	E9																															39

ASSEMBLY LANGUAGE FORMAT
PSEUDO INSTRUCTIONS

SYMBOL	MNEMONIC	EXP	COMMENTS
Optional	ORG	EXP 16	Sets Location Counter to value of EXP 16
Optional	DS	EXP 16	Adds value of EXP 16 to Location Counter
Required	EQU	EXP 16	Permanently assigns value of EXP 16 to "SYMBOL" specified by user
Required	SET	EXP 16	Temporarily assigns value of EXP 16 to "SYMBOL" specified by user
Optional	DB	EXP 8, EXP 8, . . .	Assigns single-byte value of expression(s) to consecutive memory locations
Optional	DW	EXP 16, EXP 16, . . .	Assigns double-byte value of expression(s) to consecutive memory locations
Optional	IF	EXP 16	Assembles statements between IF and ENDIF when value of EXP 16 ≠ 0
Optional	ENDIF	——	Terminates conditional IF assembly
Required	MACRO	P1, P2	Assigns statement between MACRO and ENDM to "SYMBOL" specified
Optional	ENDM	——	Terminates MACRO assignments
Optional	END	——	Indicates end of source program

INC (INR) OR DEC (DCR) REGISTER OR MEMORY
INC (INX) OR DEC (DCX) REGISTER PAIR
ROTATE ACCUMULATOR LEFT (RLC) OR RIGHT (RRC)
ROTATE ACC AND CY LEFT (RAL) OR RIGHT (RAR)
SET CARRY (STC)
COMPLEMENT CARRY (CMC)
DECIMAL ADJUST ACCUMULATOR (DAA)

NOTE

Both Function and Assembly Language Mnemonics Shown for Instructions. B$_2$ = Second Byte of Instruction, B$_3$ = Third Byte of Instruction, [XX] = Content of Memory as Addressed by XX, M = [HL], R = Register, RP = Register Pair, ∧ = Logic AND, V = Logic OR, ∀ = Exclusive OR.

OTHER MNEMONICS

NOP = NO OPERATION
EI = ENABLE INTERRUPT
DI = DISABLE INTERRUPT
HLT = HALT
XTHL = EXCHANGE (TOP OF STACK) WITH (HL)
RST X = RESTART, X = 0 – 7
CMA = COMPLEMENT ACCUMULATOR

PC REGISTER CONTROL MNEMONICS

1	= UNCONDITIONAL JUMP (JMP)
2	= UNCONDITIONAL CALL (CALL)
3	= UNCONDITIONAL RETURN (RET)
1 2 3	= CONDITIONAL JMP (JXX), CALL (CXX), RET (RXX)

for	CARRY BIT		PARITY BIT		ZERO BIT		SIGN BIT	
of	1	0	1	0	1	0	1	0
XX	C	NC	PE	PO	Z	NZ	M	P

PCHL = (HL) → PC REGISTER

SPECIAL INSTRUCTIONS

NOP	00	HLT	76	STC	37
EI	FB	DAA	27	CMC	3F
DI	F3	CMA	2F	XTHL	E3

PROGRAM COUNTER CONTROL INSTRUCTIONS

JMP	C3	CALL	CD	RET	C9	RST 0	C7
JNZ	C2	CNZ	C4	RNZ	C0	RST 1	CF
JZ	CA	CZ	CC	RZ	C8	RST 2	D7
JNC	D2	CNC	D4	RNC	D0	RST 3	DF
JC	DA	CC	DC	RC	D8	RST 4	E7
JPO	E2	CPO	E4	RPO	E0	RST 5	EF
JPE	EA	CPE	EC	RPE	E8	RST 6	F7
JP	F2	CP	F4	RP	F0	RST 7	FF
JM	FA	CM	FC	RM	F8	PCHL	E9

INCREMENT/DECREMENT & SHIFT INSTRUCTIONS

INR A	3C	DCR A	3D	INX B	03	RLC	07
INR B	04	DCR B	05	INX D	13	RRC	0F
INR C	0C	DCR C	0D	INX H	23	RAL	17
INR D	14	DCR D	15	INX SP	33	RAR	1F
INR E	1C	DCR E	1D	DCX B	0B		
INR H	24	DCR H	25	DCX D	1B		
INR L	2C	DCR L	2D	DCX H	2B		
INR M	34	DCR M	35	DCX SP	3B		

CONSTANTS		STANDARD SETS		OPERATORS
0BDH, 1AH	Hex	A SET 7		(,)
105D, 105	Decimal	B SET 0		*, /, MOD, SHL, SHR
720, 72Q	Octal	C SET 1		+, –
11011B, 00110B	Binary	D SET 2		NOT
'TEST', 'A', 'B'	ASCII	E SET 3		AND
		H SET 4		OR, XOR
		L SET 5		
		M SET 6		
		SP SET 6		
		PSW SET 6		

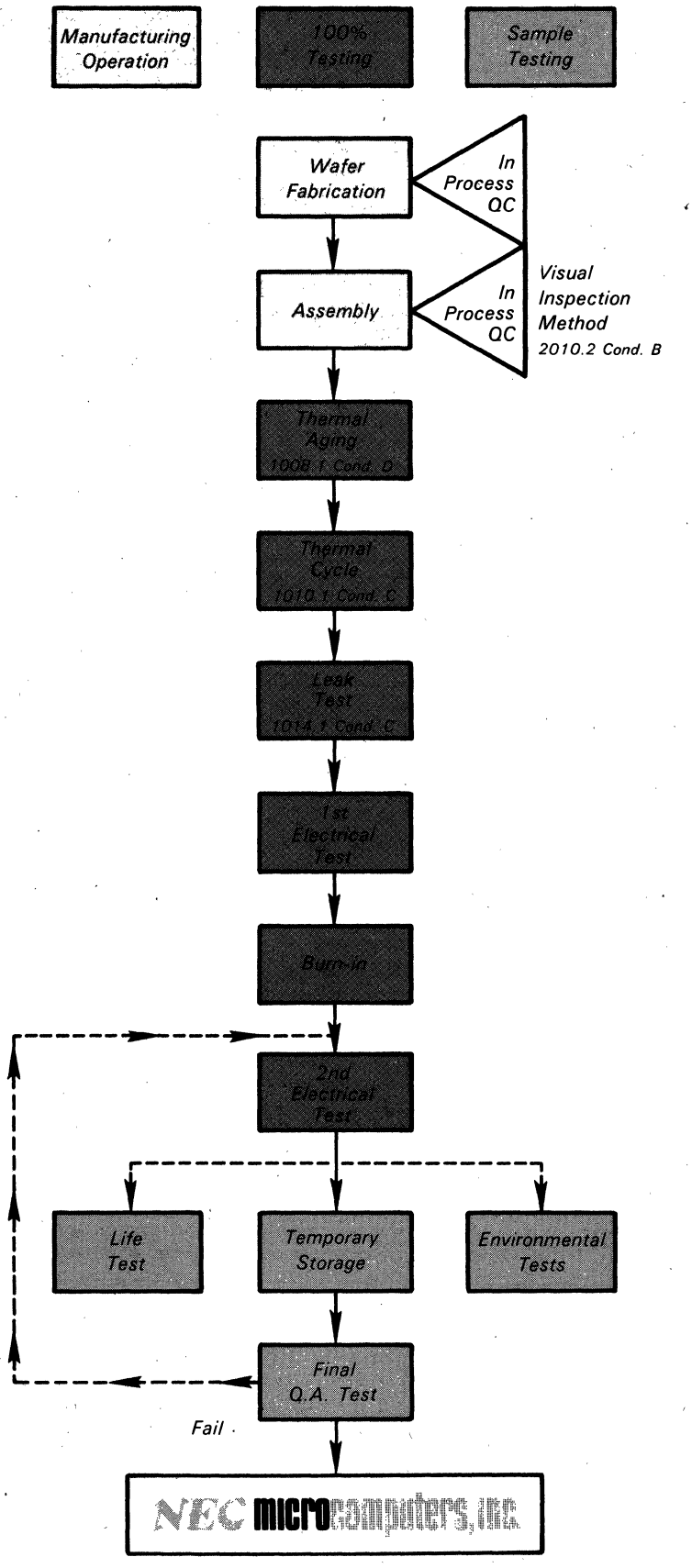
NEC Quality Assurance Procedures

One of the important factors contributing to the final quality of our memory and microcomputer components is the attention given to the parts during the manufacturing process. All Production Operations in NEC follow the procedures of MIL Standard 883A. Of particular importance to the reliability program are three areas that demonstrate NEC's commitment to the production of components of the highest quality.

I. Burn-In — All memory and microcomputer products are dynamically burned in at an ambient temperature sufficient to bring the junction to a temperature of 150 °C. The duration of the burn-in is periodically adjusted to reflect the production history and experience of NEC with each product. 100% of all NEC memory and microcomputer products receive an operational burn-in stress.

II. Electrical Test — Memory and microcomputer testing at NEC is not considered a statistical game where the device is subjected to a series of pseudo random address and data patterns. Not only is this unnecessarily time consuming, but it does not effectively eliminate weak or defective parts. NEC's test procedures are based on the internal physical and electrical organization of each device and are designed to provide the maximum electrical margin for solid board operation. For further information on NEC's testing procedures see your local NEC representative.

III. After completion of all 100% test operations, production lots are held in storage until completion of two groups of extended sample testing: an operating life test and a series of environmental tests. Upon successful completion of these tests, the parts are released from storage and sent to final Q.A. testing.



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